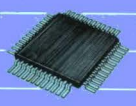
SANYO

'85 SEMICONDUCTOR HANDBOOK

MICROCOMPUTERS & MOS INTEGRATED CIRCUITS



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1985 SEMICONDUCTOR HANDBOOK

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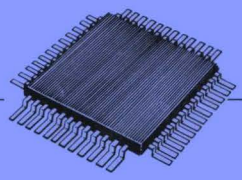
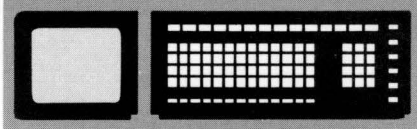


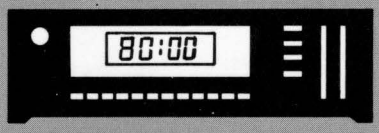
MOS IC, LSI

LC, LM type

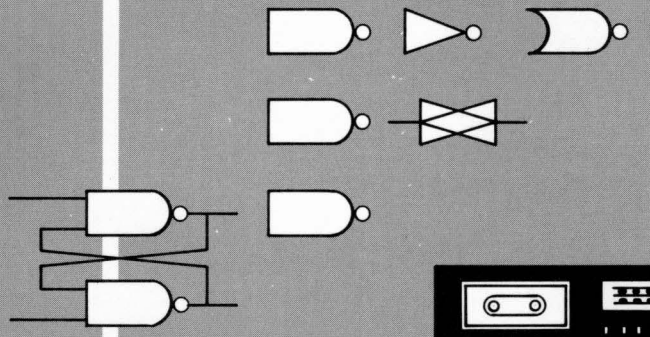


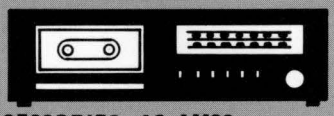
4 BIT MICROCOMPUTERS

ELECTRONIC TUNING SYSTEM FREQ-VOLT SYNTHESIZER SYSTEMS

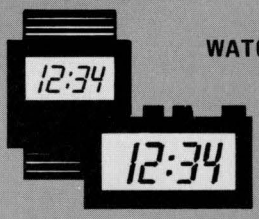


STANDARD LOGICS



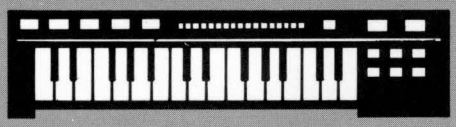


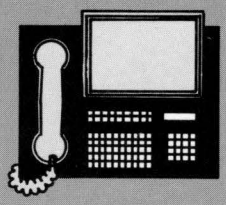
AUDIO ACCESSORIES, AS AMSS



WATCHES/CLOCKS

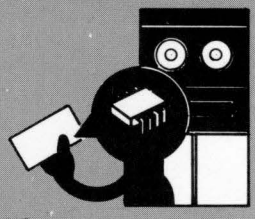
MUSICAL INSTRUMENTS





TELEPHONE APPLICATIONS

MEMORIES



SPEECH SYNTHESIS APPLICATIONS

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TOKYO SANYO ELECTRIC CO.,LTD.
SEMICONDUCTOR DIVISION

PRODUCT INDEX

Table of Contents

1. FUNCTIONAL INDEX TO MICRO-COMPUTERS/MOS INTEGRATED CIRCUITS

This CHAPTER gives a summary of all micro-computers/MOS integrated circuits available from Tokyo Sanyo Semiconductor Division as standard products.

PRODUCT SELECTION GUIDE BY USE

Note * : Under development, DIP: Dual-in-line package, SEP: Single-end package, QIP: Quad-in-line package, MFP: Miniflat package

MICROCOMPUTERS (Included among the following are microcomputers with an on-chip LCD driver.)

• 4 BITS, SINGLE CHIP (N-MOS INTEGRATED CIRCUIT)

Type Number	Page	Case			Applications	ROM (Bytes)	RAM (Bits)	Stacks	Cycle Time (μs)	I_{DD} (mA)	Port		Remarks
		Package	Pins	Package No.							Max. Voltage (V)	Max. Current (mA)	
LM6402A	54	DIP	42	3014A	Basic Type	2K	128X4	4	10	30	15	40	Evaluation chip LM64PG99
LM6405A	54	DIP	42-S	3025B	Basic Type	1K	64X4	4	10	30	15	40	Evaluation chip LM64PG99
LM6402H	62	DIP	42	3014A	Medium-Speed Type	2K	128X4	4	5	35	15	40	Evaluation chip LM64PG99
LM6405H	62	DIP	42-S	3025B	Medium-Speed Type	1K	64X4	4	5	35	15	40	Evaluation chip LM64PG99
LM6402G	70	DIP	42	3014A	High-Speed Type	2K	128X4	4	3	35	15	50	Evaluation chip LM64PG99
LM6405G	70	DIP	42-S	3025B	High-Speed Type	1K	64X4	4	3	35	15	50	Evaluation chip LM64PG99
LM6402L	87	DIP	42	3014A	Low-Power Type	2K	128X4	4	20	10	12	40	Evaluation chip LM64PG99
LM6405L	87	DIP	42-S	3025B	Low-Power Type	1K	64X4	4	20	10	12	40	Evaluation chip LM64PG99
LM6413E	95	DIP	28-S	3029A	Economy Type	2K	128X4	2	4	17	15	20	Evaluation chip LM64PG98
LM6416E	103	DIP	28-S	3029A	Economy Type	1K	64X4	2	4	17	15	20	Evaluation chip LM64PG97
LM6417E	114	DIP	22	3010A	Economy Type	1K	64X4	2	4	17	15	20	Evaluation chip LM64PG97

• 4 BITS, SINGLE CHIP (C-MOS INTEGRATED CIRCUIT)

LC6502C	145	DIP	42	3014A	Basic Type	2K	128X4	4	10	0.5	5	2	Evaluation chip LC65PG99
LC6505C	145	DIP QIP	42-S 64	3025B 3026B	Basic Type	1K	64X4	4	10	0.5	5	2	Evaluation chip LC65PG99
LC6502B	131	DIP	42	3014A	High-Voltage Type	2K	128X4	4	10	0.5	High voltage	10	FLT direct drivable, evaluation chip LC65PG99
LC6505B	131	DIP QIP	42-S 64	3025B 3026B	High-Voltage Type	1K	64X4	4	10	0.5	High voltage	10	FLT direct drivable, evaluation chip LC65PG99
LC6502D	157	DIP DIP	42-S	3025B 3014A	High-Voltage Type	2K	128X4	4	10	0.5	High voltage	10	FLT Direct drivable, low-input threshold
LC6505D	157	QIP	42-S	3026B	High-Voltage Type	1K	64X4	4	10	0.5	High voltage	10	FLT direct drivable, low-input threshold
LC6510C	158	DIP	42-S	3025B	High-Performance Type	4K	256X4	8	5	1.0	5	2	
***LC6523**	159	DIP	30-S	3047A	Economy Type	2K	128X4	4	3	1.5	15	20	With serial port
***LC6526**	159	DIP	30-S	3047A	Economy Type	1K	64X4	4	3	1.5	15	20	With serial port
***LC6527**	159	DIP	18	3007A	Economy Type	1K	64X4	4	3	1.5	15	20	
LC5700N	168	QIP	64	3026B	Low-Voltage Type	1.39KX14	84X4	8	420	3μA	–	–	LCD direct drivable (98 segments), also available in chip form
***LC5732**	181	Chip (QIP 64)		3026B	On-chip LCD driver, Low-voltage operation, Very low current	2KX8 Bits	48X4	1	122	3μA	–	–	LCD direct drivable (81 segments)
LC5800	185	QIP	80	3044B		2KX16	152X4	8	244,122	3μA	–	–	LCD direct drivable (126 segments), also available in chip form
***LC5812**	217	Chip (QIP 80)		3044B		2KX16 Bits	152X4	8	40	10μA	–	–	LCD direct drivable (126 segments)
LC5850	219	QIP	64	3026B		1KX15	64X4	4	244,122	3μA	–	–	LCD direct drivable (75 segments), also available in chip form
***LC5851**	239	QIP	64	3026B		1KX15 Bits	64X4	4	40	3μA	–	–	Pseudo serial output, LCD direct drivable (75 segments)

Continued on next page.

Continued from preceding page.

• 8 BITS, SINGLE CHIP (N-MOS INTEGRATED CIRCUIT)

Type Number	Page	Case			Applications	ROM (Bytes)	RAM (Bits)	Stacks	Cycle Time (μs)	I_{DD} (mA)	Port		Remarks
		Package	Pins	Package No.							Max. Voltage (V)	Max. Current (mA)	
***LM8802**	243	DIP	42-S	3025B	–	2K	128X8	16	1	60	15	20	Evaluation chip LM88PG99
***LM8804**	243	DIP	42-S	3025B	–	4K	256X8	16	1	60	15	20	Evaluation chip LM88PG99
***LM8852**	243	DIP	64-S	–	–	2K	128X8	16	1	60	15	20	Evaluation chip LM88PG99
***LM8854**	243	DIP	64-S	–	–	4K	256X8	16	1	60	15	20	Evaluation chip LM88PG99

• MICROCOMPUTER PERIPHERALS/SPEECH SYSTHESIS APPLICATIONS/MEMORIES

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
LC3100	247	DIP	24	3011A	128K Mask ROM	ROM dedicated to speech synthesis (See description of speech synthesis LSI.)
LC3101	260	DIP DIP	42 42-S	3014A 3025B	ROM dedicated to Speech Synthesis	ROM dedicated to speech synthesis (See description of speech synthesis LSI.)
LC3514	273	DIP	18	3007A	4K Static RAM	High speed (address access time=200ns)
LC3514D	277	DIP	18	3007A	4K Static RAM	Wide operating voltage range (V_{CC}=3.0 to 6.0V), low standby current (I_{CCS}=1μA at T_a=45°C)
LC3514E	277	DIP	18	3007A	4K Static RAM	Wide operating voltage range (V_{CC}=3.6 to 6.0V)
LC3514L	273	DIP	18	3007A	4K Static RAM	High speed (address access time=200ns), low standby current (I_{CCS}=1μA at T_a=60°C)
***LC3516**	281	DIP	24	3011A	C-MOS 16K Static RAM (2K X 8 bits)	High speed, low standby current, pin compatible with 2716 (EPROM)
***LC3517**	282	DIP	24	3011A	C-MOS 16K Static RAM (2K X 8 bits)	High speed, low standby current, pin compatible with 2716 (EPROM)
LC7800	283	DIP	28-S	3029A	Input Expander of Microcomputer	Peripheral of microcomputer (LM6400 series), (1 to 4) X 4 circuits
LC7800N	283	DIP	28	3012A	Input Expander of Microcomputer	Peripheral of microcomputer (LM6400 series), (1 to 4) X 4 circuits
LC7900	289	SEP	8	3016B	System Clock Generator	4MHz Xtal OSC, frequency divider (800kHz, 400kHz, 62.5kHz, 31.25Hz output)
LC7960	291	DIP	16	3006A	3-Digit BCD Counter, Decoder, Driver	Suited for use in systems counting and indicating number of pulses generated during a certain period of time
LC7961	295	DIP	20	3008A	4-Digit BCD Counter	4-digit LED direct drive, dynamic display, max. count display 9999, cascade connection available
LC8100	300	DIP	28	3012A	PARCOR System-Applied 1-Chip Speech Synthesizer	Male & female voices, speech duration of approx. 20 sec, automatic power-on/down function
LM3700	320	DIP	28	3012A	40K Mask ROM (4K X 10 bits)	Direct connectable to 16-bit CPU (CP1610)
LM3710	324	DIP	28	3012A	80K Mask ROM (8K X 10 bits)	Direct connectable to 16-bit CPU (CP1610)
***LM3764**	328	DIP	28	3012A	64K Mask ROM (8K X 8 bits)	Pin compatible with 2764 (EPROM)
LM8942	329	DIP	16	3006A	Hex Inverter Buffer	6-MOS transistor array suited for designing various kinds of interface

C MOS STANDARD LOGICS

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
LC4001B	333	DIP	14	3003A	Quad 2 input NOR Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4001BM	336	MFP	14	3034A	Quad 2 input NOR Gate	Standard logic SSI (4000B series), miniflat package version of LC4001B
LC4011B	337	DIP	14	3003A	Quad 2 input NAND Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4011BM	340	MFP	14	3034A	Quad 2 input NAND Gate	Standard logic SSI (4000B series), miniflat package version of LC4011B
LC4012B	341	DIP	14	3003A	Dual 4 input NAND Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4013B	344	DIP	14	3003A	Dual D-FF	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4013BM	348	MFP	14	3034A	Dual D type Flip Flop	Standard logic SSI (4000B series), miniflat package version of LC4013B
LC4015B	349	DIP	16	3006A	Dual 4-Stage Static Shift Register	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4016B	353	DIP	14	3003A	Quad Bilateral Switch	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4016BM	357	MFP	14	3034A	Quad Bilateral Switch	Standard logic SSI (4000B series), miniflat package version of LC4016B
LC4019B	358	DIP	16	3006A	Quad AND-OR Select Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4020B	362	DIP	16	3006A	14-Stage Binary Counter	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4023B	366	DIP	14	3003A	Tripple 3 input NAND Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4025B	369	DIP	14	3003A	Tripple 3 input NOR Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4027B	372	DIP	16	3006A	Dual J-K Master Slave Flip Flop	Standard logic SSI (4000B series), directly interchangeable with 4000B series of ohter suppliers
LC4028B	376	DIP	16	3006A	BCD to Decimal Decoder	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4040B	380	DIP	16	3006A	12-Stage Binary Counter	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4049B	384	DIP	16	3006A	Hex Buffer/Converter Inverting Type	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4050B	387	DIP	16	3006A	Hex Buffer/Converter non-inverting Type	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4050BM	390	MFP	16	3035A	Hex Buffer/Converter non-inverting Type	Standard logic SSI (4000B series), miniflat package version of LC4050B
LC4066B	391	DIP	14	3003A	Quad Bilateral Switch	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4066BH	398	DIP	14	3003A	Quad Bilateral Switch	Standard logic SSI (4000B series), V_{DD}max=25V, pin compatible with LC4066B
LC4066BM	396	MFP	14	3034A	Quad Bilateral Switch	Standard logic SSI (4000B series), miniflat package version of LC4066B
LC4066BS	397	SEP	15	3053	Quad Bilateral Switch	Standard logic SSI (4000B series), SEP package version of LC4066B
LC4069UB	403	DIP	14	3003A	Hex Inverter	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4069UBM	407	MFP	14	3034A	Hex Inverter	Standard logic SSI (4000B series), miniflat package version of LC4069UB
LC4070B	408	DIP	14	3003A	Quad 2 input Exclusive OR Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4071B	412	DIP	14	3003A	Quad 2 input OR Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4073B	415	DIP	14	3003A	Tripple 3 input AND Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4075B	418	DIP	14	3003A	Tripple 3 input OR Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4077B	421	DIP	14	3003A	Quad 2 input Exclusive NOR Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4081B	425	DIP	14	3003A	Quad 2 input AND Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4081BM	428	MFP	14	3034A	Quad 2 input AND Gate	Standard logic SSI (4000B series), miniflat package version of LC4081B
LC4082B	429	DIP	14	3003A	Dual 4 input AND Gate	Standard logic SSI (4000B series), directly interchangeable with 4000B series of ohter suppliers

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C MOS STANDARD LOGICS

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
LC4093B	433	DIP	14	3003A	Quad 2 input NAND Schmitt Trigger	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4512B	437	DIP	16	3006A	8 Channel Data Selector/Multiplexer	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4520B	442	DIP	16	3006A	Dual 4-Bit Binary Converter	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4528B	446	DIP	16	3006A	Dual Mono-Multi	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
LC4584B	451	DIP	14	3003A	Hex Schmitt Trigger	Standard logic SSI (4000B series), directly interchangeable with 4000B series of other suppliers
***LC4913**	455	DIP	14	3003A	Dual DFF with Schmitt Trigger	Standard logic SSI (4000B series), pin compatible with LC4013B
LC4966	456	DIP	14	3003A	Quad Bilateral Switch	V_{DD}max=40V, pin compatible with LC4066B
LC4969	461	DIP	8	3001A	Triple Inverter	1/2 of LC4069UB
***LC74HC00**	465	DIP	14	3003A	Quad 2 input NAND Gate	Standard logic SSI (74HC series), directly interchangeable with 74HC series of other suppliers
***LC74HC02**	466	DIP	14	3003A	Quad 2 input NOR Gate	Standard logic SSI (74HC series), directly interchangeable with 74HC series of other suppliers
***LC74HCU04**	467	DIP	14	3003A	Hex Inverter (Unbuffered)	Standard logic SSI (74HC series), directly interchangeable with 74HC series of other suppliers
***LC74HC08**	468	DIP	14	3003A	Quad 2 input AND Gate	Standard logic SSI (74HC series), directly interchangeable with 74HC series of other suppliers
***LC74HC74**	469	DIP	14	3003A	Dual D Flip-Flop with Set and Reset	Standard logic SSI (74HC series), directly interchangeable with 74HC series of other suppliers

TIMEPIECE APPLICATIONS

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
LC5613	473	—	—	—	LSI for Watch (with stopwatch), Static display	6-digit display, perpetual calendar, 3-function switch, stopwatch 1/100 sec.
LC5621	479	—	—	—	LSI for Ladies' Watch, Static display	Day-of-week flag, 4-digit display, perpetual calendar, 2-function switch, on-chip doubler
LC5633	484	—	—	—	Alarm Watch with Year Display Function, Static Display	Ag battery-powered, 6 digits (day-of-week flag), year display, alarm, perpetual calendar
LC5641	491	—	—	—	Duplex Display Watch (with alarm)	4/6-digit display (day-of-week flag), 12/24-hour mode, Ag battery-powered, alarm
LC5643	500	—	—	—	Duplex Display Watch	4/6-digit display (day-of-week flag), 12/24-hour mode, Ag battery-powered
LC5645N	508	—	—	—	Duplex Display Watch	3.5-digit display (hours-minutes/month-date/seconds), hours-minutes/month-date alternating mode, Ag battery-powered
LC7600	517	QIP	64	3026B	LCD Digital Watch	4-digit LCD static drive, alarm with snooze, up/down counter for sleep timer, tape counter, second watch
LC7650	531	DIP	8	3001A	Analog Clock (4MHz)	V_{DD}=1.5V, f_{OSC}=4.194304MHz, alarm, output pulse 46.875ms
LC7651	531	DIP	8	3001A	Analog Clock (4MHz)	V_{DD}=1.5V, f_{OSC}=4.194304MHz, alarm, output pulse 31.25ms
LC7652	533	DIP	8	3001A	Analog Clock (4MHz)	V_{DD}=1.5V, f_{OSC}=4.194304MHz, alarm with snooze, output pulse 46.875ms
LC7653	533	DIP	8	3001A	Analog Clock (4MHz)	V_{DD}=1.5V, f_{OSC}=4.194304MHz, alarm with snooze, output pulse 31.25ms
LC7660	536	DIP	8	3001A	Analog Clock (32.768kHz)	V_{DD}=1.5V, f_{OSC}=32.768kHz, 4-step alarm with snooze
LC7662	539	DIP	8	3001A	Analog Clock (32.768kHz)	V_{DD}=1.5V, f_{OSC}=32.768kHz, 3-step alarm with snooze
LC7665	542	DIP	8	3001A	Analog Clock (32.768kHz)	V_{DD}=1.5V, f_{OSC}=32.768kHz, alarm with snooze

LC7667	545	DIP	8	3001A	Analog Clock (32.768kHz)	V_{DD}=1.5V, f_{OSC}=32.768kHz, alarm with snooze
LM8361	548	DIP	40	3013A	Digital Clock	4-digit LED/FLT direct drivable, 12/24-hour mode, alarm with snooze, sleep timer, all digits flashing at power failure
LM8362	555	DIP	40	3013A	Digital Clock	Equivalent to LM8360 (except 10's hour digit 0 blanking, sleep timer fast advance)
LM8363	563	DIP	42	3014A	2-Alarm Digital Clock	4-digit LED/FLT direct drivable, 2 alarms with snooze, calendar, on-chip backup function
LM8364	573	DIP	42	3014A	2-Output 2-Alarm Digital Clock	4-digit LED/FLT direct drivable, 2 outputs for 2 alarms (with snooze), calendar, on-chip backup function
LM8365	584	DIP	42	3014A	2-Output 2-Alarm Digital Clock	Equivalent to LM8364 (except mirror image pin assignment)
LM8368	595	DIP	40	3013A	Digital Clock	Equivalent to LM8362 (except mirror image pin assignment)
LM8460	603	DIP	42-S	3025B	Up/Down Settable Digital Clock	4-digit red LED/FLT direct drivable, easy setting (up/down settable, one-touch control), 6-step alarm, 5-step dimmer control
LM8560	618	DIP	28-S	3029A	Duplex Digital Clock	4-digit LED display, duplex display, alarm, sleep timer, directly interchangeable with TMS3450

AUDIO APPLICATIONS(ACCESSORIES FOR AUDIO EQUIPMENT/LEVEL METERS/FREQUENCY INDICATORS/ELECTRONIC TUNING SYSTEMS/CB TRANSCEIVERS)

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
LC7000	629	DIP	20	3008A	Multiband SL2 Electronic Tuning System	Multiband tuning available in conjunction with control LSI (LC7200 series)
LC7010	636	DIP	42	3025B	Controller for LM7000-applied car stereo	(Designed for use in U.S., Europe), 6 channels each of FM/(MW+LW), clock, LED dynamic display
LC7120	647	DIP	20	3008A	27MHz CB Transceiver PLL Freq. Synthesizer	1-chip 1-crystal type, BCD input, active filter, 40-channel use only (designed for use in U.S.)
LC7131	650	DIP	20	3008A	27MHz CB Transceiver PLL Freq. Synthesizer	1-chip 1-crystal direct frequency divider, 40-channel use only (designed for use in U.S.)
LC7132	656	DIP	20	3021B	27MHz CB Transceiver PLL Freq. Synthesizer	1-chip 1-crystal direct frequency divider, 7-segment code program, 40-channel use (designed for use in U.S.)
LC7135	650	DIP	20	3008A	27MHz CB Transceiver PLL Freq. Synthesizer	1-chip 1-crystal direct frequency divider, 22-channel use only (designed for use in West Germany, Holland)
LC7136	650	DIP	20	3008A	27MHz CB Transceiver PLL Freq. Synthesizer	1-chip 1-crystal direct frequency divider, 40-channel use (designed for use in U.K.)
LC7137	650	DIP	20	3021B	27MHz CB Transceiver PLL Freq. Synthesizer	1-chip 1-crystal direct frequency divider, 40-channel use only (designed for use in U.K.)
LC7181	660	DIP	20	3008A	CB Transceiver Channel Selector System (Controller)	Up/down counter and channel output, BCD output, 40-channel use (designed for use in U.S.)
LC7184	667	DIP	20	3008A	CB Transceiver Channel Selector System	12-channel CB transceiver channel scan system available in conjunction with LC7191 (designed for use in West Germany)
LC7191	660	DIP	20	3008A	CB Transceiver Channel Selector System (Display use)	Decoder and LED driver for channel display of LC7181, LC7184
LC7200	670	DIP	42	3014A	Electronic Tuning (SL2 System) Controller	Manual, up/down, search, preset tuning, 5 channels each of FM, MW presettable
LC7201	670	DIP	42	3014A	Electronic Tuning (SL2 System) Controller	Manual, up/down, search, preset tuning, 6 channels each of FM, AM presettable
LC7203	670	DIP	42	3014A	Electronic Tuning (SL2 System) Controller	Manual, up/down, search, preset tuning, 6 channels each of FM, AM presettable

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AUDIO APPLICATIONS(ACCESSORIES FOR AUDIO EQUIPMENT/LEVEL METERS/FREQUENCY INDICATORS/ ELECTRONIC TUNING SYSTEMS/CB TRANSCEIVERS)

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
LC7207	670	DIP	42	3014A	Electronic Tuning (SL2 System) Controller	Manual, up/down, search, preset tuning, 7 channels each of FM, AM presettable
LC7210	691	DIP	28	3012A	PSL2 Electronic Tuning System	PSL2 system tuning use (kit available with control microcomputer, preset memory, nonvolatile memory)
LC7220	699	DIP	42	3025B	PLL Electronic Tuning System for FM/AM Radio	(Designed for use in U.S.), FM/MW, 18-dot analog display, V_{DD}=5V, f_{ref}=7.2MHz, used with LB3500 (1/8 prescaler)
LC7221	699	DIP	42	3025B	PLL Electronic Tuning System for FM/AM Radio	(Designed for use in Japan), FM/MW, 18-dot analog display, V_{DD}=5V, f_{ref}=7.2MHz, used with LB3500 (1/8 prescaler)
LC7222	699	DIP	42	3025B	PLL Electronic Tuning System for FM/AM Radio	(Designed for use in Europe), FM/MW, 18-dot analog display, V_{DD}=5V, f_{ref}=7.2MHz, used with LB3500 (1/8 prescaler)
LC7223	713	DIP	42	3025B	PLL Electronic Tuning System	(Designed for use in Japan), same as LC7221, AM1629kHz receivable
LC7225	699	QIP	64	3026B	PLL Electronic Tuning System for FM/AM Radio	(Designed for use in U.S.), FM/MW, 18-dot analog display, V_{DD}=5V, f_{ref}=7.2MHz, used with LB3500 (1/8 prescaler)
LC7226	699	QIP	64	3026B	PLL Electronic Tuning System for FM/AM Radio	(Designed for use in Japan), FM/MW, 18-dot analog display, V_{DD}=5V, f_{ref}=7.2MHz, used with LB3500 (1/8 prescaler)
LC7227	699	QIP	64	3026B	PLL Electronic Tuning System for FM/AM Radio	(Designed for use in Europe), FM/MW, 18-dot analog display, V_{DD}=5V, f_{ref}=7.2MHz, used with LB3500 (1/8 prescaler)
***LM7000**	910	DIP	20	3021B	Direct PLL Electronic Tuning System	On-chip IF counter, on-chip high-speed programmable divider capable of direct dividing FM band VCO frequency
LC7250	727	DIP	42	3014A	Digital 4-Digit Frequency Indicator (LED) with Clock	Reference frequency 4MHz, used with 1/100 prescaler, FM/MW/LM, static display, clock
LC7253	746	DIP	42	3014A	Digital 5-Digit Frequency Indicator (FLT) with Clock	Reference frequency 4MHz, used with 1/100 prescaler, FM/SW/MW/LW, static display, clock
LC7257	764	DIP	42	3014A	Digital 5-Digit Frequency Indicator (LED)	Reference frequency 4MHz, used with 1/100 prescaler, FM/SW/MW/LW, static display
LC7258	764	DIP	42	3014A	Digital 5-Digit Frequency Indicator (FLT)	Reference frequency 4MHz, used with 1/100 prescaler, FM/SW/MW/LW, static display
LC7265	780	DIP	28-S	3029A	Digital 5-Digit Frequency Indicator (LED)	Reference frequency 7.2MHz, used with 1/8 prescaler (LB3500), FM/MW/LW, static display
LC7266	780	DIP	28-S	3029A	Digital 5-Digit Frequency Indicator (FLT)	Reference frequency 7.2MHz, used with 1/8 prescaler (LB3500), FM/MW/LW, static display
***LC7267**	789	DIP	42	3025B	Digital 5-Digit Frequency Indicator (LED) with Clock	Reference frequency 7.2MHz, used with 1/8 prescaler (LB3500), FM/MW/LW, static display, clock
***LC7268**	789	DIP	42	3025B	Digital 5-Digit Frequency Indicator (FLT) with Clock	Reference frequency 7.2MHz, used with 1/8 prescaler (LB3500), FM/MW/LW, static display, clock
LC7500	796	DIP	16	3006A	Electronic Volume Controller	Electronic volume control system available in conjunction with LA2600, on-chip 5-bit up/down counter
LC7510	801	DIP	18	3007A	3-Piece Automatic Cuing System for Tape Recorder	
LC7512	801	DIP	18	3007A	3-Piece Automatic Cuing System for Tape Recorder (Automatic programming of preceding or following 1 piece)	[Automatic forward or backward cuing of desired music up to 3 pcs. from prerecorded tape, stable operation against noise pulse in unrecorded area and sound cut in recorded area]
LC7515	813	DIP	20	3021B	5-Piece Automatic Cuing System for Tape Recorder	Automatic forward or backward cuing of desired music up to 5 pcs.
LC7517	821	DIP	20	3010A	7-Piece Automatic Cuing System for Tape Recorder	Automatic forward or backward cuing of desired music up to 7 pcs.
LC7530	839	DIP	20	3008A	Electronic Volume Controller (2 channels, 16 steps, LED display)	Total resistance 50kΩ, pins for volume up/down and initialization, attenuation curve approaching type A

LC7533	843	DIP	16	3006A	Electronic Volume Controller (2 channels, 16 steps)	3V operation, total resistance 50kΩ, volume up/down, attenuation curve approaching type A
LC7534M	843	MFP	20	3036B	Electronic Volume Controller (2 channels, 16 steps), Headphone Stereo Applications	3V operation, total resistance 50kΩ, volume up/down, attenuation curve approaching type A
***LC7520**	830	DIP	28	3012A	Graphic Equalizer ECS System	Breakdown voltage 40V, 7 bands each of right/left, 2dB/step±10dB variable with up/down switch
LC7560	830	QIP	64	3057	Graphic Equalizer ECS System, LCD Driver	1/2 duty LCD drive, spectrum analyzing display of band-pass signal strength (7 bands, 2dB/step 11-dot display)
LC7570	861	DIP	40	3025B	FL Static Driver	34-segment output, on-chip pull-down resistor, 5-step AD converter
LC7572	864	DIP	18	3007A	Preset Address Display LED Driver	16-dot display, 0 to F hexadecimal display, 0 to 19 decimal display
LC7550	845	QIP	64	3026B	Level Meter (FLT) with Peak Hold Function	24 dots x 2 channels, static display, peak hold function
LC7555	852	DIP	42	3014A	Level Meter (FLT) with Peak Hold Function	12 dots x 2 channels, static display, peak hold function
LC7556	852	DIP	42	3014A	Level Meter (FLT) with Peak Hold Function	12 dots x 2 channels, static display, peak hold function, mirror image pin assignment as against LC7555
LC7815	868	DIP	28	3029A	2-Pole 4-Position Function Switch, LED Display Driver, Muting Function	4.5 to 18V/single-supply, ±4.5 to ±9V/dual-supply
LC7815H	876	DIP	28	3029A	2-Pole 4-Position Function Switch, LED Display Driver, Muting Function	4.5 to 23V/single-supply, ±4.5 to ±11.5V/dual-supply
LC7816	884	DIP	28	3029A	2-Pole 4-Position Function Switch, LED Display Driver, Muting Function	±18V/dual-supply
LC7817	891	DIP	28	3012A	2-Pole 4-Position Function Switch, LED Display Driver, Muting Function	±18V/dual-supply
***LC7820**	898	DIP	28	3029A	2-Pole 4-Position Function Switch, Tape Monitor Function, Muting Function	Breakdown voltage 40V, microcomputer-controlled, graphic equalizer input/output function
LC7910	903	DIP	16	3006A	6-Bit 64-Step AD/DA Converter	Single 5V supply, serial/parallel data output/input
LM8523	915	DIP	42	3014A	Counter for Tape Recorder	Direct drive capability of 4-digit LED/FLT, reference frequency 50/60Hz, blanking pin

OTHER APPLICATIONS(TELEPHONE APPLICATIONS, ELECTRONIC MUSICAL INSTRUMENT APPLICATIONS)

Type Number	Page	Case			Circuit Functions & Applications	Main Specifications
		Package	Pins	Package No.		
***LC7150**	929	DIP	18	3007A	PLL for Cordless Telephone	On-chip PLL for transmission/reception, on-chip unlock detector, guard tone, standby function
LC7350	933	DIP	18	3007A	Pulse Dialer	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial function
LC7351	933	DIP	20S	3021B	Pulse Dialer (with beep tone)	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial operation, beep tone
***LC7352**	937	DIP	18	3007A	Pulse Dialer	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial function, (key entry L)
LC7353	943	DIP	18	3007A	Pulse Dialer	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial function, (open drain)
LC7354	943	DIP	20S	3021B	Pulse Dialer (with beep tone)	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial function, (open drain)
LC7355	948	DIP	18	3007A	Pulse Dialer	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial function, (meeting domestic IDP requirement)
LC7356	948	DIP	20S	3008A	Pulse Dialer (with beep tone)	Low-voltage operation (V_{DD}=1.5 to 3.5V), redial function, (meeting domestic IDP requirement)
***LC7360**	954	DIP	22	3010A	Tone/Pulse Switchable Dialer	31-digit (tone + pulse) mix redial function
***LC7365**	960	DIP	16	3006A	Tone Dialer (DTMF signal generation)	Wide operating voltage range (V_{DD}=2.5 to 10V), DTMF signal generation, equivalent to S2559
LC7450	966	DIP	16	3006A	PLL for CATV RF Modulator	Video carrier/audio carrier generator, on-chip 8.0MHz oscillator
LC7460	969	DIP	16	3006A	Remote Control Transmission	8-function optical transmission, on-chip 540kHz ceramic oscillator
***LC7930**	973	QIP	60	3055A	LCD Driver	40-output segment driver or 20-output segment driver + 20-output back plate driver
LM8071	979	DIP	24	3011A	Master Tone Generator of Equal Tempered Scale for Electronic Organ	13 fundamental tones for 1 octave, driven by 2-phase clock pulses generated by a main oscillator
LM8372	984	DIP	16	3006A	Rhythm Pattern Generator	Selectable rhythms: 8, outputs for pattern generation: 6, time: simple triple time, quadruple time, output pin for tempo lamp
LM8471	988	DIP	28	3012A	Rhythm Pattern Generator	Selectable rhythms: 10, time: simple triple time, quadruple time, outputs for tone generator drive: 8, outputs for auto chord: 3, on-chip oscillator
LM8972	992	DIP	16	3006A	Rhythm Pattern Generator	Selectable rhythms: 8, outputs for pattern generation: 5, time: simple triple time, quadruple time, output pin for tempo lamp

DISCOUNTINUED PRODUCTS

C MOS IC'S, LSI'S

Type Number	Replacement	Package No.	Circuit Functions & Applications	Main Specifications
LC5631	–	–	LCD Digital Watch	V_{DD}=1.5V (Ag battery-powered)
LC5632	–	–	LCD Digital Watch	V_{DD}=3V (Li battery-powered)
LC7110	–	3008A	CB Transceiver PLL Frequency Synthesizer	Reference frequency oscillator, 9-bit programmable counter
LC7112	–	3008A	CB Transceiver PLL Frequency Synthesizer	Reference frequency oscillator, programmable counter N=3 to 511
LC7113	–	3006A	CB Transceiver PLL Frequency Synthesizer	Reference frequency oscillator, programmable counter N=64 to 191
LC7130	–	3008A	CB Transceiver PLL Frequency Synthesizer	Capable of direct dividing 16MHz band VCO frequency, BCD input, active filter
LC7180	–	3008A	CB Transceiver Channel Selector System	Up/down counter and channel output ROM, 40 channels (U.S.)
LC7190	–	3008A	CB Transceiver Channel Selector System	Up/down counter for channel memory and channel output ROM, 40 channels (U.S.)
LC7259	–	3014A	Digital Frequency Display (Green/Red LED)	FM/AM digital frequency display, green LED direct drive, static display

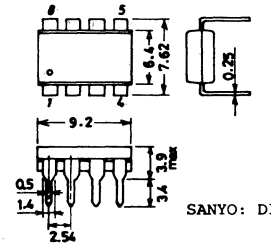
P MOS IC'S, LSI'S

Type Number	Replacement	Package No.	Circuit Functions & Applications	Main Specifications
LM3216	–	3003A	Frequency Divider for Electronic Organ	Low output impedance and 20kΩ load drive capability
LM8061	–	3011A	Digital Clock, Timer	–
LM8062	–	3011A	Digital Clock, Timer	–
LM8063	–	3011A	Digital Clock, Timer	–
LM8064	–	3011A	Digital Clock, Timer	–
LM8065	–	3011A	Digital Clock, Timer	–
LM8072	–	3011A	Unequal Tempered Scale Generator for Electronic Organ	Driven by 2-phase clock pulses generated by a main oscillator
LM8081	–	3011A	Channel Selector, Electronic SW Circuit for TV, Radio, etc.	Corresponding channel selection, bidirectional sequential channel selection, 12 channels pre-settable
LM8162	–	3011A	Digital Clock, Timer	–
LM8164	–	3011A	Digital Clock, Timer	–
LM8165	–	3011A	Digital Clock, Timer	–
LM8168	–	3011A	Digital Clock, Timer	–
LM8360	–	3013A	Digital Clock Alarm	Red LEC direct drivable (4 digits), FLT direct drivable
LM8369	–	3008A	Timer	1 to 9-hour timer using commercial frequency
LM8521	–	3014A	Tape Counter	LED, FLT direct drivable, stopwatch, auto stop, memory stop, zero stop, lap
LM8948	–	3006A	7 Buffer	H input level: 0 to 1V, L input level: -20 to -3.5V, maximum output voltage: -40Vmax.

Microcomputer/MOS IC Case Outlines

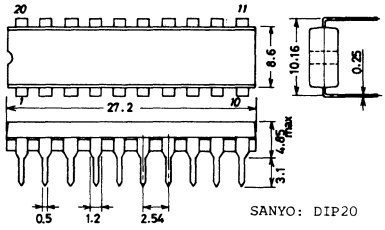
- All of Sanyo microcomputer/MOS IC case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. represent typical values.
- No marking is indicated.

Figure - 3001A
unit: mm



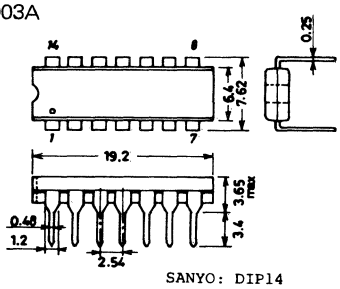
SANYO: DIP8

Figure - 3008A
unit: mm



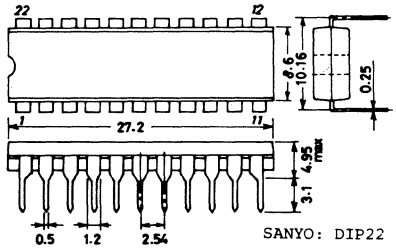
SANYO: DIP20

Figure - 3003A
unit: mm



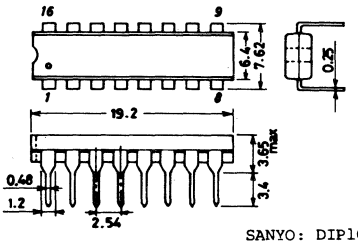
SANYO: DIP14

Figure - 3010A
unit: mm



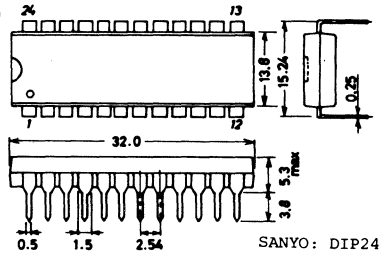
SANYO: DIP22

Figure - 3006A
unit: mm



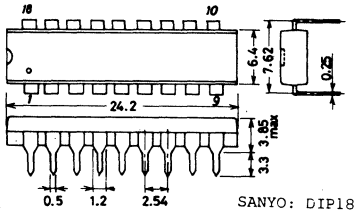
SANYO: DIP16

Figure - 3011A
unit: mm



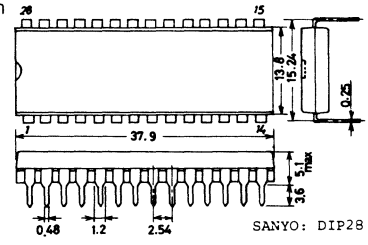
SANYO: DIP24

Figure - 3007A
unit: mm



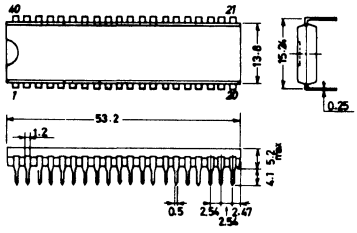
SANYO: DIP18

Figure - 3012A
unit: mm



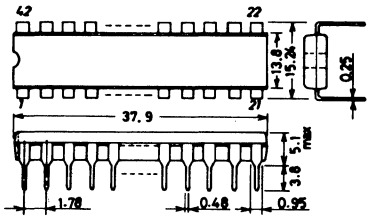
SANYO: DIP28

Figure - 3013A
unit: mm



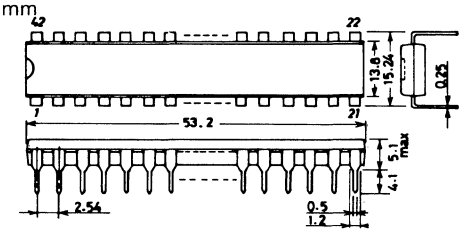
SANYO: DIP40

Figure - 3025B
unit: mm



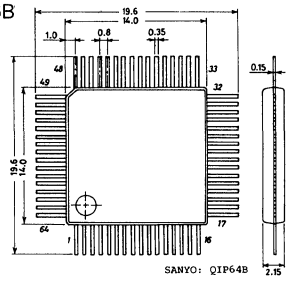
SANYO: DIP42S

Figure - 3014A
unit: mm



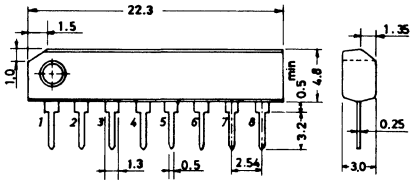
SANYO: DIP42

Figure - 3026B
unit: mm



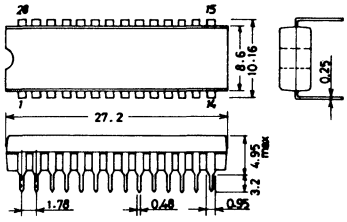
SANYO: QIP64B

Figure - 3016B
unit: mm



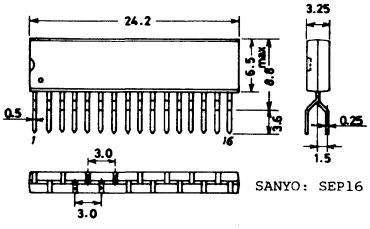
SANYO: SEP8

Figure - 3029A
unit: mm



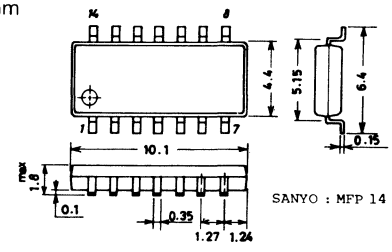
SANYO: DIP28S

Figure - 3020A
unit: mm



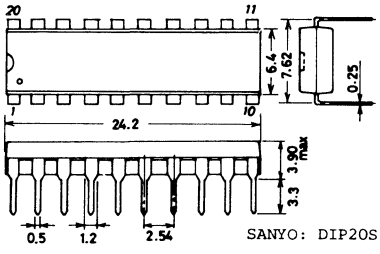
SANYO: SEP16

Figure - 3034A
unit: mm



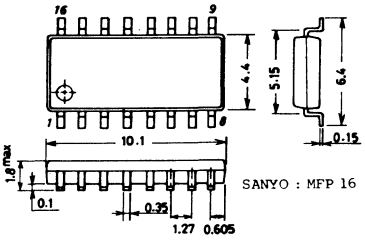
SANYO : MFP 14

Figure - 3021B
unit: mm



SANYO: DIP20S

Figure - 3035A
unit: mm



SANYO : MFP 16

Figure - 3036B
unit: mm

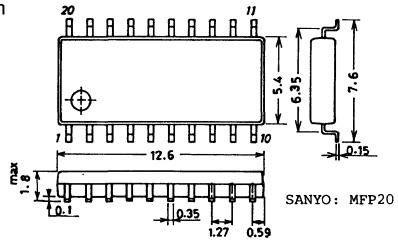


Figure 3057
unit: mm

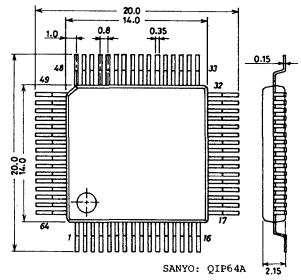


Figure - 3044B
unit: mm

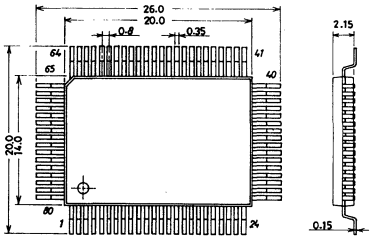


Figure 3047A
unit: mm

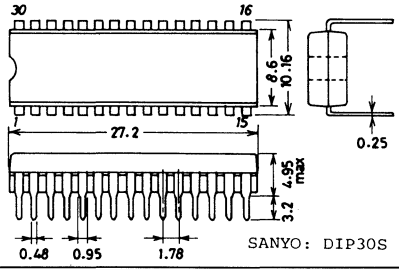


Figure 3053
unit: mm

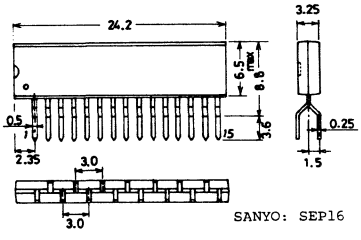
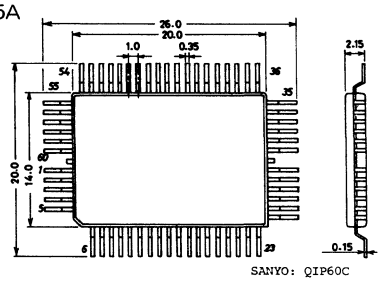


Figure 3055A
unit: mm



GENERAL INFORMATION

2. PRODUCT TYPES

2.1 Product Types

This HANDBOOK contains technical data on semiconductor devices available from Tokyo Sanyo Semiconductor Division as standard products and also on semiconductor devices being developed (as of March, 1984) for inclusion in our standard products.

No technical data on custom-made semiconductor devices or optional semiconductor devices are presented in this HANDBOOK.

If the types or characteristics of semiconductor devices do not meet your requirements, you can ask consultation. We provide custom-made versions, new developments, and/or options of our semiconductor devices according to consultation.

[Table 2.1] Sanyo Semiconductor Device Numbering System

Type Number	Description	Registered with
LAXXXX	Monolithic bipolar linear IC	Sanyo
LBXXXX	Monolithic bipolar digital IC	Sanyo
LCXXXX	Monolithic C-MOS IC	Sanyo
LDXXXX	Thin film IC	Sanyo
LMXXXX	Monolithic P-MOS IC	Sanyo
STKXXX	Thick film IC	Sanyo
2SAXXX	High frequency PNP transistor	EIAJ
2SBXXX	Low frequency PNP transistor	EIAJ
2SCXXX	High frequency NPN transistor	EIAJ
2SDXXX	Low frequency NPN transistor	EIAJ
2SFXXXX	Reverse blocking thyristor	EIAJ
2SJXX	P-channel FET	EIAJ
2SKXX	N-channel FET	EIAJ
2SMXXX	Bidirectional thyristor	EIAJ
1SXXXX	Diode	EIAJ
TSXXX	Silicon transistor	Sanyo
TGXXX	Germanium transistor	Sanyo
DSXXX	Silicon diode	Sanyo
DGXXX	Germanium diode	Sanyo
SZXX	Reference diode	Sanyo
SZAXX	Reference diode	Sanyo
SDTXXX	Thermistor	Sanyo

2.2 Type Numbers

Type numbers in Table 2.1 are roughly divided into two groups: EIAJ numbers and Sanyo numbers.

(1) EIAJ (Electronic Industries Association of Japan) numbers

These are serial numbers registered with the Electronic Industries Association of Japan.

We use EIAJ numbers for discrete transistors only. Some numbers may be followed by A, B, C, etc. to classify the characteristic.

For semiconductor devices other than discrete transistors, we use Sanyo numbers described in (2) below.

(2) Sanyo numbers

Type numbers for integrated circuits are not standardized yet in the semiconductor industry. Each company has its own type numbers.

Sanyo numbers for discrete transistors are temporary ones, which are changed to EIAJ numbers after completion of thier development unless there arise special circumstances.

For diodes, we use Sanyo numbers without changing to EIAJ numbers.

2.3 Symbols

Symbols are often used to represent the characteristics of semiconductor devices. A simple description is given to each symbol presented in this HANDBOOK. No description is given to symbols which are self-explanatory or are not commonly used.

Generally speaking, symbols and their suffixes are written in capital letters for DC characteristics and small letters for AC characteristics. This rule is observed in this HANDBOOK, with some exceptions.

Suffixes are used to give supplementary explanations to symbols.

Fundamental electrical symbols and symbols used to denote figures are defined by JIS. In this HANDBOOK, symbols shown below are used to denote figures.

Figure	10^9	10^6	10^3	10^0	10^{-3}	10^{-6}	10^{-9}	10^{-12}
Symbol	G	M	k	–	m	μ	n	p

The following are units and their symbols used in this HANDBOOK.

Voltage V
Current . . . . . A
Power . . . . . W
Impedance . . . . . Ω

Admittance . . . . . S
Capacitance . . . . . F
Inductance . . . . . H
Time . . . . . sec (s), min, hour (h)
Frequency . . . . . Hz
Gain . . . . . dB
Phase angle . . . . . degree
Relative humidity . . . . . %
Temperature . . . . . °C

The following are symbols used in this HANDBOOK.

ACA : Adjacent channel attenuation (unit: dB)

AMR : AM rejection (unit: dB)

BW : Bandwidth (unit: Hz)

c_i, c_o : Input/output capacitance (unit: F)

$2f_{itweet}$: Tweet interference (unit: dB, %)

g_i, b_i : Input conductance, $y_i=g_i+jb_i$ (unit: S)

g_o, b_o : Output conductance, $y_o=g_o+jb_o$ (unit: S)

I_{CC}, I_{DD} : Current dissipation (unit: A)

I_{CCO} : Quiescent current (unit: A)

i_i, i_o : Input/output current (unit: A)

I_O : Output current in amp (unit: A)

I_{IH}, I_{IL} : H/L-level input current (unit: A)

I_{OH}, I_{OL} : H/L-level output current (unit: A)

I_L : Lamp drive current (multiplex IC) (unit: A)

I_n : Current in pin n (unit: A)

NF : Noise figure (unit: dB)

PBW : Power bandwidth (unit: Hz)

P_d : Power dissipation in IC (unit: W)

P_{dmax} : Allowable power dissipation (unit: W)

PG : Power gain (unit: dB)

Q_s : Usable sensitivity (unit: dB, dB/m, V, V/m)

Sep : Stereo separation (unit: dB)

r_i, r_o : Input/output resistance (unit: Ω)

T_a : Ambient temperature (unit: °C)

T_c : Case temperature (unit: °C)

T_{opg} : Operating temperature (unit: °C)

T_{stg} : Storage temperature (unit: °C)

t_f : Fall time (unit: sec)

t_{stg} : Storage time (unit: sec)

t_{on} : Turn-on time=delay time t_d+rise time t_r (unit: sec)

t_{off} : Turn-off time=storage time t_{stg}+fall time t_f (unit: sec)

THD : Total harmonic distortion (no unit, %)

V_{CC} : Supply voltage (unit: V)

V_{CCmax} : Maximum supply voltage (unit: V)

$V_{DD}, V_{DDmax}, V_{GG}, V_{GGmax}$: Supply voltage for MOS IC (unit: V)

v_i, v_o : Input/output voltage (unit: V)

V_{IH}, V_{IL} : H/L-level input voltage (unit: V)

V_{OH}, V_{OL} : H/L-level output voltage (unit: V)

V_L : Lamp lighting level (unit: V)

V_n : Voltage on pin n (unit: V)

V_{m-n} : Voltage on pin m to pin n (unit: V) I_{m-n} is defined likewise.

V_{NO} : Output noise voltage (unit: V)

VG : Voltage gain (unit: dB)

V_S : Maximum sensitivity (unit: dB, dB/m, V, V/m)

$|y_f|$: Output short-circuit forward transfer admittance

$y_f = |y_f| \exp(j\phi f)$ (unit: S)

Besides the above-mentioned, the following established symbols are used. Ground-Gnd, load resistance — R_L, signal to noise ratio — S/N, AGC voltage — V_{AGC}, oscillation voltage — V_{osc}, oscillation voltage variation — ΔV_{osc}, input — IN (or in, input, etc.), output — OUT (or out, output, etc.), impedance elements — R, L, C, time — t.

2. PRODUKTTYPEN UND SYMBOLE

2.1 Produkttypen

In diesem Handbuch sind von Sanyo entwickelte, hergestellte und in den Handel gebrachte Standardprodukte enthalten.

Auch für zur Zeit (März 1984) in der Entwicklung befindliche Produkte werden die Daten angegeben. Spezialanfertigungen und Sonderzubehör sind nicht in diesem Handbuch enthalten.

Wenn die Kennwerte der Produkte nicht den Anforderungen des Kunden entsprechen, stehen wir zur Beratung bereit. Wir bieten kundenspezifische Versionen, neue Entwicklungen und/oder Optionen unserer Produkte gemäß Beratung.

Tabelle 2.1 Sanyo Halbleiter-Produkte Sortentabelle

Typen-Nummer	Beschreibung	Registriert
LAXXXX	Monolithischer Bipolar-Linear-IC	Sanyo
LBXXXX	Monolithischer Bipolar-Digital-IC	Sanyo
LCXXXX	Monolithischer C-MOS IC	Sanyo
LDXXXX	Dünnschicht-IC	Sanyo
LMXXXX	Monolithischer P-MOS IC	Sanyo
STKXXX	Dickschicht-IC	Sanyo
2SAXXX	Hochfrequenz-PNP-Transistor	EIAJ
2SBXXX	Niederfrequenz-PNP-Transistor	EIAJ
2SCXXXX	Hochfrequenz-NPN-Transistor	EIAJ
2SDXXX	Niederfrequenz-NPN-Transistor	EIAJ
2SFXXXX	Rückwärts sperrender Thyristor	EIAJ
2SJXX	P-Kanal-FET	EIAJ
2SKXX	N-Kanal-FET	EIAJ
2SMXXX	2-Weg-Thyristor	EIAJ
1SXXXX	Diode	EIAJ
TSXXX	Silizium-Transistor	Sanyo
TGXXX	Germanium-Transistor	Sanyo
DSXXX	Silizium-Diode	Sanyo
DGXXX	Germanium-Diode	Sanyo
SZXX	Zenerdiode	Sanyo
SZAXX	Referenzdiode	Sanyo
SDTXXX	Thermistor	Sanyo

2.2 Typennummern

Wie aus Tabelle 2.1 ersichtlich, gibt es verschiedene Typennummern, diese Nummern fallen hauptsächlich in eine der beiden Gruppennummern der EIAJ (Elektronic Industries Association of Japan) und Sanyo-Nummern.

(1) EIAJ-Nummer

Es handelt sich hierbei um die Folgenummer, die von der EIAJ dem Produkt zugewiesen wird, und zwar in der Reihenfolge der Beantragung durch ein Mitglied der EIAJ gemäß den durch den EIAJ vorgegebenen Spezifikationen und Klassifikationen.

EIAJ-Nummern werden nur für unsere diskreten Transistoren verwendet. A, B oder C usw. können zu EIAJ-Nummern hinzugefügt werden, um zusätzliche Eigenschaften bzw. Kennwerte eines Produkts auszuweisen. Alle weiteren Halbleitererzeugnisse von Sanyo werden durch die Sanyo-Nummern (2) identifiziert.

(2) Sanyo-Nummern

Bei ICs liegt es in der Natur der Sache, daß ihre Numerierung noch nicht genormt ist und die Hersteller jeweils eigene Numerierungssysteme für ihre IC-Produkte verwenden.

Sanyo-Nummern werden im allgemeinen während der Entwicklung vorübergehend für diskrete Transistoren verwendet. Nachdem die Entwicklung abgeschlossen ist, werden diese Nummern grundsätzlich gegen EIAJ-Nummern ausgetauscht, falls nicht ausdrücklich anderweitig festgelegt ist. Für Dioden bleiben Sanyo-Nummern erhalten.

2.3 Für Halbleiterprodukte verwendete Symbole

Symbole werden auch zur Darstellung der Kennwerte von Halbleiterprodukten verwendet. Die in diesem Handbuch verwendeten Symbole werden in diesem Abschnitt kurz vorgestellt. Es sind jedoch keine Symbole enthalten, die nur die Bedeutung enthalten bzw. solche ohne Assoziation zu mehreren Modellen.

Mit einigen wenigen Ausnahmen werden für Symbole und Zusätze, die die Gleichstromwerte veranschaulichen, Großbuchstaben verwendet und für Wechselstromwerte Kleinbuchstaben. Der an ein Symbol angehängte Zusatz (Suffix) weist auf externe Merkmale des Symbols hin.

Die grundlegenden Symbole für Elektrizität und die Anzahl Stellen sind durch JIS (Japanischer Industrie-Standard) definiert. In diesem Handbuch wird die Anzahl der Stellen durch die folgenden Symbole dargestellt:

Anzahl Stellen	10^9	10^6	10^3	10^0	10^{-3}	10^{-6}	10^{-9}	10^{-12}
Symbol	G	M	k	–	m	μ	n	p

Die grundlegenden elektrischen Ausdrücke werden durch die folgenden Symbole dargestellt:

Spannung	V
Strom	A
Leistung	W
Impedanz	Ω
Admittanz	S
Kapazität	F
Induktivität	H
Zeit	sec (s), min, hour (h)
Frequenz	Hz
Dezibel	dB
Phasenwinkel	Grad (°)
Relative Luftfeuchtigkeit	%
Temperatur	°C

Die hauptsächlichen elektrischen Symbole werden basierend auf der obigen Zeichenvereinbarung wie folgt dargestellt:

ACA : Einzelsignal-Selektivität (Einheit: dB)

AMR : AM-Unterdrückung (Einheit: dB)

BW : Bandbreite (Einheit: Hz)

c_i, c_o : Eingangs/Ausgangs-Kapazität (Einheit: F)

$2f_{itweet}$: Hochton-Störverhältnis (Einheit: dB, %)

g_i, b_i : Eingangsleitwert, $y_i = g_i + jb_i$ (Einheit: S)

g_o, b_o : Ausgangsleitwert, $y_o = g_o + jb_o$ (Einheit: S)

I_{CC}, I_{DD} : Verluststrom (Einheit: A)

I_{CCO} : Ruhestrom (Einheit: A)

i_i, i_o : Eingangs/Ausgangs-Strom (Einheit: A)

I_O : Ausgangsstrom durch die Verstärker-Schaltkreise (Einheit: A)

I_{IH}, I_{IL} : Eingangsstrom mit hohem/niedrigem Pegel (Einheit: A)

I_{OH}, I_{OL} : Ausgangsstrom mit hohem/niedrigem Pegel (Einheit: A)

I_L : Lampentreiberstrom (Multiplex-ICs) (Einheit: A)

I_n : Strom durch Stift n (Einheit: A)

NF : Rauschfaktor (Einheit: dB)

PBW : Leistungsbandbreite, gemessen mit konstanten Klirrfaktor (Einheit: Hz)

P_d : Verlustleistung von IC unter bestimmten Bedingungen (Einheit: W)

$P_{d\,max.}$: Max. zulässiger Wert der Verlustleistung (P_d). (Einheit: W)

PG : Leistungsverstärkung (Einheit: dB)

Q_s : Effektive Empfindlichkeit (Einheit: dB, dB/m, V, V/m)

Sep. : Stereokanaltrennung (Einheit: dB)

r_i, r_o : Eingangs/Ausgangs-Widerstand (Einheit: Ω)

T_a : Umgebungstemperatur (Einheit: °C)

T_c : Gehäusetemperatur (Einheit: °C)

T_{opg} : Betriebstemperatur (Einheit: °C)

T_{stg} : Lagertemperatur (Einheit: °C)

T_f : Abfallzeit (Einheit: sec)

t_{stg} : Speicherzeit (Einheit: sec)

t_{on} : Einschaltzeit, t_{on} = Verzögerungszeit t_d + Anstiegszeit t_r (Einheit: sec)

t_{off} : Ausschaltzeit, t_{off} = Speicherzeit t_{stg} + Abfallzeit t_f (Einheit: sec)

THD : Gesamtklirrfaktor (Einheit: keine oder %)

V_{CC} : Versogungsspannung (Einheit: V)

$V_{CC\,max.}$: Max. Nennwert von V_{CC} (Einheit: V)

V_{DD}, $V_{DD\,max}$, V_{GG}, $V_{GG\,max.}$: Versorgungsspannung. V_{CC} wird nicht immer für MOS ICs verwendet, da die Spannungsversorgung auf verschiedene Weise erfolgt. (Einheit: V)

v_i, v_o : Eingangs/Ausgangsspannung (Einheit: V)

V_{IH}, V_{IL} : Eingangsspannung mit hohem/niedrigem Pegel (Einheit: V)

V_{OH}, V_{OL} : Ausgangsspannung mit hohem/niedrigem Pegel (Einheit: V)

V_L : Lampenleuchtpegel (Einheit: V)

V_n : Spannung an Stift n (Einheit: V)

V_{m-n} : Spannung von Stift m an Stift n (Einheit: V)
Das gleiche gilt für I_{m-n}.

V_{NO} : Ausgangsrauschspannung (Einheit: V)

VG : Spannungsverstärkung (Einheit: dB)

V_s : Max. Empfindlichkeit (Einheit: dB, dB/m, V, V/m)

$|y_f|$: Admittanz für Ausgangs-Kurzschluß-Vorwärts-Spannungsübersetzung

$y_f = |y_f|_{exp}(j\phi f)$ (Einheit: S)

Darüberhinaus wird eine allgemein übliche Benennung verwendet für Ausdrücke wie Erdung (Gnd), Lastwiderstand (R_L), Fremdspannungsabstand (S/N), AGC-Spannung (V_{AGG}), Schwingspannungsschwankung (V_{OSC}), Eingang (IN, in, oder input), Ausgang (OUT, out, oder output), Impedanzelemente (R, L oder C), Zeit (t) usw..

2. NUMEROS DE TYPE ET SYMBOLES UTILISES DANS CE MANUEL

2.1 Numéros de type

Les numéros de types indiqués dans de manuel sont ceux des types standard qui sont fabriqués maintenant (mars 1984) et le seront dans un avenir proche. Les commandes spéciales n'y figurent pas.

Regardez ce manuel, et s'il y a un produit ou une caractérisque qui ne vous conviennent pas, n'hésitez pas à nous consulter. Nous pouvons mettre à votre disposition des produits sur commande, mettre au point de nouveaux produits ou des caractéristiques spécifiques.

Tableau 2.1 Liste des dénominations des semi-conducteurs Sanyo

Numéro de type	Description	Enregistré sous
LAXXXX	CI linéaire bipolaire monolithique	Sanyo
LBXXXX	CI digital bipolaire monolithique	Sanyo
LCXXXX	CI monolitique C-MOS	Sanyo
LDXXXX	Pellicule CI	Sanyo
LMXXXX	CI monolitique P-MOS	Sanyo
STKXXX	Pellicule CI	Sanyo
2SAXXX	Transistor haute fréquence PNP	EIAJ
2SBXXX	Transistor basse fréquence PNP	EIAJ
2SCXXX	Transistor haute fréquence NPN	EIAJ
2SDXXX	Transistor basse fréquence NPN	EIAJ
2SFXXXX	Thyristor à blocage inversé	EIAJ
2SJXX	FET de canal P	EIAJ
2SKXX	FET de canal N	EIAJ
2SMXXX	Thyristor bidirectionnel	EIAJ
1SXXXX	Diode	EIAJ
TSXXX	Transistor au silicium	Sanyo
TGXXX	Transistor au germanium	Sanyo
DSXXX	Diode au silicium	Sanyo
DGXXX	Diode au germanium	Sanyo
SZXX	Diode double	Sanyo
SZAXX	Diode double	Sanyo
SDTXXX	Thermistor	Sanyo

2.2 Numéro de produit

Il y a beaucoup de numéros de produits (numéro de type) dans le tableau 2.1, mais les plus importants sont les numéros EIAJ et SANYO.

(1) Numéros de l'Electronic Industries Association of Japan (EIAJ)

Ce sont les numéros attribués selon l'ordre d'enregistrement, conformément à la classification et prescription fixées.

Maintenant, dans notre société, nous nous consacrons à l'application des transistors de guidage de disque, et à la fin, il y a aussi la classification des caractéristiques A, B, C, etc.

Les autres semi-conducteurs portent un numéro SANYO (2).

(2) Numéro SANYO

En ce qui concerne les caractéristiques des CI, aujourd'hui, dans notre pays, elles ne sont pas uniformes, et chaque société leur donne ses propres numéros.

De plus, en principe, les numéros des transistors de guidage de disque SANYO, sont provisoires, et à la fin de l'étape de mise au point, ils seront convertis s'il n'y a pas de problème spécial, en numéros EIAJ.

Pour les diodes, le numéro SANYO sera utilisé tel quel.

2.3 Symboles et abréviations utilisés pour les semi-conducteurs

Si on veut indiquer les caractéristiques d'un semi-conducteur, souvent sans symbole, on utilise l'abréviation. Ici, nous vous donnons une proposition et explication simples de ces symboles et abréviations. Cependant, nous résumerons lorsque l'explication n'est pas nécessaire, ou si différents types possèdent les mêmes caractéristiques.

En général, le symbole et le chiffre annexe sont majuscules pour les caractéristiques du courant continu, et minuscules pour le courant alternatif. Il y a des exceptions, mais elles sont conformes à l'usage.

Le chiffre est un complément du symbole.

Le symbole qui indique fondamentalement un symbole électrique et son cœfficient sont définis par JIS, mais nous vous donnons le tableau de cœfficients suivants pour ce manuel.

Cœfficient	10^9	10^6	10^3	10^0	10^{-3}	10^{-6}	10^{-9}	10^{-12}
	G	M	k	—	m	u	n	p

Les unités utilisées sont les suivantes:

Tension	V
Courant	A
Puissance	P
Impédance	Ω
Admittance	S
Capacitance	F
Inductance	H
Temps	sec. (s), min, heure (h)
Fréquence	Hz
Gain	dB
Phase angulaire	degré
Humidité relative	%
Température	°C

Sur la base des éléments précédents, nous vous donnons la liste des abréviations principales:

ACA	: Degré de choix d'un signal (unité: dB)
AMR	: Rapport de pression AM (unité: dB)
BW	: Largeur de bande (unité: Hz)
c_i, c_o	: Capacitance d'entrée et de sortie (unité: Hz)
$2f_{itweet}$	: Rapport de brouillage (unité: dB, %)
g_i, b_i	: Conductance d'entrée $y_i=g_i+jb_i$ (unité: S)
g_o, b_o	: Conductance de sortie, $y_o=g_o+jb_o$ (unité: S)
I_{CC}, I_{DD}	: Courant consommé (unité: A)
I_{CCO}	: Courant sans signal (unité: A)
i_i, i_o	: Courants d'entrée et de sortie (unité: A)
I_O	: Courant de sortie du circuit d'amplification (unité: A)
I_{IH}, I_{IL}	: Puissance d'entrée H, courant de niveau L (unité: A)
I_{OH}, I_{OL}	: Puissance de sortie H, courant de niveau L (unité: A)
I_L	: Courant d'entraînement de lampe (CI multiplex) (unité: A)
I_n	: Courant circulant dans la fiche n (unité: A)
NF	: Cœfficent de bruits parasites (unité: dB)
PBW	: Largeur de la bande de puissance de sortie (unité: Hz)
P_d	: Courant consommé par le CI sur la base de conditions subsidiaires (unité: W)
$P_{d\ max}$	: Tolérance de consommation de courant (unité: W)
PG	: Gain de courant (unité: dB)
Q_s	: Sensibilité utile (unités: dB, dB/m, V, V/m)
SEP.	: Degré de séparation stéréo (unité: dB)
r_i, r_o	: Résistance aux puissances d'entrée et de sortie (unité: Ω)
T_a	: Température ambiante (unité: °C)
T_c	: Température du cas (unité: °C)
T_{opg}	: Température de fonctionnement (unité: °C)
T_{stg}	: Température ambiante maintenue (unité: °C)
t_f	: Temps de chute. Définision du circuit de mesure (unité: sec)
t_{stg}	: Temps d'emmagasinage (unité: sec)
t_{on}	: Temps d'ouverture = temps de retard t_d + temps de montée t_r (unité: sec)
t_{off}	: Temps de fermeture = temps d'emmagasinage t_{stg} + temps de chute t_f (unité: sec)
THD	: Taux de distorsion des hautes fréquences (unité: aucune. %)
V_{CC}	: Temps d'alimentation (unité: V)
$V_{CC\ max}$	: Tension d'alimentation maxi (unité: V)
V_{DP}, $V_{DD\ max}$, V_{GG}, $V_{GG\ max}$	: Dans le cas du CI MOS, il y a des cas où le V_{CC} n'est pas indiqué, cela signifie une tension dui diffère de par son mode d'application (unité: V)
v_i, v_o	: Tensions d'entrée et de sortie (unité: V)
V_{IH}, V_{IL}	: Puissance d'entrée H, niveau de tension L (unité: V)
V_{OH}, V_{OL}	: Puissance de sortie H, niveau de tension L (unité: V)
V_L	: Niveau d'allumage de lampe (unité: V)
V_n	: Tension de la fiche n (unité: V)
V_{m-n}	: Tension de la fiche m par rapport à la fiche n (unité: V) I_{m-n} est défini de la même manière
V_{NO}	: Tension parasite de puissance de sortie (unité: V)
VG	: Gain de tension (unité: dB)
V_s	: Sensibilité maxi (unités: dB, dB/m, V, V/m)
$\lvert y_f \rvert$	: Admittance de transmission de court-circuitage de la puissance de sortie $y_f = \lvert y_f \rvert_{exp}\ (j\phi f)$ (unité: S)

En outre, les autres éléments, mise à la masse Gnd, résistance à la charge R_L, taux de bruits parasites par rapport aux signaux S/N, tension AGC V_{AGC}, tension d'oscillation V_{OSC}, variation de tension d'oscillation ΔV_{OSC}, puissance d'entrée IN (ou in, input, apr ex.), puissance de sortie OUT (ou out, output, par ex.), données d'impédance R, L, C, unité de temps t, sont ordinaires.

2. 本手册所登载的品种和符号略号

2.1 登载的品种

本手册记载内容是目前敝公司开发，制造，销售的标准品以及正在开发中的产品到一九八四年三月为止的数据．至于特别定购品和特殊选别品，本手册设有记载．

阅读本手册后，如这些品种或特性不能满足要求，请与敝公司连络．我们可与顾客洽商，提供定做，新开发或特殊选别等服务．

〔表2.1〕 三洋半导体产品型号分类表

型　号	内　　容	号码登记对象
LA ××××	单块双极线性集成电路	三 洋
LB ××××	单块双极数字集成电路	三 洋
LC ××××	单块 C-MOS 集成电路	三 洋
LD ××××	薄膜集成电路	三 洋
LM××××	单块 P-MOS 集成电路	三 洋
STK×××	厚膜集成电路	三 洋
2SA ×××	高频用 PNP 晶体管	EIAJ
2SB ×××	低频用 PNP 晶体管	EIAJ
2SC ××××	高频用 NPN 晶体管	EIAJ
2SD ×××	低频用 NPN 晶体管	EIAJ
2SF ××××	反向阻档三极晶体用流管	EIAJ
2SJ ××	P 沟道场效应晶体管	EIAJ
2SK ××	N 沟道场效应晶体管	EIAJ
2SM×××	双向三极管	
1S××××	二极管	
TS ×××	硅晶体管	三 洋
TG ×××	锗晶体管	三 洋
DS ×××	硅晶体二极管	三 洋
DG ×××	锗二极管	三 洋
SZ ××	齐纳二极管	三 洋
SZA ××		三 洋
SDT ×××	热敏电阻	三 洋

2.2 产品号码

如表 2.1 所示，有多种产品号码，大概可分为 EIAJ 号码和三洋独自号码两种．

(1) 电子机械工业会 EIAJ 号码

这是日本电子机械工业会（Electronic Industries Association of Japan）会员按指定的规定和分类申请登录的顺序号码．

目前敝公司只在分立式晶体管方面采用这号码，另外，在这些号码后面有时再加A，B，C，…等，以便表示特性分类．

除这些产品外的半导体产品，采用(2)的三洋号码．

(2) 三洋号码

由于其性质上的原因，集成电路目前设实现全国统一号码，每公司都用其独自号码．

原则上，分立式晶体管的三洋号码是暂定性的，因此，除非另有特殊情形，将会改为 EIAJ 号码．

至于二极管，继续使用三洋号码．

2.3 半导体产品的记号，略号

表示半导体产品的特性时，使用各种记号或略号．在此简单地定义，说明本手册内所用的记号，略号．至于极明显，不需加以说明的，或设有通用性的记号等，恕省略说明．

一般地说，记号及其附加字母，直流特性时采用大写字母，交流特性时采用小写字母，虽稍有例外，但基本上采用了惯用方法．

附加字母是记号的补足．

基本的电气记号和表示位数的记号，被定于 JIS．在此列举本手册所用的位数表示记号如下：

位数	10^9	10^6	10^3	10^0	10^{-3}	10^{-6}	10^{-9}	10^{-12}
	G	M	k	—	m	μ	n	p

单位如下：

电压……V
电流……A
电力……W
阻抗……Ω
导纳……S
电容……F
电感……H
时间……sec（s），min，hour（h）
频率……Hz
增益……dB
相角……degree
相对温度……%
温度……℃

下面列举主要记号，略号：

ACA ：1 信号选择度.（单位dB）

AMR ：AM 抑压比.（单位dB）

BW ：带宽.（单位Hz）

c_i，c_o ：输入输出容量.（单位F）

$2f_{itweet}$ ：笛音妨害比.（单位dB，%）

g_i，b_i ：输入导电，$y_i = g_i + jb_i$（单位S）

g_o，b_o ：输出导电，$y_o = g_o + jb_o$（单位S）

I_{CC}，I_{DD} ：消耗电流.（单位A）

I_{CCO} ：静态电流.（单位A）

i_i，i_o ：输入输出电流.（单位A）

I_O ：增幅电路的输出电流.（单位A）

I_{IH}，I_{IL} ：输入H，L电平电流.（单位A）

I_{OH}，I_{OL} ：输出H，L电平电流.（单位A）

I_L ：电灯驱动电流.（多路集成电路）.（单位A）

I_n ：流于管脚n的电流.（单位A）

NF ：噪声指数. 参照V_{NO}（单位dB）

PBW ：功率带宽.（单位Hz）

P_d ：在附带条件下，集成电路的耗电量.（单位W）

$P_{d\ max}$ ：容许耗电量.（单位W）

PG ：电力增益.（单位dB）

Q_S ：实用灵敏度. 以AM接收机得到S/N 20dB，以FM接收机得到S/N 30dB 的标准功率所需的标准试验调制输入电平的最小值.（单位dB，dB/m，V，V/m）

Sep. ：立体声分离度.（单位dB）

r_i，r_o ：输入输出阻抗.（单位Ω）

T_a ：周围温度.（单位℃）

T_c ：机壳温度.（单位℃）

T_{opg} ：动作周围温度.（单位℃）

T_{stg} ：贮藏周围温度.（单位℃）

t_f ：下降时间.（单位sec）

t_{stg} ：积累时间.（单位sec）

t_{on} ：接通时间＝延迟时间t_d＋上升时间t_r.（单位sec）

t_{off} ：断开时间＝积累时间t_{stg}＋下降时间t_f.（单位sec）

THD ：全谐波失真.（无单位，%）

V_{CC} ：电源电压或推荐电源电压.（单位V）

$V_{CC\ max}$ ：最大电源电压.（单位V）

V_{DD}，$V_{DD\ max}$，V_{GG}，$V_{GG\ max}$：MOS集成电路的电源电压，最大电源电压. 如是MOS，有时不写V_{CC}，这是由于电源输入方法不同之缘故.（单位V）

v_i，v_o ：输入输出电压.（单位V）

V_{IH}，V_{IL}：输入H，L电平电压.（单位V）

V_{OH}，V_{OL}：输出H，L电平电压.（单位V）

V_L ：电灯发亮电平.（单位V）

V_n ：管脚n的电压.（单位V）

V_{m-n} ：管脚m对管脚n的电压.（单位V）
I_{m-n}也同样地被定义.

V_{NO} ：输出噪声电压.（单位V）

VG ：电压增益.（单位dB）

V_S ：最大灵敏度.（单位dB，dB/m，V，V/m）

$|y_f|$ ：输出短路顺传达导纳.
$y_f = |y_f| \exp(j\phi_f)$（单位S）

除了这些以外，接地Gnd，负荷阻抗R_L，信号对噪声比S/N，AGC电压V_{AGC}，振荡电压V_{OSC}，振荡电压变动ΔV_{OSC}，输入IN（或in，input等），输出OUT（或out，output等），阻抗零件R，L，C，时间单位t等均接惯用.

2. 掲載品種과 記号略号

2.1 掲載品種

이 핸드북의 개재품종은 현재 폐사에서 개발·제조·판매하고 있는 중의 표준품에 대하여, 그리고 개발중의 제품에 대하여서는 1984년 3월 현재의 데이터를 기재하고 있읍니다. 特注品이나 特殊選別品에 대하여서는 생략하고 있읍니다.

이 핸드북을 보시여 만일 이 것들의 품종 또는 특성에 만족하지 않은 경우에는 사양없이 상담하여 주시기 바랍니다. 의논함으로서 주문생산, 신기개발, 또는 특수선별등의 용이가 있읍니다.

〔표2.1〕 三洋半導体製品型名分類表

型　名	内　容	番号登録製造所
LA××××	monolithic bipolar linear IC	三洋独自
LB××××	monolithic bipolar digital IC	三洋独自
LC××××	monolithic bipolar C-MOS IC	三洋独自
LD××××	薄膜IC	三洋独自
LM××××	monolithic P-MOS IC	三洋独自
STK×××	厚膜IC	三洋独自
2SA×××	高周波用 PNP トランジスタ	EIAJ
2SB×××	低周波用 PNP トランジスタ	EIAJ
2SC××××	高周波用 NPN トランジスタ	EIAJ
2SD×××	低周波用 NPN トランジスタ	EIAJ
2SF××××	逆阻止ダイリスタ	EIAJ
2SJ××	P-channel FET	EIAJ
2SK××	N-channel FET	EIAJ
2SM×××	双方向性ダイリスタ	EIAJ
1S××××	ダイオード	EIAJ
TS×××	シリコントランジスタ	三洋独自
TG×××	ゲルマニュトランジスタ	三洋独自
DS×××	シリコンダイオード	三洋独自
DG×××	ゲルマニュダイオード	三洋独自
SZ××	ゼナダイオード	三洋独自
SZA ××		三洋独自
SDT ×××	ダイアミスター	三洋独自

2.2 製品番号

제품번호는 표 2.1 에 표시하는바 다종합니다. 대별하면 EIAJ 넘버와 三洋(SANYO)독자의 넘버의 2 종류가 있읍니다.

(1) 電子機械工業会 EIAJ 넘버

이것은 日本電子機械工業会(Electronic Industries Association of Japan)会員이 지정된 규정·분류에 따라 등록신청한 순서에 따른 번호입니다.

현재 폐사에서는 디스크리트트랜지스터만에 적용하고 있으며 또한 그 말미에 A, B, C, … 등을 붙여 특성의 분류를 할 경우도 있읍니다.

이것들 이외의 반도체제품은 (2)의 三洋넘버를 쓰고 있읍니다.

(2) 三洋넘버

IC 에 관하여서는 그 성질상, 현재에 이르기까지 전국적인 통일이 이룩하지 않고 있으며 각사 각색의 번호가 붙여 있읍니다.

그리고 디스크리트트랜지스터의 三洋넘버는 원칙적으로 잠정적인 것이며 개발단계를 넘으면 특별한 사정이 없는한 EIAJ 넘버에 변경됩니다.

다이오드에 대하여서는 三洋넘버를 그대로 사용하고 있읍니다.

2.3 반도체제품에 사용하는 記号·略号

반도체제품의 특성을 표시할 경우, 자주 기호나 약호가 사용됩니다. 여기서는 이 핸드북에서 사용되고 있는 기호·약호에 대하여 간단한 정의와 해설을 하고 있읍니다. 단 설명이 맹백히 필요 없는 것이나 수종류에 걸쳐 공통성이 없는 기호등은 생략하고 있유니다.

일반적으로 기호 및 그의 접미기호는 직류특성에서는 대문자로, 교류특성에서는 소문자로 사용하고 있읍니다. 예외도 있읍니다만 관용에 따르고 있읍니다.

접미기호의 의미는 그의 기호의 보충입니다.

기본적인 전기기호 및 자릿수를 표시하는 기호는 JIS 에 결정되어 있읍니다만, 이 핸드북에서 사용하는 자릿수표시기호에 대하여 설명합니다.

자릿수	10^9	10^6	10^3	10^0	10^{-3}	10^{-6}	10^{-9}	10^{-12}
	G	M	k	—	m	μ	n	p

단위는 다음과 같습니다.

전압……V
전류……A
전력……W
임피던스……Ω
어드미턴스……S
커패시턴스……F
인덕턴스……H
시간……sec (s), min, hour (h)
주파수……Hz
배율……dB
위상각……degree
상대습도……%
온도……°C

이상을 기본으로 주요한 기호·약호를 열거합니다.

ACA : 1 信号選択度. (단위 dB)
AMR : AM 抑圧比. (단위 dB)
BW : 帯域幅. (단위 Hz)
c_i, c_o : 入出力容量. (단위 F)
$2f_{itweet}$: 笛音妨害比. (단위 dB, %)
g_i, b_i : 入力콘덕턴스, $y_i = g_i + jb_i$. (단위 S)
g_o, b_o : 出力콘덕탄스, $y_o = g_o + jb_o$. (단위 S)
I_{CC}, I_{DD} : 消費電流. (단위 A)
I_{CCO} : 無信号電流. (단위 A)
i_i, i_o : 入出力電流. (단위 A)
I_O : 増幅回路에 있어서의 出力電流. (단위 A)
I_{IH}, I_{IL} : 入力 H, L 레벨電流. (단위 A)
I_{OH}, I_{OL} : 出力 H, L 레벨電流. (단위 A)
I_L : 램프駆動電流. (multiplex IC). (단위 A)
I_n : 핀 n 에 흐르는 전류. (단위 A)
NF : 雑音指数. (단위 dB)
PBW : 出力帯域幅, 파우어밴드幅. (단위 Hz)
P_d : 付帯条件하에서 IC에 소비되는 전력. (단위 W)
$P_{d\ max}$: 許容消費電力. (단위 W)
PG : 電力利得. (단위 dB)
Q_S : 実用感度. (단위 dB, dB/m, V, V/m)
Sep. : 스테레오分離度. (단위 dB)
r_i, r_o : 入出力抵抗. (단위 Ω)
T_a : 周囲温度. (단위 °C)
T_c : 케이스温度. (단위 °C)
T_{opg} : 動作周囲温度. (단위 °C)
T_{stg} : 保存周囲温度. (단위 °C)
t_f : 下降時間. (단위 sec)
t_{stg} : 蓄積時間. (단위 sec)
t_{on} : turn on 時間 = 遅延時間 t_d + 上昇時間 t_r. (단위 sec)
t_{off} : turn off 時間 = 蓄積時間 t_{stg} + 下降時間 t_f. (단위 sec)
THD : 全高調波歪率. Total Harmonic Distortion. (단위없음, %)
V_{CC} : 電源電圧. (단위 V)
$V_{CC\ max}$: 最大電源電圧. (단위 V)
V_{DD}, $V_{DD\,max}$, V_{GG}, $V_{GG\,max}$: MOS IC 의 경우, 회로에 따라 V_{CC} 로 표시하지 않은 경우가 있지만, 이것은 전원을 걸리는 방법에 따라 구분하고 있어 모두다 전원전압을 의미합니다. (단위 V)
v_i, v_o : 入出力電圧. (단위 V)
V_{IH}, V_{IL} : 入力 H, L 레벨전압. (단위 V)
V_{OH}, V_{OL} : 出力 H, L 레벨전압. (단위 V)
V_L : 램프点灯레벨. (단위 V)
V_n : 핀 n 의 전압. (단위 V)
V_{m-n} : 핀 m 의 핀 n 에 대한 전압. (단위 V) I_{m-n} 도 동일하게 정의합니다.
V_{NO} : 出力雑音電圧. (단위 V)
VG : 電圧利得. (단위 V)
V_S : 最大感度. (단위 dB, dB/m, V, V/m)
$|y_f|$: 出力短絡順伝達어드미턴스. $y_f = |y_f| \exp(j\phi_f)$ (단위 S)

이것들 이외에, 接地 Gnd, 負荷抵抗 R_L, 信号対雑音比 S/N, AGC 電圧 V_{AGC}, 発振電圧 V_{OSC}, 発振電圧変動 ΔV_{OSC}, 入力 IN (또는 in, input 등), 出力 OUT (또는 out, output 등), 임피턴스素子 R, L, C, 時間単位 t 등 관용에 따라 있읍니다.

3. MAXIMUM RATINGS

3.1 Necessity and Meaning of Maximum Ratings

Because of the exponential dependence of the carrier density in a semiconductor device on temperature, integrated circuit function is significantly affected by temperature.

If a high voltage is applied to the PN junction in an integrated circuit, carriers receive energy and the cumulative multiplication of carriers may take place to cause electron avalanche, resulting in an abrupt voltage drop. Current does not cause such an abrupt change as caused by voltage, but may cause gradual changes in characteristics, whereby a semiconductor device becomes functionally useless; and further, power dissipation at the junction, i.e. the product of current and voltage, may be converted into thermal energy, thereby leading to thermal breakdown of the semiconductor device. Thus, voltage, current, power dissipation constitute important parameters which limit the operating functions of semiconductor devices.

It is necessary for the user to observe limiting values specified for voltage, current, power dissipation, and temperature applicable to any integrated circuit of a specified type. These limiting values are called "Maximum Ratings".

JIS C7030 (Testing Methods for Transistors) defines absolute maximum ratings as follows:

> Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any transistor device of a specified type as defined by its published data. These limiting values must not be exceeded under the worst probable conditions. The transistor device manufacturer chooses these values to guarantee normal operation of the device.

Maximum ratings for integrated circuits, though not yet defined by JIS, are defined by replacing the above-mentioned "transistor" by "integrated circuit". It should be noted, however, that when one rating reaches its maximum value another rating is not allowed to exceed its maximum value. For example, it is assumed that when current within its maximum allowable value is fed under unfavorable conditions where heat is removed less than intended the maximum power dissipation is exceeded. This is a wrong use of an integrated circuit because the maximum power dissipation is exceeded though current feeding involves no problem. Unconditional current feeding is not allowed even if such current does not exceed its maximum allowable value, and at the same time other maximum ratings must not be exceeded.

In determining maximum ratings, it is necessary to consider not only such properties of semiconductor chips as mentioned above but also structural material other than semiconductor chip itself, mold resin, chip soldering material.

For circuit design, thermal design of electronic equipment, it is strictly prohibited to use semiconductor devices in a state where absolute maximum ratings are exceeded. This is the first step toward using semiconductor devices properly.

3.2 Maximum Voltage Ratings

Integrated circuits have a lot of PN junctions. If voltage applied to the PN junction is increased, the cumulative multiplication of carriers attributable to high electric field in space charge layer of the junction may cause electron avalanche to occur, thereby resulting in a very large current flow that may break down the PN junction when the resistance of a limiting resistor is not large enough.

Avalanche multiplication factor M at the PN junction is given experimentally by Miller as follows:

$$M = \frac{1}{1 - (V_A/V_B)^n} \quad \ldots\ldots\ldots\ldots\ldots \quad (1)$$

where V_A : Applied voltage

V_B : Voltage at $M = \infty$, that is, V_B is the voltage at which electron avalanche causes collector current to flow on a large scale.

Maximum voltage ratings ($V_{GG\ max}$, $V_{DD\ max}$, etc.) specified on catalogs are generally fixed, with the variations in device characteristics considered, so that the voltage (especially drain voltage) at each PN junction does not exceed the above-mentioned V_B. Generally speaking, the larger the resistivity on the high-resistance side of the PN junction becomes, the higher V_B becomes.

Besides PN junction breakdown, if the polarity of the PN junction is reversed contrary to the de-

sign or a high voltage is applied to the field isolator that isolates internal elements (MOS transistor, etc.), forming a channel in the field area, a large current flow may occur in an unexpected region, resulting in breakdown of the integrated circuits. Latchup in C-MOS integrated circuits, being also in the same category as this phenomenon, causes internal parasitic thyristor to be turned on by external trigger voltage, holding large current and leading to breakdown of the integrated circuits.

Therefore, care should be taken that voltage having the opposite polarity from that specified must not be applied to the PN junction by the action of external pulse or through misoperation. Such voltage, even if applied, must not exceed 0.3V. This specific value may be specified on catalogs; but even if not specified, this rule must be observed. For input voltage or output voltage, there are some cases where this value on catalogs is with respect to V_{DD}, instead of GND. Channel formation in the field area and latchup in C-MOS integrated circuits are not expressly specified, but these phenomena can never occur as long as maximum voltage applied to each pin is observed.

MOS integrated circuits are such that channel current is controlled by applying voltage across gate and substrate or source. Silicon dioxide is mostly used for gate oxide. Normally, an electric field of approximately 10MV/cm, which differs with oxide thickness and quality (particularly, defect density), causes breakdown of this oxide (ex. 100V for an oxide thickness of 1000Å). Breakdown of the PN junction is caused by avalanche current, while breakdown of this oxide is caused instantly by corona discharge. According to the latest information, if voltage is applied for a long time even in a low electric field, breakdown may occur at a lower voltage. Surge voltage, even if its pulse width is small, can cause breakdown easily. Almost all the MOS integrated circuits developed recently contain a protector in the gate area and their data show that their breakdown strength is equal to that of bipolrar integrated circuits.

The above-mentioned leads to maximum voltage ratings of MOS integrated circuits defined below.

(1) Maximum supply voltage
$V_{DD\ max}$, $V_{GG\ max}$, $V_{CC\ max}$, $V_{SS\ max}$, etc.

(2) Maximum voltage on input/output pin
$V_{IN\ max}$, $V_{OUT\ max}$, etc. (May be defined by peak value.)

(3) Maximum voltage on pin

Designing so that these maximum voltage ratings are not exceeded involves no problem in practical use, even if no details of the internal circuit of a MOS integrated circuit are known to you.

3.3 Maximum Current Ratings

For maximum voltage ratings, a rather clear indication is available because an abrupt change in characteristics appears as mentioned in 3.2. For maximum current ratings, however, there is no such indication as breakdown caused by voltage. Normally, maximum current ratings are determined based on the following.

(1) Overcurrent at which internal bonding wire is burnt out

(2) Current with electromigration of evaporation wiring (normally, Al) on chip considered

(3) Current at which output transistor on-resistance causes internal power dissipation to exceed P_d max

(4) Current under which parasitic thyristor in chip is not latched up or turned on (Also definable by maximum voltage)

Designing, with the following maximum ratings on catalogs observed, involves no problem in practical use.

(1) Maximum output current $I_{OUT\ max}$

(2) Allowable current on specified pin
$I_{OL\ max}$

3.4 Maximum Temperature Ratings

(1) Junction temperature T_j

As mentioned above, integrated circuit operation is sensitive to temperature. As the temperature rises, thermal agitation of semiconductor crystal becomes violent and a large number of electron-hole pairs are generated by this energy. If electron-hole pairs are generated much more than minority carriers, the property of an intrinsic semiconductor results, thereby stopping the normal operation of a semiconductor device. The surface phenomenon of a semiconductor device affects semiconductor characteristics adversely; chemical change of the surface is also accelerated as the temperature rises. This is expressed by the well-known Arrhenius' equation as follows:

$$\exp^{(-E/kT_j)} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

where E: Activation energy
k: Boltzmann's constant
T_j: Junction temperature

It is very important to limit the temperature to which a semiconductor device is subjected. The allowable temperature differs with semiconductor's energy gap E_g; for silicon elements, a temperature of 150°C to 175°C is allowed. For the plastic molded type using silicon, however, the allowable temperature is normally limited to 125°C to 150°C because of the heat-resisting property of plastic.

The following relation between temperature T_j and life L of integrated circuits is known empirically.

$$\ln L = A + \frac{B}{T_j} \quad \text{(3)}$$

where A, B: Constant

(2) Storage temperature T_{stg} (min, max)

Junction temperature T_j in (1) is the temperature at which a semiconductor device can be safely operated. The temperature range in which a semiconductor device can be safely stored is specified as storage temperature T_{stg}.

A minimum storage temperature is specified so that the difference in thermal expansion coefficients at various areas in an integrated circuit causes no mechanical damage to the integrated circuit.

(3) Operating temperature T_{opg} (min, max)

Integrated circuit function, ex. the logic function of a MOS integrated circuit, can be guaranteed over this temperature range. However, operating characteristics specified at T_a = 25°C are not always guaranteed over this temperature range.

Guarantee for nonbreakdown depends on P_d, T_a mentioned below. Unlike P_d and T_a, T_{opg} provides guarantee for continuous operation.

3.5 Maximum Power Dissipation Rating

Power dissipation in an integrated circuit is converted into thermal energy, which raises junction temperature Tj. This means that it is necessary to limit power dissipation. Power dissipation and junction temperature are closely related with each other as shown below.

$$T_j = \theta P_d + T_a \quad \text{(4)}$$

where θ: Thermal resistance
P_d: Power dissipation
T_a: Ambient temperature or case temperature

T_j depends on both ambient temperature T_a and self-heat generation by power dissipation P_d; failure rate or life L almost entirely depends on T_j as shown in (3). Even if T_j remains the same, life L tends to be shortened when P_d accounts for a great deal. This is supposed to be due to the fact that an electric field is formed on the junction and ions remaining in the vicinity of the junction receive energy and move, which accelerates deterioration.

The maximum allowable power dissipation of our integrated circuits is determined as follows:

First, thermal resistance θ is measured and power dissipation P_d is calculated at which junction temperature T_j becomes 100°C to 150°C for epoxy resin molded integrated circuits. Then, a long operating life test is conducted based on this power dissipation. The maximum allowable power dissipation is determined from the results of this test.

The absolute maximum power dissipation rating is determined based on the following.

Absolute maximum ratings are limiting values which must not be exceeded even for a moment under the worst probable conditions to guarantee the characteristics and life of semiconductor devices. Our specifications for semiconductor devices specify the life assurance for using our semiconductor devices at absolute maximum ratings. In designing a circuit, the worst probable conditions of the following parameters should be considered and care should be taken that absolute maximum ratings must not be exceeded.

(1) Supply voltage regulation
(2) Variations in electrical characteristics of electrical parts (integrated circuits, transistors, resistors, capacitors, etc.)
(3) Maximum power dissipation of integrated circuit at the time of circuit adjustment
(4) Ambient temperature
(5) Variations in input signal
(6) Application of abnormal pulse

The maximum power dissipation rating is indicated on our catalogs as follows:

(1) $P_{d\ max}$
$P_{d\ max}$ is allowed at T_a.
(2) $P_{d\ (seg)\ max}$
Especially for Type Nos. with a driver, the

maximum segment output power is specified.

(3) No indication of $P_{d\ max}$
The maximum power dissipation is allowed when $V_{DD\ max}$, $V_{GG\ max}$, $V_{IN\ max}$, $V_{OUT\ max}$, etc. are applied at T_{opg}.

4. RELIABILITY

Electronics, in recent years, has been rapidly advanced into both industrial and commercial electric equipment fields and semiconductor devices occupy a major part of such apparatus. At the same time the requirements for electronics equipment has grown and diversified.

The highest priority must be given to product reliability and design and close attention paid to manufacturing processes. It is also important to achieve high performance and reliability of semiconductor devices in products under various environmental conditions.

This Chapter describes what reliability is and the reliability guarantee system of Sanyo Electric's semiconductor devices.

4.1 Definition of Reliability

The reliability of semiconductor devices is generally considered as use satisfaction, but this is a fairly subjective definition. More concretely, quantitatively, and objectively, it is better defined as the probability of performance capabilities expected of the devices under certain use and environmental conditions, in which the reliability is represented as a mathematical expression of probability.

The failure of electronics products is usually described with bathtub curves as shown in Fig. 4.1. When analyzing such distribution curves, it is convenient to approximate the failure distribution to the nearest distribution function. For example, these functions are often used in analysis:

1) Normal distribution function
2) Logarithmic normal distribution function
3) Exponential distribution function
4) Weibel distribution function

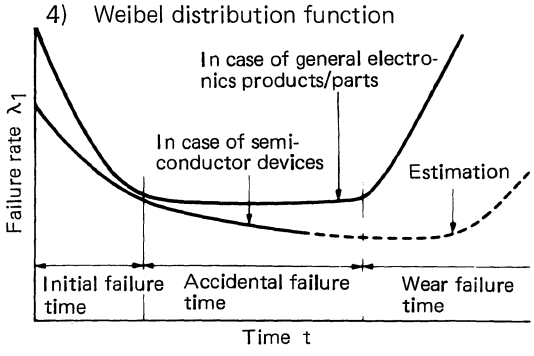


Fig. 4.1 Failure Rate Curves of Electronics Products/Parts and Semiconductor Devices

1) and 2) are used for wear failure time, 3) for accidental failure time, and 4) for any of initial, accidental or wear failure time.

4.2 Scales of Reliability

The following scales are used in general to express reliability:

N(0) . . Number of samples
N(t) . . Number of samples maintaining expected performance after t hours.
r(t) . . Number of failures after t hours.

(1) Survival rate (Reliability function) R(t)

$$R(t)=\frac{N(t)}{N(0)}=\frac{N(0)-r(t)}{N(0)} \quad \ldots\ldots\ldots\ldots (1)$$

(2) Cumulative failure rate (Life distribution function) F(t)

$$F(t)=\frac{r(t)}{N(0)}=\frac{N(0)-N(t)}{N(0)}=1-R(t) \quad \ldots\ldots (2)$$

(3) Failure generation rate (Failure density function) f(t)

$$f(t)=\frac{1}{N(0)}\times\frac{dr(t)}{dt}=\frac{dF(t)}{dt}=\frac{dR(t)}{d(t)} \quad \ldots\ldots\ldots (3)$$

(4) Instantaneous failure rate λ(t)

$$\lambda(t)=\frac{1}{N(t)}\times\frac{dr(t)}{dt}=\frac{f(t)}{R(t)}=\frac{d\ln R(t)}{dt} \quad \ldots\ldots (4)$$

Thus, it is possible to express functions 1), 2) and 3) as those of λ(t):

$$R(t)=\exp\left[-\int_{0-}^{t}\lambda(t)dt\right] \quad \ldots\ldots\ldots\ldots (5)$$

$$F(t)=1-\exp\left[-\int_{0}^{t}\lambda(t)dt\right] \quad \ldots\ldots\ldots (6)$$

$$f(t)=\lambda(t)\times R(t)=\lambda(t)\exp\left[-\int_{0}^{t}\lambda(t)dt\right] \quad \ldots (7)$$

(5) Average life μ

Suppose lives of samples are t_1, t_2, ...,

$$\mu=\frac{\sum_{i=1}^{N} ti}{N(0)}=\int_{0}^{t} t\,f(t)dt \quad \ldots\ldots\ldots\ldots (8)$$

Mean time between failures (MTBF) can also be represented with the same equation, which is in turn used to replace the defective part.

Neither instantaneous failure rate (λ(t)) nor average life (μ) is easy to estimate using test results

or actual data. Usually the following reliability index is used for estimation:

(6) Reliability index Ri

$$Ri=\frac{N(t)}{N(0)Xt} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (9)$$

This is generally represented with unit of % / 1,000 h, but sometimes

Fit (Failure Unit) = 10^{-9}/h

is used.

4.3 Weibel Probability Paper

Electric bulbs are known to be represented with an exponential relation

$$R(t)=\exp(-t/t_L)$$

where, R(t) is survival rate without failures versus time and t_L the average life of bulbs. However, this relationship is not always applicable to transistors. R(t) is then given by the following equation, and this R(t) is called the "Weibel function". m in these equations is determined from experimental data. The exponential function mentioned above is therefore given only when m=1.

$$R(t)=\exp(-t^m/t_0) \text{ (Reliability function)} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (10)$$

$$F(t)=1-R(t) \text{ (Cumulative distribution function)} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (11)$$

$$f(t)=m\frac{t^{m-1}}{t_0}\exp(-t^m/t_0) \text{ (Probability density function)} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (12)$$

$$\lambda(t)=\frac{f(t)}{R(t)}=m\frac{t^{m-1}}{t_0} \text{ (Instantaneous failure rate)} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (13)$$

where, t_0 : scale parameter

m : model parameter

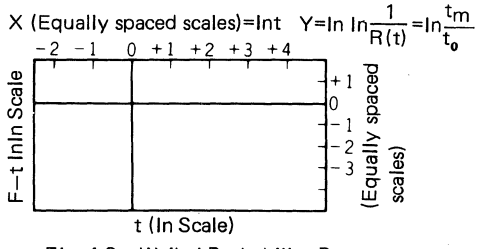


Fig. 4.2 Weibel Probability Paper

Failure distribution of semiconductor elements are plotted using the Weibel function. Weibel probability paper is useful for the plotting. Fig. 4.2 illustrates the structure of the Weibel paper.

Cumulative failure rate F(t) is entered on the probability paper as a function of time t. And by reading the chart, model parameter m and scale parameter t_0 are estimated.

In the chart shown in Fig. 4.2, slope between X=lnt and Y=[ln ln l/R(t)] is m, and lnln l/R(t) gives ln (l/t_0) where the curve cuts the y-axis (ln t=0), whereby, t_0 is found.

m is an important parameter in the Weibel distribution. Meaning of the values of m and the actual effects are described below. .

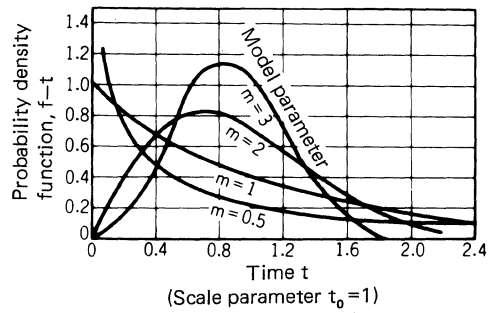


Fig. 4.3 Variation of Probability Density Function with Model Parameter

(1) Meaning of m values

i) m<1 Failure rate decreases with time (initial failure).

ii) m=1 Failure rate is constant regardless of time (accidential failure).

iii) m>1 Failure rate increases with time (wear failure).

See Fig. 4.3 for actual curves.

(2) When m in the chart on the Weibel probability paper changes midway it is assumed that the failure mechanism change at that point. This suggests that it is important in the accelerated life test not to change the m condition in acceleration or non-acceleration state.

(3) Acceleration ccefficient is defined as the proportion of instantaneous failure rate. Assuming λ(t) in equation (4) is a function of T_j, given

$$\lambda(t, T_j)=m(T_j)\frac{t^{m(T_j)^{-1}}}{t_0(T_j)} \quad \cdots\cdots\cdots\cdots \quad (14)$$

Then, acceleration coefficient $\rho(T_{j1}, T_{j2})$ concerning the joint temperature can be expressed by means of relation

$$\rho(T_{j1}, T_{j2}) = \frac{\lambda(t, T_{j2})}{\lambda(t, T_{j1})} = \frac{t_0(T_{j1})m(T_{j2})t^{m(T_{j2})-1}}{t_0(T_{j2})m(T_{j1})t^{m(T_{j1})-1}} \quad \cdots\cdots (15)$$

If $m(T_{j1})=m(T_{j2})$ in the above two terms, then

$$\rho(T_{j1}, T_{j2}) = \frac{t_0(T_{j1})}{t_0(T_{j2})} \quad \cdots\cdots (16)$$

Thus, the acceleration coefficient can be found from the Weibel probability paper.

(4) Mean time between failures (MTBF)

MTBF can be found from t_0 and m:

$$MTBF = t_0^{\frac{1}{m}} \Gamma(1+\frac{1}{m}) \quad \cdots\cdots (17)$$

(5) Failure rate of semiconductor devices tends to gradually decrease over thousands h with m changing in the order of 0.5 to 0.7 as far as there is no special stress applied.

4.4 Methods of Reliability Tests

As mentioned in the previous sections, Sanyo Electric uses an integrated product control system from designing and manufacturing processes to shipment and follow-up services to maintain the high quality and reliability of our semiconductor devices.

Test methods to confirm the reliability are described in this section. The methods are determined mainly observing JIS, JIS original form of EIAJ, MIL-STD, IEC, British Standard, and CECC, etc., and tests are conducted by laying particular stress in accelerated life testing at the maximum ratings.

(1) JIS (Japanese Industrial Standard)

JIS-C-5022	Test Methods for Heat-Resistance of Electronics Component Parts
JIS-C-5023	Test Methods for Moisture-Resistance of Electronics Component Parts (in stationary state)
JIS-C-5025	Test Methods for Vibration of Electronics Component Parts
JIS-C-5028	Methods of Brine Spraying Test for Electronics Component Parts
JIS-C-5031	Test Methods for Air-Tightness of Electronics Component Parts
JIS-C-5035	Test Methods for Terminal Strength of Electronics Component Parts
JIS-C-5036	Test Methods for Long-Term Electric Operation of Electronics Component Parts
JIS-C-5003	Test Methods for Failure Rate of Electronics Component Parts
JIS-C-5030	Test Methods for Temperature Cycle of Electronics Component Parts
JIS-C-5021	Test Methods for Cold-Resistance of Electronics Component Parts
JIS-C-5027	Test Methods for Low Temperature Preservation of Electronics Component Parts
JIS-C-5020	General Rules of Test Methods for Weather-Proofness and Mechanical Strength of Electronics Component Parts
JIS-C-7021	Methods of Enviornmental and Durability Tests for Individual Semiconductor Devices
JIS-C-7022	Methods of Environmental and Durability Tests for Semiconductor Integrated Cirucits
JIS-Z-2371	Methods of Brine Spraying Test

(2) MIL Standard

MIL-STD-750B	Test Methods for Semiconductor Devices
MIL-STD-202E	Test Methods for Electronics and Electric Component Parts
MIL-STD-883B	Test Methods and Procedures for Microelectronics

(3) IEC Standard

Publication 147-4 Publication 147-5	Essential ratings and characteristics of semiconductor devices and general principles of measuring methods

(4) British Standard

BS9400	Specification for Integrated Electronic Circuits of Assessed Quality: Generic Data and Methods of Test.

(5) CECC Standard

CECC 50000	Generic Specification: Discrete Semiconductor Devices.
CECC 90000	Generic Specification: Monolithic Integrated Circuits.

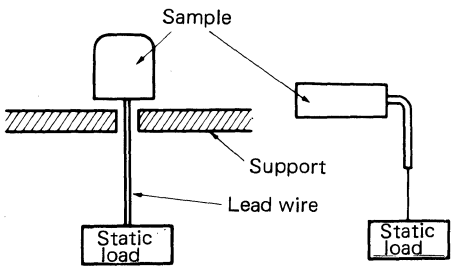
4.4.1 Mechanical tests

(1) Tensile test for lead-in wires

Test sample is held as shown in Fig. 4.4, and the specified static load (see below) is applied to each lead wire in the axial direction for 10±1 seconds. Each wire is then checked whether or not it falls out.

[Table 4.1]

Nominal Sectional Area mm^2	Nominal Wire Diameter (In case of circular section) mm	Load kg
0.05 or less	0.25 or less	0.1
more than 0.05 to 0.07 or less	more than 0.25 to 0.3 or less	0.25
more than 0.07 to 0.2 or less	more than 0.3 to 0.5 or less	0.5
more than 0.2 to 0.5 or less	more than 0.5 to 0.8 or less	1
more than 0.5 to 1.2 or less	more than 0.8 to 1.25 or less	2
more than 1.2	more than 1.25	4



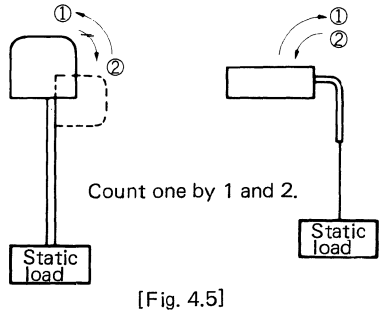
[Fig. 4.4]

(2) Fatigue test for lead wires

The test sample is held as shown in Fig. 4.5 and the specified static load is applied on each lead wire in the axial direction, and each is bent the specified number of times (twice) to check whether or not the wire falls out. One bending consists of folding the wire at right angles from the horizontal and the straightening of it again for about 5 sec. Each wire should be bent in the same direction on the same plane each time.

[Table 4.2]

Nominal Sectional Area mm^2	Nominal Wire Diameter (In case of circular section) mm	Load kg
0.05 or less	0.25 or less	0.05
more than 0.05 to 0.07 or less	more than 0.25 to 0.3 or less	0.125
more than 0.07 to 0.2 or less	more than 0.3 to 0.5 or less	0.25
more than 0.2 to 0.5 or less	more than 0.5 to 0.8 or less	0.5
more than 0.5 to 1.2 or less	more than 0.8 to 1.25 or less	1
more than 1.2	more than 1.25	2



[Fig. 4.5]

(3) Drop test

Test sample is allowed to drop from 100 cm height on a maple plate (30 by 30 cm, 3 cm min. thick) three times in such a way that it does not strike the plate with the lead wires. Specified check items are then inspected.

(4) Vibration fatigue test

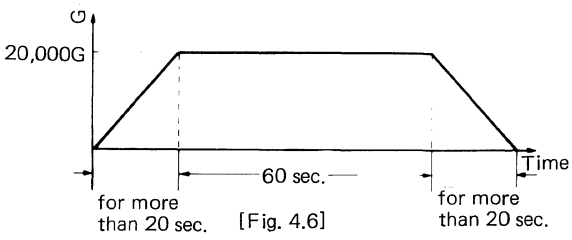
Test sample is fixed on the vibration plate of a vibration test device so as to transmit the generated vibration to the sample completely, and the vibration is applied under the following conditions to inspect the specified check items:

[Table 4.3]

Vibration Type	Frequency Variation
Frequency Range	10 to 2,000 Hz
Full Amplitude/ Acceleration	1.5 mm or 20G
Sweep Rate	10 to 2,000 to 10 Hz about 20 min
Variation of Sweep Frequency	Logarithm
Test Hours (Full)	2h each for X, Y, and Z

(5) Centrifugal acceleration test

Test sample is firmly fixed on the support of a centrifugal acceleration test device and applied with 20,000G of acceleration in three directions perpendicular to each other (X, Y, and Z directions), respectively for 60 sec (G: acceleration of gravity 9.8 m/sec^2). Specified check items are then inspected. The sample should be accelerated or decelerated for more than 20 sec to reach the specified level.



[Fig. 4.6]

(6) Impact test

Using an appropriate tool, the test sample is firmly fixed on an impact test device so that the impact from the test device completely is transmitted to the sample, and a 1,500G impact is applied to the sample in three direction perpendicular to each other (X, Y, and Z directions) three times, respectively. Damage to the sample is first checked, and then the specified check items are inspected.

4.4.2 Environmental tests

(1) Resistance to soldering heat test

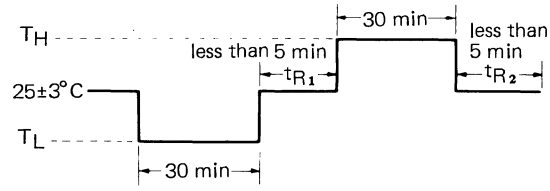
Without applying any flux, all lead wires of a test sample are subject to a solder bath (Sn 60% + Pb 40%) at 260±10°C for 10±1 sec as wire length of 1.0 to 1.5mm from the component remain in the solder bath. Removed from the solder bath, the sample is left at room temperature for more than 1h, and the specified check items are inspected.

(2) Solderability test

Applying a rosin flux on all lead wires of a test sample, the wires are subject to a solder bath (Sn 60% + Pb 40%) at 230±5°C for 5±0.5 sec as 1.0 to 1.5mm wire lengths from the component remain in the solder bath. These are removed and left as they are before the specified check items are inspected. If all lead wires cannot be dipped into the solder bath at once, it is allowed to dip them in turn.

(3) Temperature cycle test

The test sample is alternately put in a constat low temperature and constant high temperature containers. The sample should be preserved in each container long enough to reach the thermal equilibrium state. After 10 cycles are finished, the sample is left at room temperature for 2h, and the specified check items are inspected. T_H and T_L are the highest and lowest temperatures in absolute maximum rating T_{stg}.



[Fig. 4.7]

(4) Brine spraying test (Corrosion-resistance test)

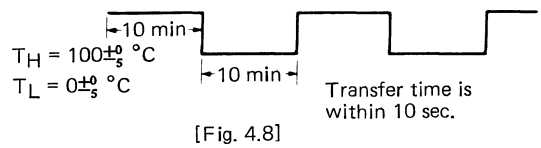
Test sample is subject to brine spraying for 24 ±2h, and washed completely with cool water at room temperature before the specified check items are inspected. The following conditions are applied to the brine spraying testing:

Condition 1 . . . . Brine concentration: 5±1%, internal temperature of container: 35±2°C

Condition 2 . . . . Brine spraying rate: specified amount of salt (10,000 to 50,000 mg/m^2/day) is deposited when 5±1% brine is sprayed.

(5) Thermal impact test

Test sample is alternately dipped in a low temperature liquid (ice and water) and a high temperature liquid (boiling water) — the latter is first applied. The time is as shown in Fig. 4.8. After 5 cycles are finished the sample is left at room temperature for 2h before the check items are inspected.



[Fig. 4.8]

(6) Pressure cooker test

Test sample is applied with 15 psi (Ta = 121°C) for the specified time (40h), and left at room temperature for 2h. Check items are then examined.

4.4.3 Life tests

(1) High temperature operation life test

Test sample connected to a specified external circuit is operated continuously at a specified temperature and supply voltage for 1,000h, and then left at room temperature for 2h before the check items are inspected.

(2) High temperature storage life test

Test sample is held at the highest storage temperature T_H of the absolute maximum rating for the specified time (1,000h), and left at room temperature for 2h. The check items are then inspected.

(3) Low temperature storage life test

Test sample is held at the lowest storage temperature T_L of the absolute maximum rating for the specified time (1,000h) and left at room temperature for 2h. The check items are then inspected.

(4) High temperature, high humidity storage life test

Test sample is stored for 1,000h at a temperature of 65±3°C and a relative humidity of 95±5% and left at room temperature for 2h. The specified check items are then inspected.

(5) High temperature, high humidity operation test

Test sample is operated for 500h at a temperature of 85±3°C and a relative humidity of 85±5% under the specified bias condition and left at room temperature for 2h. The specified check items are then inspected.

Bias Conditions:

Bias condition	ON/OFF condition
Reverse bias	Continuous
Forward bias	ON for 1 hour/OFF for 3h

5. QUALITY ASSURANCE SYSTEM

5.1 Introduction

As electronics products become larger and of higher density, the demands for high quality and reliability of semiconductor devices, used in such equipment, are increasing. To satisfy these user demands, Sanyo Electric pays close attention to market research, determination of user's requirements, product quality and reliability in development, design, and mass-production planning of semiconductor devices. At the same time, the selection of raw materials and parts is thoroughly discussed and evaluated from various aspects in terms of reliability. Standards for mass-production are determined after completely confirming the correctness of materials and parts.

At the mass production stage, every kind of control is used to maintain the quality intended for the design stage.

Particularly, stress is laid on product quality control through acceptance of raw materials and parts, the full manufacturing process, and final product inspection so that the final products meet the user's need.

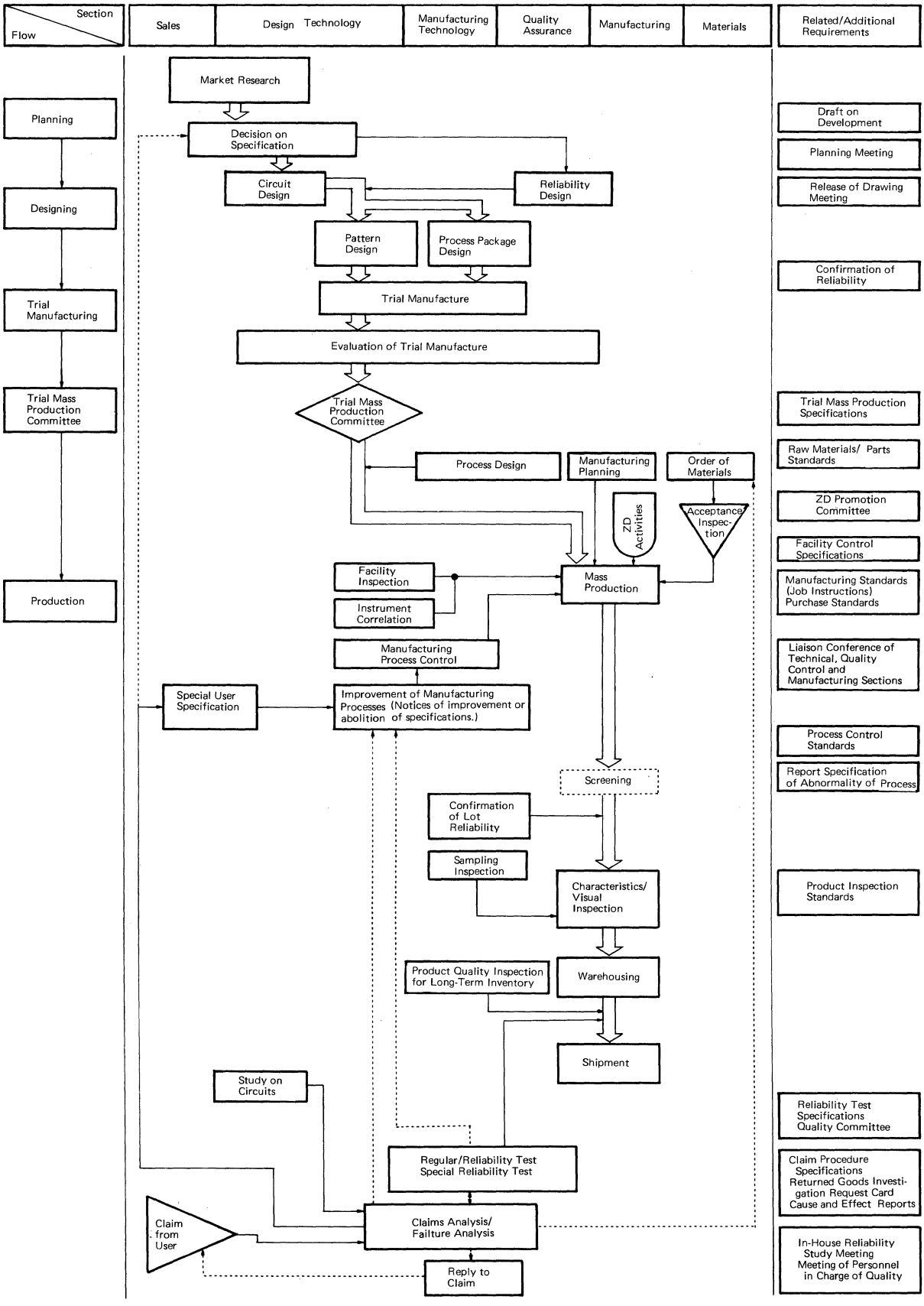
Sample inspection and reliability tests are also conducted at the shipping stage to insure the quality and reliability of all products. Information on the quality and reliability is most important to guarantee our semiconductor products after shipment, particularly for investigation of claimed defects by users or from the market place.

5.2 Quality Assurance System

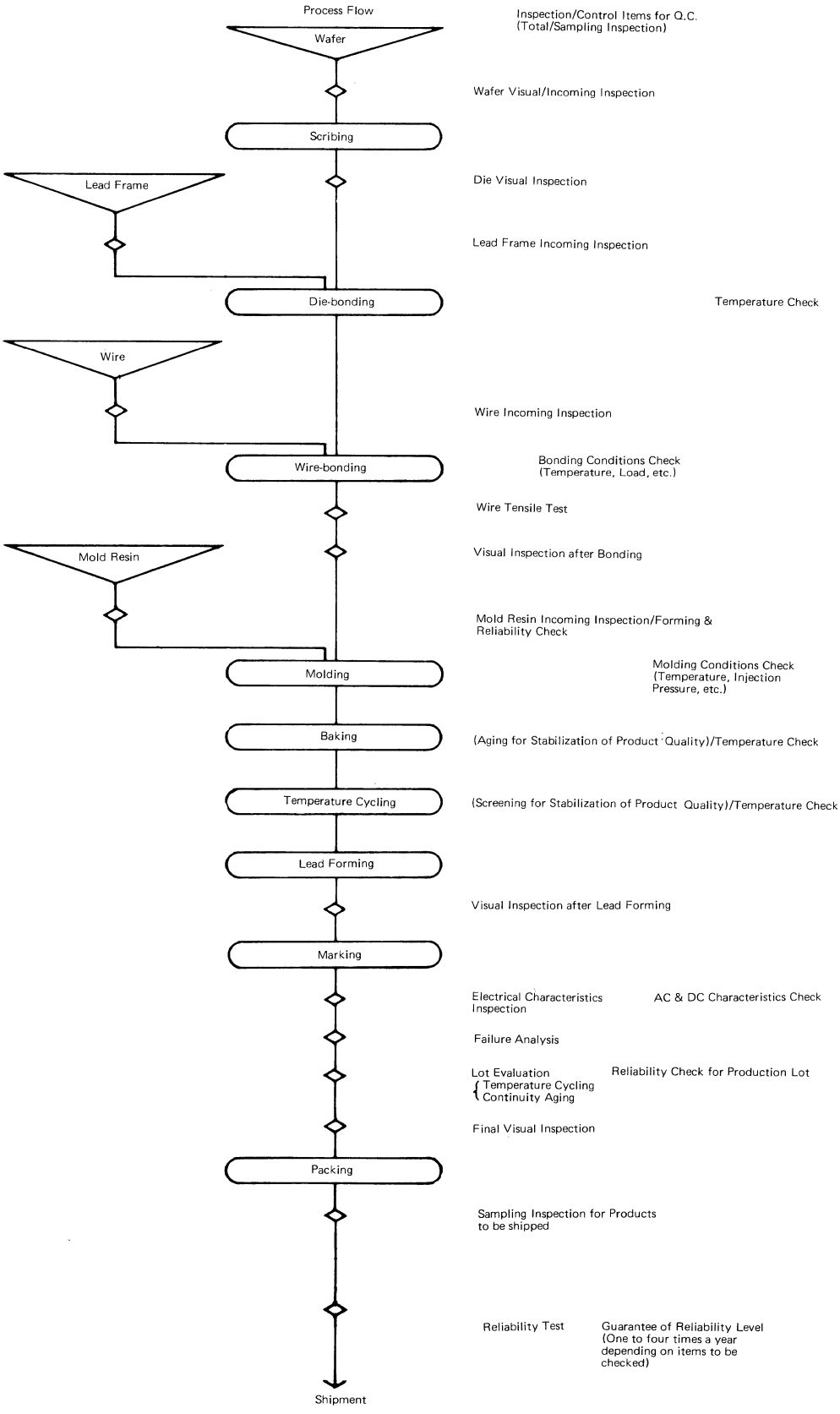
Sanyo Electric's quality assurance system as stated above is illustrated in Fig. 5.1.

5.3 Quality Control in Manufacturing Processes

Fig. 5.2 shows a flow chart of various inspection and control instnaces necessary for quality control during manufacturing.



[Fig. 5.1] Quality Assurance System

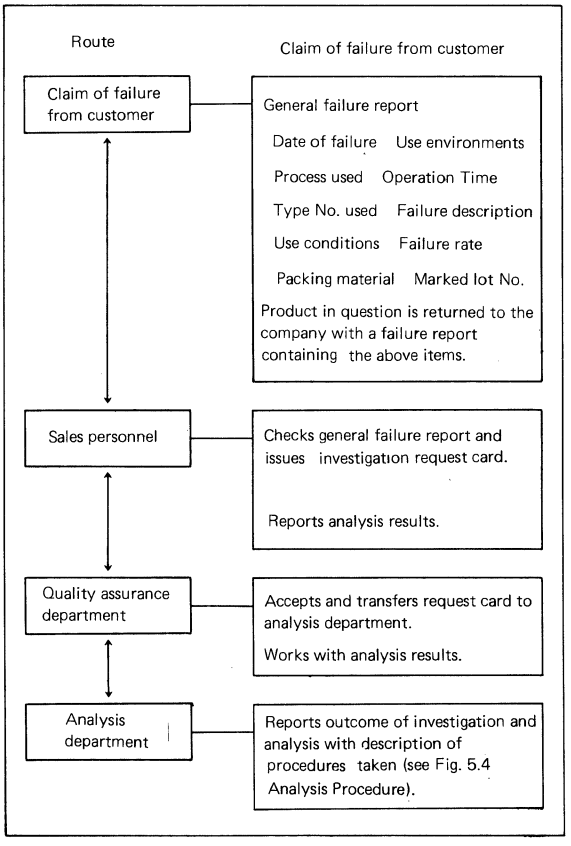

Process Flow
Inspection/Control Items for Q.C.
(Total/Sampling Inspection)
Wafer
Wafer Visual/Incoming Inspection
Scribing
Lead Frame
Die Visual Inspection
Lead Frame Incoming Inspection
Die-bonding
Temperature Check
Wire
Wire Incoming Inspection
Wire-bonding
Bonding Conditions Check
(Temperature, Load, etc.)
Wire Tensile Test
Mold Resin
Visual Inspection after Bonding
Mold Resin Incoming Inspection/Forming &
Reliability Check
Molding
Molding Conditions Check
(Temperature, Injection
Pressure, etc.)
Baking
(Aging for Stabilization of Product Quality)/Temperature Check
Temperature Cycling
(Screening for Stabilization of Product Quality)/Temperature Check
Lead Forming
Visual Inspection after Lead Forming
Marking
Electrical Characteristics
Inspection
AC & DC Characteristics Check
Failure Analysis
Lot Evaluation
Temperature Cycling
Continuity Aging
Reliability Check for Production Lot
Final Visual Inspection
Packing
Sampling Inspection for Products
to be shipped
Reliability Test
Guarantee of Reliability Level
(One to four times a year
depending on items to be
checked)
Shipment

[Fig. 5.2]

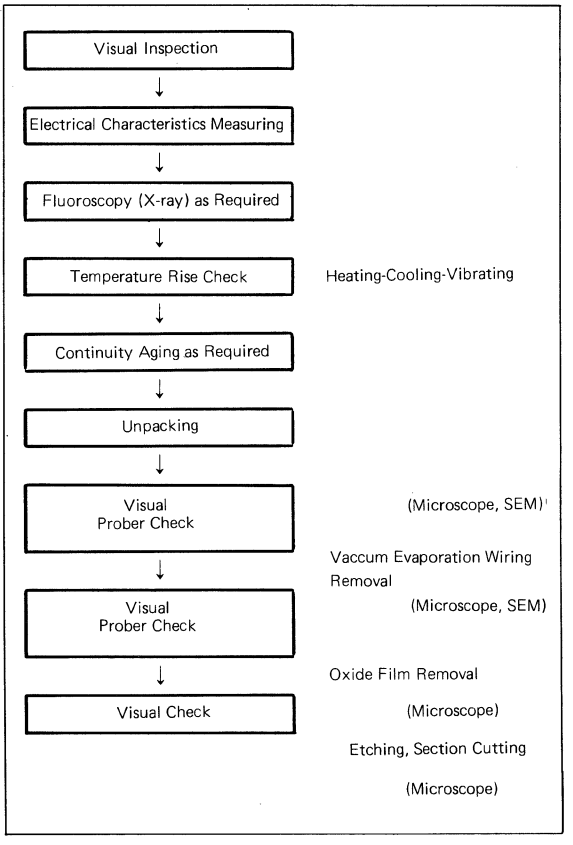
5.4 Failure Analysis

Analysis of product defects, found in the user's process or in the field, and in the manufacturing process or reliability testing at the factory, provides an important function to obtain information on, for example, failure modes and mechanisms, and by using it as feedback, to upgrade the quality and reliability of ICs. Based on this concept, Sanyo Electric handles user claims on defective products found during use or in the field as shown in Fig. 5.3.

Fig. 5.4 shows a typical failure analysis procedure used by semiconductor manufacturers. This is, however, only an example, and the procedure will vary depending on the failure mode or degree.



[Fig. 5.3] Detective Goods Handling Route



[Fig. 5.4] Failure Analysis Procedure

5.5 Failure Modes and Failure Factors

The reliability level of semiconductor ICs is lowered by failures. To find the cause of failures is, therefore, important to provide data for measures to be taken for increasing the reliability level.

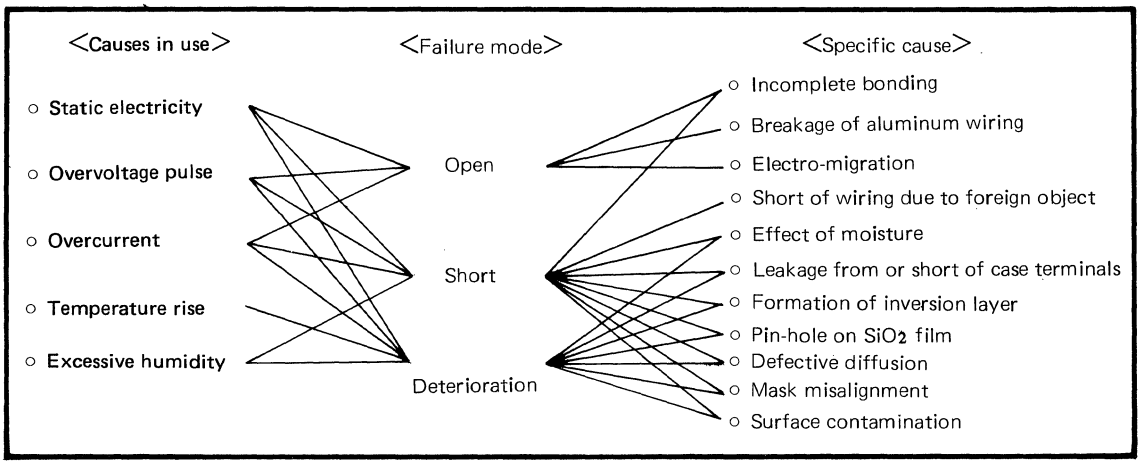
The failure modes of semiconductor ICs are roughly classified in the following three categories:

(1) Open wiring/connector
(2) Short of wiring/connection
(3) Deterioration, fluctuation of electrical characteristics

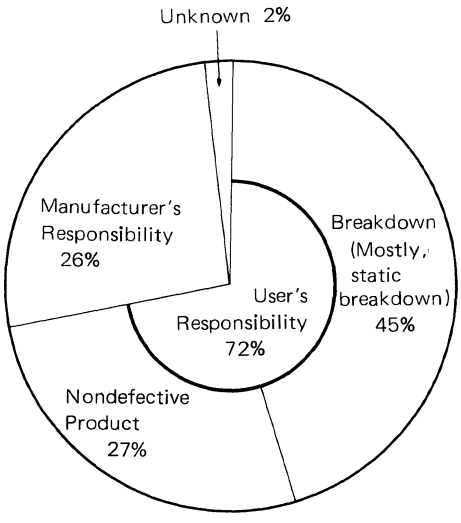
Relationship between these failure modes and causes is shown in Fig. 5.5.

The failure mechanism describes how the failure took place, and as shown in Fig. 5.5, various failure mechanisms such as chemical reaction, corrosion, alloying, thermal expansion, thermal contraction, etc. can be summarized in the three failure modes.

Fig. 5.6 gives an example of classification of defectives in semiconductor ICs found by the user, by factor. As the figure clearly shows, a considerable ratio of the failures is caused at the design or use stage.



[Fig. 5.5] Failure Modes and Causes



(December, 1982 to November, 1983)

[Fig. 5.6] Failure Factors in User Process

6. CAUTIONS FOR USING MONOLITHIC MOS IC

6.1 Shipping/Storage

(1) Never soak ICs in water or electro-conductive liquids. Do not use or leave ICs in high humidity or in an acidic gas environment.

(2) Use a metal box or wrap with aluminum foil for shipping the IC. Do not handle with gloves of vinyl or nylon. Keep mechanical vibrations and shocks as small as possible during shipping.

(3) Care should be taken in that moisture may condense on the IC if an excessive temperature change is encountered (e.g. by moving IC from a cold place to warm one).

(4) Do not expose the unsealed chips to direct sunlight at low temperature. The unsealed chips should be stored in a dust-free, nitrogenous gas environment.

6.2 Mounting

(1) Do not use as a terminal the pins which are not specified for the particular connection in the equivalent circuit diagram. Certain non-use pins are connected internally and wiring to a pin which looks free, or an actual free pin, may cuase trouble such as oscillation if used for a relaying terminal.

(2) Avoid unreasonable stress on the IC pins for print wiring. Allow sufficient clearance between the V_{DD}, V_{GG}, and V_{SS} lines and other input lines for high voltage-resistant ICs.

(3) Since most metal cased transistors have the casings connected to the collector, component layout which allows contact between an IC and a transistor may result in damaging the IC.

(4) Do not use a circuit tester to determine if an IC is "dead" or "alive".

(5) Do not bend the leads (especially for DIP = dual-in-line type).

(6) Be sure to observe correct mounting direction of the ICs when mounting on printed-circuit board. Applying power to a reverse mounted IC can damage it.

(7) Soldering should be performed as quickly as possible.

For dipping machine

. . . . . less than 10 seconds at 270°C

For soldering iron

. . . . . less than 4 seconds at 360°C

When the above conditions are difficult to satisfy, or for products for which high reliability is required, low melting-point solder should be considered. The same consideration must also be made for removing ICs from the printed-circuit board.

(8) When using the reflow method to solder ICs packaged in the miniflat or flat package, their reliability may be adversely affected if the resin part is allowed to stand at a high temperature for a long time. Therefore, soldering must be performed as quickly as possible to prevent the temperature of the resin part from rising. Since the use of an infrared heater may cause local temperature increase, avoid direct irradiation on the resin surface.

	Miniflat package (SOP)	Flat package
Reflow method	Less than 30 seconds at 260°C	Less than 10 seconds at 260°C
Solder dip method	Less than 10 seconds at 260°C	Unavailable

(9) Before soldering, check for no AC 100V leakage. If checking for AC leakage is not practicable:

- Ground the soldering iron. or
- Use a low voltage (6 to 10V) iron.

(10) Flux with strong acidity or alkalinity for soldering may result in corrosion on the IC leads or deterioration of electrical response.

The removal of residual flux by flushing is generally required after soldering to ensure system reliability. When the IC is used after being subjected to lead forming, contact us beforehand, because cleaning with flux may have some adverse effect on the reliability of the IC.

(11) After soldering, confirm that the IC leads have been soldered properly. Air spaces and cold solders may easily be mistaken for IC failure.

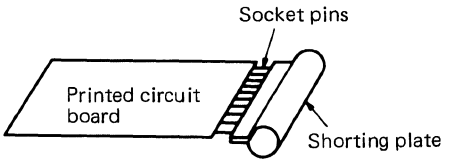
(12) Be careful of AC leakage to human bodies, test equipment, work bench, belt conveyor, etc. from electrical equipment. Charge prevention processed work benches and belt conveyors must be used.

(13) The humidity must be controlled in the

work room when static electricity is easily generated.

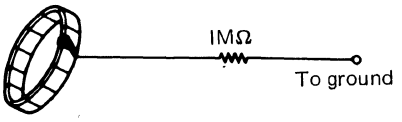
(14) An aluminum plate should be placed on the work bench when placing ICs on the work bench.

(15) The printed-circuit board socket pins must be shorted to the IC ground after mounting the IC, using a shorting plate.



[Fig. 6.1]

(16) The human body must be grounded by a metallic bracelet etc. When handling the IC.



[Fig. 6.2]

(17) The wiring arrangement and procedure must be made so as to avoid static electricity from affecting the IC.

6.3 Inspection/Measurement

(1) A sight check of the printed-circuit board for solder bridges and cold solders should be performed before applying power to the IC. Solder bridges and cold solders can damage the IC when power is applied.

The above problems are often detected before the IC is actually destroyed by applying power (V_{CC}) voltage gradually from low voltage to high, while observing the output and the power supply current etc.

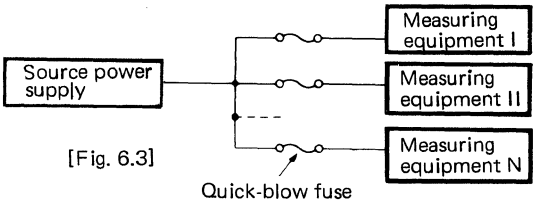
(2) Check for abnormal pulses when switching power supply, test equipment, etc. on/off.

Insert a surge-absorbing diode into the connection to the IC.

(3) Use care on the timing of applying power voltage to each IC terminal when turning the power on/off. Basically, the V_{CC} and Gnd terminals must be powered first. Failure to observe this may destroy the equivalent of the IC circuit, damaging the IC.

(4) The power supply for measurement should be equipped with a current limiter. Note that many ICs are destroyed by excessive current.

(5) When applying power for the test jigs in parallel, from a common power supply, each power line should be fused with quick-blow fuses.



[Fig. 6.3]

(6) If large-capacity capacitors are used in the V_{DD} line and output pins etc., care must be taken not to short out the IC pins just after turning off the power, or the IC may be damaged.

(7) Observe the following cautions when applying voltage to the IC:

(a) Do not check pin voltage more than necessary.
(b) Avoid plugging the IC in and out.
(c) Once voltage is applied, avoid soldering.

(8) Do not apply excessive voltage. The MOS ICs are high impedance elements and, although equipped with protection, special care must be taken against the impulse type abnormal voltage.

(9) The measurement jigs for the acceptance inspection should satisfy the measurement conditions of the specifications. Interchanging the correction sample is recommended.

6.4 Maximum Ratings and Allowable Operating Range

Actually, the maximum ratings for the monolithic IC are continuously guaranteed. However, unless otherwise specified, during the circuit design, the fundamental "the maximum ratings should never be exceeded even a moment" is followed.

An explanation of maximum ratings for monolithic ICs follows. Also, the relationship between 2 or 3 items which are necessary in designing circuits using ICs and the maximum ratings is clarified.

(1) Maximum power voltage $V_{DD\ max}$, $V_{GG\ max}$ Maximum supply voltage

The defective rate of the IC per 1000 hours for most ICs is less than 1% when the IC is continuously operated with the specified power voltage

and at ambient temperature which causes the chip temperature to be $T_{stg\ max}$. Data is provided with the categories for which it is helpful to provide such a data to estimate what happens when the supply voltage exceeds $V_{DD\ max}$ and $V_{GG\ max}$. However, such data is judged to be unnecessary for normal circuit design, and we again recommend that design be such that the supply voltage does not exceed $V_{DD\ max}$ and $V_{GG\ max}$ for even a moment.

(2) Storage temperature $T_{stg\ max}$, $T_{stg\ min}$

Continuous storage of ICs under this temperature condition will give a defective ratio for most categories of less than 0.5% per 1000 hours.

(3) Allowable power dissipation $P_{d\ max}$

$P_{d\ max}$ can be expressed in various ways in relation to the ambient temperature T_a and the heat sink. Certain ICs cannot actually accept the theoretically determined $P_{d\ max}$. In such a case, specifying $P_{d\ max}$ for an IC can be misleading.

The following various cases relate the $P_{d\ max}$ indication of monolithic ICs:

(a) When $P_{d\ max}$ is not specified:

This situation covers most ICs which have almost no power dissipation in the normal use. Any maximum ratings, such as $V_{DD\ max}$ and $V_{GG\ max}$, maximum supply current etc., can be applied without using a heat sink and at the maximum operating temperature.

(b) When only $P_{d\ max}$ is specified:

Unless the particular T_a is not specified, up to $P_{d\ max}$ can be applied at the maximum operating temperature. When a specific T_a is given, it is self-explanatory that the P_d can be applied until the temperature reaches T_a. The temperature at the IC chip will be equal to $T_{stg\ max}$ when $P_{d\ max}$ is applied at T_a estimated above, except for case (a).

Defective ratio for most categories will be less than 1% per 1000 hours when the IC is continuously operated with the chip temperature at $T_{stg\ max}$.

(4) Operating temperature $T_{opg\ max}$, $T_{opg\ min}$

This term has a slightly different nuance than other kinds of maximum ratings. Operating the IC within this temperature range, and within the suggested or allowable operating range (as described later) can guarantee the minimum circuit functions, (such as logic function) though the expected operation response at $T_a = 25°C$ is not guaranteed. In other words, the operating temperature affects guaranteeing the circuit function, and does not guarantee the operation response.

(5) Other maximum ratings

Ratings without the time-limitation specified are continuously guaranteed.

(6) Allowable operating range

The allowable operating range mainly applies to digital ICs. An excess of this limit prevents the logic operation which is the inherent circuit function of the digital IC. However, the expected logic operation can be guaranteed with any values within the allowable operating range at the operating temperature specified.

6.5 Circuit Design

In the actual design process, consider the effect from the following parameters. Each term described in section "2" must not exceed the applicable maximum ratings.

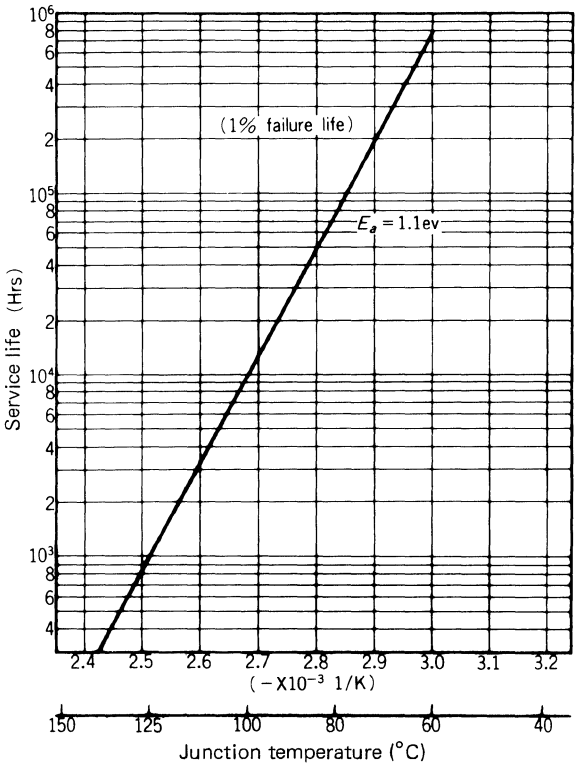
- Supply voltage fluctuation
- Electrical variations of electrical components (ICs, resistors, capacitors, etc.)
- Ambient temperature
- Input and clock signals fluctuation
- Abnormal pulse spikes

ICs with the allowable operating range specified must be operated within that range.

6.6 Derating

Derating (load reduction) is defined as operating a component under specifications below the specific maximum rating, thus reducing the electrical or mechanical stress on the component, for extended service life and lowered defective ratio. The kind of electrical stress subject to derating are voltage, current, junction temperatures, power loss, and the mechanical stress is vibration, impact and stretch, etc.

In the actual design procedure, we recommend keeping these factors as low as possible. Figure 6.4 shows an example of the relationship between the junction temperature and the service life of an IC for an operation test.



[Fig. 6.4] Accelerated operation test

6.7 Noise Margin and Others

(1) Since the MOS IC is a high impedance element, care should be taken regarding impulsive noises entering the signal line of the IC.

The effect attributable to impulsive noises can be minimized by making the V_{DD}/V_{SS} line pattern wide. Especially, make the pattern wider for a large current flow in the V_{DD}/V_{SS} line.

(2) For CMOS ICs, do not apply voltage higher than V_{DD} and voltage lower than V_{SS} to the input/output pins, or a latch-up phenomenon will be caused.

(3) In applications where a capacitor is connected across IC output and GND, this capacitor is charged when the output is at "H" level and is discharged through an output transistor on the IC when the output is at "L" level. Therefore, be careful that too large a capacitor value may cause excessive current to flow instantaneously, resulting in the deterioration of the IC.

MICROCOMPUTERS

- **Pin Numbering**

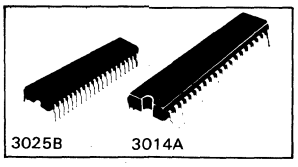
When you face the top side (marking side) of the package, numbering starts with ① assigned to the pin located, in a counterclockwise direction, immediately after the index point and turns counterclockwise.

MICROCOMPUTER LINEUP

				Type No.	ROM	RAM (Bits)	Stacks	Cycle Time	IDD	Port: Max. Voltage	Port: Max. Current	Function: Interrupt: Internal	Function: Interrupt: External	Function: Serial I/O	Function: Timers	Function: Instructions	Function: Power-down	Package	Remarks
Single Chip	4 Bits	N-MOS	Basic Type	LM6402A	2K bytes	128×4	4	10/sec	30mA	15V	40mA	1	1	—	1	82	—	DIP-42	
				LM6405A	1K	64×4												DIP-42S	
			Medium-Speed Type	LM6402H	2K	128×4	4	5	35	15	40	1	1	—	1	82	—	DIP-42	
				LM6405H	1K	64×4												DIP-42S	
			High-Speed Type	LM6402G	2K	128×4	4	3	38	15	50	1	1	—	1	82	—	DIP-42	
				LM6405G	1K	64×4												DIP-42S	
			Low-Power Type	LM6402L	2K	128×4	4	20	10	12	40	1	1	—	1	82	—	DIP-42	
				LM6405L	1K	64×4												DIP-42S	
			Economy Type	LM6413E	2K	128×4	2	4	17	15	20	—	—	—	1	65	—	DIP-28S	
				LM6416E	1K	64×4												DIP-28S	
				LM6417E	1K	64×4												DIP-22	
		C-MOS	Basic Type	LC6502C	2K	128×4	4	10	0.5	5	2	1	1	—	1	79	With	DIP-42 DIP-42S QIP-64	
				LC6505C	1K	64×4													
			High-Voltage Type	LC6502B	2K	128×4	4	10	0.5	High voltage	10	1	1	—	1	79	With	DIP-42	FLT direct drivable
				LC6505B	1K	64×4					2							DIP-42S	
			High-Performance Type	LC6514B*	4K	256×4	8	5	1	High voltage	10	1	1	—	1	80	With	DIP-42	FLT direct drivable
				LC6510C*	4K	256×4				5	2							DIP-42S	
				LC6515B*	4K	256×4	8	5	1	High voltage	10	1	1	—	1	80	With	DIP-42	FLT direct drivable Timepiece backup available
				LC6511C*	4K	256×4				5	2							DIP-42S	Timepiece backup available
			Economy Type	LC6523C*	2K	128×4	4	3	1.5	15	20	1	1	With	1	79	With	DIP-30S	
				LC6526C*	1K	64×4								With					
				LC6527C*	1K	64×4						—		—	1	51	With	DIP-18	
				LC6528C*	0.5K	32×4						—		—					
			Low-Voltage Type V_{DD}1.5V or 3.0V	LC5700N	1.39K×14 bits	84×4	8	420	3μA	—	—	4	—	—	1	71	With	Chip (QIP-64)	LCD direct drivable (98 segments)
				LC5800	2K×16	152×4	8	244 122	3μA	—	—	3	1	—	1	121	With	Chip (QIP-80)	LCD direct drivable (126 segments) Low-current I/O:20 in all
				LC5812*	2K×16	152×4	8	50	30μA	—	—	3	1	—	1	132	With	Chip (QIP-80)	LCD direct drivable (126 segments) Low-current I/O:20 in all
				LC5850	1K×15	64×4	4	244 122	3μA	—	—	2	1	—	1	78	With	Chip (QIP-64)	LCD direct drivable (75 segments) Low-current I/O:22 in all
	8 Bits	N-MOS		LM8051*	4K bytes	128×8	64 (RAM)	1	125mA	7	3.2	3	2	With	2	111	With	DIP-40	External ROM, RAM available
				LM8854*	4K	256×8	16	1	60	15	30	2	2	With	2	101	With	DIP-64S	
				LM8804*	4K	256×8	16	1	60	15	30	2	2	With	2	101	With	DIP-42S	
				LM8852*	2K	128×8	16	1	60	15	30	2	2	With	2	101	With	DIP-64S	
				LM8802*	2K	128×8	16	1	60	15	30	2	2	With	2	101	With	DIP-42S	
Multi Chip	16 Bits	N-MOS		LM8086*	—	—	—	0.6	360	—	—	2		—	—	133	Without	DIC-40	
				LM8088*	—	—	—	0.6	350	—	—	2		—	—	133	Without	DIP-40	

* : Under development

LM6402A, 6405A



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer

Ⓔ 1020B

OUTLINE

LM6402A and 6405A are N-channel MOS 4-bit microcomputers with ROM, RAM, ALU, I/O ports, timer, and clock generator, built on a single chip. The microcomputer, for control applications, has a ROM memory with a maximum capacity of 2K bytes, a RAM with 128 x 4 bits, I/O ports with 35 terminals, and internal PLA.

1) Hardware features (reduction in externally connected component parts)
   * An N-channel E/D MOS for a single 5 V power supply
   * C MOS and TTL compatible
   * LED driver output ports (2 ports/8 pins)
   * 24 character PLA
   * Dual purpose I/O ports (7 ports/27 pins)
   * Flexible output (open drain/with pull-up resistors)
   * Clock oscillator (with externally connected ceramic oscillating element)
   * Cycle time 10 μs
   * 1K byte/2K byte pin compatible
   * Programmable input threshold voltages (normal/high thresholds)
   * Initial reset and external interrupt input terminals containing Schmitt gate at external.

2) Software features (effective utilization of ROM capacity)
   * 4-level subroutine nesting feasible
   * Interrupt functions (external/internal)
   * Builtin programmable timer capable of a wide range of designations (timer, pulse count, and pulse width measure)
   * A rich variety of instructions of 82 kinds
   * Automatic page select
   * 1K byte/2K byte instruction compatible

Note: The LM6400 series is structured in the following way to permit optimum usage.

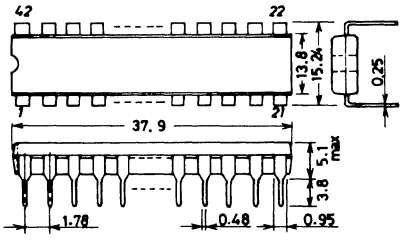
Model	Application	ROM	RAM	Cycle time	I_{DD} (typ)	Package	Remarks
LM6402A	General use	2K bytes	128 x 4 bits	10 μs	30 mA	DIP-42 DIP-42S	
LM6405A	General use	1K bytes	64 x 4 bits	10 μs	30 mA	DIP-42 DIP-42S	
LM6402H	Medium speed use	2K bytes	128 x 4 bits	5 μs	35 mA	DIP-42 DIP-42S	
LM6405H	Medium speed use	1K bytes	64 x 4 bits	5 μs	35 mA	DIP-42 DIP-42S	
LM6402L	Low power consumption use	2K bytes	128 x 4 bits	20 μs	10 mA	DIP-42 DIP-42S	
LM6405L	Low power consumption use	1K bytes	64 x 4 bits	20 μs	10 mA	DIP-42 DIP42S	
LM6416E	Small scale use	1K bytes	64 x 4 bits	4 μs	17 mA	DIP-28S	

— Continued on next page

For details, refer to LM6400 Series User's Manual.

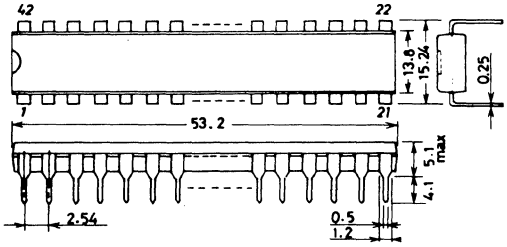
Model	Application	ROM	RAM	Cycle time	I_{DD} (typ)	Package	Remarks
LM6499	Evaluation chip for LM6402A, H, L and LM6405A, H, L	Externally connected 2K bytes		5 ~ 10 μs	30 mA	QIC-80	
LM6497	Evaluation chip for LM6416E	Externally connected 2K bytes		4 μs	20 mA	QIC-80	

Case Outline 3025B-D42SIC
(unit : mm)



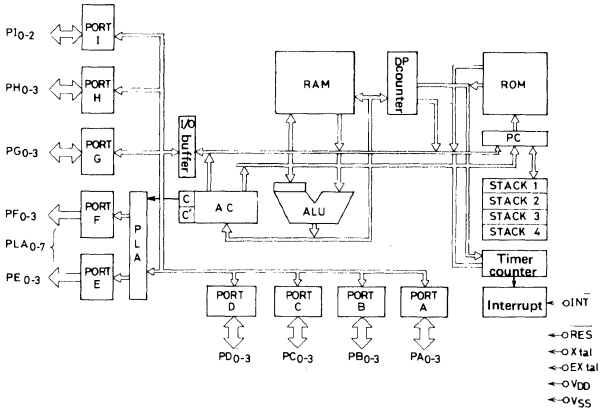
SANYO: DIP42S

Case Outline 3014A-D42IC
(unit : mm)

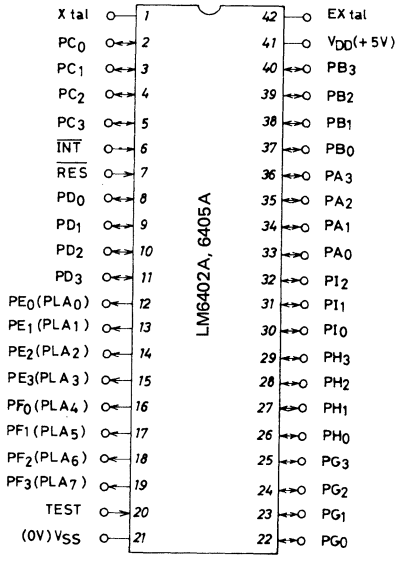


SANYO: DIP42

System block diagram [LM6402A, 6405A]



Package and terminal names



Terminal name		
Xtal, EXtal:	Oscillating element for OSC	
$\overline{INT}$:	Interrupt	
$\overline{RES}$:	Reset	
PA_{0-3}:	Input/output ports A_{0-3}	
PB_{0-3}:	Input/output ports B_{0-3}	
PC_{0-3}:	Input/output ports C_{0-3}	
PD_{0-3}:	Input/output ports D_{0-3}	
PE_{0-3} (PLA_{0-3}):	Output ports	E_{0-3} (PLA outputs$_{0-3}$)
PF_{0-3} (PLA_{4-7}):	Output ports	F_{0-3} (PLA outputs$_{4-7}$)
PG_{0-3}:	Input/output ports G_{0-3}	
PH_{0-3}:	Input/output ports H_{0-3}	
PI_{0-2}:	Input/output ports I_{0-2}	
TEST:	Test	

Terminal functions

Terminal name	Input/output	Functions
$\overline{INT}$	Input	Interrupt request input terminal.
$\overline{RES}$	Input	Reset input terminal.
$PA_{3\text{-}0}$	Input Input/output (Note 1)	Input/output ports A_3-A_0. During input, can provide 4-bit input and single-bit test. During output, can provide 4-bit output and single-bit set and reset.
$PB_{3\text{-}0}$	Input Input/output (Note 1)	Input/output ports B_3-B_0. During input, can provide 4-bit input and single-bit test. During output, can provide 4-bit output and single-bit set and reset.
$PC_{3\text{-}0}$	Input/output	Input/output ports C_3-C_0. During input, can provide 4-bit input and single-bit test. During output, can provide 4-bit output, single-bit set and reset, and immediate data output.
$PD_{3\text{-}0}$	Input/output	Input/output ports D_3-D_0. During input, can provide 4-bit input and single-bit test. During output, can provide 4-bit output, single-bit set and reset, and immediate data output.
$PE_{3\text{-}0}$	Output	Output ports E_3-E_0. Can provide 4-bit output and single-bit set and reset. PLA outputs are fed from this terminal and $PF_{3\text{-}0}$.
$PF_{3\text{-}0}$	Output	Output ports F_3-F_0 Can provide 4-bit output and single-bit set and reset. PLA outputs are fed out from this terminal and $PE_{3\text{-}0}$.
$PG_{3\text{-}0}$	Input Input/output Output (Note 1)	Input/output ports G_3-G_0. During input, can provide 4-bit input and single-bit test. During output, can provide 4-bit output and single-bit set and reset.
$PH_{3\text{-}0}$	Input Input/output Output (Note 1)	Input/output ports H_3-H_0. During input, can provide 4-bit input and single-bit test. During output, can provide 4-bit output and single-bits set and reset.
$PI_{2\text{-}0}$	Input/output	Input/output ports I_2-I_0. During input, can provide 3-bit input and single-bit test. During output, can provide 3-bit outputs and single-bit set and reset.
Xtal	Input/output	Terminal for external connection of resonant circuit for internal clock oscillation. Connect a ceramic, resonator across this terminal and Extal terminal.
EXtal	Input	Terminal for supplying external clock. When employing internal clock oscillation, connect a ceramic, resonator or across this terminal and Extal terminal.
V_{DD}	Input	Power supply terminal: Normally connected to +5 V.
V_{SS}	–	Connect to 0 V of power supply.
TEST	Input	LSI test terminal: Normally connect to V_{SS}(0 V).

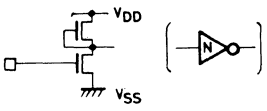
(Note 1): Mask programming can be used to designate input, input/output, or output.

Input/output designation table

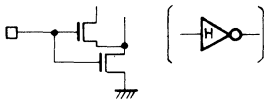
Option \ Port	A	B	C	D	E	F	G	H	I
Input dedicated	N H	N H					N H	N H	
Output dedicated					OD	OD	OD PU	OD PU	
Input/output common	N, OD H, OD	N, OD H, OD	N, OD N, PU H, OD H, PU	N, OD N, PU H, OD H, PU			N, OD N, PU H, OD H, PU	N, OD N, PU H, OD H, PU	N, OD H, OD

N: Normal input gate
H: High-threshold input gate
OD: Open-drain output
PU: Pull-up resistor equipped output

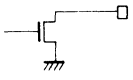
Input-dedicated normal input gate (N)



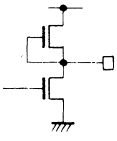
Input dedicated, high-threshold input gate (H)



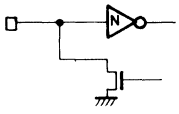
Output dedicated open-drain output (OD)



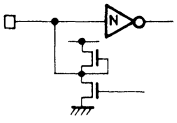
Output dedicated pull-up resistor output (PU)



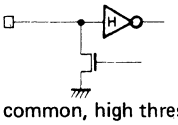
Input/output common, normal input, open-drain output (N, OD)



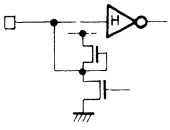
Input/output common, normal input, pull-up resistor output (N, PU)



Input/output common high-threshold input, open-drain output (H, PU)

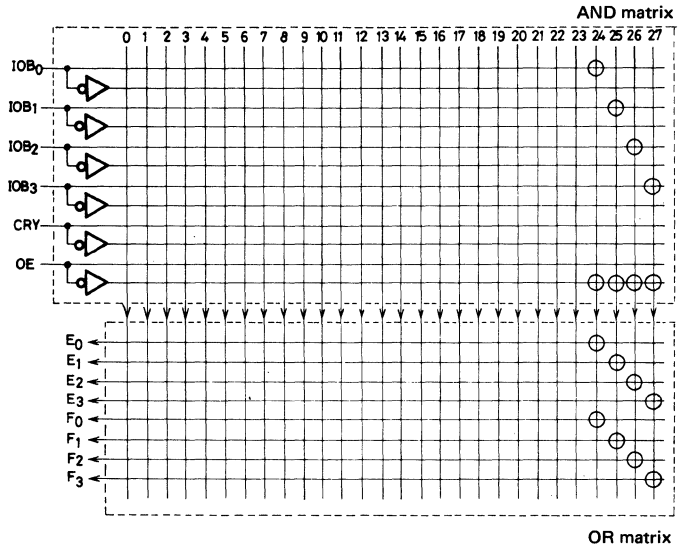


Input/output common, high threshold input, pull-up resistor output (H, PU)



PLA for E and F ports

User-designated mask programmable



ABSOLUTE MAXIMUM RATINGS/T_a = 25°C, V_{SS} = 0 V			min	max	unit
Maximum power-supply voltage	V_{DD} max		−0.3	+10	V
Input voltage	V_{IN}		−0.3	+12	V
Output voltage	V_{OUT} (1)	When output transistors are off	−0.3	+12	V
Average output current	I_{OHA}	for each pull-up spec terminal	−2.0	0	mA
(to be applied to any 100 ms period)	I_{OLA} (1)	total of all terminals in C and D ports	0	20	mA
	I_{OLA} (2)	for each terminal in E and F ports	0	40	mA
	I_{OLA} (3)	total of either E or F port	0	100	mA
	I_{OLA} (4)	total of all terminals in A, B, G, H, and I ports	0	50	mA
Peak output current	I_{OHP}	for each pull-up spec terminal	−2.0	0	mA
	I_{OLP} (1)	for each output terminal in other than E and F ports	0	4	mA
	I_{OLP} (2)	for each terminal in E and F ports	0	40	mA
	I_{OLP} (3)	total of either E or F port	0	100	mA
Allowable power dissipation	P_d max	T_a = −30 ~ +70°C		600	mW
Operating temperature	T_{opg}		−30	+70	°C
Storage temperature	T_{stg}		−55	+125	°C

RECOMMENDED OPERATING CONDITIONS/T_a = −30 ~ +70°C, V_{SS} = 0 V				min	typ	max	unit
Recommended power supply voltage		V_{DD}		4.5	5.0	5.5	V
Normal input specs for input-dedicated port and input/output common port	(H) level input voltage	V_{IH} (1)	Input/output style "N" "N, OD" "N, PU"	2.2		V_{DD}	V
	(L) level input voltage	V_{IL} (1)	Input/output style "N" "N, OD" "N, PU"	V_{SS}		0.6	V
High threshold input specs for input dedicated port and input/output common port	(H) level input voltage	V_{IH} (2)	Input/output style "H" "H, OD" "H, PU"	0.6V_{DD}		V_{DD}	V
	(L) level input voltage	V_{IL} (2)	Input/output style "H" "H, OD" "H, PU"	V_{SS}		0.25V_{DD}	V

				min	typ	max	unit
$\overline{INT}$, $\overline{RES}$	(H) level input voltage	V_{IH} (3)		$0.7V_{DD}$		V_{DD}	V
	(L) level input voltage	V_{IL} (3)		V_{SS}	$0.25V_{DD}$		V
EXtal	(H) level input voltage	V_{IH} (4)		$0.7V_{DD}$		V_{DD}	V
	(L) level input voltage	V_{IL} (4)		V_{SS}		0.6	V
	Clock cycle time	$t_c(\phi)$	V_{DD} = 5 V ± 10% Refer to Fig. 1	2.4		2.6	μs
	(H) level clock pulse width	$t_{w\phi H}$	V_{DD} = 5 V ± 10 % Refer to Fig. 1	0.8			μs
	(L) level clock pulse width	$t_{w\phi L}$	V_{DD} = 5 V ± 10 % Refer to Fig. 1	0.8			μs
Externally-connected resistor value for oscillation		R	Refer to Fig. 2		1000		kΩ
Externally-connected capacitor value for oscillation		C_1	Refer to Fig. 2		220		pF
		C_2	Refer to Fig. 2		220		pF
TEST	(L) level input voltage	V_{IL} (6)	V_{DD} = 5 V ± 10%	V_{SS}		0.4	V

Refer to "Input/output designation table" for "N", "H" "N, OD" "N, PU" "H, OD" "H, PU"

ELECTRICAL CHARACTERISTICS/T_a = −30 ~ +70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

				min	typ	max	unit
Input dedicated port and $\overline{RES}$	(H) level input current	I_{IH} (1)	Input/output style "N" "H" V_{IN} = V_{DD}			10	μA
	(L) level input current	I_{IL} (1)	Input/output style "N" "H" V_{IN} = V_{SS}	−10			μA
Input/output common port with open-drain spec output	(H) level input current	I_{IH} (2)	Input/output style "N, OD" "H, OD" V_{IN} = V_{DD}			10	μA
	(L) level input current	I_{IL} (2)	Input/output style "N, OD" "H, OD" V_{IN} = V_{SS}	−10			μA
Input/output common port with pull-up spec output	(L) level input current	I_{IL} (3)	Input/output style "N, PU" "H, PU" V_{DD} = 5 V ± 10% V_{IN} = 0.4 V	−1.6			mA
Pull-up specs for output dedicated or input/output common port	(L) level output voltage	V_{OL} (1)	Input/output style "PU" "N, PU" "H, PU" I_{OL} = 1.6 mA			0.4	V
	(H) level output voltage	V_{OH} (1)	Input/output style "PU" "N, PU" "H, PU" I_{OH} = −50μA	$0.8V_{DD}$		V_{DD}	V
		V_{OH} (2)	Input/output style "PU" "N, PU" "H, PU" I_{OH} = −80μA	$0.66V_{DD}$		V_{DD}	V
		V_{OH} (3)	Input/output style "PU" "N, PU" "H, PU" I_{OH} = −100μA	$0.48V_{DD}$		V_{DD}	V

				min	typ	max	unit
Open drain specs for output dedicated or input/output common port	(L) level output voltage	V_{OL} (2)	Input/output style "OD" "N, OD" "H, OD" I_{OL} = 1.8 mA			0.4	V
	Output-off leakage current	I_{OFF} (1)	Input/output style "OD" "N, OD" "H, OD" V_{OH} = 10 V			30	μA
		I_{OFF} (2)	Input/output style "OD" "N, OD" "H, OD" V_{OH} = 5.5 V			10	μA
E and F ports	(L) level output voltage	V_{OL} (3)	I_{OL} = 20 mA			2	V
	Output-off leakage current	I_{OFF} (3)	V_{OH} = 10 V			30	μA
		I_{OFF} (4)	V_{OH} = 5.5 V			10	μA
Current dissipation		I_{DD}	V_{DD} = 5.5 V When input/output terminals are open and OSC oscillating		30		mA
Input terminal capacitance		C_I			10		pF

Refer to "Input/output designation table" for "N" "H" "N, OD" "N, PU" "H, OD" "H, PU" "OD" "PU".

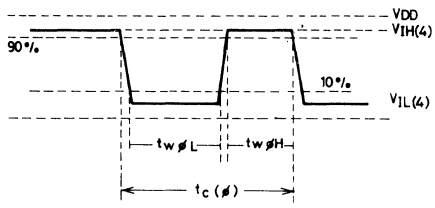


Fig. 1 EXtal input waveform

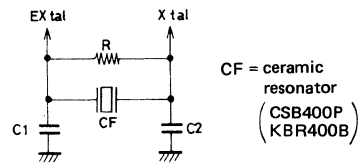


Fig. 2 Recommended oscillating circuit

APPLICATION DEVELOPMENT TOOLS

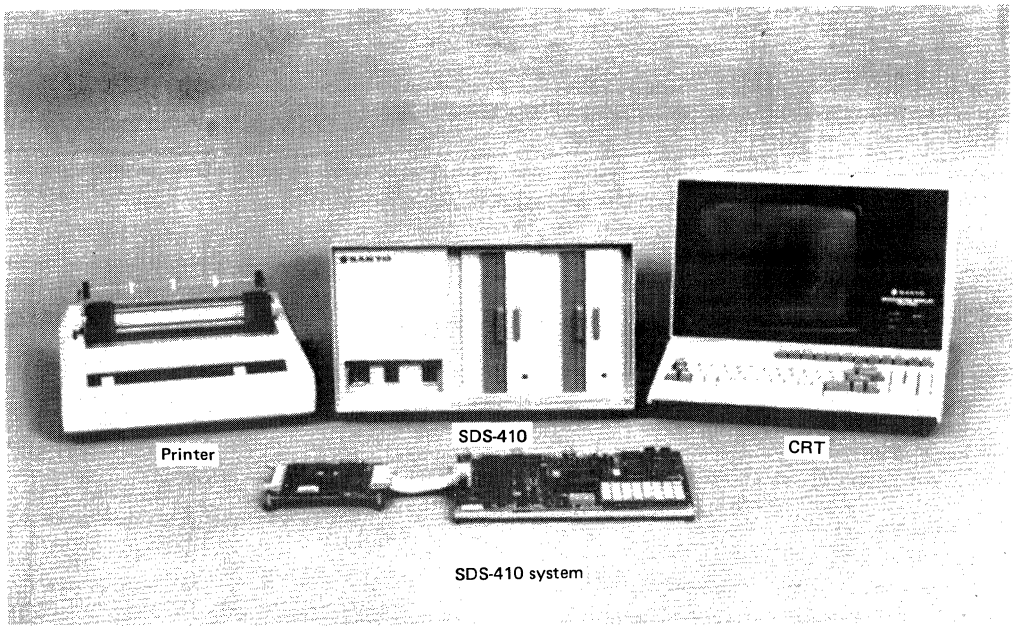
For LM 6402A and 6405A application development, evaluation chip (LM6499) and dedicated equipment called "application development tools" are available.

- SDS-410
  Using a CPU with floppy disks, CRT, and printer, makes development of application programs easier, quicker, and with greater efficiency. Connecting EVA-410 with a CPU, makes it possible to debug programs and write data into EPROMs (with an EPROM WRITER function contained in EVA-410).

- EVA-410
  This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. By replacing the target board, this kit can be used for application development of CMOS microcomputers (LC6500 series) as well as the LM6400 series.

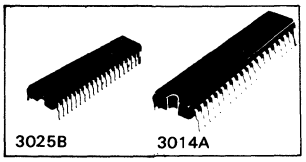
- EVA-401
  This is a board combining an EPROM and LM6499. It is used for mounting evaluation or trial production of sets after application development programs are completed.

- LM64PG99
  This is a system evaluation chip intended for application development tool of the single-chip 4-bit microcomputer LM6400 series. A 24-pin socket for program EPROM and PLA EPROM is provided on the package surface. By mounting this chip on the user's application equipment, using the LM6400 series operation of the equipment can be checked in terms of hardware/software. The LM64PG99 can be used very effectively in equipment made by way of trial.



SDS-410 system

LM6402H, 6405H



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1021B

OUTLINE

LM6402H and 6405H are N-channel MOS 4-bit microcomputers with ROM, RAM, ALU, I/O ports, timer, and clock generator, built on a single chip. The microcomputer, for control applications, has a ROM memory with a maximum capacity of 2K bytes, a RAM with 128 x 4 bits, I/O ports with 35 terminals, and internal PLAs. As their 5 μs cycle time is relatively fast, they are also well suited for sophisticated control.

1) Hardware features (reduction in externally connected component parts)
   * An N-channel E/D MOS for a single 5 V power supply
   * C MOS and TTL compatible
   * LED driver output ports (2 ports/8 pins)
   * 24 character PLAs
   * Dual purpose I/O ports (7 ports/27 pins)
   * Flexible output (open drain/with pull-up resistors)
   * Clock oscillator (with externally connected ceramic oscillating element)
   * Cycle time 5 μs
   * 1K byte/2K byte pin compatible
   * Programmable input threshold voltages (normal/high thresholds)
   * Initialized resetting and builtin Schmitt gate at external interrupt terminal

2) Software features (effective utilization of ROM capacity)
   * 4-level subroutine nesting feasible
   * Interrupt functions (external/internal)
   * Builtin programmable timer capable of a wide range of designations (timer, pulse count, and pulse width measurement)
   * A rich variety of instructions of 82 kinds
   * Automatic step forward with page designation
   * 1K byte/2K byte instruction compatible

Note: The LM6400 series is structured in the following way to permit optimum usage.

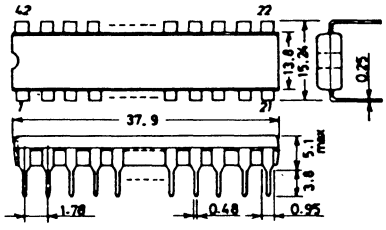
Model	Application	ROM	RAM	Cycle time	I_{DD} (type)	Package	Comments
LM6402A	General use	2K bytes	128 x 4 bits	10 μs	30 mA	DIP-42 DIP-42S	
LM6405A	General use	1K bytes	64 x 4 bits	10 μs	30 mA	DIP-42 DIP-42S	
LM6402H	High speed uses	2K bytes	128 x 4 bits	5 μs	40 mA	DIP-42 DIP-42S	
LM6405H	High speed uses	1K bytes	64 x 4 bits	5 μs	40 mA	DIP-42 DIP-42S	
LM6402L	Low power consumption usage	2K bytes	128 x 4 bits	20 μs	10 mA	DIP-42 DIP-42S	New development
LM6405L	Low power consumption usage	1K bytes	64 x 4 bits	20 μs	10 mA	DIP-42 DIP42S	New development
LM6416E	Small scale usage	1K bytes	64 x 4 bits	5 ~ 10 μs	20 mA	DIP-28S	New development

(continued on next page)

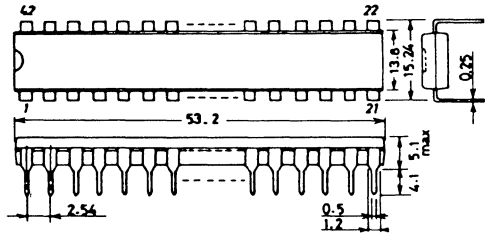
For details, refer to LM6400 Series User's Manual.

Model	Application	ROM	RAM	Cycle time	I_{DD} (type)	Package	Comments
LM6499	Evaluation chip for LM6402A, H, L and LM6405A, H, L	Externally connected 2K		5 ~ 10 μs	30 mA	QIC-80	
LM6497	Evaluation chip for LM6416E	Externally connected 2K		5 ~ 10 μs	20 mA	QIC-80	New development

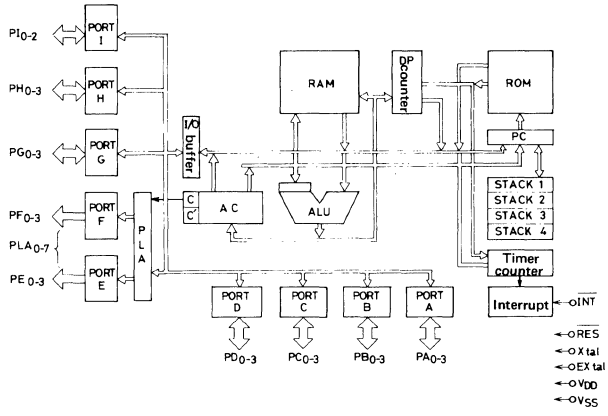
Case Outline 3025B-D42SIC
(unit: mm) DIP-42S



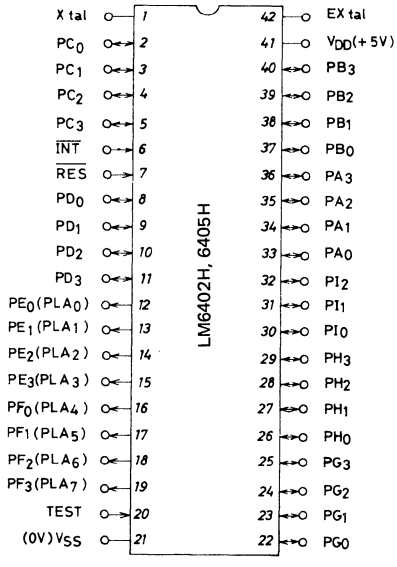
Case Outline 3014A-D42IC
(unit: mm) DIP-42



System block diagram [LM6402H, 6405H]



Package and terminal names



Terminal name

Xtal, EXtal:	Oscillating element for OSC
$\overline{INT}$:	Interrupt
$\overline{RES}$:	Reset
PA_{0-3}:	Input/output ports A_{0-3}
PB_{0-3}:	Input/output ports B_{0-3}
PC_{0-3}:	Input/output ports C_{0-3}
PD_{0-3}:	Input/output ports D_{0-3}
PE_{0-3} (PLA_{0-3}):	Output ports E_{0-3} (PLA outputs$_{0-3}$)
PF_{0-3} (PLA_{4-7}):	Output ports F_{0-3} (PLA outputs$_{4-7}$)
PG_{0-3}:	Input/output ports G_{0-3}
PH_{0-3}:	Input/output ports H_{0-3}
PI_{0-2}:	Input/output ports I_{0-2}
TEST:	Test

Terminal functions

Terminal name	Input/outputs	Functions
$\overline{INT}$	Input	Interrupt request input terminal.
$\overline{RES}$	Input	Reset input terminal.
$PA_{3\text{-}0}$	Input Input/output (Note 1)	Input/output ports A_3-A_0. On input, can provide 4-bit input and can test bits. On output, can provide 4-bit output and can set and reset bits.
$PB_{3\text{-}0}$	Input Input/output (Note 1)	Input/output ports B_3-B_0. On input, can provide 4-bit input and can test bits. On output, can provide 4-bit output and can set and reset bits.
$PC_{3\text{-}0}$	Input/output	Input/output ports C_3-C_0. On input, can provide 4-bit input and can test bits. On output, can provide 4-bit output, can set and reset bits, and can perform immediate data output.
$PD_{3\text{-}0}$	Input/output	Input/output ports D_3-D_0. On input, can provide 4-bit input and can test bits. On output, can provide 4-bit output, can set and reset bits, and can perform immediate data output.
$PE_{3\text{-}0}$	Output	Output ports E_3-E_0. Can provide 4-bit output and can set and reset bits, PLA outputs are fed from this terminal and $PF_{3\text{-}0}$.
$PF_{3\text{-}0}$	Output	Output ports F_3-F_0 Can provide 4-bit output and can set and reset bits. PLA outputs are fed out from this terminal and $PE_{3\text{-}0}$.
$PG_{3\text{-}0}$	Input Input/output Output (Note 1)	Input/output ports G_3-G_0. On input, can provide 4-bit input and can test bits. On output, can provide 4-bit output and can set and reset bits.
$PH_{3\text{-}0}$	Input Input/output Output (Note 1)	Input/output H_3-H_0. On input, can provide 4-bit input and can test bits. On output, can provide 4-bit output and can set and reset bits.
$PI_{2\text{-}0}$	Input/output	Input/output ports I_2-I_0. On input, can provide 3-bit input and can test bits. On output, can provide 3-bit outputs and can set and reset bits.
Xtal	Input/output	Terminal for external connection of resonant circuit for internal clock oscillation. Connect a ceramic, or other oscillating element across this terminal and Extal terminal.
EXtal	Input	Terminal for supplying external clock. When employing internal clock oscillation, connect a ceramic, or other oscillating element across this terminal and Xtal terminal.
V_{DD}	Input	Power supply terminal: Normally connected to +5 V.
V_{SS}	–	Connect to 0 V of power supply.
TEST	Input	LSI test terminal: Normally connect to V_{SS}(0 V).

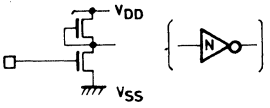
(Note 1): Mask programming can be used to designate input, input/output, or output.

Input/output designation table

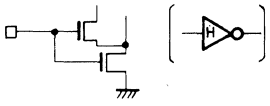
Option \ Port	A	B	C	D	E	F	G	H	I
Input dedicated	N H	N H					N H	N H	
Output dedicated					OD	OD	OD PU	OD PU	
Input/output common	N, OD H, OD	N, OD H, OD	N, OD N, PU H, OD H, PU	N, OD N, PU H, OD H, PU			N, OD N, PU H, OD H, PU	N, OD N, PU H, OD H, PU	N, OD H, OD

N: Normal input gate
H: High-threshold input gate
OD: Open-drain output
PU: Pull-up resistor equipped output

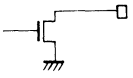
Input-dedicated normal input gate (N)



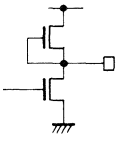
Input dedicated, high-threshold input gate (H)



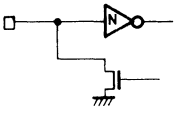
Output dedicated open-drain output (OD)



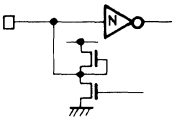
Output dedicated pull-up resistor output (PU)



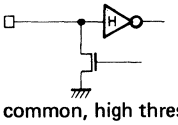
Input/output common, normal input, open-drain output (N, OD)



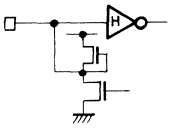
Input/output common, normal input, pull-up resistor output (N, PU)



Input/output common high-threshold input, open-drain output (H, PU)

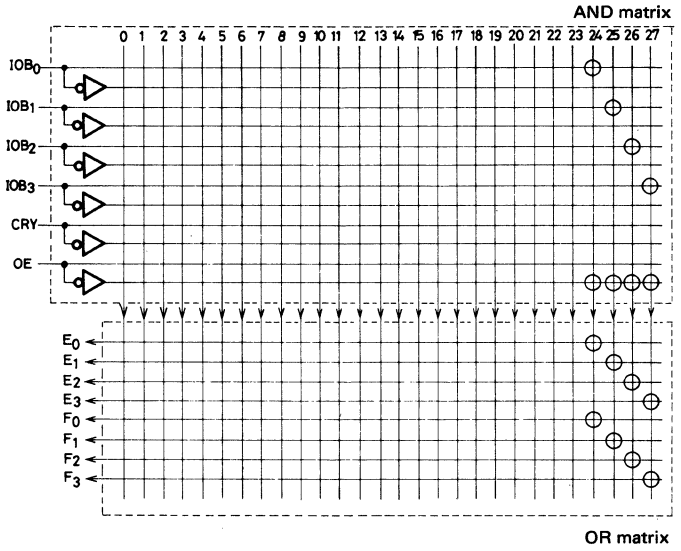


Input/output common, high threshold input, pull-up resistor output (H, PU)



PLA for E and F ports

User-designated mask programmable



ABSOLUTE MAXIMUM RATINGS/T_a = 25°C, V_{SS} = 0 V			min	max	unit
Maximum power-supply voltage	V_{DD} max		−0.3	+8	V
Input voltage	V_{IN}		−0.3	+12	V
Output voltage	V_{OUT} (1)	When output transistors are off	−0.3	+12	V
Average output current	I_{OHA}	for each pull-up spec terminal	−2.0	0	mA
(to be applied to any 100 ms period)	I_{OLA} (1)	total of all terminals in C and D ports	0	20	mA
	I_{OLA} (2)	for each terminal in E and F ports	0	40	mA
	I_{OLA} (3)	total of either E or F port	0	100	mA
	I_{OLA} (4)	total of all terminals in A, B, G, H, and I ports	0	50	mA
Peak output current	I_{OHP}	for each pull-up spec terminal	−2.0	0	mA
	I_{OLP} (1)	for each output terminal in other than E and F ports	0	4	mA
	I_{OLP} (2)	for each terminal in E and F ports	0	40	mA
	I_{OLP} (3)	total of either E or F port	0	100	mA
Allowable power dissipation	P_d max	T_a = −30 ~ +70°C		600	mW
Operating ambient temperature	T_{opg}		−30	+70	°C
Storage ambient temperature	T_{stg}		−55	+125	°C

RECOMMENDED OPERATING CONDITIONS/T_a = −30 ~ +70°C, V_{SS} = 0 V				min	typ	max	unit
Recommended power supply voltage		V_{DD}		4.5	5.0	5.5	V
Normal input specs for input-dedicated port and input/output common port	(H) level input voltage	V_{IH} (1)	Input/output style "N" "N, OD" "N, PU"	2.2		V_{DD}	V
	(L) level input voltage	V_{IL} (1)	Input/output style "N" "N, OD" "N, PU"	V_{SS}		0.6	V
High threshold input specs for input dedicated port and input/output common port	(H) level input voltage	V_{IH} (2)	Input/output style "H" "H, OD" "H, PU"	0.6V_{DD}		V_{DD}	V
	(L) level input voltage	V_{IL} (2)	Input/output style "H" "H, OD" "H, PU"	V_{SS}		0.3V_{DD}	V

				min	typ	max	unit
$\overline{INT}$, $\overline{RES}$	(H) level input voltage	V_{IH} (3)		$0.7V_{DD}$		V_{DD}	V
	(L) level input voltage	V_{IL} (3)		V_{SS}		$0.3V_{DD}$	V
EXtal	(H) level input voltage	V_{IH} (4)		$0.8V_{DD}$		V_{DD}	V
	(L) level input voltage	V_{IL} (4)		V_{SS}		1.0	V
	Clock cycle time	$t_c(\phi)$	V_{DD} = 5 V ± 10% Refer to Fig. 1	1.2		1.3	μs
	(H) level clock pulse width	$t_{w\phi H}$	V_{DD} = 5 V ± 10 % Refer to Fig. 1	0.4			μs
	(L) level clock pulse width	$t_{w\phi L}$	V_{DD} = 5 V ± 10 % Refer to Fig. 1	0.4			μs
Xtal	(H) level input voltage	V_{IH} (5)					V
	(L) level input voltage	V_{IL} (5)					V
Externally-connected resistance value for oscillation		R	Refer to Fig. 2		1000		kΩ
Externally-connected capacitance value for oscillation		C_1	Refer to Fig. 2		220		pF
		C_2	Refer to Fig. 2		220		pF
TEST	(L) level input voltage	V_{IL} (6)	V_{DD} = 5 V ± 10%	V_{SS}		0.4	V

Refer to "Input/output designation table" for "N", "H" "N, OD" "N, PU" "H, OD" "H, PU"

ELECTRICAL CHARACTERISTICS/T_a = −30 ~ +70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

				min	typ	max	unit
Input dedicated port and $\overline{RES}$	(H) level input current	I_{IH} (1)	Input/output style "N" "H" V_{IN} = V_{DD}			10	μA
	(L) level input current	I_{IL} (1)	Input/output style "N" "H" V_{IN} = V_{SS}	−10			μA
Input/output common port with open-drain spec output	(H) level input current	I_{IH} (2)	Input/output style "N, OD" "H, OD" V_{IN} = V_{DD}			10	μA
	(L) level input current	I_{IL} (2)	Input/output style "N, OD" "H, OD" V_{IN} = V_{SS}	−10			μA
Input/output common port with pull-up spec output	(L) level input current	I_{IL} (3)	Input/output style "N, PU" "H, PU" V_{DD} = 5 V ± 10% V_{IN} = 0.4 V	−1.6			mA
Pull-up specs for output dedicated or input/output common port	(L) level output voltage	V_{OL} (1)	Input/output style "PU" "N, PU" "H, PU" I_{OL} = 1.6 mA			0.4	V
	(H) level output voltage	V_{OH} (1)	Input/output style "PU" "N, PU" "H, PU" I_{OH} = −50μA	$0.8V_{DD}$		V_{DD}	V
		V_{OH} (2)	Input/output style "PU" "N, PU" "H, PU" I_{OH} = −80μA	$0.66V_{DD}$		V_{DD}	V
		V_{OH} (3)	Input/output style "PU" "N, PU" "H, PU" I_{OH} = −100μA	$0.48V_{DD}$		V_{DD}	V

				min	typ	max	unit
Open drain specs for output dedicated or input/output common port	(L) level output voltage	V_{OL} (2)	Input/output style "OD" "N, OD" "H, OD" I_{OL} = 1.8 mA			0.4	V
	Output-off leakage current	I_{OFF} (1)	Input/output style "OD" "N, OD" "H, OD" V_{OH} = 10 V			30	μA
		I_{OFF} (2)	Input/output style "OD" "N, OD" "H, OD" V_{OH} = 5.5 V			10	μA
E and F ports	(L) level output voltage	V_{OL} (3)	I_{OL} = 20 mA			2	V
	Output-off leakage current	I_{OFF} (3)	V_{OH} = 10 V			30	μA
		I_{OFF} (4)	V_{OH} = 5.5 V			10	μA
Current consumption		I_{DD}	V_{DD} = 5.5 V When input/output terminals are open and OSC oscillating		35		mA
Input terminal capacitance		C_I			10		pF

Refer to "Input/output designation table" for "N" "H" "N, OD" "N, PU" "H, OD" "H, PU" "OD" "PU".

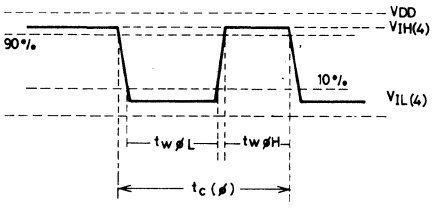


Fig. 1 EXtal input waveform

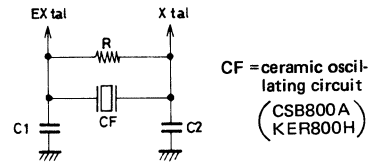


Fig. 2 Recommended oscillating circuit

Application Development Tools

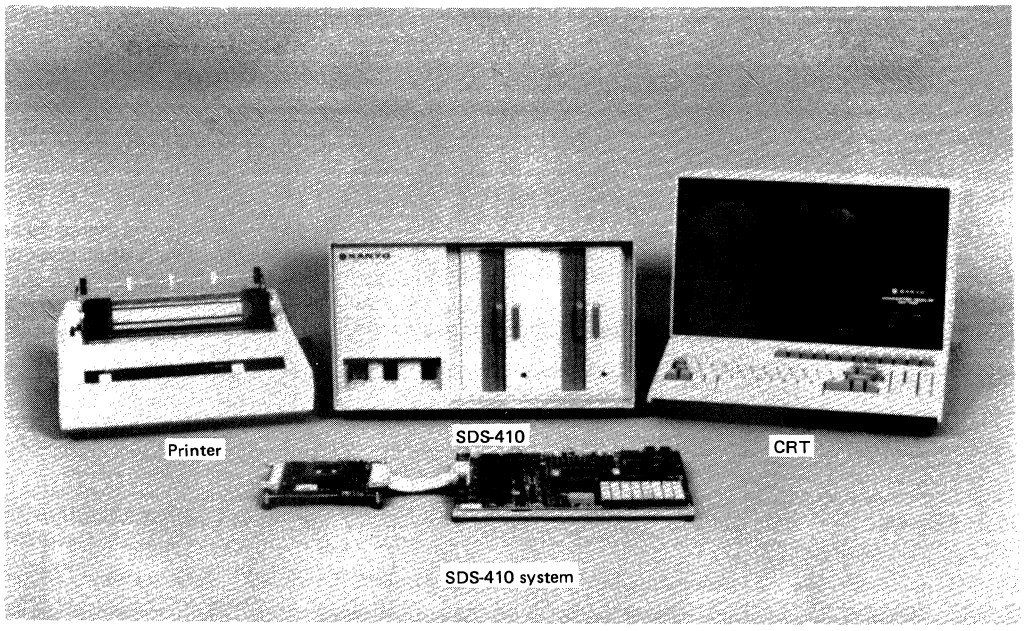
For convenience of application development of the LM6402H/6405H, the evaluation chip (LM6499) and dedicated equipment called "application development tools" are available.

- SDS-410
  This is a combination of floppy disks-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be made (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled or data can be written into EPROM's (using EPROM WRITER function contained in the EVA-410).

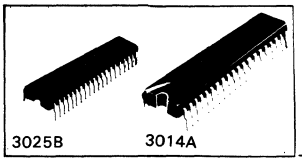
- EVA-410
  This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. By replacing the target board, this kit can be used for application development of CMOS microcomputers (LC6500 series) as well as the LM6400 series.

- EVA-401
  This is a board with an EPROM and the LM6499 combined. This board is used for mounting evaluation or trial production of sets after application development programs are completed.

- LM64PG99
  This is a system evaluation chip intended for application development tool of the single-chip 4-bit microcomputer LM6400 series. A 24-pin socket for program EPROM and PLA EPROM is provided on the package surface. By mounting this chip on the user's application equipment, operation of the equipment can be checked in terms of hardware/software. The LM64PG99 can be used very effectively in equipment made by way of trial.


Printer
SDS-410
CRT
SDS-410 system

LM6402G, 6405G



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1303A

General Description

The LM6402G/6405G are single-chip 4-bit N channel MOS microcomputers intended for use in control-oriented applications. They contain a ROM (2048 bytes (2K bytes)), a RAM (128 x 4 bits), an ALU, I/O ports (35 pins), a timer, a clock generator, a PLA. They are improved versions of the LM6402A/6405A and the LM6402H/6405H, in which a prescaler for system clock is contained and 3 options of frequency division are allowed. Other functions are the same as those of the LM6402A/6405A and the LM6402H/6405H. The following table shows a comparison between the LM6402/5G and the LM6402/5A, H in terms of newly added functions.

Item	LM6402/5 A, H	LM6402/5 G
Minimum cycle time	5 μs or 10 μs	2.94 μs
OSC	800k or 400k Ceramic oscillation	800k or 400k Ceramic Oscillation 1/1 divider RC oscillation 1/1 divider 4 MHz Ceramic Oscillation 1/3 divider 4M: Ceramic, 4.19M: Crystal Oscillation 1/4 divider External clock 1/1, 1/3, 1/4 divider } Option
I/O voltage	+12 V	+15 V
Output current maximum rating (Peak current per pin I_{OL})	Other than E, F = 4 mA E, F = 40 mA	Other than E, F = 30 mA E, F = 50 mA

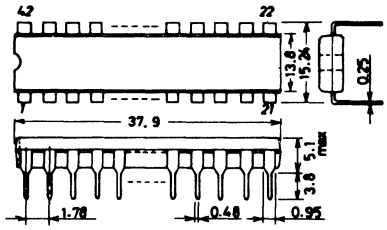
1) Hardware features (Reduction in external parts)
- Clock generator, frequency divider (3 options of 1/1, 1/3, or 1/4 division)
  Ceramic oscillation, crystal oscillation available: f_{max} = 4.2 MHz, RC Oscillation available
- Cycle time: 2.94 μs min.
- Input/output common ports (7 ports/27 pins), open drain, input/output ports direct interfacable to 12V – operated equipment
- Flexible output configuration (Open drain, pull-up resistor attached)
- Input threshold voltage select (Normal, high threshold)
- LED driver-contained output ports (All ports are capable of delivering large current.)
- 24-character PLA
- Initial reset and external interrupt input pins containing Schmitt gate
- 1K bytes/2K bytes pin compatible
- Single 5 V supply, N channel, E/D MOS

2) Software features (Effective use of ROM capacity)
- 4-level subroutine nesting
- Interrupt function (External/internal)
- Programmable timer with wide setting range (Timer, pulse count, pulse width measure)
- Powerful instruction set of 82 instructions
- 1K bytes/2K bytes instruction compatible

3) Evaluation chip
- Evaluation chip LM6499, Piggyback LM64PG99, and prescaler IC board (G2 board) are available for use in the application development of the LM6402G/6405G.

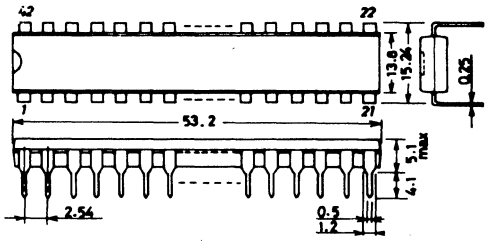
For details, refer to LM6400 Series User's Manual.

Case Outline 3025B-D42SIC
(unit: mm)



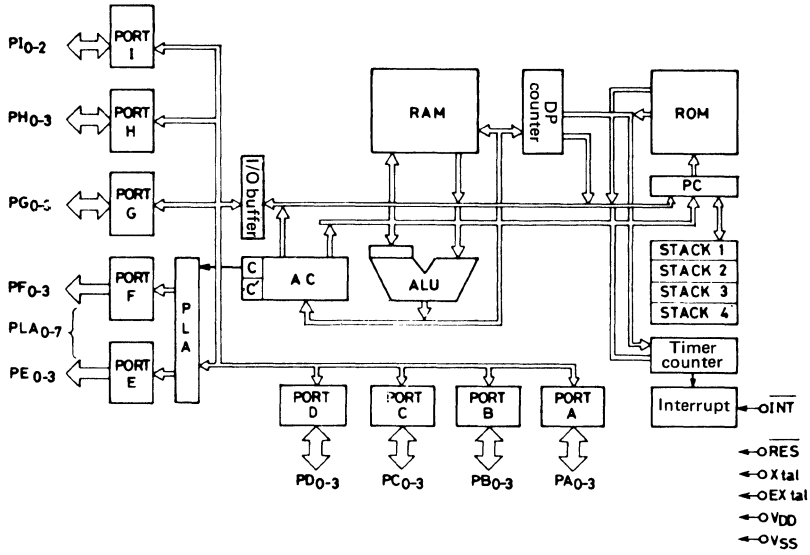
SANYO: DIP42S

Case Outline 3014A-D421C
(unit: mm)

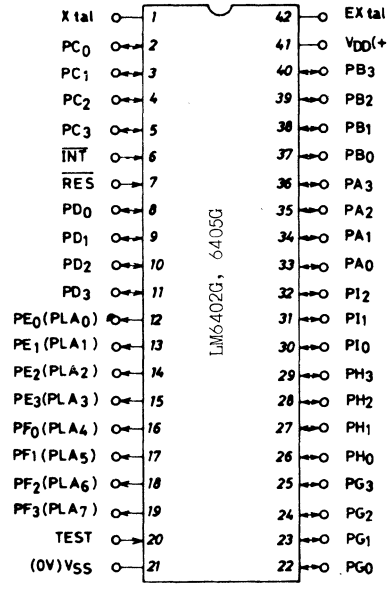


SANYO: DIP42

System Block Diagram



Package and Pin Assignment



Pin Name		
Xtal, EXtal	:	OSC resonator attached externally
INT	:	Interrupt
RES	:	Reset
$PA_{0 \text{ to } 3}$	:	Input/output ports $A_{0 \text{ to } 3}$
$PB_{0 \text{ to } 3}$	:	Input/output ports $B_{0 \text{ to } 3}$
$PC_{0 \text{ to } 3}$	:	Input/output ports $C_{0 \text{ to } 3}$
$PD_{0 \text{ to } 3}$	:	Input/output ports $D_{0 \text{ to } 3}$
$PE_{0 \text{ to } 3}$ ($PLA_{0 \text{ to } 3}$)	:	Output ports $E_{0 \text{ to } 3}$ (PLA output $_{0 \text{ to } 3}$
$PF_{0 \text{ to } 3}$ ($PLA_{4 \text{ to } 7}$)	:	Output ports $F_{0 \text{ to } 3}$ (PLA mode $_{4 \text{ to } 7}$)
$PG_{0 \text{ to } 3}$	:	Input/output ports $G_{0 \text{ to } 3}$
$PH_{0 \text{ to } 3}$	:	Input/output ports $H_{0 \text{ to } 3}$
$PI_{0 \text{ to } 2}$	:	Input/output ports $I_{0 \text{ to } 2}$
TEST	:	Test

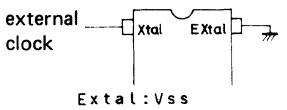
Optional Functions

1) OSC select table

OSC Option	Frequency	Resonator	Divider	Option Code	Cycle Time*
RC oscillation	770kHz typ	C=82 pF, R=10kΩ	1/1	A	5.2 μs typ
Ceramic Oscillation	400kHz*	KBR400B, CSB400p	1/1	B	10 μs
	800kHz*	KBR800H, CSB800A	1/1	B	5 μs
	3.58MHz*	CSA3.58MG, KBR3.58M	1/3	C	3.35 μs
			1/4	D	4.47 μs
	4.0MHz*	CSA4.00MG, KBR4.0M	1/3	C	3 μs
			1/4	D	4 μs
	4.1MHz*	CSA4.10MG, KBR4.1M	1/4	D	3.9 μs
Crystal Oscillation	4.19MHz*	NKD HC-18U 4.194304MHz, LM6402G	1/4	D	3.82 μs
External Clock **	100kHz ~ 1.36MHz		1/1	B	40 ~ 2.94 μs
	300kHz ~ 4.08MHz		1/3	C	40 ~ 2.94 μs
	400kHz ~ 5.0MHz		1/4	D	40 ~ 3.2 μs

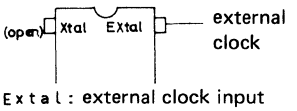
CAS, CSB: Murata Seisakusyo Corp. KBR: Kyocera Corp. NKD: Nikko Denshi Corp.
CYCLE TIME = (1/frequency) x DIVIDER (1,3,4) x 4
* At typical OSC frequency. DSC frequency has an error of approximately ±2 %.
** External Clock Input Circuit (There are differences in input waveform between circuit I and circuit II)

Circuit I



Extal : Vss
Xtal : external clock input

Circuit II



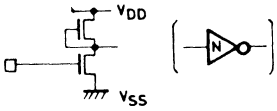
Extal : external clock input
Xtal : open

2) Input/output select table

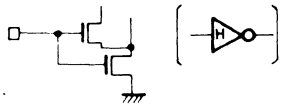
Port / Option	A	B	C	D	E	F	G	H	I
Input only	N H	N H					N H	N H	
Output only					OD	OD	OD PU	OD PU	
Input/output common	N, OD H, OD	N, OD H, OD	N, OD N, PU H, OD H, PU	N, OD N, PU H, OD H, PU			N, OD N, PU H, OD H, PU	N, OD N, PU H, OD H, PU	N, OD H, OD

N : Normal input gate
H : High threshold input gate
OD : Open drain output
PU : Output with pull-up resistor

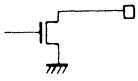
Input only [normal input gate (N)]



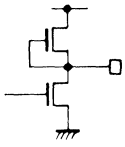
Input only [high threshold input gate (H)]



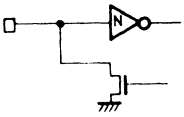
Output only [open drain output (OD)]



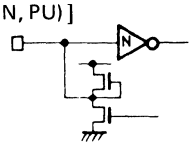
Output only [output with pull-up resistor (PU)]



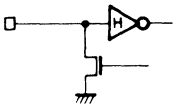
Input/output common [normal input open drain output (N, OD)]



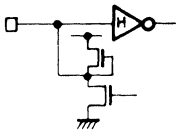
Input/output common [normal input, output with pull-up resistor (N, PU)]



Input/output common [high threshold input, open drain output (H, OD)]



Input/output common [high threshold input, output with pull-up resistor (H, PU)]



Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0 V				unit
Maximum supply voltage	V_{DD} max		−0.3 ~ +8	V
Maximum input voltage	V_{IN} max		−0.3 ~ +15	V
Maximum output voltage	V_{OUT}	Output transistor OFF	−0.3 ~ +15	V
Average output current	I_{OHA}	Each pin of pull-up spec.	−2.0 ~ 0	mA
(Note 1)	I_{OLA} 1	Each output pin other than E, F ports	0 ~ 18	mA
	I_{OLA} 2	Each pin of E, F ports	0 ~ 30	mA
	I_{OLA} 3	All pins of E or F ports	0 ~ 75	mA
	I_{OLA} 4	All pins of A, B, G, H, I ports	0 ~ 120	mA
	I_{OLA} 5	All pins of C, D ports	0 ~ 50	mA
Peak output current	I_{OHP}	Each pin of pull-up spec.	−2.0 ~ 0	mA
(Note 2)	I_{OLP} 1	Each output pin other than E, F ports	0 ~ 30	mA
	I_{OLP} 2	Each pin of E, F ports	0 ~ 50	mA
	I_{OLP} 3	All pins of E or F ports	0 ~ 125	mA
	I_{OLP} 4	All pins of A,B G,H,I ports	0 ~ 190	mA
	I_{OLP} 5	All pins of C,D ports	0 ~ 80	mA
Allowable power dissipation	P_d max	T_a = −30 ~ +70°C	600	mW
Operating temperature	T_{opg}		−30 ~ +70	°C
Storage temperature	T_{stg}		−55 ~ +125	°C

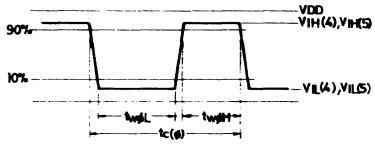
(Note 1) Applicable to any 100 ms period.
(Note 2) Limit value that must not be exceeded even momentarily.

Allowable Operating Ranges/T_a = −30 ~ +70°C, V_{SS} = 0 V				min	typ	max	unit
Supply voltage		V_{DD}		4.5	5.0	6.5	V
Input port & input/output commom port: normal input spec.	"H" level input voltage	V_{IH1}	Input/output circuit "N" "N, OD" "N,PU"	2.2			V
	"L" level input voltage	V_{IL1}	Input/output circuit "N" "N, OD" "N,PU"	V_{SS}		0.6	V
Input port & input/output commom port: high threshold input spec.	"H" level input voltage	V_{IH2}	Input/output circuit "H" "H, OD" "H,PU"	0.6 V_{DD}			V
	"L" level input voltage	V_{IL2}	Input/output circuit "H" "H, OD" "H,PU"	V_{SS}		0.3V_{DD}	V
$\overline{INT}$, $\overline{RES}$	"H" level input voltage	V_{IH3}		0.7V_{DD}			V
	"L" level input voltage	V_{IL3}		V_{SS}		0.3V_{DD}	V

Xtal [External clock option ; for option B,C,D ; Extal=0V]	"H" level input voltage	V_{IH} 4		0.2V_{DD}+2.8		V_{DD}	V
	"L" level input voltage	V_{IL} 4		V_{SS}		1.4	V
	Clock cycle	tcφ	1/3 divider option	0.245		3.3	μs
			1/4 divider option	0.20		2.5	μs
			1/1 divider option	0.735		10	μs
	Instruction cycle time	tcl	tcφ x division x 4	2.94		40	μs
	"H" level clock pulse width	twφH	See Fig. 1. B, C, D option	0.1			μs
	"L" level clock pulse width	twφL	See Fig. 1. B, C, D option	0.1			μs
Extal [External clock applied ; for option B,C,D ; Xtal=open]	"H" level input voltage	V_{IH} 5		0.5V_{DD}+1.5		V_{DD}	V
	"L" level input voltage	V_{IL} 5		V_{SS}		1.0	V
	Clock cycle	tcφ	1/3 divider option	0.735		3.3	μs
			1/4 divider option	0.735		2.5	μs
			1/1 divider option	0.735		10	μs
	Instruction cycle time	tcl	tcφ x division x 4	2.94		40	μs
	"H" level clock pulse width	twφH	See Fig. 1. B, C, D option	0.3			μs
	"L" level clock pulse width	twφL	See Fig. 1. B, C, D option	0.3			μs
Extal, Xtal [oscillation]	External resistance for ceramic or crystal oscillation	R1		900	1000	1100	kΩ
	External capacitance for ceramic or crystal oscillation	C1,C2	f_{osc}=400, 800 kHz (C1,C2)	200	220	240	pF
			f_{osc}=4.0, 4.19 MHz C1, Fig2-(1), (2)	35	39	43	pF
			C2, Same as above	20	22	24	pF
	Pull-Up resistance for crystal oscillation	Rp	See Fig. 2-(2).	3.5	3.9	4.3	kΩ
	External resistance for RC oscillation	R2	See Fig. 3.	5	10	20	kΩ
	External capacitance for RC oscillation	C3		50	82	240	pF
TEST	"L" level input voltage	V_{IL6}				0.4	V

Electrical Characteristics/T_a = −30 to 70°C, V_{DD} = 4.5 to 6.5 V, V_{SS} = 0 V				min	typ	max	unit
Input port & $\overline{RES}$, $\overline{INT}$ Extal [B,C,D option]	"H" level input current	I_{IH1}	Input/output circuit "N" "H", V_{IN} = 13.5 V			5	μA
	"L" level input current	I_{IL1}	Input/output circuit "N" "H", V_{IN} = V_{SS}	−5			μA
Input/output common port [Output: Open drain]	"H" level input current	I_{IH2}	Input/output circuit, "N, OD" "H, OD" V_{IN} = 13.5 V, output Tr off			5	μA
	"L" level input current	I_{IL2}	Input/output circuit, "N, OD" "H, OD" V_{IN} = V_{SS}, output Tr off	−5			μA
Input/output common port [Output: Pull-up]	"L" level input current	I_{IL3}	Input/output circuit "N, PU" "H, PU", V_{DD} = 5 V±10 % V_{IN} = 0.4 V	−1.6			mA
Output port or input/output common port [Pull-up]	"L" level output voltage	V_{OL1}	Input/output circuit "PU" "N, PU" "H, PU" I_{OL} = 14 mA			1.5	V
	"H" level output voltage	V_{OH1}	Input/output circuit "PU" "N, PU" "H, PU" I_{OH} = −50 μA	0.8V_{DD}			V
		V_{OH2}	Input/output circuit "PU" "N, PU" "H, PU" I_{OH} = −80 μA	0.66V_{DD}			V
		V_{OH3}	Input/output circuit "PU" "N", PU" "H, PU" I_{OH} = −100 μA	0.48V_{DD}			V
Output port or input/output common port [Open drain]	"L" level output voltage	V_{OL2}	Input/output circuit "OD" "N, OD" "H, OD" I_{OL} = 15 mA			1.5	V
	Output OFF leak current	I_{OFF1}	Input/output circuit "OD""N, OD" "H, OD" V_{OH} = 13.5 V			5	μA
		I_{OFF2}	Input/output circuit "OD" "N, OD" "H, OD" V_{OH} = V_{DD}			1	μA
E, F port	"L" level output voltage	V_{OL3}	I_{OL} = 25 mA			2	V
	Output OFF leak current	I_{OFF3}	V_{OH} = 13.5 V			5	μA
		I_{OFF4}	V_{OH} = V_{DD}			1	μA
Xtal [B,C,D option, Extal=0V]	"H" level input current	I_{IH3}	V_{IN} = V_{DD}			5	μA
	"L" level input current	I_{IL4}	V_{IN} = 1V	−5.8			mA
Current dissipation		I_{DD}	OSC oscillation, LM6402G		38	73	mA
			output open, LM6405G		38	73	mA
Input pin capacitance		C_I			10		pF
RC oscillation frequency		f_{OSC}	C = 82 pF, R = 10 kΩ 0 ~ 70°C*	670	770	885	kHz
			Same as above −30 ~ 70°C*	670	770	895	kHz
			See Fig. 3. Including stray capacitance of substrate wiring				

For "N", "H", "N, OD", "N, PU", "H, OD", "H, PU", "OD", "PU", refer to input/output select table.



Extal input:$V_{IH}(5)$, $V_{IL}(5)$
Xtal input: $V_{IH}(4)$,$V_{IL}(4)$

Fig. 1 Extal, Xtal input waveform

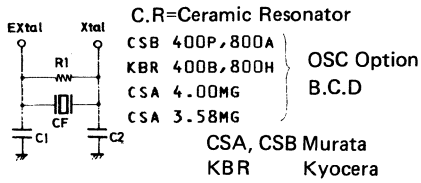


Fig. 2-(1) Recommended OSC circuit (1) / Ceramic resonator

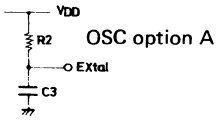


Fig. 3 Recommended OSC circuit (3)/RC OSC

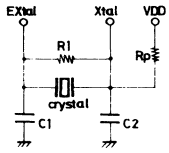
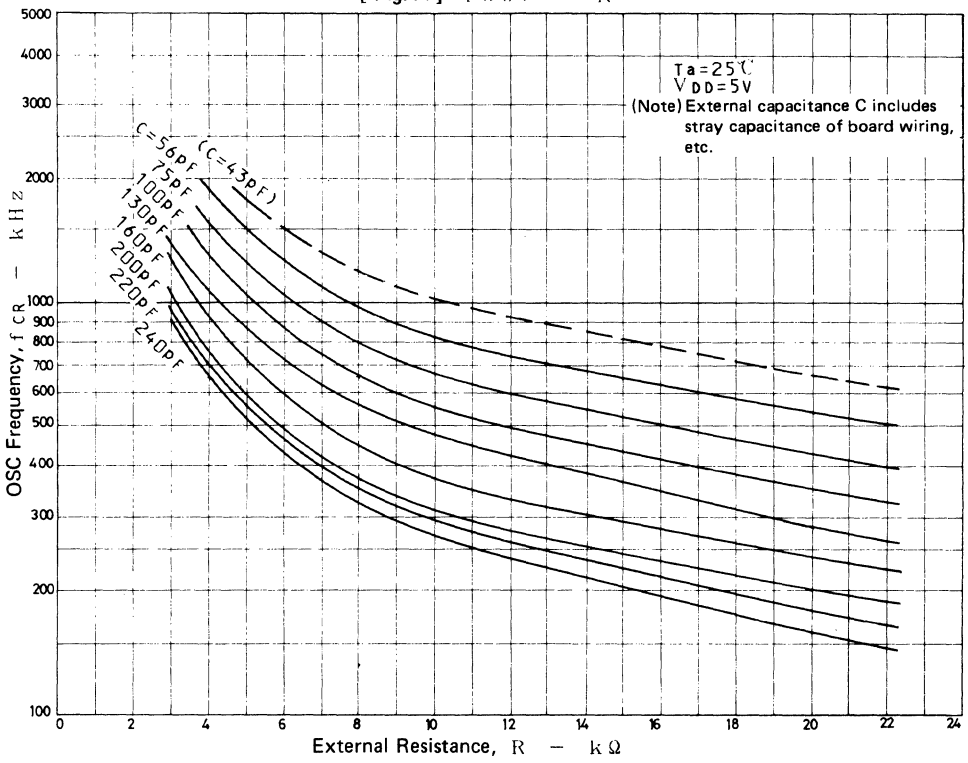
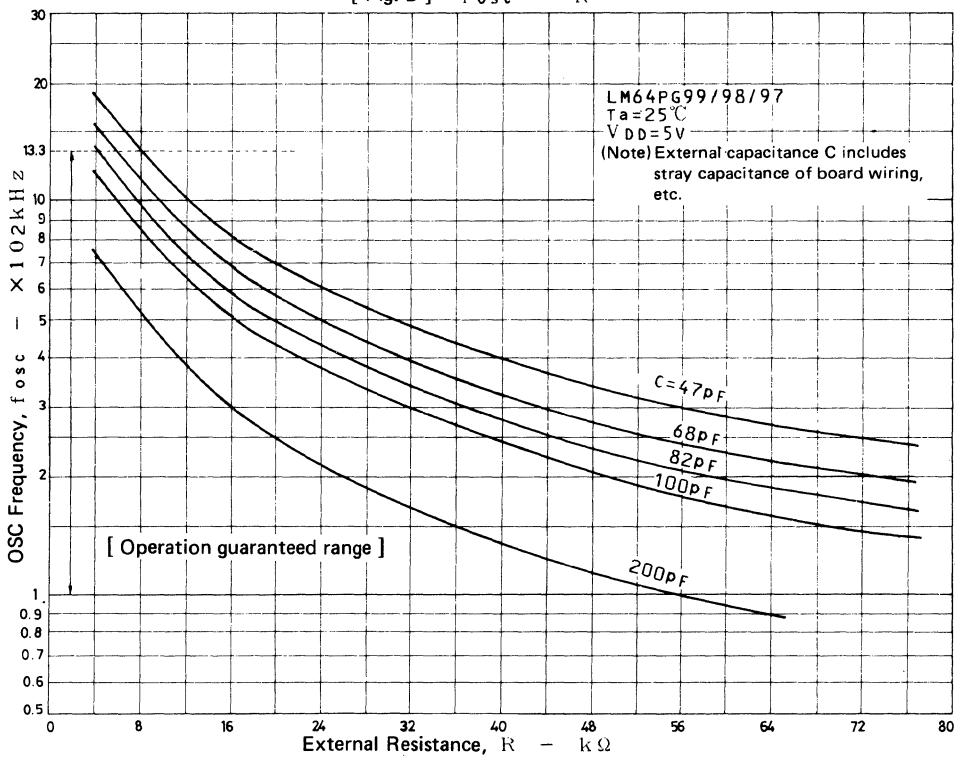


Fig. 2-(2) Recommended OSC circuit (2) / Crystal resonator

[Fig. A] fosc – R



[Fig. B] fosc – R



CR oscillation of LM6402G/05G, LM64PG99

(1) For the variation range of CR oscillation frequency of the LM6402G/05G, the following are guaranteed at external constants of C=82pF, R=10kohm only.

① fosc= 670min ~770typ ~885max kHz /Ta= 0~+70℃

② fosc= 670min ~770typ ~895max kHz /Ta=-30~+70℃

(2) If other frequency than typical value 770kHz is used at other constants than C=82pF, R=10kohm, fix CR constants referring to "OSC frequency vs. standard external resistance characteristics" in Fig. A. In this case, take care of the following.
① Oscillation cycle must be within the range (0.75 to 10.0 usec.) of recommended operation clock cycle at OSC pin.
② CR constants must be selected from among recommended external constants (C=56 to 240pF, R=5 to 20kohm).
It should be noted that outgoing inspection is performed under the frequency variation condition at C=82pF, R=10kohm.

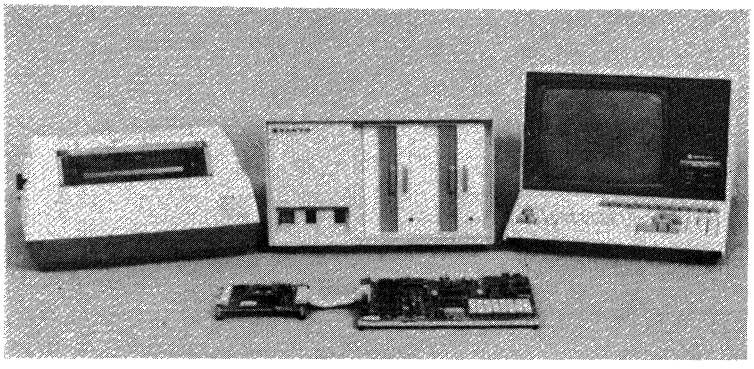
(3) The LM64PG99 alone is not capable of evaluating for the LM6402G/05G. CR oscillation option. It is necessary to simulatedly mount CR on the conversion board (G2 socket). CR constants of the LM64PG99 are fixed referring to "OSC frequency vs. standard external resistance characteristics" in Fig. B. When the LM64PG99 is used to evaluate the LM6402G/05G for CR oscillation option, an oscillation frequency nearly equivalent to that of the LM6402G/05G can be obtained by mounting C=82pF, R=10kohm on the conversion board as with the LM6402G/05G.
However, the oscillation frequency obtained must be checked.

Application development tools

Evaluation chip LM6499 and the dedicated equipment called "application development tools" are available to facilitate application development tools for the LM6402G. For details of the application development tools, refer to 'MANUAL FOR DEVELOPMENT TOOLS'.

(1) SDS-410 system
This is a combination of floppy disks-provided CPU, CRT, and printer. This system makes it possible for application development program of microcomputers to be made (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, program can be debugged and assembled or data can be written into EPROM (using EPROM WRITER function contained in the EVA-410).

(2) EVA-410 + TB1 (6499)
This is an evaluation kit having EPROM WRITER function, of parallel/serial data communication with external equipment (SDS-410, etc.). This kit makes it possible for application development programs to be corrected or debugged. The LM6499 is mounted on the TB1.

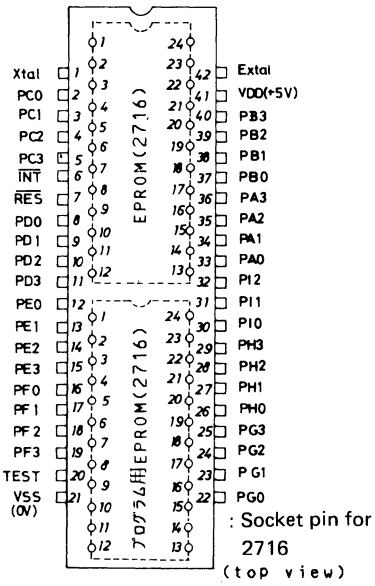


(3) LM64PG99

The LM64PG99 is provided with 24-pin sockets for 2 EPROMs for programming and "PLA through" on its package surface.

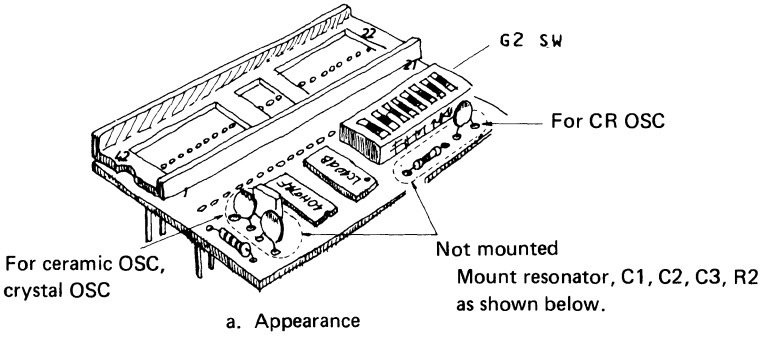
Xtal, Extal	: OSC ceramic resonator	
$\overline{\text{INT}}$	: Pseudo interrupt	
$\overline{\text{RES}}$	: Reset	
PA0~3	: Input/output ports	A0~3
PB0~3	: Input/output ports	B0~3
PC0~3	: Input/output ports	C0~3
PD0~3	: Input/output ports	D0~3
PE0~3	: Output ports	E0~3
PF0~3	: Output ports	F0~3
PG0~3	: Input/output ports	G0~3
PH0~3	: Input/output ports	H0~3
PI0~2	: Input/output ports	I0~2
TEST	: Test	

Pin assignmnent LM64PG99

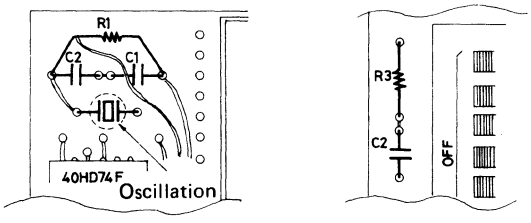


(4) Conversion board for the LM6402G/05G (G2 socket)

- For evaluating the LM6402G/05G, the LM64PG99 and the conversion circuit shown in Fig. a are used jointly.
- For evaluating the LM6402G/05G, the EVA-410-TB1 and the conversion circuit shown in Fig. a are used jointly.



a. Appearance



[For ceramic OSC, crystal OSC] [For CR OSC]

b. Where to mount resonator, C1, C2, C3, R2

When the LM64PG99 is used:

OSC	External connection of OSC circuit	Frequency division		G2 SW 1	2	3	4	5	6	7	8
(1) CR OSC	Target board	1/1		on	off	off	X	X	on	X	X
	G2	1/1		off	off	off	X	X	off	X	X
(2) Ceramic OSC 400~800kHz	Target board	1/1		on	off	off	X	X	on	X	X
	G2	Unavailable									
(3) 4MHz band OSC	Target board	Unavailable									
4MHz CF 1/3 division	G2	1/3		off	off	on	on	on	off	on	off
4MHz CF 1/4 division		1/4		off	off	on	on	on	off	off	on
4.19MHz crystal	Target board (Note)	1/1	Xtal	on	off	off	X	X	on	X	X
			Extal	off	off	off	X	X	on	X	X
(4) External clock		1/3	Xtal	off	off	on	off	off	off	on	off
			Extal	off	on	on	off	off	off	on	off
		1/4	Xtal	off	off	on	off	off	off	off	on
			Extal	off	on	on	off	off	off	off	on
	G2	Unavailable									

How to set the socket G2 SW when the EVA-410-TB1 is used

OSC	External connection of OSC circuit	Frequency division		TB1 SW3 5	6	7	8	G2 SW 1	2	3	4	5	6	7	8
(1) CR OSC	Target board	1/1		on	on	off	off	on	off	off	X	X	on	X	X
	G2	1/1		off	off	off	off	off	off	off	X	X	off	X	X
	EVA-TB1	1/1		off	off	off	off								
(2) Ceramic OSC 400~800kHz	Target board	1/1		on	on	off	off	on	off	off	X	X	on	X	X
	G2	Unavailable													
	EVA-TB1	1/1		off	off	on	on								
(3) 4MHz band OSC	Target board	Unavailable													
4MHz CF 1/3 division	G2	1/3		off	on	off	off	off	off	on	on	on	off	on	off
4MHz CF 1/4 division		1/4		off	on	off	off	off	off	on	on	on	off	off	on
4.19MHz crystal 1/4 division	EVA-TB1	Unavailable													
(4) External clock	Target board (Note)	1/1	Xtal	on	off	off	off	on	off	off	X	X	on	X	X
			Extal	off	on	off	off	off	off	off	X	X	on	X	X
		1/3	Xtal	off	on	off	off	off	off	on	off	off	off	on	off
			Extal	off	on	off	off	off	on	on	off	off	off	on	off
		1/4	Xtal	off	on	off	off	off	off	on	off	off	off	off	on
			Extal	off	on	off	off	off	on	on	off	off	off	off	on
	G2	Unavailable													
	EVA-TB1	Unavailable													

- When a divider is used, a ceramic filter on the target board cannot be used for evaluation. A ceramic filter must be mounted on the G2 socket.
  ON: SW-on mode
  OFF SW-off mode
  X: SW may be placed in any position.

(Note) When applying the clock signal at the Xtal pin in the external drive mode, wire jumper JP and set the switch.
When applying the clock signal at the Extal pin in the external drive mode, set the switch without wiring jumper JP.

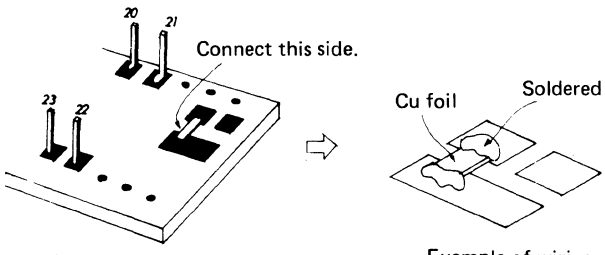
Proper cares in using the LM64PG99

LM64PG99

- Mount the program EPROM and the PLA EPROM. Even when the PLA function is not used, the PLA EPROM (through PLA) must be mounted.
- For evaluating the input/output option as pull-up resistor-contained type output port, connect an external resistor to the pin of the LM64PG99.
- All input/output ports are input/output common and of high threshold input, open drain output type. E,F ports are dedicated to output.

Wiring change according to use/nonuse of PLA function

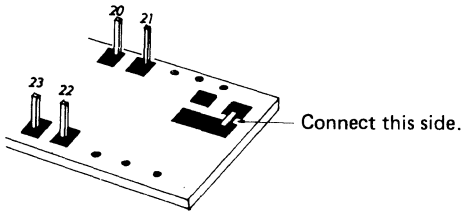
(1) Wiring change when the PLA function is used
When the PLA function is used in evaluating the LM6402G/05G with the LM64PG99, wire the jumper on the package bottom as follows:



(When PLA is used)

Example of wiring

(2) Wiring change when the PLA function is not used
When the PLA function is not used in evaluating the LM6402G/05G, wire the jumper on the package bottom as follows:
For the PLA EPROM, the (through PLA) with data for nonuse of PLA written.



Insert the following data-written EPROM 2716 (through PLA) into the PLA EPROM.

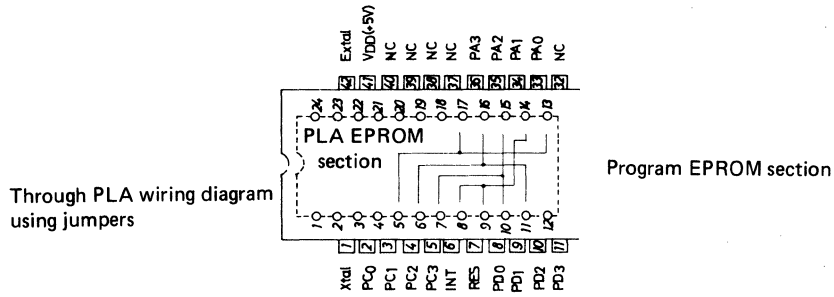
Data for dedicated EPROM (through PLA) (HEX notation)

EPROM address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 1 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 2 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 3 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 4 0																
0 5 0																
:																
:																

For EPROM addresses 40H onward, any data are acceptable.

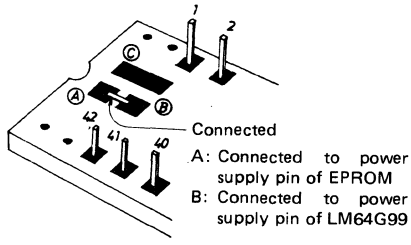
(This data are commonly called 'through PLA'.)

The through PLA EPROM function can be fulfilled by wiring jumpers. The wiring diagram is shown below.



Selection of power supply EPROM (External power supply)
Normally, an EPROM dissipates a current of 50 to 100mA (i.e.200mA max./2 EPROM's).
The power capacity of a user system is not enough, an external power supply can be used.

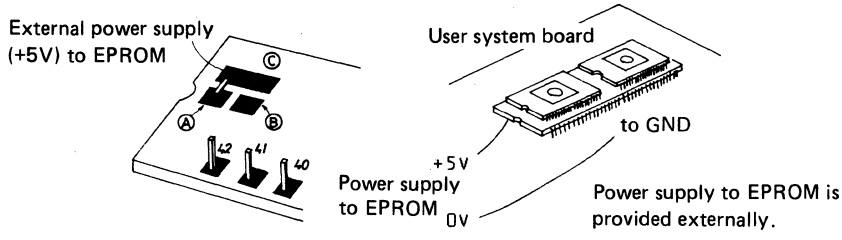
(1) The same power supply is used for the LM64PG99 and EPROM at the time of shipment. A jumper for EPROM power supply select is provided on the package bottom of the LM64PG99. The power supply to the EPROM is connected to the power supply pin (V_{DD} pin) of the LM64PG99 as shown below.



The same power supply is used for the LM64PG and EPROM at the time of shipment.

(2) How to provide external power supply to the EPROM

- Remove the wiring connecting patterns (A) and (B).
- Using this jumper, connect patterns (A) and (C).
- Connect external power supply (+5V) to pattern (C) and external power supply (0V) to GND (0V) of the user system board. See below.



LM6402G, 6405G Instruction Set

Notations

AC	: Accumulator	X	: Working register X	INT FF	: Interrupt FF
An	: Accumulator bit n	Y	: Working register Y	INTE FF	: Interrupt enable FF
C	: Carry FF	Z	: Working register Z	STACK	: Stack
C	: Carry save FF	W	: Working register W	P_t	: Port
Carry	: Carry from ALU	R	: Working register R	M	: Memory
Borrow	: Borrow from ALU	S	: Working register S	[M(DP)]	: Memory contents addressed by DP
DP	: Data pointer	F	: Flag	( )	: Contents
PC	: Program counter	TMFF	: Timer FF	←	: Transfer direction, result
		TIMER	: Timer	⊻	: Exclusive-or

Instruction	Mnemonic		Instruction code $D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Byte	Machine cycle	Operation	Description of operation	skip condition
Accumulator handling instruction	CLA	Clear AC	1 0 0 1	0 0 0 0	1	1	AC←0	The contents of the AC are cleared.	
	CLC	Clear C	0 0 0 0	1 0 1 1	1	1	C←0	The contents of the C are cleared.	
	CMA	Complement AC	0 0 0 1	0 0 0 0	1	1	AC←($\overline{AC}$)	The contents of the AC are complemented.	
	CIA	Complement & Increment AC	0 0 0 1	0 0 0 1	1	1	AC←($\overline{AC}$)+1	The contents of the AC are complemented and incremented by 1. The C is unaffected.	
	INC	Increment AC and skip if Carry	0 0 0 0	1 1 0 1	1	1	AC←(AC)+1 skip if Carry	The contents of the AC are incremented. If carry is generated, the instruction immediately following the INC is skipped. The C is unaffected.	Carry
	DEC	Decrement AC and skip if Borrow	0 0 0 0	1 1 1 1	1	1	AC←(AC)-1 skip if Borrow	The contents of the AC are decremented. If carry is generated, the instruction immediately following the DEC is skipped. The C is unaffected.	Borrow
	STC	Set C	0 0 0 1	1 0 1 1	1	1	C←1	The C is set.	
	XC	Exchange C with C'	0 0 0 1	1 0 1 0	1	1	(C)⇄(C')	The contents of the C and the contents of the C' are exchanged.	
	RAR	Rorate AC Right	0 0 1 1	0 0 0 0	1	1	(C)→A_3,(An)→An-1 (A_0)→C	The contents of the AC are rotated right through the C.	
Memory handling instruction	INM	Increment M skip if Carry	0 0 0 1	1 1 0 1	1	1	M(DP)←[M(DP)]+1 skip if Carry	The contents of the memory M(DP) are incremented. The AC, C are unaffected. If the result is [M(DP)]=0, the instruction immediately following the INM is skipped.	[M(DP)]=0
	DEM	Decrement M skip if Borrow	0 0 0 1	1 1 1 1	1	1	M(DP)←[M(DP)]-1 skip if Borrow	The contents of the memory M(DP) are decremented. The AC, C are unaffected. If the result is [M(DP)]=F, the instruction immediately following the DEM is skipped.	[M(DP)]=F
Arithmetic operation instruction	AD	Add M to AC skip if Carry	0 0 0 0	1 0 0 0	1	1	AC←(AC)+[M(DP)] skip if Carry	Binary addition of the contents of the AC and the contents of the memroy M(DP) is performed and the result is stored in the AC. If carry is generated, the instruction immediately following the AD is skipped.	Carry
	ADS	Add M to AC with C Skip if Carry	0 0 0 0	1 0 0 1	1	1	AC,C←(AC)+[M(DP)]+(C) skip if Carry	Binary addition of the contents of the AC, C and the contents of the memory M(DP) is performed and the result is stored in the AC, C. If carry is generated, the instruction immediately following the ADS is skipped.	Carry
	ADC	Add M to AC with C	0 0 0 1	1 0 0 1	1	1	AC, C←(AC)+[M(DP)]+(C)	Binary addition of the contents of the AC, C and the contents of the memory M(DP) is performed and the result is stored in the AC, C.	
	DAA	Decimal adjust AC in Addition	0 0 0 0	0 1 1 0	1	1	AC←(AC)+6	6 is added to the AC. The C is unaffected. This instruction is used for decimal addition adjust.	
	DAS	Decimal adjust AC in Subtraction	0 0 0 0	1 0 1 0	1	1	AC←(AC)+10	10 is added to the AC. The C is unaffected. This instruction is used for decimal subtraction adjust.	
	EXL	Exclusive OR Logic	0 0 0 1	1 0 0 0	1	1	AC←(AC)⊻[M(DP)]	The contents of the AC and the contents of the memory M(DP) are exclusive-or'd and the result is stored in the AC.	
Load/store instruction	LI*	Load AC with Immediate data	1 0 0 1	$I_3I_2I_1I_0$	1	1	AC←$I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ are loaded in the AC.	
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP)←(AC)	The contents of the AC are stored in the memory M(DP).	
	L	Load AC with M	0 0 1 1	1 0 0 0	1	1	AC←[M(DP)]	The contents of the memory M(DP) are loaded in the AC.	
	LM	Load AC with M and Modify DP_H	0 0 1 1	1 0 M_1M_0	1	1	AC←[M(DP)] DP_H←(DP_H)⊻M_1M_0	The contents of the memory M(DP) are loaded in the AC and then the DP_H is modified with the DP_H⊻M_1M_0.	
	X	Exchange AC with M	0 0 1 0	1 0 0 0	1	1	(AC)⇄[M(DP)]	The contents of the memory M(DP) and the contents of the AC are exchanged.	
	XM	Exchange AC with M and Modify DP_H	0 0 1 0	1 0 M_1M_0	1	1	(AC)⇄[M(DP)] DP_H←(DP_H)⊻M_1M_0	The contents of the memory M(DP) and the contents of the AC are exchanged and then the DP_H is modified with the DP_H⊻M_1M_0.	

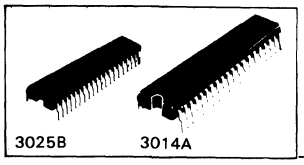
Instruction	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Byte	Machine cycle	Operation	Description of operation	skip condition
Load/store instruction	XD	Exchange AC with M then Decrement DP_L	0 0 1 0	1 1 0 0	1	2	(AC)⇄[M(DP)] DP_L←(DP_L)-1 skip if Borrow	The contents of the memory M(DP) and the contents of the AC are exchanged and then the contents of the DP_L are decremented. If the result is (DP_L)=F, the instruction immediately following the XD is skipped.	(DP_L)=F
	XMD	Exchange AC with M and Modify DP_H then Decrement DP_L	0 0 1 0	1 1 M_1M_0	1	2	(AC)⇄[M(DP)] DP_H←(DP_H)∨M_1M_0 DP_L←(DP_L)-1 skip if Borrow	The contents of the memory M(DP) and the contents of the AC are exchanged and then the DP_H is modified with the (DP_H)∨M_1M_0 and the contents of the DP_L are decremented. If the result is (DP_L)=F, the instruction immediately following the XMD is skipped.	(DP_L)=F
	XI	Exchange AC with M and Increment DP_L	0 0 1 1	1 1 0 0	1	2	(AC)⇄[M(DP)] DP_L←(DP_L)+1 skip if Carry	The contents of the memory M(DP) and the contents of the AC are exchanged and then the contents of the DP_L are incremented. If the result is (DP_L)=0, the instruction immediately following the XI is skipped.	(DP_L)=0
	XMI	Exchang AC with M and Modify DP_H then Increment DP_L	0 0 1 1	1 1 M_1M_0	1	2	(AC)⇄[M(DP)] DP_H←(DP_H)∨M_1M_0 DP_L←(DP_L)+1 skip if Carry	The contents of the memory M(DP) and the contents of the AC are exchanged and then the DP_H is modified with the (DP_H)∨M_1M_0 and the contents of the DP_L are incremented. If the result is (DP_L)=0, the instruction immediately following the XMI is skipped.	(DP_L)=0
Data pointer handling instruction	LDI	Load DP with Immediate data	0 0 0 1 0 $I_6I_5I_4$	0 1 0 1 $I_3I_2I_1I_0$	2	2	DP_H←$I_6I_5I_4$ DP_L←$I_3I_2I_1I_0$	The DP is loaded with the 2nd byte immediate data I_6 to I_0.	
	LDZ	Load DP_H and DP_L with Zero and immediate data respectively	1 0 0 0	$I_3I_2I_1I_0$	1	1	DP_H←0 DP_L←$I_3I_2I_1I_0$	The DP_H is loaded with 0 and the DP_L with the immediate data $I_3I_2I_1I_0$.	
	DED	Decrement DP	0 0 0 1	0 0 1 1	1	1	DP_L←(DP_L)-1 skip if Borrow	The contents of the DP_L are decremented. If the result is (DP_L)=F, the instruction immediately following the DED is skipped.	(DP_L)=F
	IND	Increment DP	0 0 1 1	0 0 1 1	1	1	DP_L←(DP_L)+1 skip if Carry	The contents of the DP_L are incremented. If the result is (DP_L)=0, the instruction immediately following the IND is skipped.	(DP_L)=0
	TAL	Transfer AC to DP_L	0 0 0 0	0 1 1 1	1	1	DP_L←(AC)	The contents of the AC are transferred to the DP_L.	
	TLA	Transfer DP_L to AC	0 0 0 1	0 0 1 0	1	1	AC←(DP_L)	The contents of the DP_L are transferred to the AC.	
Working register handling instruction	XHX	Exchange DP_H with X	0 1 0 0	1 1 1 1	1	2	(DP_H)⇄(X)	The contents of the DP_H and the contents of the working register X are exchanged.	
	XLY	Exchange DP_L with Y	0 1 0 0	1 1 1 0	1	2	(DP_L)⇄(Y)	The contents of the DP_L and the contents of the working register Y are exchanged.	
	THX	Transfer DP_H to X	0 1 0 0	0 1 1 1	1	2	X←(DP_H)	The contents of the DP_H are transferred to the working register X.	
	TLY	Transfer DP_L to Y	0 1 0 0	0 1 1 0	1	2	Y←(DP_L)	The contents of the DP_L are transferred to the working register Y.	
	XAZ	Exchange AC with Z	0 1 0 0	1 0 1 0	1	2	(AC)⇄(Z)	The contents of the AC and the contents of the working register Z are exchanged.	
	XAW	Exchange AC with W	0 1 0 0	1 0 1 1	1	2	(AC)⇄(W)	The contents of the AC and the contents of the working register W are exchanged.	
	TAZ	Transfer AC to Z	0 1 0 0	0 0 1 0	1	2	Z←(AC)	The contents of the AC are transferred to the working register Z.	
	TAW	Transfer AC to W	0 1 0 0	0 0 1 1	1	2	W←(AC)	The contents of the AC are transferred to the working register W.	
	XHR	Exchange DP_H with R	0 1 0 0	1 1 0 1	1	2	(DP_H)⇄(R)	The contents of the DP_H and the contents of the working register R are exchanged.	
	XLS	Exchange DP_L with S	0 1 0 0	1 1 0 0	1	2	(DP_L)⇄(S)	The contents of the DP_L and the contents of the working register S are exchanged.	
Bit handling instruction	SMB	Set Memory data Bit	0 1 1 1	1 0 B_1B_0	1	1	M(DP,B_1,B_0)←1	A single bit of the memory specified by the DP which is designated by 2 bits (B_1,B_0) of the instruction is set.	
	RMB	Reset Memory data Bit	0 1 1 0	1 0 B_1B_0	1	1	M(DP,B_1,B_0)←0	A single bit of the memory specified by the DP which is designated by 2 bits (B_1,B_0) of the instruction is reset.	
	TMB	Test Memory data Bit	0 1 0 1	1 0 B_1B_0	1	1	skip if [M(DP,B_1,B_0)]=1	A signle bit of the memory specified by the DP which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the TMB is skipped.	[M(DP,B_1,B_0)]=1
	TAB	Test AC Bit	0 0 1 0	0 1 B_1B_0	1	1	skip if [AC(B_1,B_0)]=1	A single bit of the contents of the AC which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the TAB is skipped.	[AC(B_1,B_0)]=1
	CMB	Compare AC bit with M data Bit	0 0 1 1	0 1 B_1B_0	1	1	skip if [AC(B_1,B_0)]=[M(DP,B_1,B_0)]	The bit of the contents of the AC and the bit of the contents of the memory M(DP) which are designated by 2 bits (B_1,B_0) of the instruction are compared, and if equal the instruction immediately following the CMB is skipped.	[AC(B_1,B_0)]=[M(DP,B_1,B_0)]
	SFB	Set Flag Bit	0 1 1 1	1 1 B_1B_0	1	2	F(B_1,B_0)←1	A single bit out of flag 4 bits which is designated by 2 bits (B_1,B_0) of the instruction is set.	

Instruction	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Byte	Machine cycle	Operation	Description of operation	skip condition
Flag handling instruction	RFB	Reset Flag Bit	0 1 1 0	1 1 B_1B_0	1	2	$F(B_1,B_0)\leftarrow 0$	A single bit out of flag 4 bits which is designated by 2 bits (B_1,B_0) of the instruction is reset.	
	FBT	Test Flag Bit skip if True	0 1 0 1	1 1 B_1B_0	1	2	skip if $[F(B_1,B_0)]=1$	A single bit out of flag 4 bits which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the FBT is skipped.	$[F(B_1,B_0)]=1$
	FBF	Test Flag Bit, skip if False	0 0 1 0	0 0 B_1B_0	1	2	skip if $[F(B_1,B_0)]=0$	A single bit out of flag 4 bits which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 0 the instruction immediately following the FBF is skipped.	$[F(B_1,B_0)]=0$
Comparison instruction	CM	Compare AC with M	0 0 0 0	1 1 0 0	1	1	skip if $(AC)=[M(DP)]$	The contents of the AC and the contents of the memory M(DP) are compared, and if equal the instruction immediately following the CM is skipped.	$(AC)=[M(DP)]$
	CI	Compare AC with Immediate data	0 0 0 1 1 1 0 0	0 1 1 1 $I_3I_2I_1I_0$	2	2	skip if $(AC)=I_3I_2I_1I_0$	The contents of the AC and the immediate data $I_3I_2I_1I_0$ are compared, and if equal the instruction immediately following the CI is skipped.	$(AC)=I_3I_2I_1I_0$
	CLI	Compare DP_L with Immediate data	0 0 0 1 1 1 1 0	0 1 1 0 $I_3I_2I_1I_0$	2	2	skip if $(DP_L)=I_3I_2I_1I_0$	The contents of the DP_L and the immediate data $I_3I_2I_1I_0$ are compared, and if equal the instruction immediately following the CLI is skipped.	$(DP_L)=I_3I_2I_1I_0$
Skip instruciton	TC	Test Carry	0 0 0 0	0 1 0 0	1	1	skip if $(C)=1$	The contents of the carry FF are tested, and if set the instruction immediately following the TC is skipped.	$(C)=1$
	TTM	Test Timer	0 0 0 0	0 1 0 1	1	1	skip if $(TMFF)=1$	The contents of the timer FF are tested, and if set the instruction immediately following the TTM is skipped.	$(TMFF)=1$
	TIT	Test Interrupt FF	0 0 0 0	0 0 1 1	1	1	skip if $(INT\ FF)=1$ $INT\ FF\leftarrow 0$	The contents of the interrupt FF are tested, and if set the instruction immediately following the TIT is skipped. Then the contents of the interrupt FF are reset.	$(INT\ FF)=1$
Jump instruction	JCP	Jump in the Current Page	1 1 P_5P_4	$P_3P_2P_1P_0$	1	1	$PC\leftarrow P_5$ to P_0	A jump is made to the address which is designated by setting P_5 to P_0 in the low-order 6 bits of the PC.	
	JMP	Jump unconditionally	1 0 1 0 $P_7P_6P_5P_4$	$0P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	$PC\leftarrow P_{10}$ to P_0	A jump is made to the address designated with P_{10} to P_0.	
	JPA	Jump in the Current Page modified by AC	0 1 0 0	0 0 0 1	1	2	$PC\leftarrow A_3A_2A_1A_0\ 00$	A jump is made to the address which is designated by setting $A_3A_2A_1A_0$ and 00 in the high-order 4 bits and the low-order 2 bits of the low-order 6 bits of the PC respectively.	
	EI	Enable Interrupt	0 0 1 1	0 0 0 1	1	1	$INTE\ FF\leftarrow 1$	Interrupt is enabled.	
	DI	Disable Interrupt	0 0 0 0	0 0 0 1	1	1	$INTE\ FF\leftarrow 0$	Interrupt is desabled.	
Subroutine instruction	CZP	Call subroutine in the Zero Page	1 0 1 1	$P_5P_4P_3P_2$	1	1	$(PC+1)\rightarrow STACK$ $PC\leftarrow 00000P_5P_4P_3P_2 00$	1-word call instruciton to page 0.	
	CAL	Call subroutine	1 0 1 0 $P_7P_6P_5P_4$	$1P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	$(PC+2)\rightarrow STACK$ $PC\leftarrow P_{10}$ to P_0	Subroutine is called.	
	RT	Return from subroutine	0 1 0 0	1 0 0 0	1	2	$PC\leftarrow(STACK)$	Program execution is returned from subroutine.	
	RTS	Return from subroutine and Skip	0 1 0 0	1 0 0 1	1	2	$PC\leftarrow(STACK)$ skip unconditionally	Program execution is returned from subroutine and skipped.	Unconditional
I/O instruction	SEB	Set port E Bit	0 1 1 1	0 1 B_1B_0	1	2	$Pt\ E(B_1,B_0)\leftarrow 1$	A single bit of the output port E which is designated by 2 bits (B_1,B_0) of the instruction is set.	
	REB	Reset port E Bit	0 1 1 0	0 1 B_1B_0	1	2	$Pt\ E(B_1,B_0)\leftarrow 0$	A single bit of the output port E which is designated by 2 bits (B_1,B_0) of the instruciton is reset.	
	SPB	Set any Port Bit	0 1 1 1	0 0 B_1B_0	1	2	$Pt(DP_L,B_1,B_0)\leftarrow 1$	A single bit of the output port specified by the DP_L which is designated by 2 bits (B_1,B_0) of the instruction is set.	
	RPB	Reset any Port Bit	0 1 1 0	0 0 B_1B_0	1	2	$Pt(DP_L,B_1,B_0)\leftarrow 0$	A single bit of the output port specified by the DP_L which is designated by 2 bits (B_1,B_0) of the instruction is reset.	
	TPA	Test Port A Bit	0 1 0 1	0 1 B_1B_0	1	2	skip if $[PtA(B_1,B_0)]=1$	A single bit of the input port A designated by the instruction bit (B_1,B_0) is tested, and if 1 the instruction immediately following the TPA is skipped.	$[PA(B_1,B_0)]=1$
	TPB	Test any Port Bit	0 1 0 1	0 0 B_1B_0	1	1	skip if $[Pt(DP_L,B_1,B_0]=1$	A single bit of the input port specified by the DP_L which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the TPB is skipped.	$[P(DP_L,B_1,B_0)]=1$
	OE	Output AC to port E (Output PLA to port E and F)	0 1 0 0	0 1 0 0	1	2	$PtE\leftarrow(AC)$ (or $PtE,F\leftarrow PLA(AC)$)	The contents of the AC are outputted to the output port E. Or the contents of the PLA designated by the AC outputted to output ports E, F. (Selectable)	
	OP	Output AC to any Port	0 0 0 0	1 1 1 0	1	1	$Pt(DP_L)\leftarrow(AC)$	The contents of the AC are outputted to the output port designated by the DP_L.	
	OCD	Output immediate data to port C and D	0 0 0 1 $I_7I_6I_5I_4$	1 1 1 0 $I_3I_2I_1I_0$	2	2	$PtD\leftarrow I_7I_6I_5I_4$ $PtC\leftarrow I_3I_2I_1I_0$	The immediate data I_7 to I_4 and I_3 to I_0 are outputted to port D and port C respectively.	

Instruction		Mnemonic	Instruction code		Byte	Machine cycle	Operation	Description of operation	skip condition
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$					
I/O instruction	SETD	Set port C and D Bit	0 0 0 1	1 1 0 0	1	2	PtC,D(DP_L)←1	A single bit of the output ports C, D which is designated by the DP_L is set.	
	RSTD	Reset port C and D Bit	0 1 0 0	0 1 0 1	1	2	PtC,D(DP_L)←0	A single bit of the output ports C, D which is designated by the DP_L is reset.	
	IA	Input port A in AC	0 1 0 0	0 0 0 0	1	2	AC←(PtA)	The contents of the input port A are inputted to the AC.	
	IP	Input any Port in AC	0 0 1 1	0 0 1 0	1	1	AC←[Pt(DP_L)]	The contents of the input port designated by the DP_L are inputted to the AC.	
Others	STM	Set Timer	0 0 0 1 $I_7I_6I_5I_4$	0 1 0 0 $I_3I_2I_1I_0$	2	2	TMFF←0 TIMER←I_7 to I_0	The timer FF is reset. The program data are set in the timer and the timer start is instructed.	
	NOP	No Operation	0 0 0 0	0 0 0 0	1	1	No Operation	No operation. 1 machine cycle is consumed.	

* : If the LI instruction (including CLA instruction) are stacked, the LI instructions after the 2nd instruction are NOP.

LM6402L, 6405L



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1528

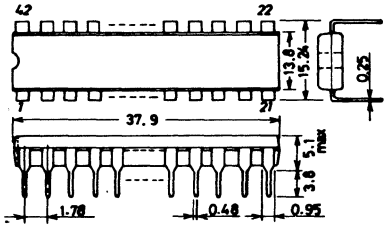
General Description

The LM6402L/6405L are single-chip 4-bit N channel MOS microcomputers intended for use in control-oriented applications. They contain a ROM (2048 bytes (2K bytes)), a RAM (128 x 4 bits), an ALU, I/O ports (35 pins), a timer, a clock generator, and a PLA on single chips.

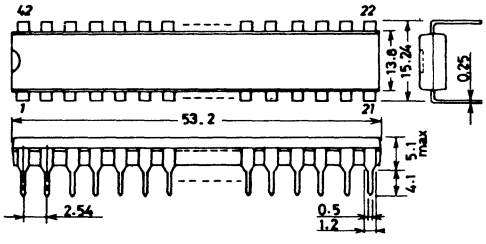
(1) Hardware features (Reduction in external parts)
- Low current dissipation (I_{DD} = 10 mA/5 V typ.)
- Wide V_{DD} range (V_{DD} = 4.5 to 9.5 V)
- Single 5 V supply, N channel E/D MOS
- C MOS, TTL compatible
- Output ports with LED driver (2 ports/8 pins)
- 24-character PLA
- Input/output common ports (7 ports/27 pins)
- Flexible output configuration (Open drain/pull-up resistor)
- Clock generator (CR connected externally)
- Cycle time 20 μs
- 1K bytes/2K bytes pin-compatible
- Input threshold valtage selectable (Normal/high threshold)
- Initial reset and external interrupt input pins with Schmitt gate

(2) Software features (Effective use of ROM capacity)
- 4-level subroutine nesting
- Interrupt function (External/internal)
- Programmable timer with wide setting range (Timer, pulse count, pulse width measure)
- Powerfull instruction set with 82 instructions
- Automatic page select
- 1K bytes/2K bytes instruction-compatible

Case Outline 3025B-D42SIC
(unit: mm)



Case Outline 3014A-D42IC
(unit: mm)

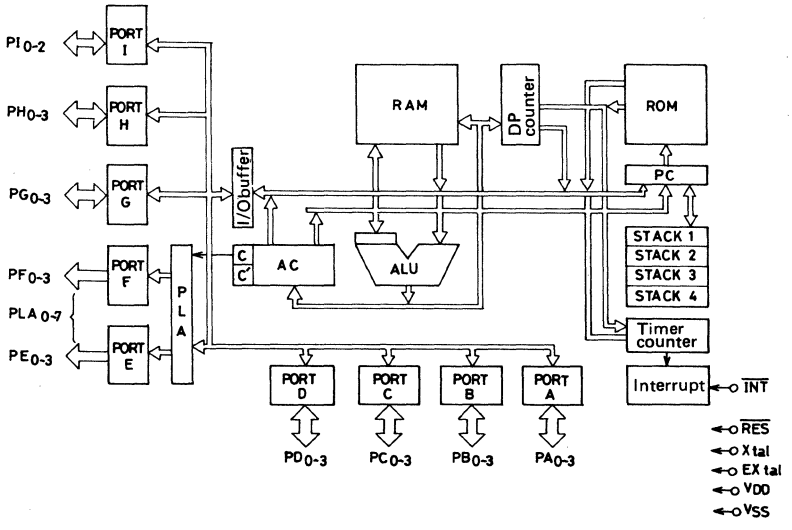


For details, refer to LM6400 Series User's Manual.

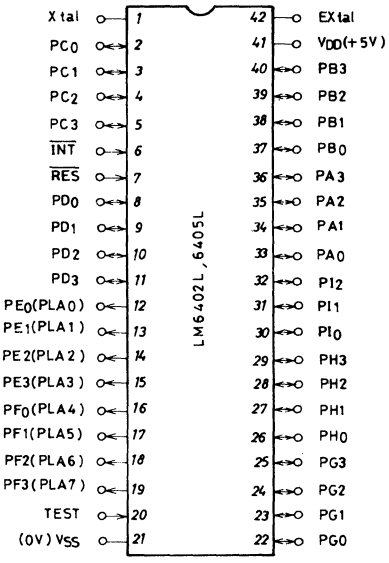
The LM6400 series include Type Nos. shown below and have various uses.

Type No.	Use	ROM	RAM	Cycle Time	I_{DD} (typ)	Case Outline	Remarks
LM6402A	General	2 K bytes	128 x 4 bits	10 μs	30 mA	DIP-42 DIP-42S	
LM6405A	General	1K bytes	64 x 4 bits	10 μs	30 mA	DIP-42 DIP-42S	
LM6402H	Medium-speed	2K bytes	128 x 4 bits	5 μs	35 mA	DIP-42 DIP-42S	
LM6405H	Medium-speed	1K bytes	64 x 4 bits	5 μs	35 mA	DIP-42 DIP-42S	
LM6402G	High-speed	2K bytes	128 x 4 bits	3 μs	38 mA	DIP-42 DIP-42S	
LM6405G	High-speed	1K bytes	64 x 4 bits	3 μs	38 mA	DIP-42 DIP-42S	
LM6402L	Low-power	2K bytes	128 x 4 bits	20 μs	10 mA	DIP-42 DIP-42S	
LM6405L	Low-power	1K bytes	64 x 4 bits	20 μs	10 mA	DIP-42 DIP-42S	
LM6416E	Small-scale	1K bytes	64 x 4 bits	4 μs	17 mA	DIP-28S	
LM6499	Evaluation chip for LM6402A, H, L, G and LM6405A, H, L, G	External 2K bytes		5 ~ 10 μs	30 mA	QIC-80	
LM6497	Evaluation chip for LM6416E	External 2K bytes		5 ~ 10 μs	20 mA	QIC-80	

System Block Diagram [LM6402L, 6405L]



Package and Pin Assignment



Pin Name

Xtal, EXtal	: OSC CR
$\overline{INT}$	: Interupt
$\overline{RES}$	: Reset
PA_{0-3}	: Input/output ports A_{0-3}
PB_{0-3}	: Input/output ports B_{0-3}
PC_{0-3}	: Input/output ports C_{0-3}
PD_{0-3}	: Input/output ports D_{0-3}
PE_{0-3} (PLA$_{0-3}$)	: Output ports E_{0-3} (PLA output $_{0-3}$)
PF_{0-3} (PLA$_{4-7}$)	: Output ports F_{0-3} (PLA output $_{4-7}$)
PG_{0-3}	: Input/output ports G_{0-3}
PH_{0-3}	: Input/output ports H_{0-3}
PI_{0-2}	: Input/output ports I_{0-2}
TEST	: Test

Pin Description

Pin Name	Input/Output	Functions
$\overline{INT}$	Input	Interrupt request input pin
$\overline{RES}$	Input	Reset input pin
PA_{0-3}	Input Input/output (Note 1)	Input/output ports A_0 to A_3 Capable of 4-bit input and single-bit test during input Capable of 4-bit output and single-bit set/reset during output
PB_{0-3}	Input Input/output (Note 1)	Input/output ports B_0 to B_3 Capable of 4-bit input and single-bit test during input Capable of 4-bit output and single-bit set/reset during output
PC_{0-3}	Input/output	Input/output ports C_0 to C_3 Capable of 4-bit input and single-bit test during input Capable of 4-bit output and single-bit set/reset and also immediate data output during output
PD_{0-3}	Input/output	Input/output ports D_0 to D_3 Capable of 4-bit input and single-bit test during input Capable of 4-bit output and single-bit set/reset and also immediate data output during output
PE_{0-3}	Output	Output ports E_0 to E_3 Capable of 4-bit output and single-bit set/reset PLA output is delivered at this pin and PF_{0-3}.
PF_{0-3}	Output	Output ports F_0 to F_3 Capable of 4-bit output and single-bit set/reset PLA output is delivered at this pin and PE_{0-3}.

Pin Name	Input/Output	Functions
$PG_{0\text{-}3}$	Input Input/output Output (Note)	Input/output ports G_0 to G_3 Capable of 4-bit input and single-bit test during input Capable of 4-bit output and single-bit set/reset during output
$PH_{0\text{-}3}$	Input Input/output Output (Note 1)	Input/output ports H_0 to H_3 Capable of 4-bit input and single-bit test during input Capable of 4-bit output and single-bit set/reset output
$PI_{0\text{-}2}$	Input/output	Input/output ports I_0 to I_2 Capable of 3-bit input and single-bit test during input Capable of 3-bit output and single-bit set/reset during output
Xtal	Input/output	Pin for internal clock generation C, R are connected to this pin and EXtal pin. When supplying clock externally, this pin must be open.
EXtal	Input	Pin for supplying clock externally When using internal clock generation, C, R are connected to this pin and Xtal pin.
V_{DD}	Input	Power supply pin Normally connected to +5 V
V_{SS}	–	Connected to 0 V of power supply
TEST	Input	LSI test pin Normally connected to V_{SS} (0 V)

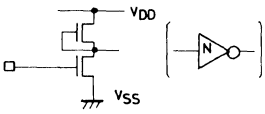
(Note 1): Mask-programming can be used to select input, input/output, output.

Input/Output Select Table

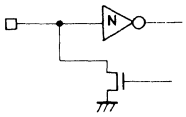
Option \ Port	A	B	C	D	E	F	G	H	I
Input only	N H	N H					N H	N H	
Output only					OD	OD	OD PU	OD PU	
Input/output common	N,OD H,OD	N,OD H,OD	N,OD N,PU H,OD H,PU	N,OD N,PU H,OD H,PU			N,OD N,PU H,OD H,PU	N,OD N,PU H,OD H,PU	N,OD H,OD

N: Normal input gate
H: High threshold input gate
OD: Open drain output
PU: Output with pull-up resistance

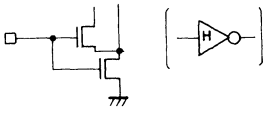
Input only, normal input gate (N)



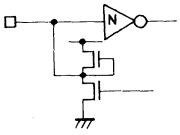
Input/output common, normal input, open drain output (N, OD)



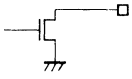
Input only, high threshold input gate (H)



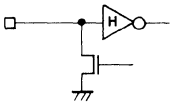
Input/output common, normal input, output with pull-up resistor (N, PU)



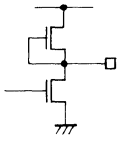
Output only, open drain output (OD)



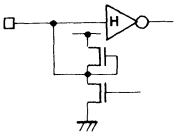
Input/output common, high threshold input, open drain output (H, OD)



Output only, output with pull-up resistor (PU)



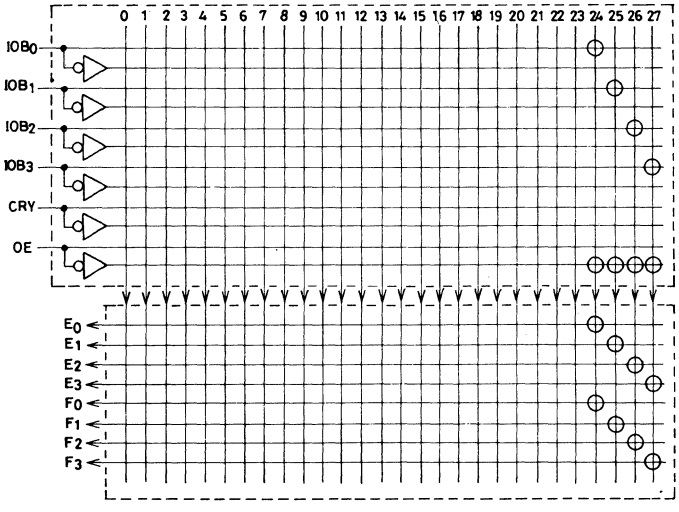
Input/output common, high threshold input, output with pull-up resistor (H, PU)



PLA for E, F ports

User-selected mask programmable

AND matrix



OR matrix

Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0 V				Unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +10	V
Input Voltage	V_{IN}		−0.3 to +12	V
Output Voltage	V_{OUT}	Output transistor OFF	−0.3 to +12	V
Average Output Current (Note 1)	I_{OHA}	Each pin with pull-up resistor	−2.0 to 0	mA
	I_{OLA} (1)	All pins of C, D ports	0 to 20	mA
	I_{OLA} (2)	Each pin of E, F ports	40	mA
	I_{OLA} (3)	All pins of E ports or F ports	0 to 100	mA
	I_{OLA} (4)	All pins of A, B, G, H, I ports	0 to 50	mA
Peak Output Current (Note 2)	I_{OHP}	Each pin with pull-up resistor	−2.0 to 0	mA
	I_{OLP} (1)	Each output pin of ports other than E, F ports	0 to 4	mA
	I_{OLP} (2)	Each pin of E, F ports	0 to 40	mA
	I_{OLP} (3)	All pins of E ports or F ports	0 to 100	mA
Allowable Power Dissipation	P_d max	T_a = 0 ~ +70°C	600	mW
Operating Temperature	T_{opg}		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

(Note 1); Applicable to any 100 ms period
(Note 2): Must not be exceeded even momentarily.

Allowable Operating Ranges/T_a = 0 ~ +70°C, V_{DD} = 4.5 ~ 9.5 V, V_{SS} = 0 V			min	typ	max	unit
Operating Voltage	V_{DD}		4.5	5.0	9.5	V
Port (input only and input/output common), normal input						
Input "H" Level Voltage	V_{IH} (1)	Input/output port configuration (N), (N, OD), (N, PU)	2.2		V_{DD}	V
Input "L" Level Voltage	V_{IL} (1)	Input/output port configuration (N), (N, OD), (N, PU)	V_{SS}		0.6	V
Port (input only and input/output common), high threshold input common						
Input "H" Level Voltage	V_{IH} (2)	Input/output port configuration (H), (H, OD), (H, PU)	0.6V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL} (2)	Input/output port configuration (H), (H,OD), (H, PU)	V_{SS}		0.3V_{DD}	V
$\overline{INT}$, $\overline{RES}$						
Input "H" Level Voltage	V_{IH} (3)		0.7V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL} (3)		V_{SS}		0.3V_{DD}	V
EXtal						
Input "H" Level Voltage	V_{IH} (4)		0.7V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL} (4)		V_{SS}		0.6	V
Clock Cycle Time	t_c (ϕ)	See Fig. 1.	5		10	μs
"H" Level Clock Pulse Width	$t_{W\phi H}$	See Fig. 1.	1.4			μs
"L" Level Clock Pulse Width	$t_{W\phi L}$	See Fig. 1.	2.7			μs
External Resistor Value for Oscillation	R	See Fig. 2.		39±2 %		kΩ
External Capacitor value for Oscillation	C	See Fig. 2.		100±5 %		pF
TEST						
Input "L" Level Voltage	V_{IL} (5)		V_{SS}		0.4	V

* For (N), (H), (N, OD), (N, PU), (H, OD), (H, PU), refer to the Input/Output Select Table.

Electrical Characteristics/T_a = 0 ~ +70°C, V_{DD} = 4.5 ~ 9.5 V, V_{SS} = 0 V			min	typ	max	unit
Port (input only) and $\overline{RES}$, $\overline{INT}$						
Input "H" Level Current	I_{IH} (1)	Input/output port configuration (N), (H), $V_{IN} = V_{DD}$			10	μA
Input "L" Level Current	I_{IL} (2)	Input/output port configuration (N), (H), $V_{IN} = V_{SS}$	−10			μA
Port (input/output common), open drain output						
Input "H" Level Current	I_{IH} (2)	Input/output port configuration (N, OD), (H, OD), $V_{IN} = V_{DD}$			10	μA
Input "L" Level Current	I_{IL} (3)	Input/output port configuration (N, OD), (H, OD), $V_{IN} = V_{SS}$	−10			μA
Port (input/output common), output with pull-up resistor						
Input "L" Level Current	I_{IL} (1)	Input/output port configuration (N, PU), (H, PU) V_{DD} = 5 V±10 %, V_{IN} = 0.4 V	−1.6			mA
TEST pin, input						
Input "L" Level Current	I_{IL} (4)	$V_{IN} = V_{SS}$	−20			μA
Port (output only or input/output common), output with pull-up resistor						
Output "L" Level Current	I_{OL} (1)	Input/output port configuration (PU), (N, PU), (H, PU), V_{DD} = 4.5 V, V_{OL} = 0.4 V	1.6			mA
	I_{OL} (2)	Input/output port configuration (PU), (N, PU), (H, PU), V_{DD} = 9.5 V, V_{OL} = 0.4 V	3.5			mA
Output "H" Level Current	I_{OH} (1)	Input/output port configuration (PU), (N, PU), (H, PU), V_{DD} = 4.5 V, V_{OH} = 2.25 V	−190		−26	μA
	I_{OH} (2)	Input/output port configuration (PU), (N, PU), (H, PU), V_{DD} = 9.5 V, V_{OH} = 4.75 V	−450		−40	μA
Port (output only or input/output common), open drain output						
Output "L" Level Current	I_{OL} (3)	Input/output port configuration (OD), (N, OD), (H, OD), V_{DD} = 4.5 V, V_{OL} = 0.4 V	1.8			mA
	I_{OL} (4)	Input/output port configuration (OD), (N, OD), (H, OD), V_{DD} = 9.5 V, V_{OL} = 0.4 V	4.0			mA
Output OFF Leak Current	I_{OFF} (1)	Input/output port configuration (OD), (N, OD), (H, OD), V_{OH} = 5.5 V			10	μA
	I_{OFF} (2)	Input/output port configuration (OD), (N, OD), (H, OD), V_{OH} = 10 V			30	μA
E, F port						
Output "L" Level Current	I_{OL} (5)	V_{DD} = 4.5 V, V_{OL} = 2 V	20			mA
	I_{OL} (6)	V_{DD} = 9.5 V, V_{OL} = 2 V	30			mA
Current Dissipation	I_{DD}	All output pins open at oscillation mode, V_{DD} = 5 V, T_a = 25°C				
		LM6402L			12	mA
		LM6405L			10	mA
CR Oscillation Frequency	f_{OSC}	C = 100 pF±5 %, R = 39 kΩ±2 % See Fig. 2.	100		200	kHz
Input Pin Capacitance	C_I			10		pF

* For (N), (H), (N, OD), (H, OD), (H, PU), (OD), (PU), refer to the Input/Output Select Table.

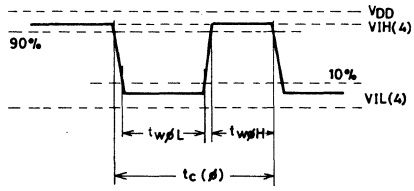


Fig. 1. EXtal input waveform

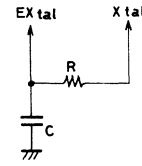


Fig. 2. Recommended oscillation circuit

Application Development Tools

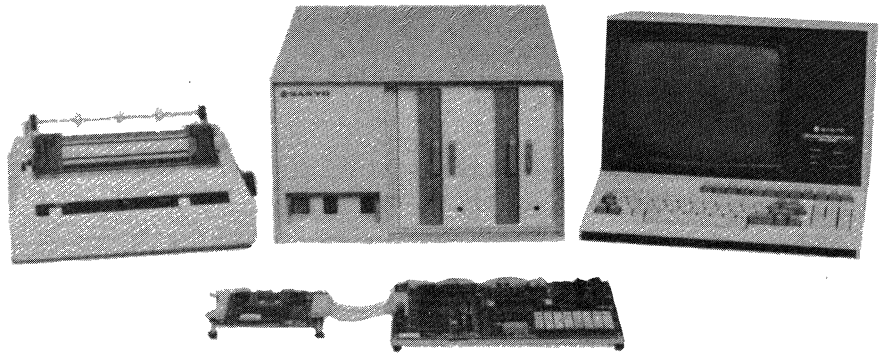
For convenience of application development of the LM6402L/6405L, the evaluation chip (LM6499) and dedicated equipment called "application development tools" are available.

- SDS-410
  This is a combination of floppy disks-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be made (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled or data can be written into EPROM's (using EPROM WRITER function contained in the EVA-410).

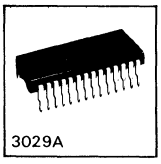
- EVA-410
  This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. By replacing the target board, this kit can be used for application development of CMOS microcomputers (LC6500 series) as well as the LM6400 series.

- EVA-401
  This is a board with an EPROM and the LM6499 combined. This board is used for mounting evaluation or trial production of sets after application development programs are completed.

- LM64PG99
  This is a system evaluation chip intended for application development tool of the single-chip 4-bit microcomputer LM6400 series. A 24-pin socket for program EPROM and PLA EPROM is provided on the package surface. By mounting this chip on the user's application equipment, operation of the equipment can be checked in terms of hardware/software. The LM64PG99 can be used very effectively in equipment made by way of trial.



LM6413E



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer tor Use in Control-Oriented Applications

Ⓔ 1379A

Description

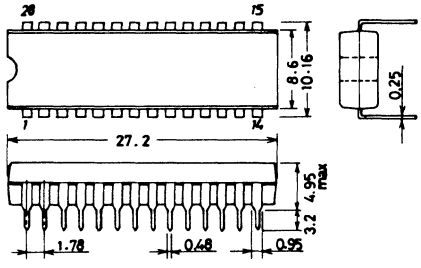
The LM6413E is a single-chip 4-bit N-channel MOS microcomputer intended for use in control-oriented applications. It contains a ROM (2048 bytes (2K bytes)), a RAM (128 x 4 bits), an ALU, I/O ports (21 pins), a timer, and a clock generator. It is a low-end model of the LM6400 series and is suited for use in cost sensitive sets.

(1) Hardware features (Reduction in external parts) : Identical to LM6416E except I_{DD}
- Cycle time : 4 to 40 μs.
- Capable of interfacing direct with 12 V (15 V (max)) peripheral circuits.
- Clock generator. CR oscillation 770 kHz typ., ceramic oscillation 400/800 kHz, drive by external oscillator 1 MHz max.
- All output ports containing LED driver. 5 ports/17 pins, I_{OL}=10 mA/V_{OL}=1.5 V.
- Input/output common ports. 2 ports/8 pins.
- Single 5 V (typ) supply and wide operating range (V_{DD}=4.5 to 6.5 V).
- Initial reset and external pseudo interrupt input pins containing Schmitt gate.

(2) Software features (Effective use of ROM capacity) : Identical to LM6416E except ROM capacity, RAM capacity
- 65 instructions compatible with LM6402/05. Flag manipulation instructions, working register manipulation instructions, carry save instruction are eliminated.
- 2-level subroutine nesting.
- Pseudo interrupt function (External/internal).
- Programmable timer with wide setting range.
- Automatic page select.

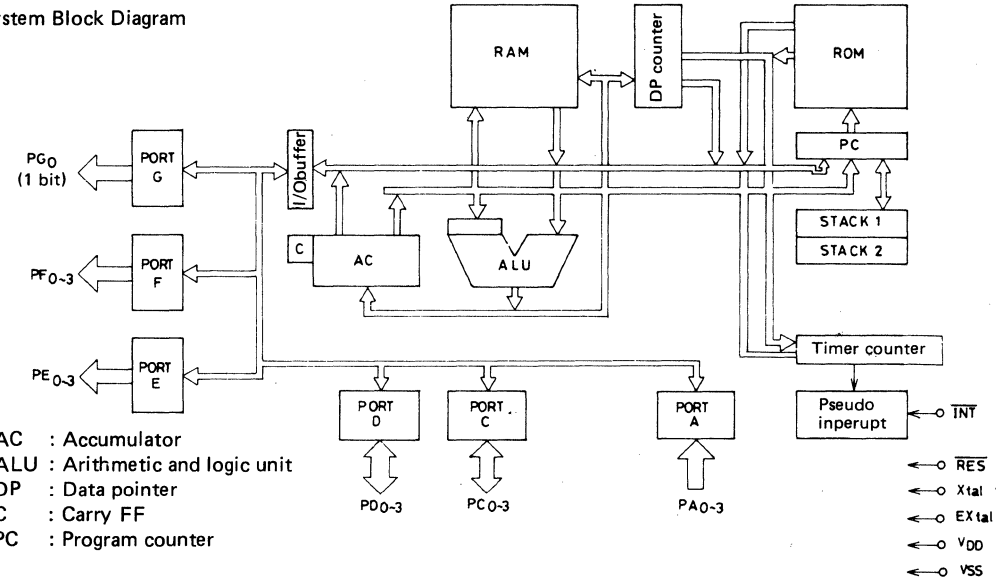
(3) Evaluation chip
- Evaluation chip LM6498 and piggyback LM64PG98 are available for use in the application development of the LM6413E.

Case Outline 3029A-D28SIC
(unit: mm)



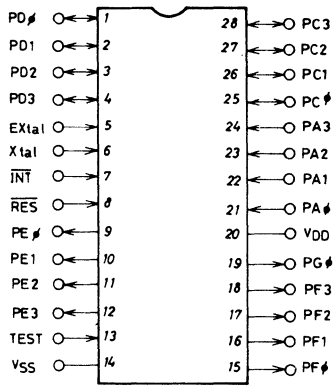
For details, refer to the instruction set table described in the separate catalog and also LM6416 Series User's Manual.

System Block Diagram



AC : Accumulator
ALU : Arithmetic and logic unit
DP : Data pointer
C : Carry FF
PC : Program counter

Package and Pin Assignment



Xtal, Extal	: OSC resonator	
INT	: Interrupt	
RES	: Reset	
PA0 to 3	: Input ports	A0 to 3
PC0 to 3	: Input/output ports	C0 to 3
PD0 to 3	: Input/output ports	D0 to 3
PE0 to 3	: Output ports	E0 to 3
PF0 to 3	: Output ports	F0 to 3
PG0	: Output ports	G0
TEST	: Test	

Pin Name	Input/output	Function
INT	Input	• Peseudo interrupt request input pin.
RES	Input	• Reset input pin.
PA0 to 3	Input	• Input ports A0 to A3. • Capable of 4-bit input and single-bit test.
PC0 to 3	Input/output	• Input/output common ports C0 to C3. • Capable of 4-bit input and single-bit test during input. • Capable of 4-bit output and single-bit set/reset and immediate data output during output.
PD0 to 3	Input/output	• Input/output common ports D0 to D3. • Capable of 4-bit input and single-bit test during input. • Capable of 4-bit output and single-bit set/reset and immediate data output during output.
PE0 to 3	Output	• Output ports E0 to E3. • Capable of 4-bit output and single-bit set/reset.
PF0 to 3	Output	• Output ports F0 to F3. • Capable of 4-bit output and single-bit set/reset.
PG0	Output	• Output ports G0. • Capable of single-bit output and single-bit set/reset.

Xtal	Input/output	• Pin for externally attaching oscillator for internal clock oscillation. • Cermaic resonator or CR is connected to this pin and pin EXtal.
EXtal	Input	• Pin for supplying external clock. • If internal clock oscillation is used, ceramic resonator or CR is connected to this pin and pin Xtal. (Ceramic OSC, CR OSC: Mask option).
V_{DD}	Input	• Power supply pin. Normally connected to +5V.
V_{SS}	–	• Connected to GND of power supply.
TEST	Input	• LSI test pin. Normally connected to V_{SS} (GND).

Absolute Maximum Ratings at T_a =25°C, V_{SS} =0V

			unit
Maximum Supply Voltage	$V_{DD}max$		–0.3 to +8 V
Maximum Input Voltage	$V_{IN}max$	EXtal pin: Up to self-oscillation level	–0.3 to +15 V
Maximum Output Voltage	$V_{OUT}max$	Output transistor: OFF	–0.3 to +15 V
Average Output Current	I_{OLa} 1	Each pin of ports	20 mA
*1	I_{OLa} 2	All pins of C, D ports	100 mA
	I_{OLa} 3	All pins of E, F, G ports	110 mA
Peak Output Current *2	I_{OLp} 1	Each pin of ports	20 mA
	I_{OLp} 2	All pins of C, D ports	120 mA
	I_{OLp} 3	All pins of E, F, G ports	130 mA
Allowable Power Dissipation	$P_d max$	–30°C ~ +70°C	400 mW
Operating Temperature	T_{opg}		–30 to +70 °C
Storage Temperature	T_{stg}		–55 to +125 °C

*1 Applicable to any 100ms period
*2 Must not be exceeded even momentarily.

Alowable Operating Conditions at T_a =–30 to +70°C, V_{SS} =0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		6.5	V
Port Input						
"H" level input voltage	V_{IH} 1		0.6V_{DD}		13.5	V
"L" level input voltage	V_{IL} 1		V_{SS}		0.3V_{DD}	V
$\overline{INT}$, $\overline{RES}$						
"H" level input voltage	V_{IH} 2		0.7V_{DD}		13.5	V
"L" level input voltage	V_{IL} 2		V_{SS}		0.3V_{DD}	V
EXtal (Selecting ceramic oscillation option and applying external clock)						
"H" level input voltage	V_{IH} 3	Xtal open	0.8V_{DD}		V_{DD}	V
"L" level input voltage	V_{IL} 3	Same as above	V_{SS}		1.0	V
Clock cycle	$t_{c\phi}$	Same as above,Refer to Fig. 1.	1.0		10.0	μs
"H" level clock pulse width	$t_{w\phi}H$	Same as above	0.3			μs
"L" level clock pulse width	$t_{w\phi}L$	Same as above	0.47			μs
Oscillator (Selecting ceramic oscillation option)						
External resistance for ceramic oscillation	R_1	Refer to Fig. 2.	900	1000	1100	kohm
External capacitance for ceramic oscillation	C_1	EXtal side 400kHz	200	220	240	pF
		EXtal side 800kHz	200	220	240	pF
	C_2	Xtal side 400kHz	200	220	240	pF
		Xtal side 800kHz	200	220	240	pF
Oscillator (Selecting CR oscillation option)						
External resistance for CR oscillation	R_2	Refer to Fig. 3.	8	10	100	kohm
External capacitance for CR oscillation	C_3	Refer to Fig. 3.	45	68	200	pF
TEST						
"L" level input voltage	V_{IL} 4		V_{SS}		0.4	V

Electrical Characteristics at T_a = −30 to +70°C, V_{DD} = 4.5 to 6.5V, V_{SS} = 0V

A Port $\overline{INT}$, $\overline{RES}$						
"H" level input current	I_{IH1}	V_{IN} = 13.5V			10	μA
"L" level input current	I_{IL1}	V_{IN} = V_{SS}	−10			μA
EXtal						
"H" level input current	I_{IH2}	V_{IN} = V_{DD}			10	μA
"L" level input current	I_{IL2}	V_{IN} = V_{SS}	−10			μA
C, D Port (Output OFF)						
"H" level input current	I_{IH3}	V_{IN} = 13.5V			10	μA
"L" level input current	I_{IL3}	V_{IN} = V_{SS}	−10			μA
C, D, E, F, G Port						
"L" level output current	I_{OL1}	V_{DD} = 4.5V, V_{OL} = 1.5V	10			mA
Output off leak current	I_{OFF1}	V_{OH} = 13.5V			10	μA
CR Oscillation Frequency (Selecting CR oscillation option)			min	typ	max	unit
	f_{OSC1}	C_3* = 68pF, R_2=10kohm *Including stray capacitance of board wiring, etc. T_a = 0 to +70°C	620	770	890	kHz
	f_{OSC2}	Ta = 0 to +70°C, T_a = −30 to +70°C	620	770	960	kHz
Current Dissipation	I_{DD1}	At 800kHz oscilation Output = Open T_a = 0 to +70°C		23	39	mA
	I_{DD2}	Ta = 0 to +70°C, T_a = −30 to +70°C		23	45	mA
Input Pin Capacitance	C_I			10		pF

Fig. 1 Extal Input Waveform

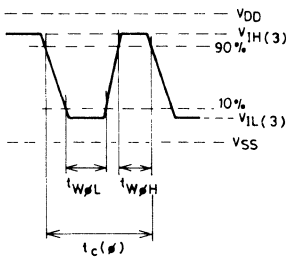
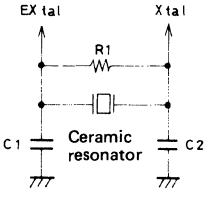
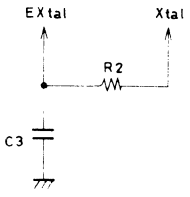


Fig. 2 Recommended Ceramic Oscillator



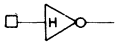
Ceramic : Ceramic resonator
KBR400B (Kyocera)
CSB400P (Murata)
KBR800H (Kyocera)
CSB800A (Murata)

Fig. 3 Recommended CR Oscillator

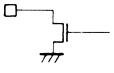


Input/output type of port

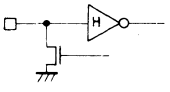
Input only
(high threshold input)



Output only
(open drain output)



Input/output common
(highthreshold input, open drain output)



CR oscillation of LM6413E, LM64PG98

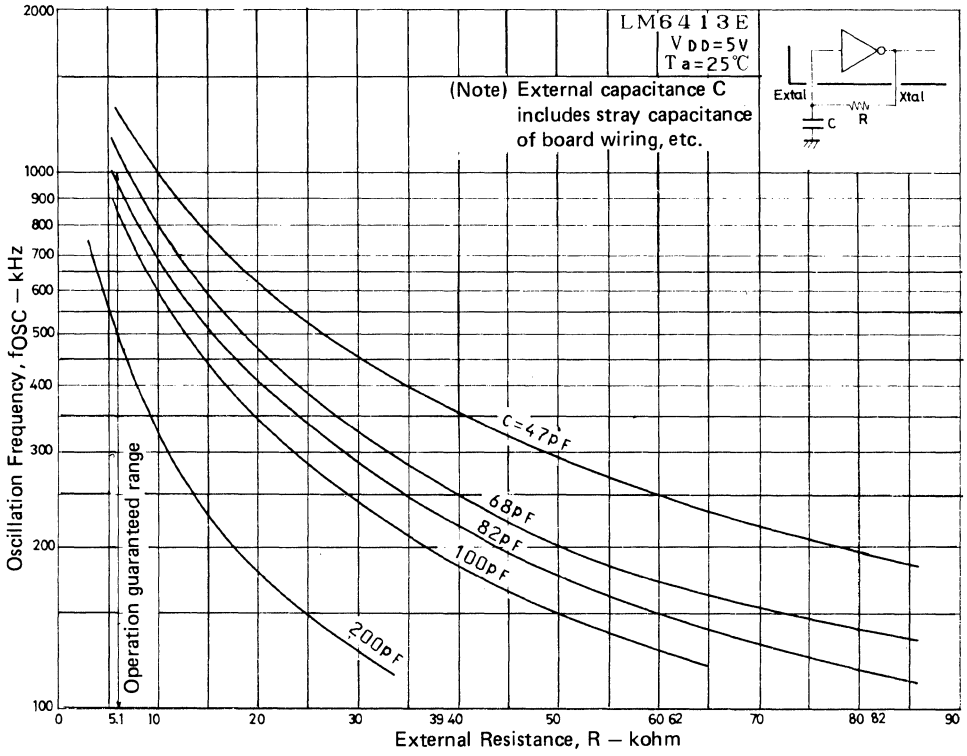
(1) For the variation range of CR oscillation frequency of the LM6413E, the following are guaranteed at external constants of (C=68pF, R=10 kohm) only.

min typ max

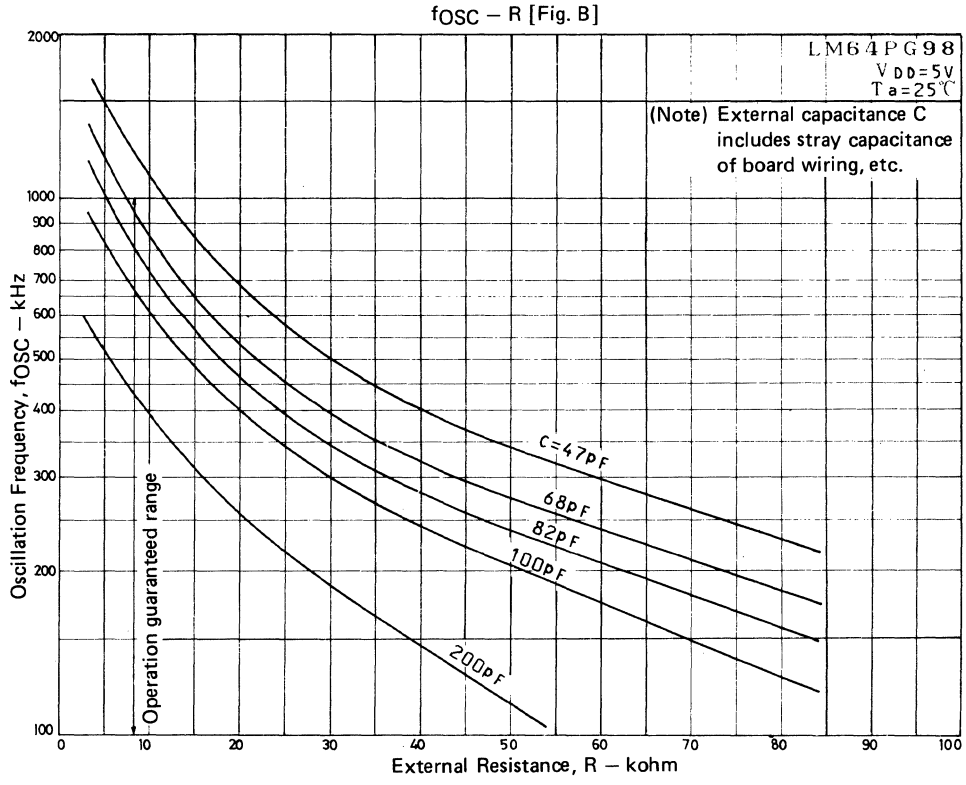
① f_{OSC} 1 = 620 to 770 to 890 kHz/ T_a = 0 to +70°C

② f_{OSC} 2 = 620 to 770 to 960 kHz/ T_a = -30 to 70°C

fOSC – R [Fig. A]



fOSC – R [Fig. B]



(2) If other frequency than typical value 770 kHz is used at other constants than (C =68pF, R = 10kohm), fix CR constants referring to "oscillation frequency vs. standard external resistance characteristics "in Fig. A. In this case, take care of the following.

1) Oscillation cycle period must be within the range (1 to 10 μs) of recommended operation clock cycle period at EXtal pin.
2) CR constants must be selected from among recommended external constants (C = 45 to 200pF, R = 8 to 100 kohm).

It should be noted that outgoing inspection is performed under the frequency variation condition at (C = 68pF, R = 10kohm).

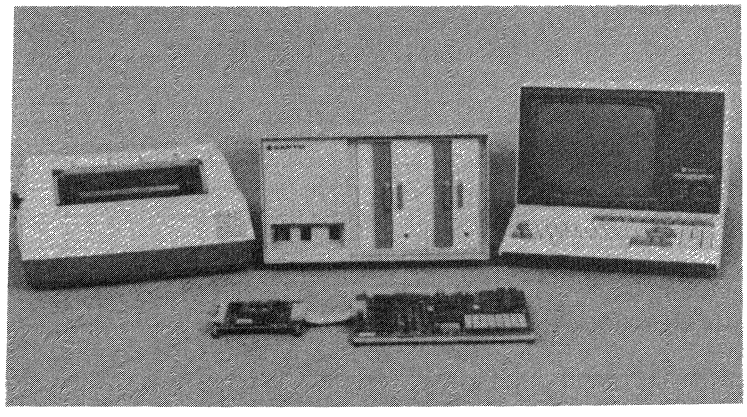
(3) CR constants of the LM64PG98 are also fixed referring to "oscillation frequency vs. standard external resistance characteristics" in Fig. B. In the application where the LM6413E is used at CR oscillation of (C = 68pF, R = 10kohm), if the LM64PG98 is used for evaluation, an oscillation frequency nearly equivalent to that of the LM6413E can be obtained by adding (parallel-connecting) approximately 20pF to capacitance C.

Application development tools

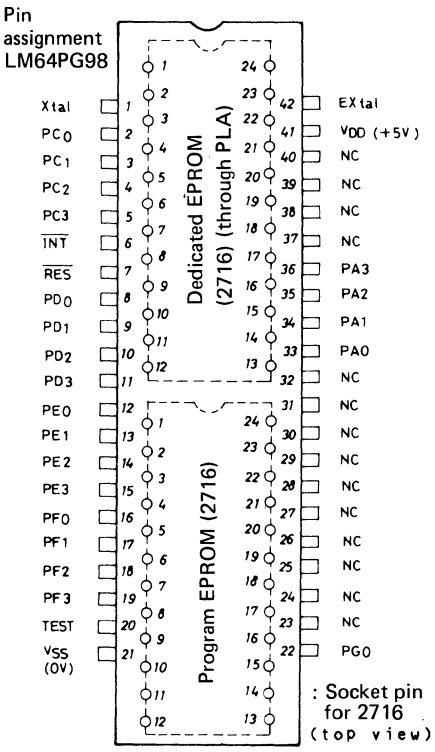
For convenience of application development of the LM6413E, the evaluation chip (LM6498) and the dedicated equipment called "application development tools" are available. For details, refer to "DEVELOPMENT TOOL MANUAL".

(1) SDS-410 system
This is a combination of floppy disks-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be constructed (edited, assembled) very seedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled or data can be written into EPROM (using EPROM WRITER function contained in the EVA-410).

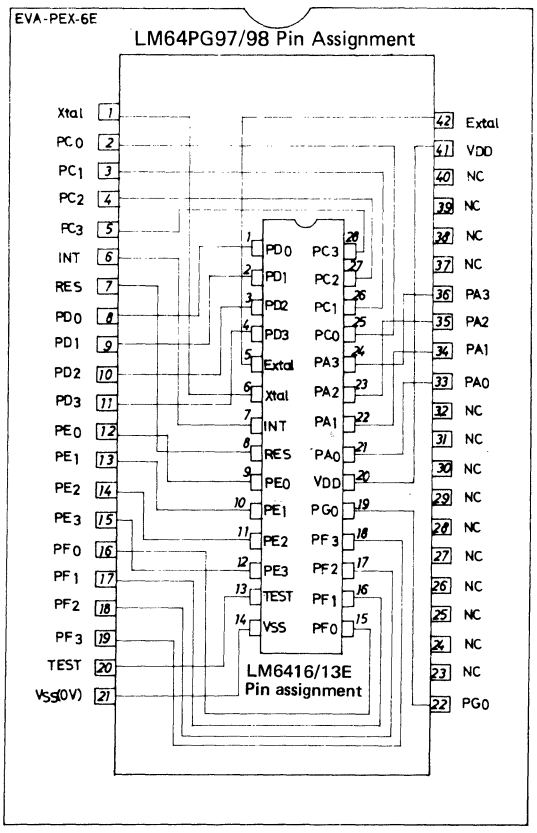
(2) EVA-410 + TB1 (6498)
This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. If the TB1 is mounted with the LM6499, replace the LM6499 with the LM6498.



(3) LM64PG98
The LM64PG98 is provided with 24-pin sockets for 2 program EPROMs and "PLA through" on its package surface. By using jointly with a board for conversion form 42-pin normal to 28-pin shrink (Note), pin-compatibleness with mass production product LM6413E is enabled. Because of its evaluation capability equivalent to the EVA-410E and its compactness, the LM64PG98 is best suited for being mounted on a prototype.
(Note)
EVA-PEX-6E (Board for conversion into LM6416E pin assignment)



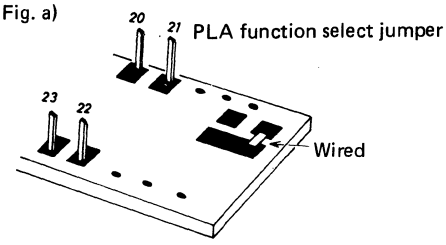
(4) Board 'EVA-PEX-6E' for conversion into LM6413E pin assignment
For evaluation of the LM6413E, the LM64PG98 and the conversion circuit are used.



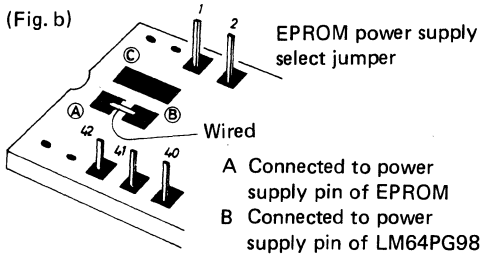
Pin assignment conversion circuit diagram from LM64PG98 to LM6413E, from LM64PG97 to LM6416E.

(5) Proper cares in using LM64PG98
Check to see the following before using the LM64PG98.
① The PLA function select jumper is connected. (Fig. a)
② In order that the EPROM power supply and the LM64PG98 power supply (V_{DD}) become the same, the jumper on the back is wired as shown in Fig. b. (Note 1).

(Fig. a)



(Fig. b)



③ Insert the following data written EPROM (2716) to the dedicated EPROM (through PLA) socket. (Note 2)

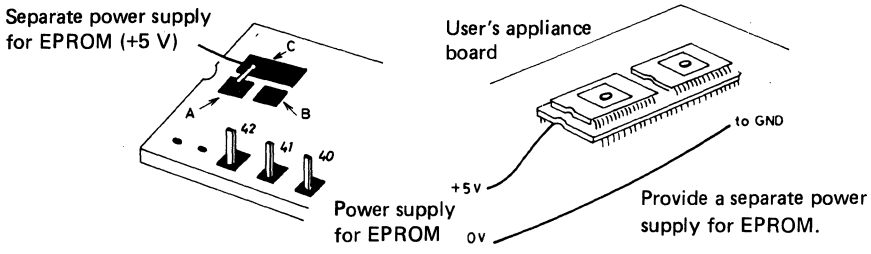
Data for dedicated EPROM (through PLA) (HEX notation)

EPROM address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 1 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 2 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 3 0	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
0 4 0																
0 5 0																
:																
:																

For EPROM addresses 40H onward, any data are acceptable.

(This data are commonly called "through PLA")

(Note 1) The EPROM dissipates relatively large current. If the power capacity of user's appliances is insufficient, wire as shown below and provide a separate power supply for the EPROM so that power can be supplied externally.



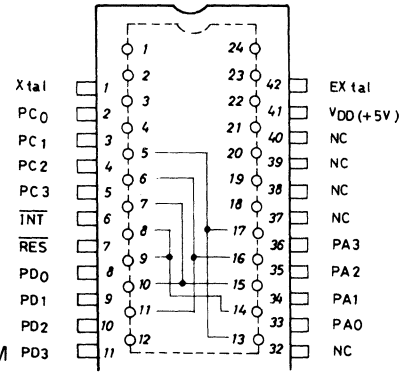
(Note 2) The connection shown below makes the evaluation possible without inserting the dedicated EPROM.

For the dedicated EPROM (through PLA) socket,

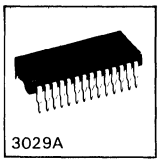
Connect pin 5 with pins 13,17.
pin 6 with pins 11,16.
pin 7 with pins 10,15.
pin 8 with pins 9.14

Other pins are open.

Connection in case of using no EPROM



LM6416E



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 995D

The LM6416E is a single-chip 4-bit N-channel MOS microcomputer intended for use in control-oriented applications. It contains a ROM (1024 bytes (1k bytes)), a RAM (64 x 4 bits), an ALU, I/O ports (21 pins), a timer, and a clock generator. It is a low-end model of the LM6400 series and is suited for use in cost sensitive sets.

(1) Hardware features (Reduction in external parts)

- Cycle time : 4 to 40us
- Capable of interfacing direct with 15V(max) peripheral circuits.
- Clock generator (Ceramic resonator or CR attached externally, fmax=1MHz).
- All output ports containing LED driver (5 ports/17 pins, I_{OL}=10mA/V_{OL}=1.5V).
- Input/output common ports (2 ports/ 8 pins).
- Single 5V (typ) supply and wide operating range (V_{DD}=4.5 to 6.5 V).
- Initial reset and external pseudo interrupt input pins containing Schmitt gate.

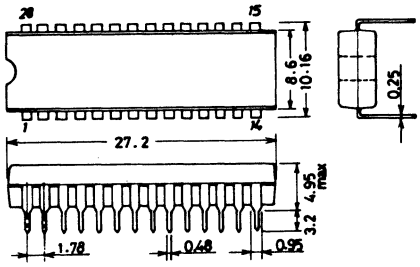
(2) Software features (Effective use of ROM capacity)

- 65 instructions compatible with LM6402/05.
- 2-level subroutine nesting.
- Pseudo interrupt function (External/internal).
- Programmable timer with wide setting range.
- Automatic page select.

(3) Evaluation chip

- Evaluation chip LM6497 and piggyback LM64PG97 are available for use in the application development of the LM6416E.

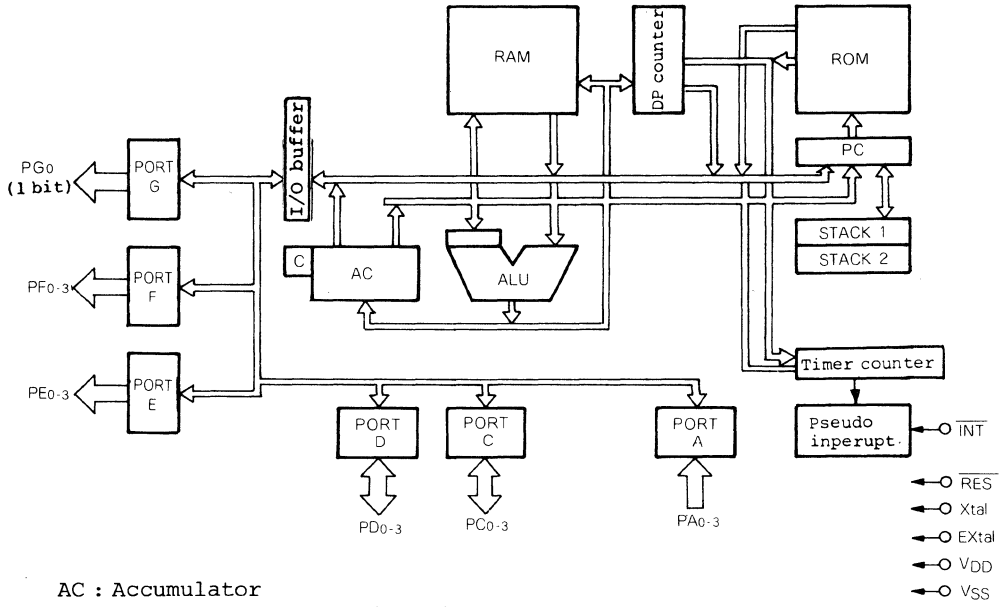
Case Outline 3029A-D28SIC
(unit:mm)



SANYO: DIP28S

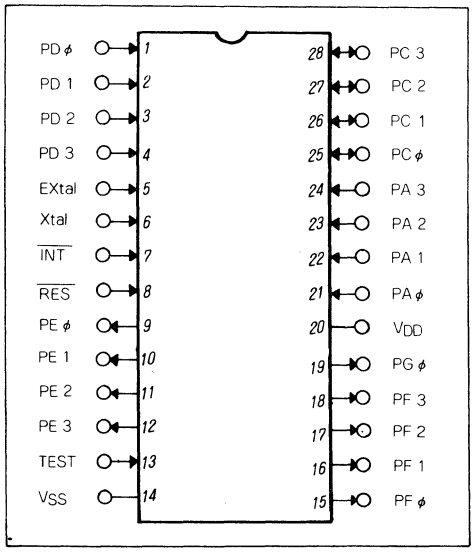
For details, refer to LM6416 Series User's Manual.

System Block Diagram



AC : Accumulator
ALU : Arithmetic and logic unit
DP : Data pointer
C : Carry FF
PC : Program counter

Package and Pin Assignment



(Pin name)

Xtal, EXtal	: OSC resonator	
$\overline{INT}$	: Interrupt	
$\overline{RES}$	: Reset	
PA_0 to 3	: Input ports	A_0 to 3
PC_0 to 3	: Input/output ports	C_0 to 3
PD_0 to 3	: Input/output ports	D_0 to 3
PE_0 to 3	: Output ports	E_0 to 3
PF_0 to 3	: Output ports	F_0 to 3
PG_0	: Output ports	G_0
TEST	: Test	

Pin Description

Pin name	Input/output	Function
$\overline{INT}$	Input	Pseudo interrupt request input pin.
$\overline{RES}$	Input	Reset input pin.
$PA_{3 \text{ to } 0}$	Input	Input ports A_3 to A_0. Capable of 4-bit input and single-bit test.
$PC_{3 \text{ to } 0}$	Input/output	Input/output common ports C_3 to C_0. Capable of 4-bit input and single-bit test during input. Capable of 4-bit output and single-bit set/reset and immediate data output during output.
$PD_{3 \text{ to } 0}$	Input/output	Input/output common ports D_3 to D_0. Capable of 4-bit input and single-bit test during input. Capable of 4-bit output and single-bit set/reset and immediate data output during output.
$PE_{3 \text{ to } 0}$	Output	Output ports E_3 to E_0. Capable of 4-bit output and single-bit set/reset.
$PF_{3 \text{ to } 0}$	Output	Output ports F_3 to F_0. Capable of 4-bit output and single-bit set/reset.
PG_0	Output	Output ports G_0. Capable of single-bit output and single-bit set/reset during output.
Xtal	Input/output	Pin for externally attaching oscillator for internal clock oscillation. Ceramic resonator or CR is connected to this pin and pin EXtal.
EXtal	Input	Pin for supplying external colock. If internal clock oscillation is used, ceramic resonator or CR is connected to this pin and pin Xtal.
V_{DD}	Input	Power supply pin. Normally connected to +5V.
V_{SS}	——	Connected to 0V power supply.
TEST	Input	LSI test pin. Normally connected to V_{SS}(0V).

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		-0.3 to +8	V
Input Voltage	V_{IN}	EXtal pin: Up to self-oscillation level	-0.3 to +15	V
Output Voltage	V_{OUT}	Output transistor : OFF	-0.3 to +15	V
Average Output Current (Applicable to any 100ms period) *1)	$I_{OLA(1)}$	Each pin of ports	20	mA
	$I_{OLA(2)}$	All pins of C,D ports	100	mA
	$I_{OLA(3)}$	All pins of E,F,G ports	110	mA
Peak Output Current *2)	$I_{OLP(1)}$	Each pin of ports	20	mA
	$I_{OLP(2)}$	All pins of C,D ports	120	mA
	$I_{OLP(3)}$	All pins of E,F,G ports	130	mA
Allowable Power Dissipation	P_dmax	-30°C to +70°C	400	mW

			unit
Operating Temperature	Topg	-30 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C

*1) Applicable to any 100ms period
*2) Must not be exceeded even momentarily.

Recommended Operation Conditions at T_a=-30 to +70°C, V_{SS}=0V

				min	typ	max	unit
Recommended Operating Supply Voltage		V_{DD}		4.5		6.5	V
Port Input	"H" level input voltage	$V_{IH(1)}$		$0.6V_{DD}$		13.5	V
	"L" level input voltage	$V_{IL(1)}$		V_{SS}		$0.3V_{DD}$	V
$\overline{INT}$, $\overline{RES}$	"H" level input voltage	$V_{IH(2)}$		$0.7V_{DD}$		13.5	V
	"L" level input voltage	$V_{IL(2)}$		V_{SS}		$0.3V_{DD}$	V
EXtal (Selecting ceramic oscillation option)	"H" level input voltage	$V_{IH(3)}$	External clock is applied.	$0.8V_{DD}$		V_{DD}	V
	"L" level input voltage	$V_{IL(3)}$	Same as above	V_{SS}		1.0	V
	Clock cycle	$t_{C(\phi)}$	Same as above, Refer to Fig. 1	1.0		10.0	us
	"H" level clock pulse width	$t_{W\phi H}$	Same as above, Xtal open	0.3			us
	"L" level clock pulse width	$t_{W\phi L}$	Same as above, Xtal open	0.47			us
Oscillator (Selecting ceramic oscillation option)	External resistance for ceramic oscillation	R1	Refer to Fig. 2	900	1000	1100	kohm
	External capacitance for ceramic oscillation	C1	EXtal side 400kHz	200	220	240	pF
			" 800kHz	200	220	240	pF
	External capacitance for ceramic oscillation	C2	Xtal side 400kHz	200	220	240	pF
			" 800kHz	200	220	240	pF
(Selecting CR oscillation option)	External resistance for CR oscillation	R2	Refer to Fig. 3	8	10	100	kohm
	External capacitance for CR oscillation	C3	Refer to Fig. 3	45	68	200	pF
TEST	"L" level input voltage	$V_{IL(4)}$		V_{SS}		0.4	V

Electrical Characteristics at T_a=-30 to +70°C, V_{DD}=4.5 to 6.5V, V_{SS}=0V

				min	typ	max	unit
A Port $\overline{INT}$, $\overline{RES}$	"H" level input current	$I_{IH(1)}$	V_{IN}=13.5V			10	uA
	"L" level input current	$I_{IL(1)}$	$V_{IN}=V_{SS}$	-10			uA
EXtal	"H" level input current	$I_{IH(2)}$	$V_{IN}=V_{DD}$			10	uA
	"L" level input current	$I_{IL(2)}$	$V_{IN}=V_{SS}$	-10			uA
C,D Port (Output OFF)	"H" level input current	$I_{IH(3)}$	V_{IN}=10(13.5)V			10	uA
	"L" level input current	$I_{IL(3)}$	$V_{IN}=V_{SS}$, Same as above.	-10			uA
C,D,E,F,G Port	"L" level output current	$I_{OL(1)}$	V_{DD}=4.5V, V_{OL}=1.5V	10			mA
	Output off leak current	$I_{OFF(1)}$	V_{OH}=13.5V			10	uA

			min	typ	max	unit
CR Oscillation Frequency (Selecting CR oscillation option)	$f_{OSC(1)}$	C=68pF* R=10kohm *Including stray capacitance of board wiring, etc. T_a=0 to +70°C	620	770	890	kHz
	$f_{OSC(2)}$	Same as above T_a=-30 to +70°C	620	770	960	kHz
Current Dissipation	$I_{DD(1)}$	At 800kHz oscilation Output=Open T_a=0 to +70°C		17	30	mA
	$I_{DD(2)}$	Same as above T_a=-30 to +70°C		17	35	mA
Input Pin Capacitance	C_I			10		pF

Fig. 1 EXtal Input Waveform

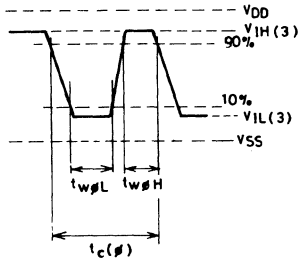
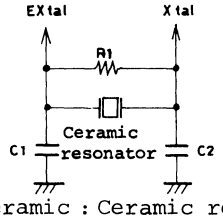
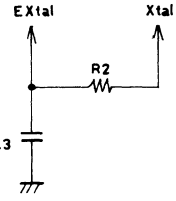


Fig. 2 Recommended Ceramic Oscillator



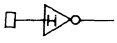
Ceramic : Ceramic resonator
- KBR400B
- CSB400P
- KBR800H
- CSB800A

Fig. 3 Recommended CR Oscillator

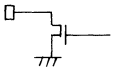


Input/output type of port

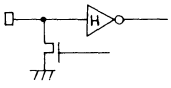
Input only (high threshold input)



Output only (open drain output)



Input/output common (highthreshold input, open drain output)



CR oscillation of LM6416E, LM64PG97

1. For the variation range of CR oscillation frequency of the LM6416E, the following are guaranteed at external constants of C=68pF, R=10kohm only.

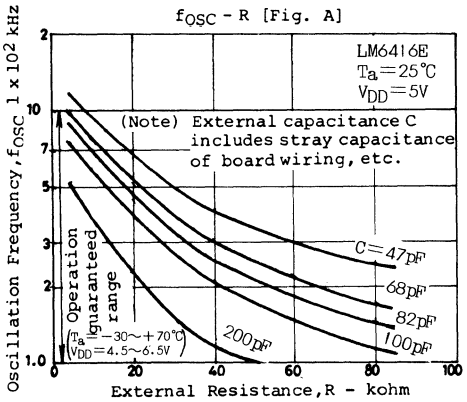
   min typ max

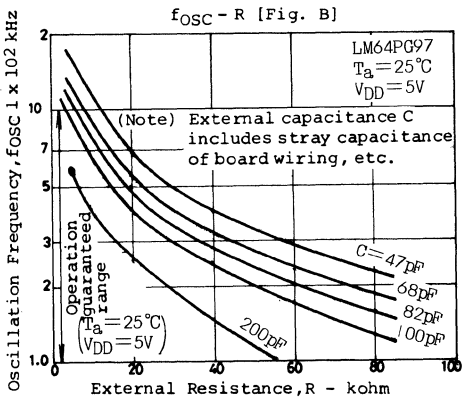
   1) $f_{OSC(1)}$ = 620 to 770 to 890 kHz (T_a=0 to +70°C)
   2) $f_{OSC(2)}$ = 620 to 770 to 960 kHz (T_a=-30 to+70°C)
2. If other frequency than typical value 770kHz is used at ohter constants than C=68pF, R=10kohm, fix CR constants referring to "oscillation frequency vs. standard external resistance characteristics" in Fig. A. In this case, take care of the following.
   1) Oscillation cycle must be within the range (1 to 10us) of recommended operation clock cycle at EXtal pin.
   2) CR constants must be selected from among recommended external constants (C=45 to 200pF, R=8 to 100kohm).

   It should be noted that outgoing inspection is performed under the frequency

variation condition at C=68pF, R=10kohm.

3. CR constants of the LM64PG97 are also fixed referring to "oscillation frequency vs. standard external resistance characteristics" in Fig. B. In the application where the LM6416E is used at CR oscillation of C=68pF, R=10kohm, if the LM64PG97 is used for evaluation, an oscillation frequency nearly equivalent to that of the LM6416E can be obtained by adding (parallel-cnnecting) approximately 20pF to capacitance C.





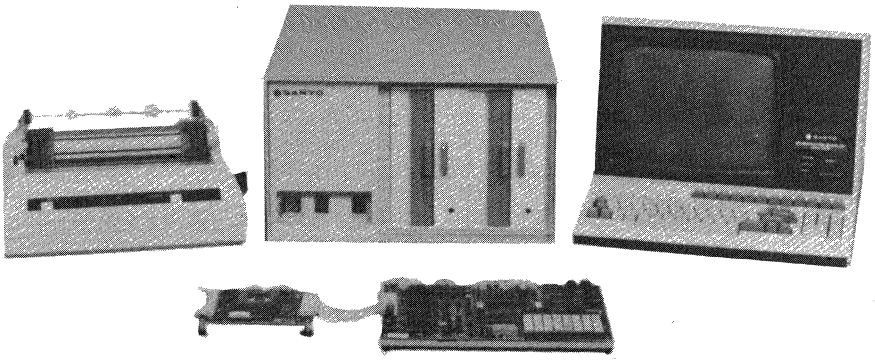
Application development tools

For convenience of application development of the LM6416E, the evaluation chip (LM6497) and the specialized equipment called "application development tools" are available. For details, refer to "DEVELOPMENT TOOL MANUAL".

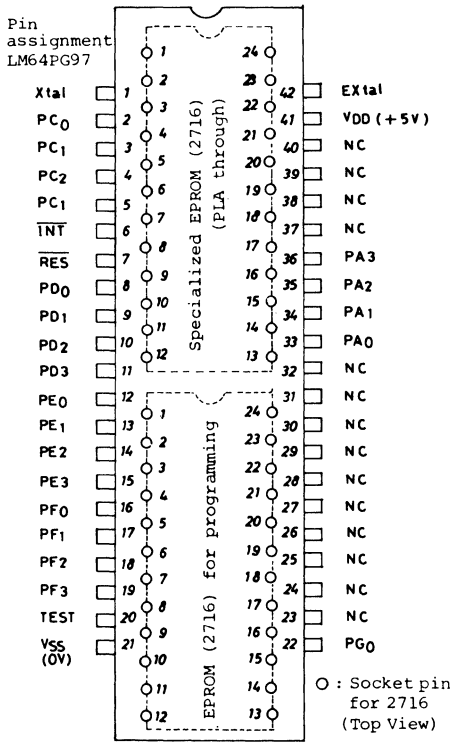
. SDS-410 system
This is a combination of floppy disks-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be constructed (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled or data can be written into EPROM (using EPROM WRITER function contained in the EVA-410).

. EVA-410 + TB1 (6497)
This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. If the TB1 is mounted with the LM6499, replace the LM6499 with the LM6497.

. EVA-401
This is a board with an EPROM and the LM6497 combined. This board is used for mounting evaluation or trial production of sets after application development programs are completed.



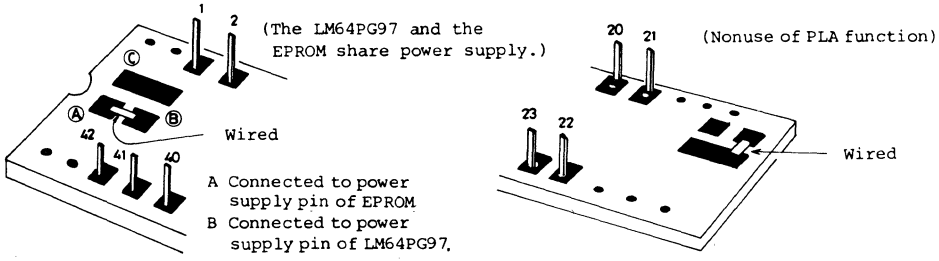
. LM64PG97
The LM64PG97 is provided with 24-pin sockets for 2 EPROMs for programming and "PLA through" on its package surface. By using jointly with a board for conversion from 42-pin normal to 28-pin shrink, pin-compatibleness with mass production product LM6416E is enabled. Because of its evaluation capability equivalent to the EVA-401 and its compactness, the LM64PG97 is best suited for being mounted on equipment made on an experimental basis.



Xtal,EXtal	: OSC resonator·CR	
$\overline{INT}$	: Pseudo interrupt	
$\overline{RES}$	: Reset	
PA_{0-3}	: Input ports	A_0 to 3
PC_{0-3}	: Input/output ports	C_0 to 3
PD_{0-3}	: Input/output ports	D_0 to 3
PE_{0-3}	: Output ports	E_0 to 3
PF_{0-3}	: Output ports	F_0 to 3
PG_0	: Output ports	G_0
TEST	: Test	

Shipment of LM64PG97

(1) Nonuse of PLA function (The LM6416E is provided with no PLA function.)
(2) In order that the EPROM power supply and the LM64PG97 power supply (V_{DD}) become the same, the jumper on the back is wired as shown below. Check to see this wiring prior to use.



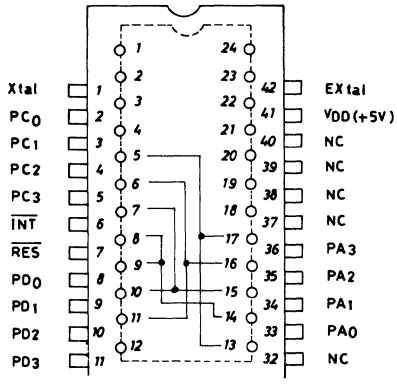
For PLA EPROM, make "PLA through" which data for nonuse of PLA function are written (see below) or connect pins direct as shown on next page if no EPROM for "PLA through" is used.

EPROM data for nonuse of PLA function (HEX notation)

EPROM address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
010	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
020	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
030	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
040																
050																
⋮																

For EPROM addresses 40_H onward, any data are acceptable.

(This data are commonly called "PLA through")

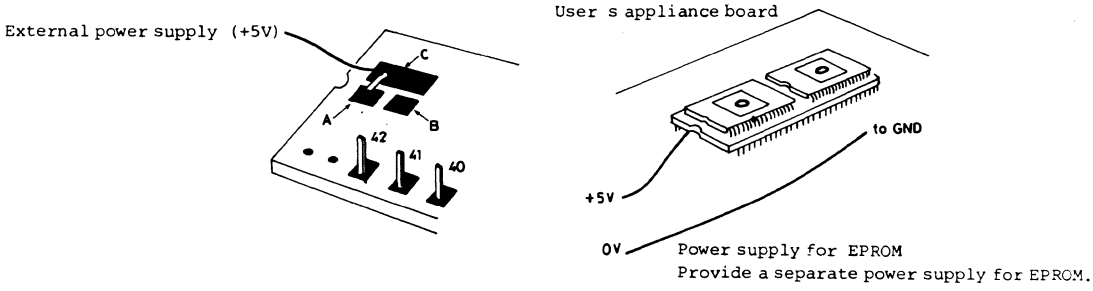


Connect pin 5 with pins 13, 17.
pin 6 with pins 11, 16.
pin 7 with pins 10, 15.
pin 8 with pins 9, 14.

Other pins are open.

Connection in case of using no EPROM for "PLA through"

EPROM dissipates relatively large current, If power capacity of user's appliances is insufficient, wire as shown below and provide a separate power supply for EPROM so that power can be supplied externally.



LM6416E INSTRUCTION SET

Notations

AC	: Accumulator	TMFF	: Timer FF	( )	: Contents
An	: Accumulator bit n	TIMER	: Timer	⟵	: Transfer direction, result
C	: Carry FF	INT FF	: Interupt FF	∨	: Exclusive-or
Carry	: Carry from ALU	STACK	: Stack		
Borrow	: Borrow from ALU	P_t	: Port		
DP	: Data pointer	M	: Memory		
PC	: Program counter	[M(DP)]	: Memory contents addressed by DP		

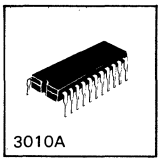
Instruction	Mnemonic		Instruction code $D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Byte	Machine cycle	Operation	Description of operation	skip condition
Accumulator handling instruction	CLA	Clear AC	1 0 0 1	0 0 0 0	1	1	AC←0	The contents of the AC are cleared.	
	CLC	Clear C	0 0 0 0	1 0 1 1	1	1	C←0	The contents of the C are cleared.	
	CMA	Complement AC	0 0 0 1	0 0 0 0	1	1	AC←($\overline{AC}$)	The contents of the AC are complemented.	
	CIA	Complement & Increment AC	0 0 0 1	0 0 0 1	1	1	AC←($\overline{AC}$)+1	The contents of the AC are complemented and incremented by 1. The C is unaffected.	
	INC	Increment AC and skip if Carry	0 0 0 0	1 1 0 1	1	1	AC←(AC)+1 skip if Carry	The contents of the AC are incremented. If carry is generated, the instruction immediately following the INC is skipped. The C is unaffected.	Carry
	DEC	Decrement AC and skip if Borrow	0 0 0 0	1 1 1 1	1	1	AC←(AC)-1 skip if Borrow	The contents of the AC are decremented. If carry is generated, the instruction immediately following the DEC is skipped. The C is unaffected.	Borrow
	STC	Set C	0 0 0 1	1 0 1 1	1	1	C←1	The C is set.	
	RAR	Rorate AC Right through C	0 0 1 1	0 0 0 0	1	1	(C)→A_3,(An)→An-1 (A_0)→C	The contents of the AC are rotated right through the C.	
Memory handling instruction	INM	Increment M skip if Carry	0 0 0 1	1 1 0 1	1	1	M(DP)←[M(DP)]+1 skip if Carry	The contents of the memory M(DP) are incremented. The AC, C are unaffected. If the result is [M(DP)]= 0, the instruction immediately following the INM is skipped.	[M(DP)]=0
	DEM	Decrement M skip if Borrow	0 0 0 1	1 1 1 1	1	1	M(DP)←[M(DP)]-1 skip if Borrow	The contents of the memory M(DP) are decremented. The AC, C are unaffected. If the result is [M(DP)]= F, the instruction immediately following the DEM is skipped.	[M(DP)]=F
Arithmetic operation instruction	AD	Add M to AC skip if Carry	0 0 0 0	1 0 0 0	1	1	AC←(AC)+[M(DP)] skip if Carry	Binary addition of the contents of the AC and the contents of the memroy M(DP) is performed and the result is stored in the AC. If carry is generated, the instruction immediately following the AD is skipped.	Carry
	ADS	Add M to AC with C Skip if Carry	0 0 0 0	1 0 0 1	1	1	AC,C←(AC)+[M(DP)]+(C) skip if Carry	Binary addition of the contents of the AC, C and the contents of the memory M(DP) is performed and the result is stored in the AC, C. If carry is generated, the instruction immediately following the ADS is skipped.	Carry
	ADC	Add M to AC with C	0 0 0 1	1 0 0 1	1	1	AC, C←(AC)+[M(DP)]+(C)	Binary addition of the contents of the AC, C and the contents of the memory M(DP) is performed and the result is stored in the AC, C.	
	DAA	Decimal adjust AC in Addition	0 0 0 0	0 1 1 0	1	1	AC←(AC)+6	6 is added to the AC. The C is unaffected. This instruction is used for decimal addition adjust.	
	DAS	Decimal adjust AC in Subtraction	0 0 0 0	1 0 1 0	1	1	AC←(AC)+10	10 is added to the AC. The C is unaffected. This instruction is used for decimal subtraction adjust.	
	EXL	Exclusive OR Logic	0 0 0 1	1 0 0 0	1	1	AC←(AC)∨[M(DP)]	The contents of the AC and the contents of the memory M(DP) are exclusive-or'd and the result is stored in the AC.	
Load/store instruction	LI *	Load AC with Immediate data	1 0 0 1	$I_3I_2I_1I_0$	1	1	AC←$I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ are loaded in the AC.	
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP)←(AC)	The contents of the AC are stored in the memory M(DP).	
	L	Load AC with M	0 0 1 1	1 0 0 0	1	1	AC←[M(DP)]	The contents of the memory M(DP) are loaded in the AC.	
	LM	Load AC with M and Modify DP_H	0 0 1 1	1 0 M_1M_0	1	1	AC←[M(DP)] DP_H←(DP_H)∨M_1M_0	The contents of the memory M(DP) are loaded in the AC and then the DP_H is modified with the DP_H∨M_1M_0.	
	X	Exchange AC with M	0 0 1 0	1 0 0 0	1	1	(AC)⇄[M(DP)]	The contents of the memory M(DP) and the contents of the AC are exchanged.	
	XM	Exchange AC with M and Modify DP_H	0 0 1 0	1 0 M_1M_0	1	1	(AC)⇄[M(DP)] DP_H←(DP_H)∨M_1M_0	The contents of the memory M(DP) and the contents of the AC are exchanged and then the DP_H is modified with the DP_H∨M_1M_0.	

Instruction	Mnemonic		Instruction code		Byte	Machine cycle	Operation	Description of operation	skip condition
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$					
Load/store instruction	XD	Exchange AC with M then Decrement DP_L	0 0 1 0	1 1 0 0	1	2	$(AC) \rightleftarrows [M(DP)]$ $DP_L \leftarrow (DP_L)-1$ skip if Borrow	The contents of the memory M(DP) and the contents of the AC are exchanged and then the contents of the DP_L are decremented. If the result is $(DP_L)=F$, the instruction immediately following the XD is skipped.	$(DP_L)=F$
	XMD	Exchange AC with M and Modify DP_H then Decrement DP_L	0 0 1 0	1 1 M_1M_0	1	2	$(AC) \rightleftarrows [M(DP)]$ $DP_H \leftarrow (DP_H) \forall M_1M_0$ $DP_L \leftarrow (DP_L)-1$ skip if Borrow	The contents of the memory M(DP) and the contents of the AC are exchanged and then the DP_H is modified with the $(DP_H) \forall M_1M_0$ and the contents of the DP_L are decremented. If the result is $(DP_L)=F$, the instruction immediately following the XMD is skipped.	$(DP_L)=F$
	XI	Exchange AC with M and Increment DP_L	0 0 1 1	1 1 0 0	1	2	$(AC) \rightleftarrows [M(DP)]$ $DP_L \leftarrow (DP_L)+1$ skip if Carry	The contents of the memory M(DP) and the contents of the AC are exchanged and then the contents of the DP_L are incremented. If the result is $(DP_L)=0$, the instruction immediately following the XI is skipped.	$(DP_L)=0$
	XMI	Exchang AC with M and Modify DP_H then Increment DP_L	0 0 1 1	1 1 M_1M_0	1	2	$(AC) \rightleftarrows [M(DP)]$ $DP_H \leftarrow (DP_H) \forall M_1M_0$ $DP_L \leftarrow (DP_L)+1$ skip if Carry	The contents of the memory M(DP) and the contents of the AC are exchanged and then the DP_H is modified with the $(DP_H) \forall M_1M_0$ and the contents of the DP_L are incremented. If the result is $(DP_L)=0$, the instruction immediately following the XMI is skipped.	$(DP_L)=0$
Data pointer handling instruction	LDI	Load DP with Immediate data	0 0 0 1 0 0 I_5I_4	0 1 0 1 $I_3I_2I_1I_0$	2	2	$DP_H \leftarrow I_5I_4$ $DP_L \leftarrow I_3I_2I_1I_0$	The DP is loaded with the 2nd byte immediate data I_5 to I_0.	
	LDZ	Load DP_H and DP_L with Zero and immediate data respectively	1 0 0 0	$I_3I_2I_1I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3I_2I_1I_0$	The DP_H is loaded with 0 and the DP_L with the immediate data $I_3I_2I_1I_0$.	
	DED	Decrement DP	0 0 0 1	0 0 1 1	1	1	$DP_L \leftarrow (DP_L)-1$ skip if Borrow	The contents of the DP_L are decremented. If the result is $(DP_L)=F$, the instruction immediately following the DED is skipped.	$(DP_L)=F$
	IND	Increment DP	0 0 1 1	0 0 1 1	1	1	$DP_L \leftarrow (DP_L)+1$ skip if Carry	The contents of the DP_L are incremented. If the result is $(DP_L)=0$, the instruction immediately following the IND is skipped.	$(DP_L)=0$
	TAL	Transfer AC to DP_L	0 0 0 0	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The contents of the AC are transferred to the DP_L.	
	TLA	Transfer DP_L to AC	0 0 0 1	0 0 1 0	1	1	$AC \leftarrow (DP_L)$	The contents of the DP_L are transferred to the AC.	
Bit handling instruction	SMB	Set Memory data Bit	0 1 1 1	1 0 B_1B_0	1	1	$M(DP,B_1,B_0) \leftarrow 1$	A single bit of the memory specified by the DP which is designated by 2 bits (B_1,B_0) of the instruction is set.	
	RMB	Reset Memory data Bit	0 1 1 0	1 0 B_1B_0	1	1	$M(DP,B_1,B_0) \leftarrow 0$	A single bit of the memory specified by the DP which is designated by 2 bits (B_1,B_0) of the instruction is reset.	
	TMB	Test Memory data Bit	0 1 0 1	1 0 B_1B_0	1	1	skip if $[M(DP,B_1,B_0)]=1$	A signle bit of the memory specified by the DP which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the TMB is skipped.	$[M(DP,B_1,B_0)]=1$
	TAB	Test AC Bit	0 0 1 0	0 1 B_1B_0	1	1	skip if $[AC(B_1,B_0)]=1$	A single bit of the contents of the AC which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the TAB is skipped.	$[AC(B_1,B_0)]=1$
	CMB	Compare AC bit with M data Bit	0 0 1 1	0 1 B_1B_0	1	1	skip if $[AC(B_1,B_0)]=[M(DP,B_1,B_0)]$	The bit of the contents of the AC and the bit of the contents of the memory M(DP) which are designated by 2 bits (B_1,B_0) of the instruction are compared, and if equal the instruction immediately following the CMB is skipped.	$[AC(B_1,B_0)]=[M(DP,B_1,B_0)]$
Comparison instruction	CM	Compare AC with M	0 0 0 0	1 1 0 0	1	1	skip if $(AC)=[M(DP)]$	The contents of the AC and the contents of the memory M(DP) are compared, and if equal the instruction immediately following the CM is skipped.	$(AC)=[M(DP)]$
	CI	Compare AC with Immediate data	0 0 0 1 1 1 0 0	0 1 1 1 $I_3I_2I_1I_0$	2	2	skip if $(AC)=I_3I_2I_1I_0$	The contents of the AC and the immediate data $I_3I_2I_1I_0$ are compared, and if equal the instruction immediately following the CI is skipped.	$(AC)=I_3I_2I_1I_0$
	CLI	Compare DP_L with Immediate data	0 0 0 1 1 1 1 0	0 1 1 0 $I_3I_2I_1I_0$	2	2	skip if $(DP_L)=I_3I_2I_1I_0$	The contents of the DP_L and the immediate data $I_3I_2I_1I_0$ are compared, and if equal the instruction immediately following the CLI is skipped.	$(DP_L)=I_3I_2I_1I_0$
Skip instruciton	TC	Test Carry	0 0 0 0	0 1 0 0	1	1	skip if $(C)=1$	The contents of the carry FF are tested, and if set the instruction immediately following the TC is skipped.	$(C)=1$
	TTM	Test Timer	0 0 0 0	0 1 0 1	1	1	skip if $(TMFF)=1$	The contents of the timer FF are tested, and if set the instruction immediately following the TTM is skipped.	$(TMFF)=1$
	TIT	Test Interrupt FF	0 0 0 0	0 0 1 1	1	1	skip if (INT FF)=1 INT FF←0	The contents of the interrupt FF are tested, and if set the instruction immediately following the TIT is skipped. Then the contents of the interrupt FF are reset.	(INT FF)=1

Instruction	Mnemonic		Instruction code		Byte	Machine cycle	Operation	Description of operation	skip condition
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$					
Jump instruction	JCP	Jump in the Current Page	1 1 P_5P_4	$P_3P_2P_1P_0$	1	1	PC←P_5 to P_0	A jump is made to the address which is designated by setting P_5 to P_0 in the low-order 6 bits of the PC.	
	JMP	Jump unconditionally	1 0 1 0 $P_7P_6P_5P_4$	0 0 P_9P_8 $P_3P_2P_1P_0$	2	2	PC← P_9 to P_0	A jump is made to the address designated with P_9 to P_0.	
	JPA	Jump in the Current Page modified by AC	0 1 0 0	0 0 0 1	1	2	PC←$A_3A_2A_1A_0$ 00	A jump is made to the address which is designated by setting $A_3A_2A_1A_0$ and 00 in the high-order 4 bits and the low-order 2 bits of the low-order 6 bits of the PC respectively.	
Subroutine instruction	CZP	Call subroutine in the Zero Page	1 0 1 1	$P_5P_4P_3P_2$	1	1	(PC+1)→STACK PC←00000$P_5P_4P_3P_2$00	1-word call instruciton to page 0.	
	CAL	Call subroutine	1 0 1 0 $P_7P_6P_5P_4$	1 0 P_9P_8 $P_3P_2P_1P_0$	2	2	(PC+2)→STACK PC← P_9 to P_0	Subroutine is called.	
	RT	Return from subroutine	0 1 0 0	1 0 0 0	1	2	PC←(STACK)	Program execution is returned from subroutine.	
	RTS	Return from subroutine and Skip	0 1 0 0	1 0 0 1	1	2	PC←(STACK) skip unconditionally	Program execution is returned from subroutine and skipped.	Unconditional
I/O instruction	SEB	Set port E Bit	0 1 1 1	0 1 B_1B_0	1	2	Pt E(B_1,B_0)←1	A single bit of the output port E which is designated by 2 bits (B_1,B_0) of the instruction is set.	
	REB	Reset port E Bit	0 1 1 0	0 1 B_1B_0	1	2	Pt E(B_1,B_0)←0	A single bit of the output port E which is designated by 2 bits (B_1,B_0) of the instruciton is reset.	
	SPB	Set any Port Bit	0 1 1 1	0 0 B_1B_0	1	2	Pt(DP_L,B_1,B_0)←1	A single bit of the output port specified by the DP_L which is designated by 2 bits (B_1,B_0) of the instruction is set.	
	RPB	Reset any Port Bit	0 1 1 0	0 0 B_1B_0	1	2	Pt(DP_L,B_1,B_0)←0	A single bit of the output port specified by the DP_L which is designated by 2 bits (B_1,B_0) of the instruction is reset.	
	TPA	Test Port A Bit	0 1 0 1	0 1 B_1B_0	1	2	skip if [PtA(B_1, B_0)]=1	A single bit of the input port A designated by the instruction bit (B_1,B_0) is tested, and if 1 the instruction immediately following the TPA is skipped.	[PA(B_1,B_0)] =1
	TPB	Test any Port Bit	0 1 0 1	0 0 B_1B_0	1	1	skip if [Pt(DP_L, B_1,B_0]=1	A single bit of the input port specified by the DP_L which is designated by 2 bits (B_1,B_0) of the instruction is tested, and if 1 the instruction immediately following the TPB is skipped.	[P(DP_L,B_1,B_0)]=1
	OE	Output AC to port E (Output PLA to port E and F)	0 1 0 0	0 1 0 0	1	2	PtE←(AC)	The contents of the AC are outputted to the output port E. Or the contents of the PLA designated by the AC outputted to output ports E, F. (Selectable)	
	OP	Output AC to any Port	0 0 0 0	1 1 1 0	1	1	Pt(DP_L)←(AC)	The contents of the AC are outputted to the output port designated by the DP_L.	
	OCD	Output immediate data to port C and D	0 0 0 1 $I_7I_6I_5I_4$	1 1 1 0 $I_3I_2I_1I_0$	2	2	PtD←$I_7I_6I_5I_4$ PtC←$I_3I_2I_1I_0$	The immediate data I_7 to I_4 and I_3 to I_0 are outputted to port D and port C respectively.	
	SETD	Set port C and D Bit	0 0 0 1	1 1 0 0	1	2	PtC,D(DP_L)←1	A single bit of the output ports C, D which is designated by the DP_L is set.	
	RSTD	Reset port C and D Bit	0 1 0 0	0 1 0 1	1	2	PtC,D(DP_L)←0	A single bit of the output ports C, D which is designated by the DP_L is reset.	
	IA	Input port A in AC	0 1 0 0	0 0 0 0	1	2	AC←(PtA)	The contents of the input port A are inputted to the AC.	
	IP	Input any Port in AC	0 0 1 1	0 0 1 0	1	1	AC←[Pt(DP_L)]	The contents of the input port designated by the DP_L are inputted to the AC.	
Others	STM	Set Timer	0 0 0 1 0 0 0 0	0 1 0 0 $I_3I_2I_1I_0$	2	2	TMFF←0 TIMER←I_3 to I_0	The timer FF is reset. The program data are set in the timer and the timer start is instructed.	
	NOP	No Operation	0 0 0 0	0 0 0 0	1	1	No Operation	No operation. 1 machine cycle is consumed.	

* : If the LI instruction (including CLA instruction) are stacked, the LI instructions after the 2nd instruction are NOP.

LM6417E



N Channel E/D MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1381A

1. Description

The LM6417E is a single-chip 4-bit N-channel MOS microcomputer intended for use in control-oriented applications. It contains a ROM (1024bytes (1k bytes)), a RAM (64 x 4 bits), an ALU, I/O ports (17 pins), a timer, and a clock generator. It is a low-end model of the LM6400 series and is suited for use in cost sensitive sets.

(1) Hardware features (Reduction in external parts)

- Cycle time : 4 to 40us
- Capable of interfacing direct with 15V(max) peripheral circuits.
- Clock generator (typ 770kHz CR attached externally).
- All output ports containing LED driver (5 ports/17 pins, I_{OL}=10mA/V_{OL}=1.5V.)
- Input/output common ports (2 ports/8 pins)
- Single 5V (typ) supply and wide operating range (V_{DD}=4.5 to 6.5 V).
- Initial reset and external pseudo interrupt input pins containing Schmitt gate.
- CMOS, TTL Compatible.
- N-channel E/D MOS.

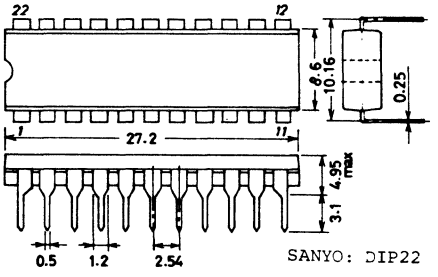
(2) Software features (Effective use of ROM capacity) [Identical to LM6416E except hardware feature]

- 65 instructions compatible with LM6402/05 and LM6416.
- 2-level subroutine nesting.
- Pseudo interrupt function (External/internal).
- Programmable timer with wide setting range.
- Automatic page select.

(3) Evaluation chip

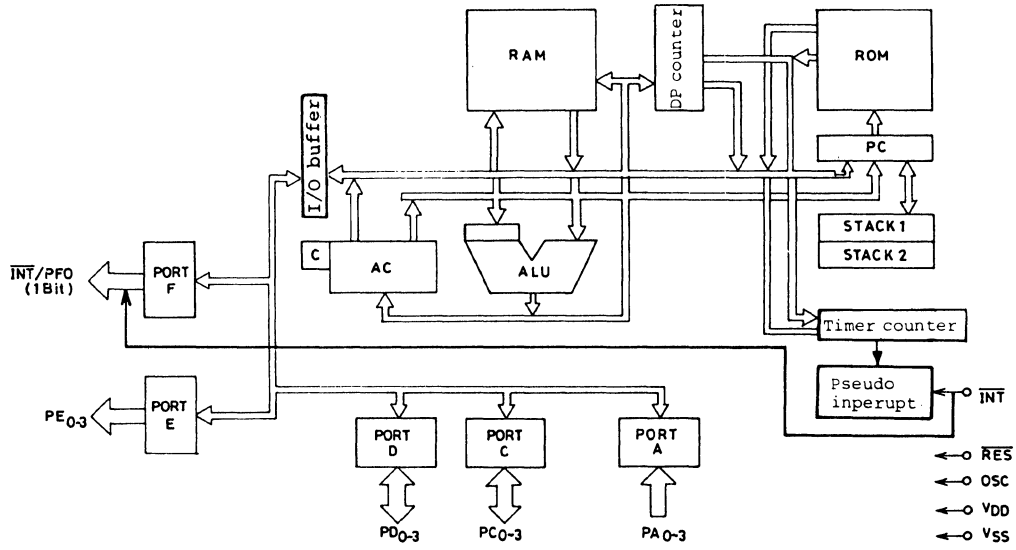
- Evaluation chip LM6497 is available for use in the application development of the LM6417E.

Case Outline 3010A-D22IC
(unit:mm)



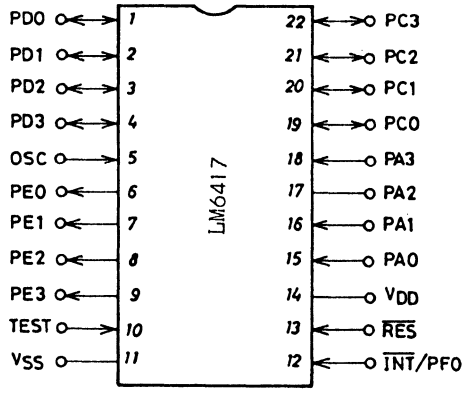
For details, refer to the instruction set table described in the separate catalog and also LM6416 Series User's Manual.

2.System Block Diagram



AC : Accumulator
ALU : Arithmetic and logic unit
DP : Data pointer
C : Carry FF
PC : Program counter

3.Package and Pin Assignment



(Pin name)

OSC	:	Oscillator	
INT/PF0	:	Interrupt/Output port F_0	
RES	:	Reset	
PA_0 to 3	:	Input ports	A_0 to 3
PC_0 to 3	:	Input/output ports	C_0 to 3
PD_0 to 3	:	Input/output ports	D_0 to 3
PE_0 to 3	:	Output ports	E_0 to 3
TEST	:	Test	

4. Pin Description

Pin name	Input/output	Function
$\overline{INT}$/PFO	Input	Pseudo interrupt request input pin/output port FO.
$\overline{RES}$	Input	Reset input pin.
$PA_{3 \text{ to } 0}$	Input	Input ports A_3 to A_0. Capable of 4-bit input and single-bit test.
$PC_{3 \text{ to } 0}$	Input/output	Input/output common ports C_3 to C_0. Capable of 4-bit input and single-bit test during input. Capable of 4-bit output and single-bit set/reset and immediate data output during output.
$PD_{3 \text{ to } 0}$	Input/output	Input/output common ports D_3 to D_0. Capable of 4-bit input and single-bit test during input. Capable of 4-bit output and single-bit set/reset and immediate data output during output.
$PE_{3 \text{ to } 0}$	Output	Output ports E_3 to E_0. Capable of 4-bit output and single-bit set/reset.
OSC	Input/output	Pin for externally connecting CR circuit for internal clock oscillation. C,R are connected to this pin or external clock is applied to this pin. (CR oscillation or external oscillation is selected by mask option.)
V_{DD}	Input	Power supply pin. Normally connected to +5V.
V_{SS}	——	Connected to 0V power supply.
TEST	Input	LSI test pin. Normally connected to V_{SS}(0V).

5. Characteristics

1) Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		-0.3 to +8	V
Input Voltage	V_{IN}		-0.3 to +15	V
Output Voltage	V_{OUT}	Output transistor : OFF	-0.3 to +15	V
Average Output Current *1	$I_{OLA(1)}$	Each pin of ports	20	mA
	$I_{OLA(2)}$	All pins of C,D ports	100	mA
	$I_{OLA(3)}$	All pins of E,F,G ports	110	mA
Peak Output Current *2	$I_{OLP(1)}$	Each pin of ports	20	mA
	$I_{OLP(2)}$	All pins of C,D ports	120	mA
	$I_{OLP(3)}$	All pins of E,F ports	130	mA
Allowable Power Dissipation	$P_d max$	Ta=-30 to +70 °C	400	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

*1 Applicable to any 100ms period
*2 Must not be exceeded even momentarily.

2) Recommended Operating Conditions at T_a=-30 to +70°C, V_{SS}=0V

				min	typ	max	unit
Recommended Operating Supply Voltage		V_{DD}		4.5		6.5	V
Port Input	"H" level input voltage	$V_{IH(1)}$		$0.6V_{DD}$		13.5	V
	"L" level input voltage	$V_{IL(1)}$		V_{SS}		$0.3V_{DD}$	V
$\overline{INT}$/PFO, $\overline{RES}$	"H" level input voltage	$V_{IH(2)}$		$0.7V_{DD}$		13.5	V
	"L" level input voltage	$V_{IL(2)}$		V_{SS}		$0.3V_{DD}$	V
OSC (Selecting external clock source option)	"H" level input voltage	$V_{IH(3)}$	External clock is applied.	$0.8V_{DD}$		V_{DD}	V
	"L" level input voltage	$V_{IL(3)}$	Same as above	V_{SS}		1.0	V
	Clock cycle	$t_{C(\phi)}$	Same as above, Refer to Fig. 1	1.0		10.0	us
	"H" level clock pulse width	$t_{W\phi H}$	Same as above,	0.3			us
	"L" level clock pulse width	$t_{W\phi L}$	Same as above,	0.47			us
OSC (Selecting CR oscillation option)	External resistance for CR oscillation	R1	Refer to Fig. 2	3.0	4.7	47	kohm
	External capacitance for CR oscillation	C1	Same as above	100	220	300	pF
TEST	"L" level input voltage	$V_{IL(4)}$		V_{SS}		0.4	V

3) Electrical Characteristics at T_a=-30 to +70°C, V_{DD}=4.5 to 6.5V, V_{SS}=0V

				min	typ	max	unit
A Port $\overline{INT}$/PFO, $\overline{RES}$ (PFO Output OFF)	"H" level input current	$I_{IH(1)}$	V_{IN}=13.5V			10	uA
	"L" level input current	$I_{IL(1)}$	V_{IN}=V_{SS}	-10			uA
OSC (Selecting external clock source option)	"H" level input current	$I_{IH(2)}$	V_{IN}=V_{DD}			10	uA
	"L" level input current	$I_{IL(2)}$	V_{IN}=V_{SS}	-10			uA
C, D Port (Output OFF)	"H" level input current	$I_{IH(3)}$	V_{IN}=13.5V			10	uA
	"L" level input current	$I_{IL(3)}$	V_{IN}=V_{SS}	-10			uA
C, D, E, F Port	"L" level output current	$I_{OL(1)}$	V_{DD}=4.5V, V_{OL}=1.5V	10			mA
	Output off. leak current	$I_{OFF(1)}$	V_{OH}=13.5V			10	uA
CR Oscillation Frequency (Selecting CR oscillation option)		$f_{OSC(1)}$	C_1=220pF*3 R_1=4.7kohm T_a=0 to +70°C	620	770	890	kHz
		$f_{OSC(2)}$	Same as above T_a=-30 to +70°C	620	770	960	kHz
Current Dissipation		$I_{DD(1)}$	At 800kHz oscilation Output=Open T_a=0 to +70°C		17	30	mA
		$I_{DD(2)}$	Same as above T_a=-30 to +70°C		17	35	mA
Input Pin Capacitance		C_I			10		pF

*3 Including stray capacitance of board wiring, etc.

Fig. 1 EXtal Input Waveform

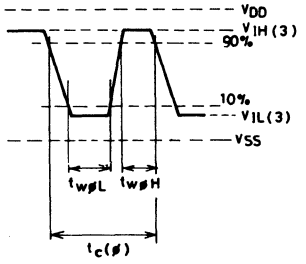
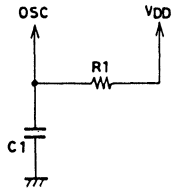
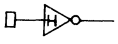


Fig. 2 Recommended Ceramic Oscillator

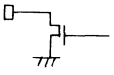


4)Input/output type of port

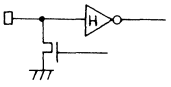
Input only
(high threshold input)



Output only
(open drain output)



Input/output common
(highthreshold input, open drain output)



5)CR oscillation of LM6417E, LM64PG97

1. For the variation range of CR oscillation frequency of the LM6417E, the following are guaranteed at external constants of C=220pF, R=4.7kohm only.

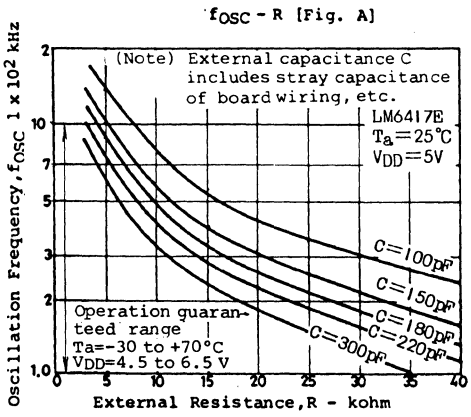
	min	typ	max	
1) $f_{OSC}(1)$ =	620 to	770 to	890 kHz	(Ta=0 to +70°C)
2) $f_{OSC}(2)$ =	620 to	770 to	960 kHz	(Ta=-30 to +70°C)

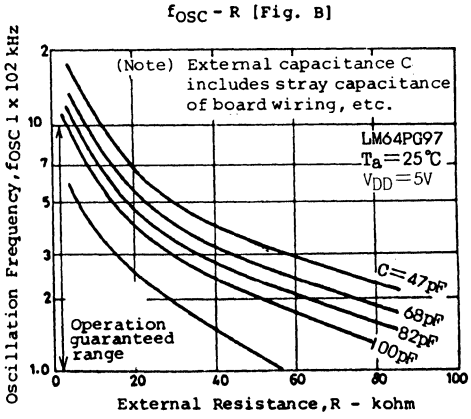
2. If other frequency than typical value 770kHz is used at other constants than C=220pF, R=4.7kohm, fix CR constants referring to "oscillation frequency vs. standard external resistance characteristics" in Fig. A. If this case, take care of the following.
   1) Oscillation cycle must be within the range (1 to 10us) of recommended operation clock cycle at EXtal pin.
   2) CR constants must be selected from among recommended external constants (C=100 to 300pF, R=3 to 47kohm).

   It should be noted that outgoing inspection is performed under the frequency variation condition at C=220pF, R=4.7kohm.
3. The LM64PG97 cannot be used to evaluate the LM6417E at CR oscillation option. By using the conversion board (EVA-PEX-7E) with C,R mounted, evaluation can simulated.

   [For details, refer to 6.5) Pin assignment conversion board (EVA-PEX-7E) for LM6417E].

   The values of C,R are fixed referring to "oscillation frequency vs. standard external resistance characteristics" in Fig. B. In the application where the LM6417E is used at CR oscillation option of C=220pF, R=4.7kohm, if the LM64PG97 is used for evaluation, an oscillation frequency nearly equivalent to that of the LM6417E can be obtained by mounting C=88pF, R=10kohm on the conversion board.

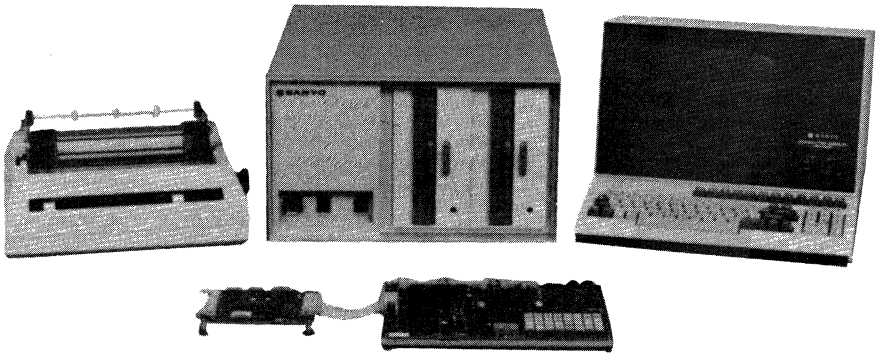




6. Application development tools

For convenience of application development of the LM6417E. the evaluation chip (LM6497) and the specialized equipment called "application development tools" are available. Evaluation is performed by jointly using the LM6416E development tool and the pin assignment conversion board(EVA-PEX-7E). For the LM6416E development tool, refer to "DEVELOPMENT TOOL MANUAL".

1) SDS-410 system
   This is a combination of floppy disks-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be constructed (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled or data can be written into EPROM (using EPROM WRITER function contained in the EVA-410).
2) EVA-410 + TB1 (6497)
   This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. If the TB1 is mounted with the LM6499, replace the LM6499 with the LM6497.
3) EVA-401
   This is a board with an EPROM and the LM6497 combined. This board is used for mounting evaluation or trial production of sets after application development programs are completed.

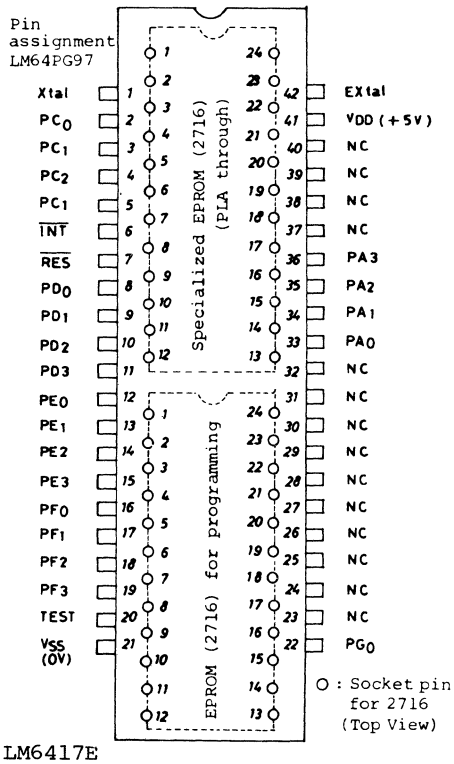


4) LM64PG97

The LM64PG97 is provided with 24-pin sockets for 2 EPROMs for programming and "PLA through" on its package surface. By using jointly with a board[*1] for conversion from 42-pin normal to 22-pin normal, pin-compatibleness with mass production product LM6417E is enabled. Because of its evaluation capability equivalent to the EVA-401 and its compactness, the LM64PG97 is best suited for being mounted on equipment made on an experimental basis.

*1 EVA-PEX-7E

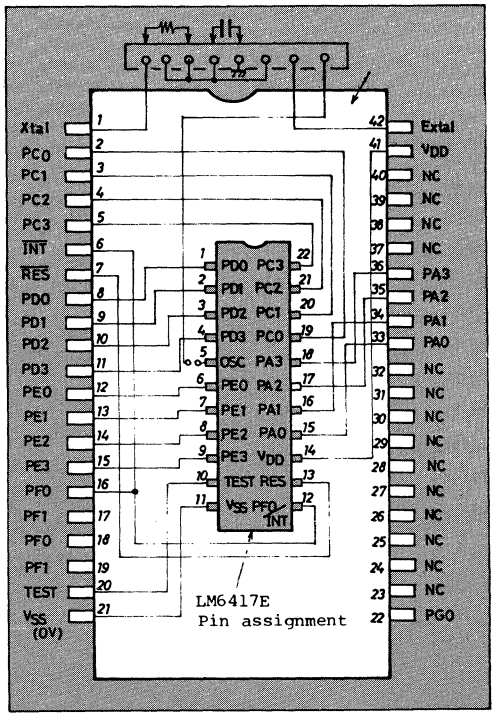
Xtal,EXtal	: OSC resonator·CR	
$\overline{INT}$	: Pseudo interrupt	
$\overline{RES}$	: Reset	
PA_{0-3}	: Input ports	A_0 to 3
PC_{0-3}	: Input/output ports	C_0 to 3
PD_{0-3}	: Input/output ports	D_0 to 3
PE_{0-3}	: Output ports	E_0 to 3
PF_{0-3}	: Output ports	F_0 to 3
PG_0	: Output ports	G_0
TEST	: Test	



5) Pin assignment conversion board (EVA-PEX-7E) for LM6417E

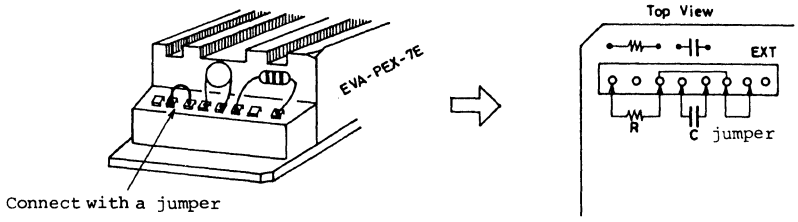
. For evaluation of the LM6417E, the LM64PG97 and the conversion circuit shown in Fig. (a) are used jointly.

Fig. (a) Circuit for pin assignment conversion from LM64PG97 to LM6417E

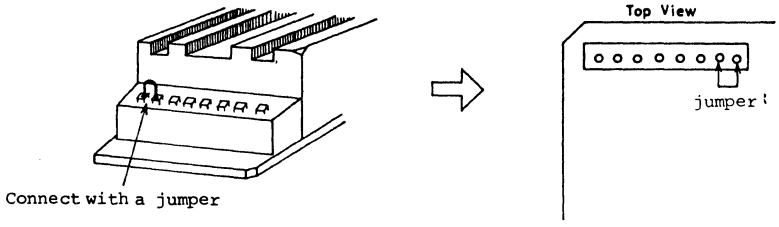


6) Wiring change at CR oscillation option, external drive option

1. Wiring change at CR oscillation option
   When evaluating the LM6417E at CR oscillation option by use of the LM64PG97, wire the jumper of the EVA-PEX-7E and mount C,R as shown below. In this case, if C, R are connected to the LM6417E OSC pin on the user application board, it is unnecessary to remove them. For oscillation frequency, refer 5.5) CR oscillation of LM6417E, LM64PG97 and select C,R so that the same frequency as that of the LM6417E can be obtained.

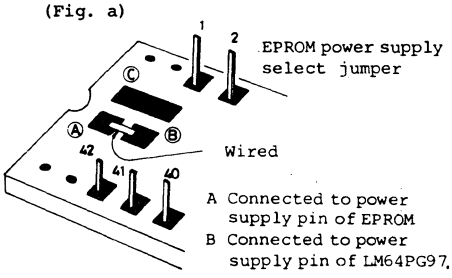


2. Wiring change at external drive option
   When evaluating the LM6417E at external drive option by use of the LM64PG97, connect the jumper of the EVA-PEX-7E as shown below.

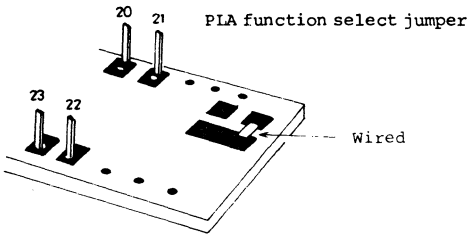


3. Check to see the following before using the LM64PG97.
   (1) The PLA function select jumper is connected. (Fig. a)
   (2) In order that the EPROM power supply and the LM64PG97 power supply (V_{DD}) become the same, the jumper on the back is wired as shown in Fig. b.(*4)

(Fig. a)



(Fig. b)



(3) Insert the following data written EPROM (2716) to the dedicated EPROM (PLA through) socket. (*5)

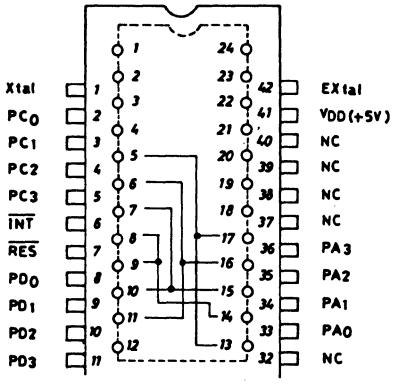
Data for dedicated EPROM (PLA through) (HEX notation)

EPROM address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
010	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
020	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
030	00	11	22	33	44	55	66	77	88	99	AA	BB	CC	DD	EE	FF
040																
050																
⋮																

For EPROM addresses 40_H onward, any data are acceptable.

(This data are commonly called "PLA through")

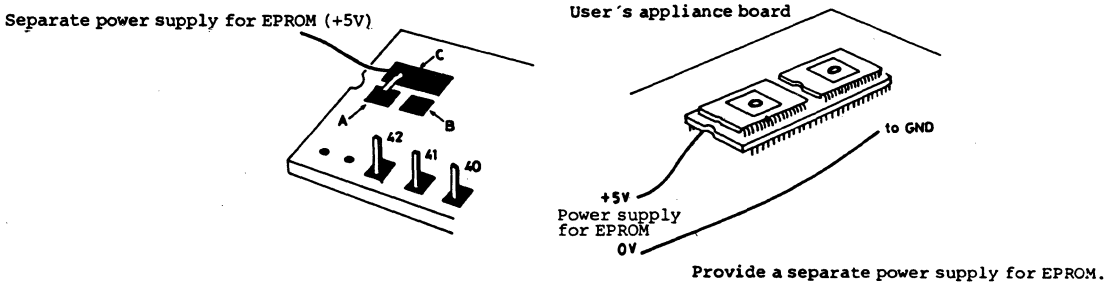
(*5) The connection shown below makes the evaluation possible without inserting the dedicated EPROM.



For the dedicated EPROM (PLA through) socket,
Connect pin 5 with pins 13,17.
pin 6 with pins 11,16.
pin 7 with pins 10,15.
pin 8 with pins 9,14.
Other pins are open.

Connection in case of using no EPROM for "PLA through"

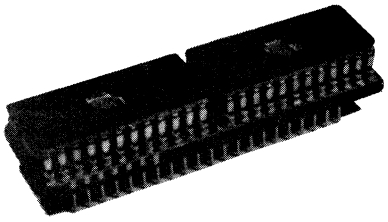
(*4) The EPROM dissipates relatively large current. If the power capacity of user's applicances is insufficient, wire as shown below and provide a separate power supply for the EPROM so that power can be supplied externally.

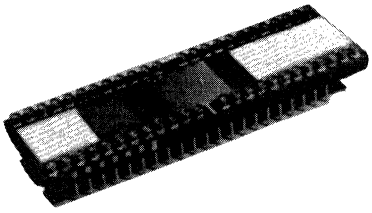


LM64PG99, 64PG98, 64PG97

System Evalustion Chip for LC6400 Series

Ⓔ1248





1. General Description

The LM64PG99/98/99 are system evaluation chips intended for application development tools of 4-bit single-chip microcomputer LM6400 series microcomputers.

With two 24-pin socket for program ROM and PLA EPROM provided on the package surface, they are designed to facilitate the development of the hardware and software for applications based on the LM6400 series microcomputers. Thus, they are ideally suited for use in prototype systems.

The LM64PG99 is for evaluation of the LM6402/05A, H, L, and the LM64PG98 is for evaluation of the LM6413E only, and the LM64PG97 is for evaluation of the LM6416/17E.

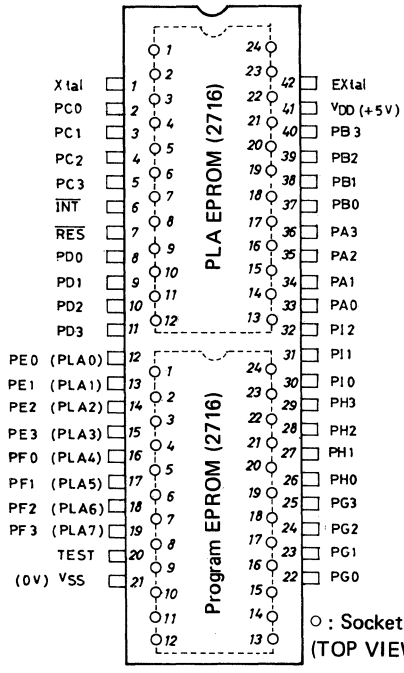
2. Features

- General-purpose 2K-byte EPROM (equivalent to Intel 2716) is usable.
- The LM64PG99 is pin compatible with mass-production products LM6402/05A, H, L, provided that pull-up resistors must be connected externally. (For evaluation of shrink package microcomputers, use the conversion
- board.)
- With the conversion board used jointly, the LM64PG98 can be pin compatible with mass-production product LM6413E.
- With the conversion board used jointly, the LM64PG97 can be pin compatible with mass-production products LM6416E and LM6417E.
- Instruction cycle time: 4 to 40 μsec.
- +5V single power supply.

Note: The LM64PG99/98/97 are designed for application development of the LM6400 series microcomputers. It should be noted that they are not suited for use under high-temperature, high-humidity conditions.

3. Pin Assignment

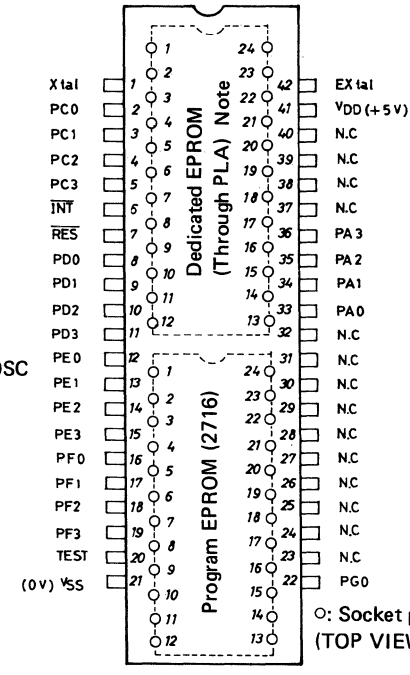
LM64PG99



○ : Socket pin for 2716
(TOP VIEW)

Xtal, EXtal	: Ceramic Resonator, CR for OSC	
$\overline{INT}$	: Interrupt	
$\overline{RES}$	: Reset	
PA_0 to 3	: Input/output ports	A_0 to 3
PB_0 to 3	: Input/output ports	B_0 to 3
PC_0 to 3	: Input/output ports	C_0 to 3
PD_0 to 3	: Input/output ports	D_0 to 3
PE_0 to 3 (PLA_0 to 3)	: Output ports	E_0 to 3 (PLA output 0 to 3)
PF_0 to 3 (PLA_4 to 7)	: Output ports	F_0 to 3 (PLA output 4 to 7)
PG_0 to 3	: Input/output ports	G_0 to 3
PH_0 to 3	: Input/output ports	H_0 to 3
PI_0 to 2	: Input/output ports	I_0 to 3
TEST	: Test	

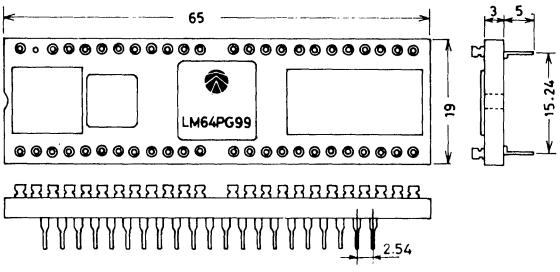
LM64PG97/98



○: Socket pin for 2716
(TOP VIEW)

Xtal, EXtal	: Ceramic Resonator, CR for OSC	
$\overline{INT}$	: Pseudo interrupt	
$\overline{RES}$	: Reset	
PA_0 to 3	: Input port	A_0 to 3
PC_0 to 3	: Input/output ports	C_0 to 3
PD_0 to 3	: Input/output ports	D_0 to 3
PE_0 to 3	: Output port	E_0 to 3
PF_0 to 3	: Output port	F_0 to 3
PG_0	: Output port	G_0
TEST	: Test	

4. Case Outline 3041
(unit: mm)



- For evaluation of the DIP-42S version of the LM6402/05A, H, L, use the board for conversion form DIP-42 to DIP-42S.
- For evaluation of the LM6416E, use the LM64PG97 in conjunction with the circuit for conversion into DIP-28S in Fig. (a).
- For evaluation of the LM6413E, use the LM64PG98 in conjunction with the circuit for conversion into DIP-28S in Fig. (a).
- For evaluation of the LM6417E, use the LM64PG97 in conjunction with the conversion circuit in Fig. (b).
- Shown in Fig. (c) are the external constants for CR oscillation of the LM64PG99/98/97 and the oscillation frequency characteristic.

Fig. (a) Circuit diagram for pin assignment conversion from LM64PG97/98 into LM6416/13E

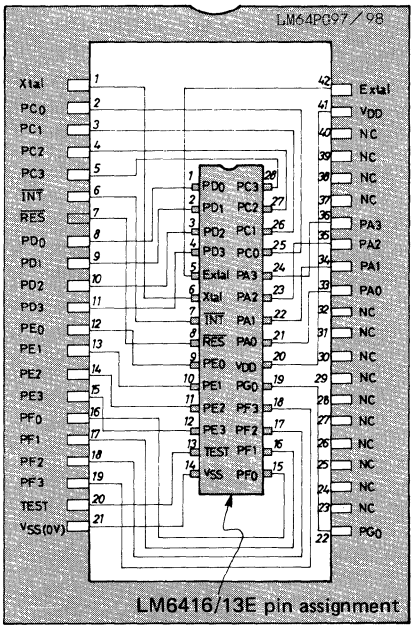


Fig. (b) Circuit diagram for pin assignment conversion from LM64PG97 into LM6417E

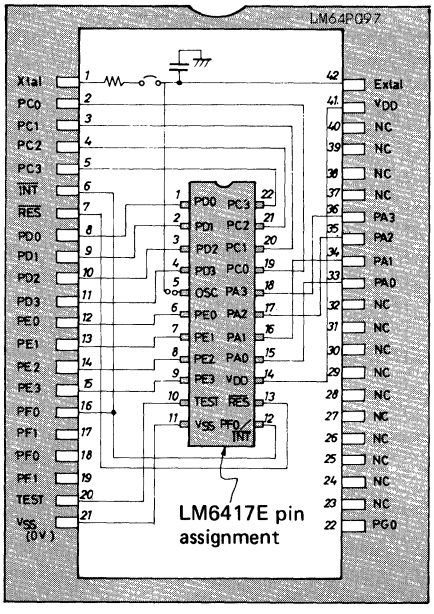
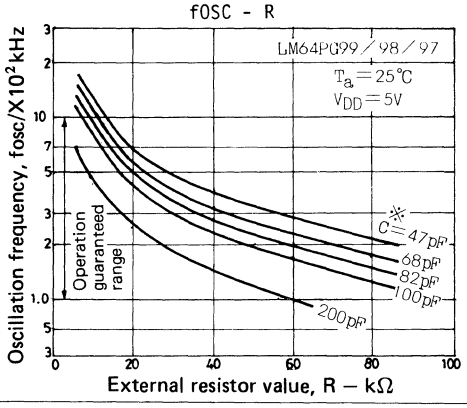


Fig. (c) External constants for CR oscillation of LM64PG99/98/97 and oscillation frequency characteristic

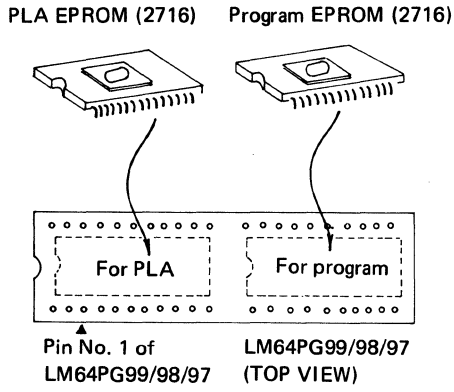


(Note) *: External capacitor value C also includes stray capacitance of the board wiring, etc.

5. EPROM Mounting

Mount the program EPROM and the PLA EPROM. For writing into the EPROM, use the EPROM writer function of the EVA-410.

For preparing data of the PLA EPROM, refer to Chapter 3, Paragraph 3.6.4 of SOFTWARE DEVELOPMENT TOOL MANUAL.



6. Table of LM6400 Series

The LM6400 series are prepared to allow an optimum selection as follows:

Type No.	Application	ROM	RAM	Cycle time	I_{DD} (typ)	Package	Remarks
LM6402A	General	2K bytes	128 x 4 bits	10μs	30mA	DIP-42 DIP-42S	
LM6405A		1K bytes	64 x 4 bits	10μs	30mA	DIP-42 DIP-42S	
LM6402H	High speed	2K bytes	128 x 4 bits	5μs	35mA	DIP-42 DIP-42S	
LM6405H		1K bytes	64 x 4 bits	5μs	35mA	DIP-42 DIP-42S	
LM6402L	Low power Dissipation	2K bytes	128 x 4 bits	20μs	10mA	DIP-42 DIP-42S	
LM6405L		1K bytes	64 x 4 bits	20μs	10mA	DIP-42 DIP-42S	
LM6413E	Small scale	2K bytes	128 x 4 bits	4 to 40μs	20mA	DIP-28S	
LM6416E		1K bytes	64 x 4 bits	4 to 40μs	17mA	DIP-28S	
LM6417E		1K bytes	64 x 4 bits	4 to 40μs	17mA	DIP-22	
LM6499	LM6402/05A, H, L system development	External 2K bytes	128 x 4 bits	5 to 20μs	30mA	QIC-80	Evaluation chip
LM6498	LM6413E system development	External 2K bytes	128 x 4 bits	4 to 40μs	20mA	QIC-80	Evaluation chip
LM6497	LM6416/17E system development	External 2K bytes	64 x 4 bits	4 to 40μs	20mA	QIC-80	Evaluation chip
LM64PG99	LM6402/05A, H, L system evaluation	External 2K bytes	128 x 4 bits	5 to 20μS	*130mA	DIC-42	Simulation chip
LM64PG98	LM6413E system evaluation	External 2K bytes	128 x 4 bits	4 to 40μs	*120mA	DIC-42	Simulation chip
LM64PG97	LM6416/17E system evaluation	External 2K bytes	64 x 4 bits	4 to 40μs	*120mA	DIC-42	Simulation chip

*Including EPROM (2716)

7. Proper Cares in Using LM64PG99, 98, 97

LM64PG99

- Mount the program EPROM and the PLA EPROM. Even when the PLA function is not used, the PLA EPROM (through PLA) must be mounted in principle. For how to prepare the through PLA, refer to SOFTWARE DEVELOPMENT TOOL MANUAL. For nonuse of the through PLA EPROM, refer to 8-(3) below.
- For evaluating the input/output option as pull-up resistor-contained type output port, connect an external resistor to the pin of the LM64PG99.
- All input/output ports are input/output common and of high threshold input, open drain output type. E, F ports are for output only.

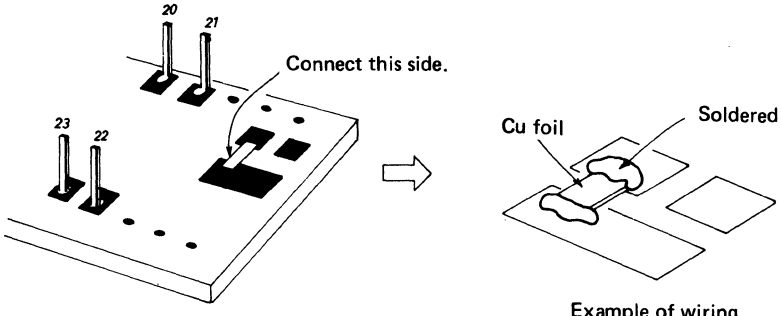
LM64PG98/97

- The LM6416/17E and LM6413E have no PLA function. However, since the LM64PG98/97 use the same package as the LM64PG99, two EPROM's for program and PLA (through PLA) must be mounted in principle when performing evaluation. For nonuse of the through PLA EPROM, refer to 8-(3) below.

8. Wiring Change according to Use/Nonuse of PLA Function

(1) Wiring change in case of use of PLA function

When the PLA function is used in evaluating the LM6402/05A, H, L with the LM64PG99, wire the jumper on the package bottom as follows:
Use the PLA EPROM with PLA data written.



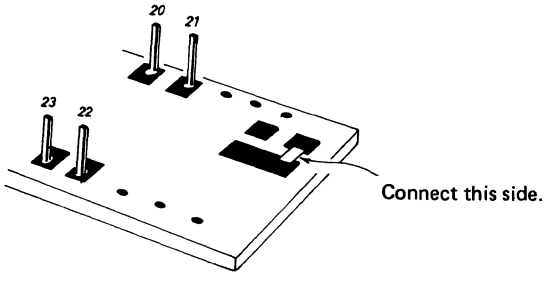
(When PLA is used)

Example of wiring

(2) Wiring change in case of nonuse of PLA function

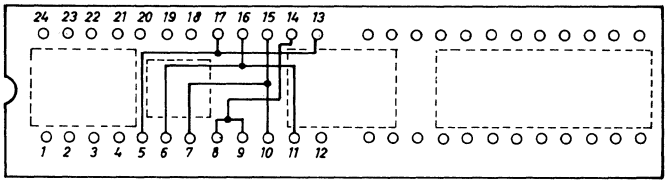
When the PLA function is not used in evaluating the LM6402/05A, H, L or when the LM6413/16/17E (with no PLA function provided) are evaluated with the LM64PG98/97, wire the jumper on the package bottom as follows:
For the PLA EPROM, use [through PLA] with data for nonuse of PLA written.

(Note)
1. The PLA function of the LM64PG98/97 is set to nonuse at the time of shipment.
2. Setting of use/nonuse of the PLA function must be made.



(3) Wiring change where no through PLA EPROM is required to be used in case of nonuse of PLA function
- The through PLA EPROM function can be fulfilled by wiring jumpers. The wiring diagram is shown in Fig. (d) below.

Fig. (d) Through PLA wiring diagram using jumpers

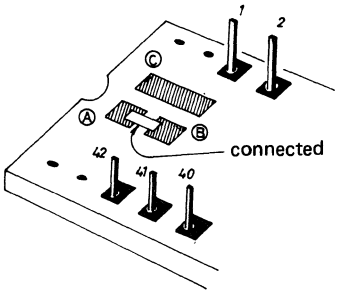


PLA EPROM section Program EPROM

9. Selection of Power Supply to EPROM (External power supply)

Normally, an EPROM dissipates a current of 50 to 100mA (i.e. 200mA max./2 EPROM's). If the power capacity of a user system is not enough, an external power supply can be used.

(1) The same power supply as to the LM64PG99/98/97 is used at the time of shipment.
A jumper for EPROM power supply select is provided on the package bottom of the LM64PG99/98/97. The power supply to the EPROM is connected to the power supply pin (V_{DD} pin) of the LM64PG99/98/97 as shown below.



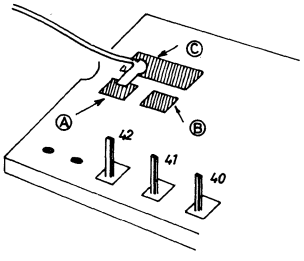
Ⓐ Connected to power supply pin of EPROM

Ⓑ Connected to power supply pin of LM64PG99/98/97

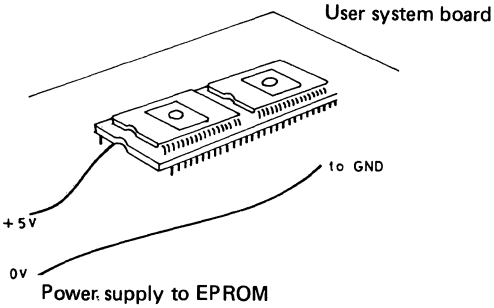
(At the time of shipment the same power supply is used for the LM64PG99/98/97 and the EPROM.)

(2) How to provide external power supply to EPROM
- Remove the wiring connecting patterns (A) and (B).
- Using this jumper, connect patterns (A) and (C).
- Connect external power supply (+5) to pattern (C) and external power supply (0V) to GND (0V) of the user system board.
  See below.

External power supply (+5V)



(External power supply to EPROM)



Power supply to EPROM

(Note)
- The LM64PG99/98/97 are designed for application development of the LM6400 series microcomputers. It should be noted that they are not suited for use under high-temperature, high-humidity conditions.
- For general-purpose 2K-byte EPROM, use Intel 2716 or its equivalent.

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +10	V
Input Voltage	V_{IN}		−0.3 to +12	V
Output Voltage	$V_{OUT(1)}$	Output transistor OFF	−0.3 to +12	V
Average Output Current	$I_{OLA(1)}$	All pins of C and D ports	20	mA
(Applicable to any 100ms	$I_{OLA(2)}$	Each pin of E and F ports	40	mA
period)	$I_{OLA(3)}$	All pins of E or F port	100	mA
	$I_{OLA(4)}$	All pins of A, B, G, H and I ports	50	mA
Peak Output Current	I_{OHP}	Each pin for pull-up	−2.0	mA
	$I_{OLP(1)}$	Each output pin other than E, and E ports	4	mA
	$I_{OLP(2)}$	Each pin of E and F ports	40	mA
	$I_{OLP(3)}$	All pins of E or F port	100	mA
Power Dissipation	P_d max	T_a=+10 to +40°C	600	mA
Operating Temperature	T_{opg}		+10 to +40	°C

Allowable Operating Ranges/T_a=25°C, V_{SS}=0V				min	typ	max	unit
Operating Supply Voltage		V_{DD}		4.5	5.0	5.5	V
Input/output common	"H" level input voltage	$V_{IH(2)}$		0.6V_{DD}			V
port for high-threshold	"L" level input voltage	$V_{IL(2)}$		V_{SS}		0.25V_{DD}	V
INT, RES	"H" level input voltage	$V_{IH(3)}$		0.7V_{DD}		V_{DD}	V
	"L" level input voltage	$V_{IL(3)}$		V_{SS}		0.25V_{DD}	V
Extal	"H" level input voltage	$V_{IH(4)}$		0.7V_{DD}		V_{DD}	V
	"L" level input voltage	$V_{IL(4)}$		V_{SS}		0.6	V
	Clock cycle time	$t_{c(\phi)}$	V_{DD}=5V±10% Refer to Fig. 1	1		10	μs
	"H" level clock pulse width	$t_{w\phi H}$	V_{DD}=5V±10% Refer to Fig. 1	0.4			μs
	"L" level clock pulse width	$t_{w\phi L}$	V_{DD}=5V±10% Refer to Fig. 1	0.4			μs
External Resistance value for oscillator		R	Refet to Fig. 2		1000		kΩ
External Capacitance value		C_1	Refer to Fig. 2		220		pF
for oscillator		C_2	Refer to Fig. 2		220		pF
TEST	"L" level input voltage	$V_{IL(6)}$	V_{DD}=5V±10%	V_{SS}		0.4	V

Electrical Characteristics/T_a=−30 to +70°C, V_{DD}=5V±10%, V_{SS}=0V				min	typ	max	unit
RES, INT	"H" input level current	$I_{IH(1)}$	V_{IN}=V_{DD}			10	μA
	"L" input level current	$I_{IL(1)}$	V_{IN}=V_{SS}	−10			μA
Input/output common port	"H" level input current	$I_{IH(2)}$	V_{IN}=V_{DD}			10	μA
	"L" level input current	$I_{IL(2)}$	V_{IN}=V_{SS}	−10			μA
Input/output common	"L" level input voltage	$V_{OL(2)}$	I_{OL}=1.8mA			0.4	V
port for open drain	Output off leak current	$I_{OFF(1)}$	V_{OH}=10V			30	μA
		$I_{OFF(2)}$	V_{OH}=5.5V			10	μA
E, F ports	"L" output level voltage	$V_{OL(3)}$	I_{OL}=20mA			2	V
	Output off leak current	$I_{OFF(3)}$	V_{OH}=10V			30	μA
		$I_{OFF(4)}$	V_{OH}=5.5V			10	μA
Current Dissipation		I_{DD}	V_{DD}=5.5V Input/output pins OPEN, OSC in oscillation (Except EPROM current)		30		mA
Input pins capacitance		C_I			10		pF

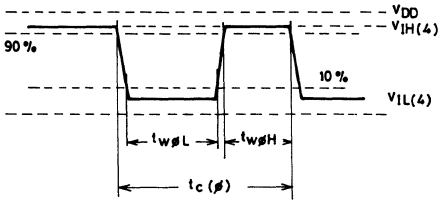
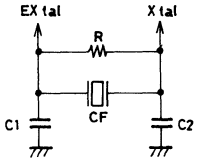


Fig. 1 EXtal input waveform

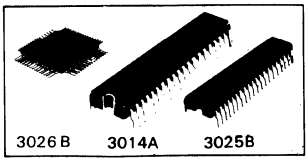


CF: Cermaic resonator
CSB 400P
KBR 400B
CSB 800A
KBR 800H

Fig. 2 Recommended oscillator for cermaic oscillation

(Note) • The LM64PG99/98/97 are designed for application development of the LM6400 series microcomputers. it should be noted that they are not suited for use under high-temperature, high-humidity conditions.
• For general-purpose 2K-byte ERPOM, use Intel 2716 or its equivalent.

LC6502B, 6505B



C MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1265A

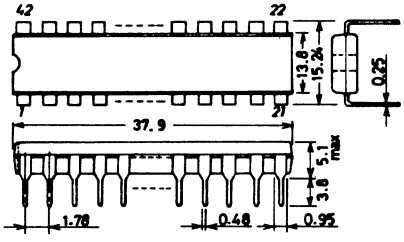
General Description

The LC6502B/05B, being identical with the standard type LC6502C/05C in the internal architecture and instruction set, are capable of interfacing direct with a fluorescent display tube because high voltage input/output ports are provided. Therefore, user's application equipment can be made with fewer parts and at less cost.

Features

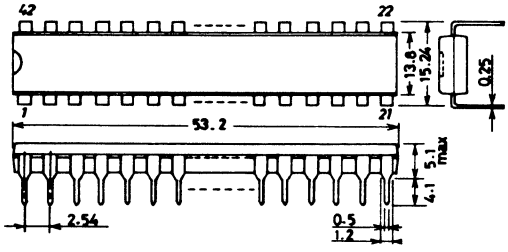
- Low power dissipation C MOS single-chip microcomputer
- Instruction set with 79 instructions being common to the LC6502C/6505C
- 2-source, 2-level interrupt (external interrupt/internal timer interrupt)
- 4-level stack
- 4-bit prescaler-contained 8-bit programmable timer
- Fluorescent display tube driver-contained input/output ports
  (1) Digits driving output ports: 10 ports
  (2) Segments driving output ports: 8 ports
  (3) High voltage input ports: 8 ports
  (4) Normal voltage input/output ports: 8 ports
- ROM, RAM
  (1) LC6502B ROM: 2048 bytes, RAM: 128x4 bits
  (2) LC6505B ROM: 1024 bytes, RAM: 64x4 bits

Case Outline 3025B-D42SIC
(unit:mm)

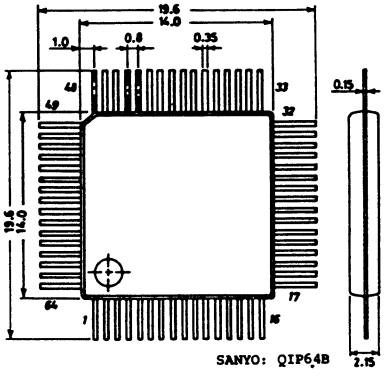


SANYO: DIP42S

Case Outline 3014A-D42IC
(unit:mm)



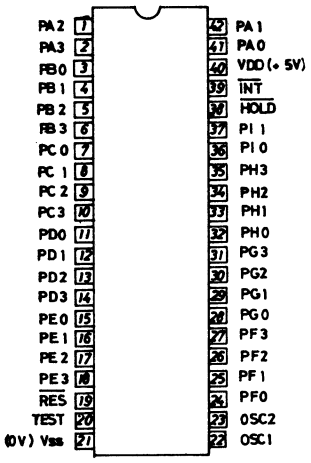
Case Outline 3026B-Q64BIC SANYO: DIP42
(unit:mm)



SANYO: QIP64B

For details, refer to LC6500 Series User's Manual.

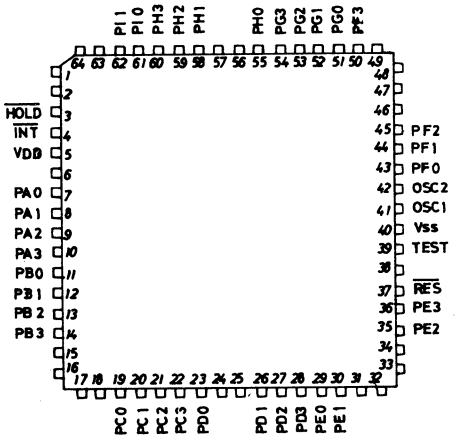
Pin Assignment



DIP42, DIP42S

Pin Name

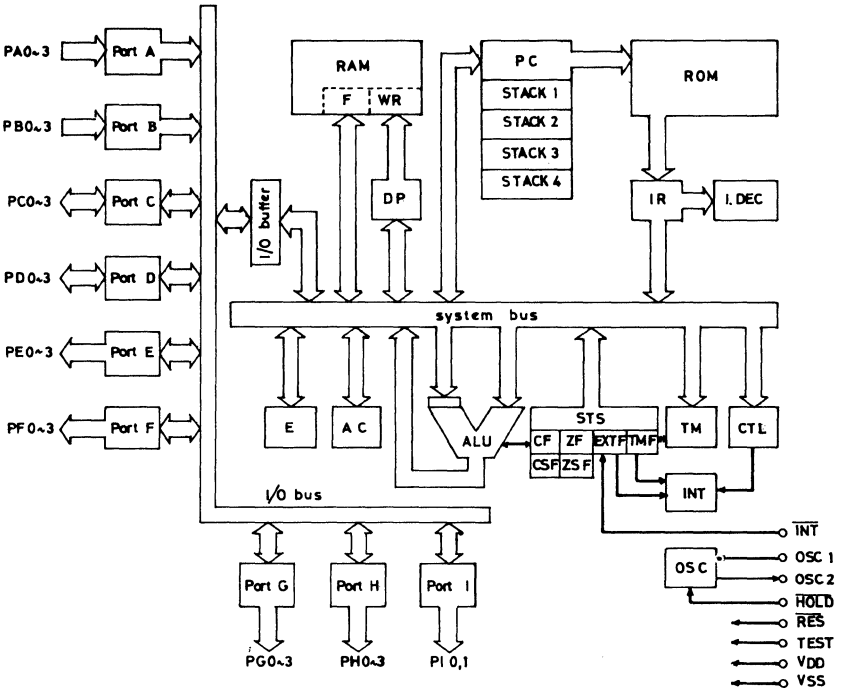
OSC1,OSC2	: C,R or cermic resonator for OSC	
INT	: Interrupt	
RES	: Reset	
HOLD	: Hold	
PA_{0-3}	: Input ports	A_{0-3}
PB_{0-3}	: Input ports	B_{0-3}
PC_{0-3}	: Input/output Common ports	C_{0-3}
PD_{0-3}	: Input/output common ports	D_{0-3}
PE_{0-3}	: Output ports	E_{0-3}
PF_{0-3}	: Output ports	F_{0-3}
PG_{0-3}	: Output ports	G_{0-3}
PH_{0-3}	: Output ports	H_{0-3}
PI_{0-3}	: Output ports	$I_{0,1}$
Test	: Test	



QIP64 (Under development)

(Note) Pins with no pin name:
No connection

System Block Diagram



RAM	: Data memory	ROM	: Program memory
F	: Flag	PC	: Program counter
WR	: Working register	INT	: Interrupt control
AC	: Accumulator	IR	: Instruction register
ALU	: Arithmetic and logic unit	I.DEC	: Instruction decoder
DP	: Data pointer	CF,CSF	: Carry flag, carry save flag
E	: E register	ZF,ZSF	: Zero flag, zero save flag
CTL	: Control register	EXTF	: External interrupt request flag
OSC	: Oscillation	TMF	: Internal interrupt request flag
TM	: Timer		
STS	: Status register		

Pin Description

Pin Name	Input/ Output	Function
$\overline{INT}$	Input	Interrupt request input pin.
$\overline{HOLD}$	Input	Hold mode request input pin.
$\overline{RES}$	Input	Reset input pin.
PA_{0-3}	Input	Input ports A_0 to A_3 **(High voltage)**. Capable of 4-bit input and single-bit decision for branch. Also used for halt mode release request input.

(continued on next page)

PB_{0-3}	Input	Input ports B_0 to B_3 (High voltage). **Capable of 4-bit input and single-bit decision for branch.**
PC_{0-3}	Input/ Output	Input/output common ports C_0 to C_3 (Normal voltage). Capable of 4-bit input and single-bit decision for branch during input. Capable of 4-bit output and single-bit set/reset during output.
PD_{0-3}	Input/ Output	Input/output common ports D_0 to D_3 (Normal voltage). Capable of 4-bit input and single-bit decision for branch during input. Capable of 4-bit output and single-bit set/reset during output.
PE_{0-3}	Output	Output ports E_0 to E_3 (Digits driver outputs). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch.
PF_{0-3}	Output	Output ports F_0 to F_3 (Digits driver outputs). Cpable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch.
PG_{0-3}	Output	Output ports G_0 to G_3 (Segments driver outputs). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch.
PH_{0-3}	Output	Output ports H_0 to H_3 (Segments driver outputs). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch.
$PI_{0,1}$	Output	Output ports I_0, I_1 (Digits driver outputs). Capable of 2-bit output and single-bit set/reset. Capable of 2-bit input of output latch contents and single-bit decision of output latch for branch.
OSC1	Input	Pin for supplying external clock. When using internal clock oscillation, C,R or ceramic resonator is conntected to this pin and pin OSC2.
OSC2	Output	Pin for externally connecting resonance circuit for internal clock oscillation.
V_{DD}	Input	Power supply pin Normally connected to +5V.
V_{SS}		Connected to 0V power supply.
TEST	**Input**	**LSI test pin. Normally connected to V_{SS}(0V).**

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}		-0.3 to +7.0	V
Input Voltage	$V_{IN(1)}$	Input pins other than ports A,B	-0.3 to V_{DD}+0.3	V Note 1
	$V_{IN(2)}$	Ports A, B	V_{DD}-40 to V_{DD}+0.3	V
Output Voltage	$V_{OUT(1)}$	Ports C,D OSC2	-0.3 to V_{DD}+0.3	V
	$V_{OUT(2)}$	POrts E,F,G,H,I	V_{DD}-40 to V_{DD}+0.3	V
Peak Output Current	$I_{O(1)}$	Ports C,D OSC2: Each pin	-2.0 to +2.0	mA
	$I_{O(2)}$	Ports E,F,I: Each pin	-15 to 0	mA
	$I_{O(3)}$	Ports G,H: Each pin	-3 to 0	mA
	$I_{O(4)}$	All pins of ports C to I	-90 to +16	mA
Allowable Power Dissipation	Pd max	Ta≦70°C	350	mW
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Note 1: For pin OSC1, up to oscillation amplitude generated when internally oscillated under the recommended oscillation conditions in Fig. 4 is allowable.

Recommended Operating Conditions at Ta=-30 to +70°C, V_{DD}=5V±10%, V_{SS}=0V

			min	typ	max	unit
Recommended Operating Supply Voltage	$V_{DD(1)}$		4.5	5.0	5.5	V
Power-down Supply Voltage	$V_{DD(2)}$	HOLD mode: $\overline{HOLD}$=$V_{IL(3)}$	2.0		5.5	V
Input "H"-Level Voltage	$V_{IH(1)}$	Ports A,B,C,D	0.7V_{DD}		V_{DD}	V
	$V_{IH(2)}$	$\overline{INT}$,$\overline{RES}$,$\overline{HOLD}$ and OSC1	0.75V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL(1)}$	Ports C,D	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	$\overline{INT}$,$\overline{RES}$,OSC1	V_{SS}		0.25V_{DD}	V
	$V_{IL(3)}$	$\overline{HOLD}$:V_{DD}=2.0～5.5V	V_{SS}		0.3V_{DD}-0.3	V
	$V_{IL(4)}$	TEST	V_{SS}		0.3V_{DD}	V
	$V_{IL(5)}$	Ports A,B	V_{DD}-35		0.3V_{DD}	V
Operating Clock Frequency	f_{extosc}	At external clock mode, input is applied to OSC1, OSC2 is open. See Fig. 2.	20		420	KHz
"H"-Level Clock Pulse Width	$t_{wØH}$	"	0.5			us
"L"-Level Clock Pulse Width	$t_{wØL}$	"	0.5			us
Clock Input Rise Time	t_{oscR}	"			0.2	us
Clock Input Fall Time	t_{oscL}	"			0.2	us
External Capacitance for CR Oscillation	C_{ext}	See Fig. 3.	33	82	470	pF
External Resistance for CR Oscillation	R_{ext}	"	20	47	200	Kohm
External Capacitance for Ceramic Oscillation	C_1	Resonator CSB400P:See Fig.4.		100±10%		pF
		" KBR400B: "		100±10%		pF
	C_2	" CSB400P: "		100±10%		pF
		" KBR400B: "		100±10%		pF
External Resistance for Ceramic Oscillation	R_1			1000±5%		Kohm
	R_2			4.7±5%		Kohm
Power-down $\overline{HOLD}$ setup Time	t_{HOLDS}	See Fig. 1.	2			ms
Power-down $\overline{HOLD}$ Hold Time	t_{HOLDH}	See Fig. 1.	50			us

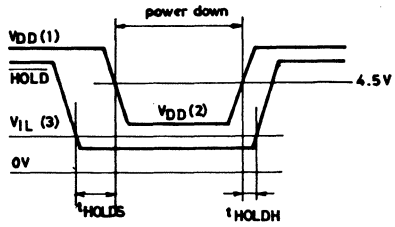


Fig. 1 Power-down mode timing

Electrical Characteristics at Ta=-30 to +70°C, V_{DD}=5.0±10%, V_{SS}=0V

			min	typ	max	unit
Input "H"-Level Current	$I_{IH}(1)$	Input pins other than ports A,B: $V_{IN}=V_{DD}$			1.0	uA
	$I_{IH}(2)$	Ports A,B: $V_{IN}=V_{DD}$			10	uA
Input "L"-Level Current	$I_{IL}(1)$	Input pins others than ports A,B: $V_{IN}=V_{SS}$	-1.0			uA
	$I_{IL}(2)$	Ports A,B: $V_{IN}=V_{DD}$-35V	-30			uA
Output "H"-Level Voltage	$V_{OH}(1)$	Ports C,D: I_{OH}=-1mA	V_{DD}-2			V
	$V_{OH}(2)$	Ports C,D: I_{OH}=-100uA	V_{DD}-0.5			V
	$V_{OH}(3)$	Ports E,F,I: I_{OH}=-10mA	V_{DD}-2.5			V
	$V_{OH}(4)$	Ports E,F,I: I_{OH}=-1mA	V_{DD}-0.6			V
	$V_{OH}(5)$	Ports G,H: I_{OH}=-2mA	V_{DD}-1.0			V
	$V_{OH}(6)$	Ports C,H: I_{OH}=-1mA	V_{DD}-0.6			V
Output "L"-Level Voltage	$V_{OL}(1)$	Ports C,D: I_{OL}=1mA			0.4	V
Output off Leak Current	$I_{OFF}(1)$	Ports C,D: $V_{OUT}=V_{DD}$			1.0	uA
	$I_{OFF}(2)$	Ports C,D: $V_{OUT}=V_{SS}$	-1.0			uA
	$I_{OFF}(3)$	Ports E,F,G,H,I: $V_{OUT}=V_{DD}$			30	uA
	$I_{OFF}(4)$	Ports E,F,G,H,I: $V_{OUT}=V_{DD}$-35V	-30			uA
Clock Oscillation Frequency for Ceramic Oscillation	f_{XOSC}	At oscillation circuit in Fig. 4: Recommended condition for ceramic oscillation	384	400	417	KHz
Clock Oscillation Frequency for CR Oscillation	f_{CROSC}	At oscillation circuit in Fig. 3: C_{ext}=82pF±5% R_{ext}=47Kohm±1%	200	300	400	KHz

(continued on next page)

			min	typ	max	unit
Current Dissipation	$I_{DD}(1)$			0.4	1.0	mA
		CR oscillation,in operating mode: C_{ext}=82pF,R_{ext}=47Kohm, Output pin open, $V_{IN}=V_{DD}$				
	$I_{DD}(2)$			0.5	1.0	mA
		Ceramic oscillation,in operating mode: Recommended oscillation condition for ceramic oscillation,output pin open, input pin $V_{IN}=V_{DD}$				
	$I_{DD}(3)$	Halt mode: V_{DD}=5V±10% At Test circuit in Fig. 5		0.5	10	uA
	$I_{DD}(4)$	Hold mode: V_{DD}=5V±10% At Test circuit in Fig. 6		0.5	10	uA
	$I_{DD}(5)$	Hold power-down mode: V_{DD}=2.0V At test circuit in Fig. 6		0.1	2	uA
Input Capacitance	C_{IN}	Ports A,B: Measured at f=1MHz		5		pF
		$\overline{RES}$,$\overline{INT}$,$\overline{HOLD}$,OSC1: Measured at f=1MHz		5		pF
Output Capacitance	C_{OUT}	OSC2: Measured at f=1MHz		10		pF
		Ports E,F,G,H,I Measured at f=1MHz Output off		20		pF
Input/Output Capacitance	C_{IO}	Ports C,D: Measured at f=1MHz,output inhibit		10		pF

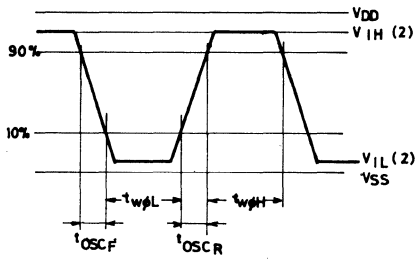


Fig. 2 OSC1 input waveform

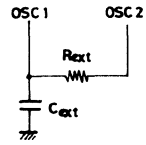
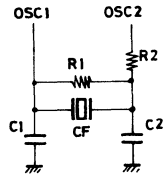
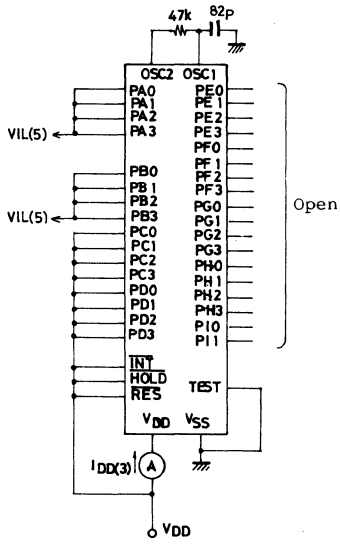


Fig. 3 Recommended oscillation circuit for CR oscillation



CF :
Ceramic resonator
CSB400P (Murata)
KBR400B (Kyocera)

Fig. 4 Recommended oscillation circuit for ceramic oscillation



Input/output common ports C,D: Output inhibit
HALT instruction is executed to cause halt mode to be entered.

Fig. 5 $I_{DD(3)}$ test circuit

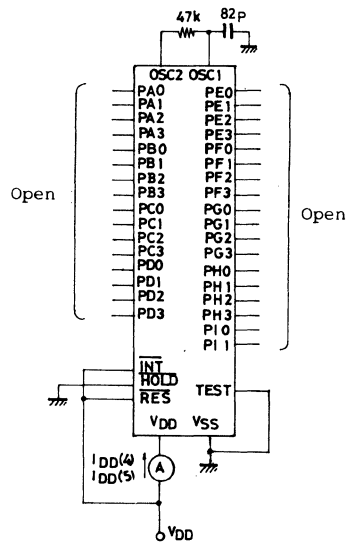


Fig. 6 $I_{DD(4)}$,$I_{DD(5)}$ test circuit

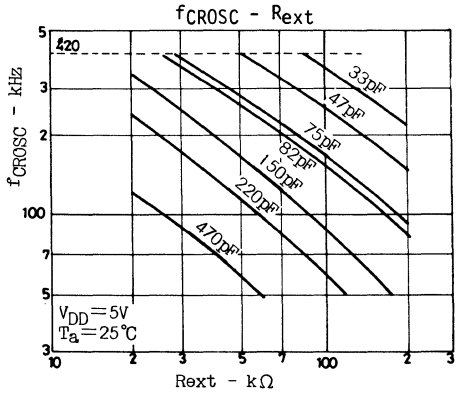


Fig. 7 CR oscillation frequency data (typical)

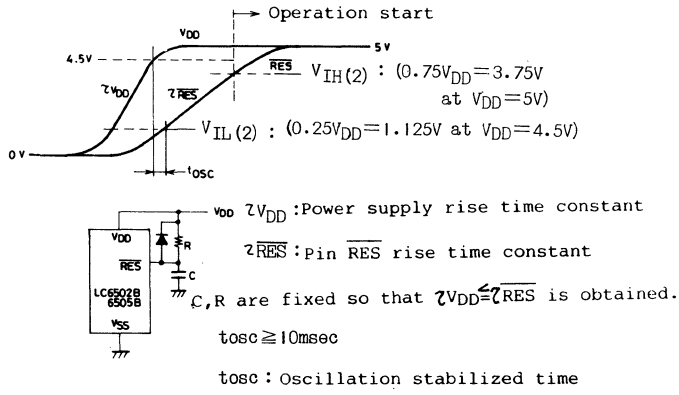


Fig. 8 Initial reset timing

Appendix 1. Support System

For application development of the LC6502B/05B,the support system for the LC6502C/05C is used.

1-1. Software support

The SDS-410 system provides source editor, cross assembler. For cross assembler, [LC6502], [LC6505] are used.

1-2. Hardware support

(1) Evaluation chip

Evaluation chip LC6599 is used. A level converter, driver are connected to high voltage ports externally. (A dedicated adaptor is available.)

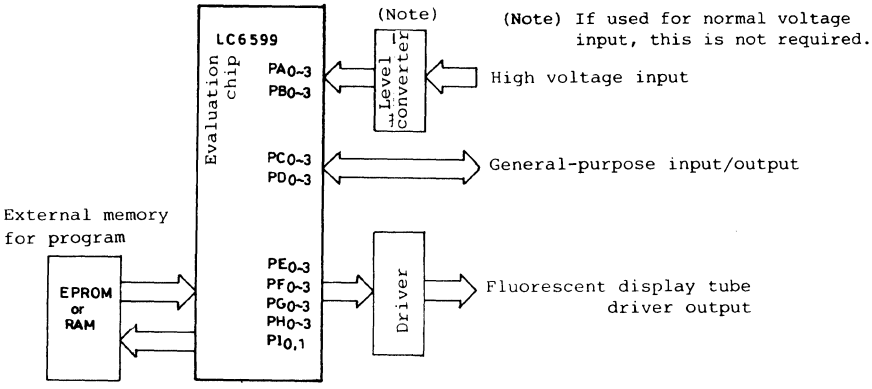


Fig. 1-1 Basic evaluation system using evaluation chip

(2) Evaluation board

Evaluation board EVA-402A and an adaptor for the LC6502B/05B are used jointly.

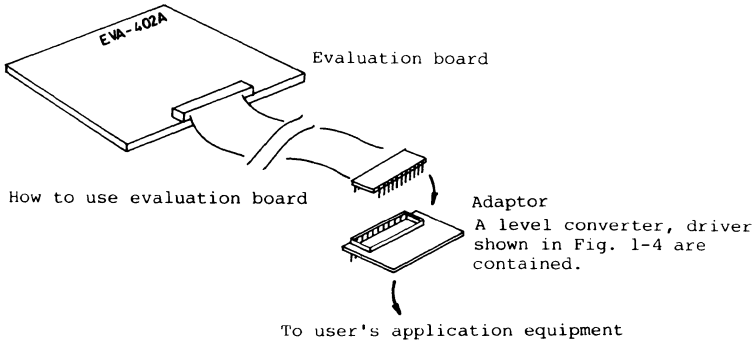


Fig. 1-2 How to use evaluation board

(3) Simulation chip

Piggyback LC65PG99 and an adaptor for the LC6502B/05B are used jointly.

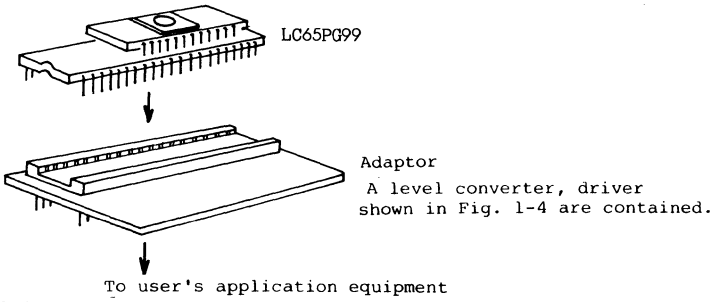


Fig. 1-3 How to use piggyback

(4) Evaluation Kit
The EVA-410 and EVA-TB2 are used. For connecting with user's application equipment, an adaptor is used.

(5) Adaptor
This is used when evaluation the LC6502B/05B with the aid of the evaluation chip and piggyback. This contains a level converter for high voltage input ports and a driver for fluorescent display tube. (See Figs. 1-4, 1-5.)

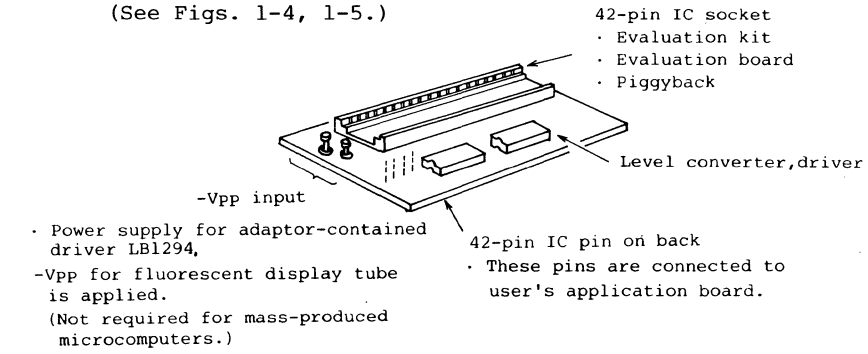


Fig. 1-4 Adaptor for LC6502B/05B

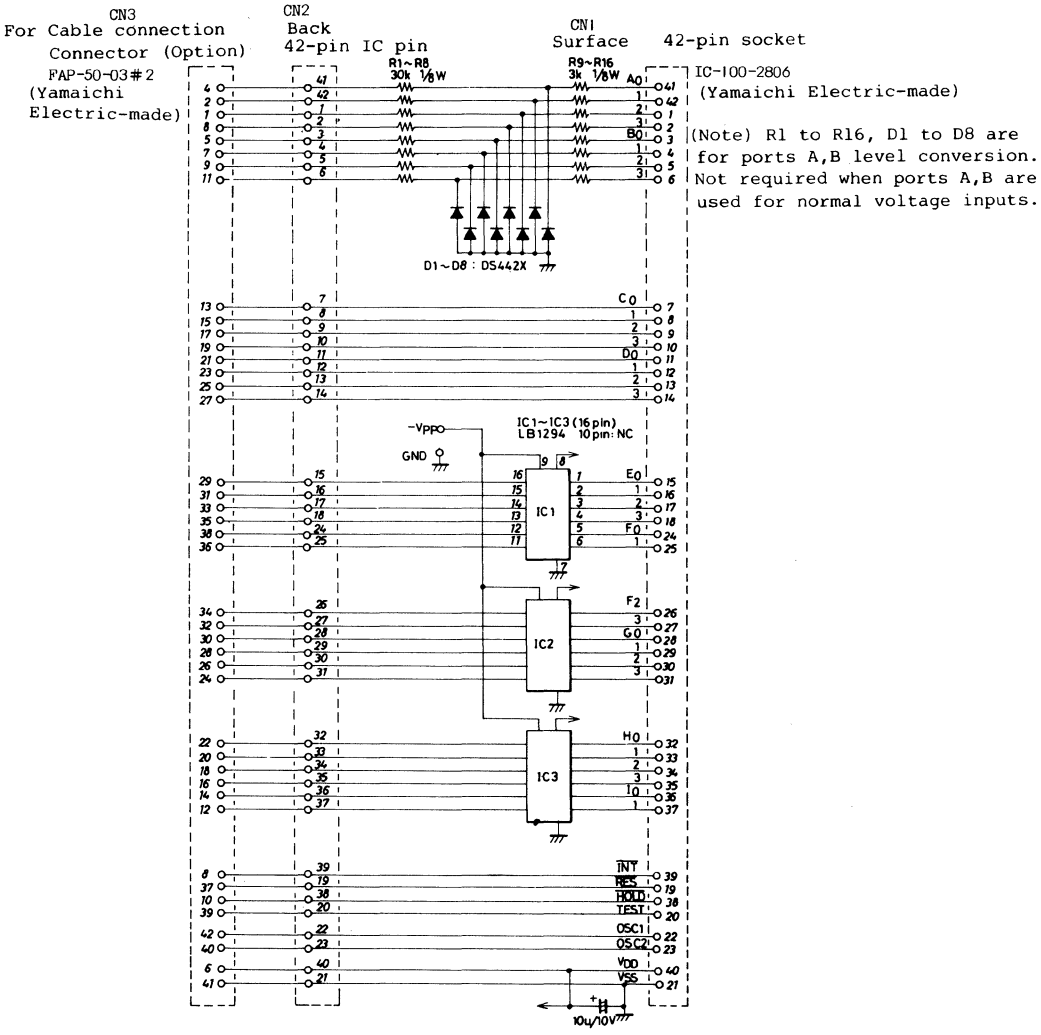


Fig. 1-5 Adaptor

Appendix 2. Internal Architecture of LC6502B,05B

The LC6502B/05B are quite identical with the standard type LC6502C/05C in the internal architecture and instruction set except that input/output ports are of high voltage type. For details, refer to "LC6500 series User's Manual".

2-1. PC

For the LC6502B/05B, this is organized with a 11-bit/10-bit binary counter respectively which specify the ROM address of an instruction to be executed next. The contents of the hig-order 3(2) bits specify a page and the contents of the low-order 8 bits specify an address in the page. The page is updated automatically. ( ) is for the LC6505B.

2-2. ROM

This is used to store user programs. For the LC6502B/05B, this is organized with 2048 x 8 bits/1024 x 8 bits respectively. By using the ROM table read instruction, the whole area can be accessed and the display pattern can be programmed.

2-3. Stack

This is used to save the contents of the PC at the subroutine call or interrupt mode. This allows subroutine nesting up to 4 levels.

2-4. DP

This is a register organized with 4-bit DP_L and 3-bit/2-bit DP_H for the LC6502B/05B respectively. When accessing the data RAM, the DP_L/DP_H specify a column address/row address respectively. When accessing the input/output ports, the DP_L specifies port A to port I.

2-5. RAM

This is a static RAM which is used to store data. For the LC6502B/05B, this is organized with 128 x 4 bits/64 x 4 bits respectively. Row address 7H(3H) is allocated for 16-bit flags and 8-word working registers which can be manipulated without being addressed by the DP.( ) is for the LC6505B.

2-6 AC,E

The AC is a 4-bit register which stores data to be processed by instructions. The E register is an auxiliary register to back up the AC and is used as a temporary register or general-purpose register at the instruction execution mode.

2-7 ALU

This is a circuit which performs arithmetic and logic operations specified by individual instructions. This ouputs not only data of operation results but also the status of carry (C) or/and zero (Z).

2-8. Status register

This is a 4-bit register which stores the status of carry or zero and the external interrupt, timer interrupt request. The contents of the status register can be tested by the branch instructions.

2-9. Timer

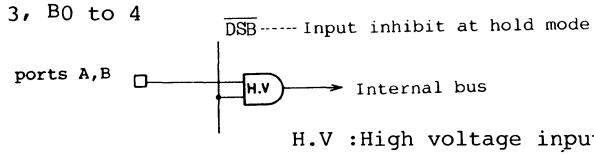
This consists of a 4-bit fixed prescaler and a 8-bit programmable timer. This counts the system clock and requests a timer interrupt when an overflow occurs.

2-10. Control register

This is a 4-bit register, 2 bits of which control input/output of input/output common ports C,D and 2 bits of which enable/disable external interrupt, internal timer interrupt.

2-11. Input/output ports there are 9 ports/34 pins from port A to I. Each port is addressed by the DP_L. Ports A,B are of high voltage input type, ports C,D are of normal voltage input/output common type, and ports E,F,G,H,I contain a fluorescent display tube driver.

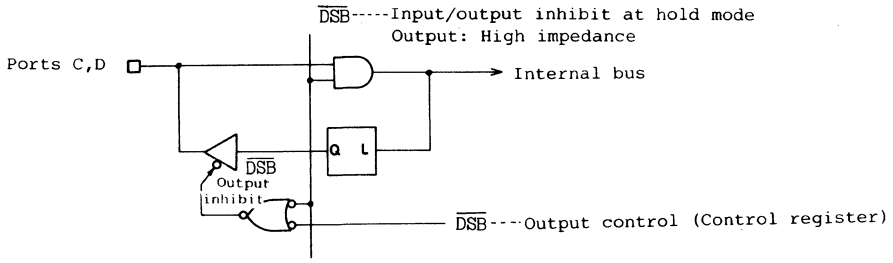
(1) Ports A_0 to 3, B_0 to 4



H.V :High voltage input(max V_{DD}-40V)

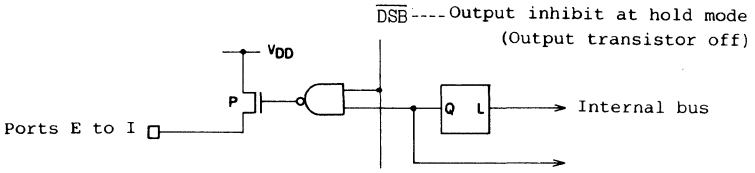
Functions · 4-bit input (IP instruction)
· Single-bit test (BP,BNP instructions)

(2) Ports C_0 to 3, D_0 to 3



Functions
1. Input mode (Output inhibit)
   - 4-bit input (IP instruction)
   - single-bit test (BP, BNP instructions)
2. Output mode
   - 4-bit output (OP instruction)
   - Single-bit set/reset (SPB, RPB instructions)

(3) Ports E_0 to 3, F_0 to 3, G_0 to 3, H_0 to 3, I_0 to 1



Functions
- 4-bit (2-bit for port I) output (OP instruction)
- 4-bit (2-bit for port I) input of output latch contents (IP instruction)
- Single-bit set/reset (SPB,RPB instructions)
  Set: The output represents a 1.---- Output transistor on
  Reset: The output represents a 0.---- Output transistor off
- Single-bit test of output latch contents (BP,BNP instructions)
- Ports E,F,I: Fluorescent display tube digits drive
- Ports G,H: Fluorescent display tube segments drive

2-12. External interrupt

The trailing edge of the signal on the $\overline{INT}$ pin is detected and the interrupt request flag in the status register is set. The occurrence of an interrupt is controlled by the enable/disable flag in the control register.

2-13. Standby

There are 2 standby modes: halt mode and hold mode. The halt mode is entered by means of program using the halt instruction. The hold mode is entered by setting the $\overline{HOLD}$ pin to ["L"] level. In the hold mode the power-down mode can be entered by reducing V_{DD}, which contributes a great deal to capacitor backup mode at the time of main power failure.

2-14. Reset

The system is initialized by setting the $\overline{RES}$ pin to ["L"] level. The contents to be initialized are as follows:

- PC — Address 000H
- Control register — 0000→Interrupt disable,Ports C,D: Output inhibit
- Status register — Timer,external interrupt flag → Reset
- Output port — Output latch (O_H) → Output transistor off

Appendix 3. Proper Cares in Using LSI

3-1. High Voltage input ports

High voltage input ports A_0 to 3, B_0 to 3 provide the input characteristic shown in Fig. 3-1. The pin input section contains a high voltage level converter. When the input level is high (V_{IH}), an "input current" of 1 to 2uA flows from the pin to the V_{SS} side through this converter. (Fig. 3-2)

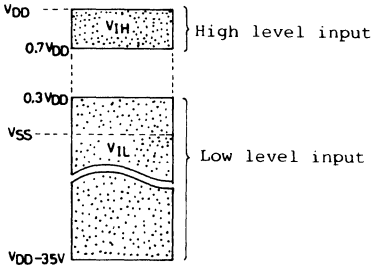


Fig. 3-1 Input level of ports A,B

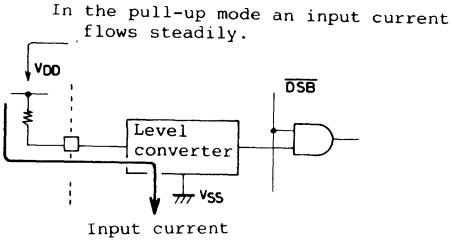
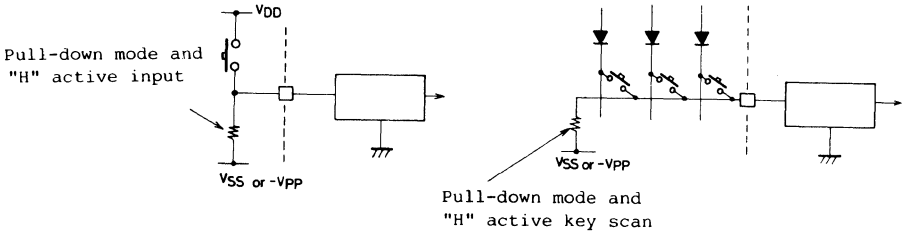


Fig. 3-2 Input current at port

When applying switch or key return signal to ports A,B in applications where capacitor or battery backup mode is entered at the time of power failure, such a circuit configuration as to cause no input current to flow must be used. Fig. 3-3 shows an example of the circuit configuration.



(a) SW input (b) Key scan input

Fig. 3-3 How to use ports A,B

3-2. Fluorescent display tube driver output

Ports E_0 to 3, F_0 to 3, I_0 to 1 (10 ports) are for high current digits driver outputs; and ports G_0 to 3, H_0 to 3 (8 ports) are for intermediate current segments driver outputs. Of course, digits driver outputs can be used as segments driver outputs. Fig. 3-4 shows a sample application.

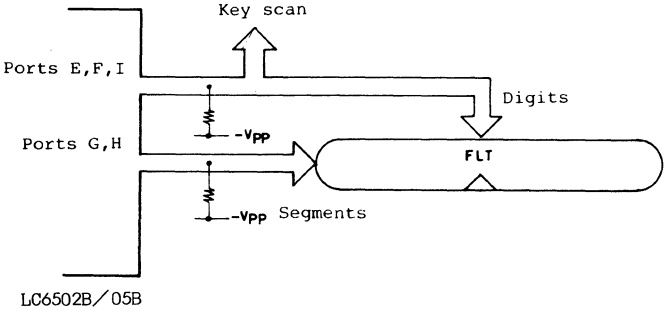


Fig. 3-4 FLT display application

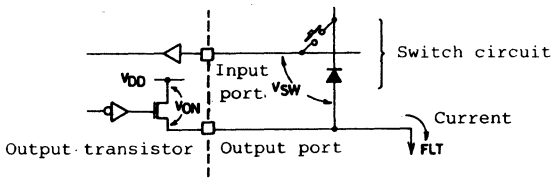
3-3. Key scan using digits drive signal

When applying the return signal to port A or port B by key scan using the FLT digits drive signal shown in Fig. 3-4, the following must be observed.

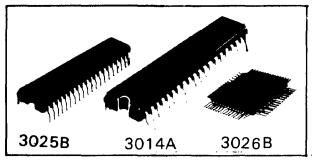
(a) From the current flowing through the FLT used and the V-I characteristic of the LC6502B/05B output port, estimate the voltage drop (V_{ON}) in the output transistor.

(b) Estimate the voltage drop (V_{SW}) in the switch circuit.

(c) judge if V_{ON} + V_{SW} meets V_{IH}/V_{IL} condition of the input port shown in Fig. 3-1; and use a driver for level return if necessary.



LC6502C, 6505C



C MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 970D

(Note) The LC6502C, 6505C heretofore in use have been changed partially in their design. Accordingly, the constant of their external part (external resistor for ceramic oscillation) has been changed as shown below. For applications to be made in and after July, 1984, the new constant must be used. For applications already made in and before June, 1984, the old constant is used.

Ceramic resonator	New constant	Old constant
CSB 400P (Murata)	2.2kΩ±5%	4.7kΩ±5%
KBR 400B (Kyocera)	4.7kΩ±5% (Unchanged)	4.7kΩ±5%

General Description

The LC6502C, 6505C, intended for use in commercial applications, are high-performance 4-bit microcomputers fabricated on single chips using CMOS process technology. They are provided with various features including low power dissipation and contain all the necessary functions, such as ALU, ROM, RAM, I/O ports, timer, cock generator, etc. in a single chip.

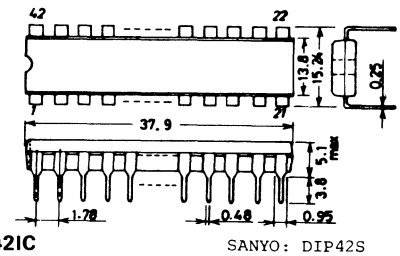
The instruction set of 80 instructions includes not only 4-bit arithmetic and logical·operation/manipulation instructions but also single-bit manipulation instructions, 8-bit table read instruction, various conditional branch instructions, etc. which are easy to use and powerful. With the hold function and halt function provided to stop the internal operation so that power dissipation can be minimized, they are suited for use in low-power applications such as battery-powered equipment.

(1) Hardware features

- Low power dissipation
- 5V single power supply
- 9-port/34-pin input/output
  - Input ports (2 ports/8 pins)
  - Input/output common ports (2 ports/8 pins)
  - Output ports (5 ports/18 pins)
- Clock generator (C, R or ceramic resonator attached externally)
- ROM capacity 1k bytes/2k bytes model pin compatible
- Initial reset ($\overline{RES}$) and external interrupt ($\overline{INT}$) and $\overline{HOLD}$ input pins containing Schmitt gate
- Hold control input to minimize power dissipation by stopping internal operation

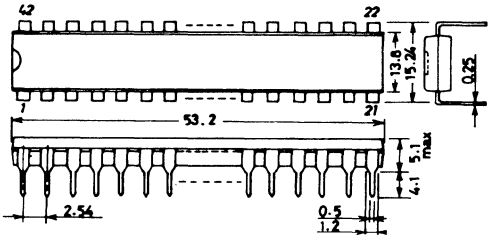
(continued on next page)

Case Outline 3025B-D42SIC
(unit: mm)



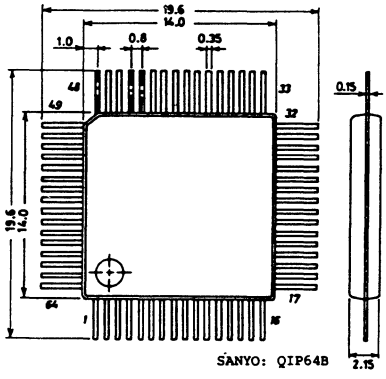
SANYO: DIP42S

Case Outline 3014A-D42IC
(unit: mm)



SANYO: DIP42

Case Outline 3026B-Q64BIC
(unit: mm)



SANYO: QIP64B

For details, refer to LC6500 Series User's Manual.

(2) Software features

- Powerful instruction set of 80 instructions
- ROM capacity 1k bytes/2k bytes model instruction compatible
- Halt function to minimize power dissipation by stopping internal operation with HALT instruction
- 4-level subroutine nesting
- Abundant flags, working registers and manipulation instructions

Flag	16 pcs.
Working register	8 pcs.
General-purpose register	1 pc.

- Interrupt function and test instruction

External interrupt	1
Internal (timer) interrupt	1

- Programmable timer (4-bit prescaler/8-bit timer)
- Basic instruction execution cycle 10μsec (clock oscillation frequency 400kHz)

(3) ROM, RAM capacity and package

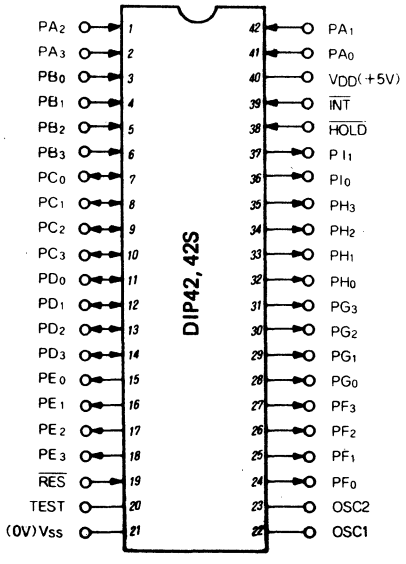
Type No.	ROM	RAM	Package	Package No.
LC6502C	2048 bytes	128 x 4 bits	DIP 42 DIP 42S DIP 64	No. 3014 No. 3025 No. 3026
LC6505C	1024 bytes	64 x 4 bits	DIP 42 DIP 42S DIP 64	No. 3014 No. 3025 No. 3026
LC65PG99	Externally attached 4096 bytes max	Built-in 192 x 4 bits max	QIC 42PG	(Note 1)
LC6599	Externally attached 4096 bytes max	Built-in 192 x 4 bits max	QIC 80	(Note 2)

(Notes 1) The LC65PG99 is a simulation chip for the LC6500 series.
(Notes 2) The LC6599 is an evaluation chip for the application development of the LC6500 series.

LC6502C/6505C Series Package/Pin Assignment

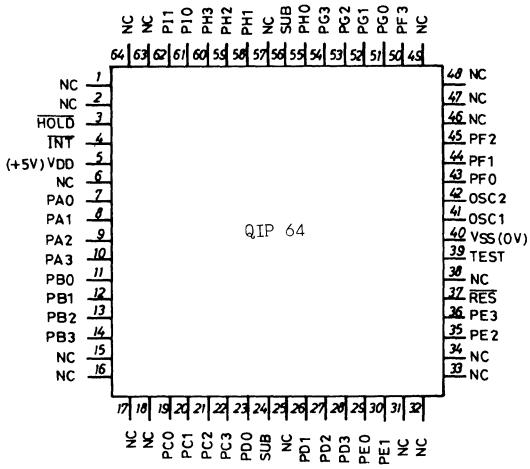
Pin name

OSC1, OSC2:	C, R or ceramic resonator for OSC
$\overline{INT}$:	Interrrupt
$\overline{RES}$:	Reset
$\overline{HOLD}$:	Hold
PA_{0-3}:	Input ports A_{0-3}
PB_{0-3}:	Input ports B_{0-3}
PC_{0-3}:	Input/output common ports C_{0-3}
PD_{0-3}:	Input/output common ports D_{0-3}
PE_{0-3}:	Output ports E_{0-3}
PF_{0-3}:	Output ports F_{0-3}
PG_{0-3}:	Output ports G_{0-3}
PH_{0-3}:	Output ports H_{0-3}
$PI_{0,1}$:	Output ports $I_{0,1}$
TEST:	Test



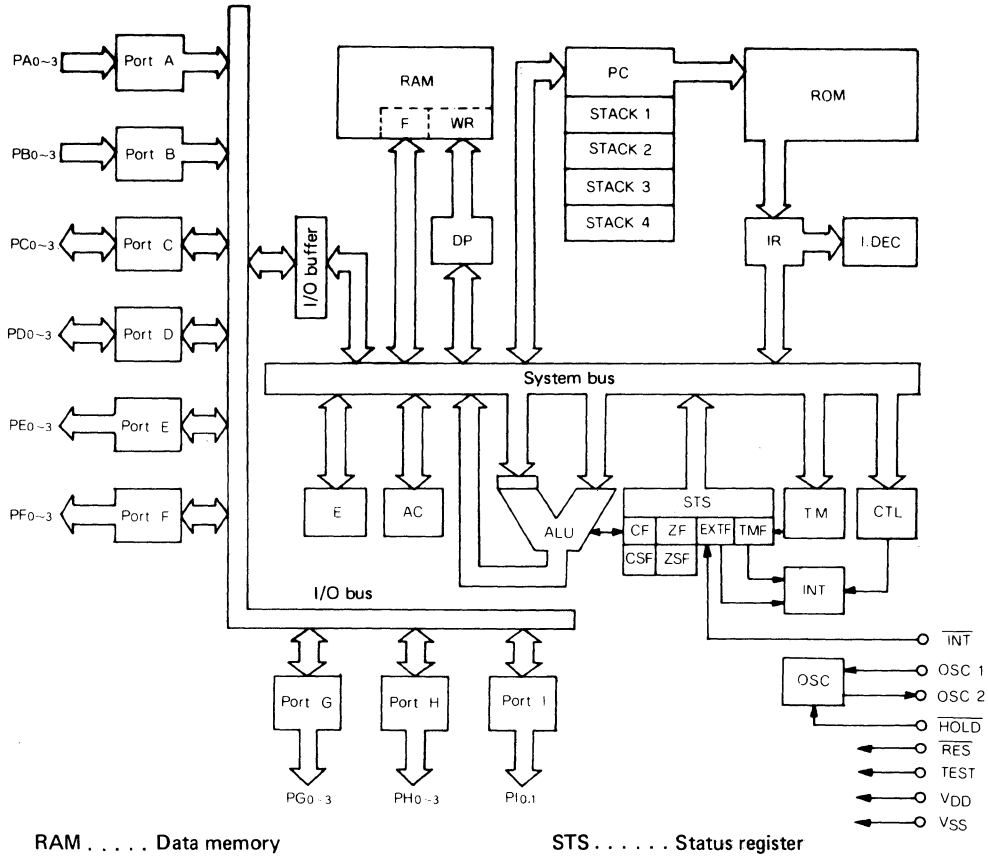
DIP 42, DIP 42S

Package (QIP64)



Note :
Do not use the NC pin, SUB pin unless otherwise instructed.

System Block Diagram (LC6502C, 6505C)



RAM . . . . . Data memory
F. . . . . Flag
WR . . . . . Working Register
AC . . . . . Accumulator
ALU . . . . . Arithmetic and logic unit
DP. . . . . Data pointer
E. . . . . E register
CTL. . . . . Control register
OSC. . . . . Oscillator
TM. . . . . Timer

STS . . . . . Status register
ROM . . . . . Program memory
PC. . . . . Program counter
INT . . . . . Interrupt control
IR . . . . . Instruction register
I.DEC. . . . . Instruction decoder
CF, CSF . . . Carry flag, carry save flag
ZF, ZSF . . . Zero flag, zero save flag
EXTF. . . . . External interrupt request flag
TMF. . . . . Internal interrupt request flag

Pin Description

Pin name	Input/ output	Function
$\overline{INT}$	Input	Interrupt request input pin
$\overline{HOLD}$	Input	Hold mode request input pin
$\overline{RES}$	Input	Reset input pin
PA_{0-3}	Input	Input ports A_0 to A_3 Capable of 4-bit input and single-bit decision for branch Used also for halt mode release request input
PB_{0-3}	Input	Input ports B_0 to B_3 Capable of 4-bit input and single-bit decision for branch
PC_{0-3}	Input/ output	Input/output common ports C_0 to C_3 Capable of 4-bit input and single-bit decision for branch during input Capable of 4-bit output and single-bit set/reset during output
PD_{0-3}	Input/ output	Input/output common ports D_0 to D_3 Capable of 4-bit input and single-bit decision for branch during input Capable of 4-bit output and single-bit set/reset during output
PE_{0-3}	Output	Output ports E_0 to E_3 Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
PF_{0-3}	Output	Output ports F_0 to F_3 Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
PG_{0-3}	Output	Output ports G_0 to F_3 Capable fo 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
PH_{0-3}	Output	Output ports H_0 to H_3 Capable of 4-bit output and single-bit set/reset Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch
$PI_{0,1}$	Output	Output ports I_0, I_1 Capable of 2-bit output and single-bit set/reset Capable of 2-bit input of output latch contents and single-bit decision of output latch for branch
OSC 1	Input	Pin for supplying external clock If internal clock oscillation is used, C, R or ceramic resonator are connected to this pin and pin OSC2.
OSC 2	Output	Pin for externally attaching oscillator for internal clock oscillation
V_{DD}	Input	Power supply pin Normally connected to +5V
V_{SS}	–	Connected to 0V power supply
TEST	Input	LSI test pin Normally connected to V_{SS} (0V)

ABSOLUTE MAXIMUM RATINGS/T_a=25°C, (V_{DD}=5V ±10% unless otherwise specified)

				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +7.0	V
Input Voltage	V_{IN}	Note 1	−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}		−0.3 to V_{DD}+0.3	V
Peak Output Current	I_{01}	Each pin of C to I ports	−2.0 to +2.0	mA
	I_{02}	All pins of C to I ports	−26 to +26	mA
Allowable Power Dissipation	P_d max	T_a=−30 to +70°C	350	mW
Operating Temperature	T_{opg}		−30 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Note 1: For OSC1 pin, up to oscillation amplitude generated when internally oscillated under the recommended oscillation conditions in Fig. 3 is allowable.

RECOMMENDED OPERATING CONDITIONS/T_a=−30 to +70°C, V_{SS}=0V

			min	typ	max	unit
Recommended Operating Supply Voltage	$V_{DD}(1)$		4.5	5.0	5.5	V
Power-down Supply Voltage	$V_{DD}(2)$	$\overline{HOLD}$=VIL(3)	2.0		5.5	V
"H" Level Input Voltage	$V_{IH}(1)$	Input pins other than $\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1	0.7V_{DD}		V_{DD}	V
	$V_{IH}(2)$	$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1 pins	0.75V_{DD}		V_{DD}	V
"L" Level INput Voltage	$V_{EL}(1)$	Input pins other than $\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$ OSC1	V_{SS}		0.3V_{DD}	V
	$V_{IL}(2)$	$\overline{INT}$, $\overline{RES}$, OSC1 pins	V_{SS}		0.25V_{DD}	V
	$V_{IL}(3)$	V_{DD}=2 to 5.5V, $\overline{HOLD}$ pins	V_{SS}		0.3V_{DD} −0.3	V
	$V_{IL}(4)$	TEST pin	V_{SS}		0.3V_{DD}	V
Operating Clock Frequency	$f_{ext\ osc}$	At external clock input, See Fig. 1	20		420	kHz
"H" Level Clock Pulse Width	$t_{W\phi H}$	"	0.5			μs
"L" Level Clock Pulse Width	$t_{W\phi L}$	"	0.5			μs
Clock Input Rise Time	t_{oscR}	"			0.2	μs
Clock Input Fall Time	t_{oscF}	"			0.2	μs
External Capacitance for CR Oscillation	C_{ext}	See Fig. 7	33	82	470	pF
External Resistance for CR Oscillation	R_{ext}	"	20	47	200	kΩ
External Capacitance for Ceramic Oscillation	C_1	See Fig. 3		100±10%		pF
	C_2	"		100±10%		pF
External Reistance for Ceramic Oscillation	R_1	"		1000±5%		kΩ
	R_2	" CSB400P (Murata)		4.7±5%		kΩ
		" KBR400B (Kyocera)		2.2±5%		kΩ
Power-down $\overline{HOLD}$ Setup Time	t_{HOLDS}	See Fig. 6	2			ms
Power-down $\overline{HOLD}$ Hold Time	t_{HOLDH}	"	50			μs

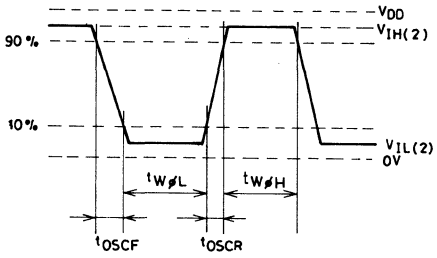
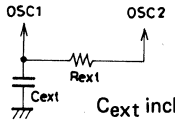
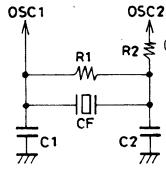


Fig. 1 OSC1 pin input waveform



C_{ext} includes wiring capacity.

Fig. 2 Recommended oscillator for CR oscillation

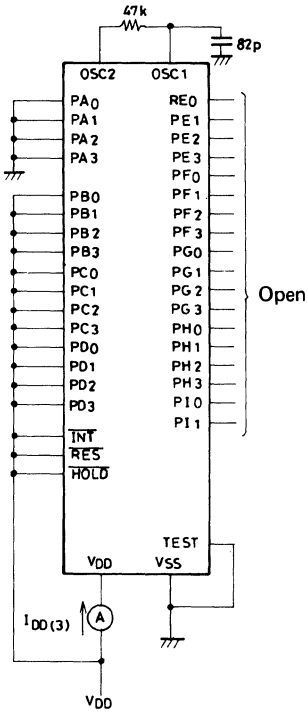


CF : Ceramic resonator

	R2
CSB400P (Murata)	2.2kΩ±5%
KBR400B (Kyocera)	4.7kΩ±5%

Fig. 3 Recommended oscillator for ceramic oscillation

ELECTRICAL CHARACTERISTICS/T_a=−30 to +70°C, V_{DD}=5V ±10%, V_{SS}=0V			min	typ	max	unit
"H" Level Input Current	I_{IH}	All input pins, $V_{IN}=V_{DD}$			1	μA
"L" Level Input Current	I_{IL}	All input pins, $V_{IN}=V_{SS}$	−1			μA
"H" Level Output Voltage	$V_{OH(1)}$	Output pins other than OSC2 I_{OH}=−1mA	V_{DD}-2			V
	$V_{OH(2)}$	Output pins other than OSC2 I_{OH}=−100μA	V_{DD}-0.5			V
"L" Level Output Voltage	V_{OL}	Output pins other than OSC2 I_{OL}=1mA			0.4	V
Output off Leak Current	$I_{OFF(1)}$	Output pins other than OSC2 $V_{OH}=V_{DD}$			1	μA
	$I_{OFF(2)}$	Output pins other than OSC2 $V_{OL}=V_{SS}$	−1			μA
Clock Oscillation Frequency for Ceramic Oscillation	f_{XOSC}	Recommended conditions for ceramic oscillation At oscillation circuit in Fig. 3	384	400	417	kHz
Clock Oscillation Frequency for CR Oscillation	f_{CROSC}	C_{ext}=82pF±5% R_{ext}=47kΩ±1% At oscillation circuit in Fig. 2	200	300	400	kHz
Current Dissipation	$I_{DD(1)}$	At CR oscillation C_{ext}=82pF R_{ext}=47kΩ Output pin open Input pin $V_{IN}=V_{DD}$		0.4	1.0	mA
	$I_{DD(2)}$	At ceramic oscillation Output pin open Input pin $V_{IN}=V_{DD}$		0.5	1.0	mA
	$I_{DD(3)}$	HALT mode V_{DD}=5V±10% At Test circuit in Fig. 4		0.5	10	μA
	$I_{DD(4)}$	HOLD Mode V_{DD}=5V±10% At test circuit in Fig. 5		0.5	10	μA
	$I_{DD(5)}$	HOLD mode power down V_{DD}=2V At test circuit in Fig. 5		0.1	2	μA
Input Capacitance	C_{IN}	f=200kHz		5		pF
Output Capacitance	C_{OUT}	f=200kHz, output high impedance		10		pF
Input/Output Capacitance	C_{IO}			10		pF



Input/output common ports C, D: Output inhibit
HALT instruction is executed to make HALT mode.

Fig. 4 $I_{DD(3)}$ test circuit

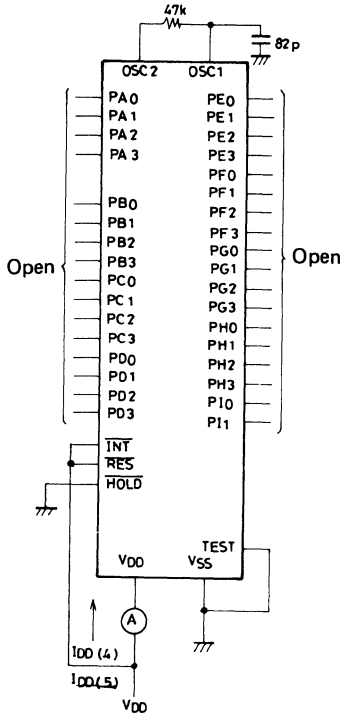


Fig. 5 $I_{DD(4)}$, $I_{DD(5)}$ test circuit

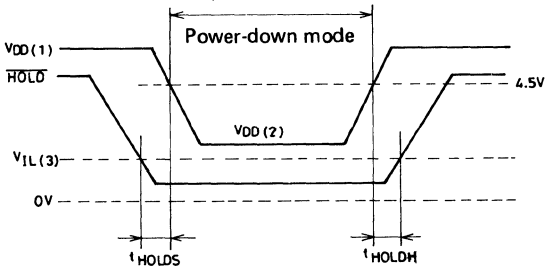


Fig. 6 Power-down mode timing

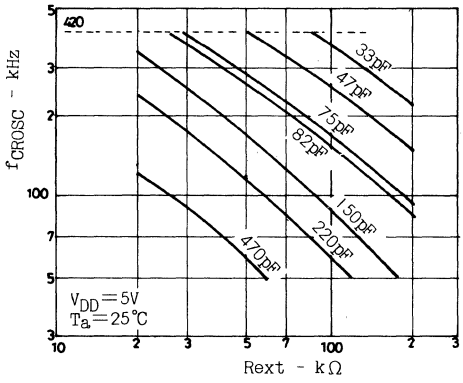
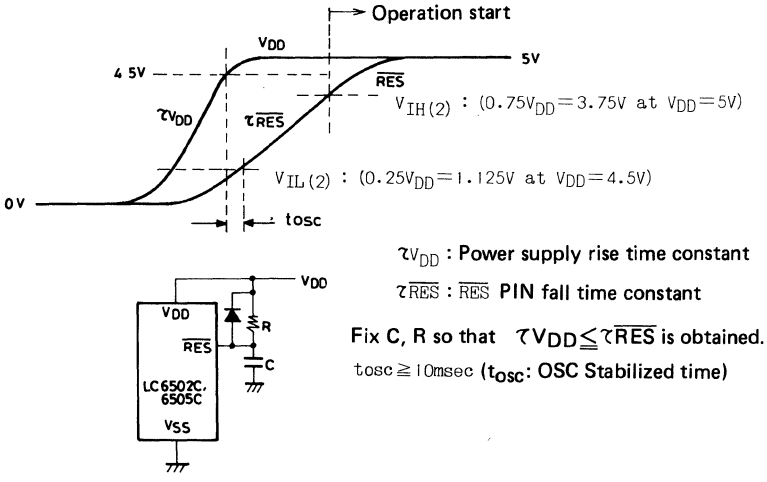


Fig. 7 CR oscillation frequency data (typical)



τV_{DD} : Power supply rise time constant

$\tau\overline{RES}$: $\overline{RES}$ PIN fall time constant

Fix C, R so that $\tau V_{DD} \leq \tau\overline{RES}$ is obtained.

tosc ≧ 10msec (t_{osc}: OSC Stabilized time)

Fig. 8 Initial reset timing

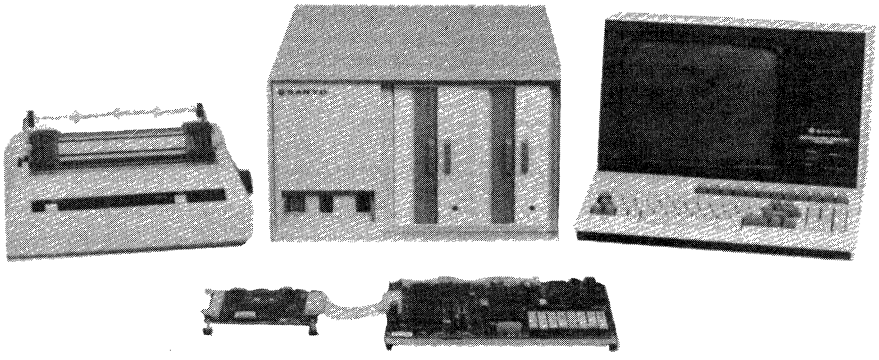
Application development tools

For convenience of application development of the LC6502C, LC6505C, the evaluation chip (LC6599), simulation chip (LC65PG99) and the specialized equipment called "application development tools" are available. For details, refer to "DEVELOPMENT TOOL MANUAL".

- SDS-410 system
  This is a combination of floppy disks-provided CPU, CRT, and printer. This system enables application development programs of microcomputers to be constructed (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled or data can be written into EPROM (using EPROM WRITER function contained in the EVA-410).

- EVA-410
  This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged. By replacing the target board, this kit can be used for application development of N channel microcomputer LM6400 series.

- EVA-402
  This is a board with an EPROM and the LC6599 combined. This board is used for mounting evaluation or trial production of sets after application development programs are completed.



LC6500 SERIES INSTRUCTION SET (BY FUNCTIONS)

Notations

AC	: Accumulator	M(DP)	: Memory addressed by DP	( ), [ ]	: Contents
ACt	: Accumulator bit t	P(DP_L)	: Input/output port addressed by DP_L	←	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
CTL	: Control register	STACK	: Stack register	−	: Subtraction
DP	: Data pointer	TM	: Timer	∧	: AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨	: Exclusive OR
EXTF	: External interrupt request flag	At, Ha, La	: Working register		
Fn	: Flag bit n	ZF	: Zero flag		
M	: Memory				

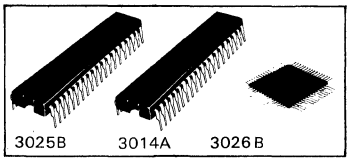
Instruction	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	✱1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), AC_{n+1} ← (AC_n), CF ← (AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇄ (E)	The AC contents and the E conents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] − 1	The M(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 1	A single bit of the M(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M(DP, B_1B_0) ← 0	A single bit of the M(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)]	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)] + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∨ [M(DP)]	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ [M(DP)]	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ [M(DP)]	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{[M(DP)]}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. Comparison result / CF / ZF [M(DP)] > (AC) / 0 / 0 [M(DP)] = (AC) / 1 / 1 [M(DP)] < (AC) / 1 / 0	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset. Comparison result / CF / ZF $I_3I_2I_1I_0$ > (AC) / 0 / 0 $I_3I_2I_1I_0$ = (AC) / 1 / 1 $I_3I_2I_1I_0$ < (AC) / 1 / 0	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 $I_3I_2I_1I_0$	2	2	(DP_L) ∨ $I_3I_2I_1I_0$	The DP_L contents and the immediate data $I_3I_2I_1I_0$ are compared.	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	✱1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← [M(DP)]	The M(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M then modify DP_H with immediate data	1 0 1 0	0 $M_2M_1M_0$	1	2	(AC) ⇄ [M(DP)] DP_H ← (DP_H) ∨ 0$M_2M_1M_0$	The AC contents and the M(DP) contents are exchanged and then the DP_H contents are modified with the contents of (DP_H) ∨ 0$M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of (DP_H) ∨ 0$M_2M_1M_0$.
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ⇄ [M(DP)]	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ⇄ [M(DP)] DP_L ← (DP_L) + 1	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP_L +1).
	XD	Exchange AC with M then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ⇄ [M(DP)] DP_L ← (DP_L) − 1	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are decremented −1.	ZF	The ZF is set/reset according to the result of (DP_L −1).
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		

Instruction	Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3 I_2 I_1 I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow I_3 I_2 I_1 I_0$	The DP_H is loaded with the immediate data $I_3 I_2 I_1 I_0$.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L)+1$	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L)-1$	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The AC contents are transferred to the DP_L		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	The DP_L contents are transferred to the AC	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	$(AC) \leftrightarrows (DP_H)$	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At	1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0	t_1 t_0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 0	1 1 1 1	1 1 1 1	$(AC) \leftrightarrows (A0)$ $(AC) \leftrightarrows (A1)$ $(AC) \leftrightarrows (A2)$ $(AC) \leftrightarrows (A3)$	The AC contents and the contents of working register At are exchanged. At is assigned one of A_0, A_1, A_2, A_3 according to $t_1 t_0$.		
	XHa XH0 XH1	Exchange DP_H with working register Ha	1 1 1 1 1 1 1 1	a 1 0 0 0 1 1 0 0	1 1	1 1	$(DP_H) \leftrightarrows (H0)$ $(DP_H) \leftrightarrows (H1)$	The DP_H contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.		
	XLa XL0 XL1	Exchange DP_L with working register La	1 1 1 1 1 1 1 1	a 0 0 0 0 0 1 0 0	1 1	1 1	$(DP_L) \leftrightarrows (L0)$ $(DP_L) \leftrightarrows (L1)$	The DP_L contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a.		
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 1$	The flag specified with $B_3 B_2 B_1 B_0$ is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3 B_2 B_1 B_0$	1	1	$Fn \leftarrow 0$	The flag specified with $B_3 B_2 B_1 B_0$ is reset.	ZF	The flags are divided into 4 groups of F_0 to F_3, F_4 to F_7, F_8 to F_{11}, F_{12} to F_{15}. The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data $B_3 B_2 B_1 B_0$.
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$PC \leftarrow PC_{11}(\cancel{X}\ \text{if}\ \overline{PC_{11}})$ $P_{10} P_9 P_8 P_7 P_6 P_5$ $P_4 P_3 P_2 P_1 P_0$	A jump to the address specified with the PC_{11} (or $\overline{PC_{11}}$) and immediate data $P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ occurs.		If the BANK and JMP instructions are executed consecutively, $PC_{11} \longrightarrow \overline{PC_{11}}$.
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	$PC_{7\sim0} \leftarrow (E, AC)$	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3 P_2 P_1 P_0$	1	1	$STACK \leftarrow (PC)+1$ $PC_{11\sim6}, PC_{1\sim0} \leftarrow 0$ $PC_{5\sim2} \leftarrow P_3 P_2 P_1 P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7 P_6 P_5 P_4$	1 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	$STACK \leftarrow (PC)+2$ $PC_{11\sim0} \leftarrow 0 P_{10} P_9 P_8 P_7$ $P_6 P_5 P_4 P_3 P_2 P_1 P_0$	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$ $CF\ ZF \leftarrow CSF, ZSF$	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	$PC_{11} \leftarrow (\overline{PC_{11}})$	The bank is changed.		Effective only when used immediately before the JMP instruction.
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $ACt=1$	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $ACt=0$	If a single bit of the AC specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(M(DP, t_1 t_0))=1$	If a single bit of the M(DP) specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 1 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(M(DP, t_1 t_0))=0$	If a single bit of the M(DP) specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(P(DP_L\ t_1 t_0))=1$	If a single bit of port $P(DP_L)$ specified with the immediate data $t_1 t_0$ is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7 P_6 P_5 P_4$	1 0 $t_1 t_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $(P(DP_L, t_1 t_0))=0$	If a single bit of port $P(DP_L)$ specified with the immediate data $t_1 t_0$ is 0, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $TMF=1$ then $TMF \leftarrow 0$	If the TMF is 1, a branch to the address specified with the immediate data $P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ within the same page occurs. The TMF is reset.	TMF	

Instruction	Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Branch instructions	BNTM addr	Branch on no timer	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \sim P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if Fn = 1	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 $P_7 P_6 P_5 P_4$	$n_3 n_2 n_1 n_0$ $P_3 P_2 P_1 P_0$	2	2	$PC_{7\sim0} \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$ if Fn = 0	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← (P(DP$_L$))	Port P(DP$_L$) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP$_L$) ← (AC)	The AC contents are outputted to port P(DP$_L$).		
	SPB bit	Set port bit	0 0 0 0	0 1 $B_1 B_0$	1	2	P(DP$_L$, $B_1 B_0$) ← 1	A single bit in port P(DP$_L$) specified with the immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 $B_1 B_0$	1	2	P(DP$_L$, $B_1 B_0$) ← 0	A single bit in port P(DP$_L$) specified with the immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 $B_3 B_2 B_1 B_0$	2	2	CTL ← (CTL) V $B_3 B_2 B_1 B_0$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 $B_3 B_2 B_1 B_0$	2	2	CTL ← (CTL) ∧ $\overline{B_3 B_2 B_1 B_0}$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		Only when all pins of port PA are set at L, stop.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used continuously in such a manner as CLA, CLA, ——, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

LC6502D, 6505D



C MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1563

General Description

The LC6502D/6505D are microcomputers that are identical with the standard type LC6502C/6505C in the internal architecture, instruction set and contain an FLT driver. They are modified versions of the LC6502B/6505B (microcomputers containing an FLT driver) and have low-threshold input ports for dynamic scan return signal input of key switch matrix.

Features

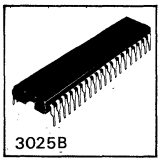
. CMOS single-chip microcomputer dissipating less power.
. Instruction set with 79 instructions common to the LC6502C/6502B, 6505C/6505B.
. 2-source, 2-level interrupt function (external interrupt/internal timer interrupt)
. 4-level stack.
. On-chip 8-bit programmable timer with 4-bit prescaler.
. Output ports with FLT driver and low-threshold input ports.
  (1) Output ports for digit drive: 10 pcs.
  (2) Output ports for segment drive: 8 pcs.
  (3) Output ports of normal breakdown voltage: 8pcs. (4 pcs.: Low-threshold input ports)
  (4) Input/output ports of normal breakdown voltage: 8 pcs.
. ROM, RAM
  (1) LC6502D ROM: 2048 bytes, RAM: 128 x 4 bits
  (2) LC6505D ROM: 1024 bytes, RAM: 64 x 4 bits

Differences between LC6502B/6505B and LC6502D/6505D

	LC6502B/6505B	LC6502D/6505D
FLT digit driving capability	$V_{OH}=V_{DD}-2.5V$ at $I_{OH}=-10mA$	$V_{OH}=V_{DD}-2.0V$ at $I_{OH}=-10mA$
Port A input conditions	$V_{IH}=0.7V_{DD}$ to V_{DD} $V_{IL}=V_{DD}-35V$ to $0.3V_{DD}$	$V_{IH}=1.7V$ to V_{DD} (Low threshold input) $V_{IL}=V_{SS}$ to $0.4V$
Ports A, B breakdown voltage	$V_{DD}-35V$ High breakdown voltage	Normal breakdown voltage

. Package: DIP42, DIP42S, QIP64

LC6510C



C MOS LSI

Single-Chip 4-Bit Microcomputer for Use in Control-Oriented Applications

Ⓔ 1565

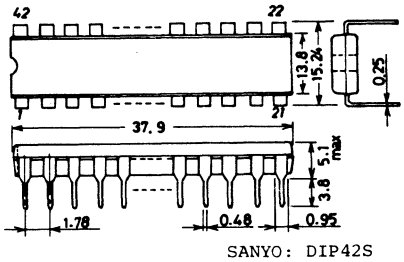
General Description

The LC6510C is a high-end model belonging to the single-chip 4-bit microcomputer LC6500 series fabricated using CMOS process technology. It contains a ROM (4096 x 8 bits), RAM (256 x 4 bits) and is especially suited for use in large-scale control-oriented applications.

Features

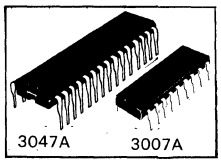
- Low power dissipation
- Program ROM capacity : 4096 x 8 bits
- Data RAM capacity : 256 x 4 bits
- Subroutine stack : 8 levels (also used for interrupt)
- Power-down by 2 standby functions
  - HALT mode : Power dissipation saving by program standby during normal operation.
  - HOLD mode : Power supply backup during power failure
- Input/output ports
  - Input : 4 bits x 2 ports
  - Input/output : 4 bits x 2 ports
  - Output : 4 bits x 4 ports
    2 bits x 1 port
- Interrupt
  External 1, Internal timer interrupt 1
- 4-bit prescaler and 8-bit program timer
- Instruction cycle time 4us(min.)
  - Normal operation 4.0 to 6.0V
  - Memory hold 1.8 to 6.0V
- Instruction set common to the LC6502, LC6505 (Program BANK instruction added)
- 42-pin shrink DIP

Case Outline 3025B-D42SIC
(unit:mm)



SANYO: DIP42S

LC6523, 6526, 6527



C MOS LSI

Single-Chip 4-Bit Microcomputer for Small-Scale Control-Oriented Applications

Ⓔ 1568

Preliminary

The LC6520 series belong to our single-chip 4-bit microcomputer LC6500 series fabricated using CMOS process technology and are suited for use in small-scale control-oriented applications.
Their basic architecture and instruction set are the same as for the LC6500 series. Two selections of pin assignment are available : 18 pins and 30 pins whose application areas are as follows :

18 pins : Circuit so far formed with standard logics and applications where the number of controls is small.
30 pins : Audio equipment (deck, player, etc.), office equipment, communications equipment, car equipment, home applicances.

Features

1) CMOS technology for low-power operation
2) ROM/RAM

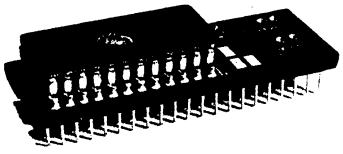
30-pin types	LC6523	ROM: 2k x 8 bits	RAM: 128 x 4 bits
	LC6526	ROM: 1k x 8 bits	RAM: 64 x 4 bits
18-pin types	LC6527	ROM: 1k x 8 bits	RAM: 64 x 4 bits

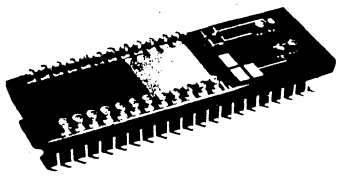
3) Instruction set
   30-pin version : 79 instructions
   18-pin version : 51 instructions
4) Wide operating voltge range from 2.5V to 6.5V (target)
5) Wide instruction cycle time from 3usec. (target) to 400usec.
6) Serial I/O port contained in 30-pin version
7) Flexible I/O ports
   . Number of ports
     30-pin version: 25, 18-pin version: 13
   . All ports
     Input/output common
     Input/common breakdown voltage: 15V (open drain)
     Output current: 10mA (sink current)
   . Option selectable for your intended system
     (A) Open drain output, pull-up resistor: Single-bit select for all ports
     (B) Output level at reset mode: 4-bit select of H/L level for port C/D respectively.
8) Interrupt function
   30-pin version: Vectored interrupt by timer overflow (instruction-testable)
   Vectored interrupt by INT pin or completion of transmit/receive at serial I/O port (instruction-testable)
   18-pin version: Flag set by timer overflow (instruction-testable)
9) Stack level: 4 levels
10) Timer: 4-bit prescaler + 8-bit programmable timer.
11) Clock oscillation option selectable for your intended system
   . Oscillator option: 1 pin C oscillation (with R), 1 pin External clock input, 2 pins CR oscillation.
   . Divider option: No divider, 1/3 divider, 1/4 divider.

LC65PG99

System Evaluation Chip for LC6500 Series

Ⓔ 1247A





1. General Description

The LC65PG99 is a simulation chip intended for use in evaluating C MOS 4-bit single-chip microcomputer LC6500 series.

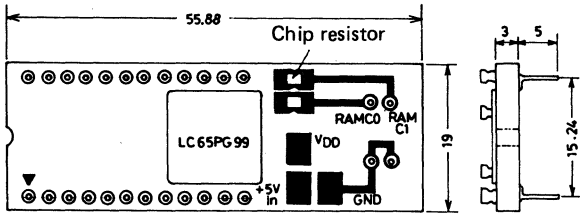
With a 24-pin socket for program EPROM provided on the package surface, it is designed to facilitate the development of the hardware and software for applications based on the LC6500 series microcomputers. Thus, it is ideally suited for use in prototype systems.

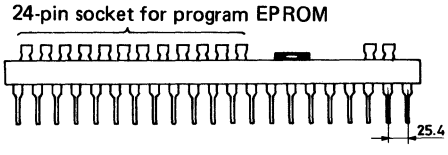
2. Features

- 2K-byte EPROM (equivalent to Intel 2716) or 4K-byte EPROM (equivalent to TI 2532) is usable.
- Built-in RAM capacity can be set according to RAM capacity of each Type No. of the LC6500 series.
- Pin compatible with the LC6500 series.
- Software compatible with the LC6500 series.
- Instruction cycle time: 10μsec.
- +5V single power supply.
- Capable of being externally supplied with power to EPROM.

Note: The LC65PG99 is designed for application development of the LC6500 series microcomputers. It should be noted that it is not suited for use under high-temperature, high-humidity conditions.

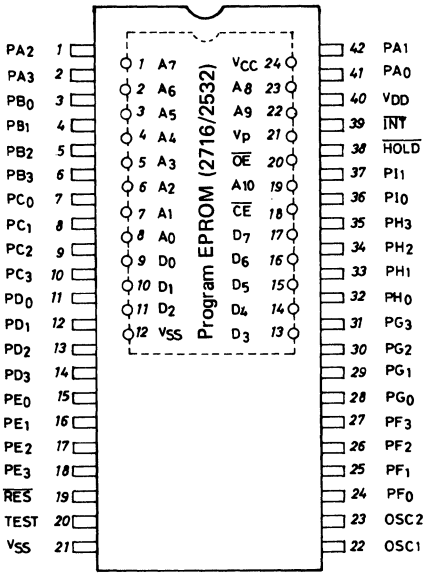
Case Outline 3040
(unit: mm)





For evaluation of 42-pin shrink package microcomputers, use the board for conversion from DIP-42 to DIP-42S.

3. Pin Assignment



OSC1, OSC2	:	Ceramic resonator, CR for OSC	
$\overline{INT}$	:	Interrupt	
$\overline{HOLD}$	:	Hold	
$\overline{RES}$	:	Reset	
$PA_{0\sim3}$	:	Input ports	$A_{0\sim3}$
$PB_{0\sim3}$	:	Input ports	$B_{0\sim3}$
$PC_{0\sim3}$	:	Input/output ports	$C_{0\sim3}$
$PD_{0\sim3}$	:	Input/output ports	$D_{0\sim3}$
$PE_{0\sim3}$	:	Output ports	$E_{0\sim3}$
$PF_{0\sim3}$	:	Output ports	$F_{0\sim3}$
$PG_{0\sim3}$	:	Output ports	$G_{0\sim3}$
$PH_{0\sim3}$	:	Output ports	$H_{0\sim3}$
$PI_{0,1}$	:	Output ports	$I_{0,1}$
TEST	:	Test	

5. Table of LC6500 Series

Type No.	Application	ROM	RAM	Cycle time	I_{DD} (typ)	Package	Remarks
LC6502C	General	2K bytes	128x4bits	10μs	0.5mA	DIP-42(S) QIP-64	
LC6505C	"	1K bytes	64x4 bits	"	"	"	
LC6502B	High breakdown voltage	2K bytes	128x4 bits	"	"	"	Built-in fluorescent display tube driver
LC6505B	"	1K bytes	64x4 bits	"	"	"	"
LC6599	LC6502/05 system development	External 4K bytes max.	192x4 bits max. (variable)	10μs	0.5mA	QIP-80	Evaluation chip
LC65PG99	LC6502/05 system evaluation	External 4K bytes max.	192x4 bits max. (variable)	"	50mA*	QIP-42PG	Simulation chip

* Including EPROM

6. How to Use

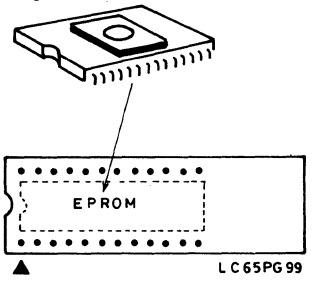
Since the LC65PG99 is capable of evaluating all Type Nos. of the LC6500 series, it is necessary to set the functions before evaluation as follows:

1. Selection of program EPROM. For Type Nos. having ROM capacity up to 2K bytes, use the 2716.
   For Type Nos. having ROM capacity exceeding 2K bytes, use the 2532.
2. Write data into the EPROM and mount it on the LC65PG99.
3. Set the built-in RAM capacity according to the RAM capacity of a Type No. to be evaluated.
4. For power supply to the EPROM, select the same power supply as for the LC65PG99 or an external power supply.

6-1. EPROM mounting

Write data into the program EPROM (2716 or 2532) and mount it. For writing into the EPROM, use the EPROM write function of the EVA-410.

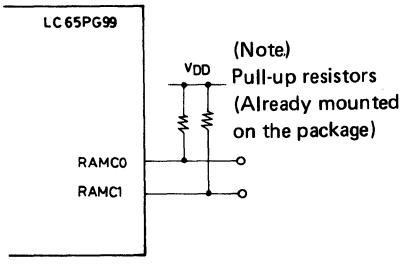
Program EPROM (2716 or 2532)



Location of pin No. 1 of LC65PG99

6-2. RAM capacity setting

Set the built-in RAM capacity (192 words max.) according to the RAM capacity of a Type No. to be evaluated. Pins (RAMC0, RAMC1) to control the RAM capacity are provided on the package surface of the LC65PG99. At the time of shipment both pins are set at "H" level with pull-up resistors as shown below. By setting these pins as shown in the Table below, the built-in RAM capacity can be changed.



(RAM capacity control pins at the time of shipment)

Built-in RAM Capacity Setting

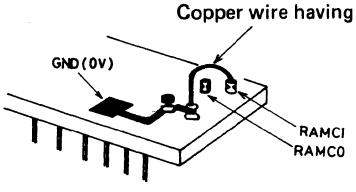
RAM capacity (Words)	RAMC1	RAMC0	Applicable Type No.
32	H	H	-
64	H	L	LC6505
128	L	H	LC6502
192	L	L	

H: V_{DD} level (+5V)
L: 0V

Note. V_{DD} for pull-up resistors is connected to the power supply pin of the EPROM. If power supply to the EPROM is provided externally as shown in 6-3 (2), V_{DD} for these pull-up resistors is also provided externally.

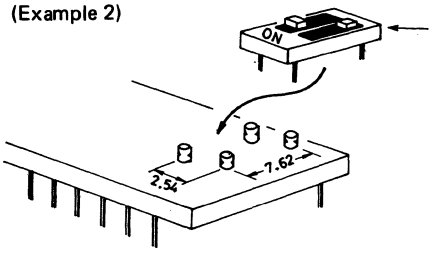
Shown below is how to set.

(Example 1)



In this example, RAMC1 pin is connected to GND (L level) and RAMC0 is open. That is, the RAM capacity is set to 128 words. (For evaluation of the LC6502)

(Example 2)

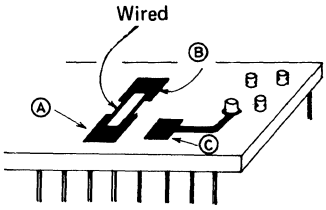


As shown left, a commercially available DIP switch can be mounted. In this example, RAMC0 side is placed in ON position and the RAM capacity is set to 64 words. (For evaluation of the LC6505)

6-3. Selection of power supply to EPROM (External power supply)

Normally, an EPROM dissipates a current of 50 to 100mA. If the power capacity of a user system is not enough, an external power supply can be used as shown in (2) below.

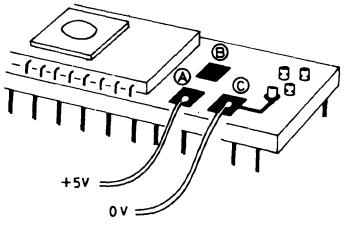
(1) The same power supply as to the LC65PG99 is used at the time of shipment.
A jumper for EPROM power supply select is provided on the package surface of the LC65PG99. At the time of shipment the power supply to the EPROM is connected to the power supply pin (V_{DD} pin) of the LC65PG99 as shown below.



Ⓐ Connected to power supply pin of EPROM
Ⓑ Connected to power supply pin of LC65PG99
Ⓒ Connected to GND (0V) pin

(At the time of shipment the same power supply is used for the LC65PG99 and the EPROM.)

(2) How to provide external power supply to EPROM
1. Remove the wiring connecting patterns (A) and (B).
2. Connect external power supply (+5V) to pattern (A) and external power supply (0V) to pattern (C) (GND pin).
3. In this case, V_{DD} for pull-up resistors at RAMC0, RAMC1 pins is also supplied from the external power supply.



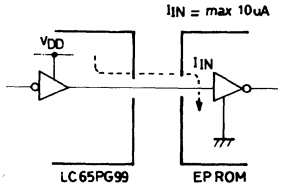
Power supply to EPROM
(External power supply to EPROM)

Note
The LC65PG99 is an LSI of CMOS structure. If a voltage lower than V_{SS} and higher than V_{DD} is applied to the input pin or output pin, a phenomenon called "latchup" peculiar to CMOS IC occurs, thereby causing breakdown or deterioration of the device.
Be careful of the supply voltage relation between the LC65PG99 and the EPROM. When applying two powers, (1) turn ON power for the LC65PG99 and then (2) turn ON power for the EPROM. When turning OFF power, reverse these steps.

6-4 Evaluation of current dissipation at standby mode

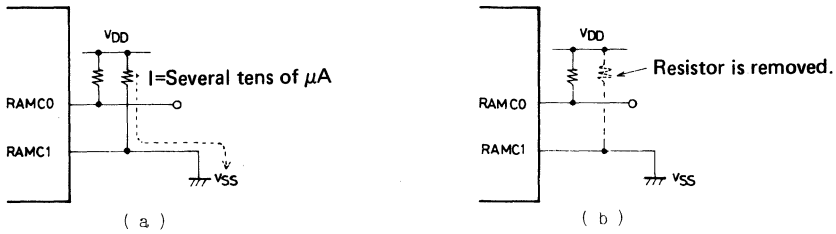
It is impossible to completely evaluate the current dissipation of the LC65PG99 at the standby mode (including transient mode) in such a case as a capacitor or battery is used as standby power source. However, by eliminating the current dissipation taken by the interface to the EPROM as described below, the steady-state current dissipation of the LC65PG99 alone can be evaluated.

(1) Elimination of the current dissipation taken by the interface to the EPROM
As shown right, the interface to the EPROM dissipates current. By removing the EPROM at the standby mode (HOLD, HALT mode), the current dissipation can be eliminated.



(A_0 to A_{10} pins)

(2) Elimination of current flowing through pull-up resistors at RAM capacity control pins (RAMC0, RAMC1)
As shown in Fig. (a), if the RAM capacity is set to 64, 128, 192 words, pull-up resistors dissipate several tens of μA. In this case, by removing a pull-up resistor, the current dissipation can be reduced.



Example of setting RAM capacity to 128 words

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V			unit	Remarks
Supply Voltage	V_{DD} max	−0.3 to +7	V	
Input Voltage	V_{IN}	−0.3 to V_{DD}+0.3	V	Note 1
Output Voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V	
Peak Output Current	$I_{O(1)}$	−2.0 to +2.0	mA	Each pin of C to I ports
	$I_{O(2)}$	−26 to +26	mA	All pins of C to I ports
	$I_{O(3)}$	−0.2 to +0.2	mA	Each pin of A_0 to A_{10} And CE
	$I_{O(4)}$	− 2.4 to +2.4	mA	All pins of A_0 to A_{10} and CE
Power Dissipation	P_d max $T_a \leqq 40$°C	350	mW	
Operating Temperature	T_{opg}	+10 to +40	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note 1: For OSC1 pin, up to oscillation amplitude is allowable which appears when causing internal oscillation under the recommended conditions at the recommended circuits in Fig. 2 and Fig. 3.

Allowable Operating Conditions/T_a=25°C, V_{SS}=0V			min	typ	max	unit	Remarks
Supply voltage	$V_{DD(1)}$		4.5	5.0	5.5	V	
Power-down Supply Voltage	$V_{DD(2)}$	$\overline{HOLD}$=$V_{IL(3)}$	2.0		5.5	V	At HOLD mode
"H" Level Input Voltage	$V_{IH(1)}$	V_{DD}=5V±10%	0.7V_{DD}		V_{DD}	V	Input pins other than $\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1 (Note 2)
	$V_{IH(2)}$	V_{DD}=5V±10%	0.75V_{DD}		V_{DD}	V	$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1 pins
"L" Level Input Voltage	$V_{IL(1)}$	V_{DD}=5V±10%	V_{SS}		0.3V_{DD}	V	Input pins other than $\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1
	$V_{IL(2)}$	V_{DD}=5V±10%	V_{SS}		0.25V_{DD}	V	$\overline{INT}$, $\overline{RES}$, OSC1 pins
	$V_{IL(3)}$	V_{DD}=2 to 5.5V	V_{SS}		0.3V_{DD} −0.3	V	$\overline{HOLD}$ pin
	$V_{IL(4)}$	V_{DD}=5V±10%	V_{SS}		0.3V_{DD}	V	TEST pin
Operating Clock Frequency	f_{extosc}	For external clock V_{DD}=5V±10%	20		420	kHz	Input at OSC1 pin Refer to Fig. 1.
"H" Level Clock Pulse Width	$t_{w\phi H}$	"	0.5			μs	"
"L" Level Clock Pulse Width	$t_{w\phi L}$	"	0.5			μs	"
Clock Input Rise Time	t_{oscR}	"			0.2	μs	"
Clock Input Fall Time	t_{oscF}	"			0.2	μs	"

(Continued on next page)

			min	typ	max	unit	
External Capacitor Value for CR Oscillation	C_{ext}		33		470	pF	Refer to Fig. 2 and 5
External Resistance Value for CR Oscillation	R_{ext}		20		220	kΩ	"
External Capacitance Value for Ceramic Oscillation	C1	CSB400P	33±10%			pF	Refer to Fig. 3
		KBR400B	33±10%			pF	"
	C2	CSB400P	33±10%			pF	"
		KBR400B	33±10%			pF	"
External Resistance Value for Ceramic Oscillation	R1		4700±5%			kΩ	"
	R2		3.9±5%			kΩ	"
Power-down $\overline{HOLD}$ Setup Time	t_{HOLDS}		2			ms	Refer to Fig. 4.
Power-down $\overline{HOLD}$ hold time	t_{HOLDH}		50			μs	"

Note 2: TEST pin is for LSI test only. It is not included in "input pin" unless otherwise specified.

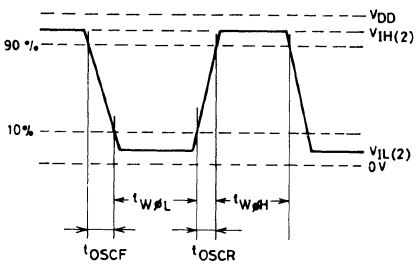


Fig. 1 Input waveform at OSC1 pin

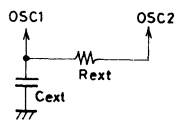


Fig. 2 Recommended oscillator for CR oscillation

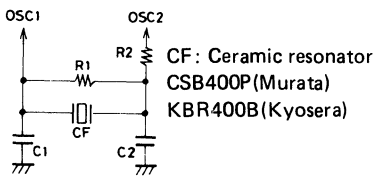


Fig. 3 Recommended oscillator for ceramic oscillation

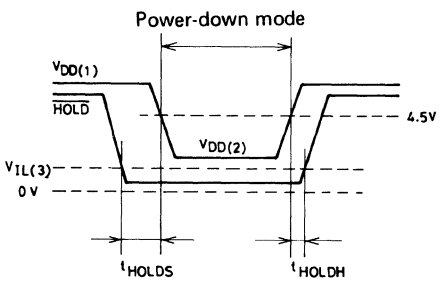
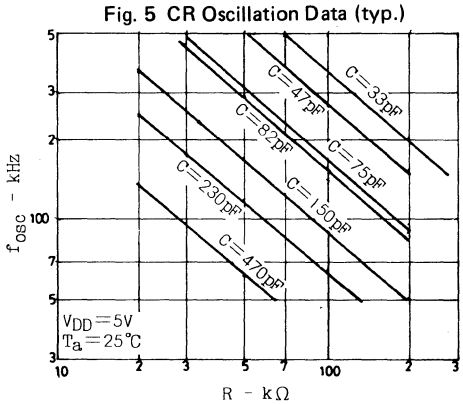


Fig. 4 Power-down MODE Timing

Fig. 5 CR Oscillation Data (typ.)



Electrical Characteristics/T_a=25°C, V_{DD}=5V±10%, V_{SS}=0V			min	typ	max	unit	Remarks
"H" Level Input Current	I_{IH}	$V_{IN}=V_{DD}$			1	μA	Each input pin
"L" Level Input Current	I_{IL}	$V_{IN}=V_{SS}$	−1			μA	"
"H" Level Output Voltage	$V_{OH(1)}$	I_{OH}=−1mA	V_{DD}−2			V	Output pins other than OSC2, A_0 to A_{10} and $\overline{CE}$
	$V_{OH(2)}$	I_{OH}=−100μA	V_{DD}−0.5			V	"
	$V_{OH(3)}$	I_{OH}=−100μA	V_{DD}−2			V	A_0 to A10 and $\overline{CE}$ pins
"L" Level Output Voltage	$V_{OL(1)}$	I_{OL}=1mA			0.4	V	Output pins other than OSC2, A_0 to A_{10} and $\overline{CE}$
	$V_{OL(2)}$	I_{OL}=100μA		0.4		V	A_0 to A_{10} and $\overline{CE}$ pins
Output OFF Leak Current	$I_{OFF(1)}$	$V_{OUT}=V_{DD}$			1	μA	Output pins toher than OSC2, A_0 to A_{10} and $\overline{CE}$
	$I_{OFF(2)}$	$V_{OUT}=V_{SS}$	−1			μA	"
Clock Oscillation Frequency for Ceramic Oscillation	f_{xosc}	Recommended conditions for ceramic oscillation	384	400	417	kHz	Oscillator in Fig. 3
Clock Oscillation Frequency for CR Oscillation	f_{CRosc}	Cext=33pF±5% Rext=100kΩ±1%	200	300	400	kHz	Oscillator in Fig. 2
Current Dissipation	$I_{DD(1)}$	Cext=33pF Rext=100kΩ Output pin open Input pin $V_{IN}=V_{DD}$		0.4	1.0	mA	At CR oscillation Refer to Fig. 2
	$I_{DD(2)}$	Recommended condition for ceramic oscillation Output pin open Input pin $V_{IN}=V_{DD}$		0.5	1.0	mA	At ceramic oscillation Refer to Fig. 3
	$I_{DD(3)}$	V_{DD}=5V±10% Test circuit in Fig. 4		0.5	10	μA	At HALT mode Refer to Fig. 6
	$I_{DD(4)}$	V_{DD}=5V±10% Test circuit in Fig. 5		0.5	10	μA	At HOLD mode Refer to Fig. 7
	$I_{DD(5)}$	V_{DD}=2V Test circuit in Fig. 5		0.1	2	μA	HOLD mode power-down Refer to Fig. 7
Input Capacitance	C_{IN}	f=200kHz		5		pF	Other than D_0 to D_7, A_0 to A_{10} and $\overline{CE}$ pins
Output Capacitance	C_{OUT}	f=200kHz Output high impedance		10		pF	"
Input/Output Capacitance	C_{IO}	"		10		pF	"

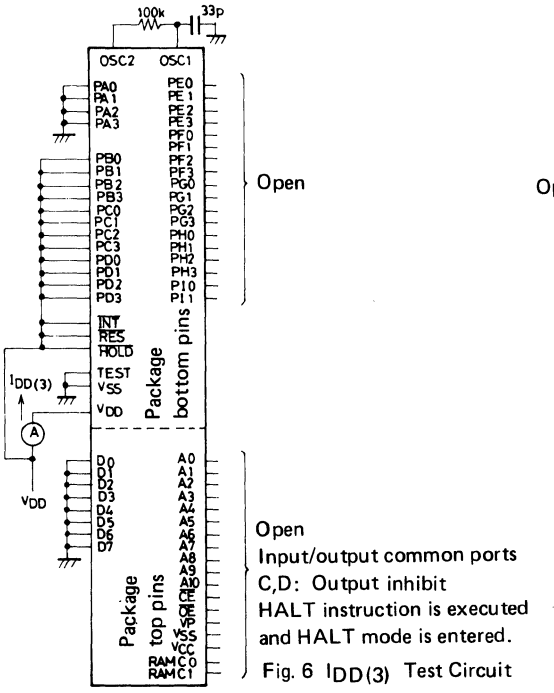


Fig. 6 $I_{DD(3)}$ Test Circuit

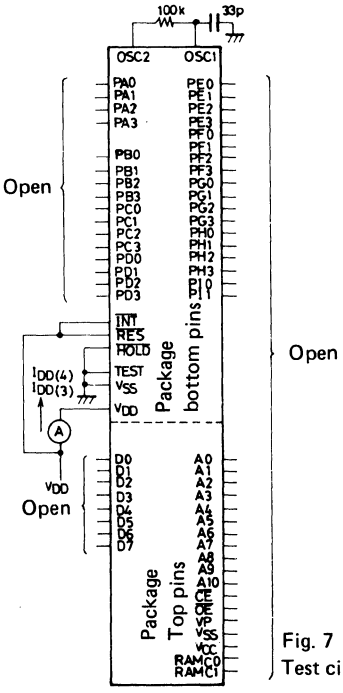
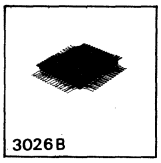


Fig. 7 $I_{DD(4)}$, $I_{DD(5)}$ Test circuit

LC5700N



C MOS LSI

Single-Chip 4-Bit Microcomputer (with LCD Driver)

Ⓔ 1498

The LC5700N is a C-MOS 4-bit microcomputer containing an LCD driver that operates on low voltage, very small current. It contains a 4-bit parallel processing arithmetic and logic unit(ALU), a program memory ROM, many LCD segment outputs, a prescaler, and a 32,768KHz crystal oscillator. It is ideally suited for use in game watch/clock applications.

Features

(1)	Instruction set	71
(2)	ROM	1,392 x 14 bits
(3)	RAM	84 x 4 bits
(4)	8-level subroutine nesting (Also used for interrupt)	
(5)	Internal timer interrupt	
(6)	Output for display	· 1/2 duty, 1/2 bias LCD drive output · Number of drivable segments: 98 segments(49x2) · Outputs exchangeable for each other by mask option
(7)	Number of key inputs (Input ports)	8 (S port, M port: 4 each)
(8)	Control output	ALARM1 OUT, ALARM2 OUT, LIGHT OUT
(9)	Oscillation frequency	32,768KHz
(10)	Ag battery (operation from 1.5V)/Li battery (operation from 3.0V) selectable (mask option)	
(11)	Built-in step-up circuit (operation from 1.5V) or step-down circuit (operation from 3.0V)	
(12)	Current dissipation	2.0uA/typ. (Ag battery); 1.0uA/typ. (Li battery)
(13)	Cycle time	Approximately 420us
(14)	Shipping style	(1) Chip (2) QIP64 (Number of drivable segments: 72)

Functions

[Watch Function]

(1) Multi-alarm function
- Daily alarm
- Weekly alarm
- Month, date specified alarm

(2) Multi-ON/OFF timer function

(3) Timer function
- Repeat function
- Analog display of remaining time
- Memory function for timer time

(4) Full automatic calendar function

(5) Up/down setting function

(6) 30-minute time signal, 1-hour time signal

(7) World watch

[Game Function]
(1) Action game
(2) Blackjack
(3) Bowling
(4) Highest score display
(5) Game speed select

[Others]
(1) Game's score display
(2) Game's remaining time display

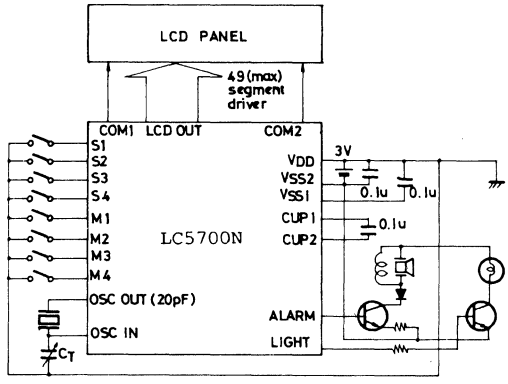
[Avaiable Combination of Functions]
Depends on ROM/RAM capacity. Table 1 shows some examples.

Table 1 Examples of Available Combination of Functions

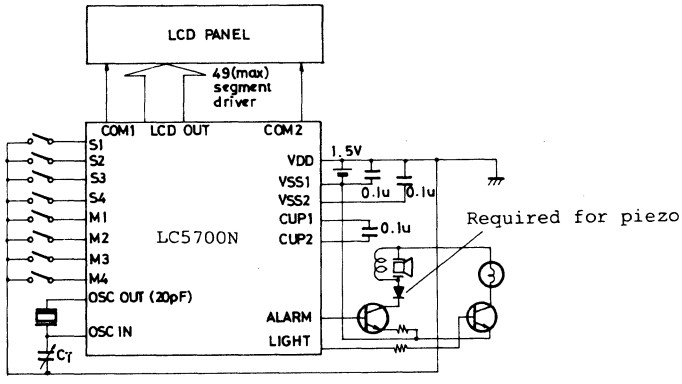
	Ex.1	Ex.2	Ex.3	Ex.4	Ex.5	Ex.6	Ex.7	Ex.8
Base Watch (Hours, minutes)	o	o	o	o	o	o	o	o
Base Watch (Month, date)	o	o	o	o	o		o	
Base Watch (Year)		o	o					
Second Watch (Hours, minutes)	o	o	o					
Second Watch (Month, date)			o					
Alarm 1	o	o	o		o	o	o	
Alarm 2	o	o	o					
Alarm 3		o						
Stopwatch (1/100 sec.)	o	o	o	o		o		
Timer	o							
Timer Signal	o	o	o				o	
World Watch				o	o			
Game 1 (SLOW/FAST)						o	o	o
Game 2								o

Application Circuit

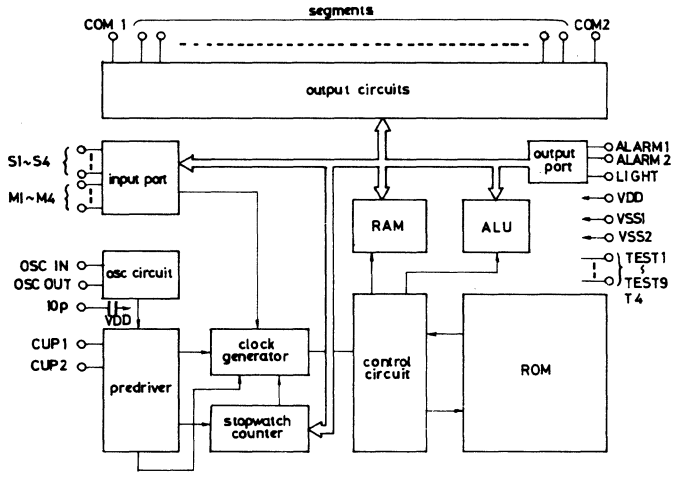
(1) Using Li battery



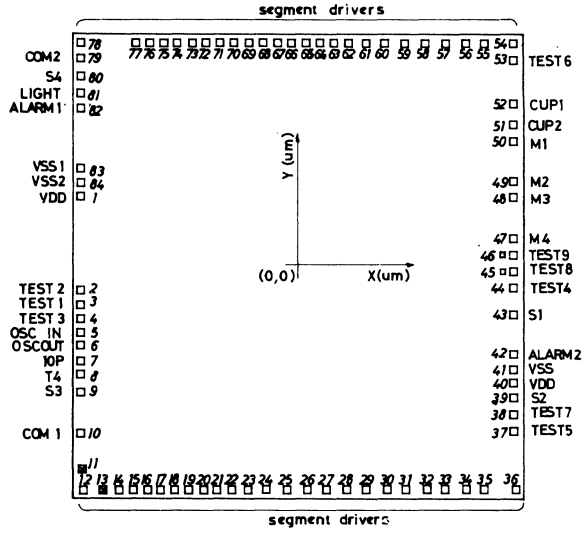
(2) Using Ag battery



Equivalent Circuit Block Diagram

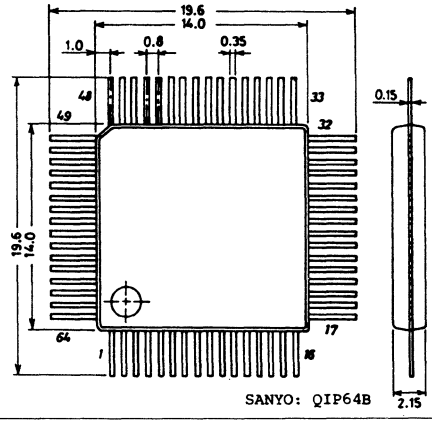


LSI Chip PAD Assignment



Chip size	5.31mm(X direction) x 5.44mm(Y direction)
Chip thickness	480um
Pad size	120um x 120um

Case Outline 3026B-Q64BIC
(unit:mm)



Pad Name, Pad Coordinates and Pin Assignment

QIP64 Pin Assignment				
	pad No.	X (μm)	Y (μm)	Pin Name
56	1	-2495	768	VDD
57	2		-266	TEST2
58	3		-446	TEST1
59	4		-627	TEST3
60	5		-808	OSC IN
61	6		-989	OSC OUT
-	7		-1170	10P
-	8		-1351	T4
62	9		-1562	S3
63	10		-2061	COM1
-	11		-2309	NC
64	12	-2495	-2563	SEGMENT
-	13	-2264		NC
1	14	-2084		SEGMENT
2	15	-1903		
3	16	-1722		
-	17	-1541		
-	18	-1360		
-	19	-1179		
-	20	-998		
-	21	-817		
-	22	-636		
4	23	-455		(PSTB5)
5	24	-275		(PSTB4)
6	25	-94		(PSTB3)
7	26	87		(PSTB2)
8	27	311		(PSTB1)
9	28	536		(DBUSC)
10	29	761		(PSTB0)
11	30	986		(PSTB2C)
12	31	1211		(DBUSa)
13	32	1436		(DBUSb)
14	33	1661		(DBUSd)
15	34	1852		(DBUSe)
16	35	2033		(DBUSf)
17	36	2495	-2563	SEGMENT(DBUSg)
18	37		-1868	TEST5
19	38		-1688	TEST7
20	39		-1472	S2
-	40		-1291	(VDD)
-	41		-1110	(VSS)
21	42	2495	-929	(ALARM2 OUT)

QIP64 Pin Assignment				
	pad No.	X (μm)	Y (μm)	Pin Name
22	43	2495	-562	S1
23	44		-266	TEST4
-	45		-85	(テニタPch)
-	46		126	(テニタNch)
25	47		306	M4
26	48		770	M3
27	49		950	M2
28	50		1417	M1
29	51		1598	CUP2
30	52		1818	CUP1
31	53		2342	TEST6
32	54	2495	2563	SEGMENT
33	55	2127		
34	56	1869		(PSTB1C)
35	57	1685		(PSTB6)
36	58	1499		(PSTB7)
37	59	1318		(PSTB8)
38	60	1137		(PSTB9)
39	61	956		(PSTB10)
-	62	775		
-	63	594		
40	64	413		
-	65	232		
-	66	51		
-	67	-130		
41	68	-311		
42	69	-491		
-	70	-672		
-	71	-853		
43	72	-1034		
44	73	-1215		
45	74	-1396		
46	75	-1577		
47	76	-1758		
48	77	-1940		
49	78	-2495	2563	SEGMENT
50	79		2373	COM2
51	80		2167	S4
52	81		1971	LIGHT OUT
53	82		1790	ALARM1 OUT
54	83		1130	VSS1
55	84	-2495	949	VSS2

- The pad coordinates are such that the chip center is taken as the origin and the values for (X,Y) represent the coordinates of the center point of each pad.
- Pin 24 of the QIP64 is connected to the substrate of the LSI. Therefore, this pin cannot be used.

Pin Description

Pin Name	Input/ Output	Functions
S1 to S4	Input	Input ports for watch sequence. Including chattering preventer.
M1 to M4	Input	Input ports. Capble of reading data of this pin direct into RAM.
ALARM1 OUT	Output	Output pin for driving control transistor (for alarm)
ALARM2 Out	Output	Output pin for driving control transistor and outputting sampling signal of clocked input port (M port)
LIGHT OUT	Output	Output pin for driving control transistor (for light)
SEGMENT	Output	Segment output pin for driving LCD
COM1,COM2	Output	Common output pin for driving LCD
OSC IN	Input	By connecting crystal resonator across this pin and OSC OUT pin, oscillator is formed.
OSC OUT	Output	By connecting crystal resonator across this pin and OSC IN pin, oscillator is formed. 20pF capacitor is connected across this pin and V_{DD} pin inside LSI.
10p	Input	10pF is connected across this pin and V_{DD} pin inside LSI. By connecting this pin and OSC OUT pin, 30pF capacitor is connected across this pin and V_{DD} pin inside LSI.
CUP1	Input	By connecting 0.1uF capacitor across this pin and CUP2 pin, doubler and halver are formed for Ag battery and Li battery respectively.
CUP2	Input/ Output	By connecting 0.1uF across this pin and CUP1 pin, doubler and halver are formed for Ag battery and Li battery respectively.
T4	Output	System clock output pin. Of system clocks(T1 to T4), T4 is outputted.
TEST1 to TEST9		Test pin
V_{DD}		Power supply pin. Normally connected to 0V
V_{SS1}		Power supply pin. For Ag battery, connected to -1.5V. For Li battery, 0.1uF capacitor is connected across this pin and V_{DD} pin.
V_{SS2}		Power supply pin. For Li battery, connected to -3V. For Ag battery, 0.1uF capacitor is connected across this pin and V_{DD} pin.
NC		Open pin (This pin cannot be used)

Description of input ports, output ports, PLA switch option

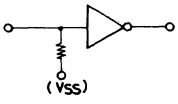
(Defer to input port, output port configurations.)

(1) LIGHT drive input

One of S1 to S4 is selected and specified for LIGHT output drive input. For example, when H level (V_{DD} level) is applied to S1 and LIGHT output is made active, S1 is specified for LIGHT drive output. If LIGHT output is not used, S4 must be used for LIGHT drive input.

(2) S2 to S4

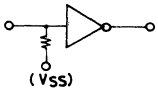
Pull-down resistance input



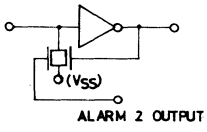
(V_{SS}): For step-up circuit, V_{SS1}.
(The same shall apply hereinafter.)
For step-down circuit, V_{SS2}.
(The same shall apply hereinafter.)

(3) S1

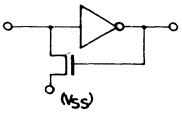
Pull-down resistance input (N.P.)



Clock pull-down resistance input(C.P.)

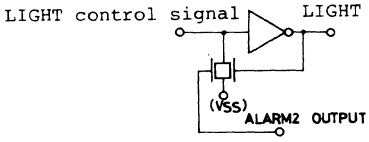


Special pull-down resistance input(I.P.)

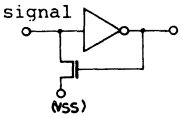


(4) M1 to M2

Clocked pull-down resistance input (C.P.)



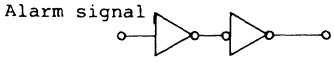
Special pull-down resistance input (I.P.)



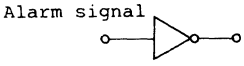
- If S1 is set to C.P. mode, M1 to M4 must be also set to C.P. mode.
- If S1 is set to I.P. mode, M1 must be also set to I.P.mode.

(5) ALARM1 OUT

Normal "L" level(L)

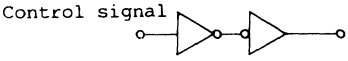


Normal "H" level(H)

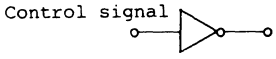


(6) ALARM2 OUT

Normal "L" level(L)

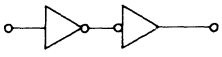


Normal "H" level(H)

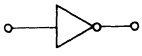


(7) LIGHT OUT

Normal "L" level(L)



Normal "H" level(H)



(8) Priority level of ALARM1 OUT/ALARM2 OUT and LIGHT OUT
When ALARM1 OUT or ALARM2 OUT is active, LIGHT OUT is nonactive.

(9) Reference frequency of ALARM1 OUT
If used for modulation output of ALARM1 OUT, 4KHz or 2KHz is specified for reference frequency.
For 4kHz: ø2 For 2kHz: ø3

(10) Specification of 1/100 second of stopwatch
- For use/nonuse of stopwatch and output of 1/100-second digit at pad No.12 to 36 or pad No.54 to 78 when using stopwatch, the following specification applies.

  Nonuse of stopwatch No.
  Use of stopwatch: Pad No. 54 to 78: Y.U.
  Pad No. 12 to 36: Y.L.
- If 1/100-second digit is at lap display mode, the display content is memorized direct in segment output latch. Therefore, if lap display is released once, the memorized content of 1/100-second digit is cleared.

(11) Specification of interrupt

a. For 1-second counter or flashing output synchronized with 1-second count, the periodical interrupt instruction (interrupt 2 instruction) is available so that a prescribed operation can be performed by applying interrupt at a certain cycle. Two interrupt intervals of 250msec. and 500msec. are available.
   250msec.: ø13
   500msec.: ø14

b. For high-speed operation to be performed internally, the interrupt instruction (interrupt 0 instruction) is available. Two interrupt intervals of 62.5msec. and 125msec. are available.
   62.5msec.: ø11
   125msec.: ø12

(12) Power supply option

- 1.5V or 3.0V external power supply is selectable. In both cases, approximately 3V is applied to LCD.
- In case of 1.5V power supply, this voltage is doubled to be applied to LCD. In case of 3.0V power supply, this voltage is halved to be internal logic voltage and intermediate voltage for LCD. In case of 3.0V power supply, a voltage nearly equal to V_{SS2} is applied to V_{SS1} at the following modes.

  (1) Initial clear

  (2) LIGHT and ALARM1/ALARM2 signals get active.

  For (1), operation never fails to occur. For(2), software is used. In both cases, software is used for specifying operation time.

  For 1.5V power supply: Double type DB

  For 3.0V power supply: Halver type HV

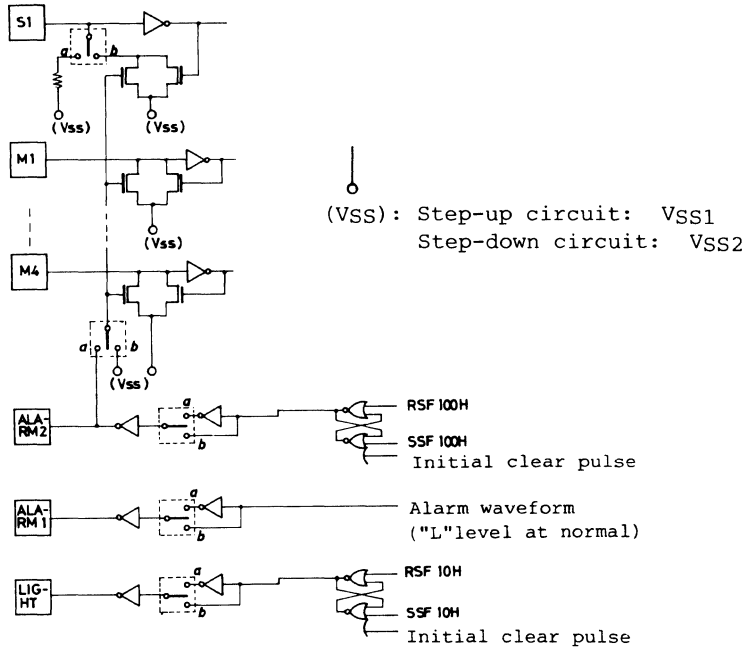
(13) Initial clear

By appling V_{DD} level to S1, S2, S3, S4 simultaneously, internal logics are all initial-cleared.

Option Specification Table

Item	Select Contents			
Line drive input	S1	S2	S3	S4
S1	N.P.	C.P./I.P.	-	-
Mi to M4	C.P.	I.P.	-	-
ALARM1 OUT	L	H	-	-
ALARM2 OUT	L	H	-	-
LIGHT OUT	L	H	-	-
Reference frequency of ALARM	ø2	ø3	-	-
Stopwatch	No.	Y.U.	Y.L.	-
Interrupt 2	ø13	ø14	-	-
Interrupt 0	ø11	ø12	-	-
Power supply circuit	DB	HV	-	-

Input Port, Control Output Configuration



PLA Option of Segment Output Section

The LC5700N is capable of changing the combination of segment outputs freely according to LCD panel. Fig.(a) shows the segment output configuration.
The LC5700N is provided with segment outputs: 25 pads and 24 pads at the upper and lower sides of LSI respectively. These respective segment drivers, being for 1/2 duty, 1/2 bias LCD, are connected to 2 latches (Fig.(b)). By switching output of this latch and signal connected to clock pin by PLA, the combination of segment outputs can be changed freely. One of DBUSa to g is connected to input pin and PSTB1C or PSTB2C and one of PSTB0 to 5 or one of PSTB6 to 11 are connected to clock pin.
In this case, however, PSTB6 to 11 are assigned to the upper segment outputs of LSI and PSTB0 to 5 are assigned to the lower segment outputs of LSI.
For example, it is impossible to assign PSTB6 to pad No.12.
One concrete example is described as follows:
As shown in Fig.(b), it is assumed that DBUSd is connected to input pin of latch X which is displayable corresponding to segment information of COM1 side, PSTB1C and PSTB1 are connected to clock pin, and DBUSa is connected to input pin which is displayable corresponding to segment information of COM2 side, PSTB2C and PSTB3 are connected to clock pin. In this case, fill out SEGMENT OUTPUT SECTION PLA OPTION INSTRUCTION as follows: As shown in Fig.(c), mark the columns of PSTB1C, PSTB1, DBUSd for COM1(X) with O, and mark the columns of PSTB2C, PSTB3, DBUSa for COM2(Y) with O. In this case, P value of strobe specification for WRT instruction is 2.
That is to say, when (WRT2, Q) instruction is executed, data at RAM address Q is outputted to DBUSa to g through data decorder. DBUSd, one of these outputs, is stored in latch X of pad No. 12 and display appears on LCD panel.
P value of strobe specification for WRT instruction is 7. When (WRT7,Q) instruction is executed, new data is stored in latch Y.
The same rule applies to other pads.
The relation between panel strobe and strobe specification for WRT instruction is shown in Fig.(d).

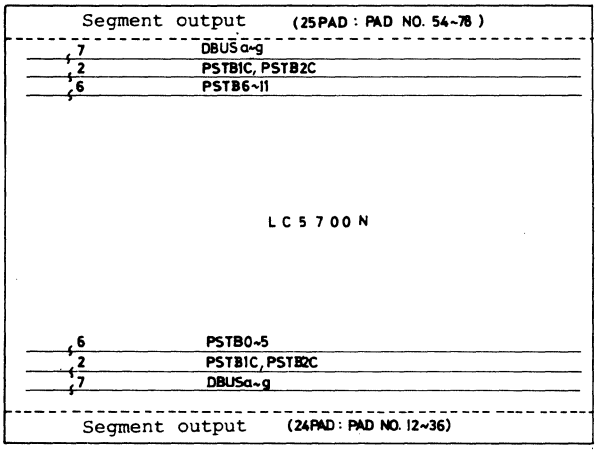


Fig. (a) Segment output configuration (1)

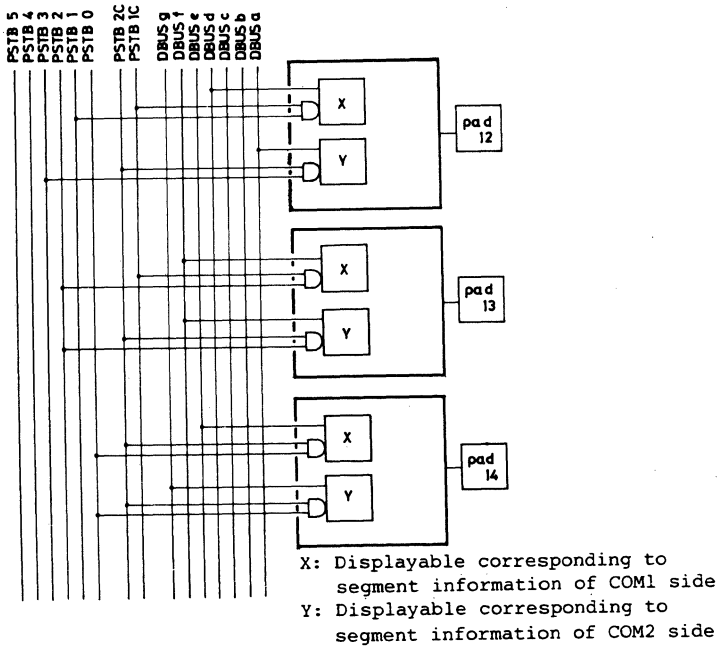


Fig. (b) Segment output configuration (2)

Pin name of corresponding LCD panel

Pin name of corresponding LCD panel

PAD NO	SEGMENT		PANEL STROBE														DATA BUS							P value of strobe specification for WRT instruction (WRT P,Q) (Q value:RAM address)
	COM 1 (X)	COM 2 (Y)	PSTB 1C	PSTB 2C	PSTB 0	PSTB 1	PSTB 2	PSTB 3	PSTB 4	PSTB 5	PSTB 6	PSTB 7	PSTB 8	PSTB 9	PSTB 10	PSTB 11	SBUS a	DBUS b	DBUS c	DBUS d	DBUS e	DBUS f	DBUS g	
12			○			○														○				2
				○				○									○							7
13			○				○															○		4
				○			○															○		5
14				○	○																○			1
				○	○																		○	1
15																								
16																								

For pad No.12 to 36, use PSTBO to 5.

For pad No.54 to 78, use PSTB6 to 11.

Fig.(C) Example of entry in segment output section PLA option instruction

PANEL STROBE													P value of strobe specification for WRT instruction (WRT P,Q) (Q value:RAM address)	Others
PSTB 1C	PSTB 2C	PSTB 0	PSTB 1	PSTB 2	PSTB 3	PSTB 4	PSTB 5	PSTB 6	PSTB 7	PSTB 8	PSTB 9	PSTB 10	PSTB 11		
○		○												0	
	○	○												1	
○			○											2	
	○		○											3	
○				○										4	
	○			○										5	
○					○									6	
	○				○									7	
○						○								8	
	○					○								9	
○							○							AH	
	○						○							BH	
○								○						CH	
	○							○						DH	
○									○					EH	
	○								○					FH	
○										○				10H	
	○									○				12H	
○											○			13H	
	○										○			14H	
○												○		15H	
	○											○		16H	
○													○	17H	
	○												○	18H	

Fig.(d) Relation between panel strobe and strobe specification for WRT instruction

[Operation from 1.5V battery]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS2}		-4.0 to +0.3	V
	V_{SS1}		-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1,S2,S3,S4,M1,M2,M3,M4, TEST1,TEST3,TEST4,TEST5, TEST6,TEST7,10P,OSCIN	V_{SS1}-0.3 to +0.3	V
Maximum Output Voltage	V_{OUT1}	OSCOUT,TEST2,CUP2,ALARM1, ALARM2,LIGHT,T4	V_{SS1}-0.3 to +0.3	V
	V_{OUT2}	All segment drivers, COM1,COM2,CUP1	V_{SS2}-0.3 to +0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C,V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.3	V
	V_{SS2}	V_{SS1}=-1.3 to -1.65V	-3.3		-2.4	V
"H"level Input Voltage	V_{IH}	V_{SS1}=-1.55V,S1,S2,S3,S4, M1,M2,M3,M4	-0.2		0	V
"L"level Input Voltage	V_{IL}	V_{SS1}=-1.55V,S1,S2,S3,S4, M1,M2,M3,M4	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	f_{opg}	V_{SS1}=-1.3 to -1.65V, Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

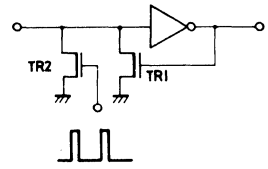
			min	typ	max	unit
Input Resistance	rIN1	V_{SS1}=-1.55V,Note 1	200		2000	kohm
	rIN2	V_{SS1}=-1.55V,TEST1,TEST3, TEST4,TEST5,TEST6,TEST7	1		100	kohm
	rIN3A	V_{SS1}=-1.55V TR1:V_{IL}=V_{SS1}+0.2V,Note 2	10		100	kohm
	rIN3B	V_{SS1}=-1.55V,TR2:Note 2	200		2000	kohm
"H"level Output Voltage	V_{OH1}	V_{SS1}=-1.55V,I_{OH}=-0.4uA, segment driver	-0.2			V
"L"level Output Voltage	V_{OL1}	V_{SS1}=1.55V,I_{OH}=-0.4uA, segment driver			V_{SS2}+0.2	V
"H"level Output Voltage	V_{OH2}	V_{SS1}=-1.55V,I_{OH}=-0.4uA, COM1,COM2	-0.2			V
"M"level Output Voltage	V_{OM}	V_{SS1}=-1.55V,I_{OH}=-4uA, I_{OL}=4uA,COM1,COM2	V_{SS1}-0.2		V_{SS1}+0.2	V
"L"level Output Voltage	V_{OL2}	V_{SS1}=-1.55V,I_{OL}=4uA, COM1,COM2			V_{SS2}+0.2	V
"H"level Output Voltage	V_{OH3}	V_{SS1}=-1.35V,I_{OH}=-250uA ALARM1,LIGHT		-0.65		V
"L"level Output Voltage	V_{OL3}	V_{SS1}=-1.35V,I_{OL}=250uA ALARM1,LIGHT		V_{SS1}+0.65		V
"H"level Output Voltage	V_{OH4}	V_{SS1}=-1.35V,I_{OH}=50uA, ALARM2	-0.65			V
"L"level Output Voltage	V_{OL4}	V_{SS1}=-1.35V,I_{OL}=50uA, ALARM2			V_{SS1}+0.65	V
Output Voltage (Doubler)	V_{SS2}	C_1=C_2=0.1uF, V_{SS1}=-1.35V	-3.3		-2.5	V
Current Dissipation	I_{DD}	C_1=C_2=0.1uF,Co=Cg=20pF, C_I=25kohm,V_{SS1}=-1.55V		2.0 (Note 3)		uA
Oscillation Start Voltage	Vstt	C_1=C_2=0.1uA,Co=Cg=20pF, C_I=25kohm	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	C1=C2=0.1uF,Co=Cg=20pF, C_I=25kohm	-1.65		-1.3	V

			min	typ	max	unit
Oscillation Start Time	t_{stt}	C1=C2=0.1uF,Co=Cg=20pF, C_I=25kohm,V_{SS1}=-1.35V			10	sec
Built-in Capacitance for Oscillation	10P	External terminal	8	10	12	pF
	20P	OSC OUT	16	20	24	pF

Note 1: Applicable to S2,S3,S4. May be applicable to S1 according to input port option.

Note 2: Applicable to M1,M2,M3,M4. May be applicable to S1 according to input port option.

Note 3: Differs with mask ROM contents.



[Operation from 3V battery]

Absolute Maximum Ratings at Ta=25±2°C,V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS2}		-4.0 to +0.3	V
	V_{SS1}		-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	TEST1,TEST3,TEST4,TEST5, TEST6,TEST7,10P,OSCIN	V_{SS1}-0.3 to +0.3	V
	V_{IN2}	S1,S2,S3,S4,M1,M2,M3,M4	V_{SS2}-0.3 to +0.3	V
Maximum Output Voltage	V_{OUT1}	TEST2,CUP2	V_{SS1}-0.3 to +0.3	V
	V_{OUT2}	All segment drivers, COM1,COM2,CUP1,ALARM1, ALARM2,LIGHT,T4	V_{SS2}-0.3 to +0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C,V_{DD}=0V

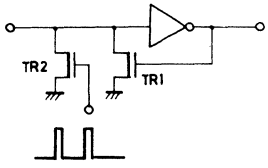
			min	typ	max	unit
Supply Voltage	V_{SS2}		-3.6		-2.0	V
	V_{SS1}		-3.6		-1.3	V
"H"level Input Voltage	V_{IH}	S1,S2,S3,S4,M1,M2,M3,M4	-0.2		0	V
"L"level Input Voltage	V_{IL}	S1,S2,S3,S4,M1,M2,M3,M4	V_{SS2}		V_{SS2}+0.2	V
Operating Frequency	f_{opg}	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C,V_{DD}=0V

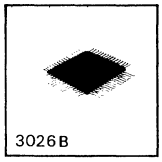
			min	typ	max	unit
Input Resistance	rIN1	V_{SS}=-2.9V,Note 1	200		2000	kohm
	rIN2	V_{SS2}=-2.9V,TEST1,TEST3, TEST4,TEST5,TEST6,TEST7	1		100	kohm
	rIN3A	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.2V, TR1:Note 2	10		100	kohm
	rIN3B	V_{SS2}=-2.9V,TR2:Note 2	200		2000	kohm
"H"level Output Voltage	V_{OH1}	V_{SS2}=-2.9V,I_{OH}=-0.4uA segment driver	-0.2			V
"L"level output Voltage	V_{OL1}	V_{SS2}=-2.9V,I_{OL}=0.4uA segment driver			V_{SS2}+0.2	V
"H"level Output Voltage	V_{OH2}	V_{SS2}=-2.9V,I_{OH}=-4uA, COM1,COM2	-0.2			V
"M"level Output Voltage	V_{OM}	V_{SS2}=-2.9V,I_{OH}=-4uA, I_{OL}=4uA,COM1,COM2	V_{SS2}/2-0.2		V_{SS2}/2+0.2	V
"L"level Output Voltage	V_{OL2}	V_{SS2}=-2.9V,I_{OL}=-4uA, COM1,COM2			V_{SS2}+0.2	V
"H"level Output Voltage	V_{OH3}	V_{SS2}=-2.4V,I_{OH}=-250uA, ALARM1,LIGHT	-0.65			V
"L"level Output Voltage	V_{OL3}	V_{SS2}=-2.4V,I_{OL}=250uA, ALARM1,LIGHT			V_{SS2} +0.65	V

			min	typ	max	unit
"H"level Output Voltage	V_{OH4}	V_{SS2}=-2.4V,I_{OH}=-50uA, ALARM2	-0.65			V
"L"level Output Voltage	V_{OL4}	V_{SS2}=-2.4V,I_{OL}=50uA, ALARM2		V_{SS2}	+0.65	V
Output Voltage(Halver)	V_{SS1}	V_{SS2}=-2.8V,C_1=C_2=0.1uF			-1.35	V
Current Dissipation	I_{DD1}	V_{SS2}=-2.9V,Co=Cg=20pF, C_I=25kohm,C_1=C_2=0.1uA		Note 3		uA
	I_{DD2}	V_{SS2}=2.5V,heavy load, C_1=C_2=0.1uF		70 Note 4		uA
Oscillation Start Voltage,V_{SS1}	V_{stt}	V_{SS1}=V_{SS2},C_1=C_2=0.1uF, Co=Cg=20pF,CI=25kohm			-1.35	V
Oscillation Hold Voltage,V_{SS2}	V_{HOLD}	· V_{SS1}=1/2V_{SS2}, C_1=C_2=0.1uF, Co=Cg=20pF,C_I=25kohm	-3.6		-2.6	V
		· Heavy load,V_{SS1}=V_{SS2}, CI=25kohm,Co=Cg=20pF, C_1=C_2=0.1uF	-3.6		-1.3	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=-2.9V, C_1=C_2=0.1uF,Co=Cg=20pF,CI=25kohm			10	sec
Built-in Capacitance for Oscillation	1OP	External terminal	8	10	12	pF
	2OP	OSC OUT	16	20	24	pF

Note 1: Applicable to S2,S3,S4. May be applicable to S1 according to input port option.
Note 2: Applicable to M1,M2,M3,M4. May be applicable to S1 according to input port option.
Note 3: Differs with mask ROM contents.
Note 4: Heavy load: At the time of initialize, lamp or buzzer drive.



LC5732



C MOS LSI

Single-Chip 4-Bit Microcomputer (with LCD Driver)

PRELIMINARY

The LC5732 is a C-MOS 4-bit microcomputer that operates on low voltage, very low current and contains an LCD driver. It also contains a 4-bit parallel processing ALU, a program memory ROM, abundant LCD segment outputs, a prescaler, a 32.768KHz crystal oscillatior.
It is especially suited for use in high-grade timepiece, time controller, LCD game with timepiece applications.

(1) Hardware features

- Supply voltage: 1.5V or 3.0V typ. (mask option)
- Very low current dissipation:
  3.0uA typ. (1.5V supply, during timekeeping operation)
  1.5uA typ. (3.0V supply, during timekeeping operation)
- Crystal oscillation for timekeeping (32.768kHz crystal connected externally) or CR oscillator
- Abundant output pins for LCD panel drive (27 pins)

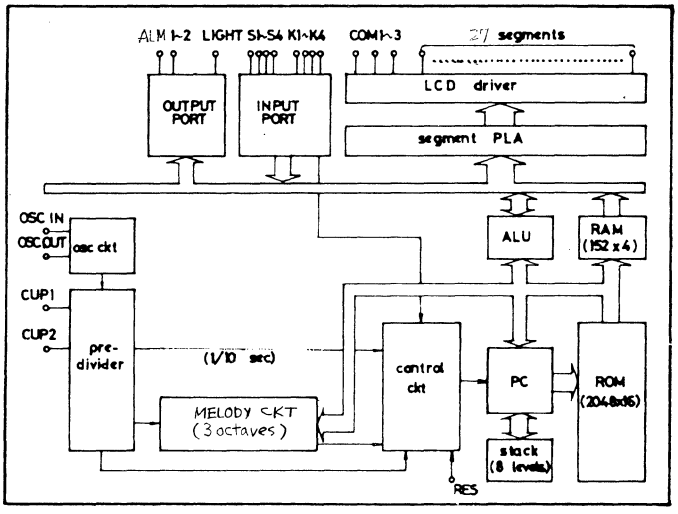
Drivable LCD panel	Number of drivable LCD segments
1/2 bias 1/3 duty	81 segments
1/2 bias 1/2 duty	54 segments
Static	27 segments

- On-chip melody function: 3 octaves
- Input/output pins
  Number of inputs: 8
  Control output pins: 3 pins
- Possible to use LCD panel drive output pins as ports for output only (mask option)
- ROM: 2048 x 8 bits
- RAM: 48 x 4 bits
- On-chip step-up circuit/step-down circuit
- Shipping style: Chip (or QIP64)

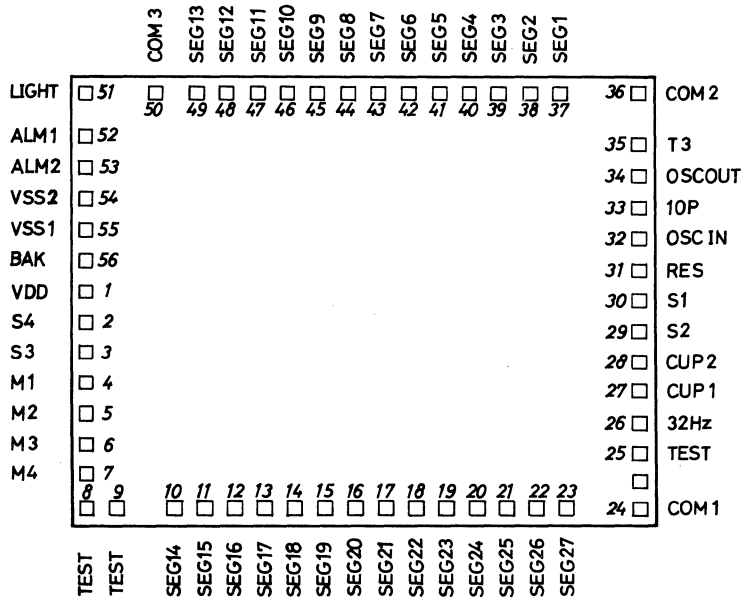
(2) Software features

- Powerful instruction set: 92 instructions
- Table read instruction
- 1-level subroutine nesting
- On-chip 15-bit divider for timekeeping (delivers overflow signal every 64ms/100ms/500ms when X'tal OSC is used)
- Halt function

(3) System block diagram

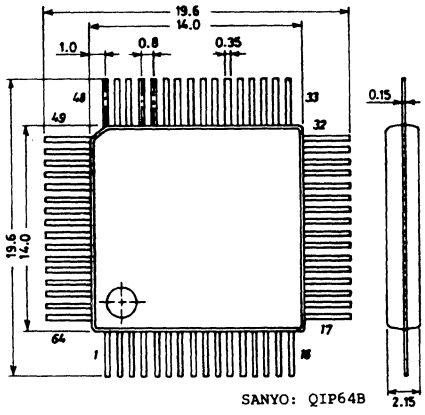


(4) Pad assignment



* SEG14 to SEG27 can be used for output ports. (Mask option)
Chip size: 4.61mm x 3.54mm
Chip thickness: 480um
Pad size: 120um x 120um

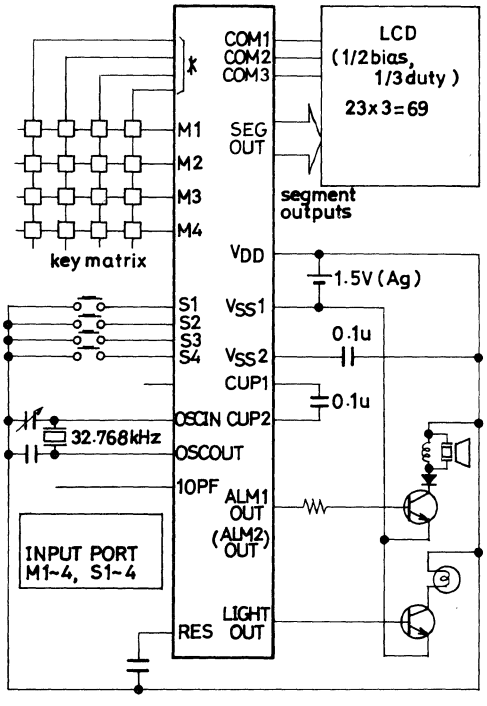
(5) Package
Case Outline 3026B-Q64BIC
(unit: mm)



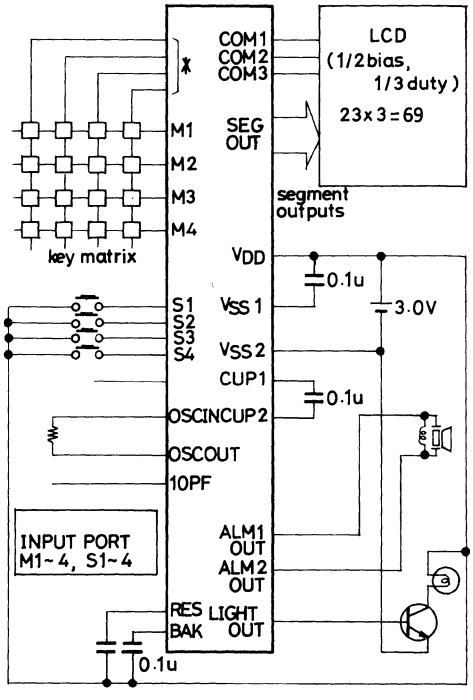
Sample Application Circuit

(1) Ag battery-used application
(1/2 bias 1/3 duty)
*: 4 segment outputs are used for output ports.

(2) Li battery-used application
(1/2 bias 1/3 duty)
*: 4 segment outputs are used for output ports.

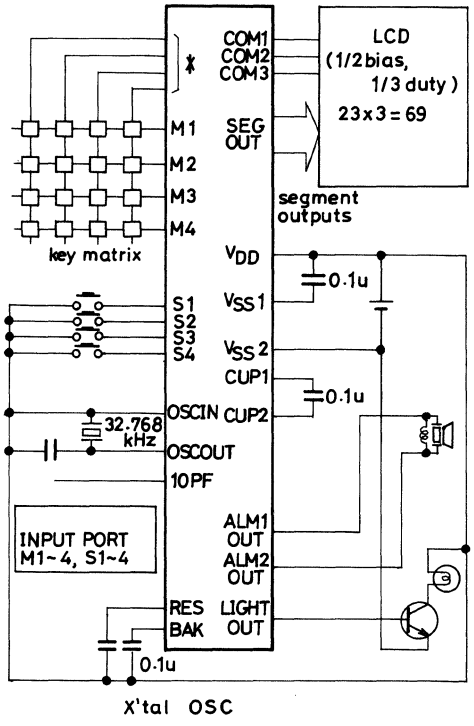


X'tal OSC

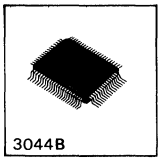


CR OSC

(3) EXT-V-used application (1/2 bias 1/3 duty)
*: 4 segment outputs are used for output ports.



LC5800



C MOS LSI

Single-Chip 4-Bit Microcomputer (with LCD Driver)

Ⓔ 1271D

The LC5800 is a C-MOS 4-bit microcomputer that operates on low voltage, very small current and contains an LCD driver. It contains a 4-bit parallel processing ALU, many LCD segment outputs, many I/O ports, a prescaler, and a 32.768kHz crystal oscillator.
It is ideally suited for use in desk-top calculator, camera, speech synthesis LSI controller, equipment controller applications as well as high-grade game watch/clock applications.

(1) Hardware features

- Supply voltage : 1.5V or 3.0V (typ.) (mask option)
- Very small current dissipation :
  3.0uA typ. (1.5V supply voltage, at watch/clock operating mode)
  1.5uA typ. (3.0V supply voltage, at watch/clock operating mode)
- Built-in crystal oscillator for watch/clock (32.768kHz crystal connected externally)
- Many output pins for LCD panel drive (42 pins)

Drivable LCD panel	Number of drivable LCD segments
1/3 bias 1/3 duty	126 segments
1/2 bias 1/3 duty	126 segments
1/2 bias 1/2 duty	84 segments
Static	42 segments

- Many input/output pins
  Ports for input only : 2 ports/8 pins
  Input/output common ports : 2 ports/8 pins
  Control output pins : 4 pins
- Possible to use LCD panel drive output pins as ports for output only (mask option)
- With initial reset pin
- ROM : 2048 x 16 bits
- RAM : 152 x 4 bits
- Cycle time : 244usec. (or 122usec./mask option)
- Built-in step-up circuit, step-down circuit
- Shipping style : Chip (or QIP80)

(2) Software features

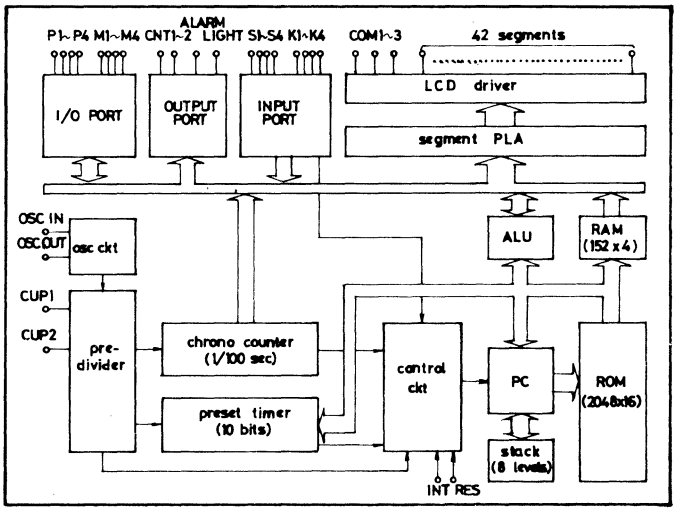
- Powerful instruction set : 121 instructions
- 8-level subroutine nesting (also used for interrupt)
- External interrupt function
- 15-bit divider for watch/clock
- Built-in counter for 1/100-second chronograph
- Built-in 10-bit programmable timer
- HALT function
- Automatic select of all address (direct addressing type)
- Built-in data pointer

(3) Application development tools

For performing application development, the evaluation chip (LC5899) and the specialized application development tools are prepared.

- SDS410 system
  Application development program of microcomputer can be made in assembly language (edit, assemble).
- EVA510 + TB51 + display board + LC5899
  By connecting to the SDS410, application development program can be corrected and debugged. The EVA510 is a control ROM-replaced version of the EVA410.
- TB51 + display board + LC5899
  By using the EPROM (2732) with application development program data written in, mounting evaluation can be performed.

Equivalent Circuit Block Diagram

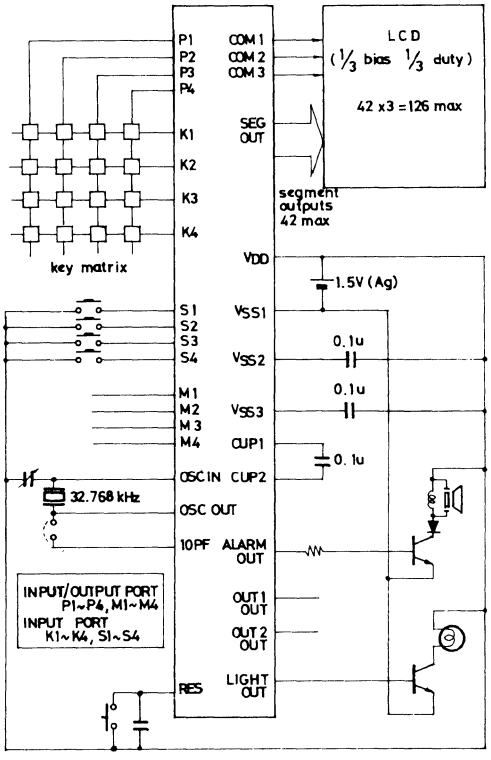


Application Areas

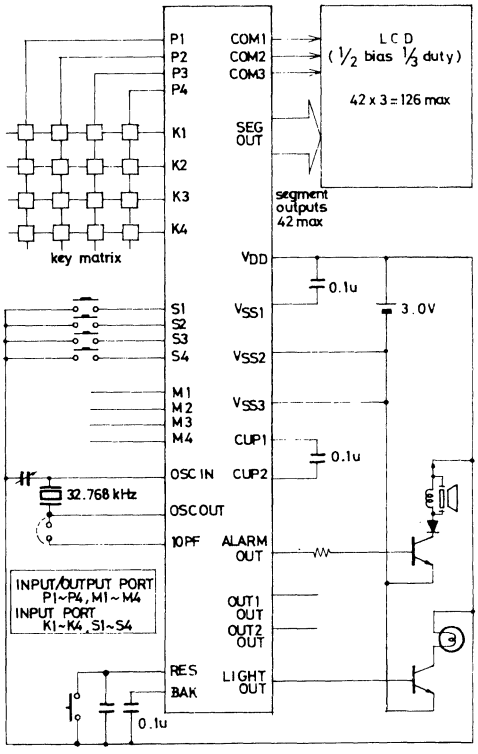
1) Multifunction watch/clock with calculator
2) Controller of speech synthesis LSI
3) Watch/clock with memory (external memory)
4) Controller of camera
5) Mechanical controller of VTR, radio cassette, deck, etc.
6) Controller of telephone dialer, etc.

Sample Application Circuits

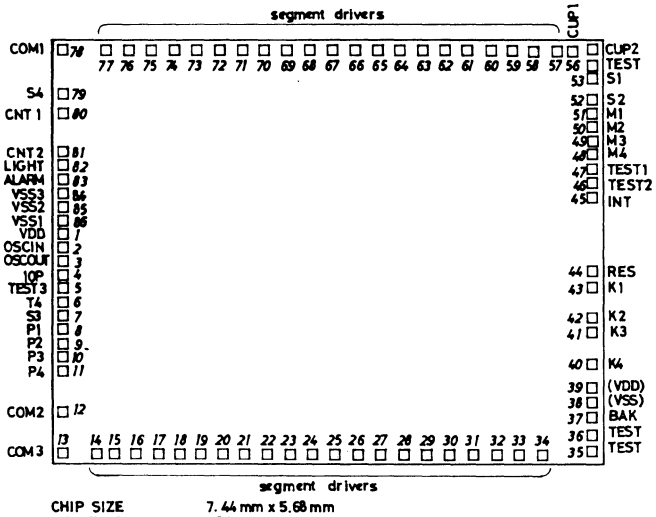
(1) Typical application circuit using Ag battery (1/3 bias 1/3 duty)



(2) Typical application circuit using Li battery (1/2 bias 1/3 duty)

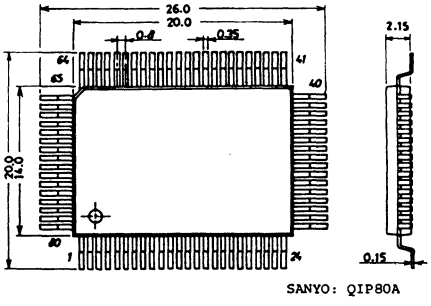


Pad Assignment of LSI Chip



CHIP SIZE 7.44 mm x 5.68 mm
CHIP THICKNESS 480 um
PAD SIZE 120 um x 120 um

Case Outline 3044B-Q80AIC (unit:mm)



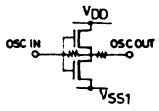
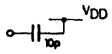
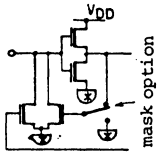
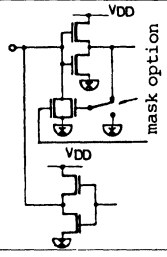
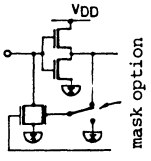
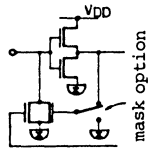
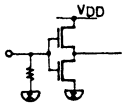
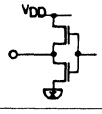
Pad Name and Coordinates

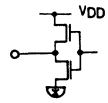
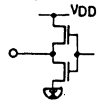
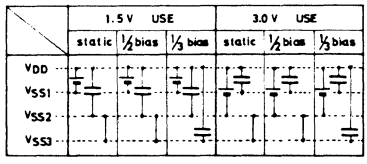
Pin assignment of QIP80				
	pad No	Pin name	X (μm)	Y (μm)
73	1	VDD	-3560	+ 193
74	2	OSCIN	〃	+ 12
75	3	OSCOUT	〃	- 168
-	4	10P	〃	- 348
76	5	TEST3	〃	- 527
77	6	T4	〃	- 708
78	7	S3	〃	- 888
-	8	P1	〃	-1068
-	9	P2	〃	-1247
79	10	P3	〃	-1428
80	11	P4	〃	-1608
1	12	COM2	〃	-2146
2	13	COM3	〃	-2684
3	14	Seg	-3042	〃
4	15	↓	-2810	〃
5	16		-2516	〃
6	17		-2221	〃
7	18		-1925	〃
8	19		-1630	〃
9	20		-1334	〃
10	21		-1040	〃
11	22		- 744	〃
12	23		- 438	〃
13	24		- 133	〃
14	25		+ 174	〃
15	26		+ 480	〃
16	27		+ 786	〃
17	28		+1093	〃
18	29		+1398	〃
19	30		+1703	〃
20	31		+2010	〃
21	32		+2315	〃
22	33	↓	+2621	〃
23	34	Seg	+2928	〃
-	35	TEST	+3560	〃
-	36	TEST	〃	-2473
25	37	BAK	〃	-2253
-	38	(VSS)	〃	-2031
-	39	(VDD)	〃	-1851
26	40	K4	〃	-1545
27	41	K3	〃	-1110
28	42	K2	〃	- 928
29	43	K1	〃	- 494

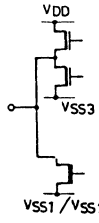
Pin assignment of QIP80				
	pad No	Pin name	X (μm)	Y (μm)
30	44	RES	+3560	- 314
32	45	INT	〃	+ 676
33	46	TEST2	〃	+ 856
34	47	TEST1	〃	+1083
35	48	M4	〃	+1264
36	49	M3	〃	+1444
37	50	M2	〃	+1623
38	51	M1	〃	+1804
39	52	S2	〃	+1983
40	53	S1	〃	+2294
-	54	TEST	〃	+2475
41	55	CUP2	〃	+2684
42	56	CUP1	+3256	〃
43	57	Seg	+3065	〃
44	58	↓	+2770	〃
45	59		+2475	〃
46	60		+2179	〃
47	61		+1884	〃
48	62		+1588	〃
49	63		+1294	〃
50	64		+ 998	〃
51	65		+ 693	〃
52	66		+ 386	〃
53	67		+ 81	〃
54	68		- 226	〃
55	69		- 532	〃
56	70		- 837	〃
57	71		-1143	〃
58	72		-1450	〃
59	73		-1756	〃
60	74		-2061	〃
61	75		-2367	〃
62	76	↓	-2674	〃
63	77	Seg	-2980	〃
64	78	COM1	-3560	〃
65	79	S4	〃	+2079
66	80	CNT1	〃	+1832
67	81	CNT2	〃	+1272
68	82	LIGHT	〃	+1092
69	83	ALARM	〃	+ 913
70	84	VSS3	〃	+ 733
71	85	VSS2	〃	+ 552
72	86	VSS1	〃	+ 372

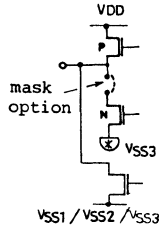
The above pad coordinates are such that the chip center is taken as the origin and the values of (X,Y) represent the coordinates of the center of each pad.
Pins 24, 31 of QIP80 : NC

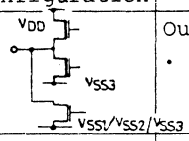
Pin Description

Pad No.	Pin Name	Input/Output	Circuit Configuration	Function
2	OSCIN	Input		32.768kHz crystal is connected across OSCIN and OSCOUT for oscillation. Used as reference clock and system clock for watch/clock.
3	OSCOUT	Output		
4	10P	-		Connected to OSCOUT and used oscillation phase compensation capacitor.
53 52 7 79	S1 S2 S3 S4	Input		Ports for input only With 16ms or 64ms chattering eliminator. By applying V_{DD} to S1 to S4 simultaneously, LSI inside is reset. (mask option)
8 9 10 11 51 50 49 48	P1 P2 P3 P4 M1 M2 M3 M4	Input/Output		Input/output pins for selecting the following 2 operations with instruction. (1) Input pin for fetching data into RAM. (2) Output pin for outputting data from RAM.
43 42 41 40	K1 K2 K3 K4	Input		(1) Input pin for fetching data into RAM through 16ms or 64ms chattering eliminator. (2) K4 signal is used to operate decimal counter (for 1/100-second count) inside LSI with instruction.
45	INT	Input		External interrupt request control input pin.
44	RES	Input		Input pin for resetting LSI inside.
37	BAK			(-) power supply pin for logic unit inside LSI. When using 3.0V supply, a capacitor must be connected across BAK and V_{DD} to prevent logic unit from malfunctioning.
80 81	CNT1 CNT2	Output		Pins for output only

<table>
<tr><th>Pad No.</th><th>Pin Name</th><th>Input/Output</th><th>Circuit Configuration</th><th>Function</th></tr>
<tr><td>82</td><td>LIGHT</td><td>Output</td><td> 
</td><td>Pin for output only.
Suited for outputting signal to drive transistor for light.</td></tr>
<tr><td>83</td><td>ALARM</td><td>Output</td><td> 
</td><td>Pin for output only.
Used to output 4kHz, 2kHz, 1kHz modulation signal with instruction.
Also used to output non-modulation signal.</td></tr>
<tr><td>1</td><td>V_{DD}</td><td></td><td></td><td>(+) Power supply pin.</td></tr>
<tr><td>84
85
86</td><td>V_{SS3}
V_{SS2}
V_{SS1}</td><td></td><td></td><td>(-) power supply pin.
. 1.5V/3.0V selectable with mask option.
For 1.5V use, apply (-) side to V_{SS1}
For 3.0V use, apply (-) side to V_{SS2}
. Also used as power supply for LCD drive.
 

The above Table shows how to connect external parts in each case.</td></tr>
<tr><td>55
56</td><td>CUP1
CUP2</td><td></td><td></td><td>Pins for connecting voltage step-up (step-down) capacitor.</td></tr>
<tr><td>78
12
13</td><td>COM1
COM2
COM3</td><td>Output</td><td> 
</td><td>Output pins for LCD panel common electrode.
The following pin is used in each case.
<table>
<tr><th></th><th>Static</th><th>1/2 duty</th><th>1/3 duty</th></tr>
<tr><td>COM1</td><td>○</td><td>○</td><td>○</td></tr>
<tr><td>COM2</td><td>–</td><td>○</td><td>○</td></tr>
<tr><td>COM3</td><td>–</td><td>–</td><td>○</td></tr>
<tr><td>Alternating frequency</td><td>32Hz</td><td>32Hz</td><td>43Hz</td></tr>
</table></td></tr>
<tr><td>14
to
22

57
to
64</td><td>Segment driver</td><td>Output</td><td> 
</td><td>Output pins for LCD panel segments.
. Also used as output ports with mask option.
. When LSI inside is in reset mode, 32Hz, 64Hz or 128Hz static light-up signal is outputted at COM1 to COM3 and each LCD segment output and all LCD panel segments light up.
. Segment PLA system is adopted to meet the requirements of free pattern on LCD panel. For segment PLA system, refer to the catalog of LC5700.</td></tr>
</table>

Pad No.	Pin Name	Input/Output	Circuit Configuration	Function
23 34 65 77	Segment driver	Output		Output pins for LCD panel segments. . Also used as output ports with mask option.
5 6 35 36 46 47 54	TEST3 T4 TEST TEST TEST2 TEST1 TEST			Test pins (not used by user).
38 39	(V_{SS}) (V_{DD})			Backup power supply pin. Normally, not used.

Note) Ag Battery : ⏚ = V_{SS1}, Li Battery : ⏚ = V_{SS2}

Operation from Ag Battery (static)

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1-4,M1-4,K1-4,P1-4, TEST-3,10P,OSCIN,INT,RES (M1-4,P1-4: Input mode)	V_{SS1}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,CUP2,OSCOUT,ALARM, LIGHT,CNT1,CNT2,M1-4,P1-4 (M1-4,P1-4: Output mode)	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT,COM1,CUP1	V_{SS2}-0.3 to 0.3	V
Operating Temperature	Topg		-20 to +65	°C
Storage Temperature	Tstg		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.3		-2.4	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,P1-4,INT, RES,(M1-4,P1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	fopg	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr.,*1,Fig.1	50		500	kohm
	R_{IN1B}	V_{SS1}=-1.55V,"L"-level pull-in tr.,*1,Fig.1	200		2000	kohm
	R_{IN2A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, input mode,"L"-level hold tr., *2,Fig.1	50		500	kohm
	R_{IN2B}	V_{SS1}=-1.55V,input mode,"L"-level hold tr.,*2,Fig.1	200		2000	kohm
	R_{IN3}	V_{SS1}=-1.55V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=-1.55V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=-1.55V, I_{OL}=0.4uA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=-1.55V, I_{OH}=-4uA, COM1	-0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=-1.55V, I_{OL}=4uA, COM1			V_{SS2}+0.2	V

			min	typ	max	unit
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=-1.35V, I_{OH}=-250uA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250uA, ALM, LIGHT, CNT1, CNT2		V_{SS1}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)		V_{SS1}+0.2		V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1uF, f_{opg}=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	$\|I_{DD}\|$	V_{SS1}=-1.55V, standard watch / clock operation, C1=C2=0.1uF, C_o=C_g=20pF, CI=25kohm, Fig. 2		2.0		uA
Oscillation Start Voltage	V_{stt}	C_o=C_g=20pF, CI=25kohm, Fig. 3	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, C_o=C_g=20pF, CI=25kohm, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	V_{SS}=-1.35V, C_o=C_g=20pF, CI=25kohm, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Li Battery [Static]

Absolute Maximum Ratings at T_a=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}-0.3 to 0.3	V
	V_{IN2}	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4 : Input mode)	V_{SS2}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{BAK}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4 : Output mode)	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at T_a=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4, K1-4, M1-4, P1-4, INT, RES (M1-4, P1-4 : Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}	V_{SS2}+0.4		V
Operating Frequency	f_{opg}	T_a=-20 to +65 °C	32		33	kHz

Electrical Characteristics at T_a=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-Level hold tr., *2, Fig. 4	50		500	kohm

			min	typ	max	unit
Input Resistance	R_{IN2B}	V_{SS2}=-2.9V,input mode,"L"-level pull-in tr.,*2,Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V,I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V,I_{OL}=0.4uA,SEGOUT		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V,I_{OH}=-4uA,COM1	-0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V,I_{OL}=4uA,COM1		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V,I_{OH}=-250uA, ALM,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V,I_{OL}=250uA, ALM,CNT1,CNT2		V_{SS2}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.4V,I_{OH}=-150uA,LIGHT	-1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.4V,I_{OL}=150uA,LIGHT		V_{SS2}+1.5		V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=-2.9V,I_{OH}=-40uA,M1-4, P1-4 (M1-4,P1-4:Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=-2.9V,I_{OL}=40uA,M1-4, P1-4 (M1-4,P1-4:Output mode)		V_{SS2}+0.4		V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V,C1=C2=0.1uF, f_{opg}=32.768kHz			-1.35	V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V,standard watch/clock operation,C1=C2=0.1uF, C_o=Cg=20pF,CI=25kohm,Fig. 5		1.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2},C_o=Cg=20pF, CI=25kohm,Fig. 6	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}≅V_{SS2}=2/2,Co=Cg= 20pF,CI=25kohm,Fig. 5			-2.6	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=-2.9V,C_o=Cg=20pF, CI=25kohm,Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [Static]

Absolute maximum Ratings at Ta=25±2°C,V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS2}	V_{SS2}=V_{SS3}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P,OSCIN,TEST3	V_{SS1}-0.3 to 0.3	V
	V_{IN2}	S1-4,M1-4,K1-4,P1-4,TEST1, TEST2,INT, RES (M1-4,P1-4 : Input mode)	V_{SS2}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,CUP2,OSCOUT	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT,COM1,CUP1,ALARM, LIGHT,CNT1,CNT2,M1-4,P1-4, (M1-4,P1-4: Output mode)	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C,V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,P1-4, INT, RES, (M1-4,P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig.13	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig.13	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-Level hold tr., *2, Fig.13	50		500	kohm
	R_{IN2B}	V_{SS2}=-2.9V, input mode, "L"-Level tr., *2, Fig.13	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V, TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4uA, SEGOUT		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4uA, COM1	-0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4uA, COM1		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250uA, ALM,LIGHT,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250uA, ALM,LIGHT,CNT1,CNT2		V_{SS2}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V, I_{OH}=-40uA, M1-4, P1-4 (M1-4,P1-4:Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.9V, I_{OL}=40uA, M1-4, P1-4, (M1-4,P1-4:Output mode)		V_{SS2}+0.4		V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V, standard watch/clock operation, C_o=C_g=20pF, CI=25kohm, Fig.14		5.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, C_o=C_g=20pF, CI=25kohm, Fig.15	-2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS2}, C_o=C_g=20pF, CI=25kohm, Fig.14			-2.0	V
Oscillation Start Voltage	t_{stt}	V_{SS1}=V_{SS2}=-2.9V, C_o=C_g=20pF, CI=25kohm, Fig.15			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Ag Battery [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}	V_{SS}=V_{SS3}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1-4, M1-4, K1-4, P1-4, TEST1-3 10P, OSCIN, INT, RES (M1-4, P1-4 : Input mode)	V_{SS1}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4 : Output mode)	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1-2, CUP1	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.3		-2.4	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4 : Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	f_{opg}	Ta=-20 to +65 °C	32		33	kHz

Electrical Characteristics at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS1}=-1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	R_{IN2A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS1}=-1.55V, input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS1}=-1.55V, TEST1,2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=-1.55V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=-1.55V, I_{OL}=0.4uA, SEGOUT		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=-1.55V, I_{OH}=-4uA, COM1-2	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS1}=-1.55V, I_{OH}=-4uA, I_{OL}=4uA, COM1-2	V_{SS1}-0.2	V_{SS1}+0.2		V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=-1.55V, I_{OL}=4uA, COM1-2		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=-1.35V, I_{OH}=-250uA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250uA, ALM, LIGHT, CNT1, CNT2		V_{SS1}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)		V_{SS1}+0.2		V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1uF, f_{opg}=32.768kHz, Fig.2			-2.5	V
Current Dissipation	$\|I_{DD}\|$	V_{SS1}=-1.55V, standard watch / clock operation, C1=C2=0.1uF, Co=Cg=20pF, CI=25kohm, Fig. 2		2.0		uA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kohm, Fig. 3	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, CI=25kohm, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	V_{SS1}=-1.55V, Co=Cg=20pF, CI=25kohm, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Li Battery [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at T_a=25±2°C, V_{DD}=0V				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}-0.3 to 0.3	V
	V_{IN2}	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4 : Input mode)	V_{SS2}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{BAK}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1-2, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4 : Output mode)	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4,K1-4,M1-4,P1-4,INT,RES (M1-4,P1-4 : Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	T_a=-20 to +65 °C	32		33	kHz

Electrical Characteristics at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr.,*1,Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V,"L"-Level pull-in tr.,*1,Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, input mode ,"L"-Level hold tr.,*2,Fig. 4	50		500	kohm
Input Resistance	R_{IN2B}	V_{SS2}=-2.9V,input mode,"L"-level pull-in tr.,*2,Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4uA,SEGOUT		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4uA,COM1-2	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=-2.9V, I_{OH}=-4uA, I_{OL}=4uA COM1-2	V_{SS2}/2-0.2	V_{SS2}/2+0.2		V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4uA,COM1-2		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250uA, ALM,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250uA, ALM,CNT1,CNT2		V_{SS2}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.4V, I_{OH}=-150uA,LIGHT	-1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.4V, I_{OL}=150uA,LIGHT		V_{SS2}+1.5		V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=-2.9V, I_{OH}=-40uA,M1-4, P1-4 (M1-4,P1-4:Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=-2.9V, I_{OL}=40uA,M1-4, P1-4 (M1-4,P1-4:Output mode)		V_{SS2}+0.4		V
Output Voltage (Halver)	V_{SS1}	V_{SS2}=-2.9V,C1=C2=0.1uF, f_{opg}=32.768kHz,Fig. 5			-1.35	V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V,standard watch/clock operation,C1=C2=0.1uF, C_o=Cg=20pF,CI=25kohm,Fig. 5		1.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}≅V_{SS2}, C_o=Cg=20pF, CI=25kohm,Fig. 6	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}=V_{SS2}/2, Co=Cg= 20pF,CI=25kohm,Fig. 5			-2.6	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=-2.9V, C_o=Cg=20pF, CI=25kohm,Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [1/2 bias,1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C,V_{DD}=0V				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	1OP,OSCIN,TEST3	V_{SS1}-0.3 to 0.3	V
	V_{IN2}	S1-4,M1-4,K1-4,P1-4,TEST1, TEST2,INT,RES (M1-4,P1-4: Input mode)	V_{SS2}-0.3 to 0.3	V
Maximu Output Voltage	V_{OUT1}	TEST3,CUP2,OSCOUT	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT,COM1-2,CUP1,ALARM, LIGHT,CNT1,CNT2,M1-4,P1-4 (M1-4,P1-4:Output mode)	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C,V_{DD}=0V			min	typ	max	unit
Supply Voltage	V_{SS1}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,P1-4,INT, RES (M1-4,PL-4: Input Mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	Ta=-20 to 65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C,V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr.,*1,Fig.4	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V,"L"-Level pull-in tr.,*1,Fig.4	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.4, input mode,"L"-Level hold tr., *2, Fig.4	50		500	kohm
	R_{IN2B}	V_{SS2}=-2.9V,input mode, "L"-Level pull-in tr.,*2,Fig.4	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2 RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V,I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V,I_{OL}=0.4uA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V,I_{OH}=-4uA, COM1-2	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=-2.9V,I_{OH}=-4uA, I_{OL}=4uA,COM1-2	V_{SS2}/2-0.2		V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V,I_{OL}=4uA, COM1-2			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V,I_{OH}=-250uA, ALM,LIGHT,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V,I_{OL}=250uA, ALM,LIGHT,CNT1,CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V,I_{OH}=-40uA M1-4,P1-4 (M1-4,P1-4 :Output mode)	-0.4			V
"L"-Level Output	V_{OL4}	V_{SS2}=-2.9V,I_{OL}=40uA, M1-4,P1-4 (M1-4,P1-4 :Output mode)			V_{SS2}+0.4	V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V,C1=C2=0.1uF, f_{opg}=32.768KHz,Fig.5			-1.35	V

			min	typ	max	unit
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V,standard watch/ clock operation,C_1=C_2=0.1uF, C_o=C_g=20pF,CI=25kohm,Fig.5		5.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2},C_o=C_g=20pF, CI=25kohm,Fig.6	-2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS2},C_o=C_g=20pF, CI=25kohm,Fig.5			-2.0	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=-2.9V,C_o=C_g=20pF, CI=25kohm,Fig.6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Ag Battery [1/2 bias,1/3 duty]

Absolute Maximum Ratings at T_a=25±2°C,V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1-4,M1-4,K1-4,P1-4,TEST1-3, 10P,OSCIN,INT,RES (M1-4, P1-4 : Input mode)	V_{SS1}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,CUP2,OSCOUT,ALARM, LIGHT,CNT1,CNT2,M1-4,P1-4 (M1-4,P1-4 : Output mode)	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT,COM1-3,CUP1	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at T_a=25±2°C,V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.3		-2.4	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,P1-4,INT,RES (M1-4,P1-4 : Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	f_{opg}	T_a=-20 to +65 °C	32		33	kHz

Electrical Characteristics at T_a=25±2°C,V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=-1.55V,V_{IL}=V_{SS1}+0.2V, "L"-level hold tr.,*1,Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS1}=-1.55V,"L"-level pull-in tr.,*1,Fig. 1	200		2000	kohm
	R_{IN2A}	V_{SS1}=-1.55V,V_{IL}=V_{SS1}+0.2V, input mode,"L"-level hold tr., *2,Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS1}=-1.55V,input mode,"L"-level hold tr.,*2,Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS1}=-1.55V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=-1.55V,I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=-1.55V,I_{OL}=0.4uA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=-1.55V,I_{OH}=-4uA, COM1-3	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS1}=-1.55V,I_{OH}=-4uA, I_{OL}=4uA,COM1-3	V_{SS1}-0.2		V_{SS1}+0.2	V

			min	typ	max	unit
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=-1.55V, I_{OL}=4uA, COM1-3		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=-1.35V, I_{OH}=-250uA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250uA, ALM, LIGHT, CNT1, CNT2		V_{SS1}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)		V_{SS1}+0.2		V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1uF, f_{opg}=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	$\|I_{DD}\|$	V_{SS1}=-1.55V, standard watch / clock operation, C1=C2=0.1uF, Co=Cg=20pF, CI=25kohm, Fig. 2		2.0		uA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kohm, Fig. 3	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, CI=25kohm, Fig. 3	-1.65		-1.30	V
Oscillation Start Time	tstt	V_{SS1}=-1.35V, Co=Cg=20pF, CI=25kohm, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Li Battery [1/2 bias, 1/3 duty]

Absolute Maximum Ratings at T_a=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}-0.3 to 0.3	V
	V_{IN2}	S1-4, M1-4, K1-4, P1-4, TEST1, TEST2, INT, RES (M1-4, P1-4 : Input mode)	V_{SS2}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{BAK}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1-3, CUP1, ALARM, LIGHT, CNT1, CNT2, M1-4, P1-4 (M1-4, P1-4 : Output mode)	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at T_a=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4, K1-4, M1-4, P1-4, INT, RES (M1-4, P1-4 : Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	T_a=-20 to +65 °C	32		33	kHz

Electrical Characteristics at T_a=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-Level hold tr., *2, Fig. 4	50		500	kohm

			min	typ	max	unit
Input Resistance	R_{IN2B}	V_{SS2}=-2.9V,input mode,"L"-level pull-in tr.,*2,Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V,I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V,I_{OL}=0.4uA,SEGOUT		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V,I_{OH}=-4uA,COM1-3	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=-2.9V,I_{OH}=-4uA, I_{OL}=4uA COM1-3	V_{SS2}/2-0.2	V_{SS2}/2+0.2		V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V,I_{OL}=4uA,COM1-3		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V,I_{OH}=-250uA, ALM,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V,I_{OL}=250uA, ALM,CNT1,CNT2		V_{SS2}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.4V,I_{OH}=-150uA,LIGHT	-1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.4V,I_{OL}=150uA,LIGHT		V_{SS2}+1.5		V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=-2.9V,I_{OH}=-40uA,M1-4, P1-4 (M1-4,P1-4:Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=-2.9V,I_{OH}=40uA,M1-4, P1-4 (M1-4,P1-4:Output mode)		V_{SS2}+0.4		V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V,C1=C2=0.1uF, f_{opg}=32.768kHz			-1.35	V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V,standard watch/clock operation,C1=C2=0.1uF, C_o=Cg=20pF,CI=25kohm,Fig. 5		1.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2},C_o=Cg=20pF, CI=25kohm,Fig. 6	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}=V_{SS2}/2,Co=Cg= 20pF,CI=25kohm,Fig. 5			-2.6	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=-2.9V,C_o=Cg=20pF, CI=25kohm,Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV (1/2 bias,1/3 duty)

Absolute Maximum Ratings at Ta=25±2°C,V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P,OSCIN,TEST3	V_{SS1}-0.3 to 0.3	V
	V_{IN2}	S1-4,M1-4,K1-4,P1-4,TEST1, TEST2,INT,RES (M1-4,P1-4:Input mode)	V_{SS2}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,CUP2,OSCOUT	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT,COM1-3,CUP1,ALARM, LIGHT,CNT1,CNT2,M1-4,P1-4 (M1-4,P1-4:Output mode)	V_{SS2}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to 65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C,V_{DD}=0V

			min	typ	max	
Supply Voltage	V_{SS1}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,P1-4,INT,RES (M1-4,P1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25± 2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr.,*1,Fig.4	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V,"L"-Level pull-in tr.,*1,Fig.4	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-Level hold tr., *1,Fig.4	50		500	kohm
	R_{IN2B}	V_{SS2}=-2.9V, input mode, "L"-Level tr.,*2,Fig.4	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4uA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4uA, COM1-3	-0.2			V
"M"-Level Output	V_{OM}	V_{SS2}=-2.9V, I_{OH}=-4uA, I_{OL}=4uA, COM1-3	V_{SS2}/2-0.2		V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4uA, COM1-3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250uA, ALM,LIGHT,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250uA ALM,LIGHT,CNT1,CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V, I_{OH}=-40uA, M1-4,P1-4 (M1-4,P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.9V, I_{OL}=40uA, M1-4,P1-4 (M1-4,P1-4:Output mode)			V_{SS2}+0.4	V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V, C1=C2=0.1uF, f_{opg}=32.768KHz)			-1.35	V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V,Standard watch/clock operation,C1=C2=0.1uF, Co=Cg=20pF,CI=25kohm,Fig.5		5.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2},Co=Cg=20pF, CI=25kohm,Fig.6	-2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS2},Co=Cg=20pF, CI=25kohm,Fig.6			-2.0	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=-2.9V,Co=Cg=20pF, CI=25kohm,Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Ag Battery [1/3 bias,1/3 duty]

Absolute Maximum Ratings at T_a=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to +0.3	V
	V_{SS2}		-4.0 to +0.3	V
	V_{SS3}		-5.5 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1-4,M1-4,K1-4,P1-4, TEST1-3,10P,OSCIN,INT,RES (M1-4,P1-4 : Input mode)	V_{SS1}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,CUP2,OSCOUT,ALARM, LIGHT,CNT1,CNT2,M1-4,P1-4 (M1-4,P1-4 : Output mode)	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	SEGOUT,COM1,COM2,COM3,CUP1	V_{SS3}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}		-3.3		-2.4	V
	V_{SS3}		-4.95		-3.7	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, K1-4, P1-4, INT, RES (M1-4, P1-4 : Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	f_{opg}	Ta=-20 to +65°C	32		33	kHz

Electrical Characteristics at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, "L"-Level hold tr., *1, Fig. 7	50		500	kohm
	R_{IN1B}	V_{SS1}=-1.55V, "L"-Level pull-in tr., *1, Fig. 7	200		2000	kohm
	R_{IN2A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, input mode, "L"-Level hold tr., *2, Fig. 7	50		500	kohm
	R_{IN2B}	V_{SS1}=-1.55V, input mode, "L"-Level pull-in tr., *2, Fig. 7	200		2000	kohm
	R_{IN3}	V_{SS1}=-1.55V, TEST1,2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=-1.55V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	V_{OM1-1}	V_{SS1}=-1.55V, I_{OH}=-0.4uA, I_{OL}=0.4uA, SEGOUT	V_{SS1}-0.2		V_{SS1}+0.2	V
"M2"-Level Output Voltage	V_{OM2-1}	" "	V_{SS2}-0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=-1.55V, I_{OL}=-0.4uA, SEGOUT	V_{SS3}-0.2		V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=-1.55V, I_{OH}=-4uA, COM1, COM2, COM3	-0.2			V
"M1"-Level Output Voltage	V_{OM1-2}	V_{SS1}=-1.55V, I_{OL}=4uA, I_{OH}=-4uA, COM1, COM2, COM3	V_{SS1}-0.2		V_{SS1}+0.2	V
"M2"-Level Output Voltage	V_{OM2-2}	" "	V_{SS2}-0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=-1.55V, I_{OL}=4uA, COM1-3			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=-1.35V, I_{OH}=-250uA, ALM, LIGHT, CNT1, CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250uA, ALM, LIGHT, CNT1, CNT2			V_{SS1}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20uA, M1-4, P1-4 (M1-4, P1-4 : Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20uA, M1-4, P1-4 : Output mode)			V_{SS1}+0.2	V
Output Voltage	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1uF, f_{opg}=32.768kHz, Fig.8			-2.5	V
	V_{SS3}	" "			-3.75	V
Current Dissipation	I_{DD}	V_{SS1}=-1.55V, standard watch/clock operation, C1 to C3= 0.1uF, C_o=Cg=20pF, CI=25kohm, Fig. 8		3.5		uA
Oscillation Start Voltage	V_{stt}	C_o=Cg=20pF, CI=25kohm, Fig. 9	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, CI=25kohm, Fig. 8	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	V_{SS1}=-1.35V, C_o=Cg=20pF, CI=25kohm, Fig. 9			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operating from Li Battery [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at T_a=25±2°C, V_{DD}=0V				unit
Maximum Supply Voltage	V_{SS1}	VBAK=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
	V_{SS2}	VBAK=V_{SS1} or V_{SS2}	-4.0 to +0.3	V
	V_{SS3}	VBAK=V_{SS1} or V_{SS2}	-5.5 to 0.3	V
Maximum Input Voltage	V_{IN1}	10P,OSCIN,TEST3	VBAK-0.3 to 0.3	V
	V_{IN2}	S1-4,M1-4,K1-4,P1-4,TEST1, TEST2,INT,RES (M1-4,P1-4 : Input mode)	V_{SS2}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,OSCOUT	VBAK-0.3 to 0.3	V
	V_{OUT2}	ALARM,LIGHT,CNT1,CNT2,M1-4, P1-4,CUP2(M1-4,P1-4:Output mode)	V_{SS2}-0.3 to 0.3	V
	V_{OUT3}	SEGOUT 1-64,COM1 to COM3, CUP1	V_{SS3}-0.3 to 0.3	V
Operating Temperature	Topg		-20 to +65	°C
Storage Temperature	Tstg		-30 to +125	°C

Allowable Operating Ranges at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Supply Voltage	VBAK		-3.6		-1.3	V
	V_{SS2}		-3.6		-2.0	V
	V_{SS3}	V_{SS3}≅V_{SS2}+V_{SS1}	-5.0		-3.9	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,P1-4,INT, RES (M1-4,P1-4 : Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=-20 to +65 °C	32		33	kHz

Electrical Characteristics at T_a=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr.,*1,Fig. 10	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V,"L"-Level pull-in tr.,*1 ,Fig. 10	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.4V, input mode,"L"-Level hold tr., *2,Fig. 10	50		500	kohm
	R_{IN2B}	V_{SS2}=-2.9V,input mode,"L"-Level pull-in tr., *2 ,Fig. 10	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2,RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V,I_{OH}=-0.4uA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	V_{OM1-1}	(V_{SS2}=-2.9V,I_{OH}=-0.4uA, I_{OL}=0.4uA,SEGOUT)	1/2V_{SS2}-0.2		1/2V_{SS2}+0.2	V
"M2"-Level Output Voltage	V_{OM2-1}	(" ")	V_{SS2}-0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V,I_{OL}=0.4uA, SEGOUT			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V,I_{OH}=-4uA,COM1-3	-0.2			V
"M1"-Level Output Voltage	V_{OM1-2}	(V_{SS2}=-2.9V,I_{OH}=-4uA I_{OL}=4uA,COM1,COM2,COM3)	1/2V_{SS2}-0.2		1/2V_{SS2}+0.2	V
"M2"-Level Output Voltage	V_{OM2-2}	(" ")	V_{SS2}-0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V,I_{OL}=4uA,COM1-3			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V,I_{OH}=-250uA, ALM,CNT1,CNT2		-0.65		V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V,I_{OL}=250uA, ALM,CNT1,CNT2			V_{SS}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.4V,I_{OH}=-150uA,LIGHT	-1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.4V,I_{OL}=150uA,LIGHT			V_{SS2}+1.5	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=-2.9V,I_{OH}=-40uA, M1-4,P1-4 (M1-4,P1-4 : Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL5}	" ,I_{OL}=40uA,			V_{SS2}+0.4	V

			min	typ	max	unit
Output Voltage	V_{SS1}	V_{SS2}=-2.9V,C1 to C4=0.1uF, fopg=32.768kHz, Fig.11			-1.35	V
	V_{SS3}	" "			-4.1	V
Current Dissipation	I_{DD}	V_{SS2}=-2.9V,standard watch/clock operation,C1 to C4=0.1uF,C_O=Cg=20pF,CI=25kohm, Fig. 11		2.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2},Co=Cg=20pF, CI=25kohm,Fig. 12	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}=V_{SS2}/2,Co=Cg=20pF,CI=25kohm,Fig. 11			-2.6	V
Oscillation Start Time	t_{stt}	V_{SS2}=-2.9V,V_{SS1}=V_{SS2},C_O=Cg=20pF,CI=25kohm,Fig. 12			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [1/3 bias,1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C,V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0 to 0.3	V
	V_{SS2}		-4.0 to +0.3	V
	V_{SS3}		-5.5 to 0.3	V
Maximum Input Voltage	V_{IN1}	10P,OSCIN,TEST3	V_{SS1}-0.3 to 0.3	V
	V_{IN2}	S1-4,M1-4,K1-4,P1-4,TEST1,2,INT,RES (M1-4,P1-4: Input mode)	V_{SS1}-0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3,OSCOUT	V_{SS1}-0.3 to 0.3	V
	V_{OUT2}	ALRM,LIGHT,CNT1,CNT2, M1-4,P1-4,CUP2 (M1-4,P1-4: Output mode)	V_{SS2}-0.3 to 0.3	V
	V_{OUT3}	SEGOUT 1-64,COM1 to COM3, CUP1	V_{SS3}-0.3 to 0.3	V
Operating Temperature	T_{opg}		-20 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C,V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-3.6		-1.3	V
	V_{SS2}		-3.6		-2.0	V
	V_{SS3}	V_{SS3}=V_{SS2}+V_{SS1}	-5.0		-3.9	V
"H"-Level Input Voltage	V_{IH}	S1-4,M1-4,K1-4,INT,RES (M1-4,P1-4: Input Mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	Ta=-20 to +65 °C	32		33	kHz

Electrical Characteristics at Ta=25±2°C,V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr.,*1,Fig.10	50		500	kohm
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig.10	200		2000	kohm
	R_{IN2A}	V_{SS2}=-2.9V,V_{IL}=V_{SS2}+0.4V, input mode, "L"-Level hold tr., *2,Fig.10	50		500	kohm
	R_{IN2B}	V_{SS}=-2.9V, input mode,"L"-Level pull-in tr.,*2,Fig. 10	200		2000	kohm
	R_{IN3}	V_{SS2}=-2.9V,TEST1,2,RES	10		300	kohm

			min	typ	max	unit
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4uA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	V_{OM1-1}	(V_{SS2}=-2.9V, I_{OH}=-0.4uA, I_{OL}=0.4uA, SEGOUT)	1/2V_{SS2}-0.2	1/2V_{SS2}+0.2		V
"M2"-Level Output Voltage	V_{OM2-1}	(V_{SS2}=-2.9V, I_{OH}=-0.4uA, I_{OL}=0.4uA, SEGOUT)	V_{SS2}-0.2	V_{SS2}+0.2		V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4uA, SEGOUT		V_{SS3}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4uA, COM1,COM2,COM3	-0.2			V
"M1"-Level Output Voltage	V_{OM1-2}	(V_{SS2}=-2.9V, I_{OH}=-4uA, I_{OL}=4uA, COM1,COM2,COM3)	1/2V_{SS2}-0.2	1/2V_{SS2}+0.2		V
"M2"-Level Output Voltage	V_{OM2-2}	(V_{SS2}=-2.9V, I_{OH}=-4uA, I_{OL}=4uA, COM1,COM2,COM3)	V_{SS2}-0.2	V_{SS2}+0.2		V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4uA, COM1,COM2,COM3		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250uA, ALM,LIGHT,CNT1,CNT2	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250uA ALM,LIGHT,CNT1,CNT2		V_{SS2}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V, I_{OH}=-40uA, M1-4,P1-4 (M1-4,P1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.9V, I_{OL}=40uA, M1-4,P1-4 (M1-4,P1-4 : Output mode)		V_{SS2}+0.4		V
Output Voltage	V_{SS1}	(V_{SS2}=-2.9V, C1 to C4=0.1uF, 0.1uF, fopg=32.768KHz, Fig.11)			-1.35	V
	V_{SS3}				-4.1	V
Current Dissipation	I_{DD}	V_{SS2}=-2.9V, standard watch/clock operation, C_1 to C4=0.1uF, Co=Cg=20pF, CI=25kohm, Fig.11		5.0		uA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kohm, Fig. 12	-2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS2}, Co=Cg=20pF, CI=25kohm, Fig.11			-2.0	V
Oscillation Start Time	t_{stt}	V_{SS2}=-2.9V, V_{SS1}=V_{SS2}, Co=Cg =20pF, CI=25kohm, Fig.12			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

*1 S1·S2·S3·S4·INT·K1·K2·K3·K4
*2 M1·M2·M3·M4·P1·P2·P3·P4

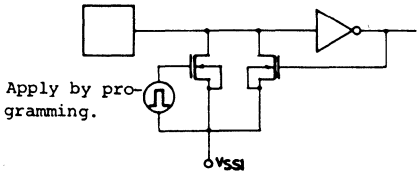


Fig. 1 Input configuration of S1-4,M1-4,K1-4,P1-4,INT

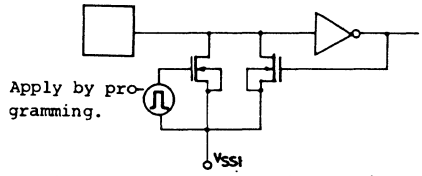


Fig. 7 Input configuration of S1-4, M1-4,K1-4,P1-4,INT

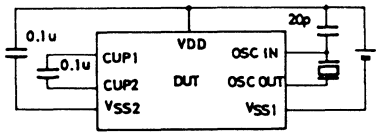


Fig. 2 Current dissipation, oscillation hold voltage test circuit

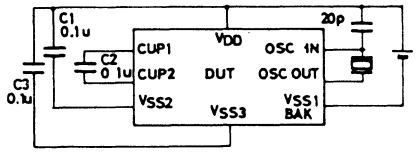


Fig. 8 Current dissipation, oscillation hold voltage test circuit

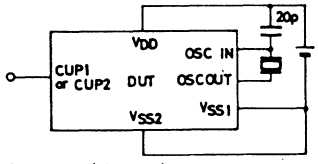


Fig. 3 Oscillation start voltage, oscillation start time, frequency stability test circuit

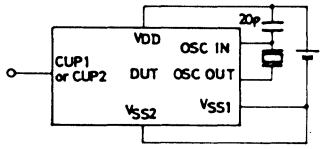


Fig. 9 Oscillation start voltage, oscillation start time, frequency stability test circuit

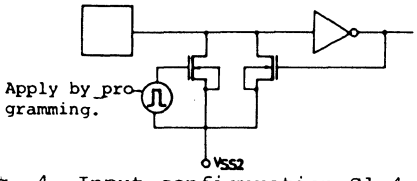


Fig. 4 Input configuration S1-4, M1-4,K1-4,P1-4,INT

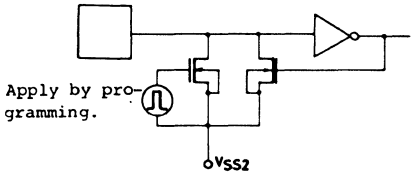


Fig. 10 Input configuration of S1-4, M1-4,K1-4,P1-4,INT

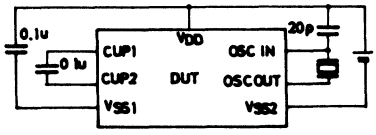


Fig. 5 Current dissipation, oscil lation hold voltage test circuit

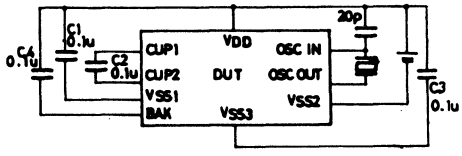


Fig. 11 Current dissipation, oscillation hold voltage test circuit

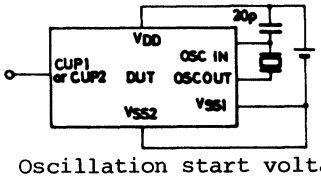


Fig. 6 Oscillation start voltage, oscillation start time, frequency stability test circuit

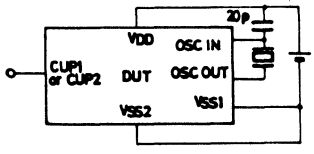


Fig. 12 Oscillation start voltage, oscillation start time frequency stability test circuit

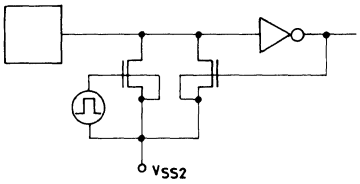


Fig. 13 Input configuration S1-4, M1-4,K1-4,P1-4,INT

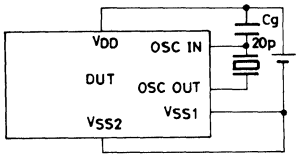


Fig. 14 Current dissipation, oscillation hold voltage test circuit

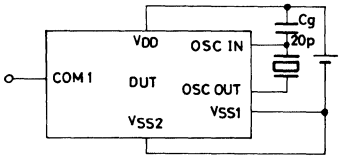


Fig. 15 Oscillation start voltage, oscillation start time, frequency stability test circuit

Summary of LC5800 Instructions

Notations

AC	: Accumulator	HQF	: Halt request flag
ACn	: Accumulator·bit n	HEFn	: Halt release enable flag
CF	: Carry flag	HRFn	: Halt release request flag
DP	: Data pointer	CC	: Chrono counter
DPF	: Data pointer flag	LSF	: Lap sample flag
SP	: Strobe pointer	LPF	: Lap mode flag
PC	: Program counter	CSTF	: Chrono start flag
[P( )]	: Contents of port ( )	CMF	: Chrono mode flag
Rx	: Memory of address x	CDF	: Chrono data decoder flag
Rxn	: Memory·bit n of address x	TM	: Timer
IEFn	: Interrupt enable flag n	L	: LCD latch
WRFn	: Working register n	( )	: Contents
E/S F	: Interrupt/switch select flag	←	: Transfer direction, result
BCF	: Bakup flag	∧	: AND
SCFn	: Start condition flag n	∨	: OR
PDF	: Pull down flag	∀	: Exclusive OR

Instruction	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Accumulator manipulation instructions·memory manipulation instructions	CLA	Clear AC	0 1 0 1 1 0 1 0 0 0 0 0 0 0 0 0	AC ← 0	The AC contents are cleared.	
	RCF	Reset CF	1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 1	CF ← 0 ≡RF1 1	The CF contents are cleared.	CF
	SCF	Set CF	1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 1	CF ← 1 ≡SF1 1	The CF is set.	CF
	MRW Y, X	Move Rx to Working Register R_Y	0 1 1 0 0 0 Y_2 Y_1 Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, R_Y ← (Rx)	The memory (Rx) contents are loaded to the AC and working register (Ry).	
	MWR X, Y	Move Working Register R_Y to R_X	0 1 1 0 0 1 Y_2 Y_1 Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (R_Y)	The working register (Ry) contents are loaded to the AC and memory (Rx).	
	SR0 X	Shift Right Rx & MSB=0	0 1 1 0 1 0 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn+1) Rx_3, AC_3 ← 0	The memory (Rx) contents are shifted right and 0 is loaded to the MSB. The same contents are loaded to the AC.	
	SR1 X	Shift Right Rx & MSB=1	0 1 1 0 1 0 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, AC_n ← (Rxn+1) Rx_3, AC_3 ← 1	The memory (Rx) contents are shifted right and 1 is loaded to the MSB. The same contents are loaded to the AC.	
	SL0 X	Shift Left Rx & LSB=0	0 1 1 0 1 0 1 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn−1) Rx_0, AC_0 ← 0	The memory (Rx) contents are shifted left and 0 is loaded to the LSB. The same contents are loaded to the AC.	
	SL1 X	Shift Left Rx & LSB=1	0 1 1 0 1 0 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn−1) Rx_0, AC_0 ← 1	The memory (Rx) contents are shifted left and 1 is loaded to the LSB. The same contents are loaded to the AC.	
	RAR X	Rotate Right Rx	0 1 1 0 1 1 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn+1) Rx_3, AC_3 ← Rx_0	The memory (Rx) contents are rotated right. The same contents are loaded to the AC.	
	RAL X	Rotate Left Rx	0 1 1 0 1 1 1 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn−1) Rx_0, AC_0 ← Rx_3	The memory (Rx) contents are rotated left. The same contents are loaded to the AC.	
	MAF X	Move CF & WRF to AC & Rx	0 1 1 1 0 1 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (CF, WRF)	The CF, WRF contents are loaded to the AC and memory (Rx). AC, Rx bit: 3 — Contents: CF; 2; 1 — WRF2; 0 — WRF1	
	MRA X	Move Rx to CF & WRF	0 0 0 0 1 1 1 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	CF, WRF ← (Rx)	The memory (Rx) contents are loaded to the CF and WRF. Bit has the same correspondence as for MAF X.	
Operation instructions	ADC X	Add AC to Rx with CF	0 1 0 0 0 0 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+(AC) +(CF)	The memory (Rx), AC, CF contents are binary-added and the result is loaded to the AC.	CF
	ADC* X	Add AC to Rx with CF	0 1 0 0 0 0 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+(AC) +(CF)	The memory (Rx), AC, CF contents are binary-added and the result is loaded to the AC, Rx.	CF
	SBCX	Subtract AC from Rx with CF	0 1 0 0 0 0 1 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, ← (Rx)+($\overline{AC}$) +(CF)	The memory (Rx) contents are binary-subtracted by the AC, CF contents and the result is loaded to the AC.	CF
	SBC* X	Subtract AC from Rx with CF	0 1 0 0 0 0 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+($\overline{AC}$) +(CF)	The memory (Rx) contents are binary-subtracted by the AC, CF contents and the result is loaded to the AC, Rx.	CF

Instruction	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Operation instructions	ADD X	Add AC to Rx	0 1 0 0 0 1 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC.	CF
	ADD* X	Add AC to Rx	0 1 0 0 0 1 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC, Rx.	CF
	SUB X	Subtract AC from Rx	0 1 0 0 0 1 1 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+($\overline{AC}$)+1	The memory (Rx) contents are binary-subtracted by the AC contents and the result is loaded to the AC.	CF
	SUB* X	Subract AC from Rx	0 1 0 0 0 1 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+($\overline{AC}$)+1	The memory (Rx) contents are binary-subtracted by the AC contents and the result is loaded to the AC, Rx.	CF
	ADN X	Add AC to Rx	0 1 0 0 1 0 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC.	
	ADN* X	Add AC to Rx	0 1 0 0 1 0 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC, Rx.	
	AND X	And AC to Rx	0 1 0 0 1 0 1 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)∧(AC)	The memory (Rx) contents and AC contents are ANDed and the result is loaded to the AC.	
	AND* X	And AC to Rx	0 1 0 0 1 0 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∧(AC)	The memory (Rx) contents and AC contents are ANDed and the result is loaded to the AC, Rx.	
	EOR X	Exclusive or AC to Rx	0 1 0 0 1 1 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)∀(AC)	The memory (Rx), AC contents are exclusive-ORed and the result is loaded to the AC.	
	EOR* X	Exclusive or AC to Rx	0 1 0 0 1 1 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∀(AC)	The memory (Rx), AC contents are exclusive-ORed and the result is loaded to the AC, Rx.	
	OR X	OR AC to Rx	0 1 0 0 1 1 1 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)V(AC)	The memory (Rx), AC contents are ORed and the result is loaded to the AC.	
	OR* X	OR AC to Rx	0 1 0 0 1 1 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)V(AC)	The memory (Rx), AC contents are ORed and the result is loaded to the AC, Rx.	
	ADCI X, Y	Add Immediate date to Rx with CF	0 1 0 1 0 0 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)+Y+(CF)	The memory (Rx) contents, Y, CF contents are binary-added and the result is loaded to the AC. The relation between absolute address of data memory (Rx) and X is as follows: Absolute address=XH+70H	CF
	ADCI* X, Y	Add Immediate data to Rx with CF	0 1 0 1 0 0 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+Y+(CF)	The memory (Rx) contents, Y are binary-added and the result is loaded to the AC, Rx.	CF
	SBCI X, Y	Subtract Immediate date & CF from Rx	0 1 0 1 0 0 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)+$\overline{Y}$+(CF)	The memory (Rx) contents are binary-subtracted by Y, CF contents and the result is loaded to the AC.	CF
	SBCI* X, Y	Subtract Immediate data & CF from Rx	0 1 0 1 0 0 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+$\overline{Y}$+(CF)	The memory (Rx) contents are binary-subtracted by Y, CF contents and the result is loaded to the AC, Rx.	CF
	ADDI X, Y	Add Immediate data to Rx	0 1 0 1 0 1 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC.	CF
	ADDI* X, Y	Add Immediate data to Rx	0 1 0 1 0 1 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC, Rx.	CF
	SUBI X, Y	Subtract Immediate data from Rx	0 1 0 1 0 1 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)+$\overline{Y}$+1	The memory (Rx) contents are binary-subtracted by Y and the result is loaded to the AC.	CF
	SUBI* X, Y	Subtract Immediate data from Rx	0 1 0 1 0 1 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+$\overline{Y}$+1	The memory (Rx) contents are binary-subtracted by Y and the result is loaded to the AC, Rx.	CF
	ADNI X, Y	Add Immediate data to Rx	0 1 0 1 1 0 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC.	
	ADNI* X, Y	Add Immediate data to Rx	0 1 0 1 1 0 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC, Rx.	

Instruction	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Operation instructions	ANDI X, Y	And Immediate data to Rx	0 1 0 1 1 0 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)∧Y	The memory (Rx) contents and Y are ANDed and the result is loaded to the AC.	
	ANDI* X, Y	And Immediate data to Rx	0 1 0 1 1 0 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∧Y	The memory (Rx) contents and Y are ANDed and the result is loaded to the AC, Rx.	
	EORI X, Y	Exclusive Or Y to Rx	0 1 0 1 1 1 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)∀Y	The memory (Rx) contents and Y are exclusive-ORed and the result is loaded to the AC.	
	EORI* X, Y	Exclusive Or Y to Rx	0 1 0 1 1 1 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∀Y	The memory (Rx) contents and Y are exclusive-ORed and the result is loaded to the AC, Rx.	
	ORI X, Y	Or Immediate data to Rx	0 1 0 1 1 1 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)∨Y	The memory (Rx) contents and Y are ORed and the result is loaded to the AC.	
	ORI* X, Y	Or Immediate data to Rx	0 1 0 1 1 1 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∨Y	The memory (Rx) contents and Y are ORed and the result is loaded to the AC, Rx.	
Data pointer and flag manipulation instructions	MDPL X	Move DPL to Rx	0 1 1 1 0 1 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (DPL)	The DPL contents are loaded to the memory (Rx).	
	MDPH X	Move DPH to Rx	0 1 1 1 0 1 1 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (DPH)	The DPH contents are loaded to the AC and memory (Rx).	
	MRDH X	Move Rx to DPH	0 1 1 0 1 0 1 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	DPH, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and DPH. (If the DPF is set with X=00H to 6FH, the memory (Rx) contents are not loaded to the DPH.)	
	MRDL X	Move Rx to DPL	0 1 1 0 1 0 0 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	DPL, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and DPL. (If the DPF is set with X=00H to 6FH, the memory (Rx) contents are not loaded to the DPL.)	
	MRSB X	Move Strove Pointer	0 1 1 0 1 0 1 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	SP, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and SP.	
	SFI X	Set Flag 1 Group	1 1 1 0 1 0 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		The flag corresponding to the data specified with X9 to X0 is set.	CF DPF
				Data of X9 to X0 / Instruction to be executed	X_0=1: SCF; X_1=1: SCEX; X_2=1: SCT1; X_3=1: SFSP	
				Data of X9 to X0 / Instruction to be executed	X_4=1: SFPD; X_5=1: COMD1; X_6=1: COMD2; X_7=1: SDPF	
				X_8=1, X_9=1	Used for test.	
	RFI X	Reset Flag 1 Group	1 1 1 0 1 1 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		Each flag is reset corresponding to SF1.	CF DPF
	SF2 X	Set Flag 2 Group	1 1 1 1 0 0 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		The flag corresponding to the data specified with X9 to X0 is se-.	BCF CMF CDF PDF HQF
				Data of X9 to X0 / Instruction to be executed	X_0=1: SCHF 1; X_1=1: SCHF 2; X_2=1: SBAK; X_3=1: LON; X_4=1: LON SLQT	
				Data of X9 to X0 / Instruction to be executed.	X_5=1: SPDR 1; X_6=1: SPDR 2; X_7=1: SPDR 4; X_8=1: SPDR 8; X_9=1: SCT 2	
	RF2 X	Reset Flag 2 Group	1 1 1 1 0 1 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		Each flag is reset corresponding to SF2.	
	SDPF	Set DPF	1 1 1 0 1 0 0 0 1 0 0 0 0 0 0 0	DPF ← 1 ≡SF1 80H	The DPF is set. The memory address is specified with the DP. If the instruction code address is 70H to 7FH, the instruction code address prevails.	DPF
	RDPF	Reset DPF	1 1 1 0 1 1 0 0 1 0 0 0 0 0 0 0	DPF ← 0 ≡RF1 80H	The DPF is reset.	DPF

Instruction	Mnemonic		Instruction code	Function	Description	Status flag to be affected
Load/store instructions	STA X	Store AC to Rx	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 0 1 1 1 0 1 1 1 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx ← (AC)	The AC contents are loaded to the memory (Rx).	
	LDS X, D	Load AC with Data & Store AC to Rx	0 1 1 1 1 D_3 D_2 D_1 D_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← D	Immediate data D is loaded to the AC and memory (Rx).	
	LDA X	Load AC from Rx	0 1 1 0 1 0 0 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)	The memory (Rx) contents are loaded to the AC.	
CPU control instructions	HALT	HALT	1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0	The operation of CPU is stopped. The following 3 conditions cause the halt mode to be released. 1) An interrupt is accepted. 2) The signal change specified by the SSW instruction is applied to port S, K. 3) The halt release condition specified by the SIC instruction is met. When an interrupt is accepted to release the halt mode, the halt mode returns by executing the RTS instruction after completion of interrupt service.		
	SSW X	Set Switch State	1 1 1 0 0 0 0 0 0 0 X_5 X_4 X_3 X_2 X_1 X_0	The data specified by X causes the halt mode to be released. The signal change at port S, K is specified. $X_0 \sim X_5$ — Signal change at input port: X_0=1 → S_1; X_1=1 → S_2; X_2=1 → S_3; X_3=1 → S_4 $X_0 \sim X_5$ — Signal change at input port: X_4=1 Fall signal at one of K1 to K4; X_5=1 Rise signal at one of K1 to K4		
	SIC X	Set/Reset Interupt Enable Flag	1 1 1 1 1 0 1 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$X_0 \sim X_8$ — Operation X_0=1: The IEF3 is set so that interrupt 3 (overflow from the divider) is accepted. X_1=1: The IEF2 is set so that interrupt 2 (overflow from the CC) is accepted. X_2=1: The IEF1 is set so that interrupt 1 (underflow from the TM) is accepted. X_3=1: The IEF0 is set so that interrupt 0 (mode shown below) is accepted. 1) Signal change at port S specified by the SSW. 2) Signal change at port K specified by the SSW. 3) Rise signal change at external interrupt pin INT. Refer to the operation for X8=1 also. X_4=1: The HEF3 is set so that overflow from the divider causes the halt mode to be released. X_5=1: The HEF2 is set so that overflow from the CC causes the halt mode to be released. X_6=1: The HEF1 is set so that underflow from the TM causes the halt mode to be released. X_7=1: The HEF0 is set so that the halt mode is released when the rise signal change is applied to INT. In this case X_8 must be 0. X_8=1: For X3=1, port S/K is selected at X8=1 (E/SF set); INT is selected at X8=0 (E/SF reset). In the case of X_7=1, X_8 must be 1.		$IEF_{0\sim3}$ $HEF_{0\sim3}$ E/SF The IEF0 to 3 are reset automatically when an interrrupt is accepted.
	SIC* X		1 1 1 1 1 1 1 0 0 0 0 0 X_3 X_2 X_1 X_0	Only X0 to X3 of the SIC instruction are significant. X4 to X8 remain unaffected.		

Instruction	Mnemonic		Instruction code								Function	Description	Status flag to be affected
			D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
CPU control instructions	MSB X	Move SCF & BCF to AC & Rx	0	1	1	1	0	1	0	1	AC, Rx ← $SCF_{1\sim3}$ BCF	The SCF1 to 3 and BCF contents are loaded to the AC and memory (Rx).	
			1	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
											The AC contents and the meaning of bit after execution of this instruction are as follows: Bit 0 ---- BCF: "1" at the backup mode Bit 1 ---- SCF1: "1" when the halt mode is released by the signal change at port K Bit 2 ---- SCF2: "1" when the halt mode is released by the SCF4 to 7 Bit 3 ---- SCF3: "1" when the halt mode is released by the signal change at port S		
	MSC X	Move SCF to AC & Rx	0	1	1	1	0	1	1	0	AC, Rx←SCF4~7	The SCF4 to 7 contents are loaded to the AC and memory (Rx).	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
											The AC contents and the meaning of bit after execution of this instruction are as follows: Case where the corresponding bit is "1". Bit 0 ---- SCF4: The halt mode is released by overflow from the divider. Bit 1 ---- SCF5: The halt mode is released by overflow from the CC. Bit 2 ---- SCF6: The halt mode is released by underflow the TM. Bit 3 ---- SCF7: The halt mode is released by the signal change at INT.		
											The SIC instruction is used to specify that the INT/port S, K.TM, CC, divider should be specified for interrupt service, halt release, or no operation.		
	NOP	No Operation	0	0	0	0	0	0	0	0			
			0	0	0	0	0	0	0	0			
	LON	Light ON	1	1	1	1	0	0	0	0	Set Light & HQF	The Light Out pin is made active and the halt request flag (HRQ) is set to cause the halt mode to be entered.	HQF
			0	0	0	1	1	0	0	0	≡SF2 18H		
	LOFF	Light OFF	1	1	1	1	0	1	0	0	Reset Light & HQF	The Light Out pin is made nonactive and the HRQ is reset.	HQF
			0	0	0	1	1	0	0	0	≡RF2 18H		
	SBAK	Set Back-up Mode	1	1	1	1	0	0	0	0		V_{SS2} is applied to the logic unit at the Li battery power supply mode. The inverter size of the oscillator is approximately doubled at the Ag, Li battery, EXTV power supply mode.	BCF
			0	0	0	0	0	1	0	0	≡SF1 4		
	RBAK	Reset Back-up Mode	1	1	1	1	0	1	0	0		The backup mode is released.	BCF
			0	0	0	0	0	1	0	0	≡RF1 4		
Chrono Instructions	MCD X	Move Chrono Counter Data to AC & Rx	0	1	1	1	0	1	0	0	AC, Rx← (CC)	The CC contents are loaded to the AC and memory (Rx).	
			1	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	MCF X	Move Chrono Flag to AC & Rx	0	1	1	1	0	1	0	1	AC, Rx←CMF, CSTF	The contents of each flag are loaded to the AC and memory (Rx).	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
											The AC contents after execution of this instruction are as follows: Bit 0 ---- LSF: "1" at the CC overflow mode at LPF=1. Bit 1 ---- LPF: "1" at the lap mode. Bit 2 ---- CSTF: "1" at the chrono start mode. Bit 3 ---- CMF: "1" at the chrono mode.		
	CCC	Clear CC	1	1	1	1	1	1	0	0	CC←0		LSF
			0	0	1	0	0	0	1	0	LSF←0		
	RLP	Reset LPF	1	1	1	1	1	1	0	0	LPF←0	The lap mode is released.	LPF
			0	1	0	0	0	0	0	0			
	CSP	Chrono Stop	1	1	1	1	1	1	0	0	CSTF←0	1/100 second pulse is inhibited from being applied to the CC.	CSTF
			1	0	0	0	0	0	0	0			

Instruction	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Chrono Instructions	CST	Chrono Start	1 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0	≡PLC 100H	1/100 second pulse is applied to the CC.	
	SCEX	Set CC External Input Mode	1 1 1 0 1 0 0 0 0 0 0 0 0 0 1 0	≡SF1 2	The CC input connected to K4 pin, instead of 1/100 pulse. At the initial mode the CC input is connected to 1/100 pulse.	
	RCEX	Reset CC External Input Mode	1 1 1 0 1 1 0 0 0 0 0 0 0 0 1 0	≡RF1 2	The CC input is connected to 1/100 pulse.	
	SCHF X	Set Chrono Flag	1 1 1 1 0 0 0 0 0 0 0 0 0 0 X_1 X_0	CMF ← 1 (at X_0=1) CDF ← 1 (at X_1=1) ≡ One of SF2	The CMF and CDF are set. When the CMF is set, the chrono start/stop, lap/lap release mode can be controlled by the signal at port S or the dedicated instruction. When the CDF is set, the data decoder is connected to the CC.	CMF CDF At the initial mode the CMF and CDF are reset.
	RCHF X	Reset Chrono Flag	1 1 1 1 0 1 0 0 0 0 0 0 0 0 X_1 X_0	CMF ← 0 (at X_0=1) CDF ← 0 (at X_1=1) ≡ One of RF2	The CMF and CDF are reset.	CMF CDF
Input/output instructions	IPP X	Input Port P to AC & Rx	0 1 1 1 0 0 0 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(P)]	The input data at input/output port P is loaded to the AC and memory (Rx).	
	IPS X	Input Port S to AC & Rx	0 1 1 1 0 0 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(S)]	The input data at input port S is loaded to the AC and memory (Rx).	
	IPM X	Input Port M to AC & Rx	0 1 1 1 0 0 0 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(M)]	The input data at input/output port M is loaded to the AC and memory (Rx).	
	IPK X	Input Port K to AC & Rx	0 1 1 1 0 0 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(K)]	The input data at input port K is loaded to the AC and memory (Rx).	
	OPP X	Output Rx to Port P	0 0 0 0 0 0 0 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	[P(P)] ← Rx	The memory (Rx) contents are loaded to input/output port P.	
	OPM X	Output Rx to Port M	0 0 0 0 1 1 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	[P(M)] ← Rx	The memory (Rx) contents are loaded to input/output port M.	
	SCT1	Set CNT OUT 1	1 1 1 0 1 0 0 0 0 0 0 0 0 1 0 0	≡SF1 4	The CNT1 OUT pin is made active (ON).	
	RCT1	Reset CNT OUT 1	1 1 1 0 1 1 0 0 0 0 0 0 0 1 0 0	≡RF1 4	The CNT1 OUT pin is made nonactive (OFF).	
	SCT2	Set CNT OUT 2	1 1 1 1 0 0 1 0 0 0 0 0 0 0 0 0	≡SF2 200H	The CNT2 OUT pin is made active (ON).	
	RCT2	Reset CNT OUT 2	1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0	≡RF2 200H	The CNT2 OUT pin is made nonactive (OFF).	
	SLGT	Set Light	1 1 1 1 0 0 0 0 0 0 0 1 0 0 0 0	≡SF2 10H	The LIGHT OUT pin is made active (ON). (Refer to the LON instruction.)	
	RLGT	Reset Light	1 1 1 1 0 1 0 0 0 0 0 1 0 0 0 0	≡RF2 10H	The LIGHT OUT pin is made nonactive (OFF). (Refer to the LOFF instruction.)	
	SAS X	Set Alarm Sound	1 1 1 1 1 0 0 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	The waveform specified by X_8 to X_0 is delivered at the Alarm Out pin. $X_7 \sim X_0$ | X_0=1 | X_1=1 | X_2=1 | X_3=1 | X_4=1 Enable Signal | 32Hz | 16Hz | 8Hz | 4Hz | 2Hz $X_7 \sim X_0$ | X_5=1 | $\overline{X_6}\overline{X_7}$=1 | $\overline{X_6}X_7$=1 | $X_6\overline{X_7}$=1 | X_6X_7=1 Enable Signal | 1Hz | 1kHz | 2kHz | 4kHz | DC At X_8=1 the signal specified by X_6, X_7 is enabled.	

Instruction	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Input/output instructions	RAS	Reset Alarm Sound	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	≡SAS 0	The Alarm Out pin is made nonactive (OFF).	
	COMD X	Change to Output Mode	1 1 1 0 1 0 0 0 0 X_1 X_0 0 0 0 0 0	≡One of SF1	Input/output port M or P is changed to the output mode. At the initial mode the port is in the input mode. X=1, X=2, X=3 correspond to port M, port P, port M, P respectively.	
	CIMD X	Change to Input Mode	1 1 1 0 1 1 0 0 0 X_1 X_0 0 0 0 0 0	≡ One of RF1	Input/output port M or P is changed to input port.	
	SPDF X	Set PDF	1 1 1 1 0 0 0 X_3 X_2 X_1 X_0 0 0 0 0 0	PDF ← 1 ≡One of SF2 $X_0 \sim X_3$ / Corresponding port: X_0=1 S; X_1=1 M; X_2=1 K, INT; X_3=1 P	The pull-down MOS transistor at the corresponding input port is turned ON.	PDF
	RPDF X	Reset PDF	1 1 1 1 0 1 0 X_3 X2 X_1 X_0 0 0 0 0 0	PDF ← 0 ≡One of RF2		PDF
	SFSP	Set High Frequency Switch Sample Mode	1 1 1 0 1 0 0 0 0 0 0 0 1 0 0 0	≡SF1 8	The 7ms chattering eliminator is connected to input port S, K.	
	RFSP	Reset High Frequency Switch Sample Mode	1 1 1 0 1 1 0 0 0 0 0 0 1 0 0 0	≡RFI 8	The 31ms chattering eliminator is connected to input port S, K. At the initial mode the RFSP mode is entered.	
	WRT Y, X	Write Rx to LCD Latch (L_Y)	0 0 0 0 Y_4 Y_3 Y_2 Y_1 Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Y=00H, 01H, 1EH, 1FH causes a different instruction to occur. For input/output of the data decoder, refer to page 60.	The memory (Rx) contents are loaded to the LCD latch (L_Y) through the data decoder. For DPF=1, X=00H to 6FH, the address of R_X is specified by DP; the address of L_Y is specified by SP.	
	WRB Y, X	Write Rx to LCD Latch (L_Y)	0 0 0 1 Y_4 Y_3 Y_2 Y_1 Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Same as above.	Same as WRT X, Y. Output data "a" to "h" corresponding to input data of the data 0 decoder are all 0.	
	WRC Y, X	Write Rx to LCD Latch (LY)	0 0 1 0 Y_4 Y_3 Y_2 Y_1 Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	For input/output of the data decoder, refer to page 60.	Same as WRT X, Y except input/output of the data decoder.	
	WRP Y, X	Write Rx to LCD Latch (L_Y)	0 0 1 1 Y_4 Y_3 Y_2 Y_1 Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	For input/output of the data decoder, refer to page 60.	Same as WRT X, Y except input/output of the data decoder.	
Jump instructions	JMP X	Jump	1 1 0 0 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$	The data specified by X_{10} to X_0 is loaded to the PC to produce an unconditional jump.	
	BAB0 X	Branch on AC bit 0 High	1 0 0 0 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_0='1'	If bit 0 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB1 X	Branch on AC bit 1 High	1 0 0 0 1 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_1='1'	If bit 1 of the AC is "1", a jump occurs. If "0" the PC is incremented +1.	
	BAB2 X	Branch on AC bit 2 High	1 0 0 1 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_2='1'	If bit 2 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB3 X	Branch on AC bit 3 High	1 0 0 1 1 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_3='1'	If bit 3 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BANZ X	Branch on AC not Zero	1 0 1 0 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC≠0	If the AC is not "0", a jump occurs. If "0", the PC is incremented +1.	
	BAZ X	Branch on AC Zero	1 0 1 1 0 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC=0	If the AC is "0", a jump occurs. If not "0", the PC is incremented +1.	

Instruction	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Jump instructions	BCNH X	Branch on CF not High	1 0 1 0 1 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	PC_{10}~PC_0 ← X_{10}~X_0 if CF≠1	If the CF is "0", a jump occurs. If "1", the PC is incremented +1.	
	BCH X	Branch on CF High	1 0 1 1 1 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	PC_{10}~PC_0 ← X_{10}~X_0 if CF=1	If the CF is "1", a jump occurs. If "0", the PC is incremented +1.	
Subroutine instructions	CALL X	Call Subroutine	1 1 0 0 1 X_{10} X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	STACK ← (PC)+1 PC_{10}~PC_0 ← X_{10}~X_0	A subroutine is called.	
	RTS	Return from Subroutine	1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0	PC ← (STACK)	A return from a subroutine occurs.	
	POP	POP the stack	1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0		The stack pointer is popped −1.	
Other instructions	STM X	Set Timer	1 1 1 0 0 1 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	For the relation between X data and time setting, refer to page	The data specified by X_9 to X_0 is loaded to the TM to start the TM.	
	RTM	Reset Timer	1 1 1 1 1 1 0 0 0 0 0 0 0 1 0 0	≡PLC 4	The TM stops operating. When using the TM to release the halt mode, this instruction is executed to stop the TM and to reset the halt release request signal. When the timer interrupt is accepted, the TM stops operating automatically.	
	SFPD	Set High Frequency Pre-Divider Over Flow Mode	1 1 1 0 1 0 0 0 0 0 0 1 0 0 0 0	≡SF1 10H	Overflow signal from the divider is changed from 2Hz to 4Hz. When watch count is based on this 2Hz/4Hz signal, this instruction must be executed so that no error occurs in watch operation.	
	RFPD	Reset High Frequency Pre-Divider Over Flow Mode	1 1 1 0 1 1 0 0 0 0 0 1 0 0 0 0	≡RF1 10H	Overflow signal from the divider is changed from 4Hz to 2Hz. At the initial mode 2Hz is set.	
	PLC X	Pulse Control	1 1 1 1 1 1 0 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		The pulse corresponding to the data specified by X_8 to X_0 is generated.	HRF_0~3

X_0~X_8	Mode after execution of instruction
X_0=1	Halt release request flag HRF3 caused by overflow from the divider is reset.
X_1=1	Halt release request flag HRF2 caused by overflow from the CC is reset.
X_2=1	Halt release request flag HRF1 caused by overflow from the TM is reset.
X_3=1	Halt release request flag HRF0 caused by the signal at input port S, K or INT is reset.
X_4=1	The last 5 bits of the divider (15 bits) are reset. When executing this instruction, X_0 must be set to "1".
X_5=1	The CC and LSF are cleared. When executing this instruction, X_1 must be set to "1". Same as the CCC instruction.
X_6=1	Same as the RLP instruction.
X_7=1	Same as the CSP instruction.
X_8=1	Same as the CST instruction.

Note) 4Hz of the SFPD, RFPD instructions is for the chip (LC5800F/5899F) whose cycle time is 244μs.
8Hz is for the chip (LC5800G/5899G) whose cycle time is 122μs.

Input/Output of data decoder at WRT instruction execution mode

Input data	Output data							
	a	b	c	d	e	f	g	h
0	1	1	1	1	1	1	0	0
1	0	1	1	0	0	0	0	0
2	1	1	0	1	0	1	1	0
3	1	1	1	1	0	0	1	0
4	0	1	1	0	0	1	1	0
5	1	0	1	1	0	1	1	0
6	1	0	1	1	1	1	1	0
7	1	1	1	0	0	0	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	0	1	1	0
A/B	1	0	0	1	1	1	1	0
C/D	0	0	0	0	0	0	1	0
E/F	0	0	0	0	0	0	0	0

Input/output of data decoder at WRC instruction execution mode

Input data	Output data							
	a	b	c	d	e	f	g	h
0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0
2	0	0	0	1	0	0	0	0
3	0	0	1	0	0	0	0	0
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	1	0
6	0	0	0	0	1	0	0	0
7	1	0	0	0	0	0	0	0
8 ~ F	0	0	0	0	0	0	0	0

Input/output of data decoder WRP instruction execution mode

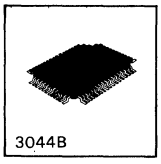
Input data	(Rx0)	(Rx1)	(Rx2)	(Rx3)	(AC0)	(AC1)	(AC2)	(AC3)
Output data	a	b	c	d	e	f	g	h

Data specified by X_9 to X_0 and set time at STM instruction execution mode

Set value										Set time (μs)
X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	
0	0	0	0	0	0	0	0	0	0	244
0	0	0	0	0	0	0	0	0	1	488
0	0	0	0	0	0	0	0	1	0	732
∫		∫				∫				∫
1	1	1	1	1	1	1	1	0	1	249512
1	1	1	1	1	1	1	1	1	0	249756
1	1	1	1	1	1	1	1	1	1	250000

Note) The set time is for the chip (LC5800F/5899F) whose cycle time is 244μs.
For the chip (LC5800G/5899G) whose cycle time is 122μs, the set time is halved.

LC5812



C MOS LSI

Single-Chip 4-Bit Microcomputer (with LCD Driver)

The LC5812 is a C MOS 4-bit microcomputer that operates on low voltage, very low current and contains an LCD driver. It also contains a 4-bit parallel processing ALU, a program memory ROM, a data memory RAM, abundant LCD segment outputs, abundant I/O ports, a prescaler, and a 32.768kHz crystal oscillator. It is especially suited for use in multifunctional telephone, camera, speech synthesis LSI, equipment, security equipment control applications.

(1) Hardware features
- Supply voltage: 3.0V typ.
- Very low current dissipation: 5.0uA typ. (during timekeeping operation by crystal oscillator only)
- On-chip CR oscillator (C, R are connected externally.)
- On-chip crystal oscillator for timekeeping (A 32.768kHz crystal is connected externally.)
- On-chip 15-bit divider for timekeeping.
- On-chip decimal counter.
- On-chip 8-bit programmable timer.
- Abundant output pins for LCD panel drive (42 pins)

Drivable LCD panel	Number of drivable LCD segments
1/3 bias 1/3 duty	126 segments
1/2 bias 1/3 duty	126 segments
1/2 bias 1/2 duty	84 segments
Static	42 segments

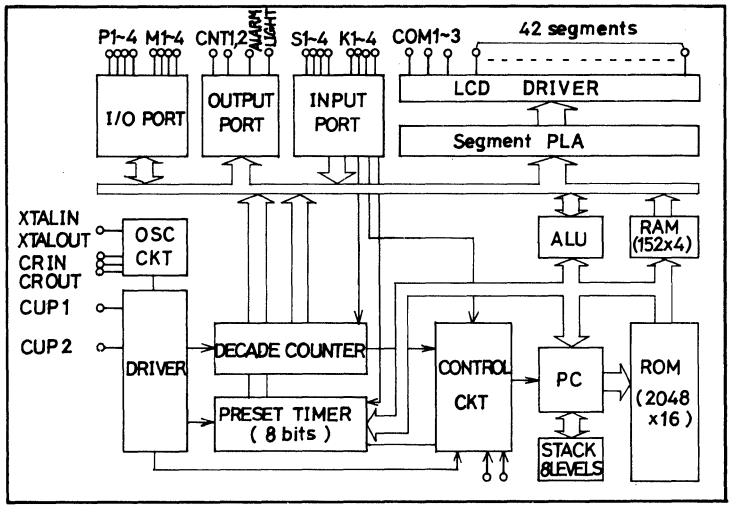
- Abundant input/output pins

Ports for input only:	2 ports/8 pins
Input/output common ports:	2 ports/8 pins
Control output pins:	4 pins

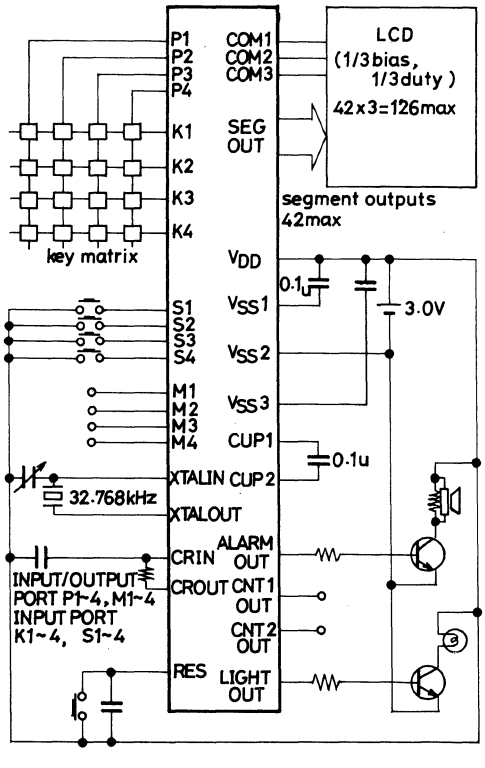
- Possible to use LCD panel drive output pins as ports for output only (mask option).
- Initial reset pin.
- ROM: 2048 x 16 bits
- RAM: 152 x 4 bits
- Cycle time: 40usec.
- On-chip step-up circuit, set-down circuit for LCD power supply.
- Shipping style: Chip (or QIP80).

(2) Software features
- Powerful instruction set: 121 instructions.
- 8-level subroutine nesting (also used for interrupt).
- External interrupt function.
- Possible to use the whole RAM area as working register (bank-selectable).
- Halt function.
- Direct addressing.
- All instructions: 1-step operation.
- On-chip data pointer.

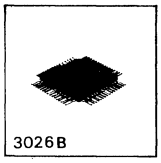
(3) Equivalent Circuit Block Diagram



(4) Sample Application Circuit (1/3 bias 1/3 duty)



LC5850



C MOS LSI

Single-Chip 4-Bit Microcomputer (with LCD Driver)

Ⓔ 1318C

The LC5850 is a C-MOS 4-bit microcomputer that operates on low voltage, very small current and contains an LCD driver. It contains a 4-bit parallel processing ALU, many LCD segment outputs, many I/O ports, a prescaler, and a 32.768kHz crystal oscillator.
It is ideally suited for use in desk-top calculator, camera, speech synthesis LSI controller, equipment controller applications as well as watch/clock applications.

(1) Hardware features

- Supply voltage: 1.5V or 3.0V (typ.) (mask option)
- Very small current dissipation:
  3.0μA typ. (1.5V supply voltage, at watch/clock operating mode)
  1.5μA typ. (3.0V supply voltage, at watch/clock operating mode)
- Built-in crystal oscillator for watch/clock (32.768kHz crystal connected externally)
- Many output pins for LCD panel drive (25 pins)

Drivable LCD panel	Number of drivable LCD segments
1/3 bias 1/3 duty	75 segments
1/2 bias 1/3 duty	75 segments
1/2 bias 1/2 duty	50 segments
Static	25 segments

- Many input/output pins
  Ports for input only: 2 ports/8 pins
  Input/output common ports: 2 ports/8 pins
  Port for output only: 1 port/4 pins
  Control output pins: 2 pins
- Possible to use LCD panel drive output pins as ports for output only (mask option)
- With initial reset pin (Port S3 for input only is used by mask option.)
- ROM: 1024 x 15 bits
- RAM: 64 x 4 bits
- Cycle time: 244μsec. (or 122μsec./mask option)
- Built-in step-up circuit, step-down circuit
- Shipping style: Chip (or QIP64B)

(2) Software features

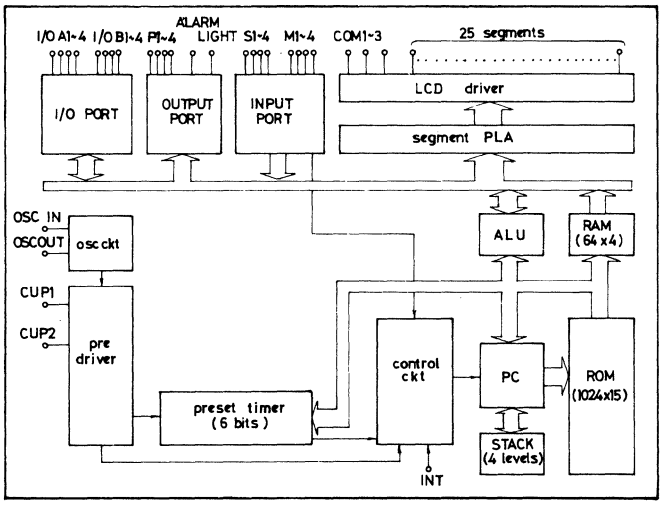
- Powerful instruction set: 78 instructions
- 4-level subroutine nesting (also used for interrupt)
- External interrupt function
- 15-bit divider for watch/clock
- Built-in 6-bit programmable timer
- HALT function
- Direct addressing type
- All instructions: Single-step operation

(3) Application development tools

For performing application development, the evaluation chip (LC5898) and the specialized application development tools are prepared.

- SDS410 system
  Application development program of microcomputer can be made in assembly language (edit, asemble).
- EVA510 + TB51 + display board + LC5898
  By connecting to the SDS410, application development program can be corrected and debugged. The EVA510 is a control ROM-replaced version of the EVA410.
- TB51 + display board + LC5898
  By using the EPROM (2732) with application development program data written in, mounting evaluation can be performed.

Equivalent Circuit Block Diagram

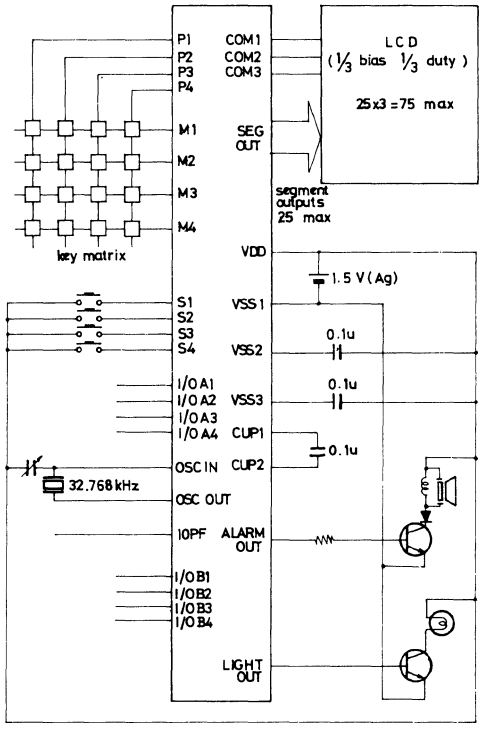


Application Areas

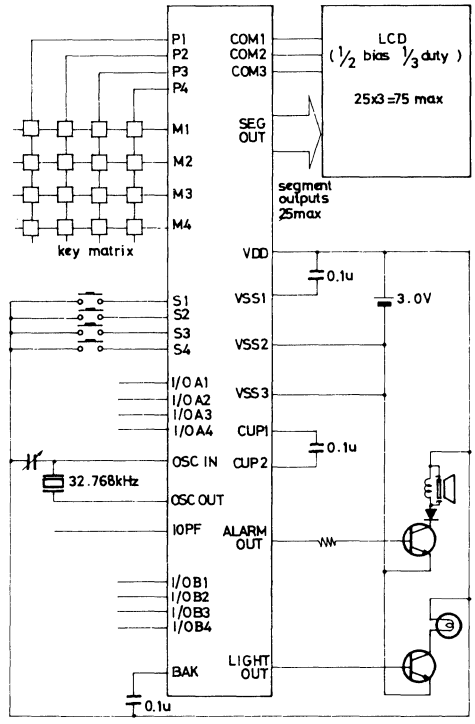
1) Watch/clock with calculator
2) Controller of speech synthesis LSI
3) Controller of camera
4) Mechanical controller of VTR, radio cassette, deck, etc.
5) Controller of telephone dialer, etc.

Sample Application Circuits

(1) Typical application circuit using Ag battery (1/3 bias 1/3 duty)

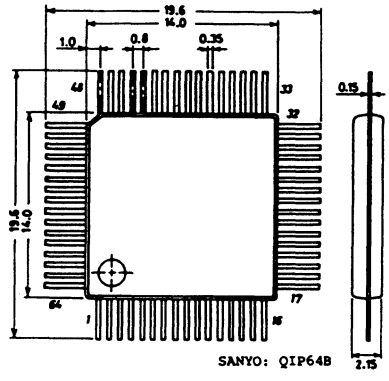


(2) Typical application circuit using Li battery (1/2 bias 1/3 duty)



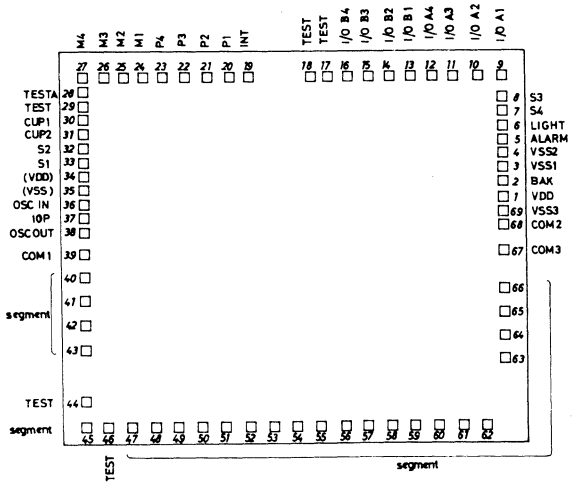
INPUT/OUTPUT PORT	I/O A1~4, I/O B1~4
INPUT PORT	S1~4, M1~4
OUTPUT PORT	P1~4

Case Outline 3026B-Q64BIC
(unit:mm)



Pad Assignment of LSI Chip

CHIP SIZE	5.72mm x 4.76mm
CHIP THICKNESS	480μm
PAD SIZE	120μm x 120μm



Pad Name and Coordinates

Pin assignment of QIP64

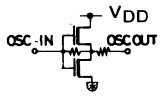
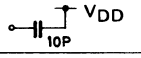
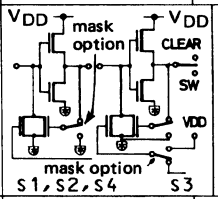
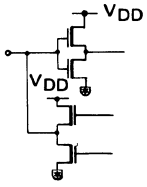
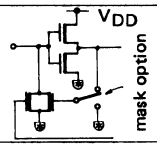
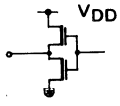
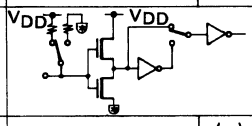
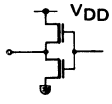
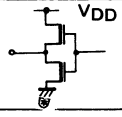
	Pad No.	Pin name	X (μm)	Y (μm)
40	1	VDD	2707	669
41	2	BAK	〃	878
42	3	VSS1	〃	1058
43	4	VSS2	〃	1238
44	5	ALARM OUT	〃	1418
45	6	LIGHT OUT	〃	1589
46	7	S4	〃	1778
47	8	S3	〃	1958
48	9	I/O A1	〃	2228
49	10	I/O A2	2385	〃
50	11	I/O A3	2070	〃
51	12	I/O A4	1800	〃
52	13	I/O B1	1530	〃
53	14	I/O B2	1260	〃
54	15	I/O B3	990	〃
55	16	I/O B4	720	〃
-	17	TEST	450	〃
-	18	TEST	239	〃
57	19	INT	-558	〃
58	20	P1	-810	〃
59	21	P2	-1098	〃
60	22	P3	-1386	〃
61	23	P4	-1674	〃
62	24	M1	-1926	〃
63	25	M2	-2178	〃
64	26	M3	-2430	〃
1	27	M4	-2707	〃
2	28	TEST A	〃	2048
3	29	TEST	〃	1868
4	30	CUP1	〃	1688
5	31	CUP2	〃	1508
6	32	S2	〃	1328
7	33	S1	〃	1148
-	34	(VDD)	〃	968
-	35	(VSS)	〃	788

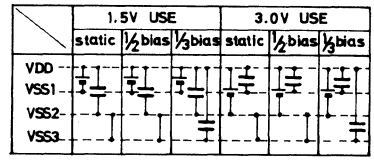
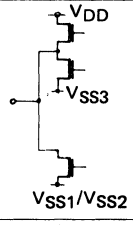
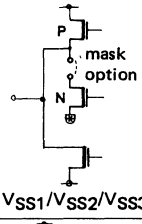
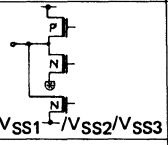
Pin assignment of QIP64

	Pad No.	Pin name	X (μm)	Y (μm)
8	36	OSC IN	-2707	608
-	37	10PF	〃	428
9	38	OSC OUT	〃	248
10	39	COMMON1	〃	-36
11	40	segment	〃	-324
12	41	〃	〃	-630
13	42	〃	〃	-936
14	43	〃	〃	-1242
-	44	TEST	〃	-1899
15	45	segment	〃	-2228
-	46	TEST	-2446	-2232
16	47	segment	-2140	-2228
17	48	〃	-1834	〃
18	49	〃	-1528	〃
19	50	〃	-1222	〃
20	51	〃	-916	〃
21	52	〃	-610	〃
22	53	〃	-304	〃
23	54	〃	2	〃
25	55	〃	308	〃
26	56	〃	614	〃
27	57	〃	920	〃
28	58	〃	1226	〃
29	59	〃	1532	〃
30	60	〃	1838	〃
31	61	〃	2144	〃
32	62	〃	2450	〃
33	63	〃	2707	-1382
34	64	〃	〃	-1087
35	65	〃	〃	-792
36	66	〃	〃	-496
37	67	COMMON3	〃	-15
38	68	COMMON2	〃	309
39	69	VSS3	〃	489

- Pins 24, 56 of QIP package: SUB (open)
- The above pad coordinates are such that the chip center is taken as the origin and the values of (X, Y) represent the coordinates of the center of each pad.

Pin Description

QIP Pin	Pad No.	Pin Name	Input /Output	Circuit Configuration	Function
8 9	36 38	OSC IN OSC OUT	Input Output		32.768kHz crystal is connected across OSCIN and OSCOUT for oscillation. Used as reference clock and system clock for watch/clock. 20pF capacitor is connected across OSCOUT and V_{DD}.
-	37	10P	-		Connected to OSCOUT and used as oscillation phase compensation capacitor.
7 6 47 46	33 32 8 7	S1 S2 S3(CLEAR /SWITCH) S4	Input		Ports for input only With 32ms chattering eliminator. S3 is used for switch input/LSI inside reset input (PLA mask option). By applying V_{DD} to S1 to S4 simultaneously, LSI inside is reset, if S3 is used for switch input.
48 49 50 51 52 53 54 55	9 10 11 12 13 14 15 16	I/O A1 I/O A2 I/O A3 I/O A4 I/O B1 I/O B2 I/O B3 I/O B4	Input /Output		Input/output pins for selecting the following 2 operations with instruction. (1) Input pin for fetching data into RAM. (2) Output pin for outputting data from RAM.
62 63 64 1	24 25 26 27	M1 M2 M3 M4	Input		Input pin for fetching data into RAM.
58 59 60 61	20 21 22 23	P1 P2 P3 P4	Output		Pin for output only.
57	19	INT	Input		External interrupt request control input pin.
41	2	BAK			(−) power supply pin for logic unit inside LSI. When using 3.0V supply, a capacitor must be connected across BAK and V_{DD} to prevent logic unit from malfunctioning.
45	6	LIGHT	Output		Pin for output only. Suited for outputting signal to drive trnasistor for light.
44	5	ALARM	Output		Pin for output only. Used to output 4kHz and 2kHz or 4kHz and 1kHz modulation signal with instruction. Also used to output non-modulation signal.

QIP Pin	Pad No.	Pin Name	Input /Output	Circuit Configuration	Function
40	1	VDD			(+) Power supply pin.
39 43 42	69 4 3	VSS3 VSS2 VSS1			(−) power supply pin. • 1.5V/3.0V selectable with mask option. For 1.5V use, apply (−) side to V_{SS1} For 3.0V use, apply (−) side to V_{SS2} • Also used as power supply for LCD drive.  The above Table shows how to connect external parts in each case.
4 5	30 31	CUP1 CUP2			Pins for connecting voltage step-up (step-down) capacitor.
10 38 37	39 68 67	COM1 COM2 COM3	Output	 	Output pins for LCD panel common electrode. The following pin is used in each case. Static / 1/2 duty / 1/3 duty COM1: ○ ○ ○ COM2: – ○ ○ COM3: – – ○ Alternating frequency: 32Hz* 32Hz* 43Hz* * Possible to make frequency 2 or 4-fold.
34 35 36	64 65 66	segment driver	Output	 	Output pins for LCD panel segments. • Also used as output ports with mask option. • When LSI inside is in reset mode, 32Hz, 64Hz, and 128Hz static light-up signal is outputted at COM1 to COM3 and each LCD segment output and all LCD panel segments light up. • Segment PLA system is adopted to meet the requirements of free pattern on LCD panel.
11 ~ 33	40 ~ 43 45 47 ~ 63	segment driver	Output	 	Output pins for LCD panel segments. • Also used as output ports with mask option.
- - 2 3 - -	17 18 28 29 44 46	TEST TEST TEST A TEST TEST TEST			Test pins (not used by user).
- -	35 34	(VSS) (VDD)			Backup power supply pin. Normally, not used.

NOTE Ag Battery : ⊕ = V_{SS1}
Li Battery, EXT-V : ⊕ = V_{SS2}

- **Operation from Ag Battery [Static]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum supply Voltage.	V_{SS1}		-4.0~+0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-4.0~+0.3	V
Maximum Input Voltage	V_{IN1}	S1-4, M1-4, I/OA1-4, I/OB1-4, 10P, OSCIN, INT, TESTA (I/OA1-4, I/OB1-4: Input mode)	V_{SS1}-0.3~0.3	V
Maximum Output Voltage	V_{OUT1}	TEST, CUP2, OSCOUT, ALARM, LIGHT, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	V_{SS1}-0.3~0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1	V_{SS2}-0.3~0.3	V
Operating Temperature	T_{opg}		-20~+65	℃
Storage Temperature	T_{stg}		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.3		-2.4	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	〃 〃	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	f_{opg}	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr., *1, Fig. 1	10		200	kΩ
	R_{IN1B}	V_{SS1}=-1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kΩ
	R_{IN2A}	V_{SS1}=-1.55V, V_{IL}=V_{SS1}, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS1}=-1.55V, V_{IH}=V_{DD}, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=-1.55V, I_{OH}=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=-1.55V, I_{OL}=0.4μA, SEGOUT		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=-1.55V, I_{OH}=-4μA, COM1	-0.2			V
"L"-Level Output Votage	V_{OL2}	V_{SS1}=-1.55V, I_{OL}=4μA, COM1		V_{SS2}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=-1.35V, I_{OH}=-250μA, ALM·LIGHT	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250μA, ALM·LIGHT		V_{SS1}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20μA, P1-4 I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20μA, P1-4 I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)		V_{SS1}+0.2		V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1μF, f_{opg}=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	$\|I_{DD}\|$	V_{SS1}=-1.55V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 2		2.0		μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kΩ, Fig. 3	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	Co=Cg=20pF, CI=25kΩ, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	Co=Cg=20pF, CI=25kΩ, V_{SS1}=−1.35V, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from Li Battery [Static]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0~+0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	-4.0~+0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TESTI/O	V_{BAK}-0.3~0.3	V
	V_{IN2}	S1-4, M1-4, INT, I/OA1-4, I/OB1-4, TESTA (I/OA1-4, I/OB1-4: Input mode)	V_{SS2}-0.3~0.3	V
Maximum Output Voltage	V_{OUT1}	TESTI/O, CUP2, OSCOUT	V_{BAK}-0.3~0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1, ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1: Output mode)	V_{SS2}-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	〃 〃	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 4	10		200	kΩ
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kΩ
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS2}=-2.9V, V_{IH}=V_{DD}, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4μA, COM1	-0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4μA, COM1			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250μA, ALM	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250μA, ALM			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V, I_{OH}=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.9V, I_{OH}=40μA I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=−2.4V, I_{OH}=−150μA, LIGHT	−1.5			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=−2.4V, I_{OL}=150μA, LIGHT			V_{SS2}+1.5	V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			-1.35	V
Current Dissipation	I_{DDI}	V_{SS2}=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 5		1.0		μA
Oscillation Start Voltage	Vstt	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kΩ, Fig. 6	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{SS1}=V_{SS2}/2, Co=Cg=20pF, CI=25kΩ, Fig. 5			-2.6	V
Oscillation Start Time	tstt	V_{SS1}=V_{SS2}=-2.9V, Co=Cg=20pF, CI=25kΩ, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from EXT-V [Static]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS2}	V_{SS2}=V_{SS3}=V_{SS1}	-4.0~+0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN	V_{SS2}-0.3~0.3	V
	V_{IN2}	S1-4, M1-4, INT, I/OA1-4, I/OB1-4, TESTA (I/OA1-4, I/OB1-4: Input mode)	V_{SS2}–0.3~0.3	V
Maximum output Voltage	V_{OUT1}	TESTCUP2, OSCOUT	V_{SS2}-0.3~0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1, ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	V_{SS2}-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS2}	V_{SS1}=V_{SS2}=V_{SS3}	–3.6		–2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	–0.4		0	V
"L"-level Input Voltage	V_{IL}	〃 〃	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=–2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 13	10		200	kΩ
	R_{IN1B}	V_{SS2}=–2.9V, "L"-Level pull-in tr., *1, Fig. 13	200		2000	kΩ
	R_{IN2A}	V_{SS2}=–2.9V, V_{IL}=V_{SS2}, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS2}=–2.9V, V_{IH}=V_{DD}, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=–2.9V, I_{OH}=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=–2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=–2.9V, I_{OH}=-4μA, COM1	-0.2			V
"L" Output Voltage	V_{OL2}	V_{SS2}=–2.9V, I_{OL}=4μA, COM1			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=–2.4V, I_{OH}=-250μA, ALM·LIGHT	-0.65			
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=–2.4V, I_{OL}=250μA, ALM, LIGHT			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=–2.9V, I_{OH}=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	–0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=–2.9V, I_{OL}=40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4: I/OB1-4: Output mode)			V_{SS2}+0.4	V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=–2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 14		5.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kΩ, Fig. 15	–2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kΩ, Fig. 14			–2.0	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=–2.9V, Co=Cg=20pF, CI=25kΩ, Fig.15			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from Ag Battery [1/2 Bias, 1/2 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	VSS1		-4.0~+0.3	V
	VSS2	VSS2=VSS3	-4.0~+0.3	V
Maximum Input Voltage	VIN1	S1-4,M1-4,I/OA1-4,I/OB1-4,10P, OSCIN,INT,TESTA (I/OA1-4, I/OB1-4: Input mode)	VSS1-0.3~0.3	V
Maximum Output Voltage	VOUT1	TEST,CUP2,OSCOUT,ALARM,LIGHT, I/OA1-4,I/OB1-4,P1-4 (I/OA1-4, I/OB1-4: Output mode)	VSS1-0.3~0.3	V
	VOUT2	SEGOUT,COM1,COM2,CUP1	VSS2-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	VSS1		-1.65		-1.30	V
	VSS2	VSS2=VSS3	-3.3		-2.4	V
"H"-Level Input Voltage	VIH	S1-4,M1-4,I/OA1-4,I/OB1-4,INT, (I/OA1-4, I/OB1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	VIL	〃 〃	VSS1		VSS1+0.2	V
Operating Frequency	fopg	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS1=-1.55V,VIL=VSS1+0.2V, "L"-Level hold tr., *1, Fig. 1	10		200	kΩ
	RIN1B	VSS1=-1.55V, "L"-Level pull-in tr., *1, Fig. 1	200		2000	kΩ
	RIN2A	VSS1=-1.55V,VIL=VSS1,INT⊘ INT pull-up resistance	200		2000	kΩ
	RIN2B	VSS1=-1.55V,VIH=VDD,INT⊘ INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	VOH1	VSS1=-1.55V,IOH=-0.4μA,SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS1=-1.55V,IOL=0.4μA,SEGOUT		VSS2+0.2		V
"H"-Level Output Voltage	VOH2	VSS1=-1.55V,IOH=-4μA,COM1·COM2	-0.2			V
"M"-Level Output Voltage	VOM	VSS1=-1.55V,IOH=-4μA, IOL=4μA,COM1·COM2	VSS1-0.2		VSS1+0.2	V
"L"-Level Output voltage	VOL2	VSS1=-1.55V,IOL=4μA,COM1·COM2		VSS2+0.2		V
"H"-Level Output Voltage	VOH3	VSS1=-1.35V,IOH=-250μA, ALM·LIGHT	-0.65			V
"L"-Level Output Voltage	VOL3	VSS1=-1.35V,IOL=250μA, ALM·LIGHT		VSS1+0.65		V
"H"-Level Output Voltage	VOH4	VSS1=-1.55V,IOH=-20μA,P1-4 I/OA1-4,I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	VOL4	VSS1=-1.55V,IOL=20μA,P1-4 I/OA1-4,I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)		VSS1+0.2		V
Output Voltage (doubler)	VSS2	VSS1=-1.35V, C1=C2=0.1μF,fopg=32.768kHz,Fig. 2			-2.5	V
Current Dissipation	IIDDI	VSS1=-1.55V,standard watch/clock operation, C1=C2 =0.1μF,Co=Cg=20pF,CI=25kΩ,Fig. 2	2.0			μA
Oscillation Start Voltage	Vstt	Co=Cg=20pF,CI=25kΩ,Fig. 3	-1.35			V
Oscillation Hold Voltage	VHOLD	Co=Cg=20pF,CI=25kΩ,Fig. 2	-1.65		-1.30	V
Oscillation Start Time	tstt	Co=Cg=20pF,CI=25kΩ,VSS1=-1.35V Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from Li Battery [1/2 Bias, 1/2 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	VSS1	VBAK=VSS1 or VSS2	-4.0~+0.3	V
	VSS2	VSS2=VSS3, VBAK=VSS1 or VSS2	-4.0~+0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN	VBAK-0.3~0.3	V
	VIN2	S1-4, M1-4, INT, I/OA1-4, I/OB1-4, TESTA (I/OA1-4, I/OB1-4: Input mode)	VSS2-0.3~0.3	V
Maximum Output Voltage	VOUT1	TEST, CUP2, OSCOUT	VBAK-0.3~0.3	V
	VOUT2	SEGOUT, COM1, COM2, CUP1, ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	VSS2-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	VBAK		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	VIH	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	VIL	〃 〃	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, VIL=VSS2+0.4V, "L"-Level hold tr., *1, Fig. 4	10		200	kΩ
	RIN1B	VSS2=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kΩ
	RIN2A	VSS2=-2.9V, VIL=VSS2, INT pull-up resistance	200		2000	kΩ
	RIN2B	VSS2=-2.9V, VIH=VDD, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4μA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4μA, COM1·COM2	-0.2			V
"M"-Level Output Voltage	VOM	VSS2=-2.9V, IOH=-4μA, IOL=4μA, COM1·COM2	VSS2/2-0.2		VSS2/2+0.2	V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4μA, COM1·COM2			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250μA, ALM	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250μA, ALM			VSS2+0.65	V
"H"-Level Output Voltage	VOH4	VSS2=-2.9V, IOH=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL4	VSS2=-2.9V, IOH=40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)			VSS2+0.4	V
"H"-Level Output Voltage	VOH5	VSS2=-2.9V, IOH=-150μA, LIGHT	-1.5			V
"L"-Level Output Voltage	VOL5	VSS2=-2.9V, IOL=150μA, LIGHT			VSS2+1.5	V
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			-1.35	V
Current Dissipation	IIDDI	VSS2=-2.9V, standard watch/clock operation, C1=C2 =0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 5		1.0		μA
Oscillation Start Voltage	Vstt	VSS1=VSS2, Co=Cg=20pF, CI=25kΩ, Fig. 6	-1.35			V
Oscillation Hold Voltage	VHOLD	VSS1=VSS2/2, Co=Cg=20pF, CI=25kΩ, Fig. 5			-2.6	V
Oscillation Start Time	tstt	VSS1=VSS2=-2.9V, Co=Cg=20pF, CI=25kΩ, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from EXT-V [1/2 Bias, 1/2 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	VSS1		-4.0~+0.3	V
	VSS2	VSS2=VSS3	-4.0~+0.3	V
Maximum Input Voltage	VIN1	10P,OSCIN	VSS2-0.3~0.3	V
	VIN2	S1-4,M1-4,INT,I/OA1-4,I/OB1-4, TESTA (I/OA1-4, I/OB1-4: Input mode)	VSS2-0.3~0.3	V
Maximum Output Voltage	VOUT1	TEST,CUP2,OSCOUT	VSS2-0.3~0.3	V
	VOUT2	SEGOUT,COM1,COM2,CUP1,ALARM, LIGHT,P1-4,I/OA1-4,I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	VSS2-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	VSS1		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	VIH	S1-4,M1-4,I/OA1-4,I/OB1-4,INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	VIL	〃 〃	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, VIL=VSS2+0.4V, "L"-Level hold tr., *1, Fig. 4	10		200	kΩ
	RIN1B	VSS2=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kΩ
	RIN2A	VSS2=-2.9V, VIL=VSS2, INT pull-up resistance	200		2000	kΩ
	RIN2B	VSS2=-2.9V, VIH=VDD, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4μA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4μA, COM1·COM2	-0.2			V
"M"-Level Output Voltage	VOM	VSS2=-2.9V, IOH=-4μA, IOL=4μA, COM1·COM2		VSS2/2-0.2	VSS2/2+0.2	V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4μA, COM1·COM2			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250μA, ALM·LIGHT	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250μA, ALM·LIGHT			VSS2+0.65	V
"H"-Level Output Voltage	VOH4	VSS2=-2.9V, IOH=-40μA, I/OA1-4,I/OB1-4,P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL4	VSS2=-2.9V, IOH=40μA, I/OA1-4,I/OB1-4,P1-4 (I/OA1-4, I/OB1-4: Output mode)			VSS2+0.4	V
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			-1.35	V
Current Dissipation	IIDDI	VSS2=-2.9V, standard watch/clock operation, C1=C2 =0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 5		5.0		μA
Oscillation Start Voltage	Vstt	VSS1=VSS2, Co=Cg=20pF, CI=25kΩ, Fig. 6	-2.2			V
Oscillation Hold Voltage	VHOLD	VSS1=VSS2/2, Co=Cg=20pF, CI=25kΩ, Fig. 5			-2.0	V
Oscillation Start Time	tstt	VSS1=VSS2=-2.9V, Co=Cg=20pF, CI=25kΩ, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from Ag Battery [1/2 Bias, 1/3 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0~+0.3	V
	V_{SS2}	$V_{SS2}=V_{SS3}$	-4.0~+0.3	V
Maximum Input Voltage	V_{IN1}	S1-4, M1-4, I/OA1-4, I/OB1-4, IOP, OSCIN, INT, TESTA (I/OA1-4, I/OB1-4: Input mode)	V_{SS1}-0.3~0.3	V
Maximum Output Voltage	V_{OUT1}	TEST, CUP2, OSCOUT, ALARM, LIGHT, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	V_{SS1}-0.3~0.3	V
	V_{OUT2}	SEGOUT, COM1, COM2, COM3, CUP1	V_{SS2}-0.3~0.3	V
Operating Temperature	T_{opg}		-20~+65	℃
Storage Temperature	T_{stg}		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		-1.65		-1.30	V
	V_{SS2}	$V_{SS2}=V_{SS3}$	-3.3		-2.4	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	V_{IL}	〃 〃	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	f_{opg}	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=-1.55V, $V_{IL}=V_{SS1}$+0.2V, "L"-Level hold tr., *1, Fig. 1	10		200	kΩ
	R_{IN1B}	V_{SS1}=-1.55V, "L"-Level pull-in tr., *1, Fig. 1	200		2000	kΩ
	R_{IN2A}	V_{SS1}=-1.55V, $V_{IL}=V_{SS1}$, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS1}=-1.55V, $V_{IH}=V_{DD}$, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=-1.55V, I_{OH}=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=-1.55V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=-1.55V, I_{OH}=-4μA, COM1·COM2·COM3	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS1}=-1.55V, I_{OH}=-4μA, I_{OL}=4μA, COM1·COM2·COM3	V_{SS1}-0.2		V_{SS1}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=-1.55V, I_{OL}=4μA, COM1·COM2·COM3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=-1.35V, I_{OH}=-250μA, ALM·LIGHT	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250μA, ALM·LIGHT			V_{SS1}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20μA, P1-4 I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20μA, P1-4 I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)			V_{SS1}+0.2	V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1μF, f_{opg}=32.768kHz, Fig. 2			-2.5	V
Current Dissipation	$\|I_{DD}\|$	V_{SS1}=-1.55V, standard watch/clock operation, C1=C2 =0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 2	2.0			μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kΩ, Fig. 3	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	Co=Cg=20pF, CI=25kΩ, Fig. 2	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	Co=Cg=20pF, CI=25kΩ, V_{SS1}=-1.35V Fig. 3			10	sec
Oscillation Correction Capacitance	IOP	External pin	8	10	12	pF
	2OP	OSCOUT	16	20	24	pF

- **Operation from Li Battery [1/2 Bias, 1/3 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0~+0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	-4.0~+0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TESTI/O	V_{BAK}-0.3~0.3	V
	V_{IN2}	S1-4, M1-4, INT, I/OA1-4, I/OB1-4, TESTA (I/OA1-4, I/OB1-4: Input mode)	V_{SS2}-0.3~0.3	V
Maximum Output Voltage	V_{OUT1}	TEST, CUP2, OSCOUT	V_{BAK}-0.3~0.3	V
	V_{OUT2}	SEGOUT, COM1·COM2·COM3, CUP1, ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	V_{SS2}-0.3~0.3	V
Operating Temperature	T_{opg}		-20~+65	°C
Storage Temperature	T_{stg}		-30~+125	°C

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	-3.6		-2.0	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	〃 〃	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	Ta=-20~+65 °C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 4	10		200	kΩ
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kΩ
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS2}=-2.9V, V_{IH}=V_{DD}, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4μA, COM1·COM2·COM3	-0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=-2.9V, I_{OH}=-4μA, I_{OL}=4μA, COM1·COM2·COM3		V_{SS2}/2-0.2	V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4μA, COM1·COM2·COM3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250μA, ALM	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250μA, ALM			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V, I_{OH}=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.9V, I_{OH}=40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=-2.9V, I_{OH}=-150μA, LIGHT	-1.5			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=-2.9V, I_{OL}=150μA, LIGHT			V_{SS2}+1.5	V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V, C1=C2=0.1μF, f_{opg}=32.768kHz, Fig. 5			-1.35	V
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=-2.9V, standard watch/clock operation, C1=C2 =0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 5		1.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kΩ, Fig. 6	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{SS1}=V_{SS2}/2, Co=Cg=20pF, CI=25kΩ, Fig. 5			-2.6	V

			min	typ	max	unit
Oscillation Start Time	tstt	VSS1=VSS2=-2.9V, Co=Cg=20pF, CI=25kΩ, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from EXT-V [1/2 Bias, 1/3 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	VSS1		-4.0~+0.3	V
	VSS2	VSS2=VSS3	-4.0~+0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN	VSS2-0.3~0.3	V
	VIN2	S1-4, M1-4, INT, I/OA1-4, I/OB1-4, TESTA (I/OA1-4, I/OB1-4: Input mode)	VSS2-0.3~0.3	V
Maximum Output Voltage	VOUT1	TEST, CUP2, OSCOUT	VSS2-0.3~0.3	V
	VOUT2	SEGOUT, COM1·COM2·COM3, CUP1, ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4 (I/OA1-4, I/OB1-4: Output mode)	VSS2-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	VSS1		-3.6		-1.3	V
	VSS2	VSS2=VSS3	-3.6		-2.0	V
"H"-Level Input Voltage	VIH	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	VIL	〃 〃	VSS2		VSS2+0.4	V
Operating Frequency	fopg	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	RIN1A	VSS2=-2.9V, VIL=VSS2+0.4V, "L"-Level hold tr., *1, Fig. 4	10		200	kΩ
	RIN1B	VSS2=-2.9V, "L"-Level pull-in tr., *1, Fig. 4	200		2000	kΩ
	RIN2A	VSS2=-2.9V, VIL=VSS2, INT pull-up resistance	200		2000	kΩ
	RIN2B	VSS2=-2.9V, VIH=VDD, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	VOH1	VSS2=-2.9V, IOH=-0.4μA, SEGOUT	-0.2			V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4μA, SEGOUT			VSS2+0.2	V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4μA, COM1·COM2·COM3	-0.2			V
"M"-Level Output Voltage	VOM	VSS2=-2.9V, IOH=-4μA, IOL=4μA, COM1·COM2·COM3	VSS2/2-0.2		VSS2/2+0.2	V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4μA, COM1·COM2·COM3			VSS2+0.2	V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250μA, ALM, LIGHT	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250μA, ALM, LIGHT			VSS2+0.65	V
"H"-Level Output Voltage	VOH4	VSS2=-2.9V, IOH=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL4	VSS2=-2.9V, IOH=40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)			VSS2+0.4	V
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			-1.35	V
Current Dissipation	IIDDI	VSS2=-2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 5		5.0		μA

			min	typ	max	unit
Oscillation Start Voltage	Vstt	Vss1=Vss2, Co=Cg=20pF, CI=25kΩ, Fig. 6	-2.2			V
Oscillation Hold Voltage	VHOLD	Vss1=Vss2/2, Co=Cg=20pF, CI=25kΩ, Fig. 5			-2.0	V
Oscillation Start Time	tstt	Vss1=Vss2=-2.9V, Co=Cg=20pF, CI=25kΩ, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from 1.5V Ag Battery [1/3 Bias, 1/3 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	Vss1		-4.0~+0.3	V
	Vss2		-4.0~+0.3	V
	Vss3		-5.5~+0.3	V
Maximum Input Voltage	VIN1	S1-4, M1-4, I/OA1-4, I/OB1-4, 10P, OSCIN, INT, TESTA (I/OA1-4, I/OB1-4: Input mode)	Vss1-0.3~0.3	V
Maximum Output Voltage	VOUT1	TEST, CUP2, OSCOUT, ALARM, LIGHT, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	Vss1-0.3~0.3	V
	VOUT2	SEGOUT, COM1·COM2·COM3, CUP1	Vss3-0.3~0.3	V
Operating Temperature	Topg		-20~+65	°C
Storage Temperature	Tstg		-30~+125	°C

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	Vss1		-1.65		-1.30	V
	Vss2		-3.3		-2.4	V
	Vss3		-4.95		-3.7	V
"H"-Level Input Voltage	VIH	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.2		0	V
"L"-Level Input Voltage	VIL	〃 〃	Vss1		Vss1+0.2	V
Operating Frequency	fopg	Ta=-20~+65 °C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	RIN1A	Vss1=-1.55V, VIL=Vss1+0.2V, "L"-Level hold tr., *1, Fig. 7	10		200	kΩ
	RIN1B	Vss1=-1.55V, "L"-Level pull-in tr., *1, Fig. 7	200		2000	kΩ
	RIN2A	Vss1=-1.55V, VIL=Vss1, INT pull-up resistance	200		2000	kΩ
	RIN2B	Vss1=-1.55V, VIH=VDD, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	VOH1	Vss1=-1.55V, IOH=-0.4μA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	VOM1-1	Vss1=-1.55V, IOH=-0.4μA, IOL=0.4μA, SEGOUT	Vss1-0.2		Vss1+0.2	V
"M2"-Level Output Voltage	VOM2-1	〃 〃	Vss2-0.2		Vss2+0.2	V
"L"-Level Output Voltage	VOL1	Vss1=-1.55V, IOL=-0.4μA, SEGOUT			Vss3+0.2	V
"H"-Level Output Voltage	VOH2	Vss1=-1.55V, IOH=-4μA, COM1·COM2·COM3	-0.2			V
"M1"-Level Output Voltage	VOM1-2	Vss1=-1.55V, IOL=4μA, IOH=-4μA, COM1·COM2·COM3	Vss1-0.2		Vss1+0.2	V
"M-2"-Level Output Voltage	VOM2-2	〃 〃	Vss2-0.2		Vss2+0.2	V
"L"-Level Output Voltage	VOL2	Vss1=-1.55V, IOL=4μA, COM1·COM2·COM3			Vss3+0.2	V
"H"-Level Output Voltage	VOH3	Vss1=-1.35V, IOH=-250μA, ALM·LIGHT	-0.65			V

			min	typ	max	unit
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=-1.35V, I_{OL}=250μA, ALM, LIGHT		V_{SS1}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=-1.55V, I_{OH}=-20μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=-1.55V, I_{OL}=20μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)		V_{SS1}+0.2		V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=-1.35V, C1=C2=0.1μF, f_{opg}=32.768kHz, Fig. 8			-2.5	V
(tripler)	V_{SS3}	〃 〃			-3.75	V
Current Dissipation	I_{DD}	V_{SS1}=-1.55V, standard watch/clock operation, C1 to C3=0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 8		3.5		μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kΩ, Fig. 9	-1.35			V
Oscillation Hold Voltage	V_{HOLD}	Co=Cg=20pF, CI=25kΩ, Fig. 8	-1.65		-1.30	V
Oscillation Start Time	t_{stt}	V_{SS1}=-1.35V, Co=Cg=20pF, CI=25kΩ, Fig. 9			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from Li Battery [1/3 Bias, 1/3 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0~+0.3	V
	V_{SS2}	V_{BAK}=V_{SS1} or V_{SS2}	-4.0~+0.3	V
	V_{SS3}	V_{BAK}=V_{SS1} or V_{SS2}	-5.5~0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN	V_{BAK}-0.3~0.3	V
	V_{IN2}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, TESTA (I/OA1-4, I/OB1-4: Input mode)	V_{SS2}-0.3~0.3	V
Maximum Output Voltage	V_{OUT1}	TEST, OSCOUT	V_{BAK}-0.3~0.3	V
	V_{OUT2}	ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4, CUP2 (I/OA1-4, I/OB1-4: Output mode)	V_{SS2}-0.3~0.3	V
	V_{OUT3}	SEGOUT, COM1~COM3, CUP1	V_{SS3}-0.3~0.3	V
Operating Temperature	T_{opg}		-20~+65	℃
Storage Temperature	T_{stg}		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}		-3.6		-2.0	V
	V_{SS3}	V_{SS3}≈V_{SS2}+V_{SS1}	-5.0		-3.9	V
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	〃 〃	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	f_{opg}	Ta=-20~+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 10	10		200	kΩ
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig. 10	200		2000	kΩ
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS}=-2.9V, V_{IH}=V_{DD}, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4μA, SEGOUT	-0.2			V

			min	typ	max	unit
"M1"-Level Output Voltage	VOM1-1	VSS2=-2.9V, IOH=-0.4μA, IOL=0.4μA, SEGOUT	VSS2/2-0.2	VSS/2+0.2		V
"M2"-Level Output Voltage	VOM2-1	〃 〃	VSS2-0.2	VSS2+0.2		V
"L"-Level Output Voltage	VOL1	VSS2=-2.9V, IOL=0.4μA, SEGOUT		VSS3+0.2		V
"H"-Level Output Voltage	VOH2	VSS2=-2.9V, IOH=-4μA, COM1·COM2·COM3	-0.2			V
"M1"-Level Output Voltage	VOM1-2	VSS2=-2.9V, IOH=-4μA, IOL=4μA, COM1·COM2·COM3	VSS2/2-0.2	VSS/2+0.2		V
"M-2"-Level Output Voltage	VOM2-2	〃 〃	VSS2-0.2	VSS2+0.2		V
"L"-Level Output Voltage	VOL2	VSS2=-2.9V, IOL=4μA, COM1·COM2·COM3		VSS3+0.2		V
"H"-Level Output Voltage	VOH3	VSS2=-2.4V, IOH=-250μA, ALM	-0.65			V
"L"-Level Output Voltage	VOL3	VSS2=-2.4V, IOL=250μA, ALM		VSS2+0.65		V
"H"-Level Output Voltage	VOH4	VSS2=-2.9V, IOH=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	VOL4	VSS2=-2.9V, IOH=40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)		VSS2+0.4		V
"H"-Level Output Voltage	VOH5	VSS2=-2.9V, IOH=-150μA, LIGHT	-1.5			V
"L"-Level Output Voltage	VOL5	VSS2=-2.9V, IOL=-150μA, LIGHT		VSS2+1.5		V
Output Voltage (halver)	VSS1	VSS2=-2.9V, C1~C4=0.1μF, fopg=32.768kHz, Fig. 11			-1.35	V
(tripler)	VSS3	〃 〃			-4.1	V
Current Dissipation	|IDD|	VSS2=-2.9V, standard watch/clock operation, C1 to C4 =0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 11	2.0			μA
Oscillation Start Voltage	Vstt	VSS1=VSS2, Co=Cg=20pF, CI=25kΩ, Fig. 12	-1.35			V
Oscillation Hold Voltage	VHOLD	VSS1=VSS2/2, Co=Cg=20pF, CI=25kΩ, Fig. 11			-2.6	V
Oscillation Start Time	tstt	VSS2=-2.9V, VSS1=VSS2, Co=Cg=20pF, CI=25kΩ, Fig. 12			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

- **Operation from EXT-V [1/3 Bias, 1/3 Duty]**

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	VSS1		-4.0~+0.3	V
	VSS2		-4.0~+0.3	V
	VSS3		-5.5~0.3	V
Maximum Input Voltage	VIN1	10P, OSCIN	VSS2-0.3~0.3	V
	VIN2	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, TESTA (I/OA1-4, I/OB1-4: Input mode)	VSS2-0.3~0.3	V
Maximum Output Voltage	VOUT1	TEST, OSCOUT	VSS2-0.3~0.3	V
	VOUT2	ALARM, LIGHT, P1-4, I/OA1-4, I/OB1-4, CUP2 (I/OA1-4, I/OB1-4: Output mode)	VSS2-0.3~0.3	V
	VOUT3	SEGOUT, COM1~COM3, CUP1	VSS3-0.3~0.3	V
Operating Temperature	Topg		-20~+65	℃
Storage Temperature	Tstg		-30~+125	℃

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	VSS1		-3.6		-1.3	V
	VSS2		-3.6		-2.0	V
	VSS3	VSS3≈VSS2+VSS1	-5.0		-3.9	V

			min	typ	max	unit
"H"-Level Input Voltage	V_{IH}	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4: Input mode)	-0.4		0	V
"L"-Level Input Voltage	V_{IL}	〃 〃	V_{SS2}	V_{SS2}+0.4		V
Operating Frequency	fopg	Ta=-20～+65 ℃	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}+0.4V, "L"-Level hold tr., *1, Fig. 10	10		200	kΩ
	R_{IN1B}	V_{SS2}=-2.9V, "L"-Level pull-in tr., *1, Fig. 10	200		2000	kΩ
	R_{IN2A}	V_{SS2}=-2.9V, V_{IL}=V_{SS2}, INT pull-up resistance	200		2000	kΩ
	R_{IN2B}	V_{SS}=-2.9V, V_{IH}=V_{DD}, INT pull-down resistance	200		2000	kΩ
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=-2.9V, I_{OH}=-0.4μA, SEGOUT	-0.2			V
"M1"-Level Output Voltage	V_{OM1-1}	V_{SS2}=-2.9V, I_{OH}=-0.4μA, I_{OL}=0.4μA, SEGOUT	V_{SS2}/2-0.2	V_{SS}/2+0.2		V
"M2"-Level Output Voltage	V_{OM2-1}	〃 〃	V_{SS2}-0.2	V_{SS2}+0.2		V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=-2.9V, I_{OL}=0.4μA, SEGOUT		V_{SS3}+0.2		V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=-2.9V, I_{OH}=-4μA, COM1・COM2・COM3	-0.2			V
"M1"-Level Output Voltage	V_{OM1-2}	V_{SS2}=-2.9V, I_{OH}=-4μA, I_{OL}=4μA, COM1・COM2・COM3	V_{SS2}/2-0.2	V_{SS}/2+0.2		V
"M-2"-Level Output Voltage	V_{OM2-2}	〃 〃	V_{SS2}-0.2	V_{SS2}+0.2		V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=-2.9V, I_{OL}=4μA, COM1・COM2・COM3		V_{SS3}+0.2		V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=-2.4V, I_{OH}=-250μA, ALM・LIGHT	-0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=-2.4V, I_{OL}=250μA, ALM・LIGHT		V_{SS2}+0.65		V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=-2.9V, I_{OH}=-40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)	-0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=-2.9V, I_{OH}=40μA, I/OA1-4, I/OB1-4, P1-4 (I/OA1-4, I/OB1-4: Output mode)		V_{SS2}+0.4		V
Output Voltage (halver)	V_{SS1}	V_{SS2}=-2.9V, C1～C4=0.1μF, fopg=32.768kHz, Fig. 11			-1.35	V
(tripler)	V_{SS3}	〃 〃			-4.1	V
Current Dissipation	$\lvert I_{DD} \rvert$	V_{SS2}=-2.9V, standard watch/clock operation, C1 to C4=0.1μF, Co=Cg=20pF, CI=25kΩ, Fig. 11		5.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kΩ, Fig. 12	-2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{SS1}=V_{SS2}/2, Co=Cg=20pF, CI=25kΩ, Fig. 11			-2.0	V
Oscillation Start Time	t_{stt}	V_{SS2}=-2.9V, V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=25kΩ, Fig. 12			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

※1 S1・S2・S3・S4・M1・M2・M3・M4

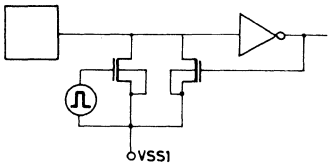


Fig. 1 Input configuration of S1-4, M1-4

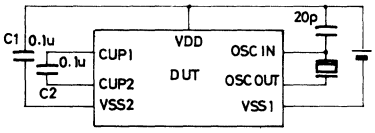


Fig. 2 Current dissipation, oscillation hold voltage test circuit

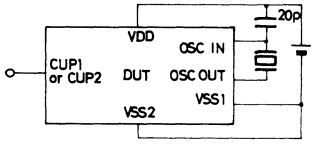


Fig. 3 Oscillation start voltage, oscillation start time, frequency stability test circuit

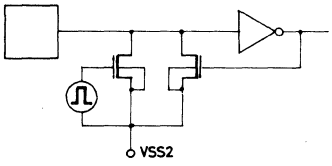


Fig. 4 Input configuration of S1-4, M1-4

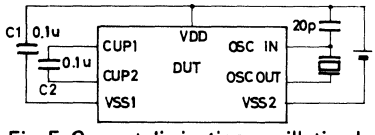


Fig. 5 Current dissipation, oscillation hold voltage test circuit

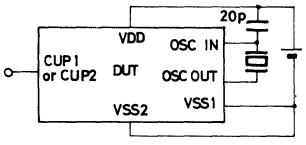


Fig. 6 Oscillation start voltage, oscillation start time, frequency stability test circuit

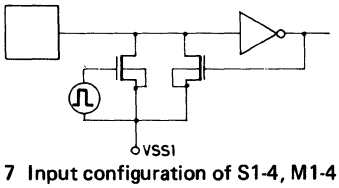


Fig. 7 Input configuration of S1-4, M1-4

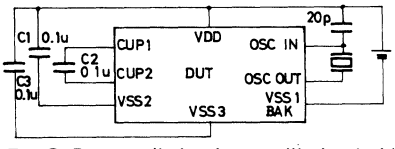


Fig. 8 Current dissipation, oscillation hold voltage test circuit

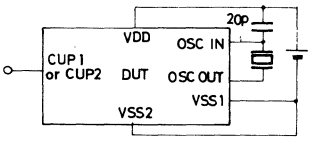


Fig. 9 Oscillation start voltage, oscillation start time, frequency stability test circut

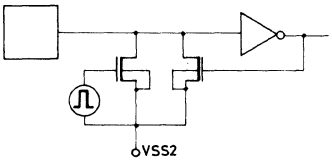


Fig. 10 Input configuration of S1-4, M1-4

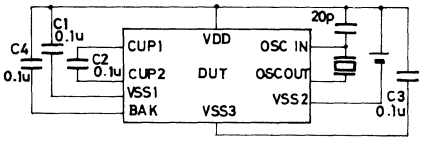


Fig. 11 Current dissipation, oscillation hold voltage test circuit

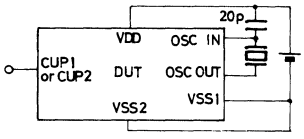


Fig. 12 Oscillation start voltage, oscillation start time, frequency stability test circuit

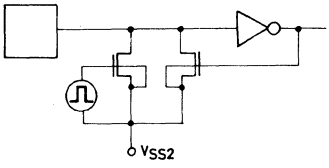


Fig. 13 Input configuration of S1-4, M1-4

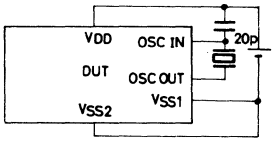


Fig. 14 Current dissipation, oscillation hold voltage test circuit

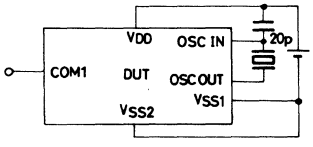
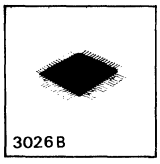


Fig. 15 Oscillation start voltage, oscillation start time, frequency stability test circuit

LC5851



C MOS LSI

Single-Chip 4-Bit Microcomputer (with LCD Driver)

TENTATIVE

The LC5851 is a C MOS microcomputer that operates on low voltage, very low current and contains an LCD driver. It also contains a 4-bit parallel processing ALU, a program memory ROM, abundant LCD segment outputs, a prescaler, a 32.768kHz crystal oscillator.
It is especially suited for use in electronic tuning system camera, speech synthesis LSI, equipment control applications.

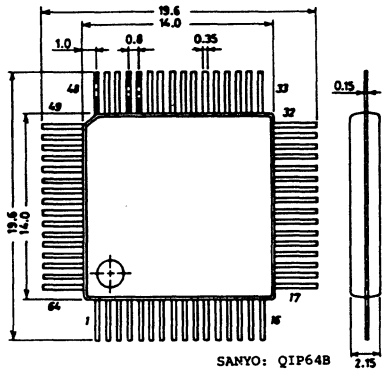
(1) Hardware featues

- Supply voltage: 1.5V or 3.0V typ. (mask option)
- Very low current dissipation:
  3.0uA typ. (1.5V Ag battery power supply, at halt mode)
  1.5uA typ. (3.0V Li battery power supply, at halt mode)
- On-chip crystal oscillator for timekeeping and lcd drive frequency (A 32.768kHz crystal is connected externally.)
- Abundant output pins for LCD panel drive (25 pins)

Drivable LCD panel	Number of drivable LCD segments
1/3 bias 1/3 duty	75 segments
1/2 bias 1/3 duty	75 segments
1/2 bias 1/2 duty	50 segments
Static	25 segments

- Abundant input/output pins
  Ports for input only: 2 ports/ 8 pins
  Input/output common ports: 2 ports/ 8 pins
  Ports for output only: 1 port/4 pins
  (also used for pseudo serial output port)
  Control output pins: 2 pins
- Possible to use LCD panel drive output pins as ports for output only (mask option)
- Initial reset pin (Port S_3 for input only is used by mask option.)
- ROM: 1024 x 15 bits
- RAM: 64 x 4 bits

Case Outline 3026B-Q64BIC
(unit:mm)

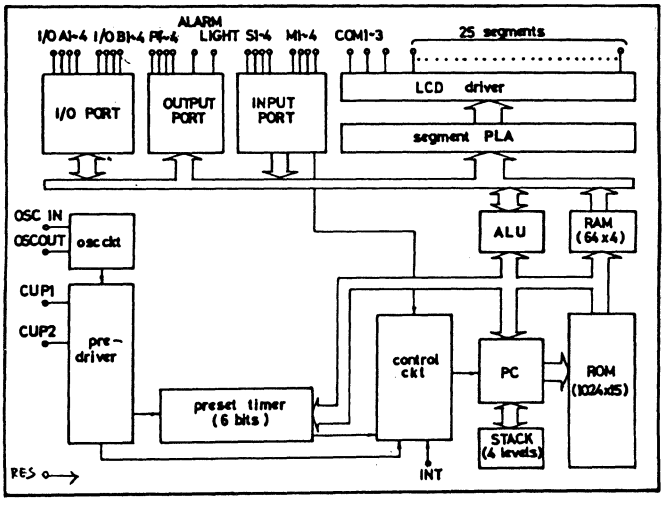


. Cycle time:
  Ag/Li battery-used applications (32K X'tal): 244usec.
  EXT-V-used applications (32K X'tal): 122usec./244usec.
  EXT-V-used applications (external input): 60usec. to 244usec.
. On-chip step-up circuit, step-down circuit.
. Shipping style: QIP64-B (or chip)
  (Specification for chip is to be agreed upon separately.)

(2) Software features
. Powerful instruction set: 78 instructions
. 4-level subroutine nesting (also used for interrupt)
. External interrupt function.
. On-chip 15-bit divider for timekeeping.
. On-chip 6-bit programmable timer.
. Halt function.
. Direct addressing.
. All instructions: 1-step operation.

(3) Application development tools
For performing application development, evaluation chip LC5895 and the dedicated application development tools are available.
. SDS410 system
  Application development program of microcomputer can be made in assembly language (edit, assemble).
. EVA510 + TB51 + display board + LC5895
  By connecting to the SDS410, application development program can be corrected and debugged. The EVA510 is a control ROM-replaced version of the EVA410.
. TB51 + display board + LC5895
  By using EPROM 2732 with application development program data written in, mounting evaluation can be performed.

Equivalent Circuit Block Diagram

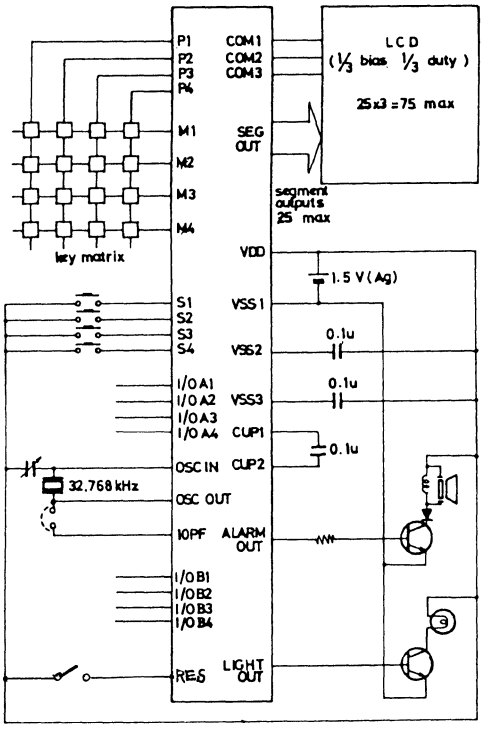


Sample Applications

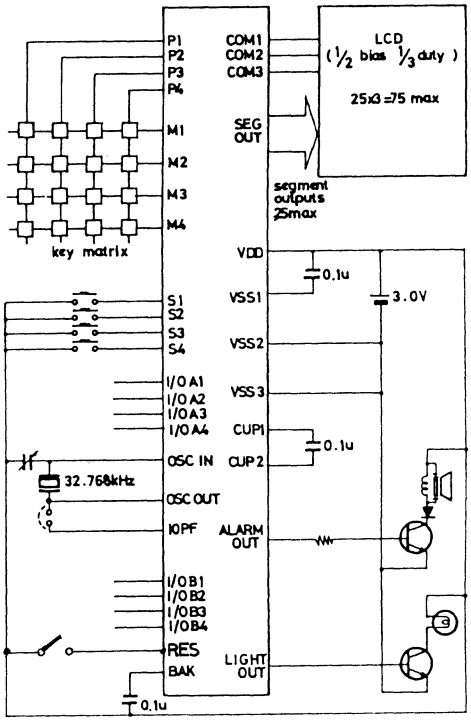
1) Controller for electronic tuning system
2) Controller for speech synthesis LSI
3) Controller for camera
4) Mechanical controller for VTR, radio cassette, deck, etc.
5) Controller for telephone dialer, etc.

Sample Application circuits

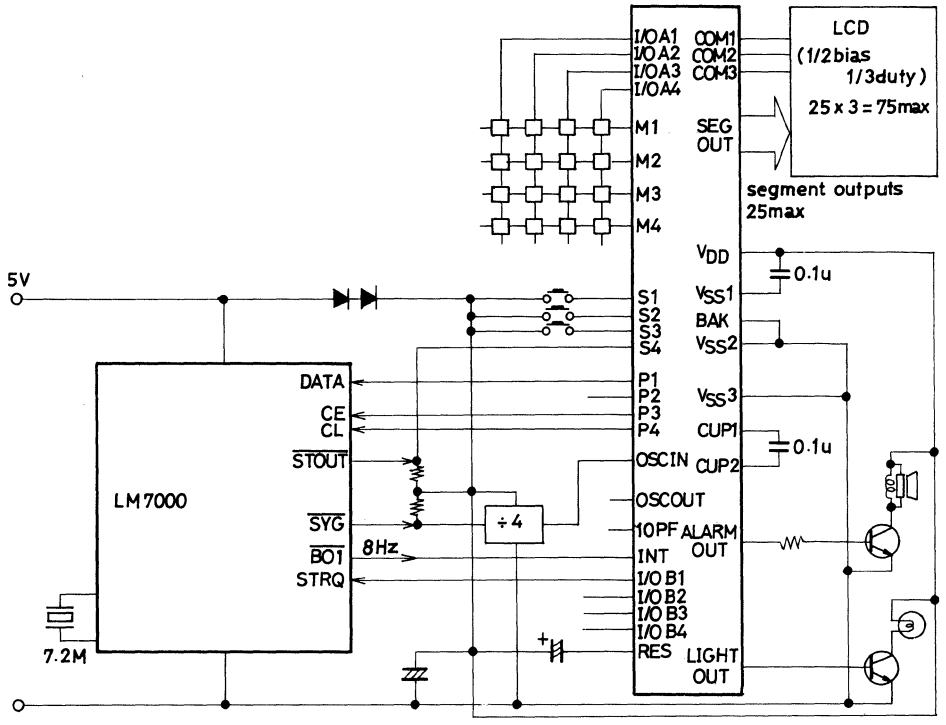
(1) 1.5V Ag battery-used application (1/3 bias 1/3 duty)



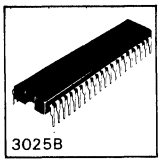
(2) 3.0V Li battery-used application (1/2 bias 1/3 duty)



INPUT/OUTPUT PORT	I/OA1~4, I/OB1~4
INPUT PORT	S1~4, M1~4
OUTPUT PORT	P1~4


I/OA1
I/OA2
I/OA3
I/OA4
COM1
COM2
COM3
LCD
(1/2bias
1/3duty)
25 x 3 = 75max
M1
M2
M3
M4
SEG
OUT
segment outputs
25max
VDD
0.1u
5V
S1
S2
S3
S4
VSS1
BAK
VSS2
DATA
CE
CL
STOUT
P1
P2
P3
P4
VSS3
CUP1
0.1u
OSCIN
CUP2
LM7000
OSCOUT
SYG
÷4
10PF
ALARM
OUT
BOT
8Hz
INT
STRQ
I/OB1
I/OB2
I/OB3
I/OB4
7.2M
RES
LIGHT
OUT

LM8800 Series



N MOS LSI

Single-Chip 8-Bit Microcomputer for Control-Oriented Applications

Ⓔ 1567

1. General Description

The LM8800 series are single-chip 8-bit microcomputers fabricated using NMOS process technology. They are intended for high-speed, high-function control of consumer equipment and control of office automation equipment. They adopt an architecture suited for control-oriented applications, perform 6-factor 4-level multi-interrupt function, and contain two 8-bit multifunction timers, a serial I/O port, I/O ports (max. 57 pins). The instruction set with 101 instructions is easy to use for control-oriented applications and powerful.

2. Architecture Features

(1) Abundant memory : ROM=4k bytes max., RAM=256 bytes max.
(2) I/O ports (max. 57 pins) : LM8854, 8852
(3) Two 8-bit multifunction timers (interval timer, event counter) and 10-bit prescaler.
(4) 8-bit PWM type DA converter : Also used for timer 1.
(5) Square wave output : Also used for timer 1.
(6) Serial I/O port : Synchronous=8 bits or asynchronous=10 bits, half-duplex 11-bit communication.
(7) Direct connectable with general-purpose master CPU to transmit/receive 8-bit parallel data.
(8) 6-factor 4-level multi-interrupt : External=2 factors, timer=2 factors, serial I/O, 8-bit bus.
(9) 16-level stack
(10) Instruction set with 101 instructions
. Single-bit processing, single-bit decision of RAM, I/O port
. Direct/indirect addressing of RAM, I/O port

3. Hardware Features (*: Average current value)

(1) High-speed operation: Instruction cycle time 1usec. min. (target)
(2) 15V breakdown voltage I/O port and 30mA*output driver (8 pcs.), 18mA*output driver (max. 38 pcs.)
(3) Single 5v supply, RAM backup capability
(4) On-chip OSC : Ceramic, crystal, CR oscillation
(5) TTL/CMOS input level selectable, pull-up/open drain output selectable.
(6) Output mode selectable at the time of reset
(7) AC wave zero-cross detector selectable

4. Contents of LM8800 Series

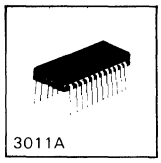
Type No.	ROM	RAM	Input/output	Input	Output	Package	Remarks
LM8854	4kx8	256x8	4x8	11	14	DIP64S	
LM8804	4k	256	4x8	3	-	DIP42,42S	
LM8852	2k	128	4x8	11	14	DIP64S	
LM8802	2k	128	4x8	3	-	DIP42,42S	
LM8899	External,8k	256x8	4x8	11	14	PGA100	Evaluation chip
LM88PG99	External,8k	256x8	4x8	11	14	DIC64S	Piggyback

PERIPHERALS/ SPEECH SYNTHESIS/MEMORIES

- **Pin Numbering**

When you face the top side (marking side) of the package, numbering starts with ① assigned to the pin located, in a counterclockwise direction, immediately after the index point and turns counterclockwise.

LC3100



C MOS LSI

128K-Bit CMOS Mask ROM

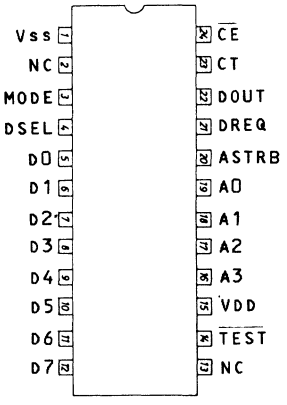
Ⓔ 1437A

The LC3100 is a 128K-bit CMOS mask ROM that contains an interface connectable direct to the speech synthesizer LSI LC8100. With one piece of this mask ROM, approximately 100 seconds of speech synthesis can be attained. A selection of 8-bit, 4-bit, or single-bit output data is allowed by means of external control. This mask ROM is also suited for use in applications other than speech synthesis.

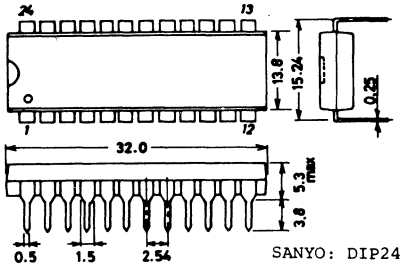
Features

• ROM capacity	128K bits
• Access time	6.9μsec typ (for operation at 800kHz typ.) 26.0μsec typ (for operation at 200kHz typ.)
• Cycle time	8.1μsec typ (for operation at 800kHz typ.) 30.6μsec typ (for operation at 200kHz typ.)
• Function	(1) Contains an interface to the LC8100 (speech synthesizer LSI). (2) Possible to select the bit length of output data. 8-bit data 4-bit data Single-bit data
• Low power dissipation	CMOS
• Current dissipation	2mA max. (at operating mode) 1μA max. (at nonoperating mode)
• Single +5V power supply	+4.5 to 6.5 V (supply voltage range)
• Package	DIP24

Pin Assignment

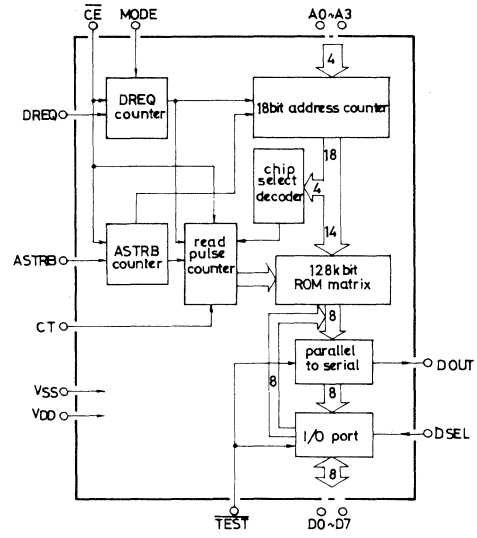


Case Outline 3011A-D24IC
(unit: mm)



Equivalent Circuit Block Diagram

A0 to A3:	18-bit address setting pins
ASTRB:	A0 to A3 strobe pin
DREQ:	ROM data request pin
DOUT:	ROM data serial output pin
CT:	Basic operation clock input pin
D0 to D7:	8-bit input/output pins
MODE:	DREQ pin input pulse count control pin
DSEL:	Output bit length select pin
$\overline{CE}$:	Power-down control pin
$\overline{TEST}$:	TEST pin
V_{DD}, V_{SS}:	Power supply pin



Description of Operation of Internal Block

- ASTRB COUNTER: Block which internally sets address information applied in 5 steps from A0 to A3 pins.
- 18bit ADDRESS COUNTER: Address counter organized with 18 bits.
- READ PULSE COUNTER: Block which generates signal to operate address decoder, data selector.
- CHIP SELECT DECODER: Makes chip select signal with 2^{14} to 2^{17} bits of 18-bit address.
- 128kbit ROM MATRIX: ROM matrix cell organized with 128K bits.
- PARALLEL TO SERIAL: Shift register which serially outputs 8-bit parallel data to DOUT pin.
- I/O PORT: Selects input/output at D0 to D7 pins.

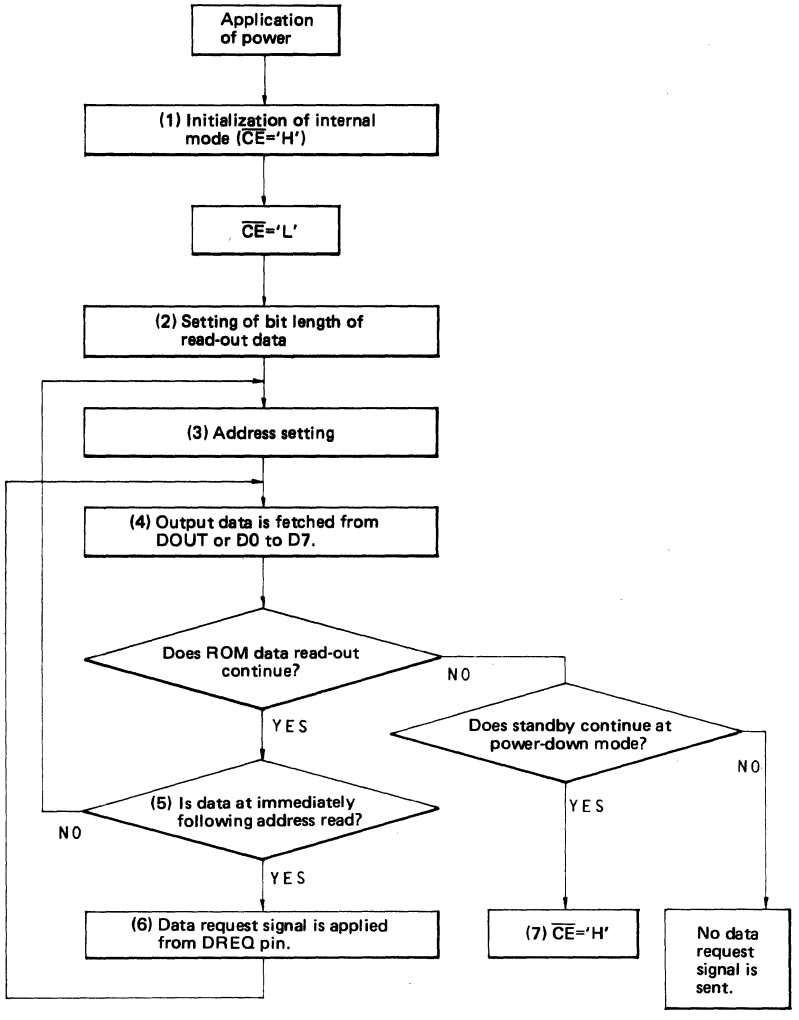
Pin Description

Pin No.	Pin Name	Input/output	Function
20	ASTRB	Input	Pin for inputting strobe signal which causes data A0 to A3 to be latched at address setting mode.
21	DREQ	Input	ROM data request signal input pin.
22	DOUT	Output	Pin for outputting ROM data serially. When used in conjunction with the LC8100, this pin is connected to DIN pin of the LC8100.
23	CT	Input	Pin for inputting basic operation clock of ROM inside. When used in conjunction with the LC8100, this pin is connected to CT pin of the LC8100.

Pin No.	Pin Name	Input/output	Function
24	$\overline{CE}$	Input	Pin for controlling initialization of LSI inside immediately after application of power and internal operation stop (power-down). For performing synthesization or ROM data read-out, set $\overline{CE}$ to 'L'.
1	V_{SS}	–	Connected to 0V of power supply.
15	V_{DD}	–	Connected to + side of power supply.
3	MODE	Input	Pin for controlling number of input pulses at DREQ pin. When ROM data read-out is performed serially in a single bit, set MODE to 'L'. When ROM data read-out is performed in 8 bits or 4 bits, set MODE to 'H'.
4	DSEL	Input	Used when ROM data read-out is performed in 4 bits. When DSEL is set to 'H', 2^4 to 2^7 bits are outputted to D0 to D3 pins.
5	D0	Input/output	Pins for outputting ROM data in 8 bits and inputting data in 8 bits.
6	D1		
7	D2		
8	D3		
9	D4		
10	D5		
11	D6		
12	D7		
14	$\overline{TEST}$	Input	LSI test pin. Open or connected to V_{DD}.
16	A3	Input	Pins for setting 18-bit address. At address setting mode, address information is inputted by 4 bits from high-order bit downward in 5 steps.
17	A2		
18	A1		
19	A0		

ROM Data Read-out Procedure

The following flowchart shows the outline of read-out procedure. (1) to (7) give a more detailed description.



(1) Initialization of internal mode

There are 4 counter blocks (ASTRB counter, 18-bit ADDRESS counter, READ PULSE counter, DREQ counter) inside the LC3100. Since initialization is required immediately after application of power, apply one 'H' level pulse to $\overline{CE}$ pin. When $\overline{CE}$ is set to 'L' level, the power-down mode is released (refer to (6)) and it is possible to start read-out any time.

(2) Setting of bit length of read-out data

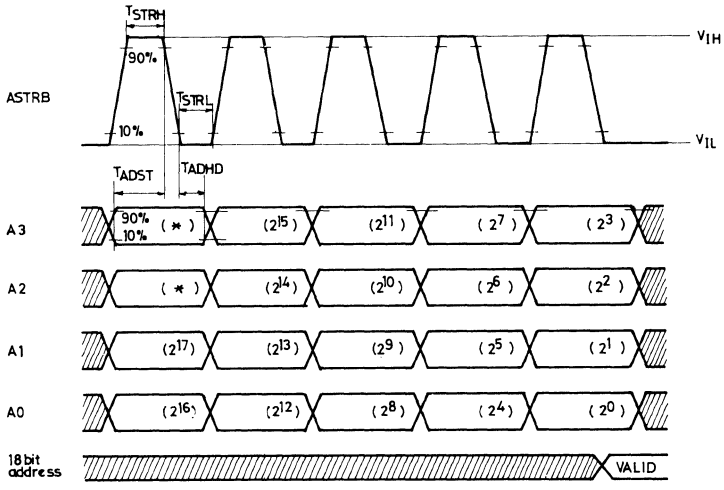
For the bit length of ROM data output, a selection of 3 lengths is allowed: 8 bits, 4 bits, and a single bit. For controlling this selection, MODE, DSEL pins are used. The following Table shows 3 types of pin setting.

DSEL \ MODE	'L'	'H'
'L'	Single-bit length (speech synthesis)	8-bit or 4-bit length or 4-bit length (Note)
'H'	–	4-bit length (Note)

(Note) When DSEL is set to 'L', 2^0 to 2^3 bits are outputted at D0 to D3 pins.
When DSEL is set to 'H', 2^4 to 2^7 bits are outputted at D0 to D3 pins.

(3) Address setting

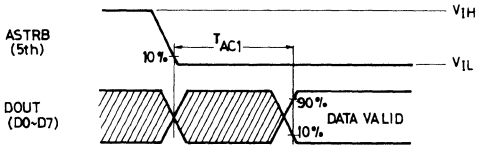
Apply 5 successive pulses to ASTRB pin. Synchronously with these pulses apply 18-bit address information to A0 to A3 pins from high-order bit downward by 4 bits in 5 steps. At this address setting mode DREQ pin must be set to 'L' level. Shown below is the timing.



(Note) • "*"=don't care.
• "2n"=Binary number at the nth bit to be set in address counter.
• For the numeric values of T_{STRH}, T_{STRL}, T_{ADST}, T_{ADHS}, refer to Electrical Characteristics.

Start of read-out of set address data

Read-out of ROM data starts at the falling of the 5th ASTRB pulse or the first (MODE='H') or the 8th (MODE=/L') DREQ pulse, and when access time T_{AC1} has elapsed 2^0 bit is outputted at DOUT pin and 2^0 to 2^7 data are outputted at D0 to D7 pins. (Refer to the following Timing Chart.)
Note) For the numeric value of T_{AC1}, refer to Electrical Characteristics.

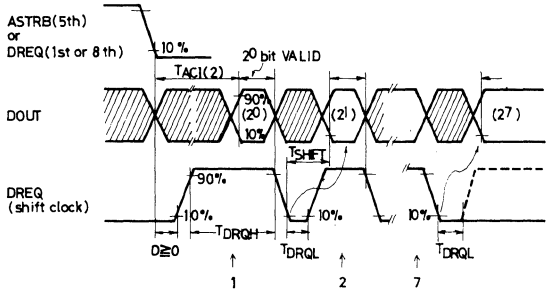


(4) Fetching of output data

As shown above, whenever access time T_{AC1} has elapsed, data can be fetched from output ports DOUT or D0 to D7 pins. (Pin setting as shown in Table in (2) is required.)

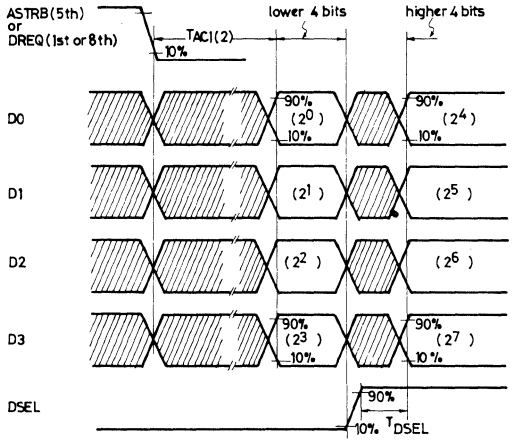
Counting one byte in a single bit from DOUT pin

Count a single bit (2^n bit) from DOUT pin. To count the following single bit (2^{n+1} bit), apply a shift clock to DREQ pin. Shown below is Timing Chart.
For the numeric values of T_{AC1}, T_{DRQH}, T_{SHFT}, refer to Electrical Characteristics.



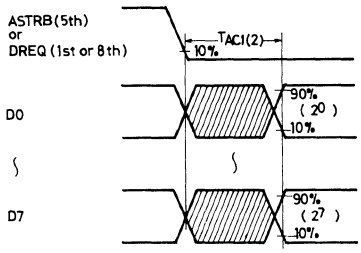
Counting one byte in 4-bits from D0 to D3 pins

In accordance with Table and (Note) in (2), fetch one byte from D0 to D3 pins by 4 bits in 2 steps. Shown below is Timing Chart.



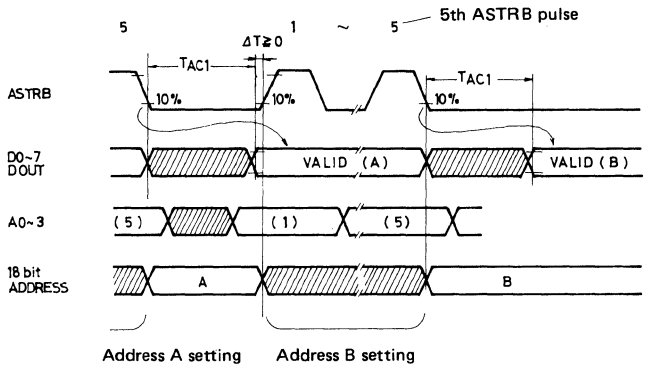
Counting one byte in 8 bits from D0 to D7 pins

Fetch 8 bits from D0 to D7 pins. Shown below is Timing Chart.

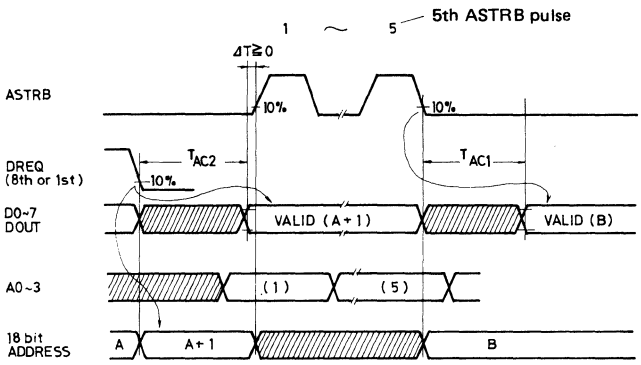


(5) Setting address again and counting data

(1) Timing for application of ASTRB pulse when address A is set and read out and then address B is set and read out.



(2) Timing for application of ASTRB pulse when data is read out by application of DREQ signal (refer to (6) below) and then address B is set and read out.



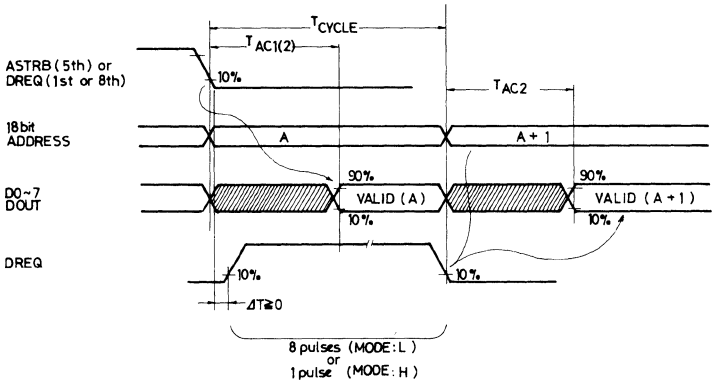
(6) Request of ROM data at the following address

When the signal shown below is applied to the LSI, the LSI begins to read out data at the address immediately following the address at which preceding data is read out.

Falling of 8th DREQ pulse (MODE='L')

Falling of 1st DREQ pulse (MODE='H')

Shown below is Timing Chart.



Note) Apply ROM data request signal after T_{CYCLE} or more has elapsed.
For the numeric value of T_{CYCLE}, refer to Electrical Characteristics.

(7) Power-down mode

When the input at $\overline{CE}$ pin is set to 'H' level, the LC3100 enters power-down mode (each block inside the LSI stops its operation, with no unnecessary current dissipated.). At this mode, the LSI inside becomes as follows and current dissipation is reduced.

(1) Input at input ports (ASTRB, DREQ, A0 to A3) is inhibited.
(It should be noted that if input is floating, current dissipation increases.)

(2) Both address decoder and data selector in 128K-bit ROM matrix stop their internal operation.

(3) Output at 3-state output pins DOUT, D0 to D7 is floating or fixed. (The user can select either of the two. Refer to "User mask") When $\overline{CE}$ is set to 'H', in addition to reduction in current dissipation as mentioned above, 4 internal counters (ASTRB COUNTER, 18-BIT ADDRESS COUNTER, READ PULSE COUNTER, DREQ COUNTER) are initialized in readiness for read-out after power-down mode release ($\overline{CE}$='L').

User mask

(1) CHIP SELECT DECODER

User mask option which makes LSI chip select signal (select, nonselect) with 2^{14} to 2^{17} bits of 18-bit addresses. Shown below is the output modes including $\overline{CE}$ pin conditions.

	$\overline{CE}$='L'	$\overline{CE}$='H' (Power-down)
Chip select	DATA is outputted from DOUT, D0 to D7 pins.	Data immediately before $\overline{CE}$='H' occurs is held and outputted. (Note)
Chip nonselect	Output at DOUT, D0 to D7 pins has a high impedance.	Output at DOUT, D0 to D7 pins has a high impedance.

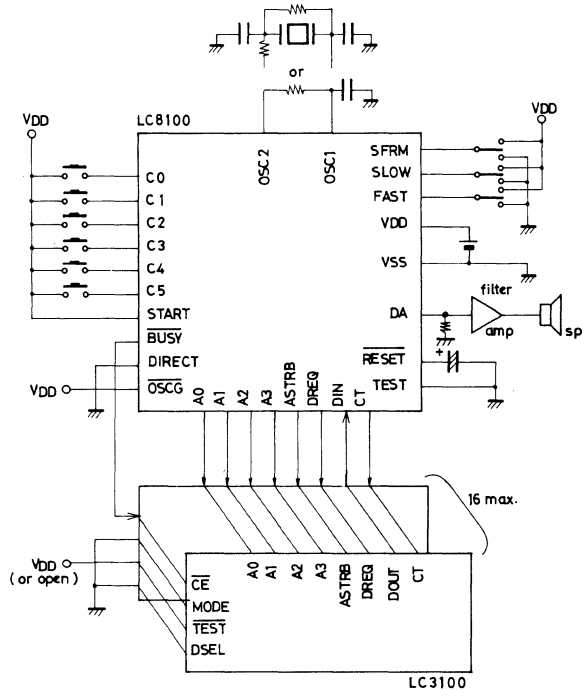
Note) In this case, the LSI only, having CHIP SELECT DECODER whose 2^{14} to 2^{17} bits are all 0, outputs data and all others have a high impedance.

(2) SW mask

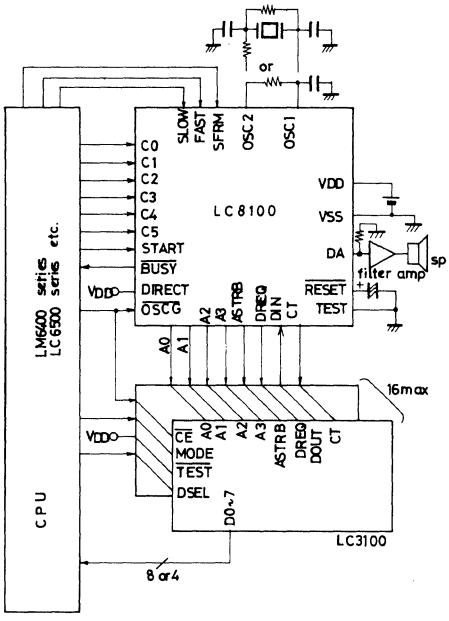
SW mask controls output at DOUT, D0 to D7 output pins in the following two ways at power-down mode. The user can select either of the two beforehand.

(i) Output at DOUT, D0 to D7 pins is set to a high impedance.
(ii) Data immediately before power-down mode is held and outputted.

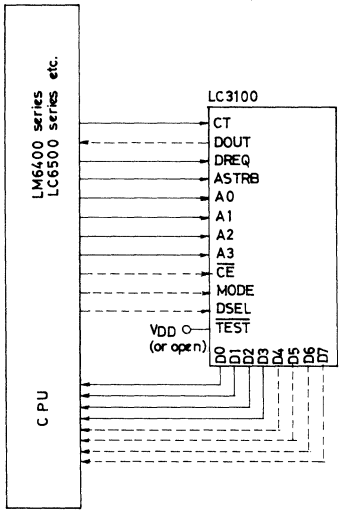
Sample Application Circuit (1) One word to one key correspondence



Sample Application Circuit (2) CPU control: Edit and synthesis with CPU



Sample Application Circuit (3) CPU control: Application other than speech synthesis



Note) Connect signals shown with dotted lines as required.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DD} max	V_{DD} pin	−3.0 to +7.0	V
Input Voltage	V_{IN}	All input pins	−0.3 to V_{DD}+0.3	V
Output Voltage	V_O	All input pins	−0.3 to V_{DD}+0.3	V
Output Current	I_O	All output pins, per pin	−2.0 to +2.0	mA
Allowable Power Dissipation	P_d max	T_a=−30 to +70°C	200	mW
Operating Temperature	T_{opg}		−30 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Allowable Operating Ranges at T_a=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 6.5V			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD} pin	4.5	5.0	6.5	V
Input 'H'-Level Voltage	V_{IH}	All input pins other than D0 to D7	0.7V_{DD}			V
Input 'L'-Level Voltage	V_{IL}	All input pins other than D0 to D7			0.3V_{DD}	V
Operating Clock Frequency	f_{CT}	Fig. 1, T_a=−30 to +60°C	150	800	960	kHz
Operating Clock 'H'-Level Pulse Width	$t_{w\phi H}$	Fig. 1	0.3			μs
Operating Clock 'L'-Level Pulse Width	$t_{w\phi L}$	Fig. 1	0.47			μs

Electrical Characteristics at T_a=−30 to +70°C, V_{DD}=4.5 to 6.5V, V_{SS}=0V			min	typ	max	unit
Input 'H'-Level Current	I_{IH}	V_{IN}=V_{DD}			1.0	μA
Input 'L'-Level Current	I_{IL}	V_{IN}=V_{SS}	−1.0			μA
Output 'H'-Level Voltage	V_{OH}	I_{OH}=−0.3mA	V_{DD}−0.6			V
Output 'L'-Level Voltage	V_{OL}	I_{OH}=0.3mA			0.6	V
Output OFF Leak Current	I_{OFF1}	V_O=V_{DD}, D0 to D7, D_{OUT} pin			1.0	μA
	I_{OFF2}	V_O=V_{SS}, D0 to D7, D_{OUT} pin	−1.0			μA
Input Pin Capacitance	C_I			5	10	pF
Pull-up Resistance	R_{up}	$\overline{TEST}$ pin	20		1000	kΩ
Current Dissipation	$I_{DD(1)}$	At operating mode, f_{CT}=960kHz, Fig. 2			2.0	mA
	$I_{DD(2)}$	At nonoperating mode, T_a=−30 to +50°C, Fig. 2			1.0	μA

AC Characteristics at T_a=−30 to +70°C, V_{DD}=4.5 to 6.5V, V_{SS}=0V, R_L=200kohm, Cp=50pF			min	typ	max	unit
Address Setup Time	T_{ADST}	Fig. 3	0.3			μs
Address Hold Time	T_{ADHD}	Fig. 3	0.3			μs
ASTRB 'H'-Level Pulse Width	T_{STRH}		0.3			μs
ASTRB 'L'-Level Pulse Width	T_{STRL}		0.3			μs
DREQ 'H'-Level Pulse Width	T_{DRQH}		0.3			μs
DREQ 'L'-Level Pulse Width	T_{DRQL}		0.3			μs
ASTRB Pulse Duration	T_{ASTRB}	Fig. 3	1.5			μs
DREQ Pulse Duration	T_{DREQ}	Fig. 4	1.5			μs
ROM Data Access Time (1)	T_{AC1}	f_{CT}=200kHz typ., Fig. 5, Note 1	26.0			μs
ROM Data Access Time (2)	T_{AC2}	f_{CT}=200kHz typ., Fig. 5, Note 1	26.0			μs
DREQ TO DOUT Delay Time	T_{SHFT}	Fig. 6	0.6			μs
DSEL TO D0–3 Delay Time	T_{DSEL}	Fig. 7	0.3			μs
Cycle Time	T_{CYCLE}	f_{CT}=200kHz typ., Fig. 8, Note 1	30.6			μs

Fig. 1 Input waveform at CT pin

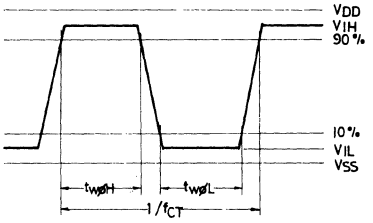
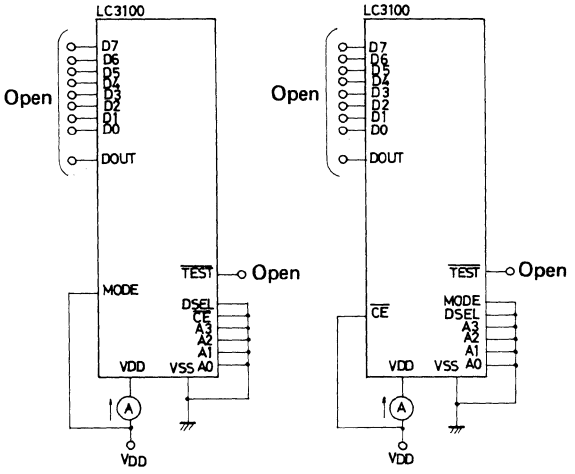


Fig. 2



I DD(1) Test Circuit I DD(2) Test Circuit

Fig. 3

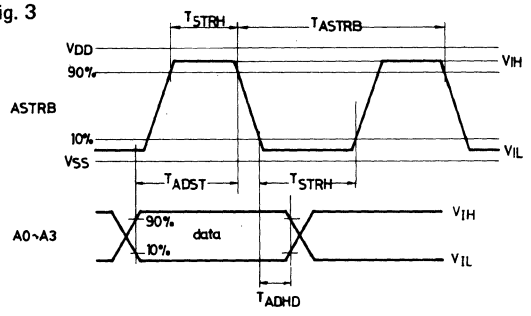
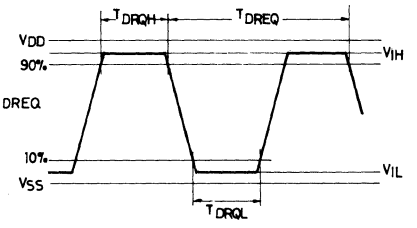
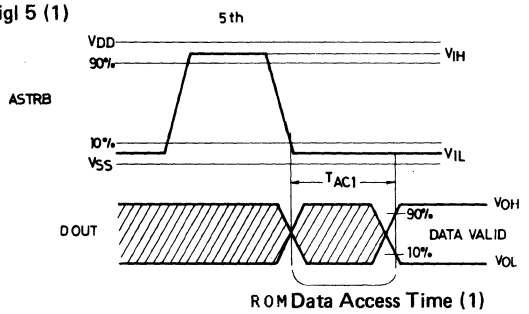


Fig. 4

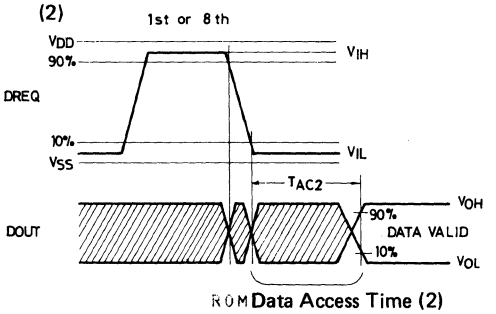


Figl 5 (1)



ROM Data Access Time (1)

(2)



ROM Data Access Time (2)

Fig. 6

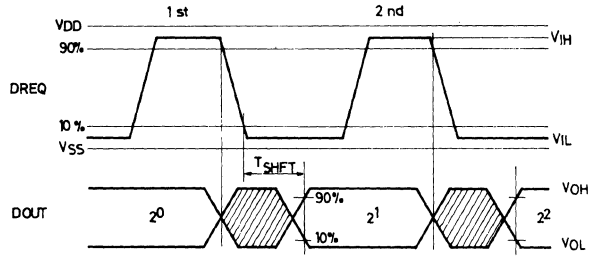


Fig. 7

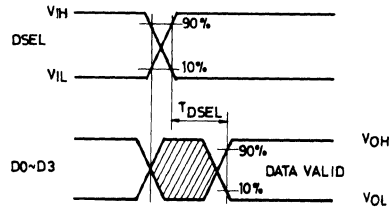
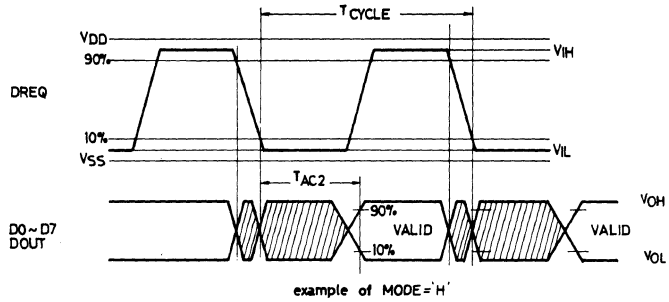


Fig. 8



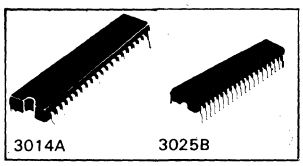
example of MODE='H'

Note 1 Use the following formulas to calculate T_{AC} max, Tcycle max for a given f_{CT}.

$$T_{AC}\ max = \frac{5000}{f_{CT}(kHz)} + 0.6\ \mu s \qquad T_{cycle}\ max = \frac{6000}{f_{CT}(kHz)} + 0.6\ \mu s$$

LC3101

C MOS LSI



128K-Bit CMOS Mask ROM

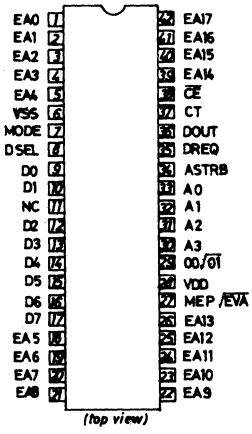
Ⓔ 1542

The LC3101 is a 128k-bit CMOS mask ROM that contains an interface connectable direct to the speech synthesizer LSI LC8100. With one piece of this mask ROM, approximately 100 seconds of speech synthesis can be attained. Since it also contains an interface connectable direct to an EPROM, speech synthesis can be attained by using this mask ROM and an EPROM jointly.
A selection of 8-bit, 4-bit, or single-bit output data is allowed by means of external control. This mask ROM is also suited for use in applications other than speech synthesis.

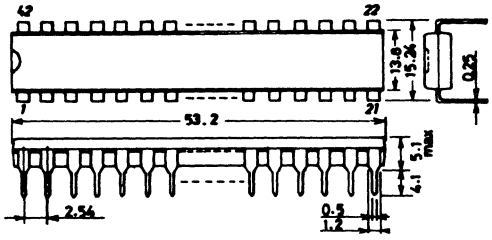
Features

- ROM capacity — 128K bits
- Access time — 25.6μsec typ (for operation at 200kHz typ.)
- Cycle time — 30.6μsec typ (for operation at 200kHz typ.)
- Function
  (1) Contains an interface to an EPROM.
  (2) Contains an interface to the LC8100 (speech synthesizer LSI).
  (3) Possible to select the bit length of output data.
  8-bit data
  4-bit data
  Single-bit data
- Low power dissipation — CMOS
- Current dissipation — 2mA max. (at operating mode)
  1μA max. (at nonoperating mode)
- Single +5V power supply — +2.7 to 6.0 V (supply voltage range)
- Package — DIP24

Pin Assignment

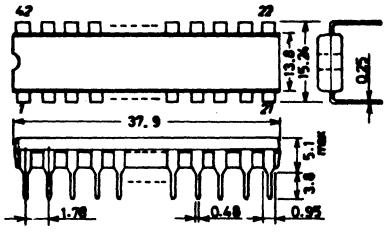


Case Outline 3014A-D42IC
(unit: mm)



SANYO: DIP42

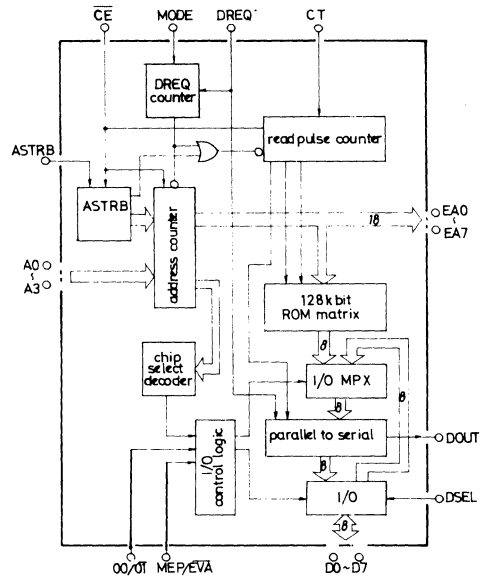
Case Outline 3025B-D42SIC
(unit: mm)



SANYO: DIP42S

Equivalent Circuit Block Diagram

A0 to A3:	18-bit address setting pins
ASTRB:	A0 to A3 strobe pin
DREQ:	ROM data request pin
DOUT:	ROM data serial output pin
CT:	Basic operation clock input pin
D0 to D7:	8-bit input/output pins
MODE:	DREQ pin input pulse count control pin
DSEL:	Output bit length select pin
$\overline{CE}$:	Power-down control pin
EA0 to EA17:	18-bit address output pins



Description of Operation of Internal Block

- ASTRB COUNTER: Block which internally sets address information applied in 5 steps from A0 to A3 pins.
- 18bit ADDRESS COUNTER: Address counter organized with 18 bits.
- READ PULSE COUNTER: Block which generates signal to operate address decoder, data selector.
- CHIP SELECT DECODER: Makes chip select signal with 2^{14} to 2^{17} bits of 18-bit address.
- 128kbit ROM MATRIX: ROM matrix cell organized with 128K bits.
- PARALLEL TO SERIAL: Shift register which serially outputs 8-bit parallel data to DOUT pin.
- I/O PORT: Selects input/output at D0 to D7 pins.

Pin Description

Pin No.	Pin Name	Input/output	Function
34	ASTRB	Input	Pin for inputting strobe signal which causes data A0 to A3 to be latched at address setting mode.
35	DREQ	Input	ROM data request signal input pin.
36	DOUT	Output	Pin for outputting ROM data serially. When used in conjunction with the LC8100, this pin is connected to DIN pin of the LC8100.
37	CT	Input	Pin for inputting basic operation clock of ROM inside. When used in conjunction with the LC8100, this pin is connected to CT pin of the LC8100.

Pin No.	Pin Name	Input/output	Function
38	$\overline{CE}$	Input	Pin for controlling initialization of LSI inside immediately after application of power and internal operation stop (power-down). For performing synthesization or ROM data read-out, set $\overline{CE}$ to 'L'.
6	V_{SS}	–	Connected to 0V of power supply.
28	V_{DD}	–	Connected to + side of power supply.
29	00/$\overline{01}$	Input	Always set to V_{SS}
7	MODE	Input	Pin for controlling number of input pulses at DREQ pin. When ROM data read-out is performed serially in a single bit, set MODE to 'L'. When ROM data read-out is performed in 8 bits or 4 bits, set MODE to 'H'.
8	DSEL	Input	Used when ROM data read-out is performed in 4 bits. When DSEL is set to 'H', 2^4 to 2^7 bits are outputted to D0 to D3 pins.
9	D0	Input/output	Pins for outputting ROM data in 8 bits and inputting data in 8 bits.
10	D1		
12	D2		
13	D3		
14	D4		
15	D5		
16	D6		
17	D7		
27	MEP/$\overline{EVA}$	Input	Open or connected to V_{DD}.
30	A3	Input	Pins for setting 18-bit address. At address setting mode, address information is inputted by 4 bits from high-order bit downward in 5 steps.
31	A2		
32	A1		
33	A0		
1	EA0	Output	18-bit address output pins.
2	EA1		
3	EA2		
4	EA3		
5	EA4		
18	EA5		
19	EA6		
20	EA7		
21	EA8		
22	EA9		
23	EA10		
24	EA11		
25	EA12		
26	EA13		
39	EA14		
40	EA15		
41	EA16		
42	EA17		

How to use the mask ROM and an EPROM jointly

The mask ROM and an external EPROM can be used jointly. Two selections of operation mode shown below are available by high-order 4 bits (EA14 to EA17) of 18-bit address.

Operation Mode Pins	D0 to D7	Operation
(1)	Output	The mask ROM contents are delivered at pins D0 to D7 and DOUT.
(2)	Input	The EPROM output contents are read in from pins D0 to D7 and are delivered at pin DOUT.

How to select the operation mode

The LC3101 contains a 4-bit chip select decoder (user option: Refer to "User mask"). Coincidence or uncoincidence with high-order 4 bits (EA14 to EA17) of 18-bit address is detected to select the operation mode.

Operation Mode	4bits of Chip Select Decoder	Operation of LC3101
(1)	Coincidence with EA14 to EA17	Pins D0 to D7: Output mode Mask ROM read enable mode
(2)	Uncoincidence with EA14 to EA17	Pins D0 to D7: Input mode Mask ROM read inhibit mode

Fig. 1 shows the schematic diagram of the control section related to these operation modes. Fig. 2 shows the assignment of 256k-byte (128k bits x 16) that can be specified by 18-bit address.

Fig. 1 Schematic Diagram of Control Section

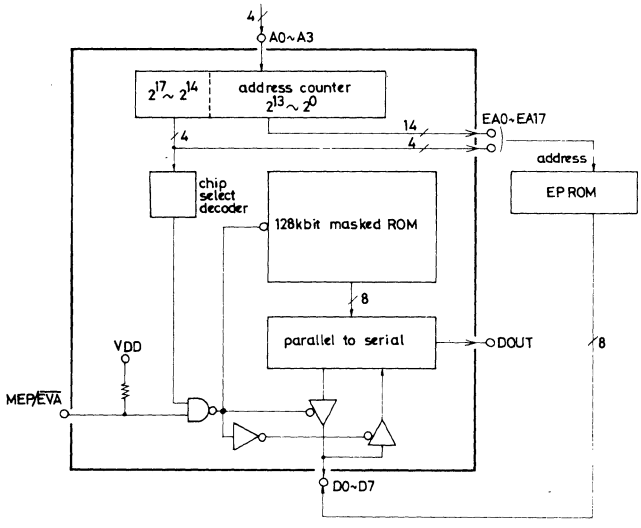
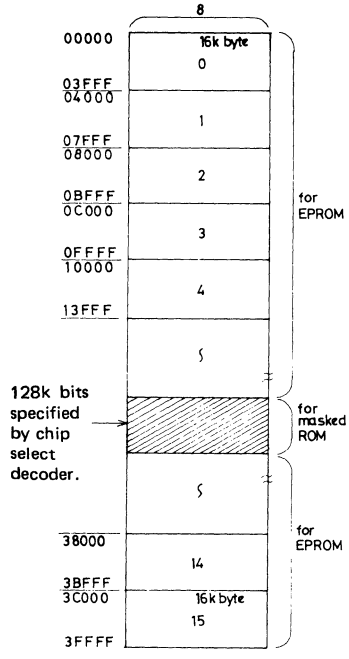
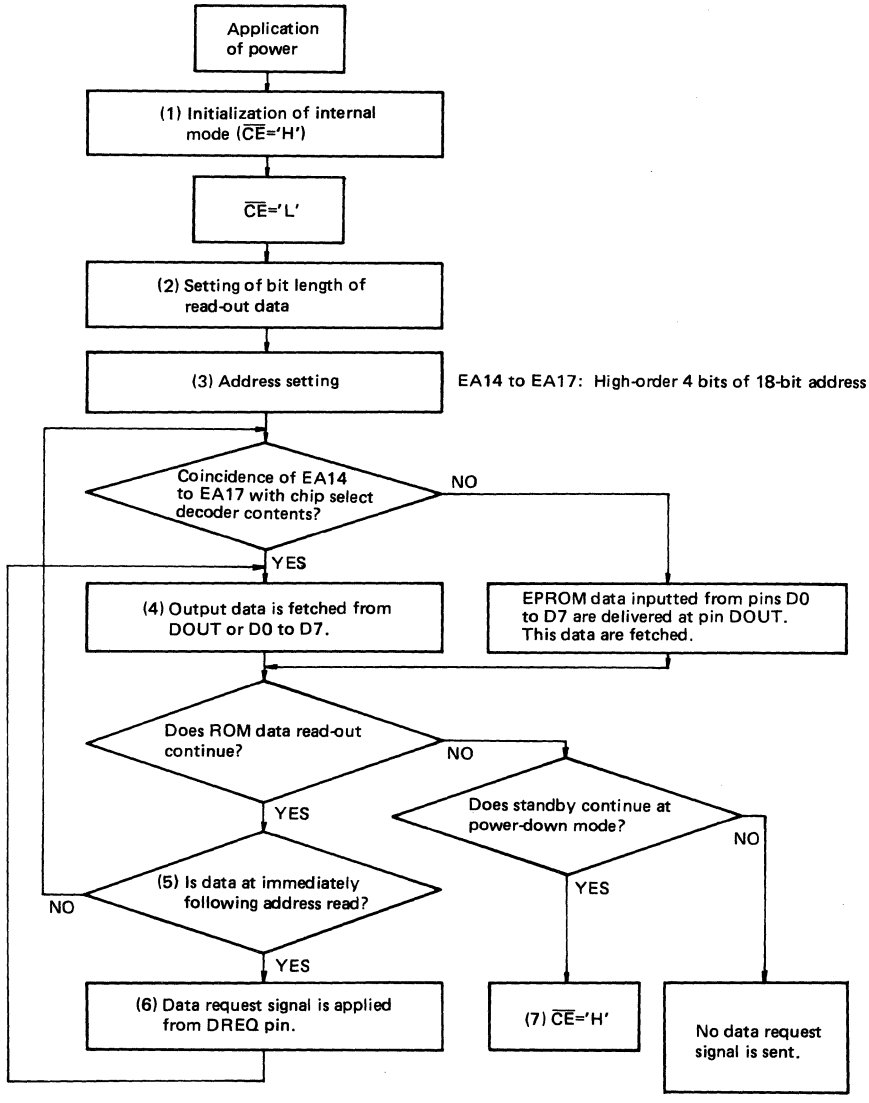


Fig. 2 Address Space Assignement



ROM Data Read-out Procedure

The following flowchart shows the outline of read-out procedure. (1) to (7) give a more detailed description.



(1) Initialization of internal mode

There are 4 counter blocks (ASTRB counter, 18-bit ADDRESS counter, READ PULSE counter, DREQ counter) inside the LC3101. Since initialization is required immediately after application of power, apply one 'H' level pulse to $\overline{CE}$ pin. When $\overline{CE}$ is set to 'L' level, the power-down mode is released (refer to (7)) and it is possible to start read-out any time.

(2) Setting of bit length of read-out data

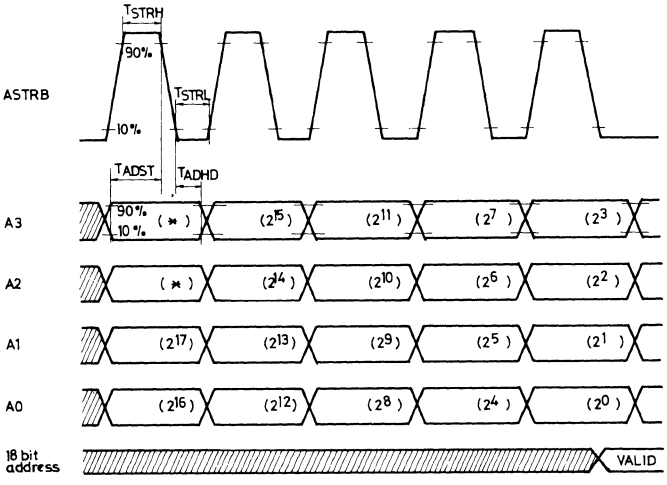
For the bit length of ROM data output, a selection of 3 lengths is allowed: 8 bits, 4 bits, and a single bit. For controlling this selection, MODE, DSEL pins are used. The following Table shows 3 types of pin setting.

DSEL \ MODE	'L'	'H'
'L'	Single-bit length (speech synthesis)	8-bit or 4-bit length or 4-bit length (Note)
'H'	–	4-bit length (Note)

(Note) When DSEL is set to 'L', 2^0 to 2^3 bits are outputted at D0 to D3 pins.
When DSEL is set to 'H', 2^4 to 2^7 bits are outputted at D0 to D3 pins.

(3) Address setting

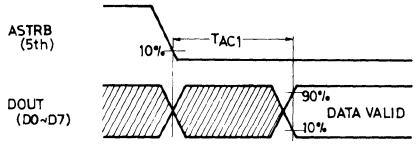
Apply 5 successive pulses to ASTRB pin. Synchronously with these pulses apply 18-bit address information to A0 to A3 pins from high-order bit downward by 4 bits in 5 steps. At this address setting mode DREQ pin must be set to 'L' level. Shown below is the timing.



(Note)
- "*"=don't care.
- "2n"=Binary number at the nth bit to be set in address counter.
- For the numeric values of T_{STRH}, T_{STRL}, T_{ADST}, T_{ADHS}, refer to Electrical Characteristics.

Start of read-out of set address data

Read-out of ROM data starts at the falling of the 5th ASTRB pulse or the first (MODE='H') or the 8th (MODE='L') DREQ pulse, and when access time T_{AC1} has elapsed 2^0 bit is outputted at DOUT pin and 2^0 to 2^7 data are outputted at D0 to D7 pins. (Refer to the following Timing Chart.)
Note) For the numeric value of T_{AC1}, refer to Electrical Characteristics.

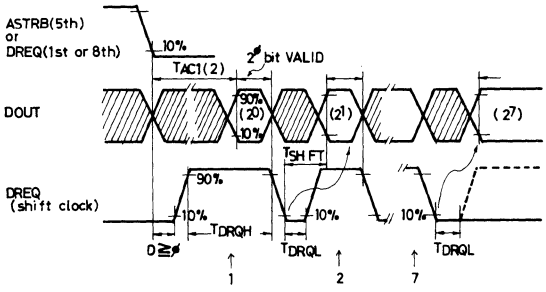


(4) Fetching of output data

As shown above, whenever access time T_{AC1} has elapsed, data can be fetched from output ports DOUT or D0 to D7 pins. (Pin setting as shown in Table in (2) is required.)

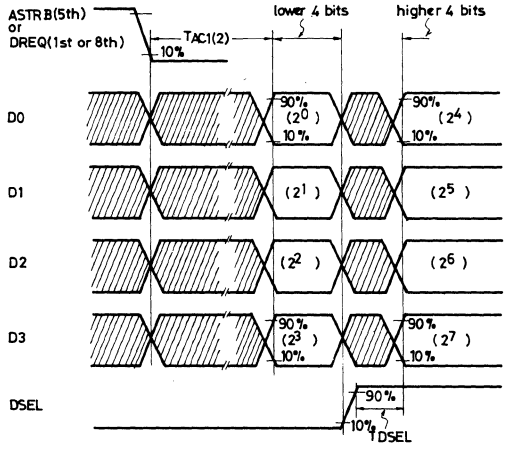
Counting one byte in a single bit from DOUT pin

Count a single bit (2^n bit) from DOUT pin. To count the following single bit (2^{n+1} bit), apply a shift clock to DREQ pin. Shown below is Timing Chart.
For the numeric values of T_{AC1}, T_{DRQH}, T_{SHFT}, refer to Electrical Characteristics.



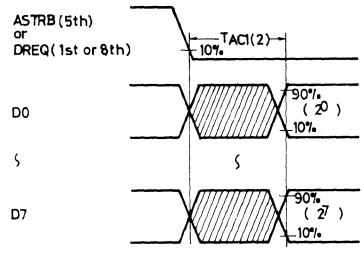
Counting one byte in 4-bits from D0 to D3 pins

In accordance with Table and (Note) in (2), fetch one byte from D0 to D3 pins by 4 bits in 2 steps. Shown below is Timing Chart.



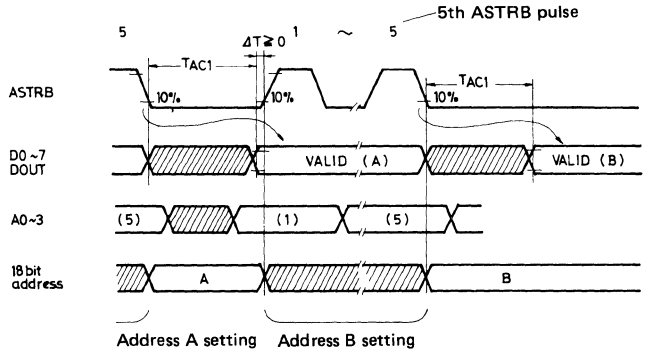
Counting one byte in 8 bits from D0 to D7 pins

Fetch 8 bits from D0 to D7 pins. Shown below is Timing Chart.

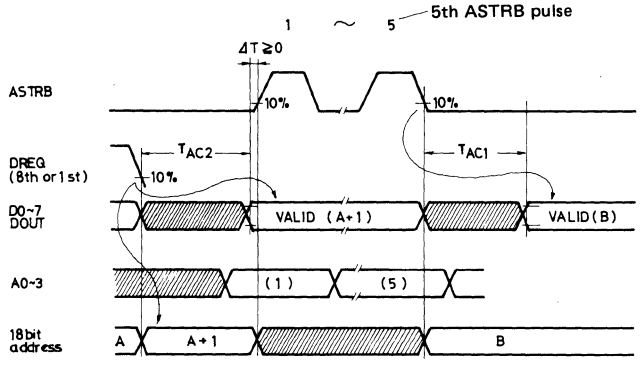


(5) Setting address again and counting data

(1) Timing for application of ASTRB pulse when address A is set and read out and then address B is set and read out.



(2) Timing for application of ASTRB pulse when data is read out by application of DREQ signal (refer to (6) below) and then address B is set and read out.



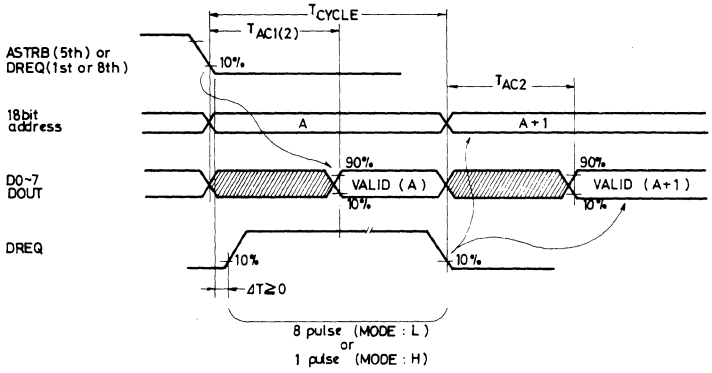
(6) Request of ROM data at the following address

When the signal shown below is applied to the LSI, the LSI begins to read out data at the address immediately following the address at which preceding data is read out.

Falling of 8th DREQ pulse (MODE='L')

Falling of 1st DREQ pulse (MODE='H')

Shown below is Timing Chart.



Note) Apply ROM data request signal after T_{CYCLE} or more has elapsed.
For the numeric value of T_{CYCLE}, refer to Electrical Characteristics.

(7) Power-down mode

When the input at $\overline{CE}$ pin is set to 'H' level, the LC3101 enters power-down mode (each block inside the LSI stops its operation, with no unnecessary current dissipated.). At this mode, the LSI inside becomes as follows and current dissipation is reduced.

(1) Input at input ports (ASTRB, DREQ, A0 to A3) is inhibited.
(It should be noted that if input is floating, current dissipation increases.)

(2) Both address decoder and data selector in 128K-bit ROM matrix stop their internal operation.

(3) Output at 3-state output pins DOUT, D0 to D7 is floating or fixed. (The user can select either of the two. Refer to "User mask") When $\overline{CE}$ is set to 'H', in addition to reduction in current dissipation as mentioned above, 4 internal counters (ASTRB COUNTER, 18-BIT ADDRESS COUNTER, READ PULSE COUNTER, DREQ COUNTER) are initialized in readiness for read-out after power-down mode release ($\overline{CE}$='L').

User mask

(1) CHIP SELECT DECODER

User mask option which makes LSI chip select signal (select, nonselect) with 2^{14} to 2^{17} bits of 18-bit addresses. Shown below is the output modes including $\overline{CE}$ pin conditions.

	$\overline{CE}$='L'	$\overline{CE}$='H' (Power-down)
Chip select	DATA is outputted from DOUT, D0 to D7 pins.	Data immediately before $\overline{CE}$='H' occurs is held and outputted. (Note)
Chip nonselect	Output at DOUT, D0 to D7 pins has a high impedance.	Output at DOUT, D0 to D7 pins has a high impedance.

Note) In this case, the LSI only, having CHIP SELECT DECODER whose 2^{14} to 2^{17} bits are all 0, outputs data and all others have a high impedance.

(2) SW mask

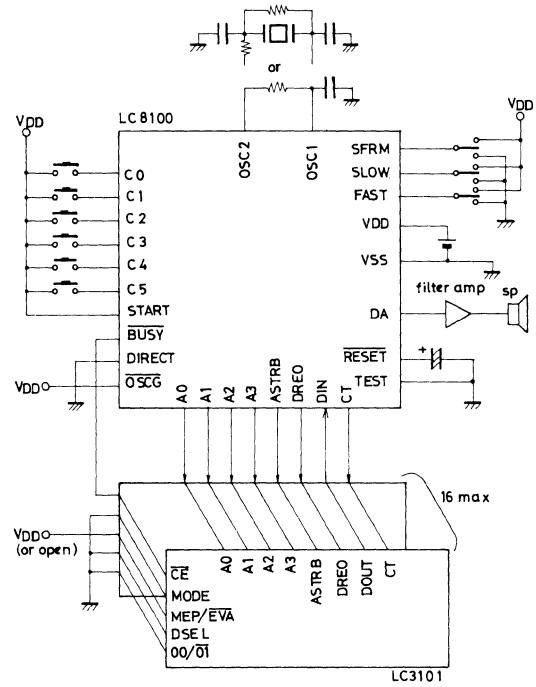
SW mask controls output at DOUT, D0 to D7 output pins in the following two ways at power-down mode. The user can select either of the two beforehand.

(i) Output at DOUT, D0 to D7 pins is set to a high impedance.

(ii) Data immediately before power-down mode is held and outputted.

Sample Application Circuit (1)

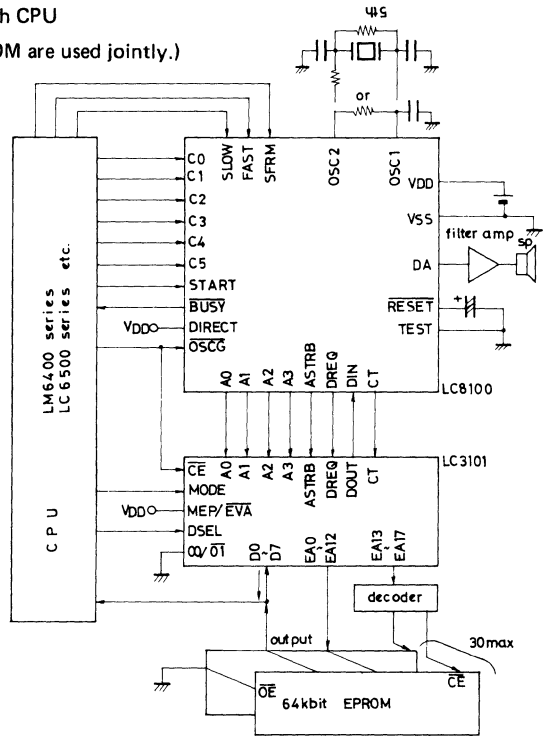
One word to one key correspondence



Sample Application Circuit (2)

CPU control: Edit and synthesis with CPU

(The mask ROM and a 64k-bit EPROM are used jointly.)



Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DD} max	V_{DD} pin	−3.0 to +7.0	V
Input Voltage	V_{IN}	All input pins	−0.3 to V_{DD}+0.3	V
Output Voltage	V_O	All output pins	−0.3 to V_{DD}+0.3	V
Output Current	I_O	All output pins, per pin	−2.0 to +2.0	mA
Allowable Power Dissipation	P_d max	T_a=−30 to +70°C	200	mW
Operating Temperature	T_{opg}		−30 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Allowable Operating Ranges at T_a=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 6.5V			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD} pin	4.5	5.0	6.5	V
Input 'H'-Level Voltage	$V_{IH(1)}$	All input pins other than D0 to D7	0.7V_{DD}			V
	$V_{IH(2)}$	D0 to D7 pins	2.2			V
Input 'L'-Level Voltage	$V_{IL(1)}$	All input pins other than D0 to D7			0.3V_{DD}	V
	$V_{IL(2)}$	D0 to D7 pins			0.6	V
Operating Clock Frequency	f_{CT}	Fig. 1, T_a=−30 to +60°C	150	800	960	kHz
Operating Clock 'H'-Level Pulse Width	t_{wOH}	Fig. 1	0.3			μs
Operating Clock 'L'-Level Pulse Width	t_{wOL}	Fig. 1	0.47			μs

Electrical Characteristics at T_a=−30 to +70°C, V_{DD}=4.5 to 6.5V, V_{SS}=0V			min	typ	max	unit
Input 'H'-Level Current	I_{IH}	V_{IN}=V_{DD}			1.0	μA
Input 'L'-Level Current	I_{IL}	V_{IN}=V_{SS}	−1.0			μA
Output 'H'-Level Voltage	V_{OH}	I_{OH}=−0.3mA	V_{DD}−0.6			V
Output 'L'-Level Voltage	V_{OL}	I_{OH}=0.3mA			0.6	V
Output OFF Leak Current	I_{OFF1}	V_O=V_{DD}, D0 to D7, D_{OUT} pin			1.0	μA
	I_{OFF2}	V_O=V_{SS}, D0 to D7, D_{OUT} pin	−1.0			μA
Input Pin Capacitance	C_I			5	10	pF
Pull-up Resistance	R_{up}	Each pin of MEP/$\overline{EVA}$, 00/$\overline{01}$	20		1000	kΩ
Current Dissipation	$I_{DD(1)}$	At operating mode, f_{CT}=960kHz, Fig. 2			2.0	mA
	$I_{DD(2)}$	At nonoperating mode, T_a=−30 to +50°C, Fig. 2			1.0	μA

AC Characteristics at T_a=−30 to +70°C, V_{DD}=4.5 to 6.5V, V_{SS}=0V, R_L=200kohm, CP=50pF			min	typ	max	unit
Address Setup Time	T_{ADST}	Fig. 3	0.3			μs
Address Hold Time	T_{ADHD}	Fig. 3	0.3			μs
ASTRB 'H'-Level Pulse Width	T_{STRH}		0.3			μs
ASTRB 'L'-Level Pulse Width	T_{STRL}		0.3			μs
DREQ 'H'-Level Pulse Width	T_{DRQH}		0.3			μs
DREQ 'L'-Level Pulse Width	T_{DRQL}		0.3			μs
ASTRB Pulse Duration	T_{ASTRB}	Fig. 3	1.5			μs
DREQ Pulse Duration	T_{DREQ}	Fig. 4	1.5			μs
ROM Data Access Time (1)	T_{AC1}	f_{CT}=200kHz typ., Fig. 5, Note 1	26.0			μs
ROM Data Access Time (2)	T_{AC2}	f_{CT}=200kHz typ., Fig. 5, Note 1	26.0			μs
DREQ TO D_{OUT} Delay Time	T_{SHFT}	Fig. 6	0.6			μs
DSEL TO D0–3 Delay Time	T_{DSEL}	Fig. 7	0.3			μs
Cycle Time	T_{CYCLE}	f_{CT}=200kHz typ., Fig. 8, Note 1	30.6			μs

Fig. 1 Input waveform at CT pin

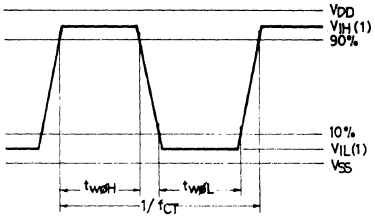
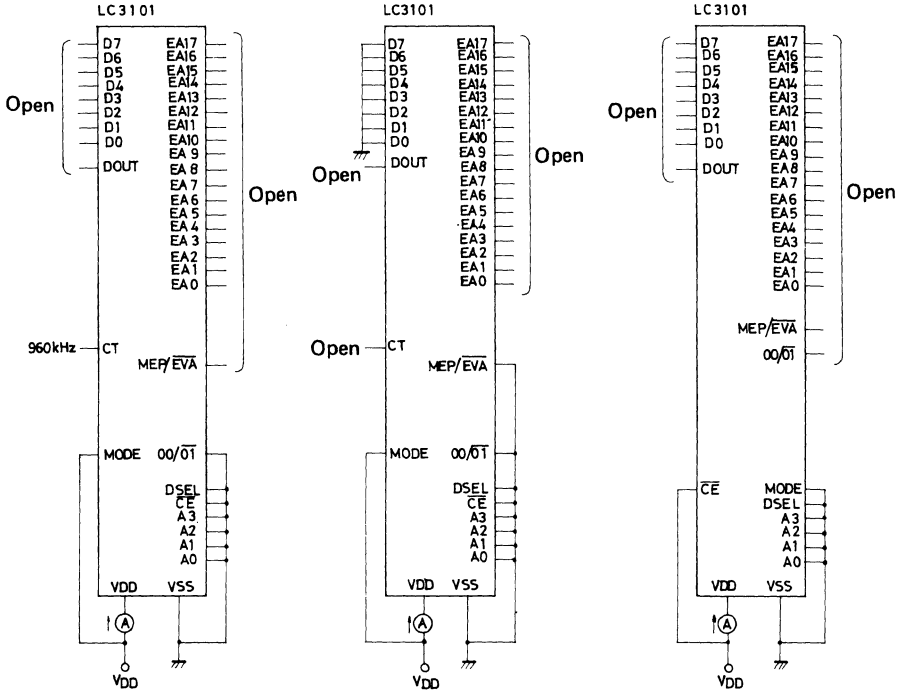


Fig. 2



$I_{DD(1)}$ Test Circuit (A) $I_{DD(1)}$ Test Circuit (B) $I_{DD(2)}$ Test Circuit

Fig. 3

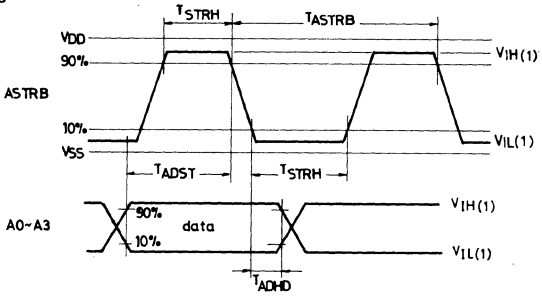


Fig. 4

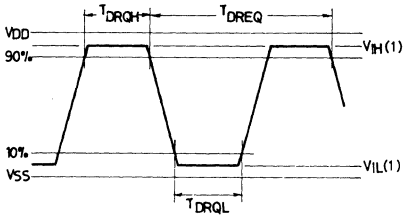
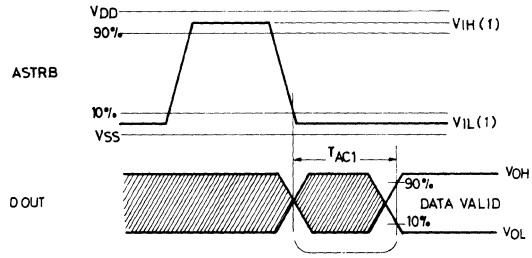
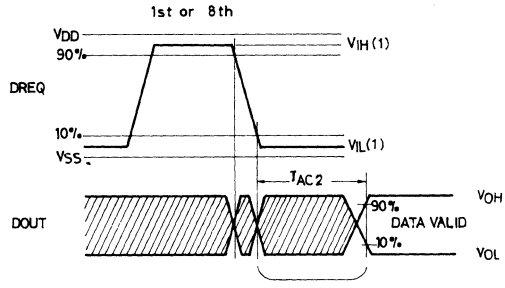


Fig. 5 (1)



ROM Data Access Time (1)

Fig. 5 (2)



ROM Data Access Time (2)

Fig. 6

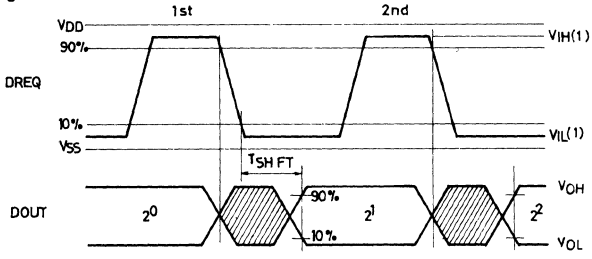


Fig. 7

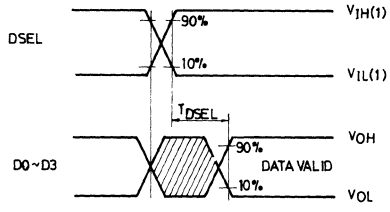
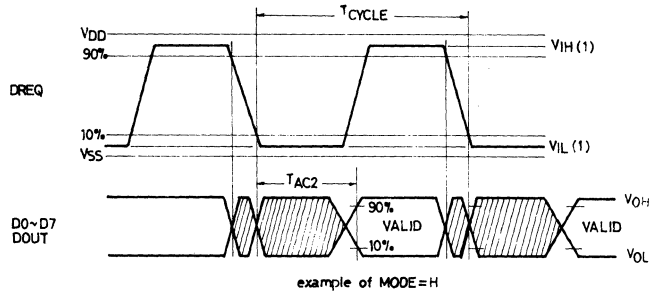


Fig. 8

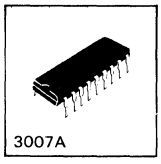


example of MODE=H

Note 1 Use the following formulas to calculate T_{AC} max, Tcycle max.

$$T_{AC}\ max = \frac{5000}{f_{CT}(kHz)} + 0.6\ \mu s \qquad T_{cycle}\ max = \frac{6000}{f_{CT}(kHz)} + 0.6\ \mu s$$

LC3514, 3514L



C MOS LSI

1024 Words by 4 Bits High-Speed CMOS Static RAM

Ⓔ 1525

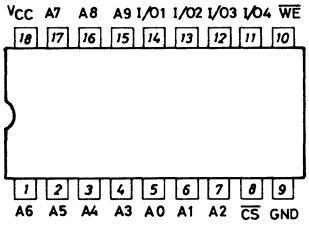
General Description

The LC3514/LC3514L are nonclocked CMOS static RAM's organized as 1024 words x 4 bits. They are compatible with worldwide standard N-channel 2114-type 4K SRAM's and have a complete CMOS circuit configuration.
With the current dissipation being low at the data hold mode or standby mode and the access time being so short as 200ns (max.), they are especially suited for use in memory systems which require a high speed and low power dissipation and battery-powered portable systems. For the LC3514L, a standby current of 1uA max. is guaranteed at 60°C.

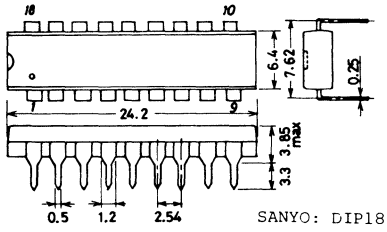
Features

- Wide speed: Address access time (t_{AA})=200ns(max)
- Low standby current
  - 1 uA(max) at Ta=60°C : LC3514L
  - 50uA(max) : LC3514
- Low data hold current.
  - 0.8uA(max) at Ta=60°C : LC3514L
  - 10uA(max) : LC3514
- Single 5V supply : 5V±10%
- Data hold supply voltage : V_{CCBB}=2.0 to 5.5V
- No clock required (Complete static memory)
- Directly TTL compatible: All inputs and outputs.
- Common data input and output using 3-state outputs.
- The output data has the same polarity as the input data.
- High-density 18-pin package.
- Pin-out compatible with 2114 NMOS RAM

Pin Assignment

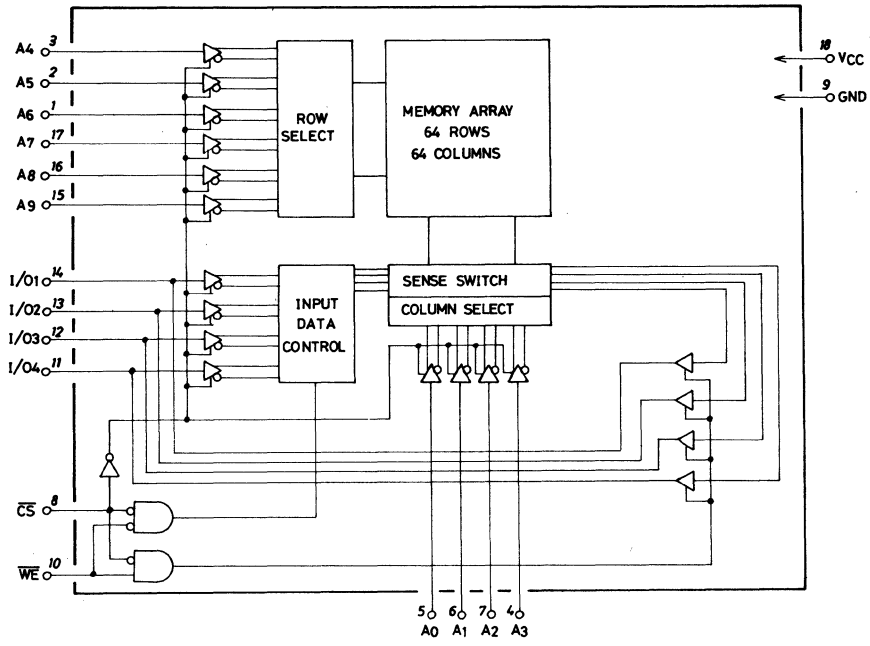


Case Outline 3007A-D18IC
(unit:mm)



SANYO: DIP18

Block Diagram



Absolute Maximum Ratings at Ta=+25°C			unit
Input Pin Voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
I/O Pin Voltage	$V_{I/O}$	-0.3 to V_{CC}+0.3	V
Maximum Supply Voltage	V_{CC}max	+8.0	V
Allowable Power Dissipation	Pdmax	400	mW
Operating Temperature	Topg	-30 to +85	°C
Storage Temperature	Tstg	-55 to +125	°C

DC Allowable Operating Current at Ta=-30 to +85°C		min	typ	max	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input "H" Level Voltage	V_{IH}	2.4		V_{CC}+0.3	V
Input "L" Level Voltage	V_{IL}	-0.3		0.8	V

DC Electrical Characteristics at Ta=-30 to +85°C, V_{CC}=5V±10%			min	typ	max	unit
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	-1.0		1.0	uA
I/O Leakage Current	I_{LO}	$V_{\overline{CS}}$=V_{IH}, $V_{I/O}$=0 to V_{CC}	-1.0		1.0	uA
Power Supply Current	I_{CCA1}	$V_{\overline{CS}}$=V_{IL}, V_{IN}=V_{CC}, I/O=open			35	mA
	I_{CCA2}	$V_{\overline{CS}}$=V_{IL}, V_{IN}=2.4V, I/O=open			40	mA
	I_{CCA3}	V_{IN}=0 or V_{CC}, I/O=open, f=1MHz $\overline{CS}$ Duty 50%			20	mA
Standby Power Supply Current	I_{CCS}	$V_{\overline{CS}}$=V_{CC}, V_{IN}=0 to V_{CC} LC3514			50	uA
		(Ta=60°C) LC3514L			1	uA
Output "H" Level Voltage	V_{OH}	I_{OH}=-1.0mA	2.4			V
Output "L" Level Voltage	V_{OL}	I_{OL}=2.0mA			0.4	V

Input/Output Capacitance at Ta=+25°C, f=1MHz			min	typ	max	unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V			10	pF
Input Capacitance	C_{IN}	$V_{I/O}$=0V			5	pF

AC Electrical Characteristics at $V_{CC}=5V\pm10\%$, Ta=-30 to +85°C

1. AC Test Conditions

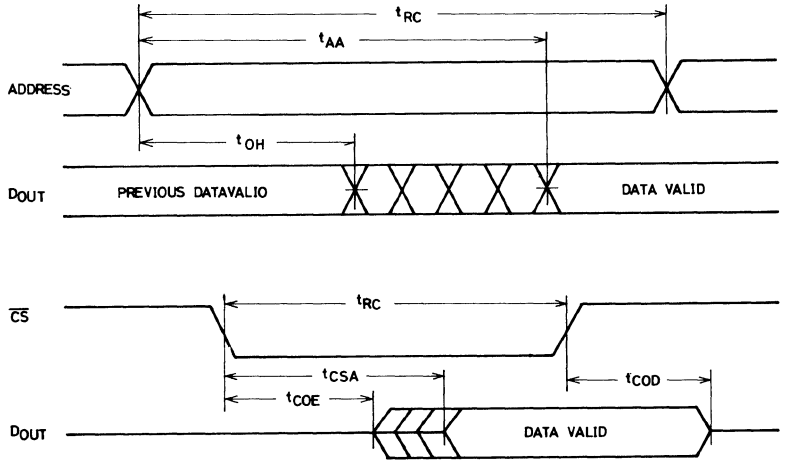
Input Pulse Voltage Level	0.8V to 2.4V
Input Rise/Fall Time	10ns
Input/Output Timing Level	1.5V
Output Load	1TTL gate + C_L=100pF

2. Read Cycle

		min	typ	max	unit
Cycle Time	t_{RC}	200			ns
Address Access Time	t_{AA}			200	ns
Chip Select Access Time*1	t_{CSA1}			200	ns
Chip Select Access Time*2	t_{CSA2}			250	ns
Output Data Hold Time	t_{OH}	20			ns
Chip Select - Output Enable Time	t_{COE}	15			ns
Chip Select - Output Disable Time	t_{COD}			60	ns

*1 t_{CSA1} applies when the nonselect time of $\overline{CS}$ is more than 100ns.
*2 t_{CSA2} applies when the nonselect time of $\overline{CS}$ is 100ns or less.

Read Cycle Timing (1)

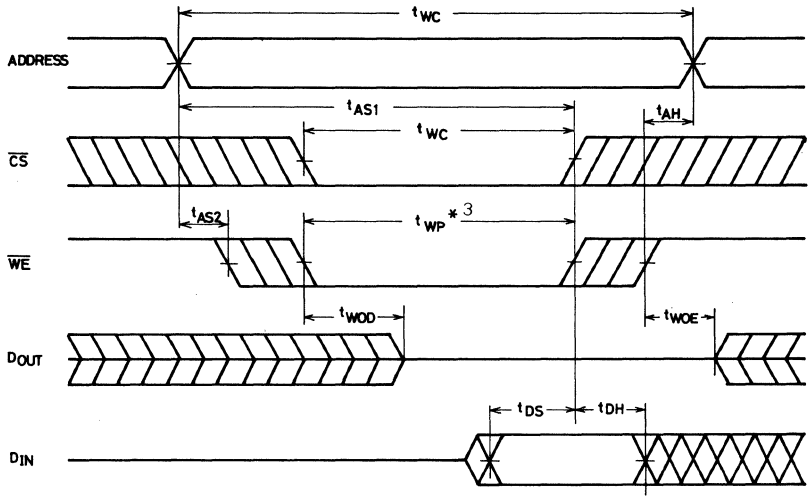


Note(1) WE is high for a read cycle.

3. Write Cycle

		min	typ	max	unit
Cycle Time	t_{WC}	200			ns
$\overline{CS}$ - Setup Time	t_{CW}	180			ns
Address Setup Time (1)	t_{AS1}	180			ns
Address Setup Time (2)	t_{AS2}	0			ns
Write Pulse Width	t_{WP}*3	180			ns
Address Hold Time	t_{AH}	0			ns
Data Setup Time	t_{DS}	120			ns
Data Hold Time	t_{DH}	0			ns
$\overline{WE}$ - Output Disable Time	t_{WOD}			60	ns
$\overline{WE}$ - Output Enable Time	t_{WOE}	0			ns

Write Cycle Timing



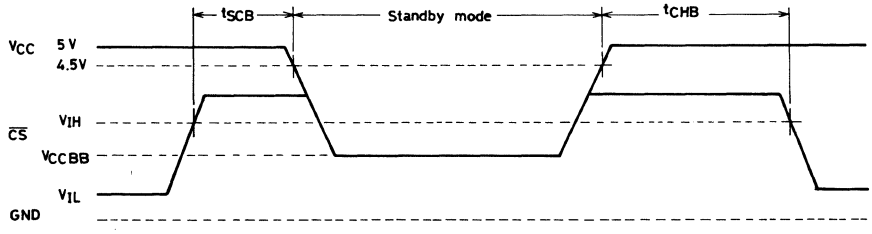
*3 t_{WP} occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

Low Supply Voltage Data Hold Characteristics at Ta=-30 to +85°C

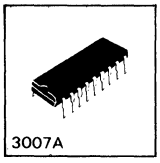
				min	typ	max	unit
Data Hold Supply Voltage	V_{CCBB}	V_{IN}=GND or V_{CC}, $V_{\overline{CS}}=V_{CC}$		2.0		5.5	V
Data Hold Power Supply Current	I_{CCBB}	V_{IN}=GND or V_{CC}, $V_{\overline{CS}}=V_{CC}$, V_{CC}=3.0V	LC3514			10	uA
			LC3514L (Ta=60°C)			0.8	uA
$\overline{CS}$ Setup Time	t_{CSB}			0			ns
$\overline{CS}$ Hold Time	t_{CHB}			t_{RC}*4			ns

*4 t_{RC} : Read cycle time

Data Hold Timing Chart



LC3514D, 3514E



C MOS LSI

1024 Words by 4 Bits CMOS Static RAM

Ⓔ 1526

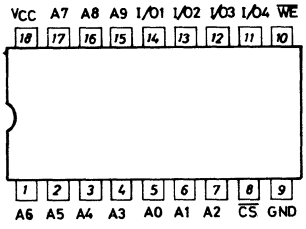
General Description

The LC3514D/LC3514E are nonclocked CMOS static RAM's organized as 1024 words x 4 bits. They are compatible with worldwide standard N-channel 2114-type 4K SRAM's and have a complete CMOS circuit configuration.
With the current dissipation being low at the data hold mode or standby mode and the operating voltage range being wide, they are especially suited for use in CMOS microcomputers, battery-powered portable systems using a CMOS logic IC, and nonvolatile memories at the battery backup mode. For the LC3514D, an operating voltage of 3.0V min. and a standby current of 1uA max. are guaranteed at 45°C.

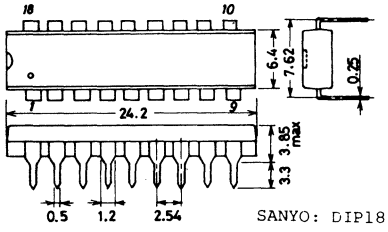
Features

- Wide operating voltage range.
  - V_{CC}=3.0 to 6.0V : LC3514D
  - V_{CC}=3.6 to 6.0V : LC3514E
- Low standby current.
  - 1 uA(max) at Ta=45°C : LC3514D
  - 10uA(max) at Ta=45°C : LC3514E
- Low data hold current.
  - 1 uA(max) at Ta=45°C : LC3514D
  - 5 uA(max) at Ta=45°C : LC3514E
- Data hold supply voltage. : V_{CCBB}=2.0 to 6.0V
- No clock required (Complete static memory).
- Directly TTL compatible: All inputs and outputs.
- Common data input and output using 3-state outputs.
- The output data has the same polarity as the input data.
- High-density 18-pin package.
- Pin-out compatible with 2114 NMOS RAM

Pin Assignment

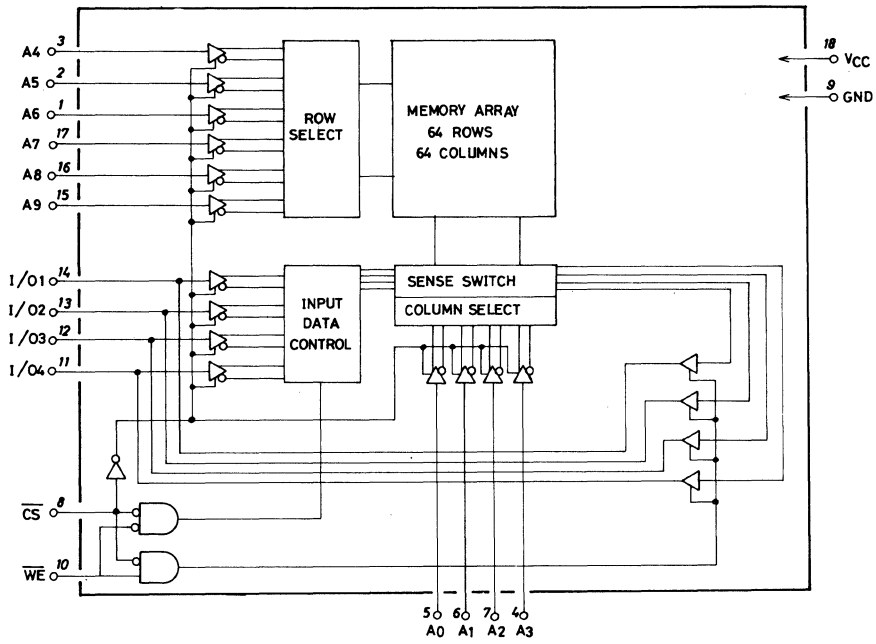


Case Outline 3007A-D18IC
(unit:mm)



SANYO: DIP18

Block Diagram



Absolute Maximum Ratings at Ta=+25°C

			unit
Input Pin Voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
I/O Pin Voltage	$V_{I/O}$	-0.3 to V_{CC}+0.3	V
Maximum Supply Voltage	V_{CC}max	+8.0	V
Allowable Power Dissipation	Pdmax	400	mW
Operating Temperature	Topg	-30 to +85	°C
Storage Temperature	Tstg	-55 to +125	°C

DC Allowable Operating Conditions at Ta=0 to +45°C

			min	typ	max	unit
Supply Voltage	V_{CC}	LC3514D	3.0	5.0	6.0	V
		LC3514E	3.6	5.0	6.0	V
Input "H" Level Voltage	V_{IH}		2.7		V_{CC}+0.3	V
Input "L" Level Voltage	V_{IL}		-0.3		0.4	V

DC Electrical Characteristics at Ta=0 to +45°C, V_{CC}=3.0 to 6.0(LC3514D), V_{CC}=3.6 to 6.0V(LC3514E)

				min	typ	max	unit
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}		-1.0		1.0	uA
I/O Leakage Current	I_{LO}	$V_{\overline{CS}}$=V_{IH}, $V_{I/O}$=0 to V_{CC}		-1.0		1.0	uA
Power Supply Current	I_{CCA1}	$V_{\overline{CS}}$=V_{IL}, V_{IN}=V_{CC}, I/O=open				35	mA
	I_{CCA2}	$V_{\overline{CS}}$=V_{IL}, V_{IN}=2.4V, I/O=open				40	mA
	I_{CCA3}	V_{IN}=0orV_{CC}, I/O=open, f=1MHz, $\overline{CS}$ Duty 50%				20	mA
Standby Power Supply Current	I_{CCS}	$V_{\overline{CS}}$=V_{CC}, V_{IN}=0toV_{CC}	LC3514D			1	uA
			LC3514E			10	uA
Output "H" Level Voltage	V_{OH}	I_{OH}=-100uA		2.4			V
Output "L" Level Voltage	V_{OL}	I_{OL}=1.0mA				0.4	V

Input/Output Capacitance at Ta=+25°C,f=1MHz

			min	typ	max	unit
Input/output Capacitance	$C_{I/O}$	$V_{I/O}$=0V			10	pF
Input Capacitance	C_{IN}	$V_{I/O}$=0V			5	pF

AC Electrical Characteristics at Ta=0 to +45°C,V_{CC}=3.0 to 6.0V(LC3514D),V_{CC}=3.6 to 6.0V(LC3514E)

1.AC Test Conditions

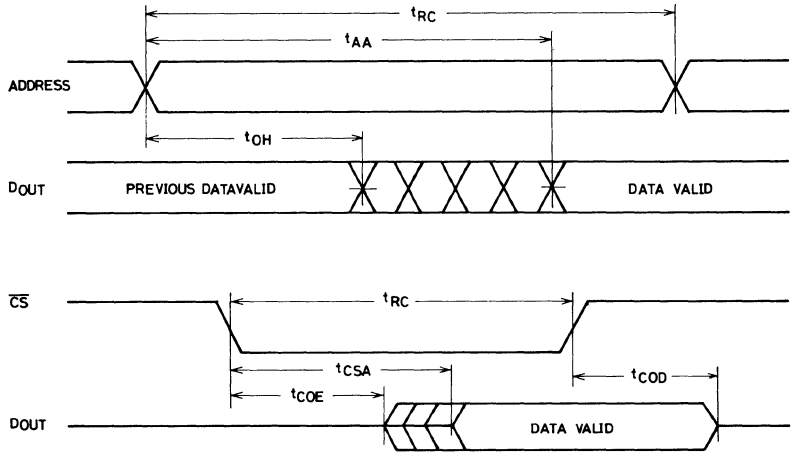
Input Pulse Voltage Level	0.4V to 2.7V
Input Rise/Fall Time	10ns
Input/Output Timing Level	1.5V
Output Load	1TTL gate + C_L=100pF

2.Read Cycle

		min	typ	max	unit
Cycle Time	t_{RC}	2.0			us
Address Access Time	t_{AA}			2.0	us
Chip Select Access Time*1	t_{CSA1}			2.0	us
Chip Select Access Time*2	t_{CSA2}			2.0	us
Output Data Hold Time	t_{OH}	10			ns
Chip Select - Output Enable Time	t_{COE}	20			ns
Chip Select - Output Disable Time	t_{COD}			500	ns

*1 t_{CSA1} applies when the nonselect time of $\overline{CS}$ is more than 100ns.
*2 t_{CSA2} applies when the nonselect time of $\overline{CS}$ is 100ns or less.

Read Cycle Timing (1)

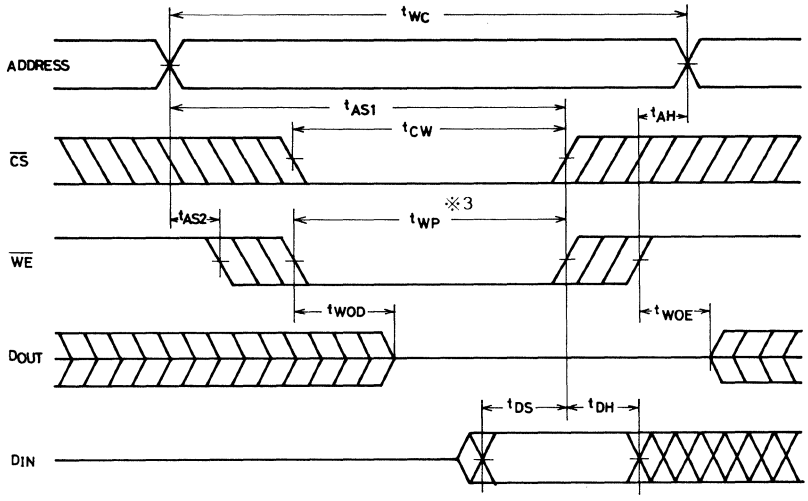


Note(1) $\overline{WE}$ is high for a read cycle.

3.Write Cycle

		min	typ	max	unit
Cycle Time	t_{WC}	2.0			us
$\overline{CS}$ - Setup Time	t_{CW}	1.5			us
Address Setup Time (1)	t_{AS1}	1.5			us
Address Setup Time (2)	t_{AS2}	100			ns
Write Pulse Width	t_{WP}*3	1.5			us
Address Hold Time	t_{AH}	100			ns
Data Setup Time	t_{DS}	1.0			us
Data Hold Time	t_{DH}	100			ns
$\overline{WE}$ - Output Disable Time	t_{WOD}			500	ns
$\overline{WE}$ - Output Enable Time	t_{WOE}	0			ns

Write Cycle Timing

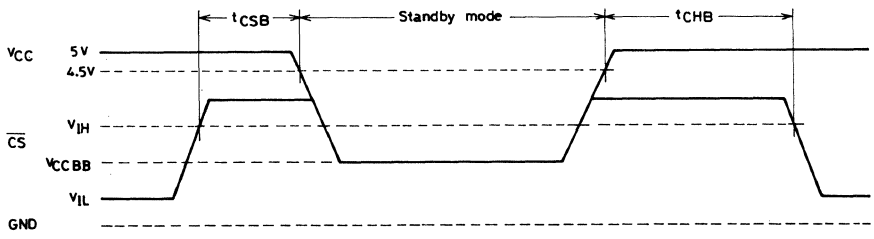


#3 t_{WP} occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

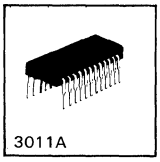
Low Supply Voltage Data Hold Characteristics at Ta=0 to +45°C			min	typ	max	unit
Data Hold Supply Voltage	V_{CCBB}	V_{IN}=GND or V_{CC}, $V_{\overline{CS}}=V_{CC}$	2.0		6.0	V
Data Hold Power Supply Current	I_{CCBB}	V_{IN}=GND or V_{CC}, $V_{\overline{CS}}=V_{CC}$, V_{CC}=3.0V	LC3514D		1	uA
			LC3514E		5	uA
$\overline{CS}$ Setup Time	t_{CSB}		0			ns
$\overline{CS}$ Hold Time	t_{CHB}		t_{RC}#4			ns

#4 t_{RC} : Read cycle time

Data Hold Timing Chart



LC3516



C MOS LSI

2048 Words by 8-Bits CMOS Static RAM

Ⓔ 1554

The LC3516 is an unclocked high-speed static CMOS static RAM that is organized as 2048 words x 8 bits and operates from a single 5V supply. It has two inputs: $\overline{CE1}$ input (chip enable input) for high-speed access and $\overline{CE2}$ input for battery applications where the whole circuit enters the standby mode with less current dissipated. It is especially suited for use in applications where battery-powered operation, battery backup operation as well as high-speed access are required.

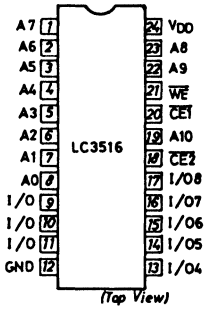
Applications

- Battery-powered portable set.
- Battery backup nonvolatile memory.

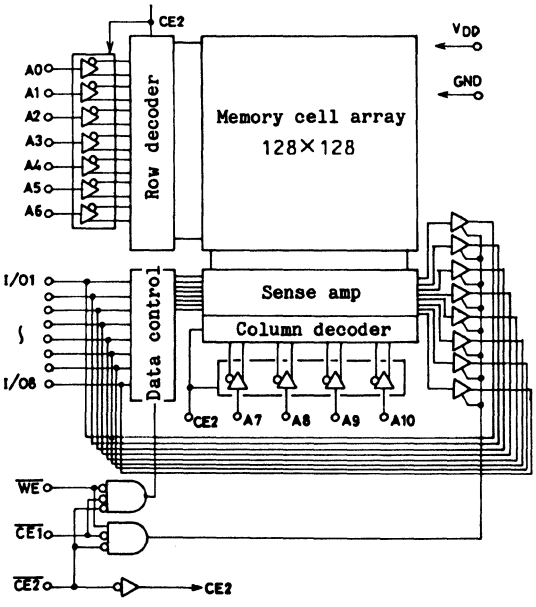
Features

- Low standby current.
  - LC3516 : 30uA
  - LC3516L : 1uA(Ta=60°C)
- Single 5V supply: V_{CC}=5V±10%
- Access time : TAA=250ns max.
- Data hold voltage: V_{CC}=2.0 to 5.5V
- Completely static operation.
- T^2L compatible at all input/output levels.
- 24-pin standard package.
- Tri-state output

Pin Assignment



Equivalent Circuit Block Diagram

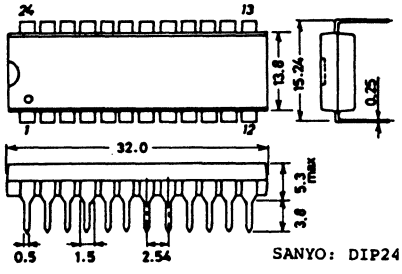


Pin Name

A0~A10	Address input
$\overline{WE}$	Read/write input
$\overline{CE1}$, $\overline{CE2}$	Chip enable input
I/O1~I/O8	Data input/output
VDD/GND	Power supply pin

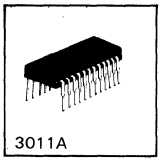
Case Outline 3011A-D24IC

(unit:mm)



SANYO: DIP24

LC3517



C MOS LSI

2048 Words by 8-Bits CMOS Static RAM

Ⓔ 1555

The LC3517 is an unclocked high-speed static RAM that is organized as 2048 words x 8 bits and operates from a single 5V supply. It has two control inputs: $\overline{CE}$ input dedicated to output tri-state control facilitating timing control in bus-used systems and $\overline{CE}$ input for battery applications where the whole circuit on chip enters the standby mode with less current dissipatated. By using in conjunction with various CMOS uCPU's, it can be applied to battery-powered portable sets and battery backup operation-required systems.

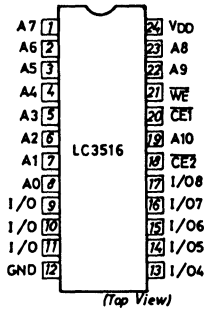
Applications

- Battery-powered portable set.
- Battery backup nonvolatile memory.

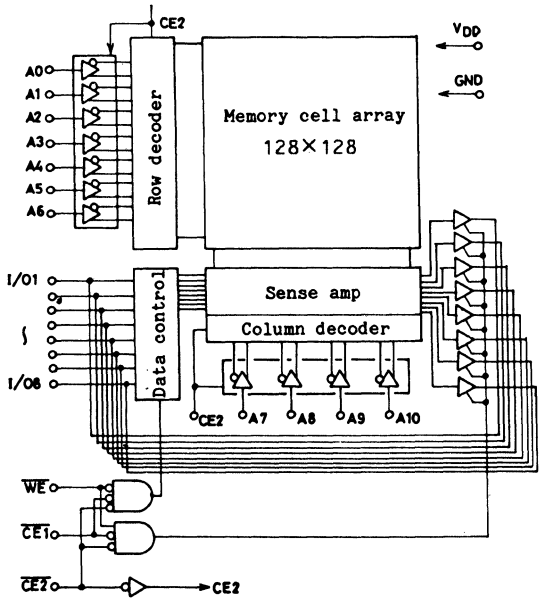
Features

- Low standby current.
  LC3517 : 30uA
  LC3517L : 1uA(Ta=60°C)
- T^2L compatible at all input/output levels.
- Access time : TAA=250ns max.
- Completely static operation.
- Single 5V supply: V_{CC}=5V±10%
- Data hold voltage: V_{CC}=2.0 to 5.5V
- Tri-state output
- 24-pin standard package
  (2716EPROM pin compatible)

Pin Assignment



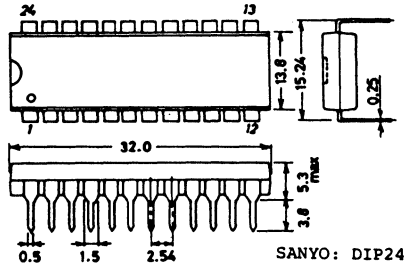
Equivalent Circuit Block Diagram



Pin Name

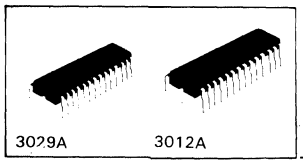
A0~A10	Address input
$\overline{WE}$	Read/write input
$\overline{CE1}$, $\overline{CE2}$	Chip enable input
I/01~I/08	Data input/output
VDD/GND	Power supply pin

Case Outline 3011A-D24IC
(unit:mm)



SANYO: DIP24

LC7800, 7800N



C MOS LSI

Input Expander

Ⓔ 907A

This is a C-MOS IC designed for use in microcomputer LSI input port expansion applications. It is especially suited for use, as a peripheral of our 4-bit microcomputer (LM6400 series, etc.), in application circuits having many input signals, application circuits with input switch common pins connected to GND, and application circuits which are incapable of using key scan signal in input signal lines.

Features

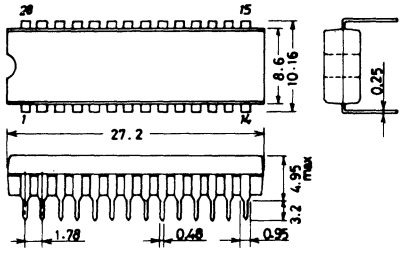
1. By connecting 1 pc. to a microcomputer LSI, the same effect as the number of microcomputer input pins increases by 8 is achieved. (Refer to sample application circuit 1.)
2. 16 input signals can be inputted to 4 input pins of a microcomputer. Namely, input expansion from 1 to 4 is available. (Refer to sample application circuit 1.)
3. By making 2-pc. parallel connection, 32 input signals can be inputted to 4 input pins of a microcomputer LSI. (Refer to sample application circuit 2.)
4. Output is of Nch MOS open drain type and signal level can be changed.
5. Since both types of TRUE and BAR are available for control input which turns off output transistors, no external inverter is required when 2-pc. parallel connection is used.

Functions

4-bit input expander IC usable as a peripheral of microcomputer LSI

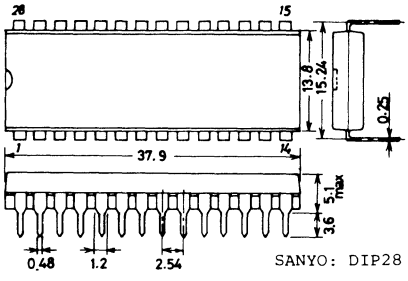
1. Out of 4-set data (16 inputs) which are organized with data of 4 bits/set; 1-set data (4 bits) are selected and outputted corresponding to 4 select input signals.
2. By applying low-level voltage to your desired 1 input pin of 4 select input pins($\overline{SA}$, $\overline{SB}$, $\overline{SC}$, $\overline{SD}$), your desired 1-set data (4 bits) of 4 sets can be selected.
3. By using inhibit input pins (INH, $\overline{INH}$)(applying "H" level voltage to INH pin and "L" level voltage to $\overline{INH}$ pin), output transistors can be turned off.

Case Outline 3029A-D28SIC
(unit:mm) (LC7800)



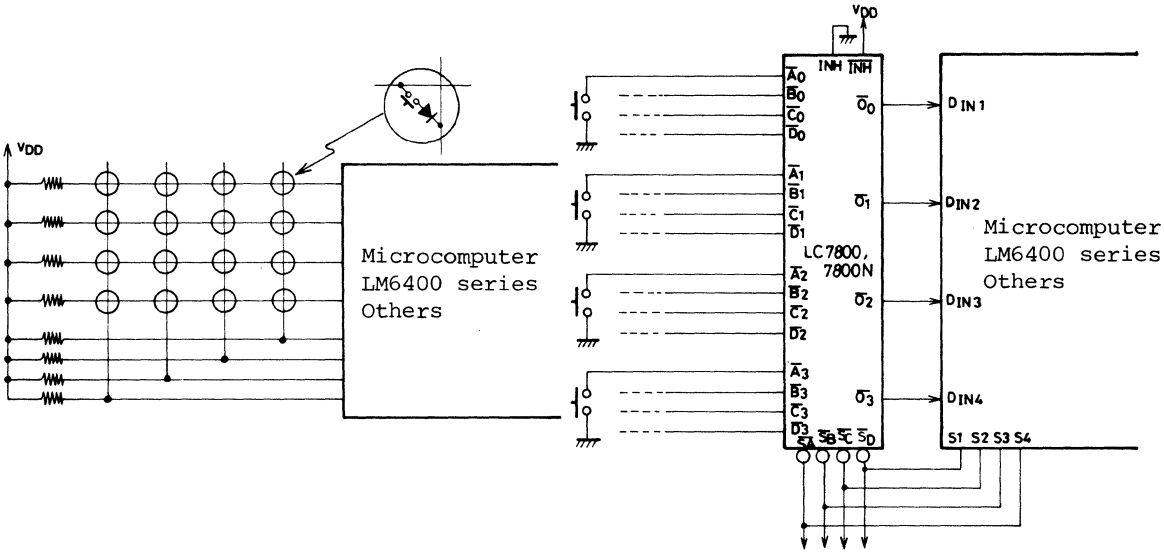
SANYO: DIP28S

Case Outline 3012A-D28IC
(unit:mm) (LC7800N)

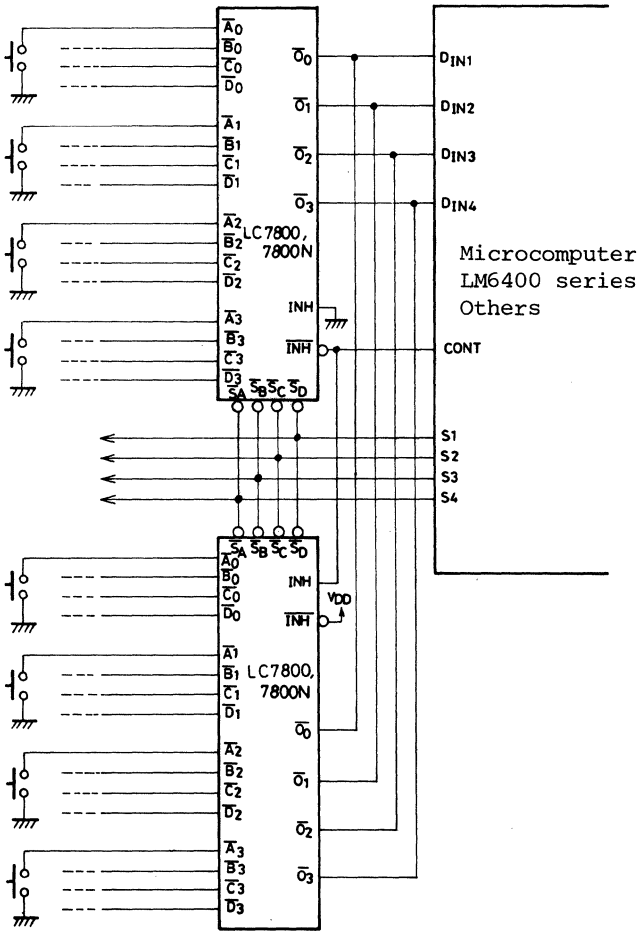


SANYO: DIP28

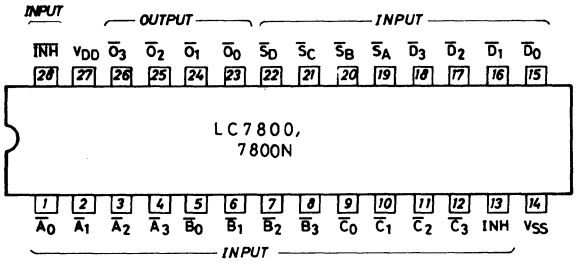
1. Application Circuit 1 :Replacement of 4:1 key matrix circuit with LC7800



Application Circuit 2 : Use in 32-input application

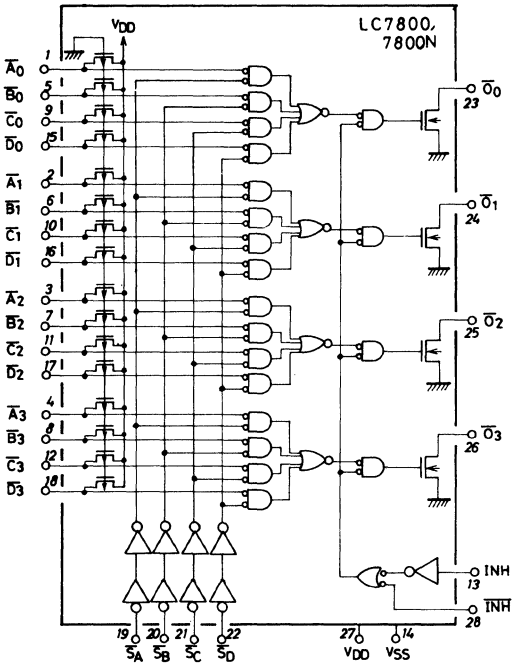


2. Pin Assignment



3. Equivalent Circuit Diagram

3-1. Equivalent Circuit Diagram



3-2. Truth Table

Input																						Output			
Data Input																Select input				inhibit input					
A				B				C				D													
$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{B0}$	$\overline{B1}$	$\overline{B2}$	$\overline{B3}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$	$\overline{C3}$	$\overline{D0}$	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$\overline{SA}$	$\overline{SB}$	$\overline{SC}$	$\overline{SD}$	INH	$\overline{INH}$	$\overline{O0}$	$\overline{O1}$	$\overline{O2}$	$\overline{O3}$
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	1	1	1
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1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	0	1	1	1	0	1
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1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	0	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	1	1	1	1	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	0	1	1	1	1
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	*	1	1	1	1
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	1	1	1	1

Note) 1 : "H" level/0 : "L" level/* : don't care

4. Pin Description

4-1. Input Pins

1) Data Input Pins ($\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$, $\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$)
   - Pins for inputting data consisting of 4 bits/set. Capable of up to 4-set data input.
   - Normal "H" level due to built-in pull-up resistor.
   - Data becomes active at "L" level.

2) Data Select Input Pins ($\overline{SA}$, $\overline{SB}$, $\overline{SC}$, $\overline{SD}$)
   - Pins for inputting 1 set out of 4 sets of data input $\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$, $\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$.
     If $\overline{SA}$, $\overline{SB}$, $\overline{SC}$, and $\overline{SD}$ are at '1' level, ($\overline{A0}$ to $\overline{A3}$), ($\overline{B0}$ to $\overline{B3}$), ($\overline{C0}$ to $\overline{C3}$), and ($\overline{D0}$ to $\overline{D3}$) are selected respectively.
   - Select input becomes active at "L" level.
   - If no pin is selected, output transistors are turned off.

3) Inhibit Input Pins (INH, $\overline{INH}$)
   - Pins for inputting signal which turns off output transistors.
   - For signal which turns off output transistors, both types of TRUE and BAR are available.
     TRUE : Inputting "H" level to INH causes output transistors to be turned off.
     BAR : Inputting "L" level to $\overline{INH}$ causes output transistors to be turned off.

4-2. Output Pins ($\overline{O_0}$, $\overline{O_1}$, $\overline{O_2}$, $\overline{O_3}$)

Data output pins
- Pins for outputting data of 1 set (1 set out of Ai, Bi, Ci, Di i=0 to 3) selected according to data select input.
- Nch MOS open drain output pins.

5. Main Specifications

Absolute Maximum Ratings at T_a=25°C

				unit
Maximum Supply Voltage	V_{DD}		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{SS}+0.5	V
Output Voltage	V_{OUT}	Output MOS-Tr off	V_{SS}-0.5 to V_{SS}+20	V
Input Current	I_{IN}		±10	mA
Output Current	I_{OUT}	Per output	+10	mA
Allowable Power Dissipation	$P_d$max	$T_a \leq 85$°C	300	mW
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C
Lead Temperature and Time	T_{sol}	t=10sec	260	°C

Allowable Operating Ranges at T_a=-40 to +85°C, V_{SS}=0V

		Pin No.		min	typ	max	unit
Supply Voltage	V_{DD}	27	V_{DD}	3		18	V
"H" Level Input Voltage	V_{IH}	1 to 8	$\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$: V_{DD}=5V	0.7V_{DD}		V_{DD}	V
		9 to 12, 15 to 18	$\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$: V_{DD}=10V	0.7V_{DD}		V_{DD}	V
		13,19 to 22,28	$\overline{SA}$ to $\overline{SD}$, INH, $\overline{INH}$: V_{DD}=15V	0.7V_{DD}		V_{DD}	V
"L" Level Input Voltage	V_{IL}	1 to 10	$\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$: V_{DD}=5V	V_{SS}		0.25V_{DD}	V
		11,12, 15 to 19	$\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$: V_{DD}=10V	V_{SS}		0.20V_{DD}	V
		13,20 to 22,28	$\overline{SA}$ to $\overline{SD}$, INH, $\overline{INH}$: V_{DD}=15V	V_{SS}		0.15V_{DD}	V

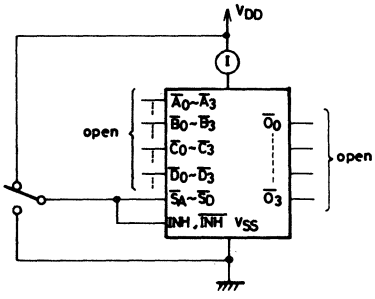
Electrical Characteristics at T_a=-40 to +85°C, V_{SS}=0V		Pin No.		min	typ	max	unit
Pin Open Voltage	V_{IO}	1 to 12, 15 to 18	$\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$, $\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$: V_{DD}=5,10,15V	0.7V_{DD}+0.2		V_{DD}	V
"L" Level Input Current	I_{IL}	1 to 12, 15 to 18	$\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$, $\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$:V_{DD}=5V	20		100	uA
		"	" :V_{DD}=10V	80		400	uA
		"	" :V_{DD}=15V	200		1000	uA
Input Leak Current	I_{IN}	All input pins	All inputs:V_I=18V, V_{DD}=18V			5	uA
		"	All inputs:V_I=V_{SS} (0V), V_{DD}=18V			-5	uA
"L" Level Output Voltage	V_{OL}	23 to 26	$\overline{O0}$ to $\overline{O3}$:I_{OL}=1.6mA, V_{DD}=5V			0.4	V
		"	$\overline{O0}$ to $\overline{O3}$:I_{OL}=3.0mA, V_{DD}=10V			0.5	V
		"	$\overline{O0}$ to $\overline{O3}$:I_{OL}=7.8mA V_{DD}=15V			1.5	V
Output Leak Current	I_{OFF}	23 to 26	$\overline{O0}$ to $\overline{O3}$:v_o=18V, Output MOS Tr off, V_{DD}=18V			5	uA
Quiescent Current Dissipation	I_{DD}	27	V_{DD}:T_a=85°C, V_{DD}=5V			15	uA
		"	" " ,V_{DD}=10V			30	uA
		"	" " ,V_{DD}=15V			60	uA
		"	V_{DD}:T_a=25°C, V_{DD}=5V			2	uA
		"	" " ,V_{DD}=10V			4	uA
		"	" " ,V_{DD}=15V			8	uA
		"	V_{DD}:T_a=-40°C, V_{DD}=5V			2	uA
		"	" " ,V_{DD}=10V			4	uA
		"	" " ,V_{DD}=15V			8	uA
Input Capacitance	C_{IN}	13,19 to 22,28	$\overline{SA}$ to $\overline{SD}$, INH, $\overline{INH}$		5	7.5	pF
	C_{IN}	1 to 12, 15 to 18	$\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$, $\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$		12	20	pF

* Current Direction : + (no sign) : Flowing into device
- : Flowing out of device

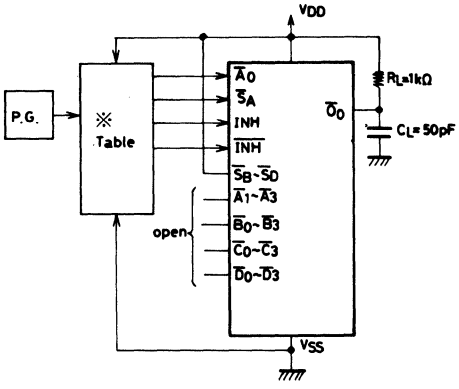
Switching Characteristics at T_a=25±2°C, C_L=50pF, R_L=1kohm			min	typ	max	unit
Output Fall Time	t_f	$\overline{O0}$ to $\overline{O3}$:V_{DD}=5V			200	ns
		" :V_{DD}=10V			100	ns
		" :V_{DD}=15V			80	ns
"L" Level Propagation Time	t_{PHL1}	$\overline{A0}$ to $\overline{A3}$, $\overline{B0}$ to $\overline{B3}$, $\overline{C0}$ to $\overline{C3}$, $\overline{D0}$ to $\overline{D3}$, $\overline{SA}$ to $\overline{SD}$ → $\overline{O0}$ to $\overline{O3}$:V_{DD}=5V			500	ns
		" :V_{DD}=10V			250	ns
		" :V_{DD}=15V			200	ns
	t_{PHL2}	INH, $\overline{INH}$ → O0 to O3:V_{DD}=5V			700	ns
		" :V_{DD}=10V			350	ns
		" :V_{DD}=15V			250	ns

Test Circuit

(1) Quiescent current dissipation

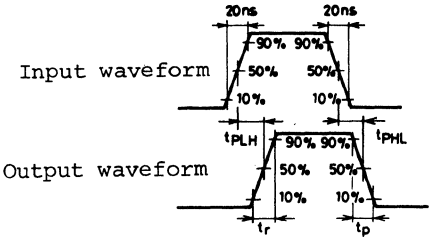


(2) Switching time test circuit and waveform



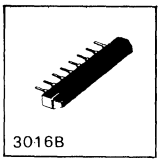
※ : Table

	$\overline{AO}$	$\overline{SA}$	INH	$\overline{INH}$
1	PG	V_{SS}	V_{SS}	V_{DD}
2	V_{SS}	PG	PG	V_{DD}
3	V_{SS}	V_{SS}	PG	V_{DD}
4	V_{SS}	V_{SS}	V_{SS}	PG



t_{PLH}, t_r depend on R_L.

LC7900



C MOS IC

System Clock Generator

Ⓔ 1185A

Use

- Reference clock generator for digital system operation

Features and Functions

- Contains crystal oscillator and frequency divider.

	Oscillation frequency		MHz 4.000000	MHz 4.194304	Frequency division radio
	C_1 pin	C_2 pin	kHz	kHz	
Output frequency	H	H	800.000	838.860	1/5
	L	L	400.000	419.430	1/10
	L	H	62.500	65.536	1/64
	H	L	31.250	32.768	1/128

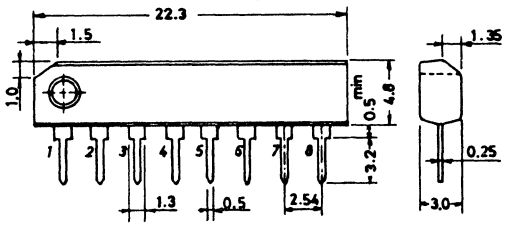
- Selects frequency division ratio (1/5, 1/10, 1/64, 1/128) with control pins (C_1, C_2) and outputs frequency division signal.
- Inhibit function to inhibit internal operation ($\overline{INH}$ pin)
- Capable of generating high-accuracy reference clock (400kHz, 800kHz) for 4-bit microcomputer (LM6402/05 series, LC6500 series)
- Operating supply voltage: 4.5 to 6.5V, operating temperature: −30 to +75°C

Absolute Maximum Ratings/T_a=25°C

			unit
Maximum Supply Voltage	$V_{DD\ max}$	$V_{SS}-0.3 \sim V_{SS}+7.5$	V
Input Voltage	V_{IN}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output Current	I_{OUT}	0~5	mA
Allowable Power Dissipation	$P_{d\ max}$	100	mW
Operating Temperature	T_{opg}	−30~+75	°C
Storage Temperature	T_{stg}	−40~+125	°C

(Continued on next page)

Case Outline 3016B-S8IC
(unit:mm)

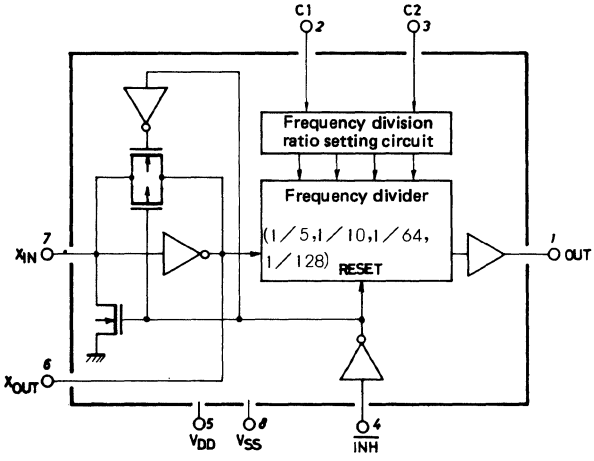


SANYO: SEP8

Allowable Operating Ranges/T_a=−30°C to +75°C			min	typ	max	unit
Supply Voltage	V_{DD}		4.5	5	6.5	V
"H" Level Input Voltage	V_{IH}		$0.7V_{DD}$		V_{DD}	V
"L" Level Input Voltage	V_{IL}		V_{SS}		$0.3V_{DD}$	V
Oscillation Frequency	f_{osc}	External capacitance C_i=C_o=22pF		4		MHz

Electrical Characteristics/V_{DD}=4.5V to 6.5 V, T_a=25°C			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	OUT, I_{OH}=−0.4mA	V_{DD}−0.6		V_{DD}	V
"L" Level Output Voltage	V_{OL}	OUT, I_{OL}=0.4mA	V_{SS}		V_{SS}+0.4	V
"H" Level Input Current	I_{IH}	C_1, C_2, $\overline{INH}$, V_{DD}=6.5V			10	μA
"L" Level Input Current	I_{IL}	C_1, C_2, $\overline{INH}$, V_{DD}=6.5V	−10			μA
Current Dissipation	I_{DD}	f_{osc}=4MHz			1.5	mA

Equivalent Circuit Block Diagram

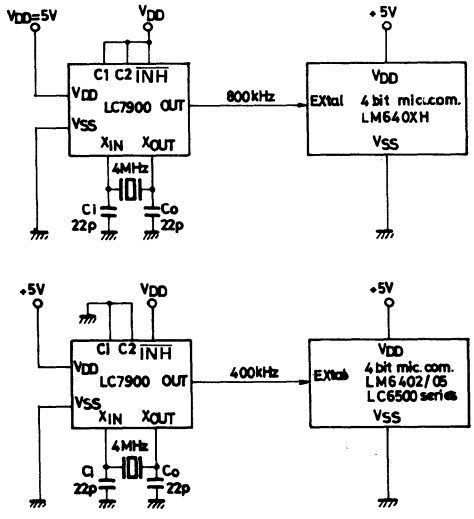


(Frequency Division Ratio Setting)

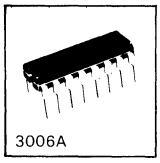
Frequency division ratio select pin		Frequency division
C_1	C_2	
H	H	1/5
L	L	1/10
L	H	1/64
H	L	1/128

H: Input high level
L: Input low level

■ **Sample Application Circuit**



LC7960



C MOS IC

3-Digit BCD Counter, Decoder, Driver

Ⓔ 474C

Features

- Especially suited for use in systems which count and indicate the number of pulses generated during a certain period of time.
- Contains a separator which generates the load signal from 3-digit BCD counter to latch and the reset signal of counter ($\overline{T/R}$ input signal fall: Load signal to latch; $\overline{T/R}$ input signal rise: Reset signal).
- Contains a 7-segment decoder, driver capable of direct driving segment current 15mA typ.
- Contains a high-order digit zero suppressor. (10^3's digit is not zero-suppressed. For count contents 0000, all digits blanking occurs.)

Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{DD}		-0.3 to +10	V
Input Voltage	V_{IN}		-0.3 to V_{DD}+0.3	V(Note 1)
Output Current	I_{OH}	Ta=-30 to +80°C	46	mA(Note 2)
Allowable Power Dissipation	Pdmax	Ta=-30 to +80°C	450	mW(Note 3)
Operating Temperature	Topg		-30 to +80	°C
Storage Temperature	Tstg		-40 to +125	°C

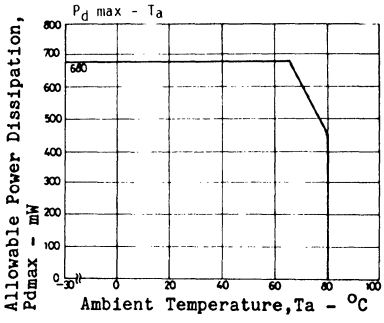
(Note 1) With the V_{SS} pin open or V_{DD} pin open, no voltage must be applied across V_{DD} and output, V_{DD} and input, V_{SS} and input.

(Note 2) The absolute maximum rating of output current is for only one output pin of pin No. 10, 11, 12, 13, 14, 15, 16 being at the high level.

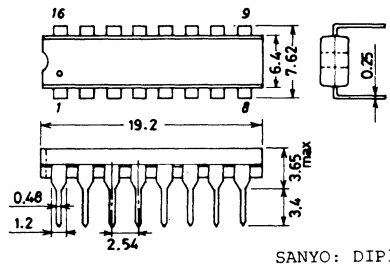
(Note 3) The absolute maximum rating of allowable power dissipation represents the average over a period of 5.2msec. or less.

Allowable Operating Ranges at Ta=25°C

				min	typ	max	unit
Operating Supply Voltage	V_{DD}			7.2		8.8	V
Segment Output Limiting Resistance	R_L		Ta=-30 to +80°C See Fig. 1.	162	180		ohm
Input High level Voltage	V_{IH}	6,7		V_{DD}-1.4			V
Input Low Level Voltage	V_{IL}	6,7				1.0	V
Input Signal Width	$t_{W(1)}$	6	See Fig. 2.	2.0			us
	$t_{W(2)}$	7	See Fig. 2.	30			us
Input Transient Time	$t_{rf(1)}$	6	See Fig. 2.			100	us
	$t_{rf(2)}$	7	See Fig. 2.			100	us



Case Outlined 3006A-D16IC
(unit:mm)



SANYO: DIP16

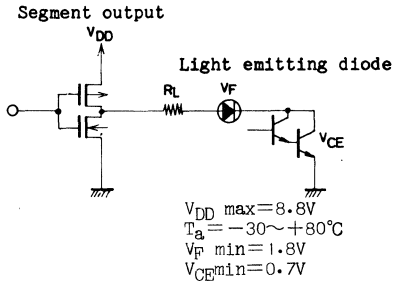


Fig. 1 R_L Test Conditions

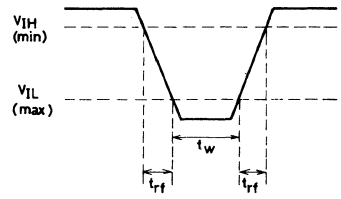


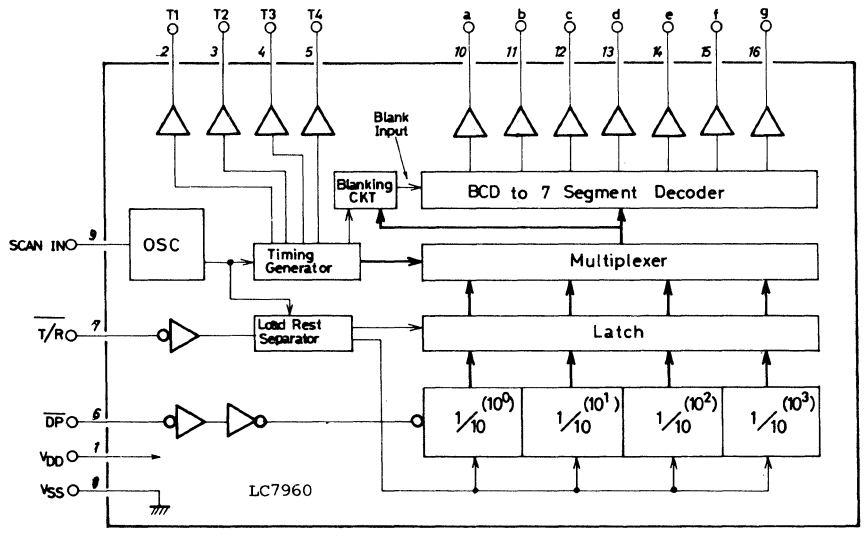
Fig. 2 Definition of Waveform

Electrical Characteristics at Ta=25°C, V_{DD}=7.2 to 8.8V

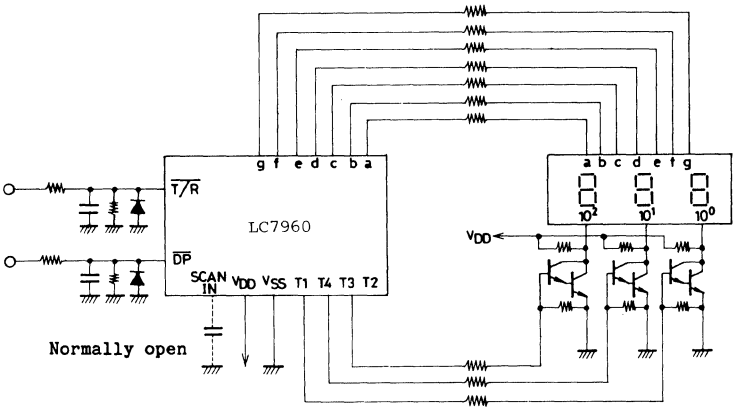
		(Pin No.)	(Conditions)	min	typ	max	unit
Output High Level Voltage	$V_{OH(1)}$	10to16	V_{DD}=7.2to8.8V,	V_{DD}-1.5	V_{DD}-0.27		V
			V_{DD}=8.8V	V_{DD}-1.4	V_{DD}-0.27		V
			at I_{OH}=-18mA, Ta=-30 to +80°C				
	$V_{OH(2)}$	2to5	I_{OH}=1mA, Ta=-30 to +85°C	V_{DD}-2.0			V
Output Low Level Voltage	$V_{OL(1)}$	10to16	I_{OH}=-0.5mA, Ta=-30to+80°C			0.6	V
	$V_{OL(2)}$	2to5	" "			0.6	V
High Level Input Current	I_{IH}	6,7	V_I=V_{DD}			10	uA
Low Level Input Current	I_{IL}	6,7	V_I=V_{SS}	-10			uA
Input Capacitance	c_{IN}	6,7	V_I=V_{SS}, f=1MHz			10	pF
Digit Signal Frequency	f_D	2to5	Pin 9=Open Ta=-30 to +80°C	0.195		1.95	kHz
Scan OSC Frequency	f_s		Pin 9=Open, f_s=512xf_D Ta=-30 to +80°C	100		1000	kHz
Current Dissipation	I_{DD}		Pins 2to5, 9to16=Open Pins 6,7=Signal applied Ta=-30 to +80°C			2.5	mA

(Note) Current direction : No sign: Flowing into IC
- : Flowing out of IC

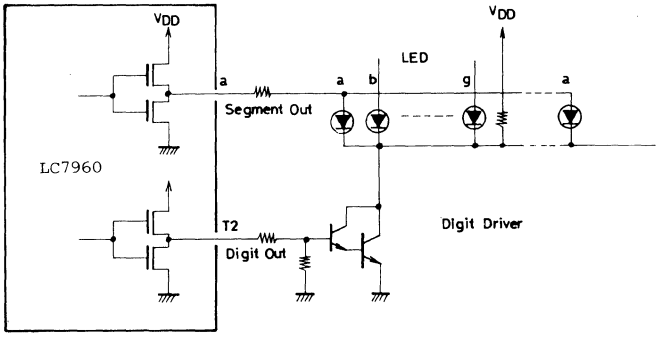
Equivalent Circuit Block Diagram



1. Sample LED Lighting

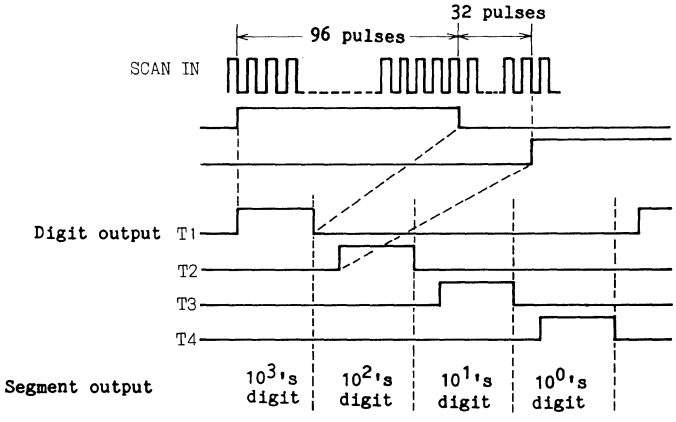


2. Output Configuration of LC7960

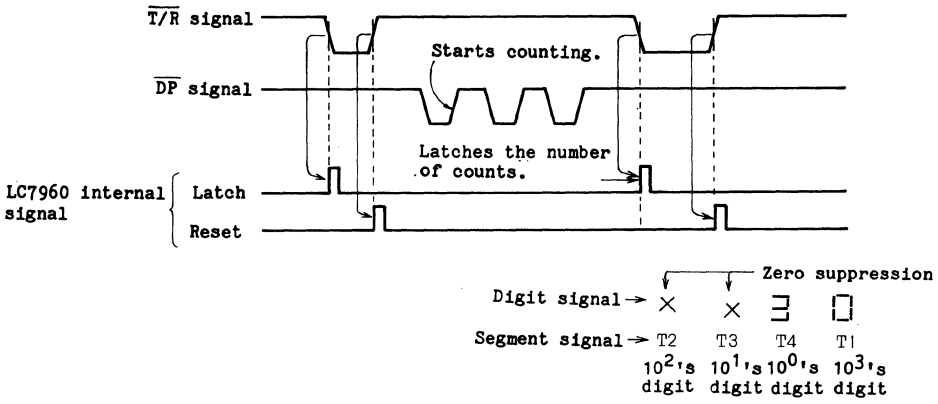


3. Time Chart

3-1. Output signal time chart



3-2. Operation time chart (Number of DP pulses=3)



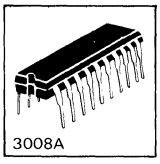
Output LED display (7 segments, 4 digits)
└→3 digits when T1 is not in use

Note : When the $\overline{T/R}$ input and $\overline{DP}$ input are set to "L" simultaneously, all digit signals are set to "L", causing the display to be unlighted. Internal signal latch/reset occur on the negative/positive transition of the $\overline{T/R}$ input signal.

4. Truth Table for Segment Output

Decoder Input Decimal	Blank Input	Segment Output a	b	c	d	e	f	g	Display
0	0	H	H	H	H	H	H	L	0
1	0	L	H	H	L	L	L	L	1
2	0	H	H	L	H	H	L	H	2
3	0	H	H	H	H	L	L	H	3
4	0	L	H	H	L	L	H	H	4
5	0	H	L	H	H	L	H	H	5
6	0	H	L	H	H	H	H	H	6
7	0	H	H	H	L	L	H	L	7
8	0	H	H	H	H	H	H	H	8
9	0	H	H	H	H	L	H	H	9
0	1	L	L	L	L	L	L	L	Blank

LC7961



C MOS LSI

4-Digit BCD Counter, Decoder, Driver

Ⓔ 734A

Use

. Decimal 4-digit counter for various displays

Features

. Latch, multiplexer, segment decoder, segment driver-contained 4-digit BCD counter for dynamic display

. Maximum count display 9999

. Cascade connection available (with carry output, blanking control pins)

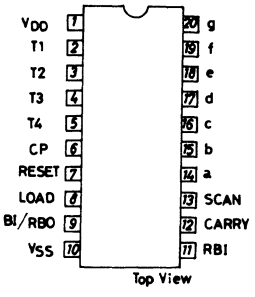
Absolute Maximum Ratings: $/T_a=25℃, V_{SS}=0V$

				unit
Maximum Supply Voltage	V_{DD} max		−0.3～+10	V
Input Voltage	V_{IN}		−0.3～(V_{DD}+0.3)	V
Output Current	I_{OH}	Peak value of each output of a, b, c, d, e, f, g	45	mA
Allowable Power Dissipation	P_d max	$T_a \leq 70℃$	600	mW
Operating Temperature	T_{opg}		−30～+70	℃
Storage Temperature	T_{stg}		−40～+125	℃

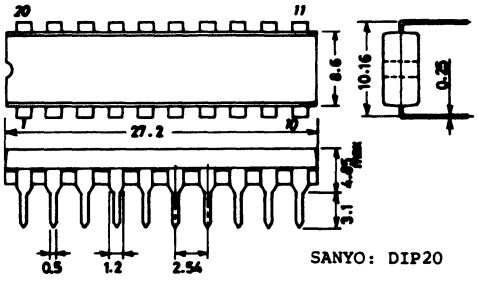
Allowable Operating Ranges $/T_a=25℃, V_{SS}=0V$

		Pin No.		min	typ	max	unit
Supply Voltage	V_{DD}	1		4		8.8	V
"H" Level Input Voltage	$V_{IH(1)}$	6		0.85V_{DD}		V_{DD}	V
	$V_{IH(2)}$	7,8,9,11		0.8V_{DD}		V_{DD}	V
"L" Level Input Voltage	$V_{IL(1)}$	6		V_{SS}		0.16V_{DD}	V
	$V_{IL(2)}$	7,8,9,11		V_{SS}		0.20V_{DD}	V
Input Frequency	f_{cp}	6	duty=40～60%			0.5	MHz
nput Pulse Width	$t_{w(1)}$	6	See Fig. 1.	0.8			μs
	$t_{w(2)}$	6	See Fig. 1.	0.8			μs
	$t_{w(3)}$	7,8	See Fig. 2.	2			μs
Input Transient Time	t_{rf}	6,7,8,11	See Fig. 2.	0		20	μs
Leading Edge Separation Time	t_{sp}	7,8	See Fig. 3. f_s=50kHz min.	50			μs
Data Setup Time	t_{stp}	6,8	See Fig. 4.	8			μs

Pin Assignment



Case Outline 3008A-D20IC
(unit:mm)



Electrical Characteristics /T_a=25℃, V_{SS}=0V, V_{DD}=4~8.8V

		Pin No.		min	typ	max	unit
"H" Level Output Voltage	$V_{OH}(1)$	14~20	I_{OH}=18mA	V_{DD}-2.3			V
	$V_{OH}(2)$	2~5,12	I_{OH}=1mA	V_{DD}-1.6			V
	$V_{OH}(3)$	9	I_{OH}=5μA	V_{DD}-0.8			V
"L" Level Output Voltage	$V_{OL}(1)$	14~20	I_{OL}=0.5mA			0.5	V
	$V_{OL}(2)$	2~5,12	I_{OL}=0.5mA			0.5	V
	$V_{OL}(3)$	9	I_{OL}=5μA			0.8	V
"H" Level Input Current	I_{IH}	6,7,8,11	V_{IN}=V_{DD}			3	μA
"L" Level Input Current	I_{IL}	6,7,8,11	V_{IN}=V_{SS}			3	μA
Current Dissipation	I_{DD}	1	Output open, OSC oscilating			2.5	mA
Output Delay Time	t_{pd}	6,12	See Fig. 5.			3	μs
Input Capacitance	C_{IN}	6,7,8,11	At f_{in}=1MHz			10	pF
Scan Oscillation Frequency	f_s	13	SCAN open, V_{DD}=5~8.8V	60		1000	kHz

Test Waveforms

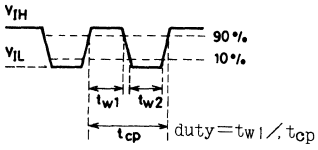


Fig 1

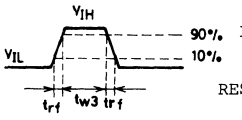
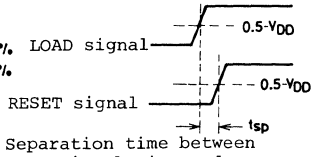
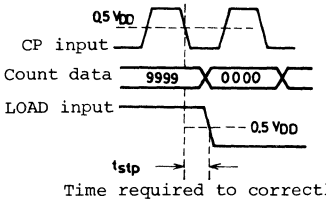


Fig 2



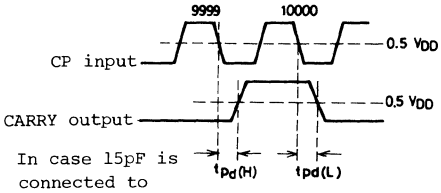
Separation time between LOAD signal rise and RESET signal rise

Fig 3



Time required to correctly load count results of CP input

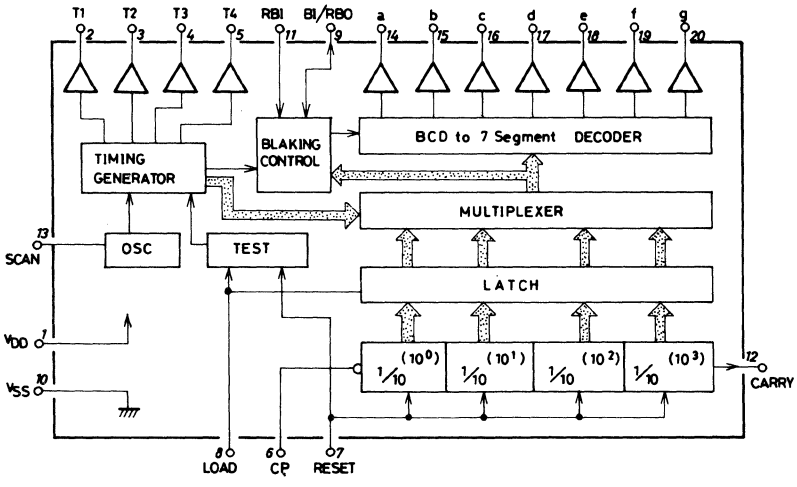
Fig 4



In case 15pF is connected to CARRY output

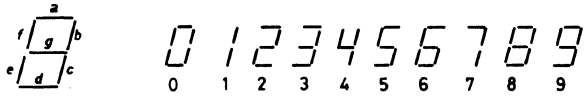
Fig 5

Equivalent Circuit Block Diagram



◆ Description of Pin Functions

Pin No.	Symbol	I/O	Function
1	V_{DD}	—	V_{DD} power supply
2	T_1	O	Outputs for displaying digits of segment signals (a to g). T1: Digit of 10^3, T2: Digit of 10^2, T3: Digit of 10^1, T4: Digit of 10^0
3	T_2	O	
4	T_3	O	
5	T_4	O	
6	CP	I	Clock input for counter. Count is made at CP input fall.
7	RESET	I	"H": Counter is reset to 0000. "L": Normal count is made.
8	LOAD	I	"H": Counter contents are outputted to MULTIPLEXER as they are. "L": Counter contents at LOAD input fall are latched.
9	BI/RBO	I	"H": If RBI is at "L", zero suppression is made; if counter contents are 0000, only 0 of least significant digit is lighted. If RBI is at "H", zero suppression is not made.
			"L": If RBI is at "L", zero suppression is made; if counter contents are 0000, all digits blanking is made. If RBI is at "H", zero suppression is not made.
			open: Output signal is outputted as it is. Blanking mode depends on output signal.
		O	If RBI is at "H", "H" is outputted unconditionally. If RBI is at "L", "L" is outputted when counter contents are 0000; "H" is outputted when counter contents are not 0000.
10	V_{SS}	—	GND (OV).
11	RBI	I	"H": Zero suppression is not made. 0000 is lighted. "L": BI/RBO is open, zero suppression is made. If counter contents are 0000, all digits blanking is made.
12	CARRY	O	If counter contents are 9999, "H"; if counter contents are other than 9999, "L".
13	SCAN	I/O	External capacitor connecting pin for OSC circuit which generates T_1 to T_4 signals
14	a	O	Segment outputs. Relation between pin names and segments and display font are as shown below. "H": Lighted, "L": Unlighted
15	b		
16	c		
17	d		
18	e		
19	f		
20	g		

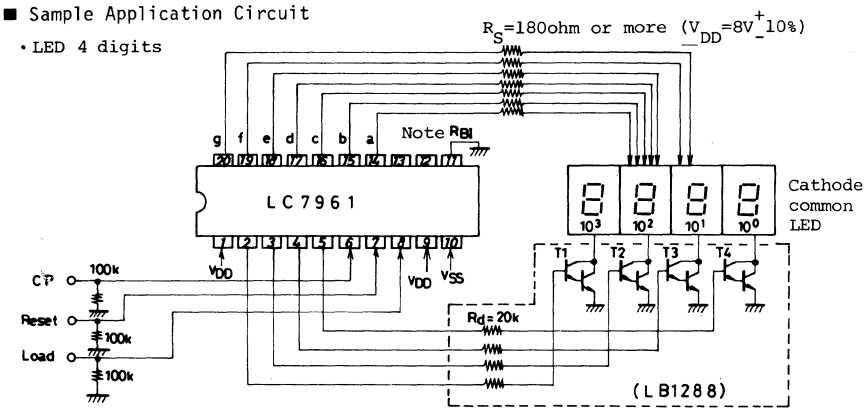


◆ How to Use Blanking Control Function

Mode	RBI	BI/RBO	Function and How to Use
1	H	X	Zero suppression is not made.
2	L	H	Zero suppression is made. Only 0 of least significant digit of counter contents 0000 is lighted. This mode is applied when 4-digit counter is used under zero suppression.
3	L	L	Zero suppression is made. All digits blanking of counter contents 0000 is made.
4	L	open	Zero suppression is made. All digits blanking of counter contents 0000 is made. When composing counter of more than 4 digits, this mode is applied on high-order side. Actually, BI/RBO output on high-order side is connected to RBI input on low-order side.
5	High -order	L	This mode is applied as low-order side when high-order side is in mode 4. Zero suppression is made. Only 0 of least significant digit of counter contents 0000 is lighted.

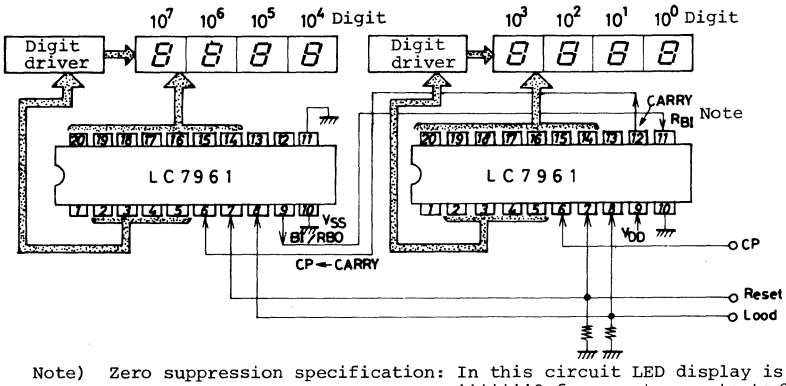
■ Sample Application Circuit

• LED 4 digits



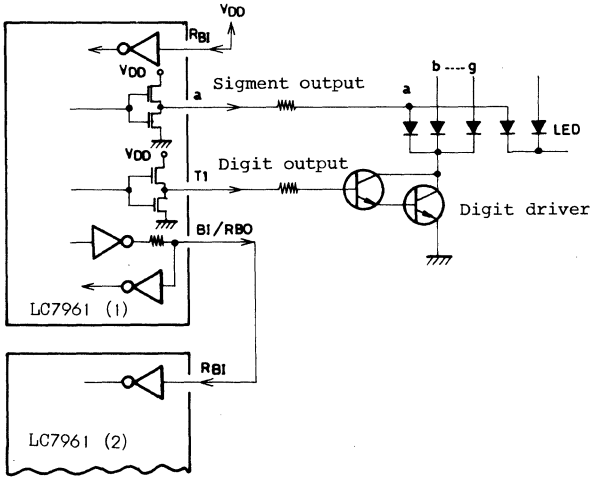
Note) Zero suppression specification: In this circuit LED display is ***0 for counter contents 0000. (*: Blanking)

• LED 8 digits

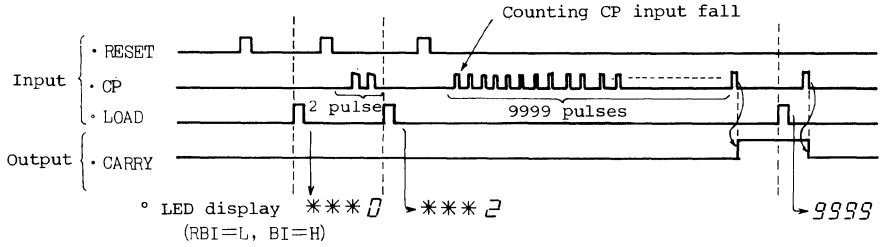


Note) Zero suppression specification: In this circuit LED display is *******0 for counter contents 0000 0000. (*: Blanking)

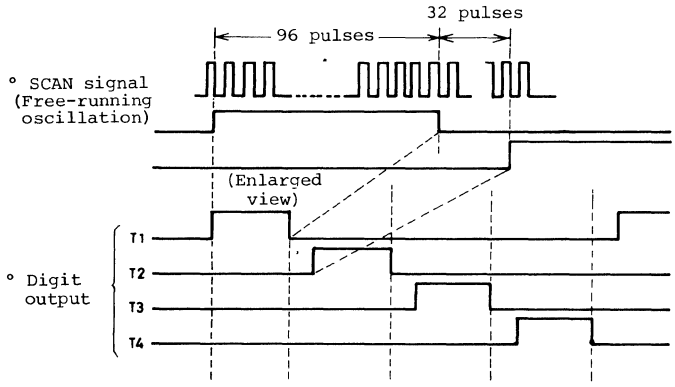
■ Input/Output Type



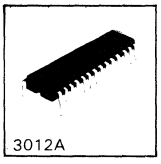
■ Input/Output Timing Chart



° Digit signal timing chart



LC8100



C MOS LSI

Single-Chip Speech Synthesizing System

Ⓔ 1436A

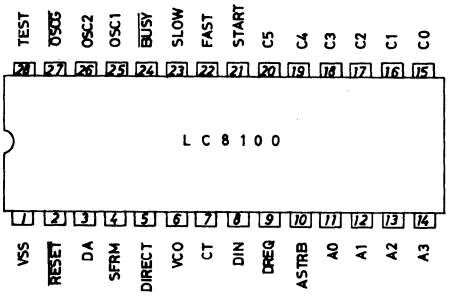
The LC8100 is a CMOS single-chip LSI that enables about 20 seconds of speech synthesis using the PARCOR method.

A speech synthesizer, a parameter ROM (32 K bits) and a DA converter, have been integrated into a single chip. The LSI also has an external extension function for the parameter ROM, an interfacing function for key switches and microcomputers, an automatic power-down function, and other features.

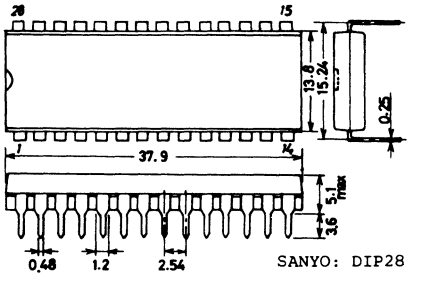
FEATURES

- Can synthesize male or female voices
- Speech duration: 14 to 28 seconds (Built-in ROM: 2400 bits/second)
- Speech duration can be lengthened:
  Up to 16 128-K-bit LC3100s can be connected together and directly interface to the ROM.
  100 seconds/piece approx. extended durations.
- Words of speech:
  63 words (by an index addressing system)
  Unlimited (by a direct addressing system)
- Veriable speech speeds:
  3 steps: −25%, 0%, and +25%
  (Further variation is feasible by combinations with the frame frequency.)
- Built-in DA converter:
  9-bit
- Selectable parameter bit rates:
  2400, 4800, or 9600 bits/second
- Automatic power-down function:
  Starts operating upon receiving a speech synthesis command, and powers down upon conclusion.
- +5V single power supply operation:
  Can operate at +2.7 through +6.5 V.
- Low power consumption:
  2mA max. drain in operating mode
  10μA max. drain in power-down mode

PIN ASSIGNMENT

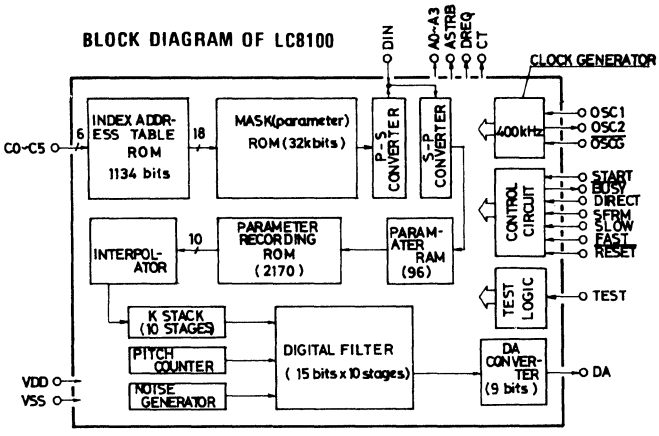


Outline Drawings 3012A-D28ID (unit: mm)



SANYO: DIP28

EQUIVALENT CIRCUIT BLOCK DIAGRAM



CO to C5:	Word selection terminals
$\overline{\text{BUSY}}$:	Output terminal indicates speech being output
SFRM:	Frame length switching
$\overline{\text{RESET}}$:	Reset
$\overline{\text{OSCG}}$:	Power-down control
DA:	DA converter
START:	Start terminal
DIRECT:	Word selecting method switching terminal
SLOW, FAST:	Speed control
OSC1, OSC2:	Oscillator element connecting terminals (400, 800 kHz ceramic resonators or CRs to be connected)
TEST:	Test terminal
VDD, VSS:	Power
DIN, AO to A3, ASTRB, DREQ, CT:	External ROM terminals

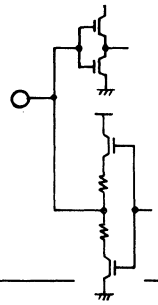
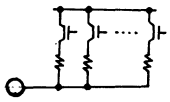
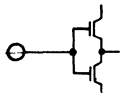
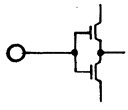
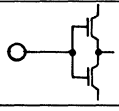
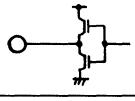
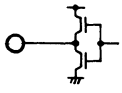
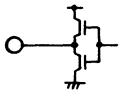
BLOCK DIAGRAM DESCRIPTION

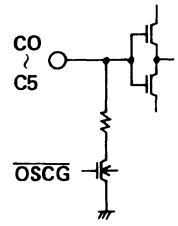
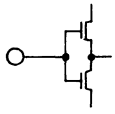
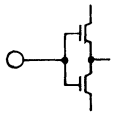
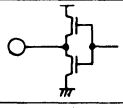
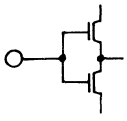
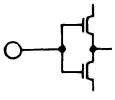
- INDEX ADDRESS TABLE ROM (63 x 18 bits):
  ROM for specifying the indexed address for words to be generated with the CO to C5 code
- MASK ROM (32 K-bits):
  ROM to store speech parameters
- P-S, S-P CONVERTER:
  Parallel-serial converter for reading out speech parameters
- PARAMETER RAM (96 bits):
  RAM to store parameters for one frame
- PARAMETER DECODING ROM ('2170 bits):
  ROM to decode parameters non-linearly
- INTERPOLATOR:
  Circuit to interpolate parameters every 2.5 msec
- K STACK:
  Register to store and operate parameters
- PITCH COUNTER, NOISE GENERATOR:
  Voiced, Unvoiced sound sources
- DIGITAL FILTER (15 bits x 10 stages):
  Lattice type digital filter
- D/A CONVERTER (9-bits): DA converter

INTERNAL SYSTEM SPECIFICATIONS

- Coding: PARCOR method
- Sampling frequency: 9.1 kHz
- Filter stages: 10 stages
- Frame period 20 msec standard (10 msec feasible)
- Parameters per frame: 48 bits/frame standard (96 bits/frame feasible)
- Parameter interpolating period: 2.5 msec
- Data compression factor: 2.4 K-bits/sec standard (4.8, 9.6 K-bits/sec feasible)
- Internal operating accuracy: 15 bits
- Synthesized sound fundamental frequencies: 50 to 500 Hz approx.
- DA converter: 9-bit (including sign bit)

TERMINAL DESCRIPTION

Terminal number	Terminal name	Input/output	Circuit type	Description of functions
2	$\overline{\text{RESET}}$	Input/ output		Resets LSI interior In the power-down state, a reset singnal is output from the LSI. When a start speech signal is applied in the power-down ($\overline{\text{OSCG}}$ is high), the reset state will be maintained for the length of time designated by the time constant of an external reset circuit (normally a capacitor connected across VSS and $\overline{\text{RESET}}$), after which operation is started.
3	DA	Output		DA converter (speech) output terminal. A constant-current-source DA converter is built in. Normally an external resistive load is connected across this terminal and VSS. In the power-down state, the output enters a high impedance state.
4	SFRM	Input		Frame length switching terminal When SFRM is high, frame length = 10 msec. When SFRM is low, frame length = 20 msec. When desiring to set for a frame length that differs from the analyzed condition, speech should be generated at a half speed or a double speed.
5	DIRECT	Input		Terminal to switch methods to specify words or phrases of speech When DIRECT is high, parameter ROM addresses (18 bits) are directly specified using the CO to C3 4-bit data 5 times. When DIRECT is low, 63 types of indexed address tables are referenced with the CO to C5 data.
7	CT	Output		Reference clock signal supplied to an external ROM (LC3100) (200 kHz typ.)
8	DIN	Input		Terminal to input data from an external ROM
9	DREQ	Output		Data request signal to an external ROM
10	ASTRB	Output		Strobe signal to instruct external ROM for latching data (AO to A3) when designating parameter addresses
11 12 13 14	A0 A1 A2 A3	Output		Terminals to output addresses to an external ROM. At synthesis start, these are output divided into 4 bits at a time and in 5 separate outputs. When not synthesizing ($\overline{\text{BUSY}}$ is high), signals input to the CO through C3 terminals are output to AO through A3. Signals input to C4 and C5 are output to ASTRAB and DREQ terminals. Accordingly, external ROM address designation and data read-out can be effected by utilizing the CO through C5 terminals.
6	V_{DD}	—		The power supply (+) side terminal

Terminal number	Terminal name	Input/output	Circuit type	Description of functions
15 16 17 18 19 20	C0 C1 C2 C3 C4 C5	Input	 When $\overline{OSCG}$ is high, the circuit is provided with a pull-down resistor.	Selects words for utterance. (1) When DIRECT is high: Using 4-bit data of CO through C3 five times, specifies the parameter ROM leading address (18 bit length). (2) When DIRECT is low: Selects words for generation by a combination of CO through C5. This is an index addressing mode where the addresses shown by the index address table (mask program) are designated by CO through C5, and up to 63 selections can be made.
21	START	Input		Start speech synthesis Leading edge starts speech generation. When DIRECT is low and START is maintained at a high level, generation will start at the leading edge of a low to high transition at CO through C5, (all of which have been held at a low level) into high level.
22 23	FAST SLOW	Input		Selects the speech speed, and specifies the parameter bit rate (bit/frame, BPF). FAST / SLOW / OPERATION L / L / 48 BPF, Normal speed L / H / 48 BPF, −25% speed H / L / 48 BPF, +25% speed H / H / 96 BPF, normal speed
24	$\overline{BUSY}$	Output		Indicates speech being synthesized or waiting oscillator circuit to settle: When speech is being generated and when the $\overline{OSCG}$ and $\overline{RESET}$ are both low, $\overline{BUSY}$ will also become low.
27	$\overline{OSCG}$	Input		Control signal for the oscillator circuit, DA converter, and resetting circuit. When $\overline{OSCG}$ is low, each of these circuits will be in an operation mode. When $\overline{OSCG}$ is high, LSI will be in a power-down mode. However, when $\overline{OSCG}$ is high, receiving a start speech instruction will induce an operation mode. The operation will stop upon concluding speech synthesis. When $\overline{OSCG}$ is high, chattering absorbing circuits will function for signals of start speech instruction.
25	OSC1	Input		Terminals for connecting oscillator elements for the oscillation circuit Ceramic oscillator elements or a CR circuit are connected to generate a 400-kHz oscillation. (An 800-kHz option is also available.)
26	OSC2	Output		
1	VSS	—	—	Power supply OV side connecting terminal. (Low potential)
28	TEST	Input	—	Terminal for testing internal circuits Normally connected to the VSS terminal.

WORD/PHRASE SELECTION METHODS

The LSI has two functions which enable three ways of utilization of word/phrase selection methods.

(1) Index Addressing Mode (When DIRECT is low)

Up to 63 words can be specified by a code at pins, CO through C5. Words or phrases coresponding to these codes are coded into the LSI index address table (ROM) at the factory on customer order (mask option). The following two applications are possible.

1) Key input mode (Refer to application example 1.)

Conditions: DIRECT = 'L', $\overline{OSCG}$ - 'H', START = 'H'
Word/phrase selection: Words/phrases corresponding to codes at CO through C5 are selected (designated in advance with the mask option).
Word/phrase synthesis start: In advance of start command, CO through C5 must be low. And then synthesis starts at a leading edge of any one of CO through C5 (due to START = 'H').
Key debounce: Key debouncing circuits function for CO through C5 signals.
Power down: The chip automatically powers on by a CO through C5 input, and automatically powers down if all CO through C5 inputs are'L' after synthesis is complete.
This mode is employed when there is less than 6 words/phrases and no editing of words/phrases is required. (More than 6 words are also possible if an encoder IC is being used.)

2) Microcomputer-controlled mode (Refer to application example 2)
Condition: Direct = 'L'
Word/phrase selection: Depending on value at CO through C5. Selects up to 63 words. (Nothing is selected when CO through C5 are all 'L'.)
Word/phrase start: A high pulse is applied to START.
Key debounce: When $\overline{OSCG}$ = 'L', key debounce circuits will not function.
Power down:

(i) When the power-down function is not employed, $\overline{OSCG}$ is low.
(ii) When it is employed, the signal applied to $\overline{OSCG}$ is controlled by a microcomputer. (Refer to the paragraph on power-down.)

This mode is employed when up to 63 words are generated under microcomputer control.

(2) Direct Addressing Mode/DIRECT = 'H'

The LC8100 has an address space for a 256 -KB. ROM, and an 18-bit address counter.

Using the CO through C4 terminals, address data can be set on the counter, Any words/phrases in excess of 63 words can be directly specified by the 18-bit address.

The specifying method is somewhat complicated, but handling of a large number of words and phrases is possible. (Refer to application example 3.)

Condition: DIRECT = 'H'
Word/phrase selection: Leading addresses for words/ phrases are designated by the CO through C3 4-bit data and the clock provided to C4.
Word/phrase start: A high pulse is applied to the START terminal.
Key debounce: When $\overline{OSCG}$ = 'L', the key debounce circuit will not function.

(i) When the power-down function is not used, $\overline{OSCG}$ is kept low 'L'.
(ii) When it is employed, $\overline{OSCG}$ is controlled by a microcomputer. (Refer to the paragraph on power-down.)

SPEECH STARTING METHODS

(1) Start Detecting Circuit

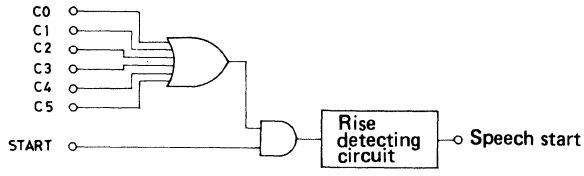


Fig. 1 Start detecting circuit conceptual diagram

Fig. 1 shows a conceptual diagram for the start detecting circuit. As seen from the figure, for word/phrase start instructions, there is a high level at one or more of CO through C5, and START = 'H'. This situation suggests the following two approaches for starting instructions:

1) First select words/phrases in advance with the CO through C5, then make START high 'H'.
2) Leave START high at all times. Make 'L' at each of CO through C5 in advance of start command, and any other code to initiate speech and select a word/phrase.

In combination with DIRECT, three approaches, as shown by application examples 1 to 3, can be taken.

(2) $\overline{\text{BUSY}}$ Signal Detection·
$\overline{\text{BUSY}}$ is an Active low at the following three conditions:

(i) During speech synthesis
(ii) A synthesis start signal is provided while $\overline{\text{BUSY}}$, = 'H', and $\overline{\text{BUSY}}$ then changes to low upon receipt of the start signal.
(iii) While $\overline{\text{OSCG}}$ = 'L' and $\overline{\text{RESET}}$ = 'L'.

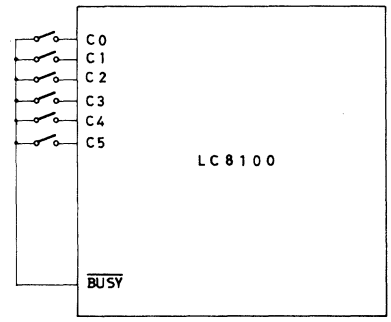
When using a microcomputer to control the LC8100 , the microcomputer must continue to monitor $\overline{\text{BUSY}}$ in the following manner:

(i) $\overline{\text{BUSY}}$ = 'H' has to be verified before enabling speech generation.
(ii) After starting speech synthesis, do not & change at pins CO through C5 (in direct addressing mode, or CO through C3 when the last digit data is impressed) until $\overline{\text{BUSY}}$ becomes 'L'.

(3) Halt–Synthesis Function
During a synthesizing operation, if a new word/phrase start instruction is provided, the LC8100 will halt synthesis, and will start synthesizing a new word/phrase.
When halting a synthesis, $\overline{\text{BUSY}}$ remains 'L'. The word/phrase selection code provided to CO through C5, is uncontrollable with $\overline{\text{BUSY}}$ as described in paragraph (ii) of (2). The signal applied to CO through C5 must not vary for the necessary length of time. (TB max; Refer to timing specification).

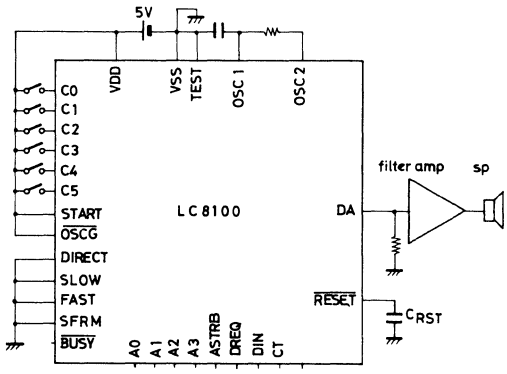
(4) Inhibitting halt–Synthesis, in Key Input Mode
In cases utilizing application circuit 1 for a key input mode (to be described later on), when a key is pushed the second time after the key debouncing period, the halt-synthesis function will be actuated. To inhibit this function, CO through C5 should be as shown in Fig. 2.
When this circuit is employed, the LSI will only receive the key inputs after synthesis is complete.

Fig. 2 Inhibitting the halt-synthesis function.



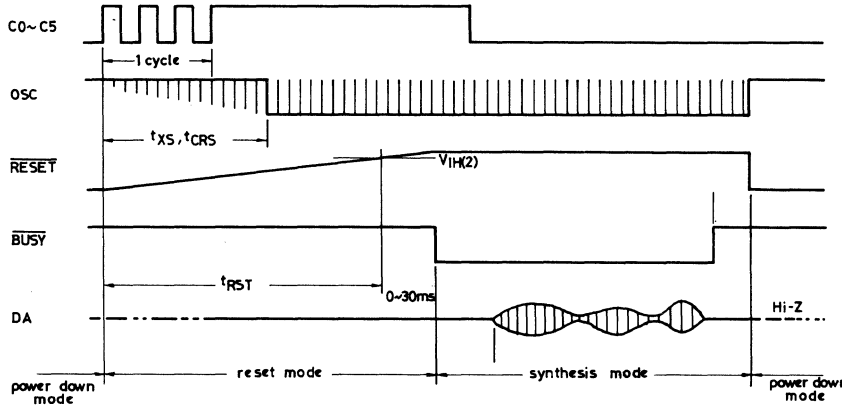
Application Example 1 One-word corresponding one-key system

Up to 6 words maximum are synthenzed in correspondence to the CO through C5 keys.
Chattering absorption for key inputs is in effect. ($\overline{OSCG}$ = 'H')



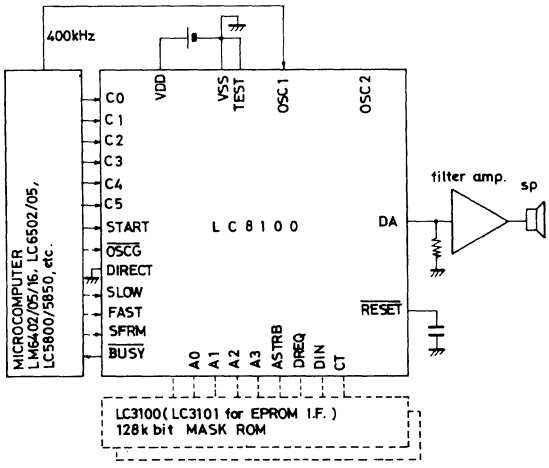
- When not in an all—'L' state, and any one of CO through C5 attains an 'H' level, power-down will be disengaged, and speech synthesis started.
- Some time is required until the OSC oscillation is stable; the LC8100 maintains $\overline{RESET}$ state for the length of time designated by the C that is added on to the $\overline{RESET}$ pin.
- Upon concluding synthesis, if CO through C5 are all at 'L' levels, the power-down mode is entered.
- When an 'H' level is held at CO through C5, synthesis will be concluded, but no power-down mode will be entered. Only when all of CO through C5 attain 'L' levels, will a power-down mode be entered.
- To vary synthesis speed, the SLOW and FAST terminals are used.

Synthesis Start Timing Chart.



Application Example 2 Microcomputer–Controlled Mode (Index Addressing)

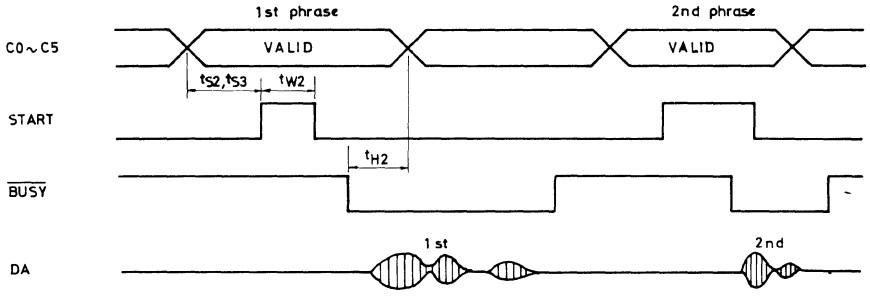
Generates up to 63 words maximum in accordance with signal at C0 through C5.



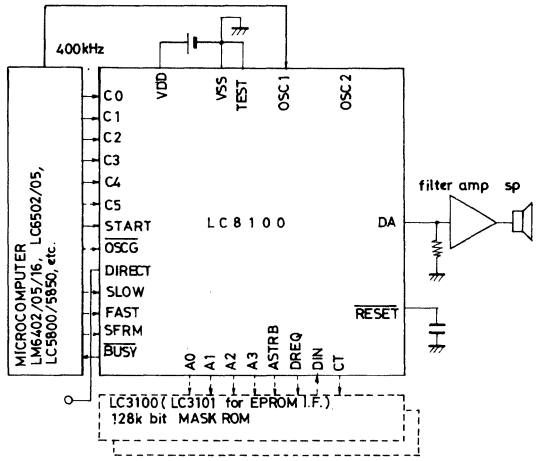
- The $\overline{\text{OSCG}}$ terminal is used for power-down control.
- To vary speech speed, use the SLOW and FAST pins.
- For speech of long duration, use LC3100 mask ROMs.
  About 100 seconds/piece; up to 16 pieces of ROMs may be connected.
- For speech employing EPROMs, LC3101 EPROM interfaces are used.

Timing Chart when starting Word/Phrase Synthesis.

- Data impressed upon C0 through C5 must be held until $\overline{\text{BUSY}}$ attains an 'L' level.



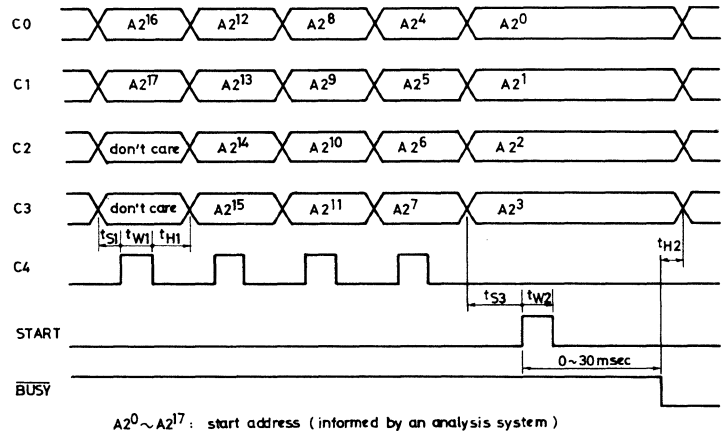
Application Example 3 Microcomputer–Controlled Mode (Direct Addressing)



By directly specifying the leading address of words/phrases through the use of CO through C4, more than 63 words may be specified.

In this process, the CO through C3 4-bit data is divided and address-specified in five separate addressings. C4 is used as a setting clock for the individual 4-bit data.

Timing Chart when starting Word/Phrase Synthesis.



- No pulse should be impressed on the C4 terminal for $A2^0$ to $A2^3$ data.
- The $A2^0$ to $A2^3$ data has to be held until $\overline{BUSY}$ attains 'L' level.

HOW TO USE POWER-DOWN MODES

In the power-down mode, the LC8100 halts oscillation and reduces current consumption to less than 10 μA. Power-down is controlled by $\overline{OSCG}$. When OSCG is at an 'L' level, LC8100 is always in an operative state.

(1) Inducing power-down mode
To make the LC8100 enter the power-down mode, keep $\overline{OSCG}$ high. If not currently generating speech, LC8100 immediately enters into the power-down mode.

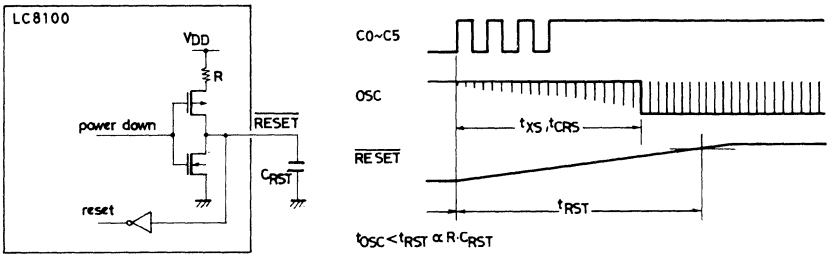
(2) Disengaging from power-down (version 1)
Lowering the $\overline{OSCG}$ terminal potential to an 'L' level disengages power-down.

(3) Disengaging power-down (version 2)
Issue a speech start command. When a speech start instruction occurs the LC8100 is in power-down mode, it will automatically disengage the power-down mode, irrespective of the signal at $\overline{OSCG}$. Immediately after disengaging from power-down and starting oscillation, oscillation is not yet unstable. The LC8100 will automatically enter into a self-reset state for a fixed length of time. (The length of time is determined by the capacitor externally connected to the $\overline{RESET}$ pin and the internal pull-up resistor. Usually, assuming C = 0.1 μF, the self-reset time is 8 to 100 msec.)

After the fixed reset time, the LC8100 starts speech synthesis in accordance with the specified start signal.

After concluding speech, if $\overline{OSCG}$ is at an 'H' level, the LC8100 will again automatically enter the power-down mode.

(4) Power-Down Example 1) ——— when LC8100 in employed as a single chip
When LC8100 is employed as a single chip, the $\overline{OSCG}$ pin is usually tied high, and the automatic power-down function is utilized. In this process, a capacitor must always be used, on the $\overline{RESET}$ pin, which will force a longer reset time than the oscillation stabilizing time.



Upon conclusion of speech synthesis, if the automatic power-down mode is induced, the LC8100 will look at C0 through C5 and START.

If (C0 + C1 + C2 + C3 + C4 + C5) · START = 'L', then it will automatically enter into the power-down mode. Otherwise it will remain operative, (non-synthesizing) until the result becomes 'O'. (Refer to application example (1) One-word, one-key system.)

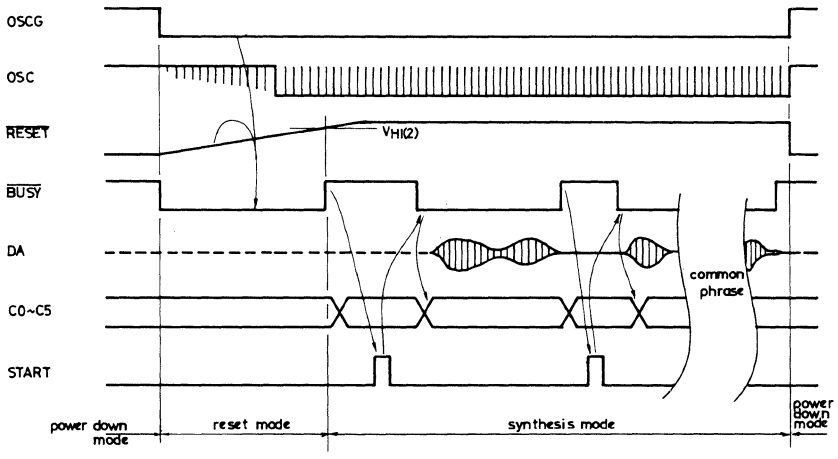
(5) Power-Down Application Example (2) ——— when editing text using a microcomputer

When editing text using a number of words, and using the power-down function as well, it will be necessary to have a microcomputer control $\overline{OSCG}$.

Upon disengaging power-down, a waiting period equalling the oscillation stabilizing time is always required. When editing text, first $\overline{OSCG}$ is reduced to an 'L' level, bringing about an operative mode. Then text is combined all the way through in the operative mode unaltered (with the oscillation going on, and with no waiting time), after which $\overline{OSCG}$ is again made high, and the power-down mode entered into.

When first disengaging power-down, the waiting time for oscillation stabilization is still required.

This waiting time is created by the capacitor externally connected to the $\overline{RESET}$ pin ($C > 0.1\ \mu F$). In order to advise the microcomputer of the stabilized oscillation after $\overline{OSCG}$ attains an 'L' level, the LC8100 outputs to the microcomputer the $\overline{BUSY}$ = 'L' for the duration of oscillation instability (reset time). Accordingly, the microcomputer is required to issue a start instruction, only after detecting $\overline{BUSY}$ = attained 'H' level.

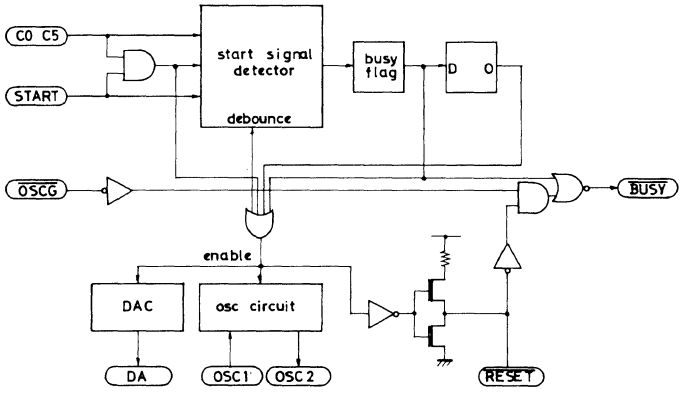


(6) The controlled status of the main circuits in power down mode and in operation mode

Status of Various Sections in Power-Down Mode

Status / Main circuit	Operation state (including non-synthesizing modes)	Power-down state
OSC	Always oscillates	Stops
DAC	Active	Output is floating
Resetting circuit	Is reset by externally setting $\overline{RESET}$ low.	• LC8100 is always in a reset state by internal reset function. • When power-down has been disengaged, reset is disengaged after the lapse of time determined by the time constant of a C externally connected to $\overline{RESET}$ terminal and the internal pull-up resistor R=200 k ohms typ.
$\overline{BUSY}$ output	An 'L' level output during synthesis An 'H' level output during non-synthesis	• Always outputs an 'H' level • When power-down is disengaged by $\overline{OSCG}$ = 'L', outputs $\overline{BUSY}$ = 'L' only during the reset period until oscillation stabilizes, in which case both $\overline{OSCG}$ and $\overline{RESET}$ remain at 'L' levels. (Although a synthesize signal has been provided, oscillation is not yet stabilized.)

Power-Down Control Circuit Outline Diagram



KEY DEBOUNCING CIRCUIT

The CO through C5 and START pins are sometimes connected to switches; at other times they are connected to a microcomputer and other output signals.

The chattering disposal circuitry is controlled by the $\overline{OSCG}$ signal to be switched on and off as required.

1) When $\overline{OSCG}$ = 'L', chattering is not supressed. Although extremely short start signals are long enough to trigger operations, the CO through C5 signals have to be continuously held until an 'L' level is output at $\overline{BUSY}$.
   Usually the $\overline{BUSY}$ output attains an 'L' level with a few msec after a start signal.
2) When $\overline{OSCG}$ = 'H', the suppress chattering circuits function.
   Chattering suppress is effective for 10 msec.

SPEECH SPEED CONTROL AND PARAMETER BIT RATES

The LC8100 has three terminals for variation of speech speeds and parameter bit rates.

These are SFRM, SLOW, and FAST, and all control the LC8100 frame length (the unit time in analysis and synthesis). The speed and the parameter bit rate are closely related to the conditions for analysis of parameters. These relations are shown in the table below.

Relations between Analysis/Synthesis conditions and Speeds (with standard speed represented by 1.0)

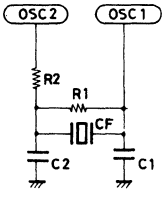
Terminal conditions for synthesis / Analysis conditions			Frame length	20 ms	10 ms	20 ms	10 ms	25 ms
			Parameters within a frame	48BITS	48BITS	96BITS	96BITS	48BITS
SFRM	FAST	SLOW						
'L'	'L'	'H'		0.75	0.375	Inhibited	Inhibited	1.0/1880BPS
'L'	'L'	'L'		1.0/2400BPS	0.5	Inhibited	Inhibited	1.25
'L'	'H'	'L'		1.25	0.625	Inhibited	Inhibited	1.5
'H'	'L'	'H'		1.5	0.75	Inhibited	Inhibited	2.0
'H'	'L'	'L'		2.0	1.0/4800BPS	Inhibited	Inhibited	2.5
'H'	'H'	'L'		2.5	1.25	Inhibited	Inhibited	3.0
'L'	'H'	'H'		Inhibited	Inhibited	1.0/4800BPS	0.5	Inhibited
'H'	'H'	'H'		Inhibited	Inhibited	2.0	1.0/9600BPS	Inhibited

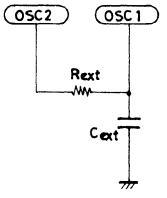
OSCILLATING CIRCUIT

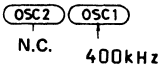
Any one of the following three types of oscillators may be utilized as the LC8100 oscillating circuit:

1) Ceramic oscillator
2) CR oscillator
3) External clock

The standard operating frequency is 400 kHz, but an 800-kHz clock, using a 1/2 frequency dividing circuit option, can also be used.





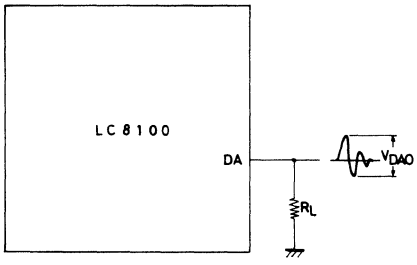


R1: 1MΩ
R2: 4.7kΩ (High-voltage version)
or 2.2kΩ (Low-voltage version)
C1: 220pF
C2: 220pF
CF: CSB400p (Murata)

Rext: 15kΩ (High-voltage version)
Cext: 330pF (High-voltage version)

DA OUTPUT TERMINAL (Audio Signal Output Terminal)

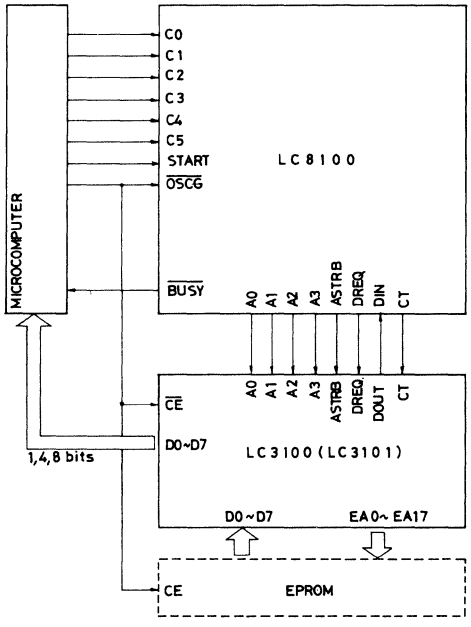
When the DA terminal is terminated with a resistor to the VSS side, audio signals are output at the DA terminal. The DA terminal becomes a high impedance in a power mode. Accordingly, when terminated with a resistor, it will be at the VSS potential.



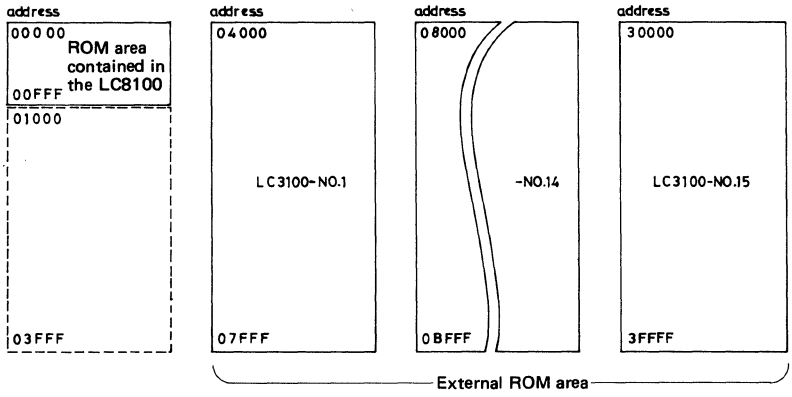
INTERFACE WITH EXTERNAL ROM

An interfacing circuit for an external ROM, LC3100 is shown below.

Both the LC8100 and LC3100 (LC3101) have built-in interfacing circuits. Accordingly, AO through A3, ASTRAB, DREQ, DOUT, and CT need only be wire connected.



Shown below is the memory map when an external ROM is used.

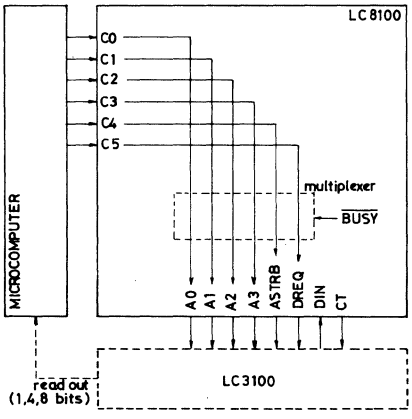


Note 1. In this organization the area from address 01000 to 03FFF cannot be used.

Note 2. If the ROM contained in the LC8100 is not used (mask option), the area from 00000 to 03FFF can be allocated to an external ROM.

Note 3. In the index addressing mode the whole ROM area can be addressed.

When storing data other than speech parameters in an external ROM:



When not synthesizing, the CO through C5 terminals and the AO through A3, ASTRAB, and DREQ terminals of the LC8100 are electrically interconnected. (See diagram)

The microcomputer, can designate the LC3100 addresses and read out the ROM contents, via the LC8100.

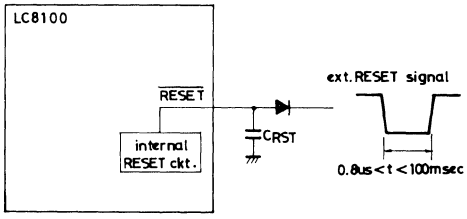
Accordingly, by storing speech parameters and data other than parameters within LC3100, the LC3100 may be utilized as an external memory for the microcomputer.

HOW TO RESET THE LSI

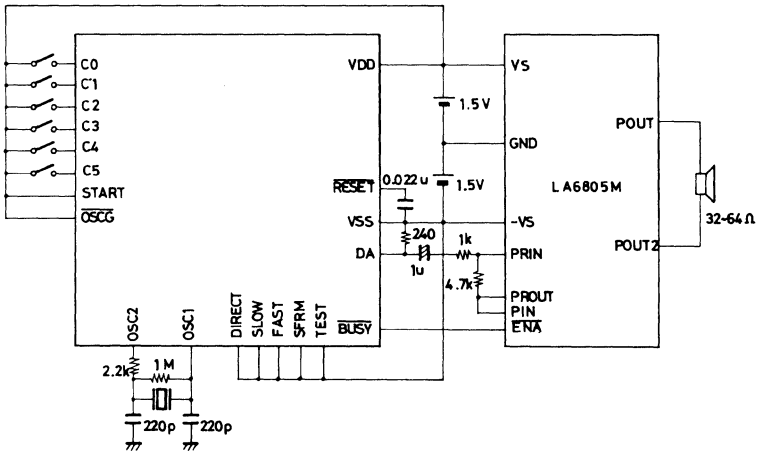
The LC8100 contains an internal RESET circuit to deliver the reset signal at the $\overline{\text{RESET}}$ pin for automatic resetting. When forcing to externally reset against this signal, the following must be observed. (Ex. Pause of speech)

(1) A diode must be connected across the $\overline{\text{RESET}}$ pin and an external signal.

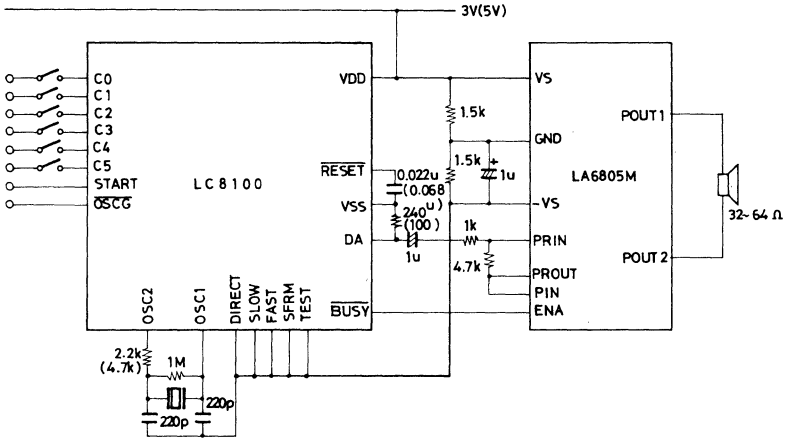
(2) The time during which the $\overline{\text{RESET}}$ pin is forced to be set to "L" level must not exceed 100ms.



APPLICATION CIRCUIT EXAMPLE 1



APPLICATION CIRCUIT EXAMPLE 2



- [Specify either the low-voltage version or the high-voltage version.]

LC8100L (Low-voltage version)

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max	V_{DD} pin	-0.3~+5.0	V
Input Voltage	V_{IN}	All input pins	-0.3~V_{DD}+0.3	V
Output Current	I_O	Except DA pin, per pin	-2.0~+2.0	mA
Output Voltage	V_{OUT}	All output pins	-0.3~V_{DD}+0.3	V
Allowable Power Dissipation	P_d max	Ta=-30℃~+70℃	200	mW
Operating Temperature	T_{opg}		-30~+70	℃
Storage Temperature	T_{stg}		-55~+125	℃

Allowable Operating Ranges/T_a=−30°C to +70°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD}	2.7	3.0	3.5	V
Input "H" Level Voltage	V_{IH}(1)	$\overline{RESET}$, all input pins other than OSC1	0.7V_{DD}		V_{DD}	V
	V_{IH}(2)	$\overline{RESET}$	0.75V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}(1)	$\overline{RESET}$, all input pins other than OSC1	V_{SS}		0.3V_{DD}	V
	V_{IL}(2)	$\overline{RESET}$	V_{SS}		0.25V_{DD}	V
External Capacitance for Ceramic OSC	C1	Composed of OSC1, OSC2, Fig. 1	typ-10%	220	typ+10%	pF
	C2	〃	typ-10%	220	typ+10%	pF
External Resistance for Ceramic OSC	R1	〃	typ-5%	1000	typ+5%	kΩ
	R2	〃	typ-5%	2.2	typ+5%	kΩ
Reset Guaranteed Constant	CRST	$\overline{RESET}$, Fig. 3	typ-10%	0.022	typ+10%	μF
Operating Frequency	fext	OSC1	200	400	520	kHz
"H" Level Clock Pulse Width	twφH	OSC1, Fig. 5	0.75	1.25		μs
"L" Level Clock Pulse Width	twφL	〃	0.75	1.25		μs
"H" Level Clock Input Voltage	VIHφ	〃	0.75V_{DD}		V_{DD}	V
"L" Level Clock Input Voltage	VILφ	〃	V_{SS}		0.25V_{DD}	V
Data Input Setting Time	tIS	DREQ, DIN, Fig. 6	1.2			μs
Chattering Absorb Time	tC	C0~C5, START, $\overline{OSCG}$=H	7.5		50	ms
Data Setup Time	tS1	C0~C3, C4, DIRECT=H, Fig. 7	0.8			μs
	tS2	C0~C5, START, DIRECT=H, Fig. 8	0.8			μs
	tS3	C0~C5, START, DIRECT=L, Fig. 8	0.8			μs
C4 Pulse Width	tw1	C4, DIRECT=H, Fig. 7	0.8			μs
START Pulse Width	tw2	START, DIRECT=H, $\overline{OSCG}$=L, Fig. 8	0.8			μs
Reset Pulse Width	tw3	$\overline{RESET}$, $\overline{OSCG}$=L OSC stabilized mode, Fig. 9	0.8			μs
Data Hold Time	tH1	C0~C3, C4, DIRECT=H, Fig. 7	0			μs
	tH2	C0~C5, BUSY, Fig. 8	0			μs

(Note) The V_{DD} range must be as specified in the Allowable Operating Ranges above unless otherwise specified.

Electrical Characteristics/T_a=−30°C to +70°C, V_{SS}=0V, V_{DD}=2.7V to 3.5V

			min	typ	max	unit
Input "H" Level Current	IIH(1)	START, $\overline{OSCG}$, DIRECT, DIN, TEST, FAST, SLOW, SFRM, C0~C5, $\overline{OSCG}$=L, VIN=V_{DD}			1.0	μA
	IIH(2)	C0~C5, $\overline{OSCG}$=H	0.5		20	μA
Input "L" Level Current	IIL(1)	START, $\overline{OSCG}$, DIRECT, DIN, TEST, FAST, SLOW, SFRM, C0~C5, VIN=V_{SS}	-1.0			μA
Output "H" Level Voltage	VOH(1)	A0~A3, ASTRB, DREQ, CT, ION=-0.3mA	V_{DD}-0.6			V
	VOH(2)	$\overline{BUSY}$, IOH=-30μA	V_{DD}-0.2			V
		$\overline{BUSY}$, IOH=-0.3mA	V_{DD}-0.6			V
	VOH(3)	OSC2, IOH=-0.3mA	V_{DD}-0.6			V

			min	typ	max	unit
Output "L" Level Voltage	$V_{OL(1)}$	A0~A3, ASTRB, DREQ, CT I_{OL}=0.3mA			0.6	V
	$V_{OL(2)}$	$\overline{BUSY}$, I_{OL}=30μA			0.2	V
		$\overline{BUSY}$, I_{OL}=1mA			0.6	V
	$V_{OL(3)}$	OSC2, I_{OL}=0.3mA			0.6	V
Reset Time	t_{RST}	$\overline{RESET}$, C_{RST}=0.022μF±10%, Fig. 3	7	20	70	ms
Pull-up Resistance	R_{UP}	$\overline{RESET}$, V_O=1/2V_{DD}	300	800	2300	kΩ
Pull-down Resistance	R_{DOWN}	$\overline{RESET}$, V_O=1/2V_{DD}	8	20	65	kΩ
"H" Threshold Voltage	V_{t*H}	$\overline{RESET}$	0.35V_{DD}	0.55V_{DD}	0.75V_{DD}	V
"L" Threshold Voltage	V_{t*L}	$\overline{RESET}$	0.25V_{DD}	0.45V_{DD}	0.70V_{DD}	V
Hysteresis Voltage	V_{HIS}	$\overline{RESET}$		0.1V_{DD}		V
Ceramic OSC Frequency	f_{XOSC}	OSC1, 2, Fig. 1	384	400	416	kHz
Cermaic OSC Stabilization Time	t_{XS}	OSC1, 2			7	ms
DA Converter Max.	V_{DAO}	DA, R_L=240Ω	0.12	0.4	1.2	Vp-p
Output Amplitude		DA, V_{DD}=3.0V, R_L=240Ω, Ta=25℃	0.22	0.4	0.7	Vp-p
DA Converter Output OFF Leak Current	I_{OFF}	DA, V_{OUT}=V_{SS}	-10			μA
Current Dissipation	I_{DD1}	V_{DD}, DA Output open, Fig. 10			2	mA
	I_{DD2}	V_{DD}, Fig. 11			10	μA
Input Pin Capacitance	C_I	All input pins, f=1MHz		5		pF

LC8100M (High-voltage version)

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DDmax}	V_{DD} pin	-0.3~+7.0	V
Input Voltage	V_{IN}	All input pins	-0.3~V_{DD}+0.3	V
Output Current	I_O	Except DA pin, per pin	-2.0~+2.0	mA
Output Voltage	V_{OUT}	All output pins	-0.3~V_{DD}+0.3	V
Allowable Power Dissipation	P_{dmax}	Ta=-30℃~+70℃	200	mW
Operating Temperature	T_{opg}		-30~+70	℃
Storage Temperature	T_{stg}		-55~+125	℃

Allowable Operating Ranges/T_a=−30°C to +70°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD}	2.7		6.5	V
Input "H" Level Voltage	$V_{IH(1)}$	$\overline{RESET}$, all input pins other than OSC1	0.7V_{DD}		V_{DD}	V
	$V_{IH(2)}$	$\overline{RESET}$	0.75V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL(1)}$	$\overline{RESET}$, all input pins other than OSC1	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	$\overline{RESET}$	V_{SS}		0.25V_{DD}	V
External Capacitance for Ceramic OSC	C_1	Composed of OSC1, OSC2, Fig. 1	typ-10%	220	typ+10%	pF
	C_2	〃	typ-10%	220	typ+10%	pF
External Resistance for Ceramic OSC	R_1	〃	typ-5%	1000	typ+5%	kΩ
	R_2	〃	typ-5%	4.7	typ+5%	kΩ
External Capacitance for CR OSC	C_{ext}	Composed of OSC1, OSC2, V_{DD}=4.5V~6.5V, Fig. 2	typ-5%	330	typ+5%	pF
External Resistance for CR OSC	R_{ext}	〃	typ-1%	15	typ+1%	kΩ
Reset Guaranteed Constant	C_{RST}	$\overline{RESET}$, Fig. 3	typ-10%	0.068	typ+10%	μF
Operating Frequency	f_{ext}	OSC1	200	400	520	kHz
"H" Level Clock Pulse Width	$t_{wφH}$	OSC1, Fig. 5	0.75	1.25		μs
"L" Level Clock Pulse Width	$t_{wφL}$	〃	0.75	1.25		μs
"H" Level Clock Input Voltage	$V_{IHφ}$	〃	0.75V_{DD}		V_{DD}	V
"H" Level Clock Input Voltage	$V_{ILφ}$	〃	V_{SS}		0.25V_{DD}	V
Data Input Setting Time	t_{IS}	DREQ, DIN, Fig. 6	1.2			μs
Chattering Absorb Time	t_C	C0~C5, START, $\overline{OSCG}$=H	7.5		50	ms

			min	typ	max	unit
Data Setup Time	t_{S1}	C0~C3, C4, DIRECT=H, Fig. 7	0.8			μs
	t_{S2}	C0~C5, START, DIRECT=H, Fig. 8	0.8			μs
	t_{S3}	C0~C5, START, DIRECT=L, Fig. 8	0.8			μs
C4 Pulse Width	t_{w1}	C4, DIRECT=H, Fig. 7	0.8			μs
START Pulse Width	t_{w2}	START, DIRECT=H, $\overline{OSCG}$=L, Fig. 8	0.8			μs
Reset Pulse Width	t_{w3}	$\overline{RESET}$, $\overline{OSCG}$=L, OSC stabilized mode, Fig. 9	0.8			μs
Data Hold Time	t_{H1}	C0~C3, C4, DIRECT=H, Fig. 7	0			μs
	t_{H2}	C0~C5, BUSY, Fig. 8	0			μs

Electrical Characteristics/T_a=−30°C to +70°C, V_{SS}=0V, V_{DD}=4.5V to 5.5V

			min	typ	max	unit
Input "H" Level Current	$I_{IH(1)}$	START, $\overline{OSCG}$, DIRECT, DIN, TEST, FAST, SLOW, SFRM, C0~C5, $\overline{OSCG}$=L, V_{IN}=V_{DD}			1.0	μA
	$I_{IH(2)}$	C0~C5, $\overline{OSCG}$=H	0.4		40	μA
Input "L" Level Current	$I_{IL(1)}$	START, $\overline{OSCG}$, DIRECT, DIN, TEST, FAST, SLOW, SFRM, C0~C5, V_{IN}=V_{SS}	-1.0			μA
Output "H" Level Voltage	$V_{OH(1)}$	A0~A3, ASTRB, DREQ, CT, I_{OH}=-0.3mA	V_{DD}-0.6			V
	$V_{OH(2)}$	$\overline{BUSY}$, I_{OH}=-0.3mA				V
	$V_{OH(3)}$	OSC2, I_{OH}=-0.3mA	V_{DD}-0.6			V
Output "L" Level Voltage	$V_{OL(1)}$	A0~A3, ASTRB, DREQ, CT I_{OL}=0.3mA	V_{DD}-0.6		0.6	V
	$V_{OL(2)}$	$\overline{BUSY}$, I_{OL}=1mA			0.6	V
	$V_{OL(3)}$	OSC2, I_{OL}=0.3mA			0.6	V
Reset Time	t_{RST}	$\overline{RESET}$, C_{RST}=0.068μF±10%, Fig. 3	7	20	70	ms
Pull-up Resistance	R_{UP}	$\overline{RESET}$, V_O=1/2V_{DD}	150	300	800	kΩ
Pull-down Resistance	R_{DOWN}	$\overline{RESET}$, V_O=1/2V_{DD}	3.5		20	kΩ
"H" Threshold Voltage	V_{t*H}	$\overline{RESET}$	0.4V_{DD}	0.55V_{DD}	0.75V_{DD}	V
"L" Threshold Voltage	V_{t*L}	$\overline{RESET}$	0.25V_{DD}	0.45V_{DD}	0.60V_{DD}	V
Hysteresis Voltage	V_{HIS}	$\overline{RESET}$		0.1V_{DD}		V
Ceramic OSC Frequency	f_{XOSC}	OSC1, 2, Fig. 1	384	400	416	kHz
Ceramic OSC stabilization Time	t_{XS}	OSC1, 2			7	ms
CR OSC Freqeuncy	f_{CROSC}	OSC1, 2, Cext=330pF±5% Rext=15kΩ±1%, Fig. 2	308	400	520	kHz
CR OSC Stabilization Time	t_{CRS}	OSC1, 2			7	ms
DA Converter Max. Output Amplitude	V_{DAO}	DA, R_L=100Ω	0.20	0.60	1.50	Vp-p
		DA, V_{DD}=5.0V, R_L=100Ω, Ta=25℃	0.40	0.60	0.90	Vp-p
DA Converter Output OFF Leak Current	I_{OFF}	DA, V_{OUT}=V_{SS}	-10			μA
Current Dissipation	I_{DD1}	V_{DD}, DA Output open, Fig. 10			2	mA
	I_{DD2}	V_{DD}, Ta=-30℃~+40℃. Fig. 11			10	μA
Input Pin Capacitance	C_I	All input pins, f=1MHz		5		pF

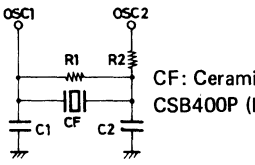


Fig. 1 Recommended Ceramic OSC Circuit

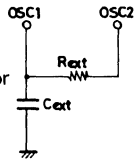


Fig. 2 Recommended CR OSC Circuit

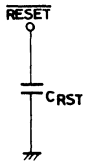


Fig. 3 Reset Circuit

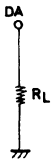


Fig. 4 DA Load Circuit

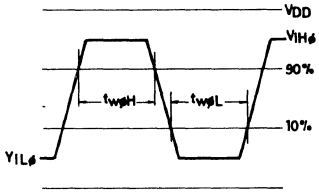


Fig. 5 OSC1 External Drive Waveform

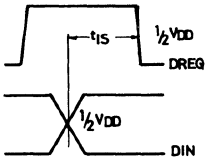


Fig. 6 Data Input Setting Time

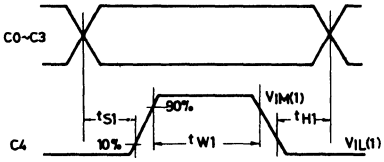


Fig. 7 Waveform at Address Setting Mode

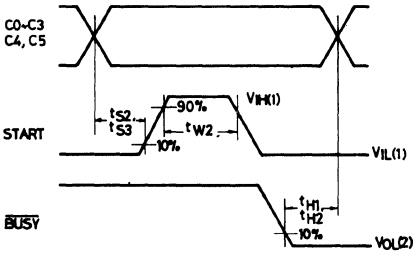


Fig. 8 Waveform at Address Setting Mode

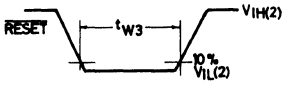
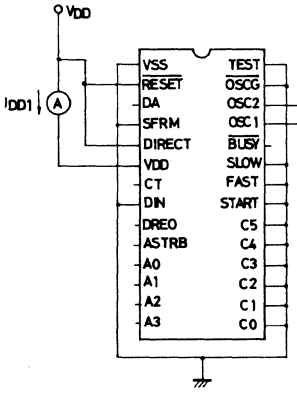


Fig. 9 Reset Waveform



(Note)
The load current of the DA converter is not included in the current dissipation specified above. In other than the power-down mode the load current of the DA converter is also dissipated besides the current dissipation of the LSI.

Fig. 10 Current Dissipation Test Circuit (Operating Mode)

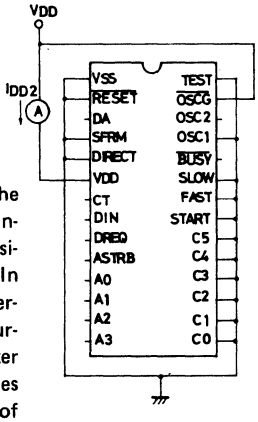
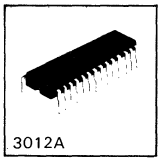


Fig. 11 Current Dissipation Test Circuit (Power-down Mode)

LM3700



N MOS LSI

4096 Words by 10-Bits Mask Programmable ROM

Ⓔ 1516

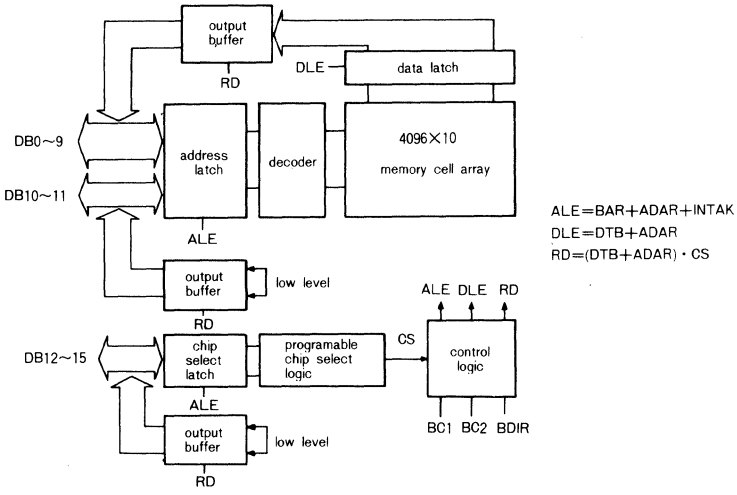
General Description

The LM3700 is a mask programmable ROM that is organized as 4096 words x 10 bits, makes the address input pins/read-out data output pins usable in common to facilitate interfacing with various uCPU's, and is designed for time-sharing address data input/read-out data output on the 3-bit control signal.

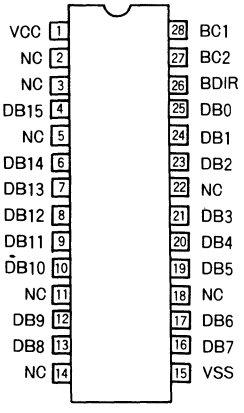
Features

- Single 5V supply : 5V±10%
- Organized as 4096 words x 10 bits
- 16-bit address latch
- 3 control code inputs : BC1, BC2, BDIR
- Mask programmable chip select decoder

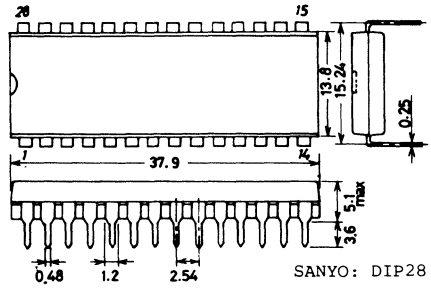
Block Diagram



Pin Assignment

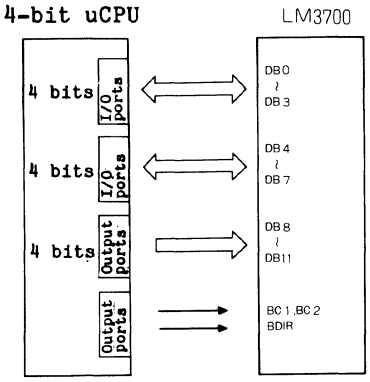


Case Outline 3012A-D28IC (unit:mm)



SANYO: DIP28

Sample Application Circuit where the LM3700 is used as an external memory (4096 x 8 bits) for a 4-bit single-chip uCPU



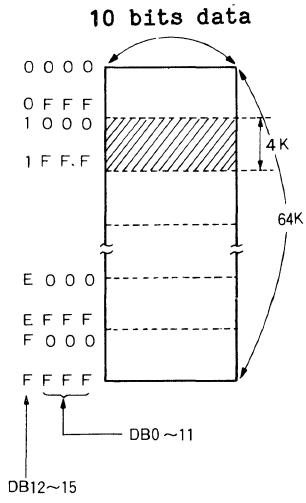
1.**Description of Operation**

The LM3700 has 3 control code input pins (BC1, BC2, BDIR) for operation mode select and 16 I/O pins (DB0 to 15) for address data input/memory data output. When a control code for selecting an input mode is applied to the control code input pins, the I/O pins are set to input use and the address data for selecting one of the 4096 words is inputted to the address latch from the DB0 to 11 pins. The chip select data is inputted to the chip select latch from the remaining DB12 to 15 pins.

When a control code for selecting an output mode is applied to the control code input pins, the I/O pins are set to output use and the 10-bit memory data is outputted from the DB0 to 9 pins if the data equivalent to the chip select code of the chip is applied to the DB12 to 15 pins. (The DB10 to 15 pins are fixed at "L" level.)

2.**Mask Programmable Chip Select Decoder**

The mask programmable chip select decoder for decoding 4 bits of DB12 to 15 can be used to place 4K x 10 bits memory data in any location of the 64K word memory address.



Any value of DB12 to 15=0 to F(HEX) can be mask-programmed as the chip select code.

3. Operation of the LM3700 Corresponding to Each Control Code

Eight combinations of 3-bit control signal cause the LM3700 to be operated as shown below.

<table>
<tr><th colspan="3">Control Code Input Pin</th><th rowspan="2">Command</th><th colspan="3">I/O Pin</th><th rowspan="2">Operation of LM3700</th></tr>
<tr><th>BDIR</th><th>BC1</th><th>BC2</th><th>DB0 to 9</th><th>DB10 to 11</th><th>DB12 to 15</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NACT</td><td colspan="3" rowspan="4">High impedance.
No memory data is outputted.</td><td>(1)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IAB</td><td>(2)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DWS</td><td>(2)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DS</td><td>(2)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ADAR</td><td rowspan="2">Memory data is outputted.</td><td colspan="2" rowspan="2">Fixed at "L" Level.</td><td>(3)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DTB</td><td>(4)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>BAR</td><td colspan="2" rowspan="2">Address data is inputted to chip select latch.</td><td rowspan="2">Chip select data is inputted to chip select latch.</td><td>(5)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>INTAK</td><td>(5)</td></tr>
</table>

Explanation of operation The No. in ( ) shown below corresponds to the No. in the Table shown above.

(1) No operation. Neither address data nor chip select data is inputted and the data for the preceding cycle is held. The output buffer is set to the high impedance state and no memory data is outputted.

(2) The LM3700 does not respond to these commands and no operation is performed as in (1).

(3) If the data equivalent to the chip select code is applied to the DB12 to 15 beforehand, the memory data is outputted. (The DB0 to 9 output the memory data and the DB10 to 15 are fixed at "L" level.)
If other data than the chip select code is applied, the output buffer is set to the high impedance state and no memory data is outputted. (A chip with a different chip select code can be wired-OR connected.) The data outputted at the I/O pins is inputted intact to the address latch, chip select latch at the end of the cycle.

(4) If the data equivalent to the chip select code is applied to the DB12 to 15 beforehand, the memory data is outputted. (The DB0 to 9 output the memory data and the DB10 to 15 are fixed at "L" level.)
If other data than the chip select code is applied, the output buffer is set to the high impedance state and no memory data is outputted. No operation is performed to input the data to the address latch, chip select latch.

(5) The I/O pins are set to input use. The address data for selecting one of the 4096 words and the chip select data are inputted to the address latch and chip select latch respectively.

Absolute Maximum Ratings at Ta=+25°C, V_{SS}=0V

			unit
Maximum Supply Voltage	$V_{CC}max$	-0.3 to 9.0	V
Input Voltage	V_{IN}	-0.3 to V_{CC}	V
Allowable Power Dissipation	Pdmax	0.35	W
Operating Temperature	Topg	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C

Allowable Operating Ranges at Ta=0 to +70°C, V_{SS}=0V

		min	typ	max	unit
Supply Voltage	V_{CC}	4.5		5.5	V
Input "H" Level Voltage	V_{IH}	2.4		V_{CC}	V
Input "L" Level Voltage	V_{IL}	0		0.7	V

DC Electrical Characteristics at Ta=0°C to +70°C, V_{SS}=0V, V_{CC}=4.5V to 5.5V

			min	typ	max	unit
Input Leakage Current	I_{IN}	V_{IN}=0V to V_{CC}	-5		5	uA
Output "H" Level Voltage	V_{OH}	I_{OH}=80uA	2.4			V
Output "L" Level Voltage	V_{OL}	I_{OL}=1.5mA			0.5	V
Current Dissipation	I_{CC}	DC1=BC2=BDIR=Don't Care Output OPEN			60	mA

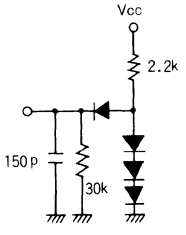
AC Electrical Characteristics at Ta=0°C to +70°C, V_{SS}=0V, V_{CC}=4.5V to 5.5V

		min	typ	max	unit
Control Code Stable Time	t_{CCS}	885			ns
Address setup Time	t_{ASU}	300			ns
Address Hold Time	t_{AH}	60			ns
No Action Time	t_{NACT}	885			ns
Output Data Delay Time	t_{DO}			350	ns
Output Data Hold Time	t_{DH}	80			ns
Floating Delay Time	t_{FL}			300	ns
Control Code Stable Time	t_{SKEW}			50	ns

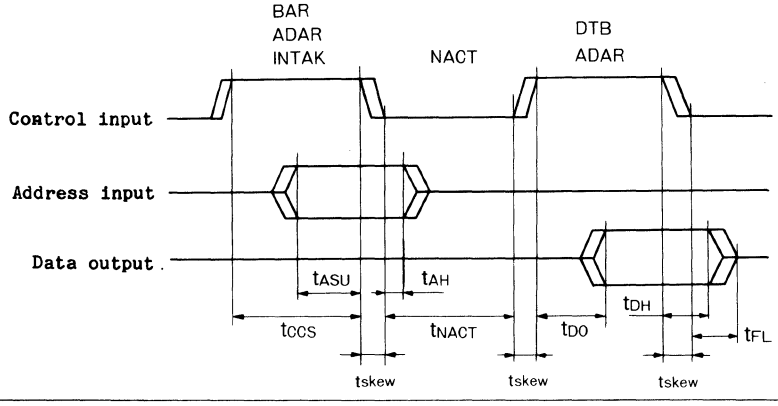
Capacitance at Ta=+25°C, V_{SS}=0V

			min	typ	max	unit
Input Capacitance	C_{IN}	V_{IN}=0V, f=1MHz			10	pF

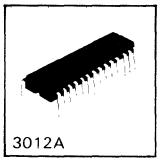
Output Load Circuit at AC Test



Timing Chart



LM3710



N MOS LSI

8192 Words by 10-Bits Mask Programmable ROM

Ⓔ 1517

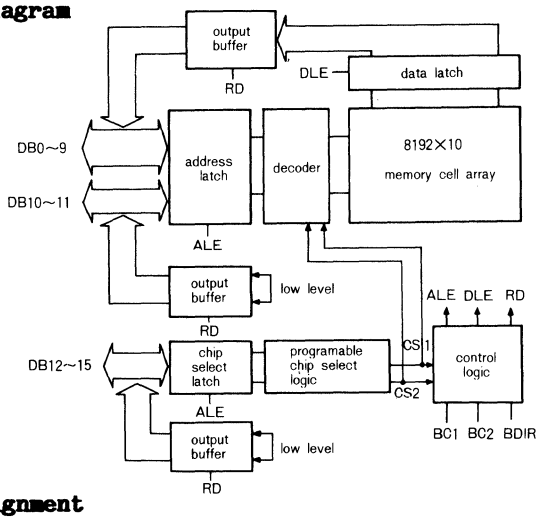
General Description

The LM3710 is a mask programmable ROM that is organized as 8192 words x 10 bits, makes the address input pins/read-out data output pins usable in common to facilitate interfacing with various uCPU's, and is designed for time-sharing address data input/read-out data output on the 3-bit control signal.

Features

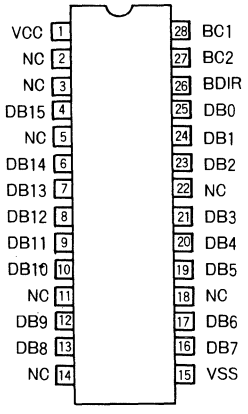
- Single 5V supply : 5V±10%
- Organized as 8192 words x 10 bits
- 16-bit address latch
- 3 control code inputs : BC1, BC2, BDIR
- 2 channels of 4-bit programmable chip select decoder

Block Diagram

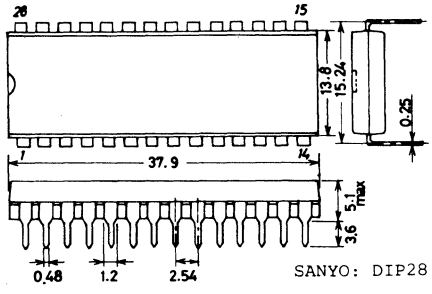


ALE=BAR+ADAR+INTAK
DLE=DTB+ADAR
RD=(DTB+ADAR)・(CS1+CS2)

Pin Assignment

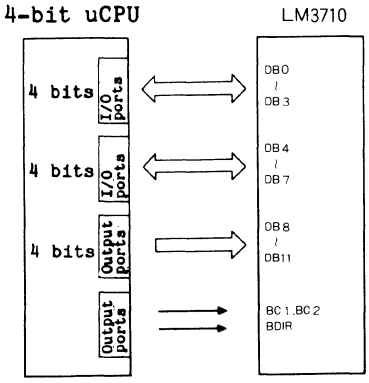


Case Outline 3012A-D28IC
(unit:mm)



SANYO: DIP28

Sample Application Circuit where the LM3710 is used as an external memory (8192 x 8 bits) for a 4-bit single-chip uCPU



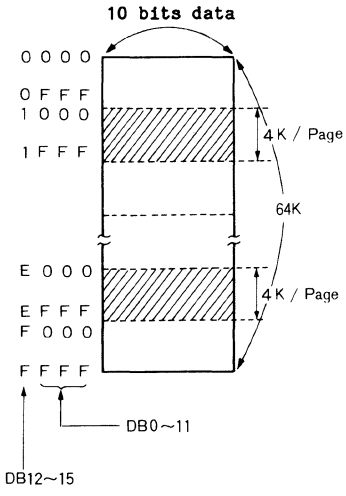
1.**Description of Operation**

The LM3710 has 3 control code input pins (BC1, BC2, BDIR) for operation mode select and 16 I/O pins (DB0 to 15) for address data input/memory data output. When a control code for selecting an input mode is applied to the control code input pins, the I/O pins are set to input use and the address data for selecting one of the 8192 words is inputted to the address latch from the DB0 to 11 pins. The chip select data is inputted to the chip select latch from the remaining DB12 to 15 pins.

When a control code for selecting an output mode is applied to the control code input pins, the I/O pins are set to output use and the 10-bit memory data is outputted from the DB0 to 9 pins if the data equivalent to the chip select code of the chip is applied to the DB12 to 15 pins. (The DB10 to 15 pins are fixed at "L" level.)

2.**Mask Programmable Chip Select Decoder**

Two channels of the mask programmable chip select decoder for decoding 4 bits of DB12 to 15 can be used to place 8K x 10 bits memory data in any location of the 64K word memory address (4k/page):



Any value of DB12 to 15=0 to F(HEX) can be mask-programmed as the chip select code.

3. Operation of the LM3710 Corresponding to Each Control Code

Eight combinations of 3-bit control signal cause the LM3710 to be operated as shown below.

Control BDIR	Code BC1	Input Pin BC2	Command	I/O Pin DB0 to 9	DB10 to 11	DB12 to 15	Operation of LM3710
0	0	0	NACT	High impedance. No memory data is outputted.			(1)
0	0	1	IAB				(2)
1	0	1	DWS				(2)
1	1	0	DS				(2)
0	1	0	ADAR	Memory data is outputted.	Fixed at "L" Level.		(3)
0	1	1	DTB				(4)
1	0	0	BAR	Address data is inputted to address latch.		Chip select data is inputted to chip select latch.	(5)
1	1	1	INTAK				(5)

Explanation of operation The No. in ( ) shown below corresponds to the No. in the Table shown above.

(1) No operation. Neither address data nor chip select data is inputted and the data for the preceding cycle is held. The output buffer is set to the high impedance state and no memory data is outputted.

(2) The LM3710 does not respond to these commands and no operation is performed as in (1).

(3) If the data equivalent to the chip select code is applied to the DB12 to 15 beforehand, the memory data is outputted. (The DB0 to 9 output the memory data and the DB10 to 15 are fixed at "L" level.)
If other data than the chip select code is applied, the output buffer is set to the high impedance state and no memory data is outputted. (A chip with a different chip select code can be wired-OR connected.) The data outputted at the I/O pins is inputted intact to the address latch, chip select latch at the end of the cycle.

(4) If the data equivalent to the chip select code is applied to the DB12 to 15 beforehand, the memory data is outputted. (The DB0 to 9 output the memory data and the DB10 to 15 are fixed at "L" level.)
If other data than the chip select code is applied, the output buffer is set to the high impedance state and no memory data is outputted. No operation is performed to input the data to the address latch, chip select latch.

(5) The I/O pins are set to input use. The address data for selecting one of the 4k words x 2 pages the chip select data are inputted to the address latch and chip select latch respectively.

Absolute Maximum Ratings at Ta=+25°C, V_{SS}=0V

			unit
Maximum Supply Voltage	$V_{CC}max$	-0.3 to 9.0	V
Input Voltage	V_{IN}	-0.3 to V_{CC}	V
Allowable Power Dissipation	Pdmax	0.75	W
Operating Temperature	Topg	-30 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C

Allowable Operating Ranges at Ta=0 to +70°C, V_{SS}=0V

		min	typ	max	unit
Supply Voltage	V_{CC}	4.5		5.5	V
Input "H" Level Voltage	V_{IH}	2.4		V_{CC}	V
Input "L" Level Voltage	V_{IL}	0		0.7	V

DC Electrical Characteristics at Ta=0°C to +70°C, V_{SS}=0V, V_{CC}=4.5V to 5.5V

			min	typ	max	unit
Input Leakage Current	I_{IN}	V_{IN}=0V to V_{CC}	-5		5	uA
Output "H" Level Voltage	V_{OH}	I_{OH}=80uA	2.4			V
Output "L" Level Voltage	V_{OL}	I_{OL}=1.5mA			0.5	V
Current Dissipation	I_{CC}	DC1=BC2=BDIR=Don't Care Output OPEN			60	mA

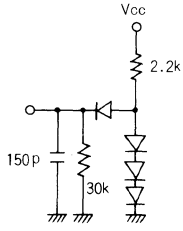
AC Electrical Characteristics at Ta=0°C to +70°C, V_{SS}=0V, V_{CC}=4.5V to 5.5V

		min	typ	max	unit
Control Code Stable Time	t_{CCS}	885			ns
Address setup Time	t_{ASU}	300			ns
Address Hold Time	t_{AH}	60			ns
No Action Time	t_{NACT}	885			ns
Output Data Delay Time	t_{DO}			350	ns
Output Data Hold Time	t_{DH}	80			ns
Floating Delay Time	t_{FL}			300	ns
Control Code Stable Time	t_{SKEW}			50	ns

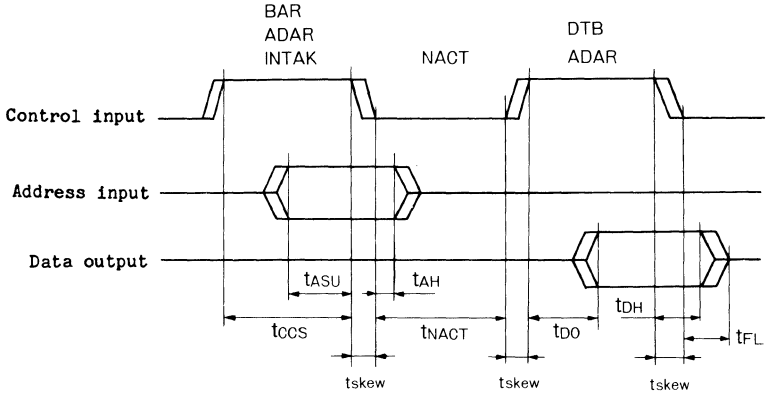
Capacitance at Ta=+25°C, V_{SS}=0V

			min	typ	max	unit
Input Capacitance	C_{IN}	V_{IN}=0V, f=1MHz			10	pF

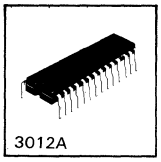
Output Load Circuit at AC Test



Timing Chart



LM3764



N MOS LSI

8192 Words by 8-Bits Mask Programmable ROM

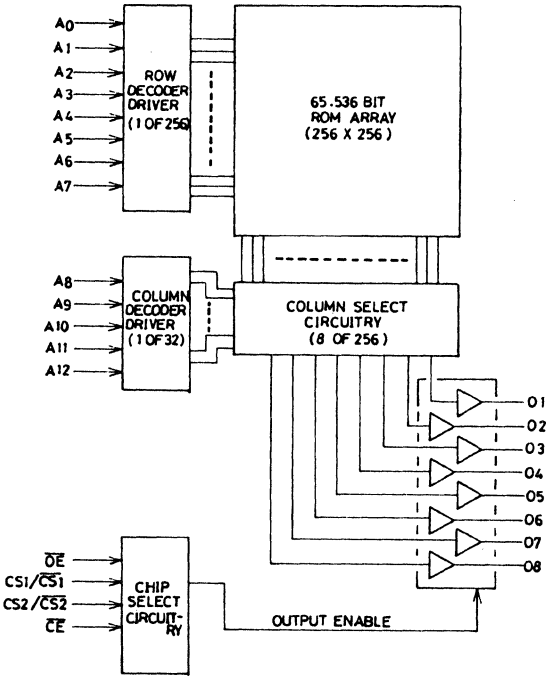
Ⓔ 1556

TENTATIVE

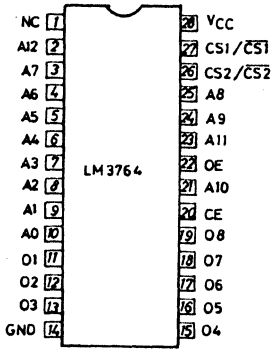
Features

- Pin compatible with 2764 EPROM
- Organized as 8192 words x 8 bits
- Single 5V supply : 5V±10%
- Three-state output: Wired-OR capability
- Programmable chip select: CS1/CS1, CS2/CS2
- Static operation
- TTL compatible: All inputs and outputs
- Access time: 250ns/350ns/450ns (max)
- Power-down mode available

Block Diagram

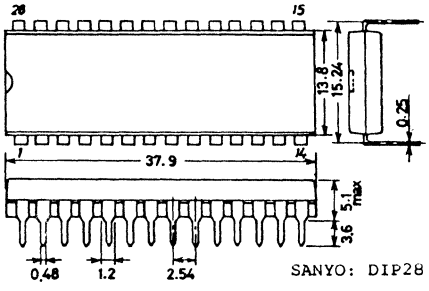


Pin Assignment



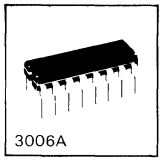
Case Outline 3012A-D28IC

(unit:mm)



SANYO: DIP28

LM8942



P MOS IC

Universal Use MOS Inverter

Ⓔ 442A

The LM8942 is a general-purpose IC suited for designing various interfaces.

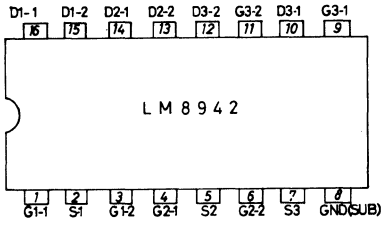
Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Input Voltage	V_{IN}	Apply voltage across one of pins (1),(3),(4),(6),(9),(11) and GND.	-20 to +0.3	V
Maximum Output Voltage	V_{OUT}	Apply Voltage across one of pins (2),(5),(7),(10),(12),(13),(14),(15),(16) and GND.	-20 to +0.3	V
Operating Temperature	Topg		-20 to +80	°C
Storage Temperature	Tstg		-40 to +125	°C

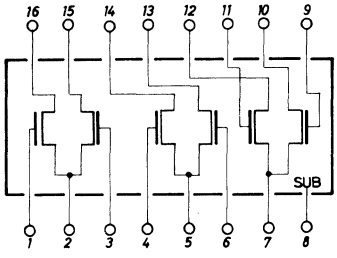
Electrical Characteristics at Ta=25°C

			min	typ	max	unit
High-Level Input Voltage	V_{IH}		-1.0			V
Low-Level Input Voltage	V_{IL}		-20		-6.0	V
High-Level Outupt Voltage	V_{OH}	V_{IH}=-6.0V, I_{DRAIN}=1mA	-1.0			V
Output Off Leak Current	I_{OL}	V_{DRAIN}=-10V			10	uA
Input Resistance	r_i	V_{IN}=-10V	1M			ohm
Input Capacitance	c_i	f=1MHz			30	pF
Output Capacitance	c_o	f=1MHz			30	pF

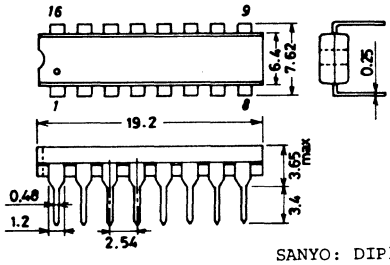
Pin Assignment



Equivalent Circuit



Case Outline 3006A-D16IC
(unit:mm)



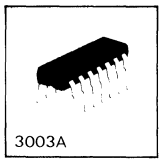
SANYO: DIP16

CMOS STANDARD LOGICS

- **Pin Numbering**

When you face the top side (marking side) of the package, numbering starts with ① assigned to the pin located, in a counterclockwise direction, immediately after the index point and turns counterclockwise.

LC4001B



C MOS IC

CMOS Logic B-Series Quad 2-Input NOR Gate

Ⓔ 858B

The LC4001B is a 2-input NOR logic IC ——— B series ——— having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

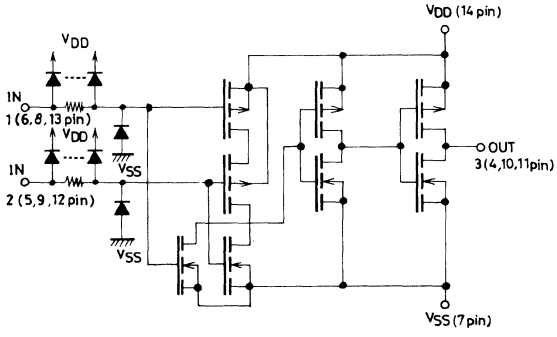
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	$P_d max$		300	mW
Lead Temeperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

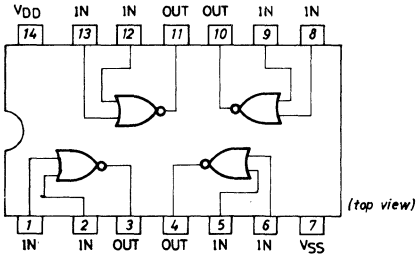
Allowable Operating Range at T_a=-40 to +85°C

Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

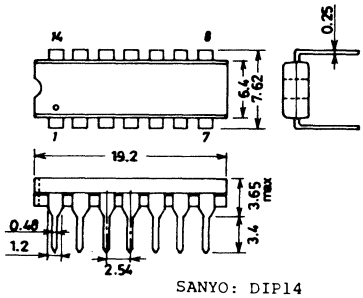
Equivalent Circuit



Pin Assignment



Case Outline 3003A-D 14IC (unit:mm)



SANYO: DIP14

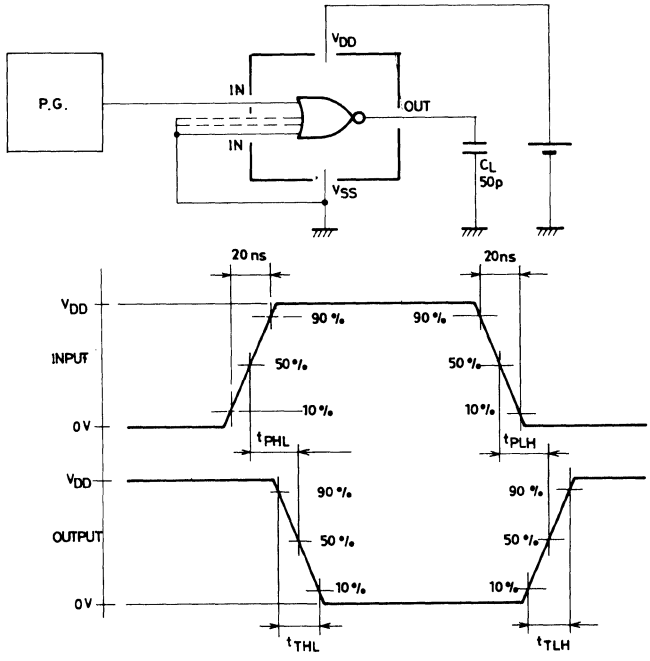
Electrical Characteristics at T_a=25±2°C, V_{SS}=0			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	-0.5	-1.0		mA
		V_{DD}=10V, V_o=9.5V, "	-1.0	-2.0		mA
		V_{DD}=15V, V_o=13.5V, "	-3.5	-7.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5	1.0		mA
		V_{DD}=10V, V_o=0.5V, "	1.0	2.0		mA
		V_{DD}=15V, V_o=1.5V, "	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1uA	3.5	2.5		V
		V_{DD}=10V, V_o=1.0V, "	7.0	5.0		V
		V_{DD}=15V, V_o=1.5V, "	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_{OUT}\|$<1uA		2.5	1.5	V
		V_{DD}=10V, V_o=1.0Vor9.0V "		5.0	3.0	V
		V_{DD}=15V, V_o=1.5Vor13.5V "		7.5	4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V		10^{-5}	1.0	uA
		V_{DD}=18V, V_{IN}=0V		-10^{5}	-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.01	1.0	uA
		V_{DD}=10V, "		0.01	2.0	uA
		V_{DD}=15V, "		0.01	4.0	uA
Input Stray Capacitance	C_{IN}	Total input		5	7.5	pF

Electrical Characteristics at T_a=-40 to +85°C, V_{SS}=0			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	-0.5			mA
		V_{DD}=10V, V_o=9.5V, "	-1.0			mA
		V_{DD}=15V, V_o=13.5V, "	-3.5			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5			mA
		V_{DD}=10V, V_o=0.5V, "	1.0			mA
		V_{DD}=15V, V_o=1.5V, "	3.5			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V, V_o=1.0V, "	7.0			V
		V_{DD}=15V, V_o=1.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, V_o=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V, V_o=1.5Vor13.5V, "			4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V			1.0	uA
		V_{DD}=18V, V_{IN}=0V			-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			7.5	uA
		V_{DD}=10V, "			15.0	uA
		V_{DD}=15V, "			30.0	uA

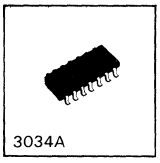
Note) Current direction ;+,no sign:Flowing into SSI, -:Flowing out of SSI.

Switching Characteristics at T_a=25±2°C, C_L=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Rise Time	t_{TLH}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching time test circuit and waveform



LC4001BM



C MOS IC

CMOS Logic B-Series Quad 2-Input NOR Gate

Ⓔ 1120A

Use

- C MOS standard logic IC for logic circuit.

Features, functions

* 2-input NOR logic gate IC (equivalent to B series, 4 2-input NOR gates contained in a single package) having wide operating voltage range, high noise margin, low power dissipation.
* Mini flat package enabling compactness of sets.

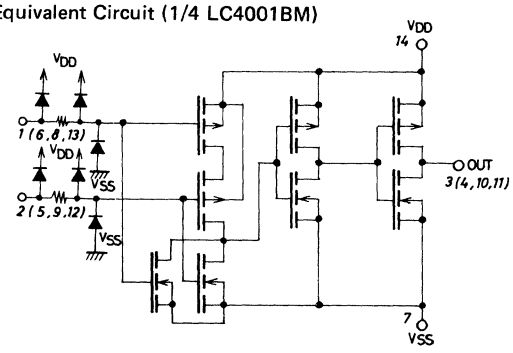
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum supply voltage	V_{DD} max		V_{SS} −0.5~V_{SS} +20	V
Input voltage	V_{IN}		V_{SS} −0.5~V_{DD}+0.5	V
Output voltage	V_{OUT}		V_{SS} −0.5~V_{DD} +0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	T_aH85°C	150	mW
Operating temperature	T_{opg}		−40~+85	°C
Storage temperature	T_{stg}		−65~+150	°C
Lead temperature. time	T_{sol}	t=10sec	260	°C

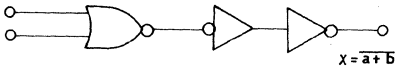
Allowable Operating Ranges/T_a=−40°C to +85°C

			unit
Supply voltage	V_{DD}	3~18	V
Input voltage	V_{IN}	0~V_{DD}	V

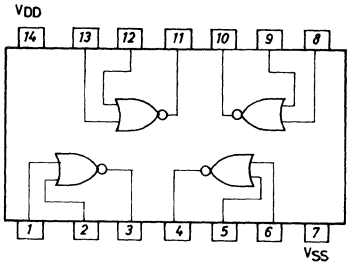
Equivalent Circuit (1/4 LC4001BM)



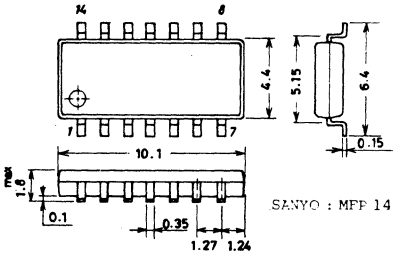
Circuit Configuration



Pin Assignment

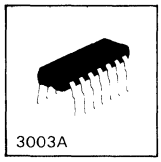


Case Outline 3034A-M14IC
(unit:mm)



For details, refer to the description of the LC4001B.

LC4011B



C MOS IC

CMOS Logic B-Series Quad 2-Input NAND Gate

Ⓔ 827D

The LC4011B is a 2-input NAND logic IC ——— B series ——— having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

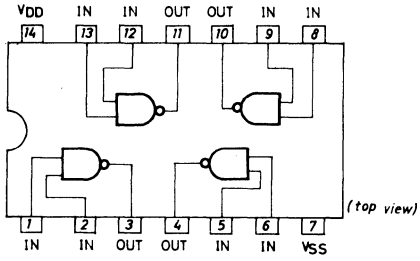
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	$P_d max$		300	mW
Lead Temperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

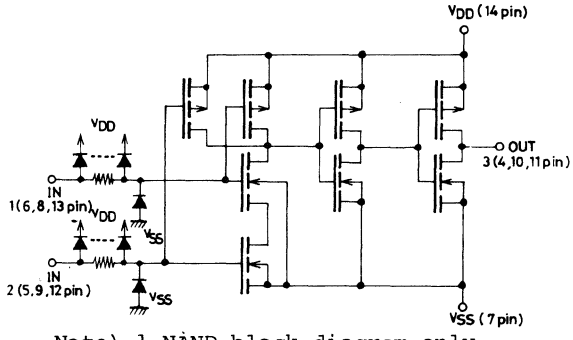
Allowable Operating Range at T_a=-40 to +85°C

Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Pin Assignment

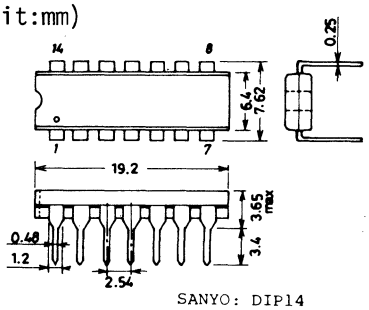


Equivalent Circuit



Note) 1 NAND block diagram only.

Case Outline 3003A-D14IC (unit:mm)



SANYO: DIP14

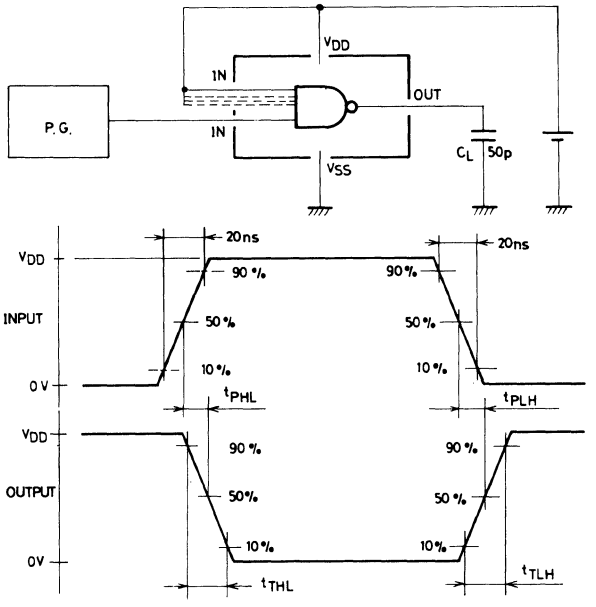
Electrical Characteristics at T_a=25±2°C, V_{SS}=0			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5	-1.0		mA
		V_{DD}=10V, V_o=9.5V, "	-1.0	-2.0		mA
		V_{DD}=15V, V_o=13.5V "	-3.5	-7.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.5	1.0		mA
		V_{DD}=10V, V_o=0.5V, "	1.0	2.0		mA
		V_{DD}=15V, V_o=1.5V, "	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_o\|$<1uA	3.5	2.5		V
		V_{DD}=10V, V_o=1Vor9V, "	7.0	5.0		V
		V_{DD}=15V, V_o=1.5Vor13.5V, "	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_o\|$<1uA		2.5	1.5	V
		V_{DD}=10V, V_o=1Vor9V, "		5.0	3.0	V
		V_{DD}=15V, V_o=1.5Vor13.5V, "		7.5	4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18VorV$_{IN}$=0		$\pm 10^{-5}$	±1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_i=V_{SS}, V_{DD}		0.01		uA
		V_{DD}=10V, "		0.01		uA
		V_{DD}=15V, "		0.01		uA
Input Stray Capacitance	C_{IN}	Total input		5	7.5	pF

Electrical Characteristics at T_a=-40 to +85°C, V_{SS}=0			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, v_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5			mA
		V_{DD}=10V, v_o=9.5V, "	-1.0			mA
		V_{DD}=15V, v_o=13.5V, "	-3.5			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, v_o=0.4V, V_{IN}=V_{DD}	0.5			mA
		V_{DD}=10V, v_o=0.5V, "	1.0			mA
		V_{DD}=15V, v_o=1.5V, "	3.5			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, v_o=0.5Vor4.5V, $\|I_o\|$<1uA	3.5			V
		V_{DD}=10V, v_o=1Vor9V, "	7.0			V
		V_{DD}=15V, v_o=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, v_o=0.5Vor4.5V, $\|I_o\|$<1uA			1.5	V
		V_{DD}=10V, v_o=1Vor9V, "			3.0	V
		V_{DD}=15V, v_o=1.5Vor13.5V, "			4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18VorV$_{IN}$=0			±1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_i=V_{SS}, V_{DD}			7.5	uA
		V_{DD}=10V, "			15	uA
		V_{DD}=15V, "			30	uA
Input Stray Capacitance	C_{IN}	Total input			-	pF

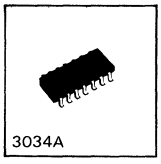
Note) Current direction ; +, no sign:Flowing into SSI, -:Flowing out of SSI.

Switching Characteristics at T_a=25±2°C, CL=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Rise Time	t_{TLH}	V_{DD}=5V		100	200	ns
	(t_r)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching time test circuit and waveform



LC4011BM



C MOS IC

CMOS Logic B-Series Quad 2-Input NAND Gate

Ⓔ 1121A

Use

* C MOS standard logic IC for logic circuit

Features, functions

* 2-input NAND logic gate IC (equivalent to B series) having wide operating voltage range, high noise margin, low power dissipation
* Mini flat package enabling compactness of sets

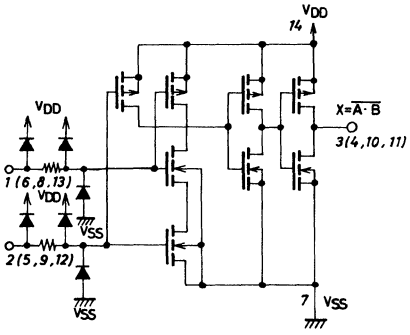
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum supply voltage	V_{DD} max		V_{SS}−0.5~V_{SS}+20	V
Input voltage	V_{IN}		V_{SS}−0.5~V_{DD}+0.5	V
Output voltage	V_{OUT}		V_{SS}−0.5~V_{DD}+0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	$T_a \leq 85°C$	150	mW
Operating temperature	T_{opg}		−40~+85	°C
Storage temperature	T_{stg}		−65~+150	°C
Lead temperature. time	T_{sol}	t=10sec	260	°C

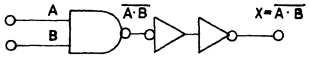
Allowable operating Ranges/T_a=−40°C~+85°C

			unit
Supply voltage	V_{DD}	3~18	V
Input voltage	V_{IN}	0~V_{DD}	V

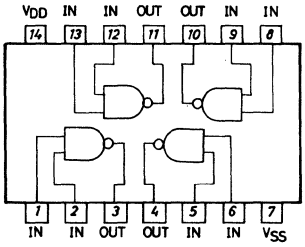
Equivalent Circuit (1/4 LC4011BM)



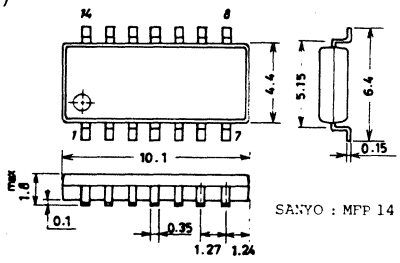
Circuit Configuration



Pin Assignment

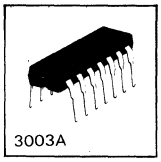


Case Outline 3034A-M14IC
(unit:mm)



For details, refer to the description of the LC4011B.

LC4012B



C MOS IC

CMOS Logic B-Series
Dual 4-Input NAND Gate

Ⓔ 1326A

The LC4012B is a 4-input NAND logic IC ——— B series ——— having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

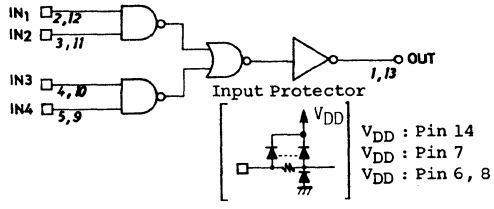
			unit
Maximum Supply Voltage	$V_{DD}max$	-0.5 to +20	V
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Allowable Power Dissipation	$P_d max$	300	mW
Operating Temperature	T_{opg}	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C

Allowable Operating Range at T_a=-40 to +85°C, V_{SS}=0V

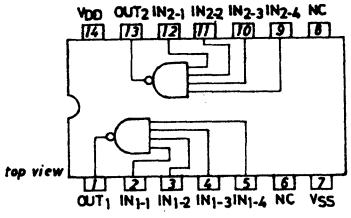
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Equivalent Circuit

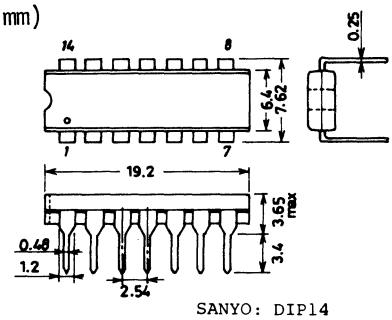
(1/2 LC4012B)



Pin Assignment (tio view)



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

Electrical Characteristics at T_a=25°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10.00		V
		V_{DD}=15V, " "	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}		0.00	0.05	V
		V_{DD}=10V, " "		0.00	0.05	V
		V_{DD}=15V, " "		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.16	-0.5		mA
		V_{DD}=10V, V_o=9.5V, "	-0.4	-1.2		mA
		V_{DD}=15V, V_o=13.5V "	-1.2	-6.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.44	1.5		mA
		V_{DD}=10V, V_o=0.5V, "	1.1	3.5		mA
		V_{DD}=15V, V_o=1.5V, "	3.0	15		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_o\|$<1uA	3.5	2.75		V
		V_{DD}=10V, V_o=1Vor9V, "	7.0	5.5		V
		V_{DD}=15V, V_o=1.5Vor13.5V, "	11.0	8.25		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1uA		2.25	1.5	V
		V_{DD}=10V, V_o=9.0V, "		4.5	3.0	V
		V_{DD}=15V, V_o=13.5V, "		6.75	4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V		10^{-5}	0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V		-10^{-5}	-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_i=V_{SS}, V_{DD}		0.01	1.0	uA
		V_{DD}=10V, "		0.01	2.0	uA
		V_{DD}=15V, "		0.02	4.0	uA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at T_a=-40°C			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, v_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.2			mA
		V_{DD}=10V, v_o=9.5V, "	-0.5			mA
		V_{DD}=15V, v_o=13.5V, "	-1.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, v_o=0.4V, V_{IN}=V_{DD}	0.52			mA
		V_{DD}=10V, v_o=0.5V, "	1.3			mA
		V_{DD}=15V, v_o=1.5V, "	3.6			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, v_o=0.5Vor4.5V, $\|I_o\|$<1uA	3.5			V
		V_{DD}=10V, v_o=1Vor9V, "	7.0			V
		V_{DD}=15V, v_o=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, V_o=9.0V, "			3.0	V
		V_{DD}=15V, V_o=13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V			-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_i=V_{SS}, V_{DD}			1.0	uA
		V_{DD}=10V, "			2.0	uA
		V_{DD}=15V, "			4.0	uA

Electrical Characteristics at T_a=+85°C, V_{SS}=0V

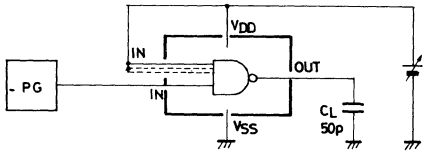
			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.12			mA
		V_{DD}=10V, V_o=9.5V, "	-0.3			mA
		V_{DD}=15V, V_o=13.5V "	-1.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.36			mA
		V_{DD}=10V, V_o=0.5V, "	0.9			mA
		V_{DD}=15V, V_o=1.5V, "	2.4			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_o\|$<1uA	3.5			V
		V_{DD}=10V, V_o=1Vor9V, "	7.0			V
		V_{DD}=15V, V_o=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, V_o=9.0V, "			3.0	V
		V_{DD}=15V, V_o=13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			1.0	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V			-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_i=V_{SS}, V_{DD}			7.5	uA
		V_{DD}=10V, "			15	uA
		V_{DD}=15V, "			30	uA

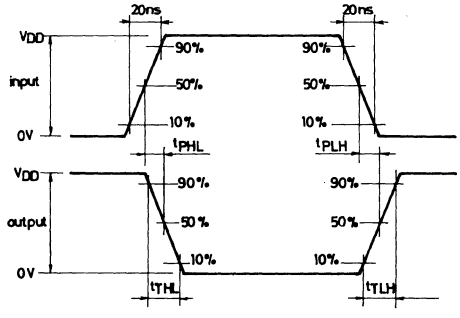
Note) Current direction ; +, no sign:Flowing into SSI, -:Flowing out of SSI.

Switching Characteristics at T_a=25±2°C, C_L=50pF, V_{SS}=0V

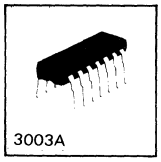
			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		200	400	ns
		V_{DD}=10V		100	200	ns
		V_{DD}=15V		80	160	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		180	350	ns
		V_{DD}=10V		90	175	ns
		V_{DD}=15V		70	125	ns
Rise Time	t_{TLH}	V_{DD}=5V		130	400	ns
	(t_r)	V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching time test circuit and waveform





LC4013B



C MOS IC

CMOS Logic B-Series Dual D-Type Flip-Flop

Ⓔ 876B

The LC4013B is an IC that consists of two independent D-type flip-flops (EIA/JEDEC standards-met IC product) having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	$P_d$max	T_a=85°C	300	mW
Lead Temperature and Time	Tsol	t=10sec	260	°C
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

Allowable Operating Range at Conditions at T_a=25°C, V_{SS}=0V

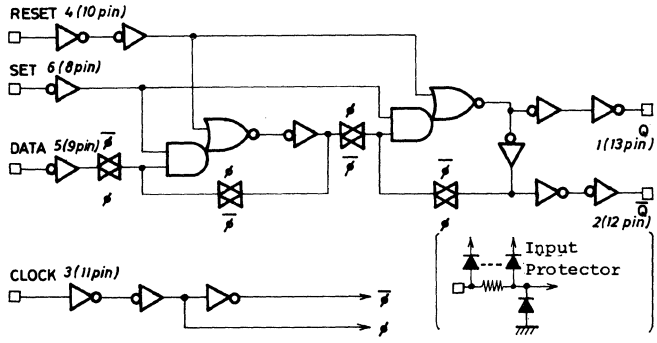
			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=-40°C to +85°C	3		18	V
Input Voltage	V_{IN}	"	0		V_{DD}	V

Truth Table

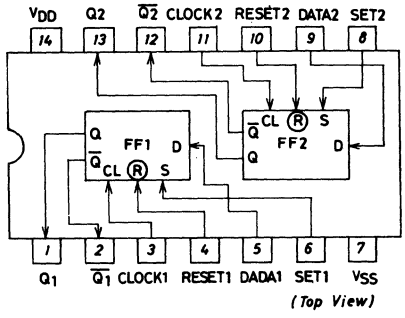
INPUTS				OUTPUTS	
CL△	D	S	Ⓡ	Q_{n+1}	$\overline{Q_{n+1}}$
*	÷	H	L	H	L
*	*	L	H	L	H
*	*	H	H	L	H
↗	L	L	L	L	H
↗	H	L	L	H	L
↘	*	L	L	Q_n•	$\overline{Q_n}$•

* : Dont Care
△ : Level Change
• : No Change

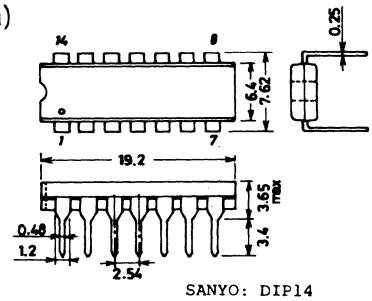
Logic Diagram (1/2 LC4013B)



Pin Assignment and Block Diagram



Case Outline 3003A-D14IC (unit:mm)



SANYO: DIP14

			min	typ	max	unit
Data Setup Time	$t_{set\ up}$	V_{DD}=5V	160			ns
		V_{DD}=10V	80			ns
		V_{DD}=15V	40			ns
Clock Frequency	f_{clk}	V_{DD}=5V	DC		1.0	MHz
		V_{DD}=10V	DC		2.0	MHz
		V_{DD}=15V	DC		3.0	MHz
Clock Rise/Fall Time	t_r clk,	V_{DD}=5V			20	us
	t_f clk	V_{DD}=10V			2.5	us
		V_{DD}=15V			1.0	us
Set/Reset Pulse Width	t_W S,R	V_{DD}=5V	300			ns
		V_{DD}=10V	200			ns
		V_{DD}=15V	160			ns

Electrical Characteristics at T_a=-40°C,V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V,$\|I_{OUT}\|$<1uA,V_{IN}=V_{SS},V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V,$\|I_{OUT}\|$<1uA,V_{IN}=V_{SS},V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V,v_o=4.6V,V_{IN}=V_{SS},V_{DD}	-0.2			mA
		V_{DD}=10V,v_o=9.5V, "	-0.5			mA
		V_{DD}=15V,v_o=13.5V, "	-1.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V,v_o=0.4V,V_{IN}=V_{SS},V_{DD}	0.52			mA
		V_{DD}=10V,v_o=0.5V, "	1.3			mA
		V_{DD}=15V,v_o=1.5V, "	3.6			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V,v_o=0.5Vor4.5V,$\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V,v_o=1.0Vor9.0V "	7.0			V
		V_{DD}=15V,v_o=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V,v_o=0.5Vor4.5V,$\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V,v_o=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V,v_o=1.5Vor13.5V, "			4.0	V
Input Leak Current	I_{IH}	V_{DD}=18V,V_{IH}=18V			0.3	uA
	I_{IL}	V_{DD}=18V,V_{IL}=0V			-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V,V_{IN}=V_{SS},V_{DD}			4.0	uA
		V_{DD}=10V, "			8.0	uA
		V_{DD}=15V, "			16.0	uA

Electrical Characteristics at T_a=25°C±2°C,V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V,$\|I_{OUT}\|$<1uA,V_{IN}=V_{SS},V_{DD}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10 00		V
		V_{DD}=15V, " "	14.95	15 00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V,$\|I_{OUT}\|$<1uA,V_{IN}=V_{DD}		0.00	0.05	V
		V_{DD}=10V, " "		0.00	0.05	V
		V_{DD}=15V, " "		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V,V_o=4.6V,V_{IN}=V_{SS},V_{DD}	-0.16			mA
		V_{DD}=10V,V_o=9.5V, "	-0.4			mA
		V_{DD}=15V,V_o=13.5V "	-1.2			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V,V_o=0.4V,V_{IN}=V_{DD}	0.44			mA
		V_{DD}=10V,V_o=0.5V, "	1.1			mA
		V_{DD}=15V,V_o=1.5V, "	3.0			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V,V_o=0.5Vor4.5V,$\|I_o\|$<1uA	3.5	2.75		V
		V_{DD}=10V,V_o=1Vor9V, "	7.0	5.5		V
		V_{DD}=15V,V_o=1.5Vor13.5V, "	11.0	8.25		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V,V_o=0.5Vor4.5V,$\|I_o\|$<1uA		2.25	1.5	V
		V_{DD}=10V,V_o=1Vor9V, "		4.5	3.0	V
		V_{DD}=15V,V_o=1.5Vor13.5V, "		6.75	4.0	V
Input Leak Current	I_{IH}	V_{DD}=18V,V_{IH}=18V		10^{-5}	0.3	uA
	I_{IL}	V_{DD}=18V,V_{IL}=0V		-10^{-5}	-0.3	uA

			min	typ	max	unit
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.01	4.0	uA
		V_{DD}=10V, "		0.01	8.0	uA
		V_{DD}=15V, "		0.01	16.0	uA

Electrical Characteristics at T_a=±85°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, v_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.12			mA
		V_{DD}=10V, v_o=9.5V, "	-0.3			mA
		V_{DD}=15V, v_o=13.5V, "	-1.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, v_o=0.4V, V_{IN}=V_{DD}	0.36			mA
		V_{DD}=10V, v_o=0.5V, "	0.9			mA
		V_{DD}=15V, v_o=1.5V, "	2.4			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, v_o=0.5Vor4.5V, $\|I_o\|$<1uA	3.5			V
		V_{DD}=10V, v_o=1Vor9V, "	7.0			V
		V_{DD}=15V, v_o=1.5Vor13.5V, "	11.7			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, v_o=0.5Vor4.5V, $\|I_o\|$<1uA			1.5	V
		V_{DD}=10V, v_o=1Vor9V, "			3.0	V
		V_{DD}=15V, v_o=1.5Vor13.5V, "			4.0	V
Input Leak Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			1.0	uA
	I_{IL}	V_{DD}=18V, V_{IL}=0V			-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			30	uA
		V_{DD}=10V, "			60	uA
		V_{DD}=15V, "			120	uA

(Note) Current direction (+, no sign : Flowing into SSI.
(- : Flowing out of SSI.

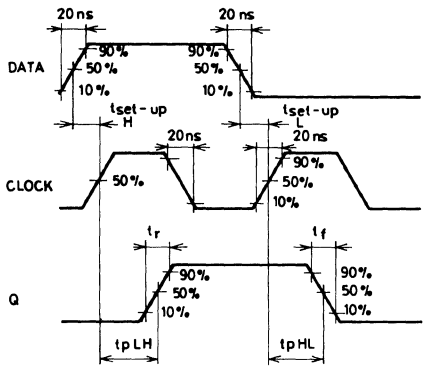
Switching Characteristics at T_a=25°C, V_{SS}=0V, C_L=50pF

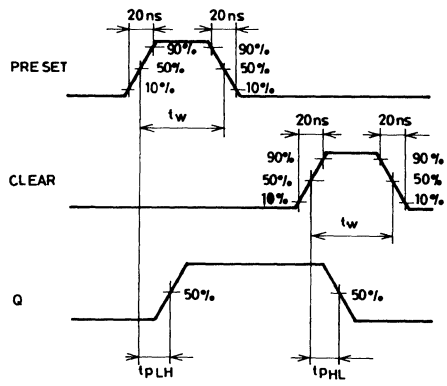
			min	typ	max	unit
Output Rise Time	T_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	T_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Data Setup Time ($t_{set\ up}$ mini)	$t_{set\ up}$	V_{DD}=5V		40	160	ns
		V_{DD}=10V		20	80	ns
		V_{DD}=15V		10	40	ns
Clock Rise/Fall Time	t_r clk	V_{DD}=5V			20	us
	t_f clk	V_{DD}=10V			2.5	us
		V_{DD}=15V			1.0	us
Clock Frequency (f max)	f_{clk}	V_{DD}=5V	1.0	2.0		MHz
		V_{DD}=10V	2.0	4.0		MHz
		V_{DD}=15V	3.0	6.0		
"H" Level Propagation Time (clk → Q, $\overline{Q}$)	t_{PLH}	V_{DD}=5V		350	700	ns
		V_{DD}=10V		150	300	ns
		V_{DD}=15V		100	200	ns
"L" Level Propagation Time (clk → Q, $\overline{Q}$)	t_{PHL}	V_{DD}=5V		300	600	ns
		V_{DD}=10V		150	300	ns
		V_{DD}=15V		100	200	ns
"H" Level Propagation Time (RESET, SET → Q, $\overline{Q}$)	t_{PLH}	V_{DD}=5V		250	500	ns
		V_{DD}=10V		150	300	ns
		V_{DD}=15V		100	200	ns
"L" Level Propagation Time (RESET, SET → Q, $\overline{Q}$)	t_{PHL}	V_{DD}=5V		250	500	ns
		V_{DD}=10V		150	300	ns
		V_{DD}=15V		100	200	ns

		min	typ	max	unit
Reset Pulse Width	t_W R, V_{DD}=5V		150	300	ns
Set Pulse Width	t_W S V_{DD}=10V		100	200	ns
	V_{DD}=15V		80	160	ns

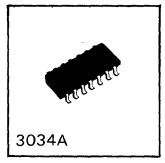
Switching Time Test Waveform

1. fmaxø, t_{PLH}, t_{PHL} (CF-Q,$\overline{Q}$), t_r, t_f, t_rø, t_fø 2. t_W, t_{PLH}, t_{PHL} (CL, FR-Q,$\overline{Q}$)





LC4013BM



C MOS IC

CMOS Logic B-Series Dual D-Type Flip-Flop

Ⓔ 1347A

The LC4013BM is an IC that consists of two independent D-type flip-flops (EIA/JEDEC requirements-met IC product) having such features as wide operating voltage range, high noise margin, low power dissipation, etc. The use of miniflat package permits sets to be small-sized.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		V_{SS}−0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}−0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leq 85°C$	150	mW
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C
Lead Temperature Time	T_{sol}	t=10sec	260	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=−40 to +85°C	3		18	V

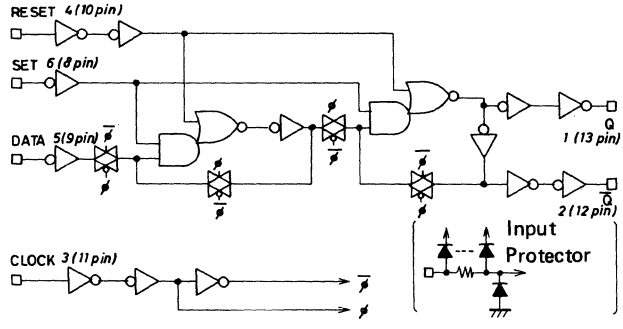
(continued on next page)

Truth Table

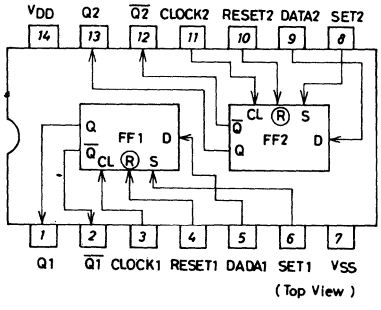
INPUTS				OUTPUTS	
CL Δ	D	S	Ⓡ	Q_{n+1}	$\overline{Q}_{n+1}$
★	★	H	L	H	L
★	★	L	H	L	H
★	★	H	H	L	H
↓	L	L	L	L	H
↓	H	L	L	H	L
↓	★	L	L	Q_n ·	$\overline{Q}_n$ ·

★ : Don't care
Δ : Level Change
● : No Change

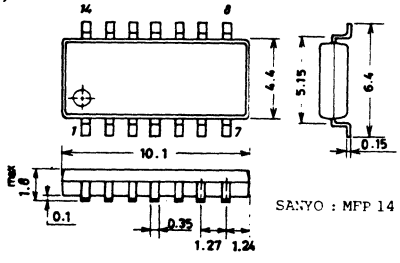
Equivalent Circuit (1/2 LC4013BM)



Pin Assignment and Block Diagram

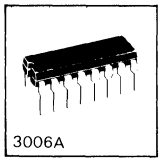


Case Outline 3034A-M14IC
(unit:mm)



For details, refer to the description of the LC4013B.

LC4015B


3006A

C MOS IC

CMOS Logic B-Series
Dual 4-Stage Static Shift Register

Ⓔ 1006B

The LC4015B is a dual 4-stage static shift register having such features as wide operating voltage range, high noise margin, low power dissipation. Each output is independent. It is possible to clear all outputs by applying asynchronous reset input externally at any time. (Equivalent to B series)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

			unit
Maximum Supply Voltage	V_{DD} max	-0.5 to +20	V
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Allowable Power Dissipation	P_d max Ta≦85°C	300	mW
Operating Temperature	Topg	-40 to +85	°C
Storage Temperature	Tstg	-65 to +150	°C

Allowable Operating Ranges at Ta=-40 to +85°C, V_{SS}=0V

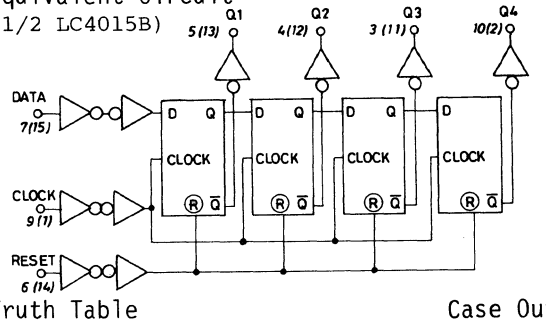
			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Electrical Characteristics at Ta=-40°C, V_{SS}=0V

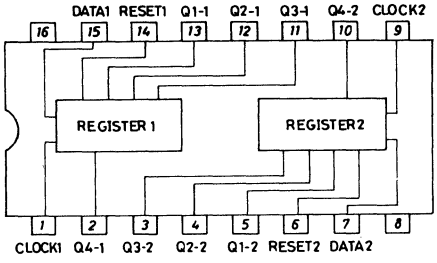
			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}, V_{SS}	4.95			V
		V_{DD}=10V, "	9.95			V
		V_{DD}=15V, "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}, V_{SS}			0.05	V
		V_{DD}=10V, "			0.05	V
		V_{DD}=15V, "			0.05	V

(continued on the next page)

Equivalent Circuit
(1/2 LC4015B)



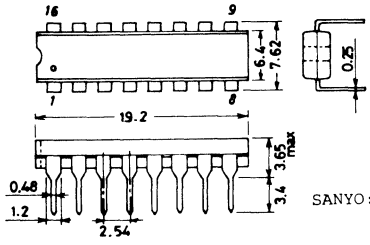
Pin Assignment



Truth Table

Input			Output			
D	R	clock	Q_1	Q_2	Q_3	Q_4
0	0	↑	0	Q_1	Q_2	Q_3
1	0	↑	1	Q_1	Q_2	Q_3
※	0	↑	nO change			
※	1	※	0	0	0	0

Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

			min	typ	max	unit
"Hi" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}, V_{SS}	-0.2			mA
		V_{DD}=10V, V_O=9.5V, "	-0.5			mA
		V_{DD}=15V, V_O=13.5V, "	-1.4			mA
"Lo" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}, V_{SS}	0.52			mA
		V_{DD}=10V, V_O=0.5V, "	1.3			mA
		V_{DD}=15V, V_O=1.5V, "	3.6			mA
"Hi" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|$<luA	3.5			V
		V_{DD}=10V, V_O=1.0or9.0V, "	5.0			V
		V_{DD}=15V, V_O=1.5Vorl3.5V, "	11.0			V
"Lo" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|$<luA			1.5	V
		V_{DD}=10V, V_O=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V, V_O=1.5Vorl3.5V, "			4.0	V
"Hi" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			0.3	uA
"Lo" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V			-0.3	uA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			20	uA
		V_{DD}=10V, "			40	uA
		V_{DD}=15V, "			80	uA

Electrical Characteristics at Ta=25±2°C, V_{SS}=0V

			min	typ	max	unit
"Hi" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<luA, V_{IN}=V_{DD}, V_{SS}	4.95	5.00		V
		V_{DD}=10V, "	9.95	10.00		V
		V_{DD}=15V, "	14.95	15.00		V
"Lo" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<luA, V_{IN}=V_{DD}, V_{SS}		0.00	0.05	V
		V_{DD}=10V, "		0.00	0.05	V
		V_{DD}=15V, "		0.00	0.05	V
"Hi" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}, V_{SS}	-0.16	-0.36		mA
		V_{DD}=10V, V_O=9.5V, "	-0.4	-0.9		mA
		V_{DD}=15V, V_O=13.5V, "	-1.2	-3.5		mA
"Lo" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}, V_{SS}	0.44	0.88		mA
		V_{DD}=10V, V_O=0.5V, "	1.1	2.25		mA
		V_{DD}=15V, V_O=1.5V, "	3.0	8.8		mA
"Hi" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|$<luA	3.5	2.27		V
		V_{DD}=10V, V_O=1.0Vor9.0V, "	7.0	5.5		V
		V_{DD}=15V, V_O=1.5Vorl3.5V, "	11.0	8.25		V
"Lo" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|$<luA		2.25	1.5	V
		V_{DD}=10V, V_O=1.0Vor9.0V, "		4.5	3.0	V
		V_{DD}=15V, V_O=1.5Vorl3.5V, "		6.75	4.0	V
"Hi" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V		10^{-5}	0.3	uA
"Lo" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V		-10^{-5}	-0.3	uA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.005	20	uA
		V_{DD}=10V, "		0.010	40	uA
		V_{DD}=15V, "		0.015	80	uA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at Ta=+85°C, V_{SS}=0V

			min	typ	max	unit
"Hi" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<luA, V_{IN}=V_{DD}, V_{SS}	4.95			V
		V_{DD}=10V, "	9.95			V
		V_{DD}=15V, "	14.95			V
"Lo" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<luA, V_{IN}=V_{DD}, V_{SS}			0.05	V
		V_{DD}=10V, "			0.05	V
		V_{DD}=15V, "			0.05	V

(continued on the next page)

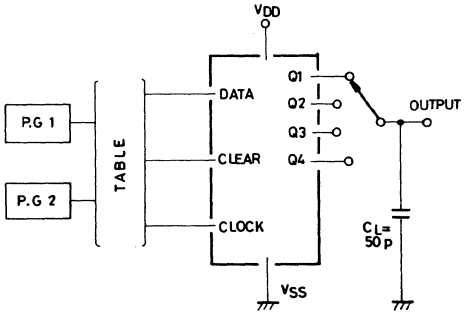
			min	typ	max	unit
"Hi" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}, V_{SS}	-0.12			mA
		V_{DD}=10V, V_O=9.5V, "	-0.3			mA
		V_{DD}=15V, V_O=13.5V, "	-1.0			mA
"Lo" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}, V_{SS}	0.36			mA
		V_{DD}=10V, V_O=0.5V "	0.9			mA
		V_{DD}=15V, V_O=1.5V, "	2.4			mA
"Hi" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|<1uA$	3.5			V
		V_{DD}=10V, V_O=1.0Vor9.0 "	7.0			V
		V_{DD}=15V, V_O=1.5Vor13.5V, "	11.0			V
"Lo" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|<1uA$			1.5	V
		V_{DD}=10V, V_O=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V, V_O=1.5Vor13.5V, "			4.0	V
"Hi" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			1.0	uA
"Hi" Level Input Current	I_{IL}	V_{DD}=18V, V_{IH}=0V			-1.0	uA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			150	uA
		V_{DD}=10V, "			300	uA
		V_{DD}=15V, V_{IN}=V_{SS}, V_{DD}			600	uA

(Note) Current direction { + (no sign): Flowing into device
- : Flowing out of device

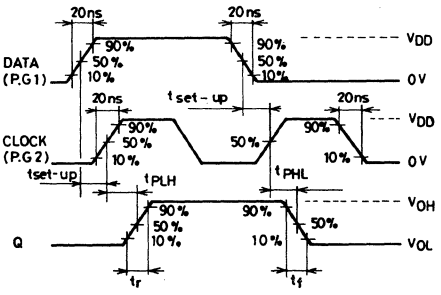
Switching Characteristics at Ta=25±2°C, V_{SS}=0V, C_L=50pF			min	typ	max	unit
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"Hi" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V clock-Q, Waveform 1		280	600	ns
		V_{DD}=10V "		130	300	ns
		V_{DD}=15V "		110	250	ns
"Lo" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V clock-Q, Waveform 1		240	600	ns
		V_{DD}=10V "		115	300	ns
		V_{DD}=15V "		90	250	ns
"	"	V_{DD}=5V Reset→Q, Waveform 2		350	700	ns
		V_{DD}=10V "		150	300	ns
		V_{DD}=15V "		120	200	ns
Maximum Clock Frequency	f_{max}	V_{DD}=5V Waveform 1	1.0	2.5		MHz
		V_{DD}=10V "	2.5	7.0		MHz
		V_{DD}=15V "	3.0	8.0		MHz
Minimum Clock Pulse Width	$t_{w(\phi)}$	V_{DD}=5V Waveform 1		185	500	ns
		V_{DD}=10V "		85	200	ns
		V_{DD}=15V "		55	150	ns
Maximum Clock Rise, Fall Time	$t_{r(\phi)}$	V_{DD}=5V Waveform 1			20	us
	$t_{f(\phi)}$	V_{DD}=10V "			2.5	us
		V_{DD}=15V "			1.0	us
Minimum Reset Pulse Width	$t_{w(R)}$	V_{DD}=5V Waveform 2		150	300	ns
		V_{DD}=10V "		75	150	ns
		V_{DD}=15V "		60	130	ns
Minimum Data Set-up Time	t_S	V_{DD}=5V Waveform 1		150	300	ns
		V_{DD}=10V "		100	200	ns
		V_{DD}=15V "		60	150	ns

Switching Time Test Circuit and Waveform

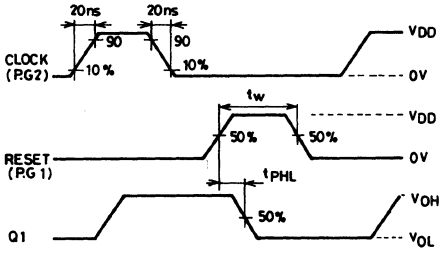
Test Circuit



Waveform 1



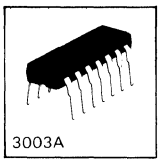
Waveform 2



TABLE

TABLE No.	MEASURE MODE	DATE	Reset	clock
1	t_{set-up} t_{PLH}, t_{PHL}	P.G.1	GND	P.G.2
2	t_w, t_{PHL} (CLEAR)	VDD	P.G.1	P.G.2

LC4016B



C MOS IC

CMOS Logic B-Series Quad Bilateral Switch

Ⓔ 1024B

The LC4016B is a bilateral switch (also called analog switch) IC (meeting EIA/JEDEC standards) having such features as wide operating voltage range, high noise margin, low power dissipation, etc. It has 4 independent bilateral switches. Setting control input (CONT) at "H" level causes the switches to be conducting, thereby resulting in a low impedance between input and output; and setting control input (CONT) at "L" level causes the switches to be nonconducting, thereby resulting in a high impedance between input and output.

On Resistance (R on)	500Ω (typ): V_{DD}=10V
	250Ω (typ): V_{DD}=15V
Off Resistance (Roff)	R off (typ) $>10^9\Omega$

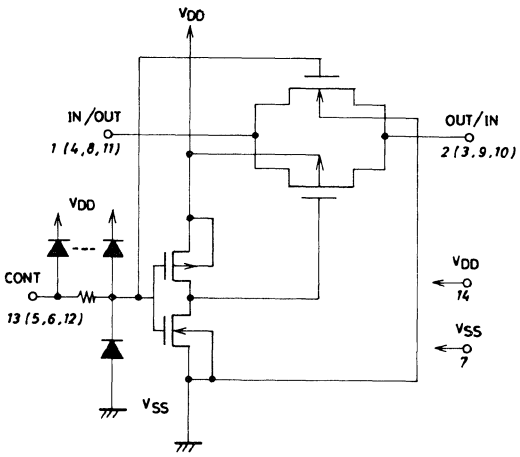
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.5 to +20	V
Input Voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leqq 85°C$	300	mW
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C
Lead Temperature. Time	T_{sol}	t=10sec	260	°C

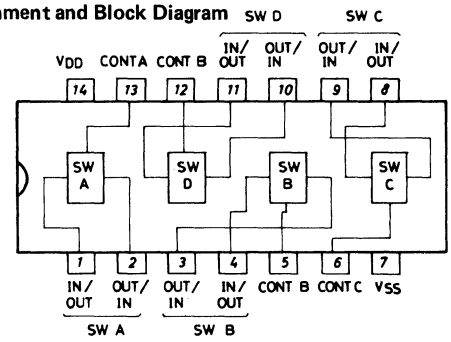
Allowable Operating Ranges/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

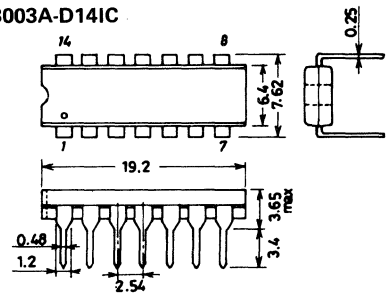
Equivalent Circuit (1/4 LC4016B)



Pin Assignment and Block Diagram



Case Outline 3003A-D14IC (unit: mm)



SANYO: DIP14

Electrical Characteristics/T_a=−40°C, V_{SS}=0V			min	typ	max	unit
Input "H" Level Control Voltage	V_{IH}	V_{DD}=5V, Current between input and output=10μA	3.5			V
		V_{DD}=10V, 〃	7.0			V
		V_{DD}=15V, 〃	11.0			V
Input "L" Level Control Voltage	V_{IL}	V_{DD}=5V, Current between input and output=10μA			1.0	V
		V_{DD}=10V, 〃			1.0	V
		V_{DD}=15V, 〃			1.0	V
On Resistance	R_{ON}	V_{DD}=10V, V_{IN}=10V			600	Ω
		V_{DD}=10V, V_{IN}=5V			1300	Ω
		V_{DD}=10V, V_{IN}=0.25V			600	Ω
		V_{DD}=15V, V_{IN}=15V			430	Ω
		V_{DD}=15V, V_{IN}=7.5V			800	Ω
		V_{DD}=15V, V_{IN}=0.25			430	Ω
		V_{DD}=5V, V_{SS}=−5V, V_{IN}=5V			600	Ω
		V_{DD}=5V, V_{SS}=−5V, V_{IN}=±0.25V			1300	Ω
		V_{DD}=5V, V_{SS}=−5V, V_{IN}=−5V			600	Ω
		V_{DD}=7.5V, V_{SS}=−7.5V, V_{IN}=7.5V			430	Ω
		V_{DD}=7.5V, V_{SS}=−7.5V, V_{IN}=±0.25			800	Ω
		V_{DD}=7.5V, V_{SS}=−7.5V, V_{IN}=−7.5V			430	Ω
Input/Output Leak Current (Switch off)	I_{OFF}	V_{DD}=18V, V_{IN}=18V, V_{OUT}=0V			±250	nA
		V_{DD}=18V, V_{IN}=0V, V_{OUT}=18V			±250	nA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{CIN}=V_{DD}, V_{SS}			1.0	μA
		V_{DD}=10V, 〃			2.0	μA
		V_{DD}=15V, 〃			4.0	μA
Control Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			0.3	μA
	I_{IL}	V_{DD}=18V, V_{IN}=0V			−0.3	μA

Electrical Characteristics/T_a=25°C±2°C, V_{SS}=0V			min	typ	max	unit
Input "H" Level Control Voltage	V_{IH}	V_{DD}=5V, Current between input and output=10μA	3.5	2.4		V
		V_{DD}=10V, 〃	7.0	4.8		V
		V_{DD}=15V, 〃	11.0	7.2		V
Input "L" Level Control Voltage	V_{IL}	V_{DD}=5V, Current between input and output=10μA		1.7	1.0	V
		V_{DD}=10V, 〃		1.7	1.0	V
		V_{DD}=15V, 〃		1.7	1.0	V
On Reistance	R_{ON}	V_{DD}=5V, V_{IN}=5V		600		Ω
		V_{DD}=5V, V_{IN}=2.5V		6000		Ω
		V_{DD}=5V, V_{IN}=0.25V		600		Ω
		V_{DD}=10V, V_{IN}=10V		250	700	Ω
		V_{DD}=10V, V_{IN}=5V		600	1500	Ω
		V_{DD}=10V, V_{IN}=0.25V		250	700	Ω
		V_{DD}=15V, V_{IN}=15V		200	500	Ω
		V_{DD}=15V, V_{IN}=7.5V		300	950	Ω
		V_{DD}=15V, V_{IN}=0.25V		200	500	Ω
		V_{DD}=5V, V_{SS}=−5V, V_{IN}=5V		250	700	Ω
		V_{DD}=5V, V_{SS}=−5V, V_{IN}=±0.25		600	1500	Ω
		V_{DD}=5V, V_{SS}=−5V, V_{IN}=−5V		250	700	Ω
		V_{DD}=7.5V, V_{SS}=−7.5V, V_{IN}=7.5V		200	500	Ω
		V_{DD}=7.5V, V_{SS}=−7.5V, V_{IN}=±0.25V		300	950	Ω
		V_{DD}=7.5V, V_{SS}=−7.5V, V_{IN}=−7.5V		200	500	Ω
ΔON Resistance (between Any 2 Switches)	ΔR_{ON}	V_{DD}=5V, V_{SS}=−5V		15		Ω
		V_{DD}=7.5V, V_{SS}=−7.5V		10		Ω

(continued on next page)

			min	typ	max	unit
Input/Output Leak Current (Switch off)	I_{OFF}	$V_{DD}=10V, V_{IN}=10V, V_{OUT}=0V$		±0.01	±125	nA
		$V_{DD}=10V, V_{IN}=0V, V_{OUT}=10V$		±0.01	±125	nA
		$V_{DD}=18V, V_{IN}=18V, V_{OUT}=0V$		±0.1	±250	nA
		$V_{DD}=18V, V_{IN}=0V, V_{OUT}=18V$		±0.1	±250	nA
Quiescent Current Dissipation	I_{DD}	$V_{DD}=5V, V_{CIN}=V_{DD}, V_{SS}$		0.001	1.0	μA
		$V_{DD}=10V$, 〃		0.001	2.0	μA
		$V_{DD}=15V$, 〃		0.001	4.0	μA
Control Input Current	I_{IH}	$V_{DD}=18V, V_{IN}=18V$		10^{-5}	0.3	μA
	I_{IL}	$V_{DD}=18V, V_{IL}=0V$		-10^{-5}	−0.3	μA

Electrical Characteristics/T_a=+85°C, V_{SS}=0V

			min	typ	max	unit
Input "H" Level Control Voltage	V_{IH}	$V_{DD}=5V$, Current between input and output=10μA	3.5			V
		$V_{DD}=10V$, 〃	7.0			V
		$V_{DD}=15V$, 〃	11.0			V
Input "L" Level Control Voltage	V_{IL}	$V_{DD}=5V$, Current between input and output=10μA			1.0	V
		$V_{DD}=10V$, 〃			1.0	V
		$V_{DD}=15V$, 〃			1.0	V
On Reistance	R_{ON}	$V_{DD}=10V, V_{IN}=10V$			900	Ω
		$V_{DD}=10V, V_{IN}=5V$			2000	Ω
		$V_{DD}=10V, V_{IN}=0.25V$			900	Ω
		$V_{DD}=15V, V_{IN}=15V$			650	Ω
		$V_{DD}=15V, V_{IN}=7.5V$			1200	Ω
		$V_{DD}=15V, V_{IN}=0.25V$			650	Ω
		$V_{DD}=5V, V_{SS}=-5V, V_{IN}=5V$			900	Ω
		$V_{DD}=5V, V_{SS}=-5V, V_{IN}=\pm0.25V$			2000	Ω
		$V_{DD}=5V, V_{SS}=-5V, V_{IN}=-5V$			900	Ω
		$V_{DD}=7.5V, V_{SS}=-7.5V, V_{IN}=7.5V$			650	Ω
		$V_{DD}=7.5V, V_{SS}=-7.5V, V_{IN}=\pm0.25V$			1200	Ω
		$V_{DD}=7.5V, V_{SS}=-7.5V, V_{IN}=-7.5V$			650	Ω
Input/Output Leak Current (Switch off)	I_{OFF}	$V_{DD}=18V, V_{IN}=18V, V_{OUT}=0V$			±1000	nA
		$V_{DD}=18V, V_{IN}=0V, V_{OUT}=18V$			±1000	nA
Quiescent Current Dissipation	I_{DD}	$V_{DD}=5V, V_{CIN}=V_{DD}, V_{SS}$			7.5	μA
		$V_{DD}=10V$, 〃			15	μA
		$V_{DD}=15V$, 〃			30	μA
Control Input Current	I_{IH}	$V_{DD}=18V, V_{IN}=18V$			1.0	μA
	I_{IL}	$V_{DD}=18V, V_{IL}=0V$			−1.0	μA

Current Direction + (no sign): Flowing into device
− : Flowing out of device

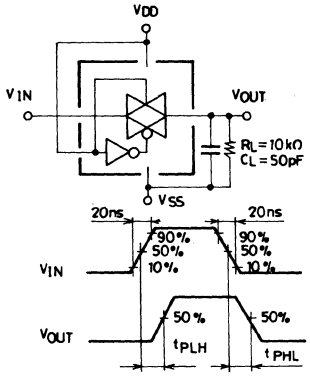
Switching Characteristics/T_a=25±2°C,

			min	typ	max	unit
Propagation Delay Time (INPUT-OUTPUT)	t_{PLH} t_{PHL}	V_{DD}=5V, R_L=10kΩ, C_L=50pF		50	100	ns
		V_{DD}=10V, 〃 〃		20	40	ns
		V_{DD}=15V, 〃 〃		16	30	ns
Propagation Time (Control-OUTPUT)	t_{PLH} t_{PHL}	V_{DD}=5V, R_L=10kΩ, C_L=50pF		100	140	ns
		V_{DD}=10V, 〃 〃		40	60	ns
		V_{DD}=15V, 〃 〃		35	50	ns
Maximum Control Input Frequency	f max(C)	V_{DD}=5V, C_L=15pF		4.0		MHz
		V_{DD}=10V, 〃		10.0		MHz
		V_{DD}=15V, 〃		12.0		MHz
Maximum Input/Output Propagation Frequency	f max(I/O)	V_{DD}=5V, V_{SS}=−5V, R_L=2kΩ, C_L=15pF ※1		8.5		MHz
		V_{DD}=5V, V_{SS}=−5V, R_L=10kΩ, 〃		7.5		MHz
		V_{DD}=5V, V_{SS}=−5V, R_L=100kΩ, 〃		5.0		MHz
Sine Wave Propagation Distortion Ratio		V_{DD}=5V, V_{DD}=−5V, R_L=10kΩ, f=1MHz ※2		0.3		%
Feed Through (Switch off)		V_{DD}=5V, V_{SS}=−5V, R_L=1kΩ ※3		600		KHz
Input Capacitance	C_{IN}	Control input		5		pF
		Switch I/O		4		pF

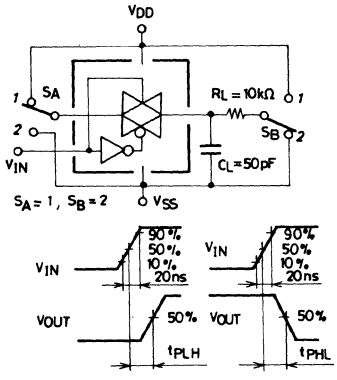
※1 Vis: ±2.5Vp-p sine wave f max (I/O): 20 log (Vos/Vis)=−3dB
※2 Vis: ±2.5Vp-p sine wave
※3 Vis: ±2.5Vp-p sine wave $f_{FEED\ THROUGH}$:20 log (Vos/Vis)=−50dB

Electrical Characteristics Test Circuits and Waveforms

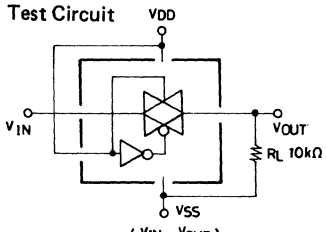
1. t_{PLH}, t_{PHL} (IN-OUT) Test Circuit



2. t_{PLH}, t_{PHL} (CONTROL-OUT) Test Circuit

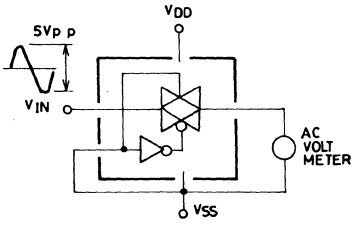


3. R_{ON} Test Circuit

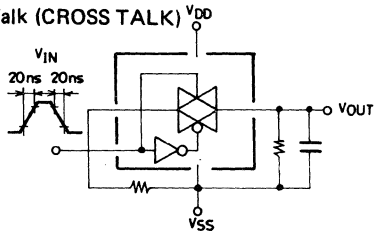


$$R_{ON} = 10 \times \frac{(V_{IN} - V_{OUT})}{V_{OUT}} \ (k\Omega)$$

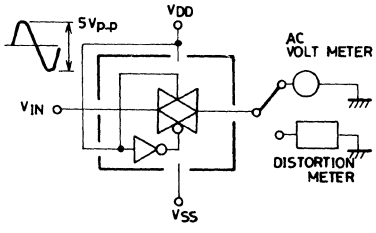
4. Feed Through (FEED THROUGH) Test Circuit



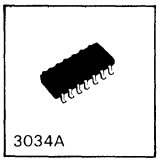
5. Cross Talk (CROSS TALK)



6. Frequency Response (f max) Distortion



LC4016BM



C MOS IC

CMOS Logic B-Series Quad Bilateral Switch

Ⓔ 1157B

The LC4016BM is a bilateral switch (also called analog switch) IC (meeting EIA/JEDEC standards) having such features as wide operating voltage range, high noise margin, low power dissipation, etc. It has 4 independent bilateral switches. Setting control input (CONT) at "H" level causes the switches to be conducting, thereby resulting in a low impedance between input and output; and setting control input (CONT) at "L" level causes the switches to be nonconducting, thereby resulting in a high impedance between input and output. Its mini flat package enables compactness of sets.

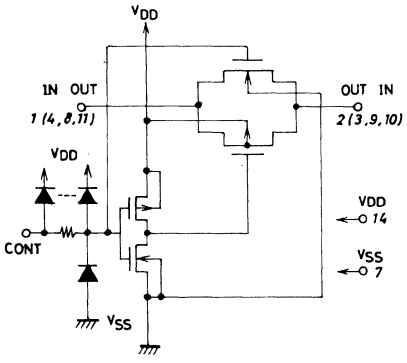
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum supply voltage	V_{DD} max		−0.5~+20	V
Input voltage	V_{IN}		−0.5~V_{DD}+0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	$T_a \leq 85°C$	150	mW
Operating temperature	T_{opg}		−40~+85	°C
Storage temperature	T_{stg}		−65~+150	°C

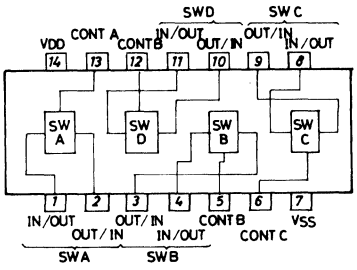
Allowable Operation condition/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply voltage	V_{DD}	3~18	V
Input voltage	V_{IN}	0~V_{DD}	V

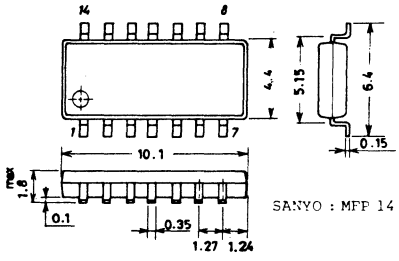
Equivalent Circuit (1/4 LC4016BM)



Pin Assignment and Block Diagram

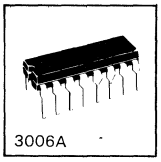


Case Outline 3034A-M14IC
(unit:mm)



For details, refer to the description of to the LC4016B.

LC4019B



C MOS IC

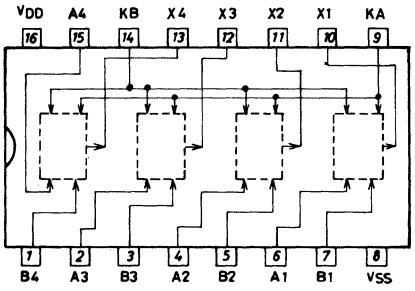
CMOS Logic B-Series Quad AND-OR Select Gate

Ⓔ 973B

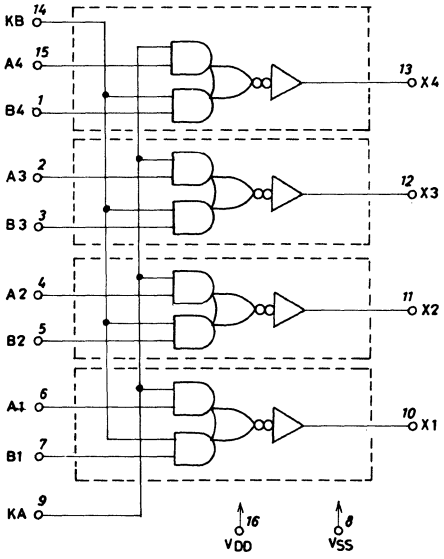
Features and Functions

- Wide operating voltage range, high noise immunity, low power dissipation
- 4 AND-OR SELECT Gates (each consists of two 2-input AND gates driving a single 2-input OR gate.)
- Input signals of A_n, B_n (n=1 to 4) are selected by select inputs K_A, K_B common to 4 circuits and are outputted to D_n (n=1 to 4).
- Suited for use in 4-bit 2-channel data selectors, multiplexers

Pin Assignment (Top View)



Equivalent Circuit

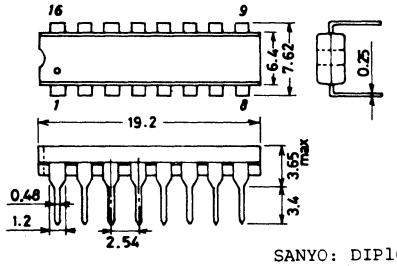


Truth Table

An	Bn	K_A	K_B	Xn
0	0	1	0	0
1	0	1	0	1
0	1	1	0	0
1	1	1	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	1
1	1	0	1	1
0	0	1	1	0
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1
※	※	0	0	0

1 : 「H」
0 : 「L」
※ : dont care
n : 1～4

Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Absolute Maximum Ratings/T_a=25°C±2°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}		$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}		$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leqq 85$°C	300	mW
Operating Temperature	T_{opg}		−40～+85	°C
Storage Temperature	T_{stg}		−65～+150	°C
Lead Temperature · Time	T_{sol}	t=10 sec	260	°C

Recommended Operating Conditions/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3～18	V
Input Voltage	V_{IN}	0～V_{DD}	V

Electrical Characteristics/T_a=−40°C, V_{SS}=0V

			min	typ	max	unit
Output "H" Level Voltage	V_{OH}	V_{DD}=5V, $\lvert I_{OUT}\rvert$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
Output "L" Level Voltage	V_{OL}	V_{DD}=5V, $\lvert I_{OUT}\rvert$<1μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
Output "H" Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.5			mA
		V_{DD}=10V, V_o=9.5V, 〃	−1.0			mA
		V_{DD}=15V, V_o=13.5V, 〃	−3.5			mA
Output "L" Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5			mA
		V_{DD}=10V, V_o=0.5V, 〃	1.0			mA
		V_{DD}=15V, V_o=1.5V, 〃	3.5			mA
Input "H" Level Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V or 4.5V, $\lvert I_{OUT}\rvert$<1μA	3.5			V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃	7.0			V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃	11.0			V
Input "L" Level Voltage	V_{IL}	V_{DD}=5V, V_o=0.5V or 4.5V, $\lvert I_{OUT}\rvert$<1μA			1.5	V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃			3.0	V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃			4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V			1.0	μA
		V_{DD}=18V, V_{IN}=0V (V_{SS})			−1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			1.0	μA
		V_{DD}=10V, 〃			2.0	μA
		V_{DD}=15V, 〃			4.0	μA

Electrical Characteristics/T_a=25°C±2°C, V_{SS}=0V

			min	typ	max	unit
Output "H" Level Voltage	V_{OH}	V_{DD}=5V, $\lvert I_{OUT}\rvert$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, 〃 〃	9.95	10.00		V
		V_{DD}=15V, 〃 〃	14.95	15.00		V
Output "L" Level Voltage	V_{OL}	V_{DD}=5V, $\lvert I_{OUT}\rvert$<1μA, V_{IN}=V_{SS}, V_{DD}		0.00	0.05	V
		V_{DD}=10V, 〃 〃		0.00	0.05	V
		V_{DD}=15V, 〃 〃		0.00	0.05	V
Output "H" Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.5	−1.0		mA
		V_{DD}=10V, V_o=9.5V, 〃	−1.0	−2.0		mA
		V_{DD}=15V, V_o=13.5V, 〃	−3.5	−7.0		mA
Output "L" Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5	1.0		mA
		V_{DD}=10V, V_o=0.5V, 〃	1.0	2.0		mA
		V_{DD}=15V, V_o=1.5V, 〃	3.5	7.0		mA

(continued on next page)

			min	typ	max	unit
Input "H" Level Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V or4.5V, $\|I_{OUT}\|$<1 μA	3.5	2.5		V
		V_{DD}=10V, V_O=1.0V or 9.0V, 〃	7.0	5.0		V
		V_{DD}=15V, V_O=1.5V or 13.5V, 〃	11.0	7.5		V
Input "L" Level Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA		2.5	1.5	V
		V_{DD}=10V, V_O=1.0V or 9.0V, 〃		5.0	3.0	V
		V_{DD}=15V, V_O=1.5V or 13.5V, 〃		7.5	4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V		10^{-5}	1.0	μA
		V_{DD}=18V, V_{IN}=0V (V_{SS})		-10^{-5}	−1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.01	1.0	μA
		V_{DD}=10V, 〃		0.01	2.0	μA
		V_{DD}=15V, 〃		0.01	4.0	μA
Input Stray Capacitance	C_{IN}	Pins A_n, B_n		5	7.5	pF
		Pins K_A, K_B		12	20	pF

Electrical Characteristics/T_a=+85°C, V_{SS}=0V

			min	typ	max	unit
Output "L" Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	13.95			V
Output "L" Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
Output "H" Level Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.4			mA
		V_{DD}=10V, V_O=9.5V, 〃	−0.8			mA
		V_{DD}=15V, V_O=13.5V, 〃	−2.8			mA
Output "L" Level Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}	0.4			mA
		V_{DD}=10V, V_O=0.5V, 〃	0.8			mA
		V_{DD}=15V, V_O=1.5V, 〃	2.8			mA
Input "H" Level Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA	3.5			V
		V_{DD}=10V, V_O=1.0V or 9.0V, 〃	7.0			V
		V_{DD}=15V, V_O=1.5V or 13.5V, 〃	11.0			V
Input "L" Level Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA			1.5	V
		V_{DD}=10V, V_O=1.0V or 9.0V, 〃			3.0	V
		V_{DD}=15V, V_O=1.5V or 13.5V, 〃			4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V			1.0	μA
		V_{DD}=18V, V_{IN}=0V (V_{SS})			−1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			7.5	μA
		V_{DD}=10V, 〃			15.0	μA
		V_{DD}=15V, 〃			30.0	μA

Current direction: + (no sign) Flowing into device,
− Flowing out of device

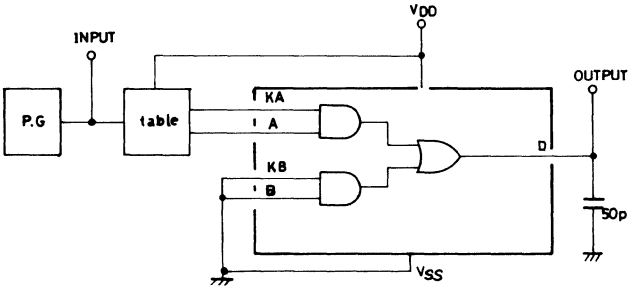
Switching Characteristics/T_a=25°C±2°C, V_{SS}=0V, C_L=50pF

				min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	A,B→D	V_{DD}=5V		150	400	ns
			V_{DD}=10V		60	120	ns
			V_{DD}=15V		50	100	ns
	t_{PLH}	K_a,K_b→D	V_{DD}=5V		150	300	ns
			V_{DD}=10V		60	120	ns
			V_{DD}=15V		50	100	ns
"L" Level Propagation Delay Time	t_{PHL}	A,B→D	V_{DD}=5V		150	300	ns
			V_{DD}=10V		60	120	ns
			V_{DD}=15V		50	100	ns

(continued on next page)

				min	typ	max	unit
	t_{PHL}	$K_a, K_b \rightarrow D$	$V_{DD}=5V$		150	300	ns
			$V_{DD}=10V$		60	120	ns
			$V_{DD}=15V$		50	100	ns
Rise Time	t_{TLH}	$A, B \rightarrow D$	$V_{DD}=5V$		100	200	ns
			$V_{DD}=10V$		50	100	ns
			$V_{DD}=15V$		40	80	ns
	t_{TLH}	$K_a, K_b \rightarrow D$	$V_{DD}=5V$		100	200	ns
			$V_{DD}=10V$		50	100	ns
			$V_{DD}=15V$		40	80	ns
Fall Time	t_{THL}	$A, B \rightarrow D$	$V_{DD}=5V$		100	200	ns
			$V_{DD}=10V$		50	100	ns
			$V_{DD}=15V$		40	80	ns
	t_{THL}	$K_a, K_b \rightarrow 0$	$V_{DD}=5V$		100	200	ns
			$V_{DD}=10V$		50	100	ns
			$V_{DD}=15V$		40	80	ns

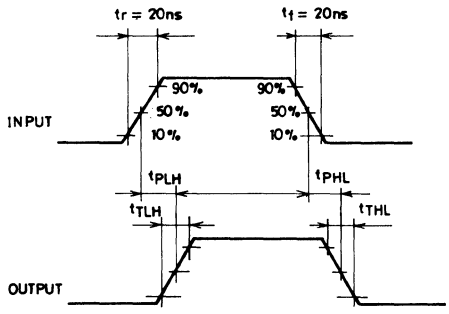
Switching Time Test Circuit and Waveform



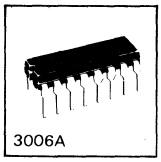
Test Conditions (table)

Test No.	K_a	A
1	P. G.	V_{DD}
2	V_{DD}	P. G.

P. G. : f=500kHz
t_r, t_f=20ns
Duty cycle



LC4020B



C MOS IC

CMOS Logic B-Series 14-Stage Binary Counter

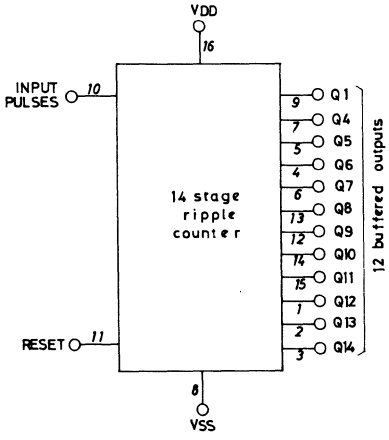
Ⓔ 1494A

The LC4020B is an asynchronous reset function-provided 14-stage ripple-carry binary counter (equivalent to B series) having such features as wide operating voltage range, high noise margin, and low power dissipation. The state of a counter advances one count on the negative transition of each clock input. "Hi" level of reset input resets all counters regardless of clock input, setting all outputs (Q1, Q4 to Q14) to "Lo" level.
Application areas include frequency dividers, control counters, and timing circuits.

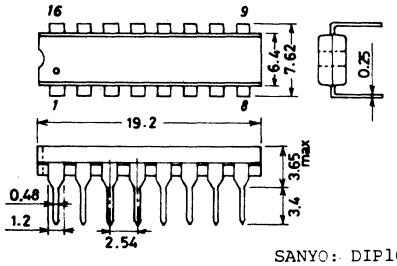
Allowable Operating Ranges at Ta=25°C				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20.0	V
Maximum Input Voltage	$V_{IN}max$		V_{SS}-0.5 to V_{DD}+0.5	V
Maximum Output Voltage	$V_{OUT}max$		V_{SS}-0.5 to V_{DD}+0.5	V
Maximum Input Current	$I_{IN}max$		±10	mA
Allowable Power Dissipation	Pdmax		300	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C
	Tsol	t=10sec	260	°C

Allowable Operating Ranges at Ta=-40 to +85°C			unit
Supply Voltage	V_{DD}	3.0 to 18.0	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Pin Assignment

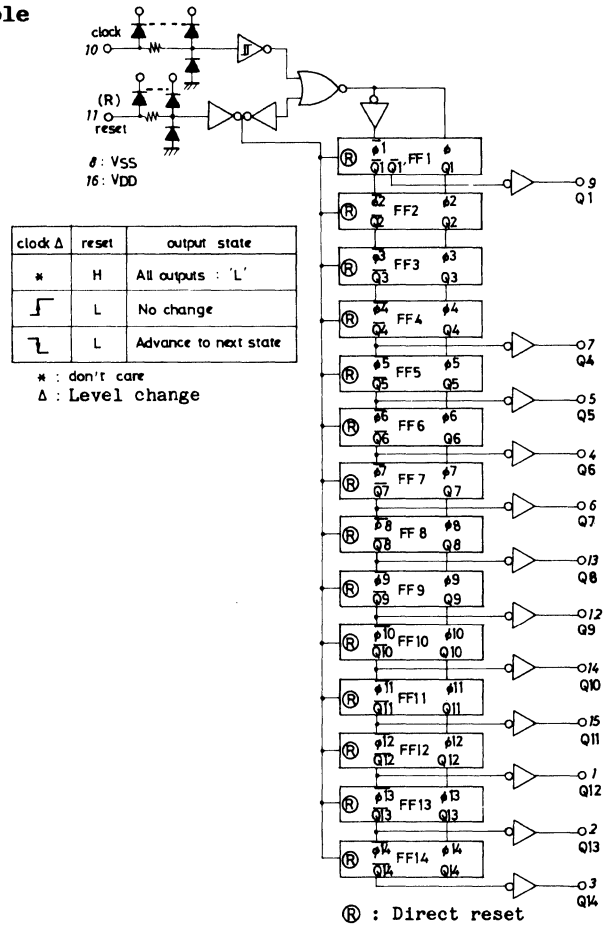


Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Equivalent Circuit and Truth Table



clock Δ	reset	output state
*	H	All outputs : 'L'
↑	L	No change
↓	L	Advance to next state

* : don't care
Δ : Level change

Electrical Characteristics at Ta=25°C, V_{SS}=0V Vo:[], V_{DD}:()

				min	typ	max	unit
Output"H"Level Voltage	V_{OH}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}, V_{DD}$,	(5V)	4.95	5.00		V
		"	(10V)	9.95	10.00		V
		"	(15V)	14.95	15.00		V
Output"L"Level Voltage	V_{OL}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}, V_{DD}$,	(5V)		0.00	0.05	V
		"	(10V)		0.00	0.05	V
		"	(15V)		0.00	0.05	V
Output"H"Level Current	I_{OH}	$V_{IN}=V_{SS}, V_{DD}$, [4.6V]	(5V)	-0.16	-0.5		mA
		" [9.5V]	(10V)	-0.4	-1.2		mA
		" [13.5V]	(15V)	-1.2	-6.0		mA
Output"L"Level Current	I_{OL}	$V_{IN}=V_{SS}, V_{DD}$, [0.4V]	(5V)	0.44	1.5		mA
		" [0.5V]	(10V)	1.1	3.5		mA
		" [1.5V]	(15V)	3.0	15.0		mA
Input"H"Level Voltage	V_{IH}	$\|I_{OUT}\|$ <1uA, [0.5,4.5V]	(5V)	3.5	2.75		V
		[1.0,9.0V]	(10V)	7.0	5.5		V
		[1.5,13.5V]	(15V)	11.0	8.25		V
Input"L"Level Voltage	V_{IL}	$\|I_{OUT}\|$ <1uA, [0.5,4.5V]	(5V)		2.25	1.5	V
		[1.0,9.0V]	(10V)		4.5	3.0	V
		[1.5,13.5V]	(15V)		6.75	4.0	V
Input"H"level Current	I_{IH}	V_{IH}=18V,	(18V)		10^{-5}	0.3	uA
Input"L"Level Current	I_{IL}	V_{IL}=0V,	(18V)		-10^{-5}	-0.3	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$,	(5V)		0.005	20	uA
Disipation		"	(10V)		0.010	40	uA
		"	(15V)		0.015	80	uA
Input Capacitance	C_{IN}				5.0	7.5	pF

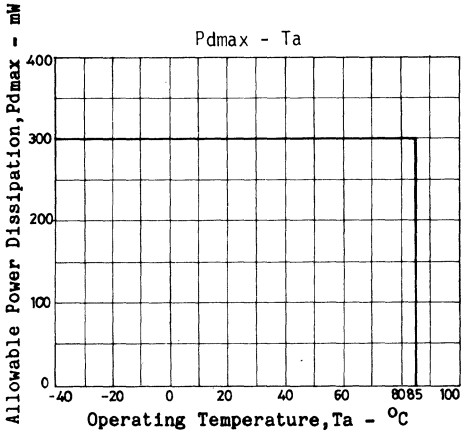
Electrical Characteristics at $Ta=-40^{o}C, V_{SS}=0V$ Vo:[], V_{DD}:()				min	typ	max	unit
Output"H"Level Voltage	V_{OH}	$\lvert I_{OUT}\rvert<1uA, V_{IN}=V_{SS}, V_{DD}$,	(5V)	4.95			V
		"	(10V)	9.95			V
		"	(15V)	14.95			V
Output"L"Level Voltage	V_{OL}	$\lvert I_{OUT}\rvert<1uA, V_{IN}=V_{SS}, V_{DD}$,	(5V)			0.05	V
		"	(10V)			0.05	V
		"	(15V)			0.05	V
Output"H"Level Current	I_{OH}	$V_{IN}=V_{SS}, V_{DD}$,	[4.6V](5V)	-0.2			mA
		"	[9.5V](10V)	-0.5			mA
		"	[13.5V](15V)	-1.4			mA
Output"L"Level Current	I_{OL}	$V_{IN}=V_{SS}, V_{DD}$,	[0.4V](5V)	0.52			mA
		"	[0.5V](10V)	1.3			mA
		"	[1.5V](15V)	3.6			mA
Input"H"Level Voltage	V_{IH}	$\lvert I_{OUT}\rvert$ <1uA,	[0.5,4.5V](5V)	3.5			V
			[1.0,9.0V](10V)	7.0			V
			[1.5,13.5V](15V)	11.0			V
Input"L"Level Voltage	V_{IL}	$\lvert I_{OUT}\rvert$ <1uA,	[0.5,4.5V](5V)			1.5	V
			[1.0,9.0V](10V)			3.0	V
			[1.5,13.5V](15V)			4.0	V
Input"H"level Current	I_{IH}	$V_{IH}=18V$,	(18V)			0.3	uA
Input"L"Level Current	I_{IL}	$V_{IL}=0V$,	(18V)			-0.3	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$,	(5V)			20	uA
Disipation		"	(10V)			40	uA
		"	(15V)			80	uA

Electrical Characteristics at $Ta=85^{o}C, V_{SS}=0V$ Vo:[], V_{DD}:()				min	typ	max	unit
Output"H"Level Voltage	V_{OH}	$\lvert I_{OUT}\rvert<1uA, V_{IN}=V_{SS}, V_{DD}$,	(5V)	4.95			V
		"	(10V)	9.95			V
		"	(15V)	14.95			V
Output"L"Level Voltage	V_{OL}	$\lvert I_{OUT}\rvert<1uA, V_{IN}=V_{SS}, V_{DD}$,	(5V)			0.05	V
		"	(10V)			0.05	V
		"	(15V)			0.05	V
Output"H"Level Current	I_{OH}	$V_{IN}=V_{SS}, V_{DD}$,	[4.6V](5V)	-0.12			mA
		"	[9.5V](10V)	-0.3			mA
		"	[13.5V](15V)	-1.0			mA
Output"L"Level Current	I_{OL}	$V_{IN}=V_{SS}, V_{DD}$,	[0.4V](5V)	0.36			mA
		"	[0.5V](10V)	0.9			mA
		"	[1.5V](15V)	2.4			mA
Input"H"Level Voltage	V_{IH}	$\lvert I_{OUT}\rvert$ <1uA,	[0.5,4.5V](5V)	3.5			V
			[1.0,9.0V](10V)	7.0			V
			[1.5,13.5V](15V)	11.0			V
Input"L"Level Voltage	V_{IL}	$\lvert I_{OUT}\rvert$ <1uA,	[0.5,4.5V](5V)			1.5	V
			[1.0,9.0V](10V)			3.0	V
			[1.5,13.5V](15V)			4.0	V
Input"H"level Current	I_{IH}	$V_{IH}=18V$,	(18V)			1.0	uA
Input"L"Level Current	I_{IL}	$V_{IL}=0V$,	(18V)			-1.0	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$,	(5V)			150	uA
Disipation		"	(10V)			300	uA
		"	(15V)			600	uA

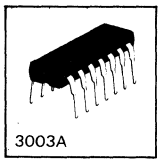
Note) Current Direction : +, no sign: Flowing into device
- : Flowing out of device

Switching Characteristics at Ta=25±2°C, V_{SS}=0V, C_L=50pF

		V_{DD}	min	typ	max	unit
Output Rise Time	t_r (t_{TLH})	5V		130	400	ns
		10V		65	200	ns
		15V		50	160	ns
Output Fall Time	t_f (t_{THL})	5V		100	200	ns
		10V		50	100	ns
		15V		40	80	ns
"H" Level Propagation Delay Time (clock-Q1)	t_{PLH}	5V		600	1000	ns
		10V		220	400	ns
		15V		180	320	ns
"L" Level Propagation Delay Time (clock-Q1)	t_{PHL}	5V		500	900	ns
		10V		170	350	ns
		15V		130	250	ns
"H" Level Propagation Delay Time (clock-Q14)	t_{PLH}	5V		4.5	8.0	us
		10V		1.5	3.0	us
		15V		1.2	2.5	us
"L" Level Propagation Delay Time (clock-Q14)	t_{PHL}	5V		4.5	8.0	us
		10V		1.5	3.0	us
		15V		1.2	2.5	us
"L" Level Propagation Delay Time (reset-Q)	t_{PHL}	5V		640	1900	ns
		10V		200	600	ns
		15V		160	500	ns
Maximum Clock Frequency	$f_{max\phi}$	5V	1.0	1.5		MHz
		10V	2.0	4.5		MHz
		15V	2.5	5.5		MHz
Minimum Reset Pulse Width	t_{wreset}	5V		160	800	ns
		10V		60	300	ns
		15V		50	250	ns
Maximum Clock Rise/ Fall Time	$t_{r\phi}, t_{f\phi}$	5V			2.0	us
		10V			2.5	us
		15V			1.0	us



LC4023B



C MOS IC

CMOS Logic B-Series Triple 3-Input NAND Gate

Ⓔ 1385A

The LC4023B is a triple 3-input NAND Gate (B series) having such features as wide operating voltage range, high noise margin, low power dissipation.

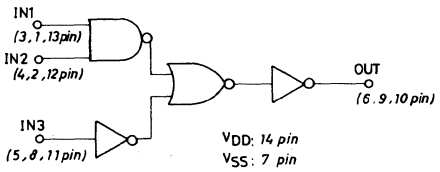
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD} max		-0.5 to +20	V
Input Voltage	V_{IN}		-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax	Ta≦85°C	300	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

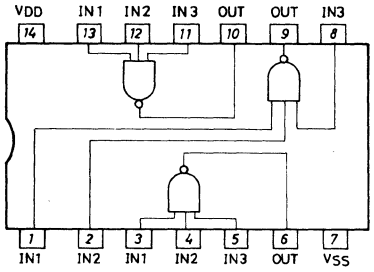
Allowable Operating Range at Ta=-40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

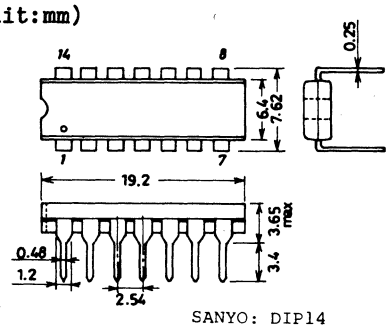
Equivalent Circuit
1/3·LC4023B



Pin Assignment (top view)



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

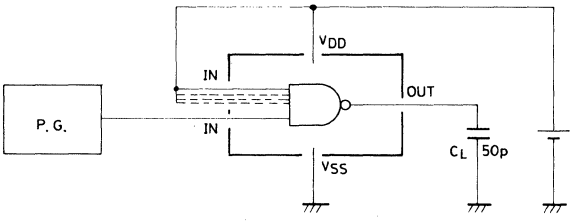
Electrical Characteristics at Ta=25±2°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5	-1.0		mA
		V_{DD}=10V, Vo=9.5V, "	-1.0	-2.0		mA
		V_{DD}=15V, Vo=13.5V, "	-3.5	-7.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, V_{IN}=V_{DD}	0.5	1.0		mA
		V_{DD}=10V, Vo=0.5V, "	1.0	2.0		mA
		V_{DD}=15V, Vo=1.5V, "	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|Io\|$<1uA	3.5	2.5		V
		V_{DD}=10V, Vo=1Vor9V, "	7.0	5.0		V
		V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|Io\|$<1uA		2.5	1.5	V
		V_{DD}=10V, Vo=1Vor9V, "		5.0	3.0	V
		V_{DD}=15V, Vo=1.5Vor13.5V "		7.5	4.0	V
Input Leakage Current	I_{IN}	V_{DD}=18V, V_{IN}=18VorV$_{IN}$=0		$\pm10^{-5}$	±1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_I=V_{SS}, V_{DD}		0.01		uA
		V_{DD}=10V, "		0.01		uA
		V_{DD}=15V, "		0.01		uA
Input Stary Capacitance	C_{IN}	All inputs		5	7.5	pF

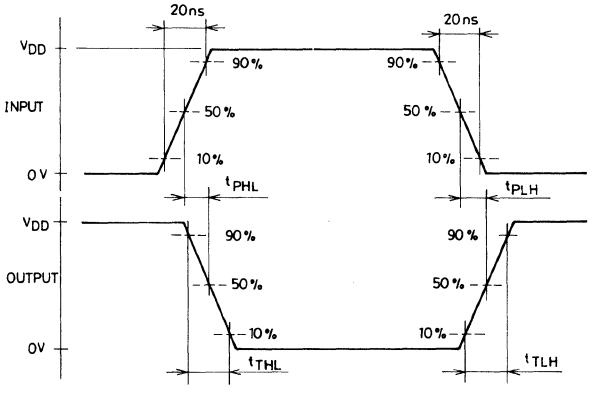
Electrical Characteristics at Ta=-40 to +85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5			mA
		V_{DD}=10V, Vo=9.5V, "	-1.0			mA
		V_{DD}=15V, Vo=13.5V, "	-3.5			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, V_{IN}=V_{DD}	0.5			mA
		V_{DD}=10V, Vo=0.5V, "	1.0			mA
		V_{DD}=15V, Vo=1.5V, "	3.5			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_O\|$<1uA	3.5			V
		V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0			V
		V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_O\|$<1uA			1.5	V
		V_{DD}=10V, Vo=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V, Vo=1.5Vor13.5V, "			4.0	V
Input Leakage Current	I_{IN}	V_{DD}=18V, V_{IN}=18Vor0V			±1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			7.5	uA
		V_{DD}=10V, "			15	uA
		V_{DD}=15V, "			30	uA
Input Capacitance	C_{IN}	All inputs			-	pF

Note) Current direction : +, no sign: Flowing into SSI.
- : Flowing out of SSI.

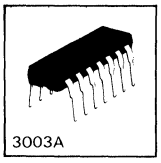
Switching Characteristics at Ta=25±2°C, C_L=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		250	400	ns
		V_{DD}=10V		110	200	ns
		V_{DD}=15V		85	160	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		180	350	ns
		V_{DD}=10V		90	175	ns
		V_{DD}=15V		75	125	ns
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching Time Test Circuit and Waveform





LC4025B



C MOS IC

CMOS Logic B-Series Triple 3-Input NOR Gate

Ⓔ 1352A

The LC4025B is a 3-input NOR logic gate IC (equivalent to B series) having wide operating voltage range, high noise margin, low power dissipation.

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.5 to +20	V
Input Voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leq 85°C$	300	mW
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

Allowable Operating Ranges/T_a=−40 to +85°C, V_{SS}=0V

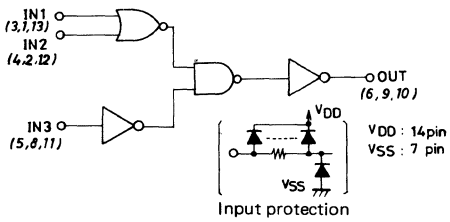
			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Electrical Characteristics/T_a=−40°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{SS}$	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{SS}$, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V

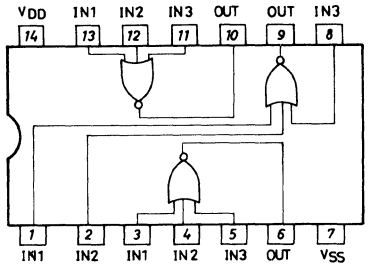
(continued on next page)

Equivalent Circuit
1/3 LC4025B

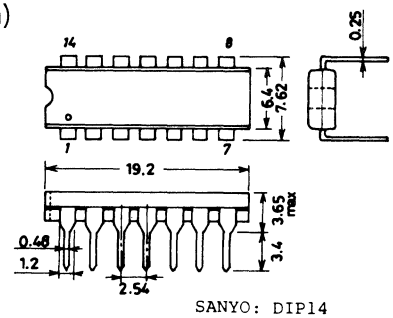


Input protection circuit

Pin Assignment (top view)



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

			min	typ	max	unit
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}$	−0.2			mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−0.5			mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−1.4			mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.52			mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.3			mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.6			mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5			V
		$V_{DD}=10V, V_O=1.0V$, 〃	7.0			V
		$V_{DD}=15V, V_O=1.5V$, 〃	11.0			V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$			1.5	V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V$, 〃			3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$, 〃			4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$			0.3	μA
		$V_{DD}=18V, V_{IN}=0V$			−0.3	μA
Quiescent Current Dissipation	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$			1.0	μA
		$V_{DD}=10V$, 〃			2.0	μA
		$V_{DD}=15V$, 〃			4.0	μA

Electrical Characteristics/T_a=25±2°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}$	4.95			V
		$V_{DD}=10V$, 〃 〃	9.95			V
		$V_{DD}=15V$, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}, V_{DD}$			0.05	V
		$V_{DD}=10V$, 〃 〃			0.05	V
		$V_{DD}=15V$, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}$	−0.16	−0.5		mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−0.4	−1.2		mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−1.2	−6.0		mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.44	1.5		mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.1	3.5		mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.0	15.0		mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5	2.75		V
		$V_{DD}=10V, V_O=1.0V$, 〃	7.0	5.5		V
		$V_{DD}=15V, V_O=1.5V$, 〃	11.0	8.25		V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$		2.25	1.5	V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V$ 〃		4.5	3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$ 〃		6.75	4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$		10^{-5}	1.0	μA
		$V_{DD}=18V, V_{IN}=0V$		-10^{5}	−1.0	μA
Quiescent Current Dissipation	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$		0.01	1.0	μA
		$V_{DD}=10V$, 〃		0.01	2.0	μA
		$V_{DD}=15V$, 〃		0.01	4.0	μA
Input Stray Capacitance	C_{IN}	All input		5	7.5	pF

Electrical Characteristics/T_a=85°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}$	4.95			V
		$V_{DD}=10V$, 〃 〃	9.95			V
		$V_{DD}=15V$, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}, V_{DD}$			0.05	V
		$V_{DD}=10V$, 〃 〃			0.05	V
		$V_{DD}=15V$, 〃 〃			0.05	V

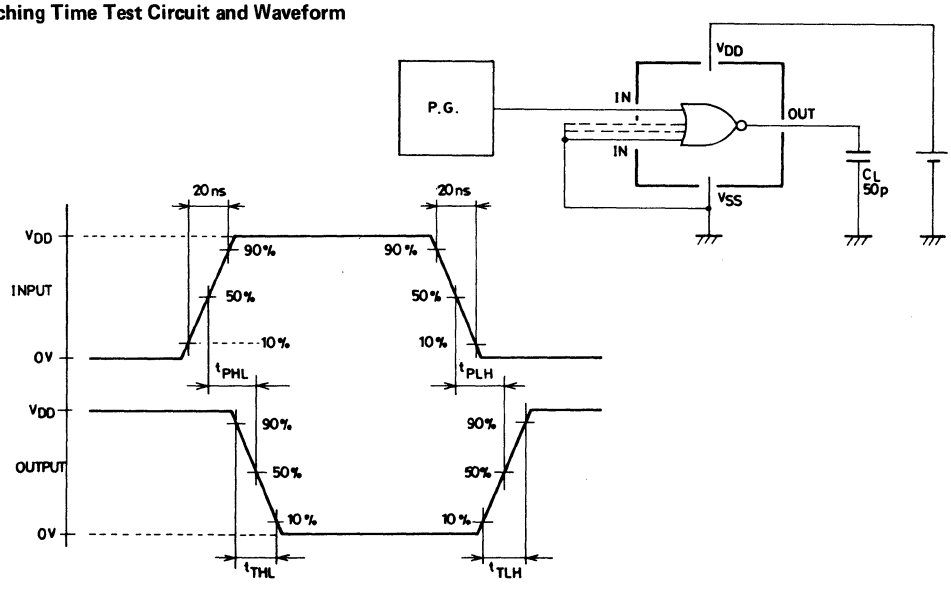
(continued on next page)

			min	typ	max	unit
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}$	−0.12			mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−0.4			mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−1.2			mA
"L" Level Input Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.44			mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.1			mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.0			mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5			V
		$V_{DD}=10V, V_O=1.0V$, 〃	7.0			V
		$V_{DD}=15V, V_O=1.5V$, 〃	11.0			V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$			2.25	V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V$, 〃			4.5	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$, 〃			6.75	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$			1.0	μA
		$V_{DD}=18V, V_{IN}=0V$			1.0	μA
Quiescent Current Dissipation	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$			7.5	μA
		$V_{DD}=10V$, 〃			15	μA
		$V_{DD}=15V$, 〃			30	μA

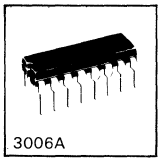
Note) Current direction: +, no sign: Flowing into device,
−: Flowing out of device

Switching Characteristics/T_a=25±2°C, C_L=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	$V_{DD}=5V$		220	400	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		80	160	ns
"L" Level Propagation Delay Time	t_{PHL}	$V_{DD}=5V$		160	350	ns
		$V_{DD}=10V$		80	175	ns
		$V_{DD}=15V$		65	125	ns
Rise Time	t_{TLH} (t_r)	$V_{DD}=5V$		130	400	ns
		$V_{DD}=10V$		65	200	ns
		$V_{DD}=15V$		50	160	ns
Fall Time	t_{THL} (t_f)	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns

Switching Time Test Circuit and Waveform



LC4027B



C MOS IC

CMOS Logic B-Series
Dual J-K Master-Slave Flip-Flop

Ⓔ 1007B

The LC4027B is a J-K master-slave flip-flop (equipment to B series) having such features as wide operating voltage range, high noise margin, low power dissipation and also having set/reset function.

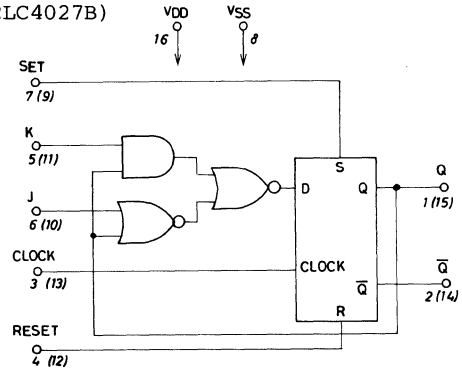
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		-0.5 to +20	V
Input Voltage	V_{IN}		-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pd max	Ta≦85°C	300	mW
Operation Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

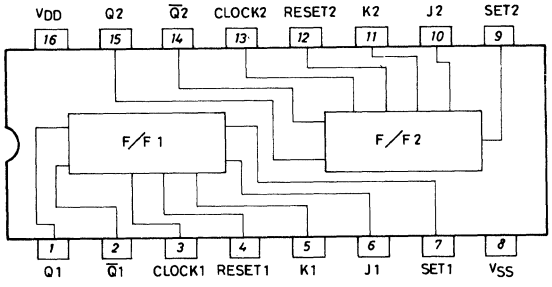
Allowable Operating Ranges at Ta=-40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Equivalent Circuit
(1/2LC4027B)



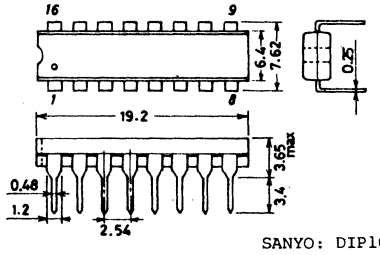
Pin Assignment



Input					Output	
R	S	J	K	clock	Q	Q̄
0	1	※	※	※	1	0
1	0	※	※	※	0	1
1	1	※	※	※	0	1
0	0	0	0	↑	Qn	Q̄n
0	0	0	1	↑	0	1
0	0	1	0	↑	1	0
0	0	1	1	↑	Q̄n	Qn
0	0	※		↓	Qn	Q̄n

※don't care
· no change
·· change

Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Electrical Characteristics at Ta=-40°C, V_{SS}=0V			min	typ	max	unit
"Hi" Level Output Voltage	V_{OH}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{DD}, V_{SS}	4.95			V
		V_{DD}=10V, "	9.95			V
		V_{DD}=15V, "	14.95			V
"Lo" Level Output Voltage	V_{OL}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{DD}, V_{SS}			0.05	V
		V_{DD}=10V, "			0.05	V
		V_{DD}=15V, "			0.05	V
"Hi" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}, V_{SS}	-0.2			mA
		V_{DD}=10V, V_O=9.5V, "	-0.5			mA
		V_{DD}=15V, V_O=13.5V, "	-1.4			mA
"Lo" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}, V_{SS}	0.52			mA
		V_{DD}=10V, V_O=0.5V, "	1.3			mA
		V_{DD}=15V, V_O=1.5V, "	3.6			mA
"Hi" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V, 4.5V, |I_{OUT}|<1uA	3.5			V
		V_{DD}=10V, V_O=1.0V, 9.0V "	7.0			V
		V_{DD}=15V, V_O=1.5V, 13.5V "	11.0			V
"Lo" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V, 4.5V, |I_{OUT}|<1uA			1.5	V
		V_{DD}=10V, V_O=1.0V, 9.0V, "			3.0	V
		V_{DD}=15V, V_O=1.5V, 13.5V, "			4.0	V
"Hi" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			0.3	uA
"Lo" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			-0.3	uA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}			4	uA
		V_{DD}=10V, "			8	uA
		V_{DD}=15V, "			16	uA

Electrical Characteristics at Ta=25±2°C, V_{SS}=0V			min	typ	max	unit
"Hi" Level Output Voltage	V_{OH}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{DD}, V_{SS}	4.95	5.00		V
		V_{DD}=10V, "	9.95	10.00		V
		V_{DD}=15V, "	14.95	15.00		V
"Lo" Level Output Voltage	V_{OL}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{DD}, V_{SS}		0.00	0.05	V
		V_{DD}=10V, "		0.00	0.05	V
		V_{DD}=15V, "		0.00	0.05	V
"Hi" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}, V_{SS}	-0.16	-0.36		mA
		V_{DD}=10V, V_O=9.5V, "	-0.4	-0.9		mA
		V_{DD}=15V, V_O=13.5V, "	-1.2	-3.5		mA
"Lo" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}, V_{SS}	0.44	0.88		mA
		V_{DD}=10V, V_O=0.5V, "	1.1	2.55		mA
		V_{DD}=15V, V_O=1.5V, "	3.0	8.8		mA
"Hi" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V, 4.5V, |I_{OUT}|<1uA	3.5	2.75		V
		V_{DD}=10V, V_O=1.0, 9.0V, "	7.0	5.5		V
		V_{DD}=15V, V_O=1.5V, 13.5V, "	11.0	8.25		V
"Lo" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V, 4.5V, |I_{OUT}|<1uA		2.25	1.5	V
		V_{DD}=10V, V_O=1.0V, 9.0V, "		4.5	3.0	V
		V_{DD}=15V, V_O=1.5V, 13.5V, "		6.75	4.0	V
"Hi" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V		10^{-5}	0.3	uA
"Lo" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V		-10^{-5}	-0.3	uA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}		0.002	4	uA
		V_{DD}=10V, "		0.004	8	uA
		V_{DD}=15V, "		0.008	16	uA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at Ta=+85°C, V_{SS}=0

			min	typ	max	unit
"Hi" Level Output Voltage	V_{OH}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{DD}, V_{SS}	4.95			V
		V_{DD}=10V, "	9.95			V
		V_{DD}=15V, "	14.95			V
"Lo" Level Output Voltage	V_{OL}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{DD}, V_{SS}			0.05	V
		V_{DD}=10V, "			0.05	V
		V_{DD}=15V, "			0.05	V
"Hi" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}, V_{SS}	-0.12			mA
		V_{DD}=10V, V_O=9.5V, "	-0.3			mA
		V_{DD}=15V, V_O=13.5V, "	-1.0			mA
"Lo" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}, V_{SS}	0.36			mA
		V_{DD}=10V, V_O=0.5V, "	0.9			mA
		V_{DD}=15V, V_O=1.5V, "	2.4			mA
"Hi" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V, 4.5V, |I_{OUT}|<1uA	3.5			V
		V_{DD}=10V, V_O=1.0V, 9.0V, "	7.0			V
		V_{DD}=15V, V_O=1.5V, 13.5V, "	11.0			V
"Lo" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V, 4.5V, |I_{OUT}|<1uA			1.5	V
		V_{DD}=10V, V_O=1.0V, 9.0V "			3.0	V
		V_{DD}=15V, V_O=1.5V, 13.5V, "			4.0	V
"Hi" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			1.0	uA
"Lo" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			-1.0	uA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}			30	uA
		V_{DD}=10V, "			60	uA
		V_{DD}=15V, "			120	uA

(Note) Current direction { + (no sign): Flowing into device
- : Flowing out of device

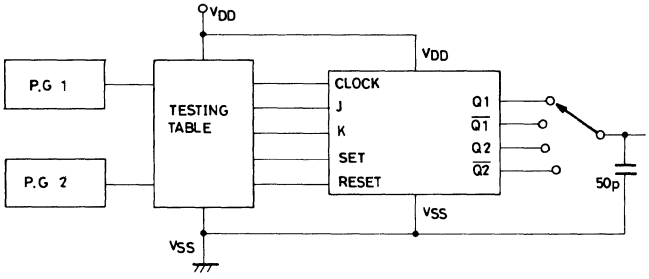
Switching Characteristics at Ta=25±2°C, Input t_r, t_f=20ns, V_{SS}=0V, C_L=50pF

			min	typ	max	unit
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"Hi" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V, clock-Q, $\bar{Q}$, Waveform 1		250	550	ns
		V_{DD}=10V, "		110	350	ns
		V_{DD}=15V, "		80	300	ns
"Lo" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V, clock-Q, $\bar{Q}$, Waveform 1		250	500	ns
		V_{DD}=10V, "		110	350	ns
		V_{DD}=15V, "		80	260	ns
"Hi" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V, set reset-Q, $\bar{Q}$, Waveform 2		250	500	ns
		V_{DD}=10V, "		110	350	ns
		V_{DD}=15V, "		80	260	ns
"Lo" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V, set reset-Q, $\bar{Q}$, Waveform 2		250	500	ns
		V_{DD}=10V, "		110	350	ns
		V_{DD}=15V, "		80	260	ns
Maximum Clock Operation Frequency	f max	V_{DD}=5V, Wave form 1	1.0	3.0		MHz
		V_{DD}=10V, "	3.0	8.0		MHz
		V_{DD}=15V, "	3.5	12.0		MHZ
Maximum Clock Rise, Fall Time	$t_{r\phi}$	V_{DD}=5V, Waveform 1			20.0	us
	$t_{f\phi}$	V_{DD}=10V, "			2.5	us
		V_{DD}=15V, "			1.0	us

(continued on the next page)

			min	typ	max	unit
Minimum Clock Pulse Width	$t_W(\phi)$	V_{DD}=5V, Waveform 1		165	330	ns
		V_{DD}=10V, "		55	110	ns
		V_{DD}=15V, "		38	75	ns
Minimum Set, Reset Pulse Width	t_W (set, reset)	V_{DD}=5V, Waveform 2		100	500	ns
		V_{DD}=10V, "		50	250	ns
		V_{DD}=15V, "		40	200	ns
Minimum Data Set-up Time	t_S	V_{DD}=5V, Waveform 3		100	250	ns
		V_{DD}=10V, "		40	125	ns
		V_{DD}=15V, "		30	100	ns

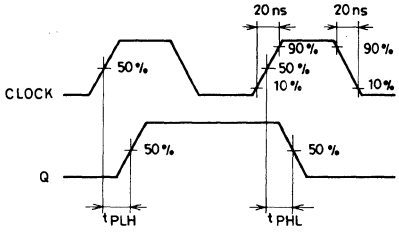
Switching Time Test Circuit and Waveform



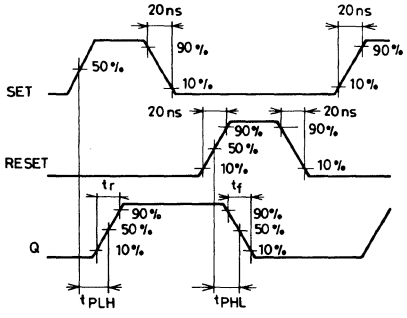
Testing Table

TEST	J	K	RESET	SET	clock
1	V_{DD}	V_{DD}	GND	GND	P.G.1
2	V_{DD}	V_{DD}	P.O.1	P.O.2	VDD
3	P.G.1	P.G.1	GND	GND	P.G.2

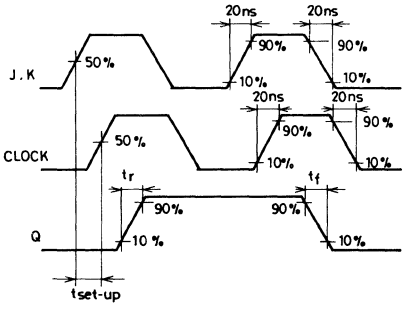
Waveform 1



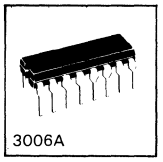
Waveform 2



Waveform 3



LC4028B



C MOS IC

CMOS Logic B-Series BCD to Decimal Decoder

Ⓔ971B

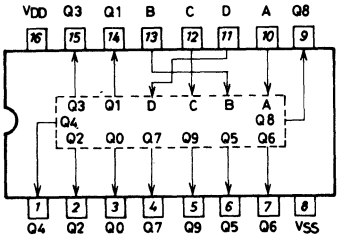
Use

. C MOS standard logic IC for logic circuit

Functions and Feature

. Wide operating voltage range, high noise margin, low power dissipation
. BCD-to-Decimal decoder that converts BCD signal into decimal signal. Of 10 outputs (Q0 to Q9), outputs coresponding to input BCD code turn to "H" level; all other outputs turn to "L" level.
. If Din is used as inhibit input by using 3 inputs (Ain to Cin), this IC can be also used as Binary-to-Octal decoder that converts binary signal into octal signal.

. Pin Assignment and Circuit Configuration (Top View)

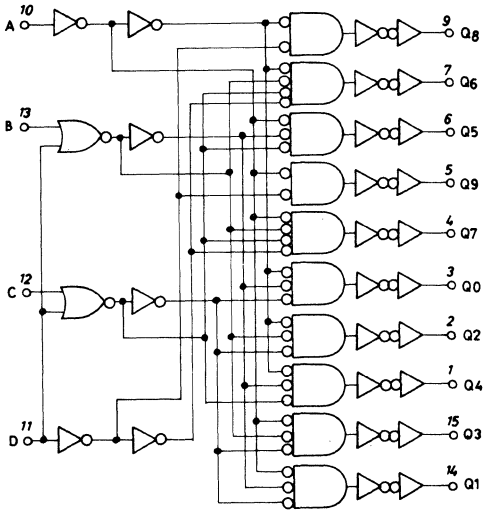


. Truth Table

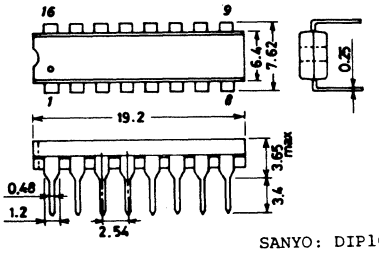
INPUT				selected OUTPUT [H]
A	B	C	D	
0	0	0	0	Q0
1	0	0	0	Q1
0	1	0	0	Q2
1	1	0	0	Q3
0	0	1	0	Q4
1	0	1	0	Q5
0	1	1	0	Q6
1	1	1	0	Q7
0	*	*	1	Q8
1	*	*	1	Q9

1 : "H" Level
0 : "L" Level
* : don't care

. Equivalent circuit



Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Allowable Operating Ranges at	Ta=25°C, V_{SS}=0V		unit
Maximum Supply Voltage	V_{DD}max	-0.5 to +20	V
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Allowable Power Dissipation	Pdmax Ta≦85°C	300	mW
Operating Temperature	Topg	-40 to +85	°C
Storage Temperature	Tstg	-65 to +150	°C

Allowable Operating Ranges at	Ta=-40 to +85°C, V_{SS}=0V		unit
Supply Voltage	V_{DD}	3.0 to 18.0	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Electrical Characteristics at	Ta=-40°C, V_{SS}=0V	min	typ	max	unit
Output"H"Level Voltage V_{OH}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
	V_{DD}=10V, " "	9.95			V
	V_{DD}=15V, " "	14.95			V
Output"L"Level Voltage V_{OL}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{SS}, V_{DD}			0.05	V
	V_{DD}=10V " "			0.05	V
	V_{DD}=15V " "			0.05	V
Output"H"Level Current I_{OH}	V_{DD}=5V, Vo=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5			mA
	V_{DD}=10V, Vo=9.5V, "	-1.0			mA
	V_{DD}=15V, Vo=13.5V, "	-3.5			mA
Output"L"Level Current I_{OL}	V_{DD}=5V, Vo=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5			mA
	V_{DD}=10V, Vo=0.5V, "	1.0			mA
	V_{DD}=15V, Vo=1.5V, "	3.5			mA
Input"H"Level Voltage V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, |I_{OUT}|<1uA	3.5			V
	V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0			V
	V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0			V
Input"L"Level Voltage V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, |I_{OUT}|<1uA			1.5	V
	V_{DD}=10V, Vo=1.0Vor9.0V, "			3.0	V
	V_{DD}=15V, Vo=1.5Vor13.5V, "			4.0	V
Input Leak Current I_{IN}	V_{DD}=18V, V_{IN}=18V			1.0	uA
	V_{DD}=18V, V_{IN}=0V			-1.0	uA
Quiescent Current I_{DD}	V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}			1.0	uA
Disipation	V_{DD}=10V "			2.0	uA
	V_{DD}=15V "			4.0	uA

Electrical Characteristics at	Ta=25°C±2°C, V_{SS}=0V	min	typ	max	unit
Output"H"Level Voltage V_{OH}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
	V_{DD}=10V, " "	9.95	10.00		V
	V_{DD}=15V, " "	14.95	15.00		V
Output"L"Level Voltage V_{OL}	V_{DD}=5V, |I_{OUT}|<1uA, V_{IN}=V_{SS}, V_{DD}		0.00	0.05	V
	V_{DD}=10V, " "		0.00	0.05	V
	V_{DD}=15V, " "		0.00	0.05	V
Output"H"Level Current I_{OH}	V_{DD}=5V, Vo=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5	-1.0		mA
	V_{DD}=10V, Vo=9.5V, "	-1.0	-2.0		mA
	V_{DD}=10V, Vo=13.5V,	-3.5	-7.0		mA
Output"L"Level Current I_{OL}	V_{DD}=5V, Vo=0.4V, V_{IN}=V_{SS}, V_{DD},	0.5	1.0		mA
	V_{DD}=10V, Vo=0.5V, "	1.0	2.0		mA
	V_{DD}=15V, Vo=1.5V, "	3.5	7.0		mA
Input"H"Level Voltage V_{IH}	V_{DD}=5V, Vo=0.5Vpr4.5V, |I_{OUT}|<1uA	3.5	2.5		V
	V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0	5.0		V
	V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0	7.5		V

			min	typ	max	unit
Input"L"Level Voltage	V_{IL}	V_{DD}=5V,Vo=0.5Vor4.5V,$\|I_{OUT}\|$<1uA		2.5	1.5	V
		V_{DD}=10V,Vo=1.0V9.0V, "		5.0	3.0	V
		V_{DD}=15V,Vo=1.5Vor13.5V, "		7.5	4.0	V
Input Leakage Current	I_{IN}	V_{DD}=18V,V_{IN}=18V,		10^5	1.0	uA
		V_{DD}=18V,V_{IN}=0V		-10^5	-1.0	uA
Quiescent Current Disipation	I_{DD}	V_{DD}=5V,V_{IN}=V_{DD},V_{SS},		0.005	1.0	uA
		V_{DD}=10V, "		0.01	2.0	uA
		V_{DD}=15V, "		0.015	4.0	uA
Input Capacitance	C_{IN}	All inputs		5.0	7.5	pF

Electrical Characteristics at Ta=85°C,V_{SS}=0V

			min	typ	max	unit
Output"H"Level Voltage	V_{OH}	V_{DD}=5V,$\|I_{OUT}\|$<1uA,V_{IN}=V_{SS},V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
Output"L"Level Voltage	V_{OL}	V_{DD}=5V,$\|I_{OUT}\|$<1uA,V_{IN}=V_{SS},V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
Output"H"Level Current	I_{OH}	V_{DD}=5V,Vo=4.6V,V_{IN}=V_{SS},V_{DD}	-0.4			mA
		V_{DD}=10V,Vo=9.5V, "	-0.8			mA
		V_{DD}=15V,Vo=13.5V, "	-2.8			mA
Output"L"Level Current	I_{OL}	V_{DD}=5V,Vo=0.4V,V_{IN}=V_{SS},V_{DD}	0.4			mA
		V_{DD}=10V,Vo=0.5V, "	0.8			mA
		V_{DD}=15V,Vo=1.5V, "	2.8			mA
Input"H"Level Voltage	V_{IH}	V_{DD}=5V,Vo=0.5Vor4.5V,$\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V,Vo=1.0Vor9.0V, "	7.0			V
		V_{DD}=15V,Vo=1.5Vor13.5V, "	11.0			V
Input"L"Level Voltage	V_{IL}	V_{DD}=5V,Vo=0.5Vor4.5V,$\|I_{OUT}\|$<1uA,			1.5	V
		V_{DD}=10V,Vo=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V,Vo=1.5Vor13.5V, "			4.0	V
Input Leakage Current	I_{IN}	V_{DD}=18V,V_{IN}=18V			1.0	uA
		V_{DD}=18V,V_{IN}=0V			-1.0	uA
Quiescent Current Disipation	I_{DD}	V_{DD}=5V,V_{IN}=V_{DD},V_{SS}			7.5	uA
		V_{DD}=10V, "			15.0	uA
		V_{DD}=15V, "			30.0	uA

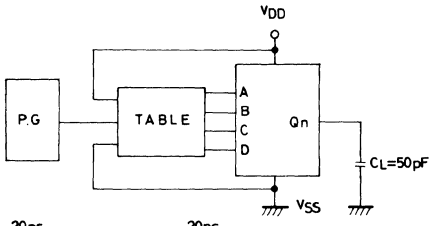
Note) Current Direction : +, no sign: Flowing into device
- : Flowing out of device

Switching Characteristics at Ta=25±2°C,V_{SS}=0V,C_L=50pF

			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		300	700	ns
		V_{DD}=10V		130	300	ns
		V_{DD}=15V		90	200	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		300	700	ns
		V_{DD}=10V		130	300	ns
		V_{DD}=15V		90	200	ns
Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Fall Time	t_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching Time Test Circuit and Waveform

Test Circuit



Waveform

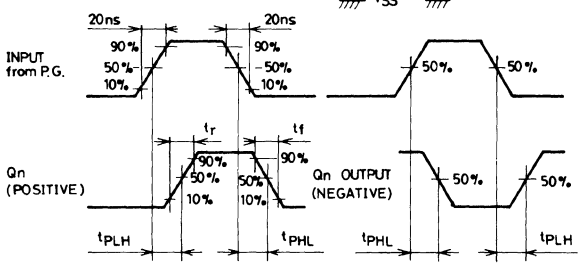
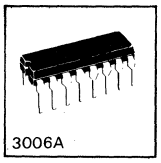


TABLE TEST CONDITION

TEST No.	INPUT CONDITION				OUTPUT	
	A	B	C	D	Pos.	Neg.
1	P.G	VSS	VSS	VSS	Q1	Q0
2	VSS	P.G	VDD	VSS	Q6	Q4
3	VDD	VDD	P.G	VSS	Q7	Q3
4	VDD	VSS	VSS	P.G	Q9	Q1
5	VSS	P.G	VSS	VSS	Q2	Q0
6	VDD	VSS	P.G	VSS	Q5	Q1
7	VSS	VSS	VSS	P.G	Q8	Q0
8	VSS	VSS	P.G	VSS	Q4	Q0
9	P.G	VDD	VSS	VSS	Q3	Q2

LC4040B



C MOS IC

CMOS Logic B-Series 12-Stage Binary Counter

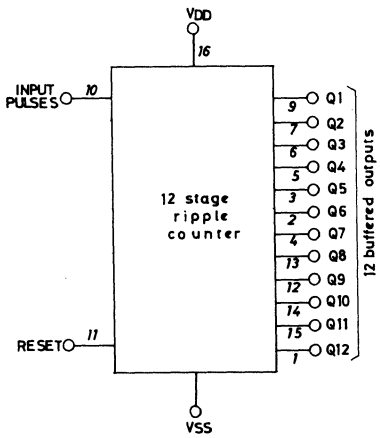
Ⓔ 1495A

The LC4040B is an asynchronous reset function-provided 12-stage ripple-carry binary counter (equivalent to B series) having such features as wide operating voltage range, high noise margin, and low power dissipation. The state of a counter advances one count on the negative transition of each clock input. "Hi" level of reset input resets all counters regardless of clock input, setting all outputs (Q1 to Q12) to "Lo" level.
Application areas include frequency dividers, control counters, and timing circuits.

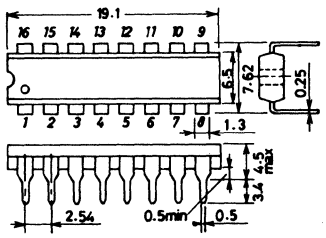
Allowable Operating Ranges at Ta=25°C				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20.0	V
Maximum Input Voltage	$V_{IN}max$		V_{SS}-0.5 to V_{DD}+0.5	V
Maximum Output Voltage	$V_{OUT}max$		V_{SS}-0.5 to V_{DD}+0.5	V
Maximum Input Current	$I_{IN}max$		±10	mA
Allowable Power Dissipation	Pdmax		300	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C
	Tsol	t=10sec	260	°C

Allowable Operating Ranges at Ta=-40 to +85°C			unit
Supply Voltage	V_{DD}	3.0 to 18.0	V
Input Voltage	V_{IN}	0 to V_{DD}	V

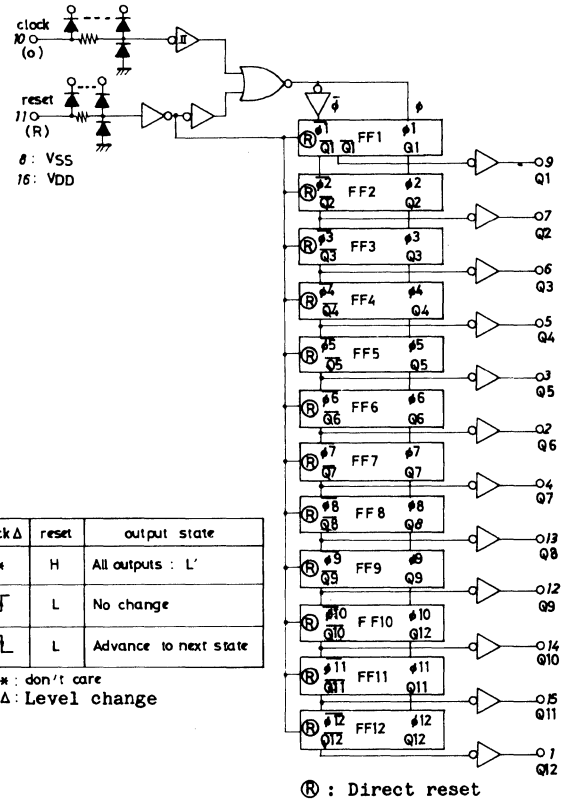
Pin Assignment



Case Outline 3006A-D16IC
(unit:mm)



Equivalent Circuit and Truth Table



clock Δ	reset	output state
*	H	All outputs : L'
⎍	L	No change
⎏	L	Advance to next state

* : don't care
Δ : Level change

Electrical Characteristics at Ta=25°C, V_{SS}=0V Vo:[], V_{DD}:()

				min	typ	max	unit
Output"H"Level Voltage	V_{OH}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}$, V_{DD},	(5V)	4.95	5.00		V
		"	(10V)	9.95	10.00		V
		"	(15V)	14.95	15.00		V
Output"L"Level Voltage	V_{OL}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}$, V_{DD},	(5V)		0.00	0.05	V
		"	(10V)		0.00	0.05	V
		"	(15V)		0.00	0.05	V
Output"H"Level Current	I_{OH}	$V_{IN}=V_{SS}$, V_{DD},	[4.6V](5V)	-0.16	-0.5		mA
		"	[9.5V](10V)	-0.4	-1.2		mA
		"	[13.5V](15V)	-1.2	-6.0		mA
Output"L"Level Current	I_{OL}	$V_{IN}=V_{SS}$, V_{DD},	[0.4V](5V)	0.44	1.5		mA
		"	[0.5V](10V)	1.1	3.5		mA
		"	[1.5V](15V)	3.0	15.0		mA
Input"H"Level Voltage	V_{IH}	$\|I_{OUT}\|$<1uA,	[0.5,4.5V](5V)	3.5	2.75		V
			[1.0,9.0V](10V)	7.0	5.5		V
			[1.5,13.5V](15V)	11.0	8.25		V
Input"L"Level Voltage	V_{IL}	$\|I_{OUT}\|$<1uA,	[0.5,4.5V](5V)		2.25	1.5	V
			[1.0,9.0V](10V)		4.5	3.0	V
			[1.5,13.5V](15V)		6.75	4.0	V
Input"H"level Current	I_{IH}	V_{IH}=18V,	(18V)		10	0.3	uA
Input"L"Level Current	I_{IL}	V_{IL}=0V,	(18V)		-10	-0.3	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD},	(5V)		0.005	20	uA
Disipation		"	(10V)		0.010	40	uA
		"	(15V)		0.015	80	uA
Input Capacitance	C_{IN}				5.0	7.5	pF

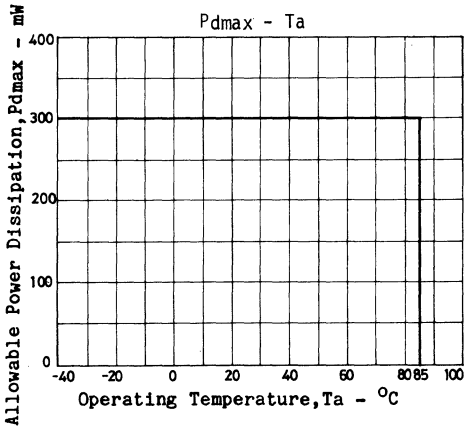
Electrical Characteristics at Ta=-40°C, V_{SS}=0V Vo:[], V_{DD}:()				min	typ	max	unit
Output"H"Level Voltage	V_{OH}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}$, V_{DD},	(5V)	4.95			V
		"	(10V)	9.95			V
		"	(15V)	14.95			V
Output"L"Level Voltage	V_{OL}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}$, V_{DD},	(5V)			0.05	V
		"	(10V)			0.05	V
		"	(15V)			0.05	V
Output"H"Level Current	I_{OH}	$V_{IN}=V_{SS}$, V_{DD}, [4.6V]	(5V)	-0.2			mA
		" [9.5V]	(10V)	-0.5			mA
		" [13.5V]	(15V)	-1.4			mA
Output"L"Level Current	I_{OL}	$V_{IN}=V_{SS}$, V_{DD}, [0.4V]	(5V)	0.52			mA
		" [0.5V]	(10V)	1.3			mA
		" [1.5V]	(15V)	3.6			mA
Input"H"Level Voltage	V_{IH}	$\|I_{OUT}\|$<1uA, [0.5,4.5V]	(5V)	3.5			V
		[1.0,9.0V]	(10V)	7.0			V
		[1.5,13.5V]	(15V)	11.0			V
Input"L"Level Voltage	V_{IL}	$\|I_{OUT}\|$<1uA, [0.5,4.5V]	(5V)			1.5	V
		[1.0,9.0V]	(10V)			3.0	V
		[1.5,13.5V]	(15V)			4.0	V
Input"H"level Current	I_{IH}	V_{IH}=18V,	(18V)			0.3	uA
Input"L"Level Current	I_{IL}	V_{IL}=0V,	(18V)			-0.3	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD},	(5V)			20	uA
Disipation		"	(10V)			40	uA
		"	(15V)			80	uA

Electrical Characteristics at Ta=85°C, V_{SS}=0V Vo:[], V_{DD}:()				min	typ	max	unit
Output"H"Level Voltage	V_{OH}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}$, V_{DD},	(5V)	4.95			V
		"	(10V)	9.95			V
		"	(15V)	14.95			V
Output"L"Level Voltage	V_{OL}	$\|I_{OUT}\|$<1uA, $V_{IN}=V_{SS}$, V_{DD},	(5V)			0.05	V
		"	(10V)			0.05	V
		"	(15V)			0.05	V
Output"H"Level Current	I_{OH}	$V_{IN}=V_{SS}$, V_{DD}, [4.6V]	(5V)	-0.12			mA
		" [9.5V]	(10V)	-0.3			mA
		" [13.5V]	(15V)	-1.0			mA
Output"L"Level Current	I_{OL}	$V_{IN}=V_{SS}$, V_{DD}, [0.4V]	(5V)	0.36			mA
		" [0.5V]	(10V)	0.9			mA
		" [1.5V]	(15V)	2.4			mA
Input"H"Level Voltage	V_{IH}	$\|I_{OUT}\|$<1uA, [0.5,4.5V]	(5V)	3.5			V
		[1.0,9.0V]	(10V)	7.0			V
		[1.5,13.5V]	(15V)	11.0			V
Input"L"Level Voltage	V_{IL}	$\|I_{OUT}\|$<1uA, [0.5,4.5V]	(5V)			1.5	V
		[1.0,9.0V]	(10V)			3.0	V
		[1.5,13.5V]	(15V)			4.0	V
Input"H"level Current	I_{IH}	V_{IH}=18V,	(18V)			1.0	uA
Input"L"Level Current	I_{IL}	V_{IL}=0V,	(18V)			-1.0	uA
Quiescent Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD},	(5V)			150	uA
Disipation		"	(10V)			300	uA
		"	(15V)			600	uA

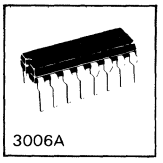
Note) Current Direction : +, no sign: Flowing into device
- : Flowing out of device

Switching Characteristics at Ta=25±2°C, V_{SS}=0V, C_L=50pF

		V_{DD}	min	typ	max	unit
Output Rise Time	t_r (t_{TLH})	5V		130	400	ns
		10V		65	200	ns
		15V		50	160	ns
Output Fall Time	t_f (t_{THL})	5V		100	200	ns
		10V		50	100	ns
		15V		40	80	ns
"H" Level Propagation Delay Time (clock-Q1)	t_{PLH}	5V		600	1000	ns
		10V		220	400	ns
		15V		180	320	ns
"L" Level Propagation Delay Time (clock-Q1)	t_{PHL}	5V		500	900	ns
		10V		170	350	ns
		15V		130	250	ns
"H" Level Propagation Delay Time (clock-Q12)	t_{PLH}	5V		4.0	7.0	us
		10V		1.5	2.7	us
		15V		1.2	2.1	us
"L" Level Propagation Delay Time (clock-Q12)	t_{PHL}	5V		4.0	7.0	us
		10V		1.5	2.7	us
		15V		1.2	2.1	us
"L" Level Propagation Delay Time (reset-Q)	t_{PHL}	5V		640	1300	ns
		10V		200	500	ns
		15V		160	400	ns
Maximum Clock Frequency	$f_{max\phi}$	5V	1.0	1.5		MHz
		10V	2.0	4.5		MHz
		15V	2.5	5.5		MHz
Minimum Reset Pulse Width	t_{wreset}	5V		200	800	ns
		10V		100	300	ns
		15V		80	250	ns
Maximum Clock Rise/ Fall Time	$t_{r\phi}, t_{f\phi}$	5V			2.0	us
		10V			2.5	us
		15V			1.0	us



LC4049B



C MOS IC

CMOS Logic B-Series Hex Buffer/Converter (Inverting Type)

Ⓔ 1025D

Features and Functions

- Inverting type hex buffer/converter IC having such features as wide operating range, high noise margin, low power dissipation, etc.
- Conveniently used as interface between C MOS and TTL, DTL because of large output current capable of direct driving one TTL or DTL.
- Also used as level converter from 15V, 10V C MOS logic circuit to 5V C MOS/TTL logic circuit because voltage up to V_{SS}+18V can be applied to input without regard to V_{DD}.
- Good transient characteristic of switching because of 3-stage inverter configuration.

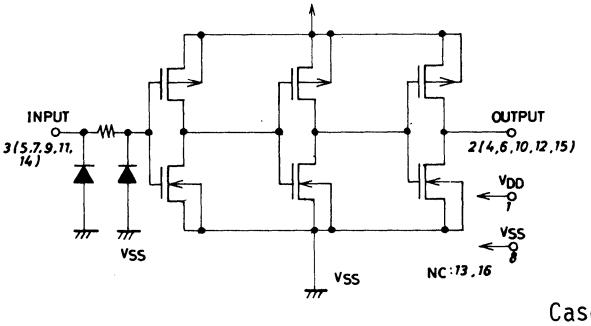
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{SS}+20	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		-10	mA
Allowable Power Dissipation	$P_d max$	$T_a \leq 85°C$	300	mW
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

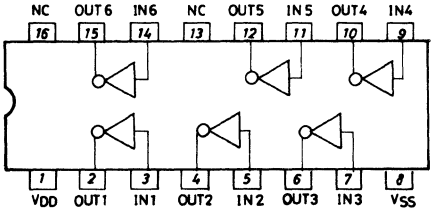
Allowable Operating Ranges at T_a=-40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

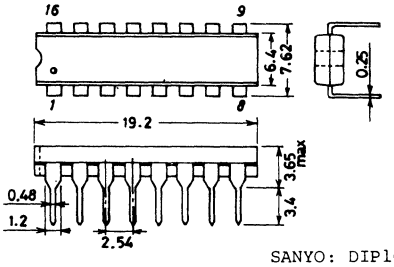
Equivalent Circuit (1/6 LC4049B)



Pin Assignment (Top view)



Case Outline (unit:mm) 3006A-D16IC



SANYO: DIP16

Electrical Characteristics at T_a=-40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|<$ 1uA, $V_{IN}=V_{SS}$	4.95			V
"L" Level Output Volt		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|<$ 1uA, $V_{IN}=V_{DD}$			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, v_o=2.5V, $V_{IN}=V_{SS}$	-1.4			mA
		V_{DD}=10V, v_o=9.5V, "	-1.4			mA
		V_{DD}=15V, v_o=13.5V, "	-4.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, v_o=0.4V, $V_{IN}=V_{DD}$	3.5			mA
		V_{DD}=10V, v_o=0.5V, "	6.0			mA
		V_{DD}=15V, v_o=1.5V, "	26.0			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, v_o=0.5V, $\|I_{OUT}\|<$ 1uA	3.5			V
		V_{DD}=10V, v_o=1.0V, "	7.0			V
		V_{DD}=15V, v_o=1.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, v_o=4.5V, $\|I_{OUT}\|<$ 1uA			1.5	V
		V_{DD}=10V, v_o=9.0V, "			3.0	V
		V_{DD}=15V, v_o=13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			-0.3	uA
Quiescent Current Dissi-	I_{DD}	V_{DD}=5V, $V_{IN}=V_{SS}, V_{DD}$			4	uA
pation		V_{DD}=10V, "			8	uA
		V_{DD}=15V, "			16	uA

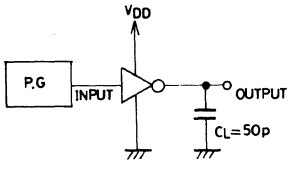
Electrical Characteristics at T_a=25°C±2°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|<$ 1uA, $V_{IN}=V_{SS}$	4.95	5.0		V
		V_{DD}=10V, " "	9.95	10.0		V
		V_{DD}=15V, " "	14.95	15.0		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|<$ 1uA, $V_{IN}=V_{DD}$		0	0.05	V
		V_{DD}=10V, " "		0	0.05	V
		V_{DD}=15V, " "		0	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, v_o=2.5V, $V_{IN}=V_{SS}$	-1.25	-2.5		mA
		V_{DD}=10V, v_o=9.5V "	-1.25	-2.5		mA
		V_{DD}=15V, v_o=13.5V "	-3.75	-10.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, v_o=0.4V, $V_{IN}=V_{DD}$	3.2	6.0		mA
		V_{DD}=10V, v_o=0.5V, "	5.0	16.0		mA
		V_{DD}=15V, v_o=1.5V "	24.0	40.0		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, v_o=0.5V, $\|I_{OUT}\|<$ 1uA	3.5	2.75		V
		V_{DD}=10V, v_o=1.0V, "	7.0	5.50		V
		V_{DD}=15V, v_o=1.5V, "	11.0	8.25		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, v_o=4.5V, $\|I_{OUT}\|<$ 1uA		2.25	1.5	V
		V_{DD}=10V, v_o=9.0V, "		4.50	3.0	V
		V_{DD}=15V, v_o=13.5V, "		6.75	4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V		10^{-5}	0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V		-10^{-5}	-0.3	uA
Quiescent Current Dissi-		V_{DD}=5V, $V_{IN}=V_{SS}, V_{DD}$		0.002	4	uA
pation		V_{DD}=10V, "		0.004	8	uA
		V_{DD}=15V, "		0.008	16	uA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at T_a=+85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, I_{OUT} 1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, v_o=2.5V, V_{IN}=V_{SS}	-1.0			mA
		V_{DD}=10V, v_o=9.5V, "	-1.0			mA
		V_{DD}=15V, v_o=13.5V, "	-3.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, v_o=0.4V, V_{IN}=V_{DD}	2.5			mA
		V_{DD}=10V, v_o=0.5V, "	3.6			mA
		V_{DD}=15V, v_o=1.5V, "	18.0			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, v_o=0.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V, v_o=1.0V, "	7.0			V
		V_{DD}=15V, v_o=1.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, v_o=4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, v_o=9.0V, "			3.0	V
		V_{DD}=15V, v_o=13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			1.0	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			-1.0	uA
Quiescent Current Dissi-	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			30	uA
pation		V_{DD}=10V, "			60	uA
		V_{DD}=15V, "			120	uA

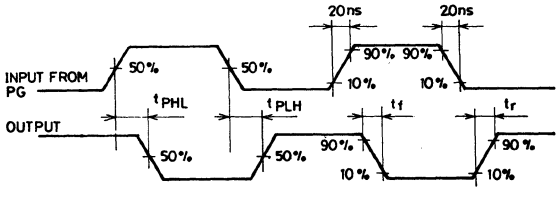
Note) Current direction (+(no sign) : Flowing into IC
- : Flowing out of IC)

Switching Characteristics at T_a=25°C±2°C, V_{SS}=0V, C_L=50pF			min	typ	max	unit
Output Rise Time	t_{TLH}	V_{DD}=5V		100	200	ns
	(t_r)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Output Fall Time	t_{THL}	V_{DD}=5V		50	100	ns
	(t_f)	V_{DD}=10V		25	50	ns
		V_{DD}=15V		20	40	ns
"H" Level Propagation	t_{PLH}	V_{DD}=5V		140	220	ns
Delay Time		V_{DD}=10V		70	110	ns
		V_{DD}=15V		50	80	ns
"L" Level Propagation	t_{PHL}	V_{DD}=5V		110	220	ns
Delay Time		V_{DD}=10V		50	110	ns
		V_{DD}=15V		40	80	ns

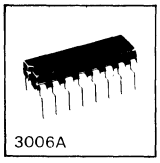
Test circuit



Wave form



LC4050B



C MOS IC

CMOS Logic B-Series Hex Buffer/Converter (Noninverting Type)

Ⓔ 1026D

The LC4050B is a noninverting type hex buffer/converter (equivalent to B series) having such features as wide operating voltage range, high noise immunity, low power dissipation, etc. It is capable of driving LED, one TTL or DTL.

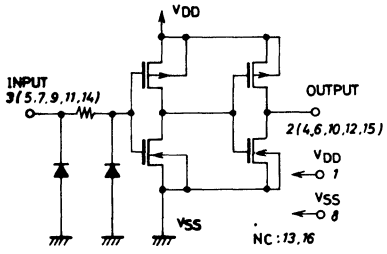
Absolute Maximum Rantings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		V_{SS}−0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}−0.5 to V_{SS}+20	V
Output Voltage	V_{OUT}		V_{SS}−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		−10	mA
Allowable Power Dissipation	P_d max	$T_a \leq 85°C$	300	mW
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C
Lead Temperature. Time	T_{sol}	10sec	+260	°C

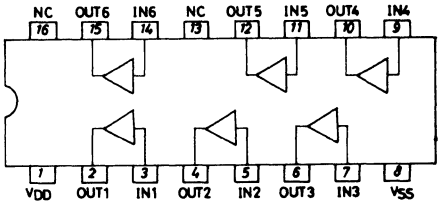
Allowable Operating Ranges/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

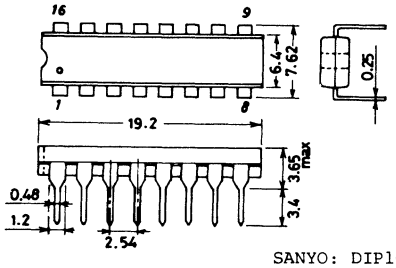
Equivalent Circuit (1/6 LC4050B)



Pin Assignment (Top View)



Case Outline 3006A-D16IC (unit: mm)



SANYO: DIP16

Electrical Characteristics/T_a=−40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_O=2.5V, V_{IN}=V_{DD}	−1.4			mA
		V_{DD}=10V, V_O=9.5V, 〃	−1.4			mA
		V_{DD}=15V, V_O=13.5V, 〃	−4.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}	3.5			mA
		V_{DD}=10V, V_O=0.5V, 〃	6.0			mA
		V_{DD}=15V, V_O=1.5V, 〃	26.0			mA
"H" Input Level Voltage	V_{IH}	V_{DD}=5V, V_O=4.5V, $\|I_{OUT}\|$<1μA	3.5			V
		V_{DD}=10V, V_O=9.0V, 〃	7.0			V
		V_{DD}=15V, V_O=13.5V, 〃	11.0			V
"L" Input Level Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V, $\|I_{OUT}\|$<1μA			1.5	V
		V_{DD}=10V, V_O=1.0V, 〃			3.0	V
		V_{DD}=15V, V_O=1.5V, 〃			4.0	V
"H" Input Level Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			0.3	μA
"L" Input Level Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			−0.3	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			4.0	μA
		V_{DD}=10V, 〃			8.0	μA
		V_{DD}=15V, 〃			16.0	μA

Electrical Characteristics/T_a=25°C±2°C, V_{SS}=0V			min	typ	max	unit
"H" Output Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}	4.95	5.50		V
		V_{DD} =10V 〃 〃	9.95	10.00		V
		V_{DD}=15V, 〃 〃	14.95	15.00		V
"L" Output Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}		0.00	0.05	V
		V_{DD}=10V, 〃 〃		0.00	0.05	V
		V_{DD}=15V, 〃 〃		0.00	0.05	V
"H" Output Level Current	I_{OH}	V_{DD}=5V, V_O=2.5V, V_{IN}=V_{DD}	−1.25	−2.5		mA
		V_{DD}=10V, V_O=9.5V, 〃	−1.25	−2.5		mA
		V_{DD}=15V, V_O=13.5V, 〃	−3.75	−10.0		mA
"L" Output Level Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}	3.2	6.0		mA
		V_{DD}=10V, V_O=0.5V, 〃	5.0	16.0		mA
		V_{DD}=15V, V_O=1.5V, 〃	24.0	40.0		mA
"H" Input Level Voltage	V_{IH}	V_{DD}=5V, V_O=4.5V, $\|I_{OUT}\|$<1μA	3.5	2.75		V
		V_{DD}=10V, V_O=9.0V, 〃	7.0	5.5		V
		V_{DD}=15V, V_O=13.5V, 〃	11.0	8.25		V
"L" Input Level Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V, $\|I_{OUT}\|$<1μA		2.25	1.5	V
		V_{DD}=10V, V_O=1.0V, 〃		4.5	3.0	V
		V_{DD}=15V, V_O=1.5V, 〃		6.75	4.0	V
"H" Input Level Current	I_{IH}	V_{DD}=18V, V_{IN}=18V		10^{-5}	0.3	μA
"L" Input Level Current	I_{IL}	V_{DD}=18V, V_{IN}=0V		-10^{-5}	−0.3	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.002	4.0	μA
		V_{DD}=10V, 〃		0.004	8.0	μA
		V_{DD}=15V, 〃		0.008	16.0	μA
Input Capacitacne	C_{IN}			5	7.5	pF

Electrical Characteristics/T_a=+85°C, V_{SS}=0V

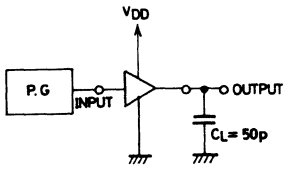
			min	typ	max	unit
"H" Output Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{DD}$	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Output Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{SS}$			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Output Level Current	I_{OH}	V_{DD}=5V, V_O=2.5V, $V_{IN}=V_{DD}$	−1.0			mA
		V_{DD}=10V, V_O=9.5V, 〃	−1.0			mA
		V_{DD}=15V, V_O=13.5V, 〃	−3.0			mA
"L" Output Level Current	I_{OL}	V_{DD}=5V, V_O=0.4V, $V_{IN}=V_{SS}$	2.5			mA
		V_{DD}=10V, V_O=0.5V, 〃	3.6			mA
		V_{DD}=15V, V_O=1.5V, 〃	18.0			mA
"H" Input Level Voltage	V_{IH}	V_{DD}=5V, V_O=4.5V, $\|I_{OUT}\|<1\mu A$	3.5			V
		V_{DD}=10V, V_O=9.0V, 〃	7.0			V
		V_{DD}=15V, V_O=13.5V, 〃	11.0			V
"L" Input Level Voltage	V_{IL}	V_{DD}=5V, V_O=0.5V, $\|I_{OUT}\|<1\mu A$			1.5	V
		V_{DD}=10V, V_O=1.0V, 〃			3.0	V
		V_{DD}=15V, V_O=1.5V, 〃			4.0	V
"H" Input Level Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			1.0	μA
"L" Input Level Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			−1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, $V_{IN}=V_{SS}$, V_{DD}			30	μA
		V_{DD}=10V, 〃			60	μA
		V_{DD}=15V, 〃			120	μA

Note) Current direction: +(no sign) Flowing into device
− Flowing out of device

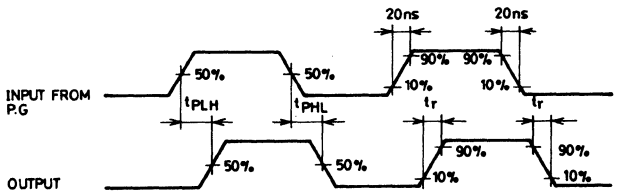
Switching Characteristics/T_a=25°C±2°C, C_L=50pF, V_{SS}=0V

			min	typ	max	unit
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Output Fall Time	t_{THL} (t_f)	V_{DD}=5V		50	100	ns
		V_{DD}=10V		25	50	ns
		V_{DD}=15V		20	40	ns
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		80	180	ns
		V_{DD}=10V		40	100	ns
		V_{DD}=15V		25	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		80	120	ns
		V_{DD}=10V		40	60	ns
		V_{DD}=15V		25	40	ns

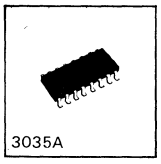
Test Circuit



Waveform



LC4050BM



C MOS IC

CMOS Logic B-Series Hex Buffer/Converter (Noninverting Type)

Ⓔ 1119A

The LC4050BM is a noninverting type Hex Buffer/Converter IC (equivalent to B series) having such features as wide operating voltage range, high noise margin, low power dissipation, etc. Its mini flat package enables compactness of sets.

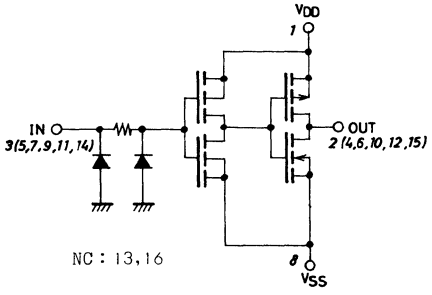
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum power supply voltage	V_{DD} max		V_{SS} −0.5~V_{SS} +20	V
Input voltage	V_{IN}		V_{SS} −0.5~V_{SS} +20	V
Input current	V_{IN}		−10	mA
Allowable power dissipation	P_d max	$T_a \leq 85°C$	150	mW
Operating temperature	T_{opg}		−40~+85	°C
Storage temperature	T_{stg}		−65~+150	°C
Lead temperature. time	T_{sol}	t=10sec	260	°C

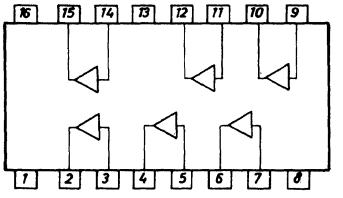
Allowable Operating ranges/T_a=−40°C to +85°C, V_{SS}=0V

			unit
Supply voltage	V_{DD}	3~18	V
Input voltage	V_{IN}	0~18	V

Equivalent Circuit (1/6 LC4050BM)

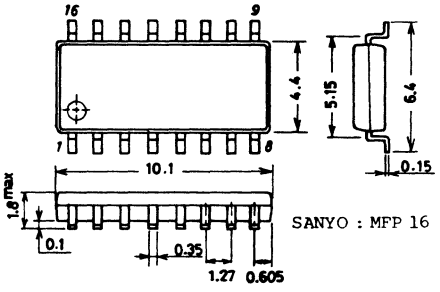


Pin Assignment



(Top View)

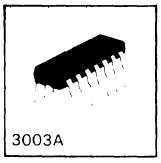
Case Outline 3035A-M16IC
(unit:mm)



SANYO : MFP 16

For details, refer to the description of the LC4050B.

LC4066B



C MOS IC

CMOS Logic B-Series Quad Bilatersl SWitch

Ⓔ 1009B

The LC4066B is a bilateral switch (also called analog switch) IC (meeting EIA/JEDEC standards) having such features as wide operating voltage range, high noise margin, low power dissipation, etc. It has 4 independent bilateral switches. Setting control input (CONT) at "H" level causes the switches to be conducting, thereby resulting in a low impedance between input and output; and setting control input (CONT) "L" level causes the switches to be nonconducting, thereby resulting in a high impedance between input and output.

On resistance (R on)	300Ω (typ):	V_{DD} = 5V
	110Ω (typ):	V_{DD} = 10V
	70Ω (typ):	V_{DD} = 15V
Off resistance (R off)	R off (typ) > 10^9 Ω	

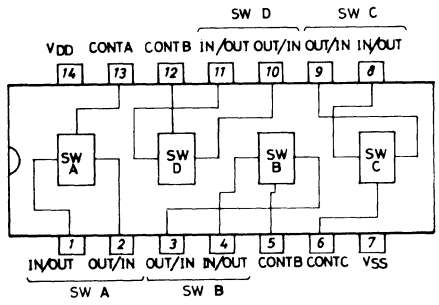
Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0 V

				unit
Maximum supply voltage	V_{DD} max		V_{SS} −0.5 ~ V_{SS} +20	V
Input voltage	V_{IN}		V_{SS} −0.5 ~ V_{DD} + 0.5	V
Output voltage	V_{OUT}		V_{SS} −0.5 ~ V_{DD} +0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	$T_a \leqq 85°C$, I_{IN}=±10 mA	300	mW
Operating temperature	T_{opg}		−40 ~ +85	°C
Storage temperature	T_{stg}		−65 ~ +150	°C
On-state voltage drop between input and output	V_I - V_O		±0.5	V
Lead temperature time	T_{sol}	t=10sec	260	°C

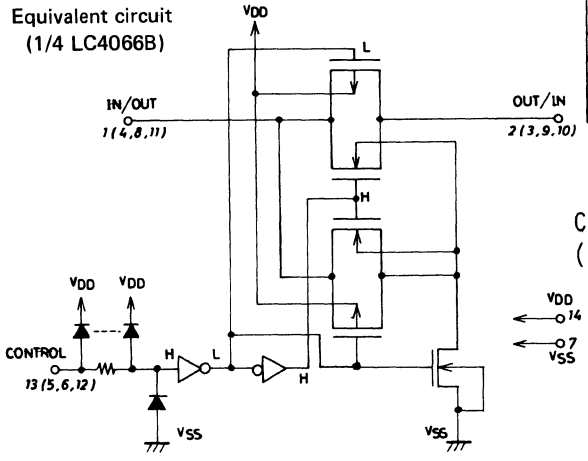
Allowable Operating Range/T_a = −40 ~ +85°C

			unit
Supply voltage	V_{DD}	3 ~ 18	V
Input voltage	V_{IN}	0 ~ V_{DD}	V

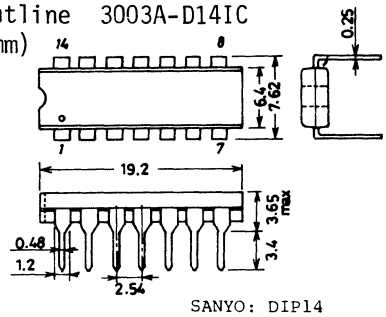
Pin assignment and block diagram



Equivalent circuit
(1/4 LC4066B)



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

			min	typ	max	unit
Electrical Characteristics/T_a = −40°C						
Input "H" level control voltage	V_{IH}	V_{DD}=5 V, Current between input and output=10 μA	3.5			V
		V_{DD}=10 V, Current between input and output=10 μA	7.0			V
		V_{DD}=15 V, Current between input and output=10 μA	11.0			V
Input "L" level control voltage	V_{IL}	V_{DD}=5 V, Current between input and output=10 μA			1.5	V
		V_{DD}=10 V, Current between input and output=10 μA			2.0	V
		V_{DD}=15 V, Current between input and output=10 μA			2.5	V
ON resistance	R_{ON}	V_{DD}=5 V,V_{IN}=5 V			500	Ω
		V_{DD}=5 V,V_{IN}=2.5 V			850	Ω
		V_{DD}=5 V,V_{IN}=0.25 V			500	Ω
		V_{DD}=10 V,V_{IN}=10 V			210	Ω
		V_{DD}=10 V,V_{IN}=5 V			210	Ω
		V_{DD}=10 V,V_{IN}=0.25 V			210	Ω
		V_{DD}=15 V,V_{IN}=15 V			140	Ω
		V_{DD}=15 V,V_{IN}=7.5 V			140	Ω
		V_{DD}=15 V,V_{IN}=0.25 V			140	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=5 V			210	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=±0.25 V			210	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=−5 V			210	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=7.5 V			140	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=±0.25 V			140	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=−7.5 V			140	Ω
Input/Output leak current (Switch off)	I_{OFF}	V_{DD}=18 V,V_{IN}=18 V,V_{out}=0 V			±250	nA
		V_{DD}=18 V,V_{IN}=0 V,V_{out}=18 V			±250	nA
Quiescent current dissipation	I_{DD}	V_{DD}=5 V,V_{IN}=V_{DD},V_{SS}			1.0	μA
		V_{DD}=10 V,V_{IN}=V_{DD},V_{SS}			2.0	μA
		V_{DD}=15 V,V_{IN}=V_{DD},V_{SS}			4.0	μA
Input "H" level control current	I_{IH}	V_{DD}=18 V,V_{IN}=18 V			0.3	μA
Input "L" level control current	I_{IL}	V_{DD}=18 V,V_{IN}=0 V			−0.3	μA

			min	typ	max	unit
Electrical characteristics/T_a = +25°C						
Input "H" level control voltage	V_{IH}	V_{DD}=5 V, Current between input and output=10 μA	3.5	2.75		V
		V_{DD}=10 V, Current between input and output=10 μA	7.0	5.5		V
		V_{DD}=15 V, Current between input and output=10 μA	11.0	8.25		V
Input "L" level control voltage	V_{IL}	V_{DD}=5 V, Current between input and output=10 μA		2.25	1.5	V
		V_{DD}=10 V, Current between input and output=10 μA		4.5	2.0	V
		V_{DD}=15 V, Current between input and output=10 μA		6.75	2.5	V
ON resistance	R_{ON}	V_{DD}=5 V,V_{IN}=5 V		200	600	Ω
		V_{DD}=5 V,V_{IN}=2.5 V		500	950	Ω
		V_{DD}=5 V,V_{IN}=0.25 V		150	600	Ω
		V_{DD}=10 V,V_{IN}=10 V		120	250	Ω
		V_{DD}=10 V,V_{IN}=5 V		100	250	Ω
		V_{DD}=10 V,V_{IN}=0.25 V		100	250	Ω
		V_{DD}=15 V,V_{IN}=15 V		90	160	Ω
		V_{DD}=15 V,V_{IN}=7.5 V		60	160	Ω
		V_{DD}=15 V,V_{IN}=0.25 V		60	160	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=5 V		120	250	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=±0.25 V		100	250	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=−5 V		100	250	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=7.5 V		90	160	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=±0.25 V		60	160	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=−7.5 V		60	160	Ω

			min	typ	max	unit
ON-state resistance between any 2 switches	R_{ON}	V_{DD}=2.5 V,V_{SS}=−2.5 V		30		Ω
		V_{DD}=5 V,V_{SS}=−5 V		15		Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V		10		Ω
Input/Output leak current (Switch off)	I_{OFF}	V_{DD}=10 V,V_{IN}=10 V,V_{out}=0 V		±0.01	±125	nA
		V_{DD}=10 V,V_{IN}=0 V,V_{out}=10 V		±0.01	±125	nA
		V_{DD}=18 V,V_{IN}=18 V,V_{out}=0 V		±0.1	±250	nA
		V_{DD}=18 V,V_{IN}=0 V,V_{out}=18 V		±0.1	±250	nA
Quiescent current dissipation	I_{DD}	V_{DD}=5 V,V_{IN}=V_{DD},V_{SS}		0.001	1.0	μA
		V_{DD}=10 V,V_{IN}=V_{DD},V_{SS}		0.001	2.0	μA
		V_{DD}=15 V,V_{IN}=V_{DD},V_{SS}		0.002	4.0	μA
Input "H" level control current	I_{IH}	V_{DD}=18 V,V_{IN}=18 V		10^{-5}	0.3	μA
Input "L" level control current	I_{IL}	V_{DD}=18 V,V_{IN}=0 V		-10^{-5}	−0.3	μA

Electrical characteristics/T_a = +85°C

			min	typ	max	unit
Input "H" level control voltage	V_{IH}	V_{DD}=5 V, Current between input and output=10 μA	3.5			V
		V_{DD}=10 V, Current between input and output=10 μA	7.0			V
		V_{DD}=15 V, Current between input and output=10 μA	11.0			V
Input "L" level control voltage	V_{IL}	V_{DD}=5 V, Current between input and output=10 μA			1.5	V
		V_{DD}=10 V, Current between input and output=10 μA			2.0	V
		V_{DD}=15 V, Current between input and output=10 μA			2.5	V
ON resistance	R_{ON}	V_{DD}=5 V,V_{IN}=5 V			800	Ω
		V_{DD}=5 V,V_{IN}=2.5 V			1300	Ω
		V_{DD}=5 V,V_{IN}=0.25 V			800	Ω
		V_{DD}=10 V,V_{IN}=10 V			300	Ω
		V_{DD}=10 V,V_{IN}=5 V			300	Ω
		V_{DD}=10 V,V_{IN}=0.25 V			300	Ω
		V_{DD}=15 V,V_{IN}=15 V			200	Ω
		V_{DD}=15 V,V_{IN}=7.5 V			200	Ω
		V_{DD}=15 V,V_{IN}=0.25 V			200	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=5 V			300	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=±0.25 V			300	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=−5 V			300	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=7.5 V			200	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=±0.25 V			200	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=−7.5 V			200	Ω
Input/Output leak current (Switch off)	I_{OFF}	V_{DD}=18 V,V_{IN}=18 V,V_{out}=0 V			±1000	nA
		V_{DD}=18 V,V_{IN}=0 V,V_{out}=18 V			±1000	nA
Quiescent current dissipation	I_{DD}	V_{DD}=5 V,V_{IN}=V_{DD},V_{SS}			7.5	μA
		V_{DD}=10 V,V_{IN}=V_{DD},V_{SS}			15	μA
		V_{DD}=15 V,V_{IN}=V_{DD},V_{SS}			30	μA
Input "H" level control current	I_{IH}	V_{DD}=18 V,V_{IN}=18 V			1.0	μA
Input "L" level control current	I_{IL}	V_{DD}=18 V,V_{IN}=0 V			−1.0	μA

Switching characteristics/T_a = 25°C±2°C

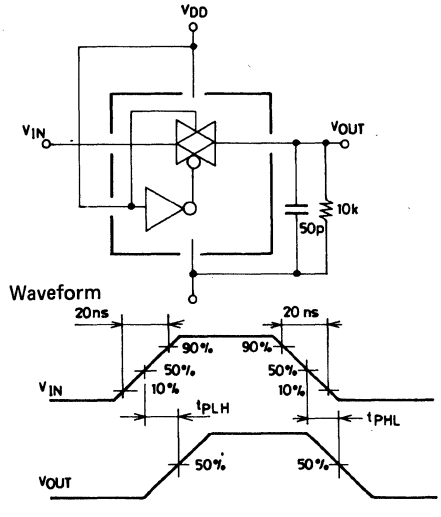
			min	typ	max	unit
Propagation delay time (Input-Output)	t_{PLH}	V_{DD}=5 V,R_L=10 kΩ,C_L=50 pF		15	45	ns
	t_{PHL}	V_{DD}=10 V,R_L=10 kΩ,C_L=50 pF		8	30	ns
		V_{DD}=15 V,R_L=10 kΩ,C_L=50 pF		5	20	ns
Propagation time (Control-Out)	t_{PLH}	V_{DD}=5 V,R_L=10 kΩ,C_L=50 pF		100	200	ns
	t_{PHL}	V_{DD}=10 V,R_L=10 kΩ,C_L=50 pF		40	70	ns
		V_{DD}=15 V,R_L=10 kΩ,C_L=50 pF		35	60	ns
Maximum control input frequency	f max (C)	V_{DD}=5 V,C_L=15 pF		3		MHz
		V_{DD}=10 V,C_L=15 pF		9		MHz
		V_{DD}=15 V,C_L=15 pF		11		MHz
Maximum propagation frequency	f max (I−0)	V_{DD}=5 V,V_{SS}=−5 V,R_L=10 kΩ, C_L=15 pF, *1		16		MHz

			min	typ	max	unit
Sine wave propagation distortion ratio		V_{DD}=5 V,V_{SS}=−5 V,R_L=10 kΩ, f=1 MHz, *2		0.1		%
Feed through (Switch off)		V_{DD}=5 V,V_{SS}=−5 V,R_L=10 kΩ, *3		*4		KHz
Crosstalk (Control-Out)		V_{DD}=5 V,R_{IN}=1 kΩ,R_{out}=10 kΩ, C_L=15 pF		*5		mV
		V_{DD}=10 V,R_{IN}=1 kΩ,R_{out}=10 kΩ, C_L=15 pF		*5		mV
		V_{DD}=15 V,R_{IN}=1 kΩ,R_{out}=10 kΩ, C_L=15 pF		*5		mV
Input capacitance	C_{IN}	Control input		5	7.5	pF
		Switch I/O		10		pF

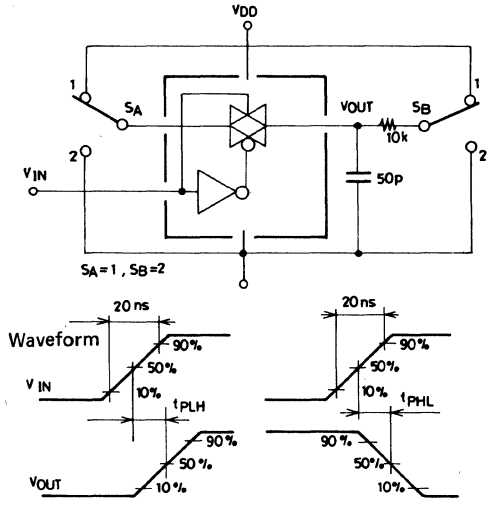
(Note) *1 Vis: ±2.5 Vp-p sine wave f max: 20 log (Vos/Vis)=−3 dB
*2 Vis: ±2.5 Vp-p sine wave
*3 Vis: ±2.5 Vp-p sine wave $f_{FEED\ THROUGH}$: 20 log (Vos/Vis)=−50 dB
*4, *5: To be determined for each user

Test Circuits and Waveforms

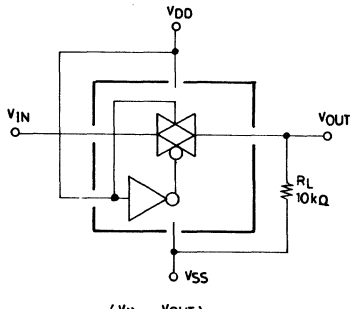
1. t_{PLH}, t_{PHL} (INT OUT) Test Circuit



2. t_{PLH}, t_{PHL} (CONTROL-OUT) Test Circuit

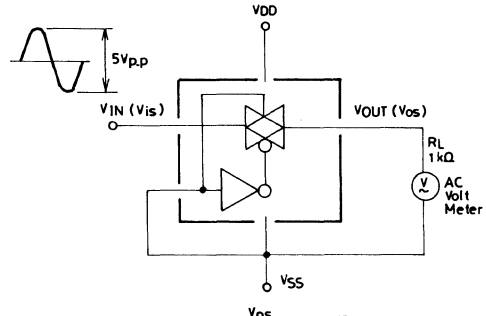


3. R_{ON} Test Circuit



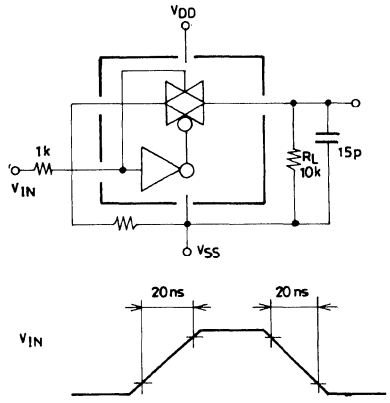
$$R_{ON} = \frac{(V_{IN} - V_{OUT})}{V_{OUT}} \times 10\ k\Omega$$

4. Feed Through (FEED THROUGH) Test Circuit

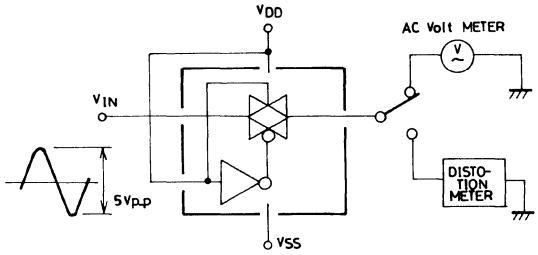


$$f : 20 \log 10 \frac{V_{os}}{V_{is}} = -50\,dB$$

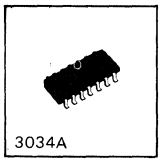
5. Crosstalk (CROSSTALK)



6. Frequency Response (f max) Distortion:
FREQUENCY RESPONCE



LC4066BM



C MOS IC

CMOS Logic B-Series Quad Bilateral Switch

Ⓔ 1118C

Uses

- C MOS standard logic IC for logic circuit
- Make/break of analog signal

Features, Functions

- Quad bilateral switch IC having wide operating voltage range, high noise margin, low power dissipation.
- Mini flat package enabling compactness of sets.

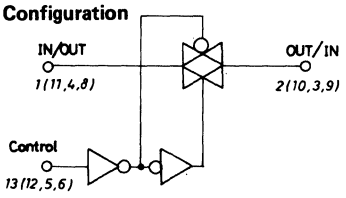
Absolute maximum ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum supply voltage	V_{DD} max		V_{SS}−0.5 to V_{SS}+20	V
Input voltage	V_{IN}		V_{SS}−0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}		V_{SS}−0.5 to V_{DD}+0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	$T_a \leq 85°C$	150	mW
Operating temperature	T_{opg}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C
Lead temperature. time	T_{sol}	t=10sec	260	°C

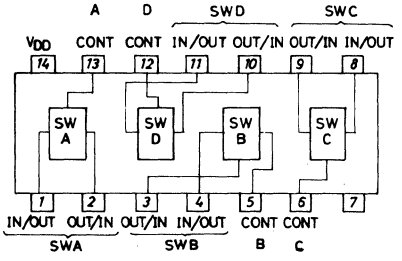
Allowable operating ranges/T_a=−40°C to +85°C

			unit
Supply voltage	V_{DD}	3 to 18	V
Input voltage	V_{IN}	0 to V_{DD}	V

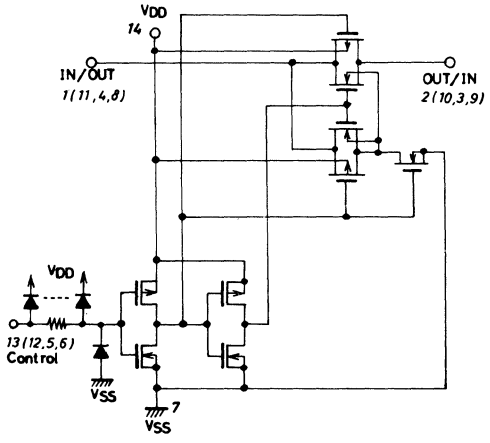
Circuit Configuration



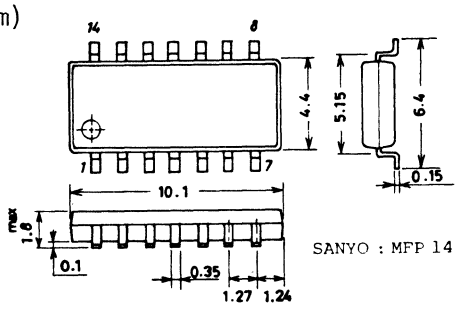
Pin Assignment



Equivalent Circuit (1/4 LC4066BM)



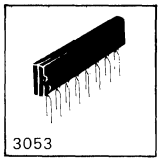
Case Outline 3034A-M14IC
(unit:mm)



SANYO : MFP 14

For details, refer to the description of the LC4066B.

LC4066BS



C MOS IC

CMOS Logic B-Series Quad Bilateral Switch

Ⓔ 1502

The LC4066BS is a bilaternal switch (also called analog switch) IC (meeting EIA/JEDEC standards) having such features as wide operating voltage range, high noise margin, low power disipation. It has 4 independent bilaternal switches. Setting control input (CONT) at "H" level causes the switches to be conducting, thereby resulting in a low impendence between input and output; and setting control input (CONT) at "L" level causes the switches to be nonconducting, thereby resulting in a high impedence between input and output.

On resistance (R on) 300ohm(typ) : V_{DD}=5V
110ohm(typ) : V_{DD}=10V
Off resistance (R off) R off (typ)>: 10 ohm

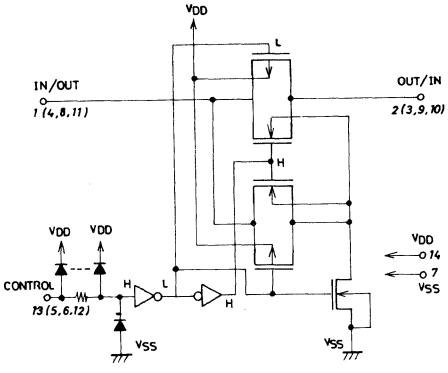
Absolute Maximum Ratings at T=25°C

				unit
Maximum Supply Voltage	V_{DD}max		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax	Ta≦85°C, I_{IN}=±10mA	150	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to -150	°C
On-State Voltage Drop between Input and Output	V_I-V_O		±0.5	V
Lead Temperature & Time	Tsol	t=10sec	260	°C

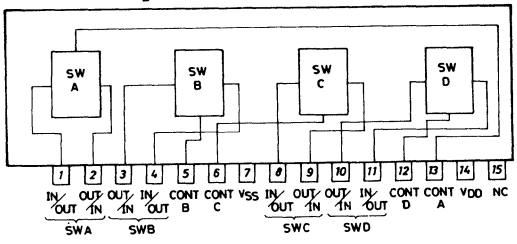
Allowable Operating Range at Ta=-40 to +85°C

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

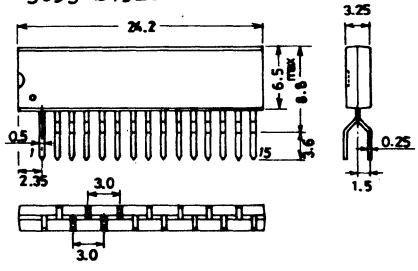
Equivalent Circuit
(1/4 LC4066BS)



Pin Assignment and Equivalent Circuit Block Diagram

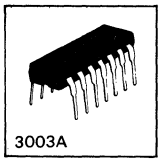


Case Outline 3053-S15IC
(unit:mm)



For details, refer to the description of the LC4066B.

LC4066BH



C MOS IC

CMOS Logic B-Series Quad Bilateral Switch

Ⓔ 1541

The LC4066BH is a bilateral switch (also called analog switch) IC (meeting EIA/JEDEC standards) having such features as wide operating voltage range, high noise margin, low power dissipation, etc. It has 4 independent bilateral switches. Setting control input (CONT) at "H" level causes the switches to be conducting, thereby resulting in a low impedance between input and output; and setting control input (CONT) at "L" level causes the switches to be nonconducting, thereby resulting in a high impedance between input and output.

On resistance (R on)	300Ω (typ):	V_{DD} = 5V
	110Ω (typ):	V_{DD} = 10V
	70Ω (typ):	V_{DD} = 15V
Off resistance (R off)	R off (typ) > 10^9 Ω	

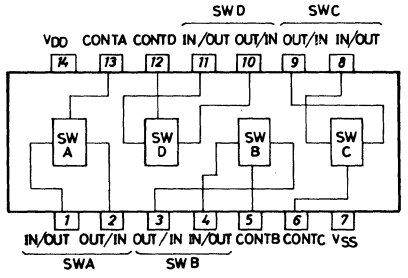
Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0 V

				unit
Maximum supply voltage	V_{DD} max		V_{SS} −0.3 to V_{SS} +25	V
Input voltage	V_{IN}		V_{SS} −0.3 to V_{SS} +0.3	V
Output voltage	V_{OUT}		V_{SS} −0.3 to V_{SS} +0.3	V
On-state voltage drop between input and output	V_I - V_O		±0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	$T_a \leq 85°C$	300	mW
Operating temperature	T_{opg}		−40 ~ +85	°C
Storage temperature	T_{stg}		−65 ~ +150	°C
Lead temperature·time	T_{sol}	t=10sec	260	°C

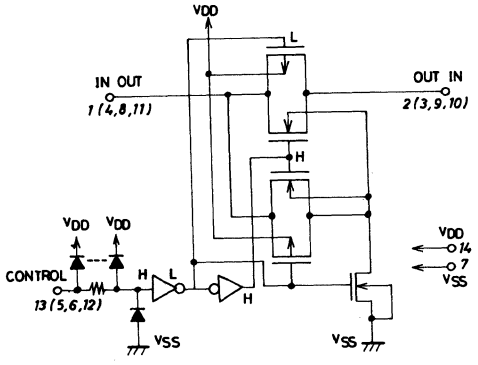
Allowable Operating Range/T_a = −40 ~ +85°C

			unit
Supply voltage	V_{DD}	3 ~ 23	V
Input voltage	V_{IN}	0 ~ V_{DD}	V

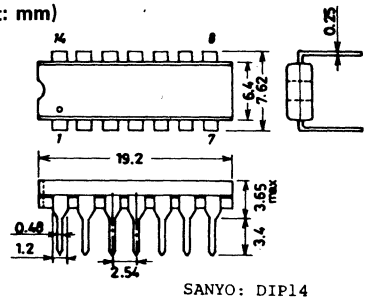
Pin Assignment and Equivalent Circuit Block Diagram



Equivalent Circuit
(1/4 LC4066BH)



Case Outline 3003A-D14IC
(unit: mm)



SANYO: DIP14

			min	typ	max	unit
Electrical Characteristics/T_a = −40°C, V_{DD}=3 to 18 V						
Input "H" level control voltage	V_{IH}	V_{DD}=5 V, Current between input and output=10 μA	3.5			V
		V_{DD}=10 V, Current between input and output=10 μA	7.0			V
		V_{DD}=15 V, Current between input and output=10 μA	11.0			V
Input "L" level control voltage	V_{IL}	V_{DD}=5 V, Current between input and output=10 μA			1.5	V
		V_{DD}=10 V, Current between input and output=10 μA			2.0	V
		V_{DD}=15 V, Current between input and output=10 μA			2.5	V
ON resistance	R_{ON}	V_{DD}=5 V,V_{IN}=5 V			500	Ω
		V_{DD}=5 V,V_{IN}=2.5 V			850	Ω
		V_{DD}=5 V,V_{IN}=0.25 V			500	Ω
		V_{DD}=10 V,V_{IN}=10 V			210	Ω
		V_{DD}=10 V,V_{IN}=5 V			210	Ω
		V_{DD}=10 V,V_{IN}=0.25 V			210	Ω
		V_{DD}=15 V,V_{IN}=15 V			140	Ω
		V_{DD}=15 V,V_{IN}=7.5 V			140	Ω
		V_{DD}=15 V,V_{IN}=0.25 V			140	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=5 V			210	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=±0.25 V			210	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=−5 V			210	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=7.5 V			140	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=±0.25 V			140	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=−7.5 V			140	Ω
Input/Output leak current (Switch off)	I_{OFF}	V_{DD}=18 V,V_{IN}=18 V,V_{OUT}=0 V			±250	nA
		V_{DD}=18 V,V_{IN}=0 V,V_{OUT}=18 V			±250	nA
Quiescent current dissipation	I_{DD}	V_{DD}=5 V,V_{IN}=V_{DD},V_{SS}			1.0	μA
		V_{DD}=10 V,V_{IN}=V_{DD},V_{SS}			2.0	μA
		V_{DD}=15 V,V_{IN}=V_{DD},V_{SS}			4.0	μA
Input "H" level control current	I_{IH}	V_{DD}=18 V,V_{IN}=18 V			0.3	μA
Input "L" level control current	I_{IL}	V_{DD}=18 V,V_{IN}=0 V			−0.3	μA

			min	typ	max	unit
Electrical characteristics/T_a = +25°C, V_{DD}=3 to 18 V						
Input "H" level control voltage	V_{IH}	V_{DD}=5 V, Current between input and output=10 μA	3.5	2.75		V
		V_{DD}=10 V, Current between input and output=10 μA	7.0	5.5		V
		V_{DD}=15 V, Current between input and output=10 μA	11.0	8.25		V
Input "L" level control voltage	V_{IL}	V_{DD}=5 V, Current between input and output=10 μA		2.25	1.5	V
		V_{DD}=10 V, Current between input and output=10 μA		4.5	2.0	V
		V_{DD}=15 V, Current between input and output=10 μA		6.75	2.5	V
ON resistance	R_{ON}	V_{DD}=5 V,V_{IN}=5 V		200	600	Ω
		V_{DD}=5 V,V_{IN}=2.5 V		500	950	Ω
		V_{DD}=5 V,V_{IN}=0.25 V		150	600	Ω
		V_{DD}=10 V,V_{IN}=10 V		120	250	Ω
		V_{DD}=10 V,V_{IN}=5 V		100	250	Ω
		V_{DD}=10 V,V_{IN}=0.25 V		100	250	Ω
		V_{DD}=15 V,V_{IN}=15 V		90	160	Ω
		V_{DD}=15 V,V_{IN}=7.5 V		60	160	Ω
		V_{DD}=15 V,V_{IN}=0.25 V		60	160	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=5 V		120	250	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=±0.25 V		100	250	Ω
		V_{DD}=5 V,V_{SS}=−5 V,V_{IN}=−5 V		100	250	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=7.5 V		90	160	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=±0.25 V		60	160	Ω
		V_{DD}=7.5 V,V_{SS}=−7.5 V,V_{IN}=−7.5 V		60	160	Ω

			min	typ	max	unit
ON-state resistance between any 2 switches	ΔR_{ON}	V_{DD}=2.5 V, V_{SS}=−2.5 V		30		Ω
		V_{DD}=5 V, V_{SS}=−5 V		15		Ω
		V_{DD}=7.5 V, V_{SS}=−7.5 V		10		Ω
Input/Output leak current (Switch off)	I_{OFF}	V_{DD}=10 V, V_{IN}=10 V, V_{OUT}=0 V		±0.01	±125	nA
		V_{DD}=10 V, V_{IN}=0 V, V_{OUT}=10 V		±0.01	±125	nA
		V_{DD}=18 V, V_{IN}=18 V, V_{OUT}=0 V		±0.1	±250	nA
		V_{DD}=18 V, V_{IN}=0 V, V_{OUT}=18 V		±0.1	±250	nA
Quiescent current dissipation	I_{DD}	V_{DD}=5 V, V_{IN}=V_{DD}, V_{SS}		0.001	1.0	μA
		V_{DD}=10 V, V_{IN}=V_{DD}, V_{SS}		0.001	2.0	μA
		V_{DD}=15 V, V_{IN}=V_{DD}, V_{SS}		0.002	4.0	μA
Input "H" level control current	I_{IH}	V_{DD}=18 V, V_{IN}=18 V		10^{-5}	0.3	μA
Input "L" level control current	I_{IL}	V_{DD}=18 V, V_{IN}=0 V		-10^{-5}	−0.3	μA

Electrical characteristics/T_a = +85°C, V_{DD}=3 to 18 V

			min	typ	max	unit
Input "H" level control voltage	V_{IH}	V_{DD}=5 V, Current between input and output=10 μA	3.5			V
		V_{DD}=10 V, Current between input and output=10 μA	7.0			V
		V_{DD}=15 V, Current between input and output=10 μA	11.0			V
Input "L" level control voltage	V_{IL}	V_{DD}=5 V, Current between input and output=10 μA			1.5	V
		V_{DD}=10 V, Current between input and output=10 μA			2.0	V
		V_{DD}=15 V, Current between input and output=10 μA			2.5	V
ON resistance	R_{ON}	V_{DD}=5 V, V_{IN}=5 V			800	Ω
		V_{DD}=5 V, V_{IN}=2.5 V			1300	Ω
		V_{DD}=5 V, V_{IN}=0.25 V			800	Ω
		V_{DD}=10 V, V_{IN}=10 V			300	Ω
		V_{DD}=10 V, V_{IN}=5 V			300	Ω
		V_{DD}=10 V, V_{IN}=0.25 V			300	Ω
		V_{DD}=15 V, V_{IN}=15 V			200	Ω
		V_{DD}=15 V, V_{IN}=7.5 V			200	Ω
		V_{DD}=15 V, V_{IN}=0.25 V			200	Ω
		V_{DD}=5 V, V_{SS}=−5 V, V_{IN}=5 V			300	Ω
		V_{DD}=5 V, V_{SS}=−5 V, V_{IN}=±0.25 V			300	Ω
		V_{DD}=5 V, V_{SS}=−5 V, V_{IN}=−5 V			300	Ω
		V_{DD}=7.5 V, V_{SS}=−7.5 V, V_{IN}=7.5 V			200	Ω
		V_{DD}=7.5 V, V_{SS}=−7.5 V, V_{IN}=±0.25 V			200	Ω
		V_{DD}=7.5 V, V_{SS}=−7.5 V, V_{IN}=−7.5 V			200	Ω
Input/Output leak current (Switch off)	I_{OFF}	V_{DD}=18 V, V_{IN}=18 V, V_{OUT}=0 V			±1000	nA
		V_{DD}=18 V, V_{IN}=0 V, V_{OUT}=18 V			±1000	nA
Quiescent current dissipation	I_{DD}	V_{DD}=5 V, V_{IN}=V_{DD}, V_{SS}			7.5	μA
		V_{DD}=10 V, V_{IN}=V_{DD}, V_{SS}			15	μA
		V_{DD}=15 V, V_{IN}=V_{DD}, V_{SS}			30	μA
Input "H" level control current	I_{IH}	V_{DD}=18 V, V_{IN}=18 V			10	μA
Input "L" level control current	I_{IL}	V_{DD}=18 V, V_{IN}=0 V			−10	μA

Current direction; + (no sign) : Flowing into device, − : Flowing out of device

Switching characteristics/T_a = 25°C±2°C

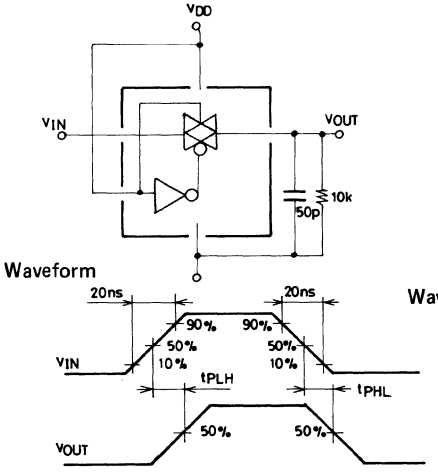
			min	typ	max	unit
Propagation delay time (Input-Output)	t_{PLH}	V_{DD}=5 V, R_L=10 kΩ, C_L=50 pF		15	45	ns
	t_{PHL}	V_{DD}=10 V, R_L=10 kΩ, C_L=50 pF		8	30	ns
		V_{DD}=15 V, R_L=10 kΩ, C_L=50 pF		5	20	ns
Propagation delay time (Control-Out)	t_{PLH}	V_{DD}=5 V, R_L=10 kΩ, C_L=50 pF		100	200	ns
	t_{PHL}	V_{DD}=10 V, R_L=10 kΩ, C_L=50 pF		40	70	ns
		V_{DD}=15 V, R_L=10 kΩ, C_L=50 pF		35	60	ns
Maximum control input frequency	f max (C)	V_{DD}=5 V, C_L=15 pF		3		MHz
		V_{DD}=10 V, C_L=15 pF		9		MHz
		V_{DD}=15 V, C_L=15 pF		11		MHz
Maximum propagation frequency	f max (I−O)	V_{DD}=5 V, V_{SS}=−5 V, R_L=10 kΩ, C_L=15 pF, *1		16		MHz

			min	typ	max	unit
Sine wave propagation distortion ratio		V_{DD}=5 V, V_{SS}=−5 V, R_L=10 kΩ, f=1 MHz, *2		0.1		%
Feed through (Switch off)		V_{DD}=5 V, V_{SS}=−5 V, R_L=10 kΩ, *3		*4		KHz
Crosstalk (Control-Out)		V_{DD}=5 V, R_{IN}=1 kΩ, R_{OUT}=10 kΩ, C_L=15 pF		*5		mV
		V_{DD}=10 V, R_{IN}=1 kΩ, R_{OUT}=10 kΩ, C_L=15 pF		*5		mV
		V_{DD}=15 V, R_{IN}=1 kΩ, R_{OUT}=10 kΩ, C_L=15 pF		*5		mV
Input capacitance	C_{IN}	Control input		5	7.5	pF
		Switch I/O		10		pF

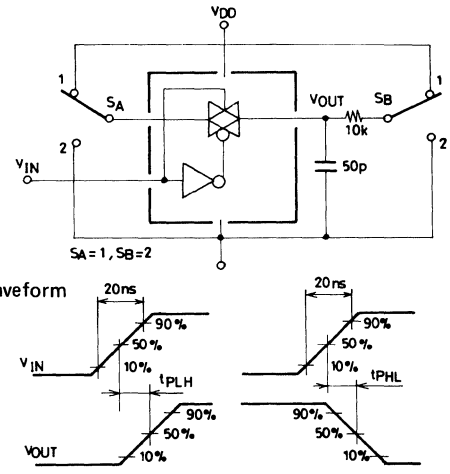
(Note) *1 Vis: ±2.5 Vp-p sine wave f max: 20 log (Vos/Vis)=−3 dB
*2 Vis: ±2.5 Vp-p sine wave
*3 Vis: ±2.5 Vp-p sine wave $f_{FEED\ THROUGH}$: 20 log (Vos/Vis)=−50 dB
*4, *5: To be determined for each user

Test Circuits and Waveforms

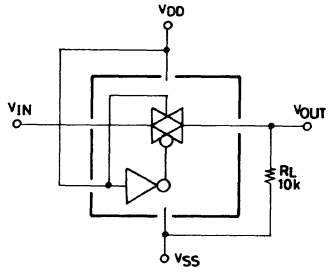
1. t_{PLH}, t_{PHL} (INT-OUT) Test Circuit



2. t_{PLH}, t_{PHL} (CONTROL-OUT) Test Circuit

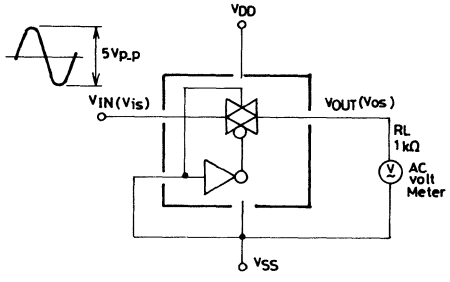


3. R_{ON} Test Circuit



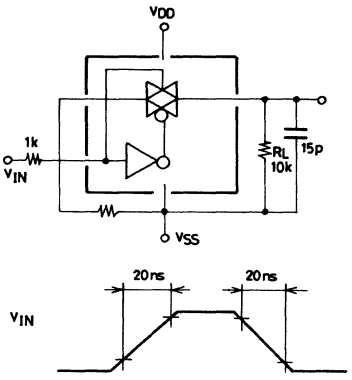
$$R_{ON} = \frac{(V_{IN} - V_{OUT})}{V_{OUT}} \times 10\ k\Omega$$

4. Feed Through (FEED THROUGH) Test Circuit

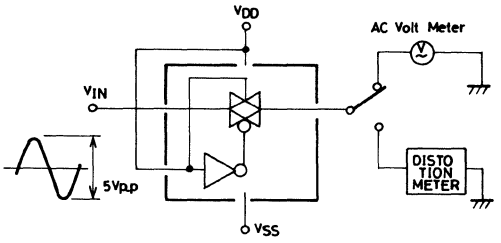


$$f : 20 \log 10 \frac{V_{os}}{V_{is}} = -50\,dB$$

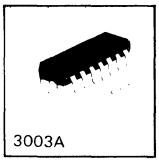
5. Crosstalk (CROSSTALK)



6. Frequency Response (f max) Distortion:
FREQUENCY RESPONCE



LC4069UB



C-MOS IC

CMOS Logic B-Series Hex Inverter

Ⓔ 877C

The LC4069UB is an IC that consists of six independent inverters (EIA/JEDEC standards-met IC product) having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

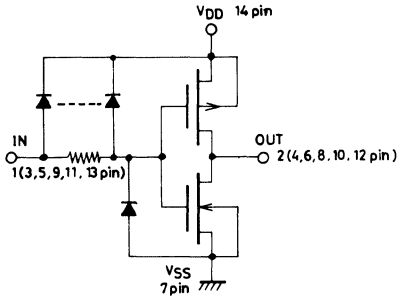
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax	Ta≦85°C	300	mW
Lead Temperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{stg}		-40 to +85	°C
Storage Temperature	T_{opg}		-65 to +150	°C

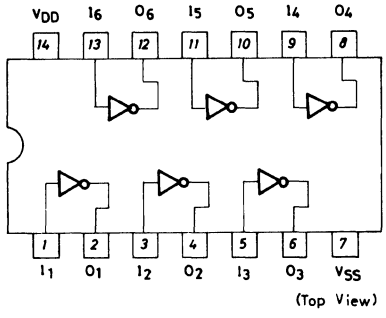
Allowable Operating Range at Ta=-40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

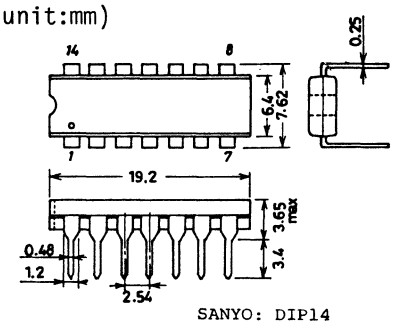
Equivalent Circuit (1/6 LC4069UB)



Pin Assignment and Block Diagram



Case Outline 3003A-D14IC (unit:mm)



SANYO: DIP14

Electrical Characteristics at Ta=-40°C, V_{SS}=0V			min	typ	max	unit
Output "H"-Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V " "	14.95			V
Output "L"-Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V,			0.05	V
Output "H"-Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	-0.61			mA
		V_{DD}=10V, V_{OH}=9.5V, V_{IN}=V_{SS}	-1.5			mA
		V_{DD}=15V, V_o=13.5V, "	-4			mA
Output "L"-Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.61			mA
		V_{DD}=10V, V_o=0.5V, "	1.5			mA
		V_{DD}=15V, V_o=1.5V, "	4			mA
Input "H"-Level Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1uA	4			V
		V_{DD}=10V, V_o=1.0, "	8			V
		V_{DD}=15V, V_o=1.5V, "	12.5			V
Input "L"-Level Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$< 1uA			1.0	V
		V_{DD}=10V, V_o=9.0V, "			2.0	V
		V_{DD}=15V, V_o=13.5V, "			2.5	V
Input Current	I_{IN}	V_{DD}=18V			±1.0	uA
Quiescent Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}*			0.25	uA
Dissipation		V_{DD}=10V, "			0.5	uA
		V_{DD}=15V, "			1.0	uA

*: All input pins connected.

Electrical Characteristics at Ta=25°C, V_{SS}=0V			min	typ	max	unit
Output "H"-Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
Output "L"-Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
Output "H"-Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	-0.51	-1.0		mA
		V_{DD}=10V, V_o=9.5V, "	-1.3	-2.6		mA
		V_{DD}=15V, V_o=13.5V, "	-3.4	-6.8		mA
Output "L"-Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.51	1.0		mA
		V_{DD}=10V, V_o=0.5V, "	1.3	2.6		mA
		V_{DD}=15V, V_o=1.5V, "	3.4	6.8		mA
Input "H"-Level Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1uA	4			V
		V_{DD}=10V, V_o=1.0V "	8			V
		V_{DD}=15V, V_o=1.5V "	12.5			V
Input "L"-Level Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1uA			1.0	V
		V_{DD}=10V, V_o=9.0V, "			2.0	V
		V_{DD}=15V, V_o=13.5V, "			2.5	V
Input Current	I_{IN}	V_{DD}=18V		$\pm10^{-5}$	±1.0	uA
Quiescent Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}*		0.01	0.25	uA
Dissipation		V_{DD}=10V, "		0.01	0.5	uA
		V_{DD}=15V, "		0.01	1.0	uA
Input Capacitance	C_{IN}			7.5	15	pF

*: All input pins connected.

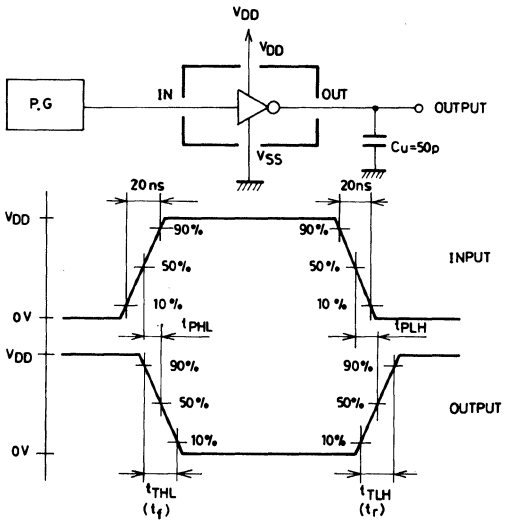
Electrical Characteristics at Ta=85°C, V_{SS}=0V			min	typ	max	unit
Output "H"-Level Voltage	V_{OH}	V_{DD}=5V, $\lvert I_{OUT}\rvert$<1uA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
Output "L"-Level Voltage	V_{OL}	V_{DD}=5V, $\lvert I_{OUT}\rvert$<1uA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
Output "H"-Level Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}	-0.36			mA
		V_{DD}=10V, V_O=9.5V, "	-0.9			mA
		V_{DD}=15V, V_O=13.5V, "	-2.4			mA
Output "L"-Level Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{DD}	0.36			mA
		V_{DD}=10V, V_O=0.5V, "	0.9			mA
		V_{DD}=15V, V_O=1.5V, "	2.4			mA
Input "H"-Level Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V, $\lvert I_{OUT}\rvert$<1uA	4			V
		V_{DD}=10V, V_O=1.0V, "	8			V
		V_{DD}=15V, V_O=1.5V, "	12.5			V
Input "L"-Level Voltage	V_{IL}	V_{DD}=5V, V_O=4.5V, $\lvert I_{OUT}\rvert$<1uA			1.0	V
		V_{DD}=10V, V_O=9.0V, "			2.0	V
		V_{DD}=15V, V_O=13.5V, "			2.5	V
Input Current	I_{IN}	V_{DD}=18V			±1.0	uA
Quiescent Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}*			7.5	uA
Dissipation		V_{DD}=10V, "			15	uA
		V_{DD}=15V, "			30	uA
Input Capacitance						

*: All input pins connected

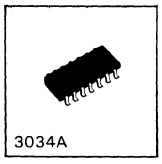
Note) Current direction (+, no sign: Flowing into device, -: Flowing out of device)

Switching Characteristics at Ta=25±2°C, C_u=50pF, V_{SS}=0V			min	typ	max	unit
"H"-Level Propagation delay Time	t_{PLH}	V_{DD}=5V		100	180	ns
		V_{DD}=10V		60	120	ns
		V_{DD}=15V		50	100	ns
"L"-Level Propagation delay Time	t_{PHL}	V_{DD}=5V		75	150	ns
		V_{DD}=10V		40	100	ns
		V_{DD}=15V		35	80	ns
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_{YHL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching Time Test Circuit and Waveforms



LC4069UBM



C MOS IC

CMOS Logic B-Series Hex Inverter

Ⓔ 1122A

The LC4069UBM is a hex inverter (EIA/JEDEC standards-met IC product) having such features as wide operating voltage range, high noise margin, low power dissipation. The use of mini flat package enables compactness of sets.

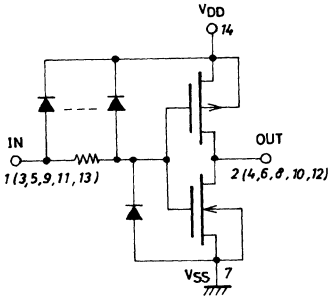
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		V_{SS} −0.5 ~ V_{SS} +20	V
Input Voltage	V_{IN}		V_{SS} −0.5 ~ V_{DD} +0.5	V
Output Voltage	V_{OUT}		V_{SS} −0.5 ~ V_{DD} +0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$Ta \leq 85°C$	150	mW
Operating Temperature	T_{opg}		−40 ~ +85	°C
Storage Temperature	T_{stg}		−65 ~ +150	°C
Lead Temperature . Time	T_{sol}	t=10 sec	260	°C

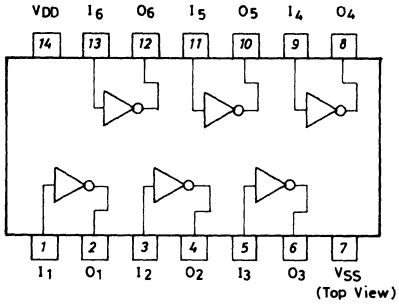
Allowable Power Dissipation/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 ~ 18	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V

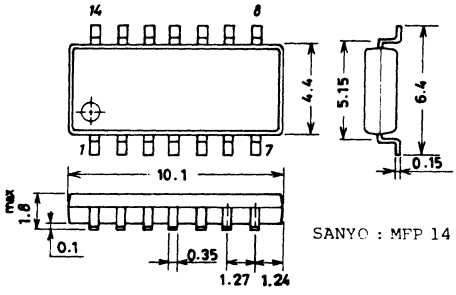
Equivalent Circuit (1/6 LC4069UBM)



Pin Assignment and Block Diagram

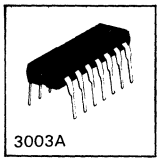


Case Outline 3034A-M14IC
(unit:mm)



For details, refer to the description of the LC4069UB.

LC4070B



C MOS IC

CMOS Logic B-Series
Quad 2 Input Exclusive-OR Gate

Ⓔ 1503

The LC4070B is a quad 2-input Exclusive-OR Gate IC (equivalent to B series) having such features as wide operating voltage range, high noise margin, low power dissipation.

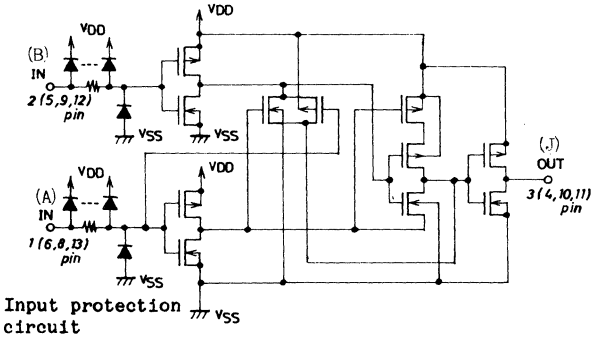
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD} max		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax		300	mW
Lead Temperature and Time	Tsol	t=10sec	260	°C
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

Allowable Operating Range at Ta=-40 to +85°C

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Equivalent Circuit(1/4 LC4070B)



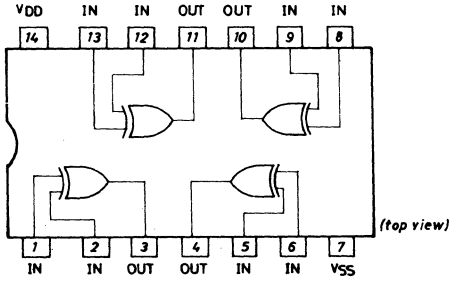
Truth Table

1 of 4 Gates

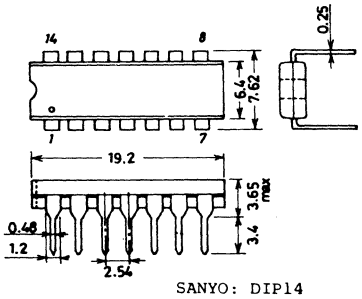
A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1=HIGH LEVEL
0=LOW LEVEL
J=A ⊕ B

Pin Assignment



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

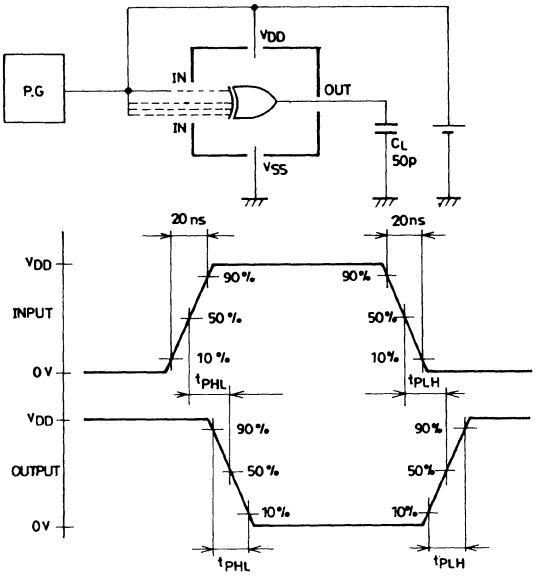
Electrical Characteristics at Ta=-40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS},V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS},V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS},V_{DD}	-0.52			mA
		V_{DD}=10V, Vo=9.5V, "	-1.3			mA
		V_{DD}=15V, Vo=13.5V, "	-3.6			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{SS},V_{DD}	0.52			mA
		V_{DD}=10V, Vo=0.5V, "	1.3			mA
		V_{DD}=15V, Vo=13.5V, "	3.6			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0			V
		V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, Vo=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V, Vo=1.5Vor13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V			0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V			-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, Vin=V_{SS},V_{DD}			1.0	uA
		V_{DD}=10V, "			2.0	uA
		V_{DD}=15V, "			4.0	uA

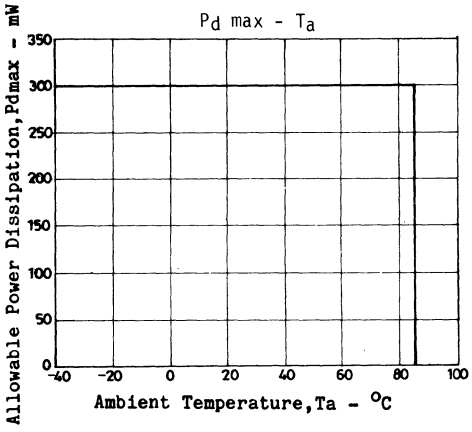
Electrical Characteristics at Ta=25°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS},V_{DD}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10.00		V
		V_{DD}=15V, " "	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS},V_{DD}		0.00	0.05	V
		V_{DD}=10V, " "		0.00	0.05	V
		V_{DD}=15V, " "		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS},V_{DD}	-0.44	-0.88		mA
		V_{DD}=10V, Vo=9.5V, "	-1.1	-2.25		mA
		V_{DD}=15V, Vo=13.5V, "	-3.0	-8.8		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{SS},V_{DD}	0.44	0.88		mA
		V_{DD}=10V, Vo=0.5V, "	1.1	2.25		mA
		V_{DD}=15V, Vo=13.5V, "	3.0	8.8		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA	3.5	2.75		V
		V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0	5.5		V
		V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0	8.25		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA		2.25	1.5	V
		V_{DD}=10V, Vo=1.0Vor9.0V, "		4.5	3.0	V
		V_{DD}=15V, Vo=1.5Vor13.5V, "		6.75	4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V		10^{-5}	0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V		-10^{-5}	-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, Vin=V_{SS},V_{DD}		0.001	1.0	uA
		V_{DD}=10V, "		0.001	2.0	uA
		V_{DD}=15V, "		0.002	4.0	uA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at $Ta=85^{o}C, V_{SS}=0V$			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1uA, Vin=V_{SS}, V_{DD}$	4.95			V
		$V_{DD}=10V,$ " "	9.95			V
		$V_{DD}=15V,$ " "	14.95			V
"L" Level Output Voltage	V_{OL}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1uA, Vin=V_{SS}, V_{DD}$			0.05	V
		$V_{DD}=10V,$ " "			0.05	V
		$V_{DD}=15V,$ " "			0.05	V
"H" Level Output Current	I_{OH}	$V_{DD}=5V, Vo=4.6V, Vin=V_{SS}, V_{DD}$	-0.36			mA
		$V_{DD}=10V, Vo=9.5V,$ "	-0.9			mA
		$V_{DD}=15V, Vo=13.5V,$ "	-2.4			mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, Vo=0.4V, Vin=V_{SS}, V_{DD}$	0.36			mA
		$V_{DD}=10V, Vo=0.5V,$ "	0.9			mA
		$V_{DD}=15V, Vo=13.5V,$ "	2.4			mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, Vo=0.5Vor4.5V, \lvert I_{OUT}\rvert<1uA$	3.5			V
		$V_{DD}=10V, Vo=1.0Vor9.0V,$ "	7.0			V
		$V_{DD}=15V, Vo=1.5Vor13.5V,$ "	11.0			V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, Vo=0.5Vor4.5V, \lvert I_{OUT}\rvert<1uA$			1.5	V
		$V_{DD}=10V, Vo=1.0Vor9.0V,$ "			3.0	V
		$V_{DD}=15V, Vo=1.5Vor13.5V,$ "			4.0	V
"H" Level Input Current	I_{IH}	$V_{DD}=18V, Vin=18V$			1.0	uA
"L" Level Input Current	I_{IL}	$V_{DD}=18V, Vin=0V$			-1.0	uA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, Vin=V_{SS}, V_{DD}$			7.5	uA
		$V_{DD}=10V,$ "			15.0	uA
		$V_{DD}=15V,$ "			30.0	uA

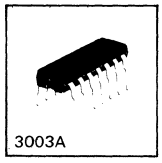
Switching Characteristics at $Ta=25\pm2^{o}C, V_{SS}=0V, C_L=50pF$			min	typ	max	unit
Output Rise Time	t_r (t_{TLH})	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
Output Fall Time	t_f (t_{THL})	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
"H" Level Propagation Delay Time	t_{PLH}	$V_{DD}=5V$		175	350	ns
		$V_{DD}=10V$		75	150	ns
		$V_{DD}=15V$		50	100	ns
"L" Level Propagation Delay Time	t_{PHL}	$V_{DD}=5V$		175	350	ns
		$V_{DD}=10V$		75	150	ns
		$V_{DD}=15V$		50	100	ns

Switching Time Test Circuit and Waveform





LC4071B



C MOS IC

C MOS Logic B-Series Quad 2-Input OR Gate

Ⓔ 859B

The LC4071B is a 2-input OR logic IC —— B series ——. having such features as wide operating range, high noise margin, low power dissipation, etc.

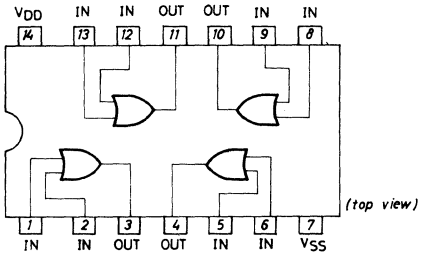
Absolute Maximum Ratings at T_a=25±2°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_dmax	T_a≦85°C, I_{IN}=±10mA	300	mW
Lead Temperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

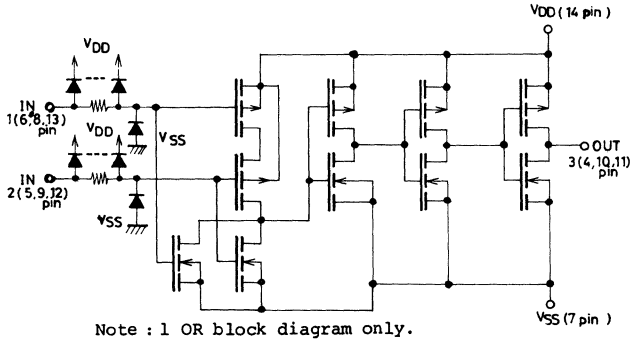
Allowable Operating Range at T_a=-40 to +85°C, V_{SS}=0V

Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Pin Assignment

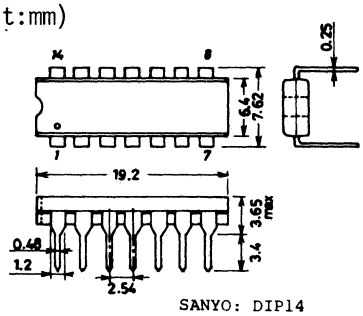


Equivalent Circuit



Note : 1 OR block diagram only.

Case Outline 3003A-D14IC (unit:mm)



SANYO: DIP14

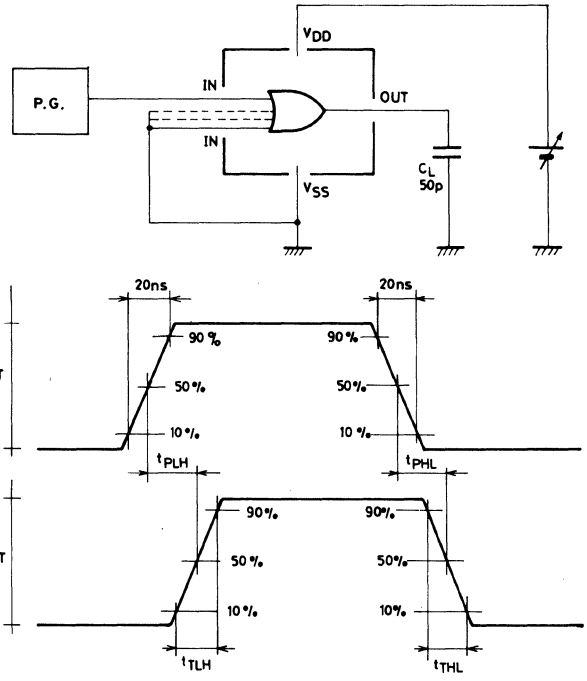
Electrical Characteristics at T_a=25±2°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5	-1.0		mA
		V_{DD}=10V, V_o=9.5V, "	-1.0	-2.0		mA
		V_{DD}=15V, V_o=13.5V, "	-3.5	-7.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}	0.5	1.0		mA
		V_{DD}=10V, V_o=0.5V, "	1.0	2.0		mA
		V_{DD}=15V, V_o=1.5V "	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1uA	3.5	2.5		V
		V_{DD}=10V, V_o=9.0V, "	7.0	5.0		V
		V_{DD}=15V, V_o=13.5V, "	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5Vor4.5V, $\|I_{OUT}\|$<1uA		2.5	1.5	V
		V_{DD}=10V, V_o=1.0or9.0V, "		5.0	3.0	V
		V_{DD}=15V, V_o=1.5or13.5V, "		7.5	4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V		10^{-5}	1.0	uA
		V_{DD}=18V, V_{IN}=0V		-10^{-5}	-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.01	1.0	uA
		V_{DD}=10V, "		0.01	2.0	uA
		V_{DD}=15V, "		0.01	4.0	uA
Input Stray Capacitance	C_{IN}	Total input		5	7.5	pF

Electrical Characteristics at T_a=-40 to +85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	-0.5			mA
		V_{DD}=10V, V_o=9.5V, "	-1.0			mA
		V_{DD}=15V, V_o=13.5V, "	-3.5			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}	0.5			mA
		V_{DD}=10V, V_o=0.5V, "	1.0			mA
		V_{DD}=15V, V_o=1.5V, "	3.5			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V, V_o=9.0V, "	7.0			V
		V_{DD}=15V, V_o=13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5or4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, V_o=1.0or9.0V, "			3.0	V
		V_{DD}=15V, V_o=1.5or13.5V, "			4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V			1.0	uA
		V_{DD}=18V, V_{IN}=0V			-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			7.5	uA
		V_{DD}=10V, "			15	uA
		V_{DD}=15V, "			30	uA

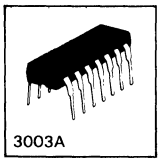
Note) Current direction ; +, no sign:Flowing into SSI, -:Flowing out of SSI.

Switching Characteristics at T_a=25±2°C, C_L=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Rise Time	t_{TLH}	V_{DD}=5V		100	200	ns
	(t_r)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching time test circuit and waveform



LC4073B



C MOS IC

CMOS Logic B-Series Triple 3-Input AND Gate

Ⓔ 1377A

The LC4073B is a 3-input AND logic IC ——— B series ——— having such features as wide operating range, high noise margin, low power dissipation, etc.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.5 to +20	V
Input Voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leqq 85°C$	300	mW
Operating Temperature	T_{opg}		40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

Allowable Operating Range at T_a=−40 to +85°C, V_{SS}=0V

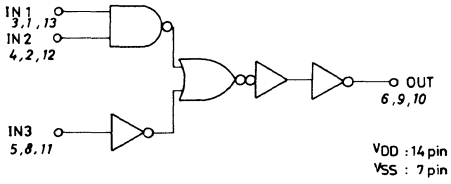
			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Electrical Characteristics at T_a= 25±2°C, V_{SS}=0V

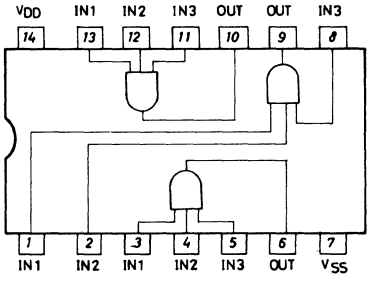
			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{DD}$	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{SS}$, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V

(continued on next page)

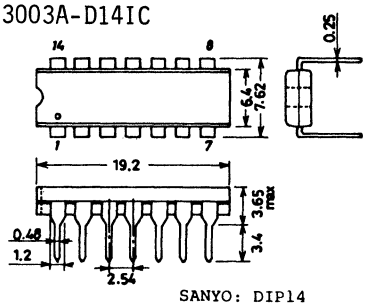
Equivalent Circuit
1/3 LC4075B



Pin Assignement (top view)



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

			min	typ	max	unit
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}$	−0.5	−1.0		mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−1.0	−2.0		mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−3.5	−7.0		mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.5	1.0		mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.0	2.0		mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5$or$4.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5	2.5		V
		$V_{DD}=10V, V_O=1.0$or$4.0V$, 〃	7.0	5.0		V
		$V_{DD}=15V, V_O=1.5$or$13.5V$, 〃	11.0	7.5		V
"L" Input Level Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V, \lvert I_{OUT}\rvert<1\mu A$		2.5	1.5	V
		$V_{DD}=10V, V_O=1.0V$, 〃		5.0	3.0	V
		$V_{DD}=15V, V_O=1.5V$, 〃		7.5	4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$		10^{-5}	0.1	μA
		$V_{DD}=18V, V_{IN}=0V$		-10^{-5}	−0.1	μA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$		0.01	1.0	μA
		$V_{DD}=10V$, 〃		0.01	2.0	μA
		$V_{DD}=15V$, 〃		0.01	4.0	μA
Input Stray Capacitance	C_{IN}	Total input		5	7.5	pF

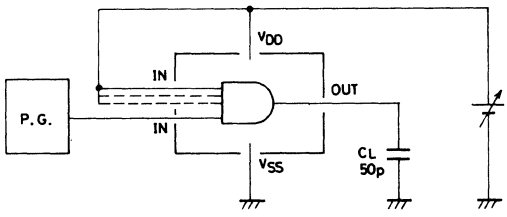
Electrical Characteristics at T_a=−40 to +85°C, V_{SS}=0V

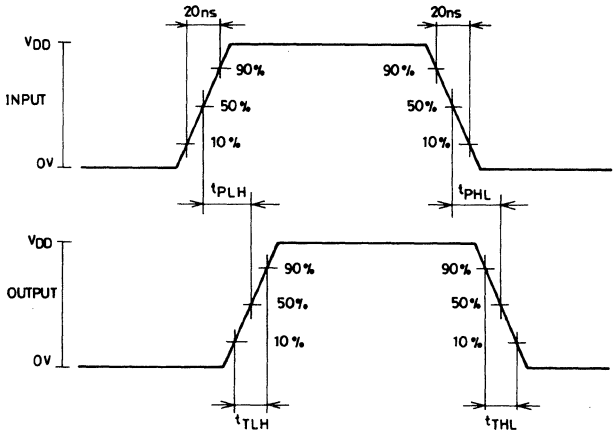
			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{DD}$	4.95			V
		$V_{DD}=10V$, 〃 〃	9.95			V
		$V_{DD}=15V$, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}, V_{DD}$			0.05	V
		$V_{DD}=10V$, 〃 〃			0.05	V
		$V_{DD}=15V$, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{DD}$	−0.5			mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−1.0			mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−3.5			mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.5			mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.0			mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.5			mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5$or$4.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5			V
		$V_{DD}=10V, V_O=1.0$or$4.0V$, 〃	7.0			V
		$V_{DD}=15V, V_O=1.5$or$13.5V$, 〃	11.0			V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V, \lvert I_{OUT}\rvert<1\mu A$			1.5	V
		$V_{DD}=10V, V_O=1.0V$, 〃			3.0	V
		$V_{DD}=15V, V_O=1.5V$, 〃			4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$			0.1	μA
		$V_{DD}=18V, V_{IN}=0V$			−0.1	μA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$			7.5	μA
		$V_{DD}=10V$, 〃			15	μA
		$V_{DD}=15V$, 〃			30	μA

Note) Current direction: +, no sign: Flowing into SSI,
−: Flowing out of SSI.

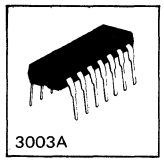
Switching Characteristics at T_a=25±2°C, C_L=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		180	350	ns
		V_{DD}=10V		90	175	ns
		V_{DD}=15V		80	150	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		160	350	ns
		V_{DD}=10V		80	170	ns
		V_{DD}=15V		70	150	ns
Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Fall Time	t_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching time test circuit and waveform





LC4075B


3003A

C MOS IC

CMOS Logic B-Series
Dual 3-Input OR Gate

Ⓔ 1368A

The LC4075B is a 3-input OR logic IC ——— B series ——— having such features as wide operating range, high noise margin, low power dissipation, etc.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.5 to +20	V
Input Voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leq 85°C$	300	mW
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

Allowable Operating Range at T_a=−40 to +85°C, V_{SS}=0V

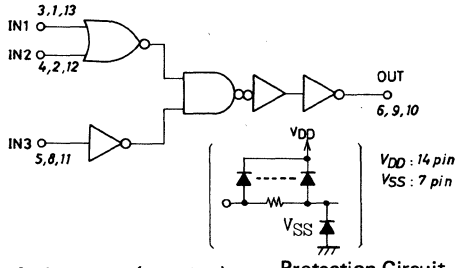
			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Electrical Characteristics at T_a=−40 to +85°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$, $V_{IN}=V_{SS}$, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS}$			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V

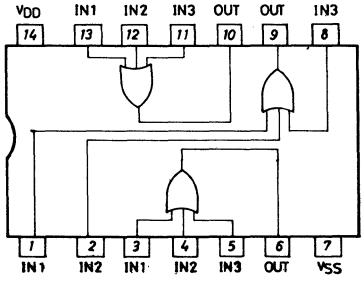
(continued on next page)

Equivalent Circuit
1/3 · LC4075B

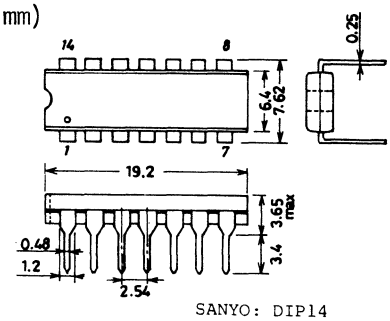


Protection Circuit

Pin Assignement (top view)



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

			min	typ	max	unit
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}, V_{DD}$	−0.5			mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−1.0			mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−3.5			mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}$	0.5			mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.0			mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.5			mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=4.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5			V
		$V_{DD}=10V, V_O=9.0V$, 〃	7.0			V
		$V_{DD}=15V, V_O=13.5V$, 〃	11.0			V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$			1.5	V
		$V_{DD}=10V, V_O=1.0$ or $9.0V$, 〃			3.0	V
		$V_{DD}=15V, V_O=1.5$ or $13.5V$, 〃			4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$			1.0	μA
		$V_{DD}=18V, V_{IN}=0V$			−1.0	μA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$			7.5	μA
		$V_{DD}=10V$, 〃			15	μA
		$V_{DD}=15V$, 〃			30	μA

Electrical Characteristics at $T_a=25\pm2°C$, $V_{SS}=0V$

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}, V_{DD}$	4.95			V
		$V_{DD}=10V$, 〃 〃	9.95			V
		$V_{DD}=15V$, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}$			0.05	V
		$V_{DD}=10V$, 〃 〃			0.05	V
		$V_{DD}=15V$, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}, V_{DD}$	−0.5	−1.0		mA
		$V_{DD}=10V, V_O=9.5V$, 〃	−1.0	−2.0		mA
		$V_{DD}=15V, V_O=13.5V$, 〃	−3.5	−7.0		mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}$	0.5	1.0		mA
		$V_{DD}=10V, V_O=0.5V$, 〃	1.0	2.0		mA
		$V_{DD}=15V, V_O=1.5V$, 〃	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=4.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5	2.5		V
		$V_{DD}=10V, V_O=9.0V$, 〃	7.0	5.0		V
		$V_{DD}=15V, V_O=13.5V$, 〃	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$		2.5	1.5	V
		$V_{DD}=10V, V_O=1.0$ or $9.0V$, 〃		5.0	3.0	V
		$V_{DD}=15V, V_O=1.5$ or $13.5V$, 〃		7.5	4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$		10^{-5}	1.0	μA
		$V_{DD}=18V, V_{IN}=0V$		-10^{-5}	−1.0	μA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}$		0.01	1.0	μA
		$V_{DD}=10V$, 〃		0.01	2.0	μA
		$V_{DD}=15V$, 〃		0.01	4.0	μA
Input Stray Capacitance	C_{IN}	Total input		5	7.5	pF

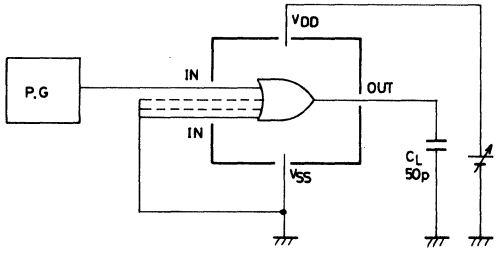
Note) Current direction: +, no sign: Flowing into SSI,
−: Flowing out of SSI.

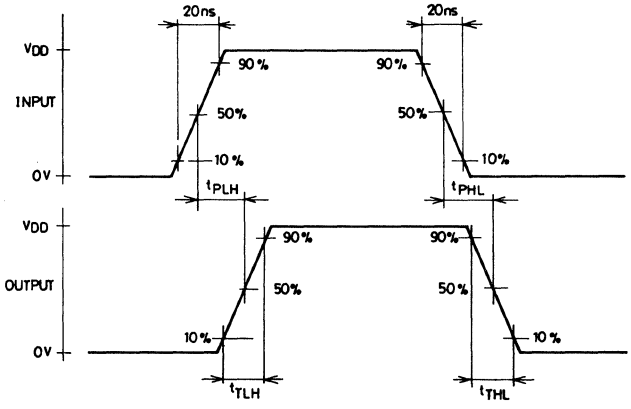
Switching Characteristics at $T_a=25\pm2°C$, $C_L=50pF$, $V_{SS}=0V$

			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	$V_{DD}=5V$		160	320	ns
		$V_{DD}=10V$		75	150	ns
		$V_{DD}=15V$		65	130	ns

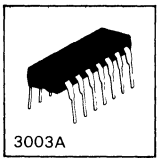
			min	typ	max	unit
"L" Level Propagation Delay Time	t_{PHL}	$V_{DD}=5V$		160	320	ns
		$V_{DD}=10V$		75	150	ns
		$V_{DD}=15V$		65	130	ns
Rise Time	t_{TLH} (t_r)	$V_{DD}=5V$		130	400	ns
		$V_{DD}=10V$		65	200	ns
		$V_{DD}=15V$		50	160	ns
Fall Time	t_{THL} (t_f)	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns

Switching time test circuit and waveform





LC4077B



C MOS IC

CMOS Logic B-Series
Quad 2-Input Exclusive-NOR Gate

Ⓔ 1504

The LC4077B is a quad 2-input Exclusive-NOR Gate IC (equivalent to B series) having such features as wide operating voltage range, high noise margin, low power dissipation.

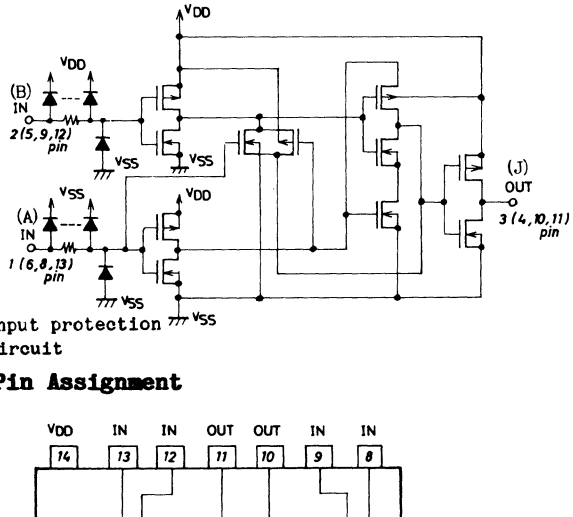
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD} max		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax		300	mW
Lead Temperature and Time	Tsol	t=10sec	260	°C
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

Allowable Operating Range at Ta=-40 to +85°C

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Equivalent Circuit(1/4 LC4077B)



Input protection circuit

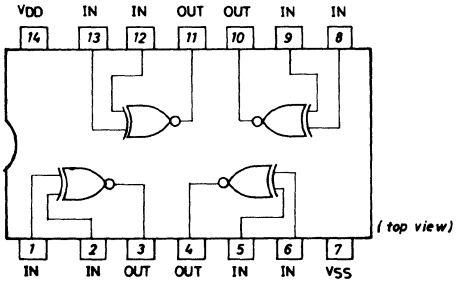
Truth Table

1 of 4 Gates

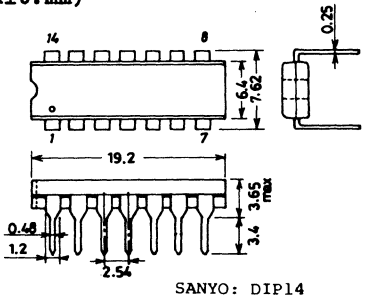
A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

1 : HIGH LEVEL
0 : LOW LEVEL
J : A ⊕ B

Pin Assignment



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

Electrical Characteristics at Ta=-40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS}, V_{DD}	-0.52			mA
		V_{DD}=10V, Vo=9.5V, "	-1.3			mA
		V_{DD}=15V, Vo=13.5V, "	-3.6			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{SS}, V_{DD}	0.52			mA
		V_{DD}=10V, Vo=1.0V, "	1.3			mA
		V_{DD}=15V, Vo=1.5V, "	3.6			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0			V
		V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, Vo=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V, Vo=1.5Vor13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V			0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V			-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, Vin=V_{SS}, V_{DD}			1.0	uA
		V_{DD}=10V, "			2.0	uA
		V_{DD}=15V, "			4.0	uA

Electrical Characteristics at Ta=25°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10.00		V
		V_{DD}=15V, " "	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS}, V_{DD}		0.00	0.05	V
		V_{DD}=10V, " "		0.00	0.05	V
		V_{DD}=15V, " "		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS}, V_{DD}	-0.44	-0.88		mA
		V_{DD}=10V, Vo=9.5V, "	-1.1	-2.25		mA
		V_{DD}=15V, Vo=13.5V, "	-3.0	-8.8		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{SS}, V_{DD}	0.44	0.88		mA
		V_{DD}=10V, Vo=1.0V, "	1.1	2.25		mA
		V_{DD}=15V, Vo=1.5V, "	3.0	8.8		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA	3.5	2.75		V
		V_{DD}=10V, Vo=1.0Vor9.0V, "	7.0	5.5		V
		V_{DD}=15V, Vo=1.5Vor13.5V, "	11.0	8.25		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA		2.25	1.5	V
		V_{DD}=10V, Vo=1.0Vor9.0V, "		4.5	3.0	V
		V_{DD}=15V, Vo=1.5Vor13.5V, "		6.75	4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V		10^{-5}	0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V		-10^{-5}	-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, Vin=V_{SS}, V_{DD}		0.001	1.0	uA
		V_{DD}=10V, "		0.001	2.0	uA
		V_{DD}=15V, "		0.001	4.0	uA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at Ta=85°C

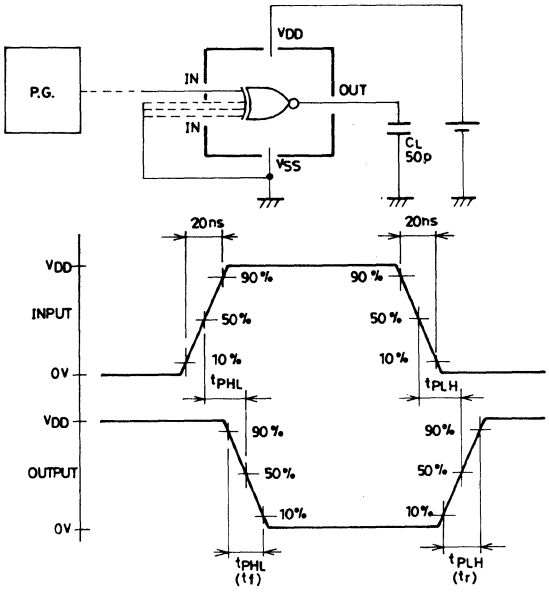
			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS},V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, Vin=V_{SS},V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V,Vo=4.6V,Vin=V_{SS},V_{DD}	-0.36			mA
		V_{DD}=10V,Vo=9.5V, "	-0.9			mA
		V_{DD}=15V,Vo=13.5V, "	-2.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V,Vo=0.4V,Vin=V_{SS},V_{DD}	0.36			mA
		V_{DD}=10V,Vo=1.0V, "	0.9			mA
		V_{DD}=15V,Vo=1.5V, "	2.4			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V,Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V,Vo=1.0Vor9.0V, "	7.0			V
		V_{DD}=15V,Vo=1.5Vor13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V,Vo=0.5Vor4.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V,Vo=1.0Vor9.0V, "			3.0	V
		V_{DD}=15V,Vo=1.5Vor13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V,Vin=18V			1.0	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V,Vin=0V			-1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V,Vin=V_{SS},V_{DD}			7.5	uA
		V_{DD}=10V, "			15.0	uA
		V_{DD}=15V, "			30.0	uA

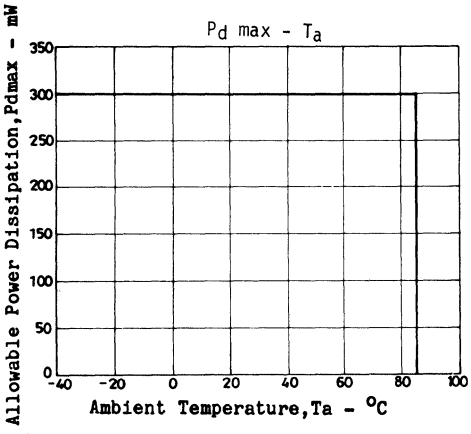
Note) Current direction: +, no sign : Flowing into device
- : Flowing out of device.

Switching Characteristics at Ta=25±2°C,V_{SS}=0V,C_L=50pF

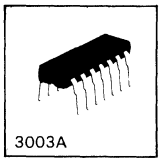
			min	typ	max	unit
Output Rise Time	t_r (t_{TLH})	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Output Fall Time	t_f (t_{THL})	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		175	350	ns
		V_{DD}=10V		75	150	ns
		V_{DD}=15V		50	100	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		175	350	ns
		V_{DD}=10V		75	150	ns
		V_{DD}=15V		50	100	ns

Switching Time Test Circuit and Waveform





LC4081B



C MOS IC

CMOS Logic B-Series Quad 2-Input AND Gate

Ⓔ 848B

The LC4081B is a 2-input AND logic IC —— B series —— having such features as wide operating range, high noise margin, low power dissipation, etc.

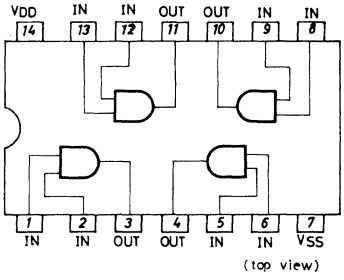
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	$P_d$max	$T_a \leq 85°C$, I_{IN}=10mA	300	mW
Lead Temeperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

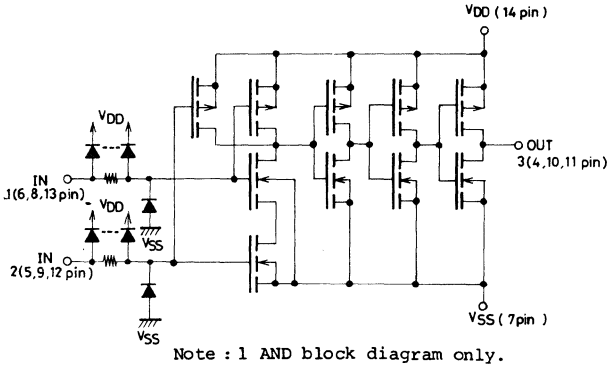
Electrical Characteristics at T_a=-40 to +85°C, V_{SS}=0V

Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Pin Assignment

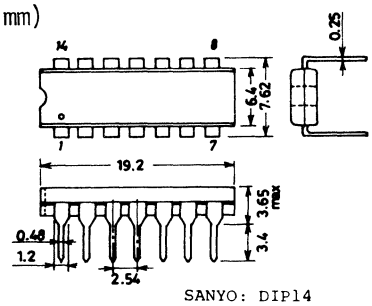


Equivalent Circuit



Note : 1 AND block diagram only.

Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

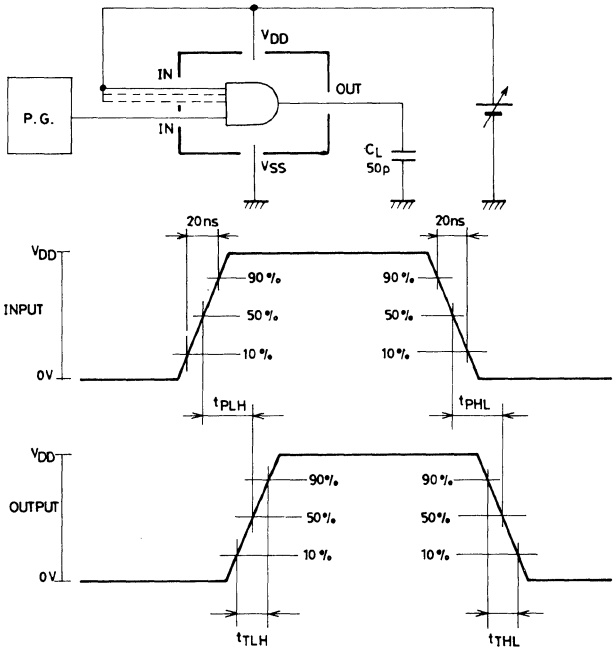
Electrical Characteristics at T_a=25±2°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{DD}	-0.5	-1.0		mA
		V_{DD}=10V, V_o=9.5V, "	-1.0	-2.0		mA
		V_{DD}=15V, V_o=13.5V, "	-3.5	-7.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5	1.0		mA
		V_{DD}=10V, V_o=0.5V, "	1.0	2.0		mA
		V_{DD}=15V, V_o=1.5V, "	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5or4.5V, $\|I_{OUT}\|$<1uA	3.5	2.5		V
		V_{DD}=10V, V_o=1.0or4.0V, "	7.0	5.0		V
		V_{DD}=15V, V_o=1.5or13.5V, "	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1uA		2.5	1.5	V
		V_{DD}=10V, V_o=1.0V, "		5.0	3.0	V
		V_{DD}=15V, V_o=1.5V "		7.5	4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V		10^{-5}	0.1	uA
		V_{DD}=18V, V_{IN}=0V		-10^{-5}	-0.1	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.01	1.0	uA
		V_{DD}=10V, "		0.01	2.0	uA
		V_{DD}=15V, "		0.01	4.0	uA
Input Stray Capacitance	C_{IN}	Total input		5	7.5	pF

Electrical Characteristics at T_a=-40 to +85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1uA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{DD}	-0.5			mA
		V_{DD}=10V, V_o=9.5V, "	-1.0			mA
		V_{DD}=15V, V_o=13.5V, "	-3.5			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5			mA
		V_{DD}=10V, V_o=0.5V, "	1.0			mA
		V_{DD}=15V, V_o=1.5V, "	3.5			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5or4.5V, $\|I_{OUT}\|$<1uA	3.5			V
		V_{DD}=10V, V_o=1.0or4.0V, "	7.0			V
		V_{DD}=15V, V_o=1.5or13.5V, "	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1uA			1.5	V
		V_{DD}=10V, V_o=1.0V, "			3.0	V
		V_{DD}=15V, V_o=1.5V, "			4.0	V
Input Leak Current	I_{IN}	V_{DD}=18V, V_{IN}=18V			0.1	uA
		V_{DD}=18V, V_{IN}=0V			-0.1	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			7.5	uA
		V_{DD}=10V, "			15	uA
		V_{DD}=15V, "			30	uA

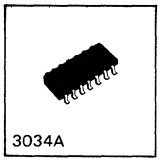
Note) Current direction ; +, no sign : Flowing into SSI, - : Flowing out of SSI .

Switching Characteristics at T_a=25±2°C, CL=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Rise Time	t_{TLH}	V_{DD}=5V		100	200	ns
	(t_r)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching time test circuit and waveform



LC4081BM



C MOS IC

CMOS Logic B-Series Quad 2-Input AND Gate

Ⓔ 1142B

The LC4081BM is a 2-input AND logic IC —— B series —— having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

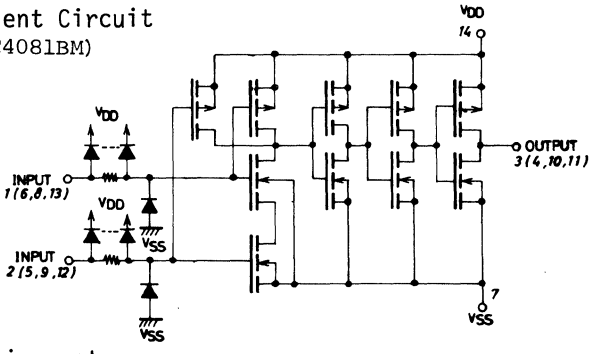
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		+10	mA
Allowble Power Dissipation	$P_d max$	$T_a \leqq 85$°C	150	mW
Lead Temperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-65 to +150	°C

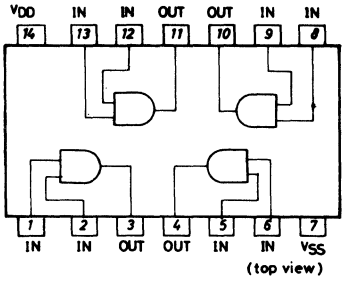
Allowable Operating Range at T_a=-40 to +85 °C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

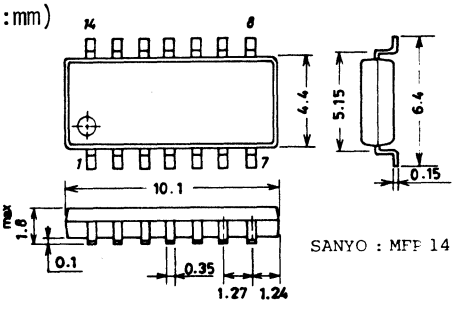
Equivalent Circuit
(1/4 LC4081BM)



Pin Assignment



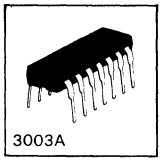
Case Outline 3034A-M14IC
(unit:mm)



SANYO : MFP 14

For details, refer to the description of the LC4081B.

LC4082B



C MOS IC

CMOS Logic B-Series Dual 4-Input AND Gate

Ⓔ 1325A

The LC4082B is a 4-input AND logic IC (equivalent to B series) having such features as wide operating voltage range, high noise margin, low power dissipation, etc.

Absolute Maximum Ratings at T_a = 25°C, V_{SS} = 0 V

				unit
Maximum supply voltage	V_{DD} max		−0.5 ~ +20	V
Input voltage	V_{IN}		−0.5 ~ V_{DD}+0.5	V
Input current	I_{IN}		±10	mA
Allowable power dissipation	P_d max	$T_a \leqq 85°C$	300	mW
Operating temperature	T_{opg}		−40 ~ +85	°C
Storage temperature	T_{stg}		−65 ~ +150	°C

Allowable Operating Range at T_a = −40 ~ +85°C, V_{SS} = 0 V

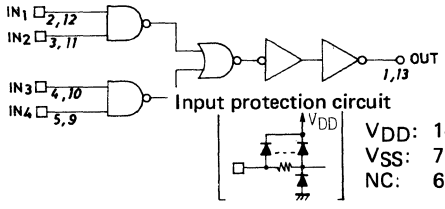
			unit
Supply voltage	V_{DD}	3 ~ 18	V
Input voltage	V_{IN}	0 ~ V_{DD}	V

Electrical Characteristics at T_a = −40 ~ +85°C, V_{SS} = 0 V

			min	type	max	unit
"H" Level Input Voltage	V_{IH}	V_{DD} = 5 V, V_o = 4.5 V, $\lvert I_o \rvert < 1\ \mu A$	3.5			V
		V_{DD} = 10 V, V_o = 9.0 V, $\lvert I_o \rvert < 1\ \mu A$	7.0			V
		V_{DD} = 15 V, V_o = 13.5 V, $\lvert I_o \rvert < 1\ \mu A$	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD} = 5 V, V_o = 0.5 V, $\lvert I_o \rvert < 1\ \mu A$			1.5	V
		V_{DD} = 10 V, V_o = 1.0 V, $\lvert I_o \rvert < 1\ \mu A$			3.0	V
		V_{DD} = 15 V, V_o = 1.5 V, $\lvert I_o \rvert < 1\ \mu A$			4.0	V

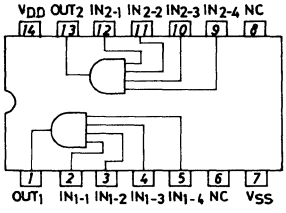
Equivalent Circuit

(1/2 LC4082B)

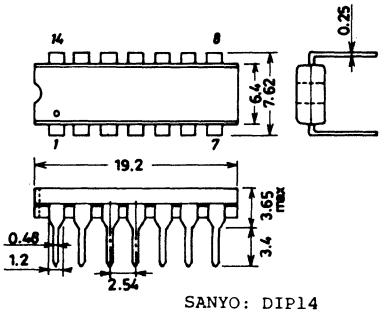


V_{DD}: 14 pin
V_{SS}: 7 pin
NC: 6,8 Pins

Pin assignment (top view)



Case Outline 3003A-D14IC
(unit: mm)



SANYO: DIP14

Electrical Characteristics/T_a = +25°C V_{SS} = 0 V			min	typ	max	unit
"H" level output voltage	V_{OH}	V_{DD} = 5 V, V_{IN} = V_{DD}, $\lvert I_{OUT}\rvert < 1\ \mu A$	4.95	5.00		V
		V_{DD} = 10 V, V_{IN} = V_{DD}, $\lvert I_{OUT}\rvert < 1\ \mu A$	9.95	10.00		V
		V_{DD} = 15 V, V_{IN} = V_{DD}, $\lvert I_{OUT}\rvert < 1\ \mu A$	14.95	15.00		V
"L" level output voltage	V_{OL}	V_{DD} = 5 V, V_{IN} = V_{DD}, V_{SS}, $\lvert I_{OUT}\rvert < 1\ \mu A$		0.00	0.05	V
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{SS}, $\lvert I_{OUT}\rvert < 1\ \mu A$		0.00	0.05	V
		V_{DD} = 15 V, V_{IN} = V_{DD}, V_{SS}, $\lvert I_{OUT}\rvert < 1\ \mu A$		0.00	0.05	V
"H" level output current	I_{OH}	V_{DD} = 5 V, V_O = 4.6 V, V_{IN} = V_{DD}	−0.16	−0.5		mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IN} = V_{DD}	−0.4	−1.2		mA
		V_{DD} = 15 V, V_O = 13.5 V, V_{IN} = V_{DD}	−1.2	−6.0		mA
"L" level output current	I_{OL}	V_{DD} = 5 V, V_O = 0.4 V, V_{IN} = V_{DD}, V_{SS}	0.44	1.5		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IN} = V_{DD}, V_{SS}	1.1	3.5		mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IN} = V_{DD}, V_{SS}	3.0	15		mA
"H" level input voltage	V_{IH}	V_{DD} = 5 V, V_O = 0.5 V, 4.5 V, $\lvert I_{OUT}\rvert < 1\ \mu A$	3.5	2.75		V
		V_{DD} = 10 V, V_O = 1.0 V, 9.0 V, $\lvert I_{OUT}\rvert < 1\ \mu A$	7.0	5.5		V
		V_{DD} = 15 V, V_O = 1.5 V, 13.5 V, $\lvert I_{OUT}\rvert < 1\ \mu A$	11.0	8.25		V
"L" level input voltage	V_{IL}	V_{DD} = 5 V, V_O = 0.5 V, $\lvert I_{OUT}\rvert < 1\ \mu A$		2.25	1.5	V
		V_{DD} = 10 V, V_O = 1.0 V, $\lvert I_{OUT}\rvert < 1\ \mu A$		4.5	3.0	V
		V_{DD} = 15 V, V_O = 1.5 V, $I_{OUT} < 1\ \mu A$		6.75	4.0	V
"H" level input current	I_{IH}	V_{DD} = 18 V, V_{IH} = 18 V		10^{-5}	0.3	μA
"L" level input current	I_{IL}	V_{DD} = 18 V, V_{IH} = 0 V		-10^{-5}	−0.3	μA
Quiescent device current	I_{DD}	V_{DD} = 5 V, V_{IN} = V_{DD}, V_{SS}		0.001	1.0	μA
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{SS}		0.001	2.0	μA
		V_{DD} = 15 V, V_{IN} = V_{DD}, V_{SS}		0.002	4.0	μA
Input stray capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics at T_a = −40°C, V_{SS} = 0 V			min	typ	max	unit
"H" level output voltage	V_{OH}	V_{DD} = 5 V, V_{IN} = V_{DD}, $\lvert I_{OUT}\rvert < 1\ \mu A$	4.95			V
		V_{DD} = 10 V, V_{IN} = V_{DD}, $\lvert I_{OUT}\rvert < 1\ \mu A$	9.95			V
		V_{DD} = 15 V, V_{IN} = V_{DD}, $\lvert I_{OUT}\rvert < 1\ \mu A$	14.95			V
"L" level output voltage	V_{OL}	V_{DD} = 5 V, V_{IN} = V_{DD}, V_{SS}, $\lvert I_{OUT}\rvert < 1\ \mu A$			0.05	V
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{SS}, $\lvert I_{OUT}\rvert < 1\ \mu A$			0.05	V
		V_{DD} = 15 V, V_{IN} = V_{DD}, V_{SS}, $\lvert I_{OUT}\rvert < 1\ \mu A$			0.05	V
"H" level output current	I_{OH}	V_{DD} = 5 V, V_O = 4.6 V, V_{IN} = V_{DD}	−0.2			mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IN} = V_{DD}	−0.5			mA
		V_{DD} = 15 V, V_O = 13.5 V, V_{IN} = V_{DD}	−1.4			mA

			min	typ	max	unit
"L" level output current	I_{OL}	V_{DD} = 5 V, V_O = 0.4 V, V_{IN} = V_{DD}, V_{SS}	0.52			mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IN} = V_{DD}, V_{SS}	1.3			mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IN} = V_{DD}, V_{SS}	3.6			mA
"H" level input voltage	V_{IH}	V_{DD} = 5 V, V_O = 0.5 V, 4.5 V, $\|I_{OUT}\| < 1\ \mu A$	3.5			V
		V_{DD} = 10 V, V_O = 1.0 V, 9.0 V, $\|I_{OUT}\| < 1\ \mu A$	7.0			V
		V_{DD} = 15 V, V_O = 1.5 V, 13.5 V, $\|I_{OUT}\| < 1\ \mu A$	11.0			V
"L" level input voltage	V_{IL}	V_{DD} = 5 V, V_O = 0.5 V, $\|I_{OUT}\| < 1\ \mu A$			1.5	V
		V_{DD} = 10 V, V_O = 1.0 V, $\|I_{OUT}\| < 1\ \mu A$			3.0	V
		V_{DD} = 15 V, V_O = 1.5 V, $\|I_{OUT}\| < 1\ \mu A$			4.0	V
"H" level input current	I_{IH}	V_{DD} = 18 V, V_{IH} = 18 V			0.3	ßA
"L" level input current	I_{IL}	V_{DD} = 18 V, V_{IH} = 0 V			−0.3	μA
Quiescent device current	I_{DD}	V_{DD} = 5 V, V_{IN} = V_{DD}, V_{SS}			1.0	μA
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{SS}			2.0	μA
		V_{DD} = 15 V, V_{IN} = V_{DD}, V_{SS}			4.0	μA

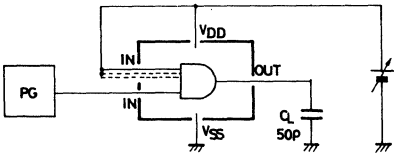
Electrical Characteristics/T_a = +85°C V_{SS} = 0 V			min	typ	max	unit
"H" level output voltage	V_{OH}	V_{DD} = 5 V, V_{IN} = V_{DD}, $\|I_{OUT}\| < 1\ \mu A$	4.95			V
		V_{DD} = 10 V, V_{IN} = V_{DD}, $\|I_{OUT}\| < 1\ \mu A$	9.95			V
		V_{DD} = 15 V, V_{IN} = V_{DD}, $\|I_{OUT}\| < 1\ \mu A$	14.95			V
"L" level output voltage	V_{OL}	V_{DD} = 5 V, V_{IN} = V_{DD}, V_{SS}, $\|I_{OUT}\| < 1\ \mu A$			0.05	V
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{SS}, $\|I_{OUT}\| < 1\ \mu A$			0.05	V
		V_{DD} = 15 V, V_{IN} = V_{DD}, V_{SS}, $\|I_{OUT}\| < 1\ \mu A$			0.05	V
"H" level output current	I_{OH}	V_{DD} = 5 V, V_O = 4.6 V, V_{IN} = V_{DD}	−0.12			mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IN} = V_{DD}	−0.3			mA
		V_{DD} = 15 V, V_O = 13.5 V, V_{IN} = V_{DD}	−1.0			mA
"L" output current	I_{OL}	V_{DD} = 5 V, V_O = 0.4 V, V_{IN} = V_{DD}, V_{SS}	0.36			mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IN} = V_{DD}, V_{SS}	0.9			mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IN} = V_{DD}, V_{SS}	2.4			mA
"H" level input voltage	V_{IH}	V_{DD} = 5 V, V_O = 0.5 V, 4.5 V, $\|I_{OUT}\| < 1\ \mu A$	3.5			V
		V_{DD} = 10 V, V_O = 1.0 V, 9.0 V, $\|I_{OUT}\| < 1\ \mu A$	7.0			V
		V_{DD} = 15 V, V_O = 1.5 V, 13.5 V, $\|I_{OUT}\| < 1\ \mu A$	11.0			V

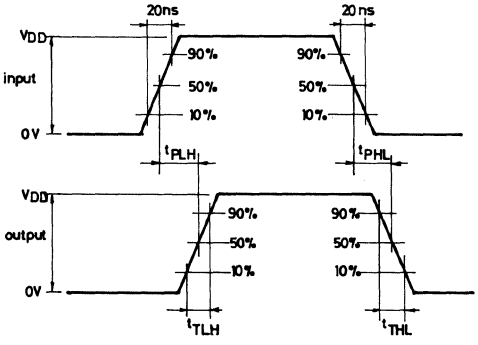
			min	typ	max	unit
"L" level input voltage	V_{IL}	V_{DD} = 5 V, V_O = 0.5 V, $\lvert I_{OUT} \rvert < 1\ \mu A$			1.5	V
		V_{DD} = 10 V, V_O = 1.0 V, $\lvert I_{OUT} \rvert < 1\ \mu A$			3.0	V
		V_{DD} = 15 V, V_O = 1.5 V, $\lvert I_{OUT} \rvert < 1\ \mu A$			4.0	V
"H" level input current	I_{IH}	V_{DD} = 18 V, V_{IH} = 18 V			1.0	μA
"L" level input current	I_{IL}	V_{DD} = 18 V, V_{IH} = 0 V			−1.0	μA
Quiescent device current	I_{DD}	V_{DD} = 5 V, V_{IN} = V_{DD}, V_{SS}			7.5	μA
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{SS}			15	μA
		V_{DD} = 15 V, V_{IN} = V_{DD}, V_{SS}			30	μA

Note) Current direction; +, no sign: Flowing into SSI, −: Flowing out of SSI.

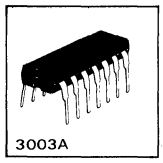
Switching Characteristics at T_a = 25±2°C, C_L = 50 pF, V_{SS} = 0 V			min	typ	max	unit
"H" level propagation delay time	t_{PLH}	V_{DD} = 5 V		180	350	ns
		V_{DD} = 10 V		90	175	ns
		V_{DD} = 15 V		80	150	ns
"L" level propagation delay time	t_{PHL}	V_{DD} = 5 V		160	350	ns
		V_{DD} = 10 V		80	175	ns
		V_{DD} = 15 V		70	150	ns
Rise time	t_{TLH} (t_r)	V_{DD} = 5 V		130	400	ns
		V_{DD} = 10 V		65	200	ns
		V_{DD} = 15 V		50	160	ns
Fall time	t_{THL} (t_r)	V_{DD} = 5 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns

Switching time test circuit and waveform





LC4093B



C MOS IC

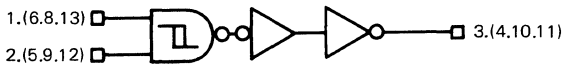
CMOS Logic B-Series Quad 2-Input NAND Schmitt Trigger

The LC4093B is a quad 2-input NAND Schmitt trigger IC (B series) having such features as wide operating voltage range, high noise margin, and low power dissipation.

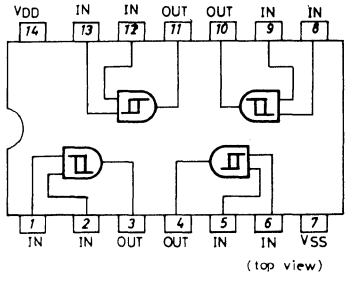
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DD} max		V_{SS}−0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}−0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max		300	mW
Lead Temperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

Allowable Operating Ranges at T_a=−40 to +85°C			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

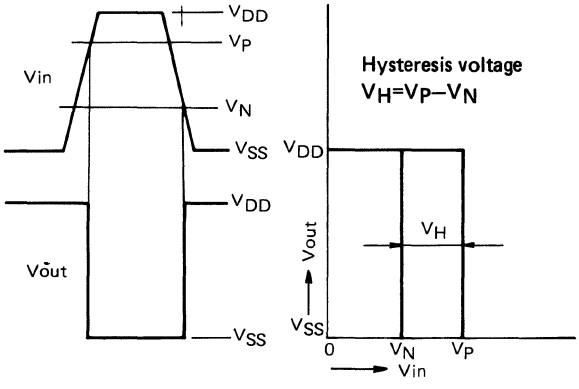
Logic Diagram



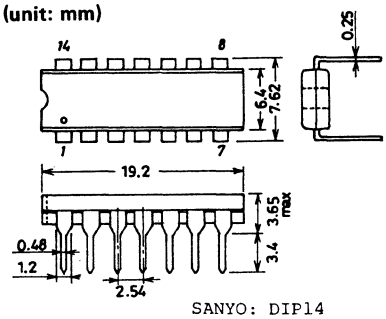
Pin Assignment



Input/Output Characteristics



Case Outline 3003A-D14IC
(unit: mm)



SANYO: DIP14

Electrical Characteristics at T_a=−40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.2			mA
		V_{DD}=10V, V_o=9.5V, "	−0.5			mA
		V_{DD}=15V, V_o=13.5V, "	−1.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.52			mA
		V_{DD}=10V, V_o=0.5V, "	1.3			mA
		V_{DD}=15V, V_o=1.5V, "	3.6			mA
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			0.3	μA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			−0.3	μA
Quiescent Device Current	I_{DD}	V_{DD}=5V			1.0	μA
		V_{DD}=10V			2.0	μA
		V_{DD}=15V			4.0	μA

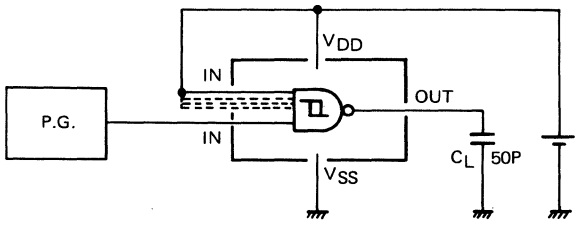
Electrical Characteristics T_a=+25°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10.00		V
		V_{DD}=15V, " "	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}		0.00	0.05	V
		V_{DD}=10V, " "		0.00	0.05	V
		V_{DD}=15V, " "		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.16	−0.5		mA
		V_{DD}=10V, V_o=9.5V, "	−0.4	−0.5		mA
		V_{DD}=15V, V_o=13.5V, "	−1.2	−6.0		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.44	1.5		mA
		V_{DD}=10V, V_o=0.5V, "	1.1	3.5		mA
		V_{DD}=15V, V_o=1.5V, "	3.0	15		mA
"H" Level Threshold Voltage	V_P	V_{DD}=5V, V_o=0.5V, 4.5V, $\|I_{OUT}\|$<1μA	2.0	2.8	3.8	V
("H" Level Input Voltage)	(V_{IH})	V_{DD}=10V, V_o=1.0V, 9.0V, "	4.0	5.8	7.6	V
		V_{DD}=15V, V_o=1.5V, 13.5V, "	6.0	8.8	11.4	V
"L" Level Threshold Voltage	V_N	V_{DD}=5V, V_o=0.5V, 4.5V, $\|I_{OUT}\|$<1μA	1.2	2.2	3.0	V
("L" Level Input Voltage)	(V_{IL})	V_{DD}=10V, V_o=1.0V, 9.0V, "	2.4	4.2	6.0	V
		V_{DD}=15V, V_o=1.5V, 13.5V, "	3.6	6.2	9.0	V
Hysteresis Voltage	V_H	V_{DD}=5V	0.3	0.55	0.8	V
(Hysteresis Voltage Range)		V_{DD}=10V	1.0	1.6	2.2	V
		V_{DD}=15V	1.4	2.6	3.8	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V		10^{-5}	0.3	μA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V		-10^{-5}	−0.3	μA
Quiescent Device Current	I_{DD}	V_{DD}=5V		0.001	1.0	μA
		V_{DD}=10V		0.002	2.0	μA
		V_{DD}=15V		0.004	4.0	μA
Input Capacitance	C_{IN}			5	7.5	pF

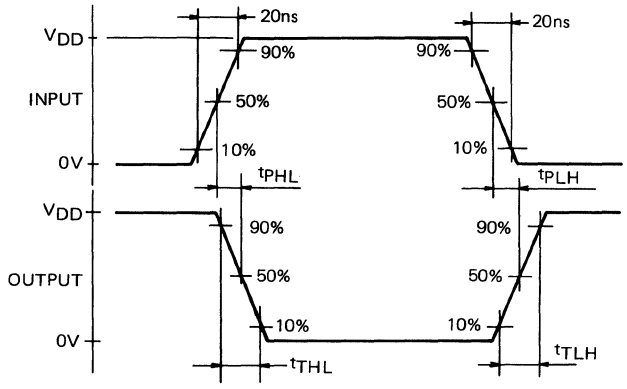
Electrical Characteristics T_a=+85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " " "	9.95			V
		V_{DD}=15V, " " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.12			mA
		V_{DD}=10V, V_o=9.5V, "	−0.3			mA
		V_{DD}=15V, V_o=13.5V, "	−1.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.36			mA
		V_{DD}=10V, V_o=0.5V, "	0.9			mA
		V_{DD}=15V, V_o=1.5V, "	2.4			mA
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			1.0	μA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			−1.0	μA
Quiescent Device Current	I_{DD}	V_{DD}=5V			7.5	μA
		V_{DD}=10V			15	μA
		V_{DD}=15V			30	μA

Note) Current direction; +, no sign: Flowing into device,
−: Flowing out of device

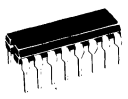
Switching Characteristics at T_a=25±2°C, CL=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Rise Time	t_{TLH}	V_{DD}=5V		100	200	ns
	(t_r)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Fall Time	t_{THL}	V_{DD}=5V		100	200	ns
	(t_f)	V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching Time Test Circuit and Waveform





LC4512B



3006A

C MOS IC

CMOS Logic B-Series
8-Channel Data Selector/Multiplexer

The LC4512B is a 8-channel data selector designed to select data input D_0 to D_7 for a given binary address input (A, B, C) combination.
Output Z is capable of being wired OR-tied because setting input DISABLE to "Hi" level permits output Z to be turned into a high impedance state.
Input DISABLE has priority for turning output Z into a high impedance state.
Setting input DISABLE to "Lo" level and input INHIBIT to "Hi" level cause data select to be inhibited and output Z to be set to "Lo" level.
The LC4512B (B series) has such features as wide operating voltage range, high noise margin, low power dissipation.

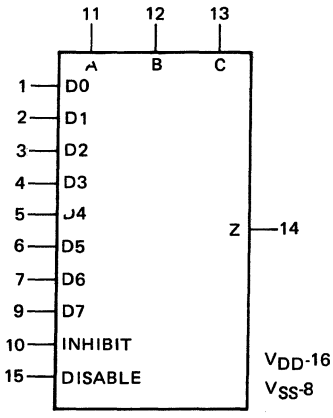
Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		V_{SS}−0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}−0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leqq 85°C$	300	mW
Lead Temperature and Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

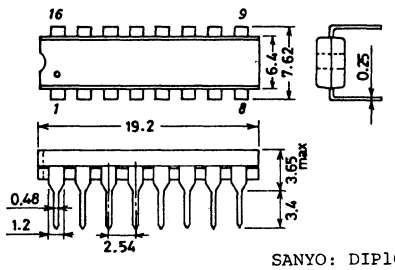
Allowable Operating Ranges at T_a=−40 to +85°C

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

Pin Assignment Circuit and Truth Table

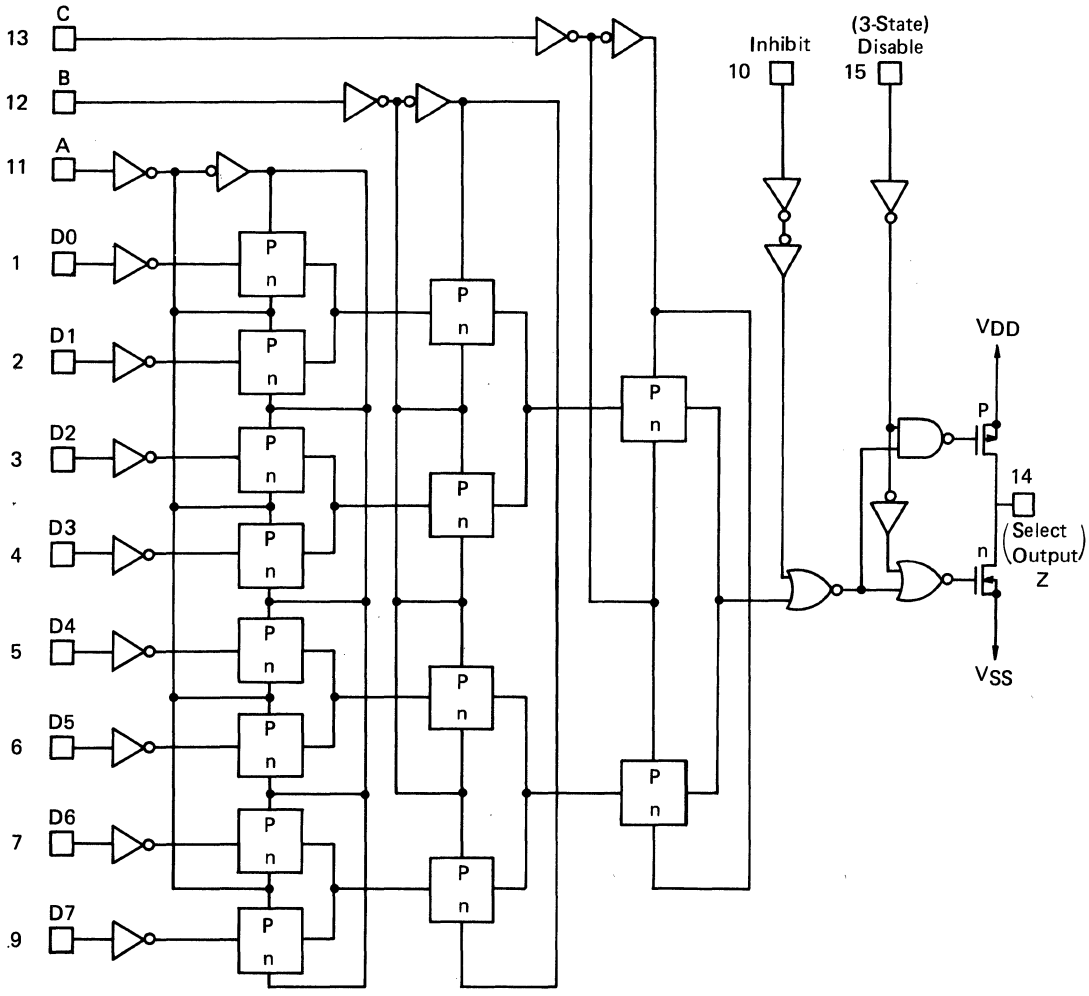


Case Outline 3006A-D16IC
(unit: mm)



SANYO: DIP16

Internal Equivalent Circuit and Truth Table



Truth Table

SEL·CONT			Inhibit	(3-Stat) Disable	(Select Output) Z
A	B	C			
0	0	0	0	0	D0
1	0	0	0	0	D1
0	1	0	0	0	D2
1	1	0	0	0	D3
0	0	1	0	0	D4
1	0	1	0	0	D5
0	1	1	0	0	D6
1	1	1	0	0	D7
X	X	X	1	0	0
X	X	X	X	1	High Z

"1": High Level
"2": Low Level
"X": Don't Care

Electrical Characteristics at T_a=−40°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_{OH}=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.2			mA
		V_{DD}=10V, V_{OH}=9.5V, "	−0.5			mA
		V_{DD}=15V, V_{OH}=13.5V, "	−1.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_{OL}=0.4V, V_{IN}=V_{SS}, V_{DD}	0.52			mA
		V_{DD}=10V, V_{OL}=0.5V, "	1.3			mA
		V_{DD}=15V, V_{OL}=1.5V, "	3.6			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_{OUT}=0.5V,4.5V, $\|I_{OUT}\|$<1μA	3.5			V
		V_{DD}=10V, V_{OUT}=1.0V,9.0V "	7.0			V
		V_{DD}=15V, V_{OUT}=1.5V,13.5V "	11.0			V
"L" Level Input Voltage	V_{IO}	V_{DD}=5V, V_{OUT}=0.5V,4.5V, $\|I_{OUT}\|$<1μA			1.5	V
		V_{DD}=10V, V_{OUT}=1.0V,9.0V, "			3.0	V
		V_{DD}=15V, V_{OUT}=1.5V,13.5V "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			0.3	μA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V			−0.3	μA
"H" Level Disable Current	I_{DH}	V_{DD}=18V, V_{OH}=18V			0.5	μA
"L" Level Disable Current	I_{DL}	V_{DD}=18V, V_{OL}=0V,			−0.5	μA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			20	μA
		V_{DD}=10V, "			40	μA
		V_{DD}=15V, "			60	μA

Electrical Characteristics T_a=+25°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10.00		V
		V_{DD}=15V, " "	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}		0.00	0.05	V
		V_{DD}=10V, " "		0.00	0.05	V
		V_{DD}=15V, " "		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_{OH}=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.16			mA
		V_{DD}=10V, V_{OH}=9.5V, "	−0.4			mA
		V_{DD}=15V, V_{OH}=13.5V, "	−1.2			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_{OL}=0.4V, V_{IN}=V_{SS}, V_{DD}	0.44			mA
		V_{DD}=10V, V_{OL}=0.5V, "	1.1			mA
		V_{DD}=15V, V_{OL}=1.5V, "	3.0			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_{OUT}=0.5V,4.5V, $\|I_{OUT}\|$<1μA	3.5	2.75		V
		V_{DD}=10V, V_{OUT}=1.0V, 9.0V, "	7.0	5.5		V
		V_{DD}=15V, V_{OUT}=1.5V, 13.5V, "	11.0	8.25		V
"L" Level Input Voltage	V_{IO}	V_{DD}=5V, V_{OUT}=0.5V,4.5V, $\|I_{OUT}\|$<1μA		2.25	1.5	V
		V_{DD}=10V, V_{OUT}=1.0V, 9.0V, "		4.5	3.0	V
		V_{DD}=15V, V_{OUT}=1.5V, 13.5V, "		6.75	4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V		10^{-5}	0.3	μA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IN}=0V		-10^{-5}	−0.3	μA
"H" Level Disable Current	I_{OH}	V_{DD}=18V, V_{OH}=18V		10^{-4}	0.5	μA
"L" Level Disable Current	I_{DL}	V_{DD}=18V, V_{OL}=0V		-10^{-4}	−0.5	μA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.005	20	μA
		V_{DD}=10V, "		0.010	40	μA
		V_{DD}=15V, "		0.015	80	μA
Input Capacitance	C_{IN}			5	7.5	pF
Disable Capacitance	C_{OUT}			17.5		pF

Electrical Characteristics T_a=+85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_{OH}=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.12			mA
		V_{DD}=10V, V_{OH}=9.5V, "	−0.3			mA
		V_{DD}=15V, V_{OH}=13.5V, "	−1.0			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_{OL}=0.4V, V_{IN}=V_{SS}, V_{DD}	0.36			mA
		V_{DD}=10V, V_{OL}=0.5V, "	0.9			mA
		V_{DD}=15V, V_{OL}=1.5V, "	2.4			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_{OUT}=0.5V, 4.5V, $\|I_{OUT}\|$<1μA	3.5			V
		V_{DD}=10V, V_{OUT}=1.0V, 9.0V, "	7.0			V
		V_{DD}=15V, V_{OUT}=1.5V, 13.5V, "	11.0			V
"L" Level Input Voltage	V_{IO}	V_{DD}=5V, V_{OUT}=0.5V, 4.5V, $\|I_{OUT}\|$<1μA			1.5	V
		V_{DD}=10V, V_{OUT}=1.0V, 9.0V, "			3.0	V
		V_{DD}=15V, V_{OUT}=1.5V, 13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, V_{IH}=18V			1.0	μA
"L" Level Input Current	I_{IL}	V_{DD}=18V, V_{IL}=0V			−1.0	μA
"H" Level Disable Current	I_{DH}	V_{DD}=18V, V_{OH}=18V			1.0	uA
"L" Level Disable Current	I_{DL}	V_{DD}=18V, V_{OL}=0V			−1.0	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V			150	μA
		V_{DD}=10V			300	μA
		V_{DD}=15V			600	μA

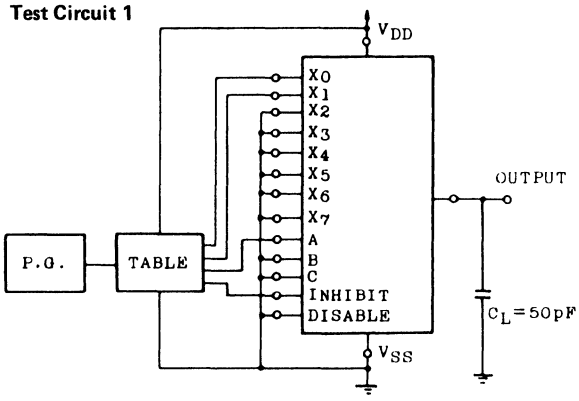
Note) Current direction; +, no sign: Flowing into device,
−: Flowing out of device

Switching Characteristics at T_a=25±2°C, CL=50pF, V_{SS}=0V			min	typ	max	unit
Output Rise Time	t_r	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_f	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"H" Level Propagation Delay Time (A, B, C – Select Out)	t_{PLH}	V_{DD}=5V		440	800	ns
		V_{DD}=10V		190	300	ns
		V_{DD}=15V		150	250	ns
"L" Level Propagation Delay Time (A, B, C – Select Out)	t_{PHL}	V_{DD}=5V		400	800	ns
		V_{DD}=10V		160	300	ns
		V_{DD}=15V		120	250	ns
"H" Level Propagation Delay Time (Dn – Select Out)	t_{PLH}	V_{DD}=5V		330	600	ns
		V_{DD}=10V		140	250	ns
		V_{DD}=15V		100	200	ns
"L" Level Propagation Delay Time (Dn – Select Out)	t_{PHL}	V_{DD}=5V		330	600	ns
		V_{DD}=10V		140	250	ns
		V_{DD}=15V		100	200	ns
"H" Level Propagation Delay Time (Inhibit – Select Out)	t_{PLH}	V_{DD}=5V		220	400	ns
		V_{DD}=10V		100	200	ns
		V_{DD}=15V		80	160	ns
"L" Level Propagation Time (Inhibit – Select Out)	t_{PHL}	V_{DD}=5V		270	500	ns
		V_{DD}=10V		130	250	ns
		V_{DD}=15V		110	200	ns
"H" Level Disable Output Time	t_{HZ}	V_{DD}=5V		95	150	ns
		V_{DD}=10V		55	100	ns
		V_{DD}=15V		45	90	ns

"L" Level Disable Output Time	t_{LZ}	V_{DD}=5V	60	150	ns
		V_{DD}=10V	40	70	ns
		V_{DD}=15V	35	60	ns
"H" Level Disable Output Time	t_{ZH}	V_{DD}=5V	120	200	ns
		V_{DD}=10V	50	100	ns
		V_{DD}=15V	45	90	ns
"L" Level Disable Output Time	t_{ZL}	V_{DD}=5V	90	150	ns
		V_{DD}=10V	40	70	ns
		V_{DD}=15V	35	60	ns

Switching Time Test Circuit and Waveform

Test Circuit 1

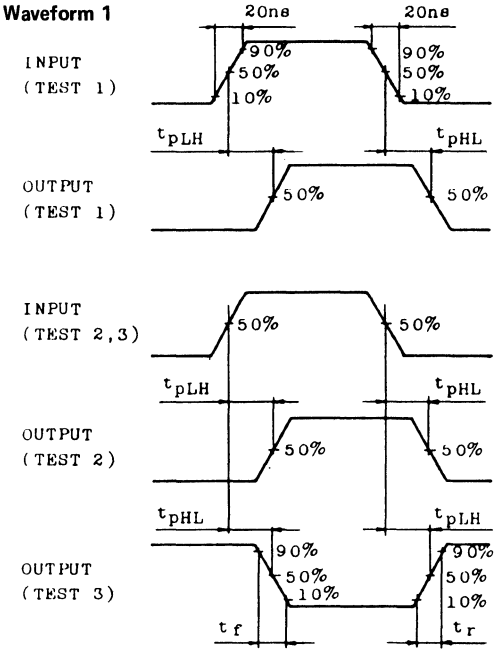


TABLE

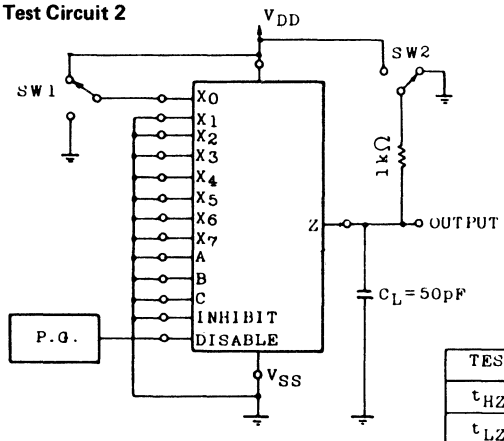
TEST	INH.	A	X_0	X_1
1	GND	P.G.	GND	V_{DD}
2	GND	GND	P.G.	GND
3	P.G.	GND	V_{DD}	GND

P.G. ; PULSE GENERATOR

Waveform 1



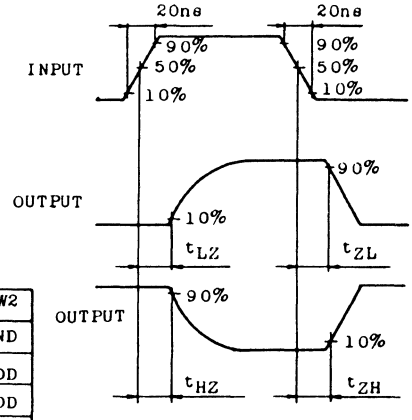
Test Circuit 2



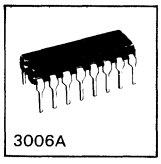
P.G. ; PULSE GENERATOR

TEST	SW1	SW2
t_{HZ}	V_{DD}	GND
t_{LZ}	GND	V_{DD}
t_{ZL}	GND	V_{DD}
t_{ZH}	V_{DD}	GND

Waveform 2



LC4520B



C MOS IC

CMOS Logic B-Series Dual Binary Up Counter

Ⓔ 1008B

Features

- Two 4-bit binary up counters consisting of 4 D-FFs of sync type are packaged in a single package. It is capable of counting, frequency-dividing BCD 2 digits or binary 8 bits.
- By applying "H" level signal to reset input, counter can be cleared (all "0" level) without regard to other inputs.
- When CLOCK enable input is at "H" level, count starts with rise of CLOCK input; when CLOCK input is at "L" level, count starts with fall of CLOCK enable input.

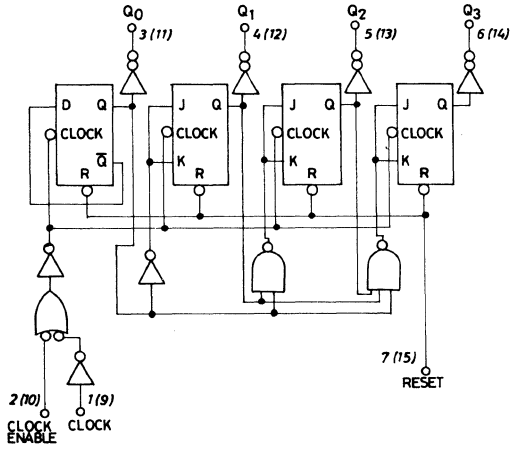
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.5 to +20	V
Input Voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leq 85°C$	300	mW
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

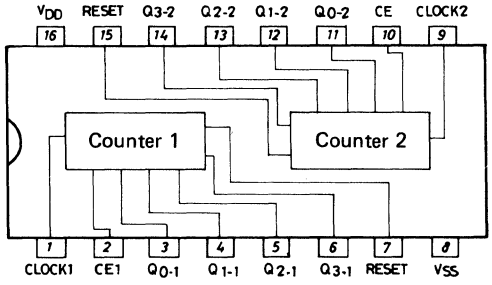
Allowable Operating Ranges/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

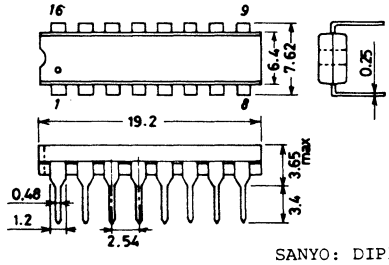
Equivalent Circuit (1/2 LC4520B)



Pin Assignment



Case Outline 3006A-D16IC
(unit: mm)



SANYO: DIP16

Electrical Characteristics/T_a=−40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Output Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Output Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.2			mA
		V_{DD}=10V, V_o=9.5V, 〃	−0.5			mA
		V_{DD}=15V, V_o=13.5V, 〃	−1.4			mA
"L" Output Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.52			mA
		V_{DD}=10V, V_o=0.5V, 〃	1.30			mA
		V_{DD}=15V, V_o=1.5V, 〃	3.60			mA
"H" Input Level Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA	3.5			V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃	7.0			V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃	11.0			V
"L" Input Level Voltage	V_{IL}	V_{DD}=5V, V_o=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA			1.5	V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃			3.0	V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃			4.0	V
"H" Input Level Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			0.3	μA
"L" Input Level Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			−0.3	μA
Quiescent Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			20	μA
Dissipation		V_{DD}=10V, 〃			40	μA
		V_{DD}=15V, 〃			80	μA

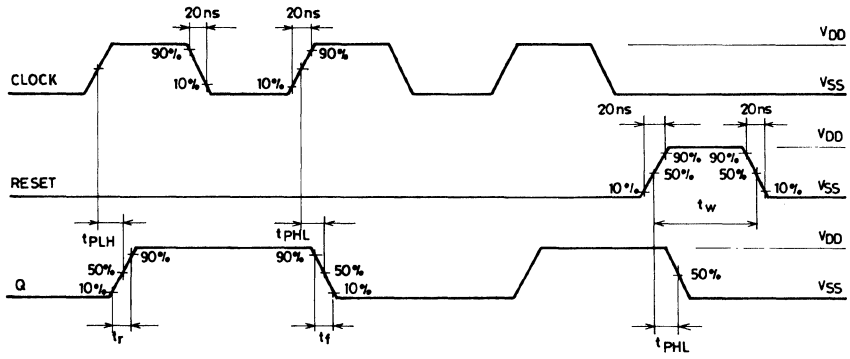
Electrical Characteristics/T_a=25°C±2°C, V_{SS}=0V			min	typ	max	unit
"H" Output Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, 〃 〃	9.95	10.00		V
		V_{DD}=15V, 〃 〃	14.95	15.00		V
"L" Output Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}		0.00	0.05	V
		V_{DD}=10V, 〃 〃		0.00	0.05	V
		V_{DD}=15V, 〃 〃		0.00	0.05	V
"H" Output Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.16	−0.36		mA
		V_{DD}=10V, V_o=9.5V, 〃	−0.4	−0.9		mA
		V_{DD}=15V, V_o=13.5V, 〃	−1.2	−3.5		mA
"L" Output Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.44	0.88		mA
		V_{DD}=10V, V_o=0.5V, 〃	1.1	2.55		mA
		V_{DD}=15V, V_o=1.5V, 〃	3.0	8.80		mA
"H" Input Level Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA	3.5	2.75		V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃	7.0	5.50		V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃	11.0	8.25		V
"L" Input Level Voltage	V_{IL}	V_{DD}=5V, V_o=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA		2.25	1.5	V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃		4.50	3.0	V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃		6.75	4.0	V
"H" Input Level Current	I_{IH}	V_{DD}=18V, V_{IN}=18V		10^{-5}	0.3	μA
"L" Input Level Current	I_{IL}	V_{DD}=18V, V_{IN}=0V		-10^{-5}	−0.3	μA
Quiescent Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}		0.005	20	μA
Dissipation		V_{DD}=10V, 〃		0.010	40	μA
		V_{DD}=15V, 〃		0.015	80	μA
Input Capacitance	C_{IN}			5	7.5	pF

Electrical Characteristics/T_a=+85°C, V_{SS}=0V			min	typ	max	unit
"H" Output Level Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Output Level Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1 μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Output Level Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.12			mA
		V_{DD}=10V, V_o=9.5V, 〃	−0.3			mA
		V_{DD}=15V, V_o=13.5V, 〃	−1.0			mA
"L" Output Level Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{SS}, V_{DD}	0.36			mA
		V_{DD}=10V, V_o=0.5V, 〃	0.9			mA
		V_{DD}=15V, V_o=1.5V, 〃	2.4			mA
"H" Input Level Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, or 4.5V, $\|I_{OUT}\|$<1 μA	3.5			V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃	7.0			V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃	11.0			V
"L" Input Level Voltage	V_{IL}	V_{DD}=5V, V_o=0.5V or 4.5V, $\|I_{OUT}\|$<1 μA			1.5	V
		V_{DD}=10V, V_o=1.0V or 9.0V, 〃			3.0	V
		V_{DD}=15V, V_o=1.5V or 13.5V, 〃			4.0	V
"H" Input Level Current	I_{IH}	V_{DD}=18V, V_{IN}=18V			1.0	μA
"L" Input Level Current	I_{IL}	V_{DD}=18V, V_{IN}=0V			−1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}			150	μA
		V_{DD}=10V, 〃			300	μA
		V_{DD}=15V, 〃			600	μA

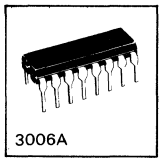
Current direction + (no sign): Flowing into device,
− : Flowing out of device

Switching Characteristics/T_a=25°C±2°C, V_{SS}=0V, C_L=50pF			min	typ	max	unit
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"H" Level Propagation Time (CLOCK→Q)	t_{pLH}	V_{DD}=5V		350	650	ns
		V_{DD}=10V		160	300	ns
		V_{DD}=15V		120	240	ns
"L" Level Propagation Time (CLOCK→Q)	t_{pLL}	V_{DD}=5V		300	600	ns
		V_{DD}=10V		130	260	ns
		V_{DD}=15V		110	220	ns
"L" Level Propagation Time (Reset→Q)	t_{pLL}	V_{DD}=5V		260	600	ns
		V_{DD}=10V		120	250	ns
		V_{DD}=15V		100	200	ns
Maximum Clock Rise, Fall Time	$t_{r\phi}$ $t_{f\phi}$	V_{DD}=5V	20.0			μs
		V_{DD}=10V	2.5			μs
		V_{DD}=15V	1.0			μs
Maximum Clock Frequency	$f_{max\phi}$	V_{DD}=5V	1.0	2.0		MHz
		V_{DD}=10V	3.5	5.8		MHz
		V_{DD}=15V	4.0	9.0		MHz
Minimum Reset Pulse Width (Reset)	tw	V_{DD}=5V		130	260	ns
		V_{DD}=10V		60	120	ns
		V_{DD}=15V		50	100	ns

CLOCK Enable = Hi



LC4528B



C MOS IC

C MOS Logic B-Series Dual Monostable Multivibrator

Ⓔ 972B

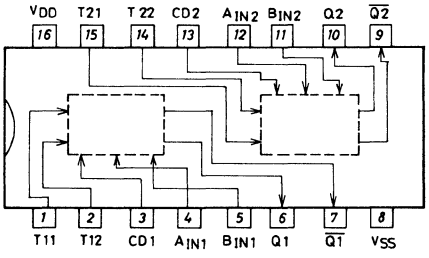
Use

- C MOS standard logic IC for logic circuit

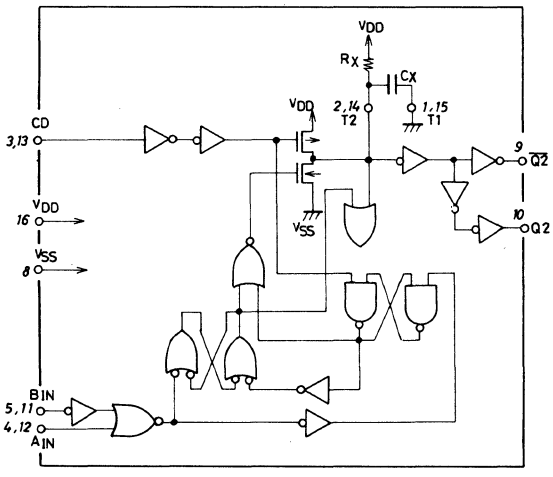
Functions, Features

- Wide operating voltage range, high noise margin, low power dissipation.
- A dual, retriggerable, resettable monostable multivibrator.
- Triggering from leading edge (AIN) or trailing edge (BIN).
- Wide range of output pulse width obtainable by adjusting external resistor (R_X). and external capactior (C_X).
- Asynchronous reset can be provided externally by setting input C_D to "L" level. Input C_D can be used as trigger inhibit input or can be used to shorten the period of time that elapses between the moment power is applied and the moment monostable operation mode is entered.

Pin Assignment & Circuit Configuration (top view)



Equivalent Circuit (LC4528B 1/2)

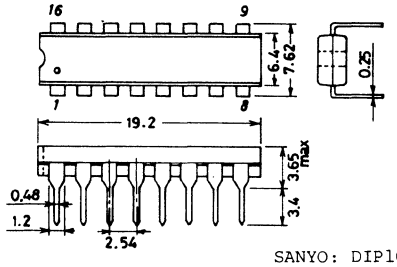


Truth Table

IN PUT			OUT PUT		Note
A	B	C_D	Q	Q̄	
↑	1	1	⎍	⎏	OUTPUT PULSE
↑	0	1	0	1	INHIBIT
1	↓	1	0	1	INHIBIT
0	↓	1	⎍	⎏	OUTPUT PULSE
*	*	0	0	1	INHIBIT

1 : ⌈H⌋ Level
0 : ⌈L⌋ Level
*: don't care

Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}		$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}		$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leqq 85$°C	300	mW
Operating Temperature	T_{opg}		−40～+85	°C
Storage Temperature	T_{stg}		−65～+150	°C
Lead Temperature and Time		10 sec.	260	°C

Allowable Operating Range at T_a=25±2°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD}	T_a=−40°C～+85°C	3～18	V
Input Voltage	V_{IN}	T_a=−40°C～+85°C	0～V_{DD}	V
External Resistance	R_X		5～1000	kΩ
External Capacitance	C_X		no limite	μF

Electrical Characteristics at T_a=−40°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.5			mA
		V_{DD}=10V, V_O=9.5V, 〃	−1.0			mA
		V_{DD}=15V, V_O=13.5V, 〃	−3.5			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}	0.5			mA
		V_{DD}=10V, V_O=0.5V, 〃	1.0			mA
		V_{DD}=15V, V_O=1.5V, 〃	3.5			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|$<1μA	3.5			V
		V_{DD}=10V, V_O=1.0Vor9.0V, 〃	7.0			V
		V_{DD}=15V, V_O=1.5Vor13.5V, 〃	11.0			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=0.5Vor4.5V, $\|I_{OUT}\|$<1μA			1.5	V
		V_{DD}=10V, V_O=1.0Vor9.8V, 〃			3.0	V
		V_{DD}=15V, V_O=1.5Vor13.5V, 〃			4.0	V
Input Leak Voltage	I_{IN}	V_{DD}=18V, V_{IN}=18V			1.0	μA
		V_{DD}=18V, V_{IN}=0V			−1.0	μA
Quiescent Device Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}			1.0	μA
		V_{DD}=10V, 〃			2.0	μA
		V_{DD}=15V, 〃			4.0	μA

Electrical Characteristics at T_a=25±2°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	4.95	5.00		V
		V_{DD}=10V, 〃 〃	9.95	10.00		V
		V_{DD}=15V, 〃 〃	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}		0.00	0.05	V
		V_{DD}=10V, 〃 〃		0.00	0.05	V
		V_{DD}=15V, 〃 〃		0.00	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}, V_{DD}	−0.5	−1.0		mA
		V_{DD}=10V, V_O=9.5V, 〃	−1.0	−2.0		mA
		V_{DD}=15V, V_O=13.5V, 〃	−3.5	−7.0		mA

(continued on next page)

			min	typ	max	unit
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.5	1.0		mA
		$V_{DD}=10V, V_O=0.5V,$ 〃	1.0	2.0		mA
		$V_{DD}=15V, V_O=1.5V,$ 〃	3.5	7.0		mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5	2.5		V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V,$ 〃	7.0	5.0		V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V,$ 〃	11.0	7.5		V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$		2.5	1.5	V
		$V_{DD}=10V, V_O=1.0V$ or $9.8V$ 〃		5.0	3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V,$ 〃		7.5	4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$		10^{-5}	1.0	μA
		$V_{DD}=18V, V_{IN}=0V$		-10^{-5}	−1.0	μA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}$		0.01	1.0	μA
		$V_{DD}=10V,$ 〃		0.01	2.0	μA
		$V_{DD}=15V,$ 〃		0.01	4.0	μA
Input Stray Capacitance	C_{IN}	All inputs		5.0	7.5	pF

Electrical Characteristics at T_a=85°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}, V_{DD}$	4.95			V
		$V_{DD}=10V,$ 〃 〃	9.95			V
		$V_{DD}=15V,$ 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	$V_{DD}=5V, \lvert I_{OUT}\rvert<1\mu A, V_{IN}=V_{SS}, V_{DD}$			0.05	V
		$V_{DD}=10V,$ 〃 〃			0.05	V
		$V_{DD}=15V,$ 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	$V_{DD}=5V, V_O=4.6V, V_{IN}=V_{SS}, V_{DD}$	−0.4			mA
		$V_{DD}=10V, V_O=9.5V,$ 〃	−0.8			mA
		$V_{DD}=15V, V_O=13.5V,$ 〃	−2.8			mA
"L" Level Output Current	I_{OL}	$V_{DD}=5V, V_O=0.4V, V_{IN}=V_{SS}, V_{DD}$	0.4			mA
		$V_{DD}=10V, V_O=0.5V,$ 〃	0.8			mA
		$V_{DD}=15V, V_O=1.5V,$ 〃	2.8			mA
"H" Level Input Voltage	V_{IH}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$	3.5			V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V,$ 〃	7.0			V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V,$ 〃	11.0			V
"L" Level Input Voltage	V_{IL}	$V_{DD}=5V, V_O=0.5V$ or $4.5V, \lvert I_{OUT}\rvert<1\mu A$			1.5	V
		$V_{DD}=10V, V_O=1.0V$ or $9.8V,$ 〃			3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V,$ 〃			4.0	V
Input Leak Current	I_{IN}	$V_{DD}=18V, V_{IN}=18V$			1.0	μA
		$V_{DD}=18V, V_{IN}=0V$			−1.0	μA
Quiescent Device Current	I_{DD}	$V_{DD}=5V, V_{IN}=V_{DD}, V_{SS}$			7.5	μA
		$V_{DD}=10V,$ 〃			15.0	μA
		$V_{DD}=15V,$ 〃			30	μA

Note) Current direction: +, no sign: Flowing into SSI,
−: Flowing out of SSI.

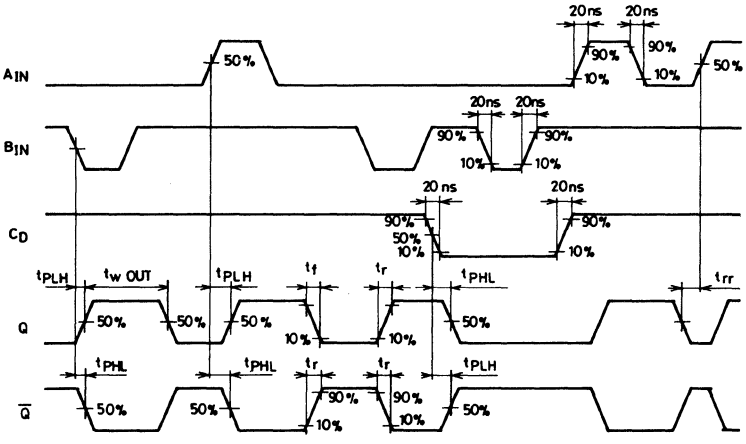
Switching Characteristics at T_a=25±2°C, CL=50pF, V_{SS}=0V

			min	typ	max	unit
Output Rise Time	t_r	$V_{DD}=5V$		130	400	ns
		$V_{DD}=10V$		65	200	ns
		$V_{DD}=15V$		50	160	ns
Output Fall Time	t_f	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns

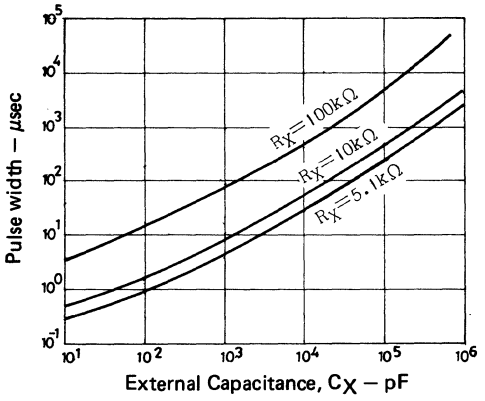
(continued on next page)

			min	typ	max	unit
"H" Level Propagation Delay Time (Ain, Bin→Q, $\overline{Q}$)	t_{PLH}	V_{DD}=5V, C_X=15pF, R_X=5kΩ		850	1600	ns
		V_{DD}=10V, 〃 〃		300	600	ns
		V_{DD}=15V, 〃 〃		200	400	ns
"L" Level Propagation Delay Time (Ain, Bin→Q, $\overline{Q}$)	t_{PHL}	V_{DD}=5V, 〃 〃		850	1600	ns
		V_{DD}=10V, 〃 〃		300	600	ns
		V_{DD}=15V, 〃 〃		200	400	ns
"H" Level Propagation Delay Time (Ain, Bin→Q, $\overline{Q}$)	t_{PLH}	V_{DD}=5V, C_X=10000pF, R_X=10kΩ		6.0	12	μs
		V_{DD}=10V, 〃 〃		2.0	5	μs
		V_{DD}=15V, 〃 〃		1.3	3	μs
"L" Level Propagation Delay Time (Ain, Bin→Q, $\overline{Q}$)	t_{PHL}	V_{DD}=5V, 〃 〃		6.0	12	μs
		V_{DD}=10V, 〃 〃		2.0	5	μs
		V_{DD}=15V, 〃 〃		1.3	3	μs
Propagation Delay Time (C_D→Q, $\overline{Q}$)	(t_{PLH} t_{PHL})	V_{DD}=5V, C_X=15pF, R_X=5kΩ		600	1200	ns
		V_{DD}=10V, 〃 〃		210	500	ns
		V_{DD}=15V, 〃 〃		160	400	ns
Propagation Delay Time (C_D→Q, $\overline{Q}$)	(t_{PLH} t_{PHL})	V_{DD}=5V, C_X=10000pF, R_X=10kΩ		5.5		μs
		V_{DD}=10V, 〃 〃		4.6		μs
		V_{DD}=15V, 〃 〃		4.0		μs
Minimum Trigger Pulse Width (Ain, Bin)	$t_{W(in)}$	V_{DD}=5V, C_X=15pF, R_X=5kΩ		130	450	ns
		V_{DD}=10V, 〃 〃		65	200	ns
		V_{DD}=15V, 〃 〃		60	150	ns
Minimum Trigger Time	t_{rr}	V_{DD}=5V, 〃 〃		0		ns
		V_{DD}=10V, 〃 〃		0		ns
		V_{DD}=15V, 〃 〃		0		ns
		V_{DD}=5V, C_X=10000pF, R_X=10kΩ		0		ns
		V_{DD}=10V, 〃 〃		0		ns
		V_{DD}=15V, 〃 〃		0		ns
Output Pulse Width	$t_{W\ OUT}$	V_{DD}=5V, C_X=15pF, R_X=5kΩ		350		ns
		V_{DD}=10V, 〃 〃		300		ns
		V_{DD}=15V, 〃 〃		250		ns
		V_{DD}=5V, C_X=10000pF, R_X=10kΩ	15	35	55	μs
		V_{DD}=10V, 〃 〃	25	50	75	μs
		V_{DD}=15V, 〃 〃	40	65	90	μs

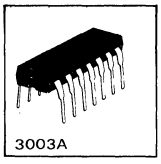
Switching Time Test Circuit and Waveform



Characteristics of output pulse width at IC typ value



LC4584B



C MOS IC

Hex Schmitt Trigger

The LC4584B is a Schmitt inverter IC (B series) having such features as wide operating voltage range, high noise margin, low power dissipation.

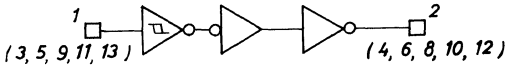
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD} max		V_{SS}-0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	Pdmax		300	mW
Lead Temperature and Time	Tsol	t=10sec	260	°C
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

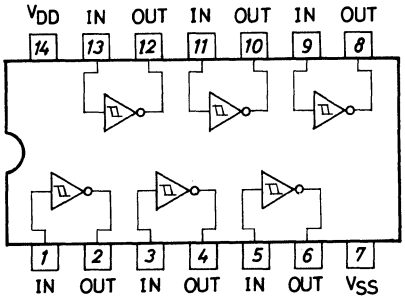
Allowable Operating Range at Ta=-40 to +85°C

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

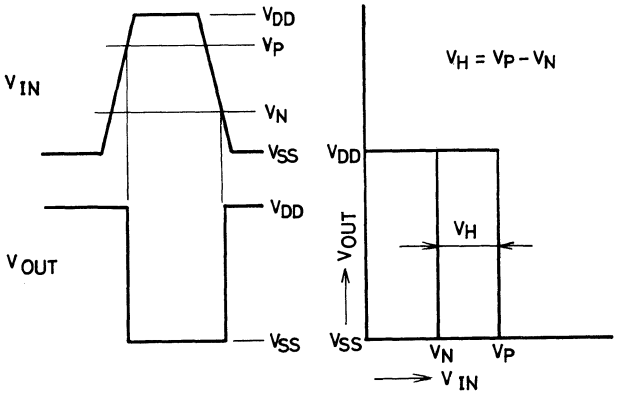
Logic Diagram



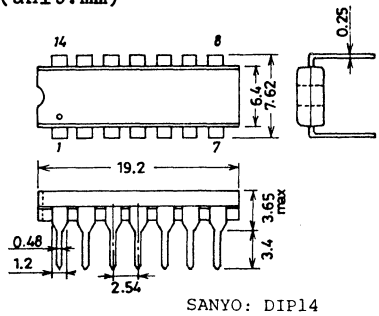
Pin Assignment



Input/Output Characteristic



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

Electrical Characteristics at Ta=-40°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, I_{OUT} <1uA, Vin=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, I_{OUT} <1uA, Vin=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS}	-0.52			mA
		V_{DD}=10V, Vo=9.5V, "	-1.3			mA
		V_{DD}=15V, Vo=13.5V, "	-3.6			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{DD}	0.52			mA
		V_{DD}=10V, Vo=0.5V, "	1.3			mA
		V_{DD}=15V, Vo=1.5V, "	3.6			mA
"H" Level Threshold Voltage	V_{IH}	V_{DD}=5V, Vo=0.4V, I_{OUT} <1uA	3.5			V
		V_{DD}=10V, Vo=0.5V, "	7.0			V
("H" Level Input Voltage)		V_{DD}=15V, Vo=1.5V, "	11.0			V
"L" Level Threshold Voltage	V_{IL}	V_{DD}=5V, Vo=4.6V, I_{OUT} <1uA			1.5	V
		V_{DD}=10V, Vo=9.5V, "			3.0	V
("L" Level Input Voltage)		V_{DD}=15V, Vo=13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V			0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V			-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V			1.0	uA
		V_{DD}=10V			2.0	uA
		V_{DD}=15V			4.0	uA

Current Direction : +, no sign: Flowing into device
- : Flowing out of device

Electrical Characteristics at Ta=25°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, I_{OUT} <1uA, Vin=V_{SS}	4.95	5.00		V
		V_{DD}=10V, " "	9.95	10.00		V
		V_{DD}=15V, " "	14.95	15.00		V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, I_{OUT} <1uA, Vin=V_{DD}		0	0.05	V
		V_{DD}=10V, " "		0	0.05	V
		V_{DD}=15V, " "		0	0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS}	-0.44	-0.88		mA
		V_{DD}=10V, Vo=9.5V, "	-1.1	-2.25		mA
		V_{DD}=15V, Vo=13.5V, "	-3.0	-8.8		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{SS}, V_{DD}	0.44	0.88		mA
		V_{DD}=10V, Vo=0.5V, "	1.1	2.25		mA
		V_{DD}=15V, Vo=1.5V, "	3.0	8.8		mA
"H" Level Threshold Voltage	V_{IH}	V_{DD}=5V, Vo=4.6V, I_{OUT} 1uA	3.5	2.75		V
		V_{DD}=10V, Vo=9.5V, "	7.0	5.5		V
("H" Level Input Voltage)		V_{DD}=15V, Vo=13.5V, "	11.0	8.25		V
"L" Level Threshold Voltage	V_{IL}	V_{DD}=5V, Vo=4.6V, I_{OUT} <1uA		2.25	1.5	V
		V_{DD}=10V, Vo=9.5V		4.5	3.0	V
("H" Level Input Voltage)		V_{DD}=15V, Vo=13.5V		6.75	4.0	V
Hysteresis Voltage	V_H	V_{DD}=5V	0.5	1.0	2.0	V
		V_{DD}=10V	1.0	2.0	4.0	V
		V_{DD}=15V	2.0	4.0	6.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V		10	0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V		-10	-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V		0.0005	1.0	uA
		V_{DD}=10V		0.001	2.0	uA
		V_{DD}=15V		0.0015	4.0	uA
Input Capacitance	C_{IN}			5	7.5	pF

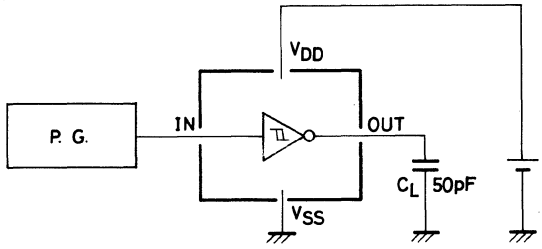
Current Direction : +, no sign: Flowing into device
- : Flowing out of device

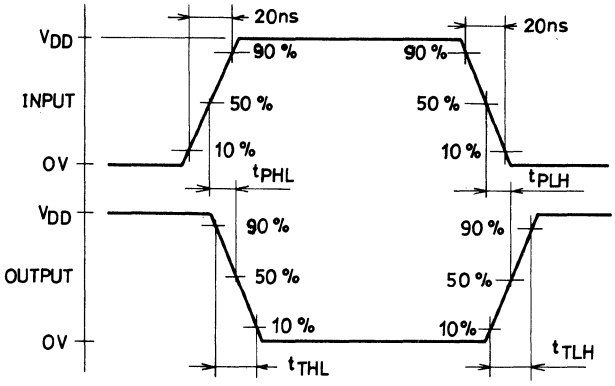
Electrical Characteristics at Ta=+85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, I_{OUT} <1uA, Vin=V_{SS}	4.95			V
		V_{DD}=10V, " "	9.95			V
		V_{DD}=15V, " "	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, I_{OUT} <1uA, Vin=V_{DD}			0.05	V
		V_{DD}=10V, " "			0.05	V
		V_{DD}=15V, " "			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, Vo=4.6V, Vin=V_{SS}	-0.36			mA
		V_{DD}=10V, Vo=9.5V, "	-0.9			mA
		V_{DD}=15V, Vo=13.5V, "	-2.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, Vo=0.4V, Vin=V_{DD}	0.36			mA
		V_{DD}=10V, Vo=0.5V, "	0.9			mA
		V_{DD}=15V, Vo=1.5V, "	2.4			mA
"H" Level Threshold Voltage ("H" Level Input Voltage)	V_{IH}	V_{DD}=5V, Vo=0.4V, I_{OUT} <1uA	3.5			V
		V_{DD}=10V, Vo=0.5V, "	7.0			V
		V_{DD}=15V, Vo=1.5V, "	11.0			V
"L" Level Threshold Voltage ("L" Level Input Voltage)	V_{IL}	V_{DD}=5V, Vo=4.6V, I_{OUT} <1uA			1.5	V
		V_{DD}=10V, Vo=9.5V, "			3.0	V
		V_{DD}=15V, Vo=13.5V, "			4.0	V
"H" Level Input Current	I_{IH}	V_{DD}=18V, Vin=18V			0.3	uA
"L" Level Input Current	I_{IL}	V_{DD}=18V, Vin=0V			-0.3	uA
Quiescent Device Current	I_{DD}	V_{DD}=5V			1.0	uA
		V_{DD}=10V			2.0	uA
		V_{DD}=15V			4.0	uA

Current Direction : +,no sign: Flowing into device
- : Flowing out of device

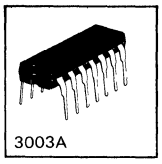
Switching Characteristics at Ta=25±2°C, V_{SS}=0V, C_L=50pF			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		125	250	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Output Rise Time	t_r (t_{TLH})	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Output Fall Time	t_f (t_{THL})	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching Time Test Circuit and Waveform





LC4913



C MOS IC

Dual Dff with Schmitt Trigger

TENTATIVE

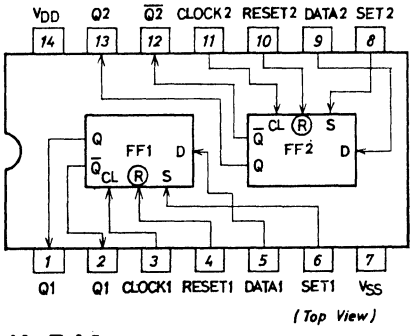
Case Outline : 14-pin DIP plastic package

Use : C-MOS standard logic IC for logic circuit

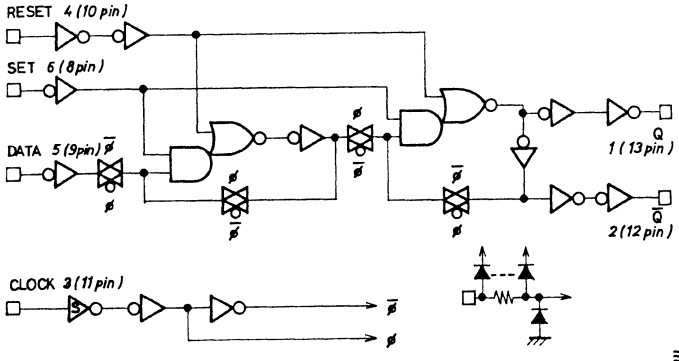
Features and Function : Dual D type flip-flop having such features as wide operating voltage range, high noise margin, low power dissipation.

Pin Assignment, Circuit Configuration, and Equivalent Circuit

.Pin Assignment and Circuit Configuration



. Equivalent Circuit Diagram (1/2 LC4913B)



Truth Table

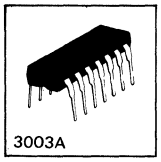
INPUTS				OUTPUTS	
CL△	D	S	Ⓡ	Q_{n+1}	$\overline{Q_{n+1}}$
*	*	H	L	H	L
*	*	L	H	L	H
*	*	H	H	L	H
↑	L	L	L	L	H
↑	H	L	L	H	L
↓	*	L	L	Q_n•	$\overline{Q_n}$•

* : Don't Care
△ : Level Change
• : No Change

Electrical Characteristics

Absolute Maximum Ratings at Ta=25°C±2°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		V_{SS}-0.5		V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}-0.5		V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5		V_{DD}+0.5	V
Input Current	I_{IN}				±10	mA
Output Current	I_{OUT}				-	mA
Allowable Power Dissipation	Pd	Ta≦85°C, I_{IN}=±10mA			300	mW
Operating Temperature	Topg		-40		+85	°C
Storage Temperature	Tstg		-65		+150	°C
Lead Temperature and Time	Tsol			260°C	10sec.	

LC4966



C MOS IC

CMOS Logic
Quad Bilateral Switch

Ⓔ 1536

The LC4966 is identical to the LC4066B,LC4066BH in functions, but has a wider operating voltage range. It consists of four independent switches. Setting the control inut (CONT) at "H" level causes the switches to be conducting, thereby resulting in a low impedance between input and output; and setting the control input (CONT) at "L" level causes the switches to be nonconducting, thereby resulting in a high impedance between input and output.

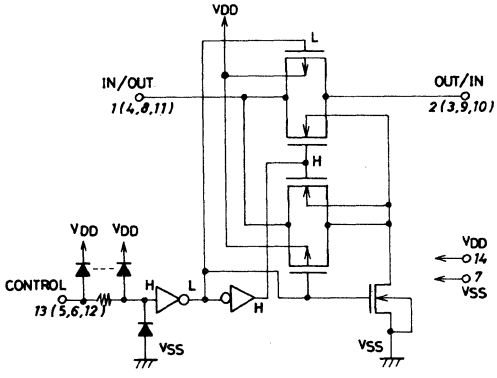
Absolute Maximum Ratings at T=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		V_{SS}-0.5 to V_{SS}+40	V
Input Voltage	V_{IN}		V_{SS}-0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
On-State Voltage Drop between Input and Output	V_I-V_O		±0.5	V
Lead Temperature & Time	Tsol	t=10sec	260	°C
Allowable Power Dissipation	Pdmax	Ta≦85°C, I_{IN}=±10mA	300	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

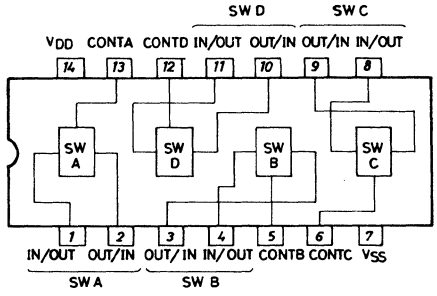
Allowable Operating Range at Ta=-40 to +85°C

			unit
Supply Voltage	V_{DD}	3 to 37	V
Input Voltage	V_{IN}	0 to V_{DD}	V

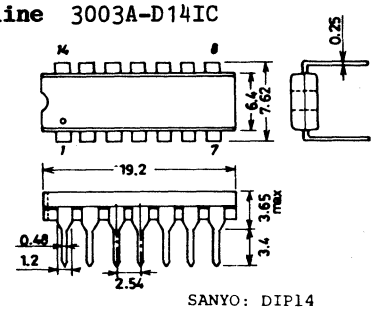
Equivalent Circuit
(1/4 LC4966)



Pin Assignment and Equivalent Circuit Block Diagram



Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

Electrical Characteritics	at Ta=25±2°C, V_{SS}=0V		min	typ	max	unit
Input "H" Level Control Voltage	V_{IH}	V_{DD}=5V, Current between input and output=10uA	4.0	2.5		V
		V_{DD}=10V, Current between input and output=10uA	5.0	3.5		V
		V_{DD}=15V, Current between input and output=10uA	5.5	4.0		V
		V_{DD}=20V, Current between input and output=10uA	6.5	4.5		V
		V_{DD}=25V, Current between input and output=10uA	7.0	5.0		V
		V_{DD}=30V, Current between input and output=10uA	8.0	5.5		V
		V_{DD}=35V, Current between input and outut=10uA	8.0	5.5		V
		V_{DD}=37V, Current between input and output=10uA	8.0	5.5		V
Input "L" Level Control Voltage	V_{IL}	V_{DD}=5V, Current between input and output=10uA		2.5	1.0	V
		V_{DD}=10V, Current between input and output=10uA		3.5	2.0	V
		V_{DD}=15V, Current between input and output=10uA		4.0	2.5	V
		V_{DD}=20V, Current between input and output=10uA		4.5	2.5	V
		V_{DD}=25V, Current between input and output=10uA		5.0	3.0	V
		V_{DD}=30V, Current between input and output=10uA		5.5	3.0	V
		V_{DD}=35V, Current between input and output=10uA		5.5	3.0	V
		V_{DD}=37V, Current between input and output=10uA		5.5	3.0	V
ON Resistance	R_{ON}	V_{DD}=5V, V_{IN}=5V, I=±1mA		110	220	ohm
		V_{DD}=5V, V_{IN}=2.5V, "		90	180	ohm
		V_{DD}=5V, V_{IN}=0.25V, "		110	220	ohm
		V_{DD}=10V, V_{IN}=10V, I=±3mA		70	140	ohm
		V_{DD}=10V, V_{IN}=5V, "		50	100	ohm
		V_{DD}=10V, V_{IN}=0.25V, "		70	140	ohm
		V_{DD}=15V, V_{IN}=15V, I=±3mA		60	120	ohm
		V_{DD}=15V, V_{IN}=7.5V, "		40	80	ohm
		V_{DD}=15V, V_{IN}=0.25V, "		60	120	ohm
		V_{DD}=20V, V_{IN}=20V, I=±3mA		60	120	ohm
		V_{DD}=20V, V_{IN}=10V, "		40	80	ohm
		V_{DD}=20V, V_{IN}=0.25V, "		60	120	ohm
		V_{DD}=30V, V_{IN}=30V, I=±3mA		50	100	ohm
		V_{DD}=30V. V_{IN}=15V, "		35	70	ohm
		V_{DD}=30V, V_{IN}=0.25V, "		50	100	ohm
		V_{DD}=37V, V_{IN}=38V, I=±3mA		45	90	ohm
		V_{DD}=37V, V_{IN}=19V, "		30	60	ohm
		V_{DD}=37V, V_{IN}=0.25V, "		45	90	ohm
		V_{DD}=5V, V_{SS}=-5V, V_{IN}=5V, I=3mA		70	140	ohm
		V_{DD}=5V, V_{SS}=-5V, V_{IN}=±0.25V, "		50	100	ohm
		V_{DD}=5V, V_{SS}=-5V, V_{IN}=-5V, "		70	140	ohm

			min	typ	max	unit
On Resistance	R_{ON}	V_{DD}=7.5V,V_{SS}=-7.5V,V_{IN}=5V,I=3mA		60	120	ohm
		V_{DD}=7.5V,V_{SS}=-7.5V,V_{IN}=±0.25V, I=3mA		40	80	ohm
		V_{DD}=7.5V,V_{SS}=-7.5V,V_{IN}=-5V, I=3mA		60	120	ohm
		V_{DD}=10V,V_{SS}=-10V,V_{IN}=10V,I=±3mA		60	120	ohm
		V_{DD}=10V,V_{SS}= -10V,V_{IN}=±0.25V, I=±3mA		40	80	ohm
		V_{DD}=10V,V_{SS}=-10V,V_{IN}=-10V, I=±3mA		60	120	ohm
		V_{DD}=15V,V_{SS}=-15V,V_{IN}=15V,I=±3mA		50	100	ohm
		V_{DD}=15V,V_{SS}=-15V,V_{IN}=±0.25V, I=±3mA		35	70	ohm
		V_{DD}=15V,V_{SS}=-15V,V_{IN}=-15V,I=±3mA		50	100	ohm
		V_{DD}=18.5V,V_{SS}=-18.5V, V_{IN}=19V,=±3mA		45	90	ohm
		V_{DD}=18.5V,V_{SS}=-18.5V, V_{IN}=±0.25V,I=±3mA		30	60	ohm
		V_{DD}=18.5V,V_{SS}=-18.5V, V_{IN}=-19V,I=±3mA		45	90	ohm
Input/Output OFF Leak Current	I_{OFF}	V_{DD}=37V,V_{IN}=38V,V_{OUT}=0V		±1	±500	nA
		V_{DD}=37V,V_{IN}=0V,V_{OUT}=38V		±1	±500	nA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V		0.001	1	uA
		V_{DD}=10V		0.001	2	uA
		V_{DD}=15V		0.002	4	uA
		V_{DD}=20V		0.004	8	uA
		V_{DD}=25V		0.01	20	uA
		V_{DD}=30V		0.02	40	uA
		V_{DD}=35V		0.04	80	uA
		V_{DD}=37V		0.1	160	uA
Input "H" Level Control Current	I_{IH}	V_{DD}=37V,V_{IN}=38V		10	3	uA
Input "L" Level Control Current	I_{IL}	V_{DD}=37V,V_{IN}=0V		-10	3	uA
Input Capacitance	C_{IN}	Control input		5	7.5	pF
		Switch I/O		10		pF

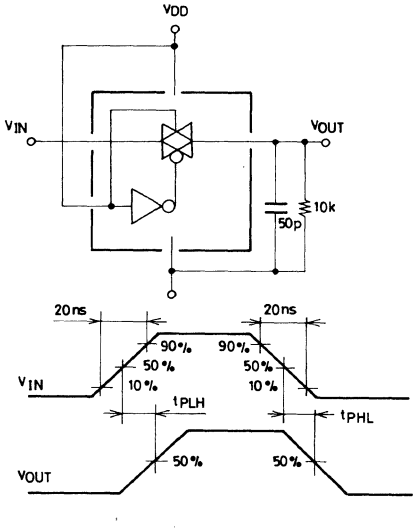
Switching Characteristics	at Ta=25°C±2°C		min	typ	max	unit
Propagation Delay Time (Input-Output)	t_{PLH} t_{PHL}	V_{DD}=5V,R_L=10kohm,C_L=50pF		15	45	ns
		V_{DD}=10V, "		10	30	ns
		V_{DD}=15V, "		8	25	ns
		V_{DD}=20V, "		8	25	ns
		V_{DD}=25V, "		8	25	ns
		V_{DD}=30V, "		7	25	ns
		V_{DD}=35V, "		7	25	ns
		V_{DD}=37V, "		7	25	ns
Propagation Delay Time (Control-Out)	t_{PLH} t_{PHL}	V_{DD}=5V,R_L=10kohm,C_L=50pF		100	200	ns
		V_{DD}=10V, "		40	70	ns
		V_{DD}=15V, "		35	60	ns
		V_{DD}=20V, "		35	60	ns
		V_{DD}=25V, "		35	60	ns
		V_{DD}=30V, "		35	60	ns
		V_{DD}=35V, "		35	60	ns
		V_{DD}=37V, "		35	60	ns

			min	typ	max	unit
Maximum Control Input Frequency	f max (C)	V_{DD}=5V, C_L=15pF		1.0		MHz
		V_{DD}=10V, "		1.0		MHz
		V_{DD}=20V, "		1.0		MHz
		V_{DD}=30V, "		1.0		MHz
		V_{DD}=37V, "		1.0		MHz
Maximum Propagation Frequency	f max (I-O)	V_{DD}=5V, V_{SS}=-5V, R_L=10kohm, C_L=15pF *1		35		MHz
		V_{DD}=10V, V_{SS}=-10V		40		MHz
		V_{DD}=15V, V_{SS}=-15V		50		MHz
		V_{DD}=18.5V, V_{SS}=-18.5V		50		MHz
Sine Wave Propagation Distortion Ratio		V_{DD}=5V, V_{SS}=-5V, R_L=10kohm, f=1kHz *2		0.010		%
		V_{DD}=10V, V_{SS}=-10V		0.005		%
		V_{DD}=15V, V_{SS}=-15V		0.005		%
		V_{DD}=18.5V, V_{SS}=-18.5V		0.005		%
Feed Through (Switch-Off)		V_{DD}=5V, V_{SS}=-5V, R_L=10kohm, *3		1		MHz
		V_{DD}=10V, V_{SS}=-10V		1		MHz
		V_{DD}=15V, V_{SS}=-15V		1		MHz
		V_{DD}=18.5V, V_{SS}=-18.5V		1		MHz

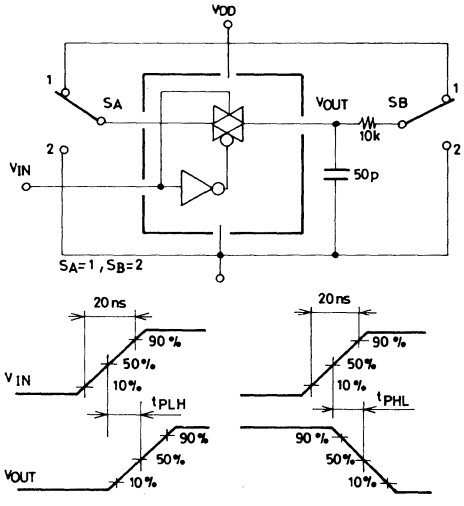
(Note) *1 Vis : ±2.5Vp-p sine wave fmax: 20log 10(Vos/Vis)=-3dB.
*2 Vis : ±2.5Vp-p sine wave.
*3 Vis : ±2.5Vp-p sine wave f_{FEED} THROUGH: 20log(Vos/Vis)=-50dB

Test Circuit and Waveform

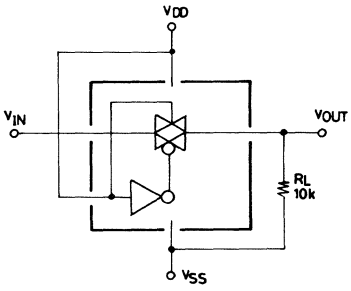
1. t_{PLH}, t_{PHL}(INT OUT) Test Circuit



2. t_{PLH}, t_{PHL}(CONTROL OUT) Test Circuit

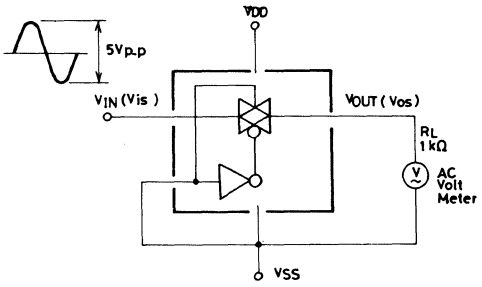


3. R_{ON} Test Circuit



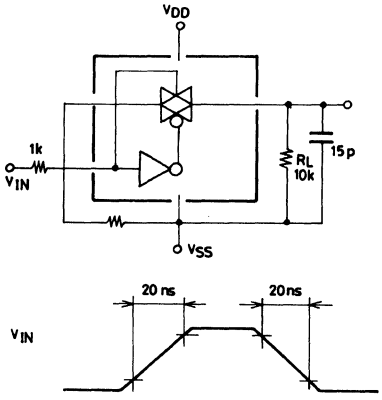
$$R_{ON} = \frac{(V_{IN} - V_{OUT})}{V_{OUT}} \times 10\ k\Omega$$

4. Feed Through Test Circuit

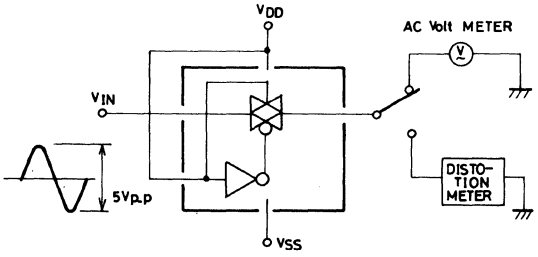


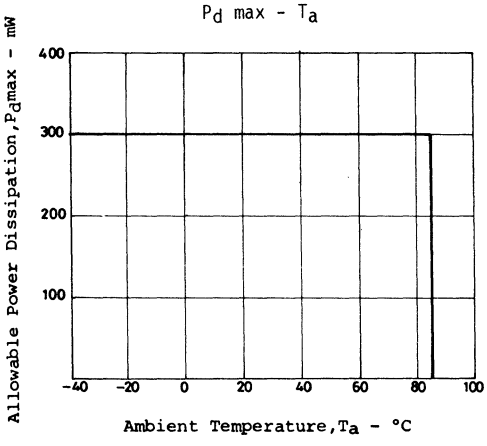
$$f : 20 \log 10 \frac{V_{os}}{V_{is}} = -50\,dB$$

5. Crosstalk

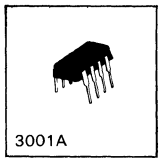


6. Frequency Response (fmax)





LC4969



C MOS IC

CMOS Logic Triple Inverter

Ⓔ 1102B

The LC4969 is a triple inverter (EIA/JEDEC standards-met IC product) having such features as wide operating voltage range, high noise immunity, low power dissipation, etc.

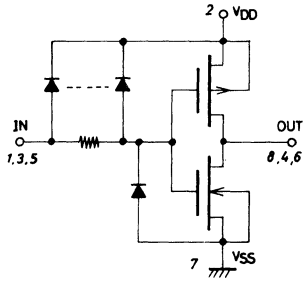
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		V_{SS}−0.5 to V_{SS}+20	V
Input Voltage	V_{IN}		V_{SS}−0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}−0.5 to V_{DD}+0.5	V
Input Current	I_{IN}		±10	mA
Allowable Power Dissipation	P_d max	$T_a \leq 85°C$	150	mW
Lead Temperature. Time	T_{sol}	t=10sec	260	°C
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

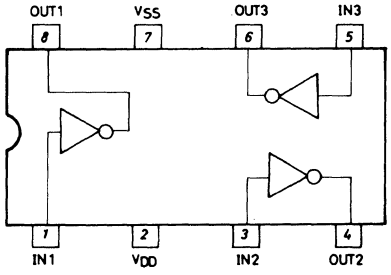
Allowable Operating Ranges/T_a=−40 to +85°C, V_{SS}=0V

			unit
Supply Voltage	V_{DD}	3 to 18	V
Input Voltage	V_{IN}	0 to V_{DD}	V

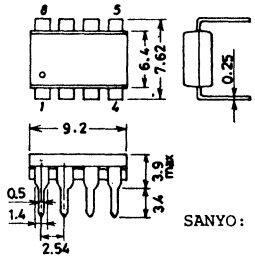
Equivalent Circuit (1/3 LC4969)



Pin Assignement and Block Diagram



Case Outline 3001A-D8IC
(unit:mm)



SANYO: DIP8

Electrical Characteristics/T_a=−40°C, V_{SS}=0V

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	−0.61			mA
		V_{DD}=10V, V_o=9.5V, 〃	−1.5			mA
		V_{DD}=15V, V_o=13.5V, 〃	−4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.61			mA
		V_{DD}=10V, V_o=0.5V, 〃	1.5			mA
		V_{DD}=15V, V_o=1.5V, 〃	4			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1μA	4			V
		V_{DD}=10V, V_o=1.0V, 〃	8			V
		V_{DD}=15V, V_o=1.5V, 〃	12.5			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1μA			1.0	V
		V_{DD}=10V, V_o=9.0V, 〃			2.0	V
		V_{DD}=15V, V_o=13.5V 〃			2.5	V
Input Current	I_{IN}	V_{DD}=18V			±1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}※			0.25	μA
		V_{DD}=10V, 〃			0.5	μA
		V_{DD}=15V, 〃			1.0	μA

*: All input pins connected.

Electrical Characteristics/T_a=25°C, V_{SS}=0

			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	−0.51	−1.0		mA
		V_{DD}=10V, V_o=9.5V, 〃	−1.3	−2.6		mA
		V_{DD}=15V, V_o=13.5V, 〃	−3.4	−6.8		mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.51	1.0		mA
		V_{DD}=10V, V_o=0.5V, 〃	1.3	2.6		mA
		V_{DD}=15V, V_o=1.5V, 〃	3.4	6.8		mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1μA	4			V
		V_{DD}=10V, V_o=1.0V 〃	8			V
		V_{DD}=15V, V_o=1.5V, 〃	12.5			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1μA			1.0	V
		V_{DD}=10V, V_o=9.0V, 〃			2.0	V
		V_{DD}=15V, V_o=13.5V, 〃			2.5	V
Input Current	I_{IN}	V_{DD}=18V		$\pm 10^{-5}$	±1.0	μA
Quiescent Current Dissipation	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}※		0.01	0.25	μA
		V_{DD}=10V, 〃		0.01	0.5	μA
		V_{DD}=15V, 〃		0.01	1.0	μA
Input Capacitance	C_{IN}			7.5	15	pF

*: All input pins connected.

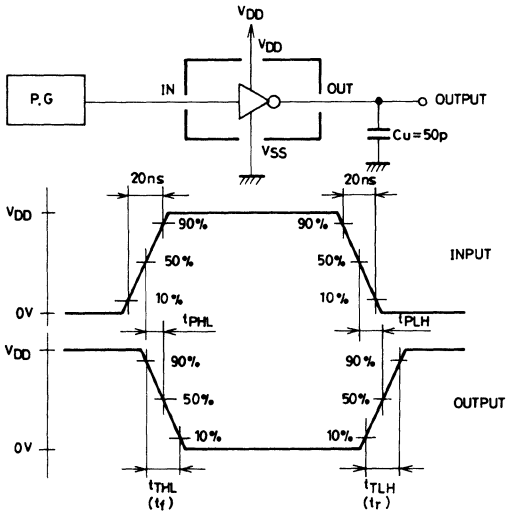
Electrical Characteristics/T_a=85°C, V_{SS}=0V			min	typ	max	unit
"H" Level Output Voltage	V_{OH}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}	4.95			V
		V_{DD}=10V, 〃 〃	9.95			V
		V_{DD}=15V, 〃 〃	14.95			V
"L" Level Output Voltage	V_{OL}	V_{DD}=5V, $\|I_{OUT}\|$<1μA, V_{IN}=V_{DD}			0.05	V
		V_{DD}=10V, 〃 〃			0.05	V
		V_{DD}=15V, 〃 〃			0.05	V
"H" Level Output Current	I_{OH}	V_{DD}=5V, V_o=4.6V, V_{IN}=V_{SS}	−0.36			mA
		V_{DD}=10V, V_o=9.5V, 〃	−0.9			mA
		V_{DD}=15V, V_o=13.5V, 〃	−2.4			mA
"L" Level Output Current	I_{OL}	V_{DD}=5V, V_o=0.4V, V_{IN}=V_{DD}	0.36			mA
		V_{DD}=10V, V_o=0.5V, 〃	0.9			mA
		V_{DD}=15V, V_o=1.5V, 〃	2.4			mA
"H" Level Input Voltage	V_{IH}	V_{DD}=5V, V_o=0.5V, $\|I_{OUT}\|$<1μA	4			V
		V_{DD}=10V, V_o=1.0V, 〃	8			V
		V_{DD}=15V, V_o=1.5V, 〃	12.5			V
"L" Level Input Voltage	V_{IL}	V_{DD}=5V, V_o=4.5V, $\|I_{OUT}\|$<1μA			1.0	V
		V_{DD}=10V, V_o=9.0V, 〃			2.0	V
		V_{DD}=15V, V_o=13.5V, 〃			2.5	V
Input Current	I_{IN}	V_{DD}=18V			±1.0	μA
Quiescent Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{SS}, V_{DD}※			7.5	μA
Dissipation		V_{DD}=10V, 〃			15	μA
		V_{DD}=15V, 〃			30	μA

*: All input pins connected.

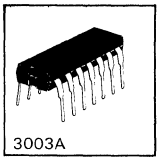
Note) Current direction: (+, no sign: Flowing into device, −: Flowing out of device).

Switching Characteristics/T_a=25±2°C, C_u=50pF, V_{SS}=0V			min	typ	max	unit
"H" Level Propagation Delay Time	t_{PLH}	V_{DD}=5V		100	180	ns
		V_{DD}=10V		60	120	ns
		V_{DD}=15V		50	100	ns
"L" Level Propagation Delay Time	t_{PHL}	V_{DD}=5V		75	150	ns
		V_{DD}=10V		40	100	ns
		V_{DD}=15V		35	80	ns
Output Rise Time	t_{TLH} (t_r)	V_{DD}=5V		130	400	ns
		V_{DD}=10V		65	200	ns
		V_{DD}=15V		50	160	ns
Output Fall Time	t_{THL} (t_f)	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns

Switching Time Test Circuit and Waveforms



LC74HC00



C MOS IC

Quad 2-Input NAND Gate

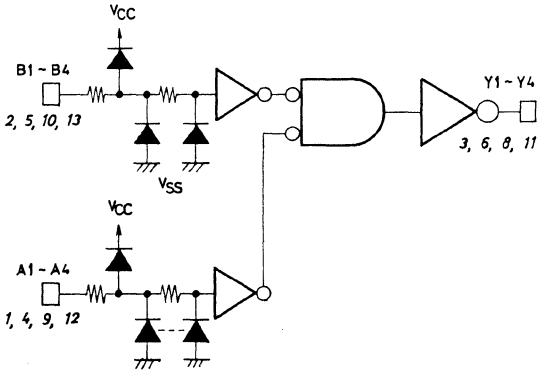
PRELIMINARY

1. The LC74HC00 consists of 4 identical 2-input NAND gates.
2. Uses CMOS silicon gate process technology to achieve operating speeds similar to LSTTL (74LS00) gates with the low power dissipation and high noise margin of standard CMOS IC's.
3. Has buffered outputs, improving the input-output propagation characteristic.
4. All inputs and outputs are protected from damage.
5. The LC74HC00 is functionally as well as pin-out compatible with the standard 54LS/74LS TTL logic family.

Absolute Maximum Ratings at Ta=25°C±2°C, V_{SS}=0V

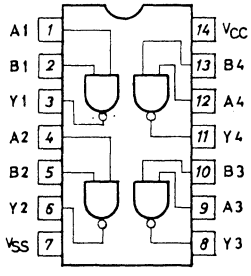
			min	typ	max	unit
Supply Voltage	V_{CC}		V_{SS}-0.5		V_{SS}+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.5		V_{CC}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5		V_{CC}+0.5	V
Output Current	I_{OUT}	Per output			±25	mA
Current Dissipation	I_{CC}/I_{GND}				±50	mA
Clamp Diode Current	I_k	Per input pin (Input protector)			±10	mA
Allowable Power Dissipation	Pd	Per package, Ta≦85°C			300	mW
Storage Temperature	Tstg		-65		+150	°C
Lead Temperature and Time	Tsol		(300°C•10sec.)			

Internal Equivalent Circuit and Logic Diagram



$\frac{1}{4}$-LC74HC00

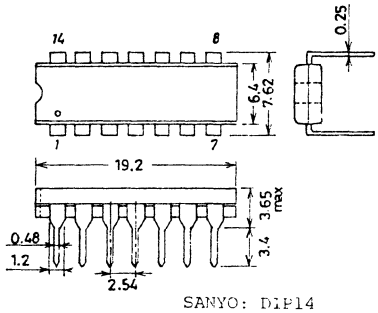
Pin Assignment



Truth Table

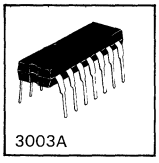
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Case Outline 3003A-D8IC
(unit:mm)



SANYO: DIP14

LC74HC02



C MOS IC

Quad 2-Input NOR Gate

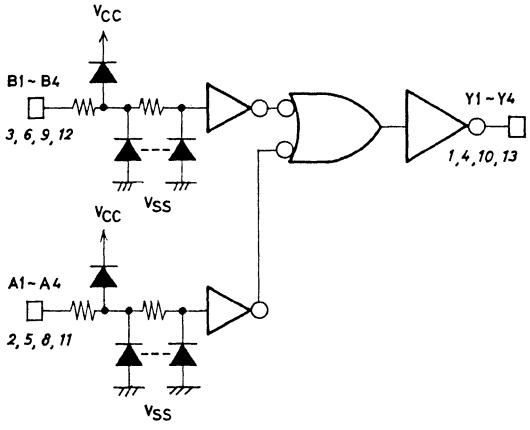
TENTATIVE

1. The LC74HC02 consists of 4 identical 2-input NOR gates.
2. Uses CMOS silicon gate process technology to achieve operating speeds similar to LSTTL (74LS02) gates with the low power dissipation and high noise margin of standard CMOS IC's.
3. Has buffered outputs, improving the input-output propagation characteristic.
4. All inputs and outputs are protected from damage.
5. The LC74HC00 is functionally as well as pin-out compatible with the standard 54LS/74LS TTL logic family.

Absolute Maximum Ratings at Ta=25°C±2°C, V_{SS}=0V

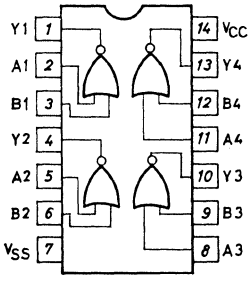
			min	typ	max	unit
Supply Voltage	V_{CC}		V_{SS}-0.5		V_{SS}+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.5		V_{CC}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5		V_{CC}+0.5	V
Output Current	I_{OUT}	Per output			±25	mA
Current Dissipation	I_{CC}/I_{GND}				±50	mA
Clamp Diode Current	I_k	Per input pin(Input protector)			±10	mA
Allowable Power Dissipation	Pd	Per package, Ta≦85°C			300	mW
Storage Temperature	Tstg		-65		+150	°C
Lead Temperature and Time	Tsol		(300°C·10sec.)			

Internal Equivalent Circuit and Logic Diagram



$\frac{1}{4}$LC74HC02

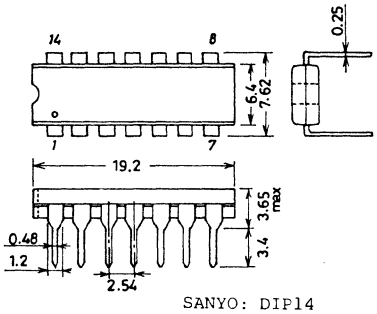
Pin Assignment



Truth Table

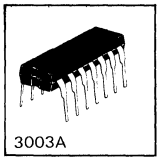
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Case Outline 3003A-D8IC
(unit:mm)



SANYO: DIP14

LC74HCU04



C MOS IC

Hex Inverter

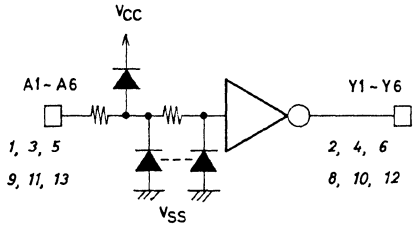
TENTATIVE

1. The LC74HCU04 consists of 6 identical unbuffered inverters.
2. Uses CMOS silicon gate process technology to achieve operating speeds similar to LSTTL (74LS04) gates with the low power dissipation and high noise margin of standard CMOS IC's.
3. All inputs and outputs are protected from damage.
4. The LC74HCU04 is functionally as well as pin-out compatible with the standard 54LS/74LS TTL logic family.

Absolute Maximum Ratings at Ta=25°C±2°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{CC}		V_{SS}-0.5		V_{SS}+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.5		V_{CC}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5		V_{CC}+0.5	V
Output Current	I_{OUT}	Per output			±25	mA
Current Dissipation	I_{CC}/I_{GND}				±50	mA
Clamp Diode Current	I_k	Per input pin(Input protector)			±10	mA
Allowable Power Dissipation	Pd	Per package, Ta≦85°C			300	mW
Storage Temperature	Tstg		-65		+150	°C
Lead Temperature and Time	Tsol		(300°C•10sec.)			

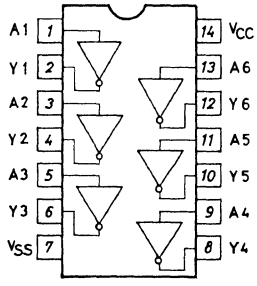
Internal Equivalent Circuit and Logic Diagram



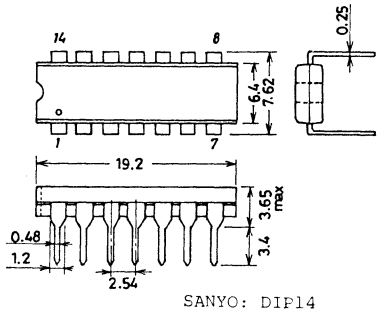
$\frac{1}{6}$LC74HCU04 Truth Table

A	Y
0	1
1	0

Pin Assignment

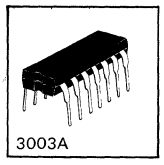


Case Outline 3003A-D8IC
(unit:mm)



SANYO: DIP14

LC74HC08



C MOS IC

Qusd 2-Input and Gate

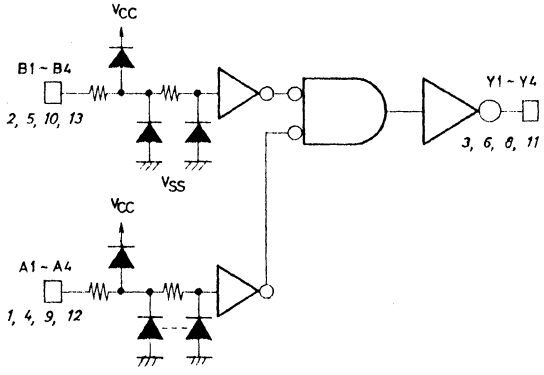
TENTATIVE

1. The LC74HC08 consists of 4 identical 2-input AND gates.
2. Uses CMOS silicon gate process technology to achieve operating speeds similar to LSTTL (74LS08) gates with the low power dissipation and high noise margin of standard CMOS IC's.
3. Has buffered outputs, improving the input-output propagation characteristic.
4. All inputs and outputs are protected from damage.
5. The LC74HC08 is functionally as well as pin-out compatible with the standard 54LS/74LS TTL logic family.

Absolute Maximum Ratings at $Ta=25^{o}C\pm2^{o}C, V_{SS}=0V$

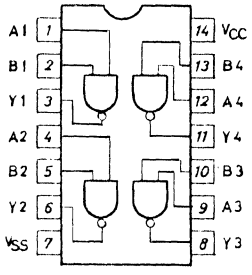
			min	typ	max	unit
Supply Voltage	V_{CC}		$V_{SS}-0.5$		$V_{SS}+7.0$	V
Input Voltage	V_{IN}		$V_{SS}-0.5$		$V_{CC}+0.5$	V
Output Voltage	V_{OUT}		$V_{SS}-0.5$		$V_{CC}+0.5$	V
Output Current	I_{OUT}	Per output			±25	mA
Current Dissipation	I_{CC}/I_{GND}				±50	mA
Clamp Diode Current	I_k	Per input pin(Input protector)			±10	mA
Allowable Power Dissipation	Pd	Per package			300	mW
Storage Temperature	Tstg		-65		+150	^{o}C
Lead Temperature and Time	Tsol		(300°C·10sec.)			

Internal Equivalent Circuit and Logic Diagram



$\frac{1}{4}$ LC74HC08

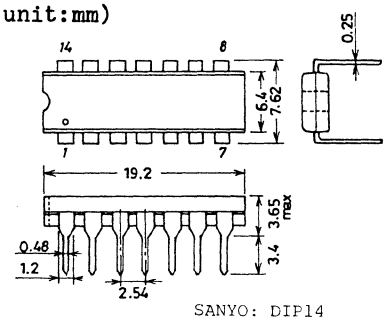
Pin Assignment



Truth Table

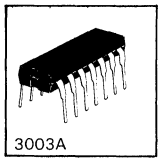
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Case Outline 3003A-D14IC
(unit:mm)



SANYO: DIP14

LC74HC74



C MOS IC

Dual D Flip-Flop with Set and Reset

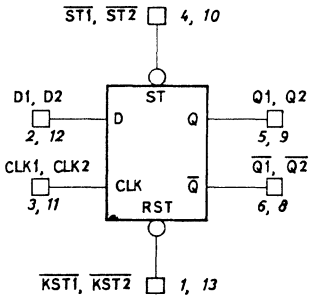
TENTATIVE

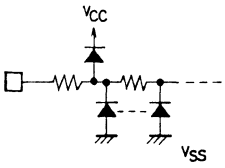
1. The LC74HC74 consists of 2 identical D type flip-flops.
2. Uses CMOS silicon gate process technology to achieve operating speeds similar to LSTTL (74LS74) gates with the low power dissipation and high noise margin of standard CMOS IC's.
3. Has buffered outputs, improving the input-output propagation characteristic.
4. All inputs and outputs are protected from damage.
5. The LC74HC74 is functionally as well as pin-out compatible with the standard 54LS/74LS TTL logic family.

Absolute Maximum Ratings at Ta=25°C±2°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{CC}		V_{SS}-0.5		V_{SS}+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.5		V_{CC}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5		V_{CC}+0.5	V
Output Current	I_{OUT}	Per output			±25	mA
Current Dissipation	I_{CC}/I_{GND}				±50	mA
Clamp Diode Current	I_k	Per input			±10	mA
Allowable Power Dissipation	Pd	Per package, Ta≦85°C			300	mW
Storage Temperature	Tstg		-65		+150	°C
Lead Temperature and Time	Tsol		(300°C·10sec.)			

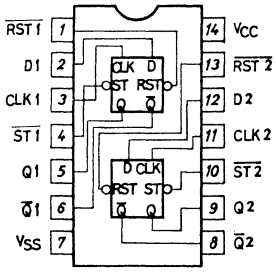
Internal Equivalent Circuit and Logic Diagram





Input protection circuit

Pin Assignment



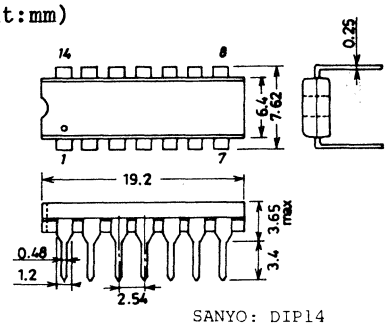
Truth Table

CLK	D	$\overline{ST}$	$\overline{RST}$	Q	$\overline{Q}$
X	X	0	1	1	0
X	X	1	0	0	1
X	X	0	0	1	1
↑	1	1	1	1	0
↑	0	1	1	0	1
0	X	1	1	Qn	$\overline{Qn}$

X : Don't Care

↑ : Level Change

Case Outline 3003A-D8IC
(unit:mm)



SANYO: DIP14

TIMEPIECES

- **Pin Numbering**

When you face the top side (marking side) of the package, numbering starts with ① assigned to the pin located, in a counterclockwise direction, immediately after the index point and turns counterclockwise.

LC5613

C MOS LSI

LCD Digital Watch

Ⓔ 671

Use

LCD digital watch with chronograph

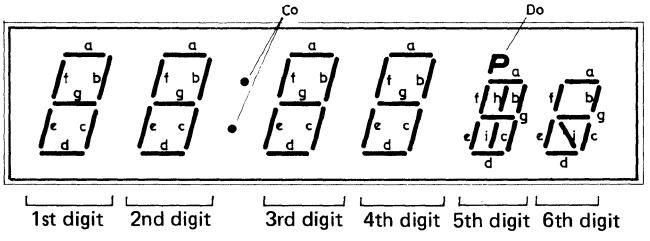
Functions

1. 6 functions (hours, minutes, seconds, month, date, day of week)
2. Stopwatch function (minutes, seconds, 1/10 second, 1/100 second): Max. countable time 59 minutes 59 seconds 99

Features

1. 6-digit display
   Real time: (hours, minutes, seconds), (month, date, day of week) } Selectable
   Stopwatch: (minutes, seconds, 1/10, 1/100)
2. 3 function switches
3. Lap function of stopwatch
4. Perpetual calendar function: Programmed to count date in February up to the 28th.
5. Error within ±30 seconds correctable
6. Oscillation frequency: 32.768 kHz
7. LCD lighting system: 32 Hz static lighting system
8. Supply voltage: 1.5 V, with doubler circuit

Sample Panel Format



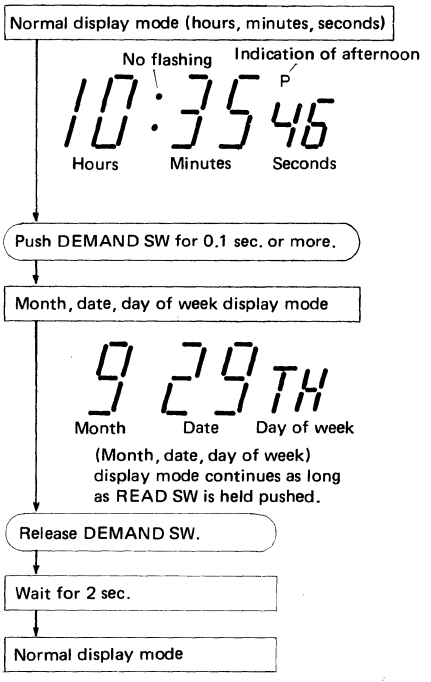
Display Font

Numeral	0	1	2	3	4	5	6	7	8	9
Display	0	1	2	3	4	5	6	7	8	9

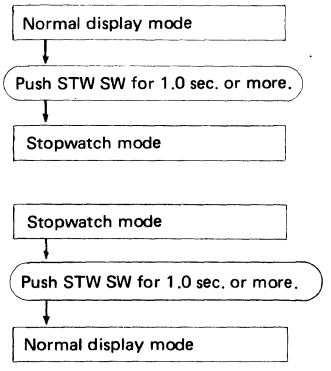
Day of week	Sun.	Mon.	Tues.	Wed.	Thur.	Fri.	Sat.
Display	SU	MO	TU	WE	TH	FR	SA

1. Display Function

1. Readout of month, date, day of week

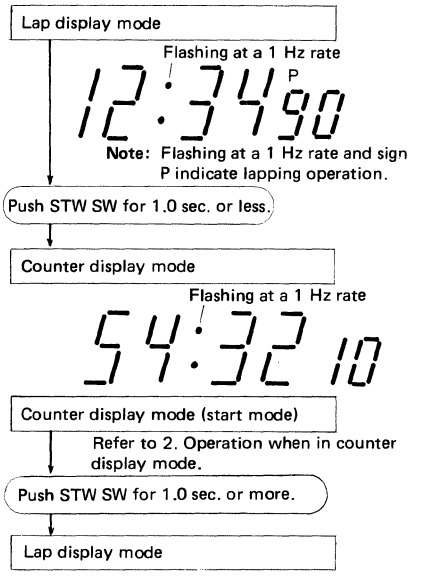


2. Stopwatch mode

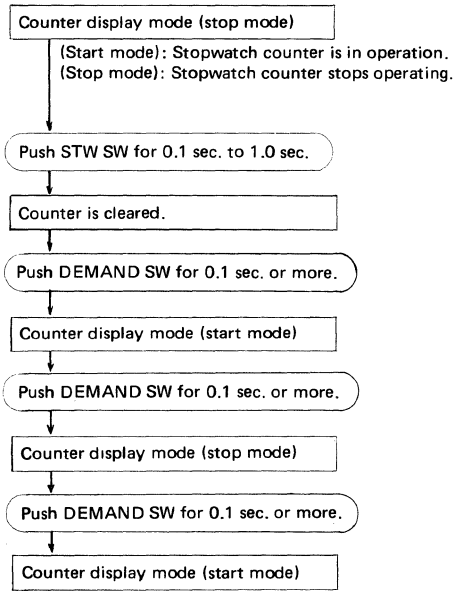


2. Stopwatch Operation

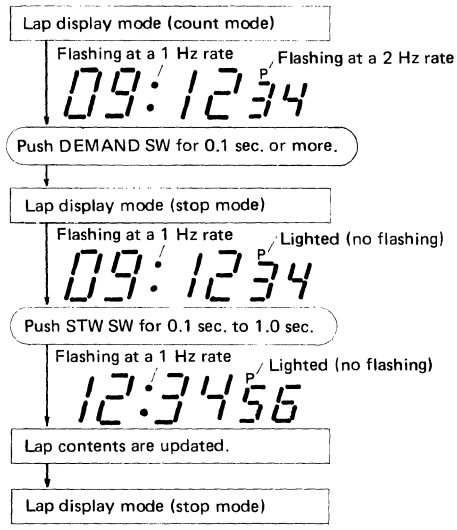
1. Change of display contents



2. Operation when in counter display mode

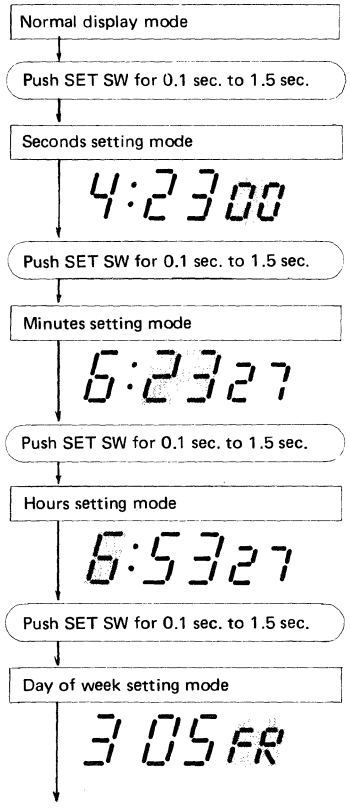


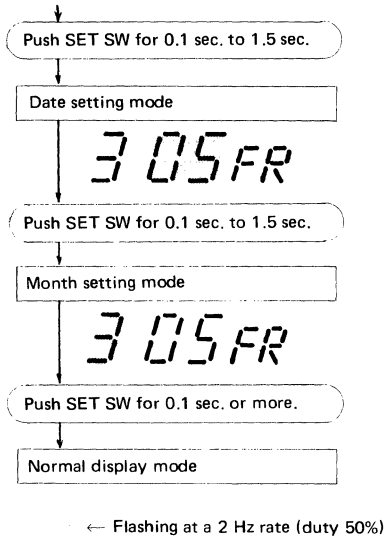
3. Operation when in lap display mode



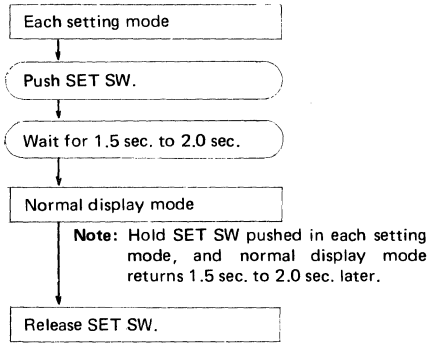
3. Setting Operation

1. Setting mode

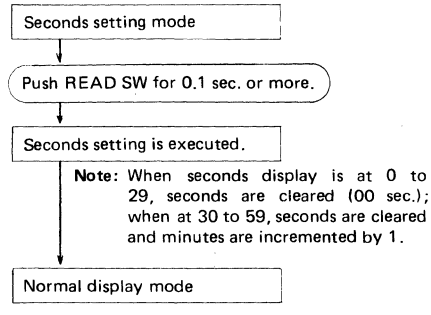




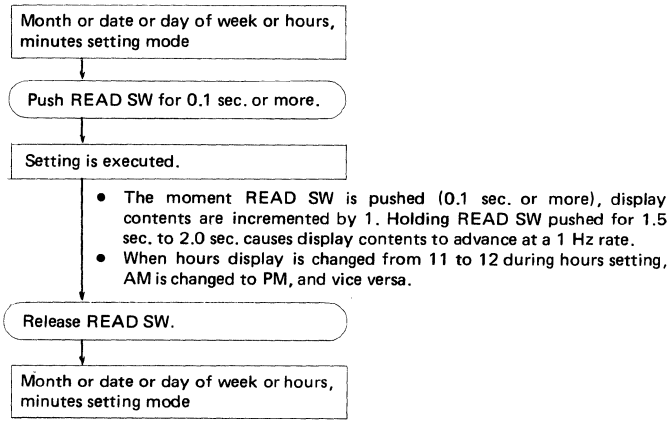
2. Return from setting mode



3. Execution of seconds setting



4. Execution of month, date, day of week, hours, minutes setting



4. Others

1. Perpetual calendar function
   Programmed to count date in February up to the 28th. When executing date setting, date is counted up to the 29th. Automatic calendar for months other than February
2. Step-up circuit
   A doubler circuit is contained. Two capacitors are connected externally. Step-up frequency: 1024 Hz
3. 0 blanking
   0 in 10's place of hours, date, month is blanked out.
4. SW input pin
   - A pull-down resistor is connected across input pin and V_{SS}.
   - Setting input to V_{DD} makes this pin active.
5. LCD drive output
   Alternating frequency 32 Hz (duty 50%)
6. LCD check function
   Simultaneous push of STW SW, SET SW, and DEMAND SW causes all LCD's to be lighted.

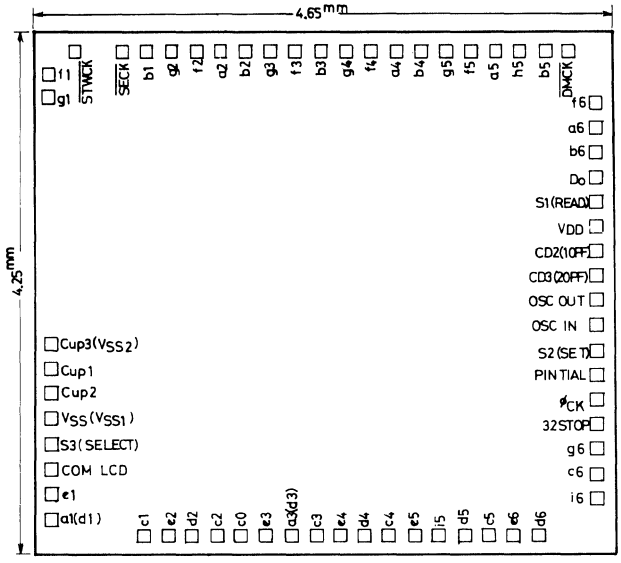
5. Electrical Characteristics

Absolute Maximum Ratings/T_a = 25°C				unit
Maximum supply voltage	V_{CC} max	V_{DD} = 0 V	−2.0 to +0.3	V
Storage temperature	T_{stg}		−30 to +125	°C
Operating temperature	T_{opg}		−15 to +65	°C

Allowable Operating Ranges/T_a = 25°C			unit
Supply voltage	V_{CC}	−1.65 to −1.35	V
Input "H" level voltage	V_{IH}	−0.2 to 0	V
Input "L" level voltage	V_{IL}	V_{SS} to V_{SS}+0.2	V
Operating frequency	f	32 k to 33 k	Hz

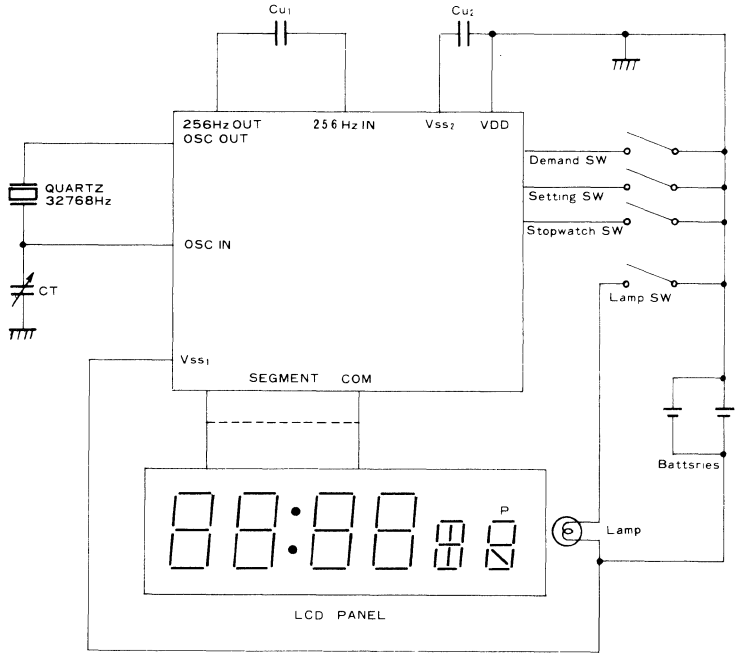
Electrical Characteristics/T_a = 25±2°C, V_{DD} = 0 V, V_{SS} = −1.35 to −1.65 V			unit
Input resistance (SW input)		45 k to 2 M	Ω
Saturation voltage (Segment input)		0 to 0.05	V
Operating voltage		6	μAmax
Display output voltage, V_{SS2}	$C_{u1} = C_{u2}$ = 0.1 μF, R_L = 3 M Ω	−2.5 to −3.3	V

6. Pad Assignment

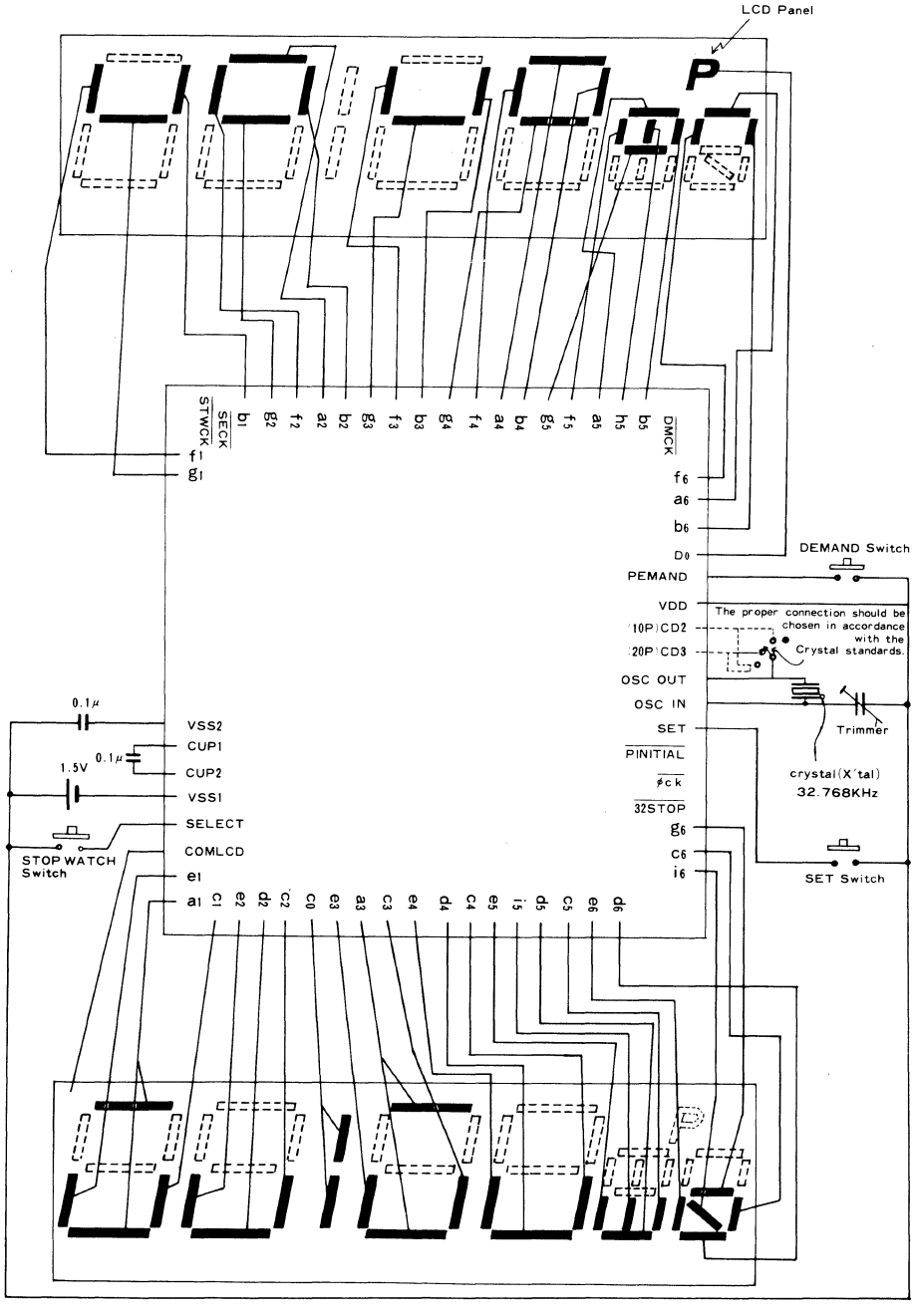


Pad NO.	Name	Pad NO.	Name
1	VDD	33	S2(SELECT)
2	S1(READ)	34	COM LCD
3	DO	35	e1
4	b6	36	a1(=d1)
5	a6	37	c1
6	f6	38	e2
7	$\overline{DMCK}$	39	d2
8	b5	40	c2
9	h5	41	co
10	a5	42	e3
11	f5	43	a3(+d3)
12	g5	44	c3
13	b4	45	e4
14	a4	46	d4
15	f4	47	c4
16	g4	48	e5
17	b3	49	i5
18	f3	50	d5
19	g3	51	c5
20	b2	52	e6
21	a2	53	d6
22	f2	54	i6
23	g2	55	c6
24	b1	56	g6
25	$\overline{SECK}$	57	$\overline{32STOP}$
26	$\overline{STWCK}$	58	$\overline{Øck}$
27	f1	59	$\overline{PINITIAL}$
28	g1	60	S2(SET)
29	Cup3(VSS2)	61	OSC IN
30	Cup1	62	OSC OUT
31	Cup2	63	CD3(20PF)
32	VSS(VSS1)	64	CD2(10PF)

7. Sample Application Circuit



A Standard Circuit Diagram



LC5621

C MOS LSI

LCD Digital Watch

Ⓔ 674

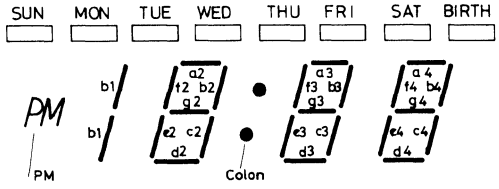
Use

4-digit 8-flag basic digital watch

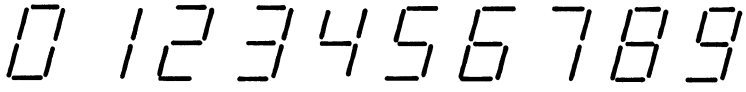
Features

1. 6 functions (month, date, day of week, hours, minutes, seconds)
2. 4-digit display (month, date) (hours, minutes) (seconds)
3. 7-flag display (day of week)
4. 2 function switches (READ switch, SET switch)
5. Perpetual calendar: Programmed to count date in February up to the 28th.
6. Error within ±30 seconds correctable.
7. Oscillation frequency: 32.768kHz
8. Lighting system: 32Hz static LCD lighting system.
9. Supply voltage: 1.5V, With doubler circuit.

Sample Display

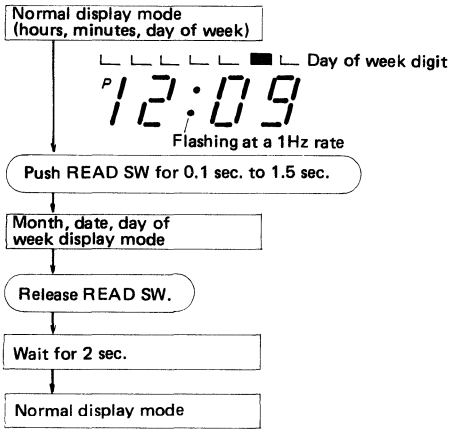


Display Font

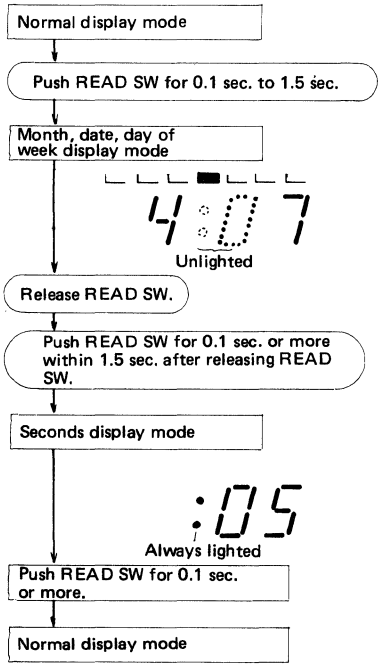


1. Readout Operation

1. Readout of month, date, day of week

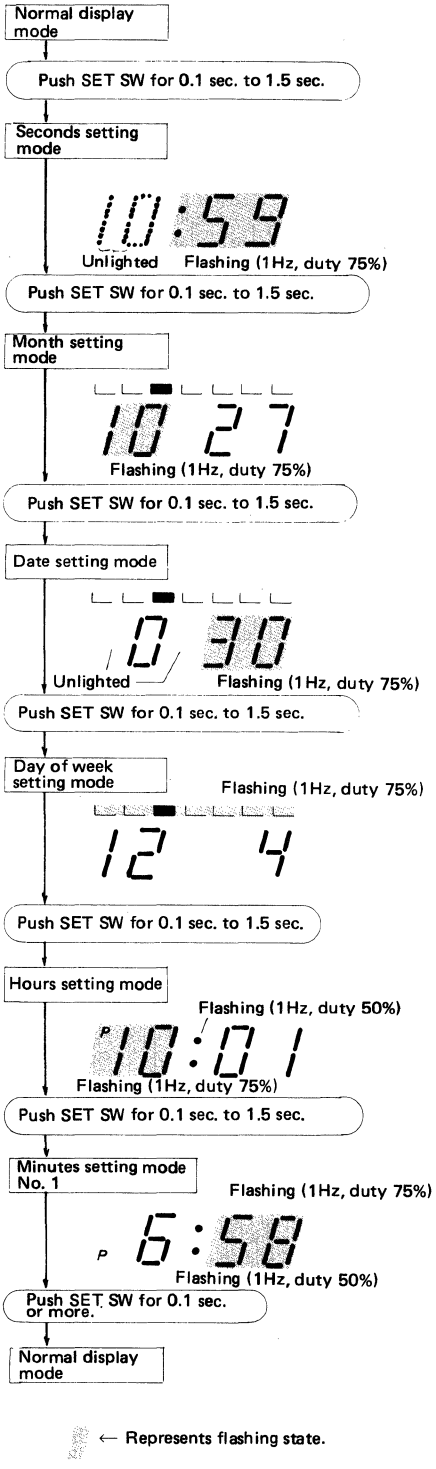


2. Readout of seconds

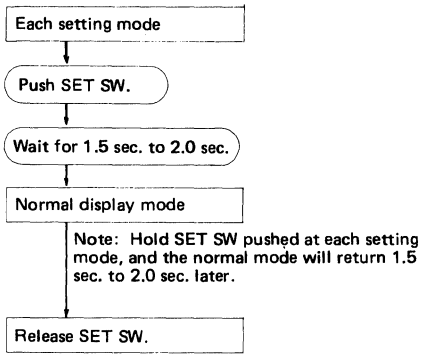


2. Setting Operation

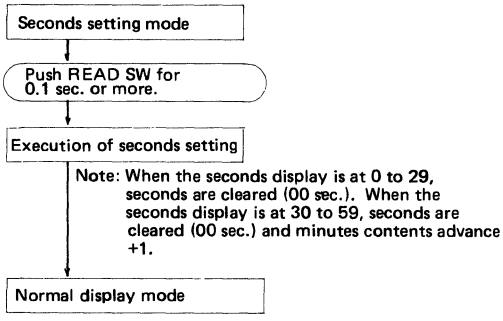
1. Setting mode



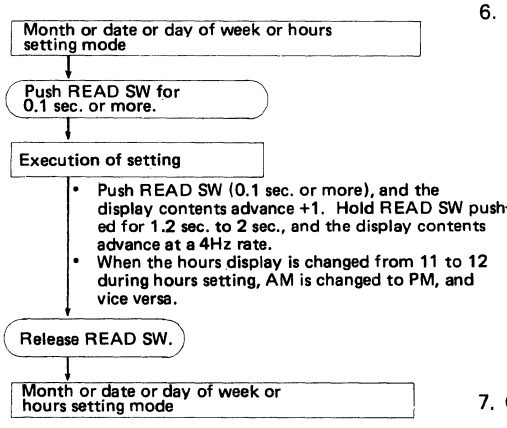
2. Return from setting mode



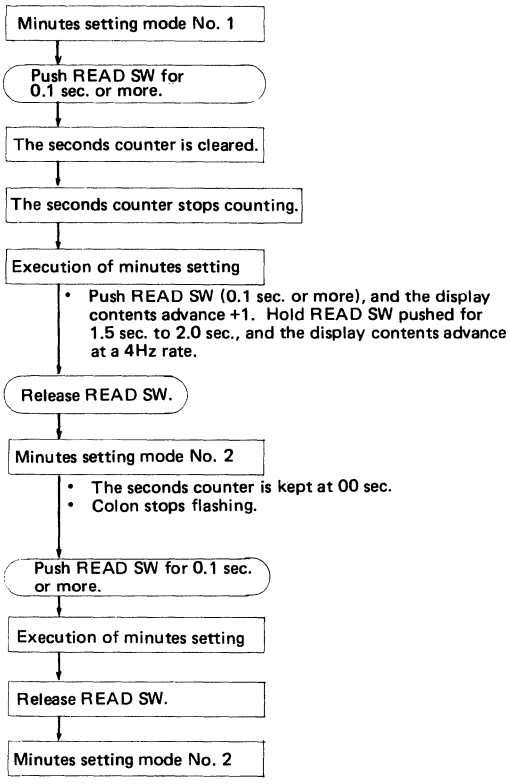
3. Execution of seconds setting



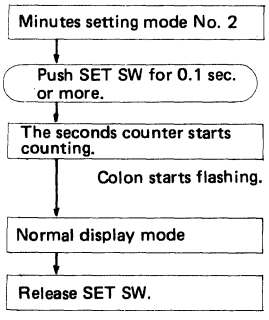
4. Execution of month, date, day of week, hours setting



5. Execution of minutes setting



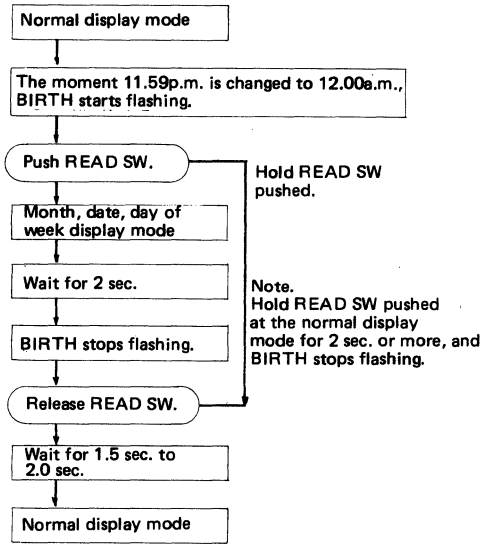
6. Release from minutes setting mode No. 2



7. Operation of BIRTH otuput

(continued on next page)

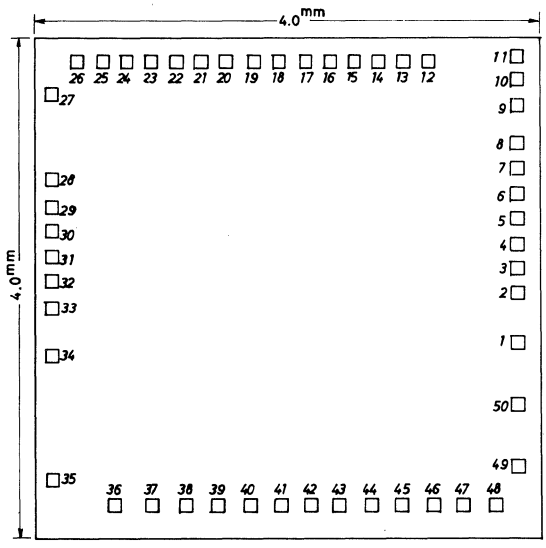
7. Operation of BIRTH output



3. Others

1. Perpetual calendar
   Programmed to count date in February up to the 28th. When executing date setting, date is counted up to the 29th. Automatic calendar for months other than February.
2. Step-up circuit
   A doubler circuit is contained. Two capacitors are connected externally.
   Step-up frequency: 1024Hz.
3. 0 blanking
   Blanking of 0 in 10's place of hours, date, month.
4. SW input pin
   - A pull-down resistor is connected across input pin and V_{SS}.
   - Setting input to V_{DD} makes this pin active.
5. LCD drive output
   Alternating frequency 32Hz (duty 50%)
6. LCD check
   Simultaneous push of SET SW and READ SW at the seconds display mode causes all LCD's to be lighted.

4. Pad No. and Pin Name



1	Power supply	V_{DD}	18	O	a3	35	O	COM LCD
2	I	S2(K Set)	19	O	WED	36	O	f2
3	Power supply	V_{SS1}	20	O	COLON	37	O	g2
4	O	Cup 2	21	O	TUE	38	O	12
5	O	Cup 1	22	O	b2	39	O	d2
6	O	Cup 3 (V_{SS2})	23	O	MON	40	O	c2
7	I	S1 (K Read)	24	O	a2	41	O	f3
8	O	$\overline{\text{COM LCD}}$	25	O	SUN	42	O	g3
9	O	Birth	26*	I	$\overline{\text{DMCK}}$	43	O	13
10	O	b4	27	O	b1	44	O	d3
11	O	SAT	28	O	PM	45	O	c3
12*	I	$\overline{\text{SECK}}$	29	I	CD1(10P)	46	O	f4
13*	I	$\overline{\text{HMCK}}$	30	I	CD2(20P)	47	O	g4
14	O	a4	31	I/O	OSC OUT	48	O	14
15	O	FRI	32	I	OSC IN	49	O	d4
16	O	b3	33*	I	$\overline{\text{PINITIAL}}$	50	O	c4
17	O	THU	34*	I/O	$\overline{\text{ØCK}}$	12*,13*,26*,33*,34*:Test pin		

5. Electrical Specifications

Absolute Maximum Ratings/T_a=25±2°C, V_{DD}=0V.

				unit
Maximum Supply Voltage 1	V_{SS1max}		−2.0～+0.3	V
Maximum Input Voltage 1	V_{IN1max}		V_{SS1}−0.3～+0.3	V
Maximum Output Voltage	$V_{OUT1max}$	OSC OUT, $\overline{PINITIAL}$	V_{SS1}−0.3～+0.3	V
	V_{OUT2}	※	V_{SS2}−0.3～+0.3	V
Maximum Supply Voltage 2	V_{SS2}		−4.0～+0.3	V
Operating Temperature	Topg.		−15～+65	°C
Storage Temperature	Tstg		−30～+125	°C

※ Segment output, COM, $\overline{\varnothing_{CK}}$, Cup1, Cup2, COMbar, $\overline{SECK}$, $\overline{DMCK}$, HMCKbar

Allowable Operating Ranges/T_a=25±2°C, V_{DD}=0V.

			unit		Remarks
Supply Voltage 1	V_{SS1}	−1.65～−1.35	V		The LSI inside operates normally at a voltage down to −1.3V. (Ta=−1.5 to +60°C)
Supply Voltage 2	V_{SS2}	−3.3～−2.4	V		V_{SS1}=−1.35～−1.65 V
Input "H" Level Voltage	V_{IH}	−0.2～0	V	SW input	
Input "L" Level Voltage	V_{IL}	V_{SS1}～V_{SS1}+0.2	V	SW input	
Operating Frequency	f_{opg}	32k～33k	Hz	Ta=−15～+65°C	

Electrical Characteristics/T_a=25±2°C, V_{DD}=0V, V_{SS1}=−1.35 to −1.65V.

			min	typ	max	unit
Input Resistance	R_{IN1}	SW input	45		2000	kΩ
	R_{IN2}	Test input	1		50	kΩ
Output "H" Level Voltage 1	V_{OH1}	I_{OH}=−0.2μA, LCD segment output	−0.02			V
Output "L" Level Voltage 1	V_{OL1}	I_{OL}=−0.2μA, LCD segment output			V_{SS1}+0.02	V
Output "H" Level Voltage 2	V_{OH2}	I_{OH}=−1μA, COM, COMbar pin	−0.025			V
Output "L" Level Voltage 2	V_{OL2}	I_{OL}=1μA, COM, COMbar pin			V_{SS2}+0.025	V
Output Supply Voltage	V_{SS2}	C1, C2=0.1μF, R_L=3MΩ	−3.3		−2.5	V
Current Dissipation 1 (Operating Current)	I_{DD1}	V_{SS1}=−1.5V, C1, C2=0.1μF, Co=30pF, Cg=30pF, CI=30k, R2=∞		2	4	μA
Current Dissipation 2 (Leakage Current)	I_{DD2}	V_{SS1}=1.5V, Initial mode			0.5	μA
Oscillation Start Voltage	Vstart	Co=30pF, Cg=30pF, CI=30k, f_{opg}=32.768kHz			1.35	V
Oscillation Stop Voltage	V_{stop}	Same as above (Ta=−15～+60°C)			1.30	V
Oscillation Start Time	t_{start}	Same as above (Ta=25°C)			8	sec
Oscillation Capacitance	C_{D1}	OSC pin	8	10	12	pF
	C_{D2}	External pin	8	10	12	pF
	C_{D3}	External pin	16	20	24	pF
Output Rise Time	t_r	C_L=100pF, LCD output 10 to 90%			10	μsec
Output Fall Time	t_f	C_L=100pF, LCD output 10 to 90%			10	μsec

LC5633

C MOS LSI

LCD Digital Watch

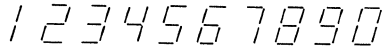
Ⓔ 892

1. Functions and Features

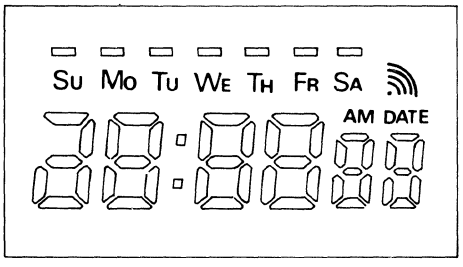
1. Supply voltage: 1.5V (with doubler provided)
2. Real Time (year, month, date, day of week [flag], hours, minutes, seconds), alarm time (hours, minutes).
3. 4 switches of MODE, SELECT, SET, LAMP.
4. Possible to select hours, minutes, day of week, date or hours, minutes, day of week, seconds, or month, date, year (date, month, year) display mode of real time.
5. Possible to select 12 or 24-hour basis.
6. Possible to select European type (DISP SELECT pin: V_{SS1} or open) or normal type (DISP SELECT pin: V_{DD}) of month, date display mode when using on 24-hour basis.
7. Perpetual calendar from the year 1980 to 2039.
8. Possible to correct error within ±30 seconds (Counting 32 to 59 seconds as a minute and disregarding 00 to 31 seconds).
9. Possible to monitor alarm tone.
10. f_{OSC}=32.768KHz

2. Display

1. 6-digit, 7-flag, 3-sign LCD
2. 32Hz static LCD drive
3. Display font



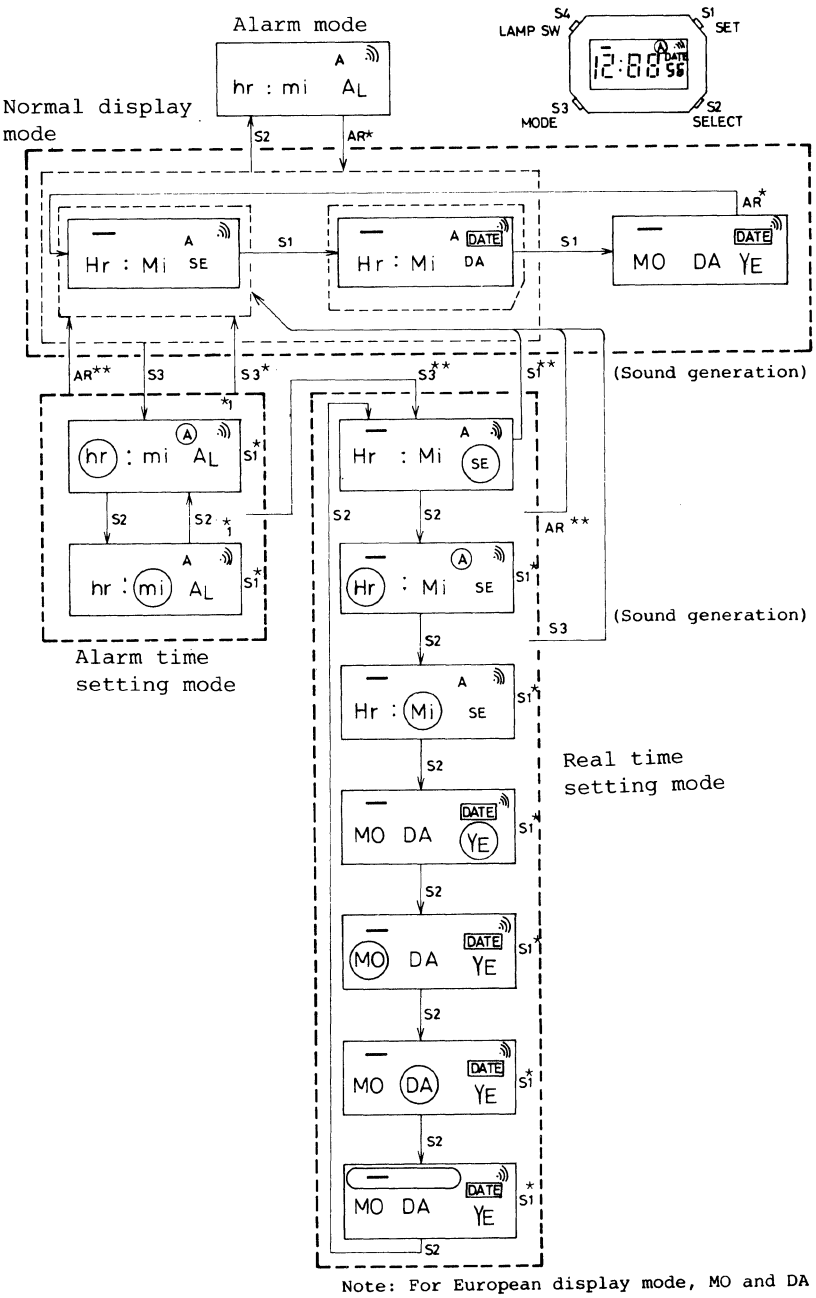
4. Panel format



D1 D2	D3 D4	D5 D6	
Hours	Minutes	Seconds	Hours, minutes, seconds display mode and hours, minutes, seconds setting mode
Month	Date	Year	Year, month, date display mode and year, month, date setting mode (12H)
Date	Month	Year	Year, month, date display mode and year, month, date setting mode (24H)
Hours	Minutes	AL	Alarm time display mode and alarm time setting mode
Hours	Minutes	Date	Hours, minutes, date display mode

5. Output pins for display
   Most significant digit: 4 segments, remaining digits: 7 segments
   - Colon : 1 pin
   - Day of week: 7 flags
   - Sign : DATE alarm set sign, AM
   - Common : 2 pins (Common, common bar)

3. Operation Flow



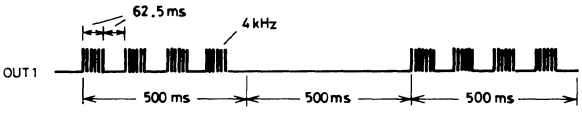
Description of operation flow

1. Hr : Mi A SE — Hours, minutes, seconds display mode of real time
2. Hr: Mi A DATE Dete — Hours, minutes, date, day of week display mode of real time
3. MO Date DATE YE — Month, date, year, day of week display mode of real time
4. hr : mi A AL — Hours, minutes display mode of alarm time
5. Alarm set sign
6. Flashing at a 1Hz rate (75% duty)
7. S1* Execution of setting
   (1) 1 advance/1 push
   (2) Holding pushed for 2 seconds or more causes fast advance at a 4Hz rate.
8. S1** 32 to 59 seconds are counted as a minute and 00 to 31 seconds are disregarded.
9. S1*** The same function as for S1*. Seconds are reset to 00.
10. AR* The normal display mode returns 1.5 seconds after releasing all switches of S1 to S3.
11. AR** The normal display mode returns 30 seconds after releasing all switches of S1 to S3.
12. 12H/24H select function
    Pushing S2 while pushing S1 changes the 12-hour (24-hour) display mode to the 24-hour (12-hour) display mode.
13. Alarm set sign select function
    Pushing S1 while pushing S2 changes the alarm set sign lighted (unlighted) to the unlighted (lighted).
14. Sound monitor
    Holding S1 pushed for 2 seconds or more while pushing S2 makes it possible to monitor the alarm sound.
15. LCD check
    Pushing all switches S1 to S3 while pushing S3 causes the whole LCD to be lighted.

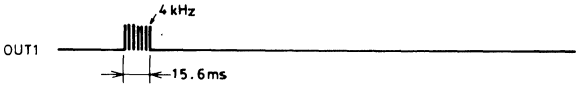
4. Pin Description

1. Input switches S1 to S3
   - For these switches, refer to 3. Operation Flow.
   - With pull-down resistor
2. Input switch S4 (LAMP input)
   - Since the oscillation start and hold characteristic of the LSI differ according as the input pin is set to V_{DD} or V_{SS1} level (or open), it is recommended to apply V_{DD} to this pin at the lamp lighted mode.
   - Alarm sound output is inhibited when V_{DD} is applied to this pin
   - With pull-down resistor
3. DISP SELECT pin
   - Pin used to select the hours, month, date, year display mode or date, month, year display mode on a 24-hour basis
   - When this pin is set to V_{SS1} level (or open), the date, month, year (European type) display mode is entered; when set to V_{DD} level, the month, date, year (normal type) display mode is entered.
   - With clocked pull-down resistor

4. OUT1 (OUT2) output pin
   (1) Alarm output sound
   - Output period: 30 seconds
   - Output waveform

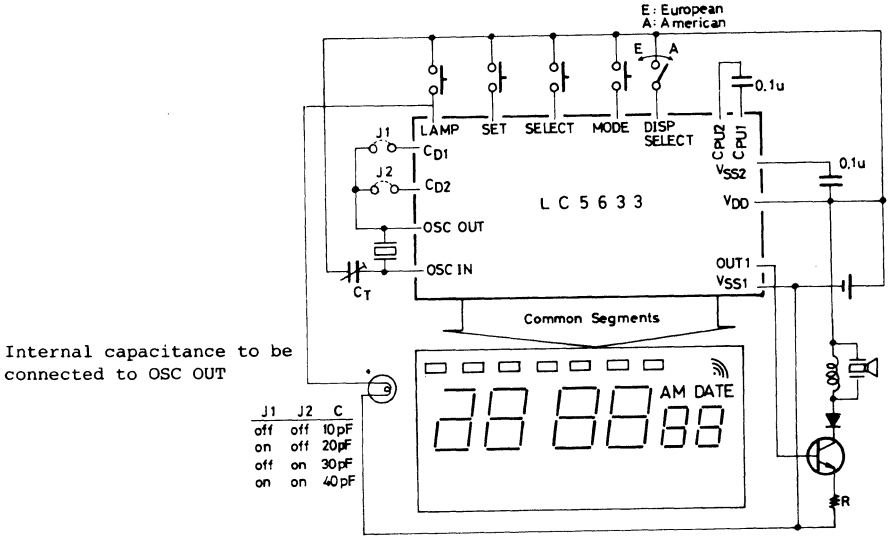


   (2) Operation check sound
   - Output period: 15msec.
   - Output wave form



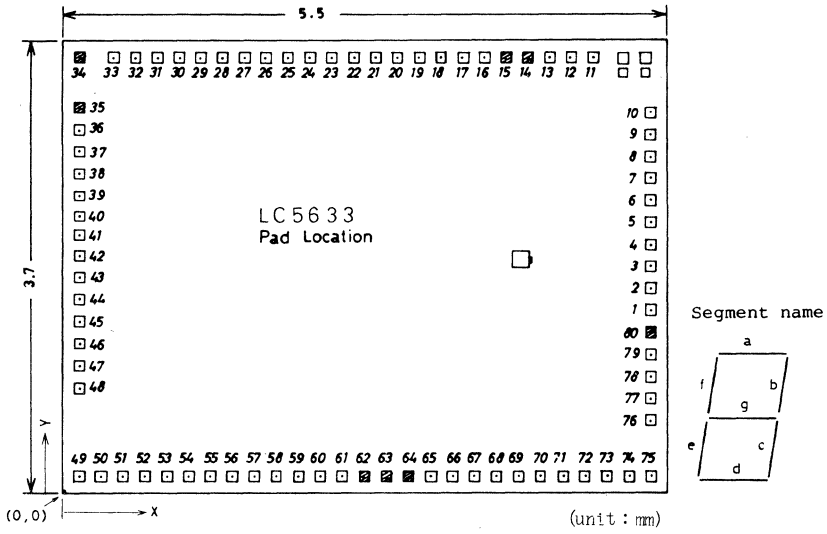
5. $\overline{\text{Initail}}$
   - When V_{SS1} is applied, the internal counter is initialized.
   - With pull-up resistor
6. OSC OUT pin
   - With 10pF capacitor for oscillation correction
7. 0 blanking
   - 0 in 10's place of year, month date, hours is blanked out.
8. LCD check function
   - Simultaneous push of S1 to S3 causes the whole LCD to be lighted.

5. Sample Application Circuit



J1	J2	C
off	off	10pF
on	off	20pF
off	on	30pF
on	on	40pF

6. Pad No. and Pin Name



Pad No.	Pin Name	Coordinates (X, Y)	Pad No.	Pin Name	Coordinates (X, Y)	Pad No.	Pin Name	Coordinates (X, Y)
1	VDD	(5.35, 1.35)	28	seg COL	(1.45, 3.55)	55	seg c2	(1.35, 0.15)
2	Disp select	(5.35, 1.55)	29	seg b2	(1.25, 3.55)	56	seg g3	(1.55, 0.15)
3	OUT2	(5.35, 1.75)	30	seg MON	(1.05, 3.55)	57	seg e3	(1.75, 0.15)
4	OUT1	(5.35, 1.95)	31	seg a2	(0.85, 3.55)	58	seg d3	(1.95, 0.15)
5	V_{SS2}	(5.35, 2.15)	32	seg f2	(0.65, 3.55)	59	seg c3	(2.15, 0.15)
6	Cup1	(5.35, 2.40)	33	seg SUN	(0.45, 3.55)	60	seg g4	(2.35, 0.15)
7	Cup2	(5.35, 2.60)	34	$\overline{\text{TEST I/OA}}$	(0.15, 3.55)	61	seg e4	(2.55, 0.15)
8	SET	(5.35, 2.80)	35	TEST A	(0.15, 3.25)	62	$\overline{\text{TEST D}}$	(2.75, 0.15)
9	seg f6	(5.35, 3.00)	36	seg b1	(0.15, 3.05)	63	$\overline{\text{TEST B}}$	(2.95, 0.15)
10	seg b5	(5.35, 3.20)	37	seg 24s	(0.15, 2.85)	64	$\overline{\text{TEST I/OB}}$	(3.15, 0.15)
11	DATE SIGN	(4.85, 3.55)	38	seg AM	(0.15, 2.65)	65	seg d4	(3.35, 0.15)
12	ALM OUT	(4.65, 3.55)	39	LAMP IN	(0.15, 2.45)	66	seg c4	(3.55, 0.15)
13	seg SAT	(4.45, 3.55)	40	CD 1	(0.15, 2.25)	67	NC	(3.75, 0.15)
14	$\overline{\text{TEST F}}$	(4.25, 3.55)	41	CD 2	(0.15, 2.05)	68	seg g5	(3.95, 0.15)
15	$\overline{\text{TEST C}}$	(4.05, 3.55)	42	OSC OUT	(0.15, 1.85)	69	seg e5	(4.15, 0.15)
16	seg a5	(3.85, 3.55)	43	OSC IN	(0.15, 1.65)	70	seg d5	(4.35, 0.15)
17	seg f5	(3.65, 3.55)	44	RO	(0.15, 1.45)	71	seg c5	(4.55, 0.15)
18	seg FR1	(3.45, 3.55)	45	V_{SS1}	(0.15, 1.25)	72	seg g6	(4.75, 0.15)
19	seg b4	(3.25, 3.55)	46	MODE	(0.15, 1.05)	73	seg e6	(4.95, 0.15)
20	seg a4	(3.05, 3.55)	47	COM	(0.15, 0.85)	74	seg d6	(5.15, 0.15)
21	seg THU	(2.85, 3.55)	48	seg e1	(0.15, 0.65)	75	seg c6	(5.35, 0.15)
22	seg f4	(2.65, 3.55)	49	seg c1	(0.15, 0.15)	76	seg b6	(5.35, 0.35)
23	seg b3	(2.45, 3.55)	50	seg g2	(0.35, 0.15)	77	seg a6	(5.35, 0.55)
24	seg WED	(2.25, 3.55)	51	NC	(0.55, 0.15)	78	$\overline{\text{COM}}$	(5.35, 0.75)
25	seg a3	(2.05, 3.55)	52	seg e2	(0.75, 0.15)	79	SELECT	(5.35, 0.95)
26	seg f3	(1.85, 3.55)	53	seg d2	(0.95, 0.15)	80	$\overline{\text{INITIAL}}$	(5.35, 1.15)
27	seg TUE	(1.65, 3.55)	54	NC	(1.15, 0.15)			

7. Main Specifications

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	Across V_{DD} and V_{SS1}	-2 to +0.3	V
	V_{SS2}	Across V_{DD} and V_{SS2}	-4 to +0.3	V
Input Voltage	V_{IN1}	OSC IN, MODE, SET, SELECT, LAMP, DISP SELECT, test pin	V_{SS1}-0.3 to +0.3	V
Output Voltage	V_{OUT1}	OSC OUT, CUP2, OUT1, OUT2, test F	V_{SS1}-0.3 to +0.3	V
	V_{OUT2}	All segments, common, common bar, CUP1	V_{SS2}-0.3 to +0.3	V
Operating Temperature	T_{opg}		-15 to +65	°C
Storage Temperature	T_{stg}		-30 to +125	°C

Allowable Operating Ranges at Ta=25±2°C, V_{DD}=0V

				unit
Supply Voltage	V_{SS1}		-1.65 to -1.3	V
	V_{SS2}		-3.3 to -2.4	V
"H"-Level Input Voltage	V_{IH}	SET, SELECT, MODE, LAMP	-0.2 to 0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1} to V_{SS1}+0.2	V
Operating Frequency	f_{opg}		+32 to +33	kHz

Electrical Characteristics/Ta=25±2°C, V_{DD}=0V, V_{SS1}=-1.55V

			min	typ	max	unit
Input Resistance	R_{IN1}	SET, SELECT, MODE, LAMP	200		2000	kohm
	R_{IN2}	Test input	1		100	kohm
	R_{IN3A}	"L"-level hold Tr, DISP SELECT, Fig 4	5		100	kohm
	R_{IN3B}	"L"-level pull-in Tr, DISP SELECT, Fig 4	200		2000	kohm
"H"-Level Output Voltage	V_{OH1}	Segment, flag, sign, colon: I_{OH}=-0.2uA	-0.1			V
	V_{OH2}	Common, Common bar: I_{OH}=-10uA	-0.1			V
	V_{OH3}	OUT1, OUT2 : V_{SS1}=-1.35V, I_{OH}=-250uA	-0.65			V
"L"-Level Output Voltage	V_{OL1}	Segment, flag, sign, colon: I_{OL}=0.2uA		V_{SS2}+0.1		V
	V_{OL2}	Common, common bar: I_{OL}=10uA		V_{SS2}+0.1		V
	V_{OL3}	OUT1, OUT2: V_{SS1}=-1.35V, I_{OL}=250uA		V_{SS1}+0.65		V
Output Supply Voltage (Step-up)	$V_{SS2\ OUT}$	C1=C2=0.1uF, Cd=30pF, Cg=30pF, C_I=25kohm: V_{SS1}=-1.65 to -1.35V, 3Mohm across V_{DD} and V_{SS2}, Fig 1	-3.3		-2.5	V
Current Dissipation	I_{DD}	C1=C2=0.1uF, Cd=30pF, Cg=30pF, C_I=25kohm: V_{SS1}=-1.55V, Fig 1		1.5	2.5	uA
Oscillation Start Voltage	V_{start}	C1=C2=0.1uF, Cd=30pF, Cg=30pF, C_I=25kohm: Fig 2			1.45	V
Oscillation Hold Time	V_{HLD}	fopg=32.768kHz±230Hz, Cd=30PF, Cg=30pF, C_I=25kohm: Fig 3			1.25	V
Oscillation Start Time	T_{start}	fopg=32.768kHz±230Hz, Cd=30pF, Cg=30pF, C_I=25kohm : Fig 2, V_1=1.55V			10	sec
Oscillation Correction Capacitance	C_{D1}	External pin	8	10	12	pF
	C_{D2}	External pin	16	20	24	pF
	C_{D3}	OSC pin	8	10	12	pF

			min	typ	max	unit
Output Rise Time	t_r	LCD segment pin, common pin, :V_{SS2}=-3.3 to -2.4V, C_L=100pF	-100	0	+100	usec
Output Fall Time	t_f	LCD segment pin, common pin, :V_{SS}=-3.3 to -2.4V C_L=100pF	-100	0	+100	usec

Fig. 1:Output Supply Voltage
Current Dissipation

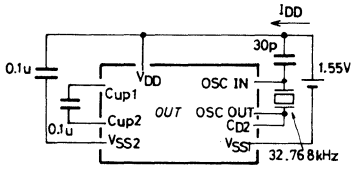


Fig.:2 Oscillation Start Voltage
Oscillation Start Time

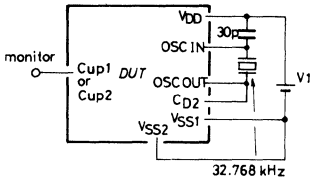


Fig. 3:Oscillation Hold Voltage

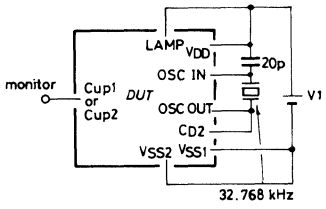
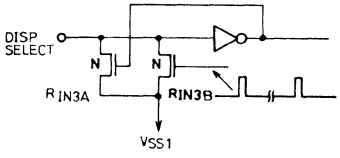


Fig. 4:DISP SELECT



LC5641

C MOS LSI

LCD Digital Watch

Ⓔ 1316

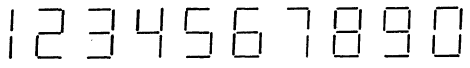
1. Functions

1. 4-digit display mode (6/4 pin: V_{DD})/6-digit display mode (6/4 pin: V_{SS1} or open) selectable.
2. Real time (month, date, day of week [flag], hours, minutes, seconds) and alarm (hours, minutes) functions.
3. 4 switches of SET switch, SELECT switch, MODE switch, LAMP switch.
4. Real time display mode selectable:
   - Hours, minutes, day of week/month, date, day of week/seconds.
     4-digit display mode.
   - Hours, minutes, seconds, day of week/hours, minutes, date, day of week.
     6-digit display mode.
5. Error within ±30 seconds correctable (Counting 32 seconds and over as a minute and disregarding 31 seconds and less).
6. Automatic calendar (Designed to automatically change February 28 to March 1).
7. European type display mode (DISP SELECT pin: V_{DD})/normal display mode (DISP SELECT pin: V_{SS1} or open) selectable . . . . . 4-digit display mode.
8. 12-hour operation mode/24-hour operation mode selectable at the touch of a switch.
9. Alarm sound monitor function.
10. Reference frequency: f_{OSC} = 32.768 Hz (Supply Voltage 1.5 V)
11. Battery voltage: 1.5 V. With built-in doubler circuit.
12. LCD light-up system by duplex drive.
13. Total number of pads: 54 pads.

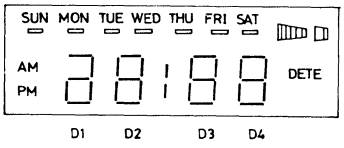
2. Display System

2.1 4-digit display mode.

1. 4-digit, 7-flag, 5-sign LCD.
2. 32 Hz duplex drive system.
3. Display font.



4. Panel layout (Example)



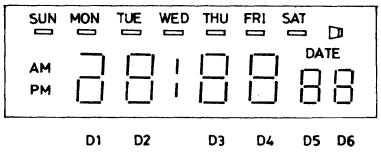
Hours	Minutes	Hours, minutes display mode and hours, minutes setting mode.
	Date	Month, date display mode and month, date, day of week setting mode (Normal display mode).
Date	Month	Date, month display mode and month, date, day of week setting mode (European type display mode).
	Seconds	Seconds display mode and seconds setting mode.
		Alarm display mode and alram setting mode.

5. Output pins for display.
   Segment output; first digit: 4 segments, Other 3 digits: 7 segments.
   - Colon: 1 segment
   - Day of week: 7 flags
   - Sign: DATE, alarm display, alarm set display, AM, PM
   - Common: COMMON 1, COMMON 2

2.2 6-digit display mode.

1. 6-digit, 7-flag, 4-sign LCD.
2. 32 Hz duplex drive system.
3. Display font.

4. Panel layout (Example)

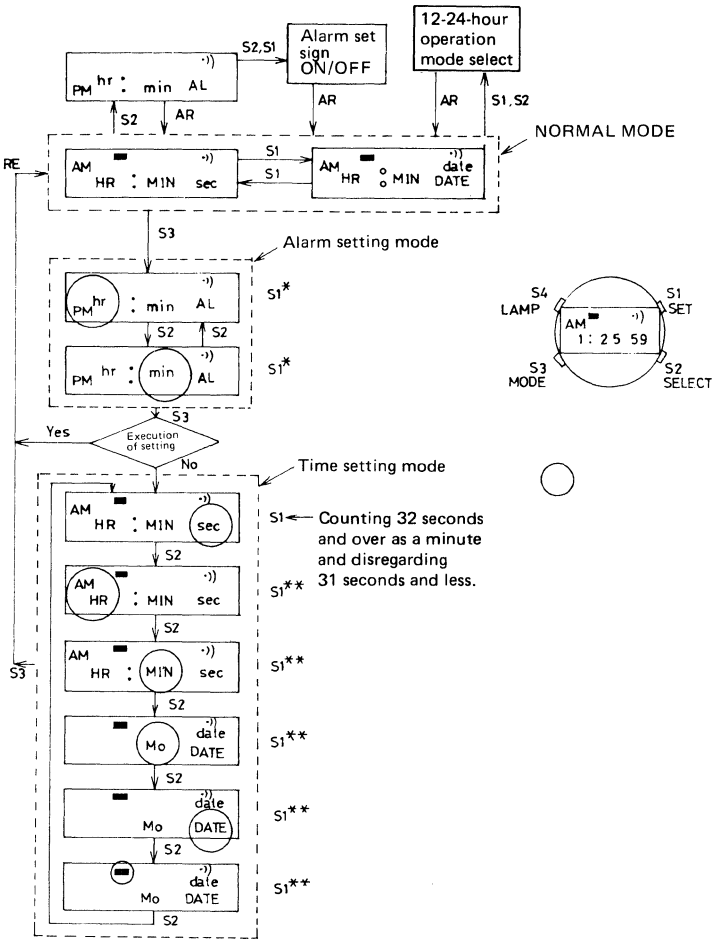


Hours	Minutes	Seconds	← Hours, minutes, seconds display mode and hours, minutes, seconds setting mode.
Hours	Minutes	Date	← Hours, minutes, date display mode.
	Month	Date	← Month, date, day of week setting mode.
Hours	Minutes		← Alram display mode and alarm hours, minutes setting mode.

5. Output pins for display
   Segment output: First digit (D_1): 4 segments, Other 5 digits (D_2 to D_6): 7 segments.
   - Colon: 1 segment
   - Sign: AM, PM, DATE, alarm set display
   - Day of week: 7 flags.
   - Common: COMMON 1, COMMON 2

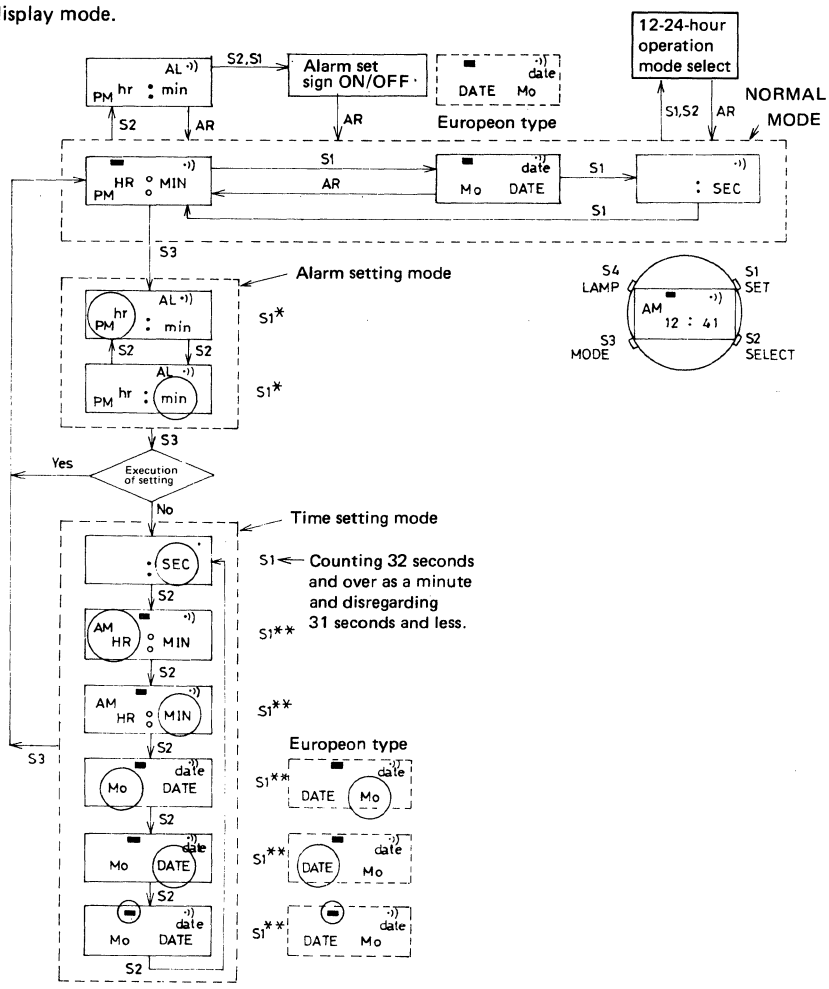
3. Operation Flow

3.1 4-digit display mode.



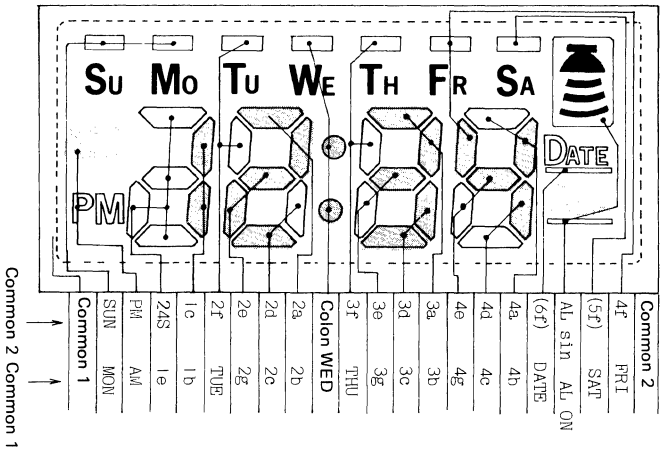
1. ◯ : Flashing at a 1 Hz rate (75% duty). Represents digit to be set.
2. AR : Normal display mode returns immediately after switch OFF.
3. AR* : Automatic return 1 second after switch OFF.
4. Colon : ⁚ Continuous light-up, ⁚ Flashing (1 Hz, 50% duty)
5. Long month/short month judge
   : Setting up to 31 is possible. The moment carry from hours to date occurs long month or short month is judged.
6. S1* : Setting is executed and alarm set sign appears.
   a. One advance per push.
   b. Holding pushed for more than 2 sec. causes fast advanve at a 4 Hz rate.
7. S_1** : Setting is executed.
   a. One advance per push.
   b. Holding pushed for more than 2 sec. causes fast advance at a 4 Hz rate.
8. Alarm output time
   : 30 sec. Alarm output is released by pushing one of S_1, S_2, S_3.
9. Alarm set sign ON/OFF
   : After pushing S_2 at normal display mode, push S_1 and S_2 simultaneously.
10. 12-hour operation mode/24-hour operation mode select
    : After pushing S_1 at normal display mode, push S_1 and S_2 simultaneously.
11. LCD check
    : Push S_1 and S_2 simultaneously.
12. Sound monitor
    : After pushing S_2 at normal display mode, push S_1 and S_2 simultaneously.

3.2 6-digit display mode.

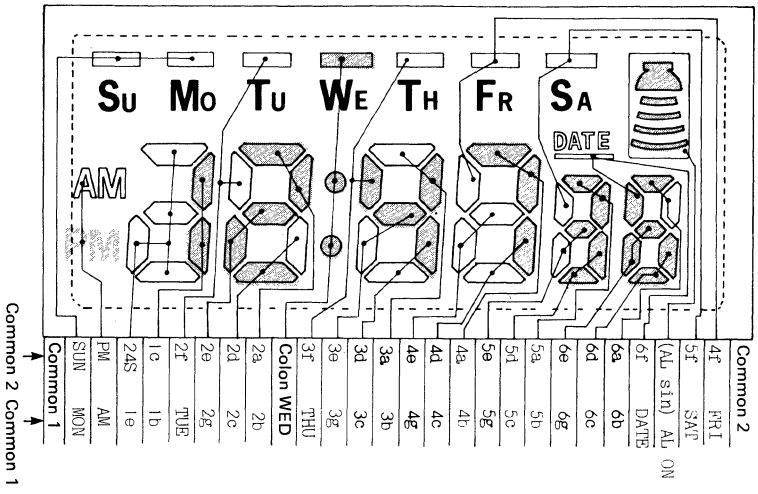


1. ◯ : Flashing at a 1 Hz rate. (75% duty). Represents digit to be set.
2. AR : Normal display mode returns immediately after switch OFF.
3. RE : Mode preceding setting mode returns.
4. Colon : ⁚ Continuous light-up, ⁚ Flashing (1 Hz, 50% duty).
5. Long month/short month judge
   : Setting up to 31 is possible. The moment carry from hours to date occurs long month or short month is judged.
6. S_1* : Setting is executed and alarm set sign appears.
   a. One advance per push.
   b. Holding pushed for more than 2 sec. causes fast advance at a 4 Hz rate.
7. S_1** : Setting is executed.
   a. One advance per push.
   b. Holding pushed for more than 2 sec. causes fast advance at a 4 Hz rate.
8. Alarm output time
   : 30 sec. Alarm output is released by pushing one of S_1, S_2, S_3.
9. Alarm set sign ON/OFF
   : After pushing S_2 at normal display mode, push S_1 and S_2 simultaneously.
10. 12-hour operation mode/24-hour operation mode select
    : After pushing S_1 at normal display mode, push S_1 and S_2 simultaneously.
11. LCD check
    : Push S_1 and S_2 simultaneously.
12. Sound monitor
    : After pushing S_2 at normal display mode, push S_1 and S_2 simultaneously.

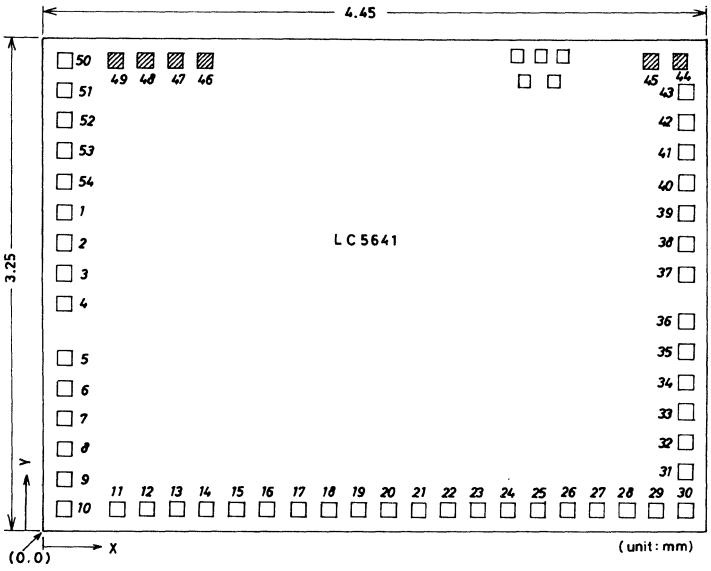
Panel Design of 4-Digit Display



Panel Design of 6-Digit Display

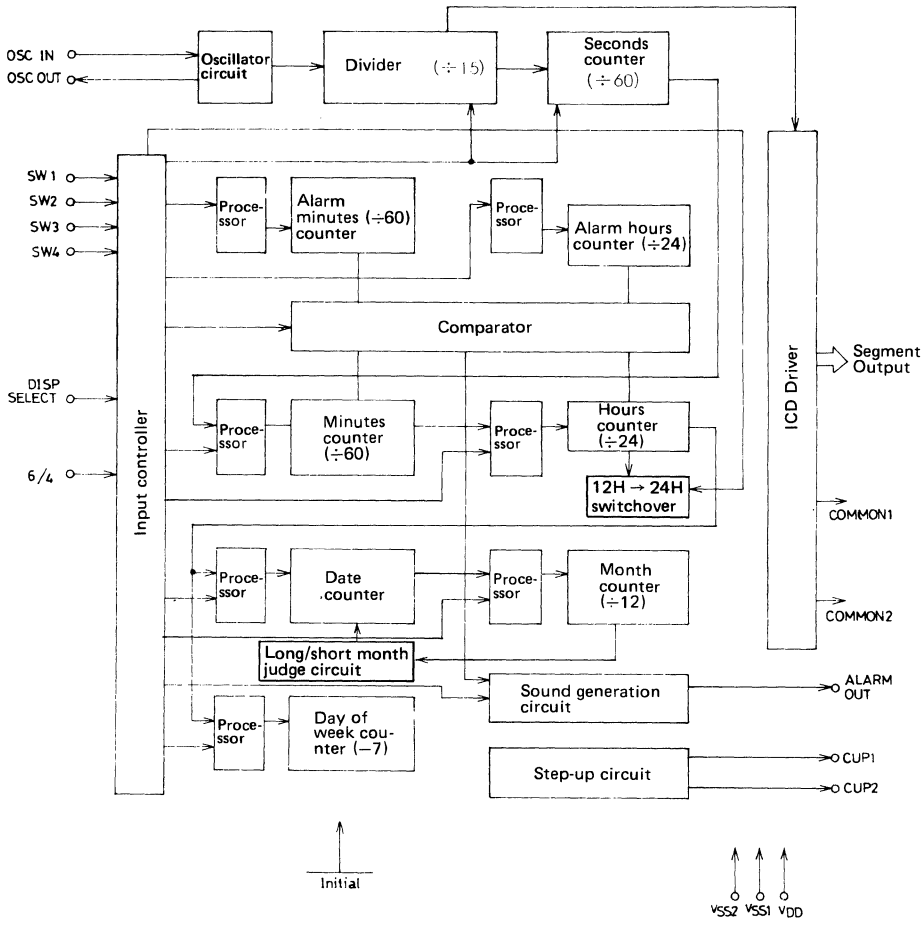


4. Pad No. and Pin Name



Pad No.	Pin Name	Coordinates (X, Y)	Pad No.	Pin Name	Coordinates (X, Y)	Pad No.	Pin Name	Coordinates (X, Y)
1	V_{DD}	(0.15, 2.1)	19	3C, 3d	(2.1 , 0.15)	37	S1	(4.3 , 1.7)
2	OSC IN	(0.15, 1.9)	20	3b, 3a	(2.3 , 0.15)	38	ALM OUT	(4.3 1.9)
3	OSC OUT	(0.15, 1.7)	21	4g, 4e	(2.5 , 0.15)	39	V_{SS1}	(4.3 , 2.1)
4	10PF	(0.15, 1.5)	22	4c, 4d	(2.7 , 0.15)	40	V_{SS2}	(4.3 , 2.3)
5	S3	(0.15, 1.15)	23	4b, 4a	(2.9 , 0.15)	41	V_{DD}	(4.3 , 2.5)
6	TEST A	(0.15, 0.95)	24	5g, 5e	(3.1 , 0.15)	42	DISP SELECT	(4.3 , 2.7)
7	COMMON 1	(0.15, 0.75)	25	5c, 5d	(3.3 , 0.15)	43	6/4	(4.3 , 2.9)
8	MON, SUN	(0.15, 0.55)	26	5b, 5a	(3.5 , 0.15)	44	TEST C	(4.3 , 3.1)
9	AM, PM	(0.15, 0.35)	27	6g, 6e	(3.7 , 0.15)	45	TEST D	(4.1 , 3.1)
10	1e, 24s	(0.15, 0.15)	28	6c, 6d	(3.9 , 0.15)	46	TEST I/O B	(1.1 , 3.1)
11	1b, 1c	(0.5 , 0.15)	29	6b, 6a	(4.1 , 0.15)	47	TEST I/O A	(0.9 , 3.1)
12	TUE, 2f	(0.7 , 0.15)	30	DATE,6f	(4.3 , 0.15)	48	TEST E	(0.7 , 3.1)
13	2g, 2e	(0.9 , 0.15)	31	ALM MK/SIN	(4.3 , 0.4)	49	TEST B	(0.5 , 3.1)
14	2c, 2d	(1.1 , 0.15)	32	Sat, 5f	(4.3 , 0.6)	50	CUP 1	(0.15, 3.1)
15	2b, 2a	(1.3 , 0.15)	33	Fri, 4f	(4.3 , 0.8)	51	CUP 2	(0.15, 2.9)
16	Wed, Col	(1.5 , 0.15)	34	COMMON 2	(4.3 , 1.0)	52	LAMP IN	(0.15, 2.7)
17	Thu, 3f	(1.7 , 0.15)	35	INITIAL	(4.3 , 1.2)	53	V_{SS1}	(0.15, 2.5)
18	3g, 3e	(1.9 , 0.15)	36	S2	(4.3 , 1.4)	54	V_{SS2}	(0.15, 2.3)

5. Block Diagram



6. Main Specifications

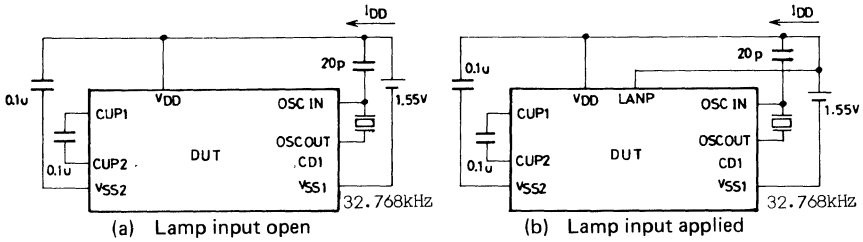
Absolute Maximum Ratings/T_a = 25±2°C, V_{DD} = 0 V				unit
Maximum supply voltage	V_{SS1}		–4 to 0.3	V
	V_{SS2}		–4 to 0.3	V
Input voltage	V_{IN1}	SET, SELECT, MODE, LAMP SW, TEST A to E, INITIAL, CD_1, OSC IN, DIGIT SELECT, DISP SELECT	V_{SS1}–0.3 to 0.3	V
Output voltage	V_{OUT1}	OSC OUT, TEST I/O A, TEST I/O B, CUP2, ALARM OUT	V_{SS1}–0.3 to 0.3	V
	V_{OUT2}	All segments, COMMON 1, COMMON 2, CUP1	V_{SS2}–0.3 to 0.3	V
Operating temperature	T_{opg}		–20 to +75	°C
Storage temperature	T_{stg}		–30 to +125	°C

Recommended Operating Conditions/T_a = 25±2°C, V_{DD} = 0 V				unit
Supply voltage	V_{SS1}	Refer to oscillation start voltage/stop voltage.	−1.65 to −1.30	V
	V_{SS2}	V_{SS1} = −1.30 to −1.65 V : Refer to oscillation start voltage/stop voltage.	−3.3 to −2.40	V
Input "H" level voltage	V_{IH}	V_{SS1} = −1.30 to −1.65 V : SET, SELECT, MODE, LAMP SW	−0.2 to 0	V
Input "L" level voltage	V_{IL}	V_{SS1} = −1.30 to 1.65 V	V_{SS1} to V_{SS1}+0.2	V
Operating frequency	f_{opg}	V_{SS1} = −1.30 to −1.65 V : T_a = −20 to +75°C	32 to 33	kHz

Electrical Characteristics/T_a = 25±2°C, V_{DD} = 0 V, V_{SS1} = −1.35 to −1.65 V			min	typ	max	unit
Input resistance	R_{IN1}	V_{SS1} = −1.55 V : SET, SELECT, MODE, LAMP SW input.	200		2000	kΩ
	R_{IN2}	Test input	1		100	kΩ
	R_{IN3A}	V_{SS1} = −1.55 V : "L" level hold Tr., DISP SELECT, 6/4 pin	10		100	kΩ
	R_{IN4A}	V_{SS1} = −1.55 V, : "L" level pull-in Tr., DISP SELECT, 6/4 pin.	200		2000	kΩ
Output "H" level voltage	V_{OH1}	V_{SS1} = −1.55 V, I_{OH} = −4 μA : Segment, flag, sign, common	−0.2			V
	V_{OH2}	V_{SS1} = −1.55 V, I_{OH} = −4 μA : COMMON 1, COMMON 2	−0.2			V
	V_{OH3}	V_{SS1} = −1.35 V, I_{OH} = −250 μA : ALARM OUT	−0.65			V
Output "L" level voltage	V_{OL1}	V_{SS1} = −1.55 V, I_{OL} = 4 μA : Segment, flag, sign, common			V_{SS2}+0.2	V
	V_{OL2}	V_{SS1} = −1.55 V, I_{OL} = 4 μA : COMMON 1, COMMON 2			V_{SS2}+0.2	V
	V_{OL3}	V_{SS1} = −1.35 V, I_{OL} = 250 μA : ALARM OUT			V_{SS1}+0.65	V
Output "M" level voltage	V_{OM}	V_{SS1} = −1.55 V, I_{OH} = −4 μA, I_{OL} = 4 μA : COMMON 1, COMMON 2	V_{SS1}−0.2		V_{SS1}+0.2	V
Input leak current	I_{off}	V_{SS1} = −2 V, V_{SS2} = −4 V : DISP SELECT off, 6/4 off.			0.1	μA
Step-up voltage	V_{SS2}	C1 = C2 = 0.1 μF, f_{opg} = 32.768 kHz, 3 MΩ across V_{DD} and V_{SS2}	−3.3		−2.5	V
Supply current	I_{DD}	Fig. 1 (a): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_l = 25 k			2.0	μA
		Fig. 1, 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_l = 25 k			20	μA
Oscillation start voltage	V_{start}	Fig. 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_l = 25k			1.45	V
		Fig. 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_l = 25k			1.30	V
Oscillation hold voltage	V_{HOLD}	Fig. 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_l = 25k			1.40	V
		Fig. 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_l = 25k			1.25	V

			min	typ	max	unit
Oscillation start time	T_{start}	Fig. 2 (a): V_1 = 1.55 V, C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25 k			10	sec
		Fig. 2 (b): V_1 = 1.40 V, C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25 k			10	sec
Oscillation correction capacitance	C_{D1}	External pin (C_{D1})	8	10	12	pF
	C_{D2}	OSC OUT contained	16	20	24	pF
Output rise time	t_r	V_{SS2} = −3.3 to −2.4 V, C_L = 100 pF: COMMON 50%, Segment 90%	−100		100	μsec
Output fall time	t_f	V_{SS2} = −3.3 to −2.4 V C_L = 100 pF: COMMON 50% Segment 10%	−100		100	μsec

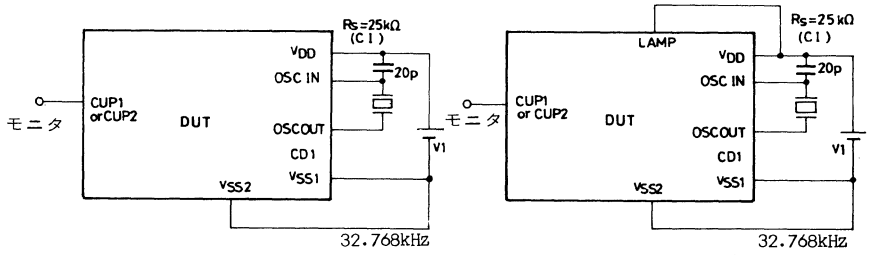
- **Current Dissipation Fig. 1**



(a) Lamp input open (b) Lamp input applied

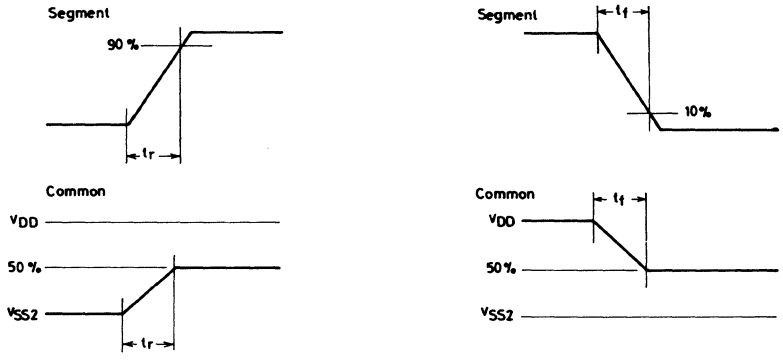
- Unentered pins are all open.
- CI ≦ 25 k

Oscillation start voltage, Oscillation stop voltage, Oscillation start time Fig. 2



(a) Lamp input open (b) Lamp input applied

Rise time and fall time of segment and common



LC5643

C MOS LSI

LCD Digital Watch

Ⓔ 1302

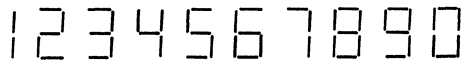
1. Functions

1. Real time (month, date, day of week [flag], hours, minutes, seconds)
2. 3 switches of SET switch, SELECT switch, LAMP switch
3. Real time display mode selectable
   Hours, minutes, day of week/month, date, day of week/seconds — 4-digit display mode
   Hours, minutes, seconds/hours, minutes date — 6-digit display mode
4. Error within ±30 seconds correctable (Counting 32 seconds and over as a minute and disregarding 31 seconds and less)
5. Automatic calendar (Designed to automatically change February 28 to March 1)
6. European type display mode (DISP SELECT pin: V_{DD})/normal display mode (DISP SELECT pin: open) selectable
7. 12-hour operation mode/24-hour operation mode selectable at the touch of a switch
8. Reference frequency: f_{OSC} = 32.768 Hz (Supply voltage 1.5 V)
9. Battery voltage: 1.5 V, With built-in doubler circuit
10. LCD light-up system by duplex drive
11. Total number of pads: 54

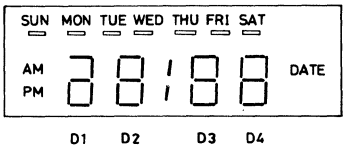
2. Display

2.1 4-Digit Display Mode

1. 4-digit, 7-flag, 3-sign LCD
2. 32 Hz Duplex drive
3. Display font



4. Panel format



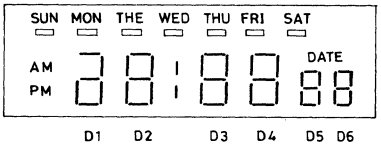
Hours	Minutes ←	Hours, minutes display mode and hours, minutes setting mode.
Month	Date ←	Month, date display mode and month, date, day of week setting mode (Normal display mode).
Date	Month ←	Date, month display mode and month, date, day of week setting mode (European type display mode).
	Seconds ←	Seconds display mode and seconds setting mode.

5. Output pins for display
   Segment output most significant digit: 4 segments, remaining 3-digits: 7 segments
   - Colon: 1 segment
   - Day of week: 7 flags
   - Sign: DATE, AM, PM
   - Common: COMMON 1, COMMON 2

2.2 6-Digit Display Mode

1. 6-digit, 7-flag, 3-sign LCD
2. 32 Hz Duplex drive
3. Display font

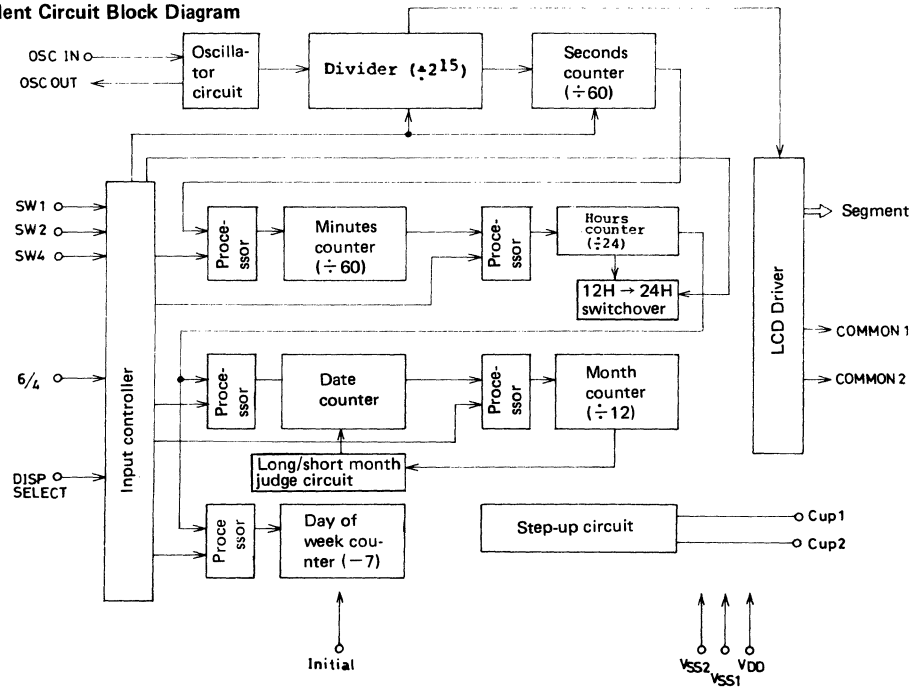
4. Panel format



Hours	Minutes	Seconds	← Hours, minutes, seconds display mode and hours, minutes, seconds setting mode.
Hours	Minutes	Date	← Hours, minutes, date display mode.
	Month	Date	← Month, date, day of week setting mode.

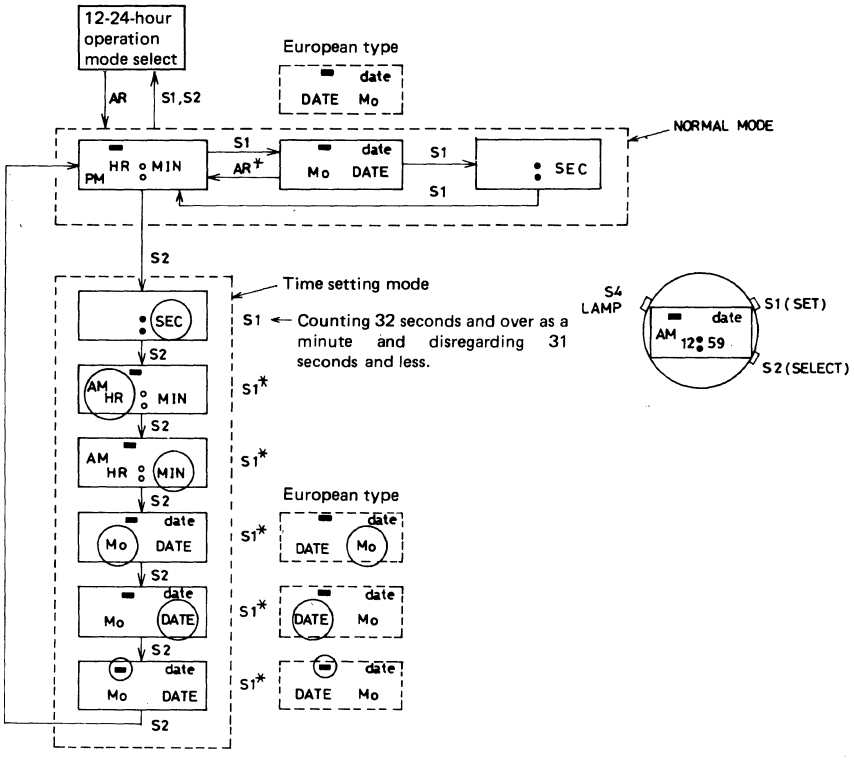
5. Output pins for display
   Most significant digit (D_1): 4 segments, remaining digits (D_2 to D_6): 7 segments
   - Colon: 1 segment
   - Sign: DATE, AM, PM
   - Day of week: 7 flags
   - Common: COMMON 1, COMMON 2

3. Equivalent Circuit Block Diagram



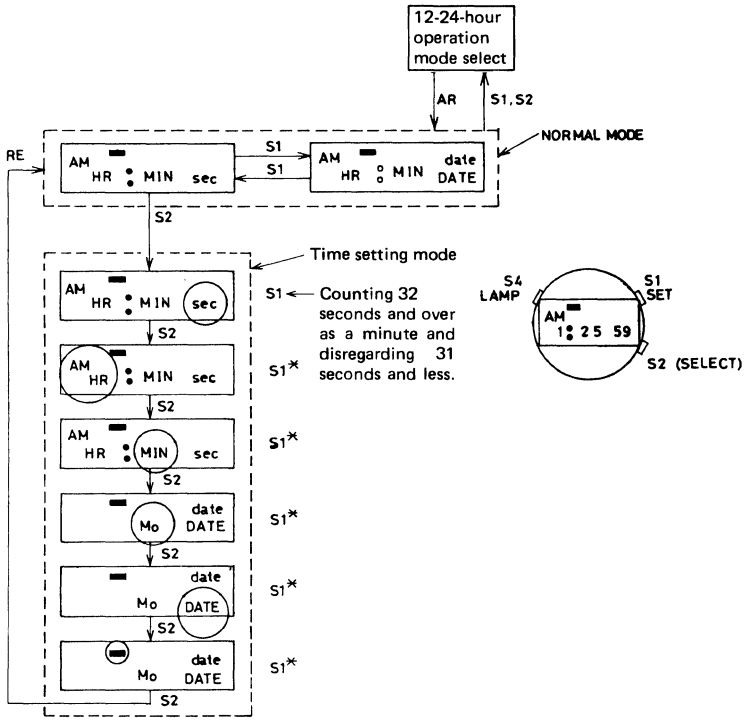
4. Operation Flow

4.1 4-digit display mode



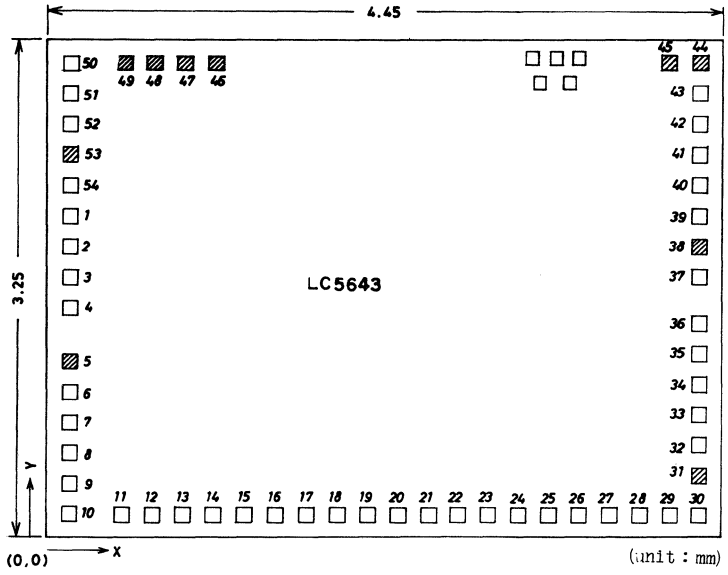
1. AR : Automatic return to normal mode immediately after switch off
2. AR* : Automatic return 1 second after switch off
3. Colon : ⁚ Continuous light-up, ⁚ Flashing (1 Hz 50% duty)
4. Long/short month discrimination
   : Settable up to 31st at setting mode
   The moment hour carry occurs, long/short month discrimination is made.
5. S1* : Execution of setting
   a. 1 advance/1 push
   b. Holding pushed for more than 2 seconds causes fast advance at a 4 Hz rate.
6. 12H/24H select
   : Simultaneous push of S1 and S2 after pushing S1 at normal mode
7. LCD check
   : Simultaneous push of S1 and S2
8. ◯ : Flashing at a 1 Hz rate (75% duty)
   Digit to be set is indicated.

4.2 6-digit display mode



1. AR : Automatic return to normal mode immediately after switch off
2. RE : Return to mode existed immediately before setting mode is entered
3. Colon : ⁚ Continuous light-up, ⁚ Flashing (1 Hz 50% duty)
4. Long/short month discrimination
   : Settable up to 31st at setting mode
   The moment hour carry occurs, long/short month discrimination is made.
5. S1* : Execution of setting
   a. 1 advance/1 push
   b. Holding pushed for more than 2 seconds causes fast advance at a 4 Hz rate.
6. 12H/24H select
   : Simultaneous push of S1 and S2 after pushing S1 at normal mode
7. LCD check
   : Simultaneous push of S1 and S2
8. ◯ : Flashing at a 1 Hz rate (75% duty)
   Digit to be set is indicated.

Pad No. and Pin Name

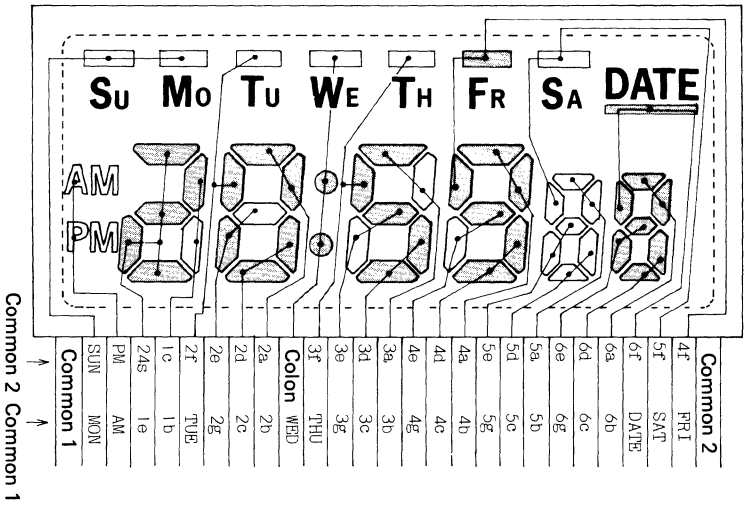


Chip thickness: 400 μm

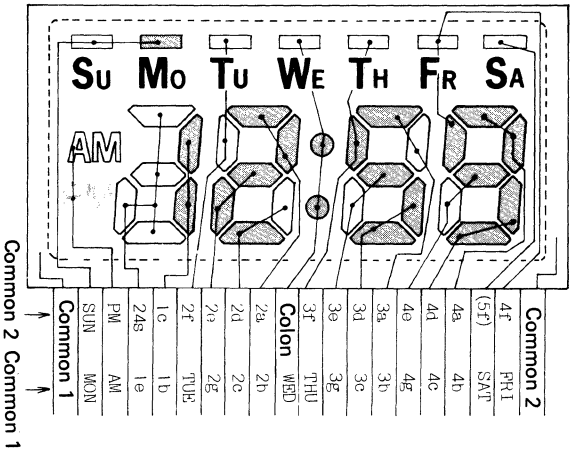
Note 1) Coordinates: Central value
Note 2) Pad size: 0.12 x 0.12
Note 3) Pad hatched: For test

Pad No.	Pin Name	Coordinates (X, Y)	Pad No.	Pin Name	Coordinates (X, Y)	Pad No.	Pin Name	Coordinates (X, Y)
1	V_{DD}	(0.15, 2.1)	19	3C, 3d	(2.1 , 0.15)	37	S1	(4.3 , 1.7)
2	OSC.IN	(0.15, 1.9)	20	3b, 3a	(2.3 , 0.15)	38	ALM OUT	(4.3 , 1.9)
3	OSC OUT	(0.15, 1.7)	21	4g, 4e	(2.5 , 0.15)	39	V_{SS1}	(4.3 , 2.1)
4	10PF	(0.15, 1.5)	22	4c, 4d	(2.7 , 0.15)	40	V_{SS2}	(4.3 , 2.3)
5	S3	(0.15, 1.5)	23	4c, 4a	(2.9 , 0.15)	41	V_{DD}	(4.3 , 2.5)
6	TEST A	(0.15, 0.95)	24	5g, 5e	(3.1 , 0.15)	42	DISP SELECT	(4.3 , 2.7)
7	COMMON 1	(0.15, 0.75)	25	5C, 5d	(3.3 , 0.15)	43	DIGIT SELECT	(4.3 , 2.9)
8	MON, SUN	(0.15, 0.55)	26	5b, 5a	(3.5 , 0.15)	44	TEST C	(4.3 , 3.1)
9	AM, PM	(0.15, 0.35)	27	6g, 6e	(3.7 , 0.15)	45	TEST D	(4.1 , 3.1)
10	1e, 24S	(0.15, 0.15)	28	6C, 6d	(3.9 , 0.15)	46	TEST I/O, B	(1.1 , 3.1)
11	1b, 1c	(0.5 , 0.15)	29	6b, 6a	(4.1 , 0.15)	47	TEST I/O, A	(0.9 , 3.1)
12	TUE, 2f	(0.7 , 0.15)	30	DATE, 6f	(4.3 , 0.15)	48	TEST E	(0.7 , 3.1)
13	2g, 2e	(0.9 , 0.15)	31	ALM MK/SIN	(4.3 , 0.4)	49	TEST B	(0.5 , 3.1)
14	2C, 2d	(1.1 , 0.15)	32	Sat, 5f	(4.3 , 0.6)	50	CUP 1	(0.15, 3.1)
15	2b, 2a	(1.3 , 0.15)	33	Fri, 4f	(4.3 , 0.8)	51	CUP 2	(0.15, 2.9)
16	Wed,Col	(1.5 , 0.15)	34	COMMON 2	(4.3 , 1.0)	52	LAMP IN	(0.15, 2.7)
17	Thu, 3f	(1.7 , 0.15)	35	INITIAL	(4.3 , 1.2)	53	V_{SS1}	(0.15, 2.5)
18	3g, 3e	(1.9 , 0.15)	36	S2	(4.3 , 1.4)	54	V_{SS2}	(0.15, 2.3)

■ **Sample 6-Digit LCD Panel**



■ **Sample 4-Digit LCD Panel**



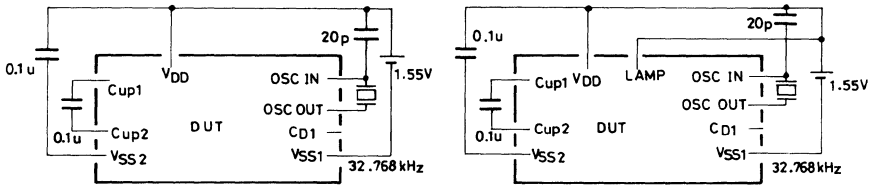
Absolute Maximum Ratings/T_a = 25±2°C, V_{DD} = 0 V				unit
Maximum supply voltage	V_{SS1}		−4 to 0.3	V
	V_{SS2}		−4 to 0.3	V
Input voltage	V_{IN1}	SET, SELECT, LAMP SW, TEST A to E, INITIAL, CD_1, OSC IN, DIGIT SELECT, DISP SELECT	V_{SS1}−0.3 to 0.3	V
Output voltage	V_{OUT1}	OSC OUT, TEST I/O A, TEST I/O B, CUP2	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	All segments, COMMON 1, COMMON 2, CUP1	V_{SS2}−0.3 to 0.3	V
Operating temperature	T_{opg}		−20 to +75	°C
Storage temperature	T_{stg}		−30 to +125	°C

Recommended Operating Conditions/T_a = 25±2°C, V_{DD} = 0 V				unit
Supply voltage	V_{SS1}		−1.65 to −1.30	V
	V_{SS2}		−3.3 to −2.40	V
Input "H" level voltage	V_{IH}	V_{SS1} = −1.30 to −1.65 V SET, SELECT, LAMP SW	−0.2 to 0	V
Input "L" level voltage	V_{IL}	V_{SS1} = −1.30 to −1.65 V SET, SELECT, LAMP SW	V_{SS1} to V_{SS1}+0.2	V
Operating frequency	f_{opg}	V_{SS1} = −1.30 to 1.65 V, T_a = −20 to +75°C	32 to 33	kHz

Electrical Characteristics/T_a = 25±2°C, V_{DD} = 0 V, V_{SS1} = −1.35 to −1.65 V			min	typ	max	unit
Input resistance	R_{IN1}	V_{SS1} = −1.55 V SET, SELECT, LAMP SW input.	200		2000	kΩ
	R_{IN2}	Test input	1		100	kΩ
	R_{IN3A}	V_{SS1} = −1.55 V "L" level hold Tr., DISP SELECT, 6/4 pin	10		100	kΩ
	R_{IN4A}	V_{SS1} = −1.55 V, "L" level pull-in Tr., DISP SELECT, 6/4 pin.	200		2000	kΩ
Output "H" level voltage	V_{OH1}	V_{SS1} = −1.55 V, I_{OH} = −4 μA Segment, flag, sign, common	−0.2			V
	V_{OH2}	V_{SS1} = −1.55 V, I_{OH} = −4 μA COMMON 1, COMMON 2	−0.2			V
Output "L" level voltage	V_{OL1}	V_{SS1} = −1.55 V, I_{OL} = 4 μA Segment, flag, sign, common		V_{SS2}+0.2		V
	V_{OL2}	V_{SS1} = −1.55 V, I_{OL} = 4 μA COMMON 1, COMMON 2		V_{SS2}+0.2		V
Output "M" level voltage	V_{OM}	V_{SS1} = −1.55 V, I_{OH} = −4 μA, I_{OL} = 4 μA COMMON 1, COMMON 2	V_{SS1}−0.2	V_{SS1}+0.2		V
Input off leak current	I_{off}	V_{SS1} = −2 V, V_{SS2} = −4 V DISP SELECT off, 6/4 off.			0.1	μA
Step-up voltage	V_{SS2}	C1 = C2 = 0.1 μF, f_{opg} = 32.768 kHz, 3 MΩ across V_{DD} and V_{SS2}	−3.3		−2.5	V
Supply current	I_{DD}	Fig. 1 (a): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25 k			2.0	μA
		Fig. 1 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25 k			20	μA
Oscillation start voltage	V_{start}	Fig. 2 (a): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25k			1.45	V
		Fig. 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25k			1.30	V
Oscillation hold voltage	V_{HOLD}	Fig. 2 (a): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25k			1.40	V
		Fig. 2 (b): C1 = C2 = 0.1 μF, C_o = C_g = 20 pF, C_I = 25k			1.25	V

			min	typ	max	unit
Oscillation start time	T_{start}	Fig. 2 (a): V_1 = 1.55 V, C1 = C2 = 0.1 μF, $C_o = C_g$ = 20 pF, C_I = 25 k			10	sec
		Fig. 2 (b): V_1 = 1.40 V, C1 = C2 = 0.1 μF, $C_o = C_g$ = 20 pF, C_I = 25 k			10	sec
Oscillation correction capacitance	C_{D1}	External pin (C_{D1})	8	10	12	pF
	C_{D2}	OSC OUT contained Fig. 2 (b): V_1 = 1.40 V, C_1 = C2 = 0.1 μF, $C_o = C_g$ = 20 pF, C_I = 25 k	16	20	24	pF
Output rise time	t_r	V_{SS2} = −3.3 to −2.4 V, C_L = 100 pF, COMMON 50%, Segment 90%	−100		100	μsec
Output fall time	t_f	V_{SS2} = −3.3 to −2.4 V, C_L = 100 pF, COMMON 50%, Segment 10%	−100		100	μsec

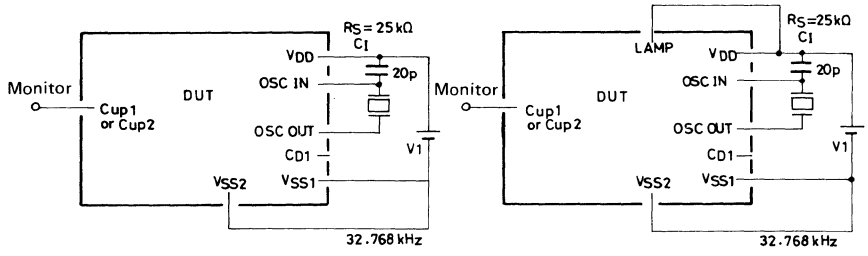
Current Dissipation Fig. 1



(a) Lamp input open (b) Lamp input applied

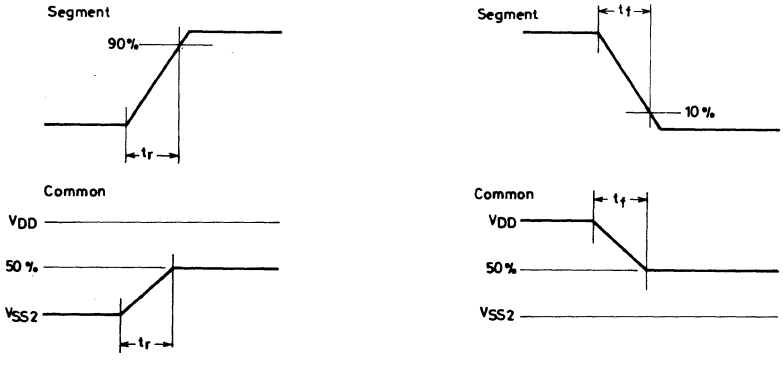
- Unentered pins are all open.
- $C_I \leqq 25$ k

Oscillation start voltage, Oscillation stop voltage, Oscillation start time Fig. 2



(a) Lamp input open (b) Lamp input applied

Rise time and fall time of segment and common



LC5645N

C MOS LSI

LCD Digital Watch

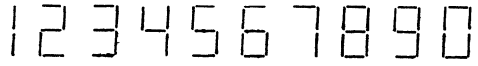
Ⓔ 1433A

1. Functions

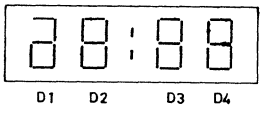
1. Real time (month, date, hours, minutes, seconds)
2. 2 switches of SET switch, SELECT switch
3. LCD light-up system by duplex drive
4. Selectable real time display mode
   - Hours, minutes display mode
   - Month, date display mode
   - Seconds display mode
5. Alternating display mode available
6. 12/24-hour operation mode selectable by chip bonding
7. Automatic calendar (Programmed to count date in February up to the 28th.)
8. Reference frequency f_{OSC}=32.768kHz
9. Battery voltage 1.5V, with built-in doubler circuit

2. Display System

1. 3-1/2 digits LCD
2. 32Hz duplex drive
3. Display font



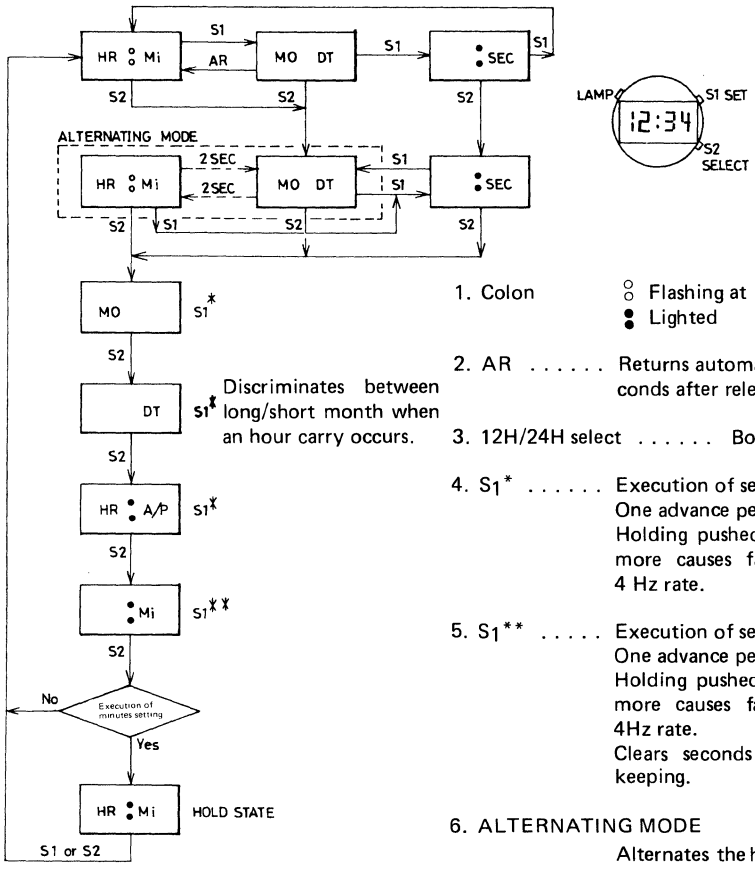
4. Panel layout



Hours	Minutes	← Hours, minutes display mode
Month	Date	← Month, date display mode
	Seconds	← Seconds display mode
Month		← Month display mode
	Date	← Date display mode
Hours		← Hours display mode
	Minutes	← Minutes display mode

5. Output pins for display . . . . . 14 pads
   Segment output 1st digit: 3 segments, 3rd digit: 6 segments, other 2 digits: 7 segments
   Colon . . . . . 1 segment
   Common . . . 2 pins of COMMON1, COMMON2
6. Total number of pads - - - 32 pads

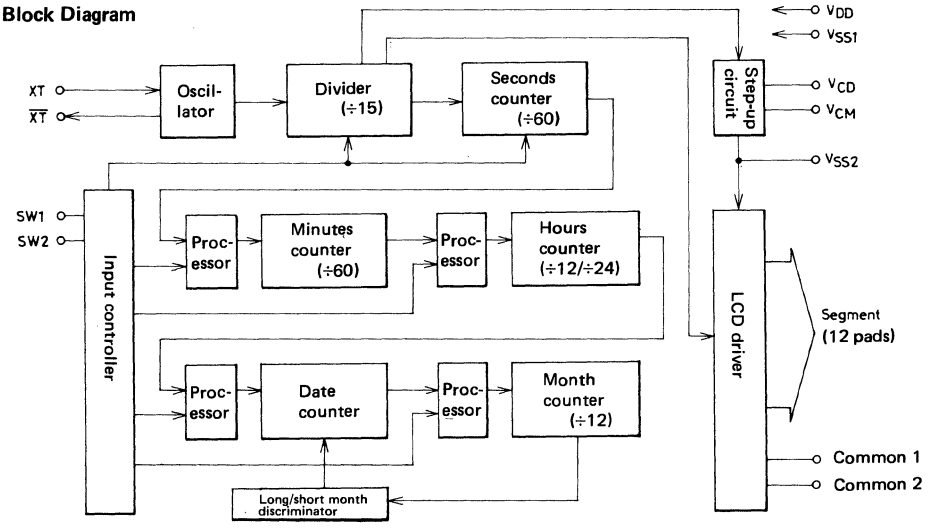
3. Operation Flow



Discriminates between long/short month when an hour carry occurs.

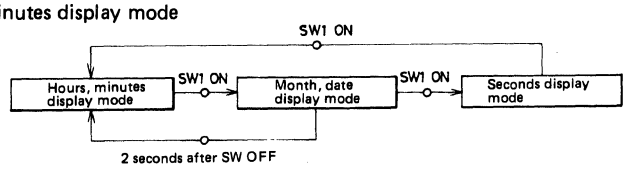
1. Colon — : Flashing at 1Hz 50% duty; : Lighted
2. AR ..... Returns automatically 1 to 2 seconds after releasing the switch.
3. 12H/24H select ..... Bonding option
4. S_1* ..... Execution of setting
   One advance per push
   Holding pushed for 1 second or more causes fast advance at a 4 Hz rate.
5. S_1** ..... Execution of setting
   One advance per push
   Holding pushed for 1 second or more causes fast advance at a 4Hz rate.
   Clears seconds and stops timekeeping.
6. ALTERNATING MODE
   Alternates the hours, minutes display mode/month, date display mode at 2-second intervals.
7. A/P ..... Indicates AM/PM in 12-hour operation mode.
   (Example)
   AM: 6:⌴A (6a.m.) — Space
   PM: 7:⌴P (7p.m.)
8. HOLD STATE
   Holds the counter and stops timekeeping
   Pushing switch S_1 or S_2 starts timekeeping.
9. Pushing switches S_1 and S_2 simultaneously causes the initial mode to occur and the hours, minutes display mode is entered as follows:
   (12H display mode) AM 1:00:00 Jan. 1
   (24H display mode) 1:00:00 Jan. 1

4. Block Diagram



5. Operating Specification

5-1. Hours, minutes display mode

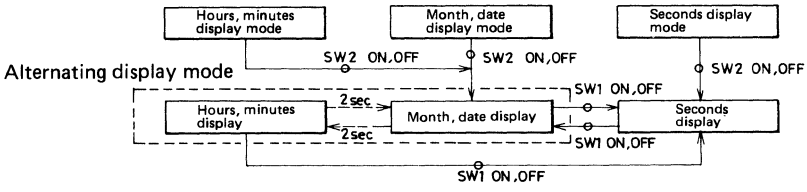


- In the hours, minutes display mode the colon flashes at a 1Hz rate and 50% duty.
- The 10's digit of hours is zero-blanked.
- In the 12-hour operation mode the hours digits change as 1 → 2 → · · · · · · → 12 → 1.
- In the 24-hour operation mode the hours digits change as 0 → 1 → · · · · · · · · · · · · → 23 → 0.

5-2. Month, date display mode
- In the month, date display mode the colon is unlighted.
- The 10's digit of both month and date is zero-blanked.
- Discrimination between long month and short month is exercised when an hour carry occurs and February date is counted up to 28th.

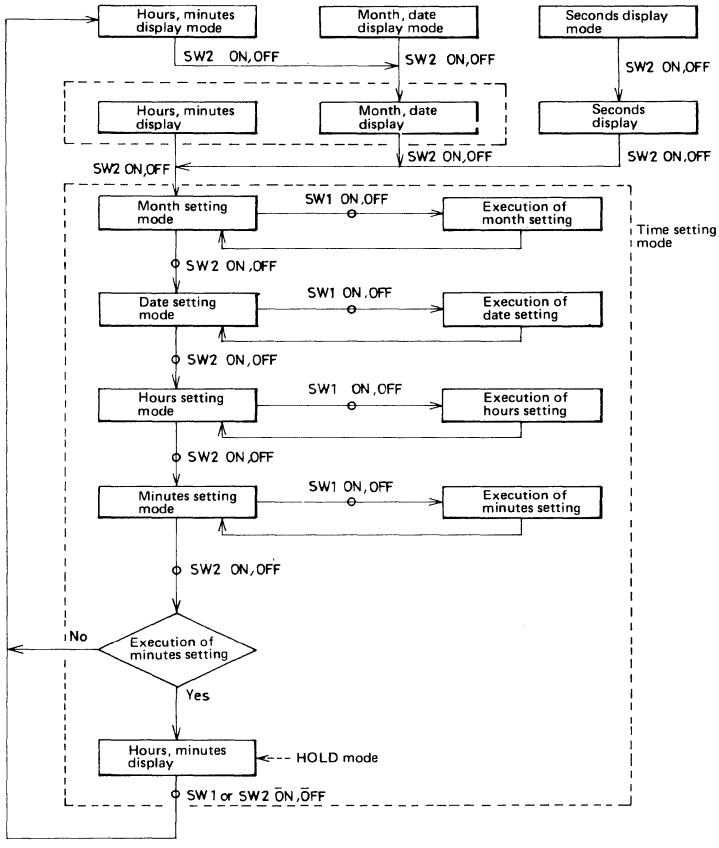
5-3. Seconds display mode
- In the seconds display mode the colon flashes.
- Seconds are displayed on the right 2 digits, with the left 2 digits blanked.

5-4. Alternating display mode



- By pushing switch S_2 in the hours, minutes display mode or month, date display mode, the alternating display mode is entered. By pushing switch S_2 and then switch S_1 in the seconds display mode, the alternating display mode is also entered.
- When the alternating display mode is entered, the month, date display appears. The hour, minutes display appears 2 seconds later, and then the month, date display returns 2 seconds later. This is repeated.

5-5. Time setting mode

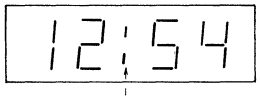


- Only the digit to be set is lighted and displayed. In the month setting mode the month digits only are displayed.
- In the month or hours setting mode the month or hours are displayed on the left 2 digits.
  In the date or minutes setting mode the date or minutes are displayed on the right 2 digits.
- In the hours or minutes setting mode the colon is lighted.
  In the month or date setting mode the colon is unlighted.
- Each time SW_1 is pushed/released in each setting mode, the display contents are incremented +1. Holding SW_1 pushed for 1 to 2 seconds or more causes the display contents to advance at a 4Hz rate.
- Execution of setting in each setting mode
  - (a) Execution of month setting . . . . . The month counter counts up to 12.
  - (b) Execution of date setting . . . . . The date counter counts up to 31 regardless of long/short month. No carry to the month digits occurs. Discrimination between long month and short month is exercised only when a carry from the hours digits occurs.
  - (c) Execution of hours setting . . . . . In the 12-hour operation mode "A" is displayed on the rightmost digit when in the morning; "P" is displayed when in the afternoon. The display contents change as 11a.m. → 12p.m. → 1p.m. or 11p.m. → 12a.m. → 1a.m.
    In the 24-hour operation mode the display contents change as 23 → 0. No carry to the date digits occurs.

(d) Execution of minutes setting . . . When minutes setting is executed, seconds are cleared and the time is held as set. This is proved by the fact that when SW_2 is pushed/released after execution of minutes setting the hours, minutes display appears but the colon remains lighted without flashing. By pushing/releasing SW_1 or SW_2 under this state, the time hold is released, timekeeping starts, and the normal hours, minutes display mode returns with the colon flashing. If in the minutes setting mode SW_2 is pushed/released without execution of minutes setting, the setting mode returns to the normal hours, minutes display mode.

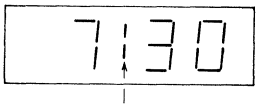
6. Sample Display of Each Mode

6-1. Hours, minutes display mode
(For the alternating display mode also, this applies.)



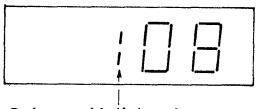
Colon: Flashing at a 1Hz rate (50% duty)
Hour, minutes display (12:54)

6-2. Month, date display mode
(For the alternating display mode also, this applies.)



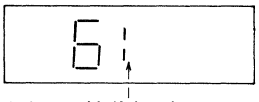
Colon: Unlighted
Month, date display (July 30)

6-3. Seconds display mode



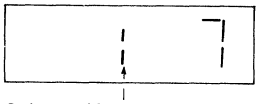
Colon: Unlighted
Seconds display (08)

6-4. Month setting mode



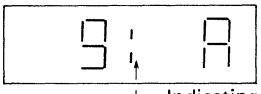
Colon: Unlighted
Month only (June)

6-5. Date setting mode



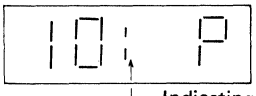
Colon: Unlighted
Date only (7)

6-6. Hours setting mode



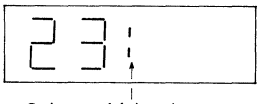
Colon: Lighted Indicating AM

12-hour operation mode Hours only
(9a.m.)



Colon: Lighted Indicating PM

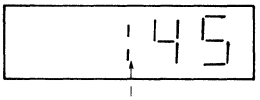
12-hour operation mode Hours only
(10p.m.)



Colon: Lighted

24-hour operation mode Hours only
(23)

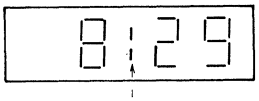
6-7. Minutes setting mode



Colon: Lighted

Minutes only (45)

6-8. Hold mode



Colon: Lighted
Hours, minutes display (8:29)

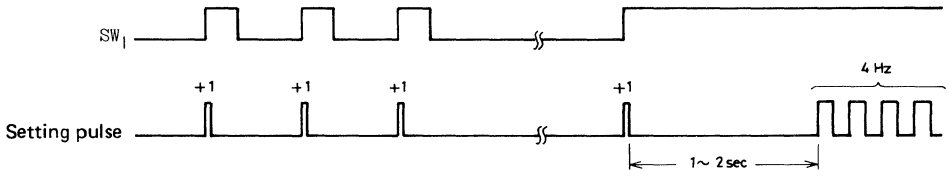
7. Others

7-1. Zero blanking . . . . . Unnecessary 0's are unlighted.
Unlighted content . . . . . The 10's digit of month, date, hours is zero-blanked.
Lighted content . . . . . 0 in the 10's digit of minutes, seconds is lighted.

7-2. Switch input voltage
The INPUT pin contains a floating preventing resistor. V_{DD} is applied to this pin to start operation.

7-3. 24/12-hour operation mode select
For the 12-hour operation mode, the 24H/12H pin is not bonded. For the 24-hour operation mode, this pin is bonded.

7-4. Setting pulse
Each time SW_1 is pushed in each setting mode, the display contents are incremented +1. Holding SW_1 pushed causes fast advance at a 4Hz rate to start approximately 1 second later.



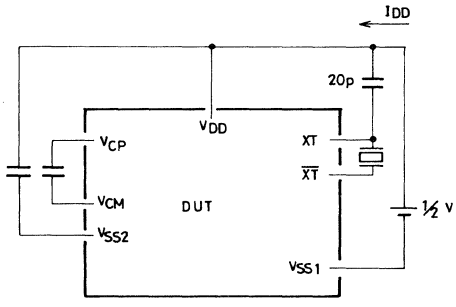
7-5. Switch chattering preventer
Chattering of 30msec. or less is prevented. (More than 30msec. is considered to be bounding.)

7-6. Step-up circuit
Two capacitors (0.1μF) are connected externally. The step-up frequency is 512Hz.

7-7. Initial clear
The circuit is built in. The initial mode can be also entered by pushing SW_1 and SW_2 simultaneously.

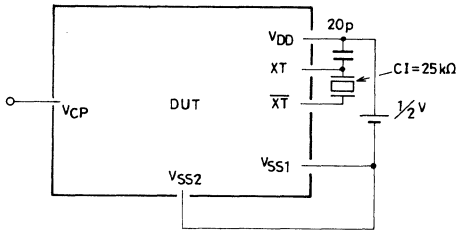
7-8. LCD output alternating frequency 32Hz

Supply current

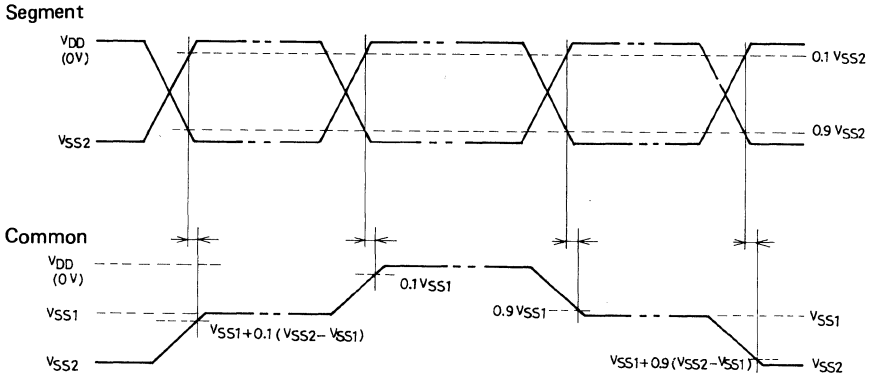


(Note) • Pins not entered are all open.
• CI≦25kohm

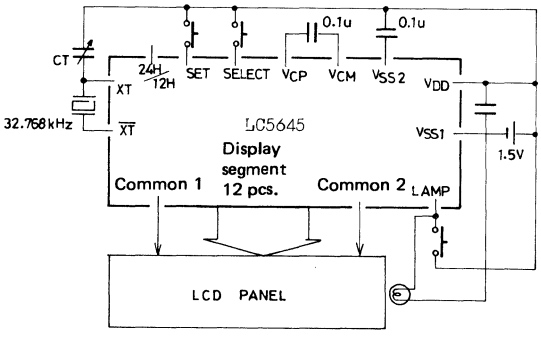
Oscillation start voltage, oscillation stop voltage, oscillation start time



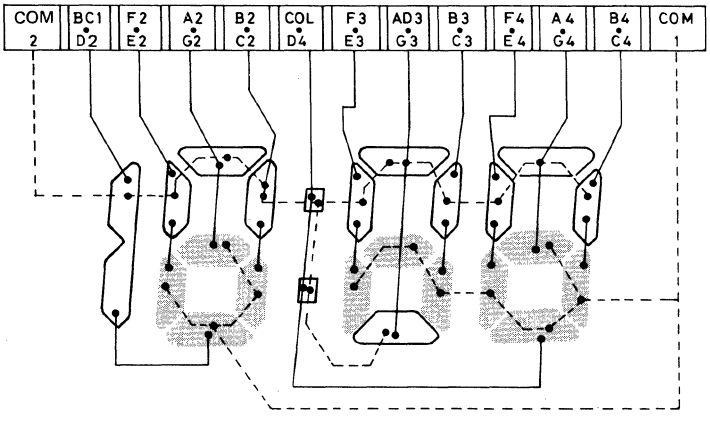
Common-segment time lag



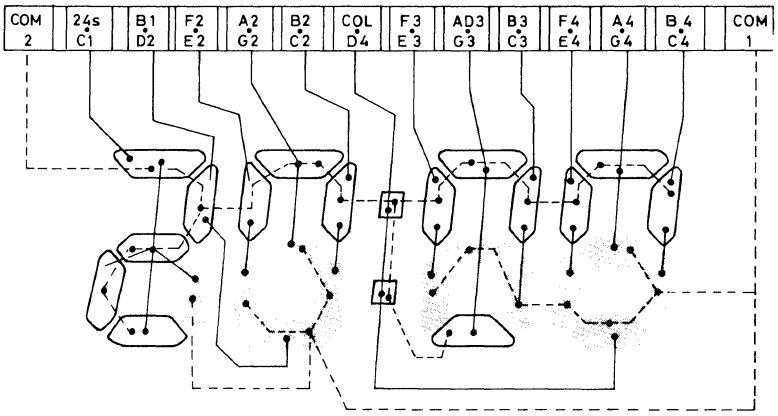
■ **Sample Application Circuit**



LCD Format (12 hour display format)



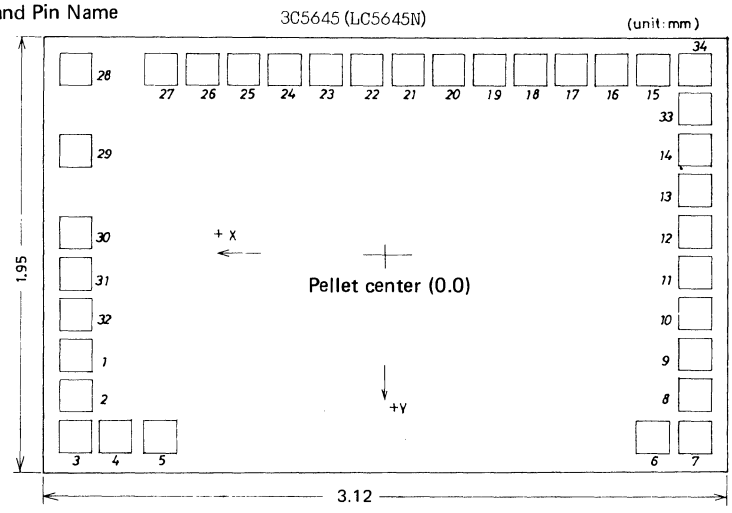
LCD Format (24 hour display format)



Pad No. and Pin Name

3C5645 (LC5645N)

(unit: mm)



Pad No.	Pin Name	X coordinates (μm)	Y coordinates (μm)	Pad No.	Pin Name	X coordinates (μm)	Y coordinates (μm)
1	V_{dd}	1407	450	18	F4/E4	−585	−822
2	V_{CP} (Cup2)	1407	630	19	B3/C3	−405	−822
3	V_{cm} (Cup1)	1407	822	20	AD3/G3	−225	−822
4	Test 2	1225	822	21	F3/E3	−45	−822
5	32Hz	1045	822	22	C_{O}1/D4	135	−822
6	Test 1	−1193	822	23	B2/C2	315	−822
7	V_{ss1}	−1407	822	24	A2/G2	495	−822
8	S2	−1407	630	25	F2/E2	675	−822
9	V_{dd}	−1407	450	26	B1/D2	855	−822
10	24H/12H	−1407	270	27	24S/C1	1035	−822
11	V_{ss2}	−1407	90	28	Common 2	1407	−822
12	Test 3	−1407	−90	29	Lamp	1407	−467
13	Test 4	−1407	−270	30	$\overline{XT}$ (Osc Out)	1407	−90
14	S1	−1407	−450	31	10PF	1407	90
15	Common 1	−1125	−822	32	XT (Osc In)	1407	270
16	B4/C4	−945	−822	33	Monitor	1407	−630
17	A4/G4	−765	−822	34	Monitor	1407	−822

* The pad coordinates are such that the pellet center is taken as the origin (0.0).

Absolute Maximum Ratings/T_a = 25°C, V_{DD} = 0V

				Unit
Maximum supply voltage (1)	V_{SS1}		−4 ~ +0.3	V
Maximum supply voltage (2)	V_{SS2}		−4 ~ +0.3	V
Input voltage	V_{IN}	S_1, S_2, LAMP, T_1 ~ T_4, XT, 24H/12H	V_{SS1} −0.3 ~ +0.3	V
Output voltage (1)	V_{OUT1}	XT, 32Hz, V_{CP}	V_{SS1} −0.3 ~ +0.3	V
Output voltage (2)	V_{OUT2}	All segments, Common1, Common2, V_{CM}	V_{SS2} −0.3 ~ +0.3	V
Operating temperature	T_{opg}		−20 ~ +75	°C
Storage temperature	T_{stg}		−30 ~ +125	°C

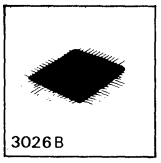
Recommended Operating Conditions/T_a = 25°C, V_{DD} = 0V

					Unit
Supply voltage (1)	V_{SS1}			−1.65 ~ −1.3	V
Supply voltage (2)	V_{SS2}	V_{SS1} = −1.3 ~ −1.65		−3.3 ~ −2.4	V
Input high level	V_{IH}	V_{SS1} = −1.55V	S_1, S_2	−0.2 ~ +0	V
Input low level	V_{IL}	V_{SS1} = −1.55V	S_1, S_2	V_{SS1} ~ +V_{SS1}+0.2	V

Electrical Characteristics/T_a = 25°C, V_{DD} = 0V, V_{SS} = −1.3 ~ −1.65V

			min	typ	max	unit
Input resistance	R_{IN1}	V_{SS1} = −1.55V, S_1, S_2, Lamp	200		2000	kΩ
Input resistance	R_{IN2}	V_{SS1} = −1.55V, test input	1		100	kΩ
Input resistance	R_{IN3}	V_{SS1} = −1.55V, "L" level hold T_r, 24H/12H	10		100	kΩ
Input resistance	R_{In4}	V_{SS1} = −1.55V, "L" level pull-in T_r, 24H/12H	200		2000	kΩ
Output "H" level voltege	V_{OH1}	V_{SS1} = −1.55V, I_{OH} = −0.4μA, segment, colon	−0.2			V
Output "L" level voltage	V_{OL1}	V_{SS1} = −1.55V, I_{OL} = 0.4μA, segment, colon			V_{SS2} +0.2	V
Output "H" level voltage	V_{OH2}	V_{SS1} = −1.55V, I_{OH} = −4μA, Common1, Common2	−0.2			V
Output "M" level voltage	V_{OM}	V_{SS1} = −1.55V, I_{OH} = −4μA, I_{OL} = 4μA, Common1, Common2	V_{SS1} −0.2		V_{SS1} +0.2	V
Output "L" level voltage	V_{OL2}	V_{SS1} = −1.55V, I_{OL} = 4μA, Common1, Common2			V_{SS2} +0.2	V
Input leakage current	I_{off}	V_{SS1} = −2V, V_{SS2} = −4V, 24/12H off mode			0.1	μA
Step-up voltage	V_{SS2}	C_1 = C_2 = 0.1μF, 3MΩ across V_{DD} − V_{SS2} f_{opg} = 32.768kHz	−3.3		−2.5	V
Supply current	I_{DD}	V_{SS1} = −1.55V, C_1 = C_2 = 0.1μF C_o = C_g = 20pF, Cl = 25kΩ		1.0	2.0	μA
Oscillation start voltage	V_{START}	C_1 = C_2 = 0.1μF, C_o = C_g = 20pF, Cl = 25kΩ			−1.45	V
Oscillation hold voltage	V_{HOLD}	C_1 = C_2 = 0.1μF, C_o = C_g = 20pF, Cl = 25kΩ			−1.3	V
Oscillation start time	t_{START}	V_{SS1} = −1.55V, C_1 = C_2 = 0.1μF, C_o = C_g = 20pF, Cl = 25kΩ			10	sec
Oscillation capacitance (10pF pin)	C_o		8		12	pF
Common-segment time lag	t_D	V_{SS2} = −3.3 ~ −2.5V, C_L = 100p	−100	100	100	μsec
Built-in Capacitance	C_D			20		PF

LC7600



C MOS LSI

LCD Digital Clock

Ⓔ 868A

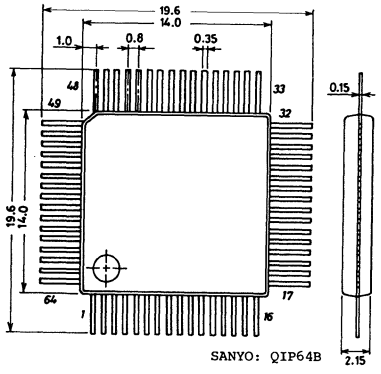
Use

- Digital clock with alarm, sleep timer for radio cassette, tape recorder applications
- Digital clock with alarm, tape counter for radio cassette, tape recorder applications
- Digital clock with alarm, second clock for travel clock applications

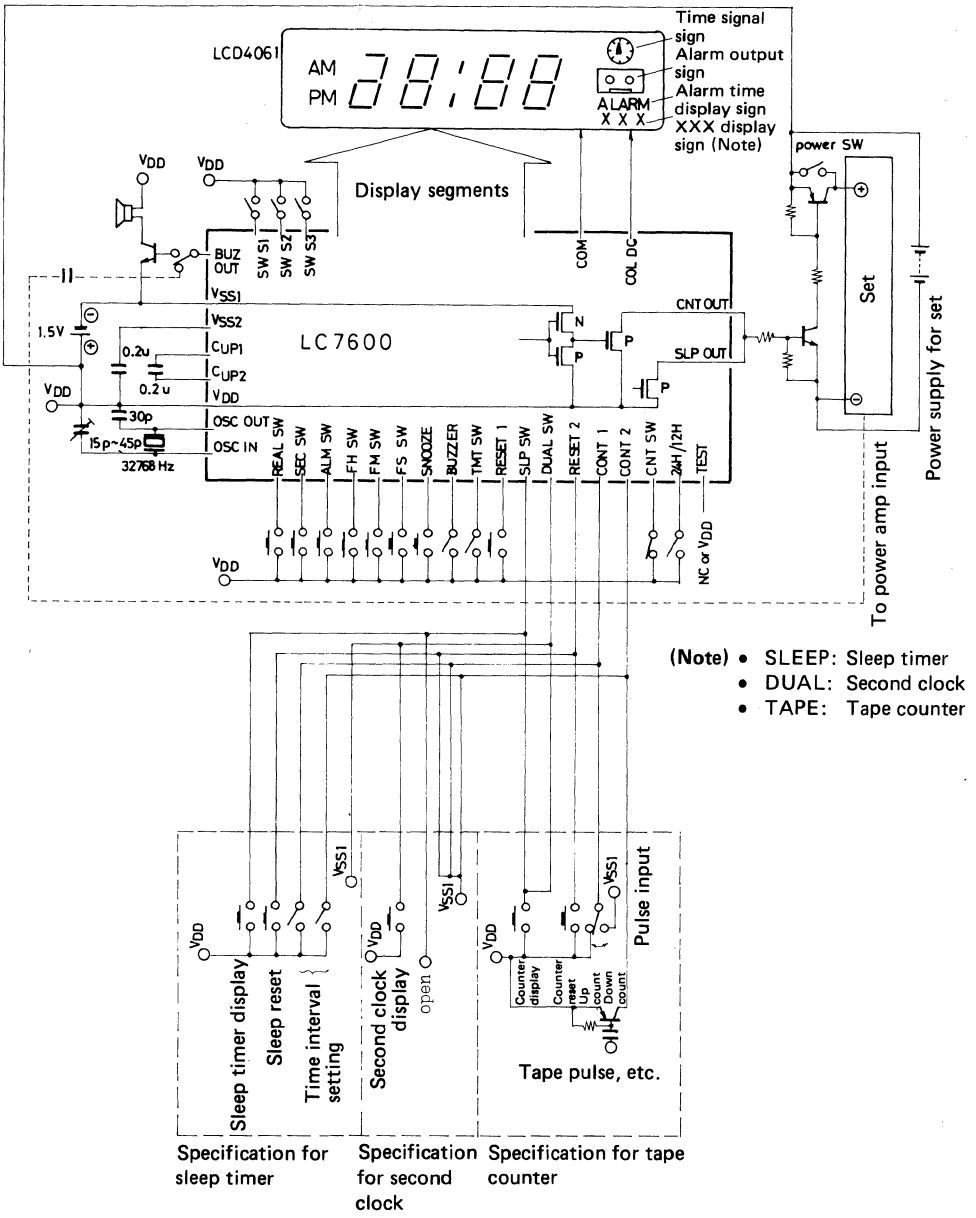
Features

- LCD static drive system: 3.5 digits, 7 segments, and various signs
- Built-in functions
  - Real time counter, counter for alarm with snooze, up/down counter
  - The up/down counter can be used for sleep timer, second clock, or tape counter by selecting one of these functions when designing a set.
- For the display mode select switch, either push switch or slide switch can be selected when designing a set.
- Various control output pins
  - Alarm control output (Settable to 15, 30, 45, 60, 90, 120 minutes)
  - Sleep output (Settable to 120 (max.), 60, 30 minutes and also settable up to 120 minutes with an increment of one minute)
  - Alarm sound output (For 4 to 5 minutes without a break)
  - Tape counter output for zero stop (Also used for sleep output)
- Various control input pins
  - Reset 1 input (For resetting alarm control output and alarm sound)
  - Reset 2 input (For resetting sleep output or tape counter)
  - Snooze input (Possible to interrupt alarm sound output for 4 to 5 minutes. Repeatedly usable)
- In applications where the push switch is selected for the display mode select switch, the real time display mode returns automatically from the alarm time display mode or sleep timer time display mode after lapse of a specified time.
- Others
  - Possible to monitor alarm sound
  - Possible to set seconds at the touch of a switch
  - Reference frequency: 32.768 kHz (X'tal)
  - V_{DD} = 1.5 V typ. (With 3 V power supply doubler for LCD drive)
  - Case outline: QIP-64
  - LC7600-used clock module: DQ-460

Case Outline 3026B-Q64BIC
(unit: mm)

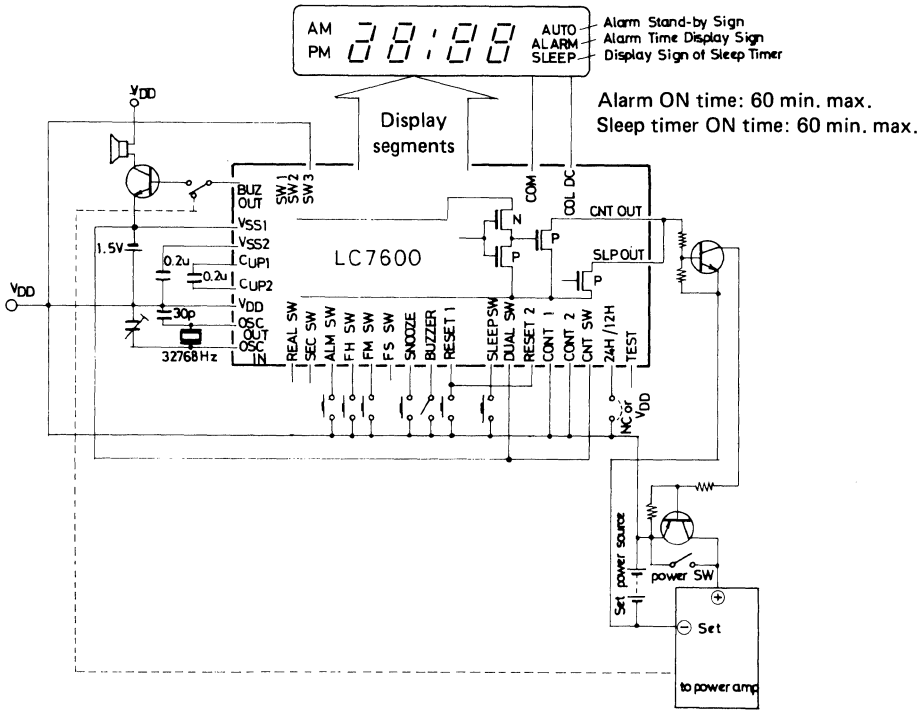


1. Sample Application Circuit (1)

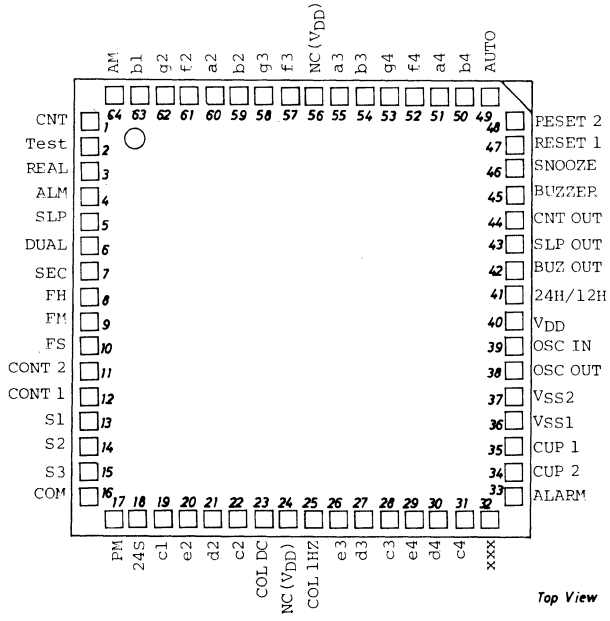


Note) If a piezo is used as the sound generator, noise from the piezo may cause malfunction. Therefore, a circuit to eliminate malfunction must be added.

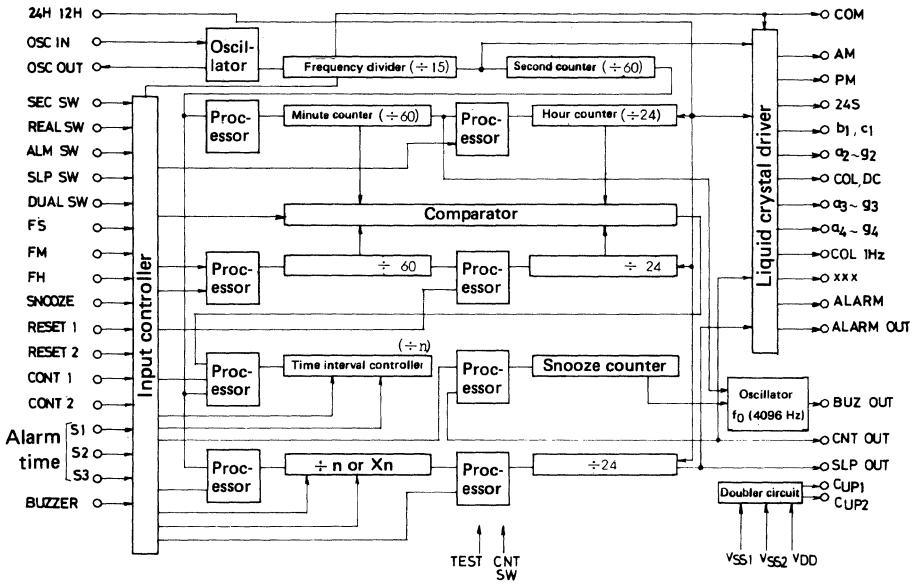
Sample Application Circuit (2)



2. Pin Assignment

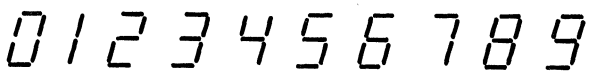


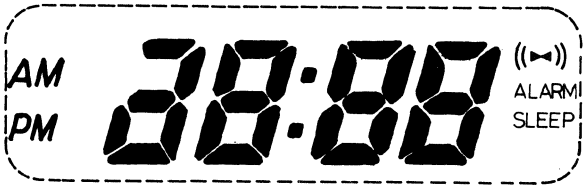
3. Equivalent Circuit Block Diagram



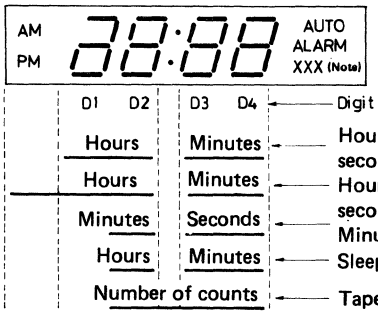
4. Display

4-1. Display font





4-2. Display segments



Hours-minutes display of real time, alarm, second clock (24-hour system)

Hours-minutes display of real time, alarm, second clock (12-hour system)

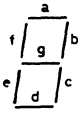
Minutes-seconds display of real time

Sleep timer display

Tape counter display Max. 999

(Note)
Each display shown below appears according to the operation mode of the counter.

Operation Mode of Counter	Display
Sleep timer	SLEEP
Second clock	DUAL
Tape counter	TAPE



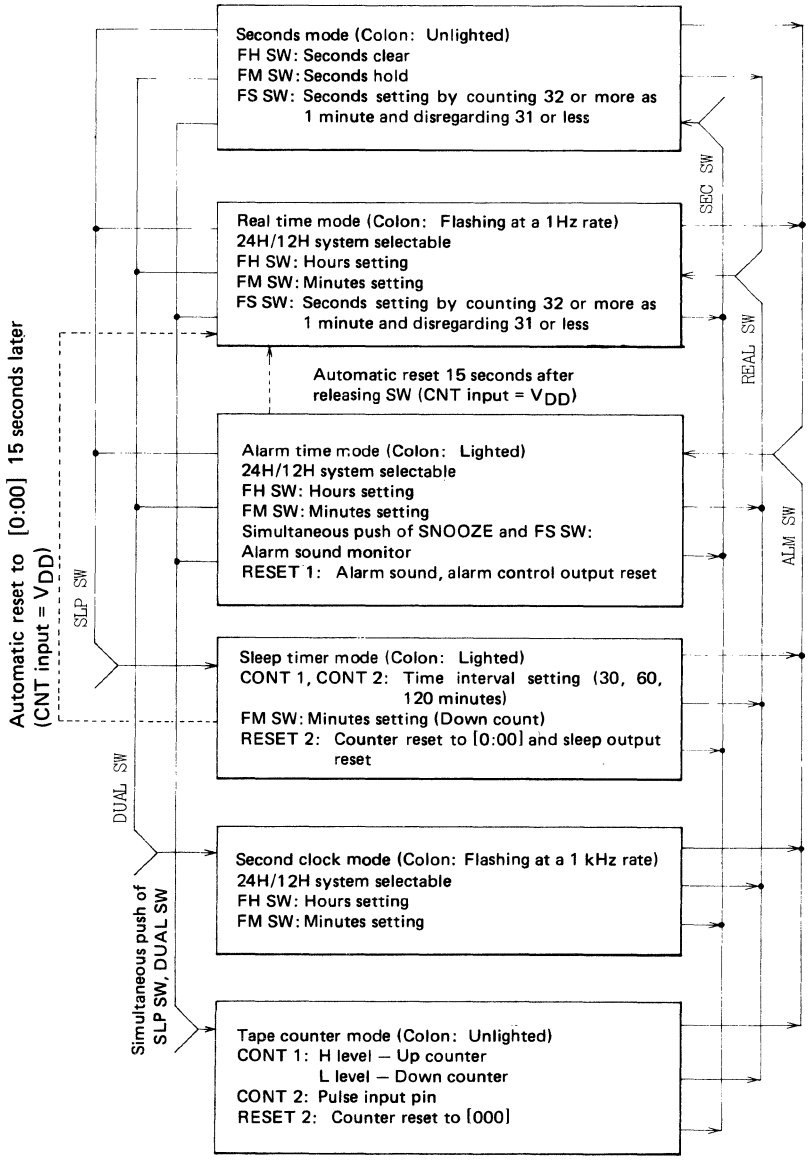
For 24S, see page 9.

4-3. Display range

(a) Real time, alarm time, second clock display
- 12-hour system/AM1:00 to PM12:59 (1 o'clock sharp in the morning to 59 minutes past 12 o'clock in the afternoon)
- 24-hour system/0:00 to 23:59 (0 hour 00 minute to 23 hours 59 minutes)

(b) Minutes-seconds display of real time/0 00 to 9 59 (0 minute 00 second to 9 minutes 59 seconds)
(c) Sleep timer display/0:00 to 2:00 (0 hour 00 minute to 2 hours 00 minute)
(d) 000 to 999 (Number of counts 000 to 999)

5. Operation Flow Chart



6. Priority of Display Mode Select Input (REAL, ALM, SLP, DUAL, SEC)

1) When V_{SS1} is applied to CNT input:

Case	REAL	ALM	SLP	DUAL	SEC	Display Mode
1	–	off	off	off	off	Real time
	on	–	–	–	–	
2	off	on	–	–	–	Alarm time
3	off	off	on	on	–	Tape counter
4	off	off	on	off	–	Sleep timer Note)
5	off	off	off	on	–	Second clock
6	off	off	off	off	on	Seconds

Note) The moment the sleep display mode is entered with the sleep output (SLP OUT) turned off, the sleep timer is set to a time interval fixed by the CONT1, CONT2 and the sleep output is turned on.

2) When V_{DD} is applied to CNT input:

Case	REAL	ALM	SLP	DUAL	SEC	Display Mode	Remarks
1	on	off	–	–	off	Real time	
2	off	on	–	–	off	Alarm time	When the mode where the alarm switch is turned on is changed to the mode where all switches are turned off, the real time display mode returns 10 seconds later.
3	off	off	on (Simultaneously)		–	Tape counter	Even when this mode is changed to the mode where all switches are turned off, the tape counter display mode is held.
4	off	off	on	off	–	Sleep timer Note)	Even when this mode is changed to the mode where all switches are turned off, the sleep timer display mode is held.
5	off	off	off	on	–	Second clock	Even when this mode is changed to the mode where all switches are turned off, the second clock display mode is held.
6	off	off	off	off	on	Seconds	

Note) 1. The moment the sleep display mode is entered with the sleep output (SLP OUT) turned off, the sleep timer is set to a time interval fixed by the CONT1, CONT2 and the sleep output is turned on.
2. The real time display mode returns automatically, 15 seconds after the sleep timer display becomes 0:00 and the sleep output (SLP OUT) is turned off.
3. on: V_{DD} level, off: open or V_{SS1}, –: V_{DD} or open or V_{SS1}

7. FH, FM , FS Operation at Each Display Mode

Display Mode	Switch	Operation
Real Time	FH	One push executes 1 setting of hours. Pushing for 2 seconds executes hours setting at a 4 Hz rate.
	FM	One push executes 1 setting of minutes. Pushing for 2 seconds executes minutes setting at a 4 Hz rate.
	FS	Clears seconds. When the seconds display is at 32 or more, minutes are incremented by 1.
Alarm Time	FH	One push executes 1 setting of hours. Pushing for 2 seconds executes hours setting at a 4 Hz rate.
	FM	One push executes 1 setting of minutes. Pushing for 2 seconds executes minutes setting at a 4 Hz rate.
	FS	Not operated.
Tape Counter	FH	Not operated.
	FM	Not operated.
	FS	Not operated.
Sleep Timer	FH	Not operated.
	FM	One push executes 1 setting of minutes. Pushing for 2 seconds executes minutes setting at a 4 Hz rate. Hours setting is coupled with minutes setting.
	FS	Not operated.
Second Clock	FH	One push executes 1 setting of hours. Pushing for 2 seconds executes hours setting at a 4 Hz rate.
	FM	One push executes 1 setting of minutes. Pushing for 2 seconds executes minutes setting at a 4 Hz rate.
	FS	Not operated.
Seconds	FH	Clears seconds of the real time.
	FM	Holds seconds of the real time.
	FS	Clears seconds of the real time. When the seconds display is at 32 or more, minutes are incremented by 1.

Note) 1. "Setting" mentioned above: Down count – Sleep timer
Up count – Other than sleep timer
2. For the sleep timer function, hours-minutes coupled setting is executed with the FM switch.
3. For other functions than the sleep timer, hours setting and minutes setting are executed separately.

8. Control Input Pin Description

8-1. Reset 1 input
1) Application of V_{DD} turns off the CNT OUT, BUZ OUT and disarms the alarm.
2) The alarm output sign (AUTO sign) is unlighted when V_{SS} is applied.

8-2. The reset 2 input works according to the operation mode (tape counter, sleep timer, second clock) of the up/down counter as follows:
1) Tape counter: Application of V_{DD} resets the contents of the counter to [000].
2) Sleep timer: Application of V_{DD} turns off the SLP OUT and disarms the sleep timer. The sleep timer is reset to 0 hour 00 minute.
3) Second clock: Not operated.

8-3. Buzzer input
1) Input pin for sounding the buzzer or playing the radio when the alarm time is reached.
2) With V_{DD} applied, the CNT OUT and BUZ OUT deliver the signal when the alarm time is reached and continue delivering the signal for 5 minutes. This serves to sound the buzzer.
3) With the pin open, the CNT OUT delivers the signal when the alarm time is reached and continues delivering the signal for a period of time determined by the S1 to S3. This serves to play the radio.

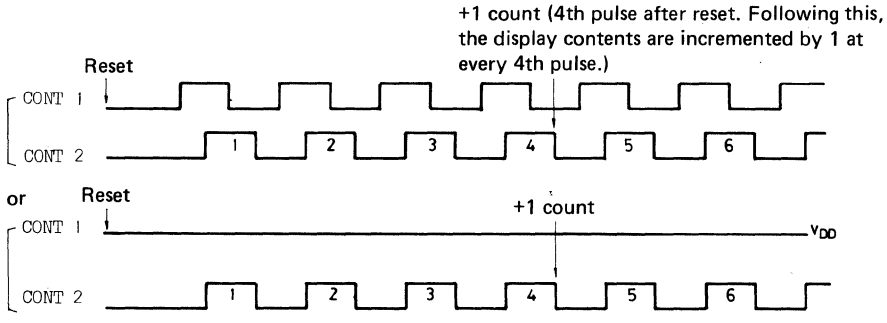
8-4. Snooze input
1) Input pin for operating the snooze function. This pin works only when V_{DD} is applied to the buzzer input.
2) Application of V_{DD} when the BUZ OUT delivers the signal turns off the BUZ OUT. The BUZ OUT is turned on again 4 to 5 minutes later and turned off 5 minutes later. (Snooze function)
3) The snooze function can be used repeatedly.
4) By setting the display mode to the alarm time display mode and applying V_{DD} to both FS input and snooze input, the buzzer sound can be monitored.

8-5. S1 to S3 input
1) Input pin for fixing the time interval of the alarm
2) The time interval is as shown below.

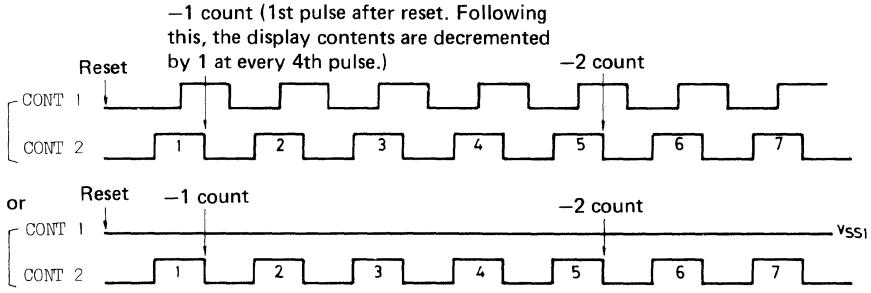
S1	S2	S3	Nominal Time Interval	Actual Time Interval
H	L	L	15 min.	18 min.
L	H	L	30 min.	34 min.
H	H	L	45 min.	48 min.
◎	L	H	60 min.	64 min.
◎	H	H	90 min.	94 min.
L	L	L	120 min.	126 min.

H: V_{DD} level
L: V_{SS1} level
◎: Either H or L

8-6. CONT1, CONT2 input
1) The CONT1, CONT2 work according to the operation mode (tape counter, sleep timer, second clock) of the up/down counter as follows:
2) Tape counter: Tape pulse input and up/down count select
(a) Operation waveform during up-counting



(b) Operation waveform during down-counting



3) Sleep timer: Max. time interval select
The time interval is shown below.

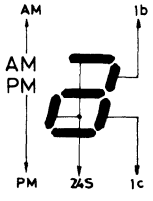
CONT 1	CONT 2	Time Interval
H	L	30 min.
◎	H	60 min.
L	L	120 min.

H: V_{DD} level
L: V_{SS1} level
◎: Either H or L

4) Second clock: Not operated

8-7. 24H/12H input

1) Input pin for selecting 24-hour system/12-hour system with AM/PM
2) Application of V_{DD} selects the 24-hour system; and making open or application of V_{SS1} selects the 12-hour system.
3) Segment correspondence



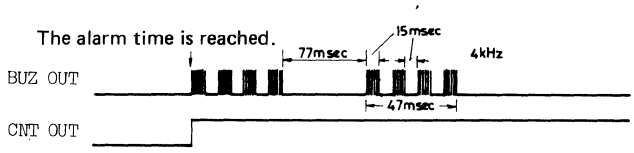
8-8. CNT input

1) Input pin for determining whether to connect the memory circuit which stores the switch on/off signal to the display input (REAL, SEC, ALM, SLP, DUAL)
2) Application of V_{SS1} causes the display mode to be entered as shown in 6.1).
3) Application of V_{DD} causes the display mode to be entered as shown in 6.2).

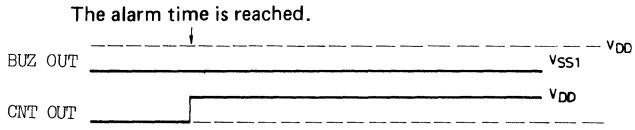
9. Output Pin Description

9-1. Buzzer output pin (BUZ OUT)
With V_{DD} applied to the buzzer pin, this pin delivers the signal to sound the alarm when the alarm time is reached. The output pin is of complementary type. (Refer to 9-2.)

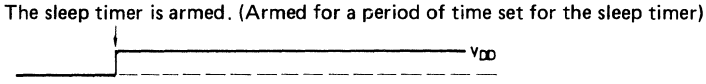
9-2. Alarm control output pin (CNT OUT)
Regardless of the buzzer pin status, this pin delivers the signal to play the radio when the alarm time is reached. The output pin is of P channel open drain type.
(1) Output waveform when V_{DD} is applied to the buzzer pin (Delivered for 5 minutes)



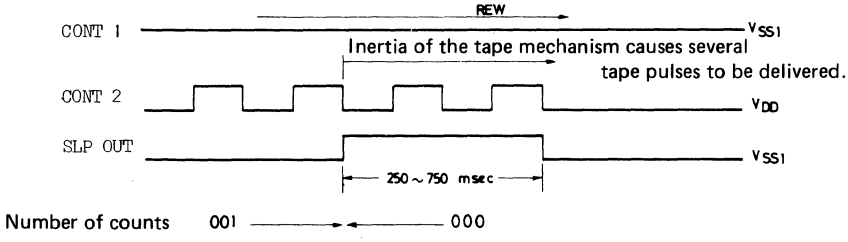
(2) Output waveform when the buzzer pin is open or set to V_{SS1}
(Delivered for a period of time determined by the S1, S2, S3)



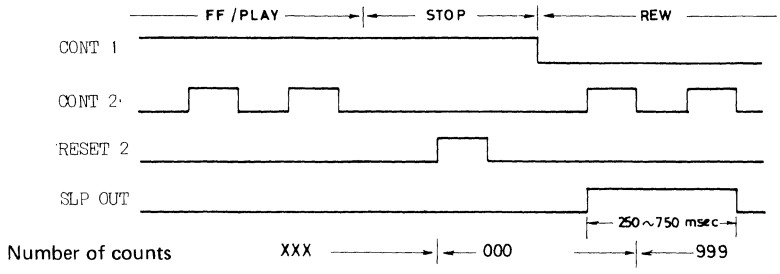
9-3. Sleep output pin (SLP OUT)
This pin works according to the operation mode (tape counter, sleep timer, second clock) of the up/down counter as follows: The output pin is of P channel open drain type.
1) Sleep timer



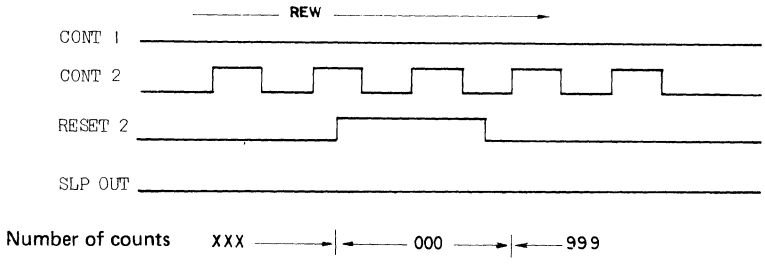
2) Tape counter
(1) The 0 stop output is delivered when the number of counts reaches 000 during down-counting.



(2) When the up-count mode (FF, PLAY) is changed to the stop mode (STOP) and the tape counter is reset and then the down-count mode (REW) is entered, the 0 stop output is delivered.



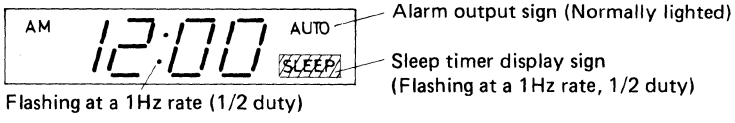
(3) Even when the tape counter is reset during down-counting (REW), no 0 stop output is delivered.



3) Second clock
Not operated

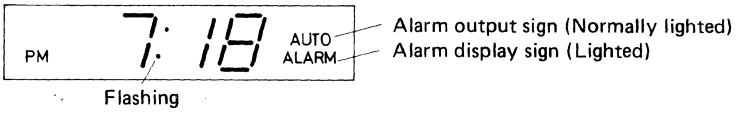
10. Sample Display at Each Operation Mode

1) Real time display mode



Hours-minutes display (12-hour system)
(12 o'clock sharp in the morning, sleep timer armed)

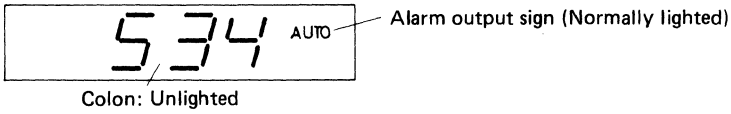
2) Alarm time display mode



Alarm time display (12-hour system)
(18 minutes past 7 o'clock in the afternoon)

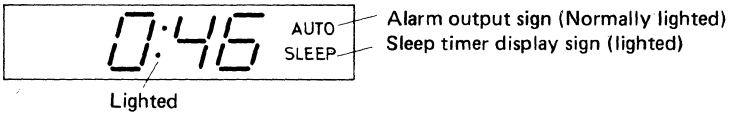
- With V_{DD} applied to the buzzer input, the BUZ OUT and CNT OUT delivers the signal for 5 minutes after the alarm time is reached. When the CNT OUT delivers the signal, the snooze function can be used. (Refer to 8-4. Snooze input.)
- When the buzzer input is open (or set to V_{SS1}), the CNT OUT delivers the signal for a time interval determined by the S1 to S3 after the alarm time is reached. (Refer to 8-5. S1 to S3 input.)
- The RESET1 input can be used to turn off the BUZ OUT, CNT OUT.

3) Seconds display mode



Seconds display: One digit of the real time and seconds are displayed. (5 minutes 34 seconds)

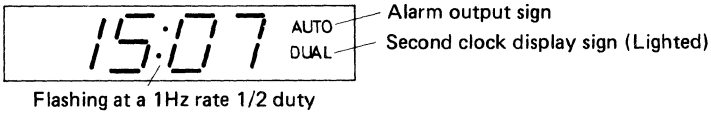
4) Sleep timer display mode



Sleep timer display (46 minutes)

- The sleep timer display sign is lighted. If other mode (real time display, seconds display, alarm time display) is entered when the sleep timer is armed, the sleep timer display sign flashes at a 1Hz rate.
- A time interval of the sleep timer is determined by the CONT1 and CONT2. (Refer to 8-6. CONT1, CONT2 input.)
- When V_{DD} is applied to the RESET2 pin, the sleep timer is reset to 0:00 minute.

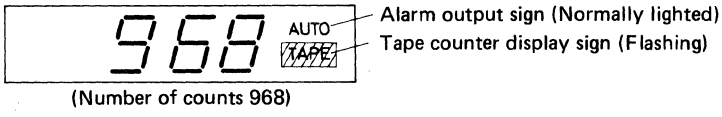
5) Second clock mode



Second clock display (24-hour system)
(15 hours 07 minutes)

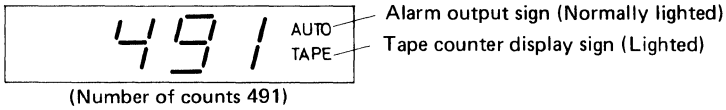
6) Tape counter display mode

Tape pulse input applied mode



(Number of counts 968)

No tape pulse input applied mode



(Number of counts 491)

- Simultaneous application of V_{DD} to the SLP pin and DUAL pin causes the display to appear.
- The tape counter display sign is held lighted when no tape pulse input is applied, and flashes at every tape pulse when the tape pulse input is applied.
- A 1/4 prescaler is contained.

11. Main Specifications

Absolute Maximum Ratings/T_a = 25°C, V_{DD} = 0V				Unit
Maximum Supply Voltage	V_{SS1}	V_{SS1} pin	−3.0 to +0.3	V
	V_{SS2}	V_{SS2} pin	−4.0 to +0.3	V
Input Voltage	V_{IN}		V_{SS1}−0.3 to +0.3	V
Output Voltage	V_{OUT}	CNT OUT, SLP OUT, output off	V_{DD}−15 to +0.3	V
Operating Temperature	T_{opg}		−20 to +70	°C
Storage Temperature	T_{stg}		−30 to +125	°C

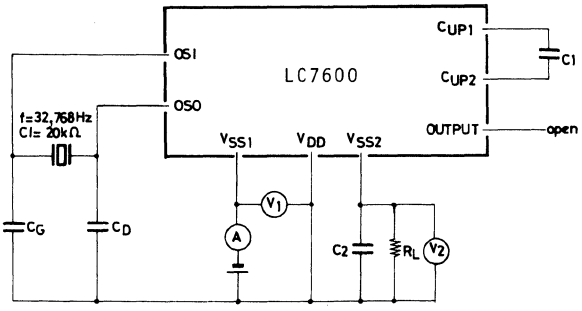
Allowable Operating Ranges/T_a = 25°C, V_{DD} = 0V			min	typ	max	unit
Supply Voltage	V_{SS1}		−2.0		−1.25	V
	V_{SS2}		−3.5		−2.2	V
"H" Level Input Voltage	V_{IH}		−0.2		0	V
"L" Level Input Voltage	V_{IL}		V_{SS1}		V_{SS1}+0.2	V
Operating Frequency of Tape Pulse	f_1	CONT1, CONT2	DC		1	kHz

Electrical Characteristics/T_a = 25°C, V_{DD} = 0V, V_{SS1} = −1.55V, V_{SS2} = −3.0V			min	typ	max	unit
"H" Level Input Current	I_{IH} (1)	CNT, V_{IN} = V_{DD}			0.1	μA
	I_{IH} (2)	FH, FM, FS, Reset 2, Test, V_{IN} = V_{DD}		15		μA
	I_{IH} (3)	Other than above, V_{IN} = V_{DD}		1.5		μA
"L" Level Input Current	I_{IL} (1)	CNT, V_{IN} = V_{SS1}	−0.1			μA
	I_{IL} (2)	FH, FM, FS, Reset 2, Test, V_{IN} = V_{SS1}	−0.1			μA
	I_{IL} (3)	Other than above, V_{IN} = V_{SS1}	−0.1			μA
"H" Level Output Voltage	V_{OH} (1)	Segment output, I_{OH} = −5 μA, V_{SS1} = −1.25V, V_{SS2} = −2.2V	V_{DD}−0.15			V
	V_{OH} (2)	COM, COLDC, I_{OH} = −100μA, V_{SS1} = −1.25, V_{SS2} = −2.2V	V_{DD}−0.15			V
	V_{OH} (3)	BUZOUT, I_{OH} = −250 μA, V_{SS1} = −1.25V, V_{SS2} = −2.2V	V_{DD}−0.5			V
	V_{OH} (4)	CNTOUT, SLPOUT, I_{OH} = −100 μA, V_{SS1} = −1.25V, V_{SS2} = −2.2V	V_{DD}−0.5			V
"L" Level Output Voltage	V_{OL} (1)	Segment output, I_{OL} = 5 μA V_{SS1} = −1.25V, V_{SS2} = −2.2V		V_{SS2}+0.15		V
	V_{OL} (2)	COM, COLDC, I_{OL} = 100 μA, V_{SS1} = −1.25V, V_{SS2} = −2.2V		V_{SS2}+0.15		V
	V_{OL} (3)	BUZOUT, I_{OL} = 250 μA, V_{SS1} = −1.25V, V_{SS2} = −2.2V		V_{SS1}+0.5		V

			min	typ	max	unit
Output Off Leak Current	I_{off}	CNTOUT, SLPOUT, V_{OL} = −5.5V			3	μA
Output Supply Voltage	V_{SS2} (OUT)	V_{SS2} output voltage, V_{SS1} = −1.25V to −2.0V	−4.0		−2.3	V
Current Dissipation	I_{DD}	X'tal: F = 32.768kHz, C_I = 20kΩ C_D = 20pF, C_G = 15pF, C1 = C2 = 0.2 μF, V_{SS1} = −1.55V		2.0	3.5	μA
Oscillation Start Voltage	V_{start}	X'tal: f = 32.768kHz, CI = 20kΩ, C_D = 20pF, C_G = 15pF, t_{start} = 10 sec	−1.4			V
Oscillation Stop Voltage	V_{stop}	X'tal: f = 32.768kHz, CI = 20kΩ, C_D = 20pF, C_G = 15pF	−1.25			V

Note) When the lamp is lighted, rush current causes the supply voltage to be outside the allowable operating range, leading to malfunction.
Therefore, it is recommended to separate the power supply for lamp from the power supply for LSI.

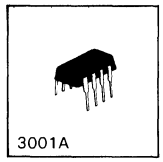
Test Circuit



f=32.768kHz
CI=20kΩ

Item	C_D	C_G	C1	C2	R_L	Measuring Instrument
Output Supply Voltage	20 pF	15 pF	0.2 μF	0.2 μF	3 MΩ	V_2
Current Dissipation	20 pF	15 pF	0.2 μF	0.2 μF	∞	A
OSC Start Voltage	20 pF	15 pF	–	–	–	V_1
OSC Stop voltage	20 pF	15 pF	–	–	–	V_1

LC7650, 7651



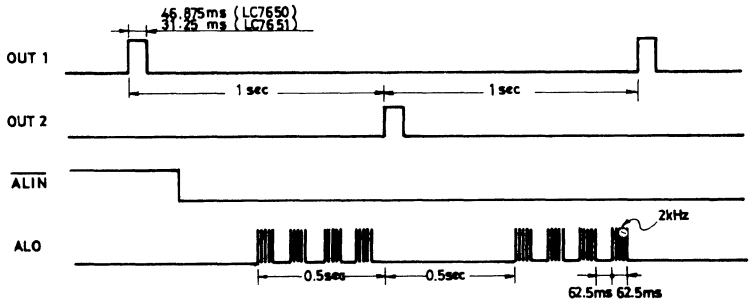
C MOS IC

Analog Clock Step Motor Driver

Ⓔ 950B

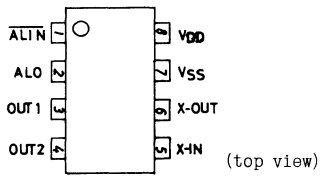
Features

1. Oscillation frequency: 4194304Hz
2. Alarm output function
   (1) Output waveform



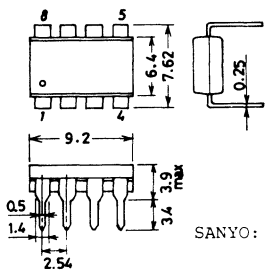
   (2) Alarm control
   By applying V_{SS} to $\overline{ALIN}$, alarm signal is outputted; and by applying V_{DD} to $\overline{ALIN}$ or making it open, alarm signal is turned off.
   (3) Test function
   By applying approximately $1/2V_{DD}$ to $\overline{ALIN}$ when V_{DD}=1.5V, 2048Hz signal appears continuously at ALO.
3. OUT1/OUT2 output waveform
   (1) Alternate outputs with a cycle of 2 seconds
   (2) Pulse width: 46.875ms (LC7650)
   31.25ms (LC7651)
4. Supply voltage 1.5V typ.
5. Current dissipation 25uA/1.5V typ.

Pin Assignment



(top view)

Case Outline 3001A-D8IC
(unit:mm)



SANYO: DIP8

Absolute Maximum Ratings at Ta=-30°C to +80°C, V_{SS}=0V

			unit
Maximum Supply Voltage	$V_{DD}max$	-0.3 to 4.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{DD}+0.3	V
Operating Temperature	Topg	-30 to +80	°C
Storage Temperature	Tstg	-55 to +125	°C

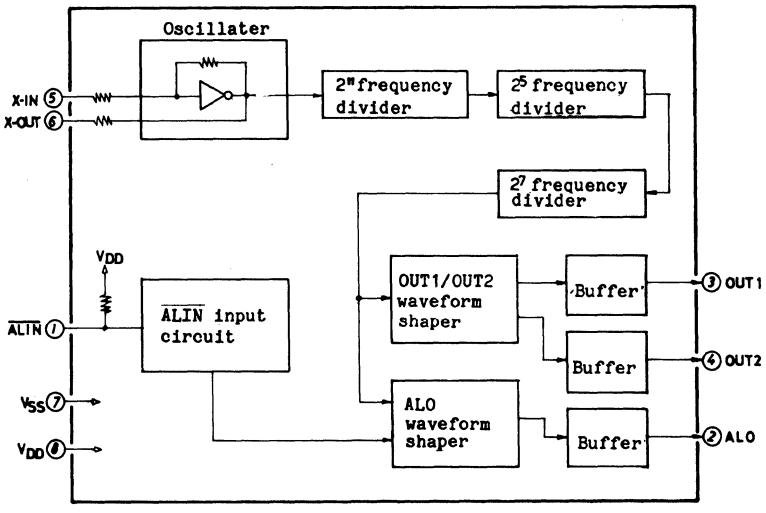
Allowable Operating Ranges at Ta=25°C, V_{DD}=1.1 to 1.9V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		1.1	1.5	1.9	V
"H" Level Input Voltage	V_{IH}	$\overline{ALIN}$ pin	0.9V_{DD}		V_{DD}	V
"L" Level Input Voltage	V_{IL}	$\overline{ALIN}$ pin	0		0.1V_{DD}	V
Operating Frequency	f_{opg}	X-IN/X-OUT pin, Xtal mounted C_G=C_D=15pF, CI=40ohm	4.1		4.3	MHz

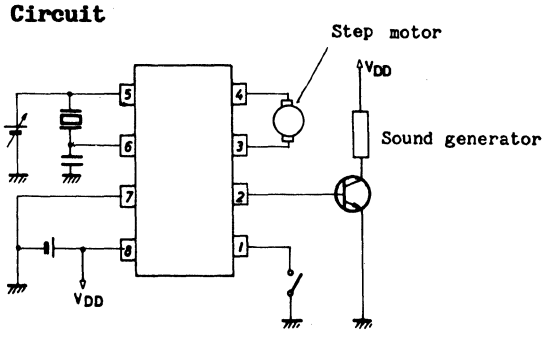
Electrical Characteristics at Ta=25°C, V_{SS}=0V, f_{osc}=4.194304MHz, C_G=C_D=15pF, CI=40ohm, dummy load R_L=300ohm

			min	typ	max	unit
Current Dissipation	I_{DD}	V_{DD}=1.5V, no load		25	35	uA
Output Saturation Voltage	R_{ON}	OUT_1/OUT_2 pin (R_P+R_N), V_{DD}=1.2V		75	100	ohm
"H" Level Output Voltage	V_{OH}	ALO pin, V_{DD}=1.2V, I_{OH}=-1mA	V_{DD}-0.3V			V
"L" Level Output Voltage	V_{OL}	ALO pin, V_{DD}=1.2V, I_{OL}=0.1mA			0.4	V
Oscillation Start Voltage	V_{start}	Within 1 second			1.1	V
Oscillation Stability	$\Delta f/f_o$	V_{DD}=1.2to1.7V, fo:at V_{DD}=1.5V	-1		1	ppm
Input Pull-up Resistance	R_{IN}	$\overline{ALIN}$ pin, V_{DD}=1.1 to 1.9V	5		500	kohm

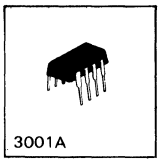
Equivalent Circuit Block Diagram



Sample Application Circuit



LC7652, 7653



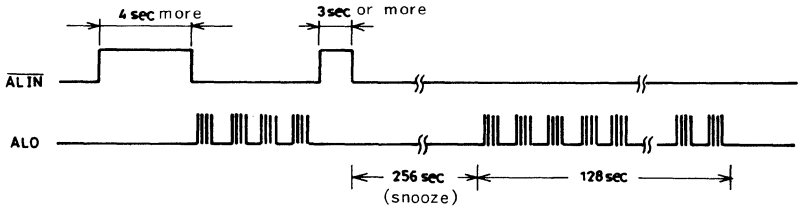
C MOS IC

Analog Clock Step Motor Driver

Ⓔ 951B

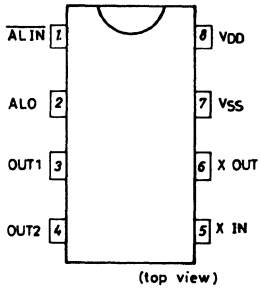
Features

1. Oscillation frequency: 4194304Hz
2. Alarm with snooze and 3-step sound pressure change
   (1) Snooze time: 256 seconds
   (2) Sound pressure change time: 1 to 8 seconds ------- Weak
   9 to 16 seconds ------ Medium
   17 to 128 seconds ---- Strong
   (3) Alarm output time: 128 seconds after applying V_{SS} to $\overline{ALIN}$
   (4) Alarm output signal and control

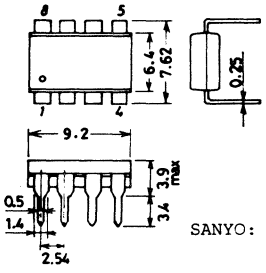


(Note) By applying V_{SS} to $\overline{ALIN}$ after applying V_{DD} to $\overline{ALIN}$ for 4 seconds or more, alarm signal is outputted.
By applying V_{SS} to $\overline{ALIN}$ after applying V_{DD} to $\overline{ALIN}$ for 3 seconds or less, snooze state occurs.

Pin Assignment

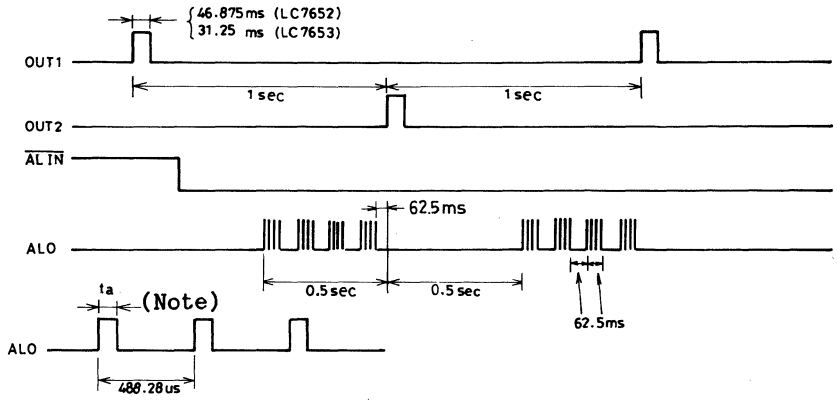


Case Outline 3001A-D8IC
(unit:mm)



SANYO: DIP8

(5) Alarm output waveform



(Note) ta: Changes as follows after alarm start.

Time after alarm start	1~8s	9~16s	17~128s
ta (μs)	31	61	244
duty (%)	6.25	12.5	50

(6) Test function
By applying approximately $1/2V_{DD}$ to $\overline{ALIN}$ when V_{DD}=1.5V, 2048Hz signal appears continuously at ALO.

3. OUT1/OUT2 output waveform
(1) Alternate outputs with a cycle of 2 seconds
(2) Pulse width: 46.875ms (LC7652)
31.25ms (LC7653)

Absolute Maximum Ratings at Ta=-30°C to +80°C, V_{SS}=0V

			unit
Maximum Supply Voltage	$V_{DD}max$	-0.3 to 4.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{DD}+0.3	V
Operating Temperature	Topg	-30 to +80	°C
Storage Temperature	Tstg	-55 to +125	°C

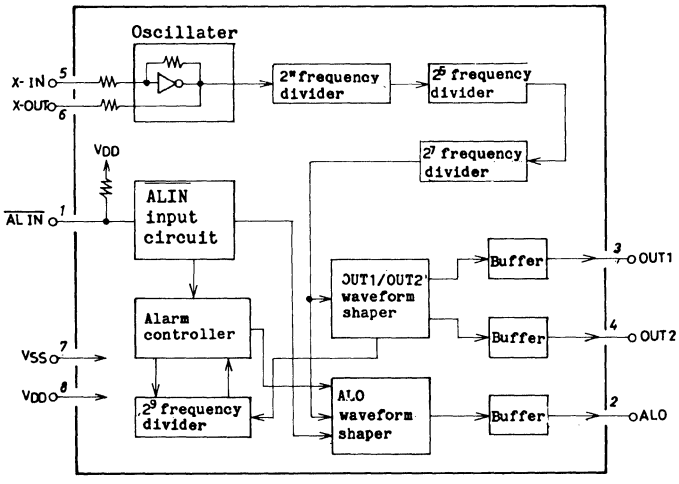
Allowable Operating Ranges at Ta=25°C, V_{DD}=1.1 to 1.9V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	$V_{DD}max$		1.1	1.5	1.9	V
"H" Level Input Voltage	V_{IH}	$\overline{ALIN}$ pin	$1.9V_{DD}$		V_{DD}	V
"L" Level Input Voltage	V_{IL}	$\overline{ALIN}$ pin	0		$0.1V_{DD}$	V
Operating Frequency	f_{opg}	X-IN/X-OUT pin, Xtal mounted C_G=C_D=15pF, CI=40ohm	4.1		4.3	MHz

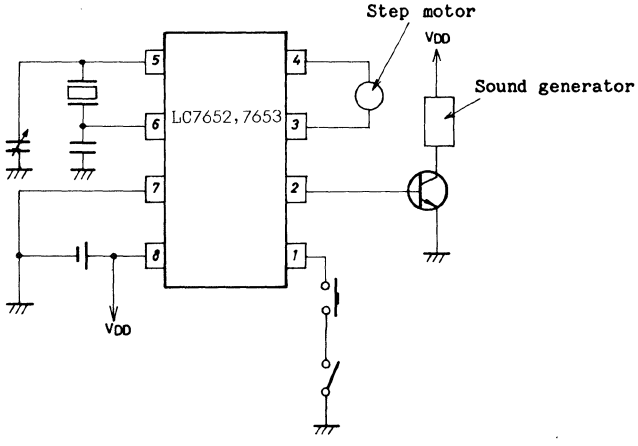
Electrical Characteristics at Ta=25°C, V_{SS}=0V, f_{osc}=4.194304MHz, C_G=C_D=15pF, CI=40ohm, dummy load R_L=300ohm

			min	typ	max	unit
Current Dissipation	I_{DD}	V_{DD}=1.5V, no load		25	40	uA
Output Saturation Voltage	R_{ON}	V_{DD}=1.2V, OUT1/OUT2 pin (R_P+R_N)		75	100	ohm
"H" Level Output Voltage	V_{OH}	V_{DD}=1.2V, I_{OH}=-1mA, ALO pin	V_{DD}-0.3			V
"L" Level Output Voltage	V_{OL}	V_{DD}=1.2V, I_{OL}=0.1mA, ALO pin			0.4	V
Oscillation Start Voltage	V_{start}	Within 1 second			1.1	V
Oscillation Stability	$\triangle f/f_o$	V_{DD}=1.2 to 1.7V, fo:at V_{DD}=1.5V	-1		1	ppm
Input Pull-up Resistance	R_{IN}	V_{DD}=1.1 to 1.9V, $\overline{ALIN}$ pin	5		500	kohm

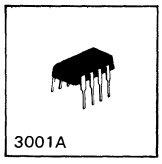
Equivalent Circuit Block Diagram



Sample Application Circuit



LC7660



C MOS IC

Analog Clock Step Motor Driver

Ⓔ 1255A

1. General Description

The LC7660 is a C MOS IC for use in analog clock step motor driver applications. With the reference frequency being 32.768kHz, it performs step motor drive output, alarm output, snooze functions and is capable of operating from a single low-voltage (1.5 V typ.) supply.

2. Function

(1) Crystal oscillator
- Oscillation freuqency: 32.768kHz

(2) OUT1, OUT2 outputs
- Alternate OUT1, OUT2 outputs with a cycle of 2 seconds
- Pulse width: 31.25ms

(3) Alarm output at ALO pin
- Fundamental frequency: 2048Hz
- Tone: Alarm tone (sound pressure) is variable in 4 steps. (Refer to 3. Alarm Waveform.)
- Capable of driving NPN transistor

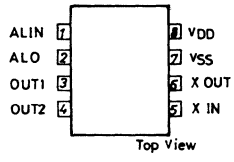
(4) Alarm control input
- Alarm input pin: ALIN pin (with pull-down resistor built in)
- By applying V_{DD} to ALIN pin after leaving ALIN pin open or at V_{SS} for 3 seconds or more, alarm signal is outputted.
- Alarm output time: 64 seconds

(5) Snooze function
- By applying V_{DD} to ALIN pin within 2 seconds after setting ALIN pin open or to V_{SS}, snooze mode is entered.
- Snooze time: 256 seconds

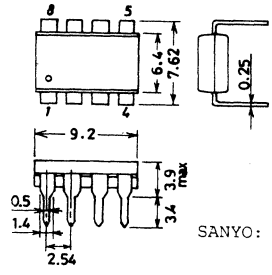
(6) Test function

By applying approximately $1/2V_{DD}$ to ALIN pin when V_{DD}=1.5V, 2048Hz singal is outputted continuously at ALO pin.

Pin Assignment

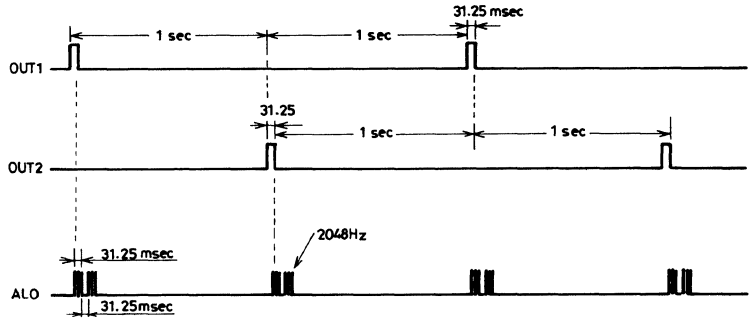


Case Outline 3001A-D8IC
(unit:mm)

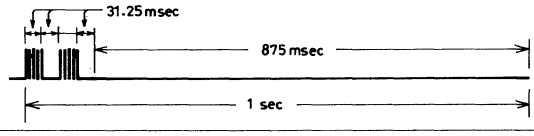
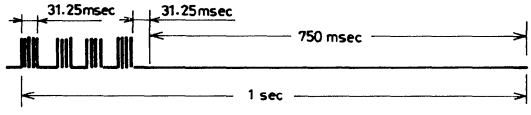
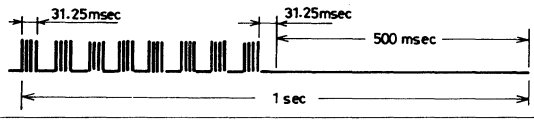
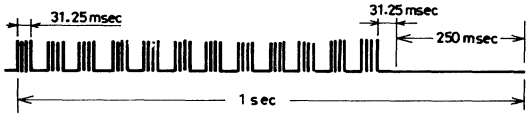


SANYO: DIP8

3. Alarm Waveform



Note: The following change in alarm waveform (ALO output waveform) occurs with the lapse of time after turning alarm ON.

Time (s) after turning alarm ON	Alarm waveform	Duty (%) of fundamental wave
0～8		6.25
9～16		12.5
17～24		25
25～64※		50

Note: Alarm stops automatically when 64 seconds have elapsed.

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

			unit
Maximum Supply Voltage	V_{DD} max	−0.3～+3.0	V
Input Voltage	V_{IN}	−0.3～V_{DD}+0.3	V
Operating Temperature	T_{opg}	−20～+80	℃
Storage Temperature	T_{stg}	−55～+125	℃

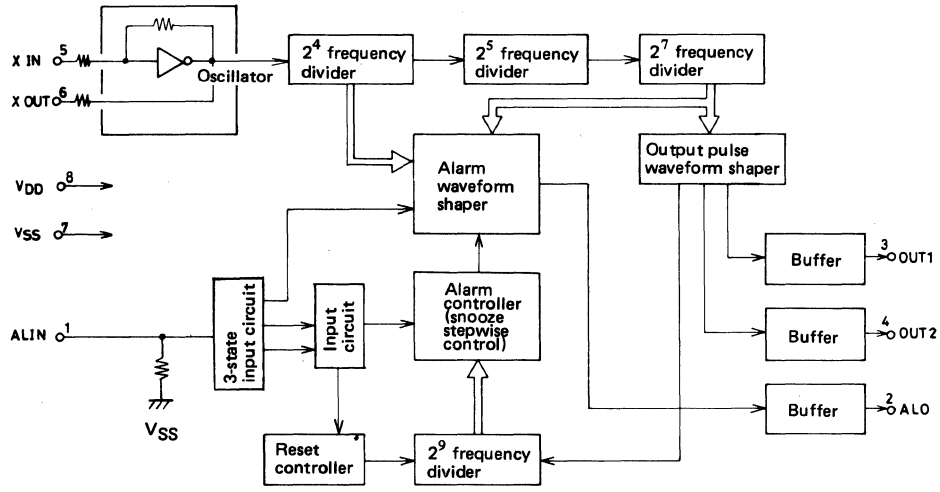
Allowable Operating Ranges/T_a=25°C, V_{DD}=1.1 to 1.8V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=−10～+50℃	1.1	1.5	1.8	V
Input "H" Level Voltage	V_{IH}	ALIN pin	0.9V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}	ALIN pin	0		0.1V_{DD}	V
Input "M" Level Voltage	V_{IM}	ALIN pin ,V_{DD}=1.5V	½V_{DD} −0.5%	½V_{DD}	½V_{DD} +0.5%	V
Operating Frequency	f_{opg}	X−IN/X−OUT pin, X'tal mounted C_G=C_D=15pF, C.I=25kΩ	32		33	kHz

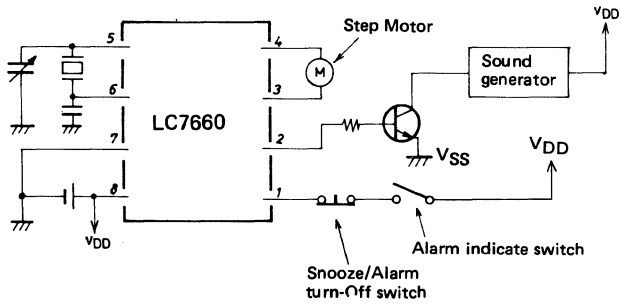
Electrical Characteristics/T_a=25°C, V_{SS}=0V, f_{OSC}=32.768kHz, C_G=15pF, C_D=15pF, C.I.=25kΩ, dummy load RL=180Ω

			min	typ	max	unit
Current Dissipation	I_{DD}	V_{DD}=1.5V, no load		3	5	μA
Output Saturation Resistance	R_{ON}	V_{DD}=1.2V, OUT1/OUT2 pin (R_P+R_N)		75	100	Ω
Output "H" Level Voltage	V_{OH}	V_{DD}=1.2V, I_{OH}=−0.5mA, ALO pin	V_{DD}−0.3			V
Output "L" Level Voltage	V_{OL}	V_{DD}=1.2V, I_{OL}=0.1mA, ALO pin			0.4	V
Oscillation Start Time	T_{start}	V_{DD}=1.2V			5	s
Oscillation Stability	$\Delta f/f_0$	$\frac{(f-f1.5)}{f1.5}$ f:at V_{DD}=1.2V or 1.7V	−3.5		3.5	ppm
Input Pull-down Resistance	R_{IN}	V_{DD}=1.1~1.8V, ALIN pin	5			kΩ

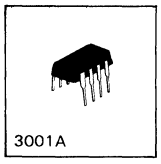
Equivalent Circuit Block Diagram



■ **Sample Application Circuit**



LC7662



C MOS IC

Analog Clock Step Motor Driver

Ⓔ 1262A

1. General Description

The LC7662 is a C MOS IC for use in analog clock step motor driver applications. With the reference frequency being 32.768kHz, it performs step motor drive output, alarm output, snooze functions and is capable of operating from a single low-voltage (1.5 V typ.) supply.

2. Function

(1) Crystal oscillator
- Oscillation freuqency: 32.768kHz

(2) OUT1, OUT2 outputs
- Alternate OUT1, OUT2 outputs with a cycle of 2 seconds
- Pulse width: 31.25ms

(3) Alarm output at ALO pin
- Fundamental frequency: 2048Hz
- Tone: Alarm tone (sound pressure) is variable in 3 steps. (Refer to 3. Alarm Waveform.)
- Capable of driving NPN transistor

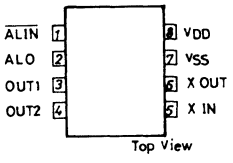
(4) Alarm control input
- Alarm input pin: $\overline{\text{ALIN}}$ pin (with pull-up resistor built in)
- By applying V_{SS} to $\overline{\text{ALIN}}$ pin after leaving $\overline{\text{ALIN}}$ pin open or at V_{DD} for 3 seconds or more, alarm signal is outputted.
- Alarm output time: 128 seconds

(5) Snooze function
- By applying V_{SS} to $\overline{\text{ALIN}}$ pin within 2 seconds after setting $\overline{\text{ALIN}}$ pin open or to V_{DD}, snooze mode is entered.
- Snooze time: 256 seconds

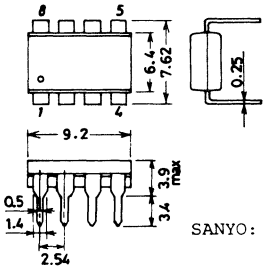
(6) Test function

By applying approximately $1/2V_{DD}$ to $\overline{\text{ALIN}}$ pin when V_{DD}=1.5V, 2048Hz singal is outputted continuously at ALO pin.

Pin Assignment

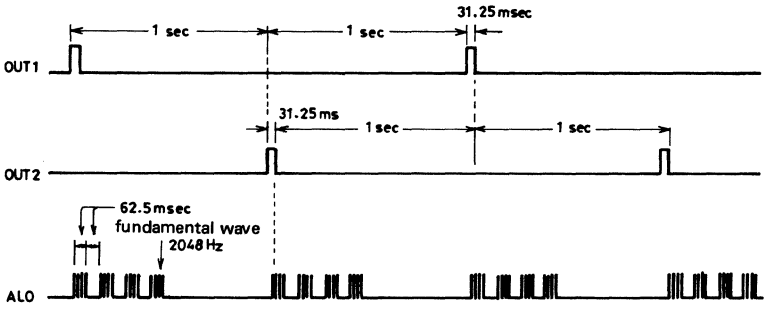


Case Outline 3001A-D8IC
(unit:mm)

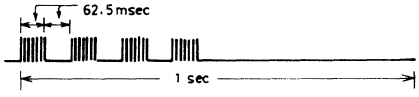
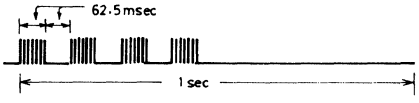
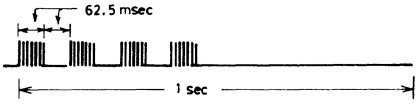


SANYO: DIP8

3. Alarm Waveform



Note 1. The following change in alarm waveform (ALO output waveform) occurs with the lapse of time after turning alarm ON.

Time (s) after turning alarm ON	Alarm waveform	Duty (%) of fundamental wave
0～8		12.5
9～16		25
17～128		50

Note 2. Only duty of fundamental wave changes with the lapse of time after turning alarm ON.

Note 3. Alarm stops automatically when 128 seconds have elapsed.

Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V

			unit
Maximum Supply Voltage	V_{DD} max	−0.3～+3.0	V
Input Voltage	V_{IN}	−0.3～V_{DD}+0.3	V
Operating Temperature	T_{opg}	−20～+80	°C
Storage Temperature	T_{stg}	−55～+125	°C

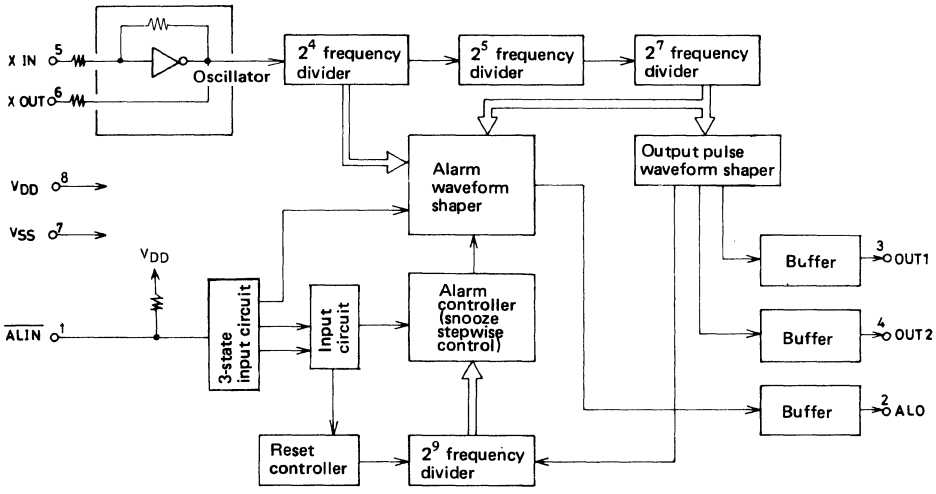
Allowable Operating Ranges/T_a=25°C, V_{DD}=1.1 to 1.8V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=−10～+50°C	1.1	1.5	1.8	V
Input "H" Level Voltage	V_{IH}	$\overline{ALIN}$ pin	0.9V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}	$\overline{ALIN}$ pin	0		0.1V_{DD}	V
Input "M" Level Voltage	V_{IM}	$\overline{ALIN}$ pin, V_{DD}=1.5V	½V_{DD} −0.5%	½V_{DD}	½V_{DD} +0.5%	V
Operating Frequency	f_{opg}	X−IN/X−OUT pin, X'tal mounted C_G=C_D=15pF, C.I=25kΩ	32		33	kHz

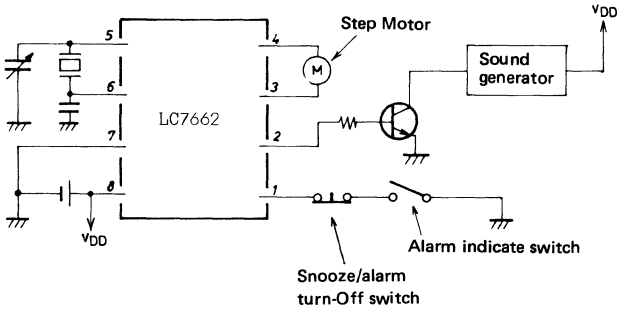
Electrical Characteristics/T_a=25°C, V_{SS}=0V, f_{OSC}=32.768kHz, C_G=15pF, C_D=15pF, C.I.=25kΩ, dummy load RL=180Ω

			min	typ	max	unit
Current Dissipation	I_{DD}	V_{DD}=1.5V, no load		3	5	μA
Output Saturation Resistance	R_{ON}	V_{DD}=1.2V, OUT1/OUT2 pin (R_P+R_N)		75	100	Ω
Output "H" Level Voltage	V_{OH}	V_{DD}=1.2V, I_{OH}=−0.5mA, ALO pin	V_{DD}−0.3			V
Output "L" Level Voltage	V_{OL}	V_{DD}=1.2V, I_{OL}=0.1mA, ALO pin			0.4	V
Oscillation Start Time	T_{start}	V_{DD}=1.2V			5	s
Oscillation Stability	$\Delta f/f_0$	$\frac{(f-f1.5)}{f1.5}$ f:at V_{DD}=1.2V or 1.7V	−3.5		3.5	ppm
Input Pull-up Resistance	R_{IN}	V_{DD}=1.1~1.8V, $\overline{ALIN}$ pin	5			kΩ

Equivalent Circuit Block Diagram



■ **Sample Application Circuit**



LC7665

3001A

C MOS IC

Analog Clock Step Motor Driver

Ⓔ 1263A

1. General Description

The LC7665 is a C MOS IC for use in analog clock step motor driver applications. With the reference frequency being 32.768kHz, it performs step motor drive output, alarm output functions and is capable of operating from a single low-voltage (1.5V typ.) supply.

2. Functions

(1) Crystal oscillator
- Oscillation frequency: 32.768kHz

(2) OUT1, OUT2 outputs
- Alternate OUT1, OUT2 outputs with a cycle of 2 seconds
- Pulse width: 31.25ms

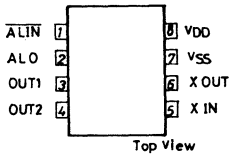
(3) Alarm output at ALO pin
- Fundamental frequency: 2048Hz
- Tone: (Refer to 3. Alarm Waveform.)
- Capable of driving NPN transistor

(4) Alarm control input
- Alarm input pin: $\overline{\text{ALIN}}$ pin (with pull-up resistor built in)
- By applying V_{SS} to $\overline{\text{ALIN}}$ pin, alarm signal is outputted.

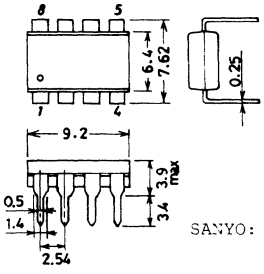
(5) Test function

By applying approximately $1/2V_{DD}$ to $\overline{\text{ALIN}}$ pin when V_{DD}=1.5V, 2048Hz signal is outputted continuously at ALO pin.

Pin Assignment

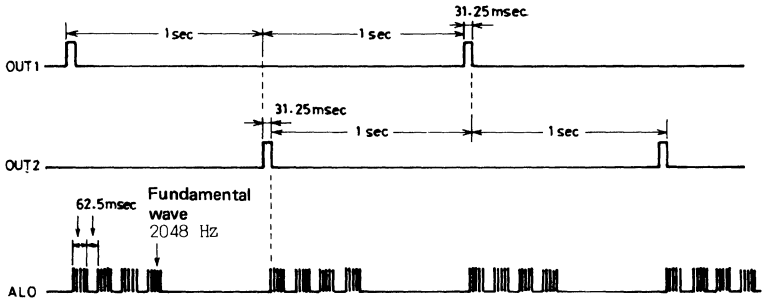


Case Outline 3001A-D8IC
(unit:mm)



SANYO: DIP8

3. Alarm Waveform



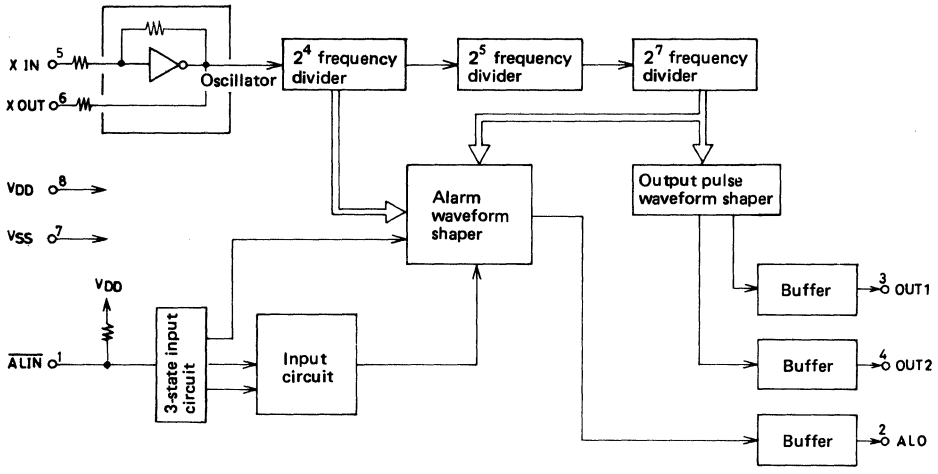
Absolute Maximum Ratings/T_a=25°C, V_{SS}=0V			unit
Maximum Supply Voltage	V_{DD} max	−0.3～+3.0	V
Input Voltage	V_{IN}	−0.3～V_{DD}+0.3	V
Operating Temperature	T_{opg}	−20～+80	°C
Storage Temperature	T_{stg}	−55～+125	°C

Allowable Operating Ranges/T_a=25°C, V_{DD}=1.1 to 1.8V, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=−10～+50°C	1.1	1.5	1.8	V
Input "H" Level Voltage	V_{IH}	$\overline{ALIN}$ pin	0.9V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}	$\overline{ALIN}$ pin	0		0.1V_{DD}	V
Input "M" Level Voltage	V_{IM}	$\overline{ALIN}$ pin, V_{DD}=1.5V	½V_{DD} −0.5%	½V_{DD}	½V_{DD} +0.5%	V
Operating Frequency	f_{opg}	X-IN/X-OUT pin, X'tal mounted C_G=C_D=15pF, C.I=25kΩ	32		33	kHz

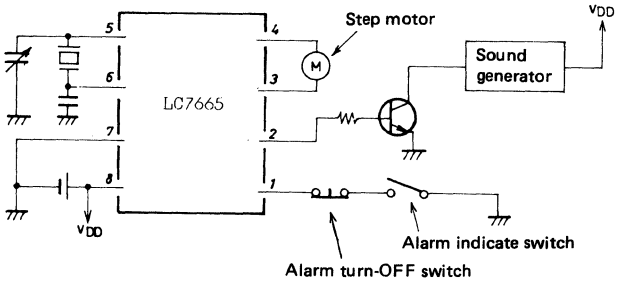
Electrical Characteristics/T_a=25°C, V_{SS}=0V, f_{OSC}=32.768kHz, C_G=15pF, C_D=15pF, C.I=25kΩ, dummy load RL=180Ω

			min	typ	max	unit
Current Dissipation	I_{DD}	V_{DD}=1.5V, no load		3	5	μA
Output Saturation Resistance	R_{ON}	V_{DD}=1.2V, OUT1/OUT2 pin (R_P+R_N)		75	100	Ω
Output "H" Level Voltage	V_{OH}	V_{DD}=1.2V, I_{OH}=−0.5mA, ALO pin	V_{DD}−0.3			V
Output "L" Level Voltage	V_{OL}	V_{DD}=1.2V, I_{OL}=0.1mA, ALO pin			0.4	V
Oscillation Start Time	T_{start}	V_{DD}=1.2V			5	s
Oscillation Stability	$\Delta f/f_o$	$\frac{(f-f1.5)}{f1.5}$ f: at V_{DD}=1.2V or 1.7V	−3.5		3.5	ppm
Input Pull-up Resistance	R_{IN}	V_{DD}=1.1～1.8V, $\overline{ALIN}$ pin	5			kΩ

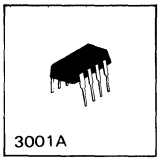
Equivalent Circuit Block Diagram



■ **Sample Application Circuit**



LC7667



C MOS IC

Analog Clock Step Motor Driver

Ⓔ 1538

General Description

The LC7667 is a C MOS IC for use in analog clock step motor driver applications. With the reference frequency being 32.768kHz, it performs step motor drive output, alarm output functions and is capable of operating from a single low-votlage(1.5V typ.) supply.

Functions

(1) Crystal oscillator
- . Oscillation frequency: 32.768kHz

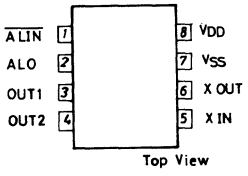
(2) OUT1, OUT2 outputs
- . Alternate OUT1, OUT2 outputs with a cycle of 2 seconds
- . Pulse width: 46.875 ms

(3) Alarm output at ALO pin
- . Fundamental frequency: 2048Hz
- . Tone: (Refer to 3. Alarm Waveform.)
- . Capable of driving NPN transistor

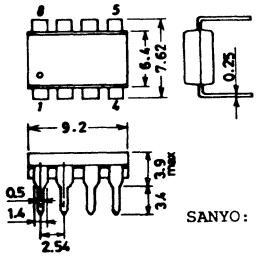
(4) Alarm control input
- . Alarm input pin: $\overline{ALIN}$ pin (wisth pull-up resistor built in)
- . By applying V_{SS} to $\overline{ALIN}$ pin, alarm signal is outputted.

(5) Test function
By applying approximately $1/2V_{DD}$ to $\overline{ALIN}$ pin when V_{DD}=1.5V, 2048Hz signal is outputted continuously at ALO pin.

Pin Assignment

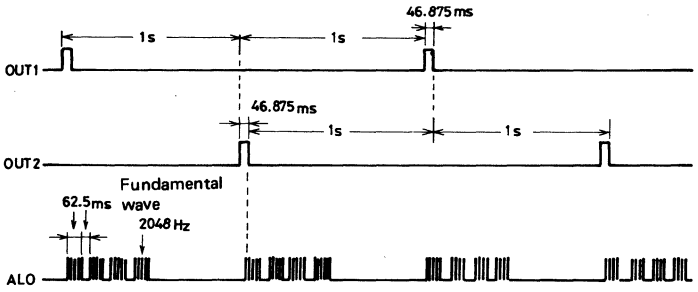


Case Outline 3001A-D8IC
(unit:mm)



SANYO: DIP8

Alarm Waveform



Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

			unit
Maximum Supply Voltage	V_{DD}max	-0.3 to +3.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operatiang Temperature	Topg	-20 to +80	°C
Storage Temperature	Tstg	-55 to +125	°C

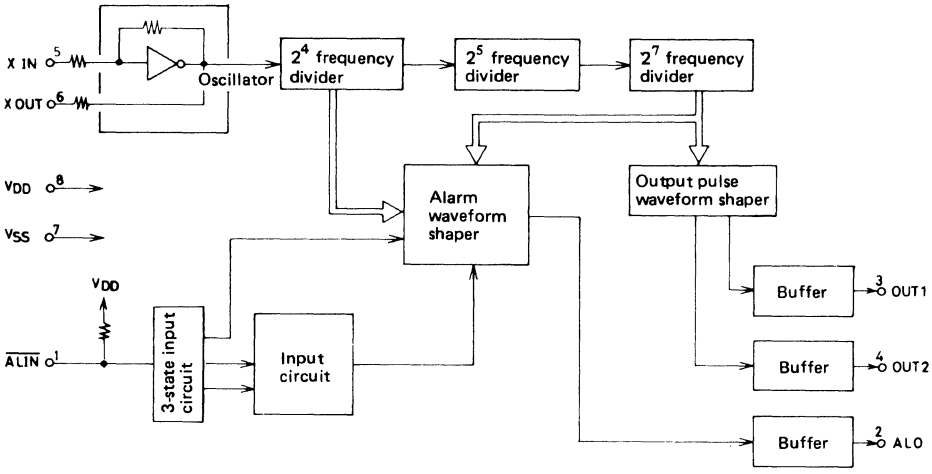
Allowable Operating Ranges at Ta=25°C, V_{DD}=1.1 to 1.8V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	Ta=-10 to +50°C	1.1	1.5	1.8	V
Input "H" Level Voltage	V_{IH}	$\overline{ALIN}$ pin	0.9V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}	$\overline{ALIN}$ pin	0		0.1V_{DD}	V
Input "M" Level Voltage	V_{IM}	$\overline{ALIN}$ pin, V_{DD}=1.5V	1/2V_{DD} -0.5%	1/2VDD	1/2V_{DD} +0.5%	V
Operating Frequency	fopg	X-IN/X-OUT pin, X'tal mounted C_G=C_D=15pF, C.I=25kohm	32		33kHz	

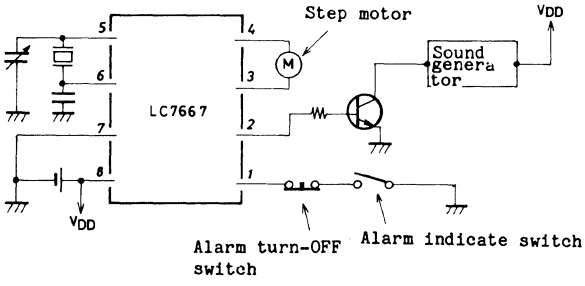
ElectricalCharacteristics at Ta=25°C, V_{SS}=0V, fosc=32.768kHz, C_G=15pF, C.I=25kohm, dummy load R_L=180ohm

			min	typ	max	unit
Current Dissipation	I_{DD}	V_{DD}=1.5V, no load		3	5	uA
Output Saturation Resistance	R_{ON}	V_{DD}=1.2V, OUT1/OUT2 pin (R_P+R_N)		75	100	ohm
Output "H" Level Voltage	V_{OH}	V_{DD}=1.2V, I_{OH}=-0.5mA, ALO pin	V_{DD}-0.3			V
Output "L" Level Voltage	V_{OL}	V_{DD}=1.2V, I_{OL}=0.1mA, ALO pin			0.4	V
Oscillation Start Time	Tstart	V_{DD}=1.2V			5	s
Oscillation Stability	$\Delta f/fo$	$\frac{(f-f1.5)}{f1.5}$ f:at V_{DD}=1.2V or 1.7V	-3.5		3.5	ppm
Input Pull-up Resistance	R_{IN}	V_{DD}=1.1 to 1.8V, $\overline{ALIN}$ pin	5			kohm

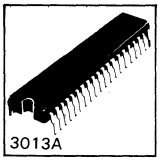
Equivalent Circuit Block Diagram



Sample Application Circuit



LM8361



P MOS LSI

Alarm Use of Digital Clock

Ⓔ 736B

Use

- Alarm clock
- Clock radio
- Timer for home appliances
- Display of time elapsed

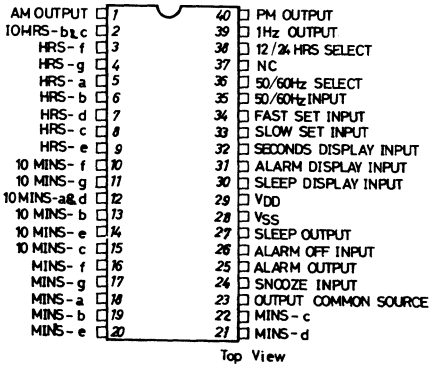
Functions

- Real time display
- Alarm with snooze function
- Sleep timer (59 minutes max.)

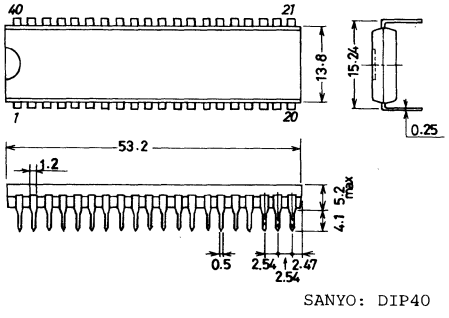
Features

1. Single-chip P-Channel ED MOS LSI
2. Possible to direct drive an LED (5mA or more, red LED)
3. Possible to direct drive a fluorescent display tube (light-up voltage 16V or less)
4. Wide operating voltage range (-8V to -16V)
5. 50Hz or 60Hz is usable as reference frequency.
6. Two selections of display mode (AM/PM 12-hour display mode or 24-hour display mode)
7. 24-hour alarm function
8. Repeatedly usable snooze function
9. Presettable 59-minute down counter (sleep timer)
10. SNOOZE pin can be used to set the sleep timer with one touch.
11. Power failure indicating function (all digits flahing: 12H display mode→ AM or OUTPUT of LSI, 24H display mode→AM, PM or b&c OUTPUT of LSI)
12. Clock input noise eliminator
13. Pin compatible with the NS MM5387, AMI S1998 A/B/C

Pin Assignment



Case Outline 3013A-D40IC (unit:mm)



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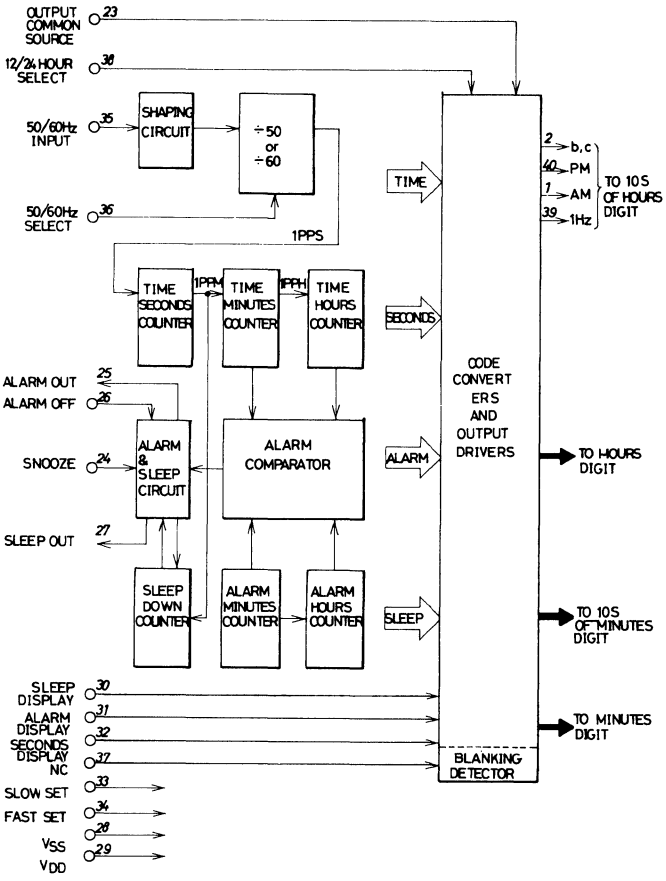
* NC pin must not be used for external connection such as a relay point.

Equivalent Circuit Block Diagram



Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DDmax}		-18 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max	Ta=70°C	0.9	W
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V		min	typ	max	unit
Supply V ltage	V_{DD}	-16	-12	-8	V
Input "H"-Level Voltage	V_{IH}	-1.0		0	V
Input "L"-Level Voltage	V_{IL}	V_{DD}		V_{DD}+2	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-12V±2V			min	typ	max	unit
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	V_{OH}=V_{SS}-2V	0.5			mA
b&c, a&d	$I_{OH}(2)$	V_{OH}=V_{SS}-2.5V	10			mA
1Hz	$I_{OH}(3)$	V_{OH}=V_{SS}-2.5V	13			mA
Other than above	$I_{OH}(4)$	V_{OH}=V_{SS}-2.5V	5		*	mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	V_{OL}=V_{DD}			5	uA
Other than above	$I_{OL}(2)$	V_{OL}=V_{DD}+1.8V			50	uA
Current Dissipation	I_{DD}	V_{DD}=-12V		3		mA

*: 11mA max. is allowed in the range where the power dissipation is 900mW and 1.2W at Ta=70°C and 25°C respectively.

1. Display
   1-1. Real time, alarm time, sleep time are displayed in the following display font by means of 4-digit 7-segment LED or fluorescent display tube.

Display font 

   1-2. Lighting system: Static lighting
   1-3. Display range
   - Time and alarm time display mode (12-hour display)
     AM1:00 to PM12:59 (highest-order digit: 0 blanking)
   - Time and alarm display mode (24-hour display mode)
   - 00,00 to 23:59 (no 0 blanking)
   - Seconds display mode
     0:00 to 9:59 (highest-order digit: blanking)
   - Sleep time display mode
     00 to 59 (highest-order and 2nd highest-order digits: blanking)

2. Input signal
   2-1. Switch signal
   - Logic "L": V_{DD}(or pin open)
   - Logic "H": V_{SS}
   2-2. 50/60Hz input signal
   - Sine wave, square wave, triangular wave, etc. of V_{DD}-V_{SS}(p-p)
   - Impedance: 1Mohm or greater

3. Output configuration
   3-1. Segment output: P-channel open drain type
   3-2. Drive output (ALARM OUT, SLEEP OUT): P-channel open drain type

4. Operation description
   4-1. 50/60Hz input
   This signal is used to drive the time counter. Commercial frequency 50/60Hz is put through the Schmitt circuit to be free from noise. A resistor (100 to 100Kohm) must be connected in series with this input pin to avoid being damaged by high-voltage noise included in the commercial power supply.
   4-2. 50/60Hz select input
   The program counter contains a 50Hz/60Hz select circuit to provide a standard frequency of 1 pulse per second. When this pin is set at "L" or open, 60Hz use is available; when at "H", 50Hz use is available.
   4-3. Display select mode

A) Alarm display input----	Setting this pin to "H" causes alarm time to be displayed.
B) Seconds display input--	Setting this pin to "H" causes the first digit of seconds and minutes to be displayed.
C) Sleep display input----	Setting this pin to "H" causes sleep time to be displayed.
D) Real time display------	When none of input in A), B), and C) are selected, or all of of them are at "L", real time is displayed.
E) Priority order of------ display	Shown below is the priority order in case where a plurality of display modes are selected.

Alarm display input	Seconds display input	Sleep display input	Display mode
L	L	L	Real time display
H	L	L	Alarm display
L	H	L	Seconds display
H	H	L	Alarm display
L	L	H	Sleep display
H	L	H	Sleep display
L	H	H	Sleep display
H	H	H	Sleep display

Note: "H": Input pin --- V_{SS} level
"L": Input pin --- V_{DD} level (or open)

4-4. Time setting input

Two pins (FAST, SLOW) are used for time setting. Setting these pins to "H" causes following operations to be performed; setting to "L" (open) causes the operations to be stopped. Setting both pins (FAST and SLOW) to "H" simultaneously causes alarm time and real time to be initialized when in the alarm display mode and seconds display mode respectively.

Display mode	Time setting input pin	Function
Real time display	FAST	Minutes contents advance at a 60Hz* rate.
	SLOW	Minutes contents advance at a 2Hz rate.
	BOTH	Minutes contents advance at a 60Hz* rate.
Alarm display	FAST	Minutes contents advance at a 60Hz* rate.
	SLOW	Minutes contents advance at a 2Hz rate.
	BOTH	AM 12:00 is set when in the 12-hour display mode. 0:00 is set when in the 24-hour display mode.
Seconds display	FAST	00 second is set. No carry to minutes is generated.
	SLOW	Seconds counting is stopped (held).
	BOTH	(When in the 12-hour display mode) the real time counter is set to AM 12:00. (When in the 24-hour display mode) the real time counter is set to 0:00.
Sleep display	FAST	Minutes contents count down at a 60Hz* rate.
	SLOW	Minutes contents count at a 2Hz rate.
	BOTH	Minutes contents count down at a 60Hz* rate.

Note: *: For 50Hz use, 50Hz shall apply.

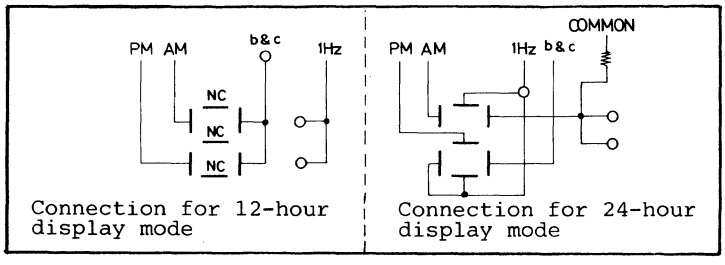
Both means that 2 input pins of FAST and SLOW are set to "H".

4-5. Output common source pin

All segment outputs are of open drain type. This pin is the common of individual source electrodes. In fluorescent display applications this pin can be used for brightness control.

4-6. 12/24-hour display mode select input

Setting this pin to "L" (open) causes the 12-hour display mode to be entered; setting to "H" causes the 24-hour display mode to be entered. The digit in 10's place is composed of 4 pins (b&c, AM, PM, 1Hz) as follows.



Connection for 12-hour display mode

Connection for 24-hour display mode

4-7. Alarm operation and output
When the alarm counter contents (alarm set time) reach the time counter contents (real time), the alarm output is turned ON. That is, the alarm output is set to "H" and turned OFF 59 minutes later. The alarm output can be turned OFF within 59 minutes by setting the ALARM OFF INPUT pin to "H". The alarm output is turned OFF temporarily by setting the SNOOZE INPUT pin to "H".

4-8. Snooze input
By connecting this pin to V_{SS}("H") temporarily while the alarm output is at "H", the alarm output is turned OFF ("L") and turned ON ("H") again 8 to 9 minutes later. This input pin contains a pull-down resistor. The snooze function can be used repeatedly as long as the alarm output is at "H".

4-9. Alarm OFF input
The alarm output is kept ON for 59 minutes. However, the alarm output can be turned OFF ("L") as soon as this pin is set to "H" momentarily during the period of 59 minutes. If the ALARM OFF input is kept at "H", the alarm output is not turned ON even when the alarm set time is reached. This pin contains a pull-down resistor.

4-10. Sleep timer and sleep output
The sleep output serves to keep the radio, etc. turned ON for any period of time up to 59 minutes. By selecting the sleep display mode (see 4-3. E), any desired period of time can be set by the operation (see 4-4.). This sleep counter is a down counter whose output is turned OFF ("L") when the counter contents reach 00 minutes.*3 When the sleep counter counts down to 00 minute, it stops counting and the sleep output is kept OFF until a desired period of time is set next. One touch permits the sleep timer to be set to 59 minutes or to be reset as shown below.

*3 It should be noted that even when the counter dose not count down to 00 minute, the SLEEP OUTPUT is turned OFF in the following cases (except when the alarm OFF operation in 4-9 is performed).
1. For 59 minutes after the alarm set time is reached
2. When the alarm set time is reached at the SLEEP OUTPUT ON-mode

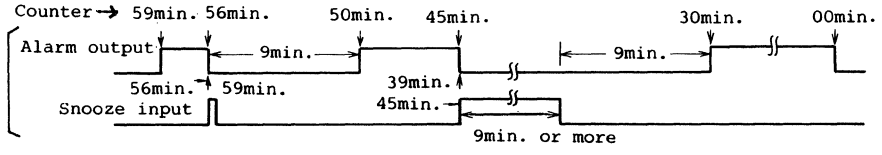
1) How to set to 59 minutes with one touch
Set the mode to a display mode other than the sleep timer display mode and resume the sleep timer display mode after setting the SNOOZE INPUT pin to "H" level temporarily, and then the sleep timer is set to 59 minutes and the SLEEP OUTPUT pin is set to "H" level.

2) How to reset the sleep timer with one touch
Set the SNOOZE INPUT pin to "H" level temporarily when the SLEEP OUTPUT is at "H" level, and the SLEEP OUTPUT pin is set to "L" level.

Note the following when using the SNOOZE INPUT pin.
a. When the snooze function is used at the alarm ON-mode (One more alarm)
b. Sleep time setting with one touch
c. Sleep time resetting with one touch
d. Sleep time hold
For a to d above, refer to the time chart shown below.

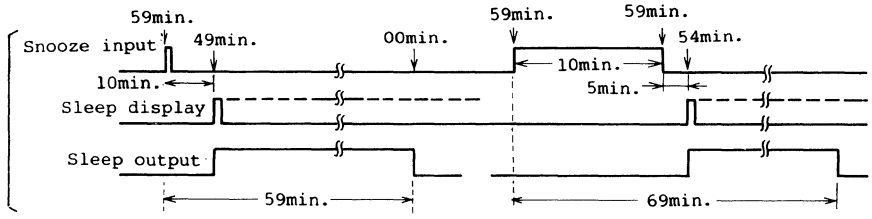
Time chart

(a)



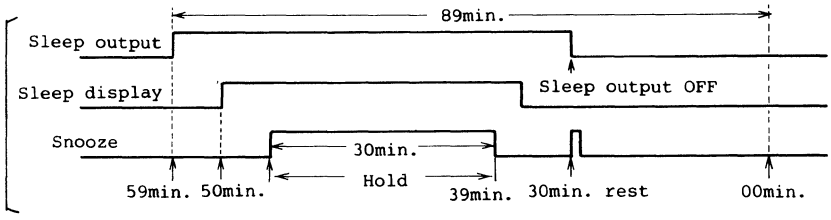
If the snooze input is set to "H" when the remaining alarm time is 59 to 56 minutes (49 to 46, ---), the remaining alarm time (including the snooze time) becomes 59 minutes (49, ---). If the snooze input is set at "H" when the remaining alarm time is 55 to 50 minutes (45 to 40, ---, 5 to 1), the remaining alarm time becomes 49 minutes (39, ---, 59).

(b)



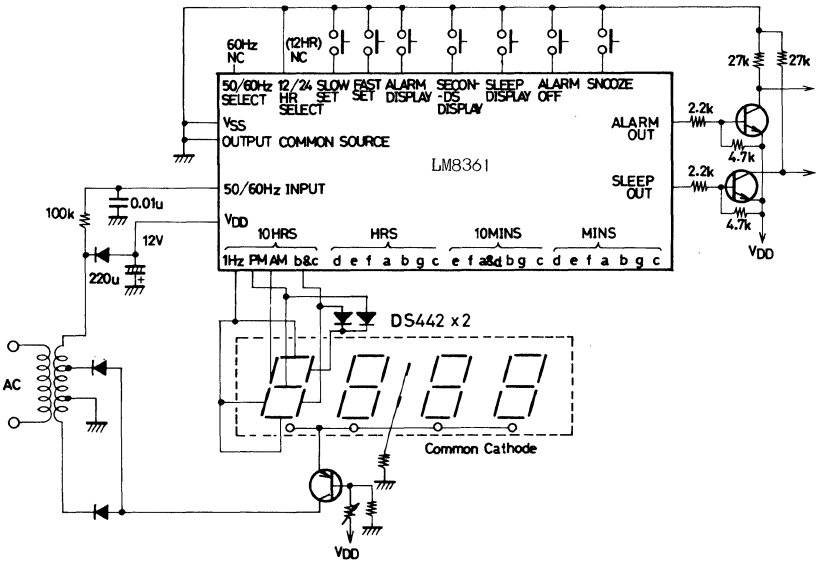
When the sleep display mode is entered after the SNOOZE INPUT pin is set to "H" level temporarily, the SLEEP OUTPUT pin is turned ON ("H"). The ON-state period continues for 59 minutes after the SNOOZE INPUT pin is to "L". Even when the SNOOZE INPUT pin is set to "H" level temporarily with the sleep display mode entered, the SLEEP OUTPUT pin is held turned ON ("H").

(c), (d)



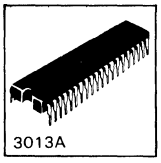
When the SNOOZE INPUT pin is set to "H" level with the SLEEP OUTPUT pin turned ON ("H"), the sleep counter stops counting. The contents of the sleep counter change as follows:
If the SNOOZE INPUT pin is set to "H" level when the remaining alarm time is 59 to 56 minutes (49 to 46, ---), the remaining alarm time becomes 59 minutes (49, ---). If the SNOOZE INPUT pin iw set to "H" level when the remaining alarm time is 55 to 50 minutes (45 to 40, ---, 5 to 1), the remaining alarm time becomes 49 minutes (39, ---, 59).
If the SNOOZE INPUT pin is set to "H" level when the SLEEP OUTPUT pin is turned ON ("H") but no sleep display mode is entered, the SLEEP OUTPUT pin is turned OFF ("L").

Sample Application Circuit



- The following LED's are available for use in this application. (For details, refer to each separate catalog.)
  LS1424, SL1476-04, SL1478, SL1494
- Pin compatible with the MM5387
- MM5387: V_{DD}=-21V typ., LM8361: V_{DD}=-12V typ.
- V_{DDmax}=23V may be applied in FLT use.

LM8362



P MOS LSI

Digital Clock Alarm

Ⓔ 1489A

Use

- Alarm clock
- Clock radio
- Timer for home appliances
- Display of time elapsed

Functions

- Real time display
- Alarm with snooze function
- Sleep timer (59 minutes max.)

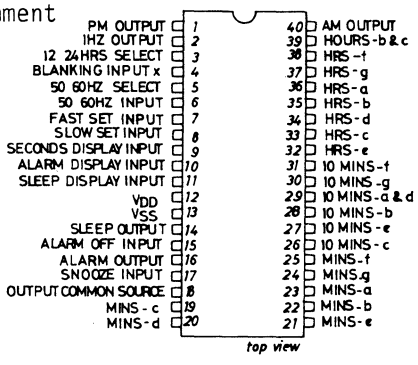
Features

- LM8362D: LED (red) use
- LM8362DH: FLT use
- LM8362DG: LED (crystal green) use
- Battery backup is avaiable for all Type Nos.
- Single-chip P-Channel ED MOS LSI
- Possible to direct drive an LED (5mA or more, red LED): LM8362D
- Possible to direct drive a fluorescent display tube (light-up voltage 21V or less): LM8362DH
- Wide operating voltage range (-6.5 to -16V) : LM8362D
- 50Hz or 60Hz is usable as reference frequency.
- Two selections of display mode (AM/PM 12-hour display mode or 24-hour display mode)
- 24-hour alarm function
- Repeatedly usable snooze function
- Presettable 59-minute down counter (sleep timer)
- Automatic decrement function of sleep timer
- Power failure indicating function (all digits flashing)
- Blanking pin for blanking out display (connectable in parallel with other LSI of P-channel open drain output type)
- Clock input noise eliminator

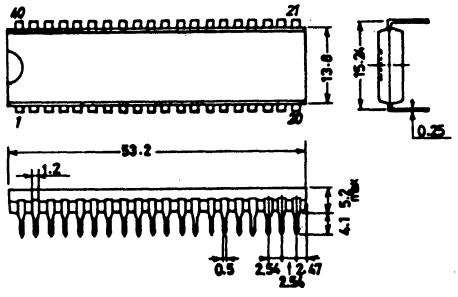
Related Type Nos.

- LM8361, LM8362, LM8363, LM8364, LM8365, LM8460, LM8560

Pin Assignment



Case Outline 3013A-D40IC (unit:mm)



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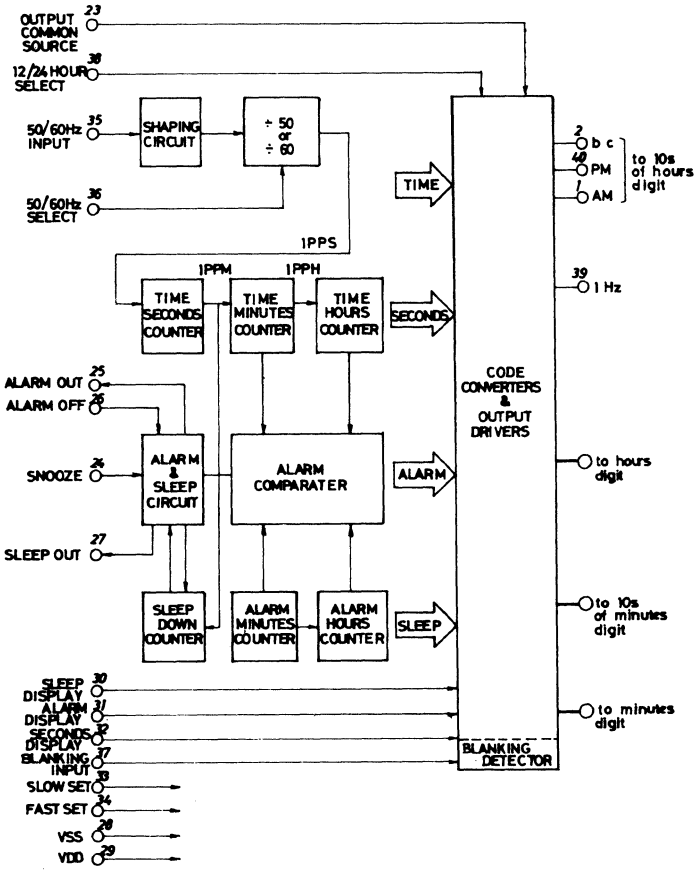
Equivalent Circuit Block Diagram



Main Specifications for LM8362D (red LED)

Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{DD}		-18 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max	Ta=70°C	0.9	W
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		-16	-12	-6.5	V
Input "H"-Level Voltage	V_{IH}		-1		0	V
Input "L"-Level Voltage	V_{IL}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
		$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-12V±2V

			min	typ	max	unit
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2V$	0.5			mA
b&c(12H mode), a&d, 1Hz	$I_{OH}(2)$	$V_{OH}=V_{SS}-2.5V$	10			mA
PM(24H mode)	$I_{OH}(3)$	$V_{OH}=V_{SS}-2.5V$	20			mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-2.5V$	5		Note 1	mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}+1.8V$			50	uA
Current Dissipation	I_{DD}	V_{DD}=-12V		3	5.5	mA

Continued from the preceding page.

Note 1: 11mA max. is allowed in the range where the power dissipation is 900mW and 1.2W at Ta=70°C and 25°C respectively.

Main Specifications for LM8362DH (FLT)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}		-23 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max.	Ta=70°C	0.2	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		-21		-6.5	V
Input "H"-Level Voltage	V_{IH}		-1		0	V
Input "L"-Level Voltage	V_{IL}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
		$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-10V to-21V

			min	typ	max	unit
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2V$	0.5			mA
b&c(12H mode), a&d, 1Hz	$I_{OH}(2)$	$V_{OH}=V_{SS}-1.0V$	2			mA
PM(24H mode)	$I_{OH}(3)$	$V_{OH}=V_{SS}-1.0V$	4			mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-1.0V$	1			mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}$			5	uA
Current Dissipation	I_{DD}	V_{DD}=-12V		3	5.5	mA

Main Specifications for LM8362DG (crystal green LED)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0

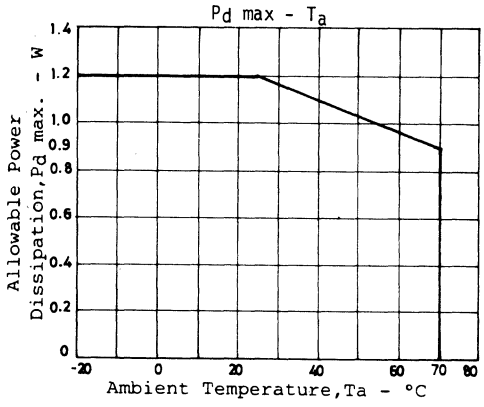
				unit
Maximum Supply Voltage	V_{DD}		-22 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max.	Ta=25°C	1.2	W
		Ta=70°C	0.9	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

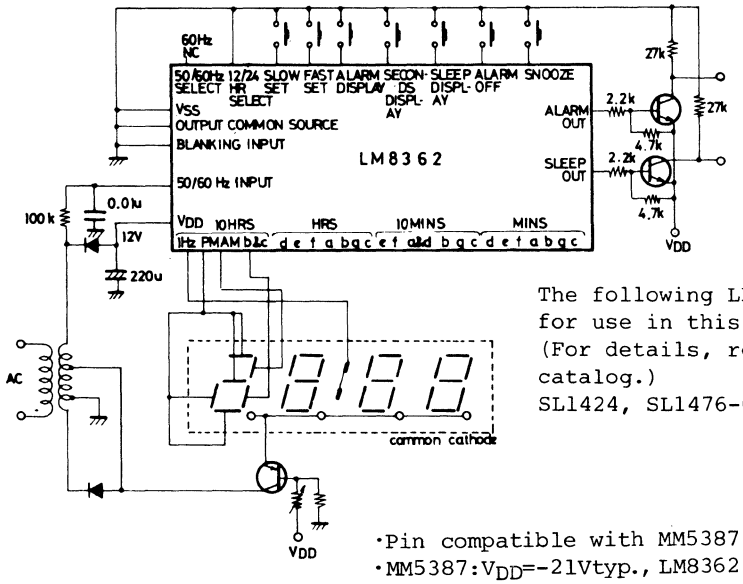
			min	typ	max	unit
Supply Voltage	V_{DD}	Display drive mode	-20	-18	-16	V
		Battery backup mode	-20		-6.5	V
Input "H"-Level Voltage	V_{IH}		-1		0	V
Input "L"-Level Voltage	V_{IL}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
		$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C,

V_{SS}=0V, V_{DD}=-18 to ±2V			min	typ	max	unit
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2V$	0.5			mA
b&c(12H mode), a&d, 1Hz	$I_{OH}(2)$	V_{DD}=-16V, $V_{OH}=V_{SS}-2.5V$	16			mA
PM(24H mode)	$I_{OH}(3)$	V_{DD}=-16V, $V_{OH}=V_{SS}-2.5V$	32			mA
Other than above	$I_{OH}(4)$	V_{DD}=-16V, $V_{OH}=V_{SS}-2.5V$	8			mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}+1.8V$			50	uA
Current Dissipation	I_{DD}	V_{DD}=-18V		3	5.5	mA



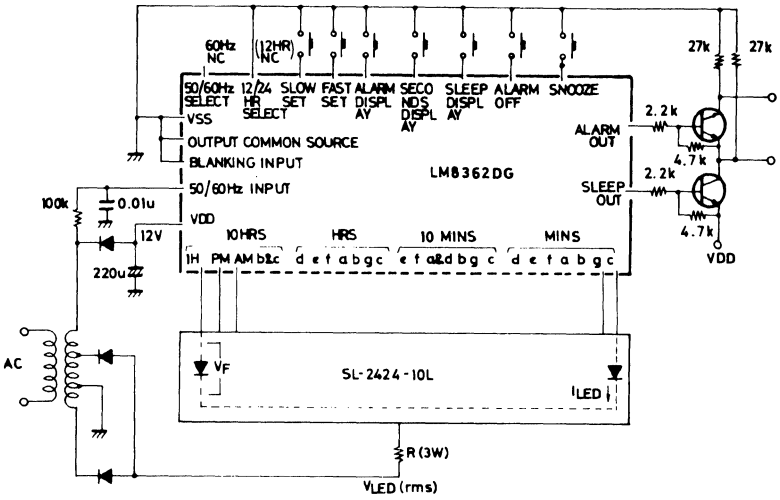
Sample Application Circuit



The following LED's are available for use in this application.
(For details, refer to each separate catalog.)
SL1424, SL1476-04, SL1478, SL1494

- Pin compatible with MM5387
- MM5387: V_{DD}=-21Vtyp., LM8362: V_{DD}=-12Vtyp.
- $|V_{DD}|$ max =23V may be applied in FLT use.

Sample Application Circuit of LM8362DG



V_{DD}=18V±2V
I_{LED}=8mA min(SL-2424-10L)
Ta max=55℃

R(Ω)	V_{LED}(V)
22±5%	9.7±1
24±5%	10.1±1
27±5%	10.7±1
30±5%	11.2±1
33±5%	11.7±1

The table shown left is for V_F=2.0.
Example: V_{LED}=11.7±0.8V
at V_F=2.0V±0.2V, R=33ohm±5%

1. Display
   1-1. Real time, alarm time, sleep time are displayed in the following display font by means of 4-digit 7-segment LED or fluorescent display tube.

   Display font 1 2 3 4 5 6 7 8 9 0

   1-2. Lighting system: Static lighing
   1-3. Display range
   - Time and alarm time display mode (12-hour display mode)
     AM1:00 to PM12:59 (highest-order digit: 0 blanking)
   - Time and alarm display mode (24-hour display mode)
     0:00 to 23:59 (highest-order digit: 0 blanking)
   - Seconds display mode
     0:00 to 9:59 (highest-order digit: blanking)
   - Sleep time display mode
     00 to 59 (highest-order and 2nd highest-order digits: blanking)
2. Input signal
   2-1. Switch signal
   - Logic "L": V_{DD}(or pin open)
   - Logic "H": V_{SS}

   2-2. 50/60Hz input signal
   - Sine wave, square wave, triangular wave, etc. of V_{DD}-V_{SS}(p-p)
   - Impedance: 1Mohm or greater
3. Output configuration
   3-1. Segment output: P-channel open drain type
   3-2. Drive output (ALARM OUT, SLEEP OUT): P-channel open drain type

4. Operation description

4-1. 50/60Hz input

This signal is used to drive the time counter. Commercial frequency 50/60Hz is put through the Schmitt circuit to be free from noise. A resistor (100 to 1000Kohm) must be connected in series with this input pin to avoid being damaged by high-voltage noise included in the commercial power supply.

4-2. 50/60Hz select input

The program counter contains a 50Hz/60Hz select circuit to provide a standard frequency of 1 pulse per second. When this pin is set at "L" or open, 60Hz use is available; when at "H", 50Hz use is available.

4-3. Display select mode

A) Alarm display input---- Setting this pin to "H" causes alarm time to be displayed.

B) Seconds display input-- Setting this pin to "H" causes the first digit of seconds and minutes to be displayed.

C) Sleep display input---- Setting this pin to "H" causes sleep time to be displayed.

D) Real time display------ When none of inputs in A), B), and C) are selected, or all of them are at "L", real time is displayed.

E) Priority order of ----- Shown below is the priority order in case display where a plurality of display modes are selected.

Alarm display input	Seconds display input	Sleep display input	Display mode
L	L	L	Real time display
H	L	L	Alarm display
L	H	L	Seconds display
H	H	L	Alarm display
L	L	H	Sleep display
H	L	H	Sleep display
L	H	H	Sleep display
H	H	H	Sleep display

Note: "H": Input pin --- V_{SS} level
"L": Input pin --- V_{DD} level (or open)
If the sleep display mode is kept on, the contents of the sleep timer count down at a 2Hz rate.

4-4. Time setting input

Two pins are used for time setting. Setting these pins to "H" causes following operations to be performed; setting to "L" (open) causes the operations to be stopped. Setting both pins (FAST and SLOW) to "H" simultaneously causes alarm time and real time to be initialized when in the alarm display mode and seconds display mode respectively.

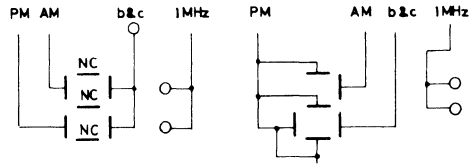
Display mode	Time setting input pin	Function
Real time display	FAST	Minutes contents advance at a 60Hz* rate.
	SLOW	Minutes contents advance at a 2Hz rate.
	BOTH	Minutes contents advance at a 60Hz* rate.
Alarm display	FAST	Minutes contents advance at a 60Hz* rate.
	SLOW	Minutes contents advance at a 2Hz rate.
	BOTH	AM 12:00 is set when in the 12-hour display mode. 0:00 is set when in the 24-hour display mode.
Seconds display	FAST SLOW BOTH	00 second is set. No carry to minutes is generated. Seconds counting is stopped (held). (When in the 12-hour display mode) the real time counter is set to AM 12:00. (When in the 24-hour display mode) the real time counter is set to 0:00.

Note: *: For 50Hz use, 50Hz shall apply.
BOTH means that 2 input pins of FAST and SLOW are set to "H".
When in the sleep display mode, the contents of the sleep counter count down at a 2Hz rate.

4-5. Blanking control input
This pin is connected to the Schmitt circuit. Normally, V_{SS}("H") is applied to this pin. If set to "L", all display drivers enter the high impedance (off) state. No pull-down resistor is contained.

4-6. Output common source pin
All segment outputs are of open drain type. This pin is the common of individual source electrodes. In fluorescent display applications this pin can be used for brightness control.

4-7. 12/24-hour display mode select input
Setting this pin to "L" (open) causes the 12-hour display mode to be entered; setting to "H" causes the 24-hour display mode to be entered. The digit in 10's place is composed of 3 pins (b&c, AM, PM) as follows:



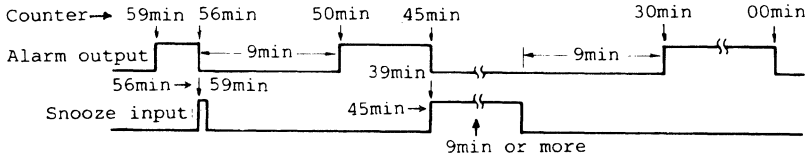
Connection for 12-hour display mode

Connection for 24-hour display mode

4-8. Alarm operation and output
When the alarm counter contents (alarm set time) reach the time counter contents (real time), the alarm output is turned ON. That is, the alarm output is set to "H" and turned OFF 59 minutes later. The alarm output can be turned OFF within 59 minutes by setting the ALARM OFF INPUT pin to "H". The alarm output is turned OFF temporarily by setting the SNOOZE INPUT pin to "H".

4-9. Snooze input
By connecting this pin to V_{SS}("H") temporarily while the alarm output is at "H", the alarm output is turned OFF ("L") and turned ON ("H") again 8 to 9 minutes later. This input pin contains a pull-down resistor. The snooze function can be used repeatedly as long as the alarm output is at "H".
Note: When using the snooze pin, the following must be noted.

Time chart



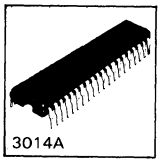
If the snooze input is set to "H" when the remaining alarm time is 59 to 56 minutes (49 to 46, ---), the remaining alarm time (including the snooze time) becomes 59 minutes (49, ---). If the snooze input is set at "H" when the remaining alarm time is 55 to 50 minutes (45 to 40, ---, 5 to 1), the remaining alarm time becomes 49 minutes (39, ---, 59).

4-10. Alarm OFF input
The alarm output is kept ON for 59 minutes. However, the alarm output can be turned OFF ("L") as soon as this pin is set to "H" momentarily during the period of 59 minutes. If the ALARM OFF input is kept at "H", the alarm output is not turned ON even when the alarm set time is reached. This pin contains a pull-down resistor.

4-11. Sleep timer and sleep output

The sleep output serves to keep the radio, etc. turned ON for any period of time up to 59 minutes. By selecting the sleep display mode (see 6-4.) , any desired period of time can be set. This sleep counter is a down counter whose output is turned OFF ("L") when the counter contents reach 00 minutes. When the sleep counter counts down to 00 minute, it stops counting and the sleep output is kept OFF until a desired period of time is set next. If the SNOOZE pin is set to "H" in other mode than the sleep display mode when the sleep output is at "H", the sleep timer output turns to "L". If the SLEEP DISPLAY input pin is kept at "H", the sleep timer contents count down at a 2Hz rate.

LM8363



P MOS LSI

Dual-Alarm Digital Clock

Ⓔ 864B

Use

- Alarm clock (Dual alarms).
- Clock radio (Dual alarms).
- Timer for household electric appliances.

Functions

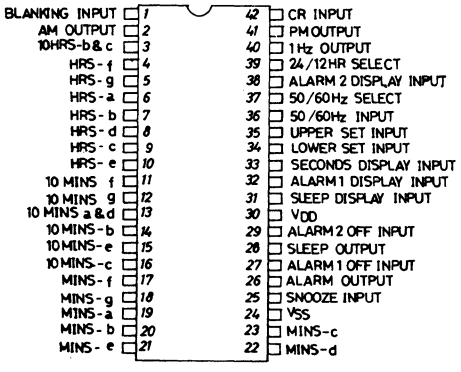
- Real time display function and month/date display function.
- Dual-alarm function with snooze function.
- Sleep timer function (Max. 59 minutes).

Features

1. P channel ED MOS LSI on a single chip.
2. Possible to direct drive LED (5mA or more, red LED). ----- LM8363D
3. Possible to direct drive fluorescent display tube (Light-up voltage : 21V or less). -----LM8363DH
4. Wide range of operating voltages (Fluorescent display tube : -6.5 to -21 V, LED : -6.5 to -16V).
5. 24-hour mode dual-alarm function.
6. Battery backup function (On-chip backup CR oscillator).
7. Month/date display function (Possible to read out by use of SNOOZE INPUT).
8. Sleep timer function (On-chip presettable max. 59-minute countdown timer).
9. Repeatedly usable snooze function.
10. 50Hz or 60Hz is usable as reference frequency.
11. Possible to select 12-hour system with AM/PM display or 24-hour system.
12. Power failure indicating function (All digits flashing).
13. Blanking pin to blank display (Possible to parallel connect with other LSI of P channel open drain output type).
14. Clock input noise suppressor.

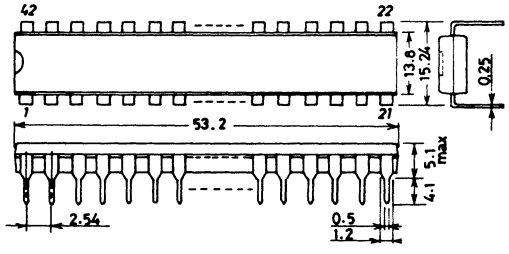
Related Products : LM8361, LM8362, LM8364, LM8365

Pin Assignment



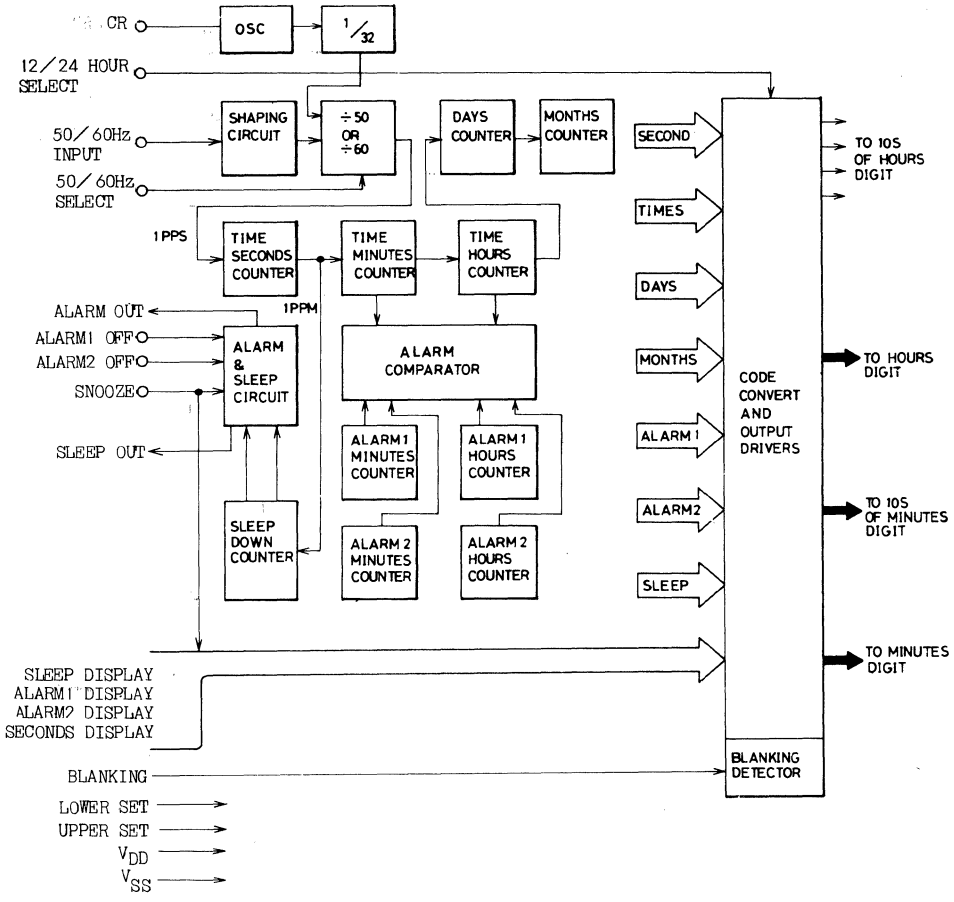
(top view)

Case Outline 3014A-D42IC
(unit:mm)



SANYO: DIP42

Equivalent Circuit Block Diagram



Main Characteristics : For LED (D, N, S specifications)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V				unit
Supply Voltage	V_{DD}		-18 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	$P_d$max	T_a=65°C	0.9	W
Operating Temperature	T_{opg}		-30 to +65	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		-16	-12	-6.5	V
Input High Level Voltage	V_{IH}	V_{DD}=-6.5 to -16V	-1		0	V
Input Low Level Voltage	V_{IL}	V_{DD}=-8.0 to -16V	V_{DD}		V_{DD}+2	V
		V_{DD}=-6.5 to -8V	V_{DD}		V_{DD}+1	V

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=-9 to -15V			min	typ	max	unit
Output High Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	V_{OH}=V_{SS}-2.5V	1.5			mA
b & c, a & d	$I_{OH}(2)$	V_{OH}=V_{SS}-2.5V	10		*	mA
1Hz	$I_{OH}(3)$	V_{OH}=V_{SS}-2.5V	15		*	mA
Other than above	$I_{OH}(4)$	V_{OH}=V_{SS}-2.5V	5		*	mA

			min	typ	max	unit
Output Leak Current						
ALARM OUT, SLEEP OUT	$I_{OL(1)}$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL(2)}$	$V_{OL}=V_{DD}$			50	uA
Input Leak Current						
ACIN	$I_{IH(1)}$	$V_{IH}=V_{SS}$			5	uA
ACIN	I_{IL}	$V_{IL}=V_{DD}$	-5			uA
Input Current (Other than AC IN)	$I_{IH(2)}$	$V_{IH}=V_{SS}$	10		200	uA
Input Pin Open Voltage (Other than AC IN)	V_{IL}	Pin open	V_{DD}		$V_{DD}+1$	V
Power Failure Detect Voltage	V_{Det}		-6.5	-4.5		V
Current Dissipation	I_{DD}	$V_{DD}=-10V$		6	10	mA

* : The segment output current is allowed max. 22mA for pins 10HRS-b&c, 10MINs a&d, and max 33mA for pin 1Hz output and max. 11mA for other than these pins in the range of 900mW of power dissipation.

Main Characteristics : For fluorescent display tube (DH, N, S specifications)

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD}		-23 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	$P_d$max	T_a=70°C	0.3	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		-21	-12	-6.5	V
Input High Level Voltage	V_{IH}	V_{DD}=-6.5 to -21V	-1		0	V
Input Low Level Voltage	V_{IL}	V_{DD}=-8.0 to -21V	V_{DD}		$V_{DD}+2$	V
		V_{DD}=-6.5 to -8.0V	V_{DD}		$V_{DD}+1$	V

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=-9V to -21V

			min	typ	max	unit
Output High Level Current						
ALARM OUT, SLEEP OUT	$I_{OH(1)}$	$V_{OH}=V_{SS}-2.5V$	1.5			mA
b & c, a & d	$I_{OH(2)}$	$V_{OH}=V_{SS}-1.0V$	2			mA
1Hz	$I_{OH(3)}$	$V_{OH}=V_{SS}-1.0V$	3			mA
Other than above	$I_{OH(4)}$	$V_{OH}=V_{SS}-1.0V$	1			mA
Output Leak Current						
ALARM OUT, SLEEP OUT	$I_{OL(1)}$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL(2)}$	$V_{OL}=V_{DD}$			2	uA
Input Leak Current						
ACIN	$I_{IH(1)}$	$V_{IH}=V_{SS}$			5	uA
ACIN	I_{IL}	$V_{IL}=V_{DD}$	-5			uA
Input Current (Other than AC IN)	$I_{IH(2)}$	$V_{IH}=V_{SS}$	10		200	uA
Input Pin Open Voltage (Other than AC IN)	V_{IL}	Pin open	V_{DD}		$V_{DD}+1$	V
Power Failure Detect Voltage	V_{Det}		-6.5	-4.5		V
Current Dissipation	I_{DD}	V_{DD}=-10V		6	10	mA

1. Display

1-1. 4-digit 7-segment static lighting system.

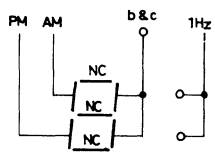
Display font 1 2 3 4 5 6 7 8 9 0

1-2. Display mode

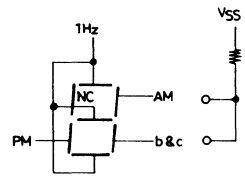
. Time and alarm time display mode (12-hour system) 1:00AM to 12:59PM (10's digit of hours : 0 blanking).
(24-hour system) 0:00 to 23:59 (10's digit of minutes : 0 blanking).

. Month/date display mode (12-hour system) 1 1 to 12 31 (10's digit of months, 10's digit of dates : 0 blanking).
(24-hour system) 1 : 1 to 31 : 12 (10's digit of months, 10's digit of dates : 0 blanking).
. Seconds display mode (12-hour system) 0 00 to 9 59 (Digit No.1:blanking).
(24-hour system) 0:00 to 9:59 (Digit No.1:blanking).
. Sleep time display mode (12-hour system) 00 to 59 (Digits No.1 and No.2 : blanking).
(24-hour system) :00 to : 59 (Digits No.1 and No.2 : blanking).

1-3. Connection for 10's digit of hours



12-hour system



24-hour system

1-4. 1Hz output
. 24-hour system ----- Used for segments a, d, g of digit No.1.
. 12-hour system ----- Real time (hours/minutes) display mode and alarm time display mode ——— Flashing at a 1Hz rate.
Month/date display mode, sleep time display mode, seconds display mode ——— OFF (Unlighted).

1-5. Month/date display mode

	Digits No.1 and No.2	Digits No.3 and No.4
24-hour system	Date	Month
12-hour system	Month	Date

1-6. Power failure indication
. All ON-state segments flash at a 1Hz rate at all display modes. ---- Power failure indication.
. Flashing to indicate power failure is released by applying the input UPPER SET INPUT or LOWER SET INPUT.

1-7. Display during backup operation
. When the count operation is performed (during backup operation) by CR-OSC oscillation frequency with no input applied to 50/60Hz INPUT, all ON-state segment outputs will be turned OFF.

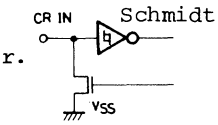
2. Input Organization

2-1. Logic level
. Logic "L" ----- V_{DD} level
. Logic "H" ----- V_{SS} level

2-2. AC INPUT
. With built-in Schmidt circuit, the input impedance is more than 1Mohm.
. The clamp circuit for a voltage being more minus than V_{DD} is built in.

2-3. BLANKING INPUT
. Input pin with pull-down resistor. If connected to V_{DD} or made open, all segments will be turned OFF; and if connected to V_{SS}, the normal ON-state will return.

2-4. CR INPUT
. This consists of a Schmidt circuit and an open drain driver.



2-5. Input pins other than above
. Input pins with pull-down resistor.

3. Output Organization

All of segment output, alarm output, and sleep output are of P channel open drain type.

4. Operation Description

4-1. Display mode selection

. The display mode is selected by using SLEEP DISPLAY INPUT, SNOOZE INPUT, ALARM 1 DISPLAY INPUT, ALARM 2 INPUT, and SECONDS DISPLAY INPUT. The order of priority given to these switch signals is as shown in Table 1.

Table 1. Order of priority given to switch signals

Switch input					Display mode
SLEEP DISPLAY	SNOOZE	ALARM 1 DISPLAY	ALARM 2 DISPLAY	SECOND	
H	-	-	-	-	Sleep display
L	H	-	-	-	Month/date display
L	L	-	H	H	Month/date display
L	L	H	L	-	Alarm 1 display
L	L	H	H	L	Alarm 1 display
L	L	L	H	L	Alarm 2 display
L	L	L	L	H	Seconds display
L	L	L	L	L	Real time display

Note: "H" : V_{SS} level is applied to input pin.
"L" : V_{DD} level is applied to input pin. (Input pin may be made open.)
"-" : V_{SS} level or V_{DD} level is applied to input pin or input pin may be made open. (Don't care)

4-2. Time setting

. Time setting is executed by applying V_{SS} level to UPPER SET INPUT and LOWER SET INPUT.
. When executing setting, no carry occurs from the low-order digit to the high-order digit.
. The operation contents at each display mode are as shown in Table 2.

Table 2. Operation contents

Display mode	Setting input	Operation contents	
Real time display	UPPER	Minutes advance at a 2Hz rate.	
	LOWER	Minutes advance at a 2Hz rate.	No carry to hours occurs. Seconds are cleared to 00.
	BOTH	Minutes advance at a 5Hz rate.	
Alarm 1 display (Alarm 2 display)	UPPER	Hours of alarm 1(alarm 2) advance at a 2Hz rate.	No carry to hours occurs.
	LOWER	Minutes of alarm 1(alarm 2) advance at a 2Hz rate.	
	BOTH	Minutes of alarm 1(alarm 2) advance at a 5Hz rate.	
Month/ date display	UPPER	Month (date) advances at a 2Hz rate.	( ) : 24-hour system. No carry occurs from the low-order digit to the high-order digit.
	LOWER	Date (month) advances at a 2Hz rate.	
	BOTH	Date (month) advances at a 5Hz rate.	
Sleep display	UPPER	No operation.	
	LOWER	Minutes of sleep timer subtract at a 2Hz rate.	
	BOTH	Minutes of sleep timer subtract at a 5Hz rate.	

Continued on the next page.

Continued from the preceding page.

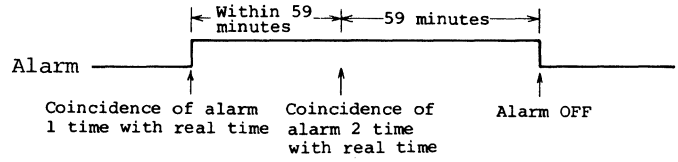
Seconds display	UPPER	Seconds counter stops running.
	LOWER	Seconds are cleared to 00. Clearing continues until switch is released.
	BOTH	Each counter is reset at follows: Real time — 12:01AM (For 24-hour system, 0:01) Alarm time— 12:00AM (For 24-hour system, 0:00) Month/date- 12 1 (For 24-hour system, 1:12)

Note : BOTH means that V_{SS} level signal is applied by pressing both switches of UPPER SET INPUT and LOWER SET INPUT.

4-3. Alarm operation

1) The 24-hour mode dual alarms of alarm 1 and alarm 2 are built in. The alarm outputs are each made available once in 24 hours. The displaying and setting of the time contents are done as shown in table 1 and Table 2 .

2) The alarm 1 time and alarm 2 time can be set independently. When the alarm 1 time coincides with the real time, ALARM OUTPUT will be turned ON (H level) and will be turned OFF (L level) automatically 59 minutes later. When the alarm 2 time coincides with the real time within 59 minutes after the alarm 1 time coincided with the real time, ALARM OUTPUT will be turned OFF automatically 59 minutes after the time with which the alarm 2 time coincided.



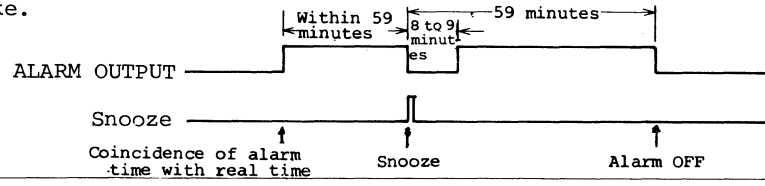
3) ALARM OUTPUT release
When the real time coincides with the alarm 1 time (alarm 2 time) and ALARM OUTPUT is turned ON, ALARM OUTPUT can be turned OFF by applying H level to ALARM 1 OFF INPUT (ALARM 2 OFF INPUT).

4) Alarm operation inhibit
The following alarm operation is available corresponding to the level setting of ALARM 1 OFF INPUT and ALARM 2 OFF INPUT.

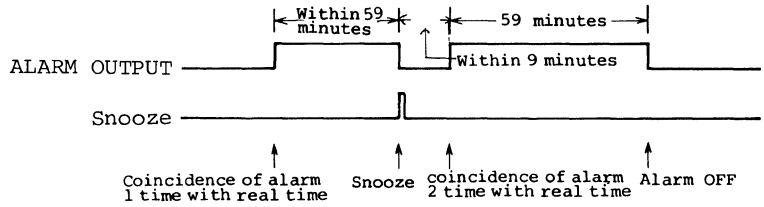
ALARM 1 OFF INPUT	ALARM 2 OFF INPUT	Operation of alarm 1	Operation of alarm 2
L	L	o	o
H	L	x	o
L	H	o	x
H	H	x	x

"L" : V_{DD} level or open.
"H" : V_{SS} level.
"o" : Normal operation.
"x" : Operation inhibit. Even if the alarm time coincides with the real time, ALARM OUTPUT will not be turned ON.

5) Snooze operation
If "H" level is applied to SNOOZE INPUT while ALARM OUTPUT is turned ON, ALARM OUTPUT will be turned OFF temporarily and will be turned ON again 8 to 9 minutes later. The snooze operation is available as often as you like.



When the alarm 2 time coincides with the real time during the snooze operation, the snooze operation will be released at this point of time and ALARM OUTPUT will be turned ON.



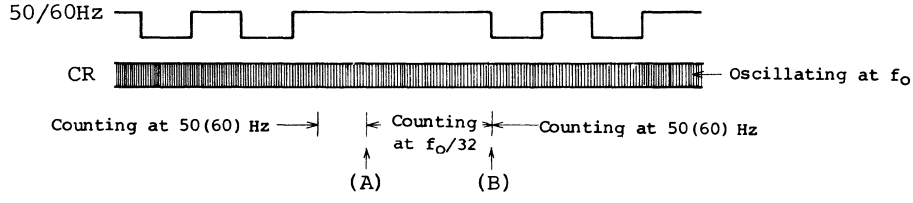
6) Relation between alarm operation and sleep operation
   . SLEEP OUTPUT is not turned ON while ALARM OUTPUT is turned ON (including the period of snooze operation).
   . Contrary to this, even if the alarm time coincides with the real time while SLEEP OUTPUT is turned ON, ALARM OUTPUT will not be turned ON.

4-4. Sleep operation

1) If "H" level is applied to SLEEP DISPLAY INPUT when both ALARM OUTPUT and SLEEP OUTPUT are turned OFF, the sleep timer will be set to 59 minutes and SLEEP OUTPUT will be turned ON. When the sleep timer reaches 0 minute after the lapse of 59 minutes, SLEEP OUTPUT will be turned OFF.
2) If "H" level is applied to SLEEP DISPLAY INPUT while SLEEP OUTPUT is turned ON, the sleep timer will not be set to 59 minutes, but will display the remaining period of time.
3) The sleep timer can be advanced fast as shown in Table 2.
4) Sleep timer release
   . If "H" level is applied to SNOOZE INPUT at other display modes than sleep display mode while SLEEP OUTPUT is turned ON, SLEEP OUTPUT will be turned OFF. If "H" level is applied to SNOOZE INPUT at the sleep display mode, the sleep timer will be preset to 59 minutes. (A simple touch of the switch permits 59 minutes to be set.)
5) Relation between alarm operation and sleep operation
   Refer to 4-3 - 6).

4-5. Backup operation

1) $|V_{DD}|$ min. for the normal operation of LSI inside is 6.5V.
2) For the backup operation during power failure, the following actions are required.
   (1) A voltage of more than 6.5V must be applied across V_{DD} and V_{SS}.
   (2) CR INPUT must be oscillated with a frequency 32 times as high as 50Hz (or 60Hz).
   In case of power failure, these (1) and (2) cause the internal reference clock to be changed-over automatically to the oscillation frequency at CR INPUT.
3) When restored to normal from power failure, the reference clock will be changed-over automatically to 50/60Hz.
4) Changeover operation time chart



(A): When there is no input applied to 50/60Hz INPUT for $1/f_o \times 64$(sec.), the reference frequency will be changed-over from 50/60Hz to $f_o/32$Hz.
(B): The moment 50/60Hz INPUT receives the input, the reference frequency will be changed-over from $f_o/32$ to 50/60Hz.

5) Rejection of interference noise to radio
By stopping oscillation at CR INPUT during application of AC power supply and starting oscillation simultaneously with power failure, the interference noise to radio due to oscillation at CR INPUT can be rejected. (Refer to Application Circuit 1.)

6) Segment output during backup operation
During the period from (A) to (B) shown in the time chart in 4), all segment outputs are turned OFF automatically.

4-6. Commercial frequency and its selection

1) The commercial frequency is inputted from 50/60Hz INPUT. This pin contains a Schmidt circuit to prevent malfunction due to external noise. It is necessary to use this pin in conjunction with a CR filter having 100 to 1000 kohm and 0.01uF to prevent LSI breakdown due to high-voltage impulse, etc. from the commercial power supply.

2) 50Hz or 60Hz is selected by use of 50/60Hz SELECT.
50Hz : 50/60 Hz SELECT is set at "H" level (V_{SS}).
60Hz : 50/60 Hz SELECT is set at "L" level (V_{DD}) or is made open.

4-7. 12/24-hour system selection

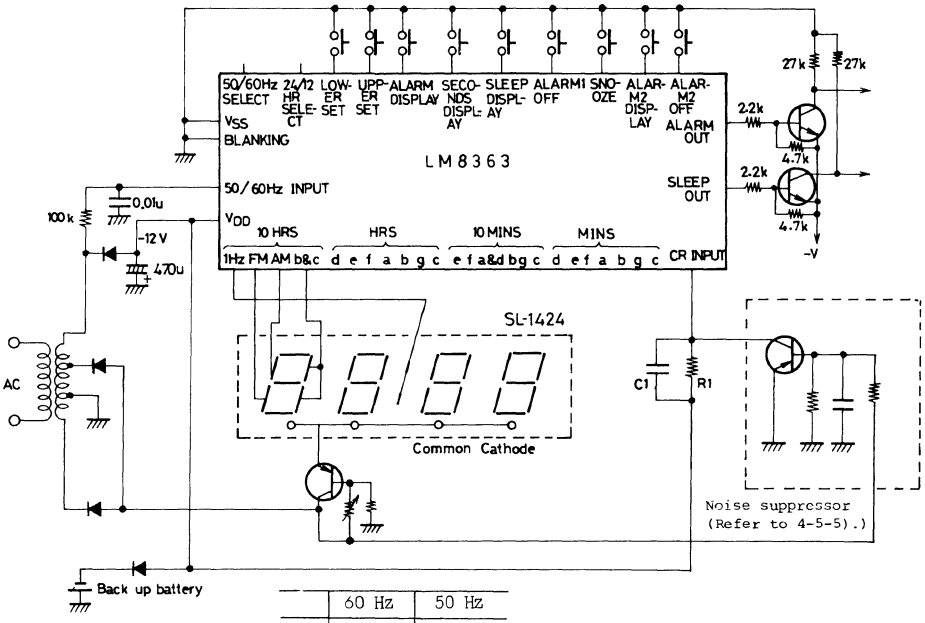
. The display content is selected as follows by use of $^{24}/_{12}$ HR SELECT.

$^{24}/_{12}$ HR SELECT	Real time and alarm time	Month/date	
		Digits No. 1 and No.2	Digits No. 3 and No.4
"H" level (V_{SS})	24-hour system	Date	Month
"L" level (V_{DD}) or open	12-hour system	Month	Date

5. Functional Table of Rank Products

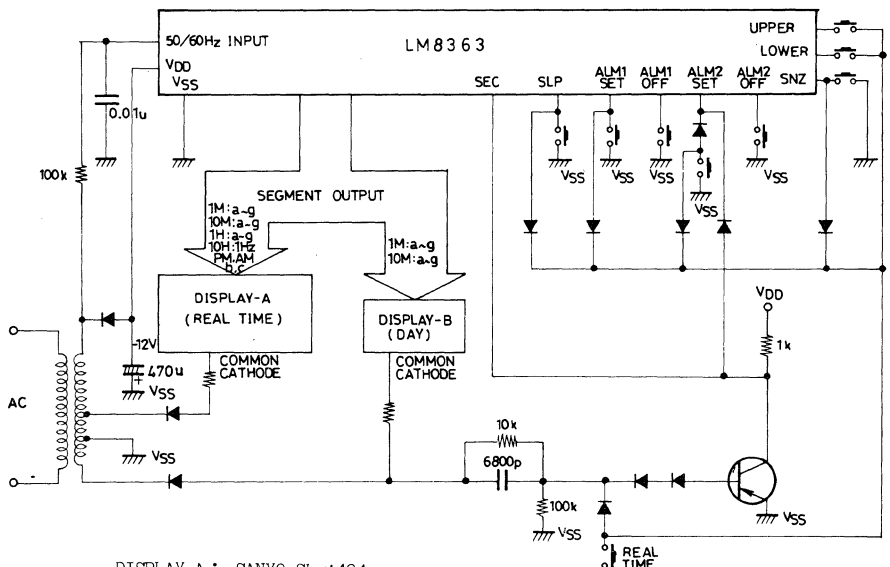
Rank	Display tube		Remarks
	LED (red)	Fluorescent disply tube	
LM8363 D	o		
LM8363 DH		o	
LM8363 N	o	o	
LM8363 S	o	o	For use in industrial applications

Application Circuit 1 : LED display (Common cathode), 12-hour system, Backup operation automatic changeover circuit (Suppression of interference noise to radio)



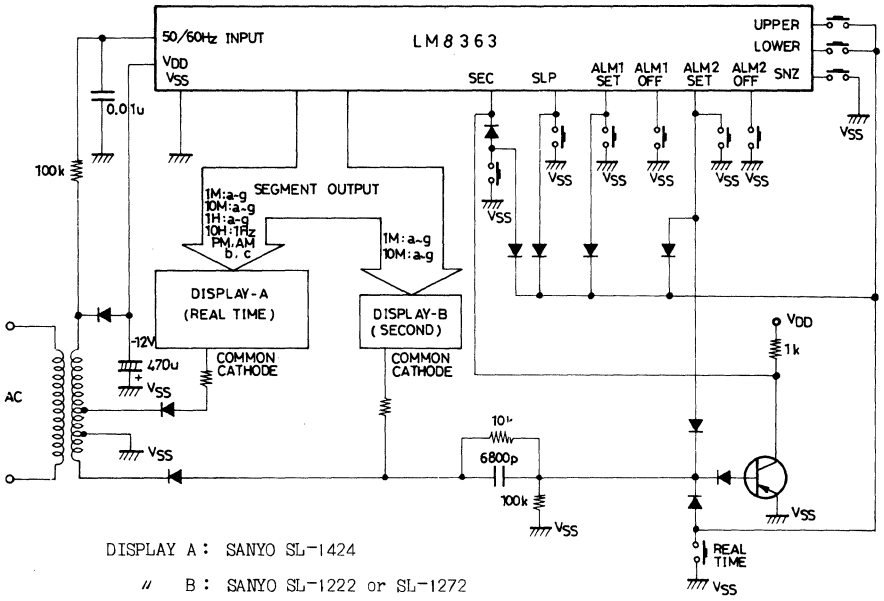
	60 Hz	50 Hz
R1	130 k	150 k
C1	0.0068u	0.0068u
f_0	1.92 k	1.6 k

Application Circuit 2 : 6-digit display (Real time + date, 12-hour system)



DISPLAY A : SANYO SL-1424
〃 B : SANYO SL-1222 or SL-1272

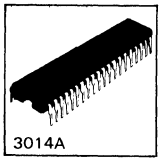
Application Circuit 3 : 6-digit display (Real time + seconds)



DISPLAY A : SANYO SL-1424

〃 B : SANYO SL-1222 or SL-1272

LM8364



P MOS LSI

Dual-Alarm Digital Clock

Ⓔ 888A

Use

- Alarm clock (Dual alarms).
- Clock radio (Dual alarms).
- ON/OFF timer for household electric appliances.

Functions

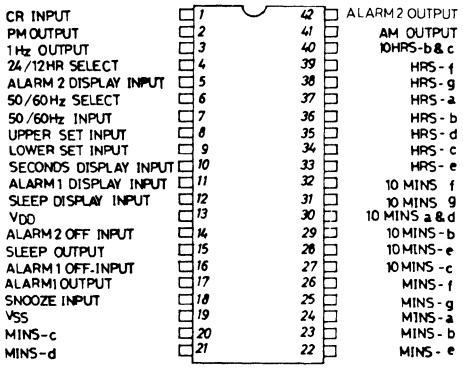
- Real time display function and month/date display function.
- Dual-alarm output function with snooze function.
- Sleep timer function (Max. 59 minutes).

Features

1. •P channel ED MOS LSI on a single chip.
2. Possible to direct drive LED (5mA or more, red LED) : LM8364D
3. Possible to direct drive fluorescent display tube (Light-up voltage : 21V or less) : LM8384DH
4. Wide range of operating voltages (-6.5 to -16 V).
5. 24-hour mode dual-alarm function. For one alarm output, DC output signal is provided. For the other alarm output, DC output signal or approximately 1600Hz modulation output signal (ON/OFF at a 1Hz rate) can be selected. Each alarm has its own alarm output signal.
6. Battery backup function (On-chip backup CR oscillator).
7. Month/date display function.
8. Sleep timer function (On-chip presettable max. 59-minute countdown timer).
9. Repeatedly usable snooze function.
10. 50Hz or 60Hz is usable as reference frequency.
11. Possible to select 12-hour system with AM/PM display or 24-hour system.
12. Power failure indicating function (All digits flashing).
13. Clock input noise suppressor.
14. Symmetrical pin assignment against LM8363 (Mirror-image pin assignment).

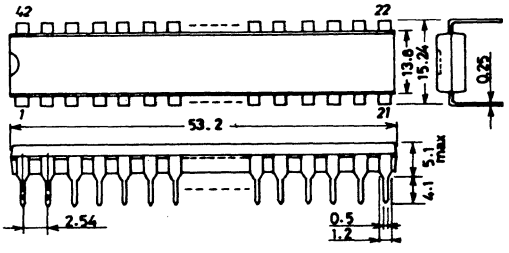
Related Products : LM8361, LM8362, LM8363, LM8365

Pin Assignment



(top view)

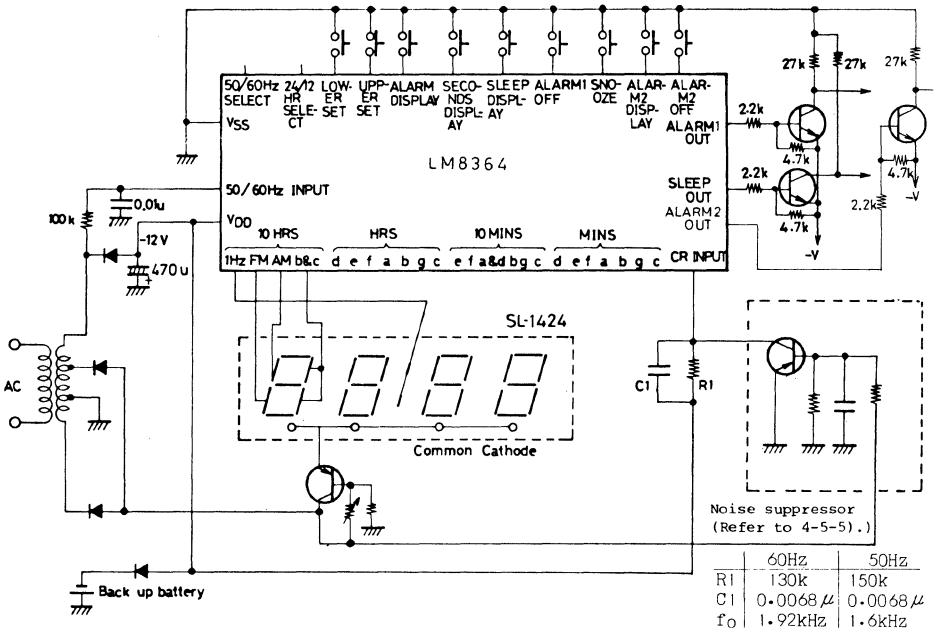
Case Outline 3014A-D42IC
(unit:mm)



SANYO: DIP42

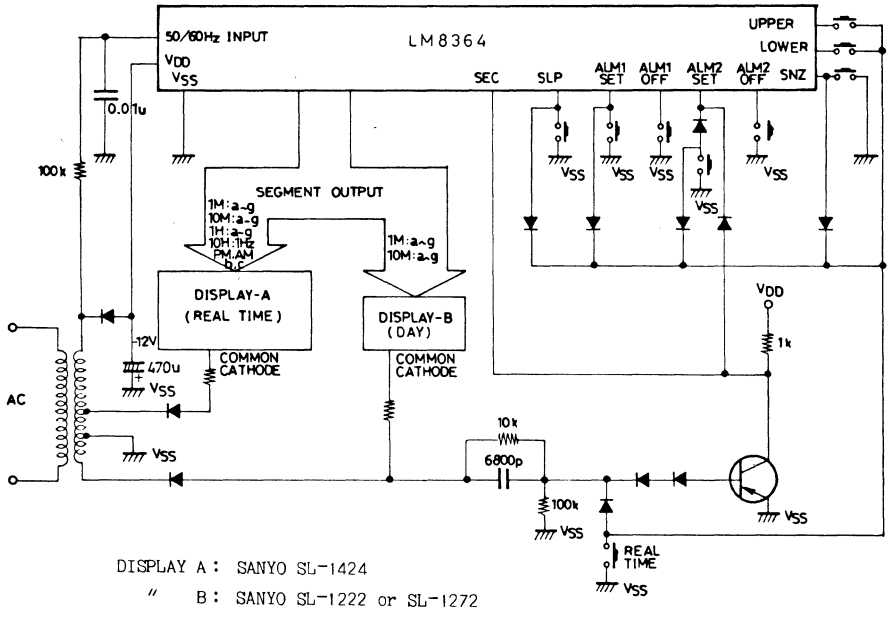
Application Circuits

(a) LED display (Common cathode), 12-hour system, Backup operation automatic changeover circuit (Suppression of interference noise to radio)



	60Hz	50Hz
R1	130k	150k
C1	0.0068μ	0.0068μ
fo	1.92kHz	1.6kHz

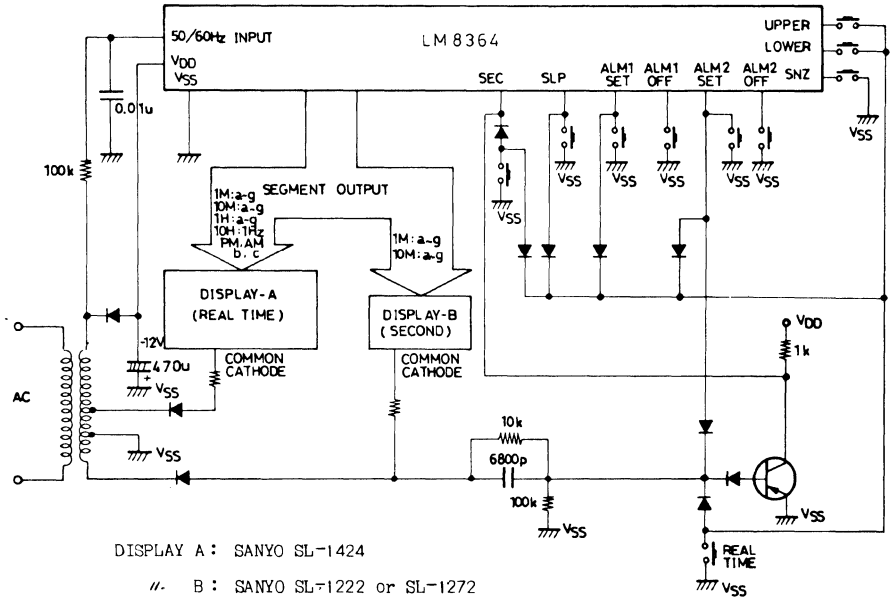
(b) 6-digit display (Real time + date, 12-hour system)



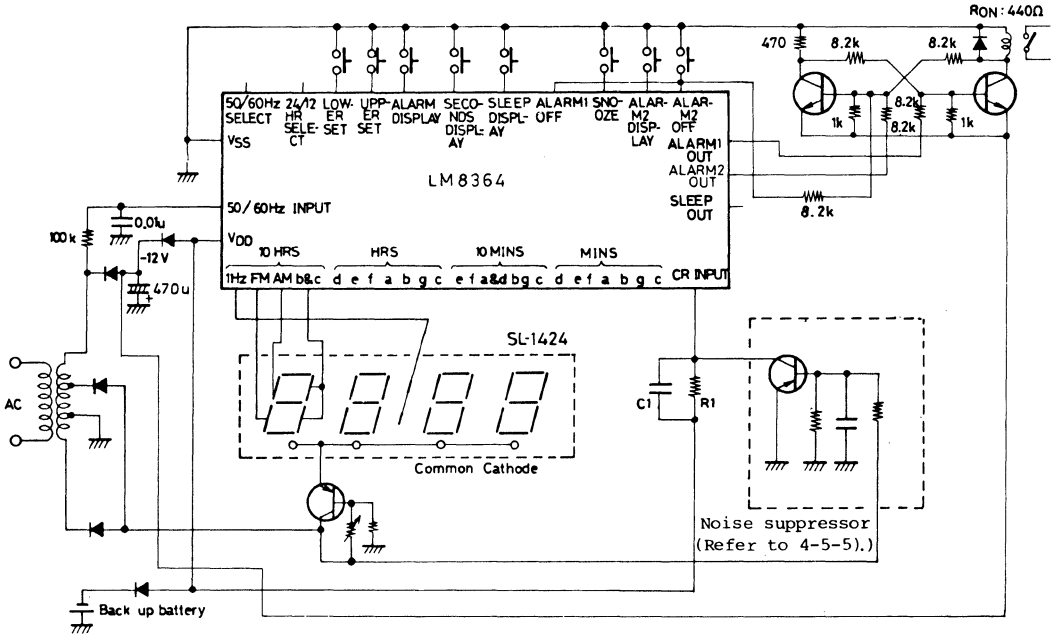
DISPLAY A : SANYO SL-1424

" B : SANYO SL-1222 or SL-1272

(c) 6-digit display (Real time + seconds)



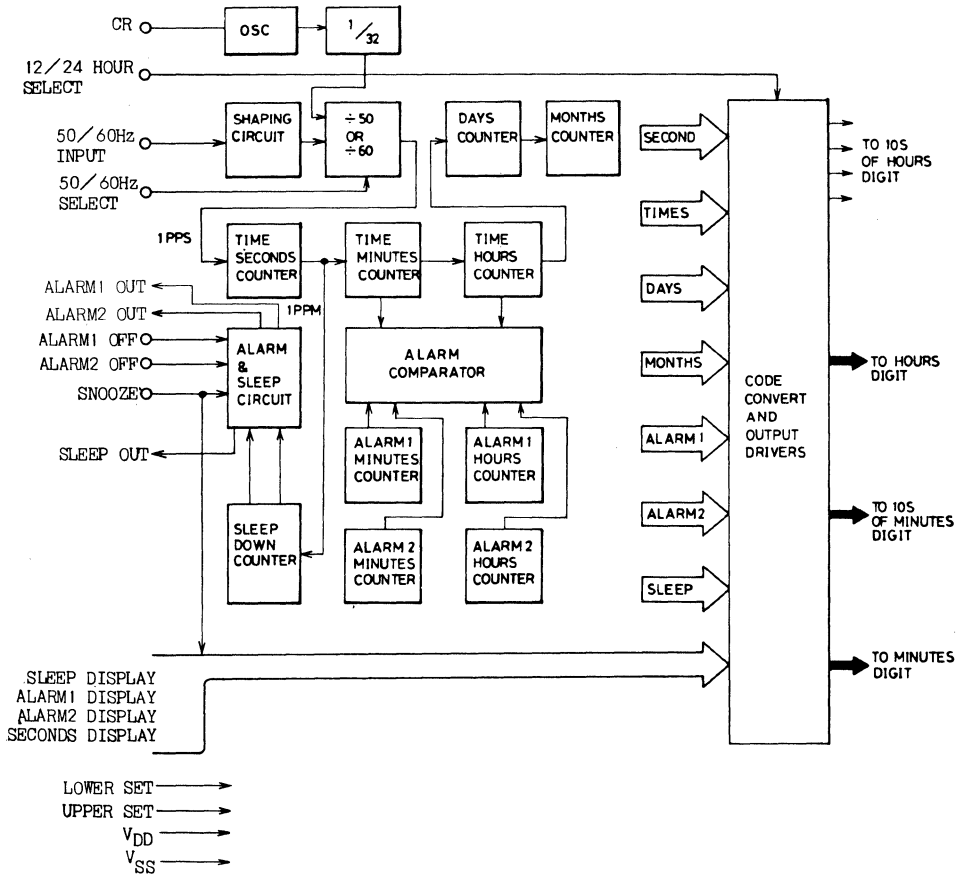
(d) ON/OFF timer, LED display (Common cathode), 12-hour system, Backup operation automatic changeover circuit (Suppression of interference noise to radio)



. Alarm 1 : ON time
. Alarm 2 : OFF time

	60Hz	50Hz
R1	130k	150k
C1	0.0068u	0.0068u
f_O	1.92kHz	1.6kHz

Equivalent Circuit Block Diagram



Main Characteristics : For LED (D, N, S, specifications)

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Supply Votlage	V_{DD}		-18 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	$P_d$max	Ta=65°C	0.9	W
Operating Temperature	T_{opg}		-30 to +65	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		-16	-12	-6.5	V
Input High Level Voltage	V_{IH}	V_{DD}=-6.5 to -16V	-1		0	V
Input Low Level Voltage	V_{IL}	V_{DD}=-8.0 to -16V	V_{DD}		V_{DD}+2	V
		V_{DD}=-6.5 to -8V	V_{DD}		V_{DD}+1	V

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=-9 to -15V			min	typ	max	unit
Output High Level Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2.5V$	1.5			mA
b & c, a & d	$I_{OH}(2)$	$V_{OH}=V_{SS}-2.5V$	10		*	mA
1Hz	$I_{OH}(3)$	$V_{OH}=V_{SS}-2.5V$	15		*	mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-2.5V$	5		*	mA
Output Leak Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}$			50	uA
Input Leak Current						
ACIN	$I_{IH}(1)$	$V_{IH}=V_{SS}$			5	uA
	I_{IL}	$V_{IL}=V_{DD}$	-5			uA
Input Current (Other than AC IN)	$V_{IH}(2)$	$V_{IH}=V_{SS}$	10		200	uA
Input Pin Open Voltage (Other than AC IN)	V_{ILopen}	Pin open	V_{DD}		V_{DD}+1	V
Power Failure Detect Voltage	V_{Det}		-6.5	-4.5		V
Current Dissipation	I_{DD}	V_{DD}=-10V		6	10	mA
Oscillation Period CR INPUT	T_{OSC}	Cl=0.0068uF, Rl=150k ohm, V_{DD}=-8V	0.569	0.625	0.681	mA

* : The segment output current is allowed max. 22mA for pins 10HRS-b&c, 10MINS a & d, and max. 33mA for pin 1Hz OUTPUT, and max. 11mA for other than these pins in the range of 900mW of power dissipation.

Main Characteristics : For fluorescent display tube (DH, N, S specifications)

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V				unit
Supply Voltage	V_{DD}		-23 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	$P_d$max	T_a=70°C	0.3	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		-21	-12	-6.5	V
Input high Level Voltage	V_{IH}	V_{DD}=-6.5 to -21V	-1		0	V
Input Low Level Voltage	V_{IL}	V_{DD}=-8.0 to -21V	V_{DD}		V_{DD}+2	V
		V_{DD}=-6.5 to -8.0V	V_{DD}		V_{DD}+1	V

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=-9 to -21V			min	typ	max	unit
Output High Level Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2.5V$	1.5			mA
b & c, a & d	$I_{OH}(2)$	$V_{OH}=V_{SS}-1.0V$	2			mA
1Hz	$I_{OH}(3)$	$V_{OH}=V_{SS}-1.0V$	3			mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-1.0V$	1			mA
Output Leak Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}$			2	uA

Continued on the next page.

Continued from the preceding page.			min	typ	max	unit
Input Leak Current						
ACIN	$I_{IH(1)}$	$V_{IH}=V_{SS}$			5	uA
	I_{IL}	$V_{IL}=V_{DD}$	-5			uA
Input current (Other than AC IN)	$I_{IH(2)}$	$V_{IH}=V_{SS}$	10		200	uA
Input Pin Open Voltage (Other than AC IN)	V_{ILopen}	Pin open	V_{DD}		$V_{DD}+1$	V
Power Failure Detect Voltage	V_{Det}		-6.5	-4.5		V
Current Dissipation	I_{DD}	$V_{DD}=-10V$		6	10	mA
Oscillation Period CR INPUT	T_{OSC}	C1=0.0068uF,R1=150k ohm,V_{DD}=-8V	0.569	0.625	0.681	mA

1. Display

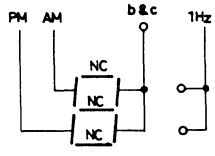
1-1. 4-digit 7-segment static lighting system.

Display font 1 2 3 4 5 6 7 8 9 0

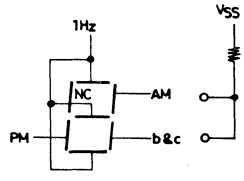
1-2. Display mode

. Time and alarm time display mode	(12-hour system)	1:00AM to 12:59PM (10's digit of hours:0 blanking).
	(24-hour system)	0:00 to 23:59 (10's digit of hours :0 blanking).
. Month/date display mode	(12-hour system)	1 1 to 12 31 (10's digit of hours, 10's digit of minutes: 0 blanking).
	(24-hour system)	1: 1 to 31:12 (10's digit of hours, 10's digit of minutes: 0 blanking).
. Seconds display mode	(12-hour system)	0 00 to 9 59 (Digit No.1: Blanking).
	(24-hour system)	0:00 to 9:59 (Disit No.1: Blanking).
. Sleep display mode	(12-hour system)	00 to 59 (Digits No. 1 and No. 2 : Blanking).
	(24-hour system)	:00 to :59 (Digits No. 1 and No. 2: Blanking).

1-3. Connection for 10's digit of hours



12-hour system



24-hour system

1-4. 1Hz output
- . 24-hour system : Used for segments a, d, g of digit No. 1.
- . 12-hour system : Real time (hours/minutes) display mode and alarm time display mode ——— Flashing at a 1Hz rate.
  Month/date display mode, sleep display mode, seconds display mode ——— OFF (Unlighted).

1-5. Month/date display mode

	Digits No.1 and No.2	Digits No.1 and No.2
24-hour system	Date	Month
12-hour system	Month	Date

1-6. Power failure indication
- . All ON-state segments flash at a 1Hz rate at all display modes. ——— Power failure indication.
- . Flashing to indicate power failure is released by applying the input to UPPER SET INPUT or LOWER SET INPUT.

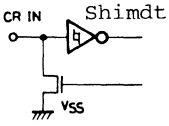
1-7. Display during backup operation
- . When the count operation is performed (during backup operation) by CR-OSC
- • oscillation frequency with no input applied to 50/60 Hz INPUT, all ON-state segment outputs will be turned OFF.

2. Input Organization

2-1. Logic level
- . Logic "L" : V_{DD} level
- . Logic "H" : V_{SS} level

2-2. AC INPUT
- . With built-in Schmidt circuit, the input impedance is more than 1Mohm.
- . The clamp circuit for a voltage being more minus than V_{DD} is built in.

2-3. CR INPUT
- . This consists of a Schmidt circuit and an open drain driver.



2-4. Input pins other than above
- . Input pins with pull-down resistor.

3. Output Organization

All of segment output, alarm output, and sleep output are of P channel open drain type.

4. Operation Description

4-1. Display mode selection
- . The display mode is selected by using SLEEP DISPLAY INPUT, ALARM 1 DISPLAY INPUT, ALARM 2 DISPLAY INPUT, and SECONDS DISPLAY INPUT. The order of priority given to these switch signals is as shown in Table 1.

Table 1. Order of priority given to switch signals

Switch input				Display mode
SLEEP DISPLAY	ALARM 1 DISPLAY	ALARM 2 DISPLAY	SECOND	
H	-	-	-	Sleep display
L	-	H	H	Month/date display
L	H	L	-	Alarm 1 display
L	H	H	L	Alarm 1 display
L	L	H	L	Alarm 2 display
L	L	L	H	Seconds display
L	L	L	L	Real time display

Note : "H" : V_{SS} level is applied to input pin.
"L" : V_{DD} level is applied to input pin.
"-" : V_{SS} level or V_{DD} level is applied to input pin or input pin may be made open.

4-2. Time setting

- Time setting is executed by applying V_{SS} level to UPPER SET INPUT and LOWER SET INPUT.
- When executing setting, no carry occurs from the low-order digit to the high-order digit.
- The operation contents at each display mode are as shown in Table 2.

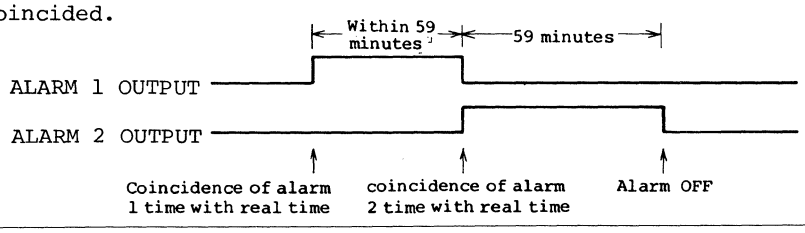
Table 2. Operation contents

Display mode	Setting input	Operation contents	
Real time display	UPPER	Minutes advance at a 2Hz rate.	
	LOWER	Minutes advance at a 2Hz rate.	No carry to hours occurs. Seconds are cleared to 00.
	BOTH	Minutes advance at a 5Hz rate.	
Alarm 1 display (alarm 2 display)	UPPER	Hours of alarm 1 (alarm 2) advance at a 2Hz rate.	
	LOWER	Minutes of alarm 1 (alarm 2) advance at a 2Hz rate.	No carry to hours occurs.
	BOTH	Minutes of alarm 1 (alarm 2) advance at a 5Hz rate.	
Month/ date display	UPPER	Month (date) advances at a 2Hz rate.	( ) : 24-hour system. No carry occurs from the low-order digit to the high-order digit.
	LOWER	Date (month) advances at a 2Hz rate.	
	BOTH	Date (month) advances at a 5Hz rate.	
Sleep display	UPPER	No operation.	
	LOWER	Minutes of sleep timer subtract at a 2Hz rate.	
	BOTH	Minutes of sleep timer subtract at a 5Hz rate.	
Seconds display	UPPER	Seconds counter stops running.	
	LOWER	Seconds are cleared to 00. Clearing continues until switch is released.	
	BOTH	Each counter is reset at follows : Real time — 12:01AM (For 24-hour system, 0:01) Alarm time — 12:00AM (For 24-hour system, 0:00) Month/date — 12 1 (For 24-hour system, 1:12)	

Note : BOTH means that V_{SS} level signal is applied by pressing both switches of UPPER SET INPUT and LOWER SET INPUT.

4-3. Alarm operation

1) The 24-hour mode dual alarms of alarm 1 and alarm 2 are built in. The alarm outputs are each made available once in 24 hours. The time contents are displayed, read out, and set as shown in Table 1 and Table 2.
2) The alarm 1 time and alarm 2 time can be set independently. When the alarm 1 time (alarm 2 time) coincides with the real time, ALARM 1 OUTPUT (ALARM 2 OUTPUT) will be turned ON (H level) and will be turned OFF (L level) automatically 59 minutes later. When the alarm 2 time coincides with the real time within 59 minutes after the alarm 1 time coincided with the real time, ALARM 2 OUTPUT will be turned ON and will be turned OFF automatically 59 minutes after the time with which the alarm 2 time coincided.

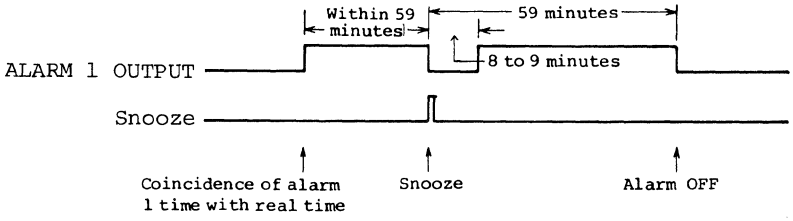


3) When the alarm 1 time and alarm 2 time, which are set at the same time, coincide with the real time simultaneously, ALARM 1 OUTPUT only will be turned ON and ALARM 2 OUTPUT will not be turned ON.
4) ALARM OUTPUT release
When the real time coincides with the alarm 1 time (alarm 2 time) and ALARM 1 OUTPUT (ALARM 2 OUTPUT) is turned ON, ALARM 1 OUTPUT (ALARM 2 OUTPUT) can be turned OFF by applying H level to ALARM 1 OFF INPUT (ALARM 2 OFF INPUT).
5) Alarm operation inhibit
The following alarm operation is available corresponding to the level setting of ALARM 1 OFF INPUT and ALARM 2 OFF INPUT.

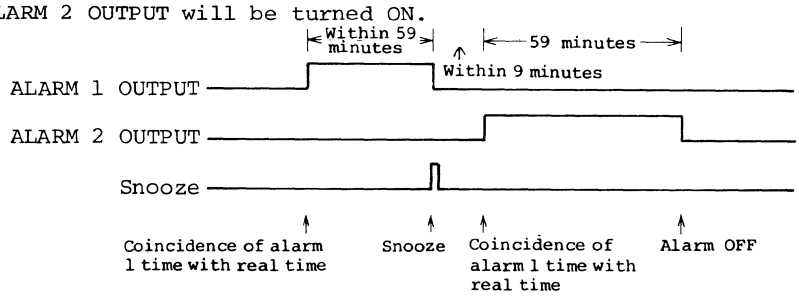
ALARM 1 OFF INPUT	ALARM 2 OFF INPUT	Operation of alarm 1	Operation of alarm 2
L	L	o	o
H	L	x	o
L	H	o	x
H	H	x	x

"L" : V_{DD} level or open.
"H" : V_{SS} level.
"o" : Normal operation.
"x" : Operation inhibit. Even if the alarm time coincides with the real time, ALARM OUTPUT will not be turned ON.

6) Snooze operation
If "H" level is applied to SNOOZE INPUT while ALARM OUTPUT is turned ON, ALARM OUTPUT will be turned OFF temporarily and will be turned ON 8 to 9 minutes later. The snooze operation is available as often as you like.

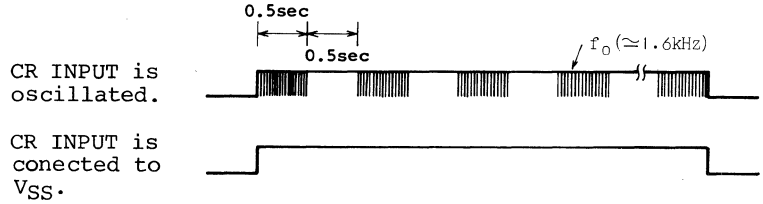


When the alarm 2 time coincides with the real time during the snooze operation, the snooze operation will be released at this point of time and ALARM 2 OUTPUT will be turned ON.



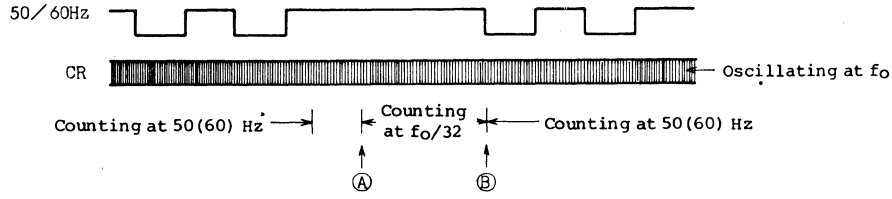
7) Relation between alarm operation and sleep operation
. SLEEP OUTPUT is not turned ON while ALARM OUTPUT is turned ON (including the period of snooze operation).
. Contrary to this, even if the alarm time coincides with the real time while SLEEP OUTPUT is turned ON, ALARM OUTPUT will not be turned ON.

8) ALARM OUTPUT waveform
For ALARM 1 OUTPUT, DC output signal is provided. For ALARM 2 OUTPUT, either of the following two output signals is selectable according as CR INPUT is oscillated or not.



4-4. Sleep operation
1) If "H" level is applied to SLEEP DISPLAY INPUT when all of ALARM 1 OUTPUT, ALARM 2 OUTPUT, and SLEEP OUTPUT are turned OFF, the sleep timer will be set to 59 minutes and SLEEP OUTPUT will be turned ON. When the sleep timer reaches 0 minutes after the lapse of 59 minutes, SLEEP OUTPUT will be turned OFF.
2) If "H" level is applied to SLEEP DISPLAY INPUT while SLEEP OUTPUT is turned ON, the sleep timer will not be set to 59 minutes, but will display the remaining period of time.
3) The sleep timer can be advanced fast as shown in Table 2.
4) Sleep timer release
If "H" level is applied to SNOOZE INPUT at other display modes than sleep display mode while SLEEP OUTPUT is turned ON, SLEEP OUTPUT will be turned OFF. If "H" level is applied to SNOOZE INPUT at the sleep display mode, the sleep timer will be preset to 59 minutes. (A simple touch of the switch permits 59 minutes to be set.)
5) Relation between alarm operation and sleep operation
Refer to 4-3-7).

4-5. Backup operation
1) $|V_{DD}|$ min. for the normal operation of LSI inside is 6.5V.
2) For the backup operation during power failure, the following actions are required.
(1) A voltage of more than 6.5V must be applied across V_{DD} and V_{SS}.
(2) CR INPUT must be oscillated with a frequency 32 times as high as 50Hz (or 60Hz).
In case of power failure, these (1) and (2) cause the internal reference clock to be changed-over automatically to the oscillation frequency at CR INPUT.
3) When restored to normal from power failure, the reference clock will be changed-over automatically to 50/60Hz.
4) Changeover operation time chart



Ⓐ : When there is no input applied to 50/60Hz INPUT for $\frac{1}{f_o} \times 64$ (sec.), the reference frequency will be changed-over from 50/60Hz to $f_o/32$ Hz.
Ⓑ : The momemt 50/60Hz INPUT receives the input, the reference frequency will be changed-over from $f_o/32$ to 50/60 Hz.

5) Rejection of interference noise to radio
By stopping oscillation at CR INPUT during application of AC power supply and starting oscillation simultaneously with power failure, the interference noise to radio due to oscillation at CR INPUT can be rejected. (Refer to Application Circuit.)

6) Segment output during backup operation
During the period from Ⓐ to Ⓑ shown in the time chart in 4), all segment outputs are turned OFF automatically.

4-6. Commercial frequency and its selection

1) The commercial frequency is inputted from 50/60Hz INPUT. This pin contains a Schmidt circuit to prevent malfunction due to external noise. It is necessary to use this pin in conjunction with a CR filter having 100 to 1000 kohm and 0.01uF to prevent LSI breakdown due to high-voltage impulse, etc. from the commercial power supply.

2) 50Hz or 60Hz is selected by use of 50/60Hz SELECT.
50Hz : 50/60Hz SELECT is set at "H" level (V_{SS}).
60Hz : 50/60Hz SELECT is set at "L" level (V_{DD}) or is made open.

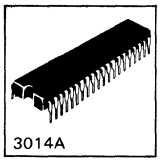
4-7. 12/24-hour system selection
The display content is selected as follows by use of 24/12 HRS SELECT.

24 / 12 HRS SELECT	Real time and alarm time	Month/date	
		Digits No. 1 and No. 2	Digits No. 1 and No.2
"H" level (V_{SS})	24-hour system	Date	Month
"L" level (V_{DD}) or open	12-hour system	Month	Date

5. Functional Table of Rank Products

Rank	Display tube		Remarks
	LED (red)	Fluorescent display tube	
LM8364 D	o		
LM8364 DH		o	
LM8364 N	o	o	
LM8364 S	o	o	For use in industrial applications

LM8365



P MOS LSI

Dual-Alarm Digital Clock

Ⓔ 1499A

Use

- Alarm clock (Dual alarm).
- Clock radio (Dual alarm).
- ON/OFF timer for household electric appliances.

Functions

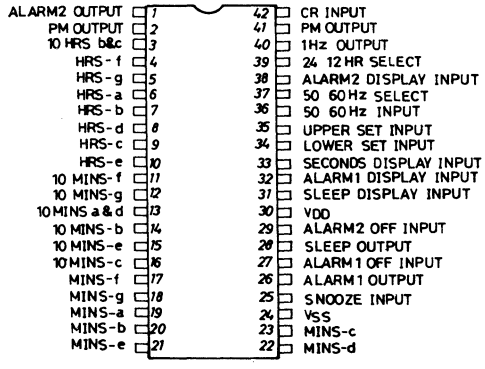
- Real time display function and month/date display function.
- Dual-alarm output function with snooze function.
- Sleep timer function (Max. 59 minutes).

Features

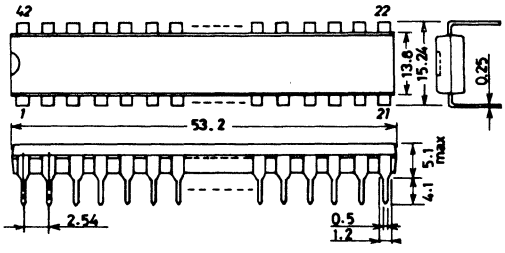
1. P channel ED MOS LSI on a single chip.
2. Possible to direct drive LED (5mA or more, red LED) : LM8365D
3. Possible to direct drive fluorescent display tube (Light-up voltage : 21V or less) : LM8365DH
4. Wide range of operating voltage (-6.5 to -16 V).
5. 24-hour mode dual-alarm function. For one alarm output, DC output signal is provided. For the other alarm output, DC output signal or approximately 1600Hz modulation output signal (ON/OFF at a 1Hz rate) can be selected. Each alarm has its own alarm output signal.
6. Battery backup function (On-chip backup CR oscillator).
7. Month/date display function.
8. Sleep timer function (On-chip presettable max. 59-minutes coundown timer).
9. Repeatedly usable snooze function.
10. 50Hz or 60Hz is usable as reference frequency.
11. Possible to select 12-hour system with AM/PM display or 24-hour system.
12. Power failure indicating function (All digits flashing).
13. Clock input noise suppressor.
14. Symmetrical pin assignment against LM8364 (Mirror-image pin assignment).

Related Products : LM8361, LM8362, LM8363, LM8364, LM8368, LM8460, LM8560

Pin Assignment



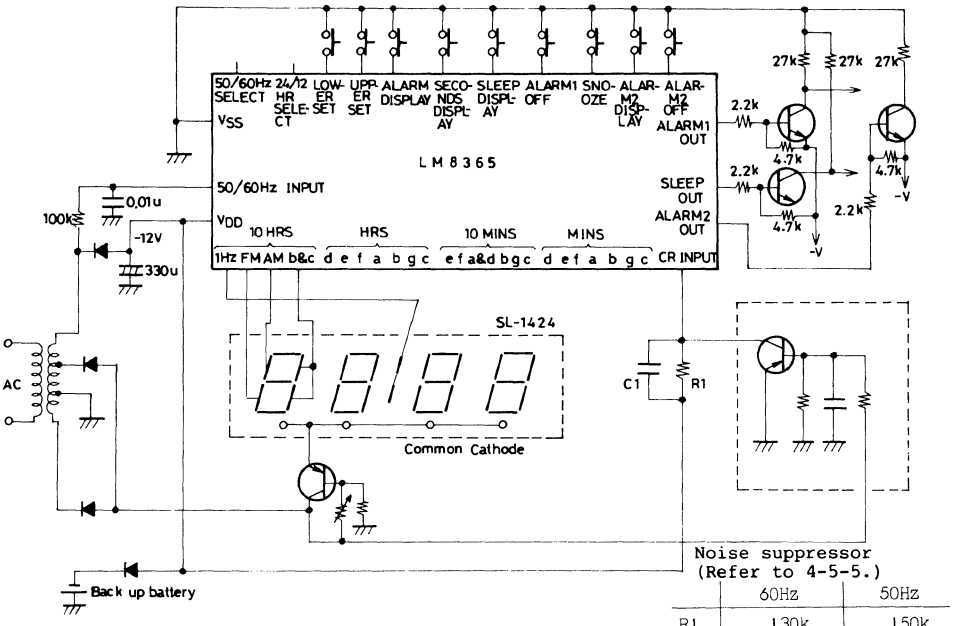
Case Outline 3014A-D42IC
(unit:mm)



SANYO: DIP42

Application Circuits

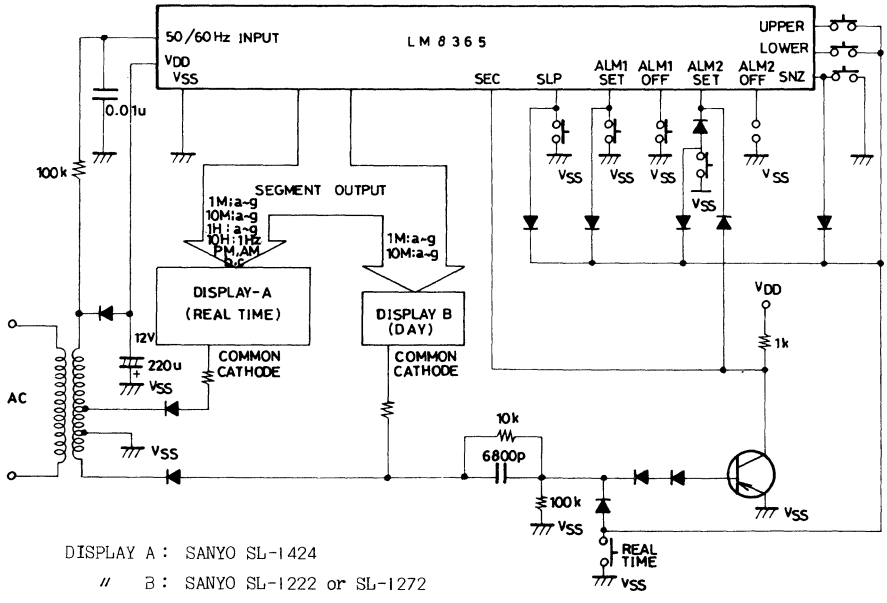
(a) LED display (Common cathode), 12-hour system, Backup operation automatic changeover circuit (Suppression of interference noise to radio)



Noise suppressor (Refer to 4-5-5.)

	60Hz	50Hz
R1	130k	150k
C1	0.0068 μ	0.0068 μ
f_0	1.92kHz	1.6kHz

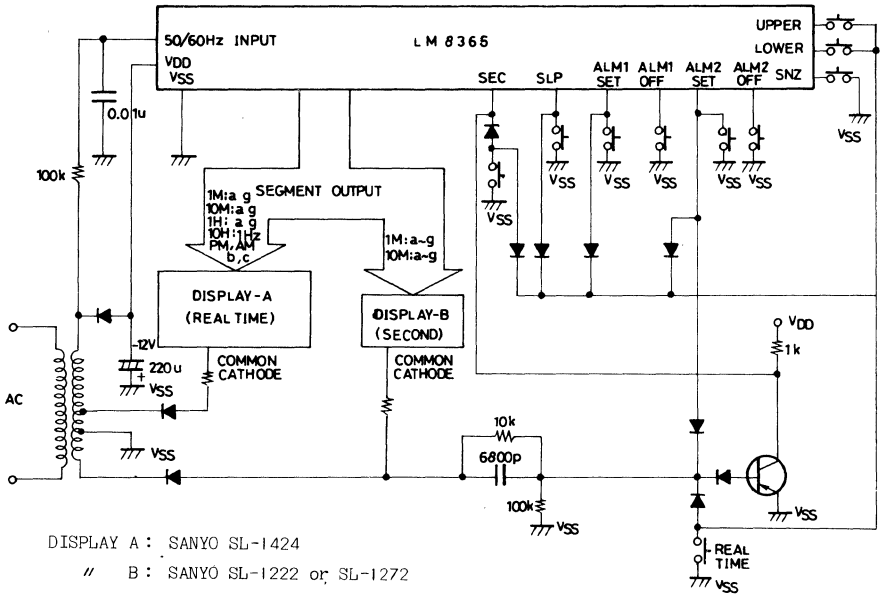
(b) 6-digit display (Real time+date, 12-hour system)



DISPLAY A : SANYO SL-1424

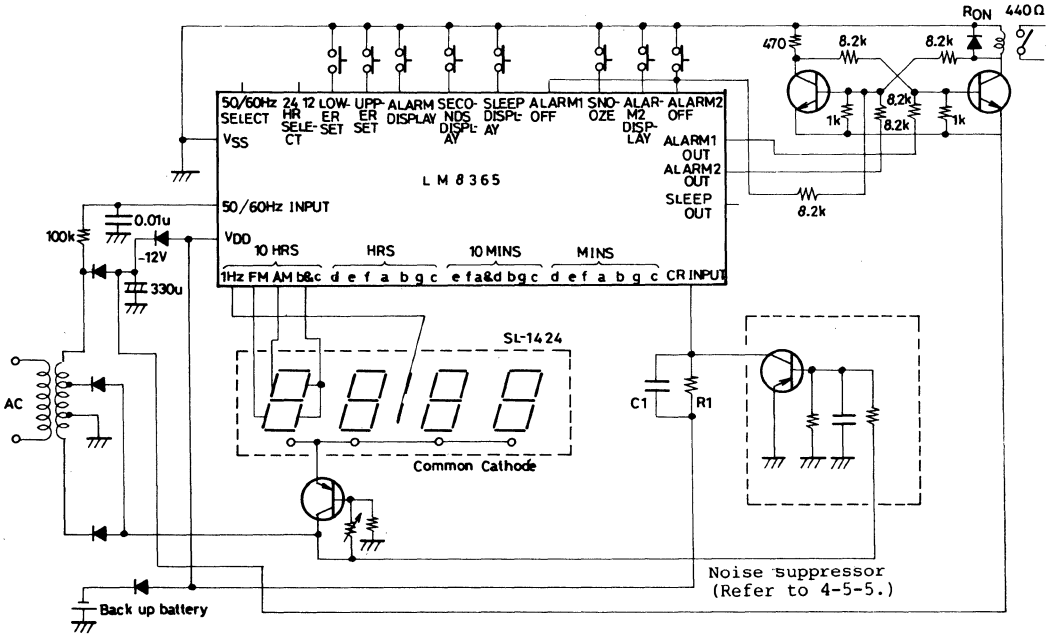
〃 B : SANYO SL-1222 or SL-1272

(c) 6-digit display (Real time+seconds)



DISPLAY A : SANYO SL-1424
〃 B : SANYO SL-1222 or SL-1272

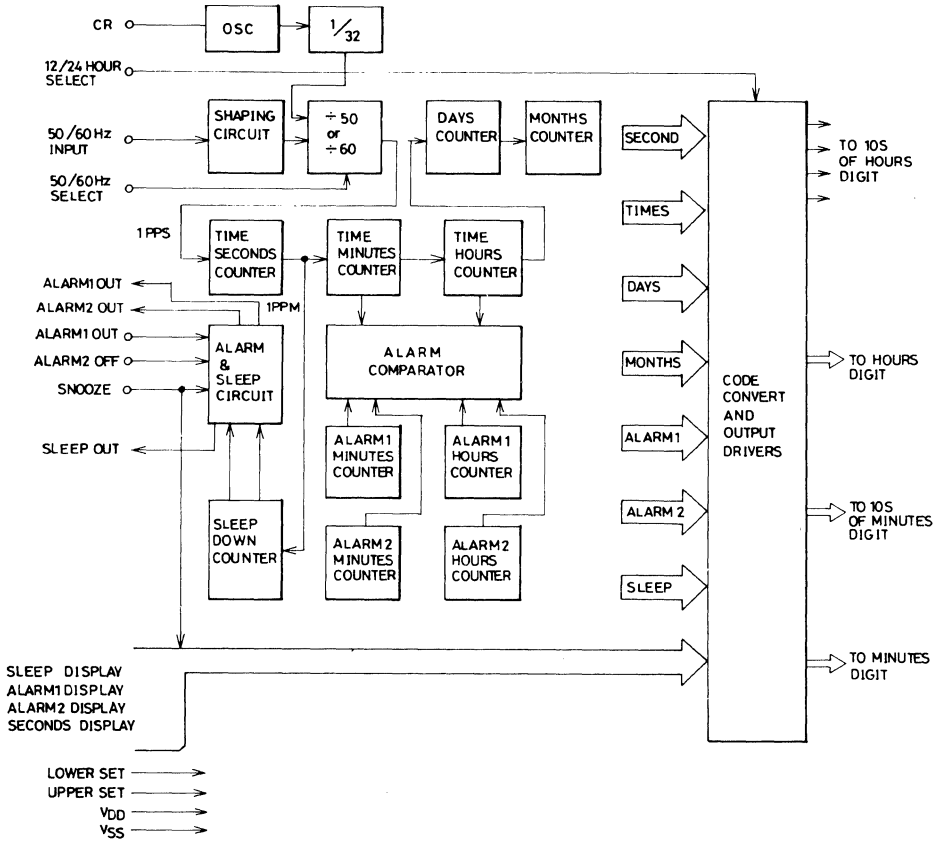
(d) ON/OFF timer, LED display (Common cathode), 12-hour system, Backup operation automatic changeover circuit (Suppression of interference noise to radio)



- Alarm 1 : ON time
- ALARM 2 : OFF time

	60Hz	50Hz
R1	130k	150k
C1	0.0068μ	0.0068μ
f_0	1.92kHz	1.6kHz

Equivalent Circuit Block Diagram



Main Characteristics : For LED (D, N, S specifications)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V				unit
Supply Voltage	V_{DD}		-18 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pdmax	Ta=65°C	0.9	W
Operating Temperature	Topg		-30 to +65	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Range at Ta=25°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		-16	-12	-6.5	V
Input High Level Voltage	V_{IH}	V_{DD}=-6.5 to -16V	-1		0	V
Input Low Level Voltage	V_{IL}	V_{DD}=-8.0 to -16V	V_{DD}		V_{DD}+2	V
		V_{DD}=-6.5 to -8V	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-9 to -15V			min	typ	max	unit
Output High Level Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2.5V$	1.5			mA
b & c, a & d	$I_{OH}(2)$	$V_{OH}=V_{SS}-2.5V$	10		*	mA
1Hz	$I_{OH}(3)$	$V_{OH}=V_{SS}-2.5V$	15		*	mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-2.5V$	5		*	mA
Output Leak Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}$			50	uA
Input Leak Current						
ACIN	$I_{IH}(1)$	$V_{IH}=V_{SS}$			5	uA
	I_{IL}	$V_{IL}=V_{DD}$	-5			uA
Input Current (Other than AC IN)	$I_{IH}(2)$	$V_{IH}=V_{SS}$	10		200	uA
Input Pin Open Voltage (Other than AC IN)	V_{ILopen}	Pin open	V_{DD}		V_{DD}+1	V
Power Failure Detect Voltage	V_{Det}		-6.5	-4.5		V
Current Dissipation	I_{DD}	V_{DD}=-10V		6	10	mA
Oscillation Period CR INPUT	T_{osc}	C1=0.0068uF, R1=150Kohm, V_{DD}=-8V	0.569	0.625	0.681	mA

* : The segment output current is allowed max. 22mA for pins 10HRS-b&c, 10MINS a & d, and max. 33mA for pin 1Hz OUTPUT, and max. 11mA for other than these pins in the range of 900mW of power dissipation.

Main Characteristics : For fluorescent display tube (DH, N, S specifications)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V				unit
Supply Voltage	V_{DD}		-23 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pdmax	Ta=70°C	0.3	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Range at Ta=25°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		-21	-12	-6.5	V
Input High Level Voltage	V_{IH}	V_{DD}=-6.5 to -21V	-1		0	V
Input Low Level Voltage	V_{IL}	V_{DD}=-8.0 to -21V	V_{DD}		V_{DD}+2	V
		V_{DD}=-6.5 to -8.0V	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-9 to -21V			min	typ	max	unit
Output High Level Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2.5V$	1.5			mA
b & c, a & d	$I_{OH}(2)$	$V_{OH}=V_{SS}-1.0V$	2			mA
1Hz	$I_{OH}(3)$	$V_{OH}=V_{SS}-1.0V$	3			mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-1.0V$	1			mA
Output Leak Current						
ALARM 1 OUT, ALARM 2 OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}$			2	uA

Continued on the next page.

Continued from the preceding page.

			min	typ	max	unit
Input Leak Current						
ACIN	$I_{IH(1)}$	$V_{IH}=V_{SS}$			5	uA
	I_{IL}	$V_{IL}=V_{DD}$	-5			uA
Input Current (Other than AC IN)	$I_{IH(2)}$	$V_{IH}=V_{SS}$	10		200	uA
Input Pin Open Voltage (Other than AC IN)	V_{ILopen}	Pin open	V_{DD}		$V_{DD}+1$	V
Power Failure Detect Voltage	V_{Det}		-6.5	-4.5		V
Current Dissipation	I_{DD}	$V_{DD}=-10V$		6	10	mA
Oscillation Period CR INPUT	T_{osc}	Cl=0.0068uF, Rl=150Kohm, $V_{DD}=-8V$	0.569	0.625	0.681	mA

1. Display

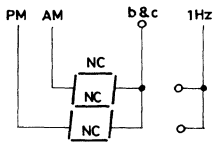
1-1. 4-digit 7-segment static lighting system.

Display font 1 2 3 4 5 6 7 8 9 0

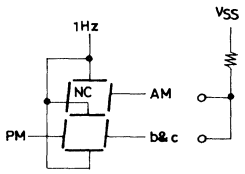
1-2. Display mode

- Time and alarm time display mode (12-hour system) 1:00AM to 12:59PM (10's digit of hours:0 blanking).
  (24-hour system) 0:00 to 23:59 (10's digit of hours:0 blanking).
- Month/date display mode (12-hour system) 1 1 to 12 31(10's digit of hours, 10's digit of minutes: 0 blanking).
  (24-hour system) 1: 1 to 31:12 (10's digit of hours, 10's digit of minutes: 0 blanking).
- Seconds display mode (12-hour system) 0 00 to 9 59 (Digit No.1:Blanking).
  (24-hour system) 0:00 to 9:59 (Digit No.1:Blanking).
- Sleep display mode (12-hour system) 00 to 59 (Digits) No.1 and No.2: Blanking).
  (24-hour system) :00 to 59 (Digits No. 1 and No.2 : Blanking).

1-3. Connection for 10's digit of hours



12-hour system



24-hour system

1-4. 1Hz output

- 24-hour system : Used for segments a, d, g of digit No.1.
- 12-hour system : Real time (hours/minutes) display mode and alarm time display mode —— Flashing at a 1Hz rate.
  Month/date display mode, sleep display mode, seconds display mode —— OFF (Unlighted).

1-5. Month/date display mode

	Digits No.1 and No.2	Digits No.1 and No.2
24-hour system	Date	Month
12-hour system	Month	Date

1-6. Power failure indication

- All ON-state segments flash at a 1Hz rate at all display mode.——Power failure indication.
- Flashing to indicate power failure is released by applying the input to UPPER SET INPUT or LOWER SET INPUT.

1-7. Display during backup operation

- When the count operation is performed (during backup operation) by CR-OSC oscillation frequency with no input applied to 50/60 Hz INPUT, all ON-state segment outputs will be turned OFF.

2. Input Organization

2-1. Logic level

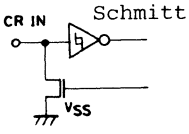
- Logic "L" : V_{DD} level
- Logic "H" : V_{SS} level

2-2. AC INPUT

- With built-in Schmidt circuit, the input impedance is more than 1Mohm.
- The clamp circuit for a voltage being more minus than V_{DD} is built in.

2-3. CR INPUT

- This consists of a Schimdt circuit and an open drain driver.



2-4. Input pins other than above

- Input pins with pull-down resistor.

3. Output Organization

All of segment output, alarm output, and sleep output are of P channel open drain type.

4. Operation Description

4-1. Display mode selection

- The display mode is selected by using SLEEP DISPLAY INPUT, ALARM DISPLAY INPUT, ALARM 2 DISPLAY INPUT, and SECONDS DISPLAY INPUT. The order of priority given to these switch signals is as shown in Table 1.

Table 1. Order of priority given to switch signals

Switch input				Display mode
SLEEP DISPLAY	ALARM 1 DISPLAY	ALARM 2 DISPLAY	SECOND	
H	-	-	-	Sleep display
L	-	H	H	Month/date display
L	H	L	-	Alarm 1 dispaly
L	H	H	L	Alarm 1 dispaly
L	L	H	L	Alarm 2 display
L	L	L	H	Seconds display
L	L	L	L	Real time display

Note : "H" : V_{SS} level is applied to input pin.
"L" : V_{DD} level is applied to input pin.
"-" : V_{SS} level or V_{DD} level is applied to input pin or input pin may be made open.

4-2. Time setting

- Time setting is executed by applying V_{SS} level to UPPER SET INPUT and LOWER SET INPUT.
- When executing setting, no carry occurs from the low-order digit to the high-order digit.
- The operation contents at each display mode are as shown in Table 2.

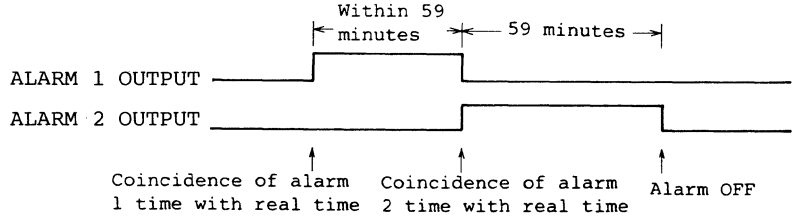
Table 2. Operation contents

Display mode	Setting input	Operation contents
Real time display	UPPER	Minutes advance at a 2Hz rate.
	LOWER	Minutes advance at a 2Hz rate. } No carry to hours occurs.
	BOTH	Minutes advance at a 5Hz rate. } Seconds are cleared to 00.
Alarm 1 display (alarm 2 display)	UPPER	Hours of alarm 1 (alarm 2) advance at a 2Hz rate.
	LOWER	Minutes of alarm 1 (alarm 2) advance at a 2Hz rate. } No carry to hours occurs.
	BOTH	Minutes of alarm 1 (alarm 2) advance at a 5Hz rate. } No carry to hours occurs.
Month/ date display	UPPER	Month (date) advances at a 2Hz rate. } ( ) : 24-hour system. No carry occurs from the low-order digit to the high-order digit.
	LOWER	Date (month) advances at a 2Hz rate. } ( ) : 24-hour system. No carry occurs from the low-order digit to the high-order digit.
	BOTH	Date (month) advances at a 5Hz rate. } ( ) : 24-hour system. No carry occurs from the low-order digit to the high-order digit.
Sleep display	UPPER	No operation.
	LOWER	Minutes of sleep timer subtract at a 2Hz rate.
	BOTH	Minutes of sleep timer subtract at a 5Hz rate.
Seconds display	UPPER	Seconds counter stops running.
	LOWER	Seconds are cleared to 00. Clearing continues until switch is released.
	BOTH	Each counter is reset at follows : Real time —— 12:01AM (For 24-hour system, 0:01) Alarm time —— 12:00AM (For 24-hour system, 0:00) Month/date —— 12 1 (For 24-hour system, 1:12)

Note: BOTH means that V_{SS} level signal is applied by pressing both switches of UPPER SET INPUT and LOWER SET INPUT.

4-3. Alarm operation

1) The 24-hour mode dual alarms of alarm 1 and alarm 2 are built in. The alarm outputs are each made available once in 24 hours. The time contents are displayed, read out, and set as shown in table 1 and Table 2.
2) The alarm 1 time and alarm 2 time can be set independently. When the alarm 1 time (alarm 2 time) coincides with the real time, ALARM 1 OUTPUT (ALARM 2 OUTPUT) will be turned ON (H level) and will be turned OFF (L level) automatically 59 minutes later. When the alarm 2 time coincides with the real time within 59 minutes after the alarm 1 time coincided with the real time. ALARM 2 OUTPUT will be turned ON and will be turned OFF automatically 59 minutes after the time with which the alarm 2 time coincided.



3) When the alarm 1 time and alarm 2 time, which are set at the same time, coincide with the real simultaneously, ALRAM 1 OUTPUT only will be turned ON and ALARM 2 OUTPUT will not be turned ON.

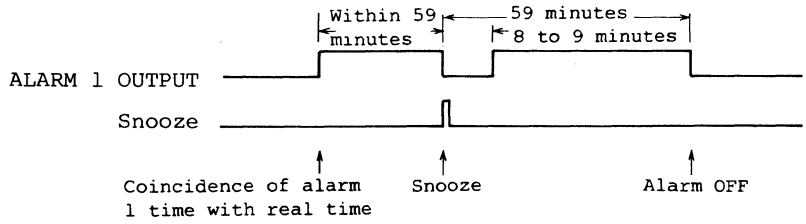
4) ALARM OUTPUT release
When the real time coincides with the alarm 1 time (alarm 2 time) and ALARM 1 OUTPUT (ALARM 2 OUTPUT) is turned ON, ALARM 1 OUTPUT (ALARM 2 OUTPUT) can be turned OFF by applying H level to ALARM 1 OFF INPUT (ALARM 2 OFF INPUT).

5) Alarm operation inhibit
The following alarm operation is aviable corresponding to the level setting of ALARM 1 OFF INPUT and ALARM 2 OFF INPUT.

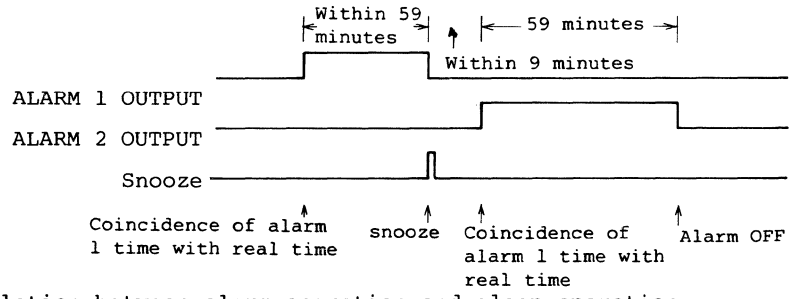
ALARM 1 OFF INPUT	ALARM 2 OFF INPUT	Operation of alarm 1	Operation of alarm 2
L	L	o	o
H	L	x	o
L	H	o	x
H	H	x	x

"L" : V_{DD} level or open.
"H" : V_{SS} level.
"o" : Normal operation.
"x" : Operation inhibit. Even if the alarm time coincides with the real time, ALRM OUTPUT will not be turned ON.

6) Snooze operation
If "H" level is applied to SNOOZE INPUT while ALARM OUTPUT is turned ON, ALARM OUTPUT will be turned OFF temporarity and will be turned ON 8 to 9 minutes later. The snooze operation is available as often as you like.

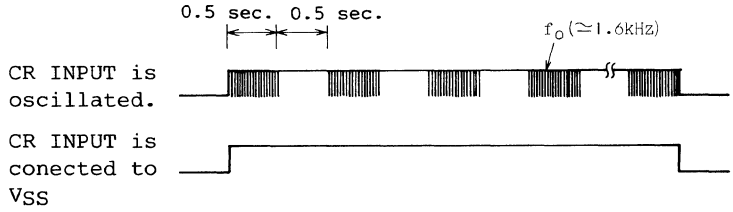


When the alarm 2 time coincides with the real time during the snooze operation, the snooze operation will be released at this point of time and ALARM 2 OUTPUT will be turned ON.



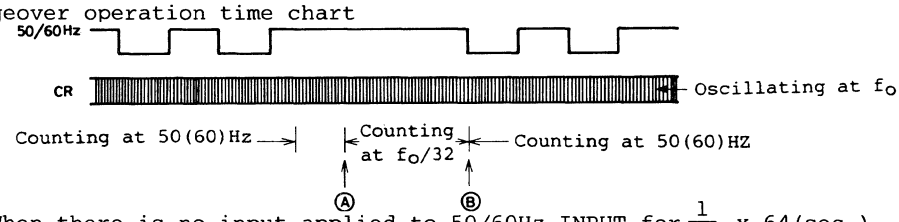
7) Relation between alarm operation and sleep operation
- SLEEP OUTPUT is not turned ON while ALARM OUTPUT is turned ON (including the period of snooze operation).
- Contrary to this, even if the alarm time coincides with the real time while SLEEP OUTPUT is turned ON, ALARM OUTPUT will not be turned ON.

8) ALARM OUTPUT waveform
For ALARM 1 OUTPUT, DC output signal is provided. For ALARM 2 OUTPUT, either of the following two output signals is selectable according as CR INPUT is oscillated or not.



4-4. Sleep operation
1) If "H" level is applied to SLEEP DISPLAY INPUT when all of ALARM 1 OUTPUT, ALARM 2 OUTPUT, and SLEEP OUTPUT are turned OFF, the sleep timer will be set to 59 minutes and SLEEP OUTPUT will be turned ON. When the sleep timer reaches 0 minutes after the lapes of 59 minutes, SLEEP OUTPUT will be turned OFF.
2) If "H" level is applied to SLEEP DISPLAY INPUT while SLEEP OUTPUT is turned ON, the sleep timer will not be set to 59 minutes, but will display the remaining period of time.
3) The sleep timer can be advanced fast as shown in Table 2.
4) Sleep timer release
If "H" level is applied to SNOOZE INPUT at other display modes than sleep display mode while SLEEP OUTPUT is turned ON, SLEEP OUTPUT will be turned OFF. If "H" level is applied to SNOOZE INPUT at the sleep display mode, the sleep timer will be preset to 59 minutes. (A simple touch of the switch permits 59 minutes to be set.)
5) Relation between alarm operation and sleep operation
Refer to 4-3-7)

4-5. Backup operation
1) $|V_{DD}|$ min. for the normal operation of LSI inside is 6.5V.
2) For the backup operation during power failure, the following actions are required.
(1) A voltage of more than 6.5V must be applied across V_{DD} and V_{SS}.
(2) CR INPUT must be oscillated with a frequency 32 times as high as 50Hz (or 60Hz).
In case of power failure, these (1) and (2) cause the internal reference clock to be changed-over automatically to the oscillation frequency at CR INPUT.
3) When restored to normal from power failure, the reference clock will be changed-over automatically to 50/60Hz.
4) Changeover operation time chart



Ⓐ : When there is no input applied to 50/60Hz INPUT for $\frac{1}{f_o}$ x 64(sec.), the reference frequency will be changed-over from 50/60Hz to $f_o/32$Hz.
Ⓑ : The momemt 50/60Hz INPUT receives the input, the reference frequency will be changed-over from fo/32 to 50/60Hz.

5) Rejection of interference noise to radio
By stopping oscillation at CR INPUT during application of AC power supply and starting oscillation simultaneously with power failure, the interference noise to radio due to oscillation at CR INPUT can be rejected. (Refer to Application Circuit.)

6) Segment output during backup operation
During the period from Ⓐ to Ⓑ shown in the time chart in 4), all segment outputs are turned OFF automatically.

4-6. Commercial frequency and its selection

1) The commercial frequency is inputted from 50/60Hz INPUT. This pin contains a Schmidt circuit to prevent malfunction due to external noise. It is necessary to use this pin in conjunction with a CR filter having 100 to 1000Kohm and 0.01uF to prevent LSI breakdown due to high-voltage impulse, etc. from the commercial power supply.

2) 50Hz or 60Hz is selected by use of 50/60Hz SELECT.
50Hz : 50/60Hz SELECT is set at "H" level (V_{SS}).
60Hz : 50/60Hz SELECT is set at "L" level (V_{DD}) or is made open.

4-7. 12/24-hour system selection

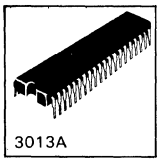
The display content is selected as follows by use of 24/12 HRS SELECT.

24/12 HRS SELECT	Real time and alarm time	Month/date	
		Digits No.1 and No.2	Digits No.1 and No.2
"H" level (V_{SS})	24-hour system	Date	Month
"L" level (V_{DD}) or open	12-hour system	Month	Date

5. Functional Table of Rank Products

Rank	Display tube		Remarks
	LED (red)	Fluorescent display tube	
LM8365D	o		
LM8365DH		o	
LM8365N	o	o	
LM8365S	o	o	For use in industrial applications

LM8368



P MOS LSI

Digital Clock Alarm

Ⓔ 1496A

Use

- Alarm clock
- Clock radio
- Timer for home appliances
- Display of time elapsed

Functions

- Real time display
- Alarm with snooze function
- Sleep timer (59 minutes max.)

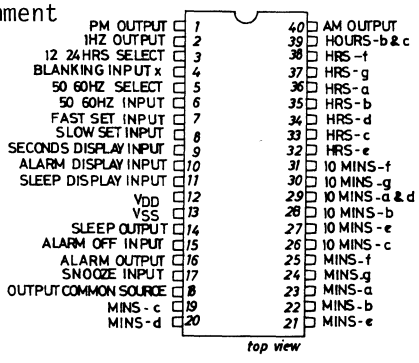
Features

- LM8368D: LED (red) use
- LM8368DH: FLT use
- LM8368DG: LED (crystal green) use
- Battery backup is avaiable for all Type Nos.
- Single-chip P-Channel ED MOS LSI
- Possible to direct drive an LED (5mA or more, red LED): LM8368D
- Possible to direct drive a fluorescent display tube (light-up voltage 21V or less): LM8368DH
- Wide operating voltage range (-6.5 to -16V) : LM8368D
- 50Hz or 60Hz is usable as reference frequency.
- Two selections of display mode (AM/PM 12-hour display mode or 24-hour display mode)
- 24-hour alarm function
- Repeatedly usable snooze function
- Presettable 59-minute down counter (sleep timer)
- Automatic decrement function of sleep timer
- Power failure indicating function (all digits flashing)
- Blanking pin for blanking out display (connectable in parallel with other LSI of P-channel open drain output type)
- Clock input noise eliminator

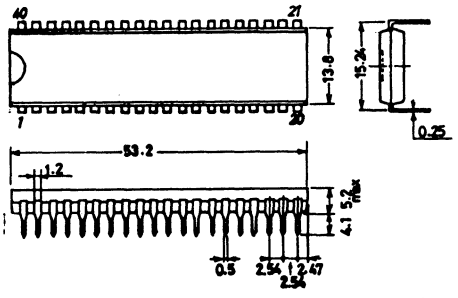
Related Type Nos.

- LM8361, LM8362, LM8363, LM8364, LM8365, LM8460, LM8560

Pin Assignment

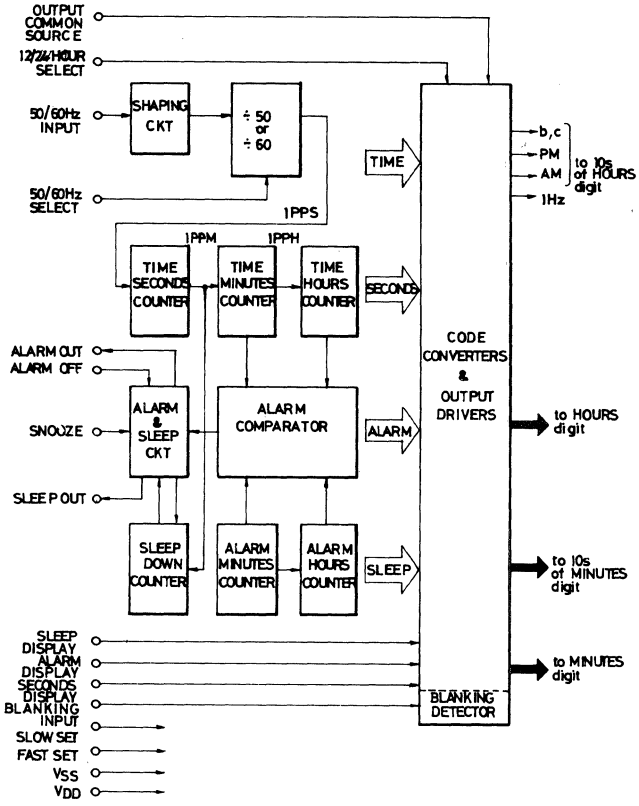


Case Outline 3013A-D40IC (unit:mm)



SANYO: DIP40

Equivalent Circuit Block Diagram



Main Specifications for LM8368D (red LED)

Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{DD}		-18 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max	Ta=70°C	0.9	W
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		-16	-12	-6.5	V
Input "H"-Level Voltage	V_{IH}		-1		0	V
Input "L"-Level Voltage	V_{IL}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
		$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-12V±2V

			min	typ	max	unit
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2V$	0.5			mA
b&c(12H mode), a&d, 1Hz	$I_{OH}(2)$	$V_{OH}=V_{SS}-2.5V$	10			mA
PM(24H mode)	$I_{OH}(3)$	$V_{OH}=V_{SS}-2.5V$	20			mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-2.5V$	5		Note 1	mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}+1.8V$			50	uA
Current Dissipation	I_{DD}	V_{DD}=-12V		3	5.5	mA

Continued from the preceding page.

Note 1: 11mA max. is allowed in the range where the power dissipation is 900mW and 1.2W at Ta=70°C and 25°C respectively.

Main Specifications for LM8368DH (FLT)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}		-23 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max.	Ta=70°C	0.2	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		-21		-6.5	V
Input "H"-Level Voltage	V_{IH}		-1		0	V
Input "L"-Level Voltage	V_{IL}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
		$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=-10V to-21V

			min	typ	max	unit
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2V$	0.5			mA
b&c(12H mode), a&d, 1Hz	$I_{OH}(2)$	$V_{OH}=V_{SS}-1.0V$	2			mA
PM(24H mode)	$I_{OH}(3)$	$V_{OH}=V_{SS}-1.0V$	4			mA
Other than above	$I_{OH}(4)$	$V_{OH}=V_{SS}-1.0V$	1			mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}$			5	uA
Current Dissipation	I_{DD}	V_{DD}=-12V		3	5.5	mA

Main Specifications for LM8368DG (crystal green LED)

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0

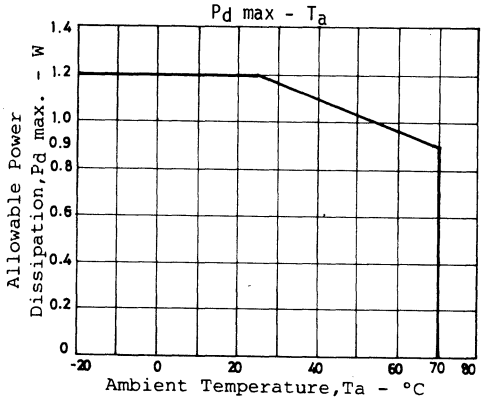
				unit
Maximum Supply Voltage	V_{DD}		-22 to +0.3	V
Input Voltage	V_{IN}		V_{DD}-0.3 to +0.3	V
Output Voltage	V_{OUT}	Output pin OFF	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd max.	Ta=25°C	1.2	W
		Ta=70°C	0.9	W
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

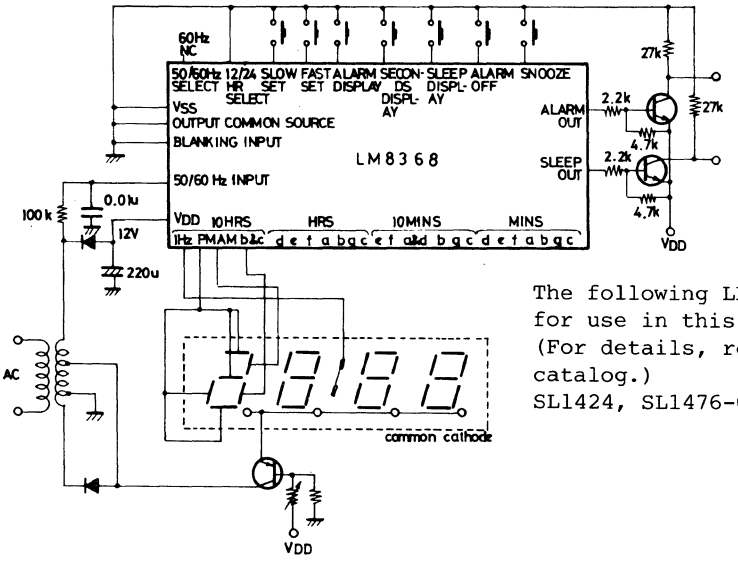
			min	typ	max	unit
Supply Voltage	V_{DD}	Display drive mode	-20	-18	-16	V
		Battery backup mode	-20		-6.5	V
Input "H"-Level Voltage	V_{IH}		-1		0	V
Input "L"-Level Voltage	V_{IL}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
		$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V

Electrical Characteristics at Ta=25°C,

			min	typ	max	unit
V_{SS}=0V, V_{DD}=-18 to ±2V						
Output "H"-Level Current						
ALARM OUT, SLEEP OUT	$I_{OH}(1)$	$V_{OH}=V_{SS}-2V$	0.5			mA
b&c(12H mode), a&d, 1Hz	$I_{OH}(2)$	V_{DD}=-16V, $V_{OH}=V_{SS}-2.5V$	16			mA
PM(24H mode)	$I_{OH}(3)$	V_{DD}=-16V, $V_{OH}=V_{SS}-2.5V$	32			mA
Other than above	$I_{OH}(4)$	V_{DD}=-16V, $V_{OH}=V_{SS}-2.5V$	8			mA
Output Leakage Current						
ALARM OUT, SLEEP OUT	$I_{OL}(1)$	$V_{OL}=V_{DD}$			5	uA
Other than above	$I_{OL}(2)$	$V_{OL}=V_{DD}+1.8V$			50	uA
Current Dissipation	I_{DD}	V_{DD}=-18V		3	5.5	mA

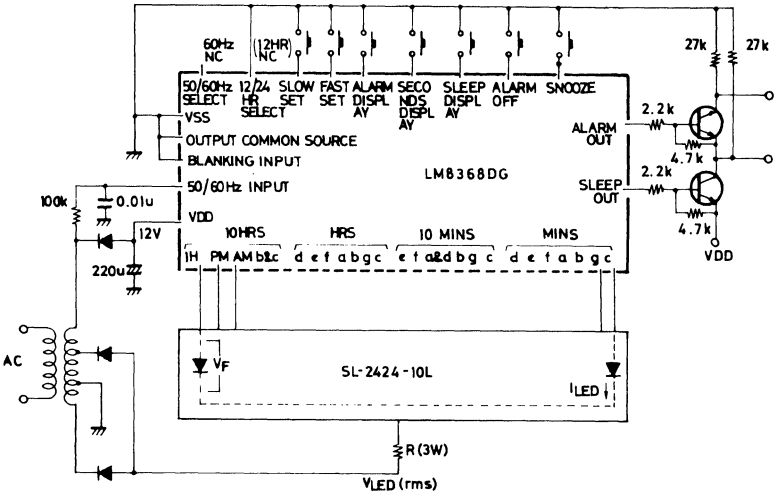


Sample Application Circuit



The following LED's are available for use in this application.
(For details, refer to each separate catalog.)
SL1424, SL1476-04, SL1478, SL1494

Sample Application Circuit of LM8368DG

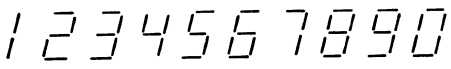


V_{DD}=18V±2V
I_{LED}=8mA min(SL-2424-10L)
Ta max=55℃

R(Ω)	V_{LED}(V)
22±5%	9.7±1
24±5%	10.1±1
27±5%	10.7±1
30±5%	11.2±1
33±5%	11.7±1

The table shown left is for V_F=2.0.
Example: V_{LED}=11.7±0.8V
at V_F=2.0V±0.2V, R=33ohm±5%

1. Display
   1-1. Real time, alarm time, sleep time are displayed in the following display font by means of 4-digit 7-segment LED or fluorescent display tube.

Display font 

   1-2. Lighting system: Static lighing
   1-3. Display range
   - Time and alarm time display mode (12-hour display mode)
     AM1:00 to PM12:59 (highest-order digit: 0 blanking)
   - Time and alarm display mode (24-hour display mode)
     0:00 to 23:59 (highest-order digit: 0 blanking)
   - Seconds display mode
     0:00 to 9:59 (highest-order digit: blanking)
   - Sleep time display mode
     00 to 59 (highest-order and 2nd highest-order digits: blanking)

2. Input signal
   2-1. Switch signal
   - Logic "L": V_{DD}(or pin open)
   - Logic "H": V_{SS}

   2-2. 50/60Hz input signal
   - Sine wave, square wave, triangular wave, etc. of V_{DD}-V_{SS}(p-p)
   - Impedance: 1Mohm or greater

3. Output configuration
   3-1. Segment output: P-channel open drain type
   3-2. Drive output (ALARM OUT, SLEEP OUT): P-channel open drain type

4. Operation description

4-1. 50/60Hz input

This signal is used to drive the time counter. Commercial frequency 50/60Hz is put through the Schmitt circuit to be free from noise. A resistor (100 to 1000Kohm) must be connected in series with this input pin to avoid being damaged by high-voltage noise included in the commercial power supply.

4-2. 50/60Hz select input

The program counter contains a 50Hz/60Hz select circuit to provide a standard frequency of 1 pulse per second. When this pin is set at "L" or open, 60Hz use is available; when at "H", 50Hz use is available.

4-3. Display select mode

A) Alarm display input---- Setting this pin to "H" causes alarm time to be displayed.

B) Seconds display input-- Setting this pin to "H" causes the first digit of seconds and minutes to be displayed.

C) Sleep display input---- Setting this pin to "H" causes sleep time to be displayed.

D) Real time display------ When none of inputs in A), B), and C) are selected, or all of them are at "L", real time is displayed.

E) Priority order of display ----- Shown below is the priority order in case where a plurality of display modes are selected.

Alarm display input	Seconds display input	Sleep display input	Display mode
L	L	L	Real time display
H	L	L	Alarm display
L	H	L	Seconds display
H	H	L	Alarm display
L	L	H	Sleep display
H	L	H	Sleep display
L	H	H	Sleep display
H	H	H	Sleep display

Note: "H": Input pin --- V_{SS} level
"L": Input pin --- V_{DD} level (or open)
If the sleep display mode is kept on, the contents of the sleep timer count down at a 2Hz rate.

4-4. Time setting input

Two pins are used for time setting. Setting these pins to "H" causes following operations to be performed; setting to "L" (open) causes the operations to be stopped. Setting both pins (FAST and SLOW) to "H" simultaneously causes alarm time and real time to be initialized when in the alarm display mode and seconds display mode respectively.

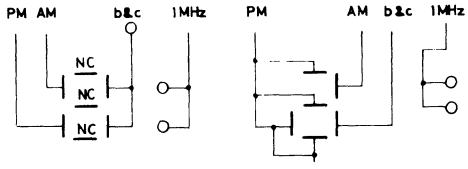
Display mode	Time setting input pin	Function
Real time display	FAST	Minutes contents advance at a 60Hz* rate.
	SLOW	Minutes contents advance at a 2Hz rate.
	BOTH	Minutes contents advance at a 60Hz* rate.
Alarm display	FAST	Minutes contents advance at a 60Hz* rate.
	SLOW	Minutes contents advance at a 2Hz rate.
	BOTH	AM 12:00 is set when in the 12-hour display mode. 0:00 is set when in the 24-hour display mode.
Seconds display	FAST SLOW BOTH	00 second is set. No carry to minutes is generated. Seconds counting is stopped (held). (When in the 12-hour display mode) the real time counter is set to AM 12:00. (When in the 24-hour display mode) the real time counter is set to 0:00.

Note: *: For 50Hz use, 50Hz shall apply.
BOTH means that 2 input pins of FAST and SLOW are set to "H".
When in the sleep display mode, the contents of the sleep counter count down at a 2Hz rate.

4-5. Blanking control input
This pin is connected to the Schmitt circuit. Normally, V_{SS}("H") is applied to this pin. If set to "L", all display drivers enter the high impedance (off) state. No pull-down resistor is contained.

4-6. Output common source pin
All segment outputs are of open drain type. This pin is the common of individual source electrodes. In fluorescent display applications this pin can be used for brightness control.

4-7. 12/24-hour display mode select input
Setting this pin to "L" (open) causes the 12-hour display mode to be entered; setting to "H" causes the 24-hour display mode to be entered. The digit in 10's place is composed of 3 pins (b&c, AM, PM) as follows:



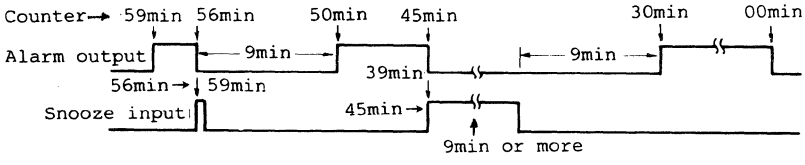
Connection for 12-hour display mode

Connection for 24-hour display mode

4-8. Alarm operation and output
When the alarm counter contents (alarm set time) reach the time counter contents (real time), the alarm output is turned ON. That is, the alarm output is set to "H" and turned OFF 59 minutes later. The alarm output can be turned OFF within 59 minutes by setting the ALARM OFF INPUT pin to "H". The alarm output is turned OFF temporarily by setting the SNOOZE INPUT pin to "H".

4-9. Snooze input
By connecting this pin to V_{SS}("H") temporarily while the alarm output is at "H", the alarm output is turned OFF ("L") and turned ON ("H") again 8 to 9 minutes later. This input pin contains a pull-down resistor. The snooze function can be used repeatedly as long as the alarm output is at "H".
Note: When using the snooze pin, the following must be noted.

Time chart



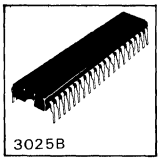
If the snooze input is set to "H" when the remaining alarm time is 59 to 56 minutes (49 to 46, ---), the remaining alarm time (including the snooze time) becomes 59 minutes (49, ---). If the snooze input is set at "H" when the remaining alarm time is 55 to 50 minutes (45 to 40, ---, 5 to 1), the remaining alarm time becomes 49 minutes (39, ---, 59).

4-10. Alarm OFF input
The alarm output is kept ON for 59 minutes. However, the alarm output can be turned OFF ("L") as soon as this pin is set to "H" momentarily during the period of 59 minutes. If the ALARM OFF input is kept at "H", the alarm output is not turned ON even when the alarm set time is reached. This pin contains a pull-down resistor.

4-11. Sleep timer and sleep output

The sleep output serves to keep the radio, etc. turned ON for any period of time up to 59 minutes. By selecting the sleep display mode (see 4-4.) , any desired period of time can be set. This sleep counter is a down counter whose output is turned OFF ("L") when the counter contents reach 00 minutes. When the sleep counter counts down to 00 minute, it stops counting and the sleep output is kept OFF until a desired period of time is set next. If the SNOOZE pin is set to "H" in other mode than the sleep display mode when the sleep output is at "H", the sleep timer output turns to "L". If the SLEEP DISPLAY input pin is kept at "H", the sleep timer contents count down at a 2Hz rate.

LM8460



P-MOS LSI

Alarm Clock

Ⓔ 1604

Functions

- Radio control circuit-contained clock with alarm
- Time setting with stem switch or UP/DOWN button
- Stepwise alarm with snooze
- 5-step dimmer control
- Sleep timer

Features

(1) One-touch control function (Easy Setting)
- Time setting with stem switch (or UP/DOWN button)
- One touch permits radio to be turned ON/OFF with logic control.
- 5-step dimmer control with one button

(2) Stepwise alarm function
- 6-step alarm tone output (stepwise alarm)
- On-chip control circuit to select radio sound or stepwise alarm tone or radio sound + stepwise alarm tone as alarm tone
- 10-minute snooze function (2-step snooze in the radio sound + stepwise alarm tone mode)

(3) Power failure backup function
- On-chip CR oscillator for timekeeping in the backup mode
- Key entry inhibiting function to prevent misoperation in the backup mode (except OFF input)

(4) LED or FLT direct drive capability

General Description of Specifications

(1) Display function
- 4-digit static display (hours-minutes or seconds display)
- Real time/alarm time/ sleep timer time display selectable
- Two selections of time format: 12-hour basis (AM/PM) or 24-hour basis
- Alarm-ON, sleep timer-ON, radio-ON display output
- Power failure indicating function (all digits flahing)
- 5-step dimmer control with one button
- FLT direct drive capability (lighting voltage 23V or less)

(2) Alarm function
- 24-hour alarm
  Delivers radio control output or alarm tone at the alarm set time according to the alarm mode
- 6-step alarm tone output (changes in 6 steps every 1 minute)
  1 tone every 2 seconds ⟶ 2 tones every 2 seconds ⟶ 2 tones every 1 second ⟶ 4 tones every 1 second ⟶ 4 tones every 0.5 second ⟶ continuous tone.

- 3 alarm modes selectable
  Radio sound/6-step alarm tone/radio sound + 6-step alarm tone (6-step alarm tone 10 minute after radio sound)
- Repeatedly usable 10-minute snooze function
  2-step snooze in the radio sound + stepwise alarm tone mode

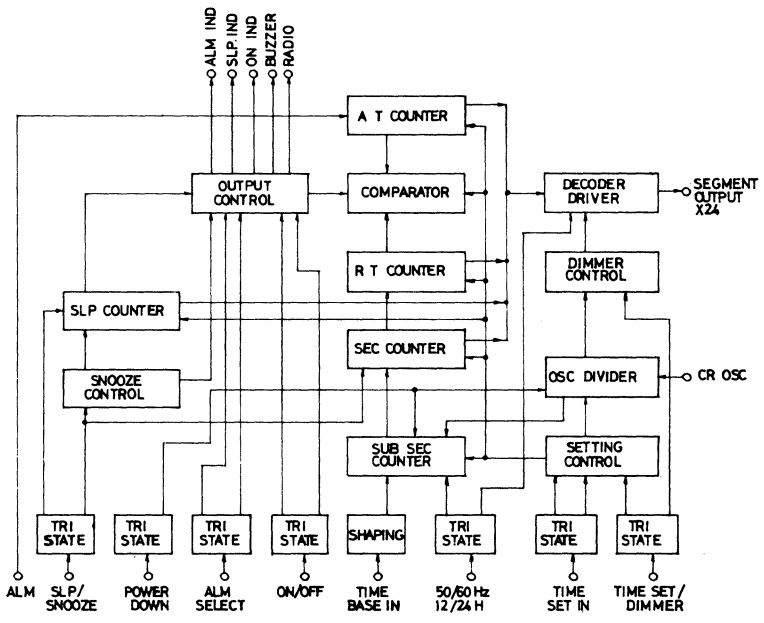
(3) Time setting method
- Time setting with stem switch or UP/DOWN button (real time, alarm time, sleep timer time)

(4) Sleep timer function
- Settable up to 59 minutes in increments of 1 minute

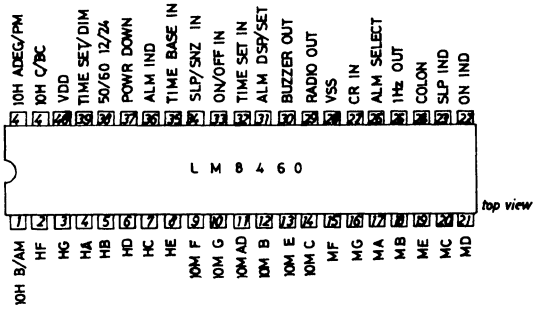
(5) Supplementary function
Fewer parts required for carry output of hours, minutes, seconds

(6) Reference frequency input
- AC 50/60Hz or CR OSC frequency (backup mode)

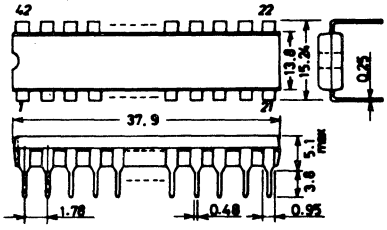
Equivalent Circuit Block Diagram



Pin Assigment

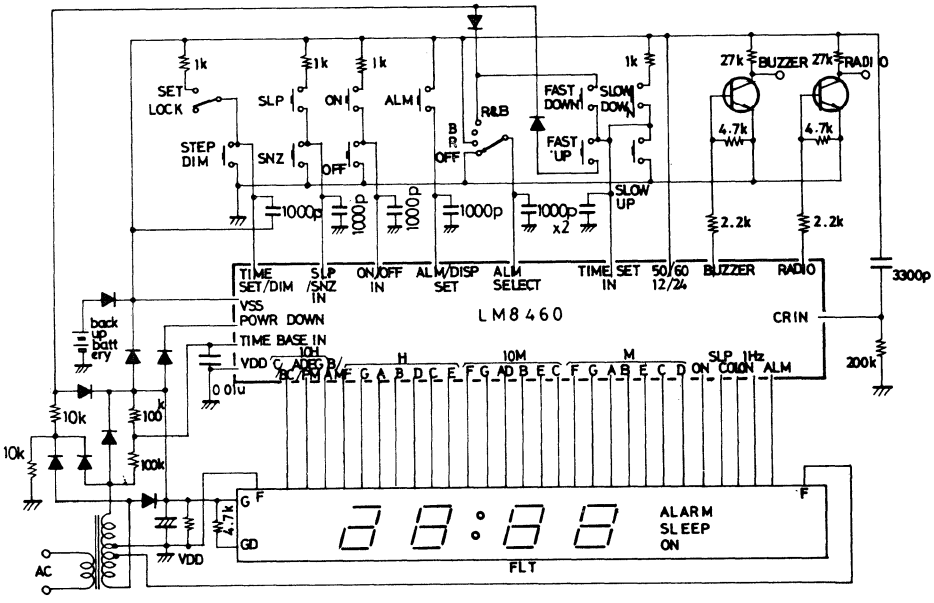


Case Outline 3025B-D42SIC
(unit:mm)



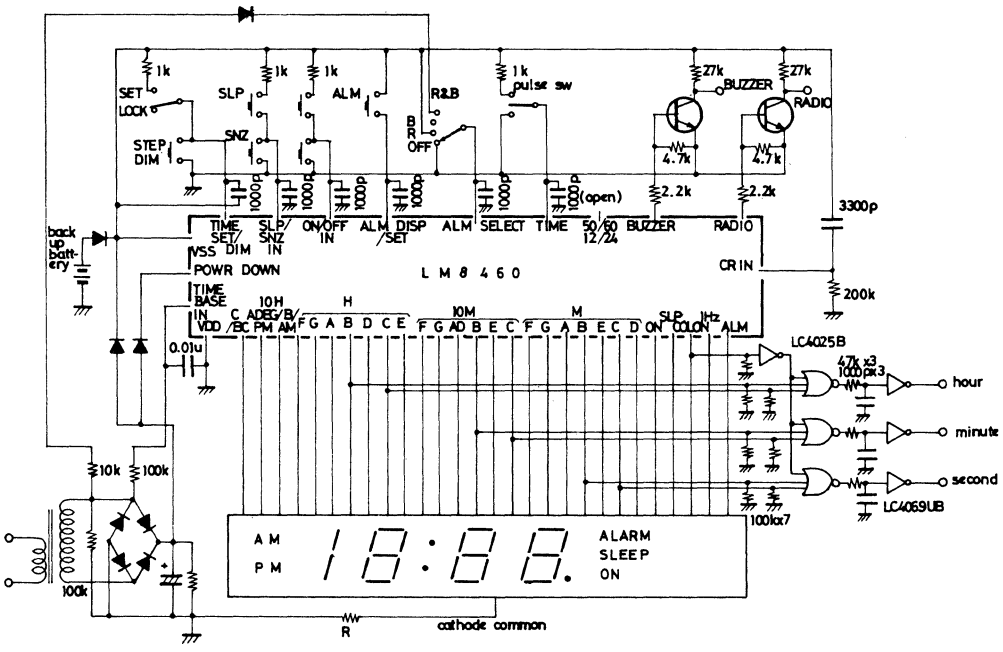
SANYO: DIP42S

Sample Application Circuit (1)
Fluorescent display tube (24-hour basis, 50Hz, fast set 100/200Hz input)



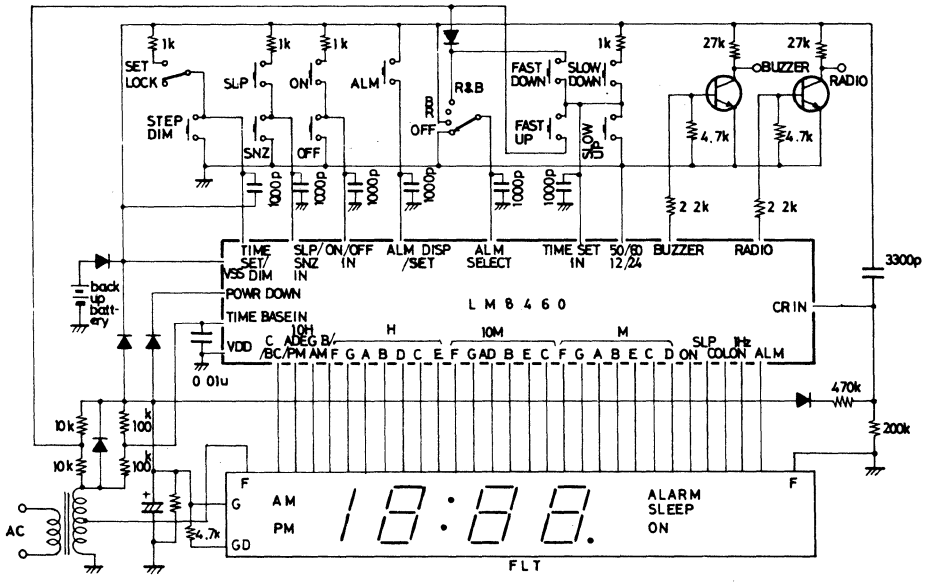
Sample Application Circuit (2)

LED display, with carry output (12-hour basis, 60Hz)



Sample Application Circuit (3)

Fluorescent display tube (12-hour basis, 50Hz, fast set 50/60Hz input)



[Main Characteristics for Fluorescent Display Tube Use]

Absolute Maximum Ratings/Ta=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DDmax}		-17.0 to +0.3	V
Maximum Input Voltage	V_{INmax}		V_{DD}-0.3 to +0.3	V
Maximum Output Voltage	V_{OUTmax}	output off	-23.0 to +0.3	V
Allowable Power Dissipation	Pdmax	Ta=70°C	0.2	W
Operating Temperature	Tstg		-30 to +70	°C
Storage Temperature	Topg		-55 to +125	°C

Allowable Operating Ranges/Ta=25°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		-7.5		-14	V
50/60Hz CR Input						
"H"-Level Input Voltage	V_{IH1}		-1		0	V
"L"-Level Input Voltage	V_{IL1}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
	V_{IL2}	$V_{DD} > -8V$, $V_{DD} \leq -7.5V$	V_{DD}		V_{DD}+1	V
Tri-state Input						
"H"-Level Input Voltage	V_{IH2}		-0.7		0	V
"M"-Level Input Voltage	V_{IM}		$\frac{1}{2}V_{DD}$-0.7		$\frac{1}{2}V_{DD}$+0.7	V
"L"-Level Input Voltage	V_{IL3}		V_{DD}		V_{DD}+1	V
Other Input						
"H"-Level Input Voltage	V_{IH3}		-1.5		0	V
"L"-Level Input Voltage	V_{IL4}		V_{DD}		V_{DD}+2	V

Electrical Characteristics/Ta=25°C, V_{SS}=0V, V_{DD}=-12V			min	typ	max	unit
Current Dissipation	I_{CC}	Input open, Output: No load		4	7	mA
Power Failure Detect Voltage		Output: No load	-6.5	-5.0		V
50/60Hz Input						
Operating Frequency			DC		2K	Hz
"H"-Level Input Current	I_{IH1}	$V_{IH}=V_{SS}$			5	uA
"L"-Level Input Current	I_{IL1}	$V_{IL}=V_{DD}$			-5	uA
CR Input						
"H"-Level Input Current	I_{IH2}	$V_{IH}=V_{SS}$			5	uA
"L"-Level Input Current	I_{IL2}	$V_{IL}=V_{DD}$, CR-OSC off			-5	uA
ALM DSP Input						
"H"-Level Input Current	I_{IH3}	$V_{IH}=V_{SS}$	10		200	uA
Voltage with Input Pin Open		V_{IN}=open	V_{DD}		V_{DD}+1	V
Pull-down Resistance				300		kohm
Inputs Except Above (tri-state input)						
"H"-Level Input Current	I_{IH4}	$V_{IH}=V_{SS}$	15		60	uA
"L"-Level Input Current	I_{IL3}	$V_{IL}=V_{DD}$	-12		-50	uA
Pull-down Resistance		V_I=1/2V_{DD}		1.0		Mohm
Pull-up Resistance		V_I=1/2V_{DD}		0.8		Mohm
Voltage with Input Pin Open		V_I=open	$\frac{1}{2}V_{DD}$-0.5	$\frac{1}{2}V_{DD}$+0.5		V
ADEG/PM Segment Output (pin 42)						
"H"-Level Output Current	I_{OH1}	$V_{OH}=V_{SS}$-1.0V, Buffer size: Large	4			mA
"L"-Level Output Current	I_{OL1}	V_{OL}=-23V, Buffer size: Large			2	uA
C/CB 1Hz·Colon Segment Output						
"H"-Level Output Current	I_{OH2}	$V_{OH}=V_{SS}$-1.0V, Buffer size: Large	2			mA
"L"-Level Output Current	I_{OL2}	V_{OL}=-23V, Buffer size: Large			2	uA
Segment Output except Above						
"H"-Level Output Current	I_{OH3}	$V_{OH}=V_{SS}$-1.0V	1			mA
"L"-Level Output Current	I_{OL3}	V_{OL}=-23V			2	uA
Output for Radio/Buzzer						
"H"-Level Output Current	I_{OH4}	$V_{OH}=V_{SS}$-2.5V	2			mA
"L"-Level Output Current	I_{OL4}	$V_{OL}=V_{DD}$			2	uA
CR Oscillation						
Stability		V_{DD}=-9V±10%			±10	%
Accuracy		V_{DD}=-9V			±10	%
Frequency		C=3300pF, R=200Kohm		2.4		kHz

[Main Characteristics for LED Use]

Absolute Maximum Ratings/Ta=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DDmax}		-17.0 to +0.3	V
Maximum Input Voltage	V_{INmax}		V_{DD}-0.3 to +0.3	V
Maximum Output Voltage	V_{OUTmax}	Output off	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	Pd_{max}	Ta=70°C	0.9	W
Operation Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

Allowable Operating Ranges/Ta=25°C, V_{SS}=0V			min	typ	max	unit
Supply Voltage	V_{DD}		-7.5		-14	V
50/60Hz CR Input						
"H"-Level Input Voltage	V_{IH1}		-1		0	V
"L"-Level Input Voltage	V_{IL1}	$V_{DD} \leq -8V$	V_{DD}		V_{DD}+2	V
	V_{IL2}	$V_{DD} > -8V$	V_{DD}		V_{DD}+1	V
Tri-state Input		$V_{DD} \leq -7.5V$				
"H"-Level Input Voltage	V_{IH2}		-0.7		0	V
"M"-Level Input Voltage	V_{IM}		$\frac{1}{2}V_{DD}$-0.7		$\frac{1}{2}V_{DD}$+0.7	V
"L"-Level Input Voltage	V_{IL3}		V_{DD}		V_{DD}+1	V
Other Input						
"H"-Level Input Voltage	V_{IH3}		-1.5		0	V
"L"-Level Input Voltage	V_{IL4}		V_{DD}		V_{DD}+2	V

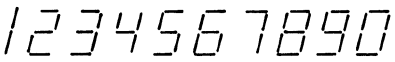
Electrical Characteristics/Ta=25°C, V_{SS}=0V, V_{DD}=-12V			min	typ	max	unit
Current Dissipation	I_{CC}	Input open, Output: No load		4	7	mA
Power Failure Detect Voltage		Output: No load	-6.5	-5.0		V
50/60Hz Input						
Operating Frequency			DC		2K	Hz
"H"-Level Input Current		$V_{IH}=V_{SS}$			5	uA
"L"-Level Input Current		$V_{IL}=V_{DD}$			-5	uA
Cr Input						
"H"-Level Input Current	I_{IH2}	$V_{IH}=V_{SS}$			5	uA
"L"-Level Input Current	I_{IL2}	$V_{IL}=V_{DD}$, CR-OSC off			-5	uA
ALM/DSP Input						
"H"-Level Input Current	I_{IH3}	$V_{IH}=V_{SS}$	10		200	uA
Voltage with Input Pin Open		V_{IN}=open	V_{DD}		V_{DD}+1	V
Pull-Down Resistance				300		kohm
Inputs Except Above (tri-state input)						
"H"-Level Input Current	I_{IH4}	$V_{IH}=V_{SS}$	15		60	uA
"L"-Level Input Current	I_{IL3}	$V_{IL}=V_{DD}$	-12		-50	uA
Pull-down Resistance		$V_I=1/2V_{DD}$		1.0		Mohm
Pull-up Resistance		$V_I=1/2V_{DD}$		0.8		Mohm
Voltage with Input Pin Open		V_I=open	$\frac{1}{2}V_{DD}$-0.5		$\frac{1}{2}V_{DD}$+0.5	V
ADEG/PM Segment Output (pin 42)						
"H"-Level Output Current	I_{OH1}	$V_{OH}=V_{SS}$-2.5V, {Buffer size:Large}	20			mA
"L"-Level Output Current	I_{OL1}	$V_{OL}=V_{DD}$, {Buffer size:Large}			5	uA
C/BC 1Hz·Colon Segment Output						
"H"-Level Output Current	I_{OH2}	$V_{OH}=V_{SS}$-2.5V, {Buffer size:Large}	10			mA
"L"-Level Output Current	I_{OL2}	$V_{OL}=V_{DD}$, {Buffer size:Large}			5	uA
Segment Output except Above						
"H"-Level Output Current	I_{OH3}	$V_{OH}=V_{SS}$-2.5V	5			mA
"L"-Level Output Current	I_{OL3}	$V_{OL}=V_{DD}$			5	uA
Output for Radio/Buzzer						
"H"-Level Output Current	I_{OH4}	$V_{OH}=V_{SS}$-2.5V	2			mA
"L"-Level Output Current	I_{OL4}	$V_{OL}=V_{DD}$			2	uA
CR Oscillation						
Stability		V_{DD}=-9V±10%			±10	%
Accuracy		V_{DD}=-9V			±10	%
Frequency		C=3300pF, R=200Kohm		2.4		kHz

Display

(1) Display font

The use of a 4-digit 7-segment LED, fluorescent display tube displays real time, alarm time, sleep time in the display font shown below.

Display font



(2) Lighting system

Static lighting

(3) Display range

- Time and alarm time display mode (12-hour basis)
  AM1:00 to PM12:59 (highest-order digit: 0 blanking)
- Time and alarm time display mode (24-hour basis)
  0:00 to 23:59 (highest-order digit: 0 blanking)
- Seconds display mode
  0:00 to 9:59 (highest-order digit (highest-order digit: blanking)
- Sleep time display mode
  0:00 to 0:59 (highest-order digit: blanking)

(4) Flashing at the power failure mode

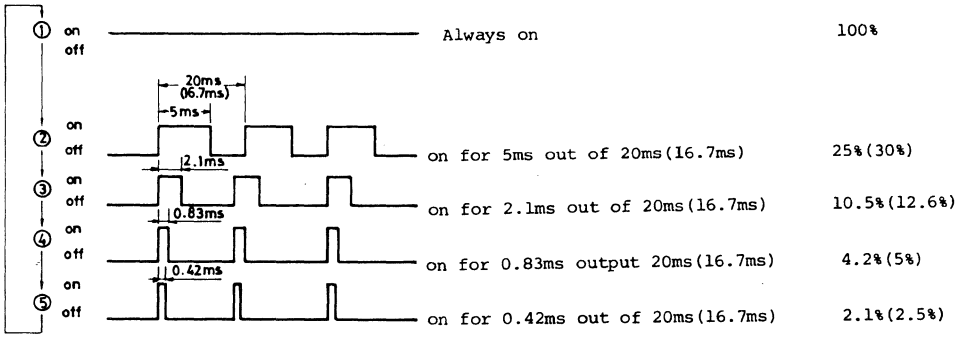
- All segments lighted flash at a 1Hz rate at all the display modes.
- Flashing at the power failure mode is released by using the TIME SET, ALM SET, or SLEEP SET. (Including the lock mode also)

(5) Display at the backup operation mode

When the POWER DOWN pin is open or set to 1/2 | V_{DD}-V_{SS}|, counting is performed based on the oscillation frequency of the CR oscillator and all the display segment outputs are turned OFF. (Blanking mode) However, the blanking mode is released for 10ms (8.3ms) after a carry from seconds to minutes occurs. The value in ( ) is for 60Hz use.

(6) Dimmer function

The application of V_{DD} level to the TIME SET/DIM pin makes it possible to change the brightness of all the segments lighted (including indicator, colon) in 5 steps as shown below.



(Note) ( ): 60Hz use, other than ( ): 50Hz use

Input configuration

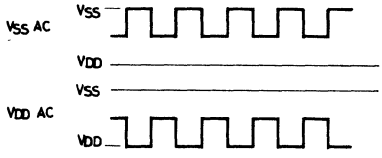
(1) Switch signal

- ALM DSP/SET pin
- Logic "L": V_{DD} (or pin open)
  Logic "H": V_{SS}
- Switches other than above (tri-state input)
  "L": V_{DD}
  "M": $1/2|V_{DD}-V_{SS}|$ (or pin open)
  "H": V_{SS}
  Shown below is the operation mode at each input pin. For details of the operation mode, refer to 4.

Applied level / Input pin name	V_{SS}		open	V_{DD}	
	AC(*1)	DC	$1/2\|V_{DD}-V_{SS}\|$	DC	AC(*1)
TIME SET IN	FAST DOWN	SLOW DOWN	NOP(*2)	SLOW UP	FAST UP
TIME SET /DIM		SET ENABLE	LOCK(RT)	LOCK(RT) DIMMER	
50 12 /60 /24		50Hz 24HR	60Hz 12HR	50Hz 12HR	
ALM SELECT	RADIO & BUZZER	RADIO	BUZZER	OFF	RADIO & BUZZER
SLP/SNE		SLEEP	NOP(*2)	SNOOZE	
POWR DOWN		NOR(*3)	POWR DOWN	NOR(*3)	
ON/OFF IN		ON	NOP(*2)	OFF	

	V_{SS}	V_{DD}(open)
ALM DSP /SET	ALM DSP /SET	NOP(*2)

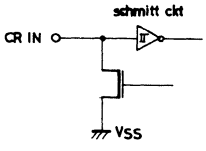
(Note) (*1)



(*2): No Operation
(*3): Normal

(2) TIME-BASE-IN input signal

- Input impedance: 1Mohm or greater
- With Schmitt circuit
- With clamp circuit



(*3) CR-IN

- With Schmitt circuit, open drain driver
- Oscillation frequency: 2400Hz
- Used for clock, alarm, dimmer, time setting at the battery backup

Output configuration

Output for segment, alarm, radio: P-channel open drain

Operation description

(1) Display mode select

The SLP/SNZ IN, ALM DSP/SET are used to select a display mode as shown below.

SLP/SNZ IN	ALM DSP/SET	Display mode
H	-	Sleep time display
L	-	Seconds display
M	H	Alarm time display
M	L	Real time display

(Note) For "H", "M", "L", refer to (1) Switch signal of Input Confuguration
"-": Don't care

(2) Time setting

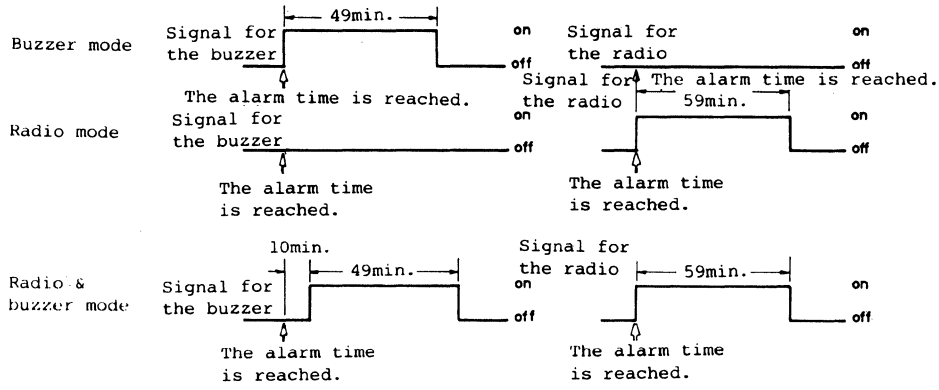
- Time setting is excuted by applying the level shown in (1) Switch signal of Input Configuration TIME SET IN pin.
- Real time setting is excuted when the TIME SET/DIM pin is set to "H".
- Shown below is the operation at each display mode.

Display mode	Setting mode	Operation	Remarks
Real time display Seconds display	FAST UP	Minutes contents are counted up at a 120Hz rate.	Seconds contents are cleared to 00.
	SLOW UP	Minutes contents are counted up at a 2Hz rate.	
	NOP	No setting is executed.	
	SLOW DOWN	Minutes contents are counted down at a 2Hz rate.	Seconds contents are cleared to 00.
	FAST DOWN	Minutes contents are counted down at a 120Hz rate.	
Alarm time display	FAST UP	Minutes contents of alarm time display are counted up at a 120Hz rate.	
	SLOW UP	Minutes contents of alarm time display are counted up at a 2Hz rate.	
	NOP	Alarm time display only	
	SLOW DOWN	Minutes contents of alarm time display are counted down at a 2Hz rate.	
	FAST DOWN	Minutes contents of alarm time display are counted down at a 120Hz rate.	
Sleep time display	FAST UP	Minutes contents of sleep time display are counted up at a 120Hz rate.	
	SLOW UP	Minutes contents of sleep time display are counted up at a 2Hz rate.	
	NOP	Minutes contents of sleep time display are counted down at a 2Hz rate 1 to 2 seconds later.	
	SLOW DOWN	Minutes contents of sleep time display are counted down at a 2Hz rate.	
	FAST DOWN	Minutes contents of sleep time display are counted down at a 120Hz rate.	

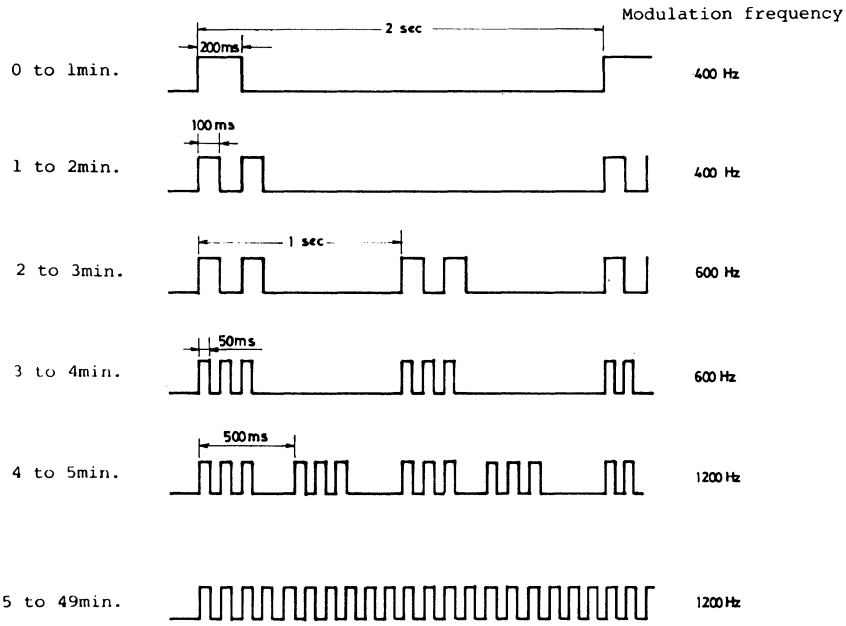
(Note)
- In the SLOW UP/DOWN setting mode, minutes contents are first counted up/down by 1 and are counted up/down at a 2Hz rate 0.5 to 1.0 second later.
- In the FAST UP/DOWN setting mode, minutes contents are counted up/down at a 120Hz rate and are counted up/down by 15 to 16 after the application of the level shown in (1) Switch signal of Input Configuration to the TIME SET IN pin is released.

(3) Alarm operation

1) Alarm on a 24-hour basis. Delivers signal for the buzzer and for the radio.
2) Signal for the buzzer and signal for the radio are turned ON/OFF at each mode of ALM SELECT as shown below.



3) Shown below is how the buzzer waveform changes with time after the buzzer is activated.

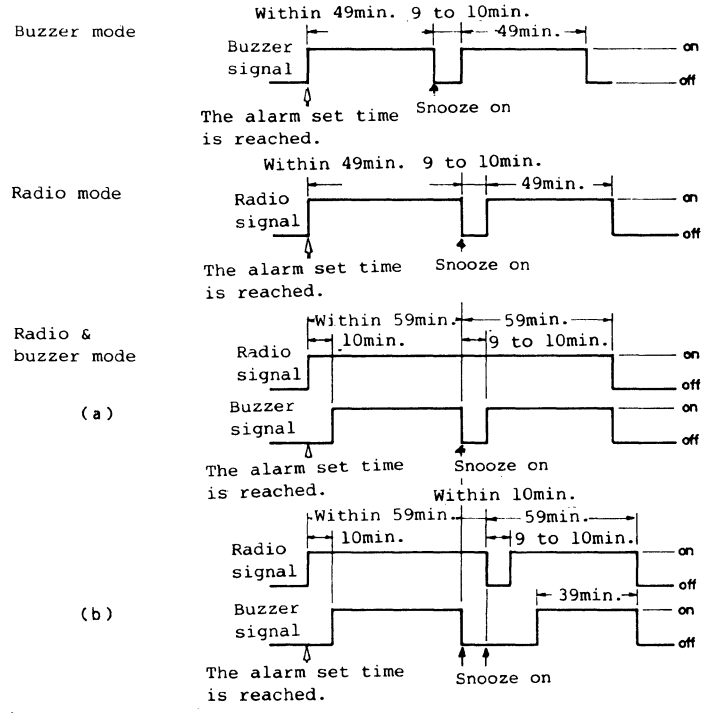


4) Output for the radio: DC level
5) Relation between alarm operation and sleep timer operation
   - If signal for the sleep timer is applied when output for the alarm is delivered (including the period when output for the snooze is delivered), output for the alarm is turned OFF and the sleep timer starts operating.
   - If signal for the alarm is applied when output for the sleep timer is delivered, the alarm mode is changed to the buzzer mode, delivering signal for the buzzer. The sleep timer operation remains unaffected. The sleep timer keeps operating for 49 minutes after the alarm time is reached.
6) Alarm operation when manually turning ON/OFF the radio
   - If signal for manually turning ON/OFF the radio is applied when output for the alarm is delivered, output for the alarm is turned OFF, turning ON/OFF the radio.
   - If signal for the alarm is applied when signal for manually turning ON the radio is applied, the alarm mode is changed to the buzzer mode, delivering signal for the buzzer. Signal for manually turning ON the radio remains applied.

7) Mode change during the alarm-activated period
   - The mode selected is entered.
   - When the radio mode or radio & buzzer mode is changed to the buzzer mode, no output is delivered for 10 minutes after the alarm set time is reached.
   - When executing down setting after the alarm set time is reached at the buzzer mode, output for the radio is delivered for the alarm set time minus 10 minutes at the radio mode or radio & buzzer mode.
   - When the buzzer mode is changed to the radio & buzzer mode, both output for the radio and output for the buzzer are delivered.
   - When the radio mode or radio & buzzer mode is changed to the buzzer mode, the radio snooze is released.
   - When both radio snooze and buzzer snooze are applied at the radio & buzzer mode and then the buzzer mode is selected after output for the radio is delivered, output for the buzzer is delivered.

(4) Snooze operation

If the SLP/SNZ IN is set to V_{DD} level when either output for the radio or output for the buzzer is delivered, the snooze function is operated.



If input is applied to the ON, OFF, SLEEP when the snooze function is in operation, the snooze is released and the mode selected is entered.

(5) Sleep timer operation

1) When the sleep time display mode is entered according to the Table in 2-1 at the sleep timer OFF-state, the sleep timer is set to 59 minutes, delivering output for the radio. When the sleep timer counts down to 0 minute after the lapse of 59 minutes, output for the radio is turned OFF.
   . When the sleep timer isin operation, the SLP IND signal is delivered.
2) If the sleep time display mode is entered when the sleep timer is in operation, the remaining time of the sleep timer is displayed.
3) If the sleep time display mode is held for 1 second or greater, the sleep time counter counts down at a 2Hz rate.

(6) Manually turning ON/OFF the radio

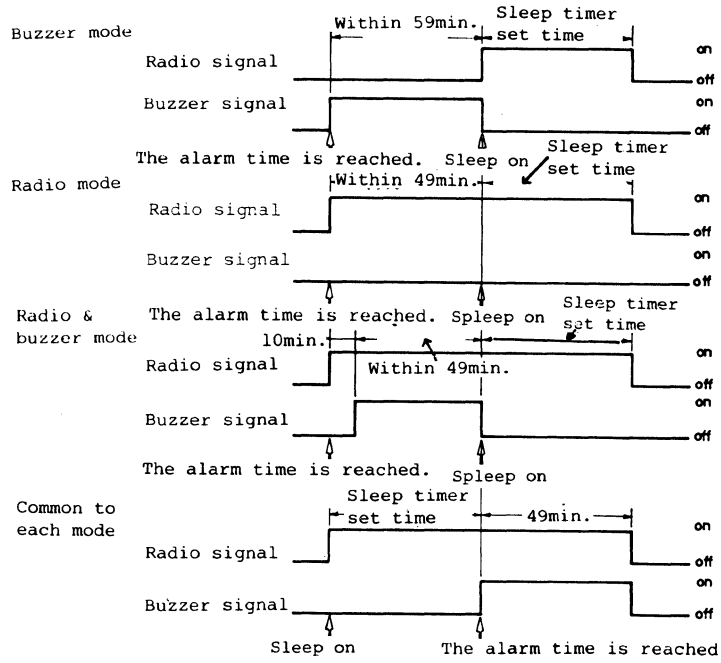
The ON/OFF pin can be used to turn ON/OFF signal for the radio as shown in the Table 2-1. When signal for manually turning ON the radio is applied,

the ON IND signal is delivered.

(7) Relations among alarm operation, sleep timer operation, manual operation

1) Relation between alarm operation and sleep timer operation

- When the sleep timer is turned ON at the alarm ON-state, the alarm operation stops and the sleep timer starts operating.
- When the alarm set time is reached at the sleep timer ON-state, signal for the buzzer is delivered unless the ALM SELECT is turned OFF. The sleep timer ON-state continues, keeping signal for the radio delivered.



2) Relation between sleep timer operation and manual operation

- When control signal for manual ON is applied at the alarm ON-state, the alarm stops operating and signal for the radio and signal for ON IND are delivered. When control signal for manual OFF is applied at the alarm ON-state, the alarm stops operating.
- If the alarm set time is reached when signal for manual ON is applied, signal for the buzzer is delivered unless the ALM SELECT is turned OFF. The manual ON-state continues, keeping signal for the radio delivered.

3) Relation between sleep timer operation and manual operation

- When the sleep timer is turned ON at the manual ON-state, the manual ON-state is released and the sleep timer starts operating.
- When signal for manual ON(or OFF)-state is applied at the sleep timer ON-state, the sleep timer ON-state is released and the manual ON(or OFF)-state is entered.
- When control input for turning ON the sleep timer and ON/OFF control input are applied simultaneously, the sleep timer set time only is displayed, with no signal for the radio delivered (ON).

4) Shown below is a summary of these relations.

Alarm operation	Sleep timer operation	Manual operation	Signal for the buzzer		Signal for the radio		SLP IND signal		ON indication		Remarks
			1	2	1	2	1	2	1	2	
1	2		(on)	off	(on)	on	off	on	off	off	Alarm → Sleep
2	1		off	on	on	on	on	on	off	off	Sleep → Alarm
1		2	(on)	off	(on)	on	off	off	off	on	Alarm → Manual
2		1	off	on	on	on	off	off	on	on	Manual → Alarm
	1	2	off	off	on	on	on	off	off	on	Sleep → Manual
	2	1	off	off	on	on	off	on	on	off	Manual → Sleep

1 : Mode of the first operation and mode of each output signal at this first operation
2 : Mode of the next operation and mode of each output signal at this next operation
ON: ON-state of output signal
OFF: OFF-state of output signal
(ON): On-state of signal for the buzzer or signal for the radio (including the snooze period)

(8) Backup operation
1) When the POWR DOWN pin is open or set to 1/2|V_{DD}-V_{SS}| level, counting is performed based on the oscillation frequency of the CR oscillator.
2) Control input other than input for manual OFF-state is inhibited at the backup mode.
3) The CR-oscillator is capable of turning 2400Hz oscillation frequency into the reference clock at the backup mode regardless of 50Hz/60Hz use.
4) All the display segment outputs are turned OFF at the backup mode. However, the blanking mode is released for 10ms (8.3ms) after a carry from seconds to minutes occurs.

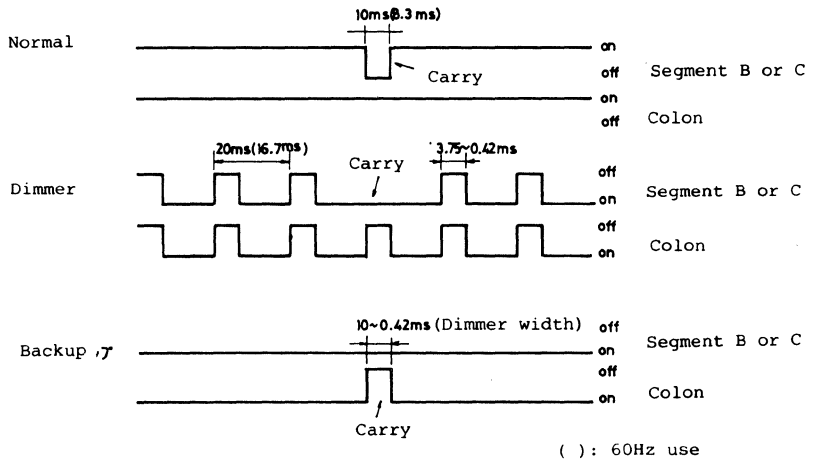
(9) Relations between backup operation and alarm operation
1) Relation between backup operation and alarm operation
- When the alarm set time is reached at the backup mode, signal for the buzzer is delivered unless the ALM SELECT is turned OFF. When the normal mode returns from the backup mode, the ALM SELECT controls the operation.
- If the backup mode is entered when the alarm is in operation, the alarm mode is changed to the buzzer mode. When the backup mode is released, the operation mode just before the backup mode is entered returns and the operation modes of the radio and buzzer are determined by the contents of the sleep timer counter. The contents of the sleep timer counter are preset to "49 minutes" if the backup mode is entered when the TIME BASE IN pin is set to V_{DD} level; and are unfixed in other cases.
- When the backup mode is entered, the snooze function is released.

2) Relation between backup operation and sleep timer operation
- If the backup mode is entered when the sleep timer is in operation, signal for the radio is turned OFF. However, the sleep timer counter continues operating normally. When the backup mode is released before the contents of the sleep timer counter reach "0 minutes", signal for the radio is turned ON for only the remaining period of time.

3) Relation between backup operation and manual operation
- If the backup mode is entered when signal for manual ON-state is applied, signal for the radio is turned OFF. Even when the backup mode is released, signal for the radio remains turned OFF.

(10) Selection of 50/60Hz and 12/24-hour basis
The 50/60 12/24 pin is used. Refer to 2-1.

(11) Carry output
1) Output for second carry, minutes carry, hour carry is delivered at the segments.
Second carry: Segments B,C of the minute digits are turned OFF simultaneously. (Pins 18, 20)
Minute carry: Segments B, C of the minute digit in 10's place are turned OFF simultaneously. (Pins 12, 14)
Hour carry : Segments B, C of the hour digits are turned OFF simultaneously. (Pins 5, 7)
2) In addition to the above, the colon (pin 24) must be turned ON to prevent malfunction from occurring at the dimmer mode or backup mode.
3) Shown below is the timing when a carry occurs.



4) Time setting mode
No carry signal is delivered at the time setting mode.

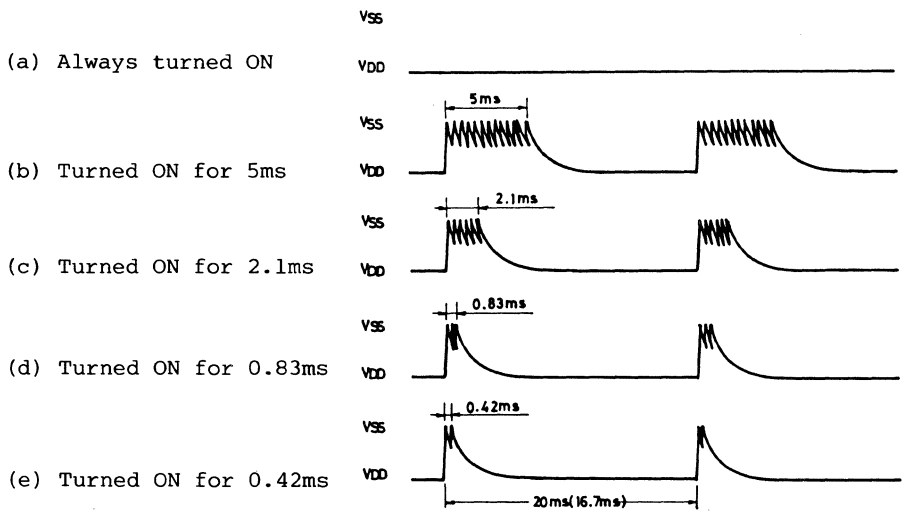
(12) CR-OSC

1) The CR-OSC starts oscillating at each mode shown below.
- Backup mode
- Buzzer ON-mode
- Dimmer control mode
- Time (alarm, sleep timer) setting mode

2) Backup mode
- Continuous oscillation of 2400Hz, which is divided by 40 to use 60Hz as the reference clock
- 50/60Hz select: 60Hz is selected automatically.

3) Buzzer ON-mode
- 2400Hz is divided into 1200Hz, 600Hz, 400Hz to be used for the buzzer tone. (Intermittent oscillation capability)

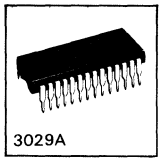
4) Dimmer control mode
- No oscillation occurs when no control is required for the dimmer (the segments are always turned ON).
- Intermittent oscillations shown below occur at the dimmer control mode.



( ): 60Hz use

5) Time setting mode
   - Oscillation occurs as long as signal is applied to the TIME SET IN. This oscillation is used for fast up/down counting at a 120Hz rate.

LM8560


3029A

P ED MOS LSI

Digital Clock Alarm

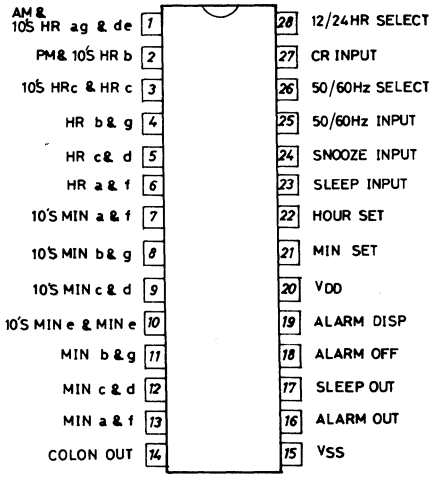
Ⓔ 1543

Applications
- Alarm clock
- Clock radio

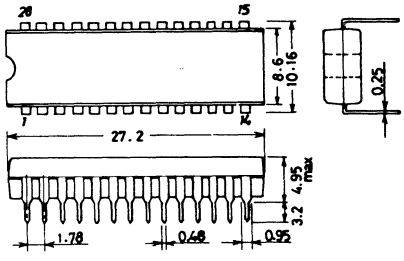
Functions
- Real time display
- Alarm with snooze
- Sleep timer (max. 59 minutes or 1 hour 59 minutes)

Features
(1) Single-chip ED MOS LSI
(2) LED direct drive by time-sharing (duplex)
(3) Wide operating voltage range
(4) Alarm on a 24-hour basis
(5) Two selections of time format: AM/PM 12-hour basis and 24-hour basis.
(6) On-chip CR oscillator for battery backup.
(7) 50Hz or 60Hz is usable as the reference frequency.
(8) Possible to automatically advance "hours", "minutes"
(9) Sleep timer (max. 59 minutes or 1 hour 59 minutes)
(10) Repeatedly usable snooze
(11) Power failure indicator
(12) 900Hz output for alarm tone

Pin Assignment



Case Outline 3029A-D28SIC
(unit:mm)



SANYO: DIP28S

Operation Description

- 50Hz/60Hz input: The on-chip Schmitt trigger circuit allows a simple RC filter at the input to remove possible line voltage transients. An internal pull-up resister is provided.
- CR input: When AC power-down occurs, the time counter enters the "hold" mode and the on-chip clock oscillator starts operating immediately. If there is no input at "50/60Hz input" during 3-clock period, this oscillator controls the time counter advance instead of "50/60Hz input". The values of CR determine the frequency of the on-chip clock oscillator. All segment outputs are off during backup oscillator operation.
  (Note) If the backup OSC is used at the power-down mode, "50/60Hz input" must be open or at V_{SS} level.
- 50/60 select input: Connecting "50/60Hz select" to V_{SS} enables 50Hz operation. For 60Hz operation, "50/60Hz select" is left unconnected: Pull-down to V_{DD} is provided by the internal pull-down resistor.
- Display mode select input (alarm display/sleep display): The internal pull-down resistor allows the use of 2 SPST (single-pole single-throw) switches to select 4 display modes listed in Table 1.

Table 1. Display Mode

Select Input		Display Mode	Digit No.1	Digit No.2	Digit No.3	Digit No.4
Alarm	Sleep					
NC	NC	Time display	10's hour,AM/PM	hour	10's minite	Minite
Vss	NC	Alarm display	10's hour,AM/PM	hour	10's minite	Minite
NC	Vss	Sleep display	Blanked	hour	10's minite	Minite
Vss	Vss	Seconds display	Blanked	Minute	10' second	Second

(Note) If V_{SS} is applied to 2 input of "alarm display" and "sleep display" simultaneously, the seconds display mode is entered.

Time setting input: Two setting inputs for 'hours' and 'minutes' are provided. The application of V_{SS} causes the time setting in Table 2 to occur. An internal pull-down resistor each is provided.

Table 2. Setting Contents

Display Mode	Set Input	Functions
Time	HOUR	'Hours' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 second later.
	MIN	'Minites' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 second later. 'Seconds' are reset.
	BOTH	Both operations shown above are performed.
Seconds (Alarm & Sleep)	HOUR(Note)	'Seconds' are cleared to [00].
	MIN	"Hold" mode.
	BOTH*	'Hours' and 'minutes' are reset to [0:00] (24-hour basis) or [12:00] (12-hour basis).

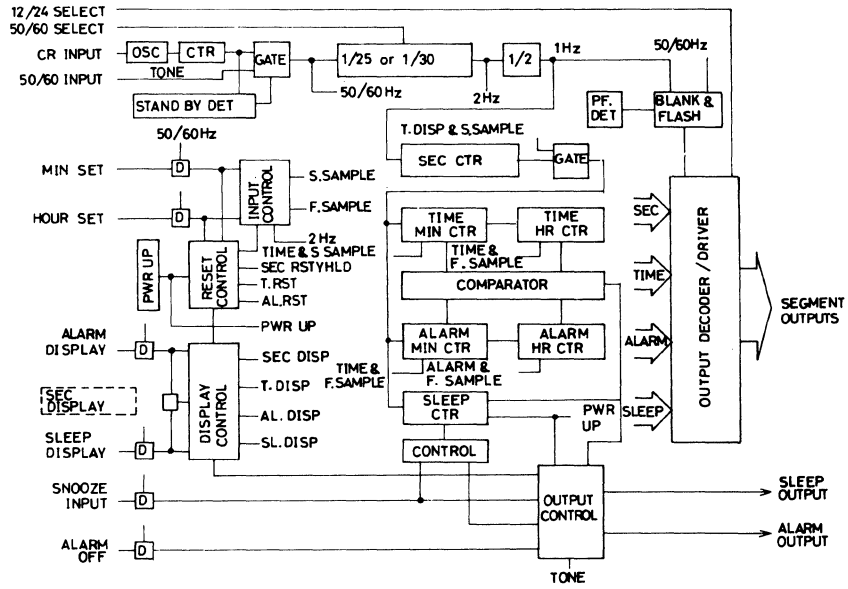
Display Mode	Set Input	Functions
Alarm	HOUR	'Hours' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 second later.
	MIN	'Minutes' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 second later.
	BOTH	'Hours' and 'Minutes' are reset to [0:00] (24-hour basis) or [12:00] (12-hour basis).
Sleep	-	The moment V_{DD} is applied to "sleep display", the sleep counter is set to [0:59].
	HOUR	The moment V_{DD} is applied to "sleep display" and "hour set" simultaneously, the sleep counter is set to [1:59].
	MIN	The sleep counter counts down at a 2Hz rate.
	BOTH	The sleep counter counts down at a 2Hz rate.

* Once the reset mode or hold mode is entered, another function input is locked until both "hour set" input and "minute set" input are released.

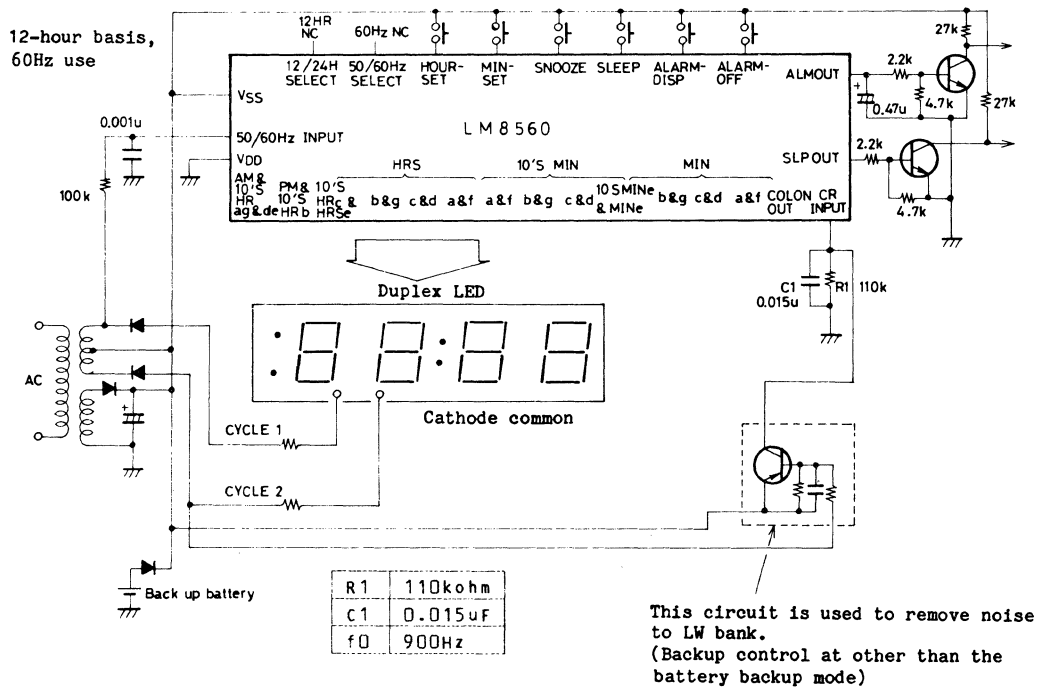
(Note) When "seconds" display is at 50 to 59, "seconds" are reset to [00] and a carry occurs to increment "minutes" +1.

- 12/24-hour select input: Leaving this pin unconnected (V_{DD}) causes the 12-hour basis to be selected; connecting this pin to V_{SS} causes the 24-hour basis to be selected. An internal pull-down resistor is provided.
- Power failure indication: If the power supply voltage drops and is applied again, all the on-segments flash and the power failure indication mode is entered.
  The power failure indication mode is released by applying V_{SS} to "hour set" or "minutes set".
- Alarm operation and alarm output:
  When the alarm set time is reached, the alarm signal is delivered. This signal continues to be delivered for 1 hour 59 minutes unless reset by "alarm off" or "snooze input". This signal is provided for the tone-signal of 900Hz with 50% duty of 2Hz gated. A simple LPF can be used to turn this alarm signal into DC signal as required.
- Snooze input: By momentarily connecting this pin to V_{SS} at the alarm on-state, the alarm output is inhibited for 8 to 9 minutes, after which the alarm signal is delivered again. The snooze function can be used repeatedly for 1 hour 59 minutes. An internal pull-down resistor is provided. By connecting "snooze input" to V_{SS} at the alarm off-state, the sleep timer counter is reset to [0:00]. (The sleep timer is reset with one touch.)
- Alarm off input: Connecting this input pin to V_{SS} inhibits the alarm output momentarily. An internal pull-down resistor is provided.
- Sleep timer and sleep output: The sleep output can be used to keep the radio turned on for any period of time up to 59 minutes or 1 hour 59 minutes. Table 2 shows how to select the period (59 minutes or 1 hour 59 minutes). This sleep timer uses a down counter. When the counter contents reach [00], the output stops being delivered, turning off the radio. By connecing "snooze input" to V_{SS} at the sleep output on-state, the sleep output is inhibited.

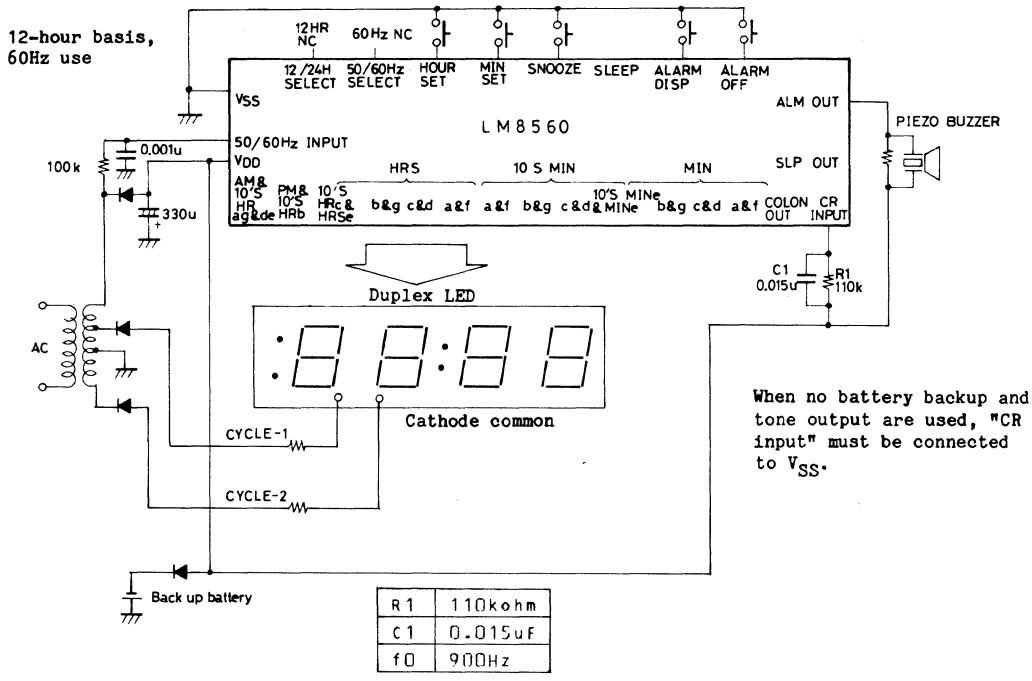
Block Diagram



Sample Application Circuit for Clock Radio Use (+ power supply)



Sample Application Circuit for Clock Use (- power supply)



R1	110kohm
C1	0.015uF
f0	900Hz

LM8560B

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		-17.0 to +0.3	V
Input Voltage (1)	$V_{IN(1)}$	50/60Hz INPUT	-17.0 to +0.3	V
Input Voltage (2)	$V_{IN(2)}$	Other than 50/60Hz INPUT	-17.0 to +0.3	V
Output Voltage	V_{OUT}		-17.0 to +0.3	V
Input Clamp Current	I_{IN}	50/60Hz INPUT	-0.4 to +0.4	mA
Allowable Power Dissipation	Pdmax	Ta=70°C	0.7	W
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0

			min	typ	max	unit
Supply Voltage	V_{DD}		-14.0		-6.5	V
Input "H" Level Voltage(1)	$V_{IH(1)}$	50/60Hz INPUT	-1.0			V
Input "L" Level Voltage(1)	$V_{IL(1)}$	50/60Hz INPUT, $V_{DD} \leq -8V$			$V_{DD}+2$	V
		" $V_{DD} > -8V$			$V_{DD}+1$	V
Input "H" Level Voltage(2)	$V_{IH(2)}$	Other than 50/60Hz INPUT, $V_{DD} \leq -8V$	-1.5			V
		Other than 50/60Hz INPUT, $V_{DD} > -8V$	-1.0			V
Input "L" Level Voltage(2)	$V_{IL(2)}$	Other than 50/60Hz INPUT, $V_{DD} \leq -8V$			$V_{DD}+2$	V
		Other than 50/60Hz INPUT, $V_{DD} > -8V$			$V_{DD}+1$	V
Input Voltage on 50/60Hz INPUT Pin	V_{AC-IN} (Note 1)	Referenced to V_{SS} (Note 2)	V_{LED} (Note 1)			V

Electrical Characteristics at Ta=25°C, V_{DD}=-12V			min	typ	max	unit
Input "H" Level Current(1)	$I_{IH(1)}$	50/60Hz INPUT, $V_{IN}=V_{SS}$			2	uA
Input "L" Level Current(1)	$I_{IL(1)}$	50/60Hz INPUT, $V_{IN}=V_{DD}$			10	uA
Input "H" Level Current(2)	$I_{IH(2)}$	Input pins other than 50/60Hz INPUT, $V_{IN}=V_{DD}$			20	uA
Input "L" Level Current(2)	$I_{IL(2)}$	Input pins other than 50/60Hz INPUT, $V_{IN}=V_{DD}$			2	uA
Output "H" Level Current(1)	$I_{OH(1)}$	ALM OUT, SLP OUT $V_{OH}=V_{SS}-1V$	5			mA
Output Leakage Current(1)	$I_{OF(1)}$	ALM OUT, SLP OUT $V_{OUT}=V_{DD}$			10	uA
Output "H" Level Current(2)	$I_{OH(2)}$	10's HR ag & de (24Hmode), $V_{OUT}=V_{SS}-1V$	36			mA
Output Leakage Current(2)	$I_{OF(2)}$	10'S HR ag & de (24Hmode), $V_{OUT}=V_{DD}$			20	uA
Output "H" Level Current(3)	$I_{OH(3)}$	Segment outputs other than above, $V_{OUT}=V_{SS}-1V$	18			mA
Output Leakage Current(3)	$I_{OF(3)}$	" $V_{OUT}=V_{DD}$			20	uA
Power Failure Detect Voltage	V_{DD}		-6.5	-5.0		V
Current Dissipation	I_{CC}	Output:Off, input with pull-down resistor: Open		5	7	mA
Stability of Oscillator for Backup	F_S	Typical value, 900Hz, V_{DD}=-9V±10%	-10		10	%
Accuracy of Oscillator for Backup	F_A	Typical value, 900Hz, V_{DD}=-9V	-10		10	%

LM8560D

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DD}max		-15.0 to +0.3	V
Input Voltage (1)	$V_{IN(1)}$	50/60Hz INPUT	-15.0 to +0.3	V
Input Voltage (2)	$V_{IN(2)}$	Other than 50/60Hz INPUT	-15.0 to +0.3	V
Output Voltage	V_{OUT}		-15.0 to +0.3	V
Input Clamp Current	I_{IN}	50/60Hz INPUT	-0.4 to +0.4	mA
Allowable Power Dissipation	Pdmax	Ta=70°C	0.7	W
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0			min	typ	max	unit
Supply Voltage	V_{DD}		-14.0		-7.5	V
Input "H" Level Voltage(1)	$V_{IH(1)}$	50/60Hz INPUT	-1.0			V
Input "L" Level Voltage(1)	$V_{IL(1)}$	50/60Hz INPUT			V_{DD}+2	V
Input "H" Level Voltage(2)	$V_{IH(2)}$	Other than 50/60Hz INPUT	-1.5			V
Input "L" Level Voltage(2)	$V_{IL(2)}$	Other than 50/60Hz INPUT			V_{DD}+2	V
Input Voltage on 50/60Hz INPUT Pin	V_{AC-IN} (Note 1)	Referenced to V_{SS} (Note 2)	2V_{LED} (Note 1)			V

Electrical Characteristics at Ta=25°C, V_{DD}=-12V			min	typ	max	unit
Input "H" Level Current(1)	$I_{IH(1)}$	50/60Hz INPUT, $V_{IN}=V_{SS}$			10	uA
Input "L" Level Current(1)	$I_{IL(1)}$	50/60Hz INPUT, $V_{IN}=V_{DD}$			10	uA
Input "H" Level Current(2)	$I_{IH(2)}$	Input pins other than 50/60Hz INPUT, $V_{IN}=V_{DD}$			20	uA
Input "L" Level Current(2)	$I_{IL(2)}$	Input pins other than 50/60Hz INPUT, $V_{IN}=V_{DD}$			10	uA

			min	typ	max	unit
Output "H" Level Current(1)	$I_{OH(1)}$	ALM OUT,SLP OUT $V_{OH}=V_{SS}-1V$	5			mA
Output Leakage Current(1)	$I_{OF(1)}$	ALM OUT,SLP OUT $V_{OUT}=V_{DD}$			10	uA
Output "H" Level Current(2)	$I_{OH(2)}$	10'S HR ag & de (24Hmode), $V_{OUT}=V_{SS}-1V$	32			mA
Output Leakage Current(2)	$I_{OF(2)}$	10'S HR ag & de (24Hmode),$V_{OUT}=V_{DD}$			20	uA
Output "H" Level Current(3)	$I_{OH(3)}$	Segment outputs other than above,$V_{OUT}=V_{SS}-1V$	16			mA
Output Leakage Current(3)	$I_{OF(3)}$	" $V_{OUT}=V_{DD}$			20	uA
Power Failure Detect Voltage	V_{DD}		-7.5	-5.0		V
Current Dissipation	I_{CC}	Output:Off,input with pull-down resistor: Open		5	7	mA
Stability of Oscillator for Backup	F_S	Typical value,900Hz, $V_{DD}=-9V\pm10\%$	-10		10	%
Accuracy of Oscillator for Backup	F_A	Typical value,900Hz, $V_{DD}=-9V$	-10		10	%

LM8560N

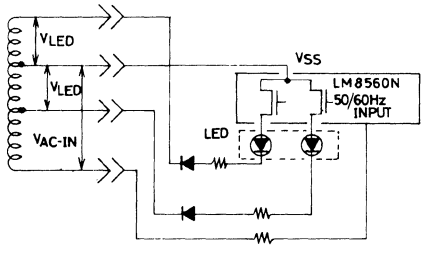
Absolute Maximum Ratings at $Ta=25^oC, V_{SS}=0V$				unit
Maximum Supply Voltage	$V_{DD}max$		-15.0 to +0.3	V
Input Voltage (1)	$V_{IN(1)}$	50/60Hz INPUT	-15.0 to +0.3	V
Input Voltage (2)	$V_{IN(2)}$	Other than 50/60Hz INPUT	-15.0 to +0.3	V
Output Voltage	V_{OUT}		-15.0 to +0.3	V
Input Clamp Current	I_{IN}	50/60Hz INPUT	-0.4 to +0.4	mA
Allowable Power Dissipation	Pdmax	$Ta=70^oC$	0.7	W
Operating Temperature	Topg		-30 to +70	^oC
Storage Temperature	Tstg		-55 to +125	^oC

Allowable Operating Ranges at $Ta=25^oC, V_{SS}=0$			min	typ	max	unit
Supply Voltage	V_{DD}		-14.0		-7.5	V
Input "H" Level Voltage(1)	$V_{IH(1)}$	50/60Hz INPUT	-1.0			V
Input "L" Level Voltage(1)	$V_{IL(1)}$	50/60Hz INPUT			$V_{DD}+2$	V
Input "H" Level Voltage(2)	$V_{IH(2)}$	Other than 50/60Hz INPUT	-1.5			V
Input "L" Level Voltage(2)	$V_{IL(2)}$	Other than 50/60Hz INPUT			$V_{DD}+2$	V
Input Voltage on 50/60Hz INPUT Pin	V_{AC-IN} (Note 1)	Referenced to V_{SS} (Note 2)	V_{LED} (Note 1)			V

Electrical Characteristics at $Ta=25^oC, V_{DD}=-12V$			min	typ	max	unit
Input "H" Level Current(1)	$I_{IH(1)}$	50/60Hz INPUT,$V_{IN}=V_{SS}$			10	uA
Input "L" Level Current(1)	$I_{IL(1)}$	50/60Hz INPUT,$V_{IN}=V_{DD}$			10	uA
Input "H" Level Current(2)	$I_{IH(2)}$	Input pins other than 50/60Hz INPUT,$V_{IN}=V_{DD}$			20	uA
Input "L" Level Current(2)	$I_{IL(2)}$	Input pins other than 50/60Hz INPUT,$V_{IN}=V_{DD}$			10	uA
Output "H" Level Current(1)	$I_{OH(1)}$	ALM OUT,SLP OUT $V_{OH}=V_{SS}-1V$	5			mA
Output Leakage Current(1)	$I_{OF(1)}$	ALM OUT,SLP OUT $V_{OUT}=V_{DD}$			10	uA

			min	typ	max	unit
Output "H" Level Current(2)	$I_{OH(2)}$	10's HR ag & de (24Hmode), $V_{OUT}=V_{SS}-1V$	36			mA
Output Leakage Current(2)	$I_{OF(2)}$	10'S HR ag & de (24Hmode), $V_{OUT}=V_{DD}$			20	uA
Output "H" Level Current(3)	$I_{OH(3)}$	Segment outputs other than above, $V_{OUT}=V_{SS}-1V$	18			mA
Output Leakage Current (3)	$I_{OF(3)}$	" $V_{OUT}=V_{DD}$			20	uA
Power Failure Detect Voltage	V_{DD}		-7.5	-5.0		V
Current Dissipation	I_{CC}	Output:Off,input with pull-down resistor: Open		5	7	mA
Stability of Oscillator for Backup	F_S	Typical value,900Hz, $V_{DD}=-9V\pm10\%$	-10		10	%
Accuracy of Oscillator for Backup	F_A	Typical value,900Hz, $V_{DD}=-9V$	-10		10	%

(Note 1)



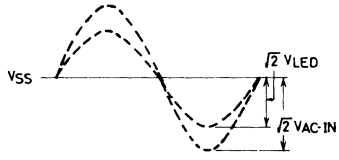
V_{AC-IN} --- Input voltage(average) on 50/60Hz INPUT pin

V_{LED} ----- Supply voltage(average) for LED

These are the values at no load mode.

[Fig. 1]

(Note 2)



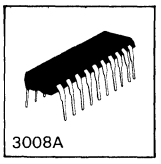
[Fig. 2]

ACCESSORIES FOR AUDIO APPLIANCES

- **Pin Numbering**

When you face the top side (marking side) of the package, numbering starts with ① assigned to the pin located, in a counterclockwise direction, immediately after the index point and turns counterclockwise.

LC7000



C MOS LSI

SL² Electronic Tuning System for Multi-Bands

Ⓔ 905A

Features

1. (1) By using in conjunction with voltage synthesizer type SL² electronic tuning control LSI (LC7200 series), a tuning system for multiband can be realized. In other words, 1 band of 2 bands (FM/AM) of control LSI can be divided into 2 parts.

   For example:

   a) 2-divided random tuning of MW and LW (medium wave and long wave) of different types of band: Refer to Sample Application Circuit 1.

   b) 2-divided random tuning of the same wide band. Example: For short wave (SW), 2-divided random tuning of SW1 and SW2 is available. For TV wave, 2-divided random tuning of "L" channel and "H" channel is available: Refer to Sample Application Circuit 2.

   (2) 2-divided band (LC7000) is selected as follows:

   a) Manual tuning:
   Alternate selection by momentary switch

   b) Auto search tuning:
   Automatic alternate selection by differential pulse signal of tuning sweep wave.

   c) Preset tuning:
   Random band read by channel switches ($\overline{CH1}$ to $\overline{CH7}$).

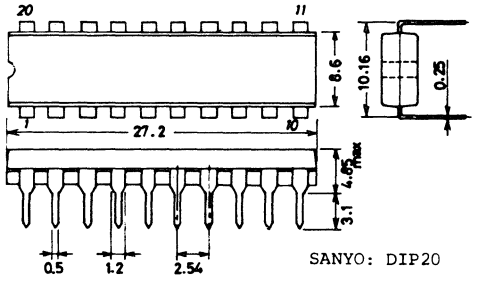
   d) Preset memory:
   Random band write by simultaneous push of channel switches ($\overline{CH1}$ to $\overline{CH7}$) and $\overline{MEMO}$ switch.

2. By connecting the CR1 pin of control LSI (LC7200 series) and the CLK pin (LC7000) in parallel, the system clock can be used in common.
3. Supply voltage (V_{DD}): 8V to 10V

Functions

1. In selecting FM band/(MW+LW) band in the 3-band (FM/MW/LW) application (FM band and (MW+LW) band), the memory band signal is generated for random preset memory and preset tuning of MW/LW band.
2. In the 2-band application (FM/SW or MW/SW), the band signal is generated for division of one band (SW) into 2 parts (BAND 1, BAND 2) and alternate search tuning of BAND 1/BAND 2.
3. 7-channel ($\overline{CH1}$ to $\overline{CH7}$) band (BAND 1 or BAND 2) memory.
4. Last band memory by battery backup at the time of power failure.

Case Outline 3008A-D20IC
(unit: mm)



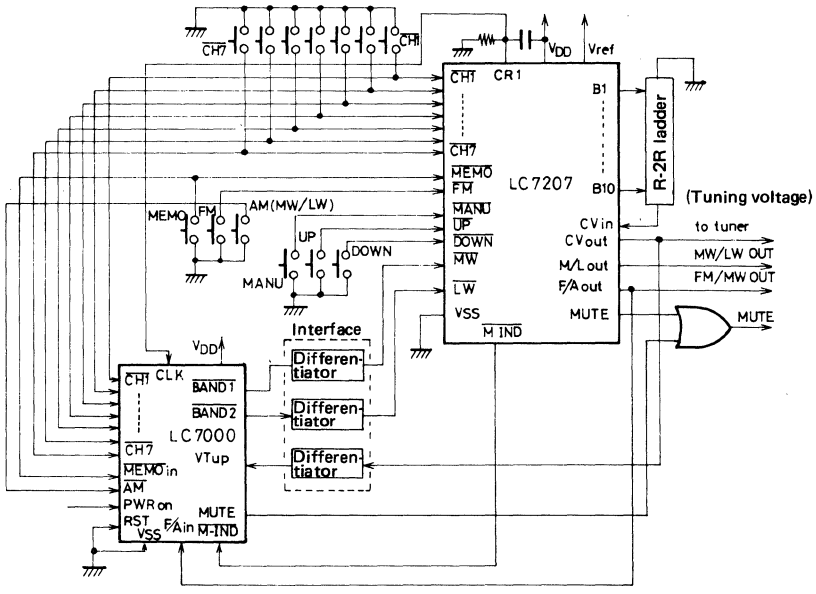
SANYO: DIP20

1. Application Circuits

■ Sample Application Circuit 1

- 3-band reception (FM/MW/LM) set: FM band – 7 stations memory capability
  MW and, LW band – 7 stations random memory capability

Band / Tuning Mode	FM Band	AM Band (MW Band + LW Band)
Manual Tuning	FM	• Toggle select of MW/LW band (AM input). • Hold of last band and last received station.
Search Tuning	FM	• Automatic band select of MW/LW band (VT up input). • Hold of last band and last received station.
Preset tuning	FM	• Random preset tuning of MW/LW band. • Hold of last band and last received station.



- Set feature

	FM	MW	LW
Band Indication	○	○	○
Band Select Input	FM	MW/LW	

Band memory

	FM1	FM2	FM3	FM4	FM5	FM6	FM7	→ Memorized by control LSI LC7207
	CH1	CH2	CH3	CH4	CH5	CH6	CH7	
	MW1	LW1	MW2	MW2	MW3	LW3	MW4	→ Memorized by LC7000

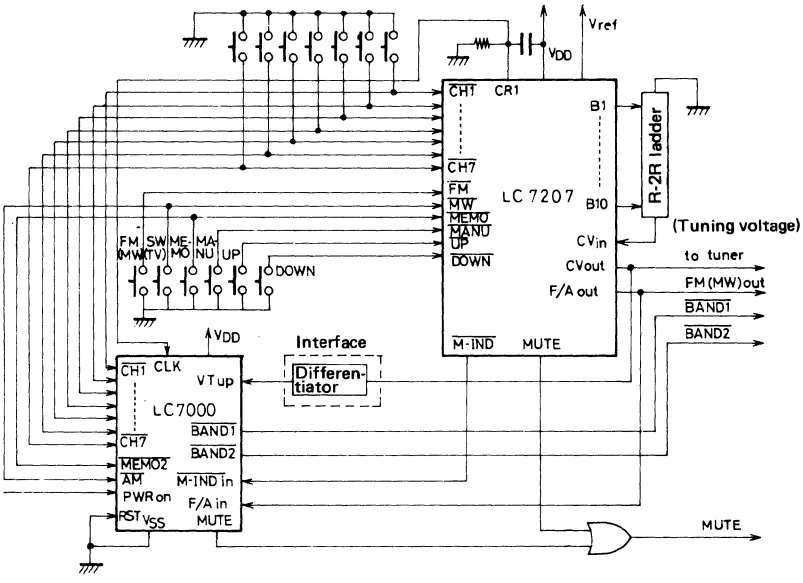
(MW/LW can be exchanged with each other.)

■ Sample Application Circuit 2

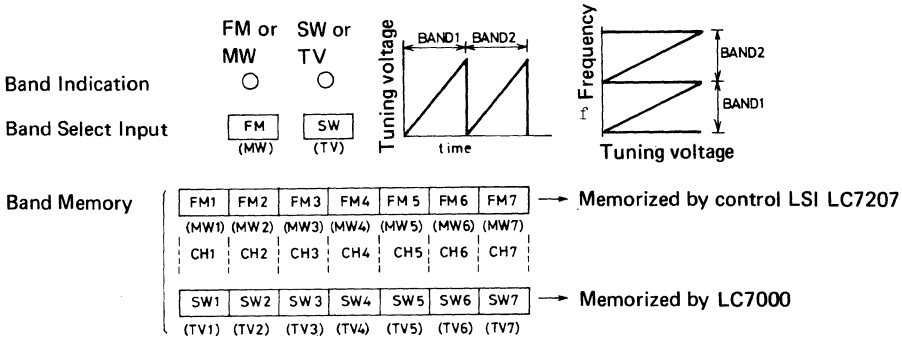
- 2-band reception: FM and (SW1 + SW2), FM and (TV1 "L" band & TV2 "H" band) set.
  MW and (SW1 + SW2), MW and (TV1 "L" band & TV2 "H" band) set.
- FM band or MW band: 7 stations memory capability.
- SW1 + SW2 or TV1 + TV2: 7 stations memory capability: Divided random tuning of the same wide band.

Band / Tuning Mode	FM or MW Band	Wide band (SW band or TV band)
Manual Tuning	FM/MW	• Toggle select of divided band (AM input). • Hold of last band and last received station.
Search Tuning	FM/MW	• Automatic band select of divided band (VT up input). • Hold of last band and last received station.
Preset Tuning	FM/MW	• Random preset tuning of the same band. • Hold of last band and last received channel.

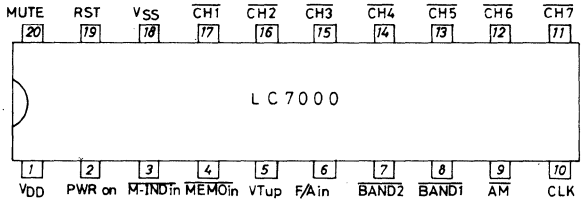
- Application where the MW band select input of the LC7207 is applied to wide band.



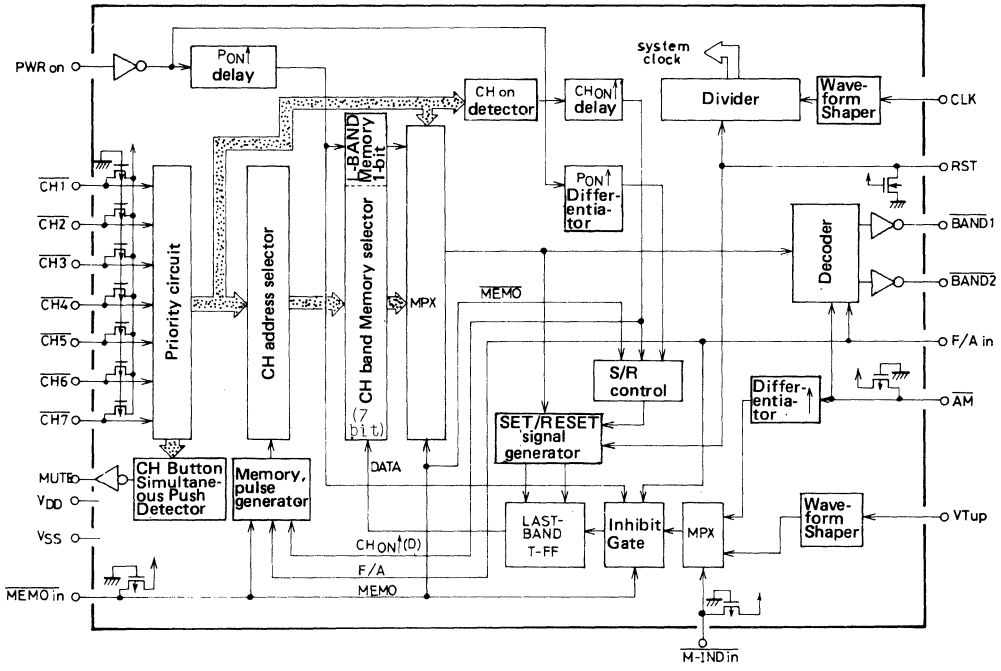
- Set Feature



2. Pin Assignment



3. Equivalent Circuit Block Diagram



4. Pin Description

4-1. Input Pin

1) Memory addressing: Channel input

- Each channel ($\overline{CH1}$ to $\overline{CH7}$) input is for addressing the band (BAND1 or BAND2) memory.
- Connected in parallel with $\overline{CH1}$ to $\overline{CH7}$ of SL^2 control LSI (LC7207) (LC7200: Up to $\overline{CH5}$, LC7201: Up to $\overline{CH6}$). "L" level makes the memory addressing input active. By setting the undermentioned $\overline{MEMO}$ pin to "L" level and then making the CH input active, that is "L" level, the present band information is stored in the memory corresponding to the CH. When the $\overline{MEMO}$ pin is at "H" level, the band information in the memory is delivered at the undermentioned $\overline{BAND1}$, $\overline{BAND2}$ pins.
- Priority order in case of simultaneously selecting CH input:
  $\overline{CH1} > \overline{CH2} >$ ---------- $> CH7$

2) Memory control input ($\overline{MEMO\ in}$)

- Memory control input used to store the band information in each channel ($\overline{CH1}$ to $\overline{CH7}$).
- Connected in parallel with the $\overline{MEMO}$ pin of SL^2 control LSI (LC7200 series). By setting the memory control input ($\overline{MEMO\ in}$) to "L" level and the memory addressing CH input ($\overline{CH1}$ to $\overline{CH7}$) to "L" level (20 msec. or more), the present band information is stored in the memory corresponding to the CH.

3) Automatic band select input (VT up)
   - The rise differential signal of the auto search sweep voltage (upward search) is applied through capacitive coupling to select MW/LW alternately in the multiband set (FM/(MW+LW) band set). In the wide band set (SW/TV band set), BAND1/BAND2 are selected alternately.
   - In the DOWN mode, the rise differential signal of the auto search sweep voltage (downward search) is inverted externally and applied.
4) Divided band mode select input (F/A in)
   - Connected to the band select output (F/A out) of SL^2 control LSI (LC7200, 7201, 7203).
   - When the F/A in input is at "L" level, the divided band mode is entered.
5) Manual band select input ($\overline{AM}$)
   - When the divided band mode (F/A in: "L" level) is entered and the $\overline{M\text{-}IND\ in}$ input is at "L" level, the $\overline{AM}$ input acts to toggle-select the divided band (BAND1, BAND2) (chattering free time: 6 to 12 msec.).
   - When the $\overline{AM}$ input is set to "L" level, either $\overline{BAND1}$ pin or $\overline{BAND2}$ pin is set to "L" level in the same timing.
6) Toggle operation mode select input ($\overline{M\text{-}IND\ in}$)
   - When the divided band mode (F/A in: "L" level) is entered and the $\overline{M\text{-}IND\ in}$ input is at "L" level, the $\overline{AM}$ input acts to select the divided band alternately.
   - When the divided band mode (F/A in: "L" level) is entered and the $\overline{M\text{-}IND\ in}$ input and all CH band select inputs ($\overline{CH1}$ to $\overline{CH7}$) are at "H" level, the VT up input acts to select the divided band alternately.
7) Backup operation control input (PWR on)
   - When the PWR on input is set to "L" level, the internal memory and flip-flop enter the backup mode.
   - When the PWR on input is set to "H" level, the operation mode is entered.
8) Clock input (CLK)
   - Connected in parallel with the CR1 pin of SL^2 control LSI (LC7200, 7201, 7203, 7207).
   - Used to apply the system clock of the LC7000.
9) Reset input (RST)
   - When the RST input is set to "H" level, the internal memory and flip-flop enter the reset mode.

4-2. Output Pin

1) Divided band 1 select otuput ($\overline{BAND1}$)
   - "L" level selects the divided band 1.
   - When the F/A in is at "H" level, the $\overline{BAND1}$ output turns "H" level. When the $\overline{AM}$ input is at "L" level, the divided band state ("L" or "H") is delivered.
   - When the RST input is at "H" level, the divided band 1 output turns "H" level.
2) Divided band 2 select output ($\overline{BAND2}$)
   - "L" level selects the divided band 2.
   - When the F/A in is at "H" level, the $\overline{BAND2}$ output turns "H" level. When the $\overline{AM}$ input is at "L" level, the divided band state ("L" or "H") is delivered.
   - When the RST input is at "H" level, the divided band 2 output turns "L" level.
3) Mute output (MUTE)
   - Simultaneous push of 2 or more CH buttons ($\overline{CH1}$ to $\overline{CH7}$) causes the mute signal to be delivered.
   - When in the mute mode, "H" level is delivered.

5. Main Specifications

Absolute Maximum Ratings/T_a=25±2°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.3～+11	V
Input Voltage	V_I		−0.3～(V_{DD}+0.3)	V
Output Voltage	V_O	Output TR OFF	−0.3～(V_{DD}+0.3)	V
Output Current	I_{OUT}		±10	mA
Allowable Power Dissipation	P_d max	T_a≦70°C	200	mW
Operating Temperature	T_{opg}		−20～+70	°C
Storage Temperature	T_{stg}		−40～+125	°C
Lead Temperature and Time	T_{sol}	t=10sec	260	°C

Allowable Operating Ranges/T_a=25±2°C (Pin No.)

				min	typ	max	unit
Supply Voltage	V_{DD}(1)	1	V_{DD}: All operations T_a=−20～+70°C	8.0		10.0	V
	V_{DD}(2)	1	V_{DD}: Memory backup : T_a=−20～+70°C	2.2		10.0	V
"H" level Input Voltage	V_{IH}(1)	3,4,6,9, 11～17	$\overline{\text{M-IND in}}$, $\overline{\text{MEMO in}}$, F/A in, AM, CH1～CH7, RST	0.75V_{DD}		V_{DD}	V
	V_{IH}(2)	10	CLK	Parallel drivable with LC7207			
	V_{IH}(3)	5	VT up : V_{DD}=8V, T_a=−20～+70°C	0.95V_{DD}		V_{DD}	V
	V_{IH}(4)	2	PWR-ON : V_{DD}=8V, T_a=−20～+70°C	0.80V_{DD}		V_{DD}	V
"L" Level Input Voltage	V_{IL}(1)	3,4,6,9, 11～17	$\overline{\text{M-IND in}}$, $\overline{\text{MEMO in}}$, F/A in, AM, CH1～CH7, RST	V_{SS}		0.25V_{DD}	V
	V_{IL}(2)	10	CLK	Parallel drivable with LC7207			
	V_{IL}(3)	5	VT up : tøw=50μs, T_a=−20～+70°C, Fig See Fig. 1.			0.7V_{DD}	V
	V_{IL}(4)	2	PWR-ON: Memory backup	V_{SS}		0.15V_{SS}	V
Input Pulse Width	tøw	5	VT up : 0.7V_{DD}, T_a=−20～+70°C, Fig 1 See Fig. 1.	50			μs
Clock Frequency	f_{in}	10	CLK	1.0	2.5	4.0	kHz

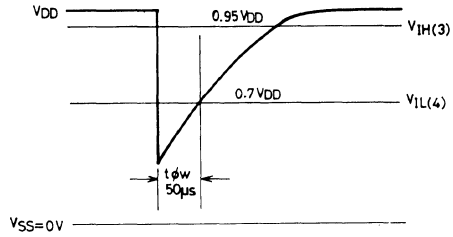
Electrical Characteristics/T_a=25±2°C, V_{DD}=8.0 to 10.0V, V_{SS}=0V

				min	typ	max	unit
"H" Level Output Voltage	V_{OH}	7,8,20	$\overline{\text{BAND2}}$, $\overline{\text{BAND1}}$, MUTE : I_{OH}=−1mA	V_{DD}−1.0		V_{DD}	V
"L" Level Output Current	V_{OL}(1)	7,8	$\overline{\text{BAND2}}$, $\overline{\text{BAND1}}$: I_{OL}=2.0mA	V_{SS}		1.0	V
	V_{OL}(2)	20	MUTE : I_{OL}=1.0mA	V_{SS}		1.0	V
"H" Level Input Current	I_{IH}(1)	2,6,10	PWR-ON, F/A in, CLK : V_I=V_{DD}			10	μA
	I_{IH}(2)	19	RST : V_I=V_{DD}	20		160	μA
"L" Level Input Current	I_{IL}(1)	3,4,9, 11～17	$\overline{\text{M-IND in}}$, $\overline{\text{MEMO in}}$, AM, $\overline{\text{CH1}}$～$\overline{\text{CH7}}$: V_I=0V	−600		−100	μA
		〃	〃 : V_I=0.8V_{DD}	−240		−40	μA
	I_{IL}(2)	2,6,10,19	PWR-ON, F/A in, CLK, RST : V_I=0V	−10			μA
Current Dissipation	I_{DD}(1)	1	V_{DD} : PWR-ON=[H], V_{DD}=10V, other pin nonactive, See Fig. 2.			2	mA
	I_{DD}(2)	2	V_{DD} : PWR-ON≦0.44V, V_{DD}=2.2V, other pin nonactive, See Fig. 2.			5	μA
Pin Open Voltage	V_{IN}(1)	3,4,9, 11～17	$\overline{\text{M-IND in}}$, $\overline{\text{MEMO in}}$, AM, $\overline{\text{CH1}}$～$\overline{\text{CH7}}$: V_{DD}=10V	8		10	V
	V_{IN}(2)	19	RST : V_{DD}=10V	0		2	V

(Note) Current direction: + (no sign): Flowing into device
− : Flowing out of device

Fig. 1: Input Waveform at VT up/DN Pin

VT up input waveform : $T_a = -20 \sim +70°C$, $V_{DD} = 8 \sim 10V$



VT up: Standard interface circuit at pin

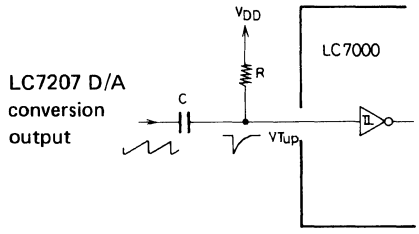
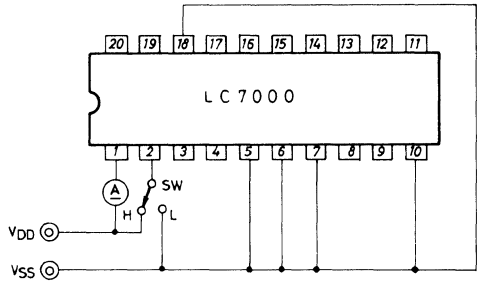
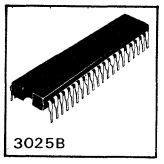


Fig. 2: Current Dissipation Test Circuit



SW	Current Dissipation Test	V_{DD}	Remarks
[H]	$I_{DD}(1)$	10 V	RWR-ON=[H]
[L]	$I_{DD}(2)$	2.2 V	PWR-ON=[L]

LC7010



C MOS LSI

Controller For LM7000-Applied Car Stereo

Ⓔ 1573A

The LC7010 is a controller for direct PLL IC LM7000. It can be used to form a PLL frequency synthesizer with clock for car use.

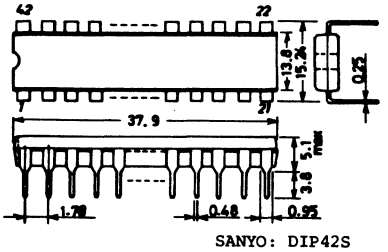
Features

- Applicable in the U.S. and Europe
- LED-used dynamic display (Cathode common)
- Clock function
  - 24-hour system (Europe), 12-hour system (U.S.)
  - Two selections of display mode : Clock preferred display, frequency preferred display
- Channel selection method (Sawtooth wave mode )
  - MANUAL (Up/down) ..... 1 channel/push. Pushing for 500msec. or more causes fast advance at a 60msec. rate channel
  - SCAN (Up) ..... 5-second reception at a time
  - SEEK (Up) ..... Received channel hold
  - SKSEEK, SK SCAN (Up) . SCAN/SEEK of SK channel only
  - PRESET ..... 6-channel preset capability for each of FM/(MW+LW)
- 4-accessory control capability (With input, display, output pin)

Receiving Frequency

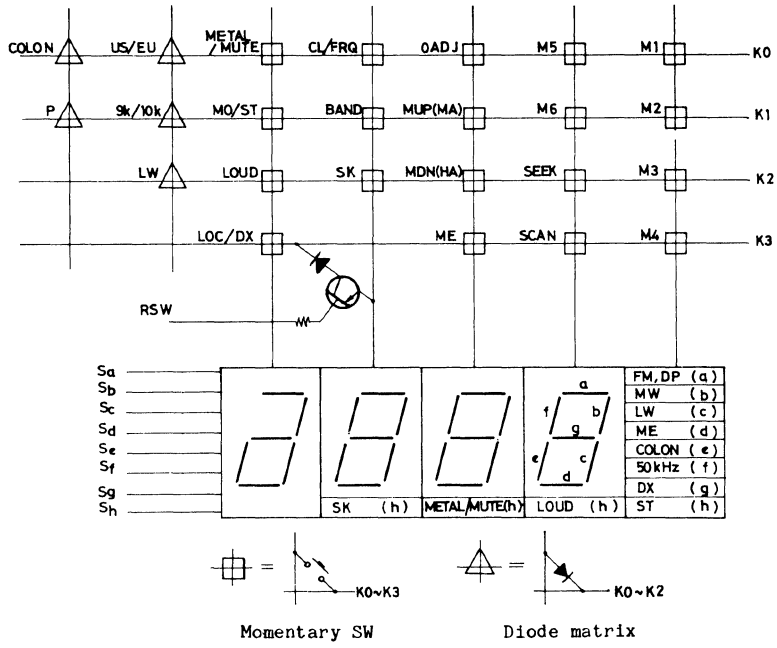
Area	Band	Receiving Frequency Range	Step	Reference Frequency	Intermediate Frequency
USA	FM	87.5 to 108.1 MHz	200kHz	100kHz	10.7 MHz
	MW1	522 to 1611 kHz	9kHz	9kHz	450 kHz
	MW2	520 to 1620 kHz	10kHz	10kHz	450 kHz
Europe	FM	87.5 to 108.0 MHz	50kHz	50kHz	10.7 MHz
	MW1	522 to 1611 kHz	9kHz	9kHz	450 kHz
	MW2	520 to 1620 kHz	10kHz	10kHz	450 kHz
	LW	153 to 281 kHz	1kHz	1kHz	450 kHz

Case Outline 3025B-D42SIC
(unit:mm)

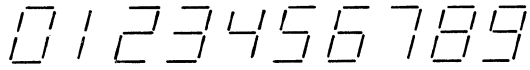


SANYO: DIP42S

Key Matrix Organization and Display



Display font



Diode Matrix

(1) Area select

	USA	Europe
US/EU	off	on

Time display: 12-hour system for USA use
24-hour system for Europe use

(2) MW 9kHz/10kHz select

	9kHz	10kHz
9k/10k	off	on

(3) LW select (only when Europe is selected in (1) above)

	With LW	Without LW
LW	off	on

(4) Clock colon select

	Flashing at a 1Hz rate	Always lighted
colon	off	on

(5) Display priority

	Clock preferred display	Frequency preferred
P	off	on

(Note) on : With diode
off : Without diode

Pin Assignment

Key Description

(1) M1 to M6

Key for writing in/calling from the preset memory

(2) ME

. Frequency display mode
Used to write a new channel in the preset memory. When this key is pushed, "ME" sign is lighted and the write enable mode is entered, and when one of M1 to M6 is pushed within 5 seconds, a frequency displayed is written. The write enable mode is released automatically in 5 seconds.

. Clock display mode
Used to set time. To set time, push MUP(HA), MDN(MA), OADJ while pushing this key.

(3) MUP(MA), MDN(HA)

. Frequency display mode
Key for manual tuning. Each time this key is pushed, the display contents go up or down by 1. When pushed for 500msec. or more, the display contents go up or down at a 60msec./step rate.

. Clock display mode (Used jointly with ME)
"HA" is the key for setting hours. The display contents go up only. Each time this key is pushed, the display contents go up by 1. When pushed for 500msec. or more, the display contents go up at a 4 hours/second rate. This setting does not affect minutes and seconds.
"MA" is the key for setting minutes. The display contents go up only. Each time this key is pushed, the display contents go up by 1. When pushed for 500msec. or more, the display contents go up at a 8 minutes/second rate. Seconds are reset to 00. No carry occurs from minutes to hours.

(4) SEEK (Up direction only)

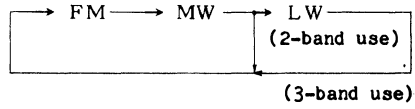
Used to search a broadcasting station automatically and hold a receiving frequency when the broadcasting station is reached. When "SCAN" key is pushed during seeking, the mode is changed to the scan mode and search tuning continues.

(5) SCAN (Up direction only)

Used to search a broadcasting station automatically and hold a receiving frequency for 5 seconds when the broadcasting station is reached. If this key is pushed again before lapse of 5 seconds, the receiving frequency continues to be hold. If nothing is done before lapse of 5 seconds, search starts again. When "SEEK" key is pushed during scanning, the mode is changed to the seek mode and search tuning continues.

(6) BAND

Band select key. Each time this key is pushed, one band is selected.



(7) OADJ (Used jointly with ME)

Key for setting to 0 minute 0 second. Used to set time by the time signal. When the minutes display is at 30 or less, hours remain unaffected; when at 31 or more, hours are incremented by 1.

Example : [Display before setting] [Display after setting]

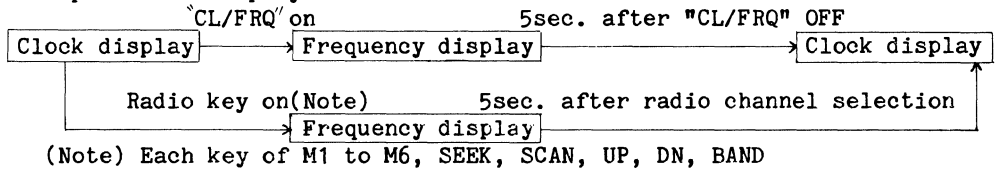
OADJ on

10:30 → 10:00

10:31 → 11:00

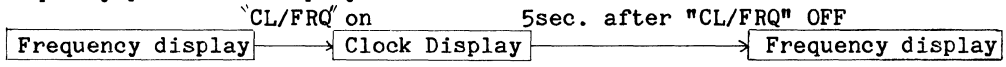
(8) CL/FRQ

. Clock preferred display mode



(Note) Each key of M1 to M6, SEEK, SCAN, UP, DN, BAND

. Frequency preferred display mode



(9) LOC/DX, MO/ST, LOUD, METAL/MUTE

The display mode and output mode caused by key operation are as follows:

Key	Display mode		Output mode
LOC/DX	LOC	Lighted	H
		Unlighted	L
MO/ST	ST	Lighted	L
		Unlighted	H
LOUD	LOUD	Lighted	H
		Unlighted	L
METAL/MUTE	METAL/MUTE	Lighted	H
		Unlighted	L

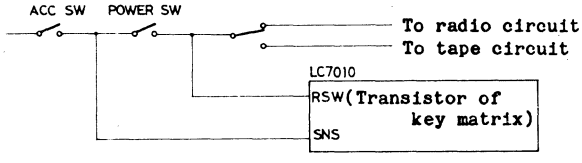
(Note) "METAL/MUTE" have 2 internal modes and share the key, display, output pin. (Refer to the Table shown below.)

(10) SK (FM use only)

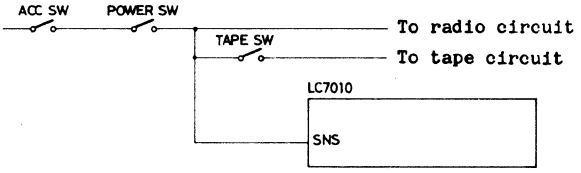
Each time this key is pushed, the SK mode is turned ON/OFF. When in the SK mode, the SK station only is seeked or scanned. The SKO pin is at "H" level.

Power SW Connection and Operation

Example 1



Example 2



SNS	RSW	Display	METAL/MUTE	LOUD	MO/ST	LOC/DX	SK
0	0	off	D	D	D	D	D
0	1	off	D	D	D	D	D
1	0	Clock	E(METAL)	E	D	D	D
1	1	P=0: Clock P=1: FRQ	E(MUTE)	E	E	E	E (FM only)

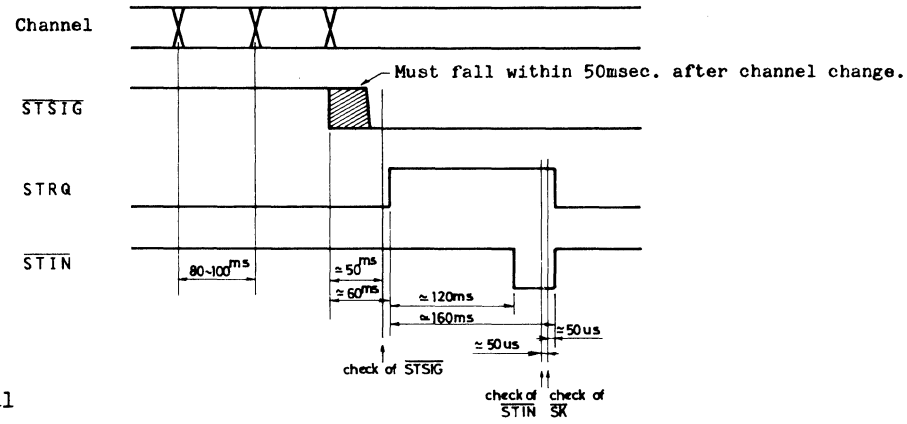
'0'='H' D: Disable
'1'='L' E: Enable

Pin Description

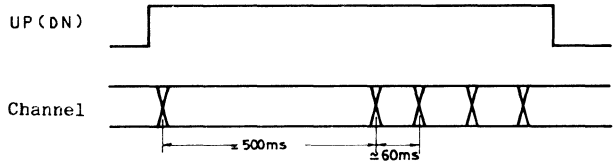
Pin Name	Pin No.	Description	Active	I/O
Sa to Sh	24~31	Display segment drive signal.	H	O
D1 to D5	32~36	Display digit drive signal. Also used as key return signal.	H	O
DS1	38	Key return signal	H	O
DS2	18			
K0 to K3	1,2, 41,42	Key input pin	H	I
AMUTE	15	Audio mute signal to be delivered at the following mode. . Band select mode . Manual up/down mode . Seek, scan mode . Preset read-out mode . Power SW ON/OFF mode . Initial power ON mode	H	O
CE	9	Data signal to be transferred to the LM7000.	H	O
CL	8	CE : Chip enable	⎍	O
DATA	7	CL : Sync clock DATA : Transfer data	-	O
STRQ	10	Signal for instructing the LM7000 to count IF	H	O
$\overline{STIN}$	5	Automatic tuning stop signal.	L	I
$\overline{STSIG}$	4	Signal for giving information that a broadcasting station is nearby during automatic tuning.	L	I
LOC	11	Output signal for selecting LOCAL/DX	H	O
$\overline{MO}$	12	Output signal for selecting monaural/stereo.	L	O
LOUD	13	Output signal for selecting loudness ON/OFF.	H	O
METAL/MUTE	14	Output signal for turning ON/OFF muting/metal.	H	O
M/L	16	Output signal for selecting AM coil.	L	O
SNS	3	Signal for turning ON/OFF ACC (ignition) SW.	H	I
$\overline{SK}$	6	SK signal input.	L	I
$\overline{INT}$	39	Clock time base signal (from the LM7000) input.	L	I
$\overline{HOLD}$	38	Connectec to V_{DD}.	-	I
OSC1	22	The system clock from the LM7000 is inputted to OSC1 or a ceramic resonator is connected to OSC1, OSC2.	-	I
OSC2	23			
$\overline{RES}$	19	Power ON clear signal input.	L	I
V_{DD}	40	Application of power (+5V).	-	-
V_{SS}	21	Application of power (0V).		
$\overline{TST}$	20	Connected to V_{SS}.	-	-
SKO	17	SK mode output signal.	H	O

Timing Description

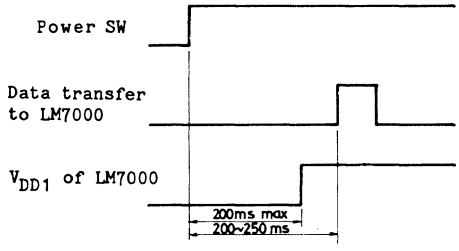
(1) SEEK, SCAN



(2) Manual



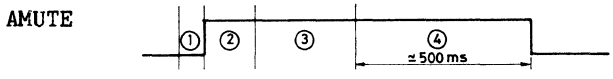
(3) Power SW ON



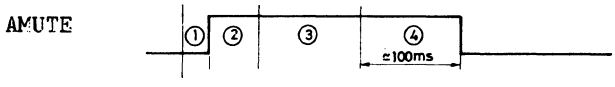
(4) Audio mute (AMUTE)

① Key chattering eliminating time (7msec.)
② Audio pre-mute time (15msec.)
③ Data transfer to PLL (50msec. to 100msec.)
④ Audio post-mute time

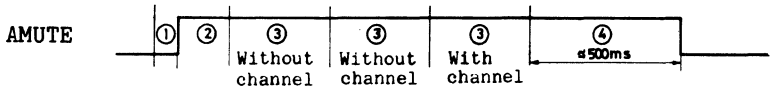
a. Band select mode, preset read-out mode



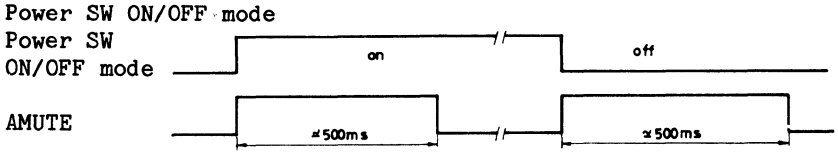
b. Manual up/down mode



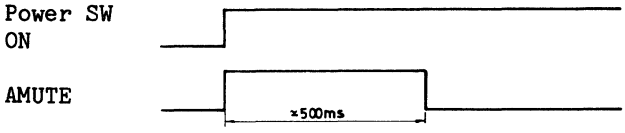
c. SEEK/SCAN MODE



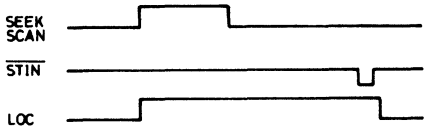
d. Power SW ON/OFF mode



e. Initial power ON mode



(5) "LOC" ON



Allowable Operaating Conditions at Ta=-30 to +70°C, V_{SS}=0V			min	typ	max	unit
Recommended Operating Supply Voltage	V_{DD}		4.5	5.0	5.5	V
"H" Level Input Voltage	V_{IH1}	Input pins other than $\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1	0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1	0.75V_{DD}		V_{DD}	V
"L" Level Input Voltage	V_{IL1}	Input pins other than $\overline{INT}$, $\overline{RES}$, OSC1	V_{SS}		0.3V_{DD}	V
	V_{IL2}	$\overline{INT}$, $\overline{RES}$, OSC1	V_{SS}		0.25V_{DD}	V
	V_{IL3}	TST	V_{SS}		0.3V_{DD}	V
Operating Clock Frequency	f_{extosc}	At external clock input, See Fig. 1	380	400	420	kHz
"H" Level Clock Pulse Width	$t_{wøH}$	" "	0.5			us
"L" Level Clock Pulse Width	$t_{wøL}$	" "	0.5			us
Clock Input Rise Time	t_{oscR}	" "			0.2	us
Clock Input Fall Time	t_{oscF}	" "			0.2	us
External Capacitance for	C1	See Fig. 2	100±10%			pF
Ceramic Oscillation	C2	"	100±10%			pF
External Resistance for	R1	"	1000±5%			kohm
Ceramic Oscillation	R2	See Fig.2. KBR400B	4.7±5%			kohm
		See Fig.2. CBS400P	2.2±5%			kohm

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V(V_{DD}=5V±10% unless otherwise specified).				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +7.0	V
Maximum Input Voltage	V_{IN}max		-0.3 to V_{DD}+0.3	V(Note)
Maximum Output Voltage	V_{OUT}max		-0.3 to V_{DD}+0.3	V
Peak Output Current	Io1	1 output pin	-2.0 to +2.0	mA
	Io2	All output pins	-26 to +26	mA
Allowable Power Dissipation	Pdmax	Ta=-30 to +70°C	350	mW
Operating Temperature	Topg		-30 to +70	°C

			unit
Storage Temperature	Tstg	-55 to +125	°C

(Note) For OSC1 pin, up to oscillation amplitude generated when internally oscillated under the allowable oscillation conditions in Fig. 2 is allowable.

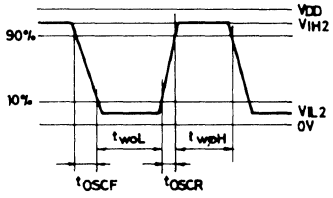


Fig. 1 OSC 1 pin input waveform

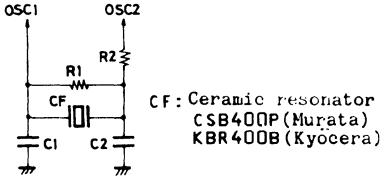
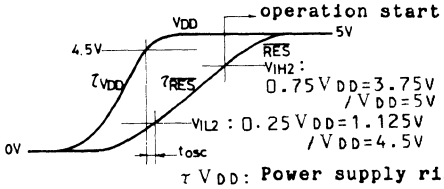


Fig. 2 Recommended oscillator for ceramic oscillation

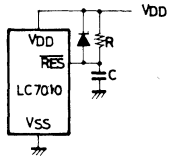
Electrical Characteristics at Ta=-30 to +70°C, V_{DD}=5V±10%, V_{SS}=0V			min	typ	max	unit
"H" Level Input Current	I_{IH}				1	uA
"L" Level Input Current	I_{IL}		-1			uA
"H" Level Output Voltage	V_{OH1}	Output pins other than OSC2 I_{OH}=-1mA	V_{DD}-2			V
	V_{OH2}	Output pins other than OSC2 I_{OH}=-100uA	V_{DD}-0.5			V
"L" Level Output Voltage	V_{OL}	Output pins other than OSC2 I_{OL}=1mA			0.4	V
Output Off Leak Current	I_{OFF1}	Output pins other than OSC2 V_{OH}=V_{DD}			1	uA
	I_{OFF2}	Output pins other than OSC2 V_{OL}=V_{SS}	-1			uA
Clock Oscillation Frequency for Ceramic Oscillation	f_{XOSC}	Conditions for ceramic oscillation, At oscillation circuit in Fig. 2	384	400	417	kHz
Current Dissipation	I_{DD}	At ceramic oscillation, output pin open, Input pin, V_{IN}=V_{DD}		0.5	1.0	mA
Input Capacitance	C_{IN}	f=1MHz		5		pF
Output Capacitance	C_{OUT}	f=1MHz, output high impedance		10		pF
Input/Output Capacitance	C_{IO}	" "		10		pF

Initial Reset Timing



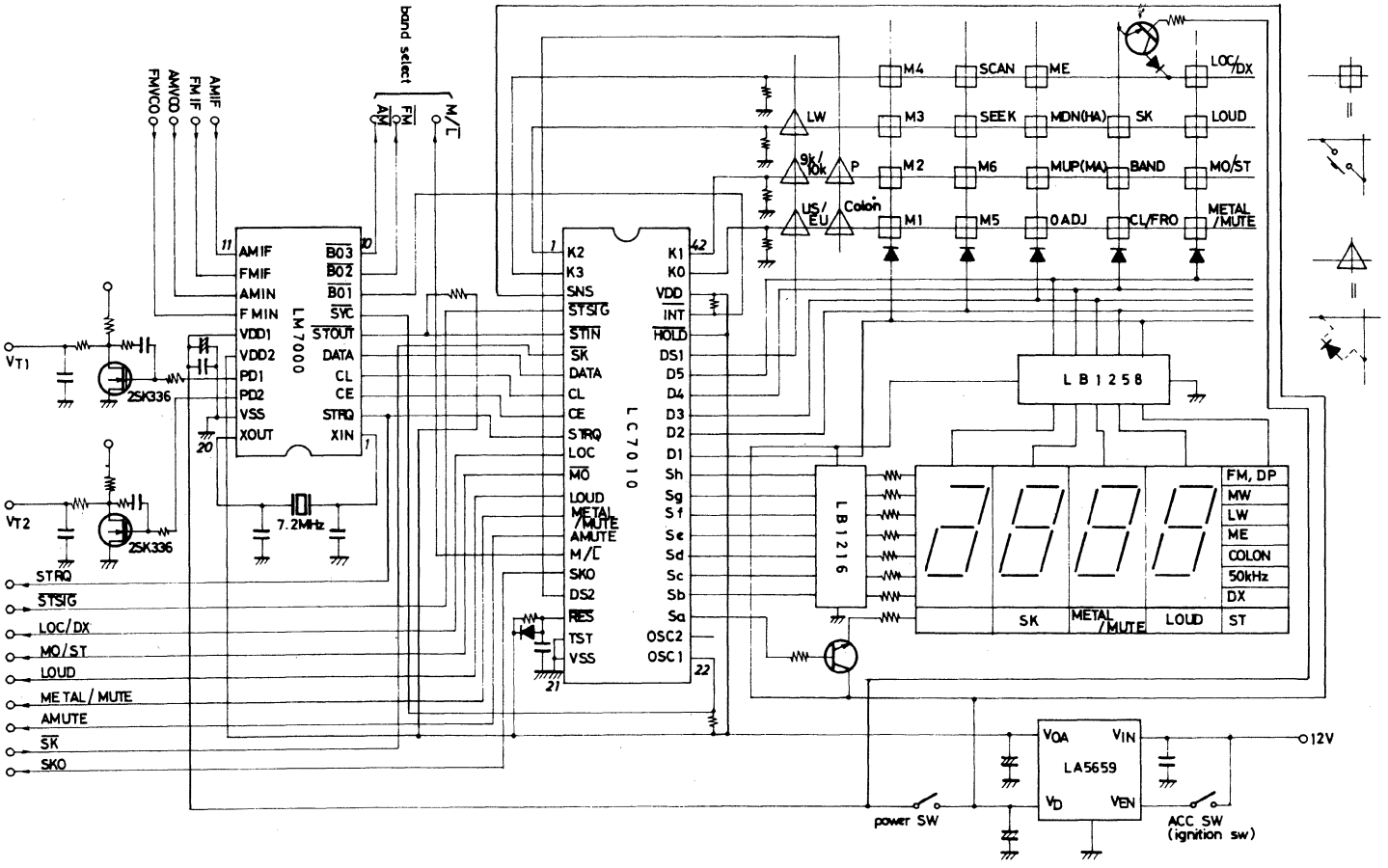
τVDD: Power supply rise time constant

τRES: RES pin rise time constant

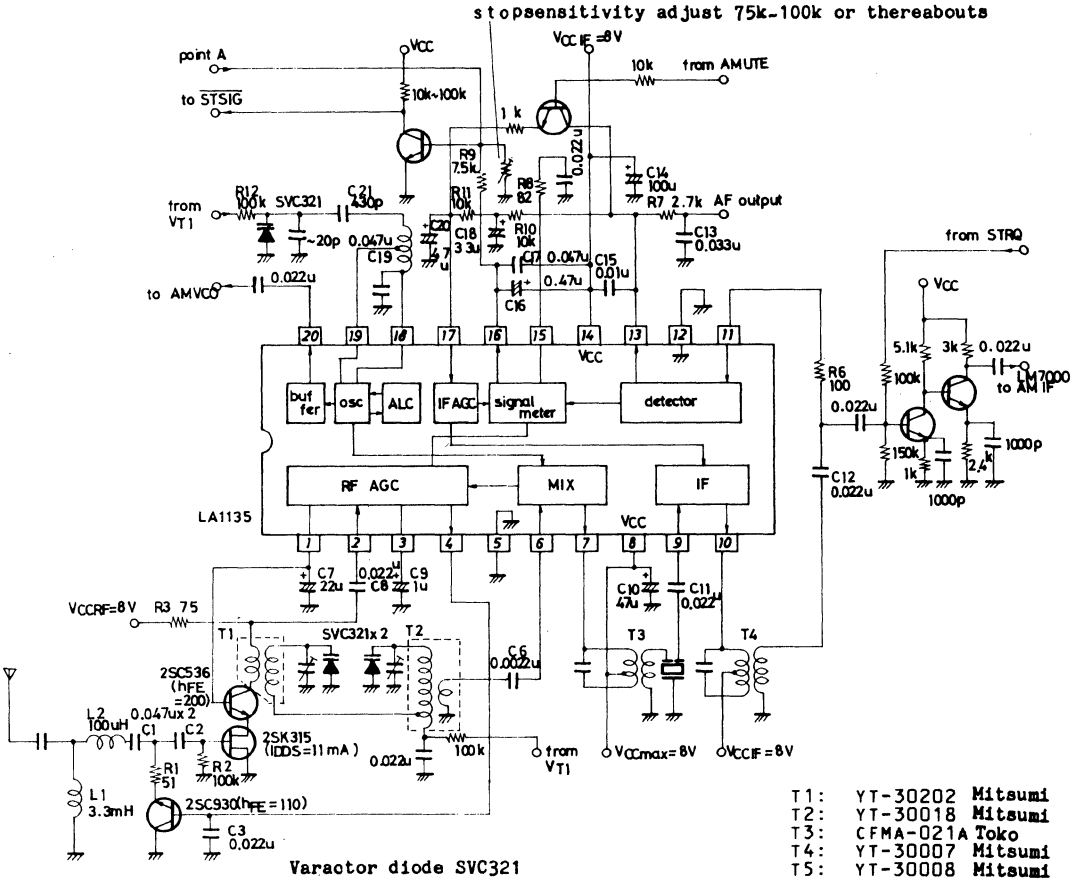


Fix C,R so that $\tau V_{DD} \lesssim \tau \overline{RES}$, $t_{OSC} \gtrsim$ 10msec are yielded.

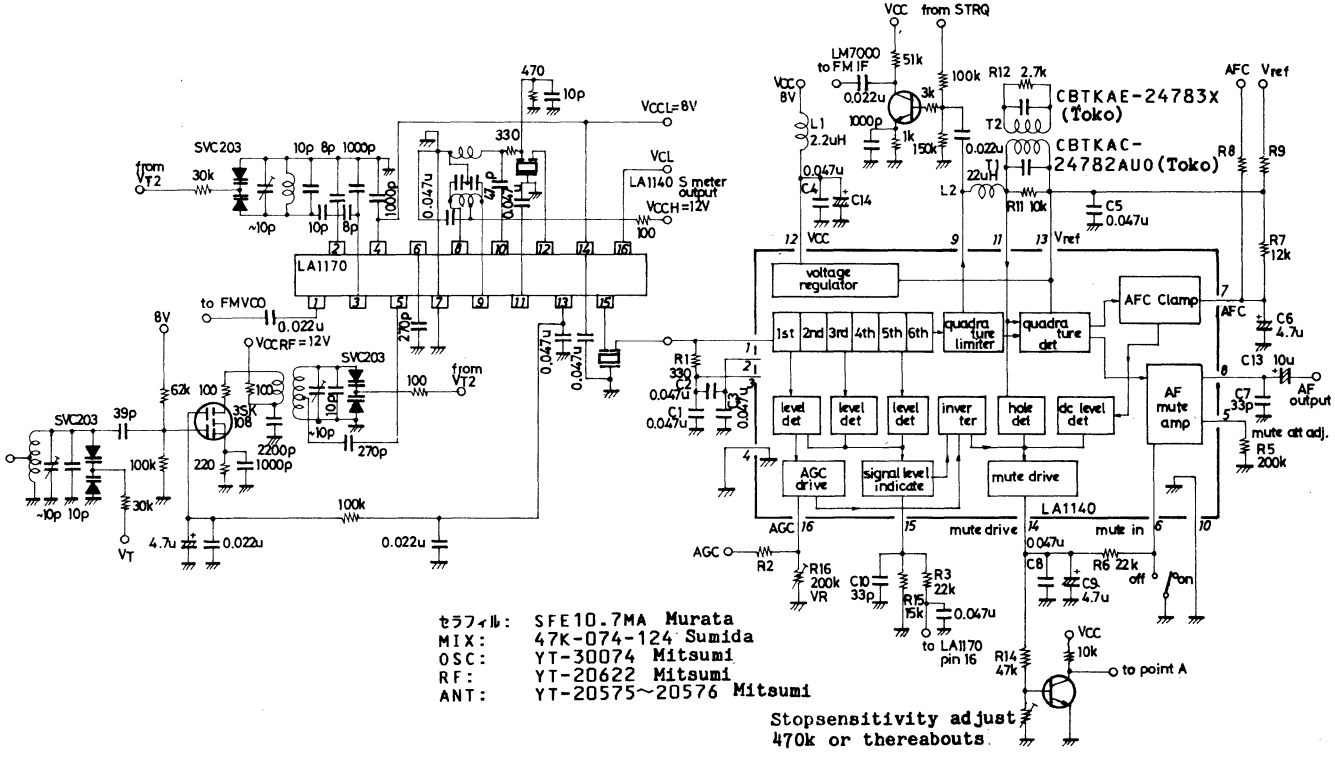
Sample Application Circuit 1



Sample Application circuit 2



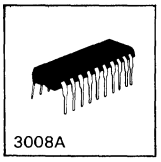
Sample Application Circuit 3



セラフィル: SFE10.7MA Murata
MIX: 47K-074-124 Sumida
OSC: YT-30074 Mitsumi
RF: YT-20622 Mitsumi
ANT: YT-20575~20576 Mitsumi

Stopsensitivity adjust
470k or thereabouts.

LC7120



C MOS LSI

CB Transceiver PLL Synthesizer

Ⓔ 407D

Functions

(1) Only one crystal is required for AM CB transceiver.
(2) Two selections of intermediate frequency: IF_1=10.695MHz, IF_2=9.785MHz.
(3) Two selections of lock monitor output:
- $\overline{LM}$ ● High level at locked mode ● Low level at unlocked mode
- LM ● Low level at locked mode ● High level at unlocked mode

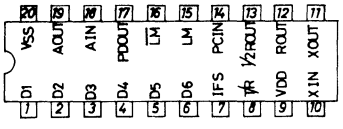
(4) Amplifier for low-pass filter.
(5) Input amplifier for programmable counter.
(6) Detector for misprogramming of programmable counter.
(7) BCD code input to programmable counter.
(8) Buffer output for reference oscillator.
(9) Output for half frequency of reference oscillator.
(10) 10.24MHz crystal oscillator (with feedback resistor).
(11) A scan type transceiver can be formed in conjunction with scan LSI LC7181/LC7191.

Absolute Maximum Ratings/T_a=25°C			unit
Maximum Supply Voltage	V_{DD} max	−0.3 to +9	V
Input Voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT} (Output OFF)	−0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opg}	−30 to +70	°C
Storage Temperature	T_{stg}	−40 to +125	°C

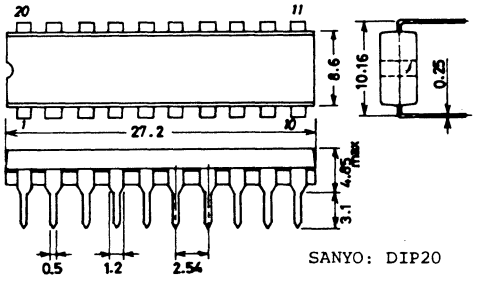
Allowable Operating Ranges/T_a=25°C	Symbol	Pin	Conditions	min	typ	max	unit
Supply Voltage	V_{DD}			6.0	7.0	8.0	V
High Level Input Voltage	V_{IH}	D1 to D6, T/R, IFS		V_{DD}−1.5			V
Low Level Input Voltage	V_{IL}	D1 to D6, T/R, IFS				1.5	V
Input Amplitude	$V_{IN}(1)$	XIN	10.25MHz, duty 50±10% sine wave, capacitive coupling	3.0		0.9V_{DD}	Vp-p
	$V_{IN}(2)$	PCIN	3.5MHz, duty 50±10% sine wave, capacitive coupling	0.7		0.66V_{DD}	Vp-p
Input Frequency	$f_{IN}(1)$	XIN	3.0Vp-p, duty 50±10% sine wave, capacitive coupling	0.5		10.25	MHz
	$f_{IN}(2)$	PCIN	0.7Vp-p, duty 50±10% sine wave, capacitive coupling	0.5		3.5	MHz

(continued on next page)

Pin Assignment



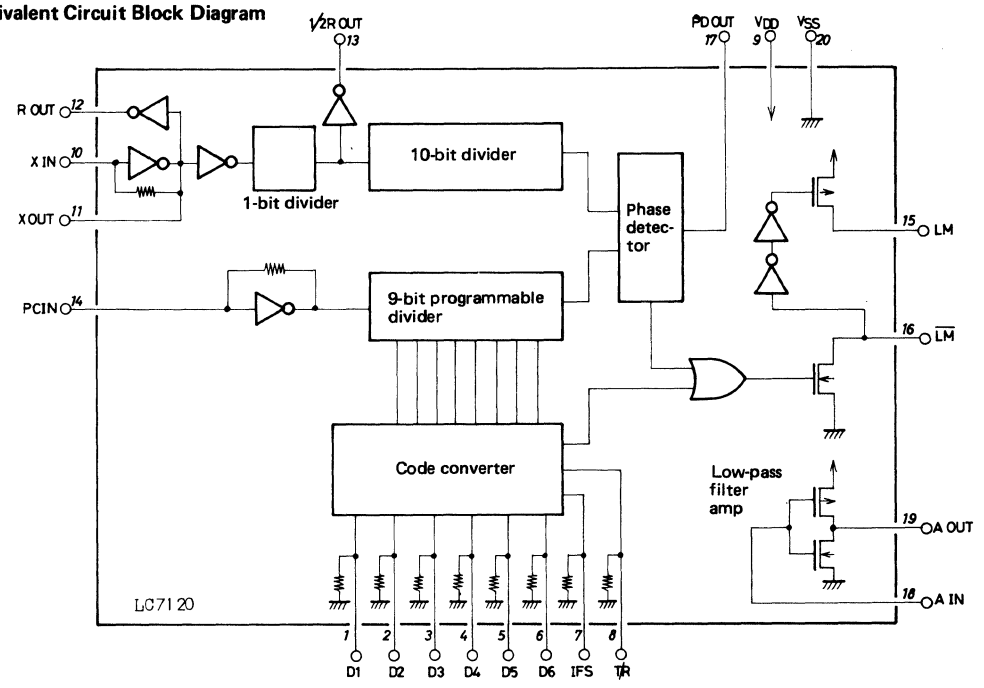
Case Outline 3008A-D20IC
(unit: mm)



Electrical Characteristics/T_a=25°C, V_{DD}=7V±1V

	(Symbol)	(Pin)	(Conditions)	min	typ	max	unit
Feedback Resistance	$R_f(1)$	XIN			7		MΩ
	$R_f(2)$	PCIN			3		MΩ
Pull-down Resistance	RP	D1 to D6, T/R, IFS			28		kΩ
Input Floating Voltage	V_{IF}	D1 to D6, T/R, IFS pin open				1.0	V
3-State OFF Leak Current	$I_{OFF}(1)$	PD OUT	$V_O=V_{DD}/2$		1		nA
Output OFF Leak Current	$I_{OFF}(2)$	$\overline{LM}$	$V_O=V_{DD}$			3.0	μA
Output OFF Leak Current	$I_{OFF}(3)$	LM	$V_O=V_{SS}$			3.0	μA
Input Current	I_{IN}	AIN	$V_1=V_{DD}, V_1=V_{SS}$		1		nA
Filter Amp Gain	VG	AIN, AOUT	$R_f=1M\Omega, f_{IN}=10kHz, Rg=600\Omega$	28			dB
Low Level Output Voltage	V_{OL}	$\overline{LM}$	$I_O=2mA$			0.9	V
High Level Output Voltage	V_{OH}	LM	$I_O=5mA$	$V_{DD}-0.9$			V
Current Dissipation	I_{DD}		$f_{IN}(1)=10.24MHz$ $f_{IN}(2)=3.5MHz$ N=182			20	mA

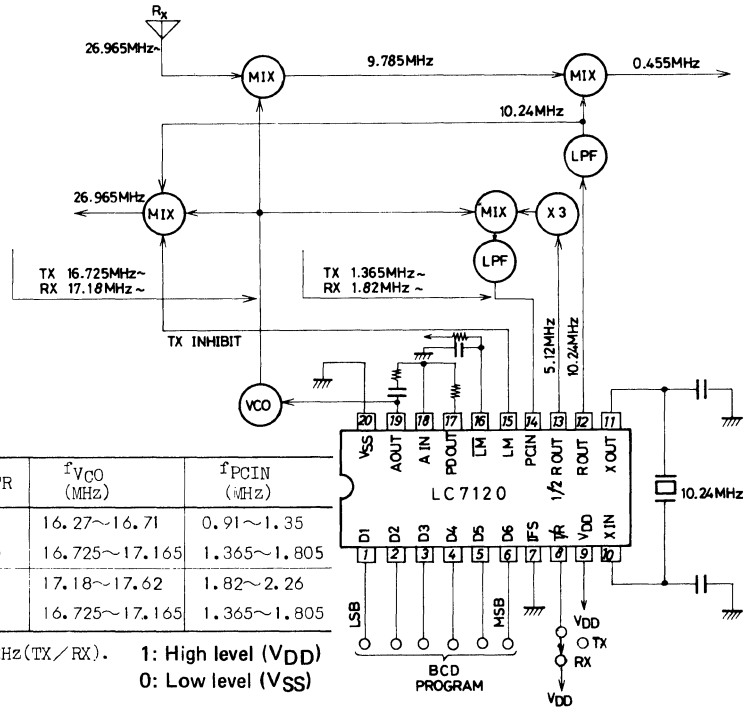
Equivalent Circuit Block Diagram



Pin Name

D1 to D6	Program input (BCD) D1 ----- LSB D6 ----- MSB
T/R	Transmission/reception select input
IFS	IF select input
AIN	Low-pass filter amp input
A OUT	Low-pass filter amp output
$\overline{LM}$	Lock monitor output (Unlock: Low)
LM	Lock monitor output (Unlock: High)
V_{SS}	GND
V_{DD}	Power supply
PD OUT	Phase detector output
1/2R OUT	1/2 reference frequency output
R OUT	Reference frequency output
XIN	Crystal oscillator input
XOUT	Crystal oscillator output
PCIN	Programmable divider input

■ Sample Application Circuit



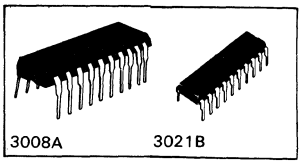
IF Frequency (MHz)	IFs	TR	f_{VCO} (MHz)	f_{PCIN} (MHz)
10.695	1	1	16.27～16.71	0.91～1.35
		0	16.725～17.165	1.365～1.805
9.785	0	1	17.18～17.62	1.82～2.26
		0	16.725～17.165	1.365～1.805

$f_{ref(PD)}$: 5kHz／5kHz(TX／RX).

1: High level (V_{DD})
0: Low level (V_{SS})

T/R: R_X when V_{DD} is applied
T_X when open or V_{SS} is applied

LC7131, -5, -6, -7



C MOS LSI

CB Transceiver PLL Frequency Synthesizer

Ⓔ 1171A

Use

PLL frequency synthesizer LSI for 27MHz CB transceivers (U.S. standard, 40ch: LC7131), (European standard, 22ch: LC7135), (U.K. standard, 40ch: LC7136, 37)

Functions, features

1. Built-in high speed programmable divider for direct PLL system.
2. PLL out-of-lock output available to inhibit transmittion.
3. Instantaneous call capability of channel 9 and 19.
4. Built-in detecting circuit of mis-program.
5. Built-in amplifier for crystal oscillator.
6. Built-in amplifier for active low-pass filter.
7. BCD code channel selection. (Pull-down resistors included)

Description of functions

- Digital Out-of-Lock Output

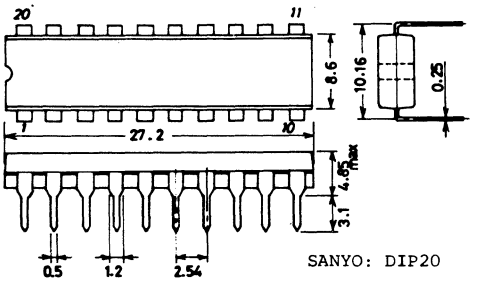
  In direct PLL system, phase difference signal's pulse width at channel change is too narrow, so it is difficult to get out-of-lock signal from phase detector in the way of using C, R components externally.

  LC7131, 7135, 7136 and 7137 make it possible to output the out-of-lock signal to have digital discriminate-expander of the pulse from phase detector internally (Detects the phase difference signal over 1.6μs pulse width, and makes it expand to 6ms output pulse).

  And also LC7131, 7135, 7136 and 7137 output the out-of-lock signal when the phase difference signal is within 1.6μs to have the detector of channel change input.

Case Outline 3021B-D20SIC
(unit:mm)

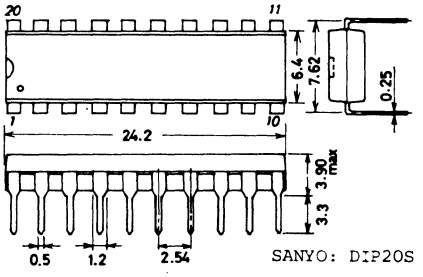
[LC7131/35/36]



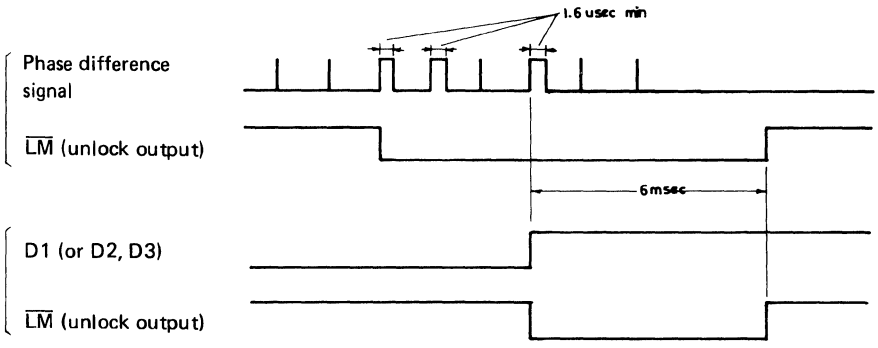
SANYO: DIP20

Case Outline 3008A-D20IC
(unit:mm)

[LC7137]



SANYO: DIP20S



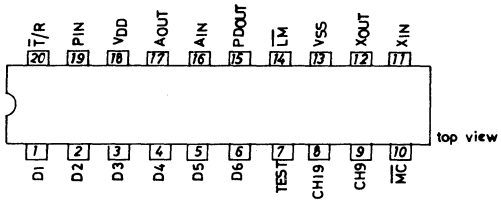
- Instantaneous call of channel 9, 19 and recourse against miscode.
  - Setting CH9 at "H" level causes channel 9 and setting CH19 at "H" level causes channel 19 to be selected.
  - Inputting miscode to D1 to D6 causes channel 9 to occur, and $\overline{MC}$ output to be "L" level.
  - The following table shows the transmitting/receiving channel corresponding to the combination of D1 to D6 and CH9 , 19.

Input			Output	
Data of D1 to D6	CH19	CH9	Channel	$\overline{MC}$
BCD code 0 to 39 (LC7131/36/37) 1 to 22 (LC7135)	0	0	Channel depending on D1 to D6	1
	0	1	Channel 9	1
	1	0	Channel 19	1
	1	1	Channel 19	1
Error program	0	0	Channel 9	0
	0	1	Channel 9	1
	1	0	Channel 19	1
	1	1	Channel 19	1

1: "H" level
0: "L" level

- Built-in amplifier for active low-pass filter
  In direct PLL system, active low-pass filter is more available, as lock-up-time of PLL using active low-pass filter is shorter than the one using passive low-pass filter. The LC7131, 7135, 7136 and 7137 contains an N channel open drain amplifier for active filter in order to make lockup time shorter.
- Channel Programming by BCD code.
  Scan type transciever can be conposed using LC7181/7191. (LC7131/36/37)

Pin Assignment



Absolute Maximum Ratings/ T_a=25°C

					unit
Maximum Supply Voltage	$V_{DD}max$			−0.3~+8.0	V
Maximum Input Voltage	$V_{IN}max$			−0.3~V_{DD}+0.3	V
Maximum Output Voltage	$V_{OUT}(1)$	$\overline{MC}$, $\overline{LM}$, A_{OUT},	output off	−0.3~+10.0	V
	$V_{OUT}(2)$	PD_{OUT},	〃	−0.3~V_{DD}+0.3	V

Maximum Output Current	$I_{OUT}(1)$	$\overline{MC}$, $\overline{LM}$	0~15	mA	
	$I_{OUT}(2)$	A_{OUT}	0~2.5	mA	
Allowable Power Dissipation	$P_d max$	T_a=70°C	300	mW	
Operating Temperature	T_{opg}		−30~+70	°C	
Storage Temperature	T_{stg}		−40~+125	°C	

Allowable Operating Ranges/T_a=25°C

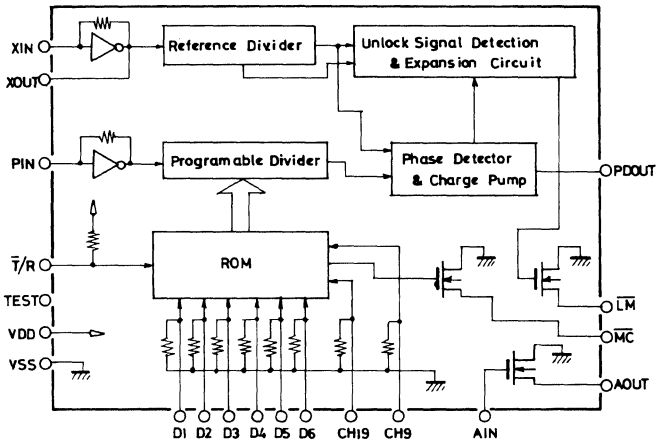
			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=−30~+70 °C	5.0	6.0	7.0	V
Output Voltage	V_{OUT}	$\overline{MC}$, $\overline{LM}$, A_{OUT}, output off	0		9.0	V
Input Amplitude	$V_{IN}(1)$	XIN, ✳, $f_{IN}(1)$=10.25MHz	1.0		0.9V_{DD}	V_{p-p}
	$V_{IN}(2)$	PIN, ✳, $f_{IN}(2)$=20MHz	1.0		0.9V_{DD}	V_{p-p}
Input Frequency	$f_{IN}(1)$	XIN, ✳, $V_{IN}(1)$=1.0V_{p-p}	1.0		10.25	MHz
	$f_{IN}(2)$	PIN, ✳, $V_{IN}(2)$=1.0V_{p-p}	1.0		20	MHz
Input "H" Level Voltage	V_{IH}	D1~D6, $\overline{T}$/R, CH9, CH19	V_{DD}−0.8			V
Input "L" Level Voltage	V_{IL}	〃 〃			0.8	V

Note*: Sinusoidal wave, capacitive coupling, T_a=−30 to +70°C

Electrical Characteristics/T_a=25°C, V_{DD}=5 to 7V.

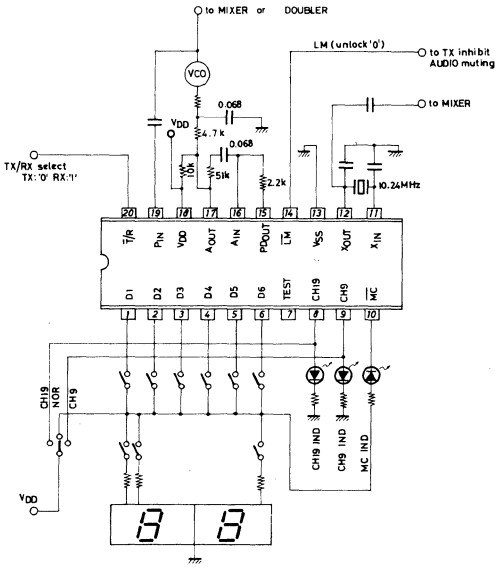
				min	typ	max	unit
Input "H" Level Current	$I_{IH}(1)$	XIN, PIN	V_{IN}=V_{DD}			8.0	μA
Input "L" Level Current	$I_{IL}(1)$	〃	V_{IN}=V_{SS}			8.0	μA
Feedback Resistance	R_F	〃			3.0		MΩ
Input Threshold Voltage	V_{th}	〃			½V_{DD}		V
Input "H" Level Current	$I_{IH}(2)$	D1~D6, CH9, CH19	V_{IN}=V_{DD}	60	180	500	μA
Input Floating Voltage	$V_{IF}(1)$	D1~D6, CH9, CH19	Input pins open			0.2	V
Input "L" Level Current	$I_{IL}(2)$	$\overline{T}$/R	V_{IN}=V_{SS}	40	140	400	μA
Input Floating Voltage	$V_{IF}(2)$	〃	Input pin open	V_{DD}−0.2			V
Input "H" Level Current	$I_{IH}(3)$	AIN	V_{IN}=V_{DD}		0.01		nA
Input "L" Level Current	$I_{IL}(3)$	〃	V_{IN}=V_{SS}		0.01		nA
"H" Level 3-state Leak Current	I_{OFFH}	PD_{OUT}	V_{OUT}=V_{DD}		0.01		nA
"L" Level 3-state Leak Current	I_{OFFL}	〃	V_{OUT}=V_{SS}		0.01		nA
Output "H" Level Current	$V_{OH}(1)$	〃	I_{OUT}=0.3mA	V_{DD}−1.0			V
Output "L" Level Voltage	$V_{OL}(1)$	〃	〃			1.0	V
Output "H" Level Voltage	$V_{OH}(2)$	XOUT	I_{OUT}=0.5mA	V_{DD}-0.35			V
Output "L" Level Voltage	$V_{OL}(2)$	〃	〃		0.35		V
Output "L" Level Voltage	$V_{OL}(3)$	A_{OUT}	〃			0.3	V
Output Off Leak Current	$I_{OFF}(1)$	〃	V_{OUT}=9V			3.0	μA
Output "L" Level Voltage	$V_{OL}(4)$	$\overline{MC}$, $\overline{LM}$	I_{OUT}=15mA			1.1	V
Output Off Leak Current	$I_{OFF}(2)$	〃	V_{OUT}=9V			5.0	μA
Current Dissipation	I_{DD}		$f_{IN}(1)$=10.25MHz, $f_{IN}(2)$=20MHz, $V_{IN}(1)$=$V_{IN}(2)$=1.0V_{p-p}, A_{IN}=V_{SS}, D1=V_{DD}, Other pins open, Number of frequency		10	20	mA

Equivalent Circuit and Block Diagram



D1 to D6:	Program input (BCD) D1.....LSB, D6.....MSB
X_{IN}, X_{OUT}:	Amplifier for crystal oscillator
V_{DD}, V_{SS}:	Power Supply
$\overline{MC}$:	Miscode Indication Output
$\overline{LM}$:	Lock Monitor output Lock.....open "1", unlock....."0"
PD_{OUT}:	Charge pump output
A_{IN}, A_{OUT}:	Amplifier for low-pass filter
P_{IN}:	Programmable divider input
$\overline{T}$/R:	Transmission/reception changeover input
	$\overline{T}$/R="0".....Transmission $\overline{T}$/R="1"
	$\overline{T}$/R="1" (or open).....reception
CH19:	Channel 19 select input
CH9:	Channel 9 select input
TEST:	LSI test pin (TEST pin: Connected to V_{SS} or open)

■ **Application Circuit**



LC7131 Program Data and Frequency Division

Channel No.	PROGRAM CODE D1	D2	D3	D4	D5	D6	RX($\overline{T}$/R='1') N	F_{VCO} (MHz)	TX($\overline{T}$/R='0') N	F_{VCO} (MHz)
1	1	0	0	0	0	0	3254	16.27	3345	16.725
2	0	1	0	0	0	0	3256	16.28	3347	16.735
3	1	1	0	0	0	0	3258	16.29	3349	16.745
4	0	0	1	0	0	0	3262	16.31	3353	16.765
5	1	0	1	0	0	0	3264	16.32	3355	16.775
6	0	1	1	0	0	0	3266	16.33	3357	16.785
7	1	1	1	0	0	0	3268	16.34	3359	16.795
8	0	0	0	1	0	0	3272	16.36	3363	16.815
9	1	0	0	1	0	0	3274	16.37	3365	16.825
10	0	0	0	0	1	0	3276	16.38	3367	16.835
11	1	0	0	0	1	0	3278	16.39	3369	16.845
12	0	1	0	0	1	0	3282	16.41	3373	16.865
13	1	1	0	0	1	0	3284	16.42	3375	16.875
14	0	0	1	0	1	0	3286	16.43	3377	16.885
15	1	0	1	0	1	0	3288	16.44	3379	16.895
16	0	1	1	0	1	0	3292	16.46	3383	16.915
17	1	1	1	0	1	0	3294	16.47	3385	16.925
18	0	0	0	1	1	0	3296	16.48	3387	16.935
19	1	0	0	1	1	0	3298	16.49	3389	16.945
20	0	0	0	0	0	1	3302	16.51	3393	16.965
21	1	0	0	0	0	1	3304	16.52	3395	16.975
22	0	1	0	0	0	1	3306	16.53	3397	16.985
23	1	1	0	0	0	1	3312	16.56	3403	17.015
24	0	0	1	0	0	1	3308	16.54	3399	16.995
25	1	0	1	0	0	1	3310	16.55	3401	17.005
26	0	1	1	0	0	1	3314	16.57	3405	17.025
27	1	1	1	0	0	1	3316	16.58	3407	17.035
28	0	0	0	1	0	1	3318	16.59	3409	17.045
29	1	0	0	1	0	1	3320	16.60	3411	17.055
30	0	0	0	0	1	1	3322	16.61	3413	17.065
31	1	0	0	0	1	1	3324	16.62	3415	17.075
32	0	1	0	0	1	1	3326	16.63	3417	.7.085
33	1	1	0	0	1	1	3328	16.64	3419	17.095
34	0	0	1	0	1	1	3330	16.65	3421	17.105
35	1	0	1	0	1	1	3332	16.66	3423	17.115
36	0	1	1	0	1	1	3334	16.67	3425	17.125
37	1	1	1	0	1	1	3336	16.68	3427	17.135
38	0	0	0	1	1	1	3338	16.69	3429	17.145
39	1	0	0	1	1	1	3340	16.70	3431	17.155
40	0	0	0	0	0	0	3342	16.71	3433	17.165

LC7135 Program Data and Frequency Division

1	1	0	0	0	0	0	3254	16.27	3345	16.725
2	0	1	0	0	0	0	3256	16.28	3347	16.735
3	1	1	0	0	0	0	3258	16.29	3349	16.745
4	0	0	1	0	0	0	3262	16.31	3353	16.765
5	1	0	1	0	0	0	3264	16.32	3355	16.775
6	0	1	1	0	0	0	3266	16.33	3357	16.785
7	1	1	1	0	0	0	3268	16.34	3359	16.795
8	0	0	0	1	0	0	3272	16.36	3363	16.815
9	1	0	0	1	0	0	3274	16.37	3365	16.825
10	0	0	0	0	1	0	3276	16.38	3367	16.835
11	1	0	0	0	1	0	3278	16.39	3369	16.845
12	0	1	0	0	1	0	3282	16.41	3373	16.865
13	1	1	0	0	1	0	3284	16.42	3375	16.875
14	0	0	1	0	1	0	3286	16.43	3377	16.885
15	1	0	1	0	1	0	3288	16.44	3379	16.895
16	0	1	1	0	1	0	3292	16.46	3383	16.915
17	1	1	1	0	1	0	3294	16.47	3385	16.925
18	0	0	0	1	1	0	3296	16.48	3387	16.935
19	1	0	0	1	1	0	3298	16.49	3389	16.945
20	0	0	0	0	0	1	3302	16.51	3393	16.965
21	1	0	0	0	0	1	3304	16.52	3395	16.975
22	0	1	0	0	0	1	3306	16.53	3397	16.985

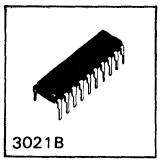
'1': logical high level
'0': logical low level

LC7136/37 Program Data and Frequency Division

Channel No.	PROGRAM CODE D1	D2	D3	D4	D5	D6	RX(T/R="1") N	TX(T/R="0") N
1	1	0	0	0	0	0	3381	2760
2	0	1	0	0	0	0	3383	2761
3	1	1	0	0	0	0	3385	2762
4	0	0	1	0	0	0	3387	2763
5	1	0	1	0	0	0	3389	2764
6	0	1	1	0	0	0	3391	2765
7	1	1	1	0	0	0	3393	2766
8	0	0	0	1	0	0	3395	2767
9	1	0	0	1	0	0	3397	2768
10	0	0	0	0	1	0	3399	2769
11	1	0	0	0	1	0	3401	2770
12	0	1	0	0	1	0	3403	2771
13	1	1	0	0	1	0	3405	2772
14	0	0	1	0	1	0	3407	2773
15	1	0	1	0	1	0	3409	2774
16	0	1	1	0	1	0	3411	2775
17	1	1	1	0	1	0	3413	2776
18	0	0	0	1	1	0	3415	2777
19	1	0	0	1	1	0	3417	2778
20	0	0	0	0	0	1	3419	2779
21	1	0	0	0	0	1	3421	2780
22	0	1	0	0	0	1	3423	2781
23	1	1	0	0	0	1	3425	2782
24	0	0	1	0	0	1	3427	2783
25	1	0	1	0	0	1	3429	2784
26	0	1	1	0	0	1	3431	2785
27	1	1	1	0	0	1	3433	2786
28	0	0	0	1	0	1	3435	2787
29	1	0	0	1	0	1	3437	2788
30	0	0	0	0	1	1	3439	2789
31	1	0	0	0	1	1	3441	2790
32	0	1	0	0	1	1	3443	2791
33	1	1	0	0	1	1	3445	2792
34	0	0	1	0	1	1	3447	2793
35	1	0	1	0	1	1	3449	2794
36	0	1	1	0	1	1	3451	2795
37	1	1	1	0	1	1	3453	2796
38	0	0	0	1	1	1	3455	2797
39	1	0	0	1	1	1	3457	2798
40	0	0	0	0	0	0	3459	2799

"1" : logical high level
"0" : logical low level

LC7132



C MOS LSI

CB Transceiver PLL Frequency Synthesizer

Ⓔ 1190A

Use

PLL frequency synthesizer LSI for 27MHz CB transceivers (U.S. standard).

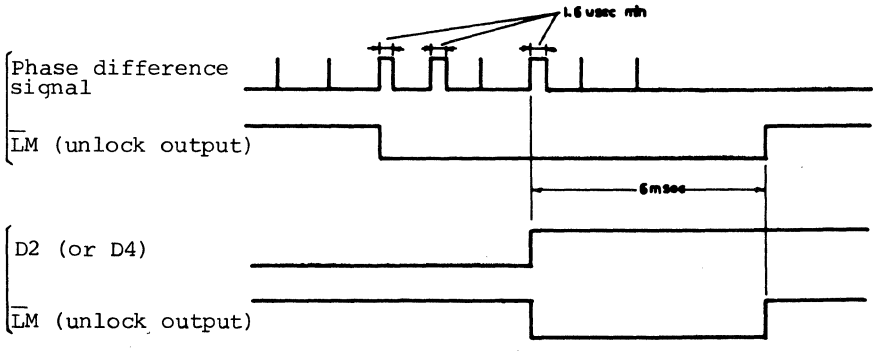
Functions, features

1. Built-in high speed programmable divider for direct PLL system.
2. Doubled-frequency of VCO applicable as transmitting frequency carrier.
3. PLL out-of-lock output available to inhibit transmittion.
4. Instantaneous call capability of channel 9.
5. Built-in detecting circuit of mis-program.
6. Built-in amplifier for crystal oscillator.
7. Built-in amplifier for active low-pass filter.
8. 7-segment code channel selection. (allowable voltage 15V)

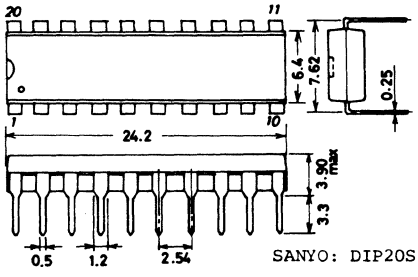
Description of functions

. Digital Out-of-Lock Output

In direct PLL system, phase difference signal's pulse width at channel change is too narrow, so it is difficult to get out-of-lock signal from phase detector in the way of using C,R components externally.
LC7132 makes it possible to output the out-of-lock signal to have digital discriminate-expander of the pulse from phase detector internally (Detects the phase difference signal over 1.6us pulse width, and makes it expand to 6ms output pulse).
And also LC7132 outputs the out-of-lock signal when the phase difference signal is within 1.6us to have the detector of channel change input.



Case Outline
3021B-D20SIC
(unit:mm)



SANYO: DIP20S

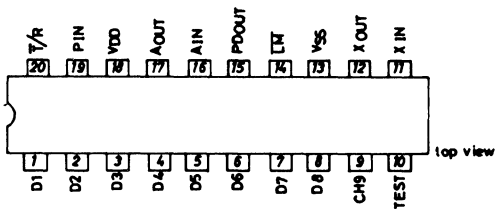
. Instantaneous call of channel 9 and recourse against miscode.
  .Setting CH9 at "H" level causes channel 9 to be selected.
  .Inputting miscode to D1 to D8 causes channel 19 to occur.
  .The following table shows the transmitting/receiving channel corresponding to the combination of D1 to D8 and CH9.

Input		Output
Data of D1 to D8	CH9	Channel
Normal code	0	Channel depending on D1 to D8
	1	Channel 9
Error program	0	Channel 19
	1	Chanel 9

1 : "H" level
0 : "L" level

. Built-in amplifier for active low-pass filter
In direct PLL system, active low-pass filter is more available, as lock-up-time of PLL using active low-pass filter is shorter than the one using passive low-pass filter. The LC7132 contains an N channel open drain amplifier for active filter in order to make lockup time shorter.

Pin Assignment



Absolute Maximum Ratings at T_a=25°C

				unit
Maximum Supply Voltage	$V_{DD}max$		-0.3 to +9.0	V
Maximum Input Voltage	$V_{IN}max(1)$	D1 to D8,CH9	-0.3 to +17	V
	$V_{IN}max(2)$	Input pins other than above.	-0.3 to V_{DD}+0.3	V
Maximum Output Voltage	$V_{OUT}(1)$	$\overline{LM}$, AOUT, output off	-0.3 to +10.0	
	$V_{OUT}(2)$	PDOUT,AOUT, output off	-0.3toV_{DD}+0 3	V
Maximum Output Current	$I_{OUT}(1)$	$\overline{LM}$	0 to 15	mA
	$I_{OUT}(2)$	AOUT	0 to 2.5	mA
Allowable Power Dissipation	Pdmax	T_a=70°C	300	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at T_a=25°C

			min	typ	max	unit
Supply Voltage	V_{DD}	Ta=-30 to +70°C	5.0		8.0	V
Output Voltage	V_{OUT}	$\overline{LM}$,A_{OUT},output off	0		9.0	V
Input Amplitude	$V_{IN}(1)$	X_{IN},*,$f_{IN}(1)$=10.25MHz	1.0		0.9V_{DD}	Vp-p
	$V_{IN}(2)$	P_{IN},*,$f_{IN}(2)$=20MHz	1.0		0.9V_{DD}	Vp-p
Input Frequency	$f_{IN}(1)$	X_{IN},*,$V_{IN}(1)$=1.0Vp-p	1.0		10.25	MHz
	$f_{IN}(2)$	P_{IN},*,$V_{IN}(2)$=1.0Vp-p	1.0		20	MHz
Input "H" Level Voltage	$V_{IH}(1)$	D1 to D8,CH9	0.8V_{DD}		15	V
	$V_{IH}(2)$	$\overline{T}$/R	0.7V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL}(1)$	D1 to D8,CH9	0		0.4V_{DD}	V
	$V_{IL}(2)$	$\overline{T}$/R	0		0.3V_{DD}	V

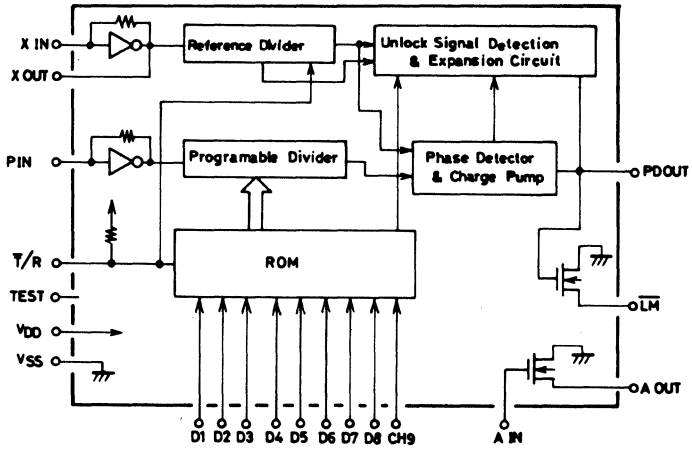
Note * : Sinusoidal wave, capacitive coupling, T_a=-30 to +70°C

Electrical Characteristics at T_a=25°C,V_{DD}=5 to 8V

				min	typ	max	unit
Input "H" Level Current	$I_{IH}(1)$	X_{IN},P_{IN}	V_{IN}=V_{DD}			40	uA
Input "H" Level Current	$I_{IH}(2)$	D1 to D8,CH9	V_{IN}=15V			5.0	uA
Input "H" Level Current	$I_{IH}(3)$	A_{IN}	V_{IN}=V_{DD}		0.01		nA
Input "L" Level Current	$I_{IL}(1)$	X_{IN},P_{IN}	V_{IN}=V_{SS}			40	uA
	$I_{IL}(2)$	D1 to D8,CH9	V_{IN}=V_{SS}			5.0	uA

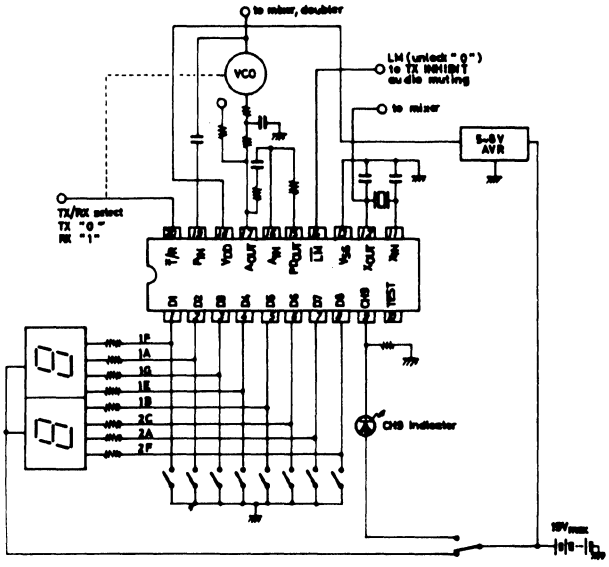
				min	typ	max	unit
Input "L" Level Current	$I_{IL}(3)$	$\overline{T}/R$	$V_{IN}=V_{SS}$	40	200	500	uA
	$I_{IL}(4)$	A_{IN}	$V_{IN}=V_{SS}$		0.01		nA
Output "H" Level Voltage	V_{OH}	PD_{OUT}	$I_{OUT}=0.3mA$	$V_{DD}-1.0$			V
Output "L" Level Voltage	$V_{OL}(1)$	PD_{OUT}	$I_{OUT}=0.3mA$			1.0	V
	$V_{OL}(2)$	A_{OUT}	$I_{OUT}=0.5mA$			0.3	V
	$V_{OL}(3)$	$\overline{LM}$	$I_{OUT}=15mA$			1.1	V
Feedback Resistance	$R_F(1)$	X_{IN}			1.0		Mohm
	$R_F(2)$	P_{IN}			0.5		Mohm
Input Threshold Voltage	V_{th}				$1/2V_{DD}$		V
"H"Level 3-State Leak Current	I_{OFFH}	PD_{OUT}	$V_{OUT}=V_{DD}$		0.01		nA
"L" Level 3-State Leak Current	I_{OFFL}	PD_{OUT}	$V_{OUT}=V_{SS}$		0.01		nA
Input Floating Voltage	$V_{IF}(1)$	$\overline{T}/R$	Input pins open	$V_{DD}-0.2$			V
Output Off Leak Current	$I_{OFF}(1)$	A_{OUT}	$V_{OUT}=9V$			3.0	uA
	$I_{OFF}(2)$	$\overline{LM}$	$V_{OUT}=9V$			5.0	uA
Current Dissipation	I_{DD}		$f_{IN}(1)=10.25MHz$, $f_{IN}(2)=20MHz$, $V_{IN}(1)=V_{IN}(2)=1.0Vp-p$ CH9=$A_{IN}=V_{SS}$, D1 to D4, D6 to D8=V_{DD}, D5=V_{SS}, Other pins open, Number of frequency divisions=3254		10	20	mA

Equivalent Circuit and Block Diagram



D1 to D8 : Program input (7-segment code)
X_{IN}, X_{OUT} : Amplifier for crystal oscillator
V_{DD}, V_{SS} : Power Supply
$\overline{LM}$: Lock monitor output Lock--open"1",unlock--"0"
PD_{OUT} : Charge pump output
A_{IN}, A_{OUT} : Amplifier for low-pass filter
P_{IN} : Programmable divider input
$\overline{T}/R$: Transmission/reception changeover input
$\overline{T}/R$="0"---Transmission $\overline{T}/R$="1"
$\overline{T}/R$="1"(or open)---reception
CH9 : Channel 9 select input
TEST : LSI test pin (TEST pin:Connected to V_{SS} or open)

Application Circuit

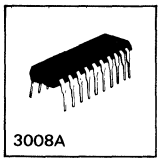


Program Data and Frequency Division

Channel No.	PROGRAM CODE D1 (1F)	D2 (1A)	D3 (1G)	D4 (1E)	D5 (1B)	D6 (2C)	D7 (2A)	D8 (2F)	RX ($\overline{T}$/R="1") N	F_{VCO} (MHz)	TX ($\overline{T}$/R="0") N	F_{VCO} (MHz)
1	1	1	1	1	0	1	1	1	3254	16.27	5393	13.4825
2	1	0	0	0	0	1	1	1	3256	16.28	5395	13.4875
3	1	0	0	1	0	1	1	1	3258	16.29	5397	13.4925
4	0	1	0	1	0	1	1	1	3262	16.31	5401	13.5025
5	0	0	0	1	1	1	1	1	3264	16.32	5403	13.5075
6	0	0	0	0	1	1	1	1	3266	16.33	5405	13.5125
7	-	0	1	1	0	1	1	1	3268	16.34	5407	13.5175
8	0	0	0	0	0	1	1	1	3272	16.36	5411	13.5275
9	0	0	0	1	0	1	1	1	3274	16.37	5413	13.5325
10	0	0	1	0	0	0	1	1	3276	16.38	5415	13.5375
11	1	1	1	1	0	0	1	1	3278	16.39	5417	13.5425
12	1	0	0	0	0	0	1	1	3282	16.41	5421	13.5525
13	1	0	0	1	0	0	1	1	3284	16.42	5423	13.5575
14	0	1	0	1	0	0	1	1	3286	16.43	5425	13.5625
15	0	0	0	1	1	0	1	1	3288	16.44	5427	13.5675
16	0	0	0	0	1	0	1	1	3292	16.46	5431	13.5775
17	-	0	1	1	0	0	1	1	3294	16.47	5433	13.5825
18	0	0	0	0	0	0	1	1	3296	16.48	5435	13.5875
19	0	0	0	1	0	0	1	1	3298	16.49	5437	13.5925
20	0	0	1	0	0	1	0	1	3302	16.51	5441	13.6025
21	1	1	1	1	0	1	0	1	3304	16.52	5443	13.6075
22	1	0	0	0	0	1	0	1	3306	16.53	5445	13.6125
23	1	0	0	1	0	1	0	1	3312	16.56	5451	13.6275
24	0	1	0	1	0	1	0	1	3308	16.54	5447	13.6175
25	0	0	0	1	1	1	0	1	3310	16.55	5449	13.6225
26	0	0	0	0	1	1	0	1	3314	16.57	5453	13.6325
27	-	0	1	1	0	1	0	1	3316	16.58	5455	13.6375
28	0	0	0	0	0	1	0	1	3318	16.59	5457	13.6425
29	0	0	0	1	0	1	0	1	3320	16.60	5459	13.6475
30	0	0	1	0	0	0	0	1	3322	16.61	5461	13.6525
31	1	1	1	1	0	0	0	1	3324	16.62	5463	13.6575
32	1	0	0	0	0	0	0	1	3326	16.63	5465	13.6625
33	1	0	0	1	0	0	0	1	3328	16.64	5467	13.6675
34	0	1	0	1	0	0	0	1	3330	16.65	5469	13.6725
35	0	0	0	1	1	0	0	1	3332	16.66	5471	13.6775
36	0	0	0	0	1	0	0	1	3334	16.67	5473	13.6825
37	-	0	1	1	0	0	0	1	3336	16.68	5475	13.6875
38	0	0	0	0	0	0	0	1	3338	16.69	5477	13.6925
39	0	0	0	1	0	0	0	1	3340	16.70	5479	13.6975
40	0	0	1	0	0	0	1	0	3342	16.71	5481	13.7025

"1" : logical high level
"0" : logical low level
"-" : don't care

LC7181, 7191


3008A

C MOS LSI

CB Transceiver Channel Selecting System

Ⓔ 669B

General Description

The LC7181 and LC7191 make a pair to form a channel scan system of 40-channel CB transceivers. The LC7181 contains an up/down counter for channel memory and a channel output ROM. The LC7191 contains a channel indication decoder and an LED driver.

Features

- The following 3 methods are available for 40-channel transceiver channel select.
  a: Manual scan b: Auto scan c: Auto search
- For forming a scan system where the microphone unit has the channel indicator, only 5 more lines are required to connect the main body to the microphone unit.
- Almost no noise because of static driving of LED.
- Instantaneous call capability of emergency channel (CH9).
- Capable of stopping the channel scan operation at the transmission mode.
- "PA" indication available in applications where the transceiver is used as a loudspeaker.
- LED driver capable of static driving of LED (15mA/V).

Functions

(1) Manual scan: Each time the UP SW/DOWN SW is pushed, the channel goes up/down by one.

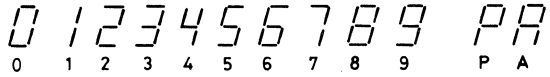
(2) Auto scan: Pushing the UP SW/DOWN SW for 1 second or more causes the channel to go up/down at a 6Hz rate.

(3) Auto search: Simultaneous push of the UP SW/DOWN SW causes the channel to advance fast (up). Applying the squelch signal to the $\overline{\text{PAUSE}}$ pin causes automatic stop when an idle channel is reached.

(4) Emergency channel: Applying the emergency signal to the $\overline{\text{CH9}}$ pin calls CH9. When the emergency signal disappears, the channel used before applying the signal returns.

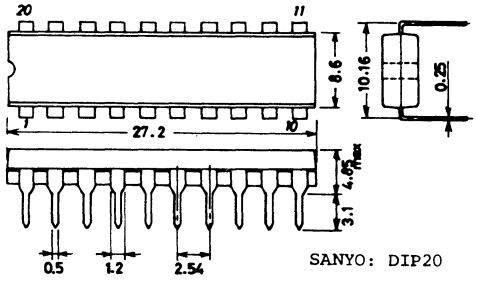
(5) Channel hold when in the transmission mode: Applying a signal to the $\overline{\text{TXI}}$ pin when in the transmission mode inhibits the channel from moving even if the UP SW/DOWN SW is pushed.

(6) Channel indication: a. 7-segment LED's are lighted in the display font shown below. 0 in the high-order digit is blanked out.
b. "PA" indication is available in applications where the transceiver is used as a loudspeaker.



(7) Connection between LC7181 and LC7191: One-shot data transfer is done through 2 lines. In applications where the microphone unit has the channel indicator, only 5 more lines are required to connect the main body and the microphone unit.

Case Outline 3008A-D20IC
(unit: mm)



SANYO: DIP20

Absolute Maximum Ratings/T_a=25°C

				unit
Maximum Supply Voltage	V_{DDmax}		−0.3～+9.0	V
Maximum Input Voltage	V_{INmax}		−0.3～V_{DD}+0.3	V
Maximum Output Voltage	V_{OUTmax}	Output OFF	−0.3～V_{DD}+0.3	V
Output "L" Level Current	I_{OLmax}	LC7191, LED current Pins: $\overline{a}$～$\overline{g}$, $\overline{10a}$～$\overline{10g}$	0～25	mA
Operating Temperature	Topg		−30～+70	°C
Storage Temperature	Tstg		−40～+125	°C

Note: No voltage shall be applied across I/O and V_{DD} with V_{SS} open.
No voltage shall be applied across I/O and V_{SS} with V_{DD} open.

Allowable Operating Ranges/T_a=25°C

				unit
Supply Voltage	V_{DD}	Electrical characteristics at V_{DD}≦6V are specified separately.	4.5～8.0	V
Input "H" Level Voltage	V_{IH}	All input pins	0.85V_{DD}～V_{DD}	V
Input "L" Level Voltage	V_{IL}	Same as above	0～0.15V_{DD}	V

LC7181 Electrical Characteristics/T_a=25°C, V_{DD}=6.0 to 8.0V

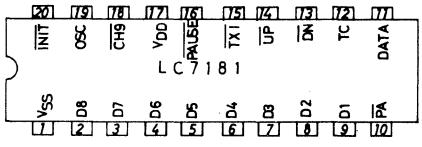
		Pins	Conditions	min	typ	max	unit
Input Floating Voltage	V_{IF}	$\overline{UP}$ $\overline{DN}$ $\overline{TXI}$ $\overline{PAUSE}$ $\overline{CH9}$	Input pin open	V_{DD}−0.7			V
Inout "L" Level Current	I_{IL}	$\overline{UP}$ $\overline{DN}$ $\overline{TXI}$ $\overline{PAUSE}$ $\overline{CH9}$	V_I=0V		250		μA
Output "L" Level Voltage	V_{OL}	TC DATA	I_O=0.5mA			0.5	V
Output OFF Leak Current	I_{OFF1}	TC DATA	V_O=V_{DD}			6.0	μA
	I_{OFF2}	D1～D8	V_O=V_{SS}			6.0	μA
Output "H" Level Voltage	V_{OH}	D1～D8	I_O=0.5mA	V_{DD}−0.5			V
Clock Pulse Cycle	T∅		C=0.015μF (polyester film) R=110kΩ (carbon)		1.17		msec
Current Dissipation	I_{DD}	f_{osc}=850Hz, $\overline{INIT}$=V_{DD} $\overline{PA}$=V_{DD}, other inputs open			1.0		mA

LC7191 Electrical Characteristics/T_a=25°C, V_{DD}=6.0 to 8.0V

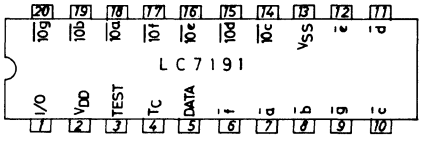
Input "H" Level Current	I_{IH}	TC, DATA	V_I=V_{DD}			5.0	μA
Input "L" Level Current	I_{IL}	TC, DATA	V_I=V_{SS}			5.0	μA
Output "H" Level Voltage	V_{OH}	I/O	I_O=0.5mA	V_{DD}−0.5			V
Output "L" Level Voltage	V_{OL}	$\overline{a}$～$\overline{g}$, $\overline{10a}$～$\overline{10g}$	Io=15mA			1.0	V
Output OFF Leak Current	I_{OFF1}	$\overline{a}$～$\overline{g}$, $\overline{10a}$～$\overline{10g}$	V_O=V_{DD}			50	μA
	I_{OFF2}	I/O	V_O=V_{DD}			6.0	μA
Current Dissipation	I_{DD}		TC, DATA=V_{SS} other pins open		3.0		mA

Pin Assignment

LC7181

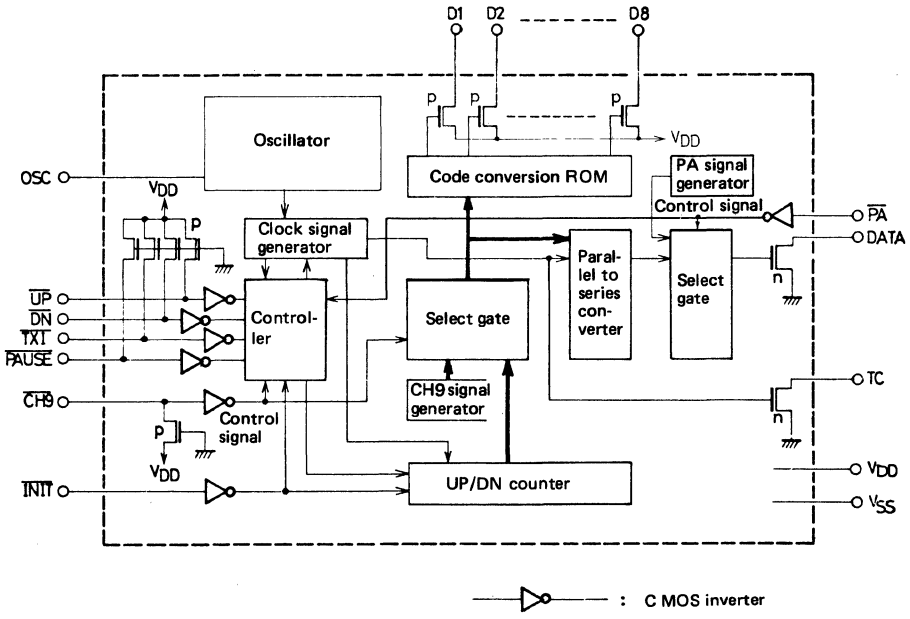


LC7191

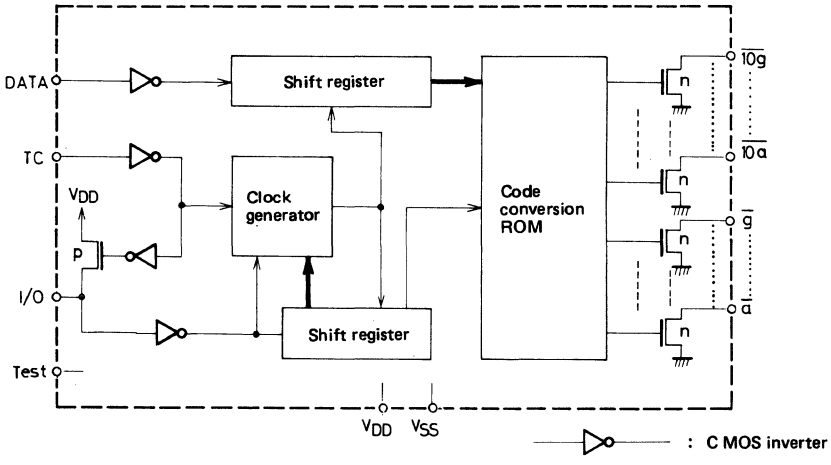


Equivalent Circuit Block Diagram

LC7181



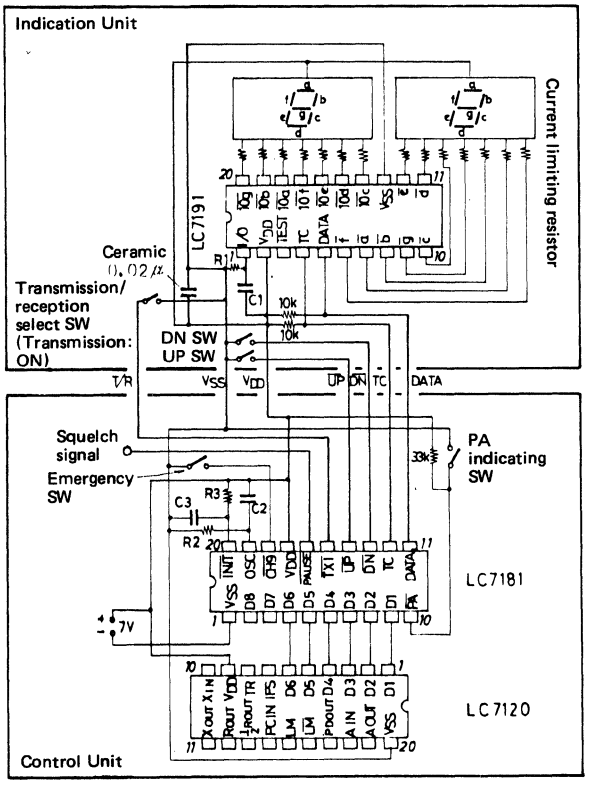
LC7191



LC7181 Channel No. to Data Output (D1 to D8) Correspondence

CH	FREQ.	Frequency Division	PROGRAM DATA (BCD)							
			D1	D2	D3	D4	D5	D6	D7	D8
1	26.965MHz	To be determined by the PLL IC used.	1	0	0	0	0	0	0	0
2	26.975		0	1	0	0	0	0	0	0
3	26.985		1	1	0	0	0	0	0	0
4	27.005		0	0	1	0	0	0	0	0
5	27.015		1	0	1	0	0	0	0	0
6	27.025		0	1	1	0	0	0	0	0
7	27.035		1	1	1	0	0	0	0	0
8	27.055		0	0	0	1	0	0	0	0
9	27.065		1	0	0	1	0	0	0	0
10	27.075		0	0	0	0	1	0	0	0
11	27.085		1	0	0	0	1	0	0	0
12	27.105		0	1	0	0	1	0	0	0
13	27.115		1	1	0	0	1	0	0	0
14	27.125		0	0	1	0	1	0	0	0
15	27.135		1	0	1	0	1	0	0	0
16	27.155		0	1	1	0	1	0	0	0
17	27.165		1	1	1	0	1	0	0	0
18	27.175		0	0	0	1	1	0	0	0
19	27.185		1	0	0	1	1	0	0	0
20	27.205		0	0	0	0	0	1	0	0
21	27.215		1	0	0	0	0	1	0	0
22	27.225		0	1	0	0	0	1	0	0
23	27.255		1	1	0	0	0	1	0	0
24	27.235		0	0	1	0	0	1	0	0
25	27.245		1	0	1	0	0	1	0	0
26	27.265		0	1	1	0	0	1	0	0
27	27.275		1	1	1	0	0	1	0	0
28	27.285		0	0	0	1	0	1	0	0
29	27.295		1	0	0	1	0	1	0	0
30	27.305		0	0	0	0	1	1	0	0
31	27.315		1	0	0	0	1	1	0	0
32	27.325		0	1	0	0	1	1	0	0
33	27.335		1	1	0	0	1	1	0	0
34	27.345		0	0	1	0	1	1	0	0
35	27.355		1	0	1	0	1	1	0	0
36	27.365		0	1	1	0	1	1	0	0
37	27.375		1	1	1	0	1	1	0	0
38	27.385		0	0	0	1	1	1	0	0
39	27.395		1	0	0	1	1	1	0	0
40	27.405		0	0	0	0	0	0	0	0

■ **Sample Application Circuit: LC7181, 7191, 7120-Applied Channel Selector System**

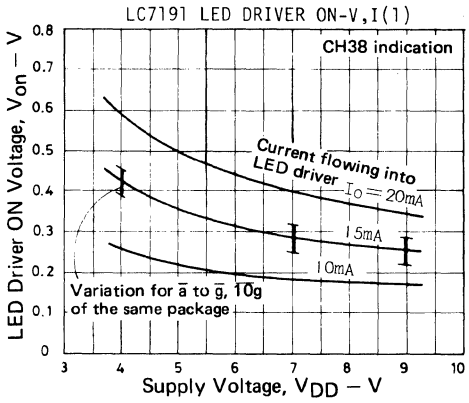


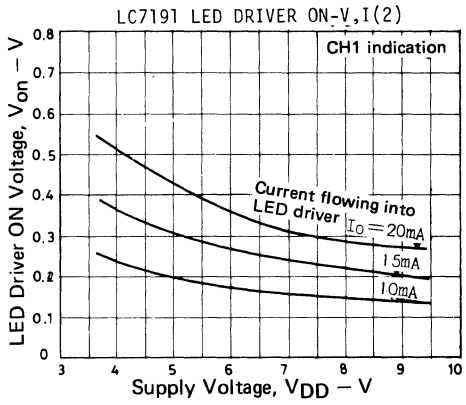
(LC7181, 7191: Scan use, LC7120: Synthesizer use)

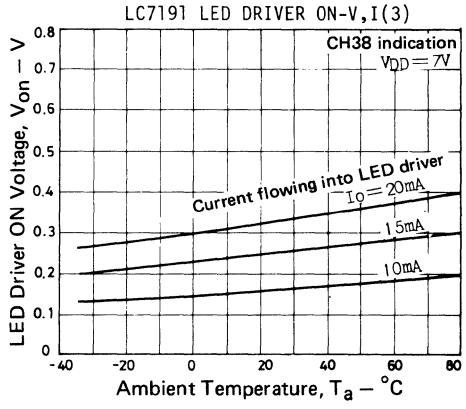
Note: If stabilization in the power supply for LED drive is not necessarily required, a power supply separate from the power supply for the LC7191 can be used. In this case, however, the LED current is not uniform.

C1=0.068μF (Polyester film) R1=180kΩ (Carbon resistor)
C2=0.015μF (Polyester film) R2=110kΩ (Carbon resistor)
C3=To be determined by the rise time of the power supply. (1.0μF for 100msec. of rise time) R3=180kΩ
C4=30pF (Connected when the distance between LC7181 and LC7191 is short)
C5=200pF (Connected when the distance between LC7181 and LC7191 is long)

- **LC7191 LED Driver ON Resistance Characteristic**

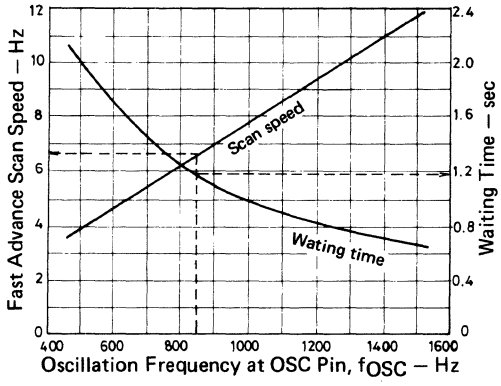






- **How to determine CR constants at LC7181 OSC pin and LC7191 I/O pin**

The OSC pin is for the oscillator that operates the LC7181/91. CR are externally connected to this pin.
The oscillation frequency at this pin determines the waiting time for transfer from manual scan to auto scan and the scan speed of auto scan when the UP SW/DN SW is held pushed.
Oscillation frequency f_{OSC}, the waiting time, and fast advance speed are shown below (Fig. A).



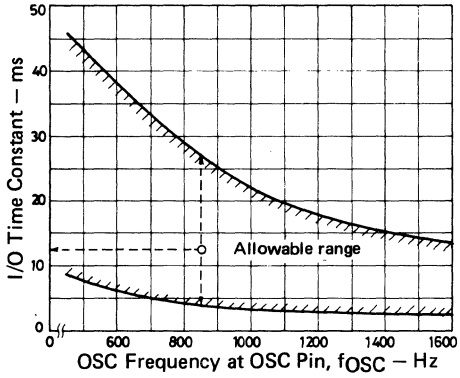
(Fig. A) Oscillation Frequency Characteristic

The fast advance speed should be as fast as possible on condition that the indication is visible. An adequate speed is 6 to 7Hz. If the fast advance speed is 6.7Hz, f_{OSC}≒850Hz and waiting time≒1.2 sec. are yielded.

The I/O pin is for eliminating the noise applied to the TC pin. CR are externally connected to this pin.
The external time constant of the I/O pin (hereinafter referred to as "I/O time constant") is determined by f_{OSC}. The relation between I/O time constant and f_{OSC} is shown in (Fig. B). I/O time constant (typ)=12ms at f_{OSC}= 850Hz.
There are various combinations of CR time constants at the OSC pin and I/O pin that meet f_{OSC} and the I/O time constant. With leak current of the LSI considered, it is desirable that the resistor value should not exceed 100kohm to 200kohm and the capacitor should be as small as possible when we consider the price.
Thus, the combinations of CR constants at the I/O pin are as follows:

(1) R=180kΩ, C=0.068μF (2) R=120kΩ, C=0.1μF (3) R=80kΩ, C=0.15μF

(1) is recommendable as the most low-priced and advantageous combination.
Next, the CR constants at the OSC pin are discussed.
The relation between external CR constants and oscillation frequency f_{OSC} is shown in (Fig. C).



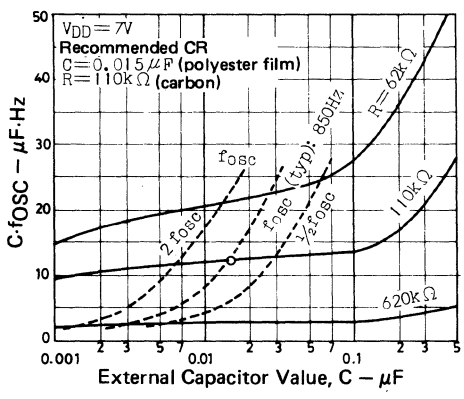
(Fig. B) Allowable Range of I/O Time Constant to OSC Frequency at OSC Pin

f_{OSC} is obtained by dividing a value on the vertical axis by its corresponding value on the transverse axis with regard to each point on the graph.

(Example) Obtaining f_{OSC} for a point marked ° on the curve of R=110kohm
Value on the vertical axis: 12.5 to 13.0μF·Hz
Value on the transverse axis: 0.015μF
Therefore, f_{OSC}=12.5 to 13.0/0.015=833 to 866(Hz)

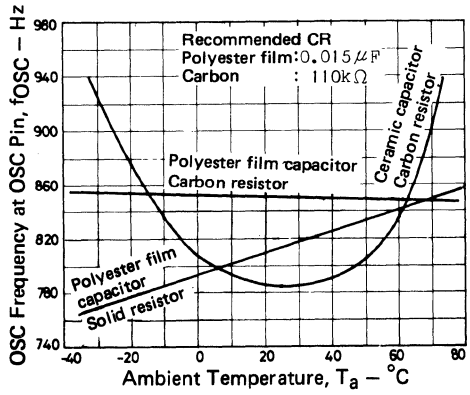
In an ideal oscillator, f_{OSC} is proportional to 1/CR. Therefore, C·f_{OSC} is proportional to 1/CR. If the resistor value is made constant, C·f_{OSC} becomes also constant. As seen from (Fig. C), the larger the resistor value is, the wider the linear region becomes. It is more desirable to make the resistor value larger. With leak current of the LSI considered, it is desirable that the resistor value should not exceed 100kohm to 200kohm and the combinations of CR constants to obtain f_{OSC}=850Hz are as follows:

(1) R=160kΩ, C=0.01μF (2) R=110kΩ, C=0.015μF (3) R=75kΩ, C=0.022μF

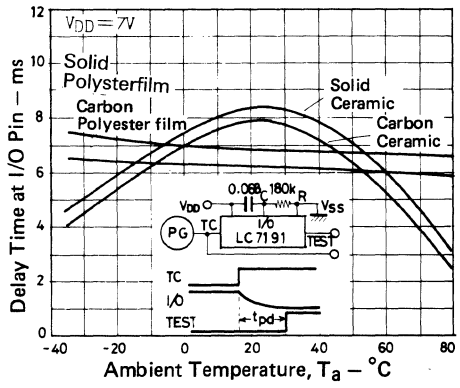


(Fig. C) C·f_{OSC} – C

(2) is recommendable for CR constants at the OSC pin because this combination is the most low-priced and suitable in terms of leak current. Next, what parts should be used when the f_{OSC}, I/O time constant to temperature characteristic is considered is discussed.
With the fast advance speed of scan and the relation between f_{OSC} and I/O time constant considered, less dependence of f_{OSC} and I/O time constant on temperature is desirable.



(Fig. D) f_{OSC} – T_a

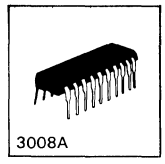


(Fig. E) Delay Time at I/O Pin – T_a

(Fig. D) and (Fig. E) show the temperature dependence of f_{OSC} and delay time at I/O pin when various external parts are combined. As seen from (Fig. D) and (Fig. E), it is most suitable to use the carbon resistor and polyester film capacitor.

(External constants recommended)
OSC pin
R=110kΩ (Carbon)
C=0.015μF (Polyester film)
I/O pin
R=180kΩ (Carbon)
C=0.068μF (Polyester film)

LC7184



C MOS LSI

CB Transceiver Channel Scanning System

Ⓔ 549B

General Description

The LC7184 and LC7191 make a pair to form a channel scan system of 12-channel CB transceivers (answering the channel plan in West Germany).

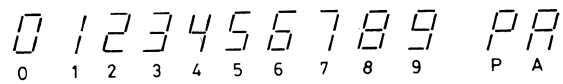
The LC7184 contains an up/down counter for channel memory and a channel output ROM. The LC7191 contains a channel indication decoder and an LED driver. (For the LC7191, refer to the separate catalog.)

Features

1. The following 3 methods are available for channel select of 12-channel (CH4 to CH15) transceivers answering the channel plan in West Germany.
   a: Manual scan b: Auto scan c: Auto search
2. For forming a scan system where the microphone unit has the channel indicator, only 5 more lines are required to connect the main body to the microphone unit.
3. Instantaneous call capability of emergency channel (CH9).
4. Capable of stopping the channel scan operation at the transmission mode.
5. "PA" indication available in applications where the transceiver is used as a loudspeaker.
6. LED driver capable of static driving of LED (15mA/V).

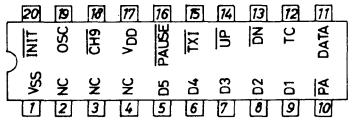
Functions

1. Manual scan : Each time the UP SW/DOWN SW is pushed, the channel goes up/down by one.
2. Auto scan : Pushing the UP SW/DOWN SW for 1 second or more causes the channel to go up/down at a 6Hz rate.
3. Auto search : Simultaneous push of the UP SW/DOWN SW causes the channel to advance fast (up). Applying the squelch signal to the PAUSE pin causes automatic stop when an idle channel is reached.
4. Emergency channel : Applying the emergency signal to the CH9 pin calls CH9. When the emergency signal disappears, the channel used before applying the signal returns.
5. Channel hold when in the transmission mode : Applying a signal to the TXI pin when in the transmission mode inhibits the channel from moving even if the UP SW/DOWN SW is pushed.
6. Channel indication : a. 7-segment LED's are lighted in the display font shown below. 0 in the high-order digit is blanked out.
   b. "PA" indication is available in applications where the transceiver is used as a loudspeaker.

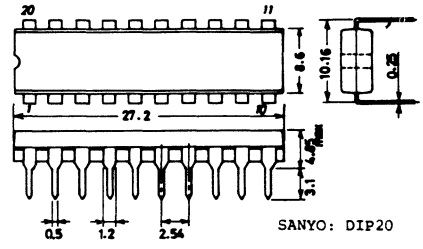


(continued on next page.)

Pin Assignment



Case Outline 3008A-D20IC
(unit: mm)



7. Connection between LC7181 and LC7191: One-shot data transfer is done through 2 lines. In applications where the microphone unit has the channel indicator, only 5 more lines are required to connect the main body and the microphone unit.
8. Output code to PLL: BCD

Absolute Maximum Ratings/T_a=25°C

				Unit
Maximum Supply Voltage	V_{DD} max		−0.3~+9.0	V
Input Voltage	V_{IN}		−0.3~V_{DD}+0.3	V
Output Voltage	V_{OUT}	Output OFF	−0.3~V_{DD}+0.3	V
Operating Temperature	T_{opg}		−30~+70	°C
Storage Temperature	T_{stg}		−40~+125	°C

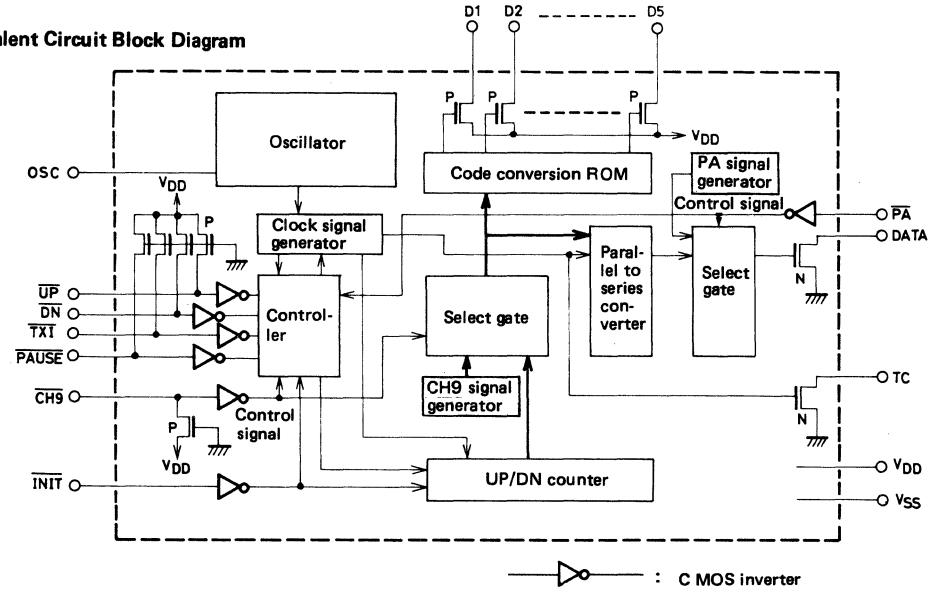
Allowable Operating Ranges/T_a=25°C

				Unit
Supply Voltage	V_{DD}		6.0~8.0	V
High Level Input Voltage	V_{IH}	All input pins (except OSC)	V_{DD}−1.0~V_{DD}	V
Low Level Input Voltage	V_{IL}	〃 〃	0~1.0	V

Electrical Characteristics/T_a=25°C, V_{DD}=6.0 to 8.0V

		Pin	Conditions	min	typ	max	Unit
Input Floating Voltage	V_{IF}	$\overline{UP}$, $\overline{DN}$, $\overline{CH9}$, $\overline{PAUSE}$, $\overline{TXI}$	Input open	V_{DD}−0.6			V
High Level Output Voltage	V_{OH}	D1~D5	I_O=0.5mA	V_{DD}−0.5			V
Low Level Output Voltage	V_{OL}	TC, DATA	I_O=0.5mA			0.5	V
High Level Input Current	I_{IH}	$\overline{INIT}$, $\overline{PA}$	V_I=V_{DD}			3.0	μA
Low Level Input Current	$I_{IL(1)}$	$\overline{UP}$, $\overline{DN}$, $\overline{CH9}$, $\overline{PAUSE}$, $\overline{TXI}$	V_I=V_{SS}	50		1250	μA
Low Level Input Current	$I_{IL(2)}$	$\overline{INIT}$, $\overline{PA}$	V_I=V_{SS}			3.0	μA
Output OFF Leak Current	$I_{OFF(1)}$	D1~D5	V_O=V_{SS}			5.0	μA
Output OFF Leak Current	$I_{OFF(2)}$	TC, DATA	V_O=V_{DD}			6.0	μA
Current Dissipation	I_{DD}	f_{osc}=850Hz, $\overline{INIT}$=V_{DD} $\overline{PA}$=V_{DD} other pins open				1.2	mA
Clock Pulse Cycle	T_{ϕ}	C : 0.015μF (polyester film) R : 110kΩ (carbon)		1.17−19%	1.17	1.17+19%	ms

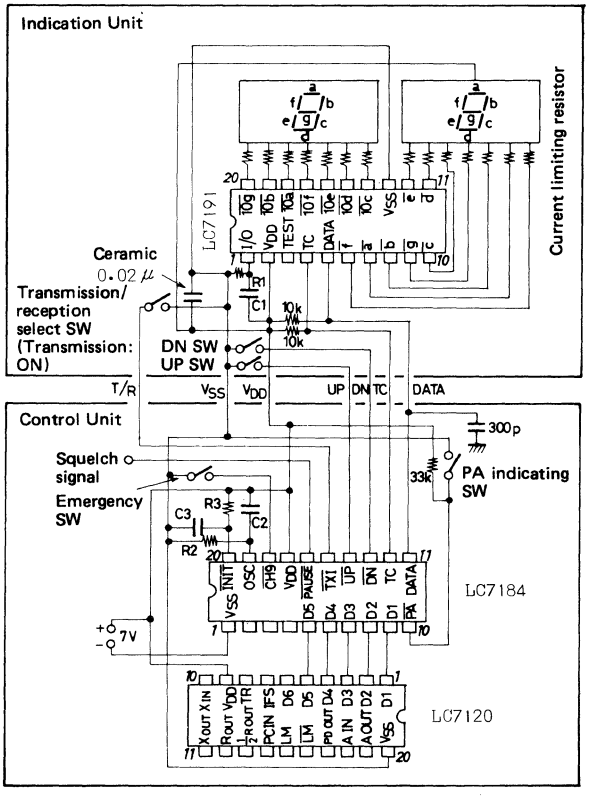
Equivalent Circuit Block Diagram



LC7184 Channel No. to Data Output (D1 to D5) Correspondence

CH	FREQ.	Frequency Division	PROGRAM DATA (BCD) D1	D2	D3	D4	D5
4	27.005	To be determined by the PLL IC used.	0	0	1	0	0
5	27.015		1	0	1	0	0
6	27.025		0	1	1	0	0
7	27.035		1	1	1	0	0
8	27.055		0	0	0	1	0
9	27.065		1	0	0	1	0
10	27.075		0	0	0	0	1
11	27.085		1	0	0	0	1
12	27.105		0	1	0	0	1
13	27.115		1	1	0	0	1
14	27.125		0	0	1	0	1
15	27.135		1	0	1	0	1

■ **Sample Application Circuit: Combination of PLL LSI and scan LSI**



● (LC7184: Scan use, LC7120: PLL Synthesizer use)

LC7200, -1,-3,-7

C MOS LSI

FM/AM Electronic Tuning Controller

Ⓔ C 731B

Use: SL^2 Synthesizer System for FM/AM (MW, LW) Radio

Functions Common to LC 7200 Series:

- Channel selection Control (manual, search, preset)
- Tuning voltage memory and control
- Optimum receiving condition control by means of the S-curve detection
- Band change-over control

Table of Contents

Features

1) As the SL^2 system, being fundamentally a voltage synthesizer, controls the receiver by direct current, the high S/N characteristics can easily be maintained with no interference to the S/N characteristics of the tuner.
2) Area of Application: World-wide FM/AM frequencies
3) Channel Selection Operation

   Manual channel selection
   Search channel selection
   (UP- and down-direction system)
   Preset channel selection
4) The time required for search channel selection within the entire receiving band is only three seconds approx.
5) Excellent tuning accuracy
6) Automatic Tuning Correction

   Fetching operation
   S-curve follow-up AFC operation
   Fine tuning operation
7) For the fetching and S-curve follow-up AFC operations, the 10 bit data is controlled at the outer ladder resistance and the rough adjustment of the tuning voltage is attained at a resolution of 1/1000 approx. In the case of fine tuning operations, the fine adjustment of the tuning voltage is attained at a high resolution of 1/6000 approx.
8) The audio muting control output can be used to eliminate any disturbing noises during band change-over.
9) The output for the purpose of controlling the radio sensitivity during search channel selection is provided.
10) The low voltage battery back-up is possible for holding the preset memory and the receiving state immediately before the main switch is turned OFF. (When the voltage regulator IC LA 5700 is used and backed-up at V_{DD} = 5V, dissipation current is 50 μA (typ).
11) C-MOS process LSI, 42 pin DIP package.
12) Supply voltage V_{DD} = +9V typ, V_{ref} = +8V typ.
13) Dissipation current I_{DD} = 5mA (during operation),
    0.2 mA (+5V during backed-up operation),
    I_{ref} = 0.7 mA (during operation)

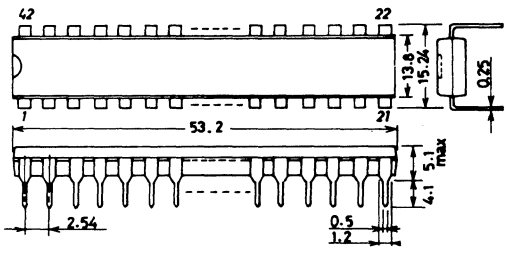
List of LC 7200 Series Models:

Differences between the models other than the common basic functions

Models	Number of Preset Stations FM/AM	Band	SK	STH	F/C	M-IND
LC7200	5/5	FM/MW	○	x	x	○
LC7201	6/6	FM/MW/LW	○	x	x	x
LC7203	6/6	FM/MW	○	○	○	x
LC7207	7/7	FM/MW/LW	x	x	x	○

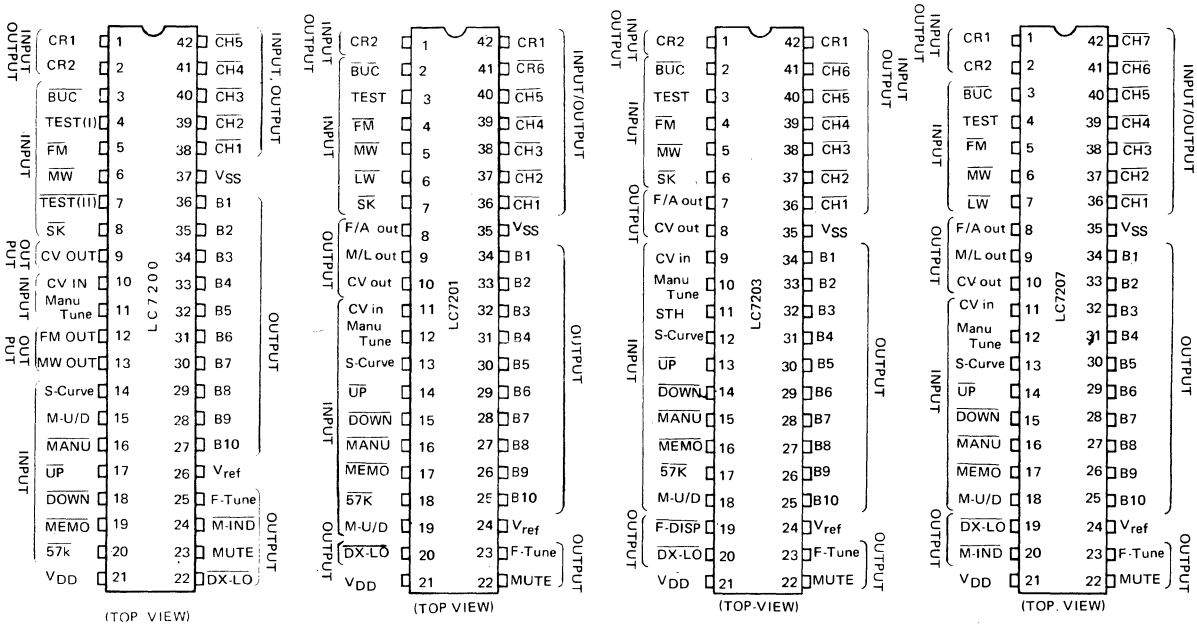
Note) SK .....The stopping function only for the traffic information system (Europe)
STH.....Short time hold (5 seconds) search function **(input pin: STH)**
F/C. ..... Automatic switching output for frequency/clock display **(input pin: F-$\overline{\text{DISP}}$)**
M-IND..... Output for displaying manual channel selection state **(output pin: M-$\overline{\text{IND}}$)**

Case Outline 3014A-D42IC
(unit: mm)

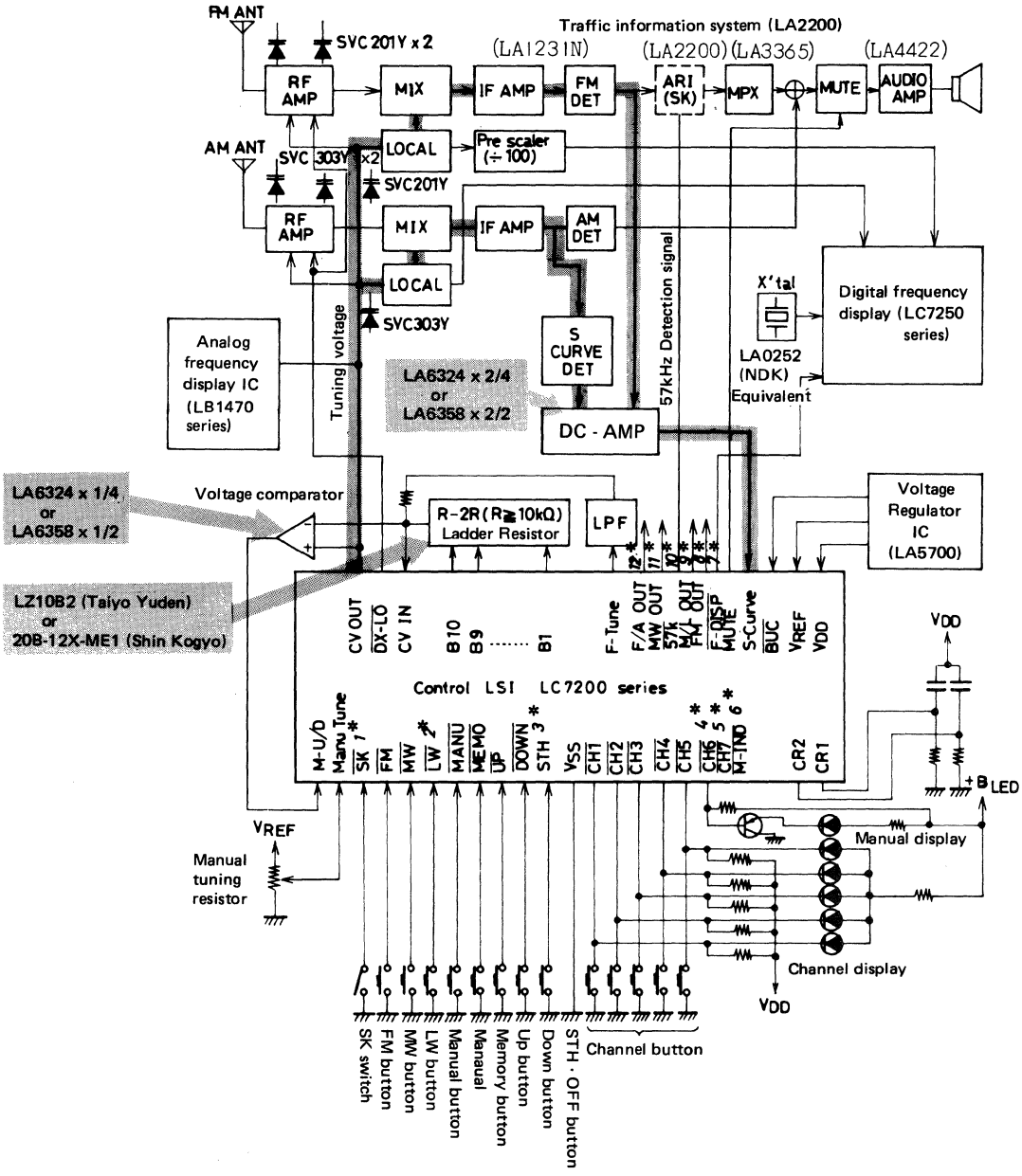


SANYO: DIP42

1. Pin Assignment



2. System Block Chart

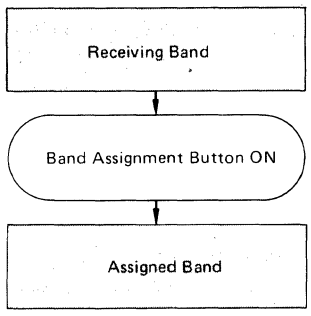


List of Pins used in Different Models (Pins without the mark * are included in all models)

	*1 SK	*2 LW	*3 STH	*4 CH6	*5 CH7	*6 M-IND	*7 F-DISP	*8 FM OUT	*9 M/L OUT	*10 57K	*11 MW OUT	*12 F/A OUT
LC7200	o					o		o		o	o	
LC7201	o	o		o					o	o		o
LC7203	o		o	o			o			o		o
LC7207		o		o	o	o			o			o

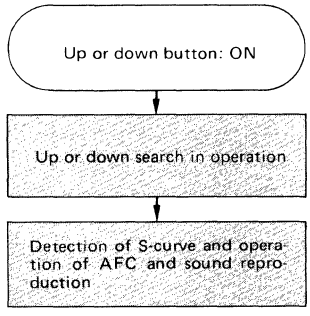
3. Flow Chart for Channel Selection

(1) Band selection



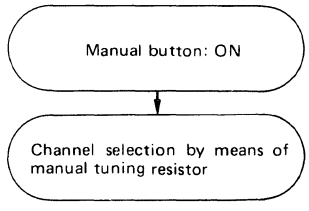
(Note) Band assignment button is to be ON for 5 seconds or more.

(2) Auto search channel selection



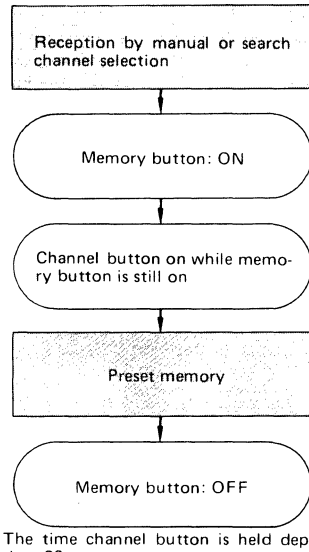
(Note) The time up or down button is held depressed is more than 5 msec.

(3) Manual channel selection



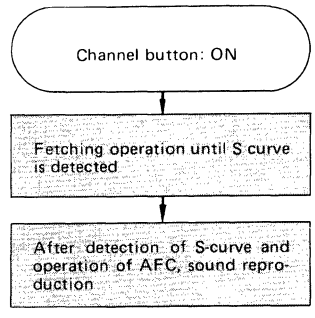
(Note) The time of manual button is held depressed is more than 5 msec.

(4) Preset memory



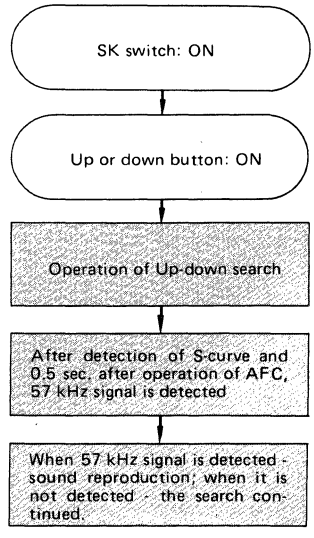
(Note) The time channel button is held depressed is more than 20 msec.

(5) Preset channel selection



(Note) The time of channel button is held depressed is more than 20 msec.

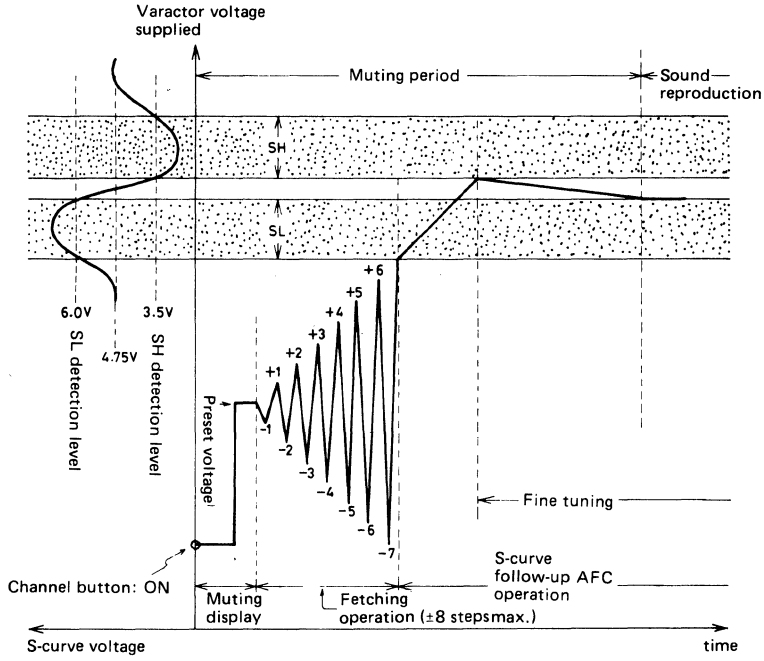
(6) Traffic information station discriminating signal (57 kHz) search channel selection (FM band only)
(No SK search on the LC7207)



(Note) The time up or down button is held depressed is more than 5 msec.

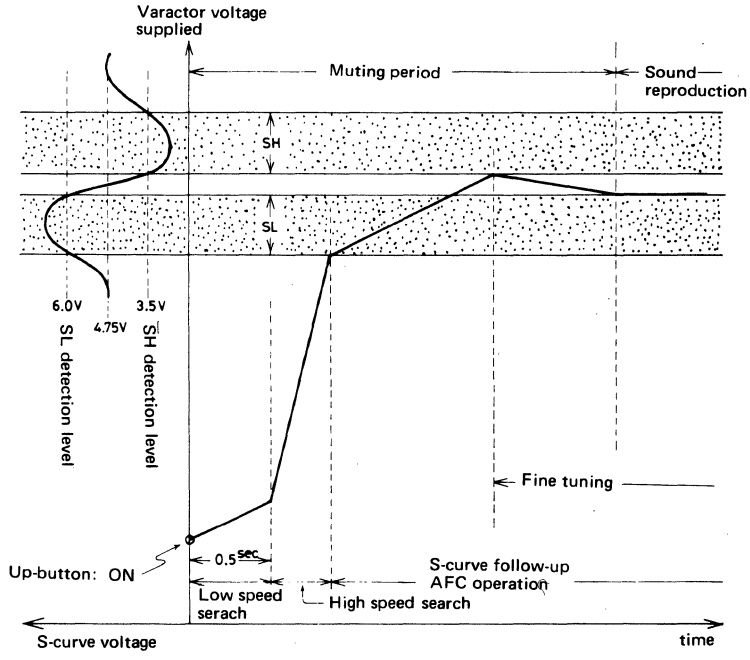
4. Fundamental Chart for Automatic Frequency Correction Operation

(1) Preset channel selection



(Note) The S-curve waveform shows the waveform at the S-curve pin of the LSI.

(2) Search channel selection



(Note) The S-curve waveform shows the waveform at S-curve pin of the LSI.

5. Function Description

5-1 Channel Selection Function

(1) Auto-search channel selection

- By switching the up-button the device will be actuated to start auto-search in the higher direction of the receiving frequency so that the desired channel is automatically selected.
- By switching the down-button the device will be actuated to start auto-search in the lower direction of the receiving frequency so that the desired channel is automatically selected.
- For search channel selection, the optimum receiving point can be obtained by the S-curve (an S-curve generation circuit is required for AM) follow-up automatic frequency correction (AFC).
- Search speed is 3 ms/step; the time required for searching over the entire receive band is approximately three seconds.
- When the search button (either up-button or down-button) is held depressed, the device will continue search operation even where an appropriate broadcasting station is in the search range.

(2) Preset channel selection

- By switching the channel button the device will be actuated to select memorized in advance.
- The tuning point of the tuner and drift are corrected by means of the fetching and S-curve follow-up AFC functions so that the preset voltage is converted into the optimum tuing voltage.
- The time required for channel selection is approximately 0.2 to 1.0 seconds.

(3) Manual channel selection

- By switching the manual button the device will be placed in a state of manual operation.
- The channel desired can be selected by turning the manual tuning resistor.
- The tuning voltage required for the manual resistor is directly applied to the variable capacitance diode through the analog switch provided in the LSI.
- When the instrument is in a state of manual operation, this is displayed by LED, which is connected to the $\overline{\text{M-IND}}$ terminal. (LC7200, 7207)

(4) Present memory

- The contents which are being received can be memorized by pressing the channel button while the memory button is held depressed.
- The memory capacity: Refer to List of LC7200 Series Models.
- The preset memory from the channel that has been manually selected is memorized by subjecting the tuning voltage to A-D conversion (10-bit digital signal).

5-2 Automatic Tuning Correction Function

(1) Fetching function

- When the position of the S-curve is shifted in the process of preset channel selection by tuning drift or some other reason, the voltage will be swung by the maximum limit within ±8 steps (approximately ±56 mV) from the originally preset voltage until the S-curve is restored to its former stage.
- When there is no S-curve in existence due to the presence of a weak electric field or some other reason, the voltage value will be returned to the originally preset voltage value after the fetching process is complete.

(2) S-curve follow-up automatic frequency correction (AFC)

- Both AM and FM receiving are corrected to the optimum receiving point by making use of the S-curve characteristics (an S-curve generation circuit is required for AM) that can be recognized in a radio in the process of auto-search or preset channel selection.
- Where tuning drift occurs on the tuner in the process of reception, the device is automatically corrected to the optimum receiving point.

(3) Fine tuning

- When automatic frequency correction (AFC) is carried out in the process of reception, pulse duration modulation signals (in 8 stages) of the F-Tune terminal output are subjected to D/A conversion, in addition to correction by 10-bit data, so that they are superimposed on ladder voltage. In other words, fine tuning can be performed at a resolution above 10 bits (equivalent to approximately 12 bits) in order to obtain a better performance from the auditory point of view.
- The amount of correction for fine tuning can be adjusted by an external resistance.

5-3 Additional Function

(1) Search channel selection for selecting the signal (57 kHz) of a traffic information broadcasting station (LC7250, 7201, 7203)

- SK mode auto-search channel selection can be made (for FM only) by adding a traffic decoder SK-type IC.
- As soon as the SK switch is turned on, the device executes auto-search to select the required broadcasting station only, which is generating signals of 57 kHz.

(2) Muting signal

- In the process of search channel selection, controlling signals (MUTE output) are generated to exclude disturbing noises which are often produced when channels or bands are changed over.

(3) Back-up function

- A state of reception when the 'back-up' process started can be maintained by means of back-up control ($\overline{\text{BUC}}$ input).
- In a state of back-up, LED will light off and the built-in oscillation circuit will be stopped to reduce the LSI current dissipation.
- Back-up supply voltage: +2.5V min.

- Dissipation current when in back-up: 50 μA typ.

(4) Order of priority in channel selection

- Procedure in channel selection
  The order of priority as to the procedures when two or more buttons are pressed simultaneously:
  1. Manual channel selection (manual button)
  2. UP search channel selection (up-button)
  3. DOWN search channel selection (down-button)
  4. Preset channel selection (channel button)
- Band change-over
  Priority will be given to FM (when FM and MW buttons are pressed simultaneously).
- Channel ($\overline{CH1}$-$\overline{CH5}$)
  Priority will be given to the button that is pressed before any other buttons.

(5) STH (Short Time Hold) Search channel selection (LC7203)

- The search channel selection mode holds a selected station; however, the STH channel selection mode keeps searching while holding a selected station for five seconds.
- The STH search channel selection mode is actuated with the STH pin open and cancelled when the "L" level (over 5 msec) is impressed to the STH pin.
  Therefore, when the STH-OFF button is depressed within five seconds after a desired station is selected by the STH search channel selection mode, the search procedure is cancelled and the selected station can be continuously received.

(6) Automatic change-over function for frequency/clock display (LC7203)

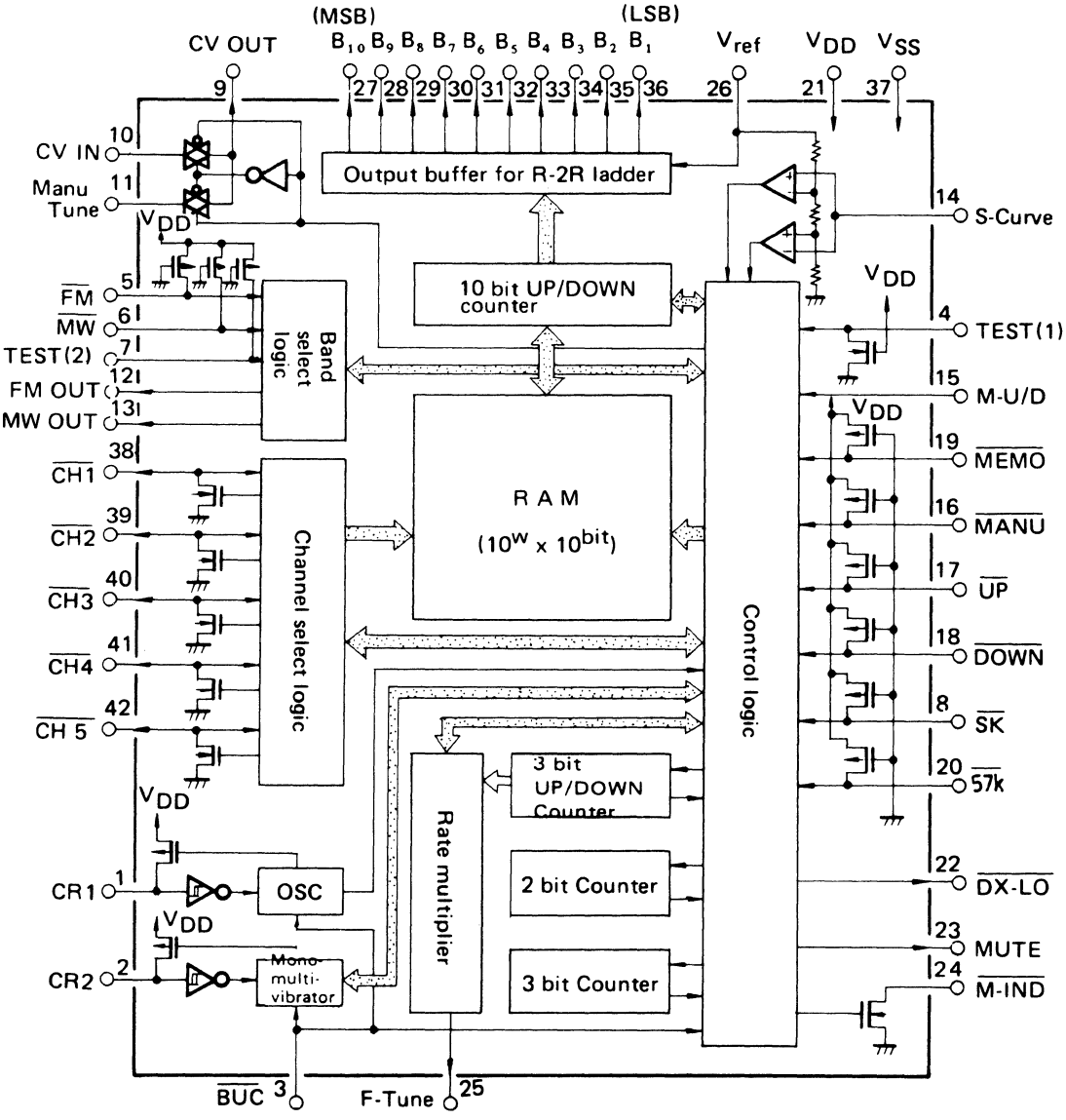
- The frequency/clock display automatic change-over control pin ($\overline{F\text{-}DISP}$) is provided for use with LSI, LC 7250/7253 with a digital frequency display (clock).
- The output of the $\overline{F\text{-}DISP}$ is at the level "L" during the following operation modes (Table 1). The display on LC7250/7253 is changed over by the use of the level "L". The time is always displayed, and this is automatically changed over to the frequency display mode when necessary.

Table 1

	Frequency display
Search Channel Section	* During channel selection and for five seconds after such. * During STH search channel selection.
Preset Channel Selection	* During channel selection and for five seconds after such.
Preset Memory	* When the memory button is ON. * For five seconds after the memory is turned OFF.
Manual Channel Section	* When the manual button is ON and for five seconds after it is turned OFF. * When the manual tuning resistor is being turned and for five seconds after being stopped.
Band Change-over	* For five seconds after the band is changed over.
Back-up Function	* For five seconds after the back-up function is in an off status.

6. Equivalent Circuit Block Diagram

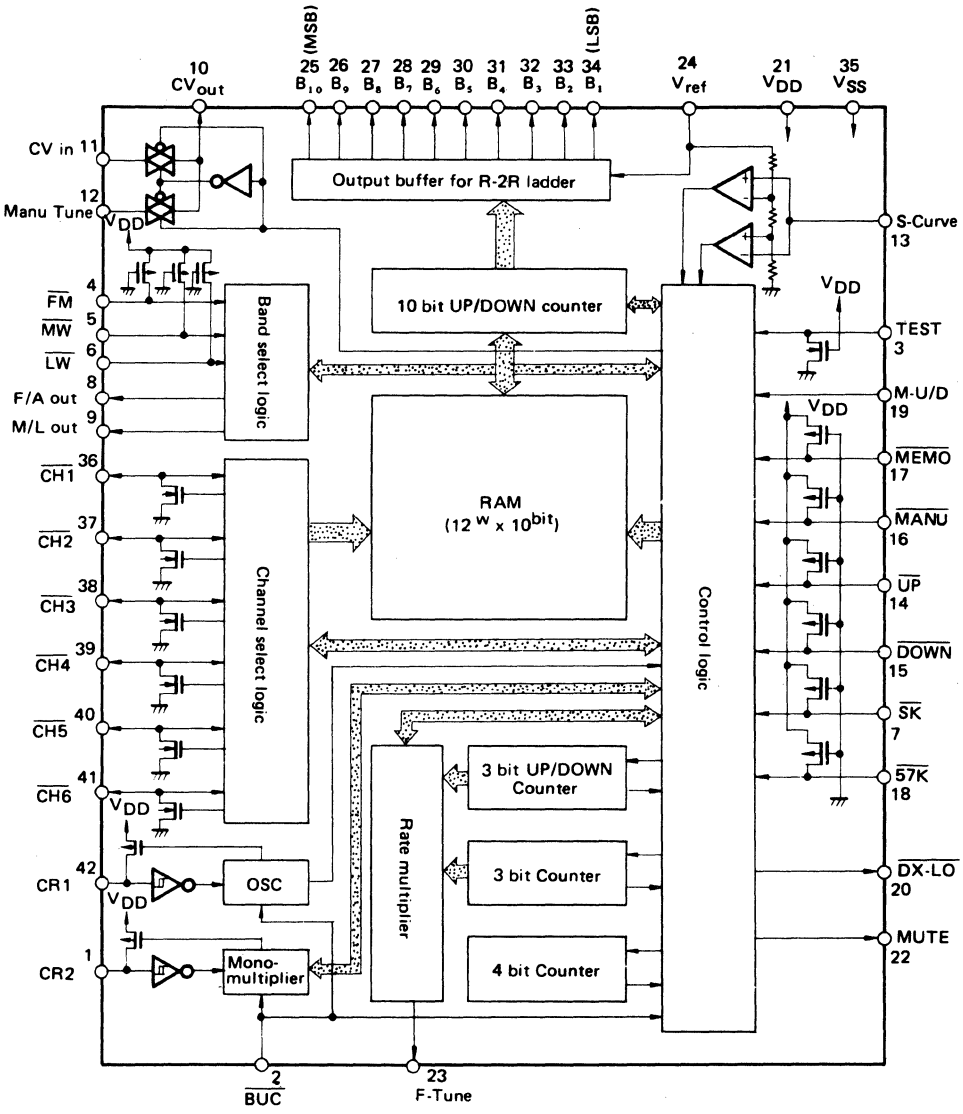
(LC7200)



NOTE: 1) The outputs from pins of F/A OUT, M/L OUT, $\overline{\text{DX-LO}}$, MUTE, F-Tune and $B_1 \sim B_{10}$ are in a complementary output form.

2) The mark ▷○ in the diagram represents a Schmitt type inverter.

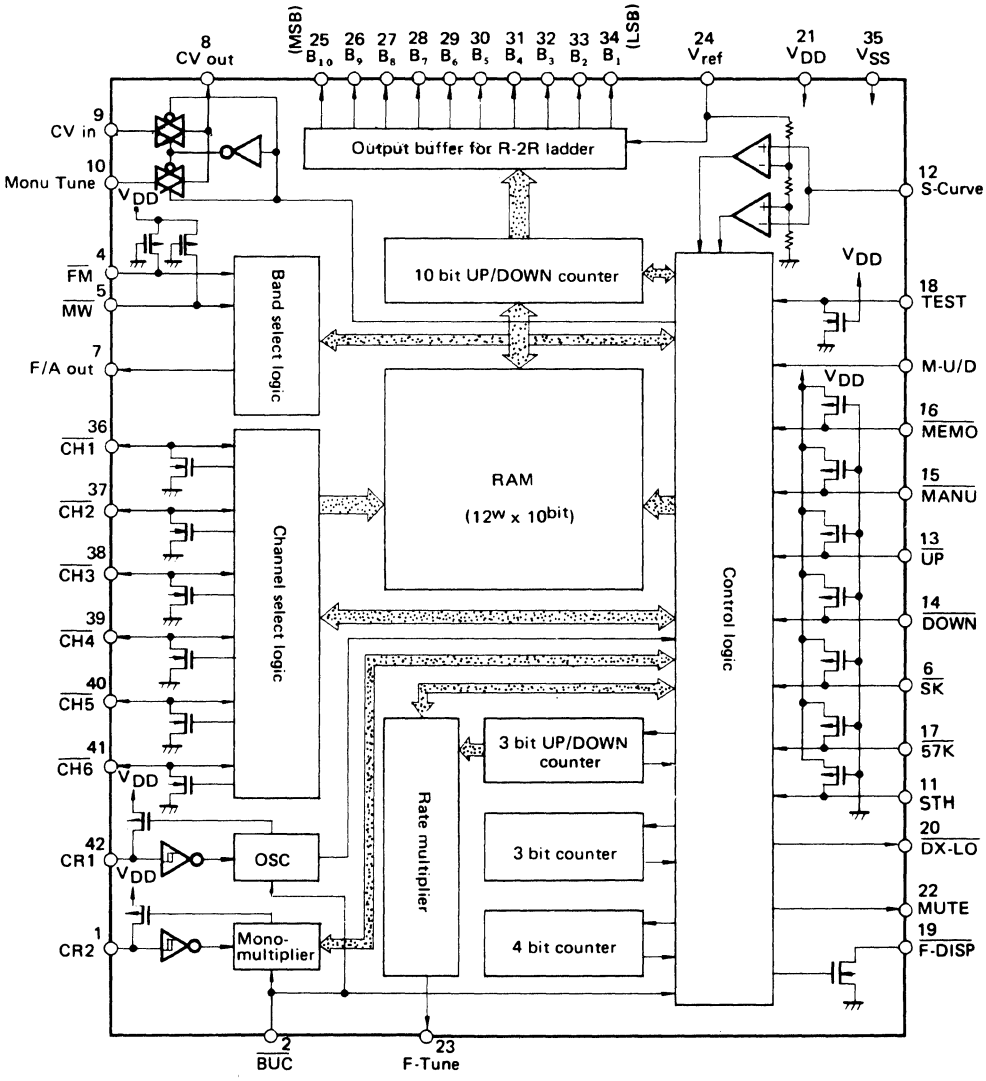
(LC7201)



NOTE: 1) The outputs from pins of F/A OUT, M/L OUT, $\overline{\text{DX-LO}}$, MUTE, F-Tune and $B_1 \sim B_{10}$ are in a complementary output form.

2) The mark ▷o in the diagram represents a Schmitt type inverter.

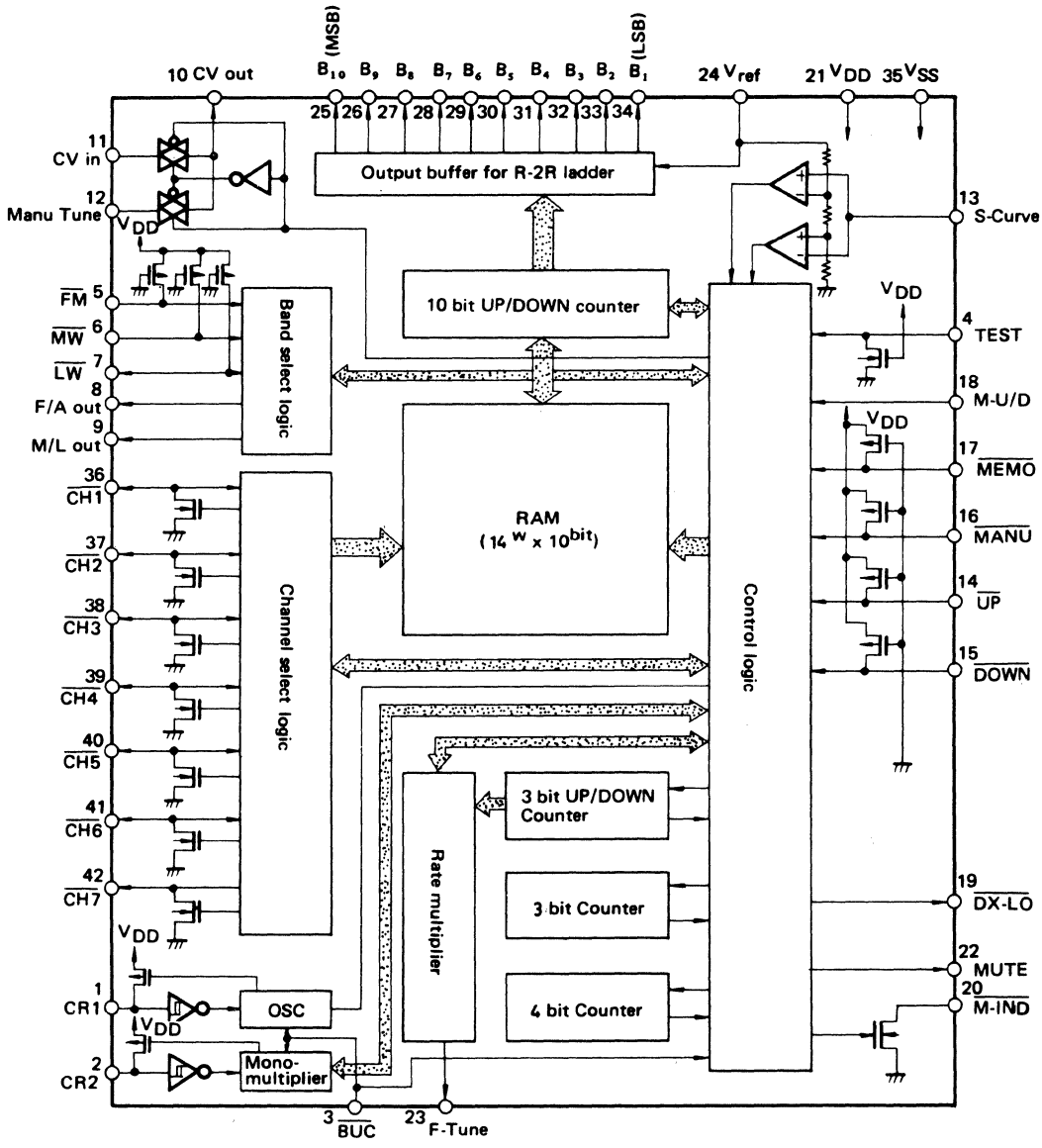
(LC7203)



NOTE: 1) The outputs from pins of F/A OUT, $\overline{\text{DX-LO}}$, MUTE, F-Tune and $B_1 \sim B_{10}$ are in a complementary output form.

2) The mark ▷o in the diagram represents a Schmitt type inverter.

(LC7207)



NOTE: 1) The outputs from pins of FM OUT, MW OUT, $\overline{\text{DX-LO}}$, MUTE, F-Tune and $B_1 \sim B_{10}$ are in a complementary output form.

2) The mark ▷○ in the diagram represents a Schmitt type inverter.

7. Terminal Function Description

7-1 Pins common to LC 7200 series

(Refer to each pin assignment chart for pin assignment)

Name of Terminal	Input/ Output	Function
CR_1	Input/ Output	• When a CR time constant circuit is connected to an outside terminal, an oscillation circuit is formed to generate basic clock pulses for the LSI system. (Oscillation period; 0.4 msec typ.)
CR_2	Input/ Output	• When a CR time constant circuit is connected to an outside terminal, a timer circuit is formed. • The pulse width of MUTE output signals is determined when bands are changed over (Operation period; 0.5 sec typ.)
$\overline{BUC}$	Input	• At the 'L' level of the back-up control terminal, the device is placed into a state of back-up.
$\overline{FM}$	Input	• FM band assignment input terminal. • At the 'L' level, the device is put into a state of FM reception, and is still maintained in this state even after the terminal is turned to 'H' level. (Duration of 'L' level: more than 5 ms)
$\overline{MW}$	Input	• MW band assignment input terminal • At the 'L' level, the device is placed into a state of MW reception, and is still maintained in this state even after the terminal is turned to 'H' level. (Duration of 'L' level; more than 5 ms)
CV OUT	Output	• The output of the analog signal transfer gate makes the voltage to the variable capacitance diode.
CV IN	Input	• The input of the analog signal transfer gate needs R-2R ladder output voltage as an input.
Manu Tune	Input	• The input of the analog signal transfer gate needs the tuning voltage generated at the manual resistor as an input.
S-Curve	Input	• S-curve voltage for FM/AM is input. • When the window type comparator provided in the LSI is at 'Input', control signals are generated for AFC. • The range of S-curve tuning points, in which S-curve follow-up AFC can be carried out, is shown in Fig. 1.
M-U/D	Input	• Ouptut signals of the external comparator, which makes up an A/D converter when in manual mode, are impressed. • At the 'H' level, 10 bit data make 'UP count' while ladder output voltage increases. • At the 'L' level, 10-bit data make 'DOWN count' while ladder output voltage decreases.

Name of Teminal	Input/ Output	Function
$\overline{UP}$	Input	• Auto-search channel selection assignment input terminal. • At the 'L' level, UP search is executed; when S-curve voltage is applied to the S-curve terminal, UP search will be brought to a halt after AFC is completed. • Duration of UP search assignment 'L' level: more than 5 ms. • Where 'L' level is maintained in the process of UP search, the search will continue even when the S-curve voltage is applied to the S-curve terminal.
$\overline{DOWN}$	Input	• Auto-search channel selection assignment input terminal. • At the 'L' level, DOWN search is executed; when S-curve voltage is applied to the S-curve terminal, DOWN search will be brought to a half after AFC is completed. • Duration of DOWN search assignment 'L' level: more than 5 ms. • Where 'L' level is maintained in the process of DOWN search, the search will continue even when the S-curve voltage is applied to the S-curve terminal.
$\overline{MEMO}$	Input	• Preset memory assignment input terminal. • While 'L' level is being maintained, memorizing is available.
$\overline{MANU}$	Input	• Manual channel selection assignment input terminal. • At the 'L' level, the device is placed into a state of manual channel selection; channel selection can be carried out by means of the manual tuning resistor. • When any of $\overline{UP}$, $\overline{DOWN}$, or channel assignment input terminal is at the 'L' level, a state of manual channel selection is cancelled.
V_{DD}	–	• Power supplying for LSI. In operation: +9V typ; In back-up: +5V typ. (LA5700 is operated)
$\overline{DX\text{-}LO}$	Output	• Output terminal to be used for controlling the sensitivity of a radio receiver in the process of auto-search. • 'L' level for auto-search only; 'H' level for ordinary purposes.
MUTE	Output	• Output terminal for control signals to be used for excluding disturbing noises which are often produced in the process of channel selection. • It is set to the 'H' level output when in search channel selection, preset channel selection, or band change-over.
F-Tune	Output	• Output terminal for fine tuning. • Correction voltage for fine tuning is generated by connecting a low-pass filter to an outside terminal. • Correction voltage is regulated with a mixing resistance and superimposed on ladder output voltage (except in fine tuning, 50% duty signal: T = 1.5 ms). • In fine tuning, pulse duration modulation signals are generated in eight states.

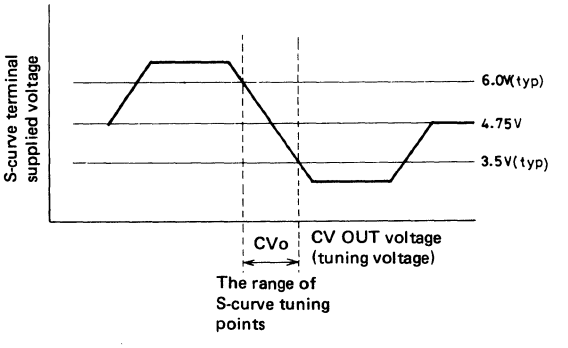
Vref	–	• Reference supply voltage (+8V typ) –
		  • for D/A converter
		  • for window type comparator and reference comparator

B1-B10	Output	• 10-bit UP/DOWN counter output (with ladder buffer built in). • D/A conversion is carried out by connecting R-2R (R = above 10 kΩ) to an outside terminal. • B10 . . . . . MSB, B1 . . . . . LSB.

Name of Terminal	Input/ Output	Function
Vss	–	• GND terminal for LSI
(LC7200) $\overline{CH1}$–$\overline{CH5}$ (LC7201) (LC7203) $\overline{CH1}$–$\overline{CH6}$ (LC7207) CH1–CH7	Inout/ Output	• Channel assignment input terminal • Receiving channel display output terminal (N-channel open drain type with an LED driver built in). • At the 'L' level, a broadcasting station memorized in advance will be selected. • When the $\overline{MEMO}$ terminal is at the 'L' level, the contents which are being received from a broadcasting station can be memorized by setting one of $\overline{CH1}$ – $\overline{CH5}$ to the 'L' level. • Duration of 'L' level for channel selection or for memory: more than 20 ms.

♦ The S curve applied to the S curve input pin of the LSI must meet the following conditions.

Model	S-curve Tuning Range		
	FM	MW	LW
LC7200	4 steps (28mV) and below	same as left	–
LC7201	8 steps (56mV) and below	same as left	64 steps (448mV) and below
LC7203	8 steps (56mV) and below	same as left	–
LC7207	As above	same as left	64 steps (448mV) and below



7-2 Pins other than common pins

LC7200	LC7201	LC7203	LC7207	Name of Pin	Input/ Output	Function
○				FM OUT	Output	• The control signal indicating the FM band reception state is output. • At the "H" level, the device is put into an FM reception status.
○				MW OUT	Output	• The control signal indicating the MW band reception state is output. • At the "H" level, the device is put into a MW reception status.
○	○	○		$\overline{SK}$	Input	• Auto-search channel selection assignment input terminal for SK mode. • At the "L" level, the device is put into the SK mode (for FM band only), at the process of search, the S-curve is detected, and; 0.5 seconds, after the $\overline{57k}$ terminal is checked in order to determine whether it is at the "L" level or "H" level. • When the $\overline{57k}$ terminal is at the "L" level, the device is in a channel selection status.
○	○	○		$\overline{57k}$	Input	• Input terminal to be used for impressing "H" or "L" level signals representing the detection of $\overline{57k}$ signals detected by the traffice decoder (SK type) IC. • In the process of SK mode auto-search, a broadcasting station, to which "L" signals through this terminal have been applied, is selected. (for FM band only). • In 0.5 seconds after search channel selection, 57 kHz signals can or cannot be confirmed.
○			○	$\overline{M\text{-}IND}$	Output	• The signal output indicating the manual channel selection state. • N channel open drain output system (The "L" level for manual channel selection.) • The external LED. driver is needed.
	○	○		F/A OUT	Output	• The control signal indicating the state of band reception is outputted. • FM band .... "H" level • AM band .... "L" level (MW/LW bands)
	○			M/L OUT	Output	• The control signal indicating the state of band reception is outputted. • MW band .... "H" level • LW band .... "L" level
	○			$\overline{LW}$	Input	• $\overline{LW}$ band as assignment input pin. • At the "L" level, the device is placed into a $\overline{LW}$ reception state, and is still maintained in this state even after the terminal is turned to the "H" level (duration of the "L" level: 5 ms or more).
		○		STH	Input	• The assignment input pin for STH search channel selection. • At the "H" level, the device is put into the STH search mode and at the "L" level (5 ms or more), STH search mode is cancelled. • Normally at "H" level.
		○		$\overline{F\text{-}DISP}$	Output	• The output pin indicating the frequency/clock change-over control signal. • Refer to 5-3(6) frequency/clock display automatic change-over function.
○				TEST (I)	Input	• Test pin of the internal LSI circuit. • At the "H" level, the device is put into a testing state. • To be connected to OPEN or "L" level when mounting.
○				$\overline{TEST\ (II)}$	Input	• Test pin of the internal LSI circuit. • At the "H" level, the device is put into a testing state. • To be connected to OPEN or "H" level when mounting.
	○	○	○	TEST	Input	• Test pin of the internal LSI circuit. • At the "H" level, the device is put into a testing state. • To be connected to OPEN or "L" level whem mounting.

8. Specifications

Absolute Maximum Ratings/Ta = 25°C, $V_{ref} \leqq V_{DD}$

Item	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage	V_{DD} max.		−0.3 to +11	V
Reference Voltage	V_{ref}		−0.3 to +10	V
Input Voltage	V_I		−0.3 to (V_{DD} + 0.3)	V
Output Voltage	V_O	Output Transistor OFF	−0.3 to (V_{DD} + 0.3)	V
Output Current	I_O	$CH_1 \sim CH_5$, CH_6, CH_7	20	mA
Allowable Power Dissipation	Pd max	Ta ≦ 75°C	300	mW
Operating Temperature	T_{opg}		−30 to +75	°C
Storing Temperature	T_{stg}		−40 to +125	°C

Allowable Operating Conditions/Ta = 25 ± 2°C, $V_{ref} \leqq V_{DD}$, V_{SS} = 0

(LC7200)

Item	Symbol	Name of pin	Conditions	min	typ	max	Units
Supply Voltage	$V_{DD}(1)$	V_{DD}		+8.0		+10.0	V
	$V_{DD}(2)$	V_{DD}		+2.5			V
Reference Voltage	V_{ref}	V_{ref}		+7.8		+8.2	V
Input "H" Level Voltage	$V_{IH}(1)$	$\overline{BUC}$, $\overline{FM}$, $\overline{MW}$, $\overline{SK}$, M-U/D $\overline{MANU}$, $\overline{UP}$, $\overline{DOWN}$ $\overline{MEMO}$, $\overline{57K}$ $\overline{CH1} \sim \overline{CH5}$		$0.75V_{DD}$		V_{DD}	V
	$V_{IH}(2)$	S-Curve		$(\frac{6}{8}+0.05)V_{ref}$		V_{DD}	V
Input "L" Level Voltage	$V_{IL}(1)$	$\overline{BUC}$, $\overline{FM}$, $\overline{MW}$, $\overline{SK}$, M-U/D $\overline{MANU}$, $\overline{UP}$, $\overline{DOWN}$ $\overline{MEMO}$, $\overline{57K}$, $\overline{CH1} \sim \overline{CH5}$		V_{SS}		$0.25V_{DD}$	V
	$V_{IL}(2)$	S-Curve		V_{SS}		$(\frac{3.5}{8}-0.05)V_{ref}$	V
Input "M" Level Voltage	V_{IM}	S-Curve		$(\frac{3.5}{8}+0.05)V_{ref}$		$(\frac{6}{8}-0.05)V_{ref}$	V
Input Voltage Range	V_I	CVin, Manu Tune		V_{SS}		V_{DD}	V
Oscillation Guarantee External Resistance	R_{X1}	CR1	C_{X1}=6800pF, Refer to Fig. 1		91		kΩ
Oscillation Guarantee External Capacity	C_{X1}	CR1	R_{X1}=91kΩ, Refer to Fig. 1		6800		pF
Operating Guarantee External Resistance	R_{X2}	CR2	C_{X2}=2.2μF, Refer to Fig. 2. (C_{X1}=6800pF, R_{X1}=91kΩ)		360		kΩ
Operation Guarantee External Capacity	C_{X2}	CR2	R_{X2}=360kΩ Refer to Fig. 2. (C_{X1}=6800pF, R_{X1}=91kΩ)		2.2		μF

Electrical Characteristics/Ta = 25± 2°C, V_{DD} = +8.0 to +10.0V, V_{ref} = +7.8 to 8.2V, $V_{ref} \leqq V_{DD}$, V_{SS} = 0V

(LC7200)

Item	Symbol	Name of Terminal	Conditions	min	typ	max	Unit
Input "H" level Current	I_{IH}	$\overline{BUC}$, S-Curve, M-U/D	$V_I = V_{DD}$			10	μA
Input "L" level Voltage	$I_{IL}(1)$	$\overline{FM}$, $\overline{MW}$, $\overline{SK}$, $\overline{MANU}$, $\overline{UP}$ $\overline{DOWN}$, $\overline{MEMO}$, $\overline{57K}$	$V_I = V_{SS}$	−170		−24	μA
	$I_{IL}(2)$	$\overline{BUC}$, S-Curve, M-U/D $\overline{CH1}$ ~ $\overline{CH5}$	$V_I = V_{SS}$	−10			μA
Output "H" level Voltage	$V_{OH}(1)$	MWout, $\overline{DX\text{-}LO}$, MUTE F-Tune	I_{OH} = −1mA	V_{DD}−1.0			V
	$V_{OH}(2)$	FM out	I_{OH} = −2mA	V_{DD}−1.0			V
	$V_{OH}(3)$	B10	I_{OH} = −0.5mA	V_{ref} −0.06			V
	$V_{OH}(4)$	B 9	I_{OH} = −0.5mA	V_{ref} −0.12			V
	$V_{OH}(5)$	B 8	I_{OH} = −0.5mA	V_{ref} −0.24			V
	$V_{OH}(6)$	B1 ~ B7	I_{OH} = −0.5mA	V_{ref} −0.48			V
Output "L" level Voltage	$V_{OL}(1)$	MW out, $\overline{DX\text{-}Lo}$, MUTE $\overline{M\text{-}IND}$, F-Tune	I_{OL} = 1mA			1.0	V
	$V_{OL}(2)$	FM out	I_{OL} = 2mA			1.0	V
	$V_{OL}(3)$	B10	I_{OL} = 0.5mA			0.06	V
	$V_{OL}(4)$	B 9	I_{OL} = 0.5mA			0.12	V
	$V_{OL}(5)$	B 8	I_{OL} = 0.5mA			0.24	V
	$V_{OL}(6)$	B1 ~ B7	I_{OL} = 0.5mA			0.48	V
	$V_{OL}(7)$	$\overline{CH1}$ ~ $\overline{CH5}$	I_{OL} = 20mA			2.0	V
On Resistance	R_{ON}	CV out, CV in, Manu-Tune	V_{IN} = 0~V_{ref}V, R_L = 100kΩ			300	Ω
Oscillation Period	$T_{(OSC)}$	CR1	R_{X1} = 91kΩ C_{X1} = 6800pF, V_{DD} = 9.0V, Refer to Fig. 1.		0.4		msec
Operation Period	$T_{(multi)}$	CR2	R_{X2} = 360kΩ, C_{X2} = 2.2μF V_{DD} = 9.0V, Refer to Fig. 2.		520		msec
Current Dissipation	$I_{DD}(1)$	V_{DD}	V_{DD} = ±10.0V, V_{ref} = +8.0V, $\overline{BUC}$ = "H", S-Curve=½V_{ref} Refer to Fig. 3.			5.0	mA
	$I_{DD}(2)$	V_{DD}	V_{DD} = +5.5V, V_{ref} = 0V, $\overline{BUC}$ = "L", Refer to Fig. 4.			200	μA
	I_{ref}	V_{ref}	V_{DD} = +8.0~ +10.0V, V_{ref} = +8.0V, S-Curve = (V_{ref}/2), No load on B1~B10 Refer to Fig. 5.			0.7	mA

Absolute Maximum Ratings/Ta = 25°C, $V_{ref} \leq V_{DD}$
(LC7201, 7203, 7207)

Item	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage	V_{DD} max.		−0.3 to +11	V
Reference Voltage	V_{ref}		−0.3 to +10	V
Input Voltage	V_I		−0.3 to (V_{DD} + 0.3)	V
Output Voltage	V_O	Output Transistor OFF	−0.3 to (V_{DD} +0.3)	V
Output Current	I_O	$\overline{CH_1}$ ~ $\overline{CH_5}$, $\overline{CH_6}$, $\overline{CH_7}$	20	mA
Allowable Power Dissipation	Pd max	Ta ≦ 75°C	300	mW
Operating Temperature	T_{opg}		−30 to +75	°C
Storage Temperature	T_{stg}		−40 to +125	°C

Allowable Operating Conditions/Ta=25°C±2°C, $V_{ref} \leqq V_{DD}$, V_{SS}=0
(LC7201, 7203, 7207)

Item	Symbol	Name of Terminal	Conditions	Limits			Unit
				min	typ	max	
Supply Voltage	$V_{DD}(1)$	V_{DD}	Total Operation	+8.0		+10.0	V
	$V_{DD}(2)$	V_{DD}	Memory Back-up Operation	+2.5		+10.0	
Reference Voltage	V_{ref}	V_{ref}	$V_{ref} \leqq V_{DD}$	+7.8		+8.2	V
Input "H" level Voltage	$V_{IH}(1)$	$\overline{FM}$, $\overline{MW}$, $\overline{LW}$, $\overline{SK}$, $\overline{UP}$, $\overline{DOWN}$, $\overline{MANU}$, $\overline{MEMO}$, $\overline{57K}$, M-U/D, $\overline{CH1}$ ~ $\overline{CH6}$ ($\overline{CH7}$), STH		0.75V_{DD}		V_{DD}	V
	$V_{IH}(2)$	$\overline{BUC}$	V_{DD}=2.5V	0.8V_{DD}		V_{DD}	V
	$V_{IH}(3)$	S-Curve		$(\frac{6}{8}+0.05)V_{ref}$		V_{DD}	V
Input "L" level Voltage	$V_{IL}(1)$	$\overline{FM}$, $\overline{MW}$, $\overline{LW}$, $\overline{SK}$, $\overline{UP}$, $\overline{DOWN}$, $\overline{MANU}$, $\overline{MEMO}$ $\overline{57K}$, M-U/D, $\overline{CH1}$ ~ $\overline{CH6}$ ($\overline{CH7}$), STH		V_{SS}		0.25V_{DD}	V
	$V_{IL}(2)$	$\overline{BUC}$	V_{DD}=2.5V	V_{SS}		0.2V_{DD}	V
	$V_{IL}(3)$	S-Curve		V_{SS}		$(\frac{3.5}{8}-0.05)V_{ref}$	V
Input "M" level Voltage	V_{IM}	S-Curve		$(\frac{3.5}{8}+0.05)V_{ref}$		$(\frac{6}{8}-0.05)V_{ref}$	V
Input Voltage Range	V_I	CVin, Manu Tune		V_{SS}		V_{DD}	V
Oscillation Guarantee External Resistance	R_{X1}	CR1	C_{X1} = 6800pF Refer to Fig. 1.		91		kΩ
Oscillation Guarantee External Capacity	C_{X1}	CR1	R_{X1} = 91kΩ Refer to Fig. 1.		6800		pF
Operation Guarantee External Resistance	R_{X2}	CR2	C_{X2} = 2.2μF Refer to Fig. 2. C_{X1} = 6800pF, R_{X1} = 91kΩ		240		kΩ
Operation Guarantee External Capacity	C_{X2}	CR2	R_{X2} = 240kΩ Refer to Fig. 2. C_{X1} = 6800pF, R_{X1} = 91kΩ		2.2		μF

Electrical Characteristics/Ta=25±2°C, V_{DD}=+8.0 to +10.0V, V_{ref}=+7.8 to +8.2V, $V_{ref} \leq V_{DD}$, V_{SS}=0V (LC7201, 7203, 7207)

Item	Symbol	Name of Terminal	Conditions	Limits min	Limits typ	Limits max	Unit
Input "H" level Current	I_{IH}	$\overline{BUC}$, S-Curve, M-U/D	$V_I = V_{DD}$			10	μA
Input "L" level Voltage	$I_{IL}(1)$	$\overline{FM}$, $\overline{MW}$, $\overline{LW}$, $\overline{SK}$, $\overline{UP}$, $\overline{DOWN}$, $\overline{MANU}$, $\overline{MEMO}$, $\overline{57K}$, STH	$V_I = V_{SS}$	−170		−24	
	$I_{IL}(2)$	$\overline{BUC}$, S-Curve, M-U/D		−10			μA
	$I_{IL}(3)$	$\overline{CH1}$ ~ $\overline{CH6}$, $\overline{CH7}$	$V_I = V_{SS}$, Output MOS-Tr OFF.	−10			
Output "H" level Voltage	$V_{OH}(1)$	M/L out, $\overline{DX\text{-}LO}$, MUTE, F-Tune	I_{OH} = −1mA	V_{DD}−1.0			V
	$V_{OH}(2)$	F/A out	I_{OH} = −2mA	V_{DD}−1.0			
	$V_{OH}(3)$	B10	I_{OH}=−0.5mA	V_{ref}−0.06			
	$V_{OH}(4)$	B9		V_{ref}−0.12			
	$V_{OH}(5)$	B8		V_{ref}−0.24			
	$V_{OH}(6)$	B1 ~ B7		V_{ref}−0.48			
Output "L" level Voltage	$V_{OL}(1)$	M/L out, $\overline{DX\text{-}LO}$, MUTE, F-Tune	I_{OL} = 1mA			1.0	V
	$V_{OL}(2)$	F/A out, $\overline{F\text{-}DISP}$, $\overline{M\text{-}IND}$	I_{OL} = 2mA			1.0	
	$V_{OL}(3)$	B10	I_{OL} = 0.5mA			0.06	
	$V_{OL}(4)$	B9				0.12	
	$V_{OL}(5)$	B8				0.24	
	$V_{OL}(6)$	B1 ~ B7				0.48	
	$V_{OL}(7)$	CH1 ~ CH6, CH7.	I_{OL} = 20mA			2.0	
On Resistance	R_{ON}	CV out, CV in, Mane-Tune	V_{IN}=0~V_{ref}V RL = 100kΩ			300	Ω
Oscillation Period	$T_{(OSC)}$	CR1	R_{X1} = 91kΩ, C_{X1} = 6800pF V_{DD} = 9.0V Refer to Fig. 1.		0.4		msec
Operation Period	$T_{(multi)}$	CR2	R_{X2} = 240kΩ, C_{X2} = 22μF V_{DD} = 90V, Refer to Fig. 2.		500		msec
Current Dissipation	$I_{DD}(1)$	V_{DD}	V_{DD} = +10.0V V_{ref} = +8.0V $\overline{BUC}$ = "H", S-Curve= ½ V_{ref}, Refer to Fig. 3.			5.0	mA
	$I_{DD}(2)$	V_{DD}	V_{DD} = +55V, V_{ref} = 0V, $\overline{BUC}$ = "L", Refer to Fig. 4.			200*	μA
	I_{ref}	V_{ref}	V_{DD} = 8.0~ +10.0V V_{ref} = +8.0V S-Curve = (V_{ref}/2) No load on B1~B10 Refer to Fig. 5.			0.7	mA

Note: *: LC7207: 50μA
When current flows into the device, the direction of current is taken to be positive (no signal);
When current flows out of the device, it is taken to be negative.

9. Measuring Circuit

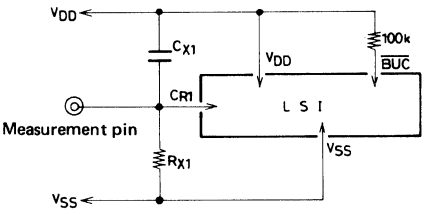
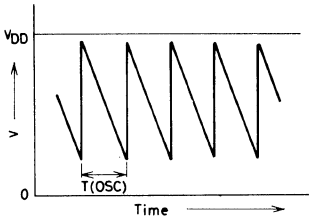


Fig. 1 Oscillation period measurement circuit



Oscillation waveform

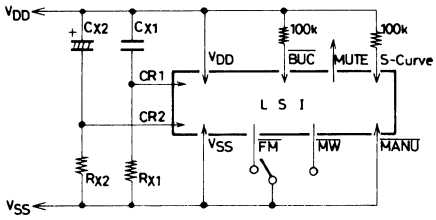
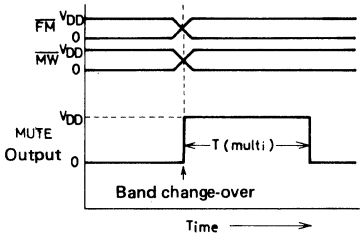


Fig. 2 Operating period [T(multi)] measurement circuit



Operating period waveform

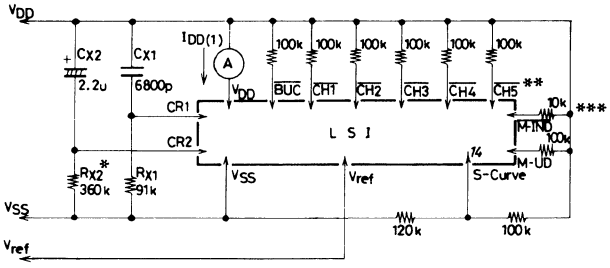


Fig. 3 Current dissipation $I_{DD}(1)$ measurement circuit

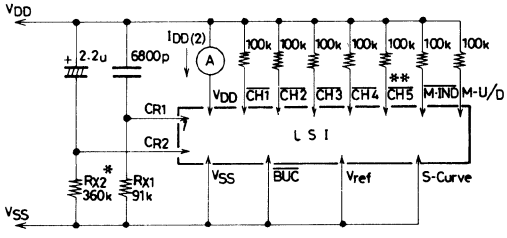


Fig. 4 $I_{DD}(2)$ measurement circuit

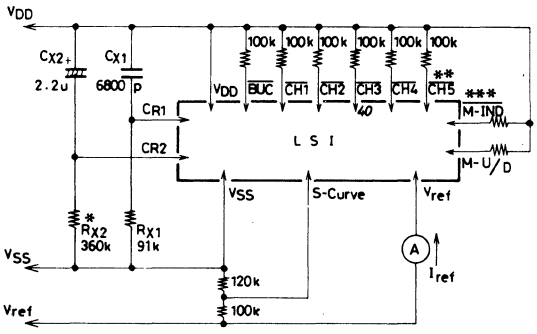


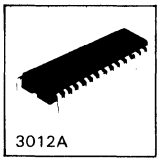
Fig. 5 I_{ref} measurement circuit

* For LC7201, 7202, 7203
R x 2 = 240kΩ

** CH6 added for LC7201 and 7203.
CH6, CH7 added for LC7207.

*** M-IND is only for LC7200, 7207.

LC7210



C MOS LSI

Tuning Circuit of PSL² Electronic Tuning System

Ⓔ 884A

The LC7210 is a C MOS LSI for the tuning section in the FM/AM radio PSL² (Phase and Signal Locked Loop) synthesizer electronic tuning system which realizes the successful introduction of the stable tuning being characteristic of PLL synthesizer, the reliable auto search tuning (covering all the world, multiband, etc.) being characteristic of SL² (Signal Locked Loop) voltage synthesizer and the reception at the just tuning point by means of AFC operation. By using a 4-bit microcomputer as a controller in conjunction with a prescaler (÷100, the high-performance and multifunction FM/AM synthesizer tuner can be made available.

1. Use

LSI for tuning section in FM/AM radio PSL² synthesizer electronic tuning system.

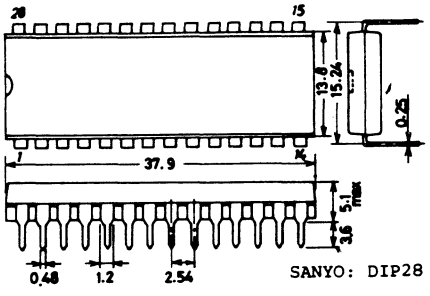
2. Features

- Controlling with a microcomputer makes it possible to extend the reception range over multiband (FM, MW, LW/FM, MW, SW1, SW2/TV, FM, MW, etc.).
- For the tuning operation, three methods of auto search, preset, and manual are available.
- The tuning control is made possible at the PLL synthesizer mode, SL² voltage synthesizer auto search mode, S curve AFC reception mode, local oscillation frequency count mode.
- The low reference oscillation frequency of 32kHz causes little harmonic interference to FM band.
- With the FM-IF ceramic filter variation adjusting function provided (±150kHz /10kHz step fine adjustment), a multirank ceramic filter can be used.
- The capability of S curve AFC reception can make the PLL control step small (10kHz step) by lowering the comparison frequency (f_{ref}=0.1kHz : FM band) regardless of the CN ratio at the time of PLL operation.
- +5V single power supply, C MOS process, DIP 28 pins.

3. Functions

- SL² auto search control.
- PLL control (Number of frequency divisions FM : 39999 max, AM : 3999 max.)
- Analog switch for S curve AFC.
- Local oscillation frequency counter (Number of counts FM, AM : 39999 max./ 10ms).
- Data generation for FM band IF offset fine adjustment (5 bits).

Case Outline 3012A-D28IC
(unit:mm)



4. Main Operation

(1) Search Operation

When a broadcasting signal is being caught by means of the search operation, the counter system is constantly doing the count operation. The local oscillation frequency information caught is transferred to the control CPU, goes through the intermediate frequency correction (FM : IF offset correction), and is displayed as the received frequency information. Based on the S signal input, the search output controls the speed of search and the execution and stop of search.

The search output is outputted from pin S out and the search voltage is obtained by connecting the external filter. The search voltage is applied to the variable capacitance diode.

(2) PLL Operation

When the preset method and manual search method are used, the counter system operates as a preset up counter and the frequency divided output (f/N) of the local oscillation input is obtained. By applying the comparison frequency (f_{ref}) and frequency divided output (f/N) to the phase comparator, the charge pump output is obtained and the PLL operation is performed.

f_{ref} : 1kHz (AM), 0.1kHz (FM)

(3) AFC Operation

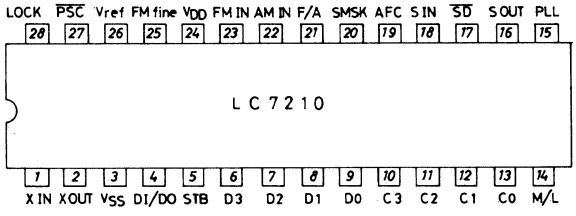
When the broadcasting signal of FM radio band is caught by means of the auto search operation and the input at pin $\overline{SD}$ is at "0" level, the analog switch between pins S in and S out becomes conductive and the local oscillation frequency is controlled, so that the reception is made at the middle point of the S signal (SL^2 reception). At this moment the local oscillation frequency information is caught through the counter system having the frequency count function, and the frequency is displayed and the frequency information at the time of preset is formed based on this information.

Note) The reception state of the LC7210 depends on the input level at pin $\overline{SD}$ as follows.

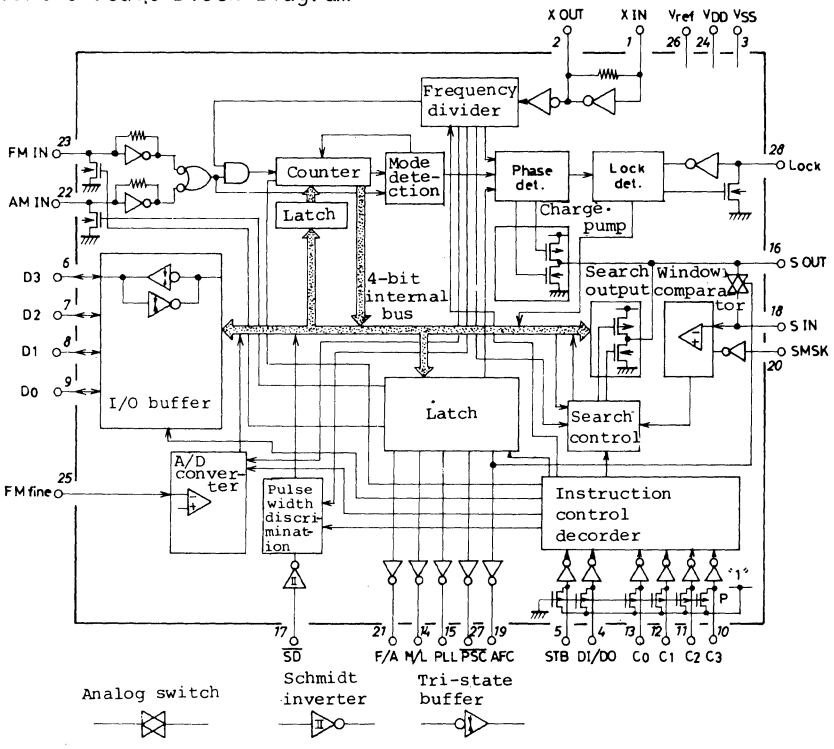
Changeover is done in response to the instruction from the controller (LM6402).

$\overline{SD}$ Input \ Mode		Auto search mode		Preset or Manual
		Tuning correction	Reception	
$\overline{SD}$="0"	FM	AFC	AFC	AFC
	MW,LW	AFC	PLL	PLL
SD="1"		AFC	PLL	PLL

5. Pin Assignment



6. Equivalent Circuit Block Diagram



Pin name	Input/output	Function
C_0, C_1, C_2, C_3	Input	Pull-up specification. Input for making the signal to designate the logic to which the internal data bus should be connected. Whether the data is input mode/output mode depends on DI/DO. (Refer to the following Table.)
M/L	Output	Push-pull. "1" only when the reception band is MW.
PLL	Output	Push-pull. "1" is outputted during the PLL operation.
S out	Output	Connected to the tri-state push-pull and analog switch. . Charge pump output is obtained at the PLL mode. . Auto search control output is obtained at the SEARCH mode. . Conductive to input pin S in through the analog switch at the AFC mode. . High impedance state at other than the above.
$\overline{SD}$	Input	Schmidt inverter input. Input pin for controlling which of $\overline{SL}^2$ reception (AFC reception) or PLL reception ($\overline{SD}$=1) should be selected at the time of FM reception.
S in	Input	Connected to the analog switch and comparator input. . Conductive to S out through the analog switch at the AFC mode, thereby enabling the AFC reception. . At the time of auto search, the S signal is passed through the window comparator for identification of SH/SL, which is used for controlling the speed, stop of search.
AFC	Output	Push-pull. "1" is outputted at the AFC mode. "0" is outputted at other than the AFC mode.
SMSK	Input	Schmidt inverter input. Input (SMSK=1) for inhibiting the control of search stop, speed by SH/SL at the time of auto search SMSK ="0" provides the control.
F/A	Output	Push-pull output. Band information output pin. "1" is outputted at the time of FM band only.
AM in	Input	Local oscillation signal input pin having a feedback resistor attached amplifier and a pull-down transistor. The pull-down transistor is turned ON at the FM mode.
FM in	Input	Pin having a feedback resistor attached amplifier and a pull-down resistor, to which 1/100 frequency divided output of the local oscillation signal is inputted. The pull-down transistor is turned OFF only at the FM mode with no AFC reception made.
V_{DD}	—	System power supply. 5V typ. is applied.
FM fine	Input	Comparator input. Input pin for generating the data to correct the center frequency shift of the FM IF filter.

Pin name	Input/output	Function
V_{ref}	—	Power supply (pin S in) for setting the window comparator level and power supply for the A/D comparator ladder network at pin FM fine.
$\overline{PSC}$	Output	Push-pull output. "0" is outputted when the PLL operation or count operation is performed at the FM mode, and "1" is outputted at any other time than this (at other than the FM mode, or AFC reception at the FM mode).
LOCK (Note 1)	Input/output	Inverter input pin having a pull-down transistor. With a CR integration circuit connected, lock detection of the PLL operation is done. Inputting "1" makes the lock state; and inputting "0" makes the unlock state.

Note 1) With the N-channel pull-down transistor attached inside the LC7210, pin LOCK must not be connected direct to the power supply such as V_{DD}, V_{ref}, etc.

8. Connection of LC7210 with LM6402A

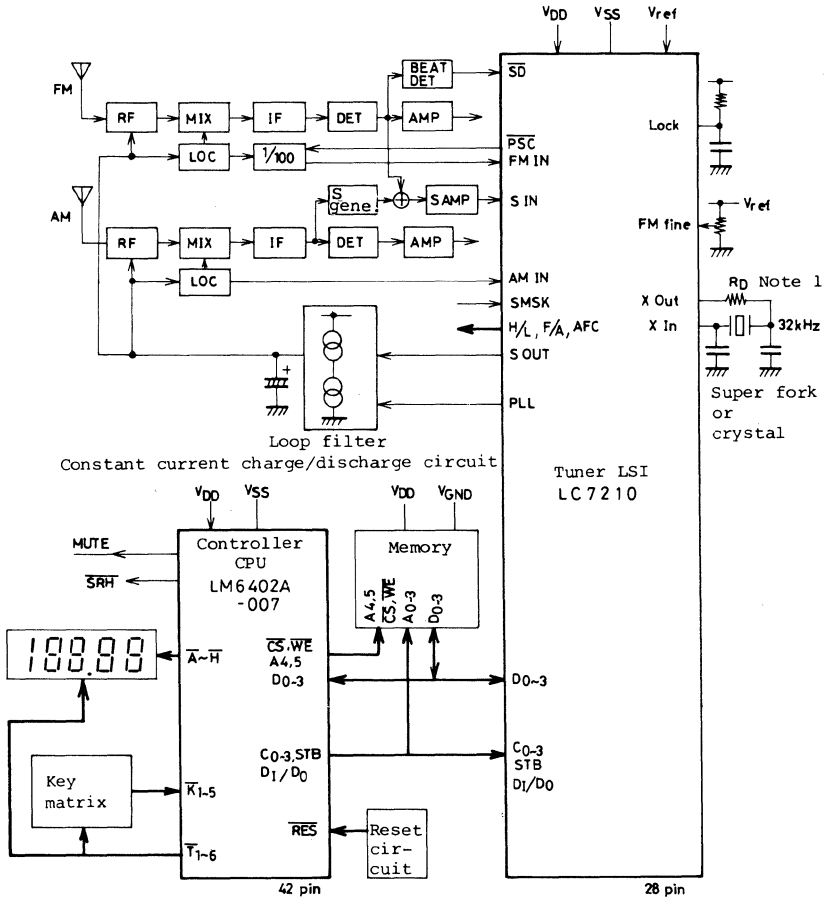
8-1 DI/DO="1" : Inputting into LC7210 externally through pin D (Completion of inputting needs STB="1".)

Control input C_3	C_2	C_1	C_0	Operation (LC7210 internal state is set externally.)
0	0	0	0	BCD 5-digit counter MSD preset data setting.
0	0	0	1	BCD 5-digit counter 4th preset data setting.
0	0	1	0	BCD 5-digit counter 3rd preset data setting.
0	0	1	1	BCD 5-digit counter 2nd preset data setting.
0	1	0	0	BCD 5-digit counter LSD preset data setting
0	1	0	1	Instruction of PLL operaiton (D_3="1"), count operation (D_3="0").
0	1	1	0	Band designation FM (D_3="1",D_2="0"),MW (D_3="0",D_2="1"),LW (D_3="0", D_2="0").
0	1	1	1	Instruction of search execution, stop : Search execution (D_3="1"), Search stop (D_3="0").
1	0	0	0	AFC operation control : AFC operation (D_3="1"),AFC stop (D_3="0")
1	0	0	1	Search direction control : Upward search (D_3="1"), Downward search (D_3="0").
1	0	1	0	Search speed change : JHS (high speed search) D_3="1", JLS (low speed search) D_3="0".
1	0	1	1	Count operation start timing instructing D input DON'T CARE.
1	1	0	0	Prescaler control signal generation, $\overline{PSC}$="0" (D_3="1") at other than AFC mode in FM band, PSC="1" (D_3="0") at all times.
1	1	0	1	FM fine A/D converting operation start timing instruction : Conversion start (D_3="1").
1	1	1	1	Synchronization system reset D input DON'T CARE

8-2 DI/DO="0" : Outputting internal contents of LC7210 outward through pin D_3 to 0.

Control input C_3 C_2 C_1 C_0	Operation
0 0 0 0	Transfer of BCD 5-digit counter MSD data to bus.
0 0 0 1	Transfer of BCD 5-digit counter 4-digit data to bus.
0 0 1 0	Transfer of BCD 5-digit counter 3-digit data to bus.
0 0 1 1	Transfer of BCD 5-digit counter 2-digit data to bus.
0 1 0 0	Transfer of BCD 5-digit counter LSD data to bus.
0 1 0 1	Search speed information output : High speed search (HS)--- "1"→D_3, Low speed search (LS)--- "0"→D_3.
0 1 1 0	PLL system lock state information output : Lock--- "1"→D_3, Unlock ---"0"→D_3.
0 1 1 1	FM fine A/D converting data output : MSB (Bit 5)→D_0.
1 0 0 0	FM fine A/D converting data output : LSB (Bit 1)→D_0.
1 0 0 1	$\overline{SD}$ pulse width discriminating output : $\overline{SD}$←"0" --- "1"→D_3, SD← "1" --- "0"→D_3.
1 0 1 0	S in input level information output : SH level input --- "1"→D_3, SL level input --- "1"→D_2.
1 1 1 0	Search state information output : Search operation --- "1"→D_3, Search stop ---"0"→D_3.

9. PSL^2 System Application Block Diagram



Note 1) If the super fork (EMF-A 32.000kHz) is used, no R_D is needed.
If the crystal (Kyoto Ceramic : KF 38J) is used, R_D is 220kohm ±10%.

10. Main Specifications

Absolute Maximum Ratings at T_a=25°C±2°C, V_{SS}=0V

Maximum Supply Voltage	V_{DD}		-0.3 to +8	V
	V_{ref}		-0.3 to +V_{DD}	V
Input Voltage	V_I		-0.3 to V_{DD}+0.3	V
Output Voltage	V_O	Output transistor Off	-0.3 to V_{DD}+0.3	V
Input-to-output Potential Difference at ON	V_I-V_O	Across S in and S out at analog SW ON.	-0.5 to +0.5	V
Output Power at Output Pin	$P_O$max	F/A,M/L,PLL,$\overline{PSC}$,Pin AFC only.	20	mW
Allowable Power Dissipation	$P_d$max	T_a≦75°C	150	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Range at T_a=25±2°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	T_a=-30 to +75°C	4.5	5	5.5	V
	V_{ref}		3.8	4	V_{DD}-0.3	V
"H" Level Input Voltage	$V_{IH}(1)$	STB,C_3 to $_0$,DI/DO,LOCK	0.75V_{DD}		V_{DD}	V
	$V_{IH}(2)$	D_0 to $_3$	0.75V_{DD}		V_{DD}	V
	$V_{IH}(3)$	$\overline{SD}$,SMSK	0.75V_{DD}		V_{DD}	V
	$V_{IH}(4)$	S in; Ta=-30 to +75°C	$V_{ref}\left(\frac{3R}{4R}+0.05\right)$		V_{DD}	V
"M" Level Input Voltage	V_{IM}	S in; Ta=-30 to +75°C	$V_{ref}\left(\frac{R}{4R}+0.05\right)$		$V_{ref}\left(\frac{3R}{4R}-0.05\right)$	V
"L" Level Input Voltage	$V_{IL}(1)$	STB,C_0 to $_3$,DI/DO,LOCK	V_{SS}	0.25V_{DD}		V
	$V_{IL}(2)$	D_0 to $_3$	V_{SS}	0.25V_{DD}		V
	$V_{IL}(3)$	$\overline{SD}$,SMSK	V_{SS}	0.25V_{DD}		V
	$V_{IL}(4)$	S in; Ta=-30 to +75°C	V_{SS}		$V_{ref}\left(\frac{R}{4R}-0.05\right)$	V
Operating Frequency	f in	AM in,FM in;0.7Vp-p;Ta-30 to +75°C	0.6		2.2	MHz
Input Amplitude	V in	AM in,FM in;duty50%, f in=2.2MHz	0.7			Vp-p
Input Voltage Range	$V_I(1)$	FM fine	V_{SS}		V_{ref}	V
	$V_I(2)$	S in	V_{SS}		V_{DD}	V
Oscillation Frequency	f_{osc}	X in,X out;Resonator:Crystal or super fork, Refer to test circuit.	30	32	34	kHz

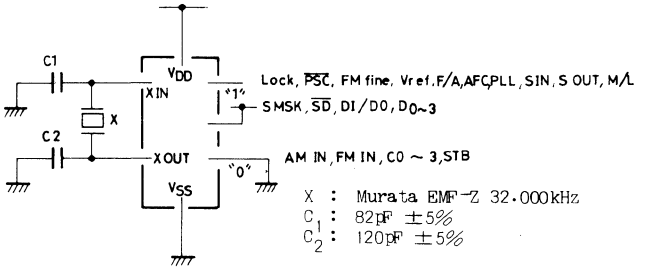
Electric Characteristics at T_a=25±2°C

			min	typ	max	unit
"H" Level Input Current	$I_{IH}(1)$	STB,C_0 to $_3$,$\overline{SD}$,SMSK,V_I=V_{DD}	0		10	uA
	$I_{IH}(2)$	S in;AFC off,V_I=V_{DD}	0		10	uA
	$I_{IH}(3)$	FM fine;V_I=V_{DD}	0		3	uA
"L" Level Input Current	$I_{IL}(1)$	D_0 to $_3$,DI/DO=1;V_I=V_{SS}	-10		0	uA
	$I_{IL}(2)$	SD,SMSK;V_I=V_{SS}	-10		0	uA
	$I_{IL}(3)$	S in;AFC off,V_I=V_{SS}	-10		0	uA
	$I_{IL}(4)$	FM fine;V_I=V_{SS}	-3		0	uA
	$I_{IL}(5)$	STB,DI/DO,C_0 to 3;V_{DD}=4.5 to5.5 V, V_I=V_{SS}	-800		-100	uA
Output Off Leak Current	$I_{OFF}(1)$	LOCK,Output stage OFF,V_O= V_{SS} to V_{DD}	-3		3	uA
	$I_{OFF}(2)$	S out;Output stage OFF,V_O= V_{SS} to V_{DD}	-5		5	uA
	$I_{OFF}(3)$	D_0 to $_3$,DI/DO=1,V_O=V_{SS} to V_{DD}	-10		10	uA
"H" Level Output Voltage	$V_{OH}(1)$	D_0 to $_3$;DI/DO=0,I_{OH}= -0.25mA	V_{DD}-0.5		V_{DD}	V
	$V_{OH}(2)$	PLL,F/A,M/L;I_{OH}=-0.5mA	V_{DD}-0.6		V_{DD}	V
	$V_{OH}(3)$	S out;(PLL mode) I_{OH}= -0.5mA	V_{DD}-0.5		V_{DD}	V
	$V_{OH}(4)$	S out;(search mode) I_{OH}= -0.5mA	V_{DD}-0.5		V_{DD}	V

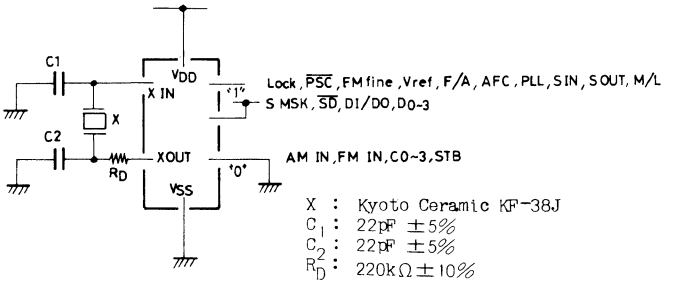
			min	typ	max	unit
"H" Level Output Voltage	$V_{OH}(5)$	$\overline{PSC}$; I_{OH}=-0.5mA	V_{DD}-1.2		V_{DD}	V
	$V_{OH}(6)$	AFC; I_{OH}=-0.5mA	V_{DD}-0.6		V_{DD}	V
"L" Level Output Voltage	$V_{OL}(1)$	D_0 to 3; DI/DO=0, I_{OL}=0.25mA	V_{SS}	V_{SS}+0.5		V
	$V_{OL}(2)$	PLL, F/A, M/L; I_{OL}=0.5mA	V_{SS}	V_{SS}+0.5		V
	$V_{OL}(3)$	S out; (PLL mode) I_{OL}=0.5mA	V_{SS}	V_{SS}+0.5		V
	$V_{OL}(4)$	S out; (Search mode) I_{OL}=0.5mA	V_{SS}	V_{SS}+0.5		V
	$V_{OL}(5)$	$\overline{PSC}$; I_{OL}=5mA	V_{SS}	V_{SS}+3		V
	$V_{OL}(6)$	AFC; I_{OL}=0.5mA	V_{SS}	V_{SS}+0.5		V
	$V_{OL}(7)$	LOCK; I_{OL}=1mA	V_{SS}	V_{SS}+0.5		V
ON Resistance	AFC on	Across S in and S out; AFC on, I=1.2mA $\lvert V_S\ in - V_S\ out \rvert \leqq 0.3V$, $V_{SS} \leqq V_S\ in, V_S\ out \leqq V_{DD}$			250	ohm
Current Dissipation	I_{DD}	V_{DD}, no load, V_{DD}=5.5V			5	mA
	I_{ref}	V_{ref}, V_{ref}=5.5V			1.2	mA

Test Circuit

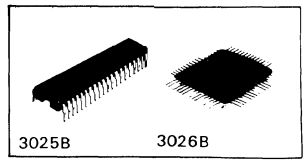
(1) Super fork EMF-A 32.000kHz (Murata Mfg. Co., Ltd.)



(2) Crystal KF-38J (Kyoto Ceramic)



LC7220, -1, -2, -5, -6, -7



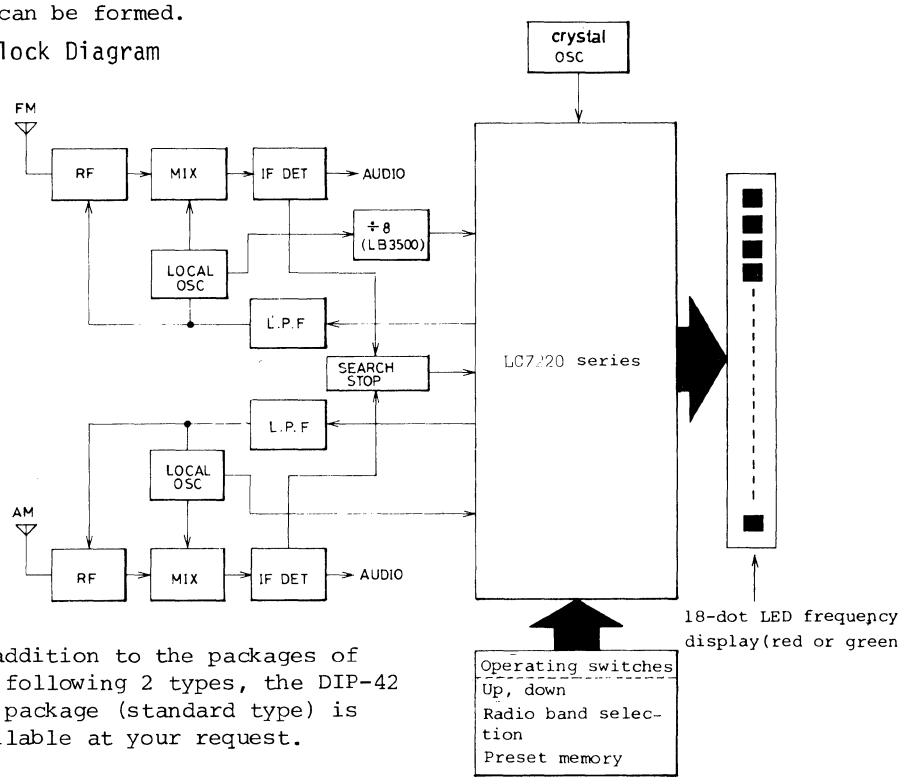
C MOS LSI

PLL Synthesizer Tuner and Controller for FM/AM Radio

Ⓔ 865D

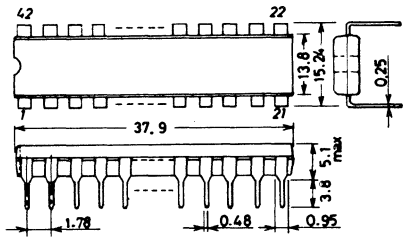
The LC7220 series is a PLL frequency synthesizer C MOS LSI designed for use in FM/AM 2-radio band radios. If used in conjunction with the LB3500 (1/8 frequency division prescaler), an electronic tuning system with 18-dot analog frequency display can be formed.

System Block Diagram



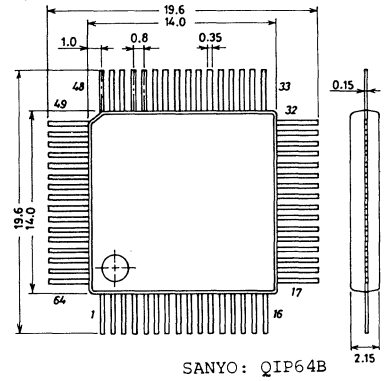
In addition to the packages of the following 2 types, the DIP-42 pin package (standard type) is available at your request.

Case Outline 3025B-D42SIC
(unit:mm) LC7200,7221,7222



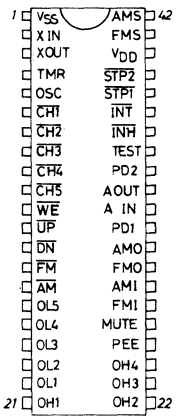
SANYO: DIP42S

Case Outline 3026B-Q64BIC
(unit:mm) LC7225,7226,7227

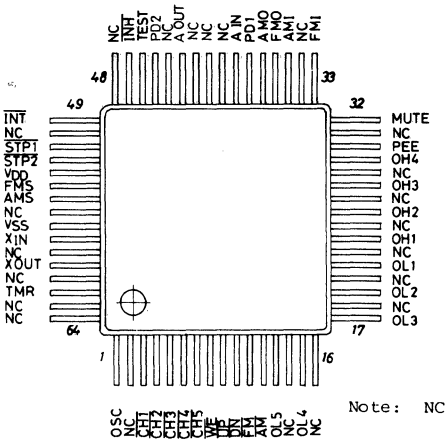


SANYO: QIP64B

Pin Assignment



LC7220,7221,7222



LC7225,7226,7227

Note: NC pin:Open

The LC7220 series offers a choice of the following types according to the destination and package.

Type No.	Package	Area	Radio band	Frequency	Step	f_{ref}	IF
LC7220 LC7225	DIP42S QIP64	U.S.A.	FM	87.5 to 108.1 MHz	200 kHz	6.25 kHz	+10.70, +10.75 MHz
			AM(1)*	520 to 1610 kHz	10 kHz	10 kHz	+450 kHz
			AM(2)*	522 to 1611 kHz	9 kHz	9 kHz	+450 kHz
LC7221 LC7226	DIP42S QIP64	Japan	FM	76.0 to 90.0 MHz	100 kHz	6.25 kHz	-10.70, -10.65 Mhz
			AM	522 to 1611 kHz	9 kHz	9 kHz	+450 kHz
LC7222 LC7227	DIP42S QIP64	Europe (U.S.A.)	FM	87.5 t o108.1 MHz	50 kHz	6.25 kHz	+10.70, +10.75 MHz
			AM(1)*	520 to 1610 kHz	10 kHz	10 kHz	+450 kHz
			AM(2)*	522 to 1611 kHz	9 kHz	9 kHz	+450 kHz

* AM(1) or AM(2) is selected by changing the pin connection.

1. Tuning method

. Manual tuning : Channel goes up or down at a 1 step/push rate.
. Auto tuning : Channel goes up or down fast.
  Auto scan mode —— Fast scanning continues regardless of the presence or absence of station.
  Auto search mode —— Searching continues until a station is detected.
  Change-over from manual tuning to auto tuning depends upon the period of time for which the $\overline{UP}$ or $\overline{DN}$ switch is pushed.
. Preset tuning : 5 stations of FM, AM each can be preset.

2. Frequency display

. For both FM and AM, 18-dot (or 9-dot) LED (red or green) display is made.
. Lighting system is static and LED driver is built in.

3. Features

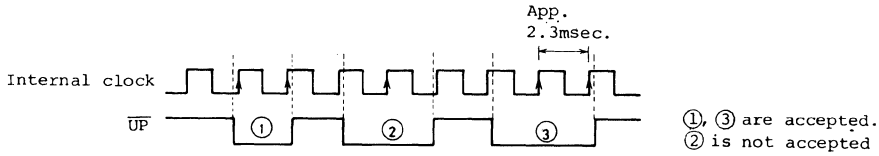
. Display, operating key, internal operation are all static.
. Phase comparator outputs are assigned to FM and AM respectively.
. Amplifier for low-pass filter is built in : N channel open drain
. Sound "peep"generating output is provided to make it possible to check the key operation auditorily.
. Muting output is provided to eliminate the noise to be generated at the time of key operation, etc.
. A quarts oscillator of 7.2MHz is used for reference frequency.
. Supply voltage V_{DD} is 4.5 to 6.5 V. (Backup voltage of 2.0V min. is usable while supply voltage is turned OFF.)

4. Description of operation

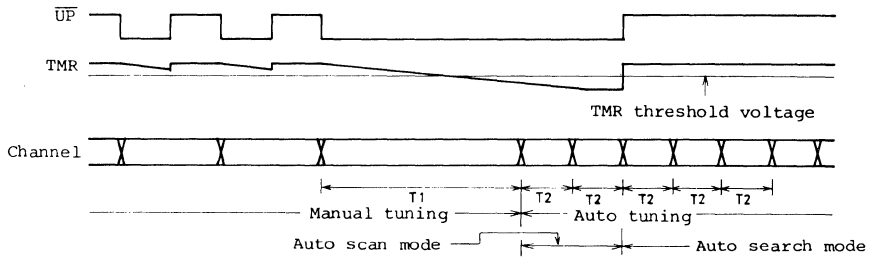
4-1 Tuning operation

(1) Up and down tuning (manual tuning, auto tuning).
  .Pushing the $\overline{UP}$ or $\overline{DN}$ switch causes channel to go up or down.
  .Considering a possible use of rotary switch to be connected to the $\overline{UP}$ and $\overline{DN}$ pins, the operation speed inside the LSI is made faster to secure the

reliable operation in response to a signal of more than approximately 4.6 msec. pulse width.



.Change-over form manual tuning to auto tuning depends upon the period of time for which the $\overline{UP}$ or $\overline{DN}$ switch is pushed. The period of time which elapses until this change-over occurs depends upon the time constant of a resistor and a capacitor connected to the TMR pin.

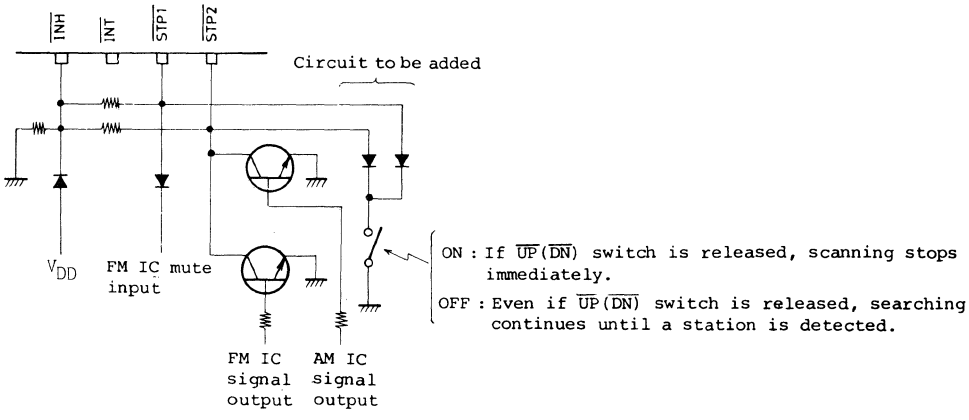


T1 : Period of time depending upon the time constant of a resistor and a capacitor connected to the TMR pin.
T2 : Period of time (2ø) depending upon the oscillation period (ø) of the OSC pin.

■ Manual tuning
Each time the $\overline{UP}$ or $\overline{DN}$ switch is pushed, channel goes up or down at a 1 step/push rate. When the upper (lower) band edge is reached, no operation occurs even if the $\overline{UP}$($\overline{DN}$) is further pushed.

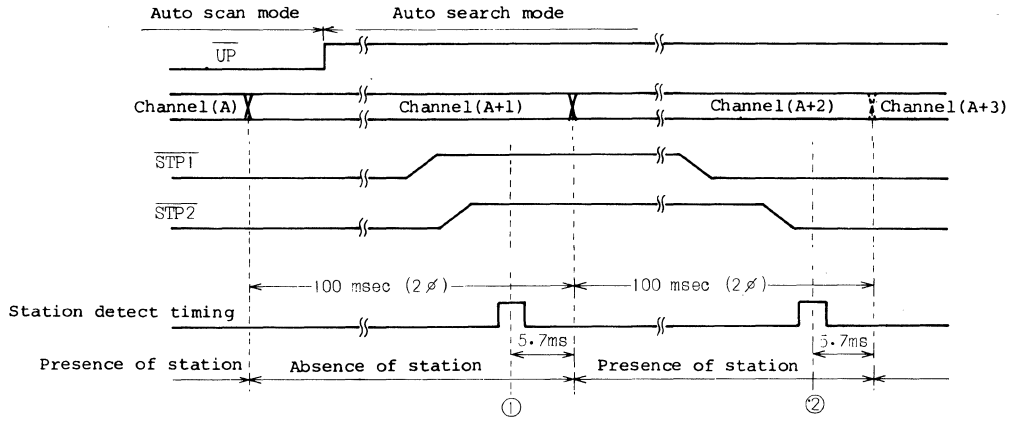
■ Auto tuning (Auto scan mode —— $\overline{UP}$ or $\overline{DN}$ switch is held pushed.)
In the auto scan mode, fast scanning continues with other key input neglected until the backup state takes place or the band edge is reached. When the band edge is reached, fast scanning stops.

.If it is desired to stop scanning immediately without causing the auto search mode to occur when the $\overline{UP}$ or $\overline{DN}$ switch is released at the auto scan mode, add the following circuit.



Auto tuning (Auto search mode —— $\overline{UP}$ and $\overline{DN}$ switches are released.)
In the auto search mode, searching stops when a station is detected. The presence or absence of station is detected approximately 5.7msec. before

the next channel change-over.



①, ② : Timing for detecting the presence or absence of station.

In order not to stop searching during the period of channel (A+1) having no station, it is necessary that at least either $\overline{STP1}$, or $\overline{STP2}$ goes high at timing (1). In order to also stop searching during the period of channel (A+2) having a station, both $\overline{STP1}$ and $\overline{STP2}$ go low at timing (2). For AM, however, $\overline{STP1}$ is neglected and $\overline{STP2}$ only works to stop searching. Auto searching is also stopped in the following cases.

- The $\overline{UP}$ or $\overline{DN}$ switch is pushed.
- The preset readout switch ($\overline{CH1}$ to $\overline{CH5}$) is pushed.
- Change-over of FM/AM radio band is made.
- The memory write switch ($\overline{WE}$) is pushed.
- The backup state takes place. (The low level voltage is applied to the $\overline{INH}$ pin.)

When the band edge is reached, the direction of searching is reversed.

(2) Preset tuning

5 stations of FM, AM each can be preset. When the initial supply voltage is applied, the frequency information of the lower band edge is preset in the memory with regard to FM and AM respectively.

.Readout of memory

Pushing one of the $\overline{CH1}$ to $\overline{CH5}$ switches causes the memory data of the relevant address to be read out and the LED driver for address display to be turned ON.

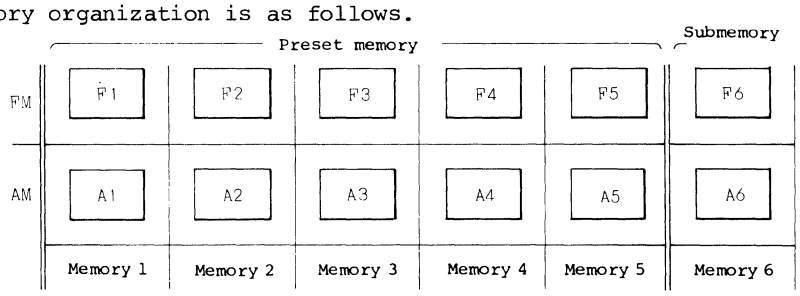
.Write of memory

Pushing the $\overline{WE}$ switch and then pushing one of the $\overline{CH1}$ to $\overline{CH5}$ switches for your desired write cause the channel being presently received to be written in the memory. Pushing the $\overline{WE}$ switch causes the LED driver to be turned ON, thereby indicating the memory writable state. The memory writable state is released in the following cases.

- One of the $\overline{CH1}$ to $\overline{CH5}$ switches is pushed to write in the memory.
- The $\overline{UP}$ or $\overline{DN}$ switch is pushed.
- Change-over of FM/AM radio band is made.
- The backup state takes place.

Even if the above key operation is not performed, the memory writable state is automatically released in 4.8 sec. (96ø).

The memory organization is as follows.



. Memory 1 to memory 5 correspond to $\overline{CH1}$ to $\overline{CH5}$ respectively. Memory 6 is a submemory to be used for memorizing the frequency at the time of manual /auto tuning. When change-over of FM/AM radio band is made, the memory data of the back side is read out in such a manner as F1↔A1, F2↔A2, F3↔A3, F4↔A4, F5↔A5, F6↔A6.

4-2 Display of received frequency

The LC7220 is used only for linear scale display by means of LED dot. If digital display is desired, it is necessary to read the local frequency by the use of counter IC. The available number of LEDs is 18 or 9. The number of channels per LED is shown below.

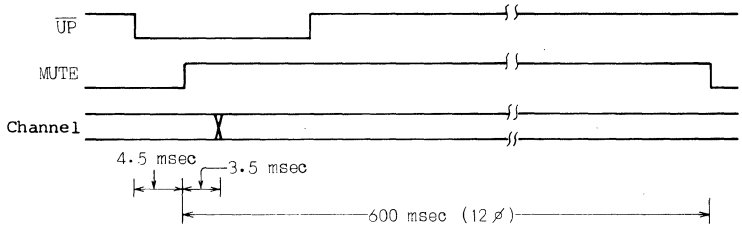
Radio band	Area	Number of channels	Number of channels/LED
FM	U.S.A.	104	6 (2)
	Japan	141	8 (5)
	European (U.S.A.)	412	24 (4)
AM	10kHz step	110	6 (8)
	9kHz step	122	7 (3)

The number of channels per LED shown in ( ) of the above Table is for the 18th LED only. In order to make the number of LEDs 9, connect the OH1 pin to the OH2 pin and the OH3 pin to the OH4 pin. In this case, the number of channels per LED becomes twice the number shown in the above Table.

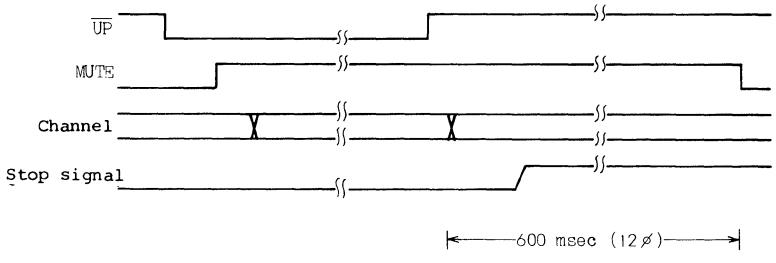
4-3 Muting output

Muting signal is outputted at the time of key operation to eliminate the noise to be generated at the time of channel change-over, etc.

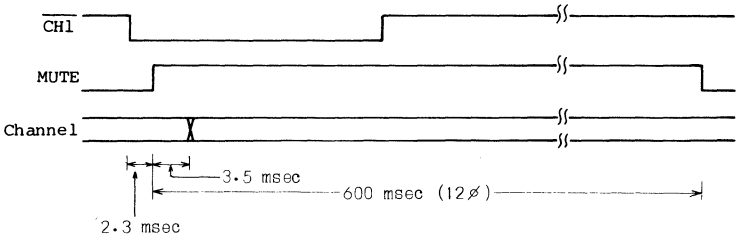
. Manual tuning ($\overline{UP}$, $\overline{DN}$)



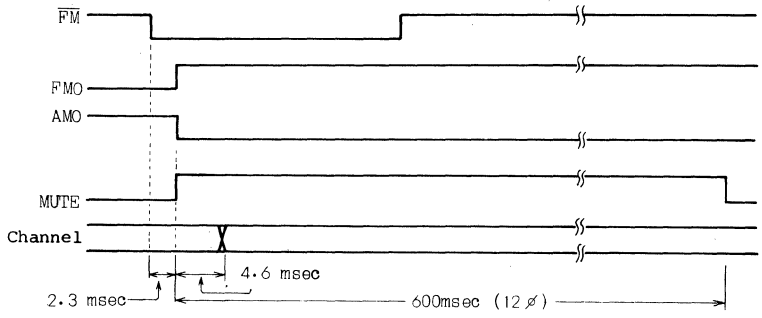
Auto search tuning ($\overline{UP}$,$\overline{DN}$)



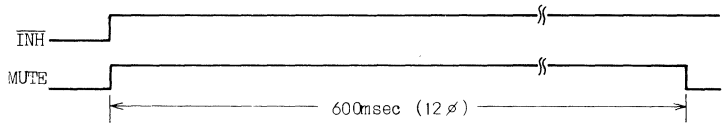
. Preset tuning ($\overline{CH1}$ to $\overline{CH5}$)



. FM/AM radio band change-over ($\overline{FM}$, $\overline{AM}$)



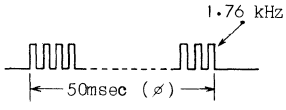
. Return from backup state ($\overline{INH}$)



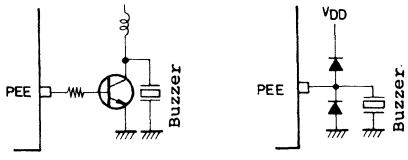
4-4 Sound "peep" output

In the following cases, sound "peep" is outputted to check the key operation.

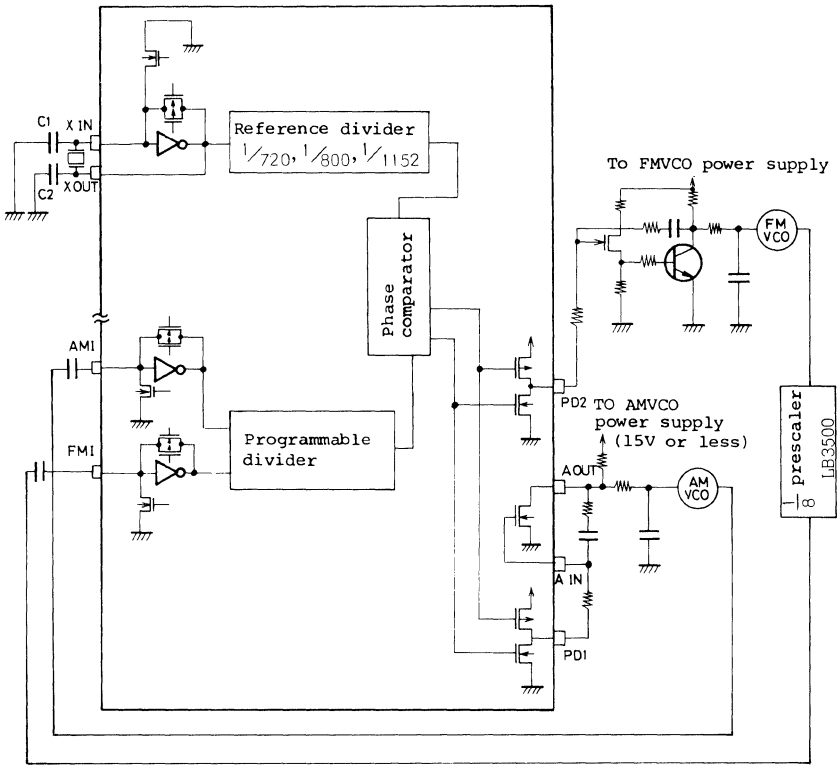
. Preset tuning is made.
. Change-over of FM/AM radio band is made.
. Manual tuning or auto tuning is being made.
. Return from the backup state is made.



In case of using a piezoelectric buzzer, it is necessary that a transistor is connected or buzzer is protected with diodes as shown below in order to prevent the LSI from being broken down by electric charge of the sound generator.



4-5 PLL Block diagram



.Since the PD1 and PD2 output the same signal, FM/AM radio band can share the low-pass filter for the purpose of reducing the cost.

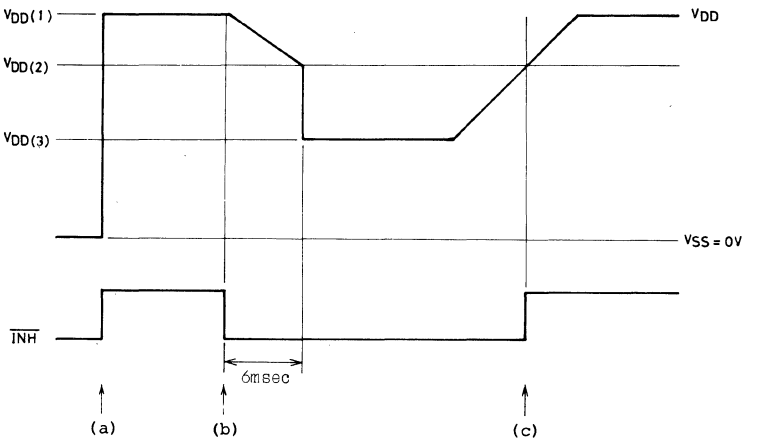
4-6 Precautions concerning power supply input and backup (Refer to the time chart on page 8.)

(a) In order to make the initial setting reliably, it is necessary to apply V_{DD}=4.5 to 6.5 V when the first power supply is inputted.

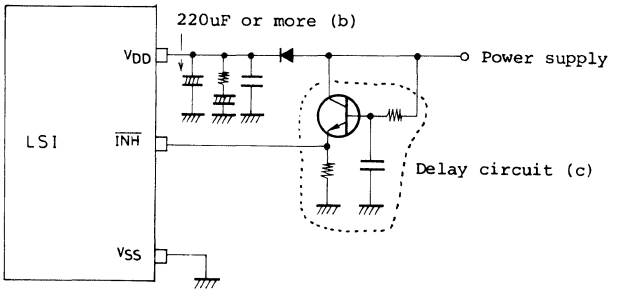
(b) If V_{DD} is made 3.5V or less (2V or more) at the backup state, it is necessary to hold V_{DD} at 3.5V or more (6.5V or less) for 6msec. or more after the $\overline{INH}$ pin is changed from "1" to "0". For this purpose, connect a capacitor of 220uF or more to the V_{DD} pin as shown in the circuit diagram on page 8.

(c) In order to release the backup state when V_{DD} is made 3.5V or less (2V or more) at the backup state, set the $\overline{INH}$ pin from "0" to "1" after V_{DD} becomes 3.5V or more (6.5V or less). For this purpose, connect a delay circuit to the $\overline{INH}$ pin as shown in the circuit on page 8.

Time chart



$V_{DD}(1)$	: Operating voltage of LSI including PLL section	4.5 to 6.5 V
$V_{DD}(2)$	: Operating voltage of other than PLL section	3.5 to 6.5 V
$V_{DD}(3)$	: Backup guaranteed voltage	2.0 to 6.5 V



4-7 Static operation

All operations of the control section including oscillation at the OSC pin are stopped at the time other than key operation. At this moment, since no frequency component lower than f_{ref} of the PLL is generated inside the LSI, no noise is generated.

4-8 Operation at backup state

In the backup state ($\overline{INH}$="0"), all key input pins other than $\overline{INT}$, $\overline{STP1}$, $\overline{STP2}$, FMS, AMS pins are set at V_{SS} level with every key operation rejected. All output pins other than XOUT pin have high impedance or are set at V_{SS} level, thereby inhibiting current from flowing out of the LSI. When returned from the backup state, the radio band and channel existed immediately before entering into the backup state take place.

4-9 Selection AM 9kHz/10kHz

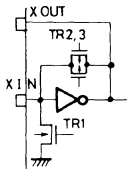
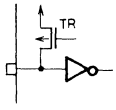
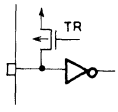
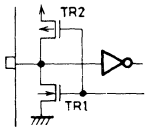
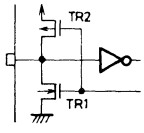
When selecting 9kHz step or 10kHz step by changing the AMS pin connection after inputting the power supply, apply the low level voltage to the $\overline{INT}$ pin for 1msec. or more after selection.

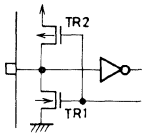
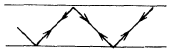
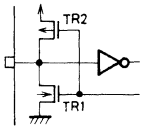
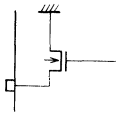
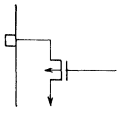
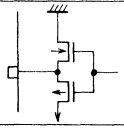
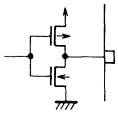
4-10 Initial setting

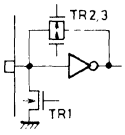
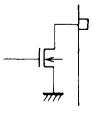
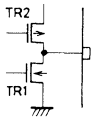
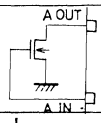
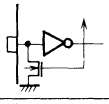
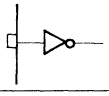
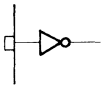
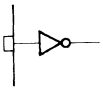
Setting the $\overline{INT}$ pin at V_{SS} level causes the initial setting inside the LSI to be made as follows.

- Preset memory ----- The frequency information of the lower band edge is preset in the memory with regard to FM and AM respectively.
- FM/AM mode -------- FM mode (FMO=1, AMO=0).
- Tuning mode ------- Up/down tuning mode.

5. Pin description

Pin name	Pin No. DIP	Pin No. QIP	Input/output type	Pin description
V_{SS}	1	57		Supply voltage apply pin —— Operation V_{DD}= 4.5 to 6.5 V, backup $V_{DD} \geqq 2V$
V_{DD}	40	53		
X_{IN}	2	58		A quarts oscillator(7.2MHz) for reference frequency is connected. In the backup state, TR1 is turned ON and TR2 and TR3 (feedback resistor) are turned OFF.
X_{OUT}	3	60		
TMR	4	62		The time constant is connected to fix the change-over time from manual tuning to auto tuning. In the backup state, TR is turned OFF.
OSC	5	1		The time constant is connected to fix each following time. If the OSC period is taken as ø (50msec.), . Sound "peep" output time —— ø(50 msec) . Scan speed —— 2ø(100msec) . Muting time —— 12ø(600msec) . Automatic release of pre-set memory writable time —— 96ø(4.8msec) In the backup state, TR is turned OFF.
$\overline{CH1}$	6	3		Address designate input pin of preset memory (Accept time 4.6msec. or more, active low level) TR1 is an LED driver and TR2 is a pull-up resistor. When the address is selected, TR1 is turned ON and TR2 is turned OFF. In the backup state, TR1 is turned ON and TR2 is turned OFF with regard to all input pins of $\overline{CH1}$ to $\overline{CH5}$.
$\overline{CH2}$	7	4		
$\overline{CH3}$	8	5		
$\overline{CH4}$	9	6		
$\overline{CH5}$	10	7		
$\overline{WE}$	11	8		Input pin for perset memory write (Accept time 1msec. or more, active low level). TR1 is an LED driver and TR2 is a pull-up resistor. Pushing the $\overline{WE}$ switch causes TR1 to be turned on and TR2 to be turned OFF, thereby leading to the preset memory writable state. Pushing one of the $\overline{CH1}$ to $\overline{CH5}$ switches at the writable state enables the preset memory write. The writable state is released in the following cases. . One of the $\overline{CH1}$ to $\overline{CH5}$ switches is pushed to write in the memory. . The $\overline{UP}$ or $\overline{DN}$ switch is pushed. . Change-over of FM/AM radio band is made. . The backup state takes place. . No operation is performed for 4.8msec.(96 ø) or more after pushing the $\overline{WE}$ switch. In the backup state, TR1 is turned ON and TR2 is turned OFF.
				Input pin for up/down tuning (Accept time 4.6msec. or more, active low level). TR1 is a pull-down resistor and TR2 is a pull-up resistor (continued on the next page)

pin name	Pin No. DIP	Pin No. QIP	Input/output type	Pin description
$\overline{UP}$	12	9		. Manual tuning:Channel goes up or down at a 1 step/push rate. . Auto tuning:Pushing the $\overline{UP}$ or $\overline{DN}$ switch longer than the period of time fixed by the time constant connected to the TMR pin causes channel to go up or down at a 100msec. (2ø)/step rate. . In the auto tuning, if the $\overline{UP}$ or $\overline{DN}$ swi-ch is held pushed, --- scanning continues even if a station is detected(auto scan mode). released, ------ searching stops if a station is detected (auto search mode). . The search waveform is triangular.  . When the band edge is reached, . scanning and tuning stop at the band edge in the auto scanning mode and manual tuning mode. . the direciton of searching is reversed in the auto search mode. In the backup state, TR1 is turned ON and TR2 is turned OFF.
$\overline{DN}$	13	10		
$\overline{FM}$	14	11		Input pin for FM/AM radio band change-over (Accept time 2.3msec. or more, active low level). TR1 is a pull-down resistor and TR2 is a pull-up resistor. In the backup state, TR1 is turned ON and TR2 is turned OFF.
$\overline{AM}$	15	12		
OL5	16	13		Output pin for frequency display LED driver. The frequency display LED is static-driven in conjunction with OH1 to OH4. In the backup state, this pin is turned OFF.
OL4	17	15		
OL3	18	17		
OL2	19	19		
OL1	20	21		
OH1	21	23		Output pin for frequency display LED driver. The frequency display LED is static-driven in conjunction with OL1 to OL5. In the backup state, this pin is turned OFF.
OH2	22	25		
OH3	23	27		
OH4	24	29		
PEE	25	30		Output pin for key operation check sound "peep". In the backup state, this pin is bound to go low.
MUTE	26	32		Output pin for muting signal. This pin goes high at the time of muting. The muting signal is outputted in the following cases. . The $\overline{UP}$ or $\overline{DN}$ switch is pushed. . The preset memory is read out. . Change-over of FM/AM radio band is made. . Return from the backup state is made. This pin is bound to go low.

Pin name	Pin No. DIP	Pin No. QIP	Input/output type	Pin description
FMI	27	33		Input pin for FM and AM programmable divider. For FM, the VCO frequency is divided into 1/8 and inputted. For AM, the VCO freqnency is direct inputted. The input sensitivity is FMI=0.7V_{p-p},AMI=0.5 Vp-p. For FMI, TR1 is turned ON and TR2 and TR3 (feedback resistor) are turned OFF at the time of AM radio band and backup state. For AMI, TR1 is turned ON and TR2 and TR3 (feedback resistor) are turned OFF at the time of FM radio band and backup state.
AMI	28	35		
FMO	29	36		Output pin for FM/AM radio band change-over control. FM radio band:FMO=Open,AMO=Low level AM radio band:FMO=low level,AMO=open
AMO	30	37		
PD1	31	39		Output pin for charge pump. The low-pass filter constant can be set independently for FM/AM each. In the backup state, TR1 and TR2 are turned OFF.
PD2	34	45		
AIN	32	39		Low-pass filter amplifier. Because of MOS FET, the high input impedance and short lockup time are possible.
AOUT	33	43		
TEST	35	46		Pin for LSI test. Normally, this pin is open or connected to V_{SS}.
$\overline{INH}$	36	47		Input pin for backup instruction. Applying the low level voltage causes the LSI to be in the backup state.
$\overline{INT}$	37	49		Input pin for initial state setting. Applying the low level voltage causes the LSI to be initialized.
$\overline{STP1}$	38	51		Input pin for applying stop signal at auto search mode. Auto searching stops in the following cases. FM:The low level voltage is applied to $\overline{STP1}$ and $\overline{STP2}$. AM:The low level voltage is applied to $\overline{STP2}$.
$\overline{STP2}$	39	52		
FMS	41	54		Input pin for FM IF selection. FMS="0" : IF=-10.70MHz —(Japanese spec.) IF=+10.70MHz —(U.S.A.,European specification) FMS="1" : IF=-10.65MHz —(Japanese spec.) IF=+10.75MHz —(U.S.A.,European specification)
AMS	42	55		Input pin for AM 9kHz/10kHz step selection. AMS="0" : 9kHz step AMS="1" : 10kHz step In Japan, the AMS pin must be connected to V_{SS}.

6. Main Characteristics

Maximum Ratings at T_a=25°C, V_{SS}=0V

Maximum Supply Voltage	V_{DD}	-0.3 to 7.5	V
Input Voltage	V_{IN}	All input pins -0.3 to V_{DD}+0.3	V
Output Voltage	$V_{OUT}(1)$	AMO,FMO,AOUT:output OFF -0.3 to 15	V
	$V_{OUT}(2)$	Output pins other than $V_{OUT}(1)$. -0.3 to V_{DD}+0.3	V
Output Current	$I_{OUT}(1)$	OH1 to OH4,OL1 to OL5, $\overline{CH1}$ to $\overline{CH5}$,$\overline{WE}$ 0 to 20	mA
	$I_{OUT}(2)$	FMO,AMO,AOUT 0 to 5	mA
Allowable Power Dissipation	$P_d$max	$T_a \leq$75°C 350	mW
Operating Temperature	T_{opg}	-30 to +75	°C
Storage Temperature	T_{stg}	-40 to +125	°C

Recommended Operation Condition at T_a=25°C

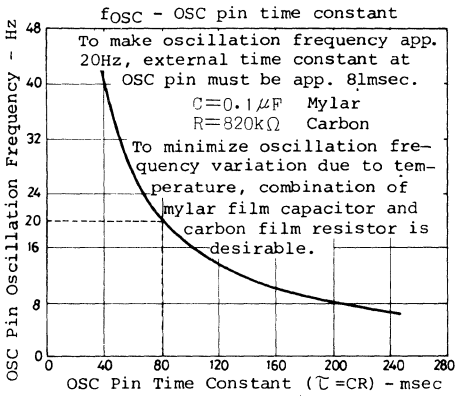
			min	typ	max	unit
Supply Voltage	$V_{DD}(1)$		4.5	5.5	6.5	V
	$V_{DD}(2)$	X'tal OSC	3.5		6.5	V
	$V_{DD}(3)$	Backup guaranteed	2.0		6.5	V
"H" Level Input Voltage	$V_{IH}(1)$	$\overline{CH1}$ to $\overline{CH5}$,$\overline{WE}$,$\overline{FM}$,$\overline{AM}$, $\overline{UP}$,$\overline{DN}$,$\overline{STP1}$ to $\overline{STP2}$, $V_{DD}(1)$,$V_{DD}(2)$	0.8V_{DD}			V
	$V_{IH}(2)$	FMS,AMS,$V_{DD}(1)$, $V_{DD}(2)$	0.95V_{DD}			V
	$V_{IH}(3)$	$\overline{INH}$,$V_{DD}(1)$,$V_{DD}(2)$	0.8V_{DD}			V
	$V_{IH}(4)$	$\overline{INH}$,V_{DD}=2.0 to 3.5V	0.85V_{DD}			V
	$V_{IH}(5)$	$\overline{INT}$,$V_{DD}(1)$,$V_{DD}(2)$	2.0		V_{DD}	V
	$V_{IH}(6)$	$\overline{INT}$,V_{DD}=2.0 to 3.5V	1.5		V_{DD}	V
"L" Level Input Voltage	$V_{IL}(1)$	$\overline{CH1}$ to $\overline{CH5}$,$\overline{WE}$,$\overline{FM}$,$\overline{AM}$,$\overline{DN}$, $\overline{STP1}$,$\overline{STP2}$,$V_{DD}(1)$,$V_{DD}(2)$			0.2V_{DD}	V
	$V_{IL}(2)$	FMS,AMS,$V_{DD}(1)$,$V_{DD}(2)$			0.05V_{DD}	V
	$V_{IL}(3)$	$\overline{INH}$,$V_{DD}(1)$,$V_{DD}(2)$			0.2V_{DD}	V
	$V_{IL}(4)$	$\overline{INH}$,V_{DD}=2.0 to 3.5V			0.15V_{DD}	V
	$V_{IL}(5)$	$\overline{INT}$,$V_{DD}(1)$,$V_{DD}(2)$	0		0.5	V
	$V_{IL}(6)$	$\overline{INT}$,V_{DD}=2.0 to 3.5V	0		0.4	V
Input Frequency	$f_{IN}(1)$	FMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $V_{IN}(1)$=0.7Vp-p	1.0		18	MHz
	$f_{IN}(2)$	AMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $V_{IN}(2)$=0.5Vp-p	0.2		3.0	MHz
Input Amplitude	$V_{IN}(1)$	FMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $f_{IN}(1)$=1.0 to 1.8MHz	0.7		0.9V_{DD}	Vp-p
	$V_{IN}(2)$	AMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $f_{IN}(2)$=0.2 to 3.0MHz	0.5		0.9V_{DD}	Vp-p
Crystal Oscillation Frequency	$f_{X'tal}$	X_{IN},X_{OUT}		7.2		MHz
OSC Oscillation Frequency	f_{OSC}	OSC,R=820kohm,C=0.1uF		20		Hz
TMR Time	T_{TMR}	TMR,R=240kohm,C=2.2uF		300		msec
$\overline{INT}$ Pin Time Constant	T_{INT}	$\overline{INT}$,rise time of V_{DD}, 200msec.	2000			msec

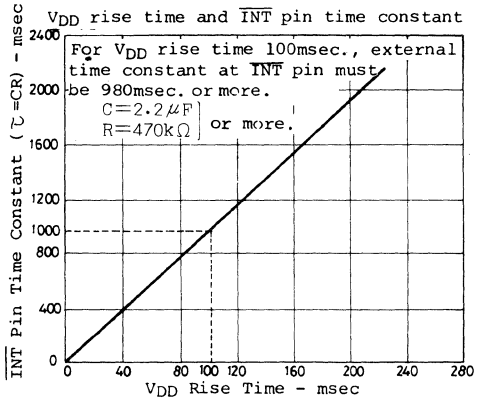
Electrical Characteristics at T_a=25°C, V_{DD}(1)			min	typ	max	unit
"H" Level Input Current	$I_{IH(1)}$	$\overline{INT}$, FMS, AMS, $V_I=V_{DD}$			2	uA
	$I_{IH(2)}$	$\overline{INH}$, $\overline{STP1}$, $\overline{STP2}$, $V_I=V_{DD}$			10	uA
	$I_{IH(3)}$	AIN, $V_I=V_{DD}$		0.01		nA
	$I_{IH(4)}$	$\overline{FM}$, $\overline{AM}$, $\overline{UP}$, $\overline{DN}$, $V_I=V_{DD}$	30		250	uA
"L" Level Input Current	$I_{IL(1)}$	$\overline{INT}$, FMS, AMS, $V_I=V_{SS}$			2	uA
	$I_{IL(2)}$	$\overline{INH}$, $\overline{STP1}$, $\overline{STP2}$, $V_I=V_{SS}$			10	uA
	$I_{IL(3)}$	AIN, $V_I=V_{SS}$		0.01		nA
	$I_{IL(4)}$	$\overline{FM}$, $\overline{AM}$, $\overline{UP}$, $\overline{DN}$, $V_I=V_{SS}$	30		250	uA
	$I_{IL(5)}$	$\overline{CH1}$ to $\overline{CH5}$, $\overline{WE}$, $V_I=V_{SS}$	30		250	uA
"H" Level Output Voltage	$V_{OH(1)}$	OH1 to OH4, I_O=15mA	V_{DD}-0.9			V
	$V_{OH(2)}$	PD1, PD2, I_O=0.5mA	V_{DD}-1.1			V
	$V_{OH(3)}$	MUTE, I_O=2mA	V_{DD}-1.1			V
	$V_{OH(4)}$	PFE, I_O=1mA	V_{DD}-1.1			V
"L" Level Output Voltage	$V_{OL(1)}$	$\overline{CH1}$ to $\overline{CH5}$, WE, I_O=15mA			1.0	V
	$V_{OL(2)}$	OL1 to OL5, I_O=15mA			0.6	V
	$V_{OL(3)}$	FMO, AMO, I_O=2mA			1.0	V
	$V_{OL(4)}$	PD1, PD2, I_O=0.5mA			1.1	V
	$V_{OL(5)}$	MUTE, I_O=0.5mA			1.1	V
	$V_{OL(6)}$	PFE, I_O=1mA			1.1	V
Output Off Leak Current	$I_{OFF(1)}$	OH1 to OH4, $V_O=V_{SS}$			10	uA
	$I_{OFF(2)}$	OL1 to OL5, $V_O=V_{DD}$			10	uA
	$I_{OFF(3)}$	FMO, AMO, V_O=13V			10	uA
"H" Level 3-state Off Leak Current	I_{OFFH}	PD1, PD2, $V_O=V_{DD}$		0.01		nA
"L" Level 3-state Off Leak Current	I_{OFFL}	PD1, PD2, $V_O=V_{SS}$		0.01		nA
Input Capacitance	C_{IN}	X_{IN}, f=1MHz		2		pF
Output Capacitance	C_{OUT}	X_{OUT}, f=1MHz		4		pF
Supply Current	$I_{DD(1)}$	*1			15	mA
	$I_{DD(2)}$	*2			10	uA
	$I_{DD(3)}$	*3			5	uA

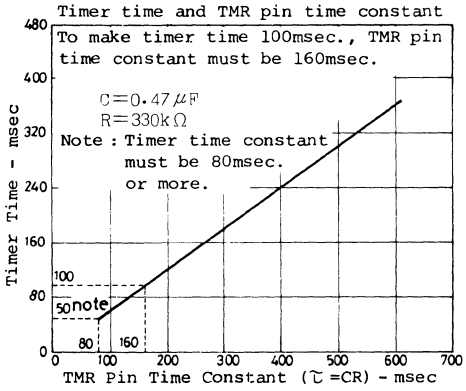
*1 : FM mode $f_{IN(1)}$=18MHz 0.7Vp-p or AM mode $f_{IN(2)}$=3MHz 0.5Vp-p, $f_{IN(3)}$= 7.2MHz, $\overline{INH}=\overline{INT}=\overline{STP1}=\overline{STP2}$=FMS=AMS=$V_{DD}$, another pin=open.

*2 : $\overline{INH}=V_{SS}$, STP1, STP2, FMS, AMS is V_{DD} or V_{SS}, $\overline{INT}=V_{DD}$, V_{DD}=6.5V.

*3 : $\overline{INH}=V_{SS}$, STP1, STP2, FMS, AMS is V_{DD} or V_{SS}, $\overline{INH}=V_{DD}$, V_{DD}=2.0V.

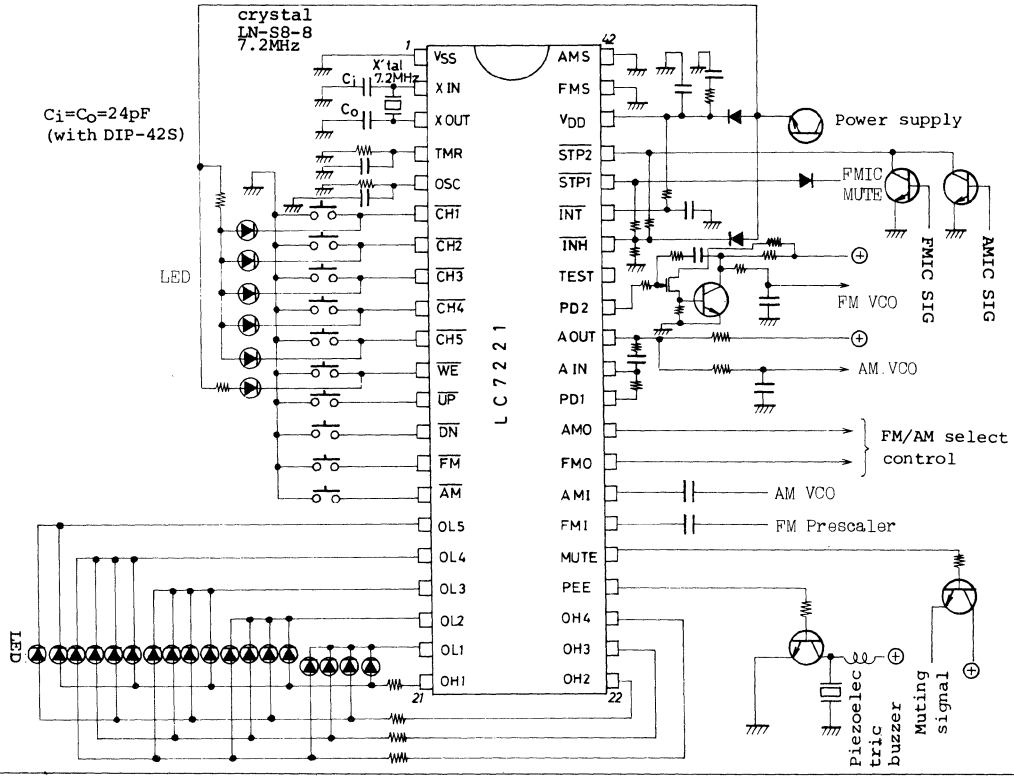




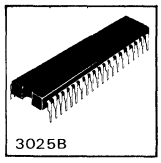


LC7220 series application circuit

(Example of LC7221 : FM IF=10.70MHz)



LC7223



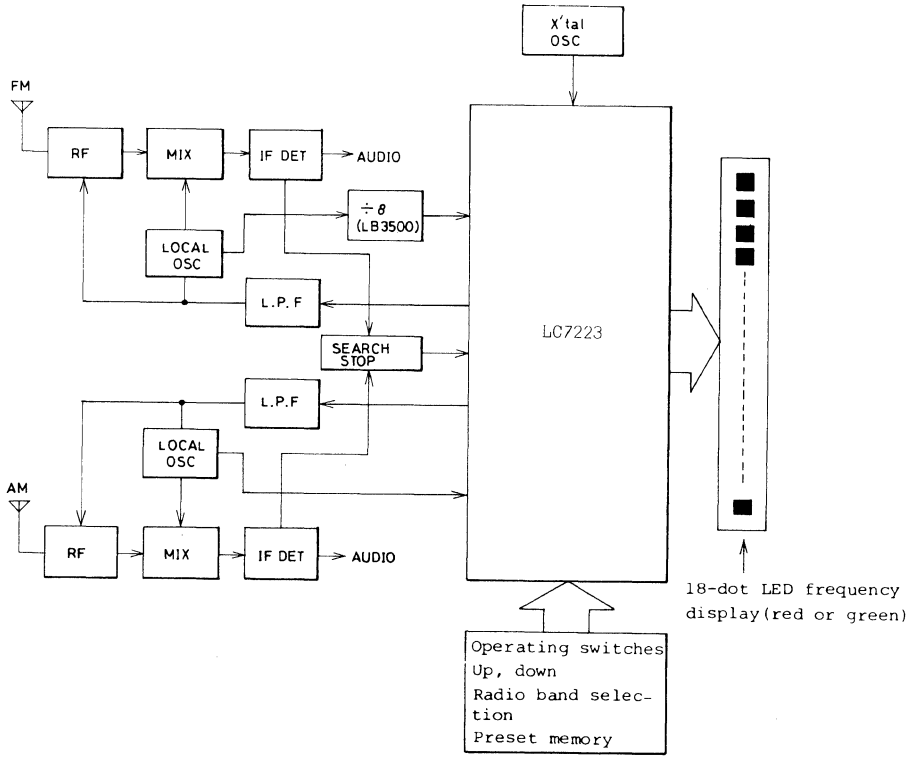
C MOS LSI

PLL Electronic Tuning System

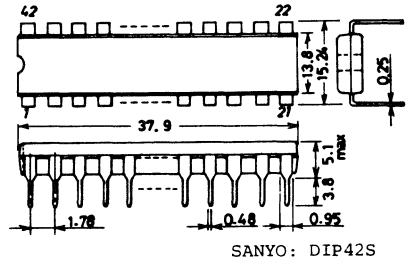
Ⓔ 1491

The LC7223 is a PLL frequency synthesizer C MOS LSI designed to be used with FM/AM 2-band radios. It is intended for domestic traffic information broadcasting (1620, 1629kHz). An electronic tuning system with 18-dot analog frequency display can be formed in conjunction with the LB3500 (1/8 prescaler).

System Block Diagram

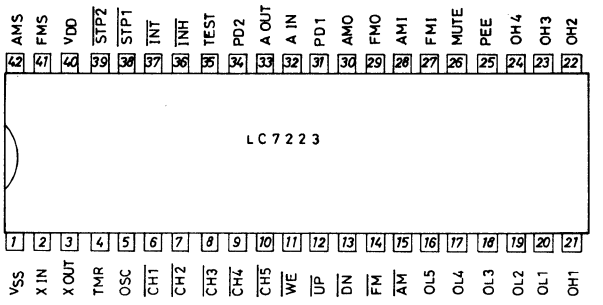


Case Outline 3025B-D42SIC
(unit:mm)



SANYO: DIP42S

Pin Assignment



The LC7220 series offers a choice of the following types according to the destination and package.

Type No.	Package	Area	Radio band	Frequency	Step	f_{ref}	IF
LC7220 LC7225	DIP42S QIP64	U.S.A.	FM	87.5 to 108.1 MHz	200 kHz	6.25 kHz	+10.70, +10.75 MHz
			AM(1)*	520 to 1610 kHz	10 kHz	10 kHz	+450 kHz
			AM(2)*	522 to 1611 kHz	9 kHz	9 kHz	+450 kHz
LC7221 LC7226	DIP42S QIP64	Japan	FM	76.0 to 90.0 MHz	100 kHz	6.25 kHz	-10.70, -10.65 Mhz
			AM	522 to 1611 kHz	9 kHz	9 kHz	+450 kHz
LC7223	DIP42S	Japan	FM	76.0 to 90.0 MHz	100 kHz	6.25 kHz	-10.70,-10.65 MHz
			AM	522 to 1629 kHz	9 kHz	9 kHz	+450 kHz
LC7222 LC7227	DIP42S QIP64	Europe (U.S.A.)	FM	87.5 t o108.1 MHz	50 kHz	6.25 kHz	+10.70, +10.75 MHz
			AM(1)*	520 to 1610 kHz	10 kHz	10 kHz	+450 kHz
			AM(2)*	522 to 1611 kHz	9 kHz	9 kHz	+450 kHz

* AM(1) or AM(2) is selected by changing the pin connection.

1. Tuning method

. Manual tuning : Channel goes up or down at a 1 step/push rate.
. Auto tuning : Channel goes up or down fast.
  Auto scan mode —— Fast scanning continues regardless of the presence or absence of station.
  Auto search mode —— Searching continues until a station is detected.
  Change-over from manual tuning to auto tuning depends upon the period of time for which the $\overline{UP}$ or $\overline{DN}$ switch is pushed.
. Preset tuning : 5 stations of FM, AM each can be preset.

2. Frequency display

. For both FM and AM, 18-dot (or 9-dot) LED (red or green) display is made.
. Lighting system is static and LED driver is built in.

3. Features

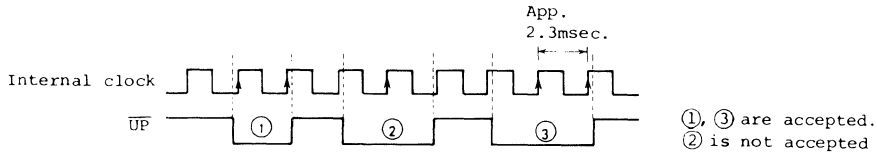
. Display, operating key, internal operation are all static.
. Phase comparator outputs are assigned to FM and AM respectively.
. Amplifier for low-pass filter is built in : N channel open drain
. Sound "peep"generating output is provided to make it possible to check the key operation auditorily.
. Muting output is provided to eliminate the noise to be generated at the time of key operation, etc.
. A quartz oscillator of 7.2MHz is used for reference frequency.
. Supply voltage V_{DD} is 4.5 to 6.5 V. (Backup voltage of 2.0V min. is usable while supply voltage is turned OFF.)

4. Description of operation

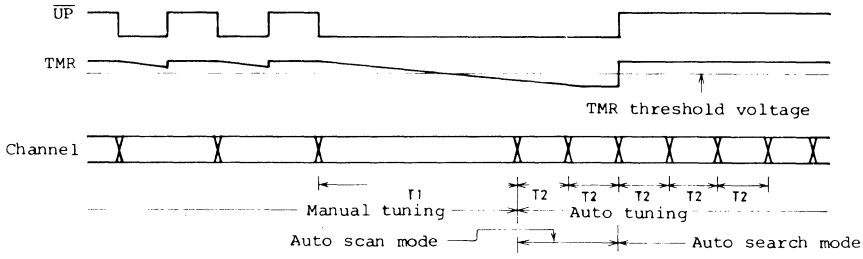
4-1 Tuning operation

(1) Up and down tuning (manual tuning, auto tuning).
  .Pushing the $\overline{UP}$ or $\overline{DN}$ switch causes channel to go up or down.
  .Considering a possible use of rotary switch to be connected to the $\overline{UP}$ and $\overline{DN}$ pins, the operation speed inside the LSI is made faster to secure the

reliable operation in response to a signal of more than approximately 4.6 msec. pulse width.



.Change-over form manual tuning to auto tuning depends upon the period of time for which the $\overline{UP}$ or $\overline{DN}$ switch is pushed. The period of time which elapses until this change-over occurs depends upon the time constant of a resistor and a capacitor connected to the TMR pin.

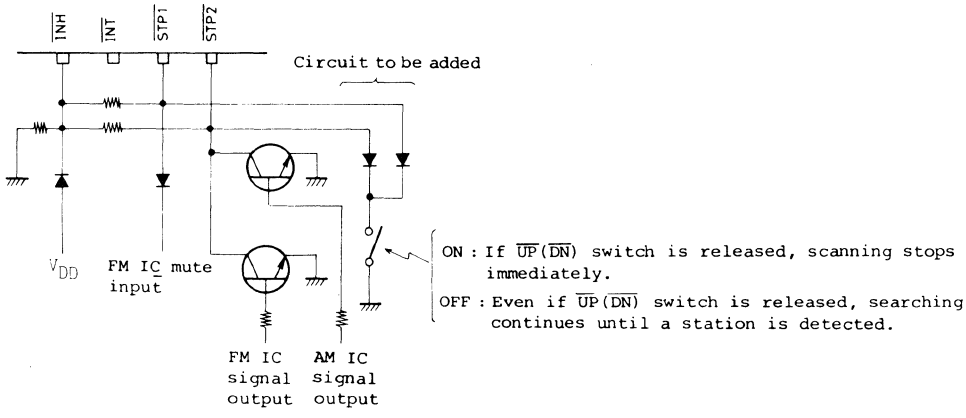


T1 : Period of time depending upon the time constant of a resistor and a capacitor connected to the TMR pin.
T2 : Period of time (2ø) depending upon the oscillation period (ø) of the OSC pin.

■ Manual tuning
Each time the $\overline{UP}$ or $\overline{DN}$ switch is pushed, channel goes up or down at a 1 step/push rate. When the upper (lower) band edge is reached, no operation occurs even if the $\overline{UP}$($\overline{DN}$) is further pushed.

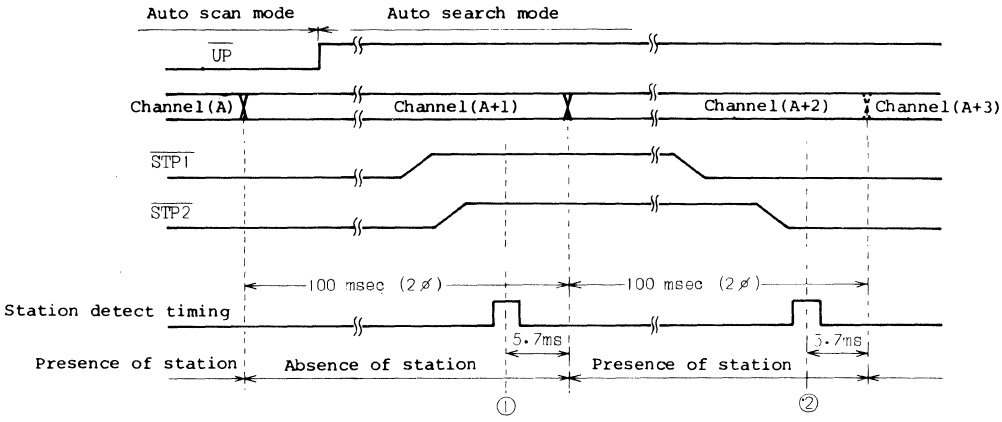
■ Auto tuning (Auto scan mode —— $\overline{UP}$ or $\overline{DN}$ switch is held pushed.)
In the auto scan mode, fast scanning continues with other key input neglected until the backup state takes place or the band edge is reached. When the band edge is reached, fast scanning stops.

.If it is desired to stop scanning immediately without causing the auto search mode to occur when the $\overline{UP}$ or $\overline{DN}$ switch is released at the auto scan mode, add the following circuit.



Auto tuning (Auto search mode —— $\overline{UP}$ and $\overline{DN}$ switches are released.)
In the auto search mode, searching stops when a station is detected. The presence or absence of station is detected approximately 5.7msec. before

the next channel change-over.



①, ② : Timing for detecting the presence or absence of station.

In order not to stop searching during the period of channel (A + 1) having no station, it is necessary that at least either $\overline{STP1}$, or $\overline{STP2}$ goes high at timing (1). In order to also stop searching during the period of channel (A + 2) having a station, both $\overline{STP1}$ and $\overline{STP2}$ go low at timing (2). For AM, however, $\overline{STP1}$ is neglected and $\overline{STP2}$ only works to stop searching. Auto searching is also stopped in the following cases.

- The $\overline{UP}$ or $\overline{DN}$ switch is pushed.
- The preset readout switch ($\overline{CH1}$ to $\overline{CH5}$) is pushed.
- Change-over of FM/AM radio band is made.
- The memory write switch ($\overline{WE}$) is pushed.
- The backup state takes place. (The low level voltage is applied to the $\overline{INH}$ pin.)

When the band edge is reached, the direction of searching is reversed.

(2) Preset tuning

5 stations of FM, AM each can be preset. When the initial supply voltage is applied, the frequency information of the lower band edge is preset in the memory with regard to FM and AM respectively.

.Readout of memory

Pushing one of the $\overline{CH1}$ to $\overline{CH5}$ switches causes the memory data of the relevant address to be read out and the LED driver for address display to be turned ON.

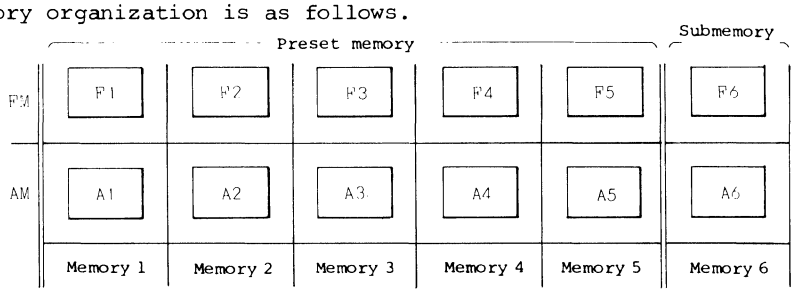
.Write of memory

Pushing the $\overline{WE}$ switch and then pushing one of the $\overline{CH1}$ to $\overline{CH5}$ switches for your desired write cause the channel being presently received to be written in the memory. Pushing the $\overline{WE}$ switch causes the LED driver to be turned ON, thereby indicating the memory writable state. The memory writable state is released in the following cases.

- One of the $\overline{CH1}$ to $\overline{CH5}$ switches is pushed to write in the memory.
- The $\overline{UP}$ or $\overline{DN}$ switch is pushed.
- Change-over of FM/AM radio band is made.
- The backup state takes place.

Even if the above key operation is not performed, the memory writable state is automatically released in 4.8 sec. (96ø).

The memory organization is as follows.



.Memory 1 to memory 5 correspond to $\overline{CH1}$ to $\overline{CH5}$ respectively. Memory 6 is a submemory to be used for memorizing the frequency at the time of manual /auto tuning. When change-over of FM/AM radio band is made, the memory data of the back side is read out in such a manner as F1↔A1, F2↔A2, F3↔A3, F4↔A4, F5↔A5, F6↔A6.

4-2 Display of received frequency

The LC7220 Series is used only for linear scale display by means of LED dot. If digital display is desired, it is necessary to read the local frequency by the use of counter IC. The available number of LEDs is 18 or 9. The number of channels per LED is shown below.

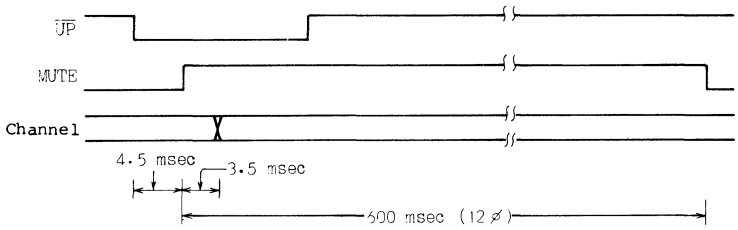
Radio band	Area	Number of channels	Number of channels/LED
FM	U.S.A.	104	6 (2)
	Japan	141	8 (5)
	European (U.S.A.)	413	24 (4)
AM	10kHz step	110	6 (8)
	9kHz step	122	7 (3)
	9kHz step	124	7 (5)

The number of channels per LED shown in ( ) of the above Table is for the 18th LED only. In order to make the number of LEDs 9, connect the OH1 pin to the OH2 pin and the OH3 pin to the OH4 pin. In this case, the number of channels per LED becomes twice the number shown in the above Table.

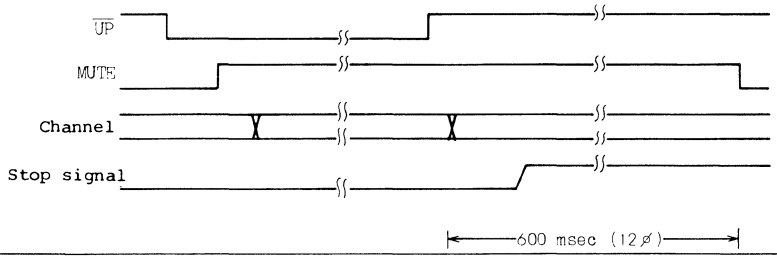
4-3 Muting output

Muting signal is outputted at the time of key operation to eliminate the noise to be generated at the time of channel change-over, etc.

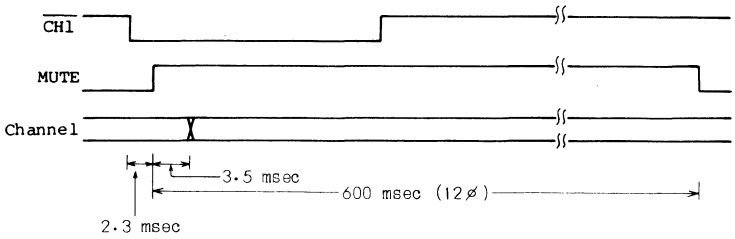
. Manual tuning ($\overline{UP}$, $\overline{DN}$)



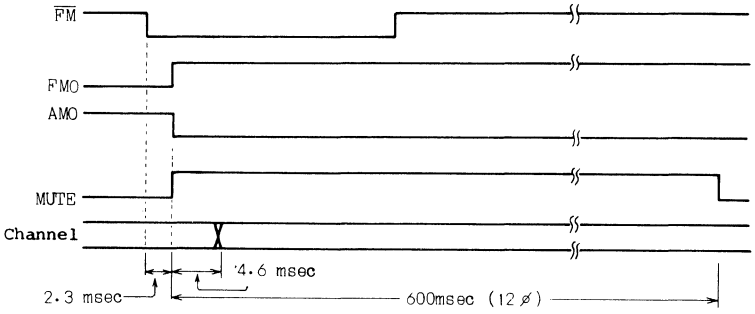
. Auto search tuning ($\overline{UP}$,$\overline{DN}$)



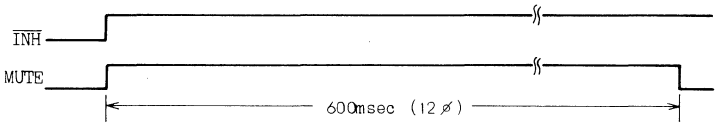
. Preset tuning ($\overline{CH1}$ to $\overline{CH5}$)



. FM/AM radio band change-over ($\overline{FM}$, $\overline{AM}$)



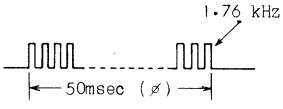
. Return from backup state ($\overline{INH}$)



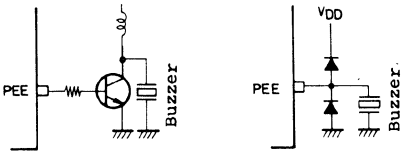
4-4 Sound "peep" output

In the following cases, sound "peep" is outputted to check the key operation.

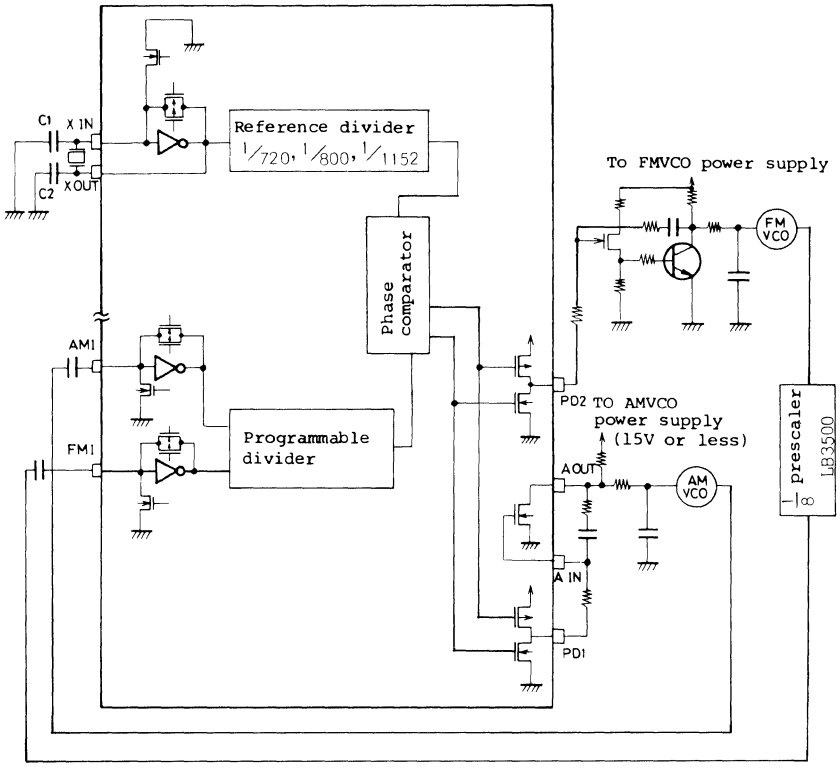
. Preset tuning is made.
. Change-over of FM/AM radio band is made.
. Manual tuning or auto tuning is being made.
. Return from the backup state is made.



In case of using a piezoelectric buzzer, it is necessary that a transistor is connected or buzzer is protected with diodes as shown below in order to prevent the LSI from being broken down by electric charge of the sound generator.



4-5 PLL Block diagram



.Since the PD1 and PD2 output the same signal, FM/AM radio band can share the low-pass filter for the purpose of reducing the cost.

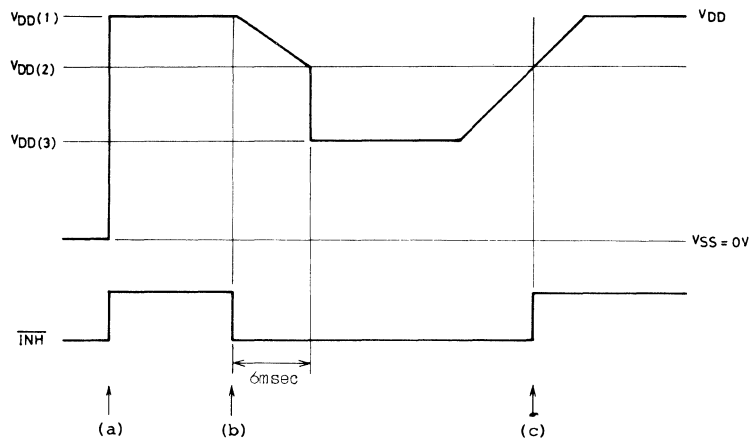
4-6 Precautions concerning power supply input and backup (Refer to the time chart on page 8.)

(a) In order to make the initial setting reliably, it is necessary to apply V_{DD}=4.5 to 6.5 V when the first power supply is inputted.

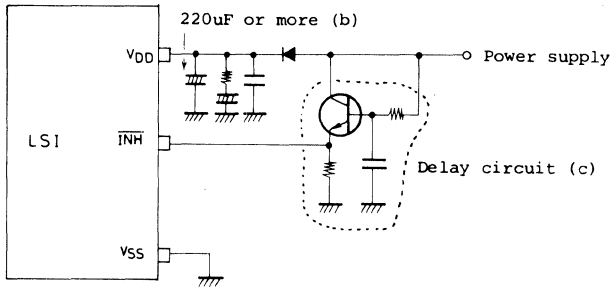
(b) If V_{DD} is made 3.5V or less (2V or more) at the backup state, it is necessary to hold V_{DD} at 3.5V or more (6.5V or less) for 6msec. or more after the $\overline{INH}$ pin is changed from "1" to "0". For this purpose, connect a capacitor of 220uF or more to the V_{DD} pin as shown in the circuit diagram on page 8.

(c) In order to release the backup state when V_{DD} is made 3.5V or less (2V or more) at the backup state, set the $\overline{INH}$ pin from "0" to "1" after V_{DD} becomes 3.5V or more (6.5V or less). For this purpose, connect a delay circuit to the $\overline{INH}$ pin as shown in the circuit on page 8.

Time chart



$V_{DD}(1)$	: Operating voltage of LSI including PLL section	4.5 to 6.5 V
$V_{DD}(2)$	: Operating voltage of other than PLL section	3.5 to 6.5 V
$V_{DD}(3)$	: Backup guaranteed voltage	2.0 to 6.5 V



4-7 Static operation

All operations of the control section including oscillation at the OSC pin are stopped at the time other than key operation. At this moment, since no frequency component lower than f_{ref} of the PLL is generated inside the LSI, no noise is generated.

4-8 Operation at backup state

In the backup state ($\overline{INH}$="0"), all key input pins other than $\overline{INT}$, $\overline{STP1}$, $\overline{STP2}$, FMS, AMS pins are set at V_{SS} level with every key operation rejected. All output pins other than XOUT pin have high impedance or are set at V_{SS} level, thereby inhibiting current from flowing out of the LSI. When returned from the backup state, the radio band and channel existed immediately before entering into the backup state take place.

4-9 Selection AM 9kHz/10kHz

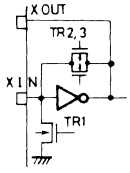
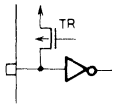
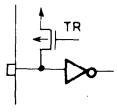
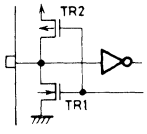
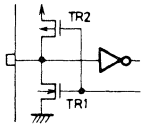
When selecting 9kHz step or 10kHz step by changing the AMS pin connection after inputting the power supply, apply the low level voltage to the $\overline{INT}$ pin for 1msec. or more after selection.

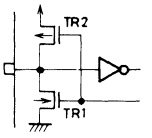
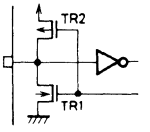
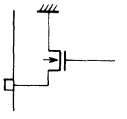
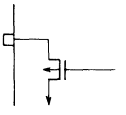
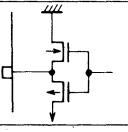
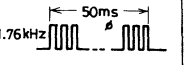
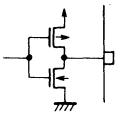
4-10 Initial setting

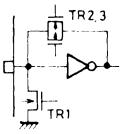
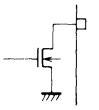
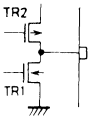
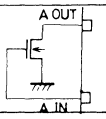
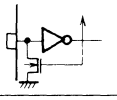
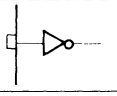
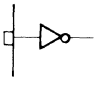
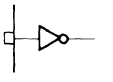
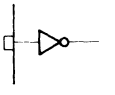
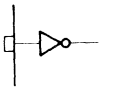
Setting the $\overline{INT}$ pin at V_{SS} level causes the initial setting inside the LSI to be made as follows.

- Preset memory ----- The frequency information of the lower band edge is preset in the memory with regard to FM and AM respectively.
- FM/AM mode -------- FM mode (FMO=1, AMO=0).
- Tuning mode ------- Up/down tuning mode.

5. Pin description

Pin name	Pin No. DIP	Pin No. QIP	Input/output type	Pin description
V_{SS}	1	57		Supply voltage apply pin —— Operation V_{DD}= 4.5 to 6.5 V, backup $V_{DD} \geqq 2V$
V_{DD}	40	53		
X_{IN}	2	58		A quartz oscillator(7.2MHz) for reference frequency is connected. In the backup state, TR1 is turned ON and TR2 and TR3 (feedback resistor) are turned OFF.
X_{OUT}	3	60		
TMR	4	62		The time constant is connected to fix the change-over time from manual tuning to auto tuning. In the backup state, TR is turned OFF.
OSC	5	1		The time constant is connected to fix each following time. If the OSC period is taken as ø (50msec.), . Sound "peep" output time —— ø(50 msec) . Scan speed —— 2ø(100msec) . Muting time —— 12ø(600msec) . Automatic release of pre-set memory writable time —— 96ø(4.8msec) In the backup state, TR is turned OFF.
$\overline{CH1}$	6	3		Address designate input pin of preset memory (Accept time 4.6msec. or more, active low level) TR1 is an LED driver and TR2 is a pull-up resistor. When the address is selected, TR1 is turned ON and TR2 is turned OFF. In the backup state, TR1 is turned ON and TR2 is turned OFF with regard to all input pins of $\overline{CH1}$ to $\overline{CH5}$.
$\overline{CH2}$	7	4		
$\overline{CH3}$	8	5		
$\overline{CH4}$	9	6		
$\overline{CH5}$	10	7		
$\overline{WE}$	11	8		Input pin for preset memory write (Accept time 1msec. or more, active low level). TR1 is an LED driver and TR2 is a pull-up resistor. Pushing the $\overline{WE}$ switch causes TR1 to be turned on and TR2 to be turned OFF, thereby leading to the preset memory writable state. Pushing one of the $\overline{CH1}$ to $\overline{CH5}$ switches at the writable state enables the preset memory write. The writable state is released in the following cases. . One of the $\overline{CH1}$ to $\overline{CH5}$ switches is pushed to write in the memory. . The $\overline{UP}$ or $\overline{DN}$ switch is pushed. . Change-over of FM/AM radio band is made. . The backup state takes place. . No operation is performed for 4.8msec.(96 ø) or more after pushing the $\overline{WE}$ switch. In the backup state, TR1 is turned ON and TR2 is turned OFF.
				Input pin for up/down tuning (Accept time 4.6msec. or more, active low level). TR1 is a pull-down resistor and TR2 is a pull-up resistor (continued on the next page)

pin name	Pin No. DIP	Pin No. QIP	Input/output type	Pin description
$\overline{UP}$	12	9		. Manual tuning:Channel goes up or down at a 1 step/push rate. . Auto tuning:Pushing the $\overline{UP}$ or $\overline{DN}$ switch longer than the period of time fixed by the time constant connected to the TMR pin causes channel to go up or down at a 100msec. (2ø)/step rate. . In the auto tuning, if the $\overline{UP}$ or $\overline{DN}$ switch is held pushed, --- scanning continues even if a station is detected(auto scan mode). released, ------ searching stops if a station is detected (auto search mode). . The search waveform is triangular.  . When the band edge is reached, . scanning and tuning stop at the band edge in the auto scanning mode and manual tuning mode. . the direciton of searching is reversed in the auto search mode. In the backup state, TR1 is turned ON and TR2 is turned OFF.
$\overline{DN}$	13	10		
$\overline{FM}$	14	11		Input pin for FM/AM radio band change-over (Accept time 2.3msec. or more, active low level). TR1 is a pull-down resistor and TR2 is a pull-up resistor. In the backup state, TR1 is turned ON and TR2 is turned OFF.
$\overline{AM}$	15	12		
OL5	16	13		Output pin for frequency display LED driver. The frequency display LED is static-driven in conjunction with OH1 to OH4. In the backup state, this pin is turned OFF.
OL4	17	15		
OL3	18	17		
OL2	19	19		
OL1	20	21		
OH1	21	23		Output pin for frequency display LED driver. The frequency display LED is static-driven in conjunction with OL1 to OL5. In the backup state, this pin is turned OFF.
OH2	22	25		
OH3	23	27		
OH4	24	29		
PEE	25	30		Output pin for key operation check sound "peep". In the backup state, this pin is bound to go low. 
MUTE	26	32		Output pin for muting signal. This pin goes high at the time of muting. The muting signal is outputted in the following cases. . The $\overline{UP}$ or $\overline{DN}$ switch is pushed. . The preset memory is read out. . Change-over of FM/AM radio band is made. . Return from the backup state is made. This pin is bound to go low.

Pin name	Pin No. DIP	Pin No. QIP	Input/output type	Pin description
FMI	27	33		Input pin for FM and AM programmable divider. For FM, the VCO frequency is divided into 1/8 and inputted. For AM, the VCO freqnency is direct inputted. The input sensitivity is FMI=0.7V_{p-p},AMI=0.5 Vp-p. For FMI, TR1 is turned ON and TR2 and TR3 (feedback resistor) are turned OFF at the time of AM radio band and backup state. For AMI, TR1 is turned ON and TR2 and TR3 (feedback resistor) are turned OFF at the time of FM radio band and backup state.
AMI	28	35		
FMO	29	36		Output pin for FM/AM radio band change-over control. FM radio band:FMO=Open,AMO=Low level AM radio band:FMO=low level,AMO=open
AMO	30	37		
PD1	31	39		Output pin for charge pump. The low-pass filter constant can be set independently for FM/AM each. In the backup state, TR1 and TR2 are turned OFF.
PD2	34	45		
AIN	32	39		Low-pass filter amplifier. Because of MOS FET, the high input impedance and short lockup time are possible.
AOUT	33	43		
TEST	35	46		Pin for LSI test. Normally, this pin is open or connected to V_{SS}.
$\overline{INH}$	36	47		Input pin for backup instruction. Applying the low level voltage causes the LSI to be in the backup state.
$\overline{INT}$	37	49		Input pin for initial state setting. Applying the low level voltage causes the LSI to be initialized.
$\overline{STP1}$	38	51		Input pin for applying stop signal at auto search mode. Auto searching stops in the following cases. FM:The low level voltage is applied to $\overline{STP1}$ and $\overline{STP2}$. AM:The low level voltage is applied to $\overline{STP2}$.
$\overline{STP2}$	39	52		
FMS	41	54		Input pin for FM IF selection. FMS="0" : IF=-10.70MHz —(Japanese spec.) IF=+10.70MHz —(U.S.A.,European specification) FMS="1" : IF=-10.65MHz —(Japanese spec.) IF=+10.75MHz —(U.S.A.,European specification)
AMS	42	55		Input pin for AM 9kHz/10kHz step selection. AMS="0" : 9kHz step AMS="1" : 10kHz step In Japan, the AMS pin must be connected to V_{SS}.

6. Main Characteristics

Maximum Ratings at T_a=25°C, V_{SS}=0V

Maximum Supply Voltage	$V_{DD}max$		-0.3 to 7.5	V
Input Voltage	V_{IN}	All input pins	-0.3 to V_{DD}+0.3	V
Output Voltage	$V_{OUT}(1)$	AMO,FMO,AOUT:output OFF	-0.3 to 15	V
	$V_{OUT}(2)$	Output pins other than $V_{OUT}(1)$.	-0.3 to V_{DD}+0.3	V
Output Current	$I_{OUT}(1)$	OH1 to OH4,OL1 to OL5, $\overline{CH1}$ to $\overline{CH5}$,$\overline{WE}$	0 to 20	mA
	$I_{OUT}(2)$	FMO,AMO,AOUT	0 to 5	mA
Allowable Power Dissipation	$P_d max$	$T_a \leq 75$°C	350	mW
Operating Temperature	T_{opg}		-30 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

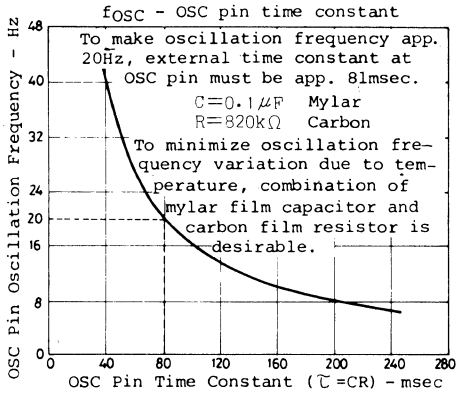
Allowable Operating Ranges at Ta=25°C			min	typ	max	unit
Supply Voltage	$V_{DD}(1)$		4.5	5.5	6.5	V
	$V_{DD}(2)$	X'tal OSC guaranteed	3.5		6.5	V
	$V_{DD}(3)$	Backup guaranteed	2.0		6.5	V
"H" Level Input Voltage	$V_{IH}(1)$	$\overline{CH1}$ to $\overline{CH5}$,$\overline{WE}$,$\overline{FM}$,$\overline{AM}$, $\overline{UP}$,$\overline{DN}$,$\overline{STP1}$ to $\overline{STP2}$, $V_{DD}(1)$,$V_{DD}(2)$	0.8V_{DD}			V
	$V_{IH}(2)$	FMS,AMS,$V_{DD}(1)$, $V_{DD}(2)$	0.95V_{DD}			V
	$V_{IH}(3)$	$\overline{INH}$,$V_{DD}(1)$,$V_{DD}(2)$	0.8V_{DD}			V
	$V_{IH}(4)$	$\overline{INH}$,V_{DD}=2.0 to 3.5V	0.85V_{DD}			V
	$V_{IH}(5)$	$\overline{INT}$,$V_{DD}(1)$,$V_{DD}(2)$	2.0		V_{DD}	V
	$V_{IH}(6)$	$\overline{INT}$,V_{DD}=2.0 to 3.5V	1.5		V_{DD}	V
"L" Level Input Voltage	$V_{IL}(1)$	$\overline{CH1}$ to $\overline{CH5}$,$\overline{WE}$,$\overline{FM}$,$\overline{AM}$,$\overline{DN}$, $\overline{STP1}$,$\overline{STP2}$,$V_{DD}(1)$,$V_{DD}(2)$			0.2V_{DD}	V
	$V_{IL}(2)$	FMS,AMS,$V_{DD}(1)$,$V_{DD}(2)$			0.05V_{DD}	V
	$V_{IL}(3)$	$\overline{INH}$,$V_{DD}(1)$,$V_{DD}(2)$			0.2V_{DD}	V
	$V_{IL}(4)$	$\overline{INH}$,V_{DD}=2.0 to 3.5V			0.15V_{DD}	V
	$V_{IL}(5)$	$\overline{INT}$,$V_{DD}(1)$,$V_{DD}(2)$	0		0.5	V
	$V_{IL}(6)$	$\overline{INT}$,V_{DD}=2.0 to 3.5V	0		0.4	V
Input Frequency	$f_{IN}(1)$	FMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $V_{IN}(1)$=0.7Vp-p	1.0		18	MHz
	$f_{IN}(2)$	AMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $V_{IN}(2)$=0.5Vp-p	0.2		3.0	MHz
Input Amplitude	$V_{IN}(1)$	FMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $f_{IN}(1)$=1.0 to 18MHz	0.7		0.9V_{DD}	Vp-p
	$V_{IN}(2)$	AMI,sinusoidal wave, capacitor coupling,$V_{DD}(1)$, $f_{IN}(2)$=0.2 to 3.0MHz	0.5		0.9V_{DD}	Vp-p
Crystal Oscillation Frequency	$f_{X'tal}$	X_{IN},X_{OUT}		7.2		MHz
OSC Oscillation Frequency	f_{OSC}	OSC,R=820kohm,C=0.1uF		20		Hz
TMR Time	T_{TMR}	TMR,R=240kohm,C=2.2uF		300		msec
$\overline{INT}$ Pin Time Constant	T_{INT}	$\overline{INT}$,rise time of V_{DD}, 200msec.	2000			msec

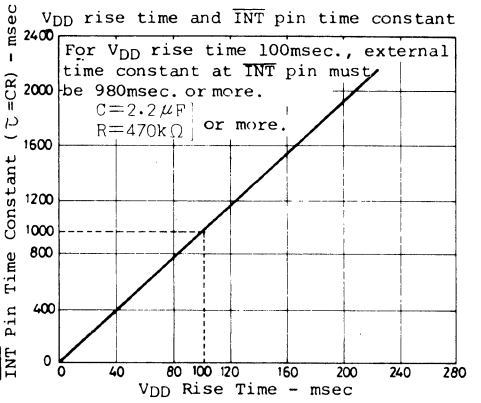
Electrical Characteristics at T_a=25°C, V_{DD}(1)			min	typ	max	unit
"H" Level Input Current	$I_{IH}(1)$	$\overline{INT}$, FMS, AMS, $V_I=V_{DD}$			2	uA
	$I_{IH}(2)$	$\overline{INH}$, $\overline{STP1}$, $\overline{STP2}$, $V_I=V_{DD}$			10	uA
	$I_{IH}(3)$	AIN, $V_I=V_{DD}$		0.01		nA
	$I_{IH}(4)$	$\overline{FM}$, $\overline{AM}$, $\overline{UP}$, $\overline{DN}$, $V_I=V_{DD}$	30		250	uA
"L" Level Input Current	$I_{IL}(1)$	$\overline{INT}$, FMS, AMS, $V_I=V_{SS}$			2	uA
	$I_{IL}(2)$	$\overline{INH}$, $\overline{STP1}$, $\overline{STP2}$, $V_I=V_{SS}$			10	uA
	$I_{IL}(3)$	AIN, $V_I=V_{SS}$		0.01		nA
	$I_{IL}(4)$	$\overline{FM}$, $\overline{AM}$, $\overline{UP}$, $\overline{DN}$, $V_I=V_{SS}$	30		250	uA
	$I_{IL}(5)$	CH1 to $\overline{CH5}$, $\overline{WE}$, $V_I=V_{SS}$	30		250	uA
"H" Level Output Voltage	$V_{OH}(1)$	OH1 to OH4, I_O=15mA	V_{DD}-0.9			V
	$V_{OH}(2)$	PD1, PD2, I_O=0.5mA	V_{DD}-1.1			V
	$V_{OH}(3)$	MUTE, I_O=2mA	V_{DD}-1.1			V
	$V_{OH}(4)$	PFE, I_O=1mA	V_{DD}-1.1			V
"L" Level Output Voltage	$V_{OL}(1)$	$\overline{CH1}$ to $\overline{CH5}$, WE, I_O=15mA			1.0	V
	$V_{OL}(2)$	OL1 to OL5, I_O=15mA			0.6	V
	$V_{OL}(3)$	FMO, AMO, I_O=2mA			1.0	V
	$V_{OL}(4)$	PD1, PD2, I_O=0.5mA			1.1	V
	$V_{OL}(5)$	MUTE, I_O=0.5mA			1.1	V
	$V_{OL}(6)$	PFE, I_O=1mA			1.1	V
Output Off Leak Current	$I_{OFF}(1)$	OH1 to OH4, $V_O=V_{SS}$			10	uA
	$I_{OFF}(2)$	OL1 to OL5, $V_O=V_{DD}$			10	uA
	$I_{OFF}(3)$	FMO, AMO, V_O=13V			10	uA
"H" Level 3-state Off Leak Current	I_{OFFH}	PD1, PD2, $V_O=V_{DD}$		0.01		nA
"L" Level 3-state Off Leak Current	I_{OFFL}	PD1, PD2, $V_O=V_{SS}$		0.01		nA
Input Capacitance	C_{IN}	X_{IN}, f=1MHz		2		pF
Output Capacitance	C_{OUT}	X_{OUT}, f=1MHz		4		pF
Supply Current	$I_{DD}(1)$	*1			15	mA
	$I_{DD}(2)$	*2			10	uA
	$I_{DD}(3)$	*3			5	uA

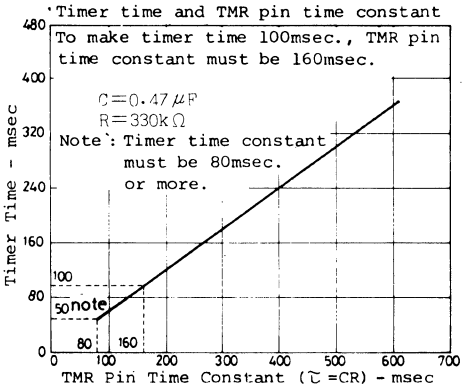
*1 : FM mode $f_{IN(1)}$=18MHz 0.7Vp-p or AM mode $f_{IN(2)}$=3MHz 0.5Vp-p, $f_{IN(3)}$= 7.2MHz, $\overline{INH}=\overline{INT}=\overline{STP1}=\overline{STP2}$=FMS=AMS=$V_{DD}$, another pin=open.

*2 : $\overline{INH}=V_{SS}$, STP1, STP2, FMS, AMS is V_{DD} or V_{SS}, $\overline{INT}=V_{DD}$, V_{DD}=6.5V.

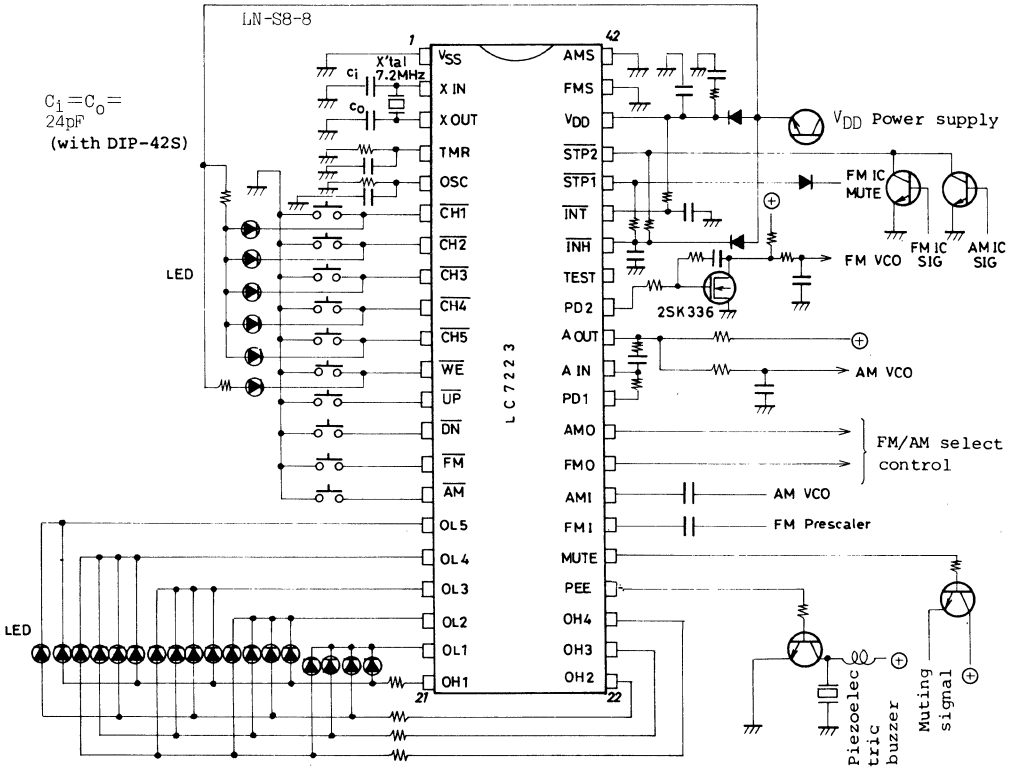
*3 : $\overline{INH}=V_{SS}$, STP1, STP2, FMS, AMS is V_{DD} or V_{SS}, $\overline{INH}=V_{DD}$, V_{DD}=2.0V.



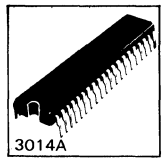




LC7223 Application Curcuit



LC7250



C MOS LSI

Digital Frequency Indicator with Clock Function (LED Use)

Ⓔ C523G

Applications

- Car radio applications: FM/AM receiving frequency display and clock display
- Home radio applications: FM/AM receiving frequency display and clock display
- Car clock applications: Hours-minutes, month-date/stopwatch display

Functions

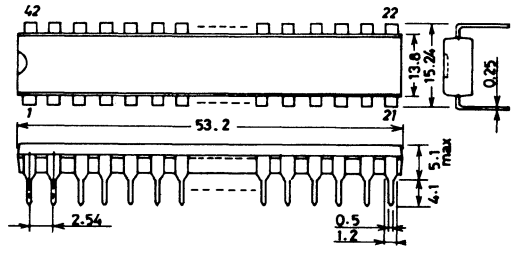
- FM receiving frequency display (4 digits)
- AM receiving frequency display (4 digits)
- Hours-minutes display
- Month-date or stopwatch display (Either of these selectable)

Features

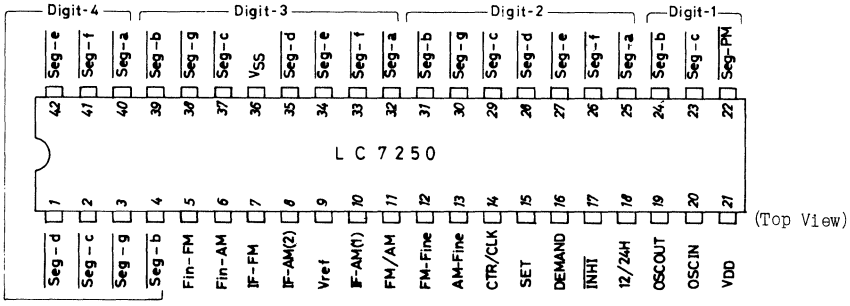
1. Single-chip C-MOS LSI for static display system
2. Capable of direct driving green LED (Drive capacity 15 mA)
3. Capable of selecting frequency display/time display
4. Uses FM/AM local oscillation signal of varactor diode, variable capacitor, or μ tuning system to digitally display FM/AM receiving frequency.
5. Covers 4 AM intermediate frequencies shown below.
   +262.5, +452.5, +455, +470kHz
6. Covers 2 FM intermediate frequencies shown below.
   +10.7, −10.7MHz
7. Capable of fine-adjusting AM/FM display frequency error independently
   - A variable resistor can be used to correct AM IF error within ±2.8kHz.
   - A variable resistor can be used to correct FM IF error within ±140kHz.
8. Two selections of display system (12-hour system with PM sign which is displayed during setting only, 24-hour system)
9. Programmed on long months (months having 31 days)/short months (months having 30 days). (Date in February is programmed to count up to the 29th.)
10. Easy to set time by the time signal.
11. Stopwatch capable of counting/displaying 1 second to 12 hours 59 minutes 59 seconds
12. Inhibit pin for inhibiting time setting with display unlighted
13. 4MHz crystal for reference frequency

★ For FLT display (5 digits) and frequency display only (without clock display), use the LC7253 and LC7259 (LED use), LC7258 (FLT use) respectively.

Case Outline 3014A-D42IC
(unit: mm)



Pin Assignment



Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0V			min	typ	max	unit
Maximum Supply Voltage	V_{DD} max		−0.3		11	V
	V_{DD} max	Cumulative applied time: 30 min. or less	−0.3		14	V
Reference Voltage	V_{ref}	$V_{ref} \leqq V_{DD}$	−0.3		10	V
	V_{ref}	$V_{ref} \geqq V_{DD}$, Cumulative applied time: 30 min. or less	−0.3		13	V
Input Voltage	V_I		−0.3		V_{DD}+0.3	V
Output Voltage	V_O	Output OFF	−0.3		V_{DD}+0.3	V
Allowable Power Dissipation	P_d max	$T_a \leqq$ +75°C			0.8	W
Allowable Power Dissipation of Segment Output	P_d (Seg) max	Other than $\overline{PM}$: I_{OL} < 25 mA			15	mW
		$\overline{PM}$: I_{OL} < 75 mA			45	mW
Operating Temperature	T_{opg}		−30		+75	°C
Storage Temperature	T_{stg}		−40		+125	°C

Allowable Operating Ranges/T_a = 25°C, V_{DD} = 8.0 to 10.3V, V_{SS} = 0V, V_{ref} = 7.9 to 9.0V $\leqq V_{DD}$, V_{ref} = 0V if V_{DD} < 8.0V

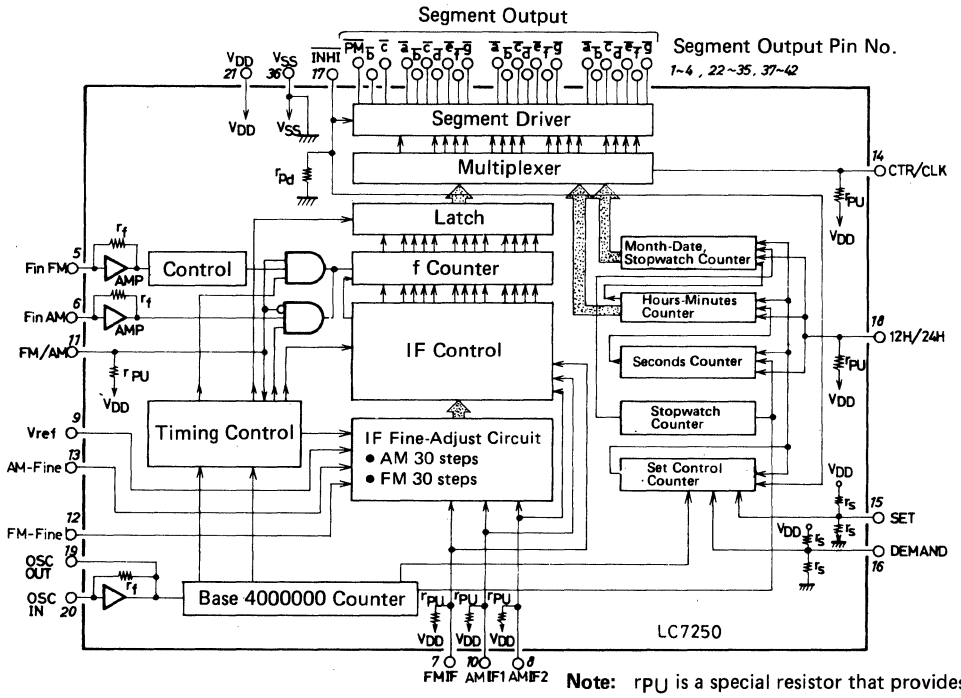
			min	typ	max	unit
Supply Voltage	$V_{DD}1$	All functions operating mode	8.0	9.3	10.8	V
	$V_{DD}2$	Only clock operating mode	4.3	5.0	8.0	V
Refrence Voltage	V_{ref}	$V_{ref} \leqq V_{DD}$	7.9	8.0	9.0	V
Input "H" Level Voltage	V_{IH1}	INHI, V_{DD} = 4.3 to 10.3V	0.75V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL1}	INHI, V_{DD} = 4.3 to 10.3V	V_{SS}		0.1V_{DD}	V
Input "H" Level Voltage	V_{IH2}	FM/AM, IF-FM, IF-AM$_1$, IF-AM$_2$, 12H/24H	0.85V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL2}	FM/AM, IF-FM, IF-AM$_1$, IF-AM$_2$, 12H/24H	V_{SS}		0.15V_{DD}	V
Input "H" Level Voltage	V_{IH3}	SET, DEMAND, CTR/CLK	0.88V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL3}	SET, DEMAND, CTR/CLK	V_{SS}		0.12V_{DD}	V
Input "M" Level Voltage	V_{IM}	SET, DEMAND, CTR/CLK	0.36V_{DD}		0.64V_{DD}	V
Input Frequency	f_{IN1}	Fin-FM, V_{P-P} = 0.7V, duty 50%	0.6		2.0	MHz
	f_{IN2}	Fin-AM, V_{P-P} = 0.7V, duty 50%	0.4		2.5	MHz
Operating Frequency	f_{opg}	Crystal is externally connected across OSC-IN and OSC-OUT.	3.5		4.2	MHz
Input Amplitude	V_{P-P}	Fin-FM, Fin-AM, Ceramic capacitor of 0.4 μF is connected across V_{DD} and V_{SS}.	0.7			V_{P-P}

Electrical Characteristics/T_a = 25°C, V_{DD} = 8.0 to 10.3V, V_{SS} = 0V, V_{ref} = 7.9 to 9.0V, $V_{ref} \leqq V_{DD}$

			min	typ	max	unit
Input Current	I_{IN}	FM-Fine, AM-Fine, V_{IN} = 0V or V_{ref}	−1		1	μA
Input "H" Level Current	I_{IH1}	IF-FM, IF-AM_1, IF-AM_2, CTR/CLK, 12H/24H, V_{IN} = 0.9V_{DD}	−80	−30	−10	μA
Input "L" Level Current	I_{IL1}	IF-FM, IF-AM1, IF-AM_2, CTR/CLK, 12H/24H, V_{IN} = 0V	−3		0	μA
Input "H" Level Current	I_{IH2}	FM/AM, V_{IN} = 0.9V_{DD}	−40	−15	−5	μA
Input "L" Level Current	I_{IL2}	FM/AM, V_{IN} = 0V	−3		0	μA
Middle Point Setting Resistance	r_s	SET, DEMAND	40	70	100	kΩ
Input Floating Voltage	V_{IF3}	SET, DEMAND, input floating	0.45V_{DD}		0.55V_{DD}	V
Input "H" Level Current	I_{IH4}	$\overline{INHI}$, V_{DD} = 4.3 to 10.3V, V_{IN} = V_{DD}	15		400	μA
Input Floating Voltage	V_{IF4}	$\overline{INHI}$, V_{DD} = 4.3 to 10.3V, input floating	0		0.3	V
Feedback Resistance	Rf_1	Feedback resistance across OSC-IN and OSC-OUT		3		MΩ
	Rf_2	Feedback resistance of Fin-FM		3		MΩ
	Rf_3	Feedback resistance of Fin-AM		3		MΩ
Output "L" Level Voltage	V_{OL1}	$\overline{PM}$, V_{DD} = 8.0V, I_{OL} = 45 mA			0.7	V
Output "L" Level Voltage	V_{OL2}	Segment outputs other than $\overline{PM}$, V_{DD} = 8.0V, I_{OL} = 15 mA			0.7	V
Output Leak Current	I_{OFF}	All segment outputs, V_{DD} = 10.3V V_{OH} = 10.3V			10	μA
Current Dissipation	I_{DD1}	V_{DD} = 10.3V, f_{opg} = 4 MHz (with crystal mounted), f_{IN2} = 2.5 MHz (0.7V_{P-P})		8	17	mA
	I_{DD2}	V_{DD} = 5.5V, f_{opg} = 4 MHz (with crystal mounted), V_{ref} = 0V, $\overline{INHI}$ = 0V		1	2.5	mA
	I_{ref}	V_{DD} = 10.3V, V_{ref} = 9V, AM-Fine = FM-Fine = V_{ref}		0.5	1.5	mA

(Note) + sign: Flowing into LSI
− sign: Flowing out of LSI

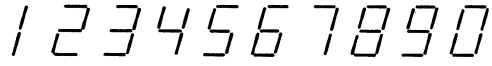
Equivalant Circuit Block Diagram



Note: r_{PU} is a special resistor that provides the specification value at "H" level and a high value at "L" level.

1. Display

1-1. Configuration and display font
3-1/2-digit, 7-segment LED's are used to display time and frequency in the display font shown below.

Font 

1.2 Display system
Static display

1-3. Display range

- Frequency (AM): 000kHz to 1999kHz (The highest-order digit "0" is blanked out.)
- Frequency (FM): 00.0MHz to 199.9MHz (The highest-order digit "0" is blanked out.)
- Clock (12-hour display system): 1:00 to PM12:59 (The highest-order digit "0" is blanked out.)
- Clock (24-hour display system): 0:00 to 23:59 (The highest-order digit "0" is blanked out.)
- Stopwatch (minutes-seconds): 0 minute 00 second to 9 minutes 59 seconds (The highest-order digit is blanked out.)
- Stopwatch (hours-minutes): 0 hour 00 minute to 12 hours 59 minutes (The highest-order digit "0" is blanked out.)

2. Input/Output Signal

2-1. Switch signal
- Logic "H": V_{DD}
- Logic "M": $1/2V_{DD}$ (Intermediate level between V_{DD} and V_{SS})
- Logic "L": V_{SS}

2-2. FM/AM frequency input
- Amplitude: 0.7V or greater
- Frequency: FM: 2.0MHz or less (FM local oscillation frequency is 1/100-divided and inputted.)
  AM: 2.5MHz or less

2-3. Reference frequency: Crystal of 4.000000MHz

2-4. Segment output: N channel open drain

3. Functional Description (Refer to Sample Application Circuit on page 14.)

3-1. Selection of month-date/stopwatch
Since the month-date counter is also used as the stopwatch counter inside the LSI, either month-date function or stopwatch function can be selected. For the description given below, refer to Sample Application Circuit. In Sample Application Circuit, providing only the CLK switch makes a clock with the month-date function; providing only the STW switch makes a clock with the stopwatch function. (If both switches are coupled, both functions are available.)

3.2 Selection of frequency display/clock display. ( ) is for using stopwatch function.
The CLK switch (or STW switch) is used to select the frequency display/clock display.
- Frequency display: Turn OFF the CLK switch (and STW switch).
- Clock display: Turn ON the CLK switch (or STW switch).

3-3. Operation for frequency display
(1) Selection of FM/AM display
- AM display: Turn ON the FM/AM switch.
- FM display: Turn OFF the FM/AM switch.

(2) Selection of IF
- FM IF +10.7MHz: Set the FM-IF pin to V_{DD}.
  FM IF −10.7MHz: Set the FM-IF pin to V_{SS}.
- AM IF +262.5kHz: Set the AM-IF (1) pin to V_{DD} and AM-IF (2) pin to V_{DD}.
  AM IF +452.5kHz: Set the AM-IF (1) pin to V_{SS} and AM-IF (2) pin to V_{DD}.
- AM IF +455.0kHz: Set the AM-IF (1) pin to V_{SS} and AM-IF (2) pin to V_{SS}.
- AM IF +470.0kHz: Set the AM-IF (1) pin to V_{DD} and AM-IF (2) pin to V_{SS}.

(3) Fine adjustment of frequency display
a. To correct an FM frequency display, follow the procedure shown below.
(i) Set the display mode to the FM display.
(ii) Input the reference FM frequency to the Fin-FM.
(iii) Change the applied voltage at the FM/AM pin from V_{DD} to $1/2V_{DD}$.
(iv) Adjust the FM-VR so that the display coincides with the reference FM frequency. The point at which flashing stops is the optimum.
(v) Change the applied voltage at the FM/AM pin from $1/2V_{DD}$ to V_{DD}.
(vi) This completes adjustment.

Example: Correcting the display to 80.0MHz. IF = −10.7MHz
(i) Set the FM/AM pin to V_{DD}.
(ii) Receive 80.0MHz and input the 1/100-divided local oscillation frequency to the Fin-FM pin.
(iii) Change the applied voltage at the FM/AM pin from V_{DD} to $1/2V_{DD}$.
(iv) Adjust the FM-VR so that the display coincides with 80.0MHz. The point at which flashing stops is the optimum.
(v) Change the applied voltage at the FM/AM pin from $1/2V_{DD}$ to V_{DD}.
(vi) This completes adjustment.

b. To correct an AM frequency display, follow the procedure shown below.
   (i) Set the display mode to the AM display.
   (ii) Input the reference AM frequency to the Fin-AM.
   (iii) Change the applied voltage at the FM/AM pin from V_{SS} to $1/2V_{DD}$.
   (iv) Adjust the AM-VR so that the display coincides with the reference AM frequency. The point at which flashing stops is the optimum.
   (v) Change the applied voltage at the FM/AM pin from $1/2V_{DD}$ to V_{SS}.
   (vi) This completes adjustment.

   Example: Correcting the display to 950kHz. IF = 455kHz

   (i) Set the FM/AM pin to V_{SS}.
   (ii) Receive 950kHz and input the local oscillation frequency to the Fin-AM pin.
   (iii) Change the applied voltage at the FM/AM pin from V_{SS} to $1/2V_{DD}$.
   (iv) Adjust the AM-VR so that the display coincides with 950kHz. The point at which flashing stops is the optimum.
   (v) Change the applied voltage at the FM/AM pin from $1/2V_{DD}$ to V_{SS}.
   (vi) This completes adjustment.

3-4. Operations related to clock
- Push the CLK switch (or STW switch).

(1) Hours-minutes display mode
- The hours-minutes display mode is entered with the hours-minutes setting switch and month-date/STW switch released.

(2) Hours-minutes setting mode and mode of setting by the time signal
- Push the hours-minutes setting switch, and the hours-minutes setting mode is entered and the display flashes at a 2Hz rate.
- Setting of hours is executed at a 2Hz rate 1.2 seconds after pushing the UPPER switch. No carry from hours to date occurs. When setting of hours is completed, the display stops flashing.
- Setting of minutes is executed at a 2Hz rate 1.2 seconds after pushing the LOWER switch. No carry from minutes to hours occurs. When setting of minutes is completed, the display stops flashing.
- Setting by the time signal is executed by pushing/releasing the LOWER switch within 1 second when the display is flashing. Setting by the time signal means that the moment minutes and seconds are cleared to 0 minute and 0 second respectively hours are incremented by 1 when the minutes display is at 30 to 59. Setting by the time signal can be executed only when the hours-minutes display is flashing.

(3) Month-date display and month-date setting mode/long month (31 days, short month (30 days) programmed (counting date in February up to the 29th). Provide the CLK switch. With the CLK switch pushed, the month-date display mode is entered and setting of month-date is executed as follows:
- Push the month-date/STW switch and release the hours setting switch, and the month-date display mode is entered.
- Setting of month is executed at a 2Hz rate 1.2 seconds after pushing the UPPER switch.
- Setting of date is executed at a 2Hz rate 1.2 seconds after pushing the LOWER switch. No carry from date to month occurs.

(4) Stopwatch mode
Provide the STW switch. With the STW switch pushed, the stopwatch operation is performed as follows:
- Push the month-date/STW switch. Release the hours setting switch.
- Push/release the UPPER switch, and the stopwatch starts counting. Push/release the UPPER switch again, and the stopwatch stops counting.
- Selecting the hours-minutes display mode/minutes-seconds display mode of stopwatch and clearing the counter.
  Push/release the LOWER switch within 1 second, and the hours-minutes display mode is entered. Push/release the LOWER switch again within 1 second, and the minutes-seconds display mode is entered. When in the minutes-seconds display mode, the PM sign flashes at a 1Hz rate.
- Hold the LOWER switch pushed for 1.2 seconds or more, and the display becomes 0:00 and the counter is cleared. When cleared, the minutes-seconds display mode is entered and the PM sign flashes. (The $\overline{PM}$ pin is turned ON/OFF.)

4. Selection of function

Selection of each function described above is summarized as follows:

- Functions related to frequency and clock

Function	Display Mode	CLK SW	STW SW	FM/AM SW
Frequency Operation	FM display	off	off	off
	AM display	off	off	on
Clock Operation	Hours-minutes or month-date display	on	◎	◎
	Hours-minutes or stop-watch display	off	on	◎

◎ : Either on or off

- Functions related to hours-minutes (Provide the CLK or STW SW.)

	Hours-minutes setting SW	Month-date/ STW SW	UPPER SW	LOWER SW
Hours-Minutes Display	off	off	◎	◎
Execution of Hours Setting	on	◎	on	off
Execution of Minutes Setting	on	◎	off	on
Execution of Setting by the Time Signal	on	◎	off	on < 1 second

◎ : Either on or off

- Functions related to month-date (Provide the CLK SW.)

	Hours-minutes setting SW	Month-date/ STW SW	UPPER SW	LOWER SW
Month-Date Display	off	on	off	off
Execution of Month Setting	off	on	on	off
Execution of Date Setting	off	on	off	on

- Functions related to stopwatch (Provide the STW SW.)

Function	UPPWER SW	LOWER SW
Stopwatch Counter, Reset	off	on > 1.2 sec.
Minutes-Seconds Display → Hours-Minutes Display or Hours-Minutes Display → Minutes-Seconds Display	off	on < 1 sec.
Start → Stop or Stop → Start	on	off

5. Pin Description

5-1. CTR/CLK (counter/clock) input
- Input pin for selecting frequency display, clock, stopwatch
  - "L" level: Hours-minutes and month-date display
  - "M" level: Hours-minutes and stopwatch display
  - "H" level: Frequency counter display

5-2. FM/AM (FM/AM select) input
- Input pin for setting the frequency counter and frequency control to FM or AM use
  - "L" level: AM display
  - "H" level: FM display

5-3. FM-IF (FM IF setting) input
- Input pin for specifying FM IF
  - IF: −10.7MHz, +10.7MHz
  - "L" level: −10.7MHz
  - "H" level: +10.7MHz

5-4. AM-IF (1), AM-IF (2) (AM IF setting) input
- IF: 262.5kHz, 452.5kHz, 470kHz, 455kHz

AM-IF (1)	AM-IF (2)	IF
⌈L⌋	⌈L⌋	+455.0 kHz
⌈H⌋	⌈L⌋	+470.0 kHz
⌈L⌋	⌈H⌋	+452.5 kHz
⌈H⌋	⌈H⌋	+262.5 kHz

5-5. FM-Fine (IF fine adjust) input
- Input pin for fine-correcting FM IF error
- Pin for inputting the voltage divided by a variable resistor connected across V_{ref} and V_{SS}

5-6. AM-Fine (IF fine adjust) input
- Input pin for fine-correcting AM IF error
- Pin for inputting the voltage divided by a variable resistor connected across V_{ref} and V_{SS}
- Fine adjust range of FM-Fine, AM-Fine
  FM-Fine: 28-step adjustable in 10kHz/step between 10.60MHz to 10.80MHz (±140kHz)
  AM-Fine: 28-step adjustable in 0.2kHz/step with IF as the center (±2.8kHz)

5-7. Fin-FM (frequency) input
- Input pin for applying FM local OSC frequency (1/100 prescaler is connected externally.)
- Pin for inputting frequency of input voltage of $0.7V_{p\text{-}p}$ or greater
- Maximum frequency: 2MHz (duty 50%)
- 1/100 prescaler is connected externally.

5-8. Fin-AM (frequency) input
- Input pin for applying MW local OSC frequency
- Pin for inputting frequency of input voltage of 0.7Vp-p or greater
- Maximum frequency: 2.5MHz (duty 50%)

5-9. OSC IN, OSC OUT (crystal oscillation)
- Input/output pin for crystal oscillation
- Input/output pin for connecting a crystal (4.000000MHz)

5-10. DEMAND (time read) input
- Input pin for selecting hours-minutes read/setting, month-date read/setting, stopwatch mode

CTR/CLK	DEMAND	Mode
⌐M⌋ or ⌐L⌋	⌐H⌋	Mode of setting by the time signal and hours-minutes setting mode
⌐M⌋ or ⌐L⌋	⌐M⌋	Time display mode
⌐L⌋	⌐L⌋	Month-date display mode and month-date setting mode
⌐M⌋	⌐L⌋	Stopwatch mode

[Note]
- The following shows how to change the month-date setting mode to the stopwatch mode or vice versa.
- Changing the month-date setting mode to the stopwatch mode
  CTR/CLK = "M", DEMAND = "L", SET = "L" (1.2 seconds or more)
- Changing the stopwatch mode to the month-date setting mode
  CTR/CLK = "L", DEMAND = "L", SET = "L" or "H" (1.2 seconds or more)
- When in the mode of setting by the time signal, all digits displayed flash (2Hz).

5-11. SET (time setting) input
- Input pin for setting hours, minutes, month, date and starting/stopping/clearing stopwatch (corresponding type)
  This input pin is set at "M" level normally. The input signal of "H"/"L" level acts in 6 ways as shown below.
- When in the mode of setting by the time signal and hours-minutes setting mode (CTR/CLK = "L" or "M")
  "H" level: Execution of hours setting
  Advance at a 2Hz rate 1.2 seconds after the pin is set to "H" level.
  "L" level: Execution of setting by the time signal and minutes setting
  Advance at a 2Hz rate 1.2 seconds after the pin is set to "L" level.
  Setting by the time signal is executed when the pin is set to "M" level within 1.0 second after set to "L" level.

[Note]
- No carry to high-order digit occurs.

- When in the month-date setting mode (CTR/CLK = "L")
  "H" level: Execution of month setting
  Advances at a 2Hz rate 1.2 seconds after the pin is set to "H" level.
  "L" level: Execution of date setting
  Advances at a 2Hz rate 1.2 seconds after the pin is set to "L" level. No carry to the month digit occurs.
- When in the stopwatch mode (CTR/CLK = "M")
  "L" level: Minutes-seconds display, hours-minutes display and clear
  The counter is cleared 1.2 seconds after the pin is set to "L" level. (Display 0:00 second)
  The minutes-seconds display mode/hours-minutes display mode are alternated when the pin is set to "M" level within 1.0 second after set to "L" level. The PM output pin turned ON/OFF at a 1Hz rate to indicate the minutes-seconds display mode.
  "H" level: Start and stop
  Start/stop are alternated by setting the pin to "L"/"M" level alternately. When cleared, the counter stops and the minutes-seconds display mode is entered and the PM pin is turned ON/OFF at a 1Hz rate.

5-12. $\overline{\text{INHI}}$ (inhibit) input pin

Input pin for turning OFF the segment pins, inhibiting the SET/DEMAND pin from functioning, and preventing the Fin-AM/Fin-FM amp from operating. In car applications, this pin is useful to minimize current dissipation when the engine is stopped.

"H" level: Normal operation

"L" level: Segment pin OFF, SET/DEMAND pin function inhibit

The reason why the SET/DEMAND pin is inhibited from functioning when at "L" level is to prevent time from being set mistakenly when the display is blanked out; and the reason why the amp is stopped from operating is to minimize current dissipated in the amp.

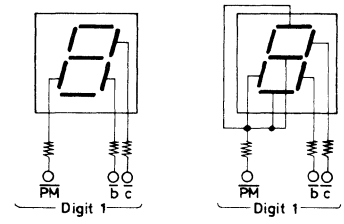
5-13. 12H/24H (hour display system select) input pin

Input pin for selecting 12-hour system with PM sign/24-hour system

"H" level: 12-hour system with PM sign

"L" level: 24-hour system

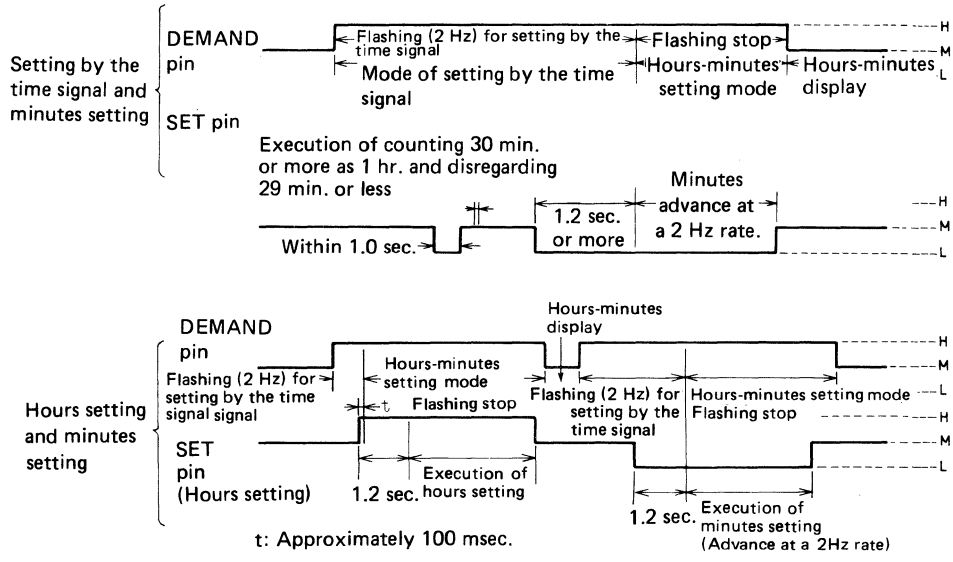
Make connection as shown right.



12-hour system 24-hour system

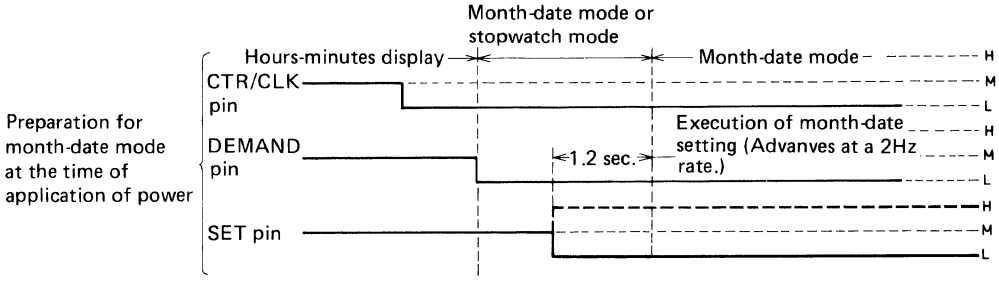
6. Timing Chart

6-1. Timing chart for time setting (CRT/CLK = "L" or "H")

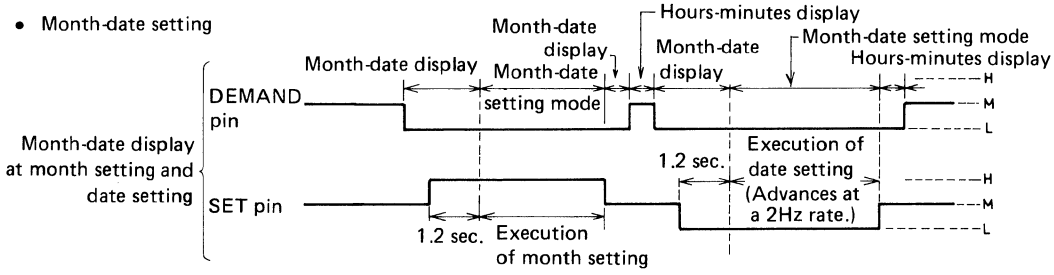


6.2 Timing chart for month-date setting

- It is unknown whether the month-date mode or stopwatch mode is entered at the time of application of power. Therefore, the month-date mode must be entered as follows:

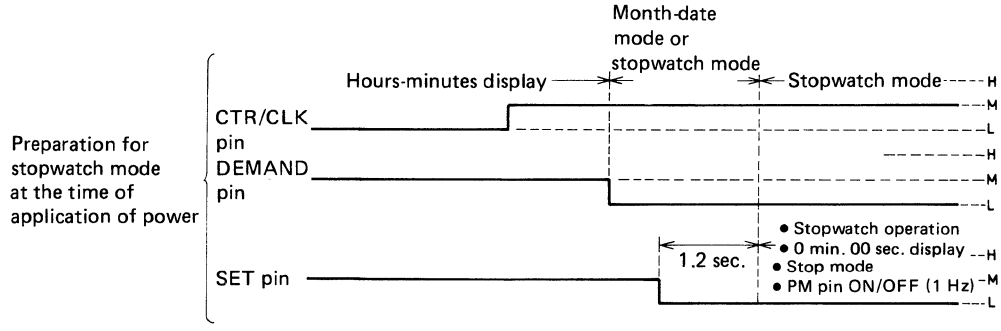


- Month-date setting

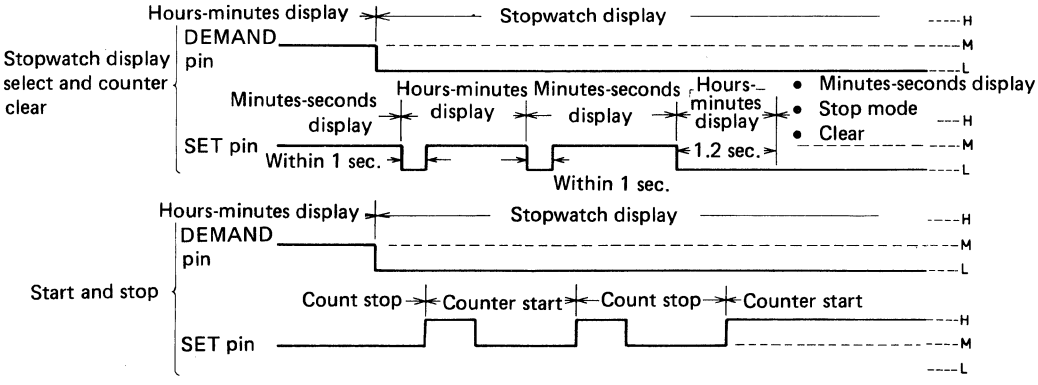


6-3. Timing chart for stopwatch mode

- It is unknown whether the month-date mode or stopwatch mode is entered at the time of application of power. Therefore, the stopwatch mode must be entered as follows:

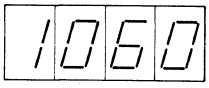


- Timing chart for stopwatch operation

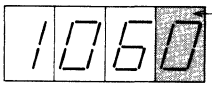


7. Sample Display at Each Mode

1. FM display: Display at 106MHz reception



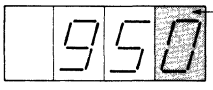
Change the applied voltage at the FM/AM pin from V_{DD} to $1/2V_{DD}$. (Correct the display error of a ceramic filter used in a set.)



Flashing at a 2Hz rate if the display error is not corrected. Adjust the FM-VR to stop flashing.

2. AM display: Display at 950kHz reception

Change the applied voltage at the FM/AM pin from V_{SS} to $1/2V_{DD}$.

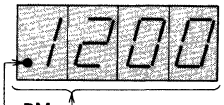


Flashing at a 2Hz rate if the display error is not corrected. Adjust the AM-VR to stop flashing.

3. Setting by the time signal: Setting to PM12:00 by the time signal

Flashing at a 2Hz rate when in the mode of setting by the time signal

Execute setting by the time signal with the SET pin.

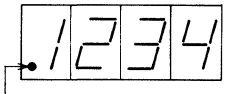


PM sign

Flashing at a 2Hz rate when in the mode of setting by the time signal

When setting by the time signal is executed, minutes become 00. If the minutes display is at 30 to 59, hours are incremented by 1 (counting 30 or more as 1hr. and disregarding 29 or less).

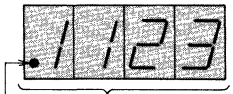
4. Hours-minutes display: Display of PM12:34



PM sign

The PM sign flashes in the afternoon when in the mode of setting by the time signal, hours-minutes display, hours-minutes setting.

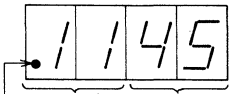
5. Hours-minutes setting: Setting to 11:45 from PM11:23



PM sign

Flashing at a 2Hz

Change the applied voltage at the SET pin from V_{DD} to $1/2V_{DD}$. After lapse of 1.2 sec., flashing stops and hours or minutes advance at a 2Hz rate.

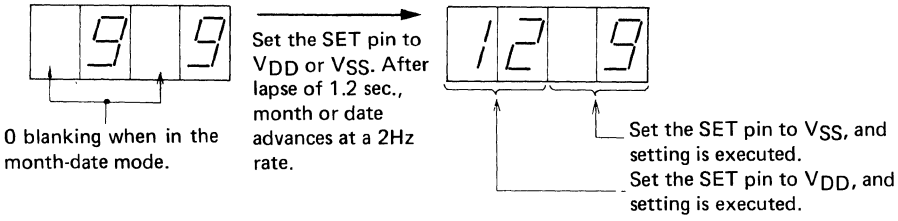


PM sign

Set the SET pin to V_{SS}, and setting is executed.

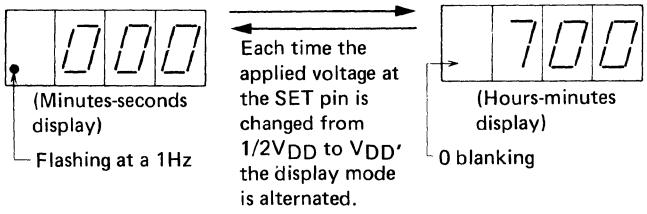
Set the SET pin to V_{DD}, and setting is executed.

6. Month-date display and setting: Setting to December 9 from September 9

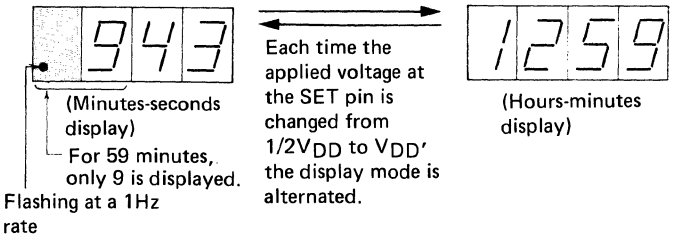


7. Stopwatch display

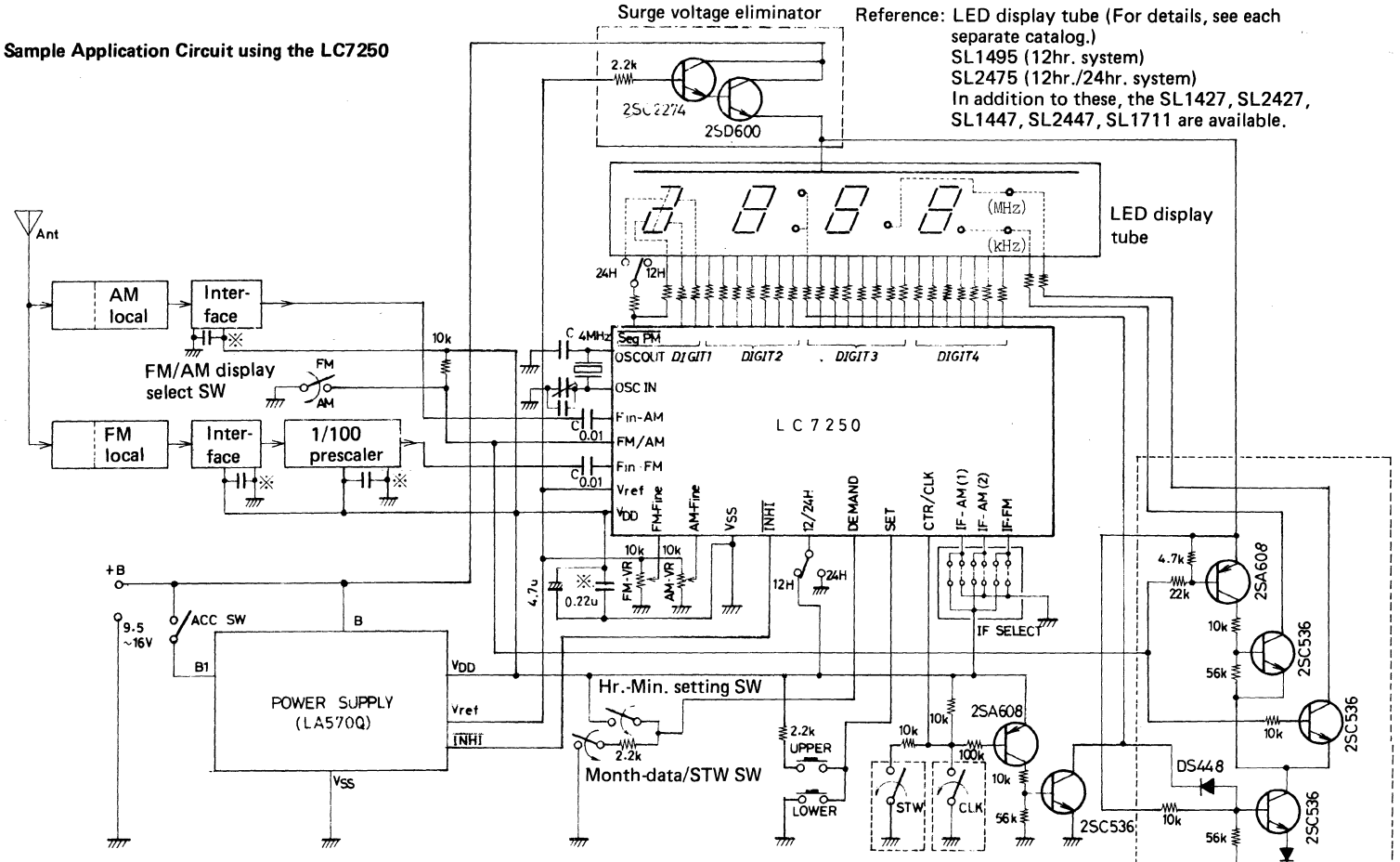
- 7 hours 00 minute 00 second



- 12 hours 59 minutes 43 seconds



8. Sample Application Circuit using the LC7250



*: Ceramic capacitor. Must be mounted as close to each pin as possible.

- For clock with month-date function, remove the STW SW and provide the CLK SW only.
- For clock with stopwatch, remove the CLK SW and provide the STW SW only.

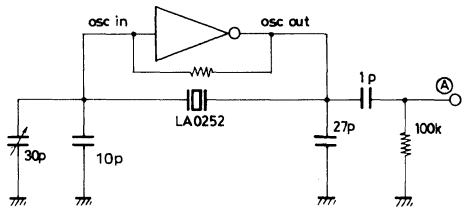
9. Proper Cares in Using IC

1. Accuracy of oscillation frequency in clock application and only frequency display application

   Clock operation: An error of 1 ppm is equivalent to a monthly error of approximately 2.6 seconds. Therefore, an error within ±10 ppm must be attained to yield a monthly error within ±30 seconds. An error within ±10 ppm is attained by adjusting the oscillation frequency to within $4.0 \times 10^6 \pm 40$Hz.

   Frequency display only: The count error shown below is attained by adjusting the oscillation frequency to within 4.0×10^6Hz±100 ppM ($4.0 \times 10^6 \pm 400$Hz).
   AM: ±100Hz
   FM: ±10kHz

2. How to adjust the oscillation frequency

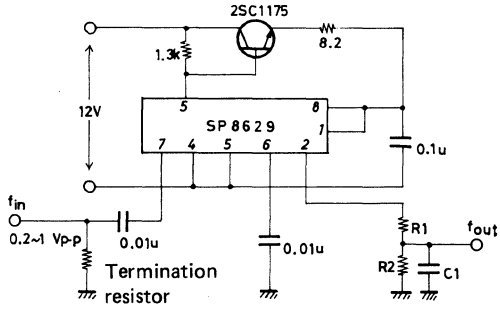


- For 10pF, 27pF, it is recommended to use capacitors having a temperature characteristic of 0 ppm.
- 27pF is a value including a stray capacitance of the board.
- Connect a probe (10pF or less, 5Mohm or more) to (A) and count with a frequency counter.
- Number of digits of counter
  Clock operation 6 digits or more
  Frequency display only 5 digits or more
- Refer to the OSC characteristic mentioned later.

3. How to improve the S/N

   The main noise source is the 4MHz oscillator and prescaler. Of course, these noise sources must be separated from the receiving system as far as possible and further it is recommended to take the necessary measures shown below around the LC7250.

   (1) Connect a capacitor of 0.22 μF (ceramic) or 2.2 μF (electrolytic) as close to the V_{DD} pin and V_{SS} pin of the LC7250 as possible.
   (2) Separate V_{DD} of the LC7250 from the power line of LED.
   Make the V_{SS} line of the LC7250 thick and short and separate it from other GND line.
   (3) Limit the amplitude of FM prescaler output to 0.7 to 1.0V.



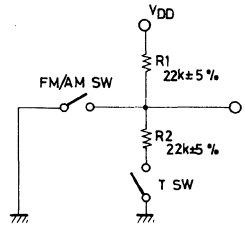
How to fix R1, R2, C1 constants

Fix the ratio of R1 to R2 and the constant of C1 so that the following waveform of f_{out} is obtained at R1 + R2 = 5 to 10 kohm, f_{in} = 120 MHz (FM upper limit frequency).

Obtain the waveform approaching a triangular waveform.

(4) If it is necessary to make S/N 60 to 70 dB or more, it is desirable to shield the LC7250 and peripheral circuit including the prescaler.

4. How to correct the error of a frequency displayed
With a frequency displayed, follow the procedure shown below. R2 and T SW are provided for this correction.



(1) How to fine-correct FM frequency displayed

	FM/AM SW	T SW
(1) Set to the FM display mode.	off	off
(2) For example, receive 80.00 MHz and input 1/100-divided FM local OSC frequency to the Fin pin.	off	off
(3) Set the FM/AM pin to $1/2V_{DD}$.	off	on
(4) Adjust FM adjusting variable resistor (FM-VR) so that the display becomes 80.0 and flashing on the 4th digit stops.	off	on
(5) Set the FM/AM pin to V_{DD}.	off	off
(6) This completes adjustment.		

(2) How to fine-correct AM frequency

	AM/AM SW	T SW
(1) Set to the AM display mode.	on	off
(2) For example, receive 950 kHz and input AM local OSC frequency to the Fin pin.	on	off
(3) Set the FM/AM pin to $1/2V_{DD}$.	on	on (Must go through this state.)
(4) Adjust AM adjusting variable resistor (AM-VR) so that the display becomes 950 and flashing on the 4th digit stops.	off	on
(5) Set the FM/AM pin to V_{SS}.	on	off
(6) This completes adjustment.		

(3) Operation during fine-connection
The counter for frequency display has 4.5 digits and gives 3.5-digit display with the 5th digit discarded. With the FM/AM pin set to $1/2V_{DD}$, flashing stops when the 5th digit is 4 or 5; flashing at a 2 Hz occurs when the 5th digit is other than 4 or 5.
In (1) above, 80.0 display is given at 80.00 MHz±40 kHz of receiving frequency. In (2) above, 950 display is given at 950 kHz±40 kHz of receiving frequency.

[Reference Data] /OSC Characteristic]

Note for designing

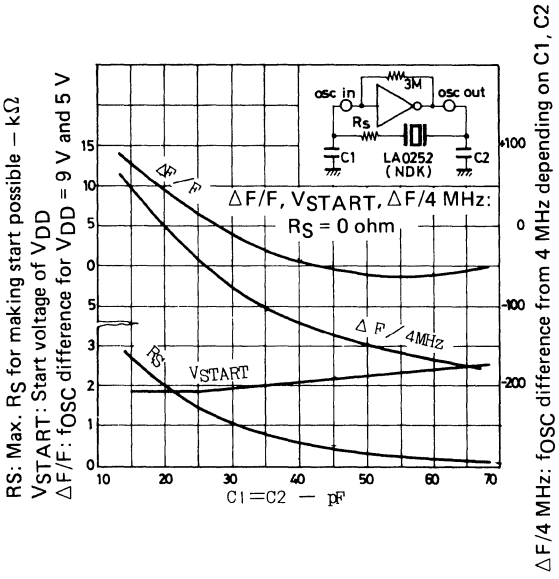
(1) C1 = C2 = 43 pF or 68 pF is recommended considering the reduced voltage characteristic ($\Delta F/F$).

(2) It is desirable to make (V_{START} R_S) C1 and C2 smaller considering the stability in oscillation.

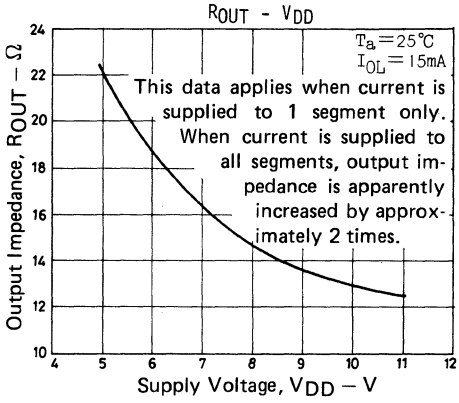
(3) C1 = C2 = 27 pF is recommended considering the balance between (1) and (2) above. This value include a stray capacitance of the board. In actual applications, it is recommended to use a ceramic capacitor of 10 pF, a trimmer capacitor of 30 pF for C1 and a ceramic capacitor of 27 pF for C2. 27 pF for C2.

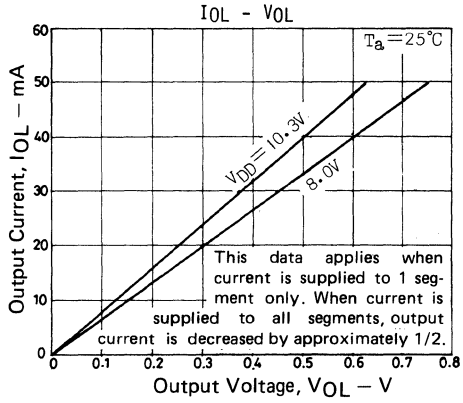
(4) Oscillation frequency (f_{OSC}) of the LA0252 must be fixed so that $\Delta F/4$ MHz = 0 ppm is yielded at C1 = C2 = 27 pF (typ). Since V_{DD}, R_S, etc. are also the factors that change f_{OSC}, information on V_{DD}, R_S, etc. should be given to the crystal manufacturer.

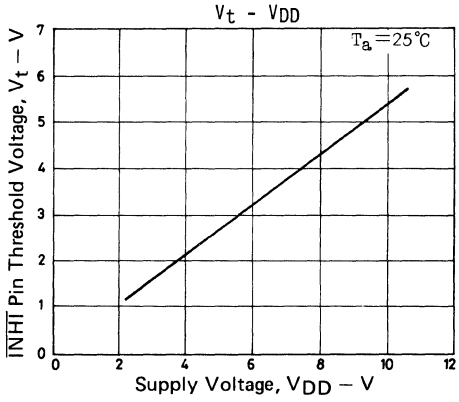
(5) 1 ppm equivalent to a monthly error of approximately 2.6 seconds

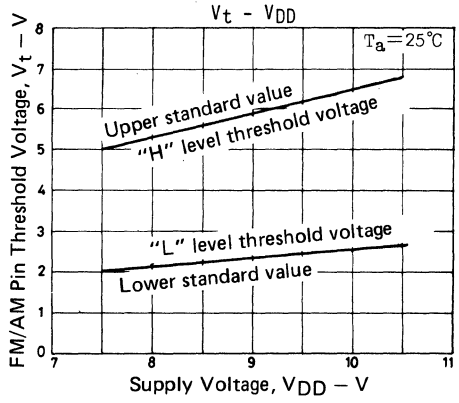


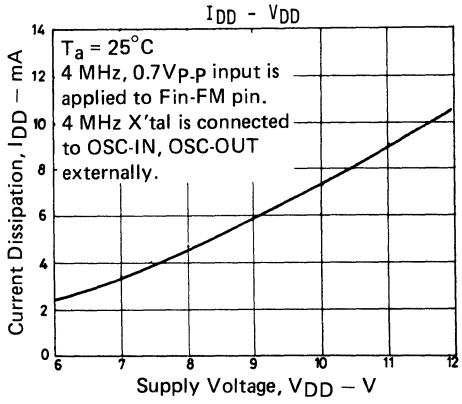
10. Various Characteristics (See below.)

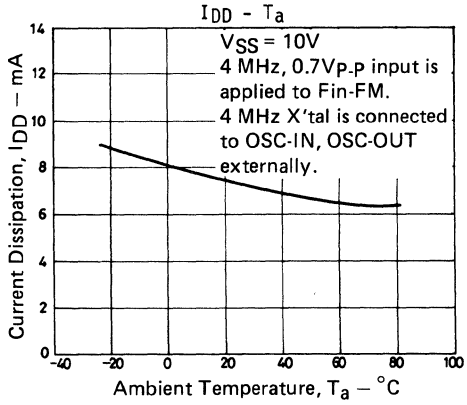

ROUT - VDD
Ta=25°C
IOL=15mA
This data applies when current is supplied to 1 segment only. When current is supplied to all segments, output impedance is apparently increased by approximately 2 times.
Output Impedance, ROUT – Ω
Supply Voltage, VDD – V

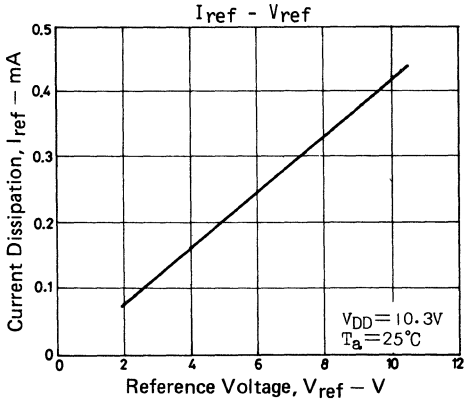

IOL - VOL
Ta=25°C
VDD=10.3V
8.0V
This data applies when current is supplied to 1 segment only. When current is supplied to all segments, output current is decreased by approximately 1/2.
Output Current, IOL – mA
Output Voltage, VOL – V

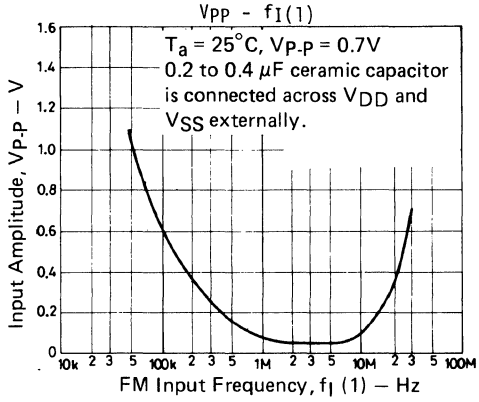

Vt - VDD
Ta=25°C
INH Pin Threshold Voltage, Vt – V
Supply Voltage, VDD – V

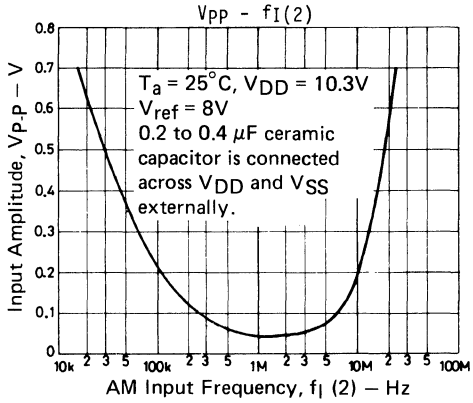

Vt - VDD
Ta=25°C
Upper standard value
"H" level threshold voltage
"L" level threshold voltage
Lower standard value
FM/AM Pin Threshold Voltage, Vt – V
Supply Voltage, VDD – V

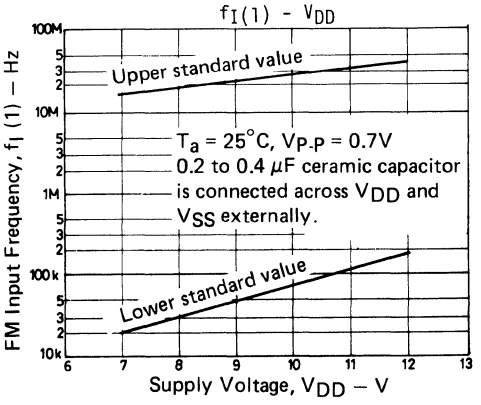

IDD - VDD
Ta = 25°C
4 MHz, 0.7Vp-p input is applied to Fin-FM pin.
4 MHz X'tal is connected to OSC-IN, OSC-OUT externally.
Current Dissipation, IDD – mA
Supply Voltage, VDD – V

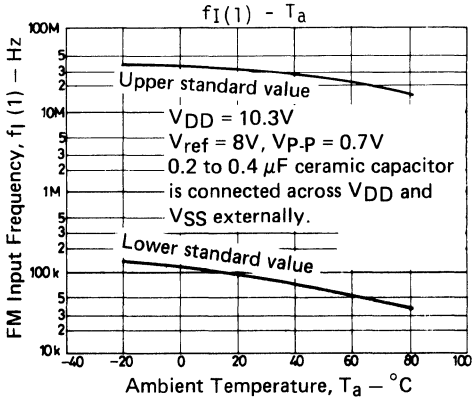

IDD - Ta
VSS = 10V
4 MHz, 0.7Vp-p input is applied to Fin-FM.
4 MHz X'tal is connected to OSC-IN, OSC-OUT externally.
Current Dissipation, IDD – mA
Ambient Temperature, Ta – °C

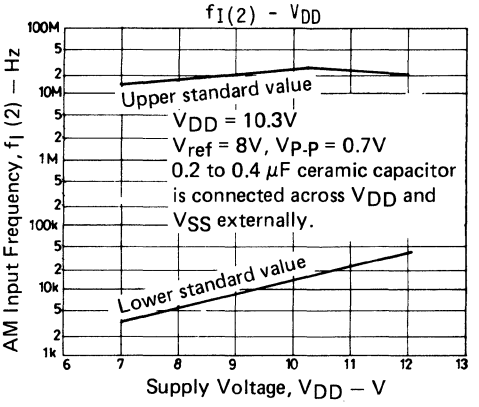

Iref - Vref
VDD=10.3V
Ta=25°C
Current Dissipation, Iref – mA
Reference Voltage, Vref – V

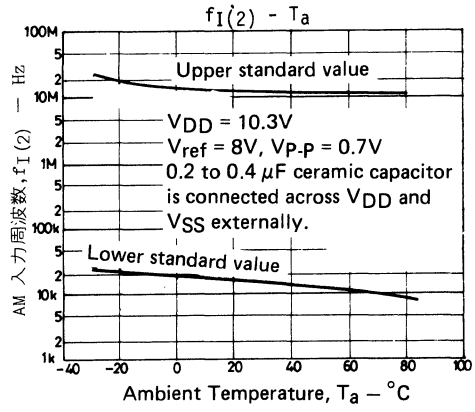

VPP - fI(1)
Ta = 25°C, VP-P = 0.7V
0.2 to 0.4 μF ceramic capacitor is connected across VDD and VSS externally.
Input Amplitude, VP-P – V
FM Input Frequency, fI (1) – Hz


VPP - fI(2)
Ta = 25°C, VDD = 10.3V
Vref = 8V
0.2 to 0.4 μF ceramic capacitor is connected across VDD and VSS externally.
Input Amplitude, VP-P – V
AM Input Frequency, fI (2) – Hz

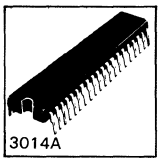

fI(1) - VDD
Upper standard value
Ta = 25°C, VP-P = 0.7V
0.2 to 0.4 μF ceramic capacitor is connected across VDD and VSS externally.
Lower standard value
FM Input Frequency, fI (1) – Hz
Supply Voltage, VDD – V


fI(1) - Ta
Upper standard value
VDD = 10.3V
Vref = 8V, VP-P = 0.7V
0.2 to 0.4 μF ceramic capacitor is connected across VDD and VSS externally.
Lower standard value
FM Input Frequency, fI (1) – Hz
Ambient Temperature, Ta – °C


fI(2) - VDD
Upper standard value
VDD = 10.3V
Vref = 8V, VP-P = 0.7V
0.2 to 0.4 μF ceramic capacitor is connected across VDD and VSS externally.
Lower standard value
AM Input Frequency, fI (2) – Hz
Supply Voltage, VDD – V


fI(2) - Ta
Upper standard value
VDD = 10.3V
Vref = 8V, VP-P = 0.7V
0.2 to 0.4 μF ceramic capacitor is connected across VDD and VSS externally.
Lower standard value
AM 入力周波数, fI (2) — Hz
Ambient Temperature, Ta – °C

LC7253



C MOS LSI

Digital Frequency Indicator with Clock Function (F Tube Use)

Ⓔ 628B

Table of Contents

USE:

- FM/SW/MW/LW receiving frequency display and clock for automobile and table top radios
- For automobile clock
  Month-day display, hour-minute display, and stop watch display

FUNCTIONS:

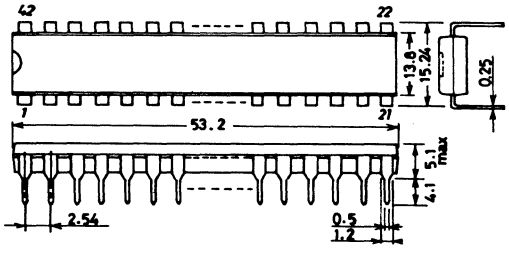
- FM receiving frequency display, 5-digit display in increments of 50kHz
- SW receiving frequency display, 5-digit display in increments of 5kHz or 4-digit display in increments of 10kHz (up to 19995kHz)
- MW/LW receiving frequency display, 4-digit display in increments of 1kHz
- Hour-minute display
- Month-day display and stop watch display
  Either month-day display or stop watch display selectable

FEATURES:

1. 1 chip C-MOS LSI for static display
2. Direct driving of fluorescent character display tube possible
3. Display changeable either to time or to frequency modes
4. Digital display of receiving frequency by using FM/SW/MW/LW local oscillation signal of varactor diode, variable capacitor, or μ tuning system, etc.
5. Selectable between three MW/LW IF frequencies (+450, +455, +469 kHz)
6. Selectable between two FM IF frequencies (+10.7, −10.7 kHz)
7. Adjustable to SW IF frequency of 466 to 472 kHz by variable resistance
8. Fine adjustment of FM/MW/LW display frequency error independently
   MW and LW . . . adjustable within ±2.8 kHz by variable resistance
   FM . . . . . .adjustable within ±140 kHz by variable resistance
9. Selectable either 12 hour display with PM sign or 24 hour display (PM sign is displayed only when setting.)

◇ Refer to related products on the next page.

Case Outline 3014A-D42IC
(unit: mm)



SANYO: DIP42

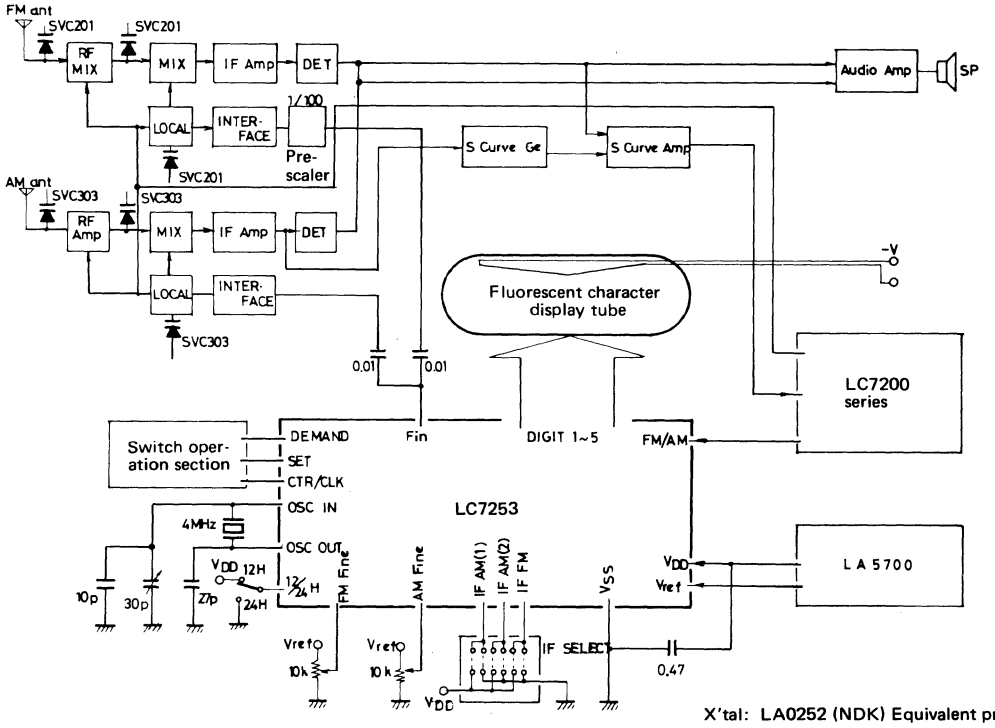
10. Programed on 30-day month and 31-day month (February is set to 29 days.)
11. Able to be set to a radio time tone with ease
12. Stop watch can count and display from 1 second to 12 hours 59 minutes 59 seconds
13. Built-in inhibit pin inhibits the time setting function keeping the display blanked ·
14. 4 MHz crystal is used as a reference frequency.

■ **Related Products**

• The models for digital frequency display series LSI LC7250 are as follows:

Function	LC7250	LC7253	LC7253G	LC7258	LC7257
Display Tube	LED	* Fluorescent character display tube	LED	* Fluorescent character display tube	LED
Display Digit	4	5 (5th digit: 0 or 5)	5 (5th digit: 0 or 5)	5 (5th digit: 0 or 5)	5 (5th digit: 0 or 5)
Band	FM/MW/LW	FM/SW/MW/LW	FM/SW/MW/LW	FM/SW/MW/LW	FM/SW/MW/LW
Clock Function	Available	Available	Available	None	None

1. LC7253 applied system block diagram

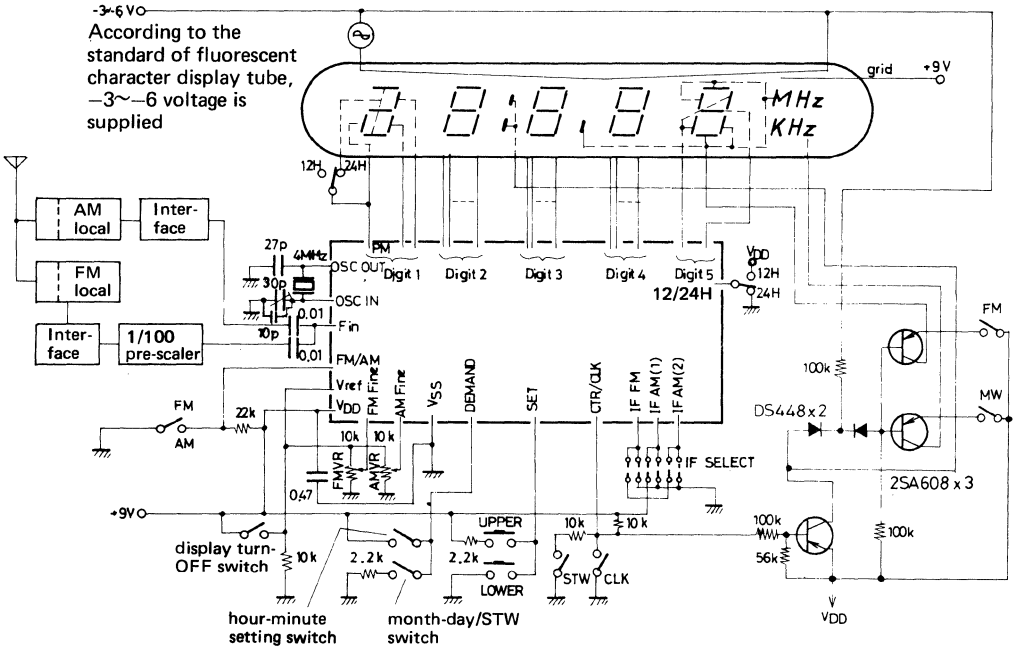


X'tal: LA0252 (NDK) Equivalent product

2. Sample application circuit (digitron display)

Band and digit	IF frequency	FM/AM	IF-FM	IF-AM(1)	IF-AM(2)
FM 5 digits	+10.7±0.14 MHz	[H]	[H]	[H], [L]	[L]
FM 5 digits	−10.7±0.14 MHz	[H]	[L]	[H], [L]	[L]
SW 5 digits	+446~472 kHz	[H]	[H]	[H], [L]	[H]
SW 4 digits	+416~472 kHz	[L]	[H]	[H], [L]	[H]
MW 4 digits	+455±2.8 kHz	[L]	[H], [L]	[L]	[L]
MW 4 digits	+469±2.8 kHz	[L]	[H], [L]	[H]	[L]
MW 4 digits	+450±2.8 kHz	[L]	[L]	[H], [L]	[H]

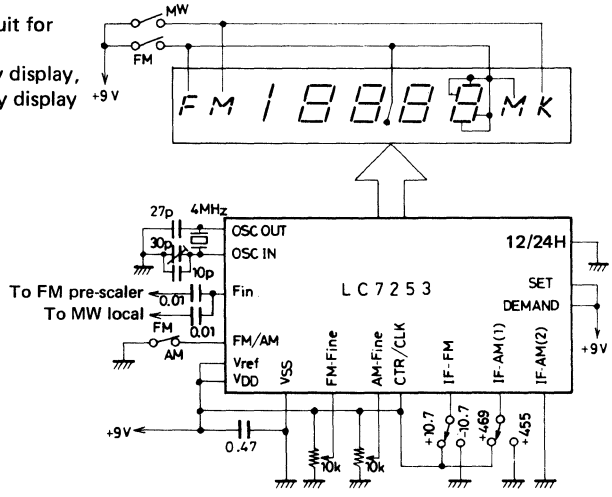
2-1) FM 5-digit, MW 4-digit display (no digital display for SW) with clock



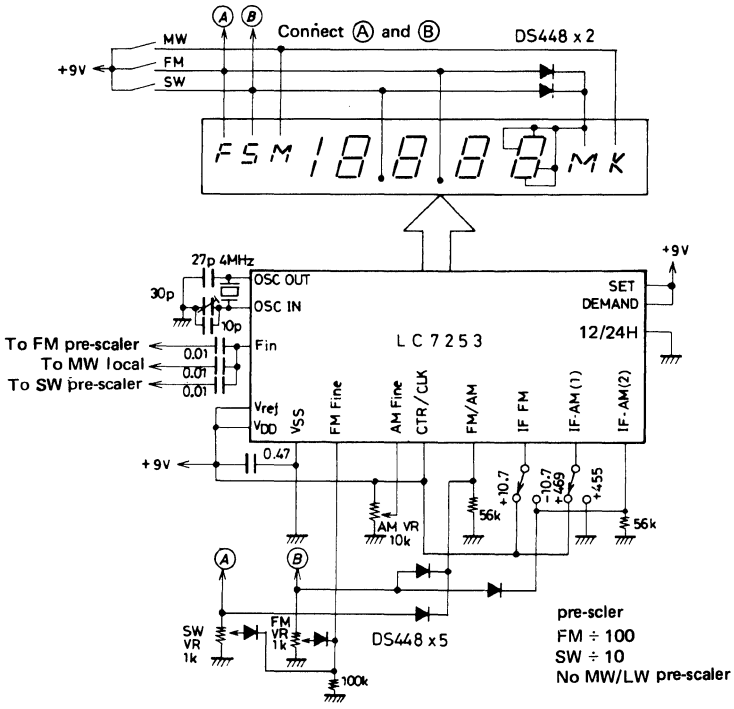
Note: If the 5th digit is not connected, FW and MW are displayed in 4 digits.

2-2) Sample application circuit for frequency display only

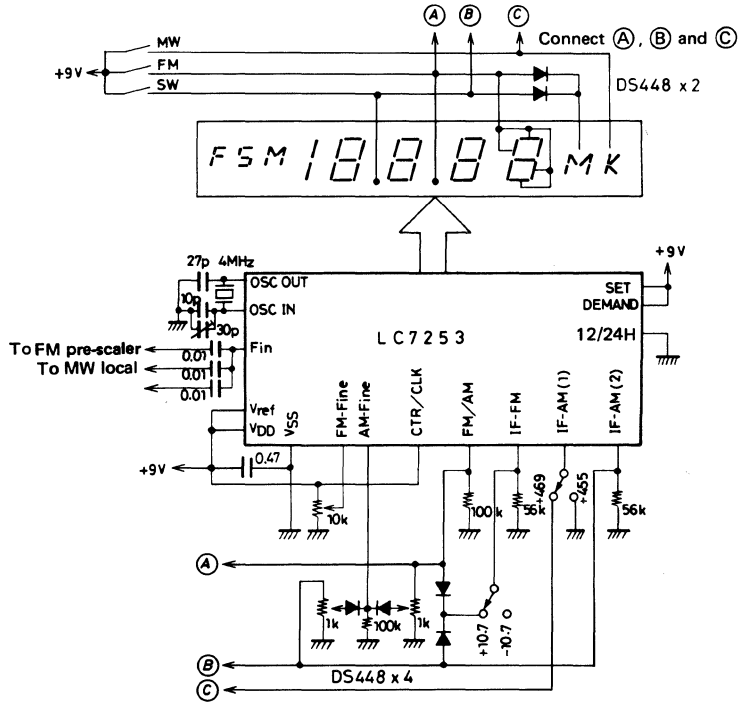
a. FM 5-digit frequency display, MW 4-digit frequency display



b. FM 5-digit frequency display, SW 5-digit frequency display, and MW 4-digit frequency display

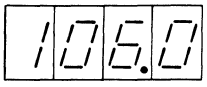


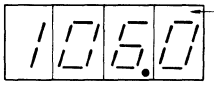
c. FM 5-digit frequency display, SW 4-digit frequency display, and MW 4-digit frequency display



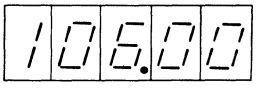
3. Sample display at each mode

3-1) FM display: Display at receiving 106 MHz

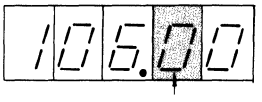




Adjust FM-VR. The best condition for receiving is where the pin of digit 5 changes from 'H' to 'L'.



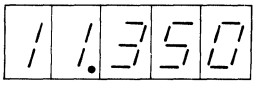
Vary FM/AM pin from V_{DD} to 1/2 V_{DD}. (Adjust ceramic filter display error, etc. per set.)



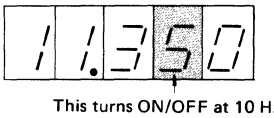
This turns ON/OFF at 10 Hz where display error has not been corrected. Stop flashing by adjusting FM-VR.

3-2) SW display: Display at receiving 11350kHz

○ SW 5-digit display

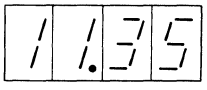


Vary FM/AM pin from V_{DD} to 1/2 V_{DD}.

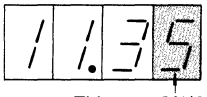


This turns ON/OFF at 10 Hz where display error has not been corrected. Stop flashing by adjusting SW-VR.

○ SW 4-digit display

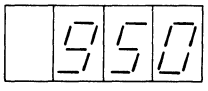


Vary FM/AM pin from V_{SS} to 1/2 V_{DD}.

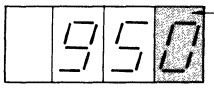


This turns ON/OFF at 10 Hz where display error has not been corrected. Stop flashing by adjusting SW-VR.

3-3) AM display: Display at receiving 950 kHz

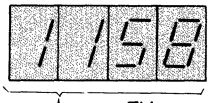


Vary FM/AM pin from V_{SS} to 1/2 V_{DD}.



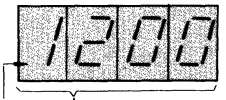
This turns ON/OFF at 10 Hz where display error has not been corrected. Stop flashing by adjusting AM-VR.

3-4) Time tone setting: Setting to 12:00 PM



This turns ON/OFF at 2 Hz at time tone set mode.

Set to time tone at SET pin.

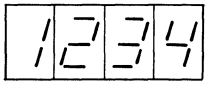


PM sign.

This turns ON/OFF at 2 Hz at time tone set mode.

In setting to time tone, minute digit changes to 00, and hour digits are added by 1 when minute display is 30 to 59. (Counts over 30 and cuts away 29 or less.)

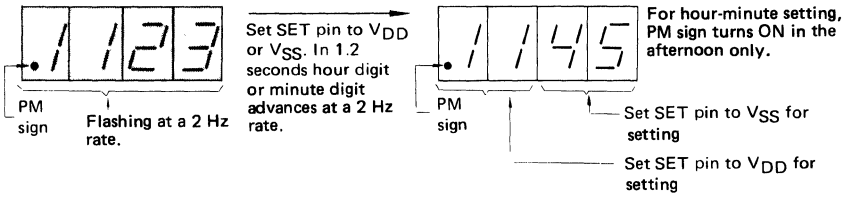
3-5) Hour-minute display: Display at 12:34



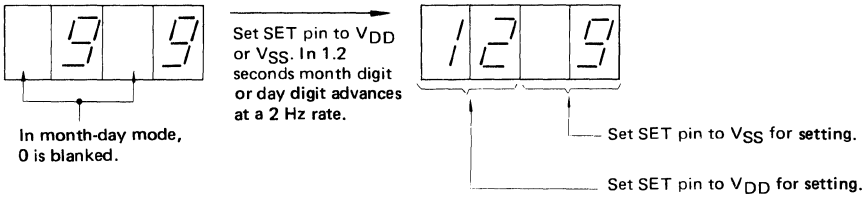
For the hour-minute display PM sign is always blanked.

0 in 10's place is blanked.

3-6) Hour-minute setting: Setting from 11:23 PM to 11:45

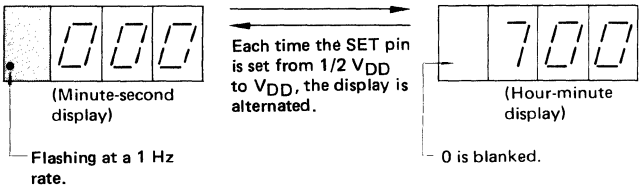


3-7) Month-day display and setting: Setting from September 9 to December 9

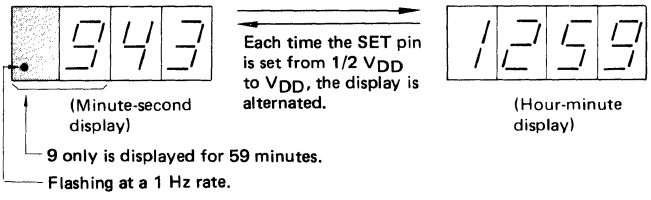


3-8) Stop watch display

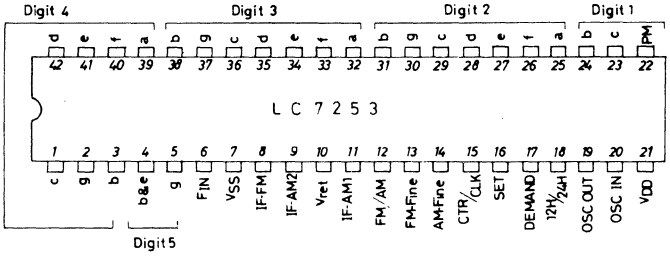
○ 7 o'clock 00 minute 00 seconds



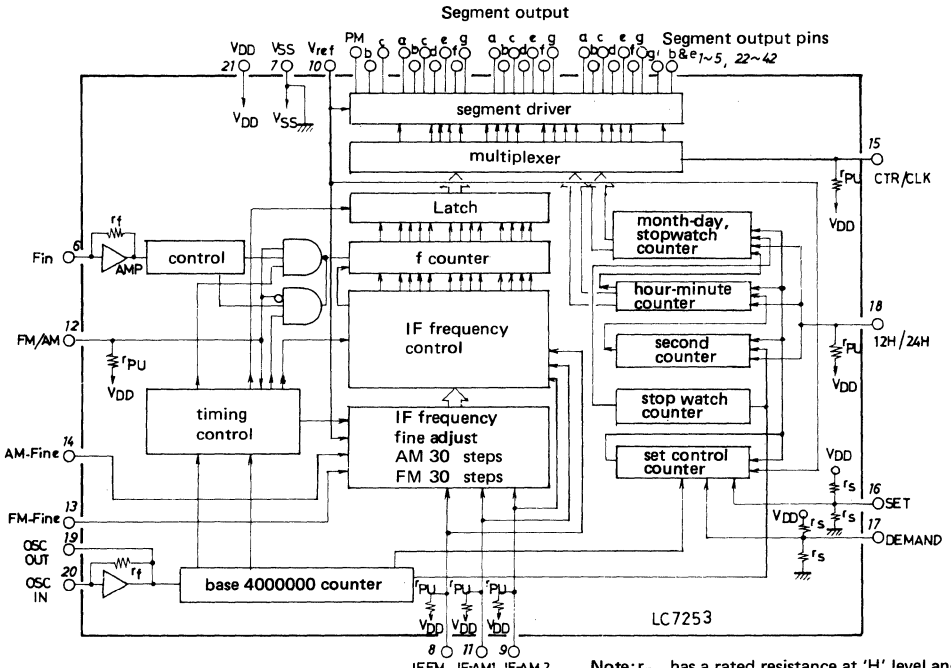
○ 12 o'clock 59 minutes 43 seconds



4. Pin assignment



5. Equivalent circuit block diagram



Note: r_{pu} has a rated resistance at 'H' level and a high resistance at 'L' level.

6. Display

6-1) Formation and display font
Time and frequency are displayed using 4 and a half digit 7 segment fluorescent character display tubes as follows:

Display font 1 2 3 4 5 6 7 8 9 0

6-2) Lighting method
- Static lighting

6-3) Display range
- Frequency (MW/LW)
  000 kHz to 1999 kHz (first digit '0' is blanked.)
- Frequency (SW)
  In 4-digit display:
  0.00 to 19.99 MHz (first digit '0' is blanked.)
  In 5-digit display:
  0.000 to 19.995 MHz (first digit ('0' is blanked.)
- Frequency (FM):
  00.00 to 99.95 MHz (first digit '0' is blanked.)
- Clock (12 hours):
  1:00 to 12:59 PM (first digit '0' is blanked.)
- Clock (24 hours):
  0.00 to 23:59 (first digit '0' is blanked.)
- Stop watch (minute-second):
  0 minute 00 second to 9 minutes 59 seconds (first digit '0' is blanked.)
- Stop watch (hour-minute):
  0:00 to 12:59 (first digit '0' is blanked.)

7. Input/output signal

7-1) Switching signal
- Logical 'H' - V_{DD}
- Logical 'M' - 1/2 V_{dd} (intermediate level between V_{DD} and V_{SS})
- Logical 'L' - V_{SS}

7-2) Fin pin input signal
- Amplitude - 0.7 V and over

- Fin pin input signal
  - FM: 2.0 MHz or less (supply input of FM local osc frequency divided to 1/100)
  - SW: 2.5 MHz or less (supply input of SW local osc frequency divided to 1/10)
  - MW/LW: 2.5 MHz or less

7-3) Reference frequency:
Use a 4.000000 MHz crystal.

7-4) Segment output:
P-channel open drain

8. Pin description

8-1) CTR/CLK (counter & clock) input pin
- Input pin for selection among frequency display, time, or stop watch
- 'L' level . . . Display of hour-minute and month-date
- 'M' level . . . Display of hour-minute and stop watch
- 'H' level . . . Display of frequency counter

8-2) FM/AM (selection of FM or AM) input pin
- Input pin for changing a frequency counter and frequency control to FM or AM
- 'L' level . . . AM display or 4-digit SW display
- 'H' level . . . FM display or 5-digit SW display

8-3) IF-FM (FM IF frequency setting) input pin
- Input pin for designating FM IF frequency. FM/AM='H', IF-AM(2)='L' only.
- IF frequency can be applied at − 10.7 MHz or at +10.7 MHz.
- 'L' level . . . −10.7 MHz
- 'H' level . . . +10.7 MHz

8-4) Setting method of AM IF frequency
- Setting method of MW or LW

FM/AM	IF-FM	IF-AM(1)	IF-AM(2)	IF frequency
[L]	[H],[L]	[L]	[L]	+455 kHz
[L]	[H],[L]	[H]	[L]	+469 kHz
[L]	[L]	[H],[L]	[H]	+450 kHz

- Setting method of SW

FM/AM	IF-FM	IF-AM(1)	IF-AM(2)	IF frequency	Digit
[H]	[H]	[H],[L]	[H]	446~472 kHz	5 digits
[L]	[H]	[H],[L]	[H]	416~472 kHz	4 digits

8-5) FM-Fine (IF frequency fine adjustment) input pin
- Fine-adjustment input pin for correcting the display error of a receiving frequency by means of the ceramic filter for FM-IF, or fine-adjustment input pin for correcting a 5-digit display error of a receiving frequency by means of the ceramic filter SW-IF.
- Input for supplying a divided voltage by inserting a variable resistor between V_{ref}-V_{SS}.

8-6) AM-Fine (IF frequency fine adjustment) input pin
- Fine-adjustment input pin for correcting a display error of a receiving frequency by means of the ceramic filter for AM-IF, or fine-adjustment input pin for correcting a 4-digit display error of a receiving frequency by means of the ceramic filter SW-IF.
- Input for supplying a divided voltage by inserting a variable resistor between V_{ref}-V_{SS}.
- Fine-adjustment range of FM-Fine and AM-Fine.
  - Range for FM:
    FM-Fine :28 steps settable at 10 kHz rate between 10.60 - 10.80 MHz (±140 kHz).
  - Range for MW/LW:
    AM-Fine :28 steps settable at 0.2 kHz rate centering IF frequency (±2.8 kHz).
  - Range for 5-digit SW:
    FM-Fine :Settable at 1 kHz/step between 446 - 472 kHz.
  - Range for 4-digit SW:
    AM-Fine :Settable at 2 kHz/step between 416 - 472 kHz.

8-7) Fin (frequency) input pin
- Input pin for supplying input of FM local osc frequency divided to 1/100 for FM display, for supply input of SW local osc frequency divided to 1/10 for SW display, and for supplying input of MW local osc frequency for MW display.
- Input signals with an input voltage over 0.7 $V_{p\text{-}p}$ (Duty 50% with rectangular waves, sinusoidal waves may be used.)
- Maximum frequency:
  2.5 MHz (AM): 2.0 MHz (FM).

8-8) OSC IN, OSC OUT (crystal oscillation)
- Input or output pin for crystal oscillation
- Input or output pin for connecting a crystal (4.000000 MHz)

8-9) Demand (reading time) input
- Selector input for reading out and setting hour-minute, reading out and setting month-day, and designating the stop watch mode.

CTR/CLK	DEMAND	MODE
[M] / [L]	[H]	Setting by time signal and hour-minute setting mode
[M] / [L]	[M]	Time display
[L]	[L]	Month-day display and month-day setting mode
[M]	[L]	Stop watch mode

Note: The following method can be used for changing modes from month-day mode to stop watch mode or from stop watch mode to month-day mode.
- In the case of changing modes from month-day setting mode to stop watch mode:

CTR/CLK='M', DEMAND='L', SET='L' (1.2 seconds and over)

- In the case of changing modes from stop watch mode to month-day setting mode: CTR/CLK='L', DEMAND='L', SET='L' or 'H' (1.2 seconds and over)
  - ○ In the mode of setting by time signal, all displayed digits are turned ON and OFF (2 Hz).

8-10) SET (time setting) input pin

- Input pin for setting hour, minute, month and day, and starting, stopping and clearing of stop watch mode (corresponding system). The ordinary position of this input pin is 'M'. The input signals for 'L' level and 'H' level consist six ways as follows.
- In the case of setting by time signal and hourminute correction mode (CTR/CLK= 'L' or 'M').

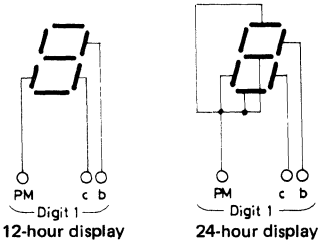
1) 'H' level
   - Hour digit setting
   - Advances at a 2 Hz rate 1.2 seconds after 'H' level is supplied.
2) 'L' level
   - ○ Setting by time signal and minute setting mode.
     - Advances at a 2 Hz rate 1.2 seconds after 'H' level is supplied.
     - Setting by time signal is executed when 'L' level is turned OFF within 1.0 second after. (Counts over 30 and cuts away 29 or less)
       Carry to higher-order digit is inhibited during setting.
   - ○ In the case of month-day setting mode (CTR/CLK='L')
3) 'H' level
   - Month digit setting
   - Advances at a 2 Hz rate 1.2 seconds after 'H' level is supplied.
4) 'L' level
   - Day digit setting mode
   - Advances at a 2 Hz rate 1.2 seconds after 'H' level is suppled.
     Carry to month digit is inhibited during setting.
   - ○ In the case of stop watch mode (CTR/CLK='M')
5) 'L' level
   - Minute-second display, hour-minute display and clear.
   - Counter is cleared 1.2 seconds after an 'L' level is supplied (Display: 0 minute 00 second)
   - Display of minute-second and hour-minute modes are alternately repeated when turned OFF within 1 second after 'L' level is supplied.
   - In order to show the minute-second display, PM output is turned ON and OFF at a 1 Hz rate.
6) 'H' level
   - Start and stop
   - Start and stop are alternately repeated when 'L' and 'M' levels are alternately supplied. At the clear mode, the counter stops and display is provided in minute-second condition mode, and PM pin is turned ON/OFF at a 1 Hz rate.

8-11) V_{ref} pin (also used for inhibition function)

- Reference voltage of FM-Fine and AM-Fine
- This pin is also used to perform the function for turning the segment pins OFF, inhibiting a SET and DEMAND function, and preventing the Fin amplifier from operating. This pin is useful for decreasing the current dissipation when a driver stops his or her car equipped with a car stereo system.
  'H' level: Normal operation
  'L' level: Segment pins OFF, inhibit of function on SET, DEMAND pins.
  Functions of SET and DEMAND pins are to be inhibited when in 'L' level, since time can be prevented from being misset when the indicator is blanked. Amplifier operation is stopped for the purpose of decreasing current dissipation in an amplifier.

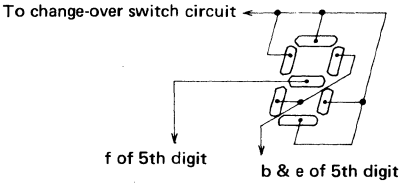
8-12) 12 H/24 H (time display system change-over) input pin

- Input for changing over between displays of 12-hour system with PM sign and 24-hour system.
  'H' level: 12-hour system with PM sign (PM sign is displayed for hour-minute setting modes only)
  'L' level: 24-hour system
- Pin connections are shown below:

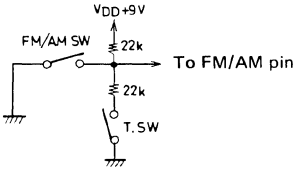


8-13) Connection method of 5th digit

- 5th digit is shown for FM/AM='H' only



9. Fine adjustment of frequency display error
(Refer to Fig. in 2-1).
In the frequency display mode (CLK switch and STW switch are both OFF) fine adjustment can be executed by setting the FM/AM pin to level 'M'.



Circuit example for setting FM/AM pin to 1/2 V_{DD} and the operating method.

The operating methods are shown as follows:

9-1) FM frequency (5 digits) display (Refer to page 5)

Items	FM/AM, SW	T.SW
a. Set to FM display mode.	off	off
b. For instance, receive 80.00 MHz; supply FM local osc frequency divided to 1/100 to Fin pin.	off	off
c. Set FM/AM pin to 1/2 V_{DD}.	off	on
d. Adjust FM VR so that 80.00 is displayed and the 4th digit stops flashing.	off	on
e. Set FM/AM pin to V_{DD}.	off	off
f. Adjustment ends.		

9-2) AM frequency (4-digit MW) display (Refer to page 5)

Items	FM/AM, SW	T.SW
a. Set to AM display mode.	on	off
b. For instance, receive 950 kHz; feed AM local osc frequency to Fin pin.	on	off
c. Set FM/AM pin to 1/2 V_{DD}	on off	on on
d. Adjust AM-VR so that 950 is displayed and the 4th digit stops flashing.	off	on
e. Set FM/AM pin to V_{SS}.	on	off
f. Adjustment ends.		

← This mode must be passed through.

9-3) Other cases
In addition to the example of Fig. in 2-1), 4-digit FM, 5-digit SW and 4-digit SW are explained below.

a. In the case of 4-digit FM
For 9-1 b., the optimum point is the point at which the fine adjustment display by means of FM-VR is 80.0, and the segment g of the 5th digit changes from 'L' to 'H'.

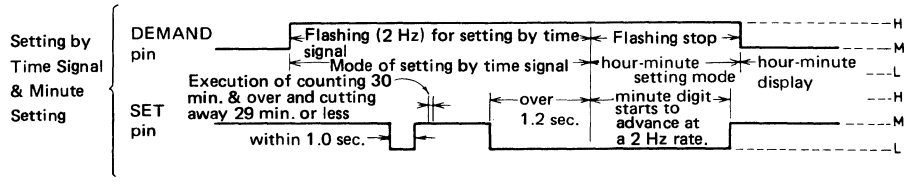
b. In the case of 5-digit SW
The adjustment method shown in 9-1 can be applied. Feed SW local osc frequency to Fin-pin and adjust SW-VR.

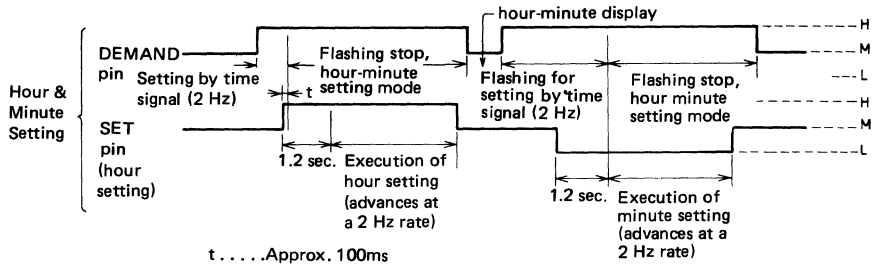
c. In case of 4-digit SW
The same method as described in 9-3 a. can be applied. Supply SW local osc frequency to Fin-pin and adjust SW-VR.

Note: Operation during fine adjustment
In the case of 5-digit FM display, 5th digit counter 0 to 4 is shown as 0, and 5 to 9 as 5. Where fine adjustment is executed by means of changing the FM/AM pin from V_{DD} to half of V_{DD}, the flashing mode stops when the numbers of the 5th digit coincide with number 2 or 7. Otherwise, the fluorescent character display tube turns on and off at a 10 Hz rate. This function is true of SW 5-digit display. In case of AM 4 digit display, 5th digit is cut away. When fine adjustment carried out by changing FM/AM pin from V_{SS} to half V_{DD}, the flashing stops when the numbers of the 4th digit coincide with number 4 or 5. Otherwise, the fluorescent character display tube turns ON/OFF at a 10 Hz rate. Therefore, in the example shown in 9-2 as above, 950 kHz display can be carried out within the range of the receiving frequency 950 kHz ±400 Hz.

10. Timing chart

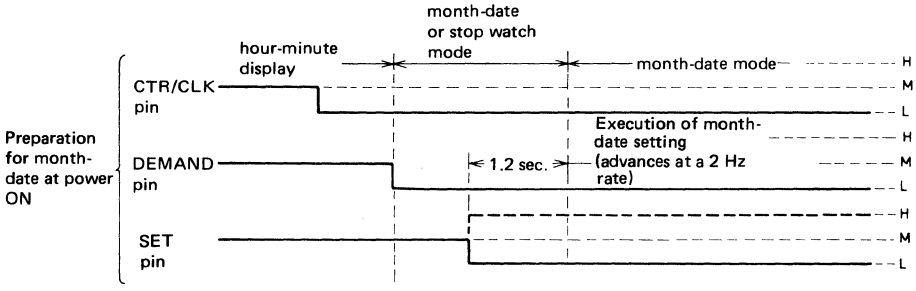
10-1) At time setting (CTR/CLK='L' or 'H')

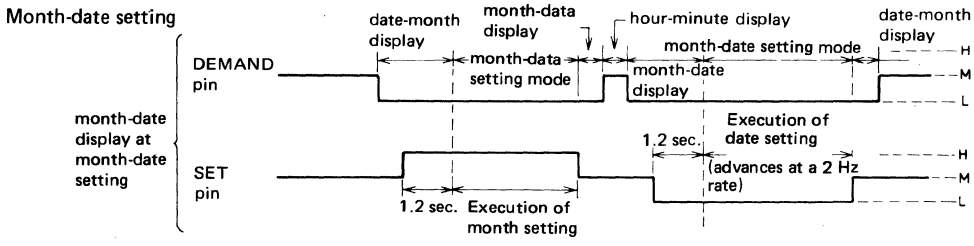




10-2) For month-date mode:

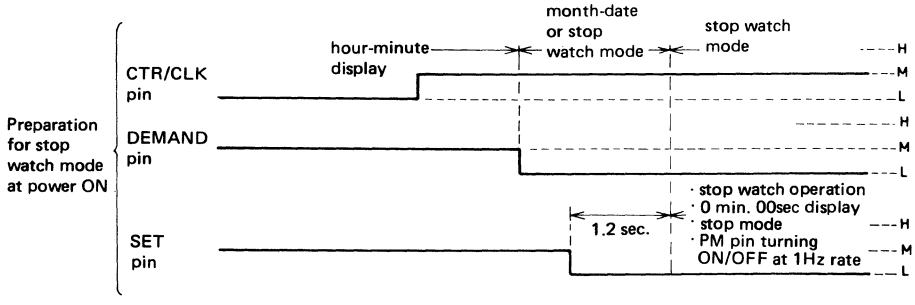
Month-date operation is available by means of the next job execution, because it is unknown whether the month-date mode or stop watch mode is set during the power ON phase.



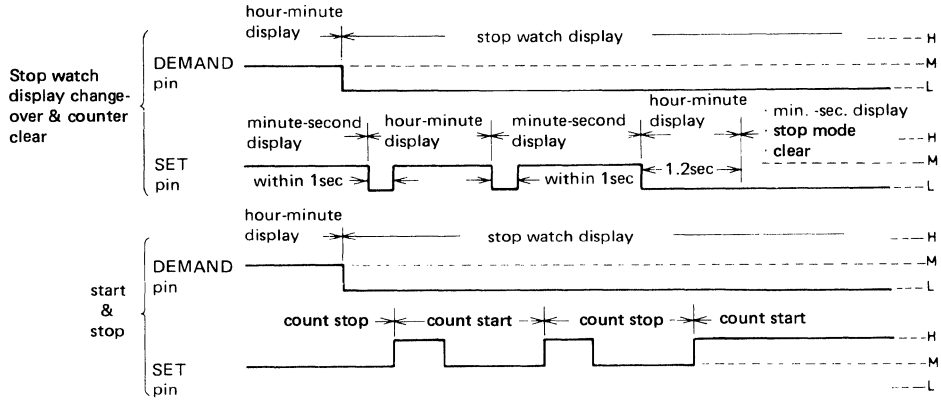


10-3) For stop watch mode:

Stop watch operation is available by means of the next job execution, because it is unkown whether the month-date mode or stop watch counter mode is set during the power ON phase.



• For stop watch mode



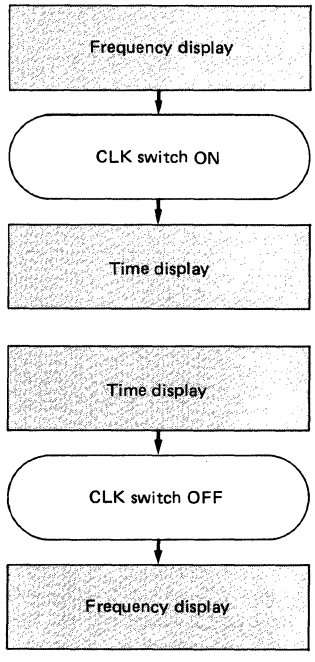
11. Operating method in sample application circuit of Fig. in 2-1)

The operating method of Fig. in 2-1 is explained in the following flow-charts. Within LSI either the month-day function or stop watch function can be used. In this example, when only the CLK switch is provided, the circuit can be used as a clock with month-day function, and when only the STW switch is provided, the circuit can be used as a clock with a stop watch function. (When both switches are set, change-over between both functions is possible.)

11-1) Change-over of display mode

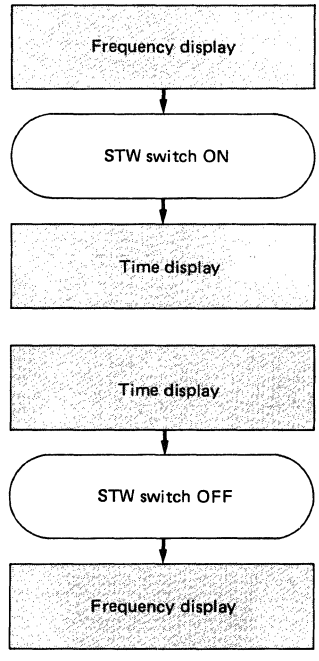
a. Clock with month-day function

◇ STW switch is not provided.

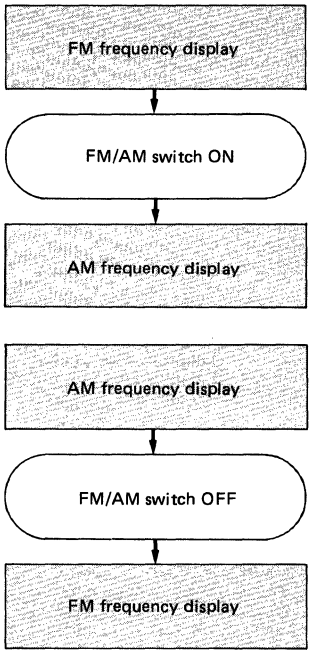


b. Clock with stop watch function

◇ CLK switch is not provided.

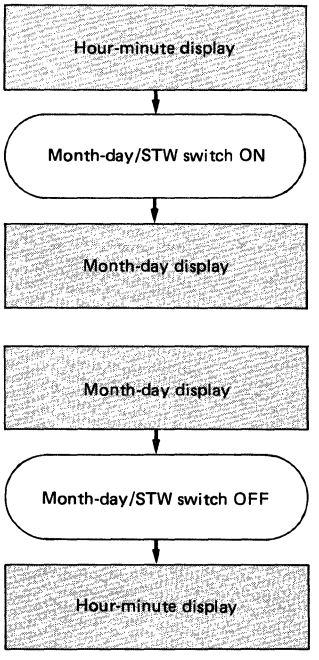


11-2) Band change-over when in the frequency display mode

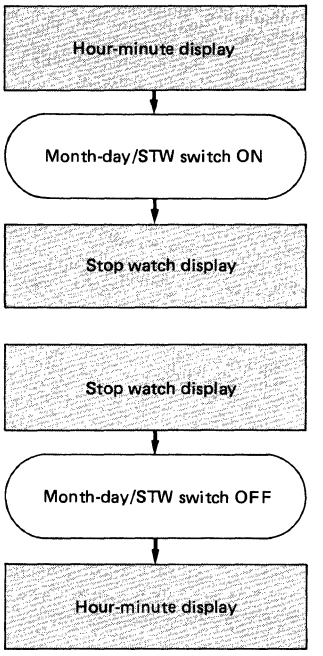


11-3) Change-over of clock display mode

a. Clock with month-day function

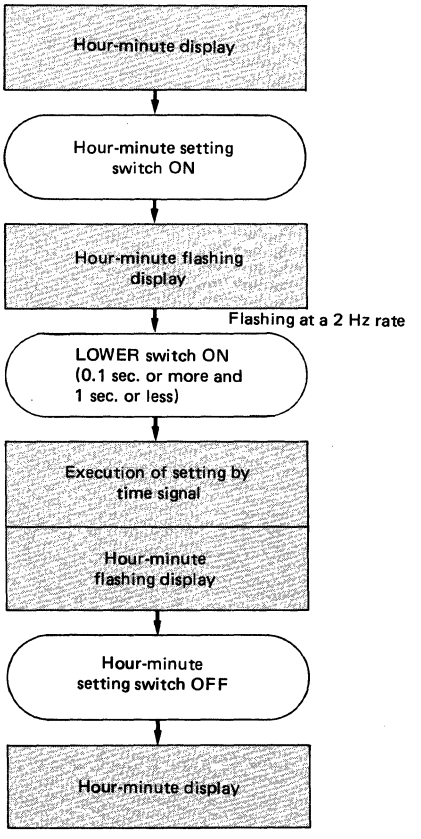


b. Clock with stop watch function

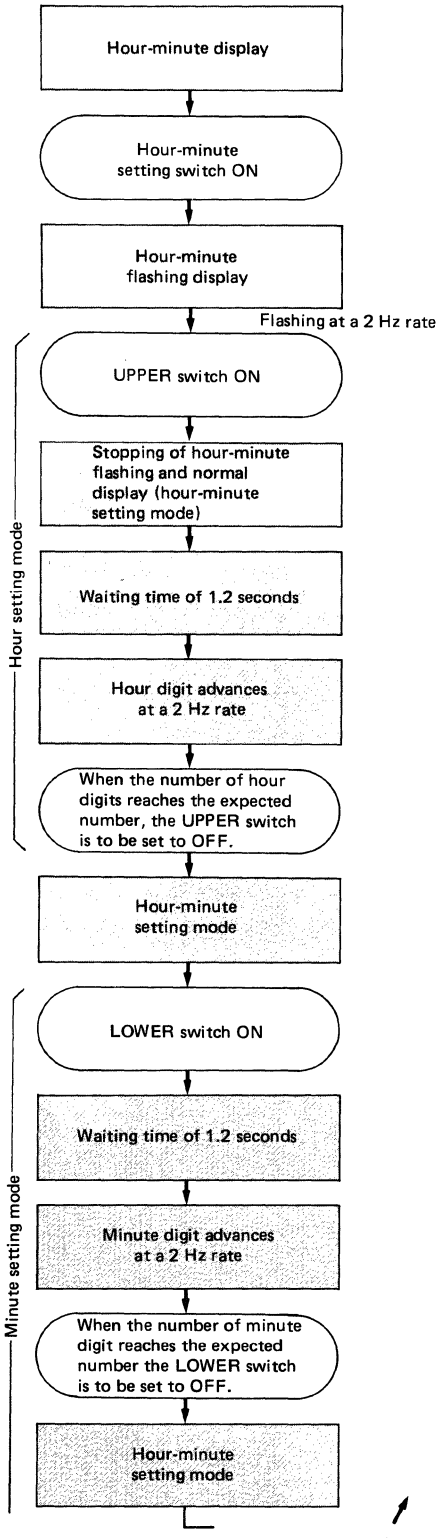


11-4) Setting method of hour-minute

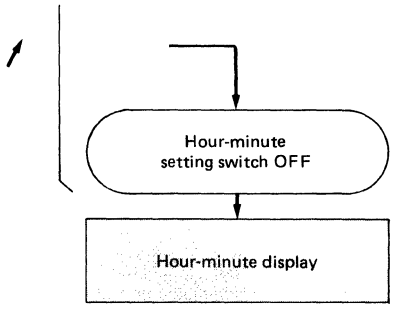
a. Setting by time signal



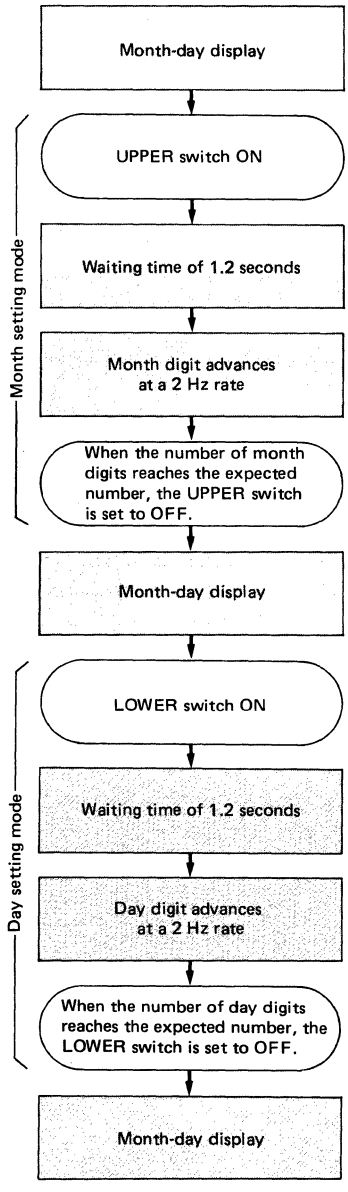
b. Hour-minute setting



(continued on the right)

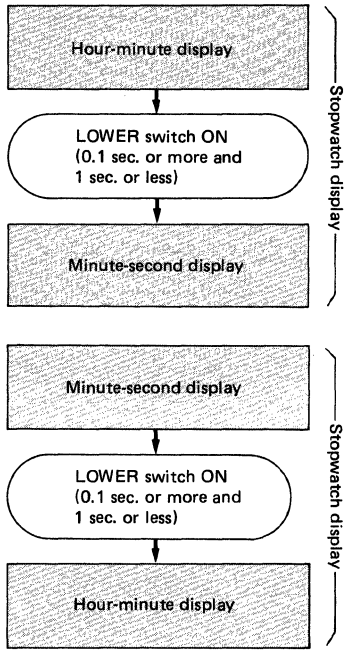


11-5) Month-day setting

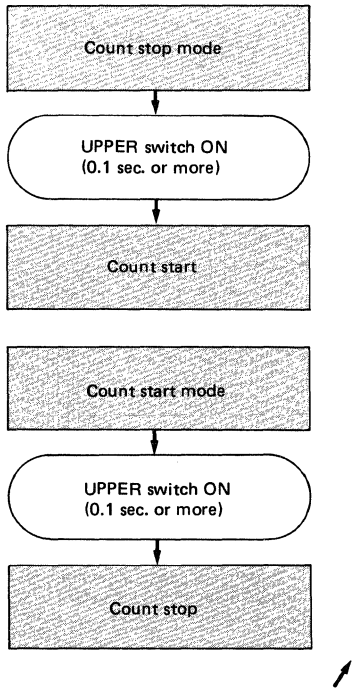


11-6) Stop watch operation

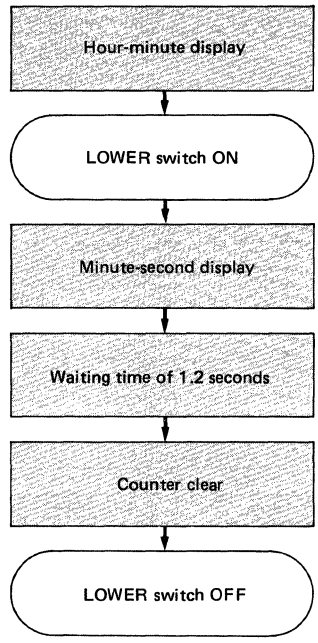
a. Change-over between hour-minute and minute-second

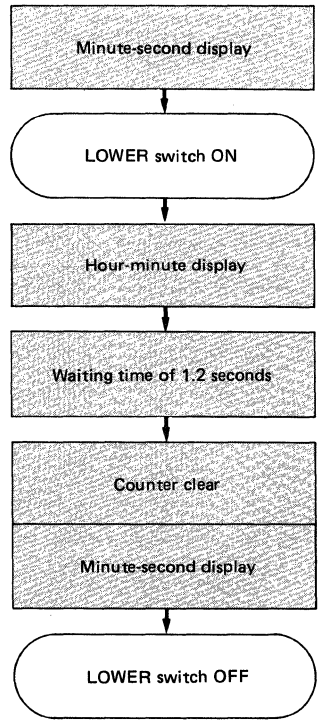


b. Start and stop



c. Clear





12. Main specifications

Absolute maximum ratings/Ta=25°C, V_{SS}=0V

				unit
Maximum supply voltage	V_{DD} max		−0.3~+11	V
Reference voltage	V_{ref}	$V_{ref} \leqq V_{DD}$	−0.3~+11	V
Input voltage	V_I		−0.3~V_{DD}+0.3	V
Output voltage	V_O	Output OFF	V_{DD}−20~V_{DD}+0.3	V
Allowable power dissipation	P_d max	Ta ≦ +75°C	400	mW
Allowable power at segment output	P_d(seg)	PM: $\|I_{OH}\|$<9mA	10	mW
		b & e: $\|I_{OH}\|$<6mA	7	mW
		Other than above: $\|I_{OH}\|$<3mA	3.5	mW
Operating temperature	T_{opg}		−30~+75	°C
Storage temperature	T_{stg}		−40~+125	°C

Allowable operating condition/Ta=25°C, V_{SS}=0V, V_{DD}=7.0~10.0V, V_{ref}=7.0~10.0V, $V_{ref} \leqq V_{DD}$, (V_{ref}=0V, V_{DD}<7.0.)

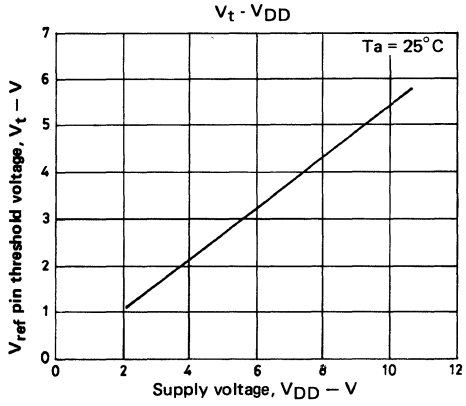
			min	typ	max	unit
Supply voltage	V_{DD}(1)	All functions operate.	7.0		10.0	V
	V_{DD}(2)	Only clock operates.	4.3	5.0	7.0	V
Reference voltage	V_{ref}(1)	Display-ON 0.8V_{DD} ≦ V_{ref} ≦ V_{DD}	7.0		10.0	V
	V_{ref}(2)	Display-OFF	0		0.12V_{DD}	V
Input 'H' level voltage	V_{IH}(1)	SET, DEMAND, CTR/CLK	0.88V_{DD}		V_{DD}	V
Input 'L' level voltage	V_{IL}(1)	SET, DEMAND, CTR/CLK	0		0.12V_{DD}	V
Input 'M' level voltage	V_{IM}	SET, DEMAND, CTR/CLK	0.36V_{DD}		0.64V_{DD}	V
Input 'H' level voltage	V_{IH}(2)	FM/AM, 12H/24H, IF-FM IF-AM(1), IF-AM(2)	0,85V_{DD}		V_{DD}	V
Input 'L' level voltage	V_{IL}(2)	FM/AM, 12H/24H, IF-FM IF-AM(1), IF-AM(2)	0		0.12V_{DD}	V
Input frequency	f_I(1)	Fin (FM/AM=[H] V_{PP} ≧ 0.7V duty=50%	0.6		2	MHz
	f_I(2)	Fin (FM/AM=[L] V_{PP} ≧ 0.7V duty=50%	0.4		2.5	MHz
Operating frequency	f_{opg}	OSC-IN, OSC-OUT, 4 MHz, external X'tal	3.5		4.2	MHz
Input frequency	V_{PP}	Fin (0.47μF ceramic capacitor across V_{DD} and V_{SS})	0.7			V_{p-p}

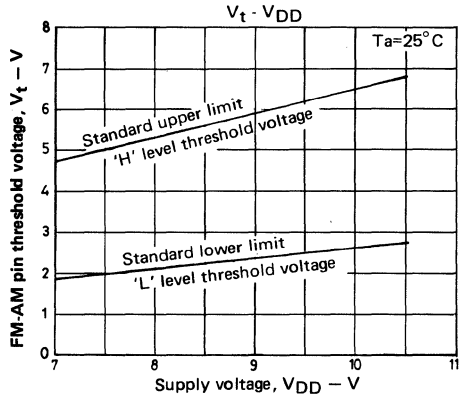
Electrical characteristics/Ta=25°C, V_{SS}=0V, V_{DD}=8~10V, V_{ref}=8~10V, $V_{ref} \leqq V_{DD}$.

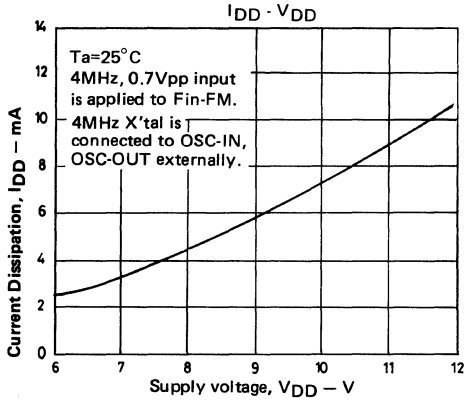
			min	typ	max	unit
Input current	I_{IN}	FM-Fine, AM-Fine, V_I=0V or V_{ref}.	−1		1	μA
Input 'H' level current	I_{IH}(1)	IF-FM, IF-AM(1), IF-AM(2), CTR/CLK, 12H/24H, V_I=0.9V_{DD}	−80	−30	−10	μA
Input 'L' level current	I_{IL}(1)	IF-FM, IF-AM(1), IF-AM(2) CTR/CLK, 12H/24H, V_I=0V	−3		0	μA
Input 'H' level current	I_{IH}(2)	FM/AM, V_I=0.9V_{DD}	−40	−15	−5	μA
Input 'L' level current	I_{IL}(2)	FM/AM, V_I=0V	−3		0	μA
Middle point setting resistor	r_s	SET, DEMAND	40	70	100	kΩ
Input floating voltage	V_{IF}	SET, DEMAND, input floating	0.45V_{DD}		0.55V_{DD}	V
Feedback resistor at Fin	r_f(1)	Feedback resistor across OSC IN and OSC OUT		3		MΩ
	r_f(2)	Feedback resistor at Fin		3		MΩ
Output 'H' level voltage	V_{OH}(1)	PM, V_{DD}=8.0V, I_{OH}=−6mA	V_{DD}−0.6			V
	VOH(2)	b & e, V_{DD}=8.0V, I_{OH}=−4mA	V_{DD}−0.6			V
	V_{OH}(3)	Segment output other than the above mentioned V_{DD}=8.0V, I_{OH}=−2mA	V_{DD}−0.6			V
Output leak current	I_{OFF}	All segment output pins V_{DD}=10V, V_{OUT}=−8V	−3		0	μA
Current dissipation	I_{DD}(1)	V_{DD}=10V, f_I(1)=2.5 MHz (0.7 V_{p-p}), f_{opg}=4 MHz (Crystal mounted.)		8	17	mA
	I_{DD}(2)	V_{DD}=5.5V, f_{opg}=4 MHz (Crystal mounted), V_{ref}=0V		1	2.5	mA
	I_{ref}	V_{DD}=10V, V_{ref}=10V, AM-Fine= FM-Fine=V_{ref}		0.6	1.5	mA

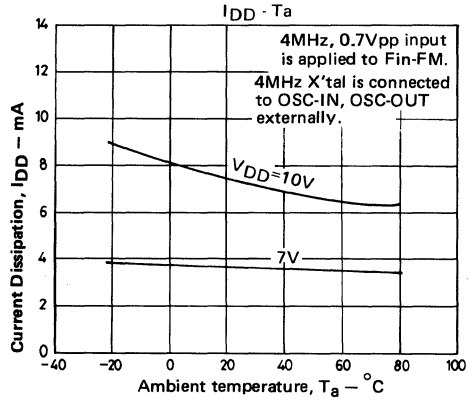
Note: Current direction: +sign: Flowing into LSI
−sign: Flowing out of LSI

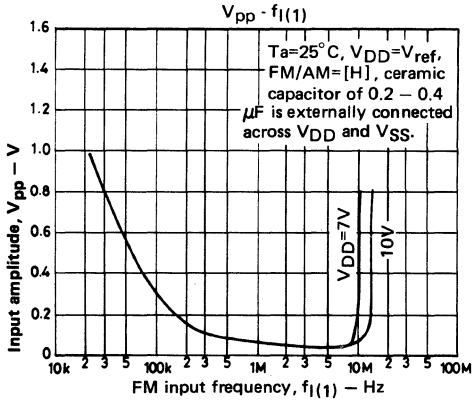
13. Main characteristics

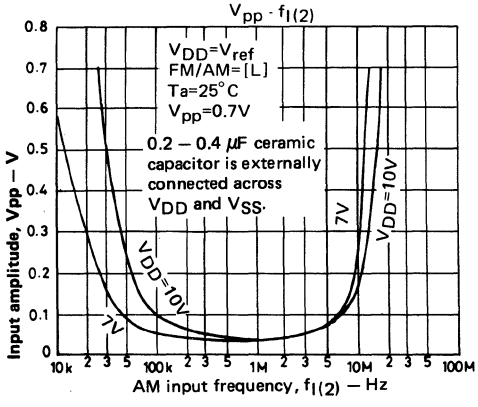


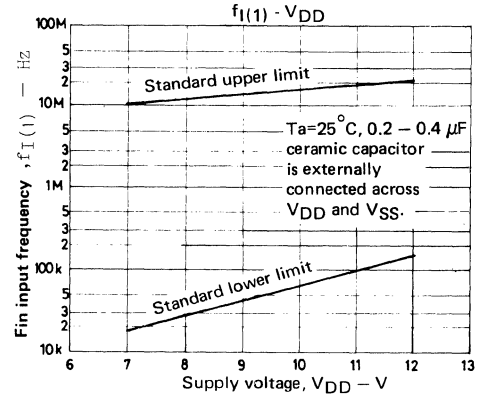


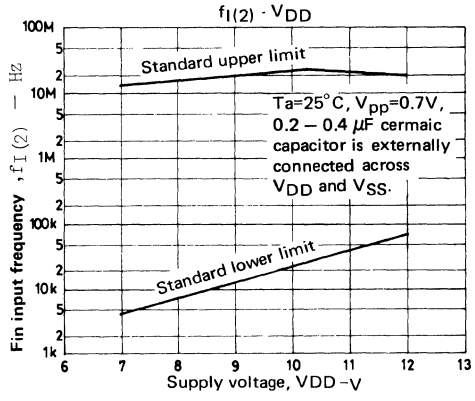


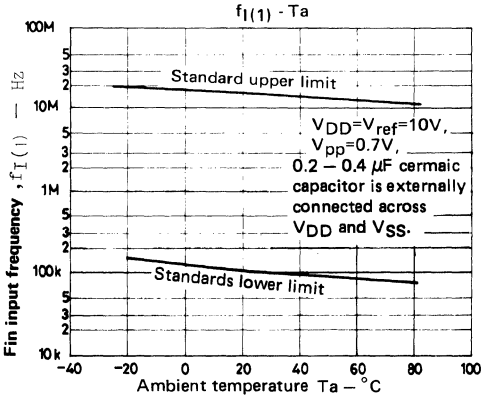


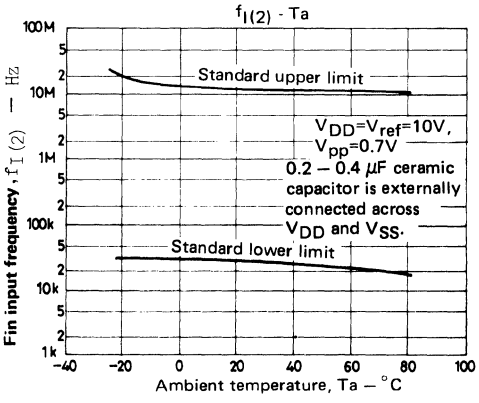


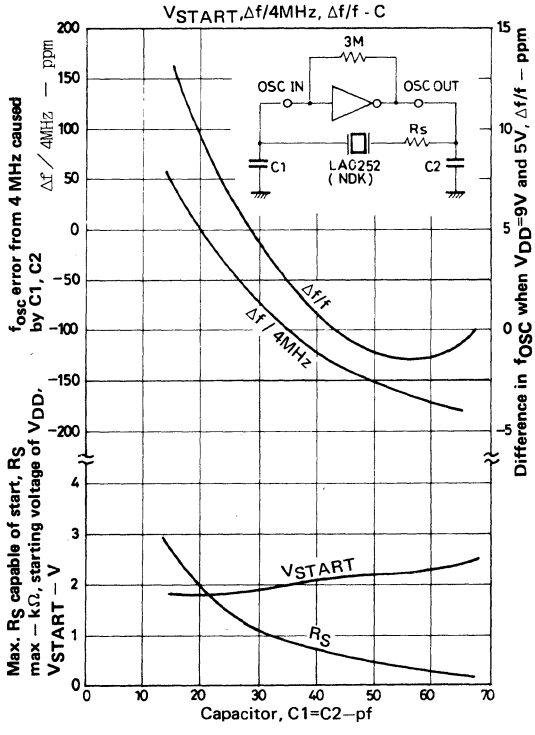




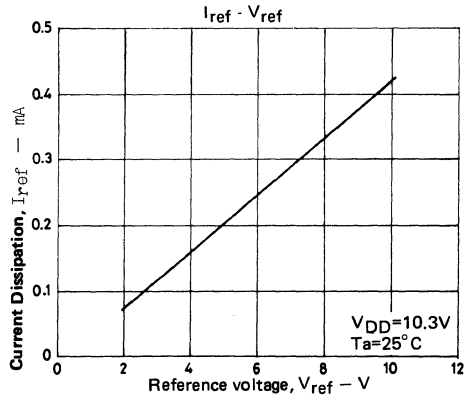








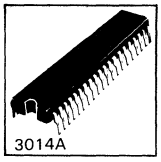
Note) R_S=0Ω; Δf/f, V_{START}, Δf/4MHz



←◆DESIGN NOTES

- It is preferable that C1 = C2 = 43 pF or 68 pF in view of voltage reducted characteristics (Δf/f).
- It is preferable that (V_{START}, Rs) C1 and C2 are maintained at small values from the view point of stable oscillation.
- C1 = C2 = 27 pF is appropriate considering the two above-mentioned points. Please note that C1 and C2 include the floating capacity of the substrate. In practice it is better to use a ceramic capacitor of 10 pF and a trimmer of 30 pF as C1 and a ceramic capacitor of 27 pF as C2. It is preferable to use ceramic capacitors having a temperature characteristic of 0 ppm. An error of OSC frequency of 1 ppm leads to a monthly error of approx. 2.6 sec.

LC7257, 7258



C MOS LSI

5-Digit Frequency Indicator

Ⓔ 786A

The LC7257 comes in two types: Red LED display (LC7257) and green LED display (LC7257F) (cathode common LED).

Use

. FM/SW/MW/LW receiving frequency display for car radios, home radios

Functions

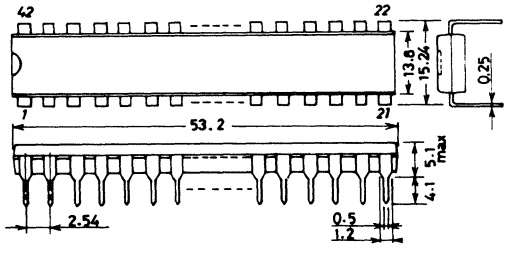
. FM receiving frequency display (5-digit display in increments of 50kHz)
. SW receiving frequency display (5-digit display in increments of 5kHz or 4-digit display in increments of 10kHz (up to 29995kHz)).
. MW/LW receiving frequency display (4-digit display in increments of 1kHz or 10kHz).

Features

1. 1-chip C-MOS LSI for static display.
2. Possible to direct drive LED (LC7257), fluorescent display tube (LC7258).
3. Digital display of receiving frequency by using FM/SW/MW/LW local oscillation signal of varactor diode, variable capacitor, or u tuning system, etc.
4. Covers 3 MW/LW intermediate frequencies (+450, +455, +469kHz).
5. Covers 2 FM intermediate frequencies (+10.7, -10.7MHz).
6. Covers SW intermediate frequencies of 466 to 472kHz selectable through fine adjustment by variable resistor.
7. Possible to fine-adjust FM/MW/LW display frequency independently.
   MW and LW ----- ±2.8kHz adjustable by variable resistor
   FM ---------- ±140kHz adjustable by variable resistor
8. MW receiving frequency display available in increments of 1kHz or 10kHz. (10kHz increment: Only for 450kHz of intermediate frequency)
9. Frequency display locking function.
10. 4MHz crystal for reference frequency.

For related products, see next page.

Case Outline 3014A-D42IC
(unit:mm)



SANYO: DIP42

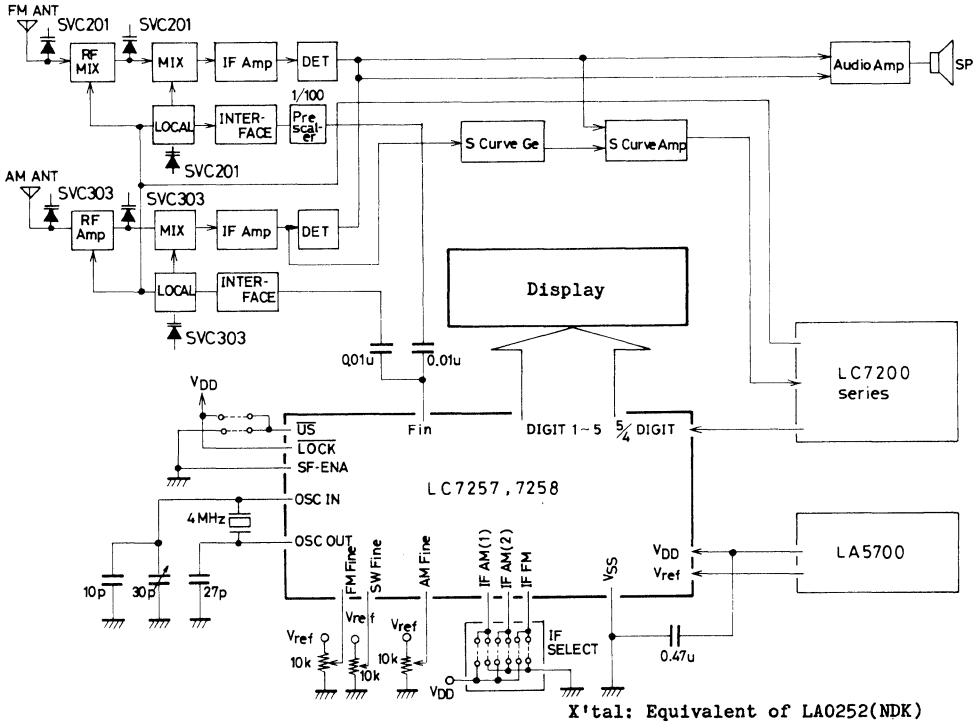
Related Products

· The following are Type Nos. belonging to digital frequency display LSI LC7250 series.

Function	LC7250	LC7253	LC7253G
Display	LED(anode common)	FLT	LED(cathode common)
Digits	4	5(5th digit:0or5)	5(5th digit:0or5)
Band	FM/MW/LW	FM/SW/MW/LW	FM/SW/MW/LW
Timepiece function	With	With	With

Function	LC7257	LC7257F	LC7258
Display	Red LED(cathode common)	Green LED(cathode common)	FLT
Digits	5(5th digit:0or5)	5(5th digit:0or5)	5(5th digit:0or5)
Band	FM/SW/MW/LW	FM/SW/MW/LW	FM/SW/MW/LW
Timepiece function	Without	Without	Without

1. LC7257, 7258 applied system block diagram

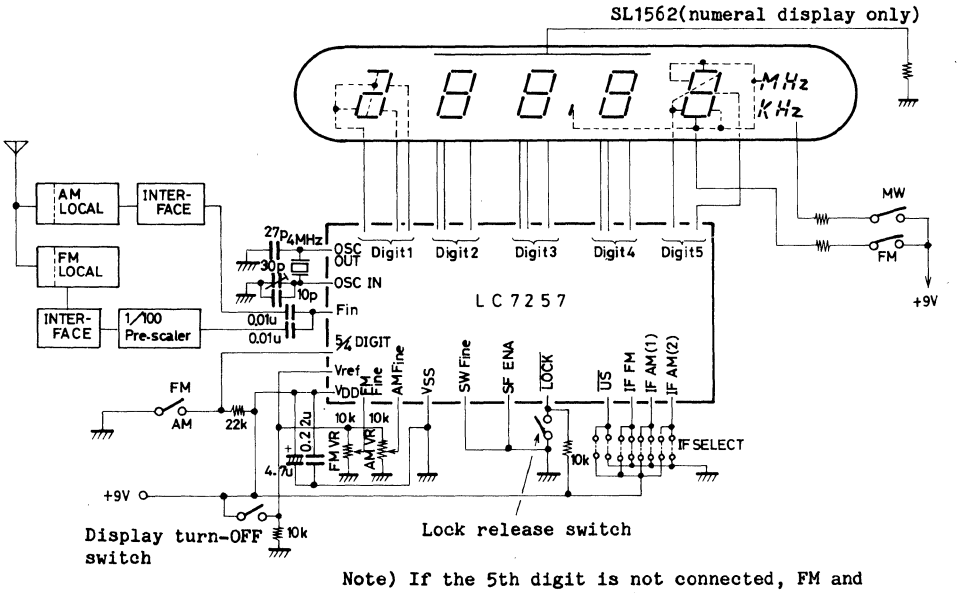


X'tal: Equivalent of LA0252(NDK)
FLT: Equivalent of 7LT-02[LC7258]
LED: Equivalent of SL1562[LC7257]

Band and digits	IF	5/4DIGIT	IF-FM	IF-AM(1)	IF-AM(2)
FM 5 digits	+10.7±0.14 MHz	[H]	[H]	[H], [L]	[L]
FM 5 digits	−10.7±0.14 MHz	[H]	[L]	[H], [L]	[L]
SW 5 digits	+446~+472 kHz	[H]	[H]	[H], [L]	[H]
SW 4 digits	+416~+472 kHz	[L]	[H]	[H], [L]	[H]
MW 4 digits	+455±2.8 kHz	[L]	[H], [L]	[L]	[L]
MW 4 digits	+469±2.8 kHz	[L]	[H], [L]	[H]	[L]
MW 4 digits	+450±2.8 kHz	[L]	[L]	[H], [L]	[H]

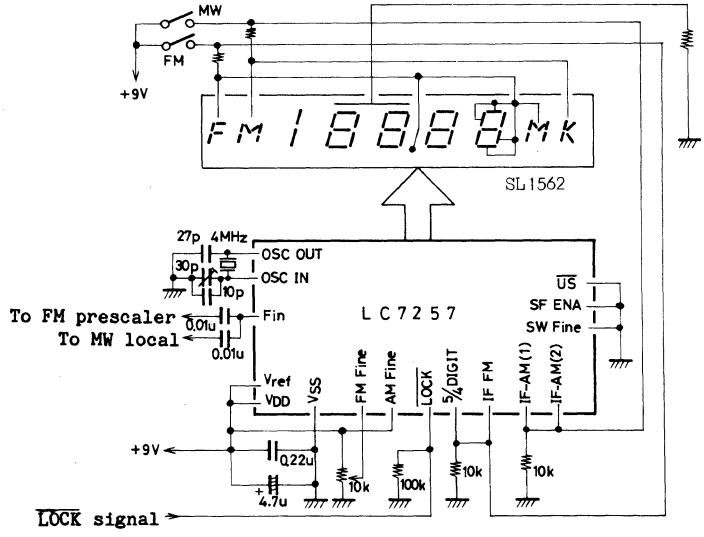
2. Sample application circuit

2-1) LC7257-applied red LED display (cathode common)
FM 5 digits, MW 4 digits (without SW display)



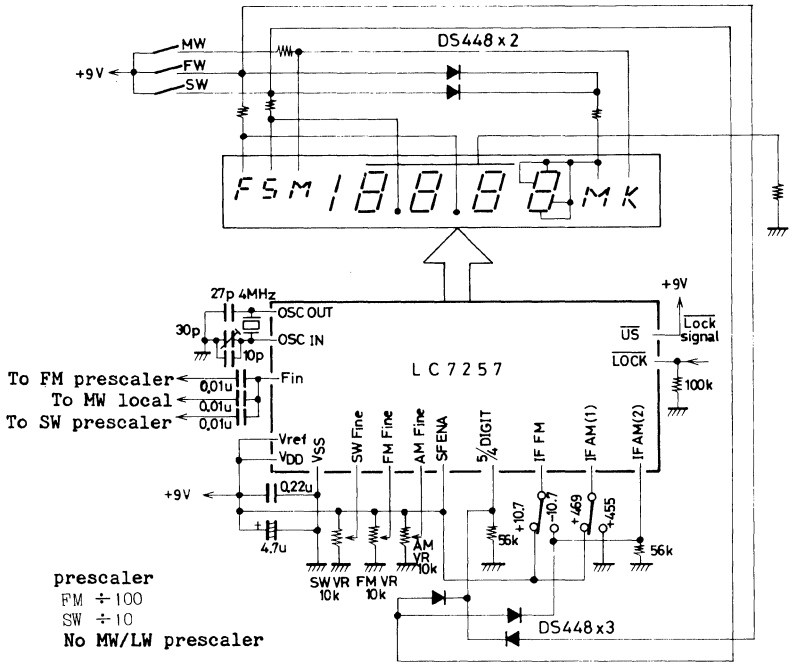
Note) If the 5th digit is not connected, FM and MW are displayed in 4 digits.
. SL1448, 1032, 1476-04

2-2) LC7257-applied red LED display (cathode common)
FM 5 digits, MW 4 digits (10kHz increment)

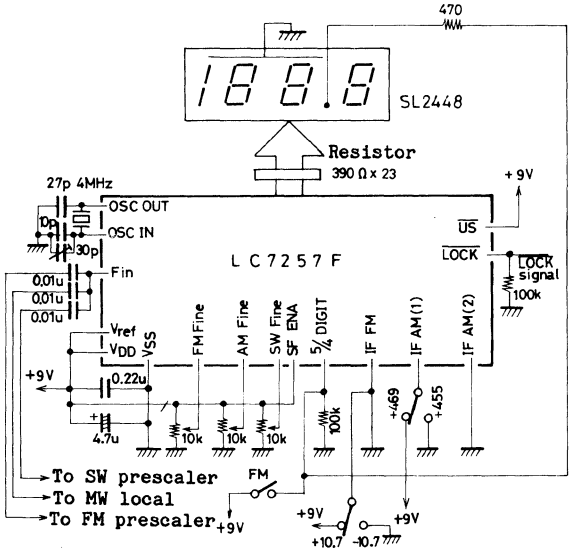


When lock is released,
V_{DD} level signal is applied.

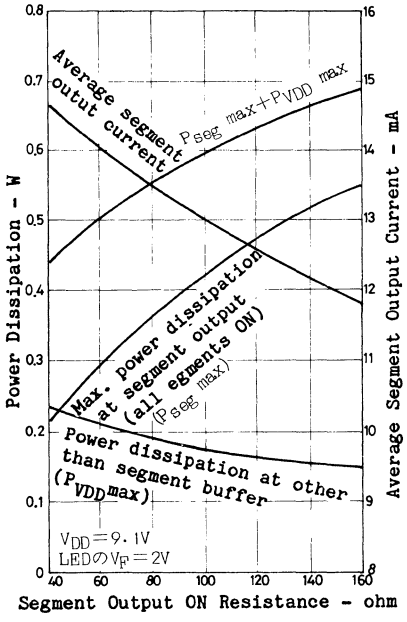
2-3) LC7257-applied red LED display (cathode common)
FM 5 digits, SW 5 digits MW 4 digits (1kHz increment)



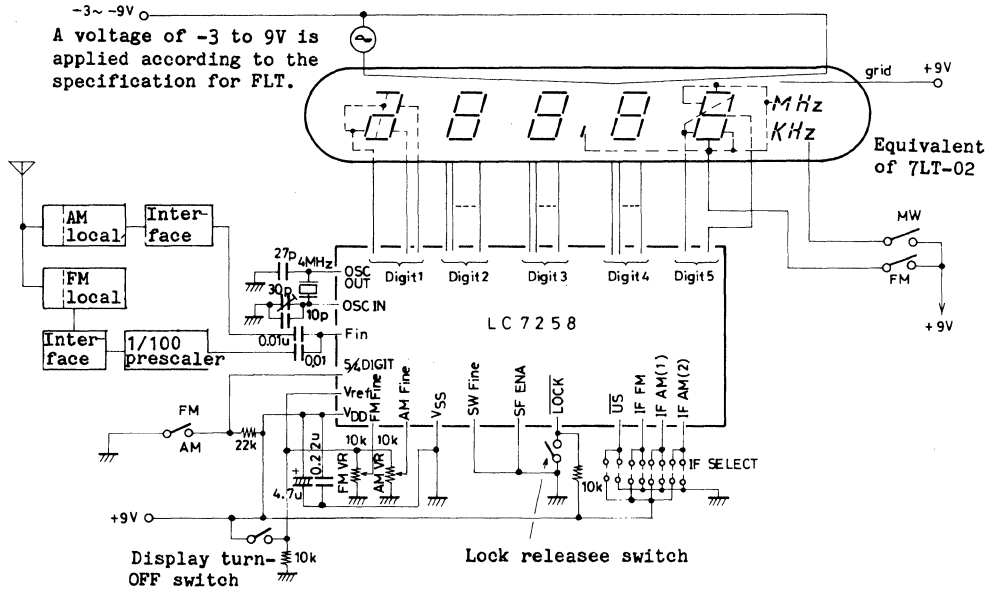
2-4) LC7257F-applied green LED display (cathode common)
FM 4 digits, MW 4 digits (1kHz) increment)



Segment current and power dissipation in the application circuit in 2-8)

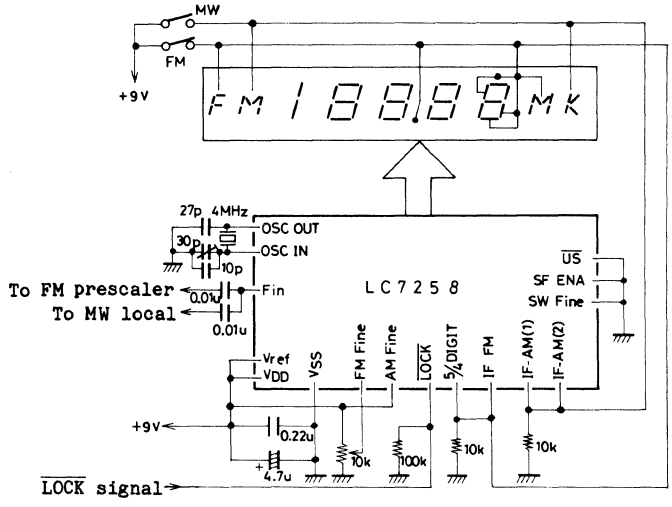


2-5) LC7258-applied FLT display
FM 5 digits, MW 4 digits (without SW display)



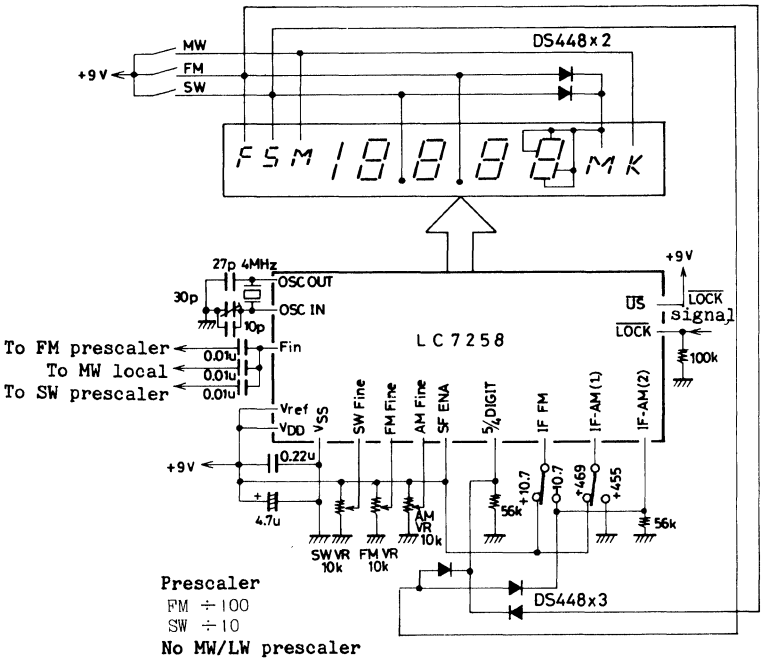
Note: If the 5th digit is not connected, FM and MW are displayed in 4 digits.

2-6) LC7258-applied FLT display
FM 5 digits, SW 5 digits, MW 4 digits (1kHz increment)

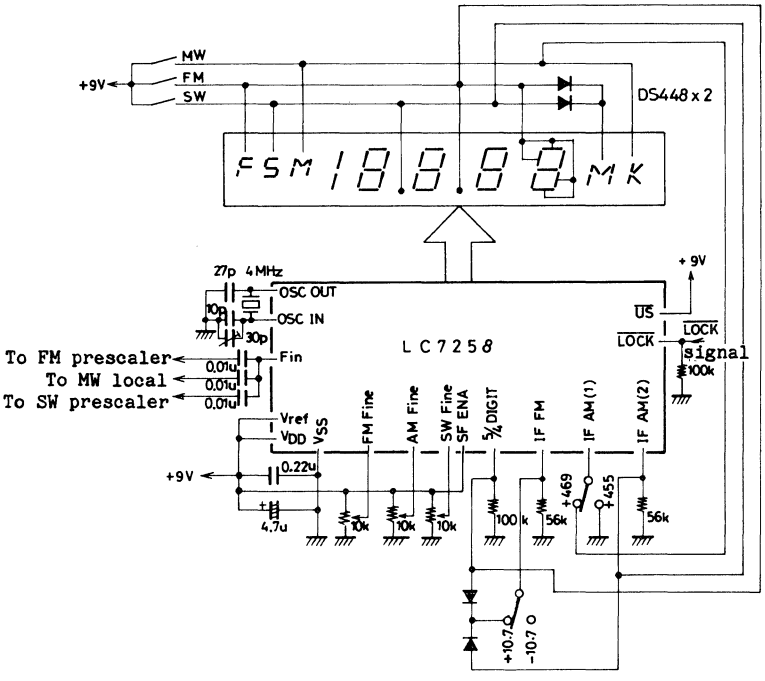


When lock is released, V_{DD} level signal is applied.

2-7) LC7258-applied FLT display
FM 5 digits, SW 5 digits, MW 4 digits (1kHz increment)



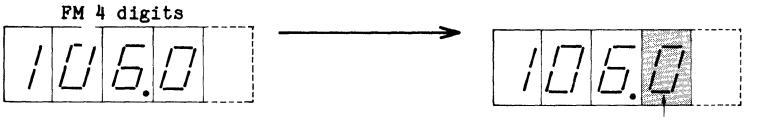
2-8) LC7258-applied FLT display
FM 5 digits, SW 4 digits, MW 4 digits (1kHz increment)



3. Sample display at each mode

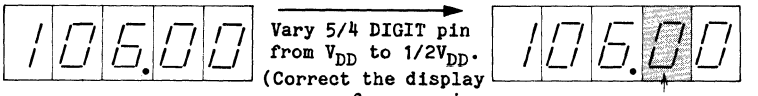
3-1) FM display: Display at 106kHz reception

FM 4 digits



Adjust FM-VR. The best condition for reception is where pin 5 for DIGIT 5 changes from "H" to "L".

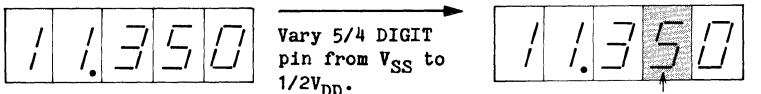
◇ FM 5 digits



Vary 5/4 DIGIT pin from V_{DD} to $1/2V_{DD}$. (Correct the display error of a ceramic filter used in a set.)

Flashing at a 10Hz rate if the display error is not corrected. Adjust FM-VR to stop flashing.

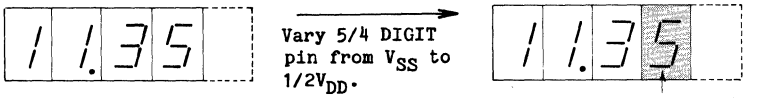
3-2) SW display: Display at 11350kHz reception



Vary 5/4 DIGIT pin from V_{SS} to $1/2V_{DD}$.

Flashing at a 10Hz rate if the display error is not corrected. Adjust SW-VR to stop flashing.

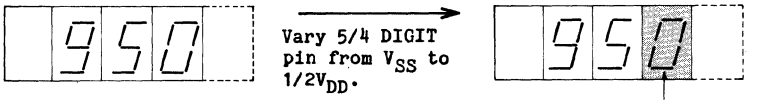
◇ SW 4 digits



Vary 5/4 DIGIT pin from V_{SS} to $1/2V_{DD}$.

Flashing at a 10Hz rate if the display error is not corrected. Adjust SW-VR to stop flashing.

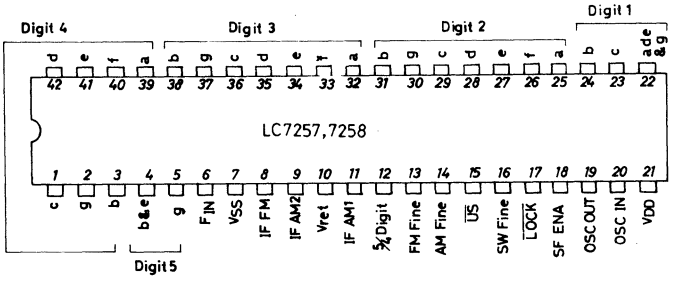
3-3) AM display: Display at 950kHz reception



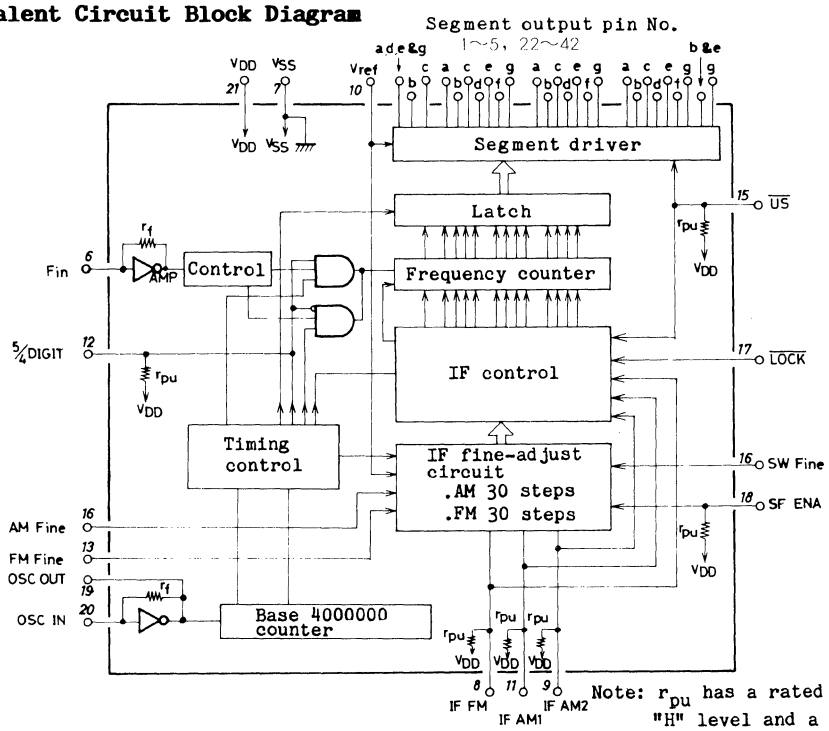
Vary 5/4 DIGIT pin from V_{SS} to $1/2V_{DD}$.

Flashing at a 10Hz rate if the display error is not corrected. Adjust AM-VR to stop flashing.

4. Pin Assignment



5. Equivalent Circuit Block Diagram

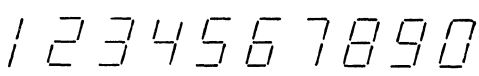


Note: r_{pu} has a rated resistance at "H" level and a high resistance at "L" level.

6. Display

6-1) Configuration and display font
4-1/2-digit, 7-segment FLT is used to display frequency in the display font shown below.

Display font



6-2) Lighting system
Static lighting

6-3) Display range (The highest-order digit "0" is blanked out.)
- Frequency (MW/LW)
  000kHz to 1999kHz
- Frequency (SW)
  4 digits: 0.00 to 29.99MHz
  5 digits: 0.000 to 29.995MHz
- Frequency (FM)
  00.0MHz to 199.9MHz

7. Input/Output Signal

7-1) Switch signal
- Logic "H" ---- V_{DD}
- Logic "M" ---- $1/2V_{DD}$ (Intermediate level between V_{DD} and V_{SS}).
- Logic "L" ---- V_{SS}

7-2) Fin pin input signal
- Amplitude ----0.5V or greater
- Fin pin input signal ----
  FM:2.0MHz or less (FM local oscillation frequency is 1/100-divided and inputted.)
  SW: 3.0MHz or less (SW local oscillation frequency is 1/10-divided and inputted.)
  MW/LW: 2.5MHz or less

7-3) Reference frequency
- Crystal of 4.000000MHz

7-4) Segment output
- P channel open drain

8. Pin Description

8-1) 5/4 DIGIT (FM/AM select) input pin
- Input pin for setting the frequency counter and frequency control to FM or AM use.
- "L" level ---- AM display or SW 4-digit display
- "H" level ---- FM display or SW 5-digit display

8-2) IF-FM (FM IF setting) input
- Input pin for specifying FM IF 5/4 DIGIT="H" level,IF-AM(2)="L" level
- IF: -10.7MHz, +10.7MHz
  "L" level ---- -10.7MHz
  "H" level ---- +10.7MHz

8-3)Setting of AM IF
- Setting of MW or LW

5/4 DIGIT	IF-FM	IF-AM (1)	IF-AM (2)	$\overline{US}$	IF	Increment of display
⌈L⌋	⌈H⌋⌈L⌋	⌈L⌋	⌈L⌋	⌈H⌋⌈L⌋	+455kHz	1kHz
⌈L⌋	⌈H⌋⌈L⌋	⌈H⌋	⌈L⌋	⌈H⌋⌈L⌋	+469kHz	1kHz
⌈L⌋	⌈L⌋	⌈H⌋⌈L⌋	⌈H⌋	⌈H⌋	+450kHz	1kHz
⌈L⌋	⌈L⌋	⌈H⌋⌈L⌋	⌈H⌋	⌈L⌋	+450kHz	10kHz

- Setting of SW

5/4 DIGIT	IF-FM	IF-AM (1)	IF-AM (2)	IF	Digits
⌈H⌋	⌈H⌋	⌈H⌋⌈L⌋	⌈H⌋	446 ~472kHz	5 digits
⌈L⌋	⌈H⌋	⌈H⌋⌈L⌋	⌈H⌋	416 ~472kHz	4 digits

8-4) FM-Fine (IF fine adjust) input
- Input pin for fine-correcting the display error of a receiving frequency by the ceramic filter for FM IF. Fine-adjust input pin for correcting the display error of a receiving frequency by the ceramic filter for IF at SF-ENA="L" when in 5-digit SW display mode.
- Input pin for applying a divided voltage by connecting a variable resistor across Vref and V_{SS}.

8-5) AM-Fine (IF fine adjust) input pin
- Input pin for fine-correcting the display error of a receiving frequency by the ceramic filter for AM IF. Fine-adjust input pin for correcting the display error of a receiving frequency by the ceramic filter for IF at SF-ENA="L" when in 4-digit SW display mode.
- Input pin for applying a divided voltage by connecting a variable resistor across Vref and V_{SS}.
- Fine-adjust range of FM-Fine,AM-Fine
  ◇FM
  28 steps settable with FM-Fine at a 10kHz/step rate between 10.60 MHz and 10.80MHz (±140kHz).
  ◇MW/LW
  28 steps settable with AM-Fine at ↗ a 0.2kHz/step rate centering on IF (±2.8kHz)
  ◇5-digit SW
  Settable with FM-Fine at a 1kHz/step rate between 446kHz and 472kHz.
  ◇4-digit SW
  Settable with AM-Fine at a 2kHz/step rate between 416kHz and 472kHz.
- SW-Fine
  Fine-adjust pin dedicated to SW
  Pin for fine-adjusting SW at SF-ENA ="H" level.
  Setting to SF-ENA="L" level permits SW fine-adjustment with FM-Fine, AM-Fine pin.

8-6) SF-ENA pin
- Refer to 8-5) SW-Fine above.

8-7) Fin (frequency) input pin
- Input pin for applying input of FM local OSC frequency divided to 1/100 for FM display, input of SW local OSC frequency divided to 1/10 for SW display, and input of MW local OSC frequency for MW display.
- Input signal with an inut voltage of 0.5Vp-p or greater (Sinusoidal wave is also acceptable. Rectangular wave : Duty 50%)
- Maximum frequency
  2.5MHz V_{DD}=6 to 10V
  3.0MHz V_{DD}=7 to 10V

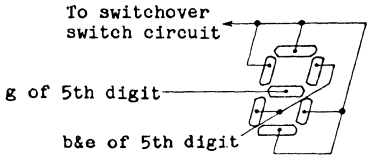
8-8) $\overline{US}$ pin
- Pin for providing 10kHz-increment frequency display at MW/LW mode.
- By setting $\overline{US}$ pin to "L" level when IF is 450kHz (5/4DIGIT=IF-FM="L", IF-AM (1)="H" or "L", IF-AM(2)="H"), 10kHz-increment display is provided. In this case, the frequency fine-adjust function is not operated, with the kHz digit rounded off to the nearest whole number.

8-9) $\overline{LOCK}$ pin
- When $\overline{LOCK}$ pin is set to "L" level, the display contents are locked regardless of the input frequency.(Lock function)
- When $\overline{LOCK}$ pin is set to "H" level, the lock function is released and the normal frequency counting operation is performed.

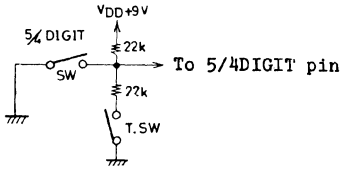
8-10) OSC IN, OSC OUT (crystal oscillation)
- Input/output pin for crystal oscillation.
- Input/output pin for connecting a crystal (4.000000MHz).

8-11) Vref pin (also used for inhibit function)
- "H" level ---- Normal operation
- "L" level ---- Segment pin OFF

8-12) Connection method of 5th digit
- The 5th digit is displayed only when 5/4DIGIT="H".



9. **Fine Adjustment of Freuency Display Error** (Refer to 2-1).
- 5/4DIGIT pin is set to "M" level.



The operating procedure is shown below.

9-1) FM frequency (5 digits) display (Refer to page 5.)

	Item	5/4DIGIT,SW	T.SW
a	Set the display mode to the FM display.	off	off
b	For example, receive 80.00MHz and apply FM local OSC frequency divided to 1/100 to Fin pin.	off	off
c	Set 5/4DIGIT pin to $1/2V_{DD}$.	off	on
d	Adjust FM-VR so that 80.00 is displayed and the 4th digit stops flashing.	off	on
e	Set 5/4DIGIT pin to V_{DD}.	off	off
f	This completes adjustment.		

9-2) AM frequency (MW 4 digits) display (Refer to page 5.)

	Item	5/4DIGIT,SW	T.SW
a	Set the display mode to the AM display.	on	off
b	For example, receive 950kHz and apply AM local OSC frequency divided to 1/100 to Fin pin.	on	off
c	Set 5/4DIGIT pin to $1/2V_{DD}$.	on off	on ← This mode must be passed through. on
d	Adjust AM-VR so that 950 is displayed and the 4th digit stops flashing.	off	on
e	Set 5/4DIGIT pin to V_{SS}.	on	off
f	This completes adjustment.		

9-3) Other cases

Besides the example of Fig. in 2-1), 4-digit FM, 5-digit SW, and 4-digit SW are described below.

.a) 4-digit FM

For 9-1) b), the point at which 80.0 isdisplayed by adjusting FM-VR and segment g of digit 5 is changed from "L" to "H" is the optimum.

.b) 5-digit SW (Refer to 2-3).)

The procedure in 9-1) is followed. Apply SW local OSC frequency to Fin pin and adjut SW-VR.

.c) 4-digit SW (Refer to 2-4).)

The same procedure as for 9-3) a) is followed. Apply SW local OSC frequency to Fin pin and adjust SW-VR.

Note) Operation during fine adjustment

In the 5-digit FM display mode, 0 is displayed when the 5th digit counter is at 0 to 4; 5 is displayed when at 5 to 9.

In case of performing fine adjustment by changing 5/4DIGIT pin from V_{DD} to $1/2V_{DD}$, flashing stops when the 5th digit is 2 or 7; flashing at a 10Hz rate occurs when the 5th digit is other than 2 or 7.

The same also holds true for 5-digit SW.

In the 4-digit AM display mode, the 5th digit is discarded.

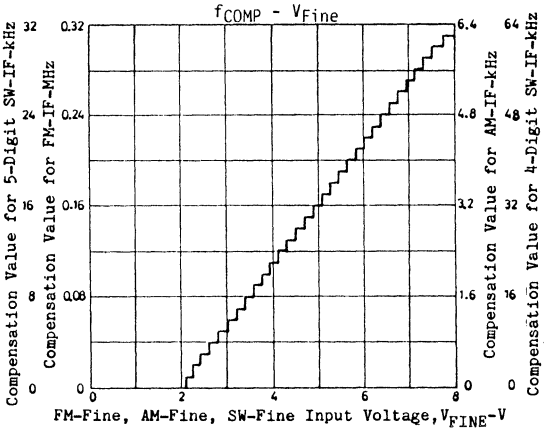
In case of performing fine adjustment by changing 5/4DIGIT pin from V_{SS} to $1/2V_{DD}$, flashing stops when the 5th digit is 4 or 5, flashing stops; flashing at a 10Hz rate occurs when the 5th digit is other than 4 or 5. Therefore, in 9-2) above, 950 display is given at 950kHz±400Hz of receiving frequency.

9-4) Internal operation for compensating frequency display error
- FM-Fine, AM-Fine, SW-Fine pins are used to compensate IF offset.

When Vref is 8V, 31-step compensation is available in the V_{Fine} range of more than 2V up to 8V. For example, when a voltage of 0 to 2V is applied to FM-Fine in the FM mode, IF is not compensated. However,when a voltage more than 2V is applied to FM-Fine, 31-step compensation is available in increments of 0.01MHz according to the voltage applied to FM-Fine (ex. 0.08MHz for

6.5V, ----, 0.31MHz for 8V). When FM-IF is exactly +10.7MHz, the compensation value is 0.16MHz.

Note: (Refer to f_{COMP} vs. V_{Fine} on next page.)



10. Main Specifications

10-1) LC7257

Absolute Maximum Ratings at Ta=25°C, Vss=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +11	V
Reference Voltage	Vref	Vref≦V_{DD}	-0.3 to +11	V
Input Voltage	Vi		-0.3 to V_{DD}+0.3	V
Output Voltage	Vo	Output off	-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta≦70°C	900	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V, V_{DD}=6.0 to 10.0V, Vref=6.0 to 10.0V, Vref≦V_{DD}

			min	typ	max	unit
Supply Voltage	V_{DD}		6.0		10.0	V
Reference Voltage	Vref(1)	Display ON 0.8V_{DD}≦Vref≦V_{DD}	6.0		10.0	V
	Vref(2)	Display OFF	0		0.12V_{DD}	V
"H"-Level Input Voltage	V_{IH}	5/4DIGIT, $\overline{LOCK}$, IF-FM, $\overline{US}$, IF-AM(1), IF-AM(2), SF-ENA	0.85V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL}	" "	0		0.12V_{DD}	V
Input Freqeuncy	f_I(1)	FIN, V_{PP}≧0.5V, duty 50%, V_{DD}=7 to 10V	0.5		3.0	MHz
	f_I(2)	FIN, V_{PP}≧0.5V, duty 50%, V_{DD}=6 to 7V	0.5		2.5	MHz
Operating Frequency	fopg	OSC-IN, OSC-OUT, 4MHz, External X'tal	3.5		4.2	MHz
Input Amplitude	V_{PP}	Fin(0.47uF ceramic capacitor across V_{DD} and V_{SS})	0.5			Vp-p

Electrical Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=8 to 10V, Vref=8 to 10V, Vref≦V_{DD}

			min	typ	max	unit
Input Current	I_{IN}	FM-Fine, AM-Fine, SW-Fine, v_i=0V or Vref	-1		1	uA
"H"-Level Input Current	$I_{IH(1)}$	$\overline{IF}$-FM, IF-AM(1), IF-AM(2), $\overline{US}$, SF-ENA, v_i=0.9V_{DD}	-80	-30	-10	uA

			min	typ	max	unit
"L"-Level Input Current	$I_{IL(1)}$	IF-FM,IF-AM(1),IF-AM(2), $\overline{LOCK}$,$\overline{US}$,SF-ENA,v_i=0V	-3		0	uA
"H"-Level Input Current	$I_{IH(2)}$	5/4DIGIT,v_i=0.9V_{DD}	-40	-15	-5	uA
"L"-Level Input Current	$I_{IL(2)}$	5/4DIGIT,v_i=0V	-3		0	uA
"H"-Level Input Current	$I_{IH(3)}$	$\overline{LOCK}$,v_i=V_{DD}	0		3	uA
Feedback Resistance	$r_f(1)$	Feedback resistance between OSC-IN and OSC-OUT		3		Mohm
	$r_f(2)$	Feedback resistance of Fin		3		Mohm
"H"-Level Output Voltage	$V_{OH}(1)$	a,d,e,b,g,V_{DD}=8.0V, I_{OH}=-32mA	V_{DD}-1.8			V
	$V_{OH}(2)$	b & e,V_{DD}=8.0V, I_{OH}=-16mA	V_{DD}-1.8			V
	$V_{OH}(3)$	Segment output pins other than above,V_{DD}=8.0V,I_{OH}=-8mA	V_{DD}-1.8			V
Output Leak Current	I_{OFF}	All segment output pins V_{DD}=10V,V_{OUT}=0V	-10		0	uA
Current Dissipation	$I_{DD}(1)$	V_{DD}=10V,$f_I(1)$=3MHz(0.5Vp-p) fopg=4MHz(crystal mounted)		8	17	mA
	Iref	V_{DD}=10V,Vref=10V,AM-Fine=FM-Fine=Vref		0.6	1.5	mA

(Note) Current direction: +: Flowing into LSI, -: Flowing out of LSI

10-2) LC7257F

Absolute Maximum Ratings at Ta=25°C,V_{SS}=0V,a,d,e&g must not be used.

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +11	V
Reference Voltage	Vref	Vref≦V_{DD}	-0.3 to +11	V
Input Voltage	v_i		-0.3 to V_{DD}+0.3	V
Output Voltage	v_o	Output off	-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta≦+65°C	1000	mW
Allowable Power Dissipation of Segment Output	$P_{d(seg)}$	b & e I_{OL}<32mA	64	mW
		other than b&e I_{OL}<16mA	32	mW
Operating Temperature	Topg		-30 to +65	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C,V_{SS}=0V,V_{DD}=8 to 10V,Vref=8 to 10V, Vref≦V_{DD}

			min	typ	max	unit
Supply Voltage	V_{DD}		8.0		10.0	V
Reference Voltage	Vref(1)	Display ON 0.8V_{DD}≦Vref≦V_{DD}	8.0		10.0	V
	Vref(2)	Display OFF	0		0.12V_{DD}	V
"H"-Level Input Voltage	V_{IH}	5/4DIGIT,$\overline{LOCK}$,IF-FM,$\overline{US}$, IF-AM(1),IF-AM(2),SF-ENA	0.85V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL}	" "	0		0.12V_{DD}	V
Input Freqeuncy	$f_I(1)$	FIN,V_{PP}≧0.5V,duty 50%	0.5		3.0	MHz
	$f_I(2)$	FIN,V_{PP}≧0.5V,duty 50%	0.5		2.5	MHz
Operating Frequency	fopg	OSC-IN,OSC-OUT,4MHz, External X'tal	3.5		4.2	MHz
Input Amplitude	V_{PP}	Fin(0.47uF ceramic capacitor across V_{DD} and V_{SS})	0.5			Vp-p

Electrical Characteristics at Ta=25°C,V_{SS}=0V,V_{DD}=8 to 10V,Vref=8 to 10V,Vref≦V_{DD}

			min	typ	max	unit
Input Current	I_{IN}	FM-Fine,AM-Fine,SW-Fine, v_i=0V or Vref	-1		1	uA

			min	typ	max	unit
"H"-Level Input Current	$I_{IH(1)}$	IF-FM,IF-AM(1),IF-AM(2), $\overline{US}$,SF-ENA,v_i=0.9V_{DD}	-80	-30	-10	uA
"L"-Level Input Current	$I_{IL(1)}$	IF-FM,IF-AM(1),IF-AM(2), $\overline{LOCK}$,$\overline{US}$,SF-ENA,v_i=0V	-3		0	uA
"H"-Level Input Current	$I_{IH(2)}$	5/4DIGIT,v_i=0.9V_{DD}	-40	-15	-5	uA
"H"-Level Input Current	$I_{IH(3)}$	$\overline{LOCK}$,v_i=V_{DD}	0		3	uA
"L"-Level Input Current	$I_{IL(2)}$	5/4DIGIT,v_i=0V	-3		0	uA
Feedback Resistance	$r_f(1)$	Feedback resistance between OSC-IN and OSC-OUT		3		Mohm
	$r_f(2)$	Feedback resistance of Fin		3		Mohm
"H"-Level Output Voltage	$V_{OH}(1)$	b&e,V_{DD}=8.0V, I_{OH}=-24mA	V_{DD}-1.8			V
	$V_{OH}(2)$	Segment output pins other than above,V_{DD}=8.0V,I_{OH}=-12mA	V_{DD}-1.8			V
	$V_{OH}(3)$	b & e,V_{DD}=8.0V,I_{OH}=-24mA, when current flows into all segment outputs	V_{DD}-2.8			V
	$V_{OH}(4)$	Segment output pins other than above,v_{DD}=8.0V,I_{OH}= -12mA,when current flows into all segment outputs	V_{DD}-2.8			V
Output Leak Current	I_{OFF}	All segment output pins V_{DD}=10V,V_{OUT}=0V	-10		0	uA
Current Dissipation	I_{DD}	V_{DD}=10V,$f_I(1)$=3MHz(0.5Vp-p) fopg=4MHz(crystal mounted)		8	17	mA
	Iref	V_{DD}=10V,Vref=10V,AM-Fine= FM-Fine=Vref		0.6	1.5	mA

(Note) Current direction: +: Flowing into LSI, -: Flowing out of LSI

10-3) LC7258

Absolute Maximum Ratings at Ta=25°C,Vss=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +11	V
Reference Voltage	Vref	Vref≦V_{DD}	-0.3 to +11	V
Input Voltage	Vi		-0.3 to V_{DD}+0.3	V
Output Voltage	Vo	Output off	-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta≦70°C	400	mW
Allowable Power Dissipation of Segment Output	Pd(seg)max	a,d,e&g: I_{OH} <12mA	14	mW
		b&e: I_{OH} <6mA	7	mW
		Other than above I_{OH} <3mA	3.5	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C,V_{SS}=0V,V_{DD}=6.0 to 10.0V,Vref=6.0 to 10.0V, Vref≦V_{DD}

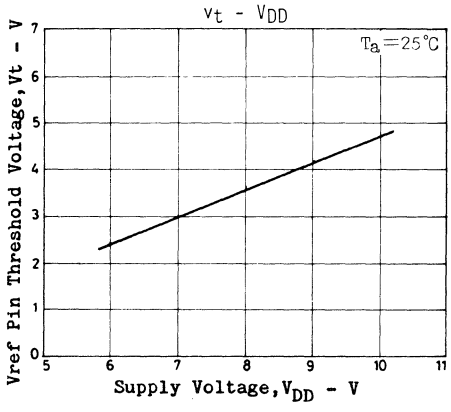
			min	typ	max	unit
Supply Voltage	V_{DD}		6.0		10.0	V
Reference Voltage	Vref(1)	Display ON 0.8V_{DD}≦Vref≦V_{DD}	6.0		10.0	V
	Vref(2)	Display OFF	0		0.12V_{DD}	V
"H"-Level Input Voltage	V_{IH}	5/4DIGIT,LOCK,IF-FM,US, IF-AM(1),IF-AM(2),SF-ENA	0.85V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL}	" "	0		0.12V_{DD}	V
Input Freqeuncy	$f_I(1)$	FIN,V_{PP}≧0.5V,duty 50%, V_{DD}=7 to 10V	0.5		3.0	MHz
	$f_I(2)$	FIN,V_{PP}≧0.5V,duty 50%, V_{DD}=6 to 7V	0.5		2.5	MHz

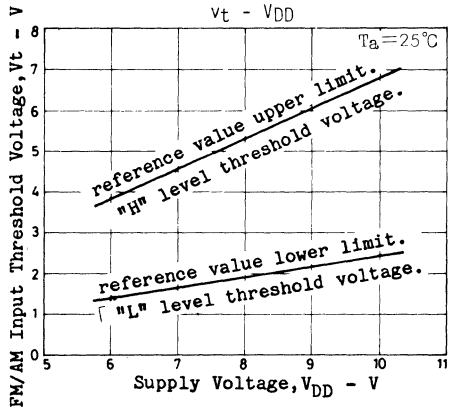
			min	typ	max	unit
Operating Frequency	fopg	OSC-IN,OSC-OUT,4MHz, External X'tal	3.5		4.2	MHz
Input Amplitude	V_{PP}	Fin(0.47uF ceramic capacitor across V_{DD} and V_{SS})	0.5			Vp-p

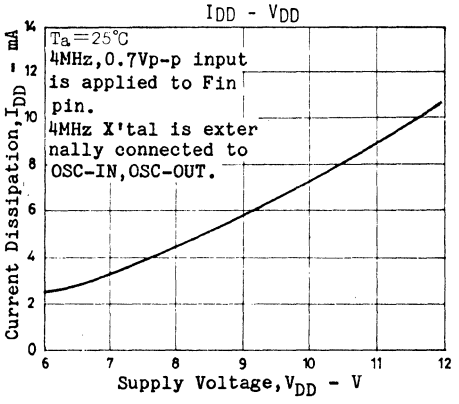
Electrical Characteristics at Ta=25°C,V_{SS}=0V,V_{DD}=8 to 10V,Vref=8 to 10V,Vref≦V_{DD}

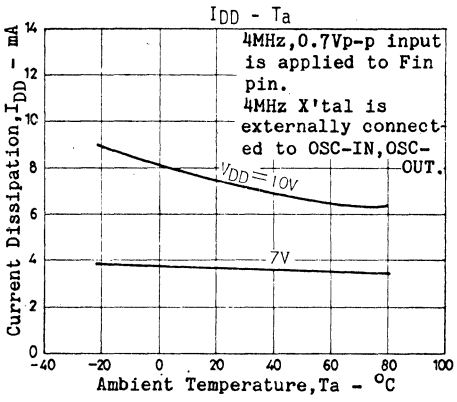
			min	typ	max	unit
Input Current	I_{IN}	FM-Fine,AM-Fine,SW-Fine, v_i=0V or Vref	-1		1	uA
"H"-Level Input Current	$I_{IH(1)}$	$\overline{IF}$-FM,IF-AM(1),IF-AM(2), $\overline{US}$,SF-ENA,v_i=0.9V_{DD},$\overline{LOCK}$	-80	-30	-10	uA
"L"-Level Input Current	$I_{IL(1)}$	IF-FM,IF-AM(1),IF-AM(2), $\overline{LOCK}$,$\overline{US}$,SF-ENA,v_i=0V	-3		0	uA
"H"-Level Input Current	$I_{IH(2)}$	5/4DIGIT,v_i=0.9V_{DD}	-40	-15	-5	uA
"L"-Level Input Current	$I_{IL(2)}$	5/4DIGIT,v_i=0V	-3		0	uA
Feedback Resistance	$r_f(1)$	Feedback resistance between OSC-IN and OSC-OUT		3		Mohm
	$r_f(2)$	Feedback resistance of Fin		3		Mohm
"H"-Level Output Voltage	$V_{OH}(1)$	a,d,e,b,g,V_{DD}=8.0V, I_{OH}=-2mA	V_{DD}-1			V
	$V_{OH}(2)$	b & e,V_{DD}=8.0V, I_{OH}=-1mA	V_{DD}-1			V
	$V_{OH}(3)$	Segment output pins other than above,V_{DD}=8.0V,I_{OH}=-0.5mA	V_{DD}-1			V
Output Leak Current	I_{OFF}	All segment output pins V_{DD}=10V,V_{OUT}=-8V	-3		0	uA
Current Dissipation	I_{DD}	V_{DD}=10V,$f_I(1)$=3MHz(0.5Vp-p) fopg=4MHz(crystal mounted)		8	17	mA
	Iref	V_{DD}=10V,Vref=10V,AM-Fine= FM-Fine=Vref		0.6	1.5	mA

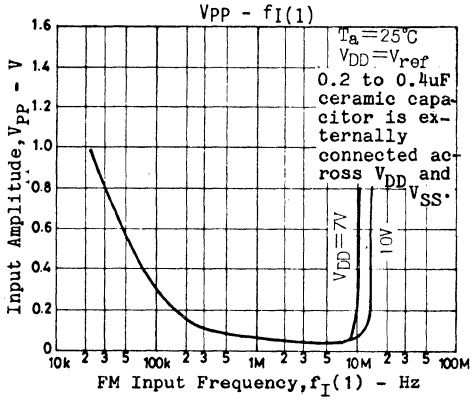
(Note) Current direction: +: Flowing into LSI, -: Flowing out of LSI

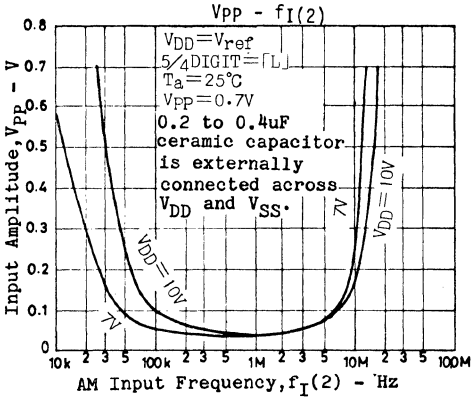


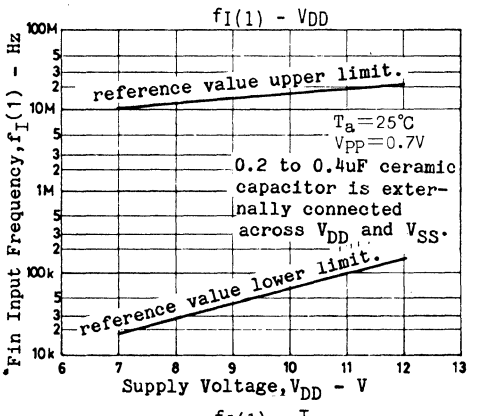


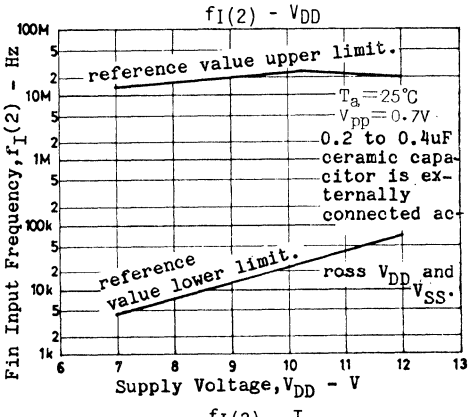

IDD - VDD
Ta=25°C
4MHz,0.7Vp-p input is applied to Fin pin.
4MHz X'tal is externally connected to OSC-IN,OSC-OUT.
Current Dissipation,IDD - mA
Supply Voltage,VDD - V

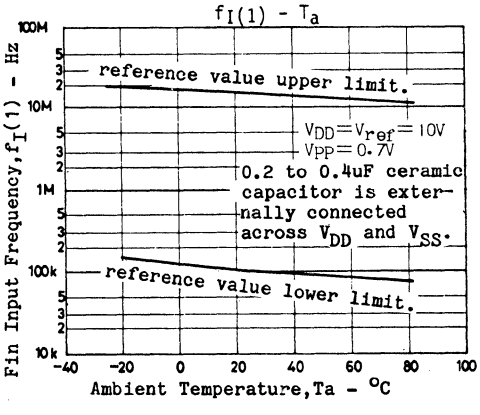

IDD - Ta
4MHz,0.7Vp-p input is applied to Fin pin.
4MHz X'tal is externally connected to OSC-IN,OSC-OUT.
VDD=10V
7V
Current Dissipation,IDD - mA
Ambient Temperature,Ta - °C

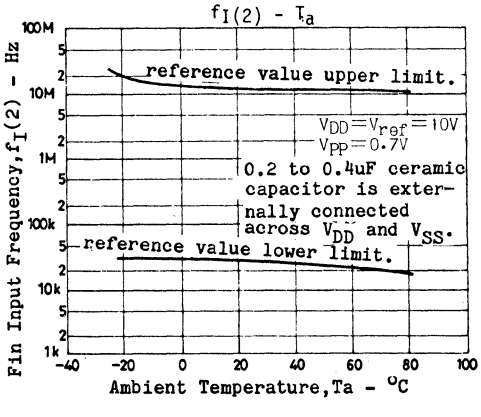

VPP - fI(1)
Ta=25°C
VDD=Vref
0.2 to 0.4uF ceramic capacitor is externally connected across VDD and VSS.
VDD=7V
10V
Input Amplitude,VPP - V
FM Input Frequency,fI(1) - Hz

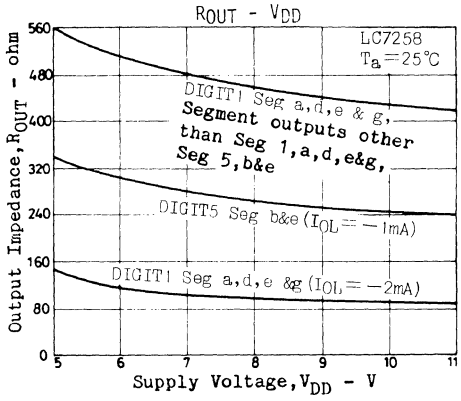

VPP - fI(2)
VDD=Vref
5/4DIGIT=⌈L⌋
Ta=25°C
VPP=0.7V
0.2 to 0.4uF ceramic capacitor is externally connected across VDD and VSS.
VDD=10V
7V
Input Amplitude,VPP - V
AM Input Frequency,fI(2) - Hz

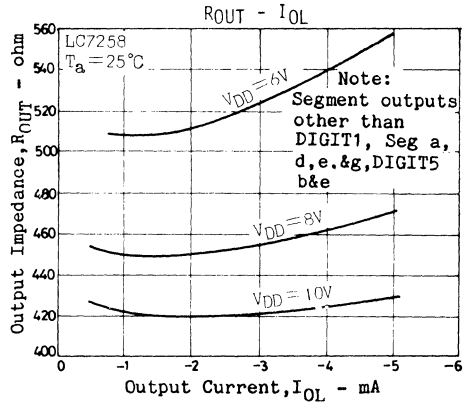

fI(1) - VDD
reference value upper limit.
Ta=25°C
VPP=0.7V
0.2 to 0.4uF ceramic capacitor is externally connected across VDD and VSS.
reference value lower limit.
Fin Input Frequency,fI(1) - Hz
Supply Voltage,VDD - V

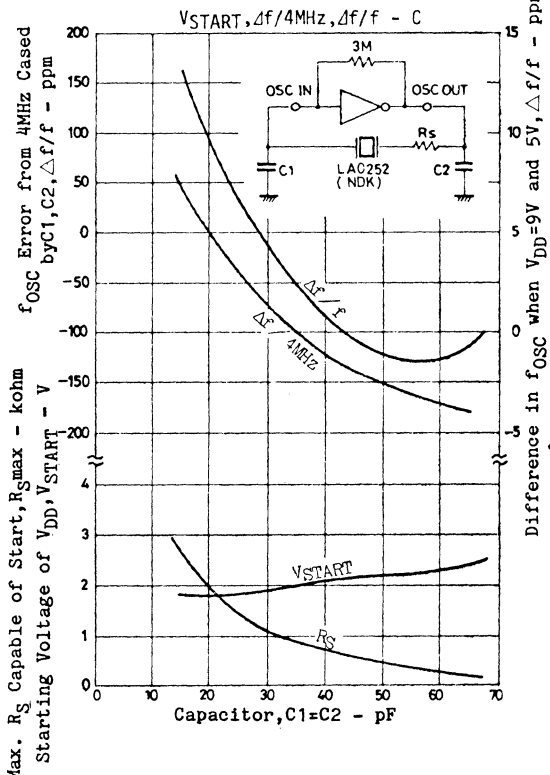

fI(2) - VDD
reference value upper limit.
Ta=25°C
VPP=0.7V
0.2 to 0.4uF ceramic capacitor is externally connected across VDD and VSS.
reference value lower limit.
Fin Input Frequency,fI(2) - Hz
Supply Voltage,VDD - V


fI(1) - Ta
reference value upper limit.
VDD=Vref=10V
VPP=0.7V
0.2 to 0.4uF ceramic capacitor is externally connected across VDD and VSS.
reference value lower limit.
Fin Input Frequency,fI(1) - Hz
Ambient Temperature,Ta - °C

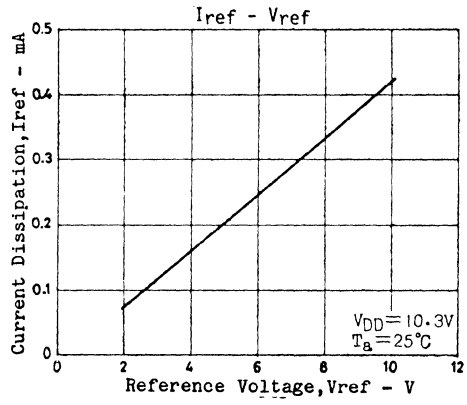

fI(2) - Ta
reference value upper limit.
VDD=Vref=10V
VPP=0.7V
0.2 to 0.4uF ceramic capacitor is externally connected across VDD and VSS.
reference value lower limit.
Fin Input Frequency,fI(2) - Hz
Ambient Temperature,Ta - °C







Note) $\Delta f/f$, V_{START}, $\Delta f/4MHz$: $R_B = 0\Omega$

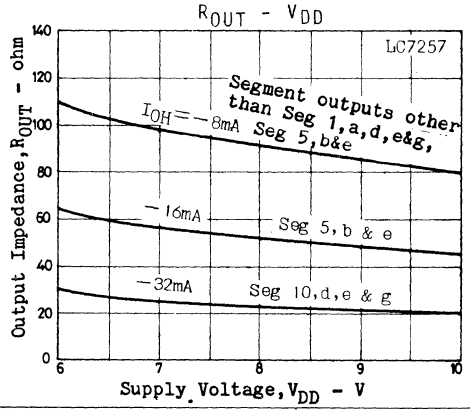


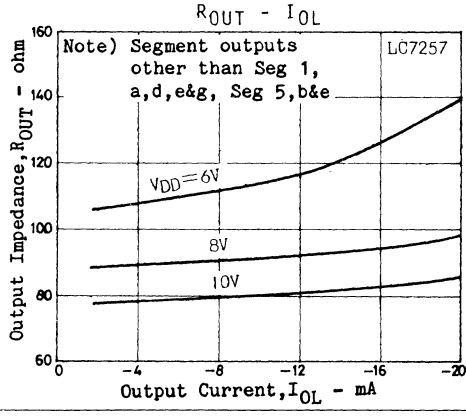
← Desgin Notes

view of voltage reduced characteristic (f/f).

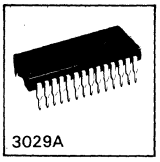
small as possible in view of oscillation stability.

the two points mentioned above. C1 C2 include the stray capacitance of the substrate. In actual applications, it is recommended to use a ceramic capacitor of 10pF and a trimmer capacitor of 30pF for C1 and a ceramic capacitor of 27pF for C2. It is desirable to use ceramic capacitors having a temperature characteristic of 0ppm.





LC7265, 7266



C MOS LSI

Received Frequency Display for Radio Receivers

Ⓔ 1197B

The LC7265 (for use in LED display applications), LC7266 (for use in fluorescent display tube display applications) are ICs designed to count the local oscillation frequency of each band of FM, MW, LW and to display the received frequency.

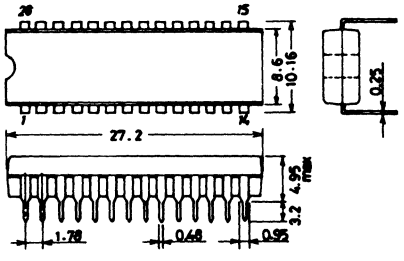
Applications

Displays received frequency in radio receivers.

Features

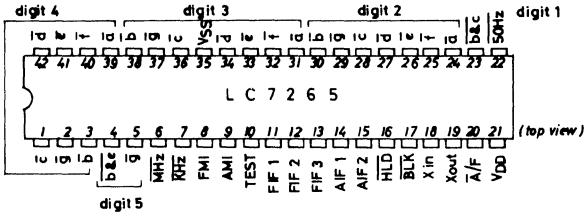
(1) Displays received frequency of each band of FM, MW, LW
LC7265 : LED static display
LC7266 : FL static display
(2) Counts local oscillation frequency and displays received frequency.
(3) Number of display digits : FM - 5 digits, MW - 4 digits, LW - 3 digits.
(4) Covers intermediate frequencies shown below.
FM : +10.700, +10.725, +10.750, +10.675 MHz
-10.700, -10.725, -10.675, -10.650 MHz
MW,LW : +450kHz ----- 10kHz Step display
+450kHz ----- 1kHz Step display
+455kHz ----- 1kHz Step display
+469kHz ----- 1kHz Step display
(5) Contains blanking circuit to turn off display.
(6) Contains hold circuit to hold display contents.
(7) Uses crystal resonator having 7.2MHz reference frequency.
(8) Uses LB3500 (÷8 prescaler) jointly at the time of FM reception.
(9) Supply voltage V_{DD} : 4.5V to 10V
(10) Package : DIP42S

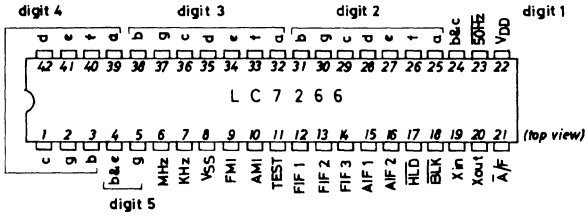
Case Outline 3029A-D28SIC
(unit:mm)



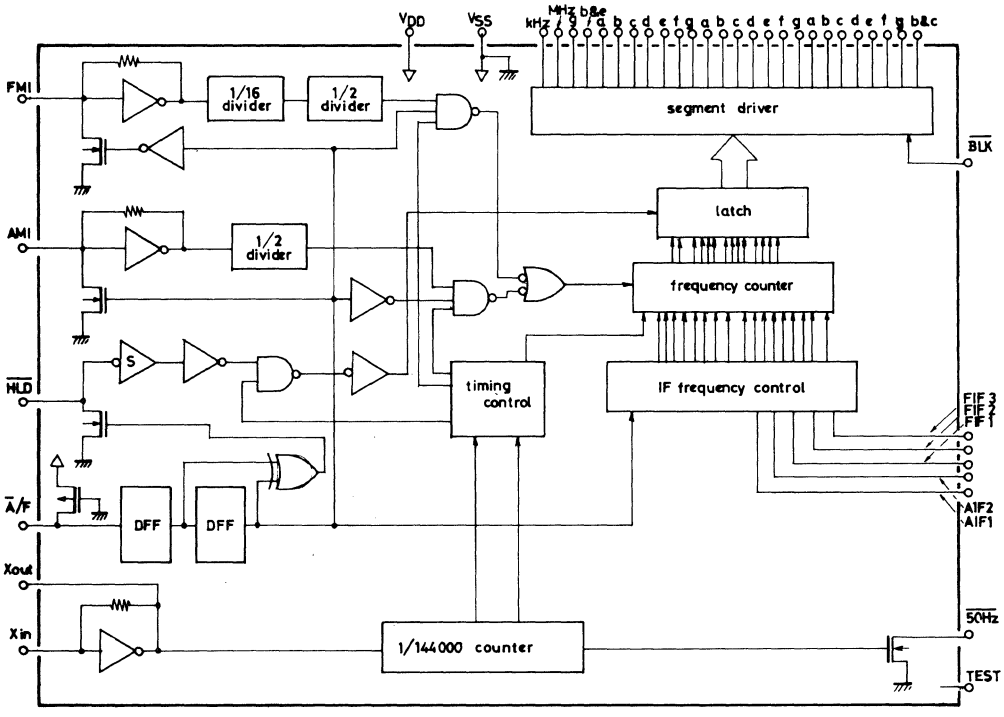
SANYO: DIP28S

Pin Assignment





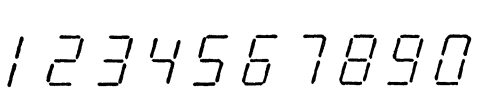
Equivalent Circuit Block Diagram (LC7266)



Note) For the LC7265, attach - (bar) to output segment symbols..

1. Display

(1) Display font



(2) Lighting system
Static lighting

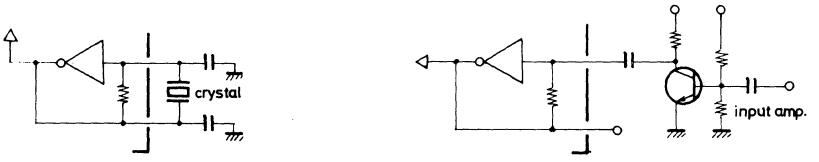
(3) Display range (High-order 1 digit : zero blanking)
FM ----- 00.00MHz to 199.95MHz 50kHz step
MW.LW ----- 000kHz to 1999kHz 10kHz or 1kHz step

2. Pin Description

(1) $\overline{a}$ to $\overline{g}$,$\overline{b\&c}$,$\overline{b\&e}$,$\overline{MHz}$,$\overline{kHz}$ ----- LED(LC7265)
a to g,b&c,b&e,MHz,kHz ----- FL (LC7266)

(2) V_{DD},V_{SS} ----- Power supply pins

(3) X_{IN},X_{OUT} ----- Crystal resonator or input amp. pin



(4) FIF(1),FIF(2),FIF(3) ----- FM IF select pins

FIF(1)	0	0	0	0	1	1	1	1
FIF(2)	0	0	1	1	0	0	1	1
FIF(3)	0	1	0	1	0	1	0	1
IF(MHz)	+10.700	+10.725	+10.675	+10.750	-10.700	-10.725	-10.675	-10.650

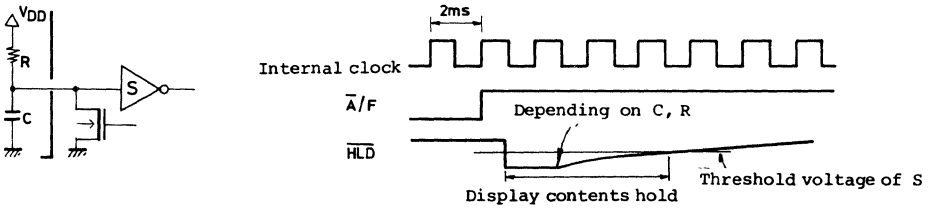
(5) AIF(1),AIF(2) ----- AM IF select pins

AIF(1)	0	0	1	1
AIF(2)	0	1	0	1
IF(kHz)	+450(2)	+450(1)	+455	+469

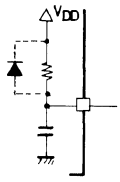
1 : High level (V_{DD})
0 : Low level (V_{SS})

(Note) 450kHz(1) : 10kHz step display
Others : 1kHz step display

(6) $\overline{HLD}$ -----Display contents hold pin
Normally, this pin is set at high level. To hold display contents, this pin is set at low level. Connecting time constant circuit to this pin makes it possible to hold display contents for a certain period of time at the time of FM/MW.LW band selection.



(7) $\overline{BLK}$ ------ Display blanking pin

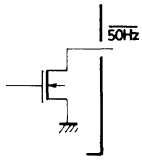


Example of blanking misdisplay at the time of application of power.

(8) FMI,AMI ----- Local oscillation signal input pins
FMI ----- For FM, 0.7Vp-p input sensitivity
AMI ----- For MW, LW, 1.0Vp-p input sensitivity (V_{DD}=8 to 10V, f_{IN}=0.5 to 0.9MHz)
0.5Vp-p input sensitivity (other than above)

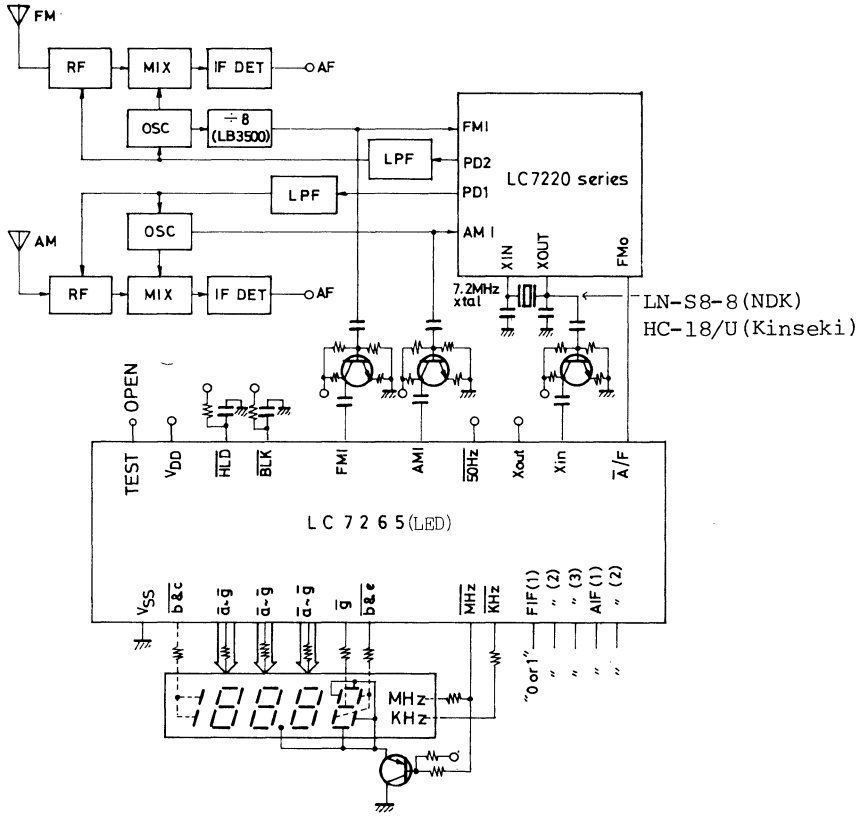
(9) $\overline{A}$/F ----- FM/MW, LW select pin
FM -------- Pin open or high level
MW,LW ----- Low level

(10) $\overline{50Hz}$ ----- 50Hz time base output pin



(11) TEST ----- LSI test pin : Normally open or connected to V_{SS}.

Application Circuit (Using LC7265 jointly with LC7220 series)



4. Main Specifications

4-1. Main Specifications for LC7265

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		-0.3 to +11	V
Input Voltage	V_{IN}	All input pins	-0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(1)}$	X_{OUT}, $\overline{HLD}$, $\overline{50Hz}$, output : OFF	-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d max$	$T_a \leq 65°C$	550	mW
Allowable Power Dissipation of Segment Outputs	$P_{d(seg)}$	$\overline{MHz}$, $\overline{b\&c}$, $\overline{b\&e}$, V_{DD}=4.5 to 6.5V, I_{OL}=33mA	30	mW
Allowable Power Dissipation of Segment Outputs	$P_{d(seg)}$	Other outputs, V_{DD}=4.5 to 6.5V, I_{OL}=16.5mA	15	mW
Allowable Power Dissipation of Segment Outputs	$P_{d(seg)}$	$\overline{MHz}$, $\overline{b\&c}$, $\overline{b\&e}$, V_{DD}=6.0 to 10V, I_{OL}=36mA	25	mW
Allowable Power Dissipation of Segment Outputs	$P_{d(seg)}$	Other outputs, V_{DD}=6.0 to 10V, I_{OL}=18mA	12	mW
Operating Temperature	Topg		-30 to +65	°C
Storage Temperature	Tstg		-40 to +125	°C
Output Voltage	$V_{O(2)}$	Output pins other than $V_{O(1)}$	0 to 15	V

Allowable Operating Ranges at T_a=25°C, V_{DD}=4.5 to 10V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		10	V
Input "H" Level Voltage	$V_{IH(1)}$	$\overline{A/F}$, $\overline{BLK}$	0.7V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL(1)}$	$\overline{A/F}$, $\overline{BLK}$	0		0.3V_{DD}	V
Input "H" Level Voltage	$V_{IH(2)}$	FIF1, FIF2, FIF3, AIF1, AIF2	0.9V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL(2)}$	FIF1, FIF2, FIF3, AIF1, AIF2	0		0.1V_{DD}	V
Input Frequency	$f_{IN(1)}$	FM1, sine wave, capacitive coupling, AMI, $V_{IN(1)}$=0.7Vp-p	1		18	MHz
"	$f_{IN(2)}$	AM1, sine wave, capacitive coupling, AMI, $V_{IN(2)}$=0.5Vp-p*	0.5		3	MHz
"	$f_{IN(3)}$	X_{IN}	0.2		7.5	MHz
Input Amplitude	$V_{IN(1)}$	FMI, sine wave, capacitive coupling, $f_{IN(1)}$=1 to 18MHz	0.7		0.9V_{DD}	Vp-p
"	$V_{IN(2)}$	AMI, sine wave, capacitive coupling, $f_{IN(2)}$=0.5 to 3MHz	0.5*		0.9V_{DD}	Vp-p
"	$V_{IN(3)}$	X_{IN}, sine wave, capacitive coupling, $f_{IN(3)}$=0.2 to 7.5MHz	1.0		0.9V_{DD}	Vp-p
Segment Current	$I_{seg(1)}$	$\overline{MHz}$, $\overline{b\&e}$, $\overline{b\&c}$	0		30	mA
"	$I_{seg(2)}$	Other outputs	0		15	mA

* : For $f_{IN(2)}$=0.5MHz to 0.9MHz and V_{DD}=8 to 10V, $V_{IN(2)}$min=1.0Vp-p applies.

Electrical Characteristics at T_a=25°C, V_{DD}=4.5 to 10V, V_{SS}=0V

			min	typ	max	unit
Input "H" Level Current	$I_{IH(1)}$	FIF1, FIF2, FIF3, AIF1, AIF2) V_I=V_{DD}	0		10	uA
Input "L" Level Current	$I_{IL(1)}$	FIF1, FIF2, FIF3, AIF1, AIF2) V_I=V_{SS}	0		10	uA
Input "H" Level Current	$I_{IH(2)}$	$\overline{BLK}$ V_I=V_{DD}	0		2	uA
Input "L" Level Current	$I_{IL(2)}$	$\overline{BLK}$ V_I=V_{SS}	0		2	uA
Input "L" Level Current	$I_{IL(3)}$	$\overline{A/F}$ V_I=V_{SS}	20		500	uA
Input Floating Voltage	$V_{IF(1)}$	$\overline{A/F}$ V_I=open	0.8V_{DD}		V_{DD}	V
Input/Output "H" Level Leakage Current	$I_{OFF(1)}$	$\overline{HLD}$, Output off, V_I=V_{DD}	0		2	uA
Output "L" Level Voltage	$V_{OL(1)}$	$\overline{HLD}$, Output on, I_o=1mA	0		1	V
Input "H" Level Threshold Voltage	V_{th}	$\overline{HLD}$	0.4V_{DD}	0.5V_{DD}	0.7V_{DD}	V
Output "L" Level Voltage	$V_{OL(2)}$	$\overline{b\&e}$, $\overline{b\&c}$, $\overline{MHz}$ V_{DD}=4.5 to 10V, I_{OL}=30mA	0		0.7	V
Output "L" Level Voltage	$V_{OL(3)}$	Segments other than above V_{DD}=4.5 to 10V, I_{OL}=15mA	0		0.7	V

			min	typ	max	unit
Output "L" Level Voltage	$V_{OL(4)}$	$\overline{50Hz}$, I_o=0.2mA	0		1.0	V
Output Off Leakage Current	$I_{OFF(2)}$	All segments output pins, V_o=13V, output off	0		10	uA
Current Dissipation	I_{DD}	FM mode, $\overline{A}$/F=open or V_{DD} $f_{IN(1)}$=18MHz, 0.7Vp-p or (AM mode, $\overline{A}$/F=V_{SS}, $f_{IN(2)}$=3MHz, 0.5Vp-p) $f_{IN(3)}$=7.2MHz, 1Vp-p FIF1, FIF2, FIF3=V_{DD} AIF1, AIF2=V_{DD} $\overline{HLD}$, $\overline{BLK}$=V_{DD} Other pins open	0		18	mA

4-2. Main Specification for LC7266

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +11	V
Input Voltage	V_{IN}		-0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(1)}$	X_{OUT}, $\overline{HLD}$, $\overline{50Hz}$, output: OFF	-0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(2)}$	Output pins other than $V_{O(1)}$	V_{DD}-20 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d$max	T_a<75°C	300	mW
Allowable Power Dissipation of Segment Output	$P_{d(seg)}$	MHz, $\|-I_{OH}\|$<18mA, T_a<75°C	9	mW
Allowable Power Dissipation of Segment Output	$P_{d(seg)}$	b&c, b&e, $\|-I_{OH}\|$<6mA, T_a<75°C	3	mW
Allowable Power Dissipation of Segment Output	$P_{d(seg)}$	Other outputs, $\|-I_{OH}\|$<3mA, T_a<75°C	1.5	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

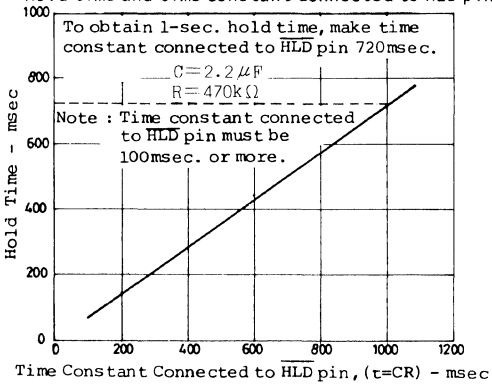
Allowable Operating Ranges at T_a=25°C, V_{DD}=4.5 to 10V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		10	V
Input "H" Level Voltage	$V_{IH(1)}$	$\overline{A}$/F, $\overline{BLK}$	0.7V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL(1)}$	$\overline{A}$/F, $\overline{BLK}$	0		0.3V_{DD}	V
Input "H" Level Voltage	$V_{IH(2)}$	FIF1, FIF2, FIF3, AIF1, AIF2	0.9V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL(2)}$	FIF1, FIF2, FIF3, AIF1, AIF2	0		0.1V_{DD}	V
Input Frequency	$f_{IN(1)}$	FMI, sine wave, capacitive coupling, $V_{IN(1)}$=0.7Vp-p	1		18	MHz
"	$f_{IN(2)}$	AMI, sine wave, capacitive coupling, $V_{IN(2)}$=0.5Vp-p*	0.5		3	MHz
"	$f_{IN(3)}$	X_{IN}	0.2		7.5	MHz
Input Amplitude	$V_{IN(1)}$	FMI, sine wave, capacitive coupling, $f_{IN(1)}$=1 to 18MHz	0.7		0.9V_{DD}	Vp-p
"	$V_{IN(2)}$	AMI, sine wave, capacitive coupling, $f_{IN(2)}$=0.5 to 3MHz	0.5*		0.9V_{DD}	Vp-p
"	$V_{IN(3)}$	XIN, sine wave, capacitive coupling, $f_{IN(3)}$=0.2 to 7.5MHz	1.0		0.9V_{DD}	Vp-p
Segment Current	$I_{seg(1)}$	MHz	0		9	mA
"	$I_{seg(2)}$	b&e, b&c	0		3	mA
"	$I_{seg(3)}$	Other outputs	0		1.5	mA

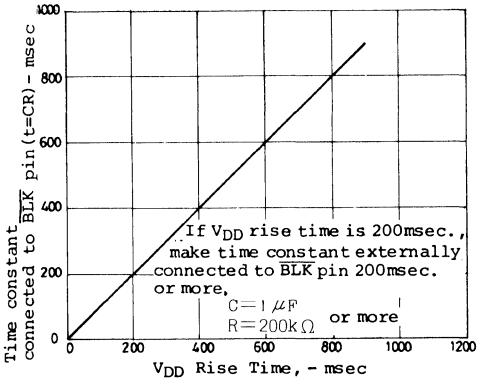
* : For $f_{IN(2)}$=0.5MHz to 0.9MHz and V_{DD}=8 to 10V, $V_{IN(2)}$min=1.0Vp-p applies.

Electrical Characteristics at T_a=25°C, V_{DD}=4.5 to 10V, V_{SS}=0V			min	typ	max	unit
Input "H" Level Current	$I_{IH(1)}$	FIF1,FIF2,FIF3 AIF1,AIF2) $V_I=V_{DD}$	0		10	uA
Input "L" Level Current	$I_{IL(1)}$	FIF1,FIF2,FIF3 AIF1,AIF2) $V_I=V_{SS}$	0		10	uA
Input "H" Level Current	$I_{IH(2)}$	$\overline{BLK}$ $V_I=V_{DD}$	0		2	uA
Input "L" Level Current	$I_{IL(2)}$	$\overline{BLK}$ $V_I=V_{SS}$	0		2	uA
Input "L" Level Current	$I_{IL(3)}$	$\overline{A}/F$ $V_I=V_{SS}$	20		500	uA
Input Floating Voltage	$V_{IF(1)}$	$\overline{A}/F$ V_I=open	0.8V_{DD}		V_{DD}	V
Input/Output "H" Level Leakage Current	$I_{OFF(1)}$	$\overline{HLD}$, Output off, $V_I=V_{DD}$	0		2	uA
Output "L" Level Voltage	$V_{OL(1)}$	$\overline{HLD}$, Output on, I_o=1mA	0		1	V
Input "H" Level Threshold Voltage	V_{th}	$\overline{HLD}$	0.4V_{DD}	0 5V_{DD}	0 7V_{DD}	V
Output "H" Level Voltage	$V_{OH(1)}$	MHz I_{OH}=-3mA	V_{DD}-1			V
" "	$V_{OH(2)}$	b&e, b&c, I_{OH}=-1mA	V_{DD}-1			V
" "	$V_{OH(3)}$	Segments other than above, I_{OH}=-0.5mA	V_{DD}-1			V
Output "L" Level Voltage	$V_{OL(2)}$	$\overline{50Hz}$ I_O=0.2mA	0		1.0	V
Output Off Leakage Current	$I_{OFF(2)}$	All segments output pins, $V_O=V_{DD}$-18V, Output off	0		3	uA
Current Dissipation	I_{DD}	FM mode, $\overline{A}/F$=open or V_{DD} $f_{IN(1)}$=18MHz, 0.7Vp-p or AM mode, $\overline{A}/F=V_{SS}$ $f_{IN(2)}$=3MHz, 0.5Vp-p $f_{IN(3)}$=7.2MHz, 1Vp-p FIF1,FIF2,FIF3=V_{DD} AIF1,AIF2=V_{DD} $\overline{HLD}$,$\overline{BLK}$=V_{DD} Other pins open	0		18	mA

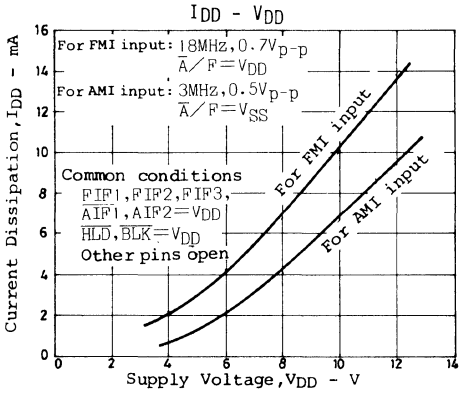
Hold time and time constant connected to $\overline{HLD}$ pin



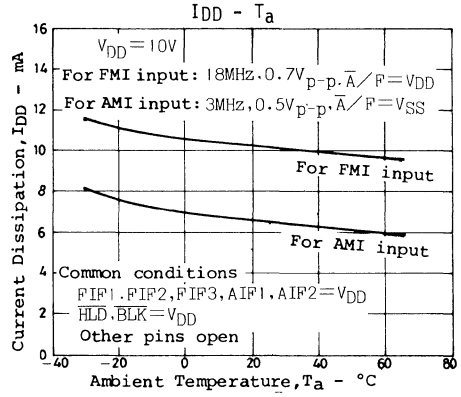
V_{DD} rise time and time constant connected to $\overline{BLK}$ pin



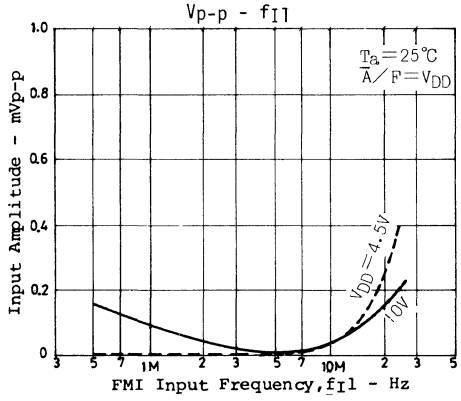
I_{DD} - V_{DD}



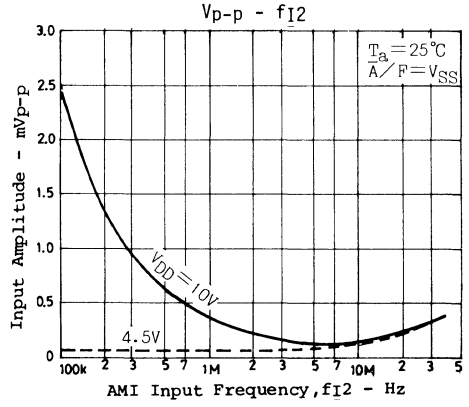
I_{DD} - T_a



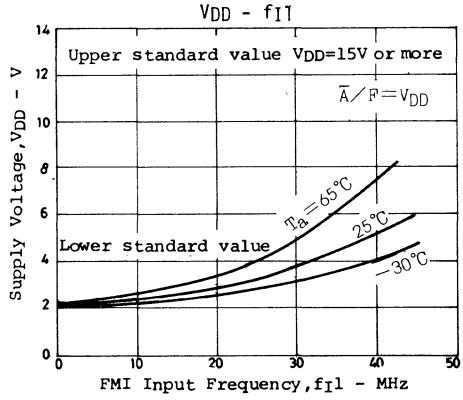
V_{p-p} - f_{I1}



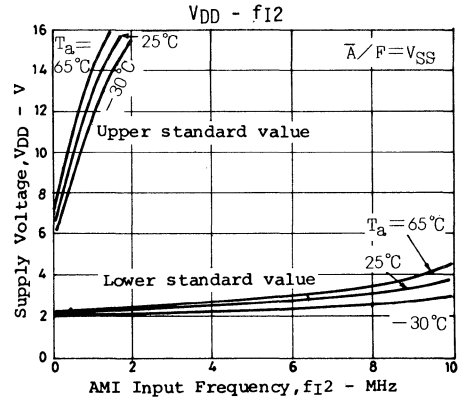
V_{p-p} - f_{I2}

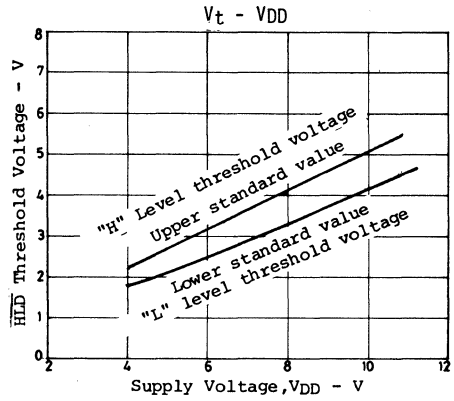


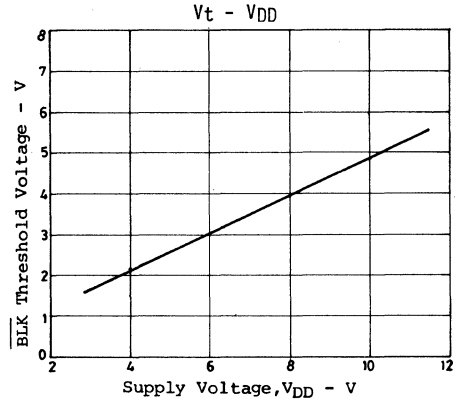
V_{DD} - f_{I1}

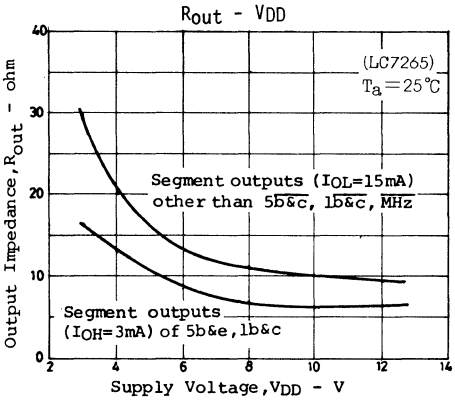


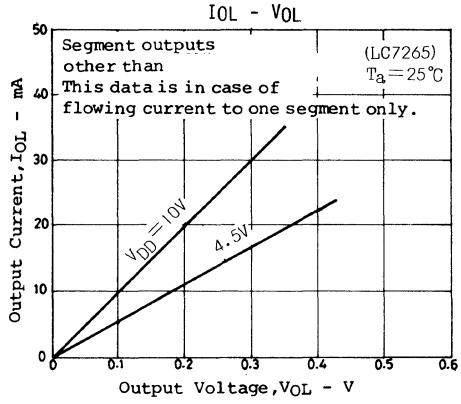
V_{DD} - f_{I2}

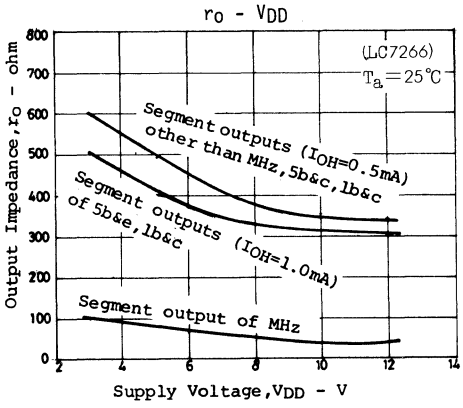


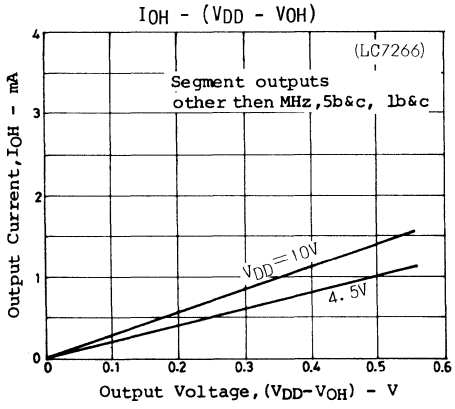

Vt - VDD
HLD Threshold Voltage - V
"H" Level threshold voltage
Upper standard value
Lower standard value
"L" level threshold voltage
Supply Voltage, VDD - V


Vt - VDD
BLK Threshold Voltage - V
Supply Voltage, VDD - V

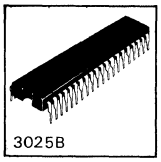

Rout - VDD
Output Impedance, Rout - ohm
(LC7265)
Ta=25℃
Segment outputs (IOL=15mA)
other than 5b&c, 1b&c, MHz
Segment outputs
(IOH=3mA) of 5b&e, 1b&c
Supply Voltage, VDD - V


IOL - VOL
Output Current, IOL - mA
Segment outputs
other than
This data is in case of
flowing current to one segment only.
(LC7265)
Ta=25℃
VDD=10V
4.5V
Output Voltage, VOL - V


ro - VDD
Output Impedance, ro - ohm
(LC7266)
Ta=25℃
Segment outputs (IOH=0.5mA)
other than MHz, 5b&c, 1b&c
Segment outputs (IOH=1.0mA)
of 5b&e, 1b&c
Segment output of MHz
Supply Voltage, VDD - V


IOH - (VDD - VOH)
Output Current, IOH - mA
(LC7266)
Segment outputs
other then MHz, 5b&c, 1b&c
VDD=10V
4.5V
Output Voltage, (VDD-VOH) - V

LC7267, 7268



C MOS LSI

Digital 5-Digit Frequency Indicator(LED) with Clock

Ⓔ 1511

TENTATIVE

Functions

(1) Capable of selecting receiving frequency display/time display.
(2) Display of receiving frequency at each band of FM/MW/LW

	Display Element	Static/dynamic	Withstand Voltage at Output Pin	Max. Current
LC7267	LED	Static	15 V	16.5 mA (V_{DD} = 4.5 ~ 6.0 V) 18 mA (V_{DD} = 6.5 V ~ 10 V)
LC7268	FLT	Static	V_{DD} ~ 20 V	−3 mA

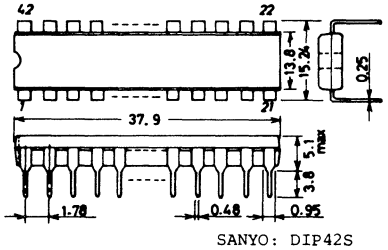
(3) Number of display digits: FM: 5 digits, MW, LW: 4 digits
(4) Covers intermediate frequencies shown below.

FM: +10.700, +10.725, +10.750, +10.675 MHz
−10.700, −10.725, −10.675, −10.650 MHz

MW, LW: +450 kHz(1) - - - 10 kHz-step display
+450 kHz(2) - - - 1 kHz-step display
+455 kHz - - - - - 1 kHz-step display
+469 kHz - - - - - 1 kHz-step display

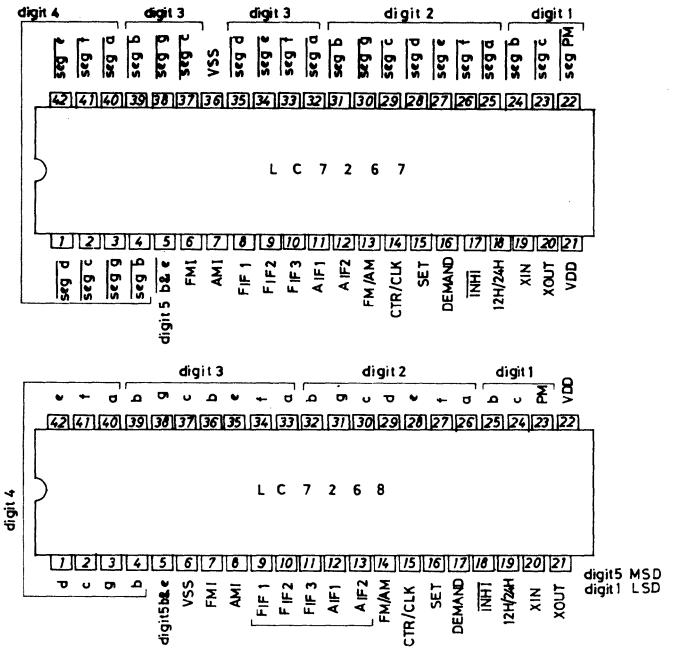
(5) In FM reception applications, the LB3500 (÷8 prescaler) is used jointly.
(6) Two selections of display system (12-hour system with PM sign, 24-hour system).
(7) Easy to set time by the time signal.
(8) Inhibit pin for inhibiting time setting with display unlighted.
(9) 7.2 MHz crystal for reference frequency.
(10) Supply voltage V_{DD}: 4.5 to 10.0 V.

Case outline 3025B-D42SIC
(unit:mm)



SANYO: DIP42S

Pin Assignment



Configuration and Display Font

4 or 4-1/2-digit segment LED's are used to display time and frequency in the display font shown below.

Display font 1 2 3 4 5 6 7 8 9 0

Lighting System

Static lighting

Display Range

- Frequency (MW, LW) 000 kHz to 1999 kHz (The highest-order digit "0" is blanked out.)
- Frequency (FM) 00.00 MHz to 199.95 MHz (The highest-order digit "0" is blanked out.)
- Clock (12-hour) PM12:00 to PM11:59 → 12:00 to 11:59
- Clock (24-hour) 0:00 to 23:59 (The highest-order digit "0" is blanked out.)

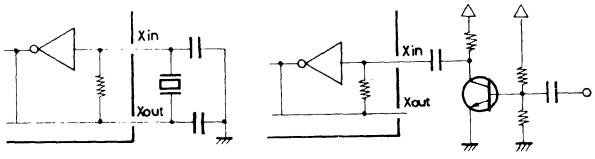
Pin Description (The LC7267/68 have the same pin name, function except output driver pins, provided that the pin No. is not necessarily the same.)

□ $\bar{a}$~$\bar{g}$, $\overline{PM}$, $\overline{b\&e}$ . . . . . LED (LC7267) driver pin

a~g, PM, b&e . . . . . FLT (LC7268) driver pin

☐ V_{DD}, V_{SS} ..... Power supply pin

☐ X_{IN}, X_{OUT} ..... Crystal oscillator, input amp pin



Crystal oscillator Input amp

☐ $F_{IF}(1)$, $F_{IF}(2)$, $F_{IF}(3)$ ..... FM IF offset value select pin

$F_{IF}(1)$	0	0	0	0	1	1	1	1
$F_{IF}(2)$	0	0	1	1	0	0	1	1
$F_{IF}(3)$	0	1	0	1	0	1	0	1
IF (MHz)	+10.700	+10.725	+10.675	+10.750	-10.700	-10.725	-10.675	-10.650

☐ $A_{IF}(1)$, $A_{IF}(2)$ ..... AM IF offset value select pin

$A_{IF}(1)$	0	0	1	1
$A_{IF}(2)$	1	0	0	1
IF (kHz)	+450(1)	+450(2)	+455	+469
Display Step	10kHz	1 kHz step		

1: High level
0: Low level

(Note) 450 kHz (1): 10 kHz-step display, others: 1 kHz-step display

☐ FMI, AMI ..... Local OSC signal input pin

FMI: For FM
AMI: For MW, LW

☐ FM/AM ..... FM/MW, LW select pin

FM: High level
MW, LW: Low level

☐ CTR/CLK ..... Frequency display/time display select pin

CTR (Counter): High level
CLK (Clock): Low level

☐ DEMAND ..... Input pin for instructing execution of setting

CTR/CLK	DEMAND	MODE
0	1	Mode of setting by the time signal and hours-minutes setting mode
0	0	Time display mode

☐ SET ..... Input pin for setting hours-minutes

This pin is set at "M" level normally. The input signal of "H"/"L" level acts as follows:
When in the mode of setting by the time signal and hours-minutes setting mode (CTR/CLK = "L" DEMAND = "H")

High level: Execution of hours setting
Advance at a 2 Hz rate 1.2 seconds after the pin is set to "H" level.

Low level: Execution of setting by the time signal and minutes setting
Advance at a 2 Hz rate 1.2 seconds after the pin is set to "L" level.
Setting by the time signal is executed when the pin is set to "M" level within 1.0 second after set to "L" level. No carry to high-order digit occurs.

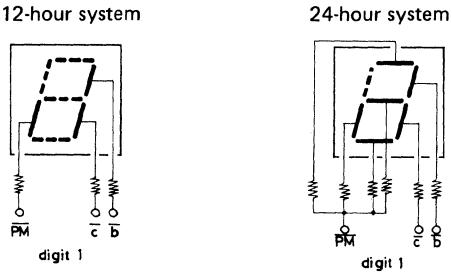
☐ $\overline{\text{INHI}}$..... Input pin for turning OFF the segment pins, inhibiting the SET/DEMAND pin from functioning, and preventing the AMI amp from operating

High level: Normal operation
Low level: Segment pin OFF, SET/DEMAND pin function inhibit

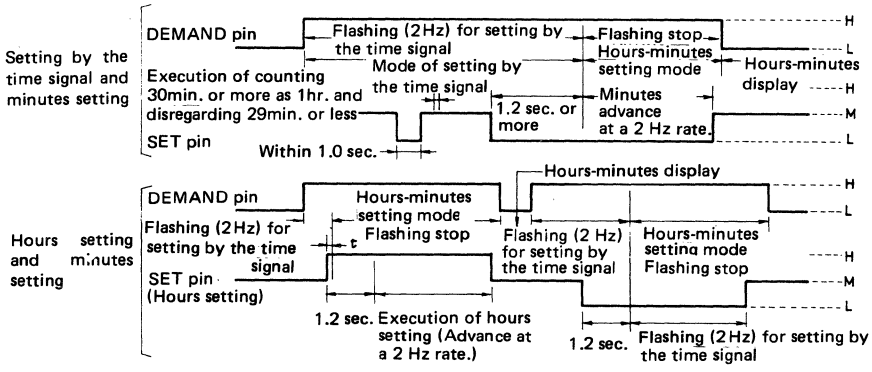
☐ 12H/24H..... Input pin for selecting 12-hour system with PM sign/24-hour system

High level: 12-hour system with PM sign
Low level: 24-hour system

Make connection of the highest-order digit as shown below.



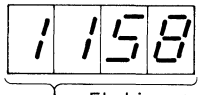
Timing Chart: Time setting (CTR/CLK = "L")



t: Approximately 100 msec.

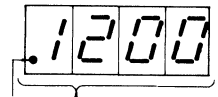
Sample Display at Each Display (Setting by the time signal, hours-minutes display, hours-minutes setting)

Setting by the time signal: Setting to PM 12:00



Execute setting by the time signal with the SET pin.

Flashing at a 2Hz rate when in the mode of setting by the time signal

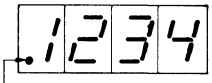


PM sign

Flashing at a 2Hz rate

When setting by the time signal is executed, minutes become 00. If the minutes display is at 30 to 59, hours are incremented by 1 (counting 30 or more as 1hr. and disregarding 29 or less).

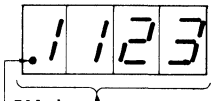
Hours-minutes display: Display of PM 12:34



PM sign

The PM sign flashes in the afternoon when in the mode of setting by the time signal, hours-minutes display, hours-minutes setting. (for 12-hour system).

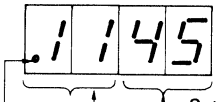
Hours-minutes setting: Setting to PM 11:45 from PM 11:23



PM sign

Flashing at a 2Hz rate

Set the SET pin to V_{DD} or V_{SS}. After lapse of 1.2sec., flashing stops and hours or minutes advance at a 2Hz rate.

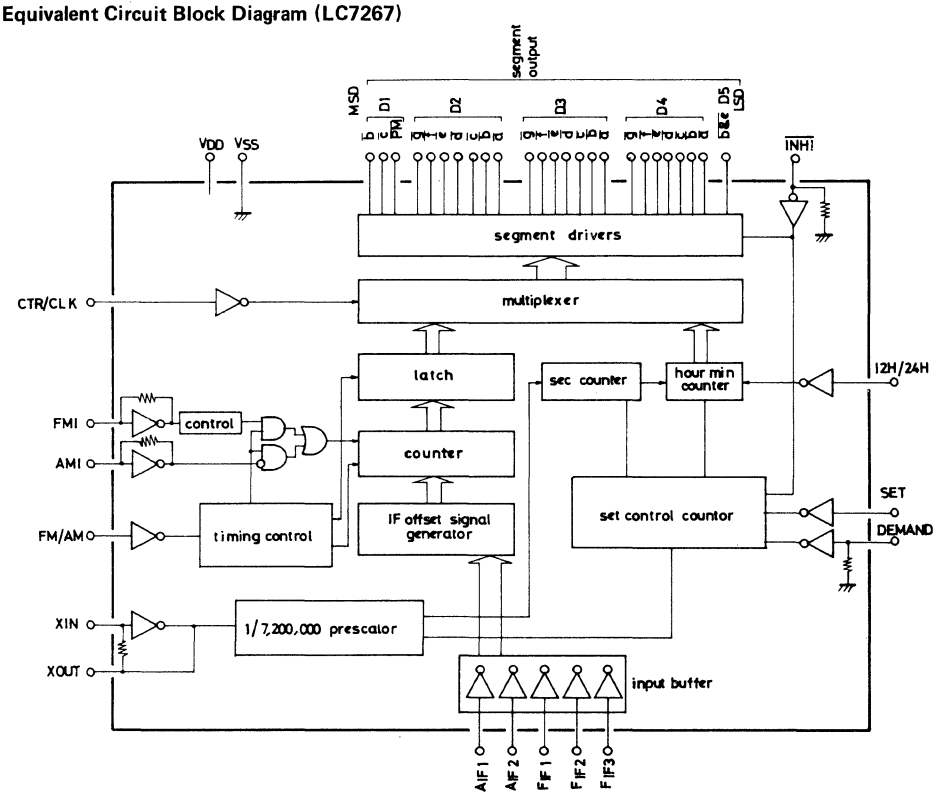


PM sign

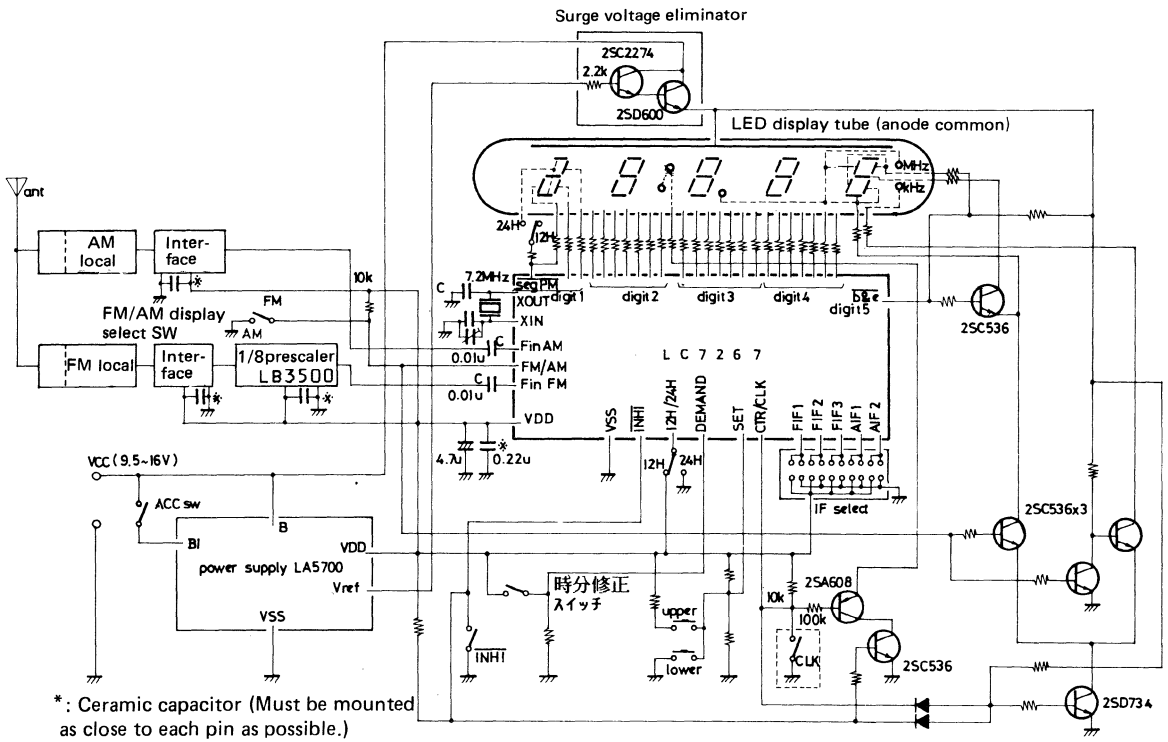
Set the SET pin to V_{SS}, and setting is executed.

Set the SET pin to V_{DD}, and setting is executed.

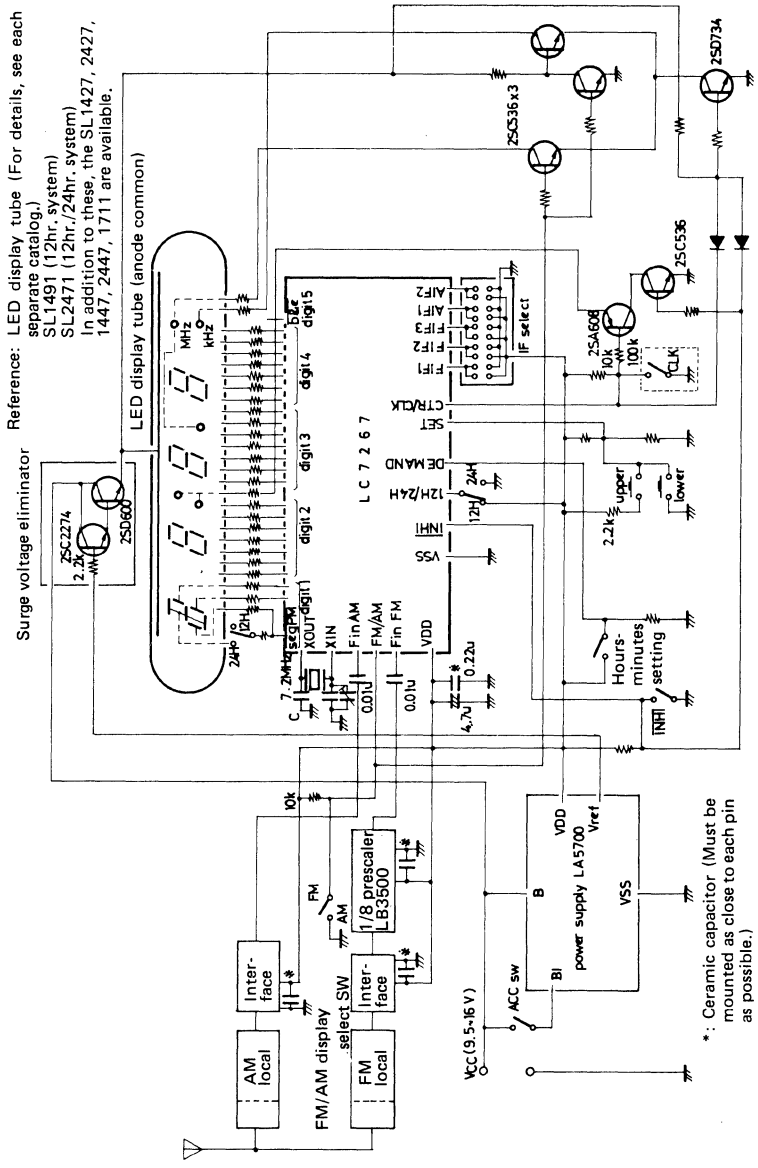
Equivalent Circuit Block Diagram (LC7267)



Sample Application Circuit 1: 5-digit display in FM use

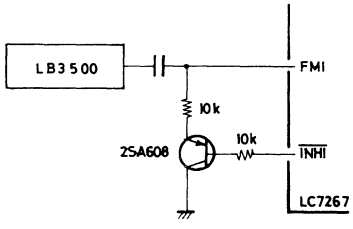


Sample Application Circuit 2: 4-digit display in FM use

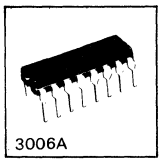


(Note) How to reduce current dissipation when display is turned off

To reduce current dissipation when display is turned off (INHI: 'L'), the circuit shown below must be connected to the FMI pin.



LC7500



C MOS IC

Electronic Attenuator Controller

Ⓔ 568B

Use

. An electronic volume control system is composed by using the LC7500 in conjunction with the electronic volume attenuator IC LA2600.

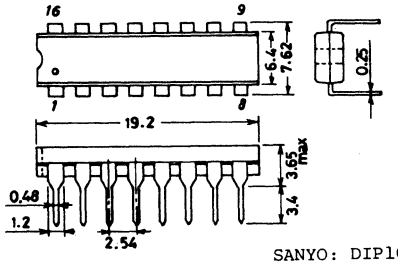
General Description

. The LC7500 contains a 5-bit binary up/down counter, an oscillation circuit, a clock signal generator, and a control circuit, etc. and provides up/down control of volume electronically.

Functions

. A 5-bit binary up/down counter is built in.
. Any value can be preset in the high-order 4 bits of the 5-bit binary up/down counter. In this case, the LSB is preset at "L" level.
. By connecting a ladder-type resistance network to the 5-bit output, the D-A conversion output is supplied to the LA2600.
. The following methods are used to cause the step to go up/down.
  a) Manual up/down
     . Each time the UP switch (or DOWN switch) is pushed, the contents of the 5-bit binary up/down counter will increase (or decrease) at a 1 step/push rate.
  b) Auto up/down
     . If the UP switch (or DOWN switch) is held pushed for more than approximately 0.6 second, the contents of the 5-bit binary up/down counter will increase (or decrease) at an approximately 5Hz rate.
     . If both of the UP and DOWN switches are pushed, the contents of the 5-bit binary up/down counter will remain unaffected.
     . When the contents of the 5-bit binary up/down counter become "31" (or "0"), the contents of the counter will not change any more even if the UP switch (or DOWN switch) is pushed further.
. Last stop memory
  Even if the UP switch (or DOWN switch) is pushed at the time of backup, the contents of the 5-bit binary up/down counter will remain unaffected.
. The clock signal generator generates the clock signal only when the UP switch (or DOWN switch) is pushed.

Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Pin Name

Pin No.	Name	Description	Pin No.	Name	Description
1	V_{DD}	Supply Voltage (+)	9	A OUT	Count output (LSB)
2	$\overline{UP}$	UP input	10	B OUT	Count output
3	$\overline{DOWN}$	DOWN input	11	C OUT	Count output
4	E IN	Preset jam data input	12	D OUT	Count output
5	D IN	Preset jam data input	13	E OUT	Count output (MSB)
6	C IN	Preset jam data input	14	V_{ref}	Reference voltage input
7	B IN	preset jam data input	15	$\overline{PRESET}$	Initialize input
8	V_{SS}	Supply voltage (-)	16	OSC	Oscillator input

Note) Output pins must not be shorted to each other.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

Maximum Supply Voltage	$V_{DD}max$		-0.3 to +11	V
Reference Voltage	V_{ref}	$V_{ref} \leqq V_{DD}$	-0.3 to +10	V
Input Voltage	V_{IN}		-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d max$		100	mW
Operating Temperature	T_{opg}		-30 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V, V_{DD}=8 to 10V, V_{ref}=7.9 to 8.1V

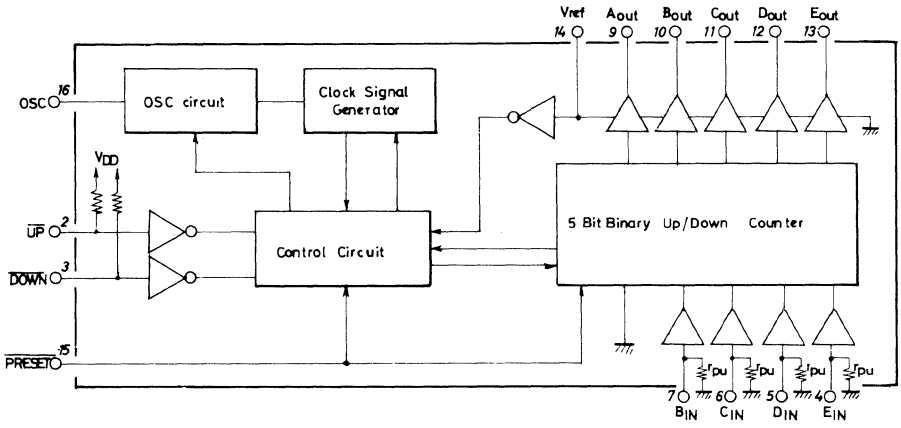
		($V_{DD} \leqq$ 8V : V_{ref}=0V)	min	typ	max	unit
Supply Voltage	V_{DD1}		8.0	9.0	10.0	V
	V_{DD2}	Backup	4.5			V
Reference Voltage	V_{ref}	$V_{ref} \leqq V_{DD}$	7.9	8.0	8.1	V
Input "H" Level Voltage	$V_{IH}(1)$	$\overline{UP}$, $\overline{DOWN}$	0.75V_{DD}		V_{DD}	V
"	$V_{IH}(2)$	$\overline{PRESET}$	4.3		V_{DD}	V
"	$V_{IH}(3)$	B_{IN}, C_{IN}, D_{IN}, E_{IN}	0.85V_{DD}		V_{DD}	V
Input "L" Level Voltage	$V_{IL}(1)$	$\overline{UP}$, $\overline{DOWN}$	V_{SS}		0.25V_{DD}	V
"	$V_{IL}(2)$	$\overline{PRESET}$	V_{SS}		0.5	V
"	$V_{IL}(3)$	B_{IN}, C_{IN}, D_{IN}, E_{IN}	V_{SS}		0.15V_{DD}	V
Pin $\overline{PRESET}$ External Time Constant	t_p	$\overline{PRESET}$, V_{DD} rise time within 10msec.	30			msec
Oscillation Guaranteed External Resistance	R_X	OSC, Carbon film Resistor, f_{osc}=640Hz		150		kohm
Oscillation Guaranteed External Capacitance	C_X	OSC, Polystyrene film capacitor, f_{osc}=640Hz		0.015		uF

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=8.0 to 10.0V, V_{ref}=+7.9 to +8.1V,

		at $V_{ref} \leqq V_{DD}$	min	typ	max	unit
Input Floating Voltage	$V_{IF}(1)$	$\overline{UP}$, $\overline{DOWN}$, Input pin open, With built-in pull-up resistor	V_{DD}-0.5			V
"	$V_{IF}(2)$	B_{IN}, C_{IN}, D_{IN}, E_{IN}, Open after applying V_{IN}=V_{SS}			0.5	V
Input "L" Level Current	$I_{IL}(1)$	$\overline{UP}$, $\overline{DOWN}$, V_{IN}=V_{SS}		-70		uA
"	$I_{IL}(2)$	$\overline{PRESET}$, V_{IN}=V_{SS}	-2			uA
"	$I_{IL}(3)$	B_{IN}, C_{IN}, D_{IN}, E_{IN}, V_{IN}=0.1V_{DD}		-13		uA
Input "H" Level Current	$I_{IH}(1)$	B_{IN}, C_{IN}, D_{IN}, E_{IN}, V_{IN}=V_{DD}			2	uA
"	$I_{IH}(2)$	$\overline{PRESET}$, V_{IN}=V_{DD}			2	uA
Output "L" Level Voltage	$V_{OL}(1)$	A OUT, I_{OL}=0.5mA		0.12		V
"	$V_{OL}(2)$	B OUT, I_{OL}=0.5mA		0.12		V
"	$V_{OL}(3)$	C OUT, I_{OL}=0.5mA		0.06		V
"	$V_{OL}(4)$	D OUT, I_{OL}=0.5mA		0.03		V
"	$V_{OL}(5)$	E OUT, I_{OL}=0.5mA		0.015		V
Output "H" Level Voltage	$V_{OH}(1)$	A OUT, I_{OH}=-0.5mA	V_{ref}-0.12			V
"	$V_{OH}(2)$	B OUT, I_{OH}=-0.5mA	V_{ref}-0.12			V
"	$V_{OH}(3)$	C OUT, I_{OH}=-0.5mA	V_{ref}-0.06			V
"	$V_{OH}(4)$	D OUT, I_{OH}=-0.5mA	V_{ref}-0.03			V
"	$V_{OH}(5)$	E OUT, I_{OH}=-0.5mA	V_{ref}-0.015			V

			min	typ	max	unit
Oscillation Frequency	f_{osc}	OSC, R_X=150kohm, C_X=150kohm		640		Hz
Current Dissipation	$I_{DD}(1)$	$\overline{UP}$, $\overline{DOWN}$=V_{SS}, V_{DD}=10V B_{IN} to E_{IN}=$\overline{PRESET}$=V_{ref}=V_{DD}			3.0	mA
"	$I_{DD}(2)$	V_{DD}=5.5V, $\overline{UP}$=$\overline{DOWN}$=open, B_{IN} to E_{IN}=$\overline{PRESET}$=V_{ref}=V_{DD}, B_{IN} to E_{IN}=$\overline{PRESET}$=V_{ref}=V_{SS},			0.2	mA
Current Dissipation	$I_{ref}(1)$	No load, $\overline{UP}$=$\overline{DOWN}$=open, B_{IN} to E_{IN}=$\overline{PRESET}$=V_{DD}			5	uA
	$I_{ref}(2)$	10k, 20k ladder-type resistor		0.5		mA

Equivalent Circuit Block Diagram



Note) r_{pu} is a special resistor which has the standard resistance value at "L" level and the high resistance value at "H" level.

Pin Description

$\overline{UP}$

- Each time the "L" level voltage is applied, the volume will increase by 1 step. However, when the maximum level (31st step) is reached, no further increase will occur.
- If the "L" level voltage is held applied for more than approximately 0.6 second, the volume will automatically increase by 1 step for every approximately 0.2 second. When the maximum level of volume is reached, the volume will automatically stop increasing.

$\overline{DOWN}$

- Each time the "L" level voltage is applied, the volume will descrease by 1 step. However, when the minimum level (0 step) is reached, no further decrease will occur.
- If the "L" level voltage is held applied for more than approximately 0.6 second, the volume will automatically decrease by 1 step for every approximately 0.2 second. When the minimum level of volume is reached, the volume will automatically stop decreasing.
- If the "L" level voltage is applied to pins $\overline{UP}$ and $\overline{DOWN}$ simultaneously, the count operation will stop.

$\overline{PRESET}$

- If the "L" level voltage is applied, the LSI inside will be initialized. The internal counter is initialized to be the value designated by jam data inputs B_{IN} to E_{IN}. The LSB is initialized to be "L" level.
- With a capacitor and a resistor attached to pin $\overline{PRESET}$ externally, preset function works only when the power supply is turned ON.

OSC
. With a capacitor and a resistor attached to pin OSC externally, oscillation of the reference frequency is provided. Oscillation is provided only when the "L" level voltage is applied to pin $\overline{UP}$ or $\overline{DOWN}$. When V_{ref} becomes "L" level, oscillation will stop.

$B_{IN}, C_{IN}, D_{IN}, E_{IN}$: Jam Data Inputs
. By attaching a capacitor and a resistor to pin $\overline{PRESET}$ as specified, the high-order 4 bits (B_{OUT} to E_{OUT}) of the counter are initialized as designated by B_{IN} to E_{IN} when the power supply is turned ON.
. At the "H" ("L") level input, the corresponding bits are initialized to be "H" ("L") level. A_{OUT} (LSB) is initialized to be "L" level.

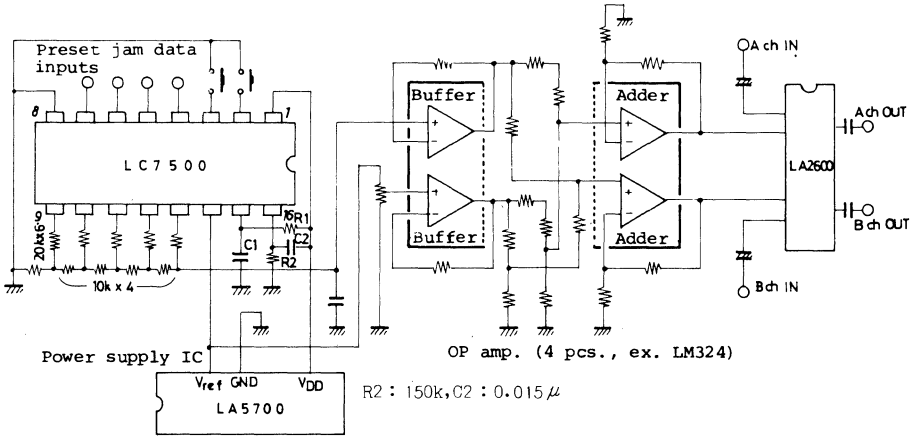
$A_{OUT}, B_{OUT}, C_{OUT}, D_{OUT}, E_{OUT}$: Count Outputs of Counter (A_{OUT}:LSC, B_{OUT}:MSB)
. The count contents of the internal 5-bit binary up/down counter are outputted. When V_{ref} is 0V (at the time of backup), the outputs will be "L" level.

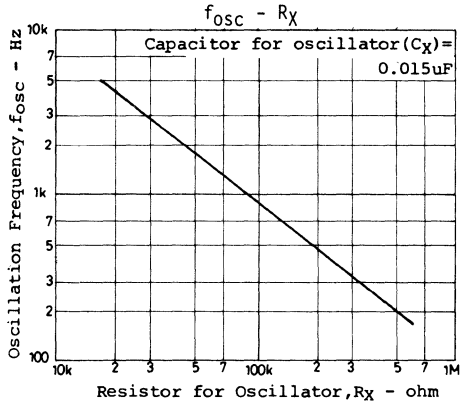
V_{ref} : Input Pin of Reference Voltage
. This is used as the power supply for the output buffers of the count outputs (A_{OUT} to E_{OUT}). Oscillation of the oscillator is stopped by detecting that V_{ref} has become 0V at the time of backup, and even if the UP or DOWN switch is pushed during backup, the holding step will not change.

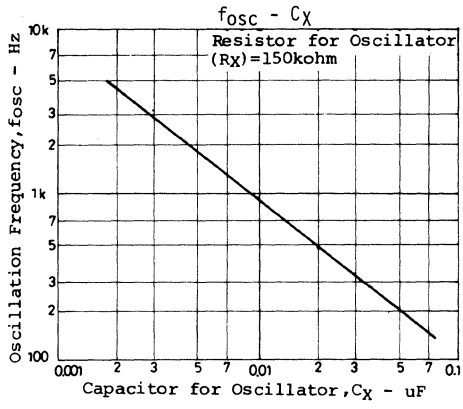
Input Signal
. Switch signal Logic "L" ----- V_{SS}
  Logic "H" ----- V_{DD}
. $\overline{PRESET}$ C, R are attached externally.
. OSC C, R are attached externally.

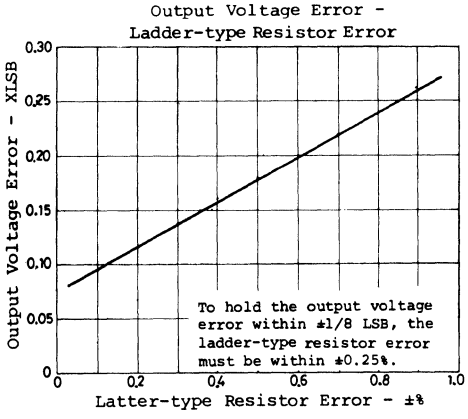
Output Organization 5 bits (32 steps)
. Complementary output Logic "L" ----- V_{SS}
  Logic "H" ----- V_{ref}
. Ladder-type resistors externally attached 10kohm, 20kohm

Application Circuit

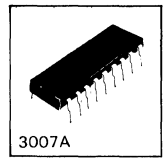



fosc - Rx
Capacitor for oscillator(Cx)=
0.015uF
Oscillation Frequency,fosc - Hz
10k
7
5
3
2
1k
7
5
3
2
100
10k
2
3
5
7
100k
2
3
5
7
1M
Resistor for Oscillator,Rx - ohm


fosc - Cx
Resistor for Oscillator
(Rx)=150kohm
Oscillation Frequency,fosc - Hz
10k
7
5
3
2
1k
7
5
3
2
100
0.001
2
3
5
7
0.01
2
3
5
7
0.1
Capacitor for Oscillator,Cx - uF


Output Voltage Error -
Ladder-type Resistor Error
Output Voltage Error - XLSB
0.30
0.25
0.20
0.15
0.10
0.05
0
To hold the output voltage
error within ±1/8 LSB, the
ladder-type resistor error
must be within ±0.25%.
0
0.2
0.4
0.6
0.8
1.0
Latter-type Resistor Error - ±%

LC7510, 7512



C MOS LSI

Automatic Music Selecting System for Tape Recorder

Ⓔ 893A

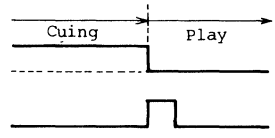
The LC7510/12 are a single chip IC that enables the automatic forward or backward cuing of your desired music up to 3 pieces from musics recorded on a tape recorder tape.

Applicable Sets :

Radio cassette, cassette deck, car stereo.

Features

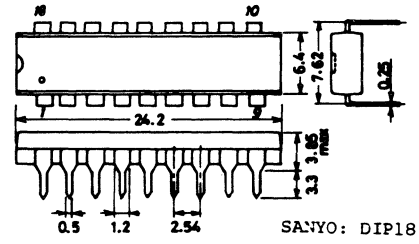
1. Unrecorded area sense unit and 3-piece cuing logic unit are built in.
2. Unrecorded area sense time and recorded area sense time are set independently bt the respective external CR, so that stable operation is made possible against pulse noise in unrecorded area and sound cut in recorded area.
3. For programming the number of musics to be cued, 2 modes are available as follows :
   . Direct set (Using 3 switches)
   . Serial set (Using 1 switch)
4. For drive output of plunger locking FF (or REW) lever while cuing, 2 types are available as follows, which are capable of meeting two kinds of deck mechanism.
   . Plunger ON while cuing
   . Plunger OFF while cuing



5. Initialization circuit to be used at the time of turning ON power supply is built in.*
   . For LC7510, no music programmed mode is initialized.
   . For LC7512, preceding or following 1 piece of music programmed mode is initialized.
6. For LC7512, it is possible to automatically reprogram preceding or following 1 piece of music immediately after cuing.* Therefore, preceding or following 1 piece of music can be cued only by operating FF (or REW) lever.
7. Input sensitivity is 250mV (typ.)
8. It is possible to direct drive LED (red or green) for displaying the number of programmed musics.
9. Wide range of operating supply voltages (V_{DD}=4.0 to 11.0 V).

* : For the differences between the LC7510 and LC7512, refer to the Table shown on page 2.

Case Outline 3007A-D18IC
(unit:mm)



SANYO: DIP18

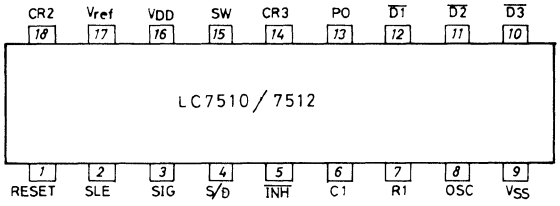
The differences between the LC7510 and LC7512 are shown below.

Item	LC7510	LC7512
Initialization at the time of turning ON power supply	No music programmed mode	Preceding or following 1 piece of music
Trigger at SW pin for serial set mode	"L"⟶ "H"	"H" ⟶ "L"
Pull-up resistor at $\overline{INH}$ pin	Used	Unused
Specification for automatic programming of preceding or following 1 piece of music immediately after cuing	Impossible	Possible (For serial set mode only)

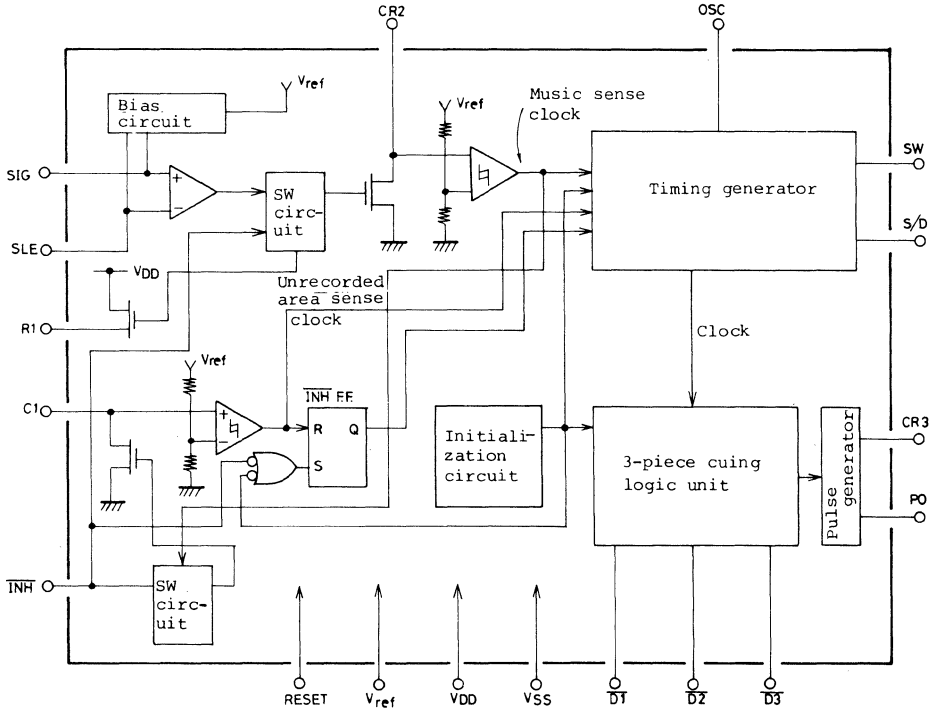
"L" : V_{SS} level
"H" : V_{DD} level

The LC7510 and LC7512 are identical in functions and characteristics except the above.

Pin Assignment

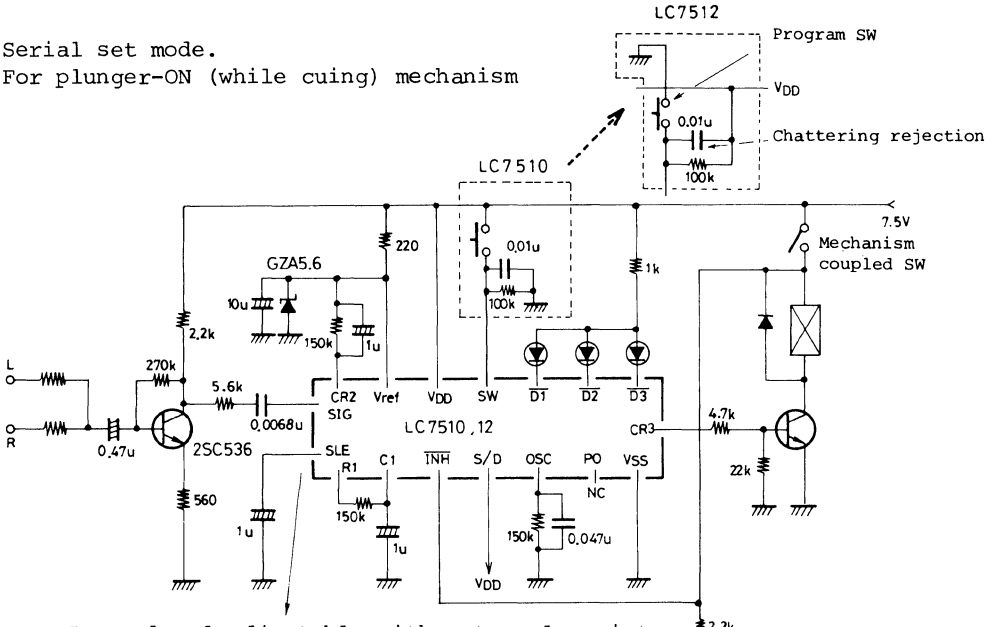


Equivalent Circuit Block Diagram



Application Circuit 1 (LC7510,7512)

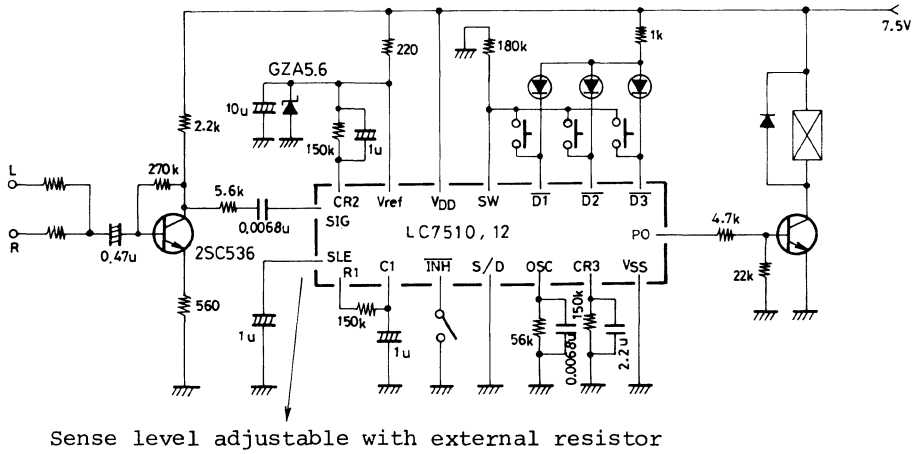
. Serial set mode.
. For plunger-ON (while cuing) mechanism



Sense level adjustable with external resistor
(Refer to Fig. 1 in Pin Description.)

Application Circuit 2 (LC7510,7512)

. Derect set mode
. For plunger-OFF (while cuing) mechanism

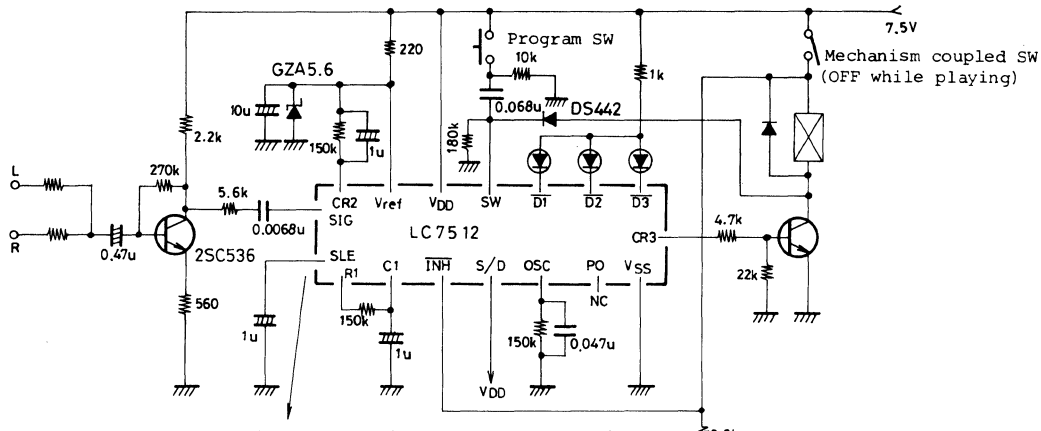


Sense level adjustable with external resistor
(Refer to Fig. 1 in Pin Description.)

Application Circuit 3 (LC7512)

- Serial set mode
- Automatic reprogramming of preceding or following 1 piece of music immediately after cuing.

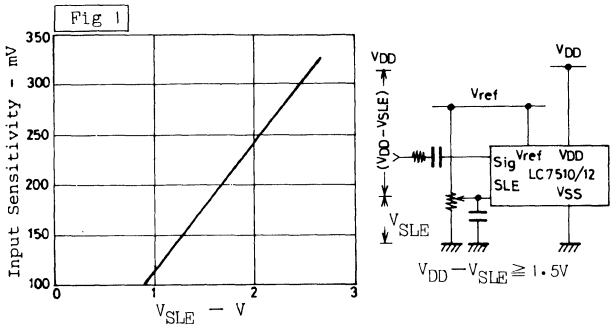
(Possible to search music 1 piece by 1 piece without programming)

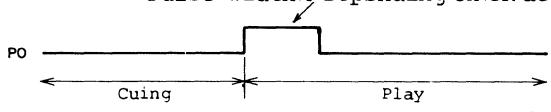
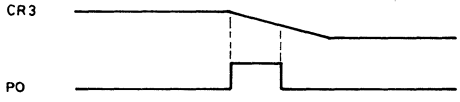
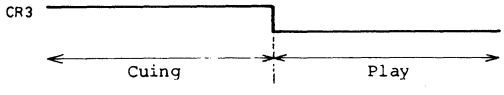


Sense level adjustable with external resistor
(Refer to Fig. 1.)

1. Pin Description

Name	Pin No.	Input/output	Pin description
V_{SS}	9		. Pin for turning ON power supply : V_{SS}=0V, V_{DD}=4.0 to 11.0 V
V_{DD}	16		
V_{ref}	17	Input	. Input pin for reference voltage which fixes comparison level of comparator and Schmidt comparator inside IC. . To perform accurate cuing operation, voltage of this pin must be stabilized with Zener diode, etc. connected outside IC.
RESET	1	Input	. Pin for forcibly resetting mode inside IC from outside. Internal initialization circuit causes resetting at the time of turning ON power supply. . With built-in Schmidt inverter. . With built-in pull-down resistor.
SLE	2	Input	. (-) input pin for audio signal input unit C MOS comparator. . Biased app. $3/8 \cdot V_{ref} + 0.05V_{ref}$ at pin open state. . Normally, app. luF capacitor must be connected between this pin and GND to reject ripple. . Varying voltage of this pin (resistance-type potential division, etc.) causes comparator sense level to be varied.

Name	Pin No.	Input/output	Pin description
SLE	2	Input	
SIG	3	Input	. (+) input pin for audio signal input unit C MOS comparator. . Inputting audio signal to this pin by capacitor coupling causes comparator to sense music. . Biased app. $3/8 \cdot V_{ref}$ at pin open state. Input impedance : 400k to 2M ohm
S/D	4	Input	. Pin for setting number of musics program mode to serial set mode or direct set mode. . Input "H" and input "L" cause serial set mode and direct set mode respectively. Input — Program mode "H" — Serial set "L" — Direct set . With built-in pull-up resistor.
$\overline{INH}$	5	Input	. Pin for inhibiting operation of unrecorded area sense unit. . Input "L" causes inhibit mode. . Normally, IC is operated with inhibit mode released only while cuing. . It is possible to freely program number of musics even during inhibit mode. . With built-in Schmidt inverter and F-F which memorizes inhibit mode. . LC7510 : With built-in pull-up resistor, LC7512 : Without pull-up resistor.
C_1	6	Input/output	. Pin for connecting external capacitor which forms recorded area sense integration circuit. . Connecting capacitor between this pin and GND causes capacitor to be charged up through R_1 pin while being in recorded area. (Refer to R_1 pin.) . With built-in Schmidt comparator, recorded area sense operation is performed when pin voltage exceeds $1/2 \cdot V_{ref}$. . Each time unrecorded area is sensed, capacitor is discharged, so recorded area sense integration is repeated and pulse noise in unrecorded area is rejected.

Name	Pin No.	Input/output	Pin description
R_1	7	Output	. Pin for connecting external resistor which forms recorded area sense integration circuit. . Connecting high resistor between this pin and C_1 pin causes capacitor of C_1 pin to be charged up through this resistor while being in recorded area. . P channel open drain output.
OSC	8	Input/output	. Pin for external CR for oscillator needed to operate internal logic unit. . Oscillation occurs only at the time of counting unrecorded area or changing program, and no oscillation occurs at the time of other than these operations. . At the time of serial set program mode, oscillator is operated as one-shot multivibrator, so program switch chattering can be rejected by increasing CR time constant.
$\overline{D_1}$ $\overline{D_2}$ $\overline{D_3}$	12 11 10	Output	. Output pin for driver for LED to display number of programmed musics. . At the time of direct set program mode, this pin is used also for driver for program switch scan. (Refer to Application Circuit 2.) . C MOS complementary circuit.
PO	13	Output	. Pin for driving plunger for plunger-OFF (while cuing) mechanism (On completion of cuing, plunger is turned ON and play mode occurs.) . Positive pulse is outputted and its pulse width depends on time constant of external CR connected to CR_3 pin. . Pch open drain output Pulse width : Depending on CR at CR_3 pin. 
CR_3	14	Input/output	. Pin for external CR which fix output pulse width at PO pin. . With built-in Schmidt inverter.  . Pin for also driving plunger for plunger-ON (while cuing) mechanism (On completion of cuing, plunger is turned OFF and play mode occurs.) . In this case, resistor only is used without capacitor. (Refer to Application Circuit 1.)  . When number of musics is programmed, "H" level is outputted. . P channel open drain output.

Name	Pin No.	Input/output	Pin description
SW	15	Input	. Input pin for program switch at both program modes of serial set mode and direct set mode. . With built-in Schmidt inverter. . Possible to direct input slow rising output signal of CR integration circuit used for switch chattering rejection
CR_2	18	Input/output	. Pin for external CR which set unrecorded area sense time. . With built-in Schmidt comparator, unrecorded area sense operation is performed when pin voltage exceeds $1/2 \cdot V_{ref}$. . Unrecorded area sense time (typ.) is calculated by the following equation. (Refer to Operation Description.) $t(typ)=0.693\ C_2R_2$ C_2:External capacitor capacitance (F) R_2:External resistor resistance (ohm)

2. Operation Description

2-1 Power supply turn-ON

Initialization at the time of turning ON power supply is made automatically by the initialization circuit, that is to say, the undermentioned $\overline{INH}$ F-F is set and the timing generator and 3-piece cuing logic unit are initialized. (Refer to Block Diagram.)

The $\overline{INH}$ F-F is set at the time of initialization, so even if "H" level is inputted to $\overline{INH}$ pin and the inhibit mode is released externally, the internal inhibit mode is not released, and unless the recorded mode continues for the period of time fixed by C_1, R_1 after turning ON power supply, the unrecorded area count operation is not performed. (Refer to 2-2.)

2-2 Cuing operation start

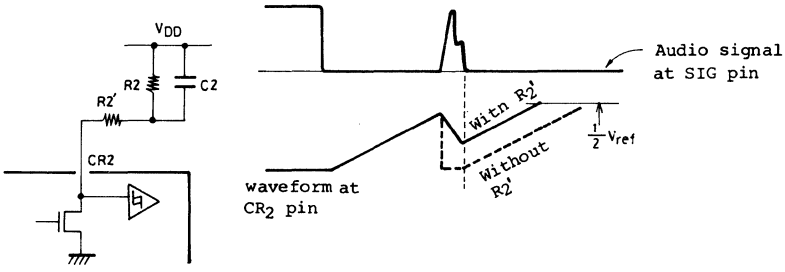
The cuing operation is started by changing-over the level of $\overline{INH}$ pin from "L" to "H" while power supply is applied. In case of the specification for automatic programming of preceding or following 1 piece of music for the LC7512, holding $\overline{INH}$ pin at "H" level causes the cuing operation to be started simultaneously with applying of power supply to the IC. In order that when the cuing operation is started with any unrecorded area this area is prevented from being sensed and when the REW cuing operation is started with any head of music the unrecorded area immediately following this head is prevented from being sensed, the unrecorded area sense unit functions as follows : (The head length depends on C_1, R_1.) In either state of these two where the cuing operation is started, C_1 is dischaged and the $\overline{INH}$ F-F is set. Then, when audio signal is inputted to SIG pin and its level exceeds the check level of the comparator, the transistor at R_1 pin is turned ON and C_1 is charged up through external resistor R_1. When the charged-up voltage exceeds the check level of the Schmidt comparator at C_1 pin, the output (recorded area sense clock) or the Schmidt comparator is set at "H" level, the $\overline{INH}$ F-F is reset, and unrecorded area sense operation in 2-3 is started. (Refer to period (A) of Time Chart.)

When releasing the inhibit mode with the mechanism coupled switch, a delay between switch-ON, OFF and signal at $\overline{INH}$ pin may be needed. Since the Schmidt inverter is built in $\overline{INH}$ pin, this delay can be easily caused by the external integration circuit.

2-3 Unrecorded area sense operation

When the level of audio signal at SIG pin exceeds the check level of the comparator, the transistor at CR_2 pin is turned ON, CR_2 pin is set at "L" level, and the external capacitor at CR_2 pin is charged up. When the tape comes to the unrecorded area and the level of audio signal at SIG pin goes

lower than the check level of the comparator transistor at CR_2 is turned OFF and capacitor C_2 starts discharging through external resistor R_2. When the voltage at CR_2 pin rises and exceeds the check level of the Schmidt comparator built in CR_2 pin, the comparator output (unrecorded area sense clock) is set at "L" level and the unrecorded area is counted. (Refer to (A) ⟶ (B) of Time Chart.) As a precaution to be taken in application, it should be noted that the following phenomenon may occur. If pulse noise exists during the unrecorded area sense operation, CR2 pin is turned ON, the external capacitor is charged up instantaneously, and the set-up period of discharge time is needed again, and thereby the unrecorded area sense operation goes imperfect. To avoid this phenomenon, the charge time must be made longer by inserting resistor R_2 between CR_2 pin and external CR.



Unrecorded area sense time t can be calculated by the following equation.

$$t = C_2R_2 \ln\left(\frac{1}{1 - \frac{1/2 \cdot V_{ref} \pm 250mV}{V_{ref}}}\right)$$

±250mV : Schmidt comparator offset. (Refer to Electrical Characteristics.)

$$t(typ) = C_2R_2 I_{n2} = 0.693 C_2R_2$$

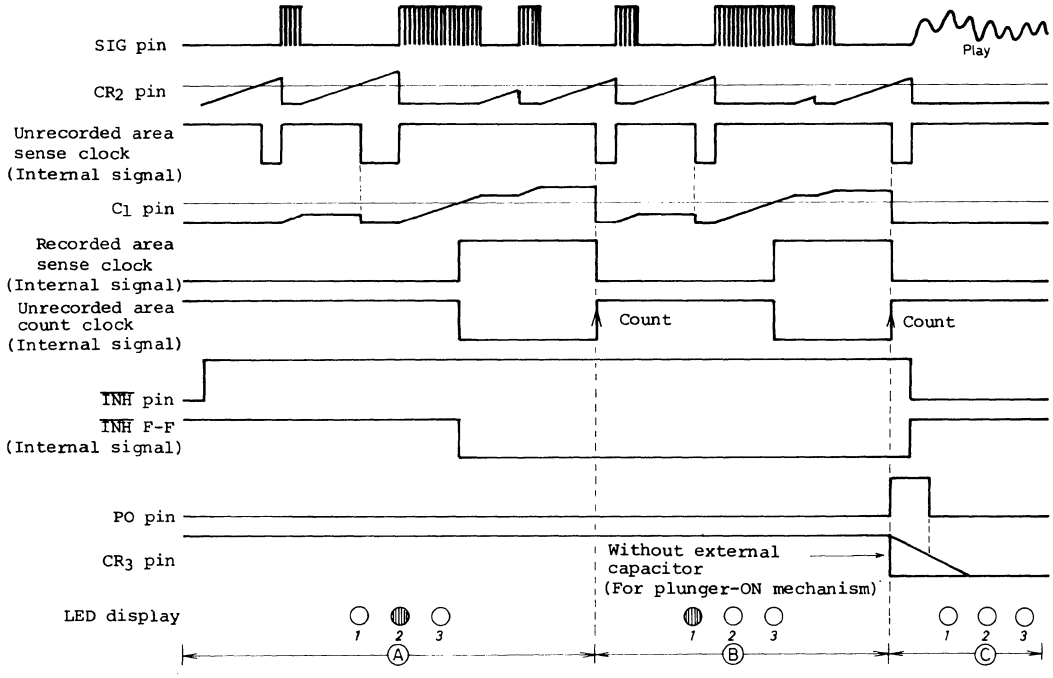
C_2 : External capacitor capacitance (F)

R_2 : External resistor resistance (ohm)

2-4 Recorded area sense operation (Pulse noise reject operation)

When the unrecorded area is sensed, the external capacitor at C_1 pin is discharged in readiness for the following recorded area sense operation and the Schmidt comparator output (recorded area sense clock) at C_1 pin is set at "L" level. The unrecorded area count clock is a NAND output of the recorded area sense clock and unrecorded area sense clock and the unrecorded area count operation is performed only when the unrecorded area count clock is changed-over from "L" level to "H" level. Therefore, when the recorded area sense clock is set at "L" level, the unrecorded area count clock remains at "H" level regardless of the unrecorded area sense clock mode and the unrecorded area count operation is stopped. This mode remains until C_1 is charged up and the Schmidt comparator output at C_1 pin is set at "H" level after the continuation of the recorded mode for the period of time fixed by C_1,R_1. When the Schmidt comparator output (recorded area sense clock) is set at "H" level, the unrecorded area count clock is set at "L" level, the unrecorded area count standby mode takes place, and when the unrecorded area following is sensed, the count operation is performed. As a result, pulse noise existing within the period of time fixed by C_1,R_1 is not identified as a recorded mode and the unrecorded area which follows noise is not counted. (Refer to period (B) of Pulse Noise Reject Operation Time Chart.) C_1 is discharged each time the unrecorded area is sensed, so if the interval between pulse noises exceeds the unrecorded area sense time fixed

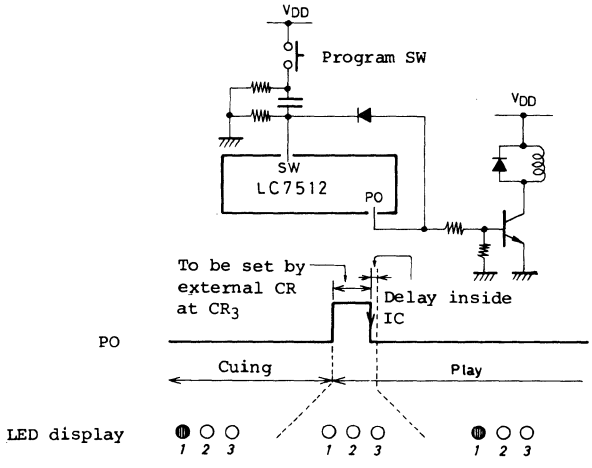
by C_2, R_2, pulse noise is not integrated C_1 no matter many times pulse noise can be rejected. Operations 2-3 to 2-4 are repeted thereafter.



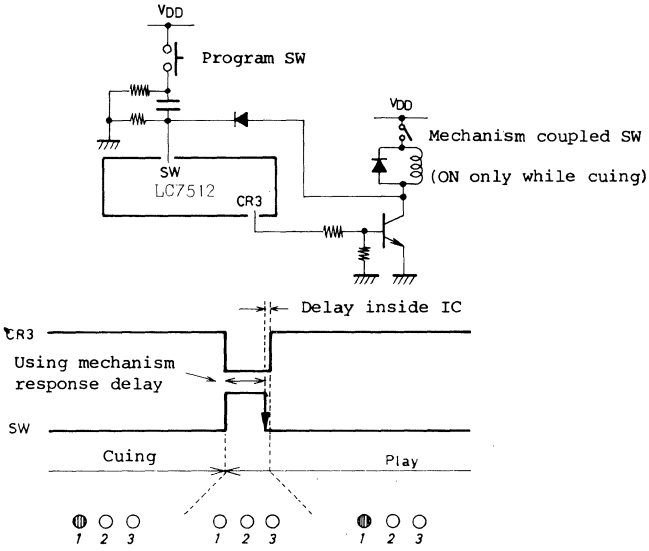
2-5 Automatic programming of music (For LC7512 serial set mode only)

The LC7512 enables the easy realization of the specification for automatic programming of preceding or following 1 piece of music because preceding or following 1 piece of music can be automatically reprogrammed immediately after play following the cuing operation by means of a simple application shown on page 9,10 and preceding or following 1 piece of music is initialized at the time of application of power.

(1) For plunger-OFF (while cuing) mechanism *when power supply is turned ON.



(2) For plunger-ON (while cuing) mechanism



3. Main Characteristics

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

Maximum Supply Voltage	V_{DD}		-0.3 to +12	V
Reference Voltage	V_{ref}		-0.3 to +11	V
Input Voltage	$V_{IN(1)}$	except SIG pin	-0.3 to V_{DD}+0.3	V
	$V_{IN(2)}$	SIG pin, external resistor 5.6k±10% (Refer to Fig.2.)	-3 to V_{DD}+3	V
Output Voltage	V_{OUT}		-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d$max	T_a≦75°C	0.3	W
Operating Temperature	T_{opg}		-30 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Range at T_a=25°C, V_{SS}=0V, V_{ref}≦V_{DD}, V_{DD}=4.0 to 11.0 V

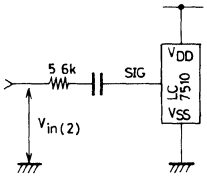
			min	typ	max	unit
Supply Voltage	V_{DD}		4.0		11	V
Reference Voltage	V_{ref}		4.0		V_{DD}	V
"H" Level Input Voltage	$V_{IH(1)}$	S/D	0.8V_{DD}		V_{DD}	V
	$V_{IH(2)}$	$\overline{INH}$, Reset, SW	0.8V_{DD}		V_{DD}	V
"L" Level Input Voltage	$V_{IL(1)}$	S/D	V_{SS}		0.2V_{DD}	V
	$V_{IL(2)}$	$\overline{INH}$, Reset, SW	V_{SS}		0.2V_{DD}	V
External Capacitor	$C_{EXT(1)}$	C_1, CR_2, CR_3			3.3	uF
	$C_{EXT(2)}$	OSC: Serial set mode			2.2	uF
External Resistor	R_{EXT}	SW: Direct set mode	162	180	198	kohm

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=4.5 to 9V, V_{ref}=4.5 to V_{DD}

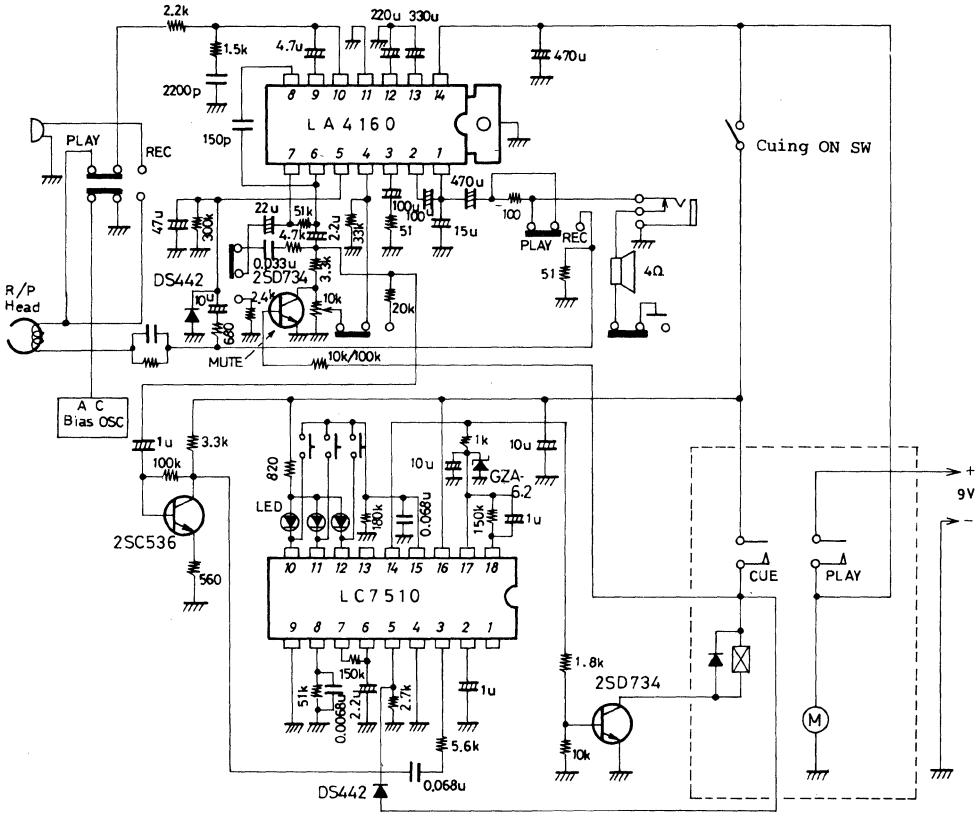
			min	typ	max	unit
Input Threshold	$V_t(1)$	SIG: AC level, V_{DD}=4.5 to 6 V	0.05V_{ref} -90		0.05V_{ref} +90	mV
	$V_t(2)$	CR_3	0.25V_{DD}		0.7V_{DD}	V
	V_{tH}	C_1, CR_2: V_{DD}=4.5 to 6V	0.5V_{ref} -250		0.5V_{ref} +250	mV
	V_{tL}	C_1, CR_2: V_{DD}=4.5 to 6V	0.375V_{ref} -250		0.375V_{ref} +250	mV

			min	typ	max	unit
"L" Level Output Current	$I_{OL(1)}$	D_1 to D_3:$V_{OL} \leq 0.2V_{DD}$, V_{DD}=4.0 to 4.5V			15	mA
		D_1 to D_3:$V_{OL} \leq 0.2V_{DD}$, $V_{DD} \geq 4.5V$			20	mA
"H" Level Output Current	$I_{OH(1)}$	CR_3,PO:$V_{OH}=V_{DD}-2.5V$			10	mA
Output OFF Leak Current	$I_{OH(2)}$	R_1,CR_3,OSC,$V_{OUT}=V_{SS}$	-2			uA
	$I_{OL(2)}$	C_1,CR_2,$V_{OUT}=V_{DD}$			2	uA
Output ON Resistance	$R_{ON(1)}$	C_1,CR_2:$V_{OUT}=V_{DD}$			300	ohm
	$R_{ON(2)}$	R_1			1	kohm
Input Impedance	Z_{in}	SIG:SLE pin AC ground	400		2000	kohm
Oscillation Frequency Accuracy	f	OSC:C=0.01uF,R=100kohm, Direct set mode.	1.12	1.60	2.08	kHz
Input Current	$I_{IL(1)}$	$\overline{INH}$ LC7510 only,S/D:$V_{in}=V_{SS}$,V_{DD}=6V	-150		-25	mA
	$I_{IH(1)}$	RESET:$V_{in}=V_{DD}$,V_{DD}=6V	25		150	mA
Input Leak Current	$I_{IH(2)}$	$\overline{INH}$(LC7512 only),SW:$V_{IN}=V_{DD}$			2	uA
	$I_{IL(2)}$	$\overline{INH}$(LC7512 only),SW:$V_{IN}=V_{SS}$	-2			uA
Supply Current	I_{ref}	V_{ref} $\overline{INH}$,SW=V_{SS},RESET,OSC, S/D,CR_3=V_{DD},others open.			2	mA
	I_{DD}	V_{DD}:$\overline{INH}$,SW=V_{SS},RESET,OSC, S/D,CR_3=V_{DD},others open.			2.5	mA

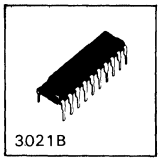
Fig. 2. : SIG pin input voltage test circuit



Application Circuit : Direct set mode
Using plunger-ON (while cuing) mechanism



LC7515



C MOS IC

Automatic Cuing Circuit for Tape Recorder

Ⓔ 1169A

The LC7515 is a C-MOS IC that enables automatic forward or backward cuing of your desired music up to 5 pieces from musics recorded on a tape recorder tape.

APPLICATIONS

- Radio cassettes, cassette decks, car stereos

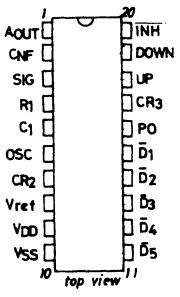
FEATURES

- Preamp., unrecorded area sense unit, and 5-piece cuing logic unit are built in.
- Unrecorded area sense time and recorded area sense time are set independently by external CR, so that stable operation is made possible against pulse noise in unrecorded area and sound cut in recorded area.
- For programming the number of musics to be cued, serial set (endless) mode in up/down direction is available.
- It is possible to direct drive 5 LEDs for displaying the number of programmed musics.
- At the time of cuing and power application, no program mode takes place.
  Automatic 1-piece programming is also enabled by external circuit. (Refer to Sample Application Circuits 3, 4.)
- Meets the requirements for deck mechanisms of 2 types (1. plunger OFF while cuing, 2. plunger ON while cuing).
- Input sensitivity: -52dBm type (f=10kHz)
- Wide operating voltage range (V_{DD}=5.0 to 11.0V) and small current dissipation ($I_{DD} \leqq 2.5$mA)
- Package: DIP20S (slim type)

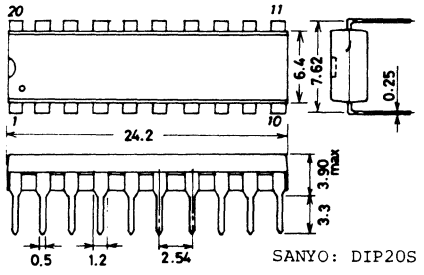
ABSOLUTE MAXIMUM RATINGS/T_a = 25°C, V_{SS} = 0V

		Pin Name	Pin No.			unit
Maximum supply voltage	V_{DD} max	V_{DD}	9		$V_{SS}-0.3 \sim V_{SS}+12$	V
Reference voltage	V_{ref}	V_{ref}	8	$V_{ref} \leqq V_{DD}$	$V_{SS}-0.3 \sim V_{SS}+11$	V
Input voltage	V_{IN}	C_{NF},SIG,UP, DOWN,$\overline{INH}$	2,3,18, 19,20		$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output voltage	V_{OUT}	A_{OUT},R_1,C_1, OSC,CR_2,PO CR_3,$\overline{D_1} \sim \overline{D_5}$	1,4,5,6, 7,16,17, 15 ~ 11	Output transistor off	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output current	I_{OUT}	$\overline{D_1} \sim \overline{D_5}$	15 ~ 11		30	mA
Power dissipation	P_d max			$T_a \leqq 75$°C	300	mW
Operating temperature	T_{opg}				−30 ~ +75	°C
Storage temperature	T_{stg}				−40 ~ +125	°C

Pin Assignment



Case Outline 3021B-D20SIC
(unit:mm)



SANYO: DIP20S

ALLOWABLE OPERATING RANGES/T_a = 25°C, V_{SS} = 0V

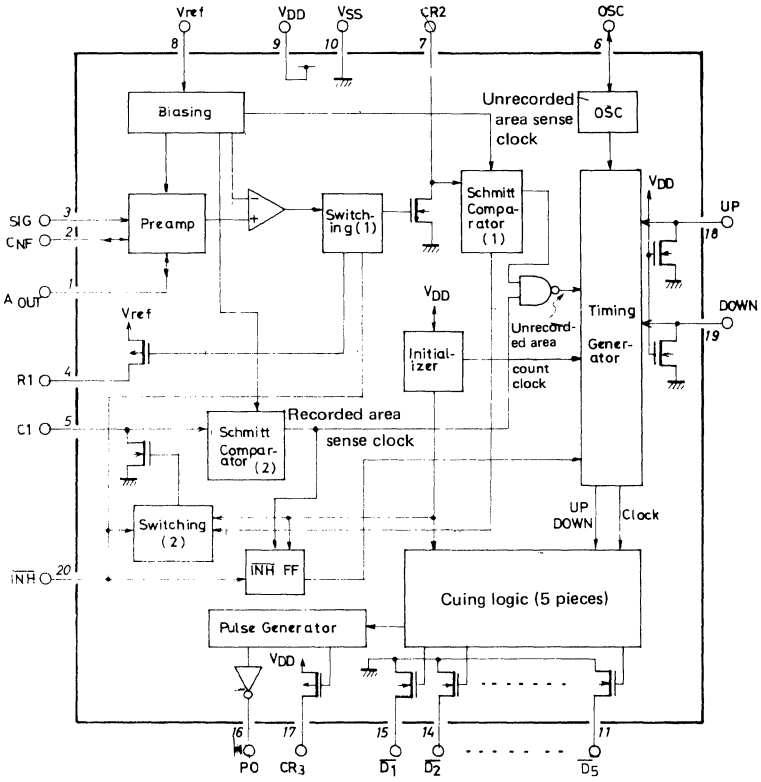
		Pin Name	Pin No.		min	typ	max	unit
Supply voltage	V_{DD}	V_{DD}	9		5		11	V
Reference voltage	V_{ref}	V_{ref}	8	$V_{ref} \leqq V_{DD}$	4		11	V
"H" level input voltage	V_{IH}	CR3,UP, DOWN,$\overline{INH}$	17,18 19,20		0.8V_{DD}		V_{DD}	V
"L" level input voltage	V_{IL}	UP,DOWN,$\overline{INH}$	18,19,20		V_{SS}		0.2V_{DD}	V
External capacitor	CEXT(1)	CI	5			1.0	2.2	μF
	CEXT(2)	CR2,CR3	7,17			1.0	10	μF
	CEXT(3)	OSC	6			0.01	2.2	μF
	CEXT(4)	C_{NF}	2		0.47	1.0	1.2	μF
	CEXT(5)	A_{OUT}-C_{NF}	1-2		33	36	39	pF
	CEXT(6)	A_{OUT}	1		470	1000	1500	pF
	CEXT(7)	SIG	3			0.1	2.2	μF
External resistor	REXT(1)	R1	4		0	100	430	kΩ
	REXT(2)	CR2	7		0.68	100	430	kΩ
	REXT(3)	CR3	17		1	100	240	kΩ
	REXT(4)	OSC	6		0.68	100	510	kΩ
	REXT(5)	C_1	5		0.68	1	10	kΩ
	REXT(6)	A_{OUT}-C_{NF}	1-2		180	240	300	kΩ
	REXT(7)	C_{NF}	2		0.51	1	3	kΩ

ELECTRICAL CHARACTERISTICS/T_a = 25°C, V_{SS} = 0V, V_{DD} = V_{ref} = 5 ~ 9V

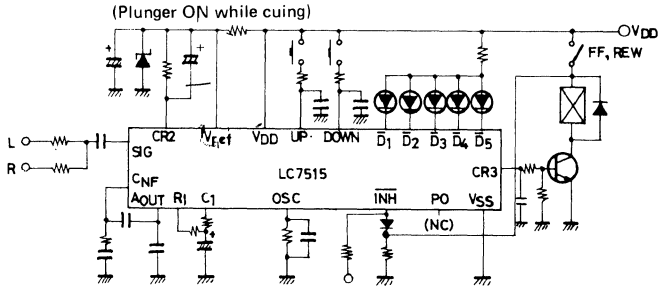
					min	typ	max	unit
Input threshold voltage	V_t	SIG	3	GAIN 48 dB, V_{DD} = 5V, f = 10kHz	−55 (1.38)	−52 (1.95)	−49 (2.75)	dB mV
	$V_{tL(1)}$	CR3	17	V_{DD} = 5 ~ 6V	0.25V_{DD}		0.7V_{DD}	V
	V_{tH}	C1,CR2	5,7	V_{DD} = 5 ~ 6V	0.5V_{ref} −250		0.5V_{ref} +250	mV
	$V_{tL(2)}$	C1,CR2	5,7	V_{DD} = 5 ~ 6V	3/8V_{ref} −250		3/8V_{ref} +250	mV
"H" level output voltage	V_{OH}	P0,CR_3	16,17	I_{OH} = −10mA	V_{DD}−2.5		V_{DD}	V
"L" level output voltage	$V_{OL(1)}$	$\overline{D1}$ ~ $\overline{D5}$	15 ~ 11	I_{OL} = 25mA	V_{SS}		V_{SS} + 1.9	V
	$V_{OL(2)}$	P0	16	I_{OL} = 10mA	V_{SS}		V_{SS} + 2.5	V
Output OFF leakage current	$I_{OFF(1)}$	R1,OSC,CR3	4,6,17	V_{OUT} = V_{SS}	−5		0	μA
	$I_{OFF(2)}$	C1,CR2	5,7	V_{OUT} = V_{DD}	0		5	μA
	$I_{OFF(3)}$	$\overline{D1}$ ~ $\overline{D5}$	15 ~ 11	V_{OUT} = V_{DD}	0		5	μA
Output ON resistance	$R_{ON(1)}$	C1,CR2	5,7	V_{DD} = 5V, V_{OUT} = V_{DD}	0		300	Ω
	$R_{ON(2)}$	R1	4	V_{DD} = 5V V_{OUT} = V_{SS}	0		1	kΩ
Input impedance	Z_{IN}	SIG	3	C_{NF}:AC grounded, f=10kHz	100	170	260	kΩ
"H" level input current	$I_{IH(1)}$	SIG	3	V_{ref} = V_{DD} = 5V, V_{IN} = V_{DD}	11.5	19.5	32.5	μA
	$I_{IH(2)}$	UP,DOWN	18,19	V_{DD} = 5V, V_{IN} = V_{DD}	10	50	100	μA
"L" level input current	$I_{IL(1)}$	SIG	3	V_{ref} = V_{DD} = 5V, V_{IN} = V_{SS}	−16	−9.5	−5	μA
Input leak current	$I_{IH(3)}$	$\overline{INH}$	20	V_{IN} = V_{DD}	0		5	μA
	$I_{IL(2)}$	$\overline{INH}$	20	V_{IN} = V_{SS}	−5		0	μA
Supply current	I_{ref}	V_{ref}	8	CR3,OSC = V_{DD}, CNF,$\overline{INH}$ = V_{SS}, others: open	0		3	mA
	I_{DD}	V_{DD}	9	CR3,OSC, V_{ref} = V_{DD} C_{NF},$\overline{INH}$ = V_{SS} others: open	0		2.5	mA

Note: Current direction (+, no sign: Flowing into device, −: Flowing out of device)

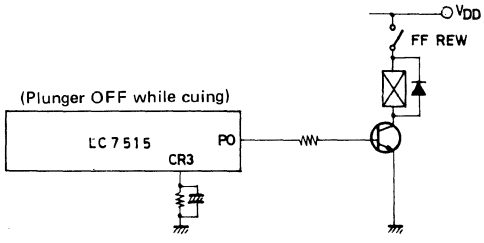
EQUIVALENT CIRCUIT BLOCK DIAGRAM



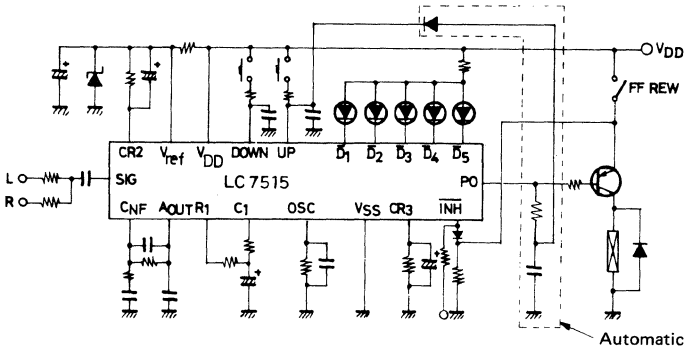
■ **SAMPLE APPLICATION CIRCUIT 1**



■ **SAMPLE APPLICATION CIRCUIT 2**

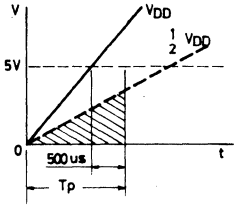


■ **SAMPLE APPLICATION CIRCUIT 3** Automatic programming of preceding or following 1 piece of music at the time of application of power or completion of cuing (Plunger ON while cuing)



Automatic programming of preceding or following 1 piece of music at the time of completion of cuing

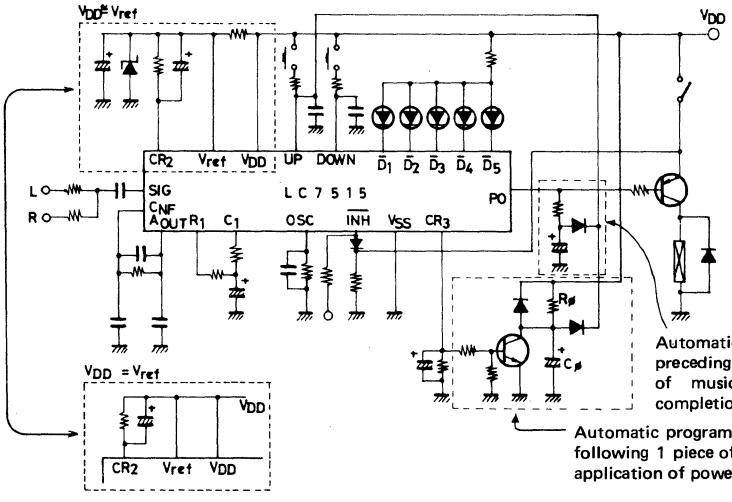
In this application, V_{DD} and V_{ref} rise modes must meet the following condition.



V_{ref} level must not exceed $1/2V_{DD}$ during T_P period.

* If V_{DD} and V_{ref} fall modes are $V_{DD} \fallingdotseq V_{ref}$ or V_{DD} = Vref, Sample Application Circuit 4 shown below can be used for automatic programming of preceding or following 1 piece of music.

■ **SAMPLE APPLICATION CIRCUIT 4** Automatic programming of preceding or following 1 piece of music at the time of application of power or completion of cuing (Plunger ON while cuing)



Automatic programming of preceding or following 1 piece of music at the time of completion of cuing

Automatic programming of preceding or following 1 piece of music at the time of application of power

- Condition
  V_{DD} rise time must be much shorter than $R\phi \cdot C\phi$ time constant.

■ **Operation Description**

(1) Application of power

Initialization at the time of application of power is made automatically by the initialization circuit, that is to say, the undermentioned $\overline{\text{INH}}$ F.F is set and the timing generator and cuing logic unit are initialized. (Refer to Block Diagram.)

(2) Cuing operation start

The cuing operation is started by changing-over the level of $\overline{\text{INH}}$ pin from "L" to "H" while power supply is applied.

In order that (1) when the cuing operation is started with any unrecorded area, this area is prevented from being sensed and (2) when the REW cuing operation is started with any head of music, the unrecorded area immediately following this head is prevented from being sensed, the unrecorded area sense unit functions as follows:

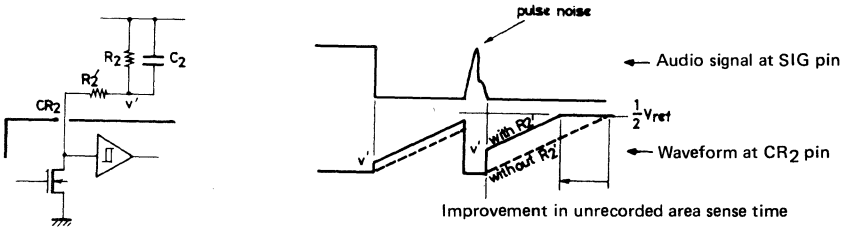
In either mode of these two where the cuing operation is started, C1 is discharged and the $\overline{\text{INH}}$ F.F is set. Therefore, for (1), audio signal is inputted to SIG pin and P channel transistor at R1 pin is turned ON and C1 is charged up through external resistor R1. When the charged-up voltage exceeds the check level of the Schmitt comparator at C1 pin, the output (recorded area sense clock) of the Schmitt comparator at C1 pin is set at "H" level, the $\overline{\text{INH}}$ F.F is reset, and unrecorded area sense operation in (3) is started. (Refer to period (A) of Timing Chart.)

For (2), since the cuing operation is started with the head of music (recorded area), C1 is charged up immediately. However, next unrecorded area comes before C1 charge-up voltage reaches the check level of the Schmitt comparator during the period of C1·R1 time constant and C1 is discharged by the built-in N channel transistor. Thus, the $\overline{\text{INH}}$ F.F is not reset and the same operation as in (1) occurs thereafter and the unrecorded area sense operation is entered.

When releasing inhibit mode with the mechanism-coupled switch, some delay between switch ON/OFF signal and $\overline{\text{INH}}$ pin input signal may be required. With the Schmitt inverter built in $\overline{\text{INH}}$ pin, this delay can be caused easily with an external integrator.

(3) When audio signal is inputted from SIG pin, N channel transistor at CR2 pin is turned ON and set at "L" level. External capacitor (C2) is charged up. When tape comes to the unrecorded area and audio signal disappears, N channel transistor at CR2 pin is turned OFF. Capacitor (C2) starts discharging through external resistor (R2). When CR2 pin voltage rises and exceeds the check level of the built-in Schmitt comparator, Schmitt comparator output (unrecorded area sense clock) changes from "H" level to "L" level and the unrecorded area is counted. (Refer to (A) → (B) of Time Chart.)

As a precaution to be taken in application, it should be noted that the following phenomenon may occur. If pulse noise exists during the unrecorded area sense operation, N channel transistor at CR2 pin is turned ON, external capacitor is charged up instantaneously, and a period of discharge time set up again is needed, and thereby the unrecorded area sense operation goes imperfect. To avoid this phenomenon, the unrecorded area sense time is improved by inserting resistor R2′ between CR2 pin and external C2, R2.



Improvement in unrecorded area sense time

Unrecorded area sense time t can be calculated by the following formula.

$$t = C_2R_2 \ln\left(\frac{1}{1-\frac{(1/2V_{ref} \pm 250mV)}{V_{ref}}}\right)$$

±250mV : Schmitt comparator offset

$$t(typ) = C_2R_2 \ln 2 = 0.693 C_2R_2$$

With no offset of Schmitt comparator

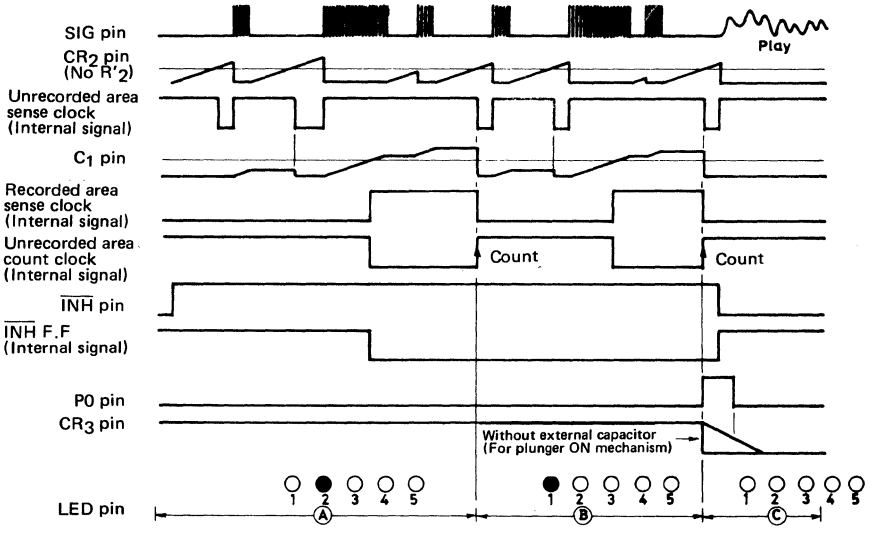
C_2 : External capacitor capacitance (F)

R_2 : External resistor resistance (ohm)

(4) Recorded area sense operation

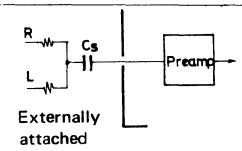
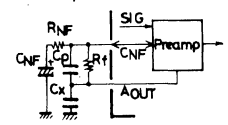
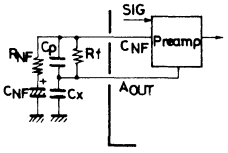
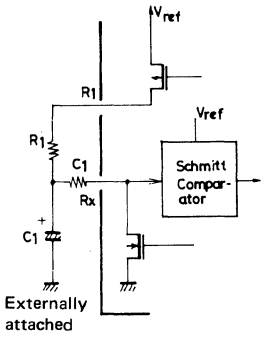
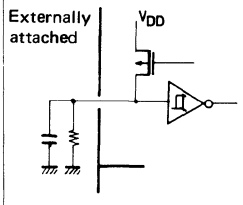
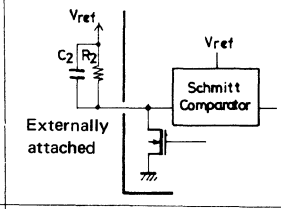
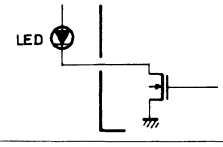
When the unrecorded area is sensed, external capacitor at C1 pin is discharged in readiness for next recorded area sense operation and Schmitt comparator output (recorded area sense clock) at C1 pin is set at "L" level. The unrecorded area count clock is a NAND output of recorded area sense clock and unrecorded area sense clock and unrecorded area count operation is performed only when unrecorded area count clock is changed-over from "L" level to "H" level. Therefore, when recorded area sense clock is set at "L" level, unrecorded area count clock remains at "H" level regardless of unrecorded area sense clock mode and unrecorded area count operation is stopped. This mode remains until C1 is charged up and Schmitt comparator output at C1 pin is set at "H" level after the continuation of recorded mode for the period of time fixed by C1, R1. When recorded area sense clock is set at "H" level at the time unrecorded area sense clock is at "H" level, unrecorded area sense clock is set at "L" level and unrecorded area count standby mode takes place. When next unrecorded area is sensed, count operation is performed. As a result, pulse noise existing within the period of time fixed by C1, R1 is not identified as a recorded mode and unrecorded area which follows noise is not counted. (Refer to period (B) of Pulse Noise Reject Operation Time Chart.) C1 is discharged each time unrecorded area is sensed and the interval between pulse noises is fixed by C, R2. If longer than unrecorded area sense time, C1 is not charged up and pulse noise can be rejected, no matter how many times pulse noise occurs. Operations of (3) to (4) are repeated thereafter.

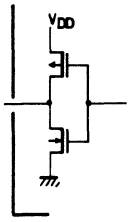
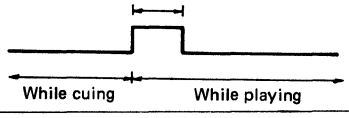
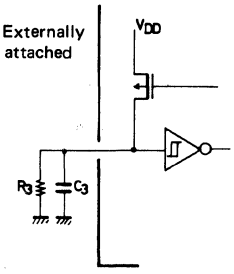
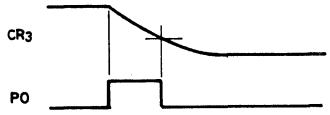
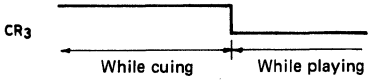
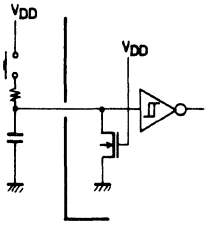
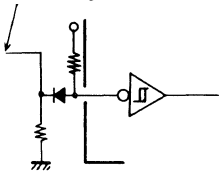
Unrecorded Area Count Operation Timing Chart



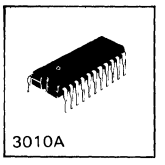
PIN DESCRIPTION

Pin Name	Pin No.	Input/Output	Pin Description
V_{DD} V_{SS}	9 10		• Pin for applying power V_{SS} = 0V, V_{DD} = 5.0 ~ 11.0V
V_{ref}	8		• Fixes check level of comparator, Schmitt comparator inside IC and supplies bias voltage of preamp. • Source power supply for P channel open drain transistor at R1 pin • To secure accurate cuing operation, voltage of this pin must be stabilized with Zener diode, etc. connected outside IC.

Pin Name	Pin No.	Input/Output	Pin Description
SIG	3		• Input pin for unrecorded area sense audio signal • Preamp. (input impedance 150kohm typ.) is built in and input sensitivity is −52dBm (typ.). • Biased 3/8Vref(typ.) at pin open mode and used with capacitor coupling
C_{NF}	2	Externally attached 	• Pin for setting preamp. gain. Used for AC amp. by connecting C, R between this pin and GND. Use capacitor with little leak current. • Biased 3/8Vref (typ.) at pin open mode
A_{out}	1		• Pin for setting preamp. gain. Used by connecting C, R between this pin and C_{NF}. • Pin for setting preamp. attenuation at high frequencies. Used by connecting C between this pin and GND.
R_1 C_1	4 5		• Pin for connecting external resistor which forms recorded area sense integrator • By connecting high resistor between this pin and C1, C1 is charged up through this resistor while being in recorded area. (Note) Recorded area sense time differs according to high input or low input. • P channel open drain • Pin for connecting external capacitor which forms recorded area sense integrator • With built-in Schmitt comparator, recorded area sense operation is performed when pin voltage exceeds 1/2Vref. • Each time unrecorded area is sensed, capacitor is discharged, so recorded area sense integral action is repeated and pulse noise in unrecorded area is rejected. • To prevent latch-up, RX is recommended.
OSC	6		• Pin for external CR for oscillator needed to operate internal logic unit. • Oscillation occurs only at the time of counting unrecorded area or changing program, and no oscillation occurs at the time of other than these operations. • Response time elapsing until program is changed after program switch (UP or DOWN) is turned ON is 3 times (3 x Tosc) as long as oscillation cycle (Tosc). • By increasing CR time constant, program SW chattering can be rejected.
CR_2	7		• Pin for external CR which set unrecorded area sense time • With built-in Schmitt comparator, unrecorded area sense operation is performed when pin voltage exceeds 1/2Vref. • Unrecorded area sense time (t) is calculated by the following formula. $t(typ.)=0.693C_2R_2$ C_2: External capacitor capacitance (F) R_2: External resistor resistance (ohm)
$\overline{D_1}$ $\overline{D_2}$ $\overline{D_3}$ $\overline{D_4}$ $\overline{D_5}$	15 14 13 12 11		• Output pin for LED driver for displaying programmed number of musics • N channel open drain output

Pin Name	Pin No.	Input/Output	Pin Description
PO	16		• Pin for outputting positive pulse after completion of cuing. Pulse width depends on time constant of CR externally attached to CR3 pin. • C MOS complementary output Pulse width: Depending on CR at CR_3 pin 
CR_3	17	Externally attached 	• Pin for external CR which fixes output pulse width at P_O pin • Input/output pin with built-in Schmitt type inverter  • Output pin for driving plunger-ON mechanism (while cuing) at no program mode at the time of completion of cuing and application of power In this case, resistor only is connected and no capacitor is used. (Refer to Sample Application Circuit 1.)  • When number of musics is programmed, high level is outputted. • P channel open drain output
UP	18		• Input pin for setting number-of-musics program in upward direction $\rightarrow \bar{D}_1 \rightarrow \bar{D}_2 \rightarrow \bar{D}_3 \rightarrow \bar{D}_4 \rightarrow \bar{D}_5 \rightarrow$ (Endless setting) • With pull-down resistor and Schmitt inverter built in internally, chattering can be rejected only by adding external resistor and capacitor. • Internal logic operates at switch input rise.
DOWN	19		• Input pin for setting number-of-musics program in downward direction $\leftarrow \bar{D}_1 \leftarrow \bar{D}_2 \leftarrow \bar{D}_3 \leftarrow \bar{D}_4 \leftarrow \bar{D}_5 \leftarrow$ (Endless setting) • Other functions are the same as for input pin for setting number-of-musics program in upward direction.
$\overline{INH}$	20	High level while unrecorded area sensing 	• Pin for inhibiting operation of unrecorded area sense unit and recorded area sense unit • Input low level causes inhibit mode. • Normally, inhibit mode is released only while cuing. • It is possible to freely program number of musics even at inhibit mode. • With built-in Schmitt inverter and FF which memorizes inhibit mode

LC7517


3010A

C MOS IC

Automatic Cuing Circuit for Tape Recorder

Ⓔ 1232A

The LC7517 is a C-MOS IC that enables automatic forward or backward cuing of your desired music up to 7 pieces from musics recorded on a tape recorder tape.

Application

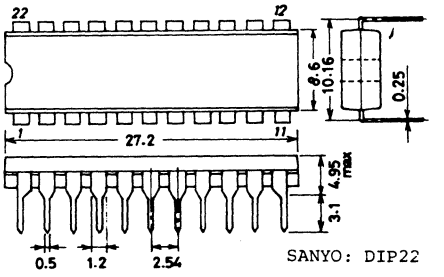
- Radio cassettes, cassette decks, car stereos

Features

- Preamp., unrecorded area sense unit, and 7-piece cuing logic unit are built in.
- Unrecorded area sense time and recorded area sense time are set independently by external CR, so that stable operation is made possible against pulse noise in unrecorded area and sound cut in recorded area.
- For programming the number of musics to be cued, serial set (endless) mode in up/down direction is available.
- It is possible to direct drive 7 LEDs for displaying the number of programmed musics.
- At the time of cuing and power application, no program mode takes place. Automatic 1-piece programming is also enabled by external circuit. (Refer to Sample Application Circuits 3, 4.)
- Meets the requirements for deck mechanisms of 2 types (1. plunger OFF while cuing, 2. plunger ON while cuing).
- Input sensitivity: −52 dBm typ (f = 10 kHz)
- Wide operating voltage range (V_{DD} = 5.0 to 11.0 V) and small current dissipation ($I_{DD} \leqq 2.5$ mA)

Absolute Maximum Ratings/T_a = 25°C, V_{SS} = 0 V		Pin Name	Pin No.	Condition		unit
Maximum supply voltage	V_{DD} max	V_{DD}	9		V_{SS} −0.3 ~ V_{SS}+12	V
Reference voltage	V_{ref}	V_{ref}	8	$V_{ref} \leqq V_{DD}$	V_{SS}−0.3 ~ V_{SS}+11	V
Input voltage	V_{IN}	C_{NF}, SIG, UP'DOWN, $\overline{INH}$	2,3,20 21,22		V_{SS}−0.3 ~ V_{DD}+0.3	V
Output voltage	V_{OUT}	A_{OUT},R1, C1,OSC, CR2,Po, CR3,$\bar{D}$1 ~ $\bar{D}$7	1,4,5,6, 7,18,19, 17 ~ 11	Output transistor off	V_{SS}−0.3 ~ V_{DD}+0.3	V
Output current	I_{OUT}	$\bar{D}$1 ~ $\bar{D}$7	17 ~ 11		30	mA
Allowable power dissipation	P_d max			$T_a \leqq 75$°C	300	mV
Operating temperature	T_{opg}				−30 ~ +75	°C
Storage temperature	T_{stg}				−40 ~ +125	°C

Case Outline 3010A-D22IC
(unit:mm)



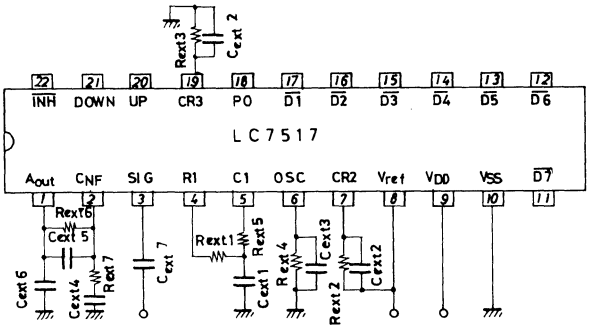
SANYO: DIP22

Allowable Operating Ranges/T_a = 25°C, V_{SS} = 0V		Pin Name	Pin No.	Condition	min	typ	max	unit
Supply voltage	V_{DD}	V_{DD}	9		5		11	V
Reference voltage	V_{ref}	V_{ref}	8	$V_{ref} \leqq V_{DD}$	4		11	V
"H" level input voltage	V_{IH}	CR3,UP, DOWN,$\overline{INH}$	19,20 21,22		0.8V_{DD}		V_{DD}	V
"L" level input voltage	V_{IL}	UP,DOWN, $\overline{INH}$	20,21,22		V_{SS}		0.2V_{DD}	V
External capacitor	$C_{EXT(1)}$	C1	5	See Fig. 1.		1.0	2.2	μF
External capacitor	$C_{EXT(2)}$	CR2,CR3	7,19	See Fig. 1.		1.0	10	μF
External capacitor	$C_{EXT(3)}$	OSC	6	See Fig. 1.		0.01	2.2	μF
External capacitor	$C_{EXT(4)}$	C_{NF}	2	See Fig. 1.	0.47	1.0	1.2	μF
External capacitor	$C_{EXT(5)}$	A_{OUT}–C_{NF}	1,2	See Fig. 1.	33	36	39	pF
External capacitor	$C_{EXT(6)}$	A_{OUT}	1	See Fig. 1.	470	1000	1500	pF
External capacitor	$C_{EXT(7)}$	SIG	3	See Fig. 1.		0.1	2.2	μF
External resistor	$R_{EXT(1)}$	R1	4	See Fig. 1.	0	100	430	kΩ
External resistor	$R_{EXT(2)}$	CR2	7	See Fig. 1.	0.68	100	430	kΩ
External resistor	$R_{EXT(3)}$	CR3	19	See Fig. 1.	1	100	240	kΩ
External resistor	$R_{EXT(4)}$	OSC	6	See Fig. 1.	0.68	100	510	kΩ
External resistor	$R_{EXT(5)}$	C1	5	See Fig. 1.	0.68	1	10	kΩ
External resistor	$R_{EXT(6)}$	A_{OUT}–C_{NF}	1,2	See Fig. 1.	180	240	300	kΩ
External resistor	$R_{EXT(7)}$	C_{NF}	2	See Fig. 1.	0.51	1	3	kΩ

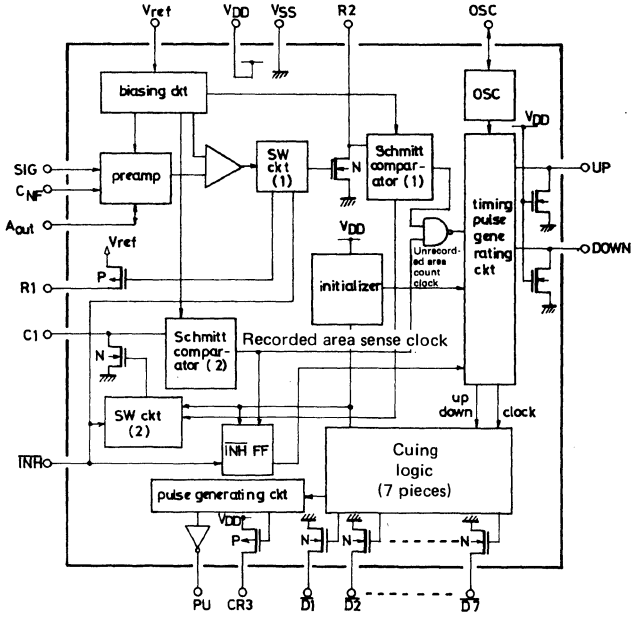
Electrical Characteristics/T_a = 25°C, V_{SS} = 0V, V_{DD} = V_{ref} = 5 ~ 9V		Pin Name	Pin No.	Condition	min	typ	max	unit
Input threshold voltage	Vt	SIG	3	GAIN,48dB, V_{DD} = 5V, f = 10kHz	–55 (1.38)	–52 (1.95)	–49 (2.75)	dBm (mV)
	$V_{tL(1)}$	CR3	19	V_{DD} = 5 ~ 6V	0.25V_{DD}		0.7V_{DD}	V
	V_{tH}	C1,CR2	5,7	V_{DD} = 5 ~ 6V	0.5V_{ref} –250		0.5V_{ref} +250	mV
	$V_{tL(2)}$	C1,CR2	5,7	V_{DD} = 5 ~ 6V	3/8 V_{ref} –250		3/8V_{ref} +250	mV
"H" level output voltage	V_{OH}	Po,CR3	18,19	I_{OH} = –10mA	V_{DD}–2.5		V_{DD}	V
"L" level output voltage	$V_{OL(1)}$	$\overline{D}$1 ~ $\overline{D}$7	17 ~ 13	I_{OL} = 25mA	V_{SS}		V_{SS}+1.9	V
	$V_{OL(2)}$	Po	18	I_{OL} = 10mA	V_{SS}		V_{SS}+2.5	V
Output OFF leak current	$I_{OFF(1)}$	R1,OSC, CR3	4,6,19	V_{OUT} = V_{SS}	–5		0	μA
	$I_{OFF(2)}$	C1,CR2	5,7	V_{OUT} = V_{DD}	0		5	μA
	$I_{OFF(3)}$	$\overline{D}$1 ~ $\overline{D}$7	5 ~ 13	V_{OUT} = V_{DD}	0		5	μA
Output ON resistance	$R_{ON(1)}$	C1,CR2	5 ~ 7	V_{DD} = 5V, V_{OUT} = V_{DD}	0		300	Ω
	$R_{ON(2)}$	R1	4	V_{DD} = 5V V_{OUT} = V_{SS}	0		1	kΩ
Input impedance	Z_{IN}	SIG	3	C_{NF} : AC grounded, f = 10 kHz	100	170	260	kΩ
"H" level input current	$I_{IH(1)}$	SIG	3	V_{ref} = V_{DD} = 5V V_{IN} = V_{DD}	11.5	19.5	32.5	μA
	$I_{IH(2)}$	UP,DOWN	20,21	V_{DD} = 5V V_{IN} = V_{DD}	10	50	100	μA
"L" level input current	$I_{IL(1)}$	SIG	3	V_{ref} = V_{DD} = 5V V_{IN} = V_{SS}	–16	–9.5	–5	μA
Input leak current	$I_{IH(2)}$	$\overline{INH}$	22	V_{IN} = V_{SS}	–5		0	μA
	$I_{IH(3)}$	$\overline{INH}$	22	V_{IN} = V_{DD}	0		5	μA
Supply current	I_{ref}	V_{ref}	8	CR3,OSC = V_{DD} C_{NF},$\overline{INH}$ = V_{SS}, others: open	0		3	mA
	I_{DD}	V_{DD}	9	CR3,OSC,V_{ref} = V_{DD} C_{NF},$\overline{INH}$ = V_{SS} others: open	0		2.5	mA

(Note) Current direction (+, no sign: Flowing into device, –: Flowing out of device)

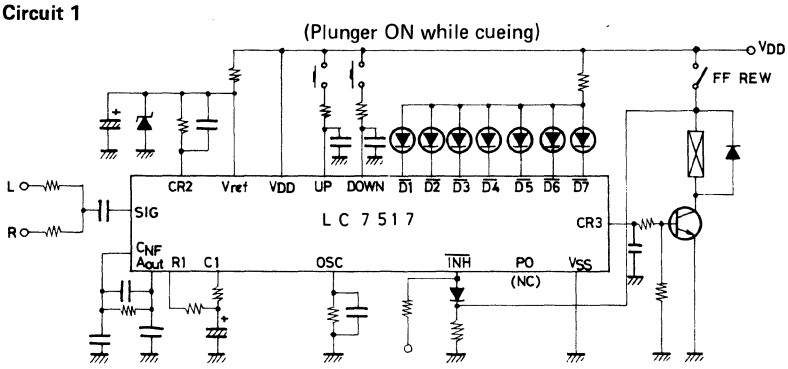
Pin Assignment and Test Circuit (Fig. 1)



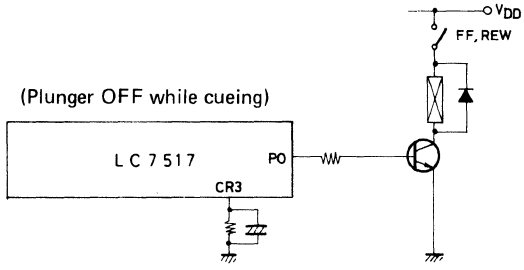
Equivalent Circuit Block Diagram



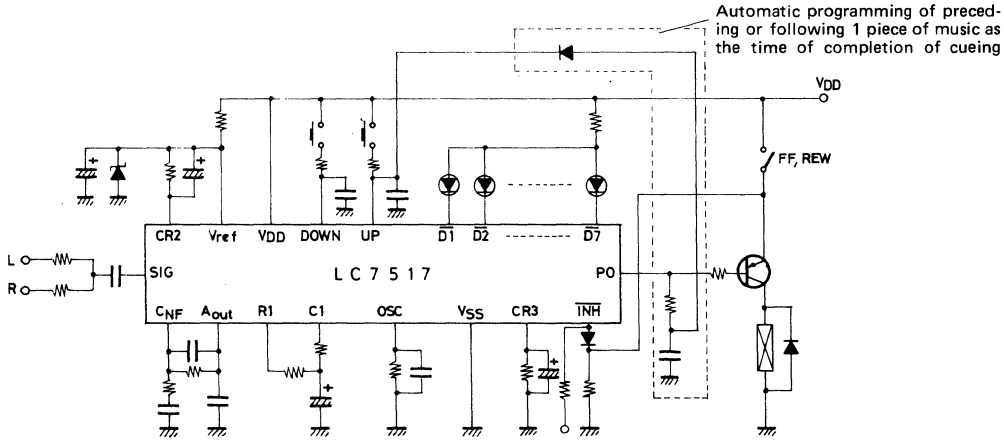
Sample Application Circuit 1



Sample Application Circuit 2

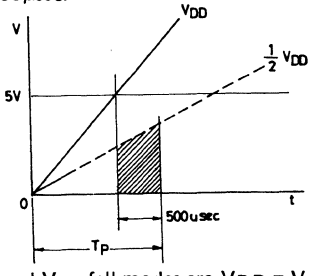


Sample Application Circuit 3: Automatic programming of preceding or following 1 piece of music at the time of application of power or completion of cuing (Plunger ON while cuing)



For automatic programming of preceding or following 1 piece of music at the time of application of power, V_{ref} rise mode must meet the following condition.

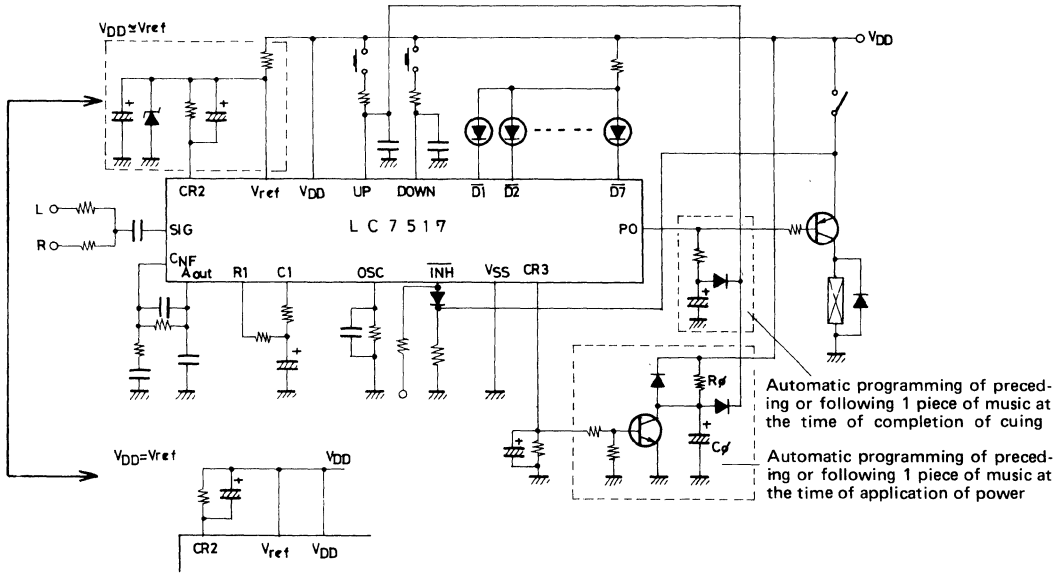
V_{ref} must not exceed 1/2 V_{DD} during the period of time elapsed until V_{DD} reaches 5V after application of power +500μsec.



- V_{ref} level must not exceed 1/2 V_{DD} during T_p period.
- Must be within the shadowed portion shown left.

*If V_{DD} and V_{ref} fall modes are $V_{DD} = V_{ref}$ or $V_{DD} \doteqdot V_{ref}$, Sample Application Circuit 4 shown below can be used for automatic programming of preceding or following 1 piece of music.

Sample Application Circuit 4: Automatic programming of preceding or following 1 piece of music at the time of application of power or completion of cuing (Plunger ON while cuing)



(Note)
V_{DD} rise time must be much shorter than Rφ·Rφ time constant.

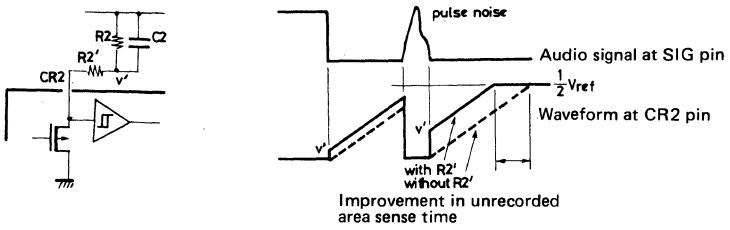
Operation Description

1) Application of power
Initialization at the time of application of power is made automatically by the initialization circuit, that is to say, the undermentioned $\overline{INH}$ F.F is set and the timing generator and cuing logic unit are initialized. (Refer to Block Diagram.)

2) Cuing operation start
The cuing operation is started by changing-over the level of $\overline{INH}$ pin from "L" to "H" while power supply is applied. In order that (1) when the cuing operation is started with any unrecorded area this area is prevented from being sensed and (2) when the REW cuing operation is started with any head of music the unrecorded area immediately following this head is prevented from being sensed, the unrecorded area sense unit functions as follows: In either mode of these two where the cuing operation is started, C1 is discharged and the $\overline{INH}$ F.F is set. Therefore, for (1), audio signal is inputted to SIG pin and P channel transistor at R1 pin is turned ON and C1 is charged up through external resistor R1. When the charged-up voltage exceeds the check level of the Schmitt comparator at C1 pin, the output (recorded area sense clock) of the Schmitt comparator at C1 pin is set at "H" level, the $\overline{INH}$ F.F is reset, and unrecorded area sense operation in (3) is started. (Refer to period (A) of Time Chart.) For (2), since the cuing operation is started with the head of music (recorded area), C1 is charged up immediately. However, next unrecorded area comes before C1 charge-up voltage reaches the check level of the Schmitt comparator during the period of C1·R1 time constant and C1 is discharged by the built-in N channel transistor. Thus, the $\overline{INH}$ F.F is not reset and the same operation as in (1) occurs thereafter and the unrecorded area sense operation is entered. When releasing inhibit mode with the mechanism-coupled switch, some delay between switch ON/OFF signal and $\overline{INH}$ pin input signal may be required. With the Schmitt inverter built in $\overline{INH}$ pin, this delay can be caused easily with an external integrator.

3) When audio signal is inputted from SIG pin, N channel transistor at CR2 pin is turned ON and set at "L" level. External capacitor (C2) is charged up. When tape comes to the unrecorded area and audio signal disappears, N channel transistor at CR2 pin is turned OFF. Capacitor (C2) starts discharging through external resistor (R2). When CR2 pin voltage rises and exceeds the check level of the built-in Schmitt comparator, Schmitt comparator output (unrecorded area sense clock) changes from "H" level to "L" level and the unrecorded area is counted. (Refer to (A) → (B) of Time Chart.) As a precaution to be taken in application, it should be noted that the

following phenomenon may occur. If pulse noise exists during the unrecorded area sense operation, N channel transistor at CR2 pin is turned ON, external capacitor is charged up instantaneously, and a period of discharge time set up again is needed, and thereby the unrecorded area sense operation goes imperfect. To avoid this phenomenon, the unrecorded area sense time is improved by inserting resistor R2′ between CR2 pin and external C2, R2.



Unrecorded area sense time t can be calculated by the following formula.

$$t = C_2R_2 \ln \left(\frac{1}{1 - \dfrac{1/2\ V_{ref} \pm 250\ \text{mV}}{V_{ref}}} \right)$$

±250 mV : Schmitt comparator offset

$t\ (\text{typ}) = C2R2\ln 2 = 0.693C2R2$

With no offset of Schmitt comparator

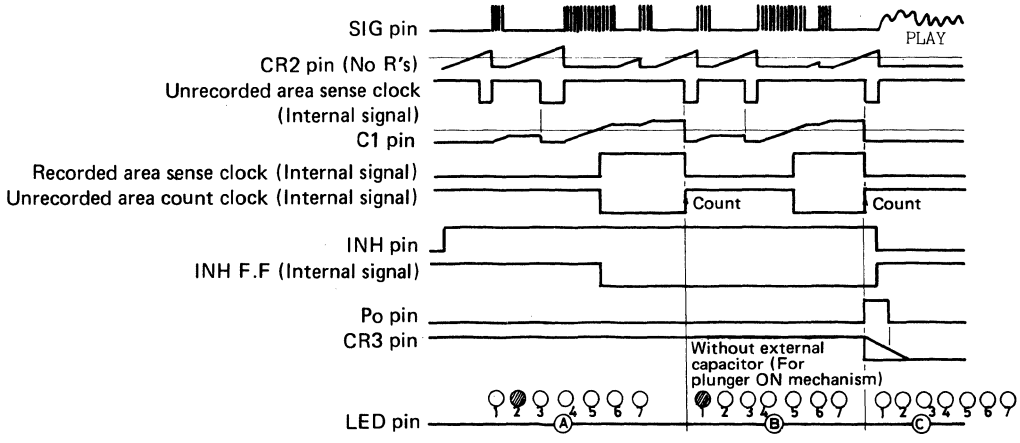
C2 : External capacitor capacitance (F)

R2 : External resistor resistance (ohm)

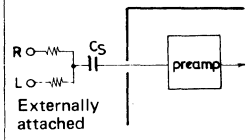
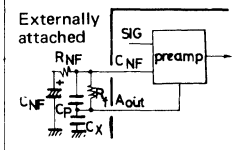
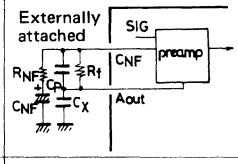
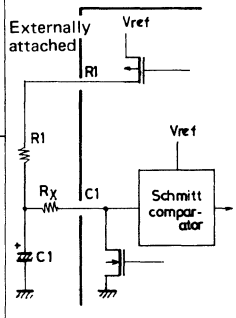
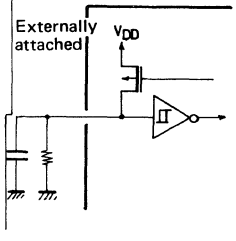
4) Recorded area sense operation

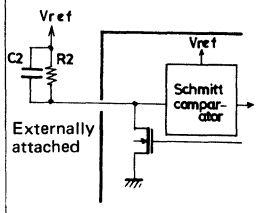
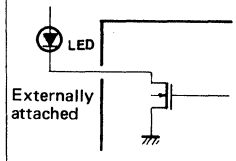
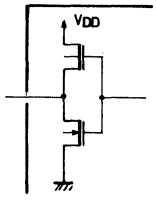
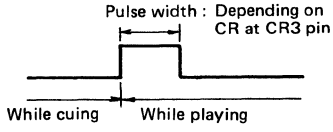
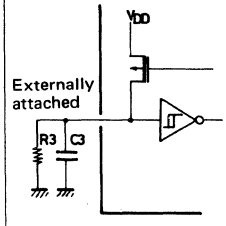
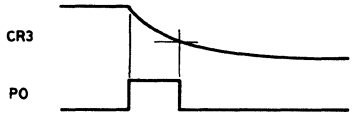
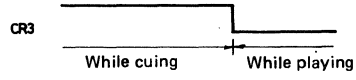
When the unrecorded area is sensed, external capacitor at C1 pin is discharged in readiness for next recorded area sense operation and Schmitt comparator output (recorded area sense clock) at C1 pin is set at "L" level. The unrecorded area count clock is a NAND output of recorded area sense clock and unrecorded area sense clock and unrecorded area count operation is performed only when unrecorded area count clock is changed-over from "L" level to "H" level. Therefore, when recorded area sense clock is set at "L" level, unrecorded area count clock remains at "H" level regardless of unrecorded area sense clock mode and unrecorded area count operation is stopped. This mode remains until C1 is charged up and Schmitt comparator output at C1 pin is set at "H" level after the continuation of recorded mode for the period of time fixed by C1, R1. When recorded area sense clock is set at "H" level at the time unrecorded area sense clock is at "H" level, unrecorded area sense clock is set at "L" level and unrecorded area count standby mode takes place. When next unrecorded area is sensed, count operation is performed. As a result, pulse noise existing within the period of time fixed by C1, R1 is not identified as a recorded mode and unrecorded area which follows noise is not counted. (Refer to period (B) of Pulse Noise Reject Operation Time Chart.) C1 is discharged each time unrecorded area is sensed and the interval between pulse noises is fixed by C, R2. If longer than unrecorded area sense time, C1 is not charged up and pulse noise can be rejected, no matter how many times pulse noise occurs. Operations of (3) to (4) are repeated thereafter.

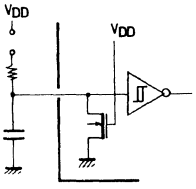
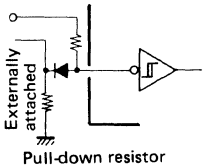
Unrecorded Area Count Operation Timing Chart



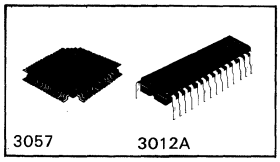
Pin Description

Pin Name	Pin No.	Input/Output	Pin Description
V_{DD} V_{SS}	9 10		• Pin for applying power: V_{SS} = 0V, V_{DD} = 5.0 ~ 11.0V
V_{ref}	8		• Fixes check level of comparator, Schmitt comparator inside IC and supplies bias voltage of preamp. • Source power supply for P channel open drain transistor at R1 pin • To secure accurate cuing operation, voltage of this pin must be stabilized with Zener diode, etc. connected outside IC.
SIG	3		• Input pin for unrecorded area sense audio signal • Preamp. (input impedance 150kohm typ.) is built in and input sensitivity is –52dBm (typ.). • Biased 3/8V_{ref} (typ.) at pin open mode and used with capacitor coupling
C_{NF}	2		• Pin for setting preamp. gain. Used for AC amp. by connecting C, R between this pin and GND. Use capacitor with little leak current. • Biased 3/8V_{ref} (typ.) at pin open mode
A_{OUT}	1		• Pin for setting preamp. gain. Used by connecting C, R between this pin and C_{NF}. • Pin for setting preamp. attenuation at high frequencies. Used by connecting C between this pin and GND.
R1	4		• Pin for connecting external resistor which forms recorded area sense integrator • By connecting high resistor between this pin and C1, C1 is charged up through this resistor while being in recorded area. (Note) Recorded area sense time differs according to high input or low input. • P channel open drain
C1	5		• Pin for connecting external capacitor which forms recorded area sense integrator • With built-in Schmitt comparator, recorded area sense operation is performed when pin voltage exceeds 1/2V_{ref}. • Each time unrecorded area is sensed, capacitor is discharged, so recorded area sense integral action is repeated and pulse noise in unrecorded area is rejected. • To prevent latch-up, R_X is recommended.
OSC	6		• Pin for external CR for oscillator needed to operate internal logic unit • Oscillation occurs only at the time of counting unrecorded area or changing program, and no oscillation occurs at the time of other than these operations. • Response time elapsing until program is changed after program switch (UP or DOWN) is turned ON is 3 times (3 x Tosc) as long as oscillation cycle (Tosc).

Pin Name	Pin No.	Input/Output	Pin Description
OSC	6	See the former page.	• By increasing CR time constant, program SW chattering can be rejected.
CR2	7		• Pin for external CR which set unrecorded area sense time • With built-in Schmitt comparator, unrecorded area sense operation is performed when pin voltage exceeds $1/2V_{ref}$. • Unrecorded area sense time (t) is calculated by the following formula. $t\ (typ) = 0.693C_2R_2$ C_2: External capacitor capacitance (F) R_2: External resistor resistance (ohm)
$\overline{D}1$ $\overline{D}2$ $\overline{D}3$ $\overline{D}4$ $\overline{D}5$ $\overline{D}6$ $\overline{D}7$	17 16 15 14 13 12 11		• Output pin for LED driver for displaying programmed number of musics • N channel open drain output
Po	18		• Pin for outputting positive pulse after completion of cuing • Pulse width depends on time constant of CR externally attached to CR3 pin. 
CR3	19		• Pin for external CR which fixes output pulse width at P_O pin • Input/output pin with built-in Schmitt type inverter • P channel open drain output  • Output pin for driving plunger-ON mechanism (while cuing) at no program mode at the time of completion of cuing and application of power In this case, resistor only is connected and no capacitor is used. (Refer to Sample Application Circuit 1.)  • When number of musics is programmed, high level is outputted.
UP	20	See next page.	• Input pin for setting number-of-musics program in upward direction $\rightarrow\overline{D}1\rightarrow\overline{D}2\rightarrow\overline{D}3\rightarrow\overline{D}4\rightarrow\overline{D}5\rightarrow\overline{D}6\rightarrow\overline{D}7\rightarrow$ (Endless setting)

Pin Name	Pin No.	Input/Output	Pin Description
UP	20	 Externally attached	• With pull-down resistor and Schmitt inverter built in internally, chattering can be rejected only by adding external resistor and capacitor. • Internal logic operates at switch input rise.
DOWN	21		• Input pin for setting number-of-musics program in downward direction $\overline{D1} \leftarrow \overline{D2} \leftarrow \overline{D3} \leftarrow \overline{D4} \leftarrow \overline{D5} \leftarrow \overline{D6} \leftarrow \overline{D7} \leftarrow$ (Endless setting) • Other functions are the same as for input pin for setting number-of-musics program in upward direction.
$\overline{INH}$	22	 Pull-down resistor	• Pin for inhibiting operation of unrecorded area sense unit and recorded area sense unit • Input low level causes inhibit mode. • Normally, inhibit mode is released only while cuing. • It is possible to freely program number of musics even at inhibit mode. • With built-in Schmitt inverter and FF which memorizes inhibit mode

LC7520, 7560



C MOS LSI

Graphic Equalizer ECS System, LCD Driver

Ⓔ 1523

TENTATIVE

Applications

Graphic equalizer	: LC7520	DIP28
LCD driver	: LC7560	QIP64-A
Control microcomputer	: LC6502	DIP42 128W + 2KB ROM or 64W + 1KB ROM

Functions

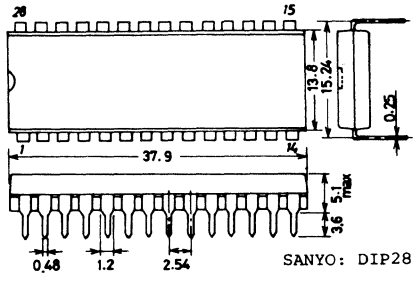
(1) LC7520
- 7 bands each of right/left.
- 2dB/step ±10dB (1 band 11 positions) variable with UP/DOWN switch.
- Microcomputer-controlled. 2 control lines.

(2) LC7560
- Dot display of setting state in each band (Flashable at the setting mode)
- Spectrum analyzing display of band-pass signal strength (7 bands, 2dB/step 11-dot display).
- Accessory display (11 kinds of MEMO, M1 to M5, R, L, MIX, LEVEL, POSITION) Total display also available.
- Display : 1/2 duty LCD (5V rating)
- Microcomputer-controlled. 2 control lines.

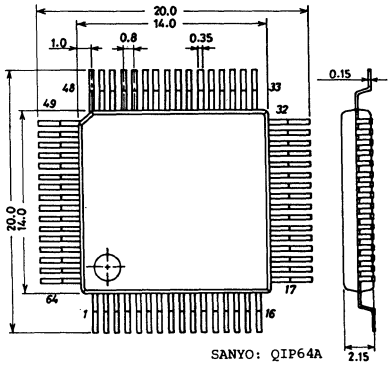
Features

(1) One touch permits the gain in each band to go up/down.
(2) Presetting makes memory call possible with one touch. Your desired frequency characteristic can be selected to the music.
(Example) User option 3 modes + Maker option 3 modes + Last channel memory
(3) One touch permits the frequency characeristic in each band to be set to 0dB (flat function). The frequency characteristic in each band can be reversed easily with respect to 0dB by means of software (reverse function).
(4) Spectrum analyzing display facilitates REC equalization.
(5) Two control lines are common to the LC7520/LC7560, thereby facilitating wiring between microcomputer and IC.

Case Outline 3012A-D28IC
(unit:mm) LC7520



Case Outline 3057-Q64AIC
(unit:mm) LC7560



LC7520

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max, V_{EE}	$V_{EE} \leq V_{SS}$	$V_{DD}-V_{EE} \leq 40$	V
	V_{ref}	$V_{SS} \leq Vref$	$V_{DD}-Vref \leq 11$	V
	V_{CC}		V_{SS} to $V_{SS}+7$	V
Input Voltage	V_{I1}	CLK,DI	$V_{SS}-0.3$ to $V_{CC}+0.3$	V
	V_{I2}	f1 to f7,IN1,IN2	$V_{EE}-0.3$ to $V_{DD}+0.3$	V
	V_{I3}	S	$Vref-0.3$ to $V_{DD}+0.3$	V
Output Voltage	V_O		$V_{EE}-0.3$ to $V_{DD}+0.3$	V
Allowable Power Dissipation	Pdmax	Ta≤75°C	150	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	$V_{EE} \leq V_{SS}$	$8 \leq V_{DD}-V_{EE} \leq 37$			V
	V_{EE}	$V_{CC}<V_{DD}$				
	V_{ref}	$V_{DD}-Vref \leq 10$	0		$V_{DD}-4.5$	V
	V_{CC}		4.5	5	5.5	V
Input "H" Level Voltage	$V_{IH(1)}$	CLK,DI	$0.8V_{CC}$		V_{CC}	V
	$V_{IH(2)}$	S	$Vref+0.9(V_{DD}-Vref)$		V_{DD}	V
Input "L" Level Voltage	$V_{IL(1)}$	CLK,DI	V_{SS}		$0.2V_{CC}$	V
	$V_{IL(2)}$	S	V_{ref}		$Vref+0.1(V_{DD}-Vref)$	V
Input Pulse Width	tøw	CLK	1			us
Setup Time	t_{setup}	DI	1			us
Hold Time	t_{hold}	DI	1			us
Delay Time	t_d	CLK			1	us

Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Distortion	THD	All bands flat, f=20kHz, Output 1V			0.005	%
Closstalk	X_{talk}		-60			dB
Setting Error	B	Other band flat	-1		1	dB
Analog SW OFF Leak	I_{OFF}	IN1,IN2,f1~f7			10	uA
Pull-down Resistance	Rpd	V_{DD}=13V,S		100		kohm
Current Dissipation	I_{DD}				1	mA
	I_{CC}				0.5	mA

LC7560

Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{DD}max		V_{SS} to V_{SS} +15	V
	V_{CC}		V_{SS} to $V_{SS}+7$	V
Input Voltage	V_{I1}	CLK,DI	$V_{SS}-0.3$ to $V_{CC}+0.3$	V
	V_{I2}	f1 to f7,T,S1,S2	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Voltage	V_O	A_1 to 11, B_1 to 11, D1 to 11, $COM_{1,2}$	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable Power Dissipation	Pdmax	Ta≤75°C	200	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

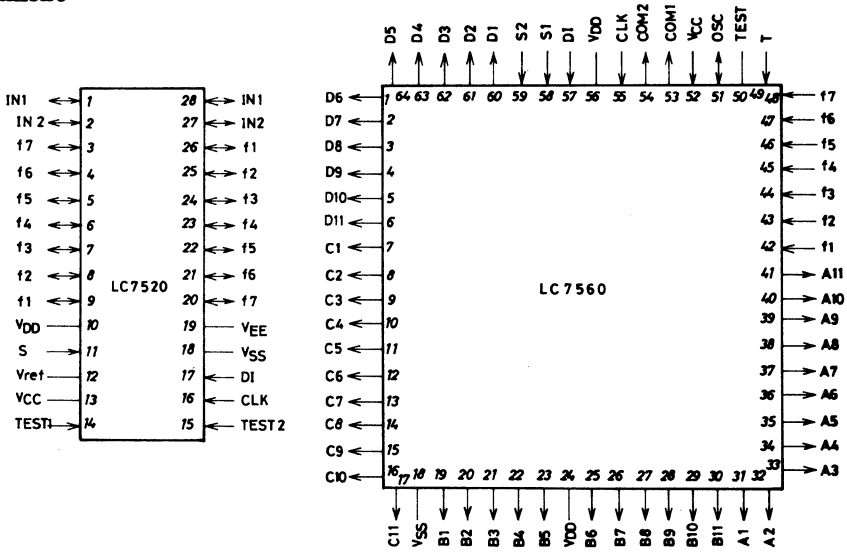
			min	typ	max	unit
Supply Voltage	V_{DD}		7.5	13	14	V
	V_{CC}		4.0	5	5.5	V
Input "H" Level Voltage	$V_{IH(1)}$	CLK,DI	$0.8V_{CC}$		V_{CC}	V
	$V_{IH(2)}$	S1,S2	$0.9V_{DD}$		V_{DD}	V

			min	typ	max	unit
Input "L" Level Voltage	$V_{IL(1)}$	CLK,DI	V_{SS}		$0.2V_{CC}$	V
	$V_{IL(2)}$	S1,S2	V_{SS}		$0.1V_{DD}$	V
Input Pulse Width	t_{pw}	CLK	1			us
Setup Time	t_{setup}	DI	1			us
Hold Time	t_{hold}	DI	1			us
Delay Time	t_d	CLK			1	us

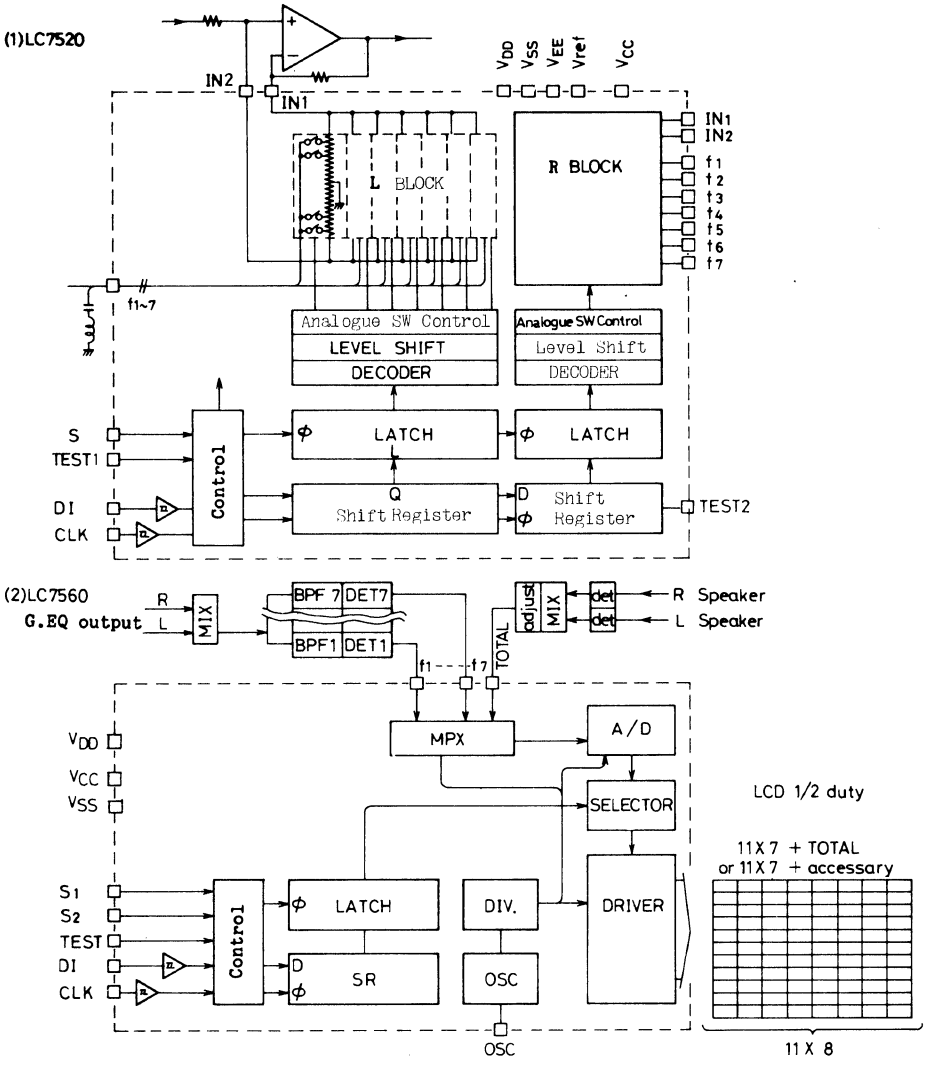
Electrical Characteristics at Ta=25°C

				min	typ	max	unit
Input Sensitivity	+10	V_{IN}		+9		+11	dB
	+8		V_{DD}=13V	+7		+9	dB
	+6		Specified circuit	+5		+7	dB
	+4			+3		+5	dB
	+2			+1		+3	dB
	0			-1		+1	dB
	-2			-3		-1	dB
	-4			-5		-3	dB
	-6			-7		-5	dB
	-8			-9		-7	dB
	-10			-11		-9	dB
Analog SW OFF Leak		I_{OFF}	f1~f7,T			10	uA
Output Impedance		Zo	COM1,2 A1~D11		10		kohm
Current Dissipation		I_{DD}				7	mA
		I_{CC}				1	mA

Pin Assignment



Equivalent Circuit Block Diagram



Pin Description

(1) LC7520

Pin Name	Pin Configuration	Description
V_{DD}		. Power supply pin +18V(typ) Power supply for audio signal.
Vref		. Power supply pin V_{DD}-5V(typ) Power supply for logic drive.
V_{SS}		. Power supply pin 0V.
V_{EE}		. Power supply pin -18V(typ) Power supply for audio signal.
V_{CC}		. Power supply pin +5V(typ).
D_I		. Pin for inputting data from CPU. . Schmitt inverter configuration.
CLK		. Pin for inputting CLK from CPU. . Schmitt inverter configuration.
IN1 IN2	IN1 IN2	. Pin for inputting audio signal. . Normally, IN1 is connected to inverting input of OP amp. . Normally, IN2 is connected to noninverting inut of OP amp. . Provided on right/left sides.
f1~f7		. Pin for connecting band-pass filter. . f1 to f7 x right/left ------- Total 14 pins.
S		. Select pin in 2-chip applications. With pull-down resistor. . "1" input: Key code 7C3 Connected to V_{DD}. . "0" input: Key code 7C2 Connected to Vref.
TEST1		. Pin for testing IC inside.
TEST2		. Normally, open.

(2) LC7560

Pin Name	Pin Configuration	Description
V_{DD}		. Power supply pin +13V(typ) Power supply for A/D conversion.
V_{CC}		. Power supply pin +5V(typ) Power supply for logic drive.
V_{SS}		. Power supply pin 0V(typ).
D_I		. Pin for inputting data from CPU. . Schmitt inverter configuration.
CLK		. Pin for inputting CLK from CPU. . Schmitt inverter configuration.
COM1 COM2		. Output pin to LCD common.
A1~A11		. Output pin to LCD segment. . Bands f1,f2.
B1~B11		. Output pin to LCD segment. . Bands f3,f4.
C1~C11		. Output pin to LCD segment. . Bands f5,f6.
D1~D11		. Output pin to LCD segment. . Band f7, total display or accessory display.
f1~f7		. Pin for inputting detection output of audio signal.

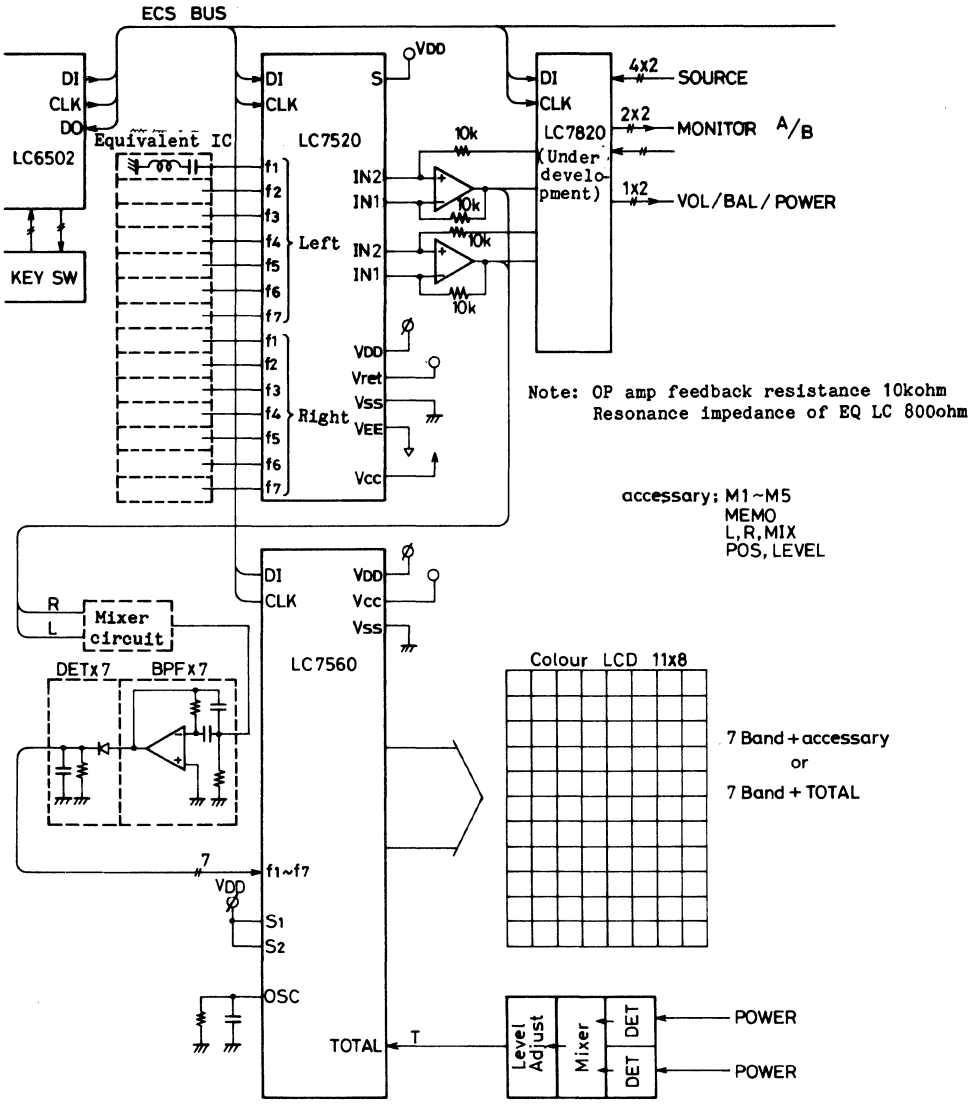
Pin Name	Pin Configuration	Description
T		. Input pin for total display. . Detection output is inputted.
OSC		. Open drain type output buffer. . Pin for connecting external C,R for oscillator.
S1,S2		. Select pin in applications where a plurality of chips (4 pcs. max.) are used.
TEST		. Pin for testing IC inside. . Normall, open.

(1) For the microcomputer, refer to the separate manual.
(2) For the control data and timing, a separate manual is in preparation.

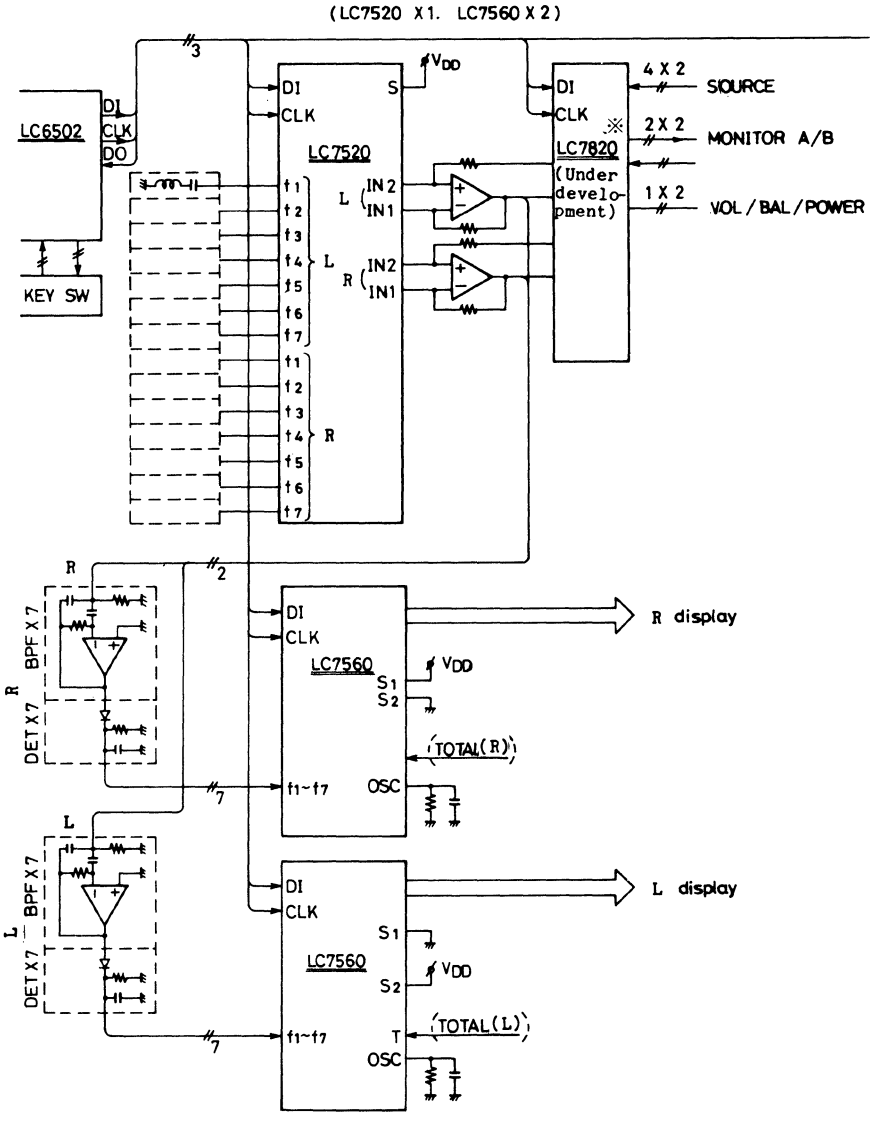
Sample Application Circuit

(1) 7-Band MIX Display(LC7520x1,LC7560x1)

(LC7520 X1 , LC7560 X1)

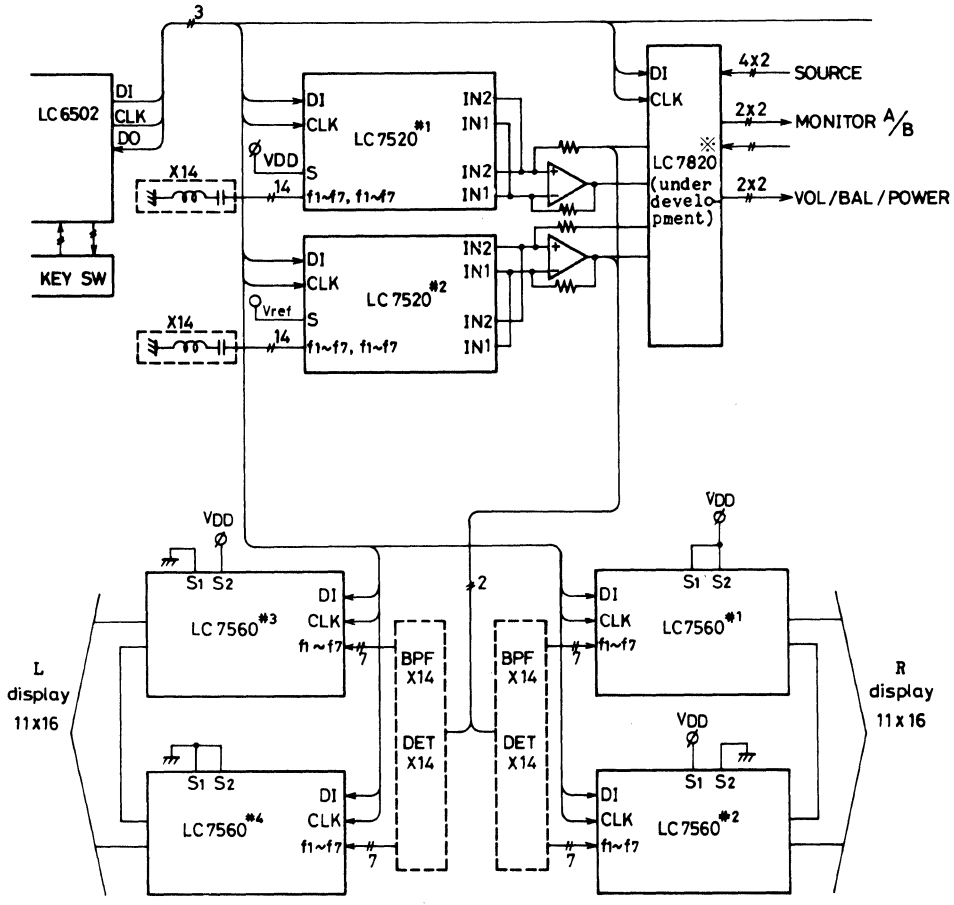


(2) 7-Band R, L Separate Display(LC7520x1,LC7560x2)

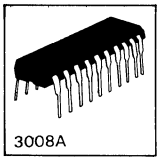


(3) 14-Band R, L Separate Display (LC7520x2, LC7560x4)

(LC7520 X2, LC7560 X4)



LC7530



C MOS LSI

Electronic Volume Controller

Ⓔ1278C

The LC7530, a C-MOS LSI, is an electronic volume controller for use in audio equipment. It is especially suited for use in adjusting the recording level of a tape deck, etc.

Features

- Has built-in dual channels.
- Attenuation curve approaching type A.
- Total resistance is 50kohm which can be varied in 16 steps.
- Attenuation amount (volume level) is displayed by means of 8 LED's.
- Has pins for volume up/down and initialization.

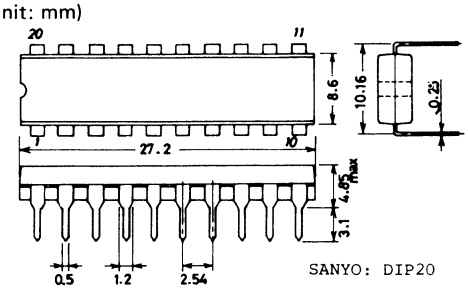
Absolute Maximum Ratings at T_a = 25°C

				Unit
Maximum supply voltage	V_{DDmax}		V_{SS}−0.3 to 16	V
Output applied voltage	V_o	IND1 to 8 off	V_{DD}−20 to V_{DD}+0.3	V
Output current	I_o	IND1 to 8 only	0 to 20	mA
Input applied voltage	V_i		V_{DD}−0.3 to V_{DD}+0.3	V
Allowable power dissipation	P_{dmax}		150	mW
Operating temperature	T_{opg}		−30 to +75	°C
Storage temperature	T_{stg}		−40 to +125	°C

Allowable Operating Ranges at T_a = 25±2°C, V_{DD} = 8 to 14V

			min	typ	max	unit
Supply voltage	V_{DD} (1)	Backup (CE=0)	3		14	V
Supply voltage	V_{DD} (2)	Normal operation	8		14	V
Input "H"−level voltage	V_{IH}	$\overline{UP}$, $\overline{DN}$, CE, $\overline{INTI}$, CR	0.75V_{DD}			V
Input "L"−level voltage	V_{IL}	$\overline{UP}$, $\overline{DN}$, CE, $\overline{INTI}$, CR	V_{SS}		0.25V_{DD}	V
Input signal amplitude	V_{IN}	SIG 1, 2	V_{SS}		V_{DD}	V

Case Outline 3008A-D20IC
(unit: mm)



Electrical Characteristics at T_a = 25±2°C

			min	typ	max	unit
Output "H"–level voltage	V_{OH} (1)	IND1 to 8, I_{OH} = –2mA, $V_{DD} \geqq 10V$	V_{DD}–2		V_{DD}	V
Output "H"–level voltage	V_{OH} (2)	IND1 to 8, I_{OH} = –20mA, $V_{DD} \geqq 10V$	3		V_{DD}	V
Pull-up resistance	R_{UP}	$\overline{INIT}$, $\overline{UP}$, $\overline{DN}$, V_{DD} = 13V	50k		80k	ohm
Pull-down resistance	R_{DN}	CE, V_{DD} = 13V	40k		70k	ohm
Input "H"–level current	I_{IH}	$\overline{INIT}$, $\overline{UP}$, $\overline{DN}$, V_{DD} = 14V V_I = 14V	0		10	μA
Input "L"–level current	I_{IL}	CE, V_{DD} = 14V, V_I = 0V	–10		0	μA
Output OFF leak current	I_{OFF} (1)	IND1 ~ 8, V_{DD} = 13V, V_o = –7V Output stage OFF	–10		0	μA
Output OFF leak current	I_{OFF} (2)	CR, V_{DD} = 14V, V_I = V_{SS} ~ V_{DD}	–3		0	μA
Channel separation	X_{tak}	COM1, COM2, 20kHz, 0dBm input		–60		dB
Crosstalk at minimum output mode	V_{omin}	COM, 20kHz, 0dBm input		–80		dB
Channel balance	ΔV_o	COM1,COM2, other than STEPO, R_L = 50kohm	–0.5		0.5	dB
Output distortion	THD	COM, f = 20kHa, R_L = 50kohm, R_g = 1kHz			0.1	%
Backup current	I_{BU}	V_{DD}, load open 1 min. after CE = "0"			1	μA

1. Pin Description

1-1. IND1 to 8 (pin No. 1 to 8)
Output pins for display of volume level: IF $\overline{INIT}$ is at "L" level, IND5 only is set to H.

Control pin of analog SW	IND 1	2	3	4	5	6	7	8
1	H							
2	H	H						
3		H						
4		H	H					
5			H					
6			H	H				
7				H				
8				H	H			
9					H			
10					H	H		
11						H		
12						H	H	
13							H	
14							H	H
15								H

*: All blanks represent floating mode.
H : P channel ON (light-up)

1-2. SIG1, 2 (pin Nos. 9, 14)
Pins for inputting signal to analog switch : Signal to be attenuated through IC is inputted.

1-3. COM1, 2 (pin Nos. 10, 13)
Pins for outputting signal from analog switch : Signal attenuated through IC is outputted.

1-4. V_M (pin No. 11)
Bias supply pin : For single-supply operation, this pin is set to 1/2V_{DD}.

1-5. V_{SS} (pin No. 12)
GND.

1-6. CE (pin No. 15)
When this pin is set to GND level, IC enters backup mode and output enters floating mode. Power dissipation also decreases.

1-7. $\overline{INIT}$ (pin No. 16)
Initial pin : When this pin is set to "L", step becomes 9 and IND5 pin is set to "H".

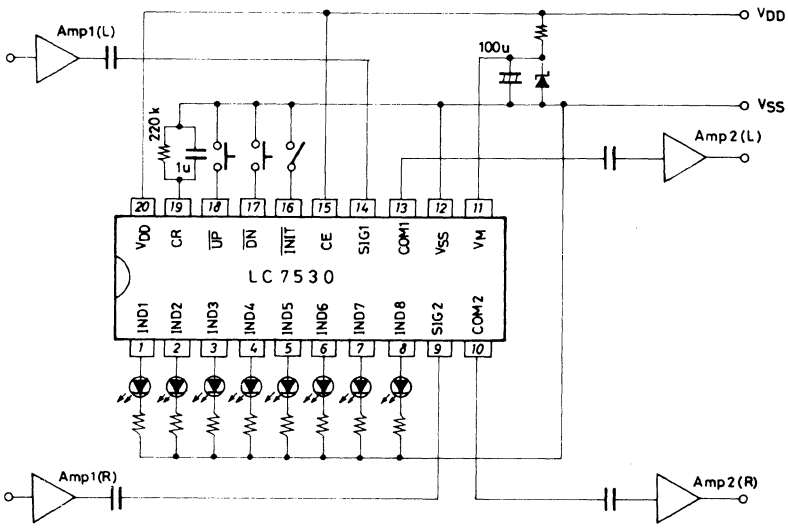
1-8. $\overline{DN}$ (pin No. 17)
When voltage on this pin falls, step drops and attenuation amount increases.
If this pin is held at "L", attenuation amount continues to increase, but if set to "H", attenuation amount stops increasing at such a step as has been reached in the instant of setting to "H".

1-9. $\overline{UP}$ (pin No. 18)
Operation for $\overline{UP}$ is the reversal of that for $\overline{DN}$.
If both $\overline{UP}$ and $\overline{DN}$ are set to "L", $\overline{UP}$ is given priority. Operation for $\overline{UP}$ and $\overline{DN}$ stops at MSB or LSB.

1-10. CR (pin No. 19)
Fixes the rate of moving step. Also used for connecting resistor, capacitor (open drain).

1-11. V_{DD} (pin No. 20)
Pin for plus power supply.

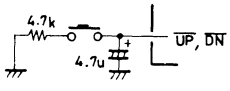
2. Sample Application Circuit

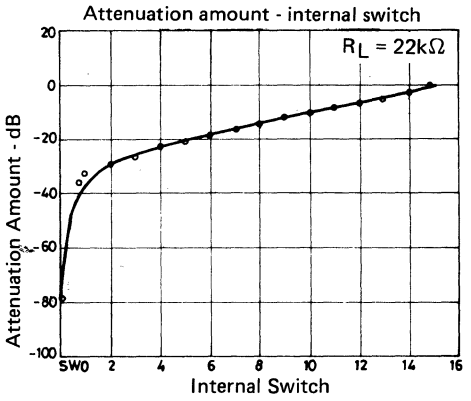


3. Proper Cares in Using IC

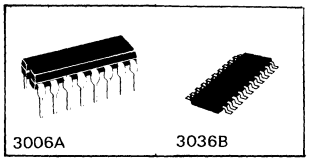
3-1. If noise generated at the time of step select becomes a problem, consider the following.
1) V_M must be grounded through low impedance.
2) A capacitor must be connected across V_{DD} and V_{SS} in the closest neighbourhood of V_{DD} pin.
3) Light-up current (IND8 to IND1) must be minimized.
4) Supply voltage must be dropped.

3-2. Prevent noise passing around from $\overline{UP}$, $\overline{DN}$ switches.




Attenuation amount - internal switch
R_L = 22kΩ
Attenuation Amount - dB
20
0
-20
-40
-60
-80
-100
SW0
2
4
6
8
10
12
14
16
Internal Switch

LC7533, 7534M



C MOS IC

Electronic Volume Controller

Ⓔ 1374A

Use : Attenuation of signal

Features :

1. C MOS process 3V typ. operation.
2. Up/down operation is performed with SW input.
3. 4-bit, 16-step counter. Step 6* is set with initial input (INIT).
4. Center tap provided.
5. Maximum attenuation : -60dB or less
6. Attenuation curve : Pseudo curve A. Left/right simultaneous setting.
   (Note) *: Step 6 means mode 6.

Absolute Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V_{DD}max	V_{SS} to 6	V
Applied Voltage	V_I	V_{SS} to V_{DD}	V
Allowable Power Dissipation	$P_d$max	100	V
Operating Temperature	Topg	-30 to +75	°C
Storage Temperature	Tstg	-40 to +125	°C

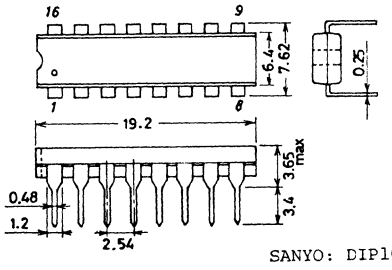
Allowable Operating Ranges at Ta=25°c

			unit
Supply Voltage	V_{DD}	2.1 to 4.5	V
Input "H" Level Voltage	V_{IH}	$0.7V_{DD}$ to V_{DD}	V
Input "L" Level Voltage	V_{IL}	0 to $0.3V_{DD}$	V

Electrical Characteristics at Ta=25°C

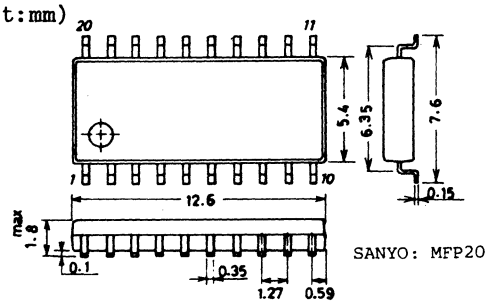
Signal Distortion	THD1	V_{DD}=3V, R_L=50kohm, f=1kHz	0.5% max
	THD2	V_{DD}=1.8V, R_L=50kohm, f=1kHz	1% typ
Output at Attenuation Mode	X_{OUT}	0dBm input, 1kHz, 51kohm load	-60dB max

Case Outline 3006A-D16IC LC7533
(unit:mm)



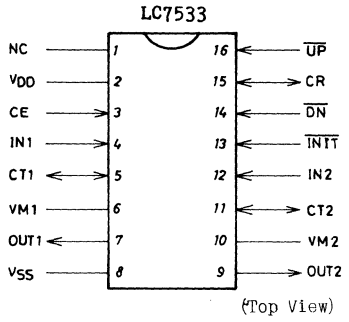
SANYO: DIP16

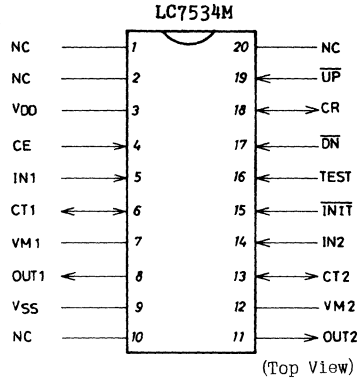
Case Outline 3036B-M20IC LC7534M
(unit:mm)



SANYO: MFP20

Pin Assignment



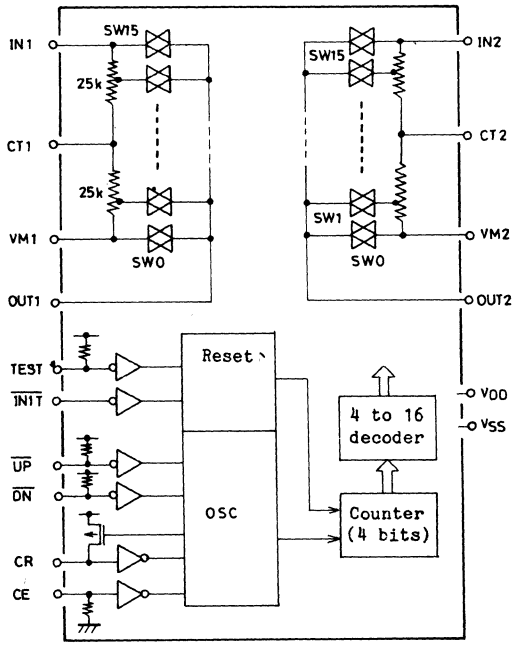


Note 1. No bonding exists on the inside of NC pin. It is recommended that the outside should be shorted to V_{DD},V_{SS},etc. on the printed circuit board.

Note 2. The MFP package only is provided with the TEST pin. It should be connected to V_{SS}.
TEST=0 causes the power on reset function to be performed.
(The power on reset function means that mode 6 is entered at the time of application of power.)

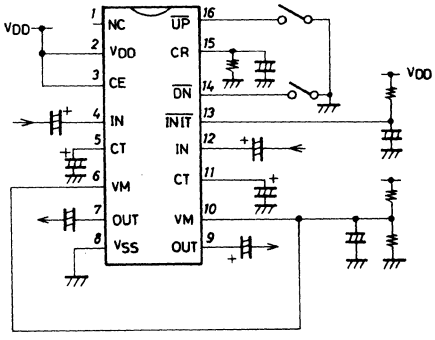
Equivalent Circuit Block Diagram

LC7533,7534M



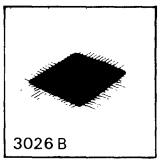
Note 1. The TEST pin is bonded only when the MFP20 is used.

Sample Application Circuit
(LC7533 DIP-16)



For V_M, $1/2V_{DD}$ bias is recommended.

LC7550



C MOS LSI

Peak Holding Level Meter

Ⓔ 889A

Application

- Peak hold level meter of tape deck.
- Peak hold level meter of power amplifier.
- General-purpose level meter.

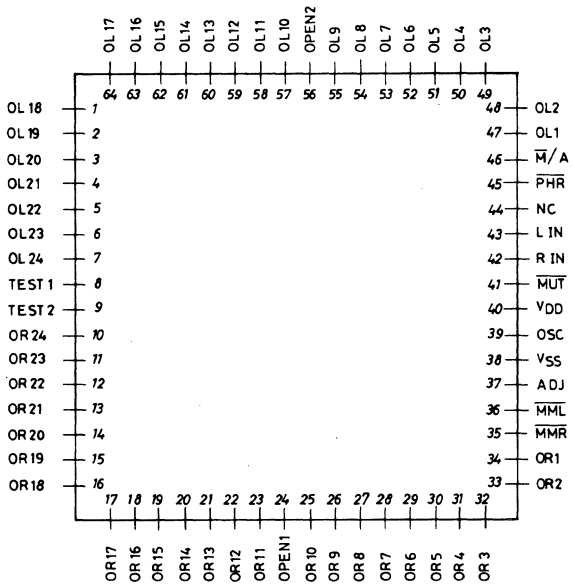
Features

- C MOS LSI for 2-channel (24 points + 24 points) peak hold level meter.
- Capable of driving a static lighting type fluorescent display tube of 23V or less.
- Two types of applications are available as follows :
  a) 2-channel peak hold level meter.
  b) 2-channel level meter.

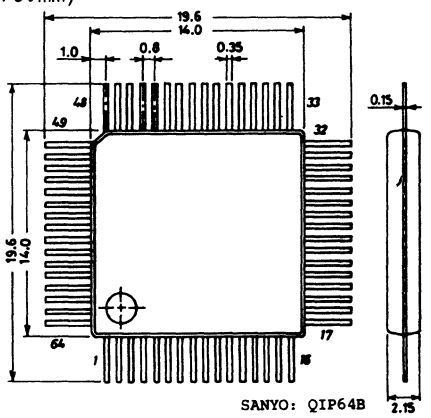
Functions

- Peak hold function.
  - The peak hold level is indicated by one point lighted.
  - The peak hold comes in 2 types as follows :
    a) Automatic reset.
    The peak hold point is reset automatically after lapse of 0.1 to 2 seconds.
    b) Manual reset.
    The peak hold point is reset by pushing a reset switch.
- Comparator level : Linear scale
- Input level at full scale : 2.5 to 5 V (Adjustable externally)

Pin Assignment

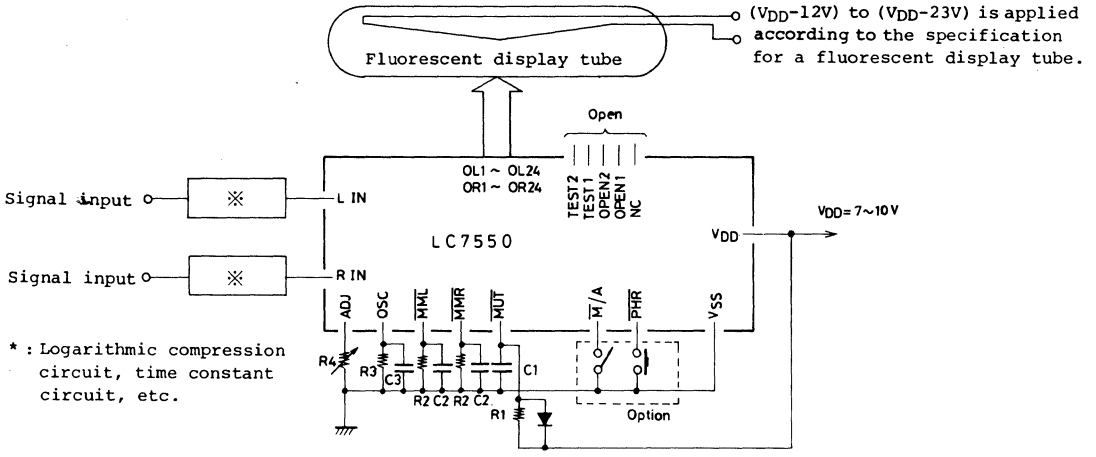


Case Outline 3026B-Q64BIC
(unit:mm)



SANYO: QIP64B

Application Circuit



Reference values of constants

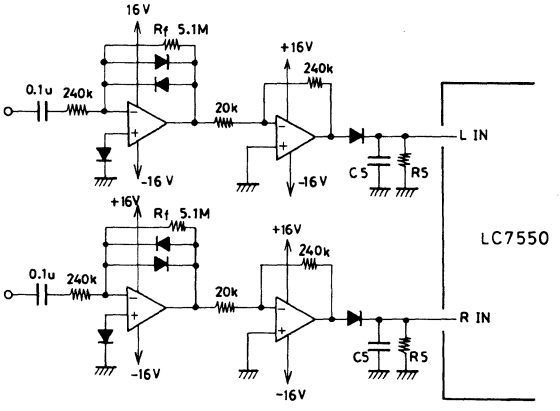
(R_1=220kohm, C_1=0.68uF) : Values for V_{DD} rise time of less than 50msec.

(R_2=470kohm, C_2=3.3uF) : Values for peak hold time of approximately 1sec.

(R_3=56kohm, C_3=1000pF) : Values for oscillation frequency of approximately 26.7kHz. It is recommended to use a carbon film resistor and a polyester film capacitor so that the variations in frequency with temperature can be minimized.

R4 : Value to be fixed by referring to the characteristic curve (V_{IN}max - ADJ pin external resistance) shown later.

Example of Logarithmic compression circuit and time constant circuit



OP amp. : LA6324

Diode : DS448

(C_5=0.33uF, R_5=1Mohm) : Time constant to fix decay time

In the application circuit, the relation between the input voltage of logarithmic compression circuit and the output voltage of time constant circuit is as shown right. If the full scale input voltage at which up to the 24th point are all lighted is taken as 2.88V and sinusoidal input voltage 295mV is taken as 0dB, the relation between the number of points lighted and the input level becomes as shown below.

Characteristic of logrithmic compression circuit and time constant circuit

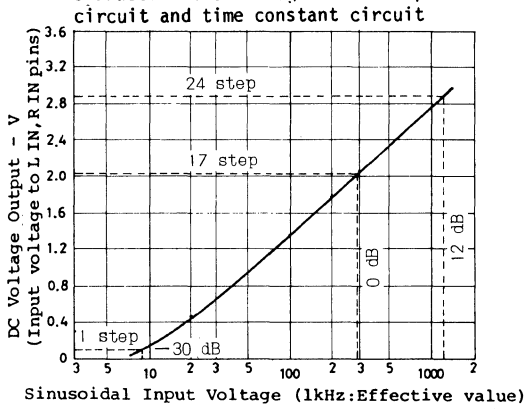
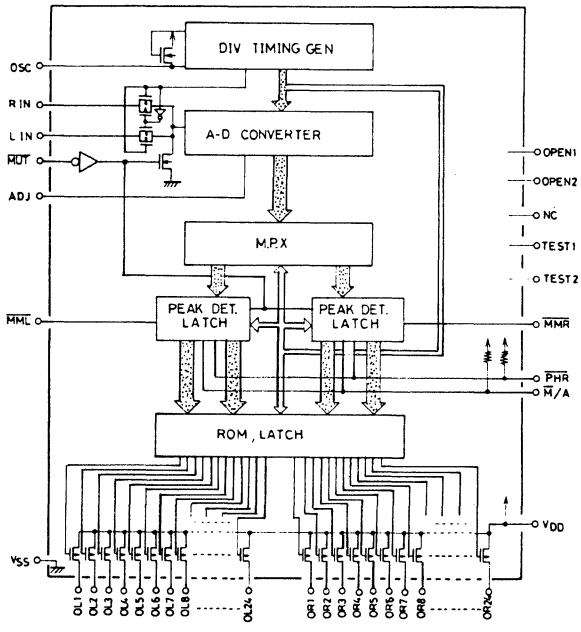


Table 1. Fluorescent Display Tube and Input Level

Number of points lighted	1	2	3	4	5	6	7	8	9	10	11	12
Input level (Approximate value) (dB)	-30	-28	-25	-23	-21	-19	-18	-16	-14	-12	-11	-8
Number of points lighted	13	14	15	16	17	18	19	20	21	22	23	24
Input level (Approximate value) (dB)	-7	-5	-3	-2	0	2	3	5	7	9	10	12

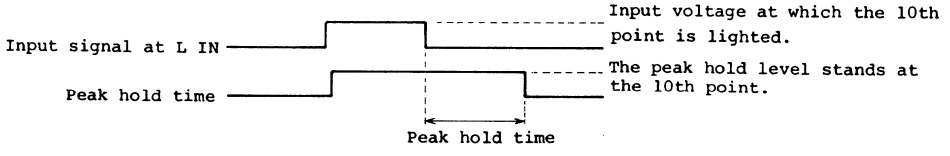
Note 1. If V_{DD} is 7.68V, it is seen from the characteristic curve (V_{INmax} - ADJ pin external resistance) that ADJ resistance 20kohm causes full scale input voltage 2.88V.
2. The temperature characteristics and the variations in diode quality, etc. are not considered in this graph.

Equivalent Circuit Blcok Diagram

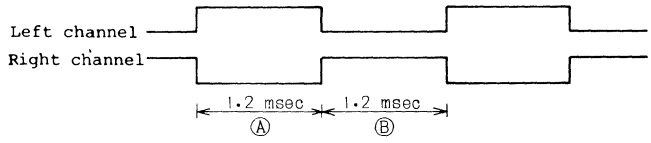


Pin Description

1. OL_1 to OL_{24}, OR_1 to OR_{24}
   - Output pins of P channel, open drain type for fluorescent display tube drive.
   - Output withstand voltage (V_{DD} - 23V) max
2. L IN, R IN
   - Input pins for display levels of left/right channels.
   - The comparator level is of linear scale and if the full scale input voltage (input voltage at which 24 points are all lighted) is taken as 3.6V the number of points lighted will be increased in such a way as 1 point, 2 points, ----- each time the voltage is increased by 150mV starting at 0V.
   - The attack, decay circuits to fix the response speed and the logarithmic amplifiers for logarithmic display are connected externally.
3. ADJ
   - Input pin for full scale adjustment
   - The input voltage (full scale input voltage) at which 24 points are all lighted can be adjusted by adjusting external resistor R_4.
   - The full scale input voltage depends on V_{DD}, the internal resistance of LSI, and R_4.
4. $\overline{M}$/A
   - Input pin for controlling changeover of manual/automatic reset of the peak hold point.
   - Automatic reset mode is available when the V_{DD} level is applied or the input pins are open; manual reset mode is available when the V_{SS} level is applied.
5. $\overline{PHR}$
   - Pin for applying the signal to reset the peak hold point at the time of manual reset mode. If the V_{SS} level is applied, the peak hold point will be reset.
     It V_{SS} remains applied to the $\overline{PHR}$ pin at the time of manual reset mode, the ordinary level meter without peak hold function will result.
6. $\overline{MML}$, $\overline{MMR}$
   - Pins for externally connecting the time constant circuit of left/right channels to fix the peak hold time at the time of automatic reset mode.



7. $\overline{MUT}$
   - Pin for externally connecting the time constant circuit to reset the peak hold function for a specified period of time and also to set the L IN/R IN inputs at the V_{SS} level at the time of application of power.
8. OSC
   - Pin for externally connecting C and R to generate control clock inside the LSI.
   - When the oscillation frequency is at 26.6kHz, the L IN/R IN input signals are alternately sampling-processed once in approximately 2.4msec.



Ⓐ : Left channel AD conversion execution

Ⓑ : Right channel AD conversion execution

9. V_{DD}, V_{SS}
. Pins for applying supply voltage.

Operations of Control Pins

Operation mode	$\overline{M}/A$	$\overline{PHR}$
With peak hold function		
. Automatic reset of peak hold point	1	x
. Manual reset of peak hold point	0	(1)*
Without peak hold function	0	0

Note) 1 : V_{DD} level applied or open.
0 : V_{SS} level applied.
X : Either V_{DD} level or V_{SS} level
(1)*: Normally V_{DD} level applied or open. V_{SS} level applied only when resetting.

Absolute Maximum Ratings at T_a=25°C

				unit
Supply Voltage	V_{DD}		-0.3 to +11	V
Input Voltage	V_{IN}	Input/output pins, OSC, $\overline{MML}$, $\overline{MMR}$, R_{IN}, L_{IN}: Output OFF	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	Output OFF, OL1 to OL24, OR1 to OR24	V_{DD}-23 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d$max	$T_a \leq 70$°C	230	mW
Allowable Power Dissipation of Segment	$P_d$seg	$I_O \leq 1.5$mA, OL1 to OL24, OR1 to OR24	3.5	mW
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-40 to +125	°C

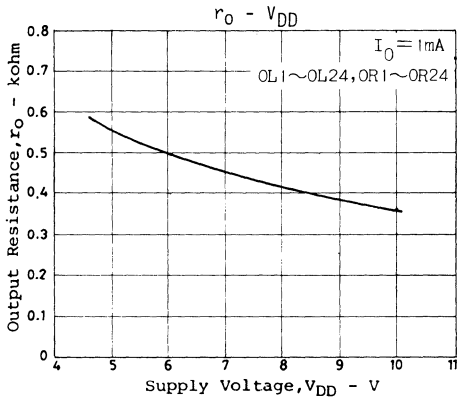
Allowable Operating Ranges at T_a=25°C, V_{DD}=7.0 to 10V, V_{SS}=0V

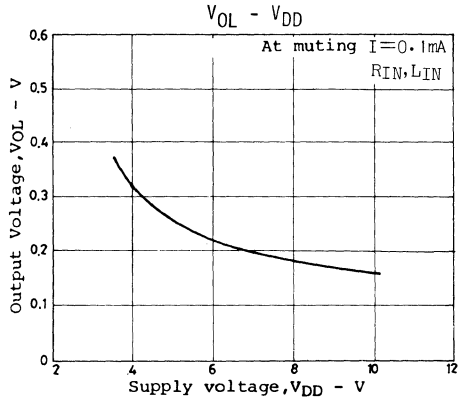
			min	typ	max	unit
Supply Voltage	V_{DD}		7.0		10.0	V
"H" Level Input Voltage	$V_{IH}(1)$	$\overline{M}/A$, $\overline{PHR}$	V_{DD}-1.1		V_{DD}	V
"L" Level Input Voltage	$V_{IL}(1)$	$\overline{M}/A$, $\overline{PHR}$	0		1.1	V
"H" Level Input Voltage	$V_{IH}(2)$	$\overline{MUT}$	0.7V_{DD}		V_{DD}	V
"L" Level Input Voltage	$V_{IL}(2)$	$\overline{MUT}$	0		0.3V_{DD}	V
Input Voltage	V_{IN}	R_{IN}, L_{IN}, $V_{IN} \leq V_{DD}$-3V	0		5	V

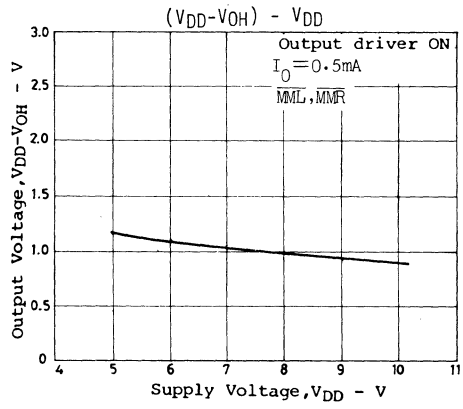
Electrical Characteristics at T_a=25°C, V_{DD}=7.0 to 10V, V_{SS}=0V

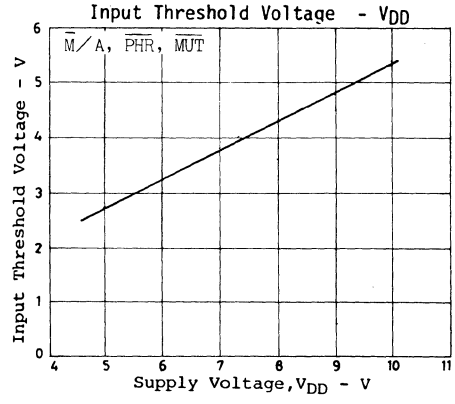
			min	typ	max	unit
Input Current	I_{IN}	$\overline{MUT}$, V_{IN}=V_{DD}			3	uA
	I_{IN}	$\overline{MUT}$, V_{IN}=V_{SS}	-3			uA
Input Floating Voltage	V_{IF}	$\overline{M}/A$, $\overline{PHR}$, Input open	V_{DD}-0.9			V
"L" Level Input Current	$I_{IL}(1)$	$\overline{M}/A$, $\overline{PHR}$, V_{IN}=V_{SS}	-550		-25	uA
"H" Level Output Current	$V_{OH}(1)$	OL1 to OL24, OR1 to OR24,	V_{DD}-2.3			V
Output OFF Leak Current	I_{OFF}	OL1 to OL24, OR1 to OR24, V_O=V_{DD}-21V	-3			uA
Input/Output OFF Leak Current	$I_{I/O}(1)$	OSC, $\overline{MML}$, $\overline{MMR}$, Output OFF $V_{I/O}$=V_{DD}			3	uA
		$V_{I/O}$=V_{DD}	-3			uA

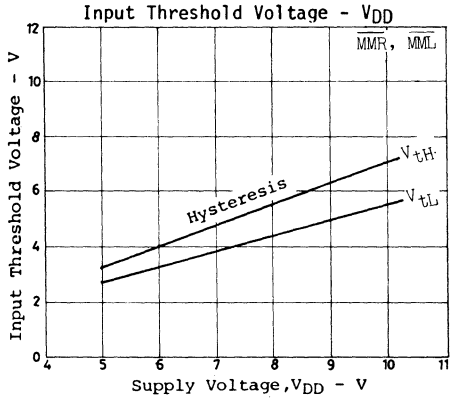
			min	typ	max	unit
	$I_{I/O(2)}$	$L_{IN}, R_{IN}, \overline{MUT}=V_{DD}$				
		$V_{I/O}=V_{DD}$			3	uA
		$V_{I/O}=V_{SS}$	-3			uA
"L" Level Output Voltage	V_{OL}	$L_{IN}, R_{IN}, I_{I/O}=0.1mA, \overline{MUT}=V_{SS}$			0.9	V
"H" Level Output Voltage	$V_{OH(2)}$	$\overline{MML}, \overline{MMR}, I_{I/O}=0.5mA$	$V_{DD}-0.9$			V
Input Offset Voltage	V_{offset}	$V_{IN} \leqq V_{DD}-3V, L_{IN}, R_{IN}$, $V_{IN}=0$ to 5V	-50		+50	mV
AD Conversion Linear Error		Full scale input voltage = 2.5 to 5 V	-1/2		1/2	LSB
Current Dissipation	I_{DD}	$f_{osc}=26.7kHz, \overline{MUT}=V_{DD}$, other pins			5	mA

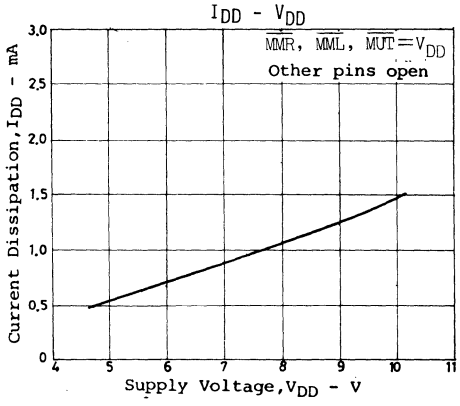


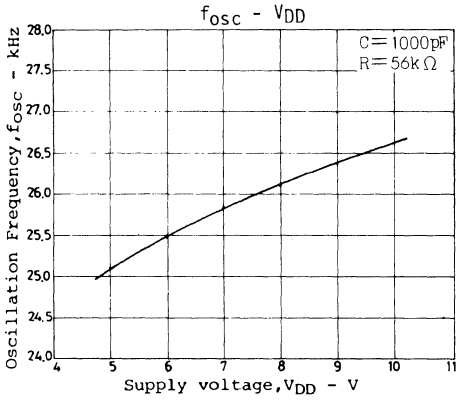


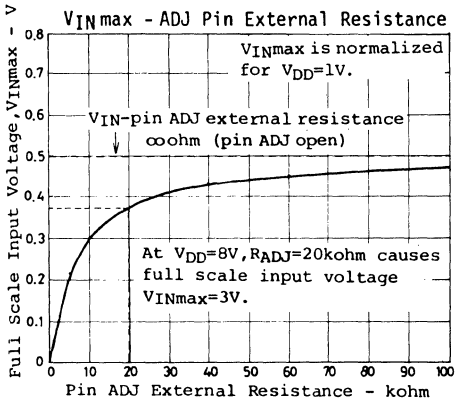


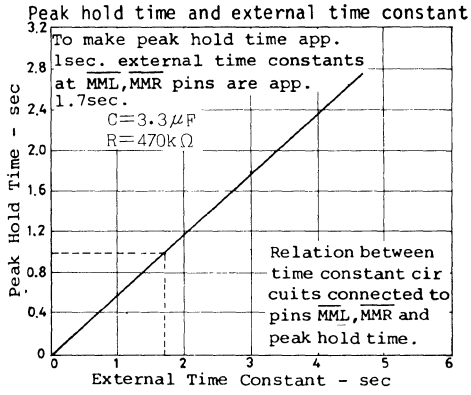


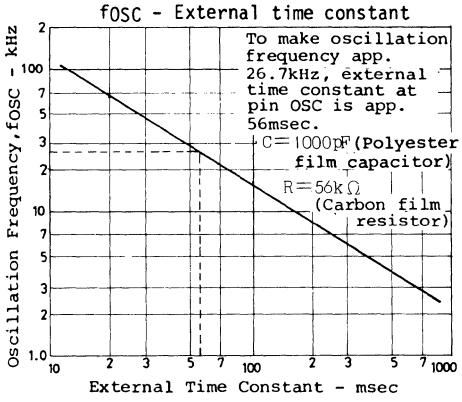


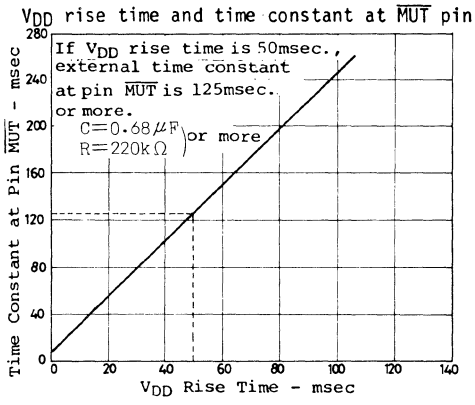



fosc - VDD
C=1000pF
R=56kΩ
Oscillation Frequency, fosc - kHz
Supply voltage, VDD - V


VINmax - ADJ Pin External Resistance
VINmax is normalized for VDD=1V.
VIN-pin ADJ external resistance ∞ohm (pin ADJ open)
At VDD=8V, RADJ=20kohm causes full scale input voltage VINmax=3V.
Full Scale Input Voltage, VINmax - V
Pin ADJ External Resistance - kohm


Peak hold time and external time constant
To make peak hold time app. 1sec. external time constants at MML, MMR pins are app. 1.7sec.
C=3.3μF
R=470kΩ
Relation between time constant cir cuits connected to pins MML, MMR and peak hold time.
Peak Hold Time - sec
External Time Constant - sec


fOSC - External time constant
To make oscillation frequency app. 26.7kHz, external time constant at pin OSC is app. 56msec.
C=1000pF (Polyester film capacitor)
R=56kΩ (Carbon film resistor)
Oscillation Frequency, fOSC - kHz
External Time Constant - msec


VDD rise time and time constant at MUT pin
If VDD rise time is 50msec., external time constant at pin MUT is 125msec. or more.
C=0.68μF
R=220kΩ
or more
Time Constant at Pin MUT - msec
VDD Rise Time - msec

LC7555, 7556

C MOS LSI

Peak Holding Level Meter

Ⓔ 724B

Applications

- Peak hold level meter of tape deck.
- Peak hold level meter of power amplifier.
- General-purpose level meter.

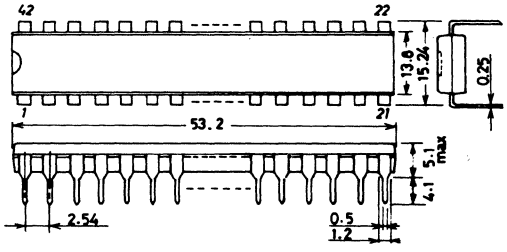
Features

- C MOS LSI for 2-channel (12 points + 12 points) peak hold level meter.
- Capable of driving a static lighting type fluorescent display tube of 23V or less.
- Three types of applications are available as follows :
  - a) 2-channel peak hold level meter.
  - b) 2-channel level mter.
  - c) Signal meter and tuning meter.

Functions

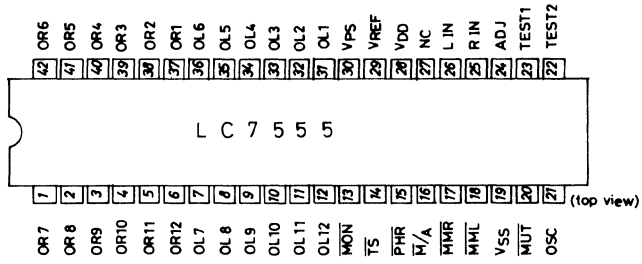
- Peak hold function.
  - 1-point peak hold.
  - Peak hold comes in 2 types as follows :
  - a) Automatic reset
    Peak hold is reset automatically after lapse of a specified period of time (settable).
  - b) Manual reset
    Peak hold is reset with a reset switch.
- Muting function
  Display is unlighted for a certain period of time at the time of application of power.
- Monaural function
  Display unbalance between left and right channels is eliminated at the time of application of monaural input signal.
- Comparator level
  - Linear scale

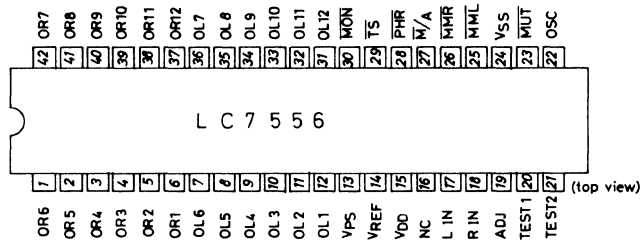
Case Outline 3014A-D42IC
(unit:mm)



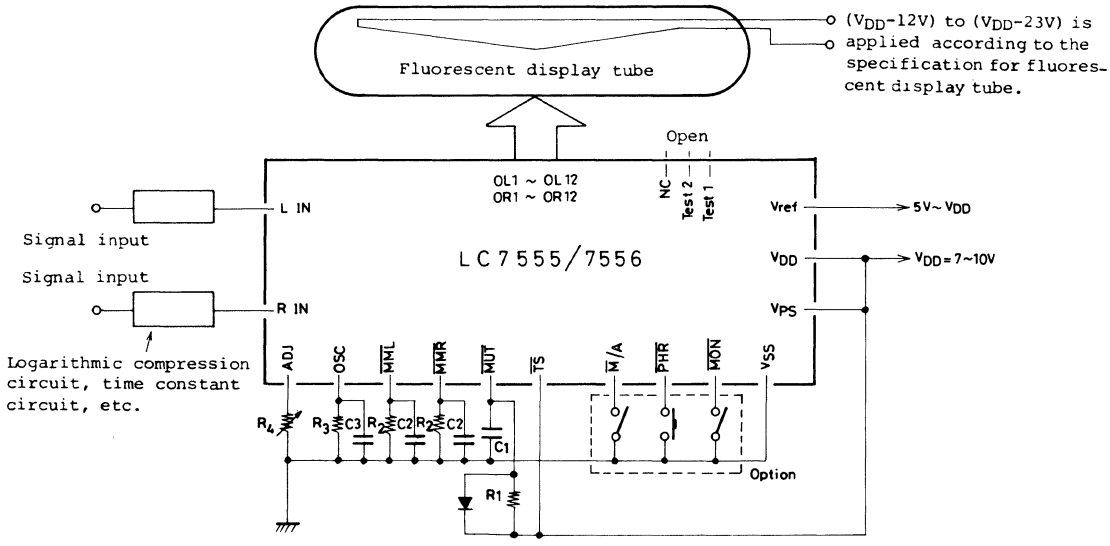
SANYO : DIP42

Pin Assignment





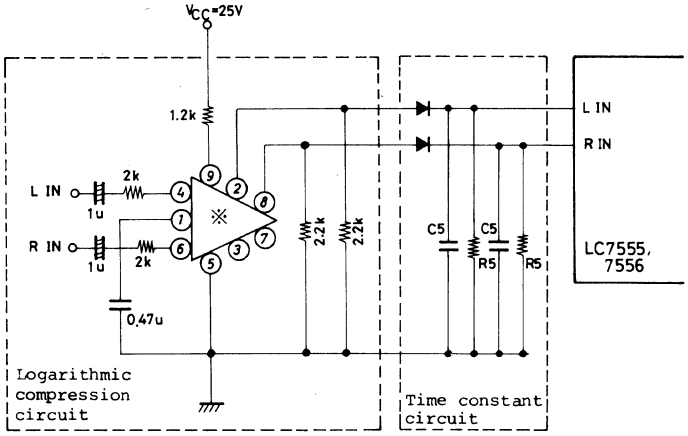
Application Circuit



Reference values of constants

- R1=220kohm,C1=0.68uF ----- Values for V_{DD} rise time of less than 50msec. Refer to Fig. 13.
- R2=470kohm,C2=3.3uF ------ Values for peak hold time of approximately 1 sec. Refer to Fig. 11.
- R3=56kohm,C3=1000pF ------ Values for oscillation frequency of approximately 26.7kHz. Refer to Fig. 12. Variations in frequency with temperature are reduced by using carbon film resistor and polyester film capacitor.
- R4=20kohm ---------- Values for displaying all points at V_{ref}=8V,V_{IN}=4V. Refer to Figs. 9, 10.

Sample logarithmic compression circuit, time constant circuit



※ : Equivalent to TA7318SP

Reference values of constants
(R5=220nF, C5=2Mohm) ..... Values for fixing recovery time.

For the logarithmic compression circuit and time constant circuit in the sample application circuit, the relation between the input voltage of logarithmic compression circuit and the output voltage of time constant circuit is as shown right. If the full scale input voltage is taken as 4V and input level 145mV is taken as 0dB, the relation between the number of points lighted and the input level becomes as shown below.

Characteristic of logarithmic compression circuit, time constant circuit

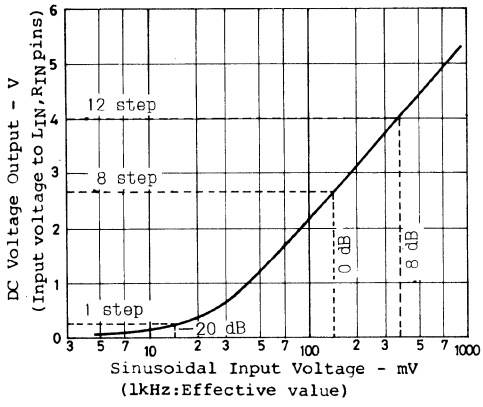
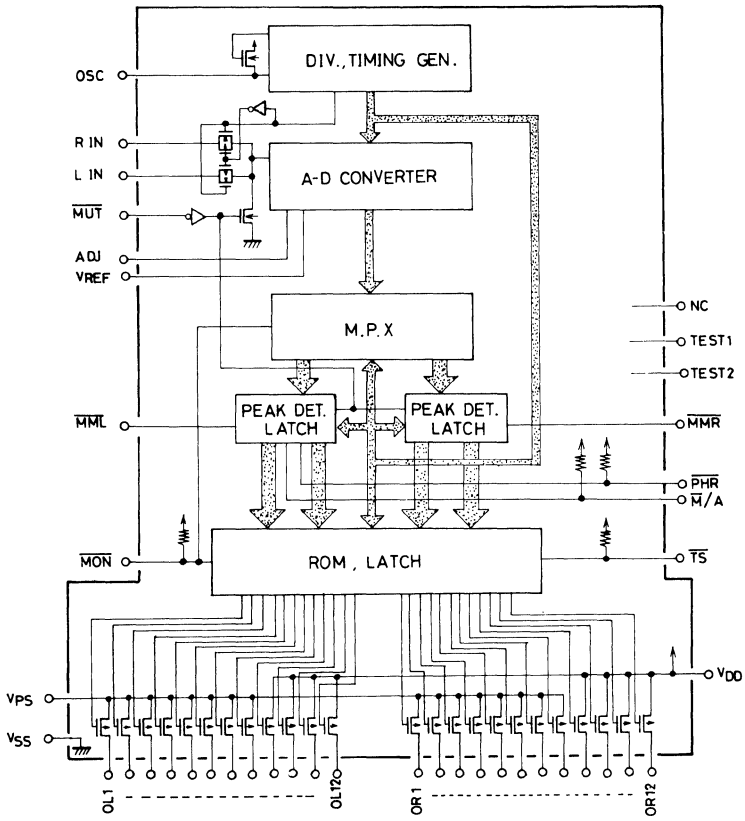


Table 1. Fluorescent Display Tube and Input Level

Number of points lighted	1	2	3	4	5	6	7	8	9	10	11	12
Input level (Approximate value)	-20	-14	-10	-8	-6	-4	-2	0	2	4	6	8

Note) If V_{ref} is 8V, it is seen from Figs. 9, 10 that ADJ resistance 20kohm causes full scale input voltage 4V.

Equivalent Circuit Block Diagram

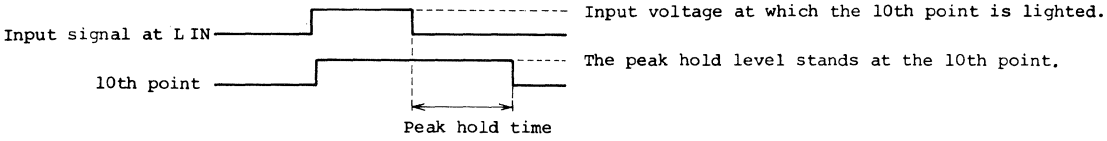


Pin Description

1. OL_1 to OL_{12}, OR_1 to OR_{12}
   - Output pins of P channel, open drain type for fluorescent display tube drive.
   - Output withstand voltage (V_{DD}-23V) max.
2. L IN, R IN
   - Input pins for display levels of left/ right channels.
   - The comparator level is of linear scale and if the full scale input voltage (input voltage at which 12 points are all lighted) is taken as 3.6V, the number of points lighted will be increased in such a way as 1 point, 2 points, ----- each time the voltage is increased by 300mV starting at 0V.
   - The attack/release (recovery) circuit to fix the response speed is attached externally. To provide logarithmic compression display, the log amplifier is attached externally.
3. ADJ
   - Input pin for full scale adjustment.
   - The input voltage (full scale input voltage) at which 12 points are all lighted can be adjusted by adjusting external resistor R_4.
   - The full scale input voltage depends on the voltage applied to V_{ref}, the internal resistance of LSI, and R_4. (Refer to Figs. 9, 10.)
4. $\overline{M}$/A
   - Input pin for controlling changeover of manual/automatic reset of the peak hold point.
   - Automatic reset mode is available when the V_{DD} level is applied or the input pins are open; manual reset mode is available when the V_{SS} level is applied.
5. $\overline{PHR}$
   - Pin for applying the signal to reset the peak hold point at the time of manual reset mode.

. If the V_{SS} level is applied, the peak hold point will be reset.
. If V_{SS} remains applied to the $\overline{PHR}$ pin at the time of manual reset mode, the ordinary level meter without peak hold function will result.

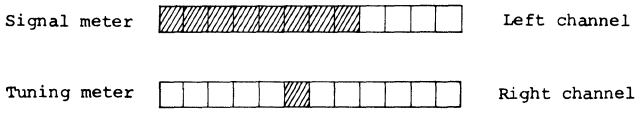
6. $\overline{MML}$, $\overline{MMR}$
. The peak hold time at the time of automatic reset mode is as shown in Fig. 11.



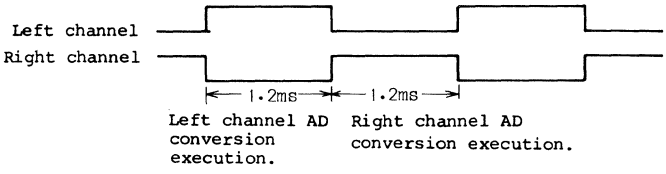
7. $\overline{MON}$
. Control input pin for monaural application only.
. The L IN signal is displyed on OL1 to OL2 and OR1 to OR12. Thus, unbalance between left and right channels is eliminated.

8. $\overline{MUT}$
. Pin for externally attaching the time constant circuit to reset the peak hold function for a specified period of time and also to set the L IN/R IN inputs at the V_{SS} level at the time of application of power.

9. $\overline{TS}$
. Pin for controlling changeover of the peak hold meter function into the tuning/signal meter.
. Operation as the peak hold level meter is available when the V_{DD} level is applied to $\overline{TS}$ or the input pins are open; operation as the tuning meter and signal meter is available when the V_{SS} level is applied.



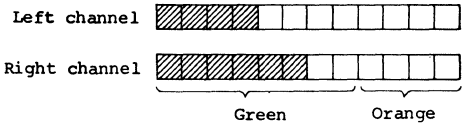
10. OSC
. Pin for externally attaching C, R to generate control clock inside the LSI.
. When the oscillation frequency is at 26.6kHz, the L IN/R IN input signals are alternately sampling-processed once in approximately 2.4msec.



. The relation between the oscillation frequency and the external constant is shown in Fig. 12.

11. V_{ref}
. Pin for connecting the reference voltage for AD conversion.

12. VPS
. Common source pin for drivers of OL1 to OL8, OR1 to OR8.
. The fluorescent display tube shown below is taken as an example. If 9V, 5V, and -10V are applied to V_{DD}, V_{PS}, and the fluorescent display tube filament respectively, -15V and -19V will be applied to the green segments and orange segments respectively.



13. V_{DD}, V_{SS}
. Pins for applying supply voltages.

Summary of Control Pin Operations

Operation mode	$\overline{TS}$	$\overline{MON}$	$\overline{M/A}$	$\overline{PHR}$
Stereo peak hold meter				
. Automatic reset of peak hold point.	1	1	1	x
. Manual reset of peak hold point.	1	1	0	(1)
Monaural peak hold meter				
. Automatic reset of peak hold point.	1	0	1	x
. Manual reset of peak hold point.	1	0	0	(1)
Stereo level meter	1	1	0	0
Monaural level meter	1	0	0	0
Tuning meter & signal meter	0	x	x	x

Note : 1 : V_{DD} level applied or open.
0 : V_{SS} level applied or open.
x : Either V_{DD} level or V_{SS} level.
(1): Normally V_{DD} level applied or open. V_{SS} applied only when resetting.

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}		-0.3 to +11	V
	V_{PS}		-0.3 to V_{DD}+0.3	V
Reference Voltage	V_{ref}		-0.3 to V_{DD}+0.3	V
Input Voltage	V_{IN}	Input/output pins OSC, $\overline{MML}$, $\overline{MMR}$, R_{IN}, L_{IN}: Output off	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	OL1 to OL8, OR1 to OR8 : Output off	V_{DD}-23 to V_{DD}+0.3	V
		OL9 to OL12, OR9 to OR12: Output off	V_{DD}-23 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d$max	$T_a \leq 70$°C	250	mW
Allowable Power Dissipation of Segments	$P_d$seg	OL1 to OL8, OR1 to OR8, $I_O \leq 1.5$mA, $V_{PS}=V_{DD}$ ($I_O \leq 0.8$mA, $V_{PS}=5V \leq V_{DD}$)	7	mW
		OL9 to OL12, OR9 to OR12, $I_O \leq 1.5$mA	7	mW
Operating Temperature	T_{opg}		-30 to +70	°C
Storage Temperature	T_{stg}		-40 to +125	°C

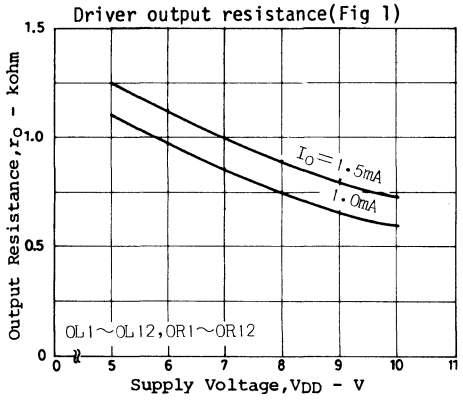
Allowable Operating Ranges at T_a=25°C, V_{SS}=0V

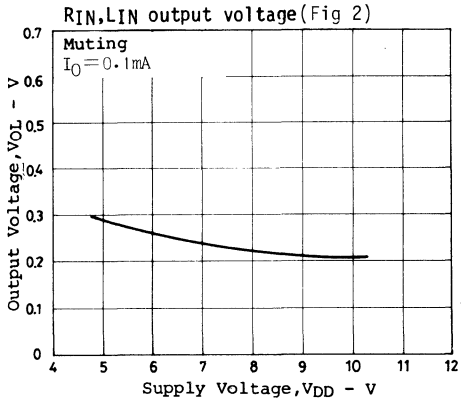
			min	typ	max	unit
Supply Voltage	V_{DD}		7		10	V
	V_{PS}		5		V_{DD}	V
Reference Voltage	V_{ref}		5		V_{DD}	V
"H"Level Input Voltage	$V_{IH(1)}$	$\overline{M/A}$, $\overline{PHR}$, $\overline{TS}$, $\overline{MON}$	V_{DD}-1.1		V_{DD}	V
"L"Level Input Voltage	$V_{IL(1)}$	$\overline{M/A}$, $\overline{PHR}$, $\overline{TS}$, $\overline{MON}$	0		1.1	
"H"Level Input Voltage	$V_{IH(2)}$	$\overline{MUT}$	0.7V_{DD}		V_{DD}	V
"L"Level Input Voltage	$H_{IL(2)}$	$\overline{MUT}$	0		0.3V_{DD}	V
Input Voltage	V_{IN}	R_{IN}, L_{IN}; $V_{IN} \leq V_{ref}$, $V_{IN} \leq V_{DD}$-3V	0		5	V
Full Scale Input Voltage		R_{IN}, L_{IN}; $V_{IN} \leq V_{ref}$, $V_{IN} \leq V_{DD}$-3V	2.5		5	V

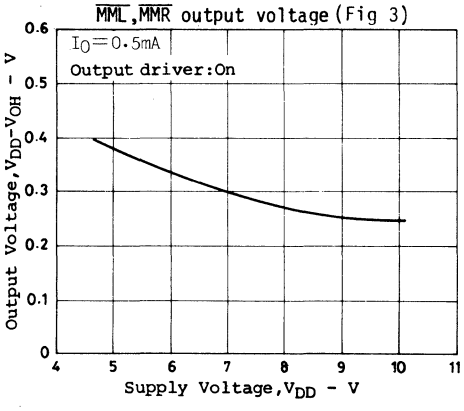
Electrical Characteristics at T_a=25°C

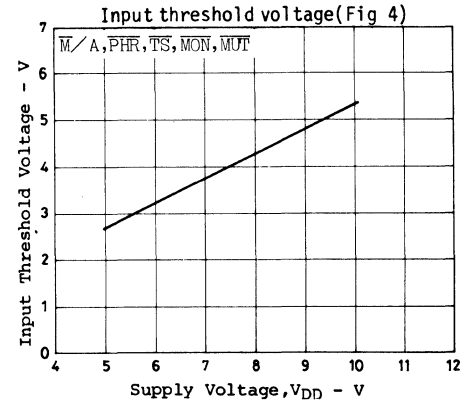
			min	typ	max	unit
Input Current	I_{IN}	$\overline{MUT}$; $V_{IN}=V_{DD}$			3.0	uA
		$\overline{MUT}$; $V_{IN}=V_{SS}$	-3.0			uA
Input Floating Voltage	V_{IF}	$\overline{M/A}$, $\overline{PHR}$, $\overline{TS}$, $\overline{MON}$; Input open	V_{DD}-0.9			V

			min	typ	max	unit
"L"Level Input Voltage	$I_{IL}(1)$	$\overline{M/A}$,$\overline{PHR}$,$\overline{TS}$,$\overline{MON}$;$V_{IN}=V_{SS}$	-550		-25	uA
"H"Level Output Voltage	$V_{OH}(1)$	OL1 to OL8,OR1 to OR8;$V_{PS}=V_{DD}$,I_O=1.5mA	V_{DD}-4.5			V
		OL1 to OL8,OR1 to OR8;$V_{PS}=5V \leqq V_{DD}$,I_O=0.8mA	V_{PS}-6.0			V
	$V_{OH}(2)$	OL9 to OL12,OR9 to OR12; I_O=1.5mA	V_{DD}-4.5			V
	$V_{OH}(3)$	MML,MMR,$I_{I/O}$=0.5mA	V_{DD}-0.9			V
Output Off Leak Current	I_{OFF}	OL1 to OL12,OR1 to OR12; $V_{PS}=V_{DD}$,$V_O=V_{DD}$-21V,Output off	-3.0			uA
Input/Output Off Leak Current	$I_{I/O}$	OSC,$\overline{MML}$,$\overline{MMR}$;Output off				
		$V_{I/O}=V_{DD}$			3.0	uA
		$V_{I/O}=V_{SS}$	-3.0			uA
		L_{IN},R_{IN};$\overline{MUT}=V_{DD}$				
		$V_{I/O}=V_{DD}$			3.0	uA
		$V_{I/O}=V_{SS}$	-3.0			uA
"L"Level Output Voltage	V_{OL}	L_{IN},R_{IN};$I_{I/O}$=0.1mA,$\overline{MUT}=V_{SS}$			0.9	V
Input Offset Voltage	V_{offset}	L_{IN},R_{IN};$V_{IN} \leqq V_{DD}$-3V, $V_{IN} \leqq V_{ref}$,V_{IN}=0 to 1V	-50		50	mV
		L_{IN},R_{IN};$V_{IN} \leqq V_{DD}$-3V, $V_{IN} \leqq V_{ref}$,V_{IN}=1 to 5V	-100		100	mV
AD Conversion Linear Error		Full scale input voltage= 2.5 to 5 V	-1/2		1/2	LSB
Current Dissipation	I_{DD}	f_{OSC}=26.7kHz,$\overline{MUT}=V_{DD}$, R_{IN},L_{IN}=0V,Other pin open		1.0	3.0	mA
Reference Supply Current	I_{ref}	V_{ref}			2.5	mA

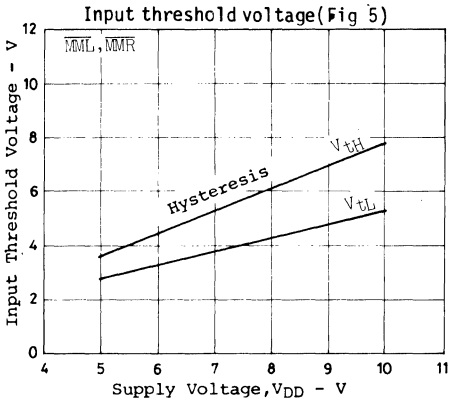




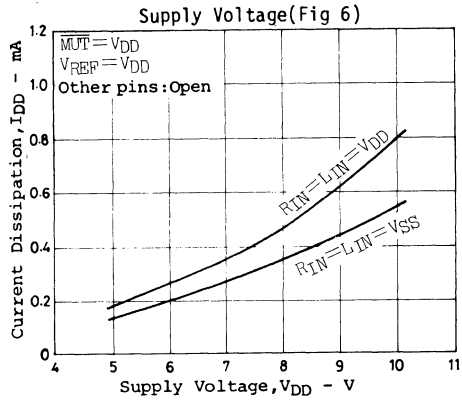




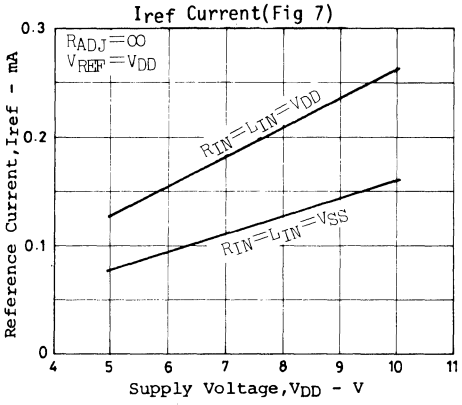
Input threshold voltage(Fig 5)



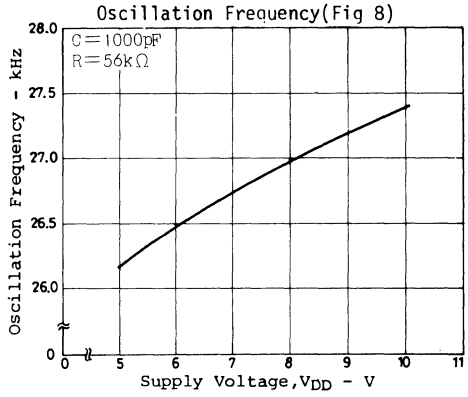
Supply Voltage(Fig 6)



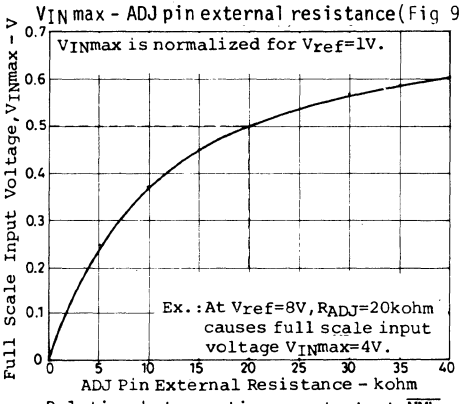
Iref Current(Fig 7)



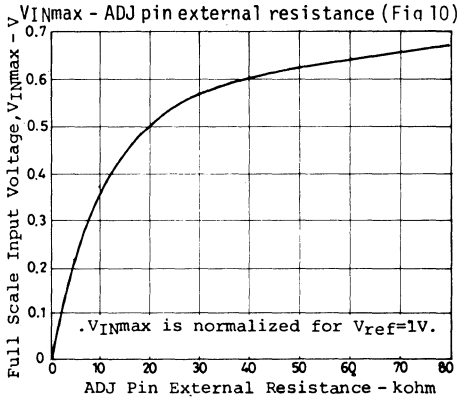
Oscillation Frequency(Fig 8)



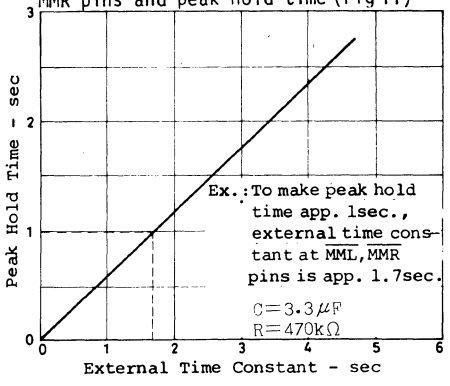
VIN max - ADJ pin external resistance(Fig 9)



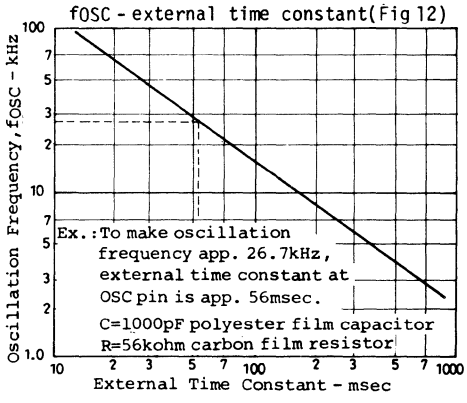
VINmax - ADJ pin external resistance (Fig 10)



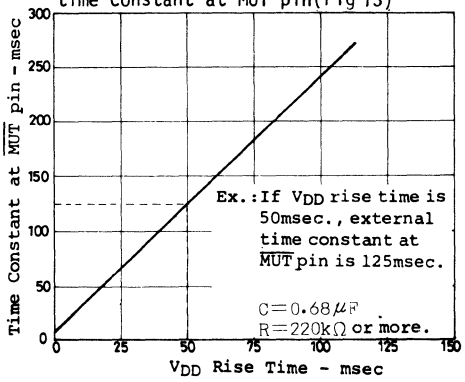
Relation between time constant at $\overline{MML}$, $\overline{MMR}$ pins and peak hold time (Fig 11)



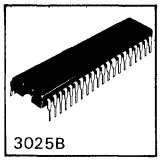
fOSC - external time constant(Fig 12)



Relation between V_{DD} rise time and time constant at $\overline{MUT}$ pin(Fig 13)



LC7570



C MOS IC

FL Static Driver

Ⓔ 1465A

Use

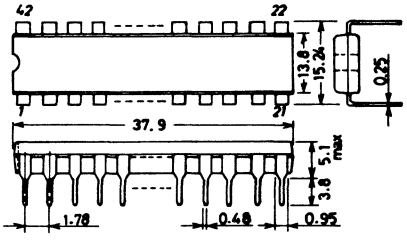
Static driver for fluorescent display tube for electronic tuning frequency display applications.

Features :

(1) 34-segment output (With pull-down resistor)
(2) 5-step A-D converter
(3) Blanking pin for blanking out display
(4) Data input : Serial input (CL, DATA, WR)

Pin Assignment

Case Outline 3025B-D42SIC
(unit:mm)



SANYO: DIP42S

Absolute Maxium Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$	V_{DD}	-0.3 to +9.0	V
Maximum Input Voltage	$V_{IN}max$	CL,DATA,WR,SIN,$\overline{BLK}$	-0.3 to +9.0	V
Maximum Output Voltage	V_{OUT}	S0 to S33,V_{FL}	V_{DD}-30toV_{DD}+0.3	V
Maximum Output Current	I_{OUT}	S0 to S33	3.0	mA
Allowable Power Dissipation	Pdmax	Ta=75°C	750	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

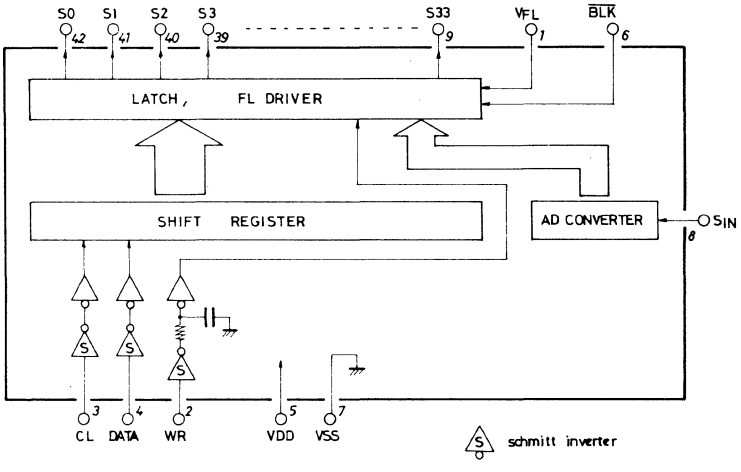
Allowable Operating Conditions at Ta=-30 to +75°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD}	V_{DD}	4.5 to 8.0	V
Input "H" Level Current	V_{IH}	$\overline{BLK}$	0.7V_{DD} to 8.0	V
Input "L" Level Current	V_{IL}	"	0 to 0.3V_{DD}	V
Rise Trigger Threshold Voltage	V_P	CL,DATA,WR	0.8V_{DD} to 8.0	V
Fall Trigger Threshold Voltage	V_N	"	0 to 0.2V_{DD}	V
Output Voltage	V_{OUT}	S0 to S33,V_{FL}	V_{DD}-25 to V_{DD}	V
Write Pulse Width	pw	WR	30 min	usec

Electrical Characteristics at Under Allowable Operating Conditions

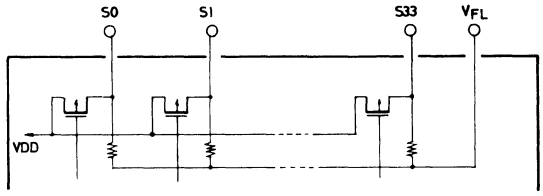
			min	typ	max	unit
Hysteresis Width	V_H	CL,DATA,WR	0.2V_{DD}		0.6V_{DD}	V
Input "H" Level Current	$I_{IH(1)}$	CL,DATA,WR,SIN,$\overline{BLK}$,V_I=8V			5.0	uA
Input "L" Level Current	$I_{IL(1)}$	" ,V_I=0V			5.0	uA
Output "H" Level Voltage	V_{OH}	S0toS33,Io=2.5mA	V_{DD}-3.0			V
Output OFF-State Voltage	V_{OFF}	" ,V_{FL}=V_{DD}-2.5V, Output OFF			V_{DD}-24	V
Self-Contained Resistance in Output	r_o	S0 to S33-V_{FL}, V_{DD}=5V,V_{FL}=-20V		130		kohm
AD Converter						
1st Step Light-Up Voltage	AD1	SIN	0.1V_{DD}			V
2nd Step Light-Up Voltage	AD2	"	0.2V_{DD}			V
3rd Step Light-Up Voltage	AD3	"	0.3V_{DD}			V
4th Step Light-Up Voltage	AD4	"	0.4V_{DD}			V
5th Step Light-Up Voltage	AD5	"	0.5V_{DD}			V
Supply Current	I_{DD}	V_{DD},input=0V,output=open			3.0	mA

Equivalent Circuit Block Diagram



Pin Description

S0 to S33, V_{FL} : Common pin for segment output and pull-down resistor



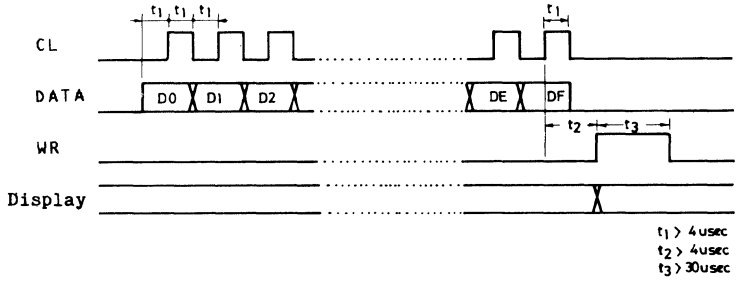
BLK : : Input for making display unlighted
$\overline{BLK}$="0"(V_{SS}) ..... Unlighted
$\overline{BLK}$="1"(V_{DD}) ..... Lighted

CL,DATA,WR : Data input

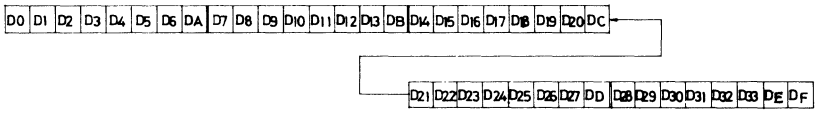
V_{DD},V_{SS} : Power supply pin

SIN : AD converter input
1st step light-up level ..... $0.1V_{DD}$(typ)
2nd step light-up level ..... $0.2V_{DD}$(typ)
3rd step light-up level ..... $0.3V_{DD}$(typ)
4th step light-up level ..... $0.4V_{DD}$(typ)
5th step light-up level ..... $0.5V_{DD}$(typ)

Data Input



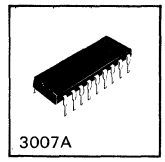
Inputting starts at D_0.



D0 to D33 : Display data
DA to DE : Dummy bit (don't care)
DF : S29 to S33 select

Dn="1":Sn="1"(=V_{DD})
Dn="0":Sn="0"(=V_{FL})
D_F="0":D29 to D33 → S29 to S33
DF="1":AD1 → S33
AD2 → S32
AD3 → S31
AD4 → S30
AD5 → S29

LC7572



C MOS IC

Preset Address Display LED Driver

Ⓔ 1464A

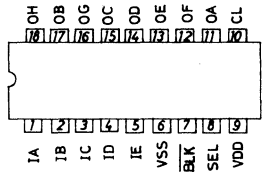
Applications :

(1) Electronic tuning preset address display.
(2) AMSS cuing number display.
(3) Record player music selection address display.

Features :

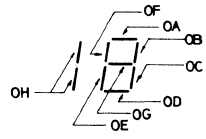
(1) 3 types of display.
 . 16-dot display
 . 0 to 19 decimal display
 . 0 to F hexadecimal display
(2) Blanking pin for blanking out display.
(3) Latch function.

Pin Assignment :

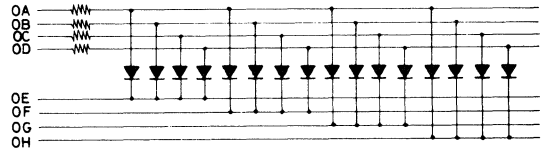


Connection

Decimal/hexadecimal

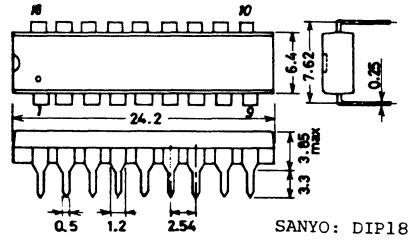


Dot



Display Font

Case Outline 3007A-D18IC
(unit:mm)



SANYO: DIP18

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$	V_{DD}	-0.3 to +9.0	V
Maximum Input Voltage	$V_{IN(1)}$	CL,IA to IE,$\overline{BLK}$	-0.3 to +9.0	V
	$V_{IN(2)}$	SEL	-0.3 to V_{DD}+0.3	V
Maximum Output Current	I_{OUT}	OA to OH	0 to 20	mA
Allowable Power Dissipation	Pdmax	Ta=85°C	300	mW
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-50 to +125	°C

Allowable Operating Conditions at Ta=-40 to +85°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD}	V_{DD}	4.5 to 8.0	V
Input "H" Level Voltage	$V_{IH(1)}$	CL,IA to IE,$\overline{BLK}$	0.7V_{DD} to 8.0	V
Input "L" Level Voltage	$V_{IL(1)}$	"	0 to 0.3V_{DD}	V
Input "H" Level Voltage	$V_{IH(2)}$	SEL	0.9V_{DD} to V_{DD}	V
Input "L" Level Voltage	$V_{IL(2)}$	"	0 to 0.1V_{DD}	V
Input "M" Level Voltage	V_{IM}	"	0.4V_{DD} to 0.6V_{DD}	V
Write Minimum Pulse Width	pw	CL	3.0min.	usec

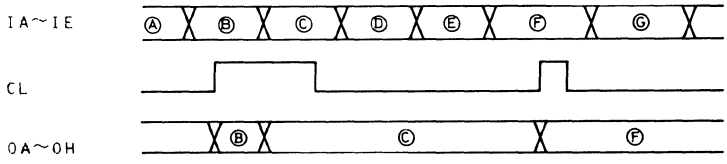
Electrical Characteristics/Under Allowable Operating Conditions

			min	typ	max	unit
Input "H" Level Current	$I_{IH(1)}$	CL,IA to IE,$\overline{BLK}$,V_I=8V			5.0	uA
Input "L" Level Current	$I_{IL(1)}$	" V_I=0V			5.0	uA
Input "H" Level Current	$I_{IH(2)}$	SEL,V_I=V_{DD}		100		uA
Input "L" Level Current	$I_{IL(2)}$	" ,V_I=0V		100		uA
Output "H" Level Voltage	$V_{OH(1)}$	OA to OH,I_O=15mA	V_{DD}-1.0			V
	$V_{OH(2)}$	" ,I_O=20mA	V_{DD}-1.25			V
Output "L" Level Voltage	$V_{OL(1)}$	OE to OH,I_O=15mA			1.0	V
	$V_{OL(2)}$	" ,I_O=20mA			1.25	V
Output Off Leak Current	I_{OFF}	OA to OD,Vo=0V			3.0	uA
Current Dissipation	I_{DD}	SEL=open,other input=0, Output=open			1.0	mA
Input Floating Voltage	V_{IF}	SEL,Input=open	0.45V_{DD}	0.55V_{DD}		V

Pin Description

IA~IE: Input pin

CL: Latch clock



$\overline{BLK}$: Input for making display unlighted

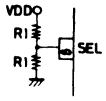
$\overline{BLK}$='0'(V_{SS})····· Unlighted

$\overline{BLK}$='1'(V_{DD})····· Lighted

SEL: Input for selecting display mode

SEL="0"(V_{SS}) ..... Dot display

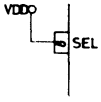
SEL="M" ..... Hexadecimal display



or

Open.

SEL="1"(V_{DD}) ..... Decimal display



V_{DD},V_{SS} : Power supply pin

OA to OH : Output pin

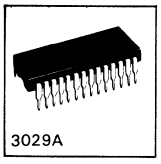
Truth Table

INPUT						OUTPUT		OUTPUT(SEL=0)							
$\overline{BLK}$	IA	IB	IC	ID	IE	SEL=1	SEL=M	OA	OB	OC	OD	OE	OF	OG	OH
	0	0	0	0	0	0	0	-	-	-	-	1	1	1	1
	1	0	0	0	0	1	1	1	-	-	-	0	1	1	1
	0	1	0	0	0	2	2	-	1	-	-	0	1	1	1
	1	1	0	0	0	3	3	-	-	1	-	0	1	1	1
	0	0	1	0	0	4	4	-	-	-	1	0	1	1	1
	1	0	1	0	0	5	5	1	-	-	-	1	0	1	1
	0	1	1	0	0	6	6	-	1	-	-	1	0	1	1
	1	1	1	0	0	7	7	-	-	1	-	1	0	1	1
	0	0	0	1	0	8	8	-	-	-	1	1	0	1	1
	1	0	0	1	0	9	9	1	-	-	-	1	1	0	1
	0	1	0	1	0	*	A	-	-	-	-	1	1	1	1
	1	1	0	1	0	*	b	-	-	-	-	1	1	1	1
	0	0	1	1	0	*	c	-	-	-	-	1	1	1	1
	1	0	1	1	0	*	d	-	-	-	-	1	1	1	1
	0	1	1	1	0	*	E	-	-	-	-	1	1	1	1
1	1	1	1	1	0	*	F	-	-	-	-	1	1	1	1
	0	0	0	0	1	10	*	-	1	-	-	1	1	0	1
	1	0	0	0	1	11	*	-	-	1	-	1	1	0	1
	0	1	0	0	1	12	*	-	-	-	1	1	1	0	1
	1	1	0	0	1	13	*	1	-	-	-	1	1	1	0
	0	0	1	0	1	14	*	-	1	-	-	1	1	1	0
	1	0	1	0	1	15	*	-	-	1	-	1	1	1	0
	0	1	1	0	1	16	*	-	-	-	1	1	1	1	0
	1	1	1	0	1	17	*	-	-	-	-	1	1	1	1
	0	0	0	1	1	18	*	-	-	-	-	1	1	1	1
	1	0	0	1	1	19	*	-	-	-	-	1	1	1	1
	0	1	0	1	1	*	*	-	-	-	-	1	1	1	1
	1	1	0	1	1	*	*	-	-	-	-	1	1	1	1
	0	0	1	1	1	*	*	-	-	-	-	1	1	1	1
	1	0	1	1	1	*	*	-	-	-	-	1	1	1	1
	0	1	1	1	1	*	*	-	-	-	-	1	1	1	1
	1	1	1	1	1	*	*	-	-	-	-	1	1	1	1
0	×	×	×	×	×	*	*	-	-	-	-	1	1	1	1

1: 'H' level
M: 1/2 V_{DD} (medium level)
0: 'L' level
-: open
*: blanking

CL=1: INPUT→OUTPUT
CL=0: HOLD

LC7815



C MOS IC

2-Pole 4-Position Analog Function Switch

Ⓔ 1039B

The LC7815 is a 2-pole 4-position analog function switch with 2 built-in C-MOS analog switches (LC4066 type). A soft touch of a button enables switchover of the input signal source of an audio amplifier.

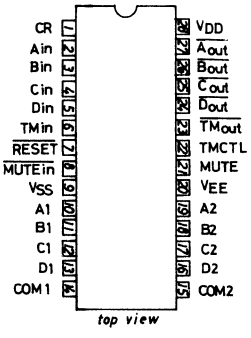
Use

Function switchover of amplifier, receiver, etc. (2 poles 4 positions)

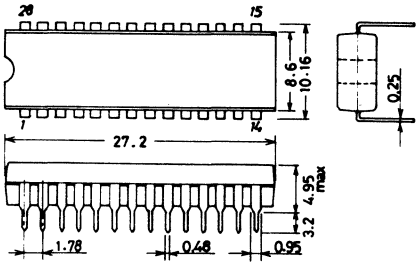
Features

1. Good distortion characteristic because of built-in analog switches of LC4066 type: Distortion 0.01 % max./ v_{in}=1Vrms, V_{DD}=15 to 18 V
2. Capable of outputting audio muting control signal to minimize noise to be generated at the time of switchover
3. Built-in controller for tape monitor switchover (using LC4066B together)
4. Built-in driver for LED which displays function mode, tape monitor mode
5. Since control input can be operated from + supply alone when using dual supplies, interface with other circuits can be achieved easily.
6. Since audio muting control signal can be triggered independently from external pin ($\overline{MUTE}_{in}$), audio muting at the time of return from backup can be achieved easily.
7. Control input pin ($\overline{RESET}$) to be used for turning OFF all analog switches
8. Backup can be performed easily because of C-MOS structure. (Backup voltage: 3 V min.)
9. Operating voltage: 4.5 to 18.0 V/single supply, ±4.5 to ±9.0 V/dual supplies
10. Package: DIP-28 (Shrink type)

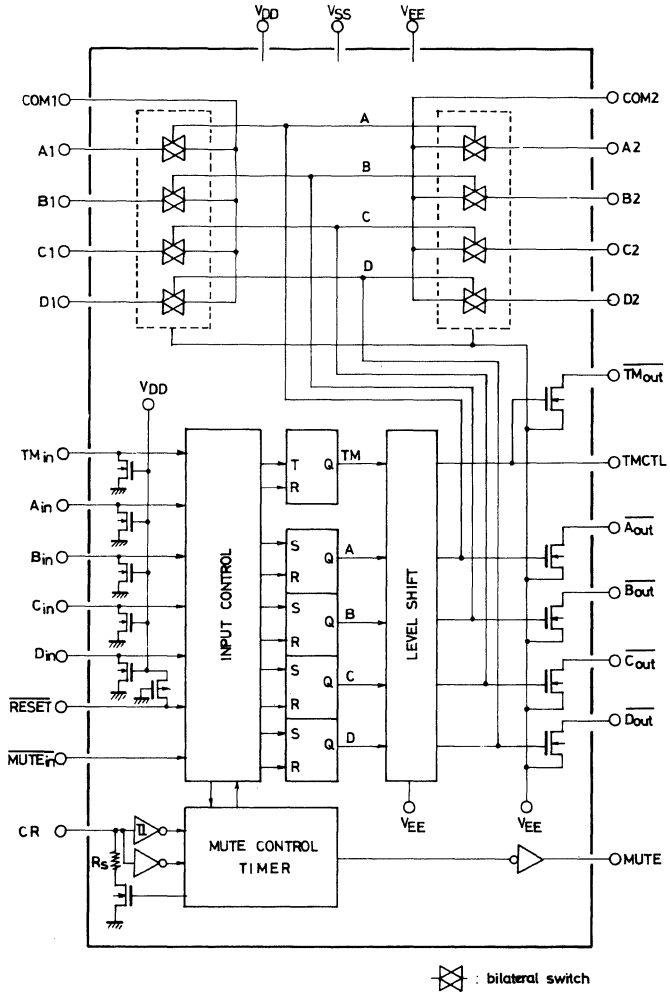
Pin Assignment



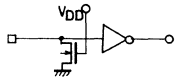
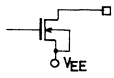
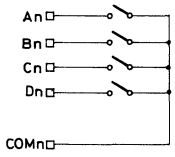
Case Outline 3029A-D28SIC
(unit: mm)



Equivalent Circuit Block Diagram

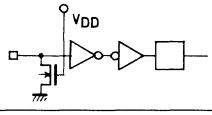
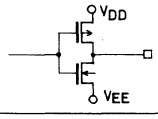
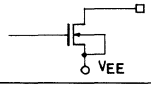
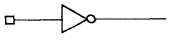
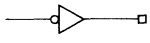
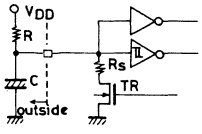
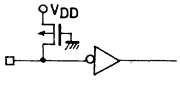


Pin Description

Pin Name	Pin No.	Type of Input/Output	Pin Functions
V_{DD} V_{SS} V_{EE}	28 9 20		• Power supply pins Single supply (+): $V_{SS}=V_{EE}=GND$ Dual supplies (+−): $V_{SS}=GND$, $V_{EE}=(-)V$
A_{in}, B_{in}, C_{in}, D_{in}	2, 3, 4, 5		• Specified input pins for turning ON individual analog switches • Priority order of simultaneous push ($A_{in}>B_{in}>C_{in}>D_{in}$) • Prevention of malfunction attributable to pulse noise (Pulse width is discriminated by muting delay time.)
$\overline{A_{out}}$, $\overline{B_{out}}$, $\overline{C_{out}}$, $\overline{D_{out}}$	27, 26, 25, 24		• Output of driver for LED which displays ON state corresponding to individual analog switches • N channel open drain (Source is connected to V_{EE}.)
A_1, B_1, C_1, D_1 A_2, B_2, C_2, D_2 COM 1 COM 2	10, 11, 12, 13 19, 18, 17, 16 14 15		• A to D: Audio signal input pins • COM: Audio signal output pins • Signal inputs (A to D) conduct according to signal inputs (A_{in} to D_{in}) as follows:

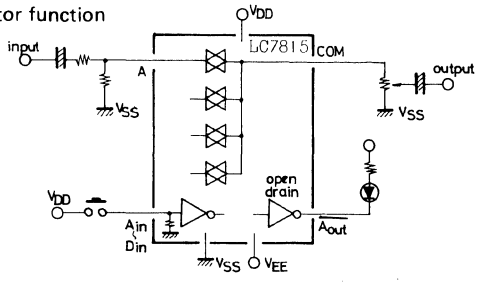
COM output		A_n	B_n	C_n	D_n
Specified input	A_{in}	1	0	0	0
	B_{in}	*	1	0	0
	C_{in}	*	*	1	0
	D_{in}	*	*	*	1

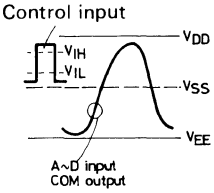
*: Don't care.

TM_{in}	6		• Input pin for specifying tape monitor mode ON/OFF • Rise of input signal is detected; monitor mode ON/OFF are inverted to monitor mode OFF/ON respectively.
TMCTL	22		• Output pin for controlling external analog switch (LC4066B) for tape monitor • Source of N channel transistor of complementary buffer output is connected to V_{EE}.
$\overline{TM_{out}}$	23		• Output pin for driver for LED which displays tape monitor state as well as external analog switch (LC4066B) for tape monitor • $\overline{TM_{out}}$ is opposite in polarity to TMCTL.
$\overline{MUTE_{in}}$	8		• Input pin for forcing audio muting control signal (MUTE) to be triggered externally • If fixed at 'L' level, MUTE output becomes 'H' level.
MUTE	21		• Output pin for audio muting control signal • Signal with pulse width to be determined by external constant at CR pin is outputted at the time of function switchover or $\overline{MUTE_{in}}$ input.
CR	1		• CR time constant pin for determining time interval of audio muting control signal • Time lag (muting delay) between muting signal rise and analog switch switchover depends on $C \cdot R_S$ time constant at the time of transistor ON.
$\overline{RESET}$	7		• Input pin for turning OFF all analog switches and resetting tape monitor flip-flop ('L' level active)

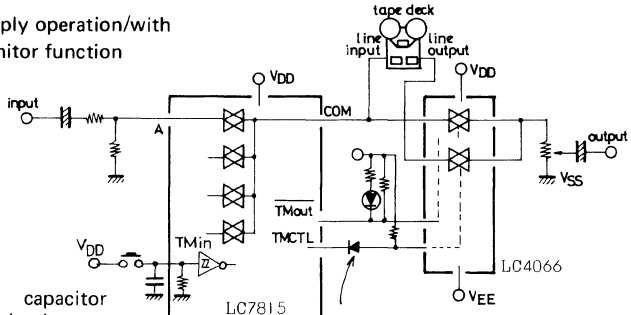
■ **Sample Application Circuits**

1. Dual-supply operation/without tape monitor function





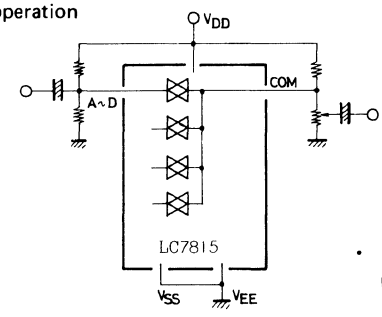
2. Dual-supply operation/with tape monitor function

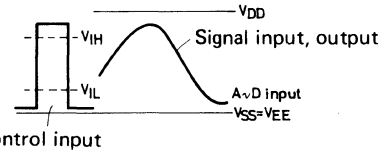


Connect a capacitor when using in the surroundings with much noise.

Diode for cutting off current flow at the backup mode.

3. Single-supply operation

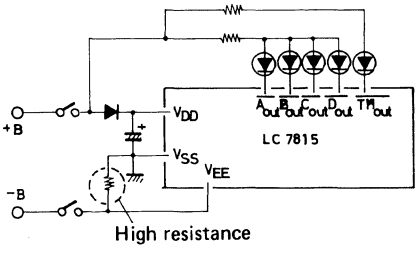




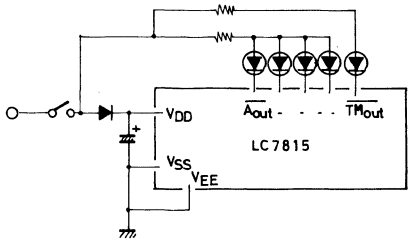
- For using tape monitor function, make connection as shown in 2 above.

4. Backup

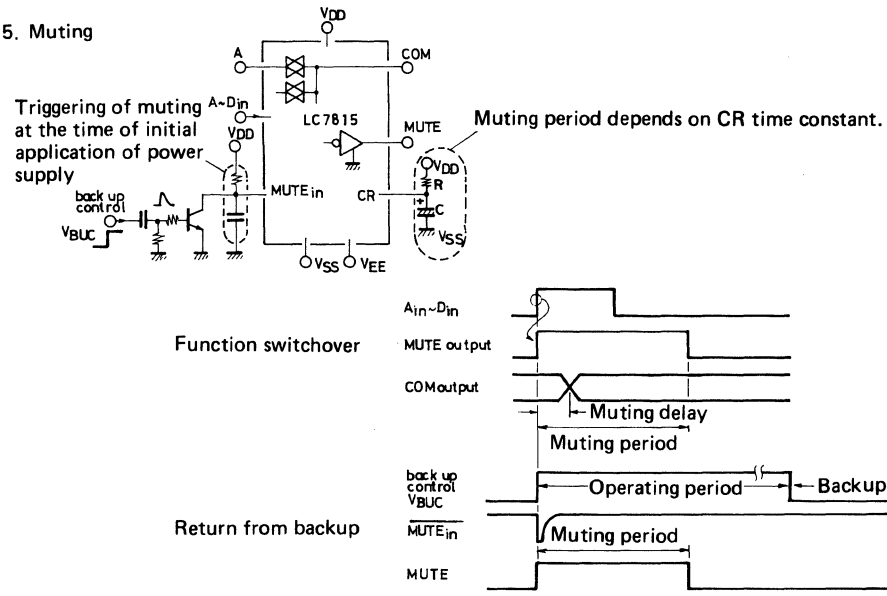
(1) Dual-supply operation



(2) Single-supply operation



5. Muting



Absolute Maximum Ratings/Ta=25 ±2°C

Maximum Supply Voltage	V_{DD}		$V_{SS}-0.3 \sim V_{EE}+20$	V
	V_{EE}		$V_{DD}-20 \sim V_{SS}+0.3$	V
Output Current	I_{OUT}	$\overline{A_{out}}$, $\overline{B_{out}}$, $\overline{C_{out}}$, $\overline{D_{out}}$, $\overline{TM_{out}}$	30	mA
Output Voltage	V_{OUT}	$\overline{A_{out}}$, $\overline{B_{out}}$, $\overline{C_{out}}$, $\overline{D_{out}}$, $\overline{TM_{out}}$	$V_{EE}-0.3 \sim V_{DD}+0.3$	V
Voltage Difference at analog switch ON	ΔV_{on}	Switch ON	0.5	V
Allowable Power Dissipation	$P_d max$	$Ta \leqq 85°C$	350	mW
Operating Temperature	T_{opg}		−40~+85	°C
Storage Temperature	T_{stg}		−40~+125	°C

Allowable Operating Ranges/Ta=−40~+85°C

Characteristic	Symbol	Pin No.	Conditions	min	typ	max	unit
Supply Voltage	V_{DD1}	V_{DD}(28)	$V_{EE} \leqq V_{SS}$	$V_{SS}+4.5$		$V_{EE}+18$	V
	V_{EE}	V_{EE}(20)	$V_{DD} \geqq V_{SS}+4.5$	$V_{DD}-18$		V_{SS}	V
	V_{DD2}	V_{DD}(28)	Backup, $V_{EE} \leqq V_{SS}$	$V_{SS}+3$		$V_{SS}+18$	V
'H' Level Input Voltage	V_{IH1}	A_{in}(2)~D_{in}(5), $\overline{RESET}$(7), $\overline{MUTE_{in}}$(8)		$0.75V_{DD}$		V_{DD}	V
	V_{IH2}	TM_{in}(6)		$0.8V_{DD}$		V_{DD}	V
'L' Level Input Voltage	V_{IL1}	A_{in}(2)~D_{in}(5), $\overline{RESET}$(7), $\overline{MUTE_{in}}$(8)		V_{SS}		$0.25V_{DD}$	V
	V_{IL2}	TM_{in}(6)		V_{SS}		$0.2V_{DD}$	V
Analog Switch Input Voltage	V_{IN}	A_1(10)~D_1(13), A_2(19)~D_2(16)		V_{EE}		V_{DD}	V
External Capacitance for Muting Timer	C	CR(1)				10	μF
External Resistance for Muting Timer	R	CR(1)	$V_{DD}-V_{SS}=4.5V$	40		100	kΩ
			$V_{DD}-V_{SS} \geqq 9V$	100		300	kΩ
Input Receiving Pulse Width	T_{IN}	A_{in}(2)~D_{in}(5), TM_{in}(6)	$V_{DD}=9V$, C=3.3μF, R=220kΩ	120			ms

Electrical Characteristics/Ta=25 ±2°C, V_{SS}=0V

Characteristic	Symbol	Pin No.	Conditions	min	typ	max	unit
'H' Level Output Voltage	V_{OH1}	TMCTL(22)	I_{OH}=−0.1mA V_{DD}=4.5~18V	0.8V_{DD}		V_{DD}	V
	V_{OH2}	MUTE(21)	I_{OH}=−0.4mA, V_{DD}=4.5V	V_{DD}−1.5		V_{DD}	V
			I_{OH}=−0.4mA, V_{DD}=9V	V_{DD}−0.5		V_{DD}	V
'L' Level Output Voltage	V_{OL1}	TMCTL(22)	I_{OL}=0.1mA	V_{EE}		0.2X (V_{DD}−V_{EE})	V
	V_{OL2}	MUTE(21)	I_{OL}=0.4mA, V_{DD}=4.5V	0		1.5	V
			I_{OL}=0.4mA, V_{DD}=9V	0		0.5	V
	VOL3	$\overline{A_{out}}$(27), to $\overline{D_{out}}$(24), $\overline{TM_{out}}$(23)	I_{OL}=7mA, V_{DD}−V_{EE}=4.5V	VEE		V_{EE}+2	V
			I_{OL}=30mA, V_{DD}−V_{EE}=9V	V_{EE}		V_{EE}+4	V
			I_{OL}=30mA, V_{DD}−V_{EE}=18V	V_{EE}		V_{EE}+2	V
Analog Switch ON Resistance	R_{on}	A_1(10), B_1(11), C_1(12), D_1(13), COM1(14), A_2(19), B_2(18), C_2(17), D_2(16) COM2(15)	I=1mA, V_{DD}−V_{EE}=4.5V		400		Ω
			I=1mA, V_{DD}−V_{EE}=9V		120		Ω
			I=1mA, V_{DD}−V_{EE}=18V		80		Ω
'H' Level Input Current	I_{IL1}	A_{in}(2), B_{in}(3), C_{in}(4), D_{in}(5), TM_{in}(6)	V_{DD}=9V, V_{IN}=V_{DD}	20		90	μA
	I_{IH2}	$\overline{MUTE}_{in}$(8)	V_{IN}=V_{DD}=18V			10	μA
'L' Level Input Current	I_{IL1}	$\overline{RESET}$(7)	V_{DD}=9V, V_{IN}=V_{DD}	−90		−20	μA
	I_{IL2}	$\overline{MUTE}_{in}$(8)	V_{IN}=V_{SS}	−10			μA
Input/Output OFF Leak Current	I_{OFF1}	$\overline{A_{out}}$(27)~$\overline{D_{out}}$(24) $\overline{TM_{out}}$(23)	Output transistor OFF Vo=V_{EE}+18V			10	μA
	I_{OFF2}	CR(1)	Output transistor OFF Vo=V_{SS}+18V			3	μA
	I_{OFF3}	A_1(10),~D_1(13), COM1(14), A2(19)~D_2(16), COM2(15)	Analog switch OFF V_{IN}=Vo=V_{EE} to 18V	−10		10	μA
Input Floating Voltage	V_{IF1}	A_{in}(2)~D_{in}(5), TM_{in}(6)	V_{DD}=4.5 to 18V			0.75	V
	V_{IF2}	$\overline{RESET}$(7)	V_{DD}=4.5 to 18V	V_{DD}−0.75			V
Total Harmonic Distortion	THD_1	COM1(14), COM2(15)	V_{IN}=1Vrms, f=1kHz, V_{DD}−V_{EE} =15 to 18V, Refer to Fig. 1.			0.01	%
	THD_2	COM1(14), COM2(15)	V_{IN}=0.1Vrms, f=1kHz, V_{DD} −V_{EE}=4.5V, Refer to Fig. 1.			0.05	%
Feedthrough (Switch OFF)	FTH	A_1(10), D_1(13) to COM1(14)	V_{DD}−VEE=18V, f=10kHz V_{in}=0.77Vrms, Refer to Fig. 2.	55			dB
		A_2(19), D_2(16) to COM2(15)	R_L=47kΩ				
Crosstalk	CT	A_1(10), D_1(13) to COM2(15)	V_{DD}−V_{EE}=18V, f=10kHz V_{in}= 0.77Vrms, Refer to Fig. 3.	75			dB
		A_2(19), D_2(16) to COM1(14)	R_L=47kΩ				
Muting period	T_{M1}	MUTE(21)	V_{DD}=9V, Refer to Fig. 4. C=3.3μF ±20%, R=220kΩ ±5%	350	580	1000	ms
	T_{M2}	MUTE(21)	V_{DD}=9V, C=3.3μF ±0%, R=220kΩ ±0%	450	580	800	ms

				min	typ	max	unit
Switch Switchover Delay Time	T_{SWD}	$A_{in}(2)$ to $D_{in}(5)$ $TM_{in}(6)$	V_{DD}=9V, Refer to Fig. 5. C=3.3μF, R=220kΩ	30	50	120	ms
Supply Current	I_{DD1}	$V_{DD}(28)$	Operating, Refer to Fig. 6. $V_{DD}-V_{EE}$=18V			1000	μA
	I_{DD2}	$V_{DD}(28)$	Backup, V_{DD}=5V, $V_{SS}=V_{EE}$			3	μA

Fig. 1 Total harmonic distortion

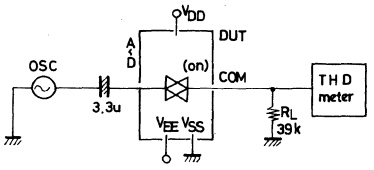
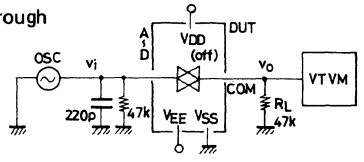


Fig. 2 Feedthrough

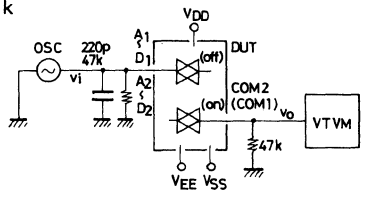


$$FTH = 20 \log \frac{v_o}{v_i} \quad (dB)$$

v_i = 770mVrms

$V_{DD} - V_{EE}$ = 18V

Fig. 3 Crosstalk



$$CT = 20 \log \frac{v_o}{v_i} \quad (dB)$$

v_i = 770mVrms

$V_{DD} - V_{EE}$ = 18V

Fig. 4 Muting period

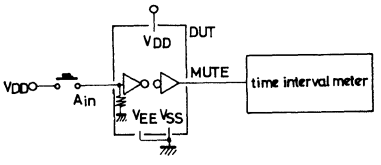


Fig. 6 Supply current

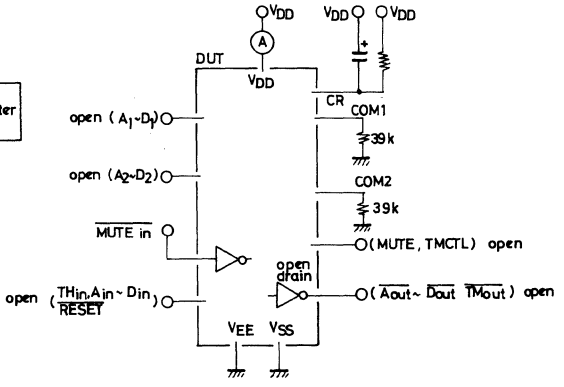
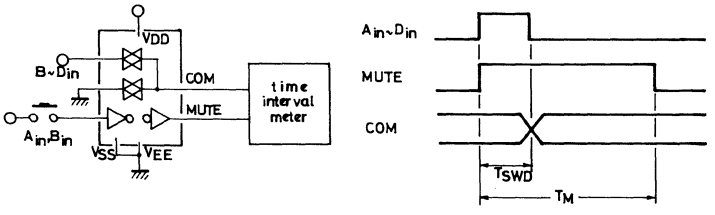
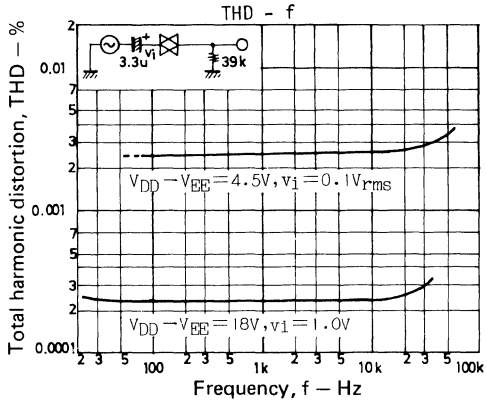


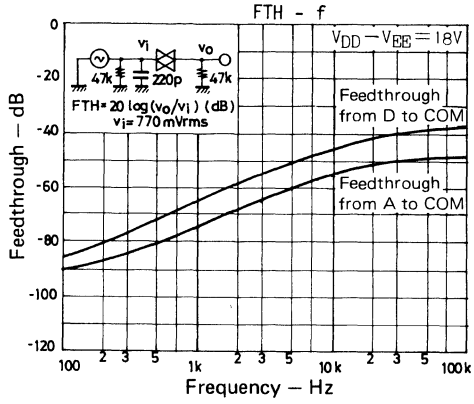
Fig. 5 Switch switchover delay time

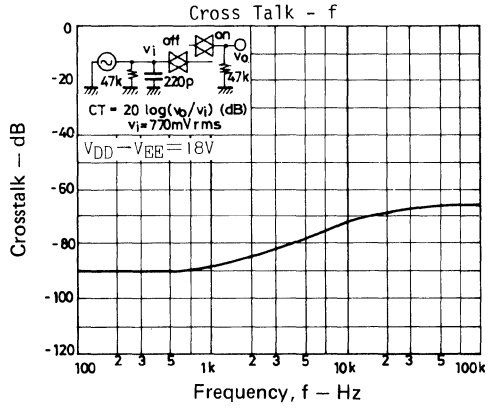


T_M: Muting period

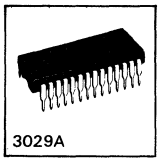
T_{SWD}: Switch switchover delay time


THD - f
Total harmonic distortion, THD — %
3.3u
vi
39k
VDD−VEE=4.5V, vi=0.1Vrms
VDD−VEE=18V, vi=1.0V
Frequency, f — Hz


FTH - f
VDD−VEE=18V
vi
vo
47k
220p
47k
FTH=20 log(vo/vi) (dB)
vi=770mVrms
Feedthrough from D to COM
Feedthrough from A to COM
Feedthrough — dB
Frequency — Hz


Cross Talk - f
off
on
vi
vo
47k
220p
47k
CT = 20 log(vo/vi) (dB)
vi=770mVrms
VDD−VEE=18V
Crosstalk — dB
Frequency, f — Hz

LC7815H



C MOS IC

2-Pole 4-Position Analog Function Switch

Ⓔ 1509

General Description

The LC7815H is a 2-pole 4-position analog function switch with 2 built-in C-MOS analog switches (LC4066 type). A soft touch of a button enables switchover of the input signal source of an audio amplifier.

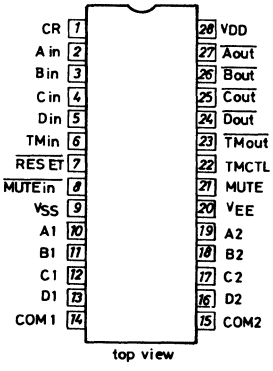
Use

Function switchover of amplifier, receiver, etc. (2 poles 4 positions)

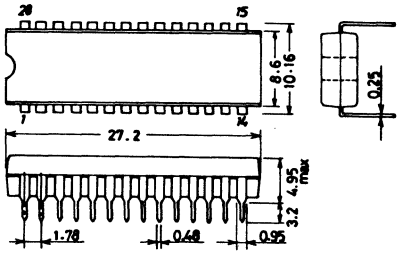
Features

1. Good distortion characteristic because of built-in analog switches of LC4066 type: Distortion 0.01 % max.) V_{in} = 1 Vrms, V_{DD} = 15 to 23 V
2. Capable of outputting audio muting control signal to minimize noise to be generated at the time of switchover
3. Built-in controller for tape monitor switchover (using LC4066B together)
4. Built-in driver for LED which displays function mode, tape monitor mode
5. Since control input can be operated from + supply alone when using dual supplies, interface with other circuits can be achieved easily.
6. Since audio muting control signal can be triggered independently from external pin ($\overline{MUTE_{in}}$), audio muting at the time of return from backup can be achieved easily.
7. Control input pin ($\overline{RESET}$) to be used for turning OFF all analog switches
8. Backup can be performed easily because of C-MOS structure. (Backup voltage: 2.4 V min.)
9. Operating voltage: 4.5 to 23 V/single supply, ±4.5 to ±11.5 V/dual supplies.
10. Package: DIP-28S (Shrink type)

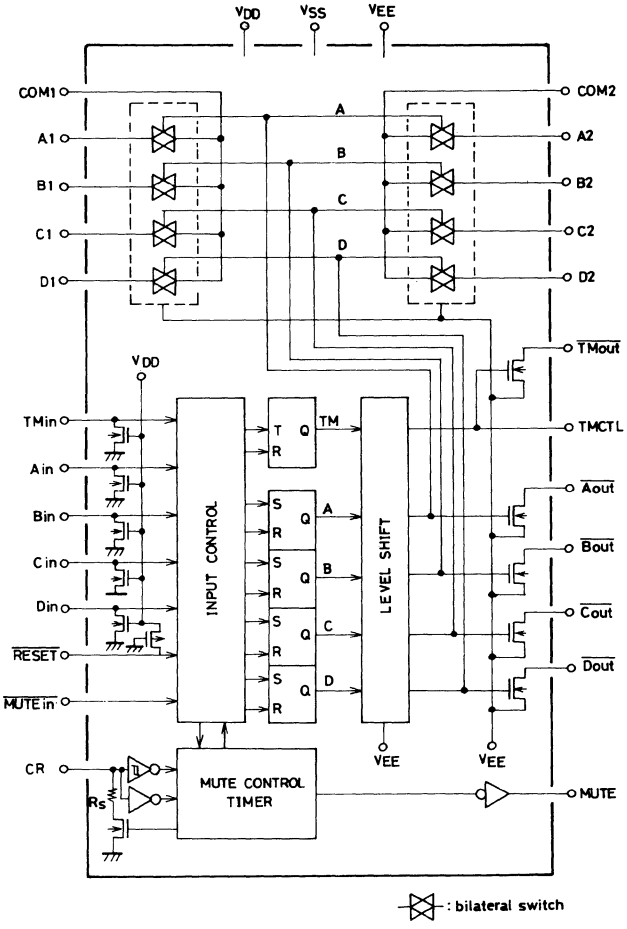
Pin Assignment



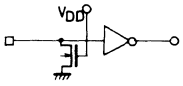
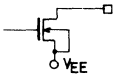
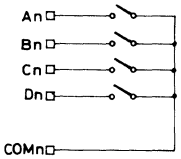
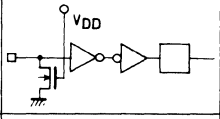
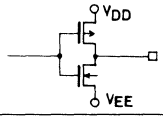
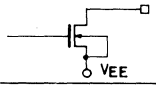
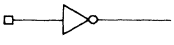
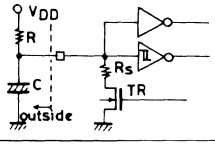
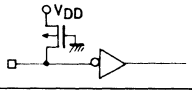
Case Outline 3029A-D28SIC
(unit: mm)



Equivalent Circuit Block Digram

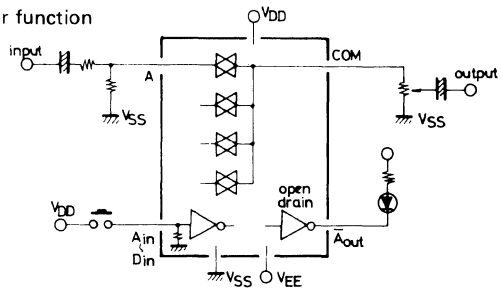


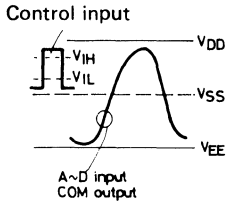
Pin Description

Pin Name	Pin No.	Type of Input/Output	Pin Functions
V_{DD} V_{SS} V_{EE}	28 9 20		• Power supply pins Single supply (+): $V_{SS}=V_{EE}=GND$ Dual supplies (+−): $V_{SS}=GND$, $V_{EE}=(-)V$
A_{in}, B_{in}, C_{in}, D_{in}	2, 3, 4, 5		• Specified input pins for turning ON individual analog switches • Priority order of simultaneous push ($A_{in}>B_{in}>C_{in}>D_{in}$) • Prevention of malfunction attributable to pulse noise (Pulse width is discriminated by muting delay time.)
$\overline{A_{out}}$, $\overline{B_{out}}$, $\overline{C_{out}}$, $\overline{D_{out}}$	27, 26, 25, 24		• Output of driver for LED which displays ON state corresponding to individual analog switches • N channel open drain (Source is connected to V_{EE}.)
A_1, B_1, C_1, D_1 A_2, B_2, C_2, D_2 COM 1 COM 2	10, 11, 12, 13 19, 18, 17, 16 14 15		• A to D: Audio signal input pins ◦ COM: Audio signal output pins ◦ Signal inputs (A to D) conduct according to signal inputs (A_{in} to D_{in}) as follows: COM output: A_n B_n C_n D_n Specified input: A_{in} 1 0 0 0 B_{in} * 1 0 0 C_{in} * * 1 0 D_{in} * * * 1 *: Don't care.
TM_{in}	6		• Input pin for specifying tape monitor mode ON/OFF • Rise of input signal is detected; monitor mode ON/OFF are inverted to monitor mode OFF/ON respectively.
TMCTL	22		• Output pin for controlling external analog switch (LC4066B) for tape monitor • Source of N channel transistor of complementary buffer output is connected to V_{EE}.
$\overline{TM_{out}}$	23		• Output pin for driver for LED which displays tape monitor state as well as external analog switch (LC4066B) for tape monitor • $\overline{TM_{out}}$ is opposite in polarity to TMCTL.
$\overline{MUTE_{in}}$	8		◦ Input pin for forcing audio muting control signal (MUTE) to be triggered externally ◦ If fixed at 'L' level, MUTE output becomes 'H' level.
MUTE	21		• Output pin for audio muting control signal ◦ Signal with pulse width to be determined by external constant at CR pin is outputted at the time of function switchover or $\overline{MUTE_{in}}$ input.
CR	1		◦ CR time constant pin for determining time interval of audio muting control signal • Time lag (muting delay) between muting signal rise and analog switch switchover depends on $C \cdot R_S$ time constant at the time of transistor ON.
$\overline{RESET}$	7		• Input pin for turning OFF all analog switches and resetting tape monitor flip-flop ('L' level active)

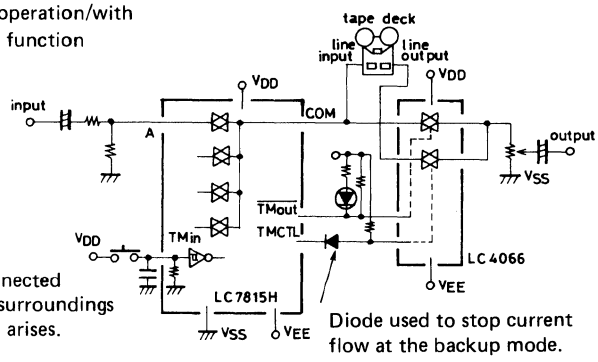
■ Application Circuits

1. Dual-supply operation/without tape monitor function





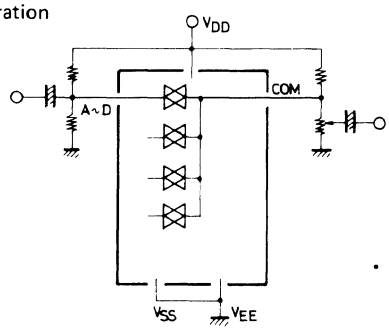
2. Dual-supply operation/with tape monitor function

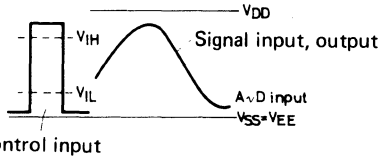


A capacitor is connected when used in the surroundings where much noise arises.

Diode used to stop current flow at the backup mode.

3. Single-supply operation

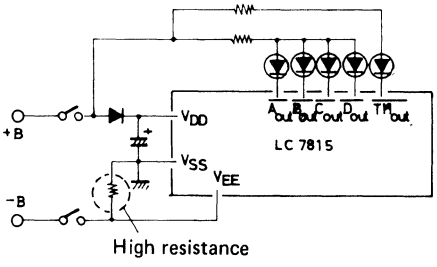




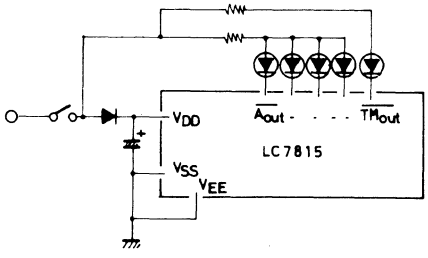
- For using tape monitor function, make connection as shown in 2 above.

4. Backup

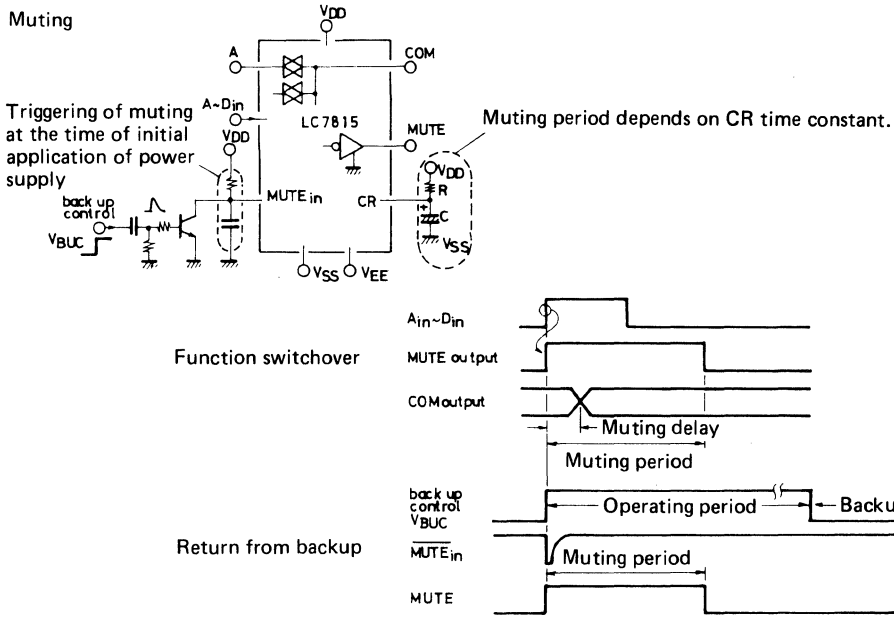
(1) Dual-supply operation



(2) Single-supply operation



5. Muting



Absolute Maximum Ratings/Ta=25 ±2°C

Maximum Supply Voltage	$V_{DD}max$		V_{SS}−0.3 to V_{EE}+25	V
	V_{EE}		V_{DD}−25 to V_{SS}+0.3	V
Output Current	I_{OUT}	$\overline{A_{out}}$, $\overline{B_{out}}$, $\overline{C_{out}}$, $\overline{D_{out}}$, $\overline{TM_{out}}$	30	mA
Output Voltage	V_{OUT}	$\overline{A_{out}}$, $\overline{B_{out}}$, $\overline{C_{out}}$, $\overline{D_{out}}$, $\overline{TM_{out}}$	V_{EE}−0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	$P_d max$	Ta≦85°C	350	mW
Voltage Difference at analog switch ON	ΔV_{on}	Switch ON	0.5	V
Operating Temperature	T_{opg}		−40 to +85	°C
Storage Temperature	T_{stg}		−40 to +125	°C

Allowable Operating Ranges/Ta=−40~+85°C

		Pin No.		min	typ	max	unit
Supply Voltage	V_{DD1}	V_{DD}(28)	V_{EE}≦V_{SS}	V_{SS}+4.5		V_{EE}+23	V
	V_{EE}	V_{EE}(20)	V_{DD}≧V_{SS}+4.5V	V_{DD}−23		V_{SS}	V
	V_{DD2}	V_{DD}(28)	Backup	V_{SS}+2.4		V_{SS}+23	V
'H' Level Input Voltage	V_{IH1}	A_{in}(2) to D_{in}(5), $\overline{RESET}$(7), $\overline{MUTE}_{in}$(8)	V_{EE}≦V_{SS}	0.75V_{DD}		V_{DD}	V
	V_{IH2}	TM_{in}(6)		0.8V_{DD}		V_{DD}	V
'L' Level Input Voltage	V_{IL1}	A_{in}(2) to D_{in}(5), $\overline{RESET}$(7), $\overline{MUTE}_{in}$(8)		V_{SS}		0.25V_{DD}	V
	V_{IL2}	TM_{in}(6)		V_{SS}		0.2V_{DD}	V
Analog Switch Input Voltage	V_{IN}	A_1(10) to D_1(13), A_2(19) to D_2(16)		V_{EE}		V_{DD}	V
External Capacitance for Muting Timer	C	CR(1)				10	μF
External Resistance for Muting Timer	R	CR(1)	V_{DD}−V_{SS}=4.5V	40		100	kΩ
			14>V_{DD}−V_{SS}≧9V	80		300	kΩ
External Resistance for Muting Timer	R	CR(1)	18>V_{DD}−V_{SS}≧14V	90		300	kΩ
			23>V_{DD}−V_{SS}≧18V	100		300	kΩ

							unit
Input Receiving Pulse Width	T_{IN}	$A_{in}(2)$ to $D_{in}(5)$, $TM_{in}(6)$	V_{DD}=9V, C=3.3μF, R=220kΩ	120			ms

Electrical Characteristics/Ta=25 ±2°C, V_{SS}=0V

		Pin No.		min	typ	max	unit
'H' Level Output Voltage	V_{OH1}	TMCTL(22)	I_{OH}=−0.1mA V_{DD}=4.5 to 23V	0.8V_{DD}		V_{DD}	V
	V_{OH2}	MUTE(21)	I_{OH}=−0.4mA, V_{DD}=4.5V	V_{DD}−1.5		V_{DD}	V
			I_{OH}=−0.4mA, V_{DD}=9V	V_{DD}−0.5		V_{DD}	V
'L' Level Output Voltage	V_{OL1}	TMCTL(22)	I_{OL}=0.1mA	V_{EE}		0.2 (V_{DD}−V_{EE})	V
	V_{OL2}	MUTE(21)	I_{OL}=0.4mA, V_{DD}=4.5V	0		1.5	V
			I_{OL}=0.4mA, V_{DD}=9V	0		0.5	V
	VOL3	$\overline{A_{out}}$(27), $\overline{B_{out}}$(26), $\overline{C_{out}}$(25), $\overline{D_{out}}$(24), $\overline{TM_{out}}$(23)	I_{OL}=7mA, V_{DD}−V_{EE}=4.5V	VEE		V_{EE}+2	V
			I_{OL}=30mA, V_{DD}−V_{EE}=9V	V_{EE}		V_{EE}+4	V
			I_{OL}=30mA, V_{DD}−V_{EE}=18V	V_{EE}		V_{EE}+2	V
Analog Switch ON Resistance	R_{ON}	A_1(10), B_1(11), C_1(12), D_1(13), COM1(14), A_2(19), B_2(18), C_2(17), D_2(16) COM2(15)	I=1mA, V_{DD}−V_{EE}=4.5V		400	1000	Ω
			I=1mA, V_{DD}−V_{EE}=9V		120	300	Ω
			I=1mA, V_{DD}−V_{EE}=18V		80	200	Ω
			I=1mA, V_{DD}−V_{EE}=23V		70	180	Ω
'H' Level Input Current	I_{IH1}	$A_{in}(2)$, $B_{in}(3)$, $C_{in}(4)$, $D_{in}(5)$, $TM_{in}(6)$	V_{IN}=V_{DD}, V_{DD}=9V	20		90	μA
			V_{IN}=V_{DD}, V_{DD}=11.5V	40		160	μA
	I_{IH2}	$\overline{MUTE_{in}}$(8)	V_{IN}=V_{DD}=18V			10	μA
'L' Level Input Current	I_{IL1}	$\overline{RESET}$(7)	V_{IN}=V_{DD}, V_{DD}=9V	−90		−20	μA
			V_{IN}=V_{DD}, V_{DD}=11.5V	−160		−40	μA
	I_{IL2}	$\overline{MUTE_{in}}$(8)	V_{IN}=V_{SS}	−10			μA
Input/Output OFF Leak Current	I_{OFF1}	$\overline{A_{out}}$(27) to $\overline{D_{out}}$(24) $\overline{TM_{out}}$(23)	Output transistor OFF Vo=V_{EE}+18V			10	μA
			Output transistor OFF Vo=V_{EE}+23V			20	μA
	I_{OFF2}	CR(1)	Output transistor OFF Vo=V_{SS}+18V			3	μA
			Output transistor OFF Vo=V_{SS}+23V			100	μA
	I_{OFF3}	A_1(10) to D_1(13), COM1(14), A_2(19) to D_2(16), COM2(15)	Analog switch OFF V_{IN}, V_o=V_{EE} to 18V	−10		10	μA
Input Floating Voltage	V_{IF1}	$A_{in}(2)$ to $D_{in}(5)$, $TM_{in}(6)$	V_{DD}=4.5 to 23V			0.75	V
	V_{IF2}	$\overline{RESET}$(7)	V_{DD}=4.5 to 23V	V_{DD}−0.75			V
Total Harmonic Distortion	THD_1	COM1(14), COM2(15)	V_{IN}=1Vrms, f=1kHz, V_{DD}−V_{EE} =15V to 23V, Refer to Fig. 1			0.01	%
	THD_2	COM1(14), COM2(15)	V_{IN}=0.1Vrms, f=1kHz, V_{DD} −V_{EE}=4.5V, Refer to Fig. 1.			0.05	%
Feedthrough (Switch OFF)	FTH	A_1(10), D_1(13) to COM1(14)	V_{DD}−V_{EE}=18V, F=10kHz V_{in}=0.77Vrms, Refer to Fig. 2. R_L=47kΩ	55			dB
		A_2(19), D_2(16) to COM2(15)					

				min	typ	max	unit
Crosstalk	CRO	A_1(10) to COM2(15) D_1(13) A_2(19) to COM1(14) D_2(16)	$V_{DD}-V_{EE}$=23V, f=10kHz V_{in}=0.77Vrms, Refer to Fig. 3 R_L=47kΩ		75		dB
Muting period	T_{M1}	MUTE(21)	V_{DD}=9V, Refer to Fig. 4. C=3.3μF ±20%, R=220kΩ ±5%	350	580	1000	ms
	T_{M2}	MUTE(21)	V_{DD}=9V, C=3.3μF ±0%, R=220kΩ ±0%	450	580	800	ms
Switch Switchover Delay Time	T_{SWD}	A_{in}(2) to D_{in}(5), TM_{in}(6)	V_{DD}=9V, Refer to Fig. 5. C=3.3μF, R=220kΩ	30	50	120	ms
Supply Current	I_{DD1}	V_{DD}(28)	Operating, Refer to Fig. 6. $V_{DD}-V_{EE}$=23V			1000	μA
	I_{DD2}	V_{DD}(28)	Backup, V_{DD}=5V, V_{SS}=V_{EE}			3	μA

Fig. 1 Total harmonic distortion

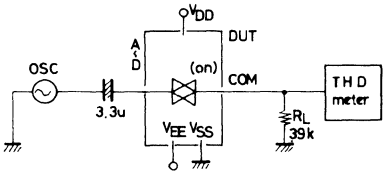
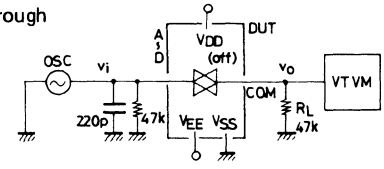


Fig. 2 Feedthrough

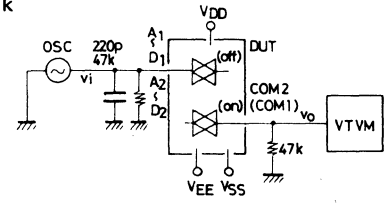


$$FTH = 20 \log \frac{V_O}{V_i} \quad (dB)$$

v_i = 770mVrms

$V_{DD} - V_{EE}$ = 18V

Fig. 3 Crosstalk



$$CT = 20 \log \frac{V_O}{V_i} \quad (dB)$$

v_i = 770mVrms

$V_{DD} - V_{EE}$ = 18V

Fig. 4 Muting period

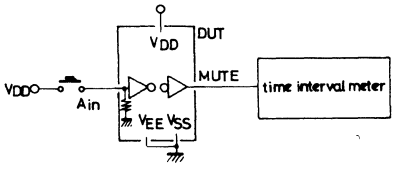
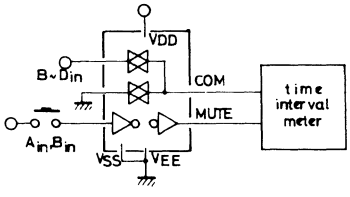
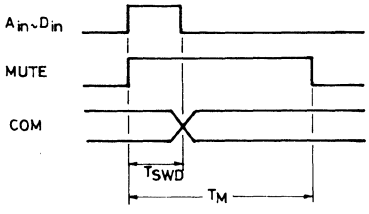


Fig. 5 Switch switchover delay time

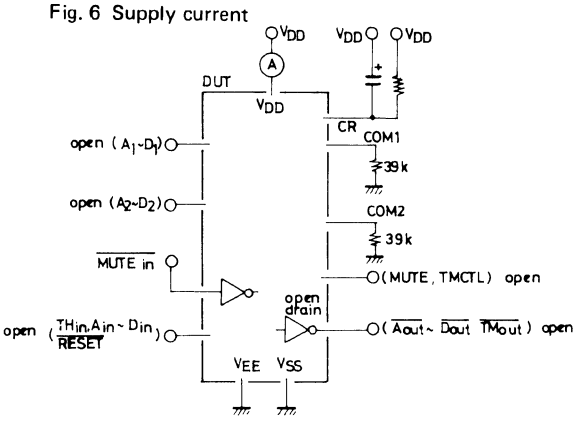


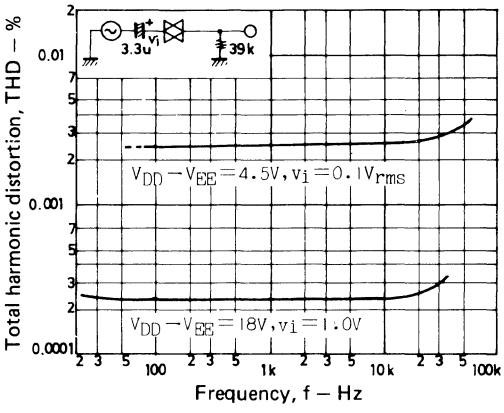


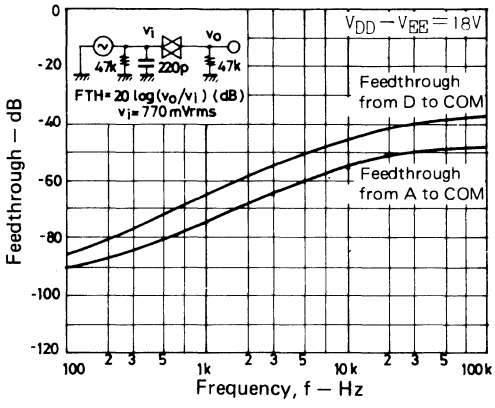
T_M: Muting period

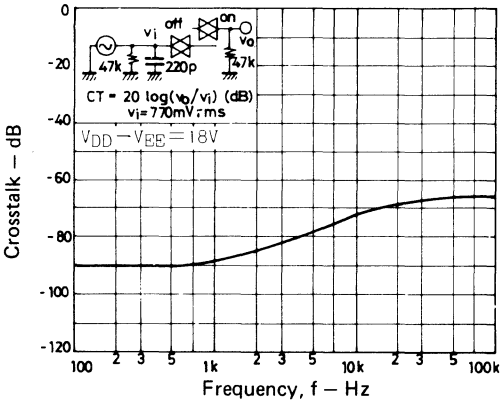
T_{SWD}: Switch switchover delay time

Fig. 6 Supply current

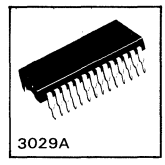








LC7816



C MOS IC

2-Pole 4-Position Analog Function Switch

Ⓔ 1520

The LC7816 is a 2-pole 4-position analog function switch with 2 built-in C-MOS analog switches (LC4966 type). A soft touch of a button enables switchover of the input signal source of an audio amplifier.

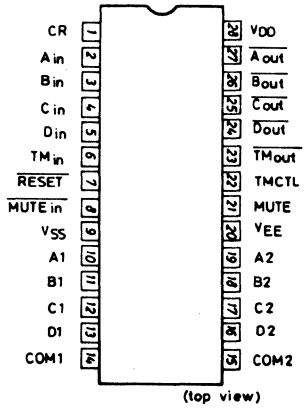
Use :

Function switchover of amplifier, receiver, etc.(2 poles 4 positions)

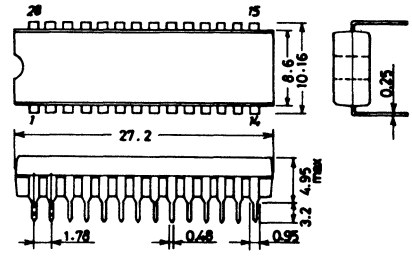
Features :

1. Good distortion characterisitc because of built-in analog switches of LC4966 type : Distortion 0.01% max./Vin=1V_{rms}, V_{DD}-V_{EE}=15 to 37V.
2. Capable of outputting audio muting control signal to minimize noise to be generated at the time of switchover.
3. Built-in controller for tape monitor switchover (using LC4966 together).
4. Built-in driver for LED which displays function mode, tape monitor mode.
5. Since control input can be operated from + supply alone when using dual supplies (+,-), interface with other circuits can be achieved easily.
6. Since audio muting control signal can be triggered independently from external pin ($\overline{MUTEin}$), audio muting at the time of return from backup can be achieved easily.
7. Control input pin ($\overline{RESET}$) to be used for turning OFF all analog switches.
8. Backup can be performed easily because of C MOS structure. (Backup voltage: 3V min.)
9. Operating voltage : ±18V/dual supplies.
10. Package : DIP-28S (Shrink type).

Pin Assignment

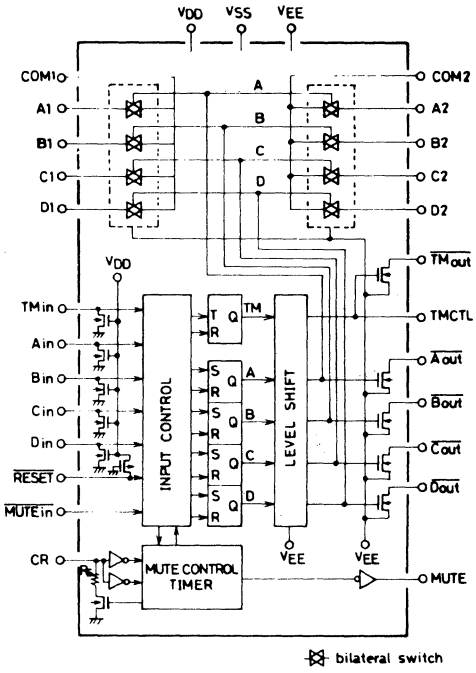


Case Outline 3029A-D28SIC
(unit:mm)



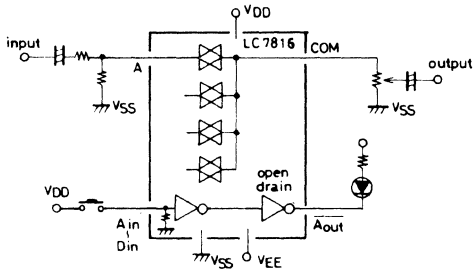
SANYO: DIP28S

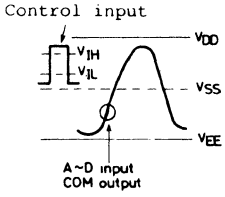
Equivalent Circuit Block Diagram



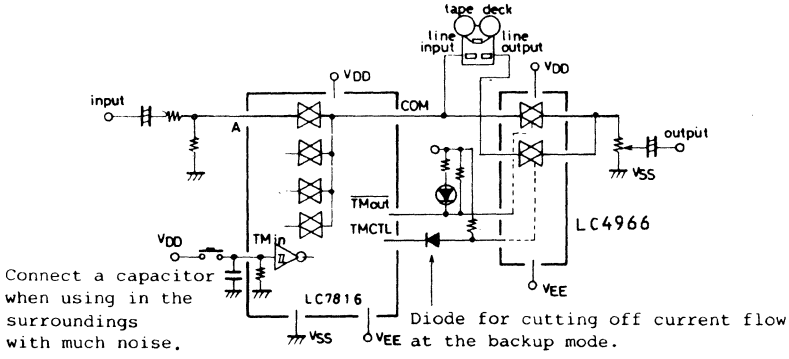
Sample Application Circuits

1. Without tape monitor function

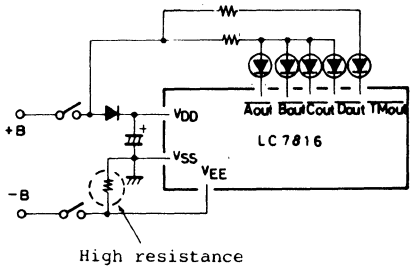




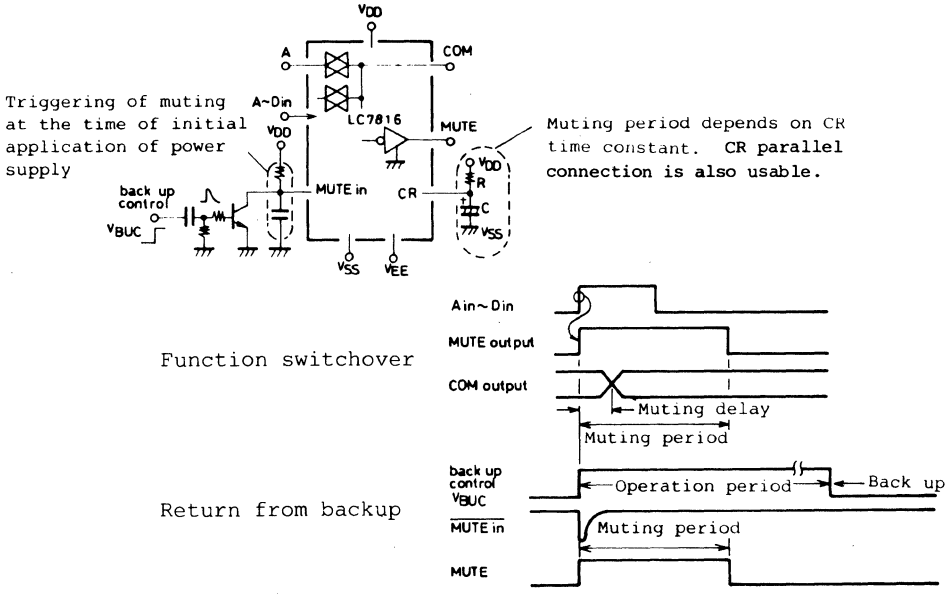
2. With tape monitor function



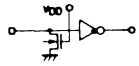
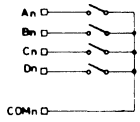
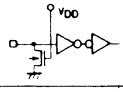
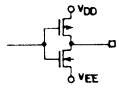
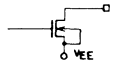
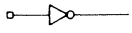
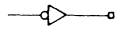
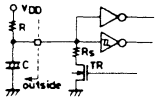
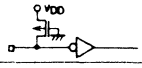
3. Backup



4. Muting



Pin Description

Pin Name	Pin No.	Type of Input/Output	Pin Functions
V_{DD} V_{SS} V_{EE}	28 9 20		·Power supply pins Dual supplies (+-): V_{SS}=GND, V_{EE}=(-)V
Ain,Bin, Cin,Din	2,3, 4,5		**.Input pins for turning ON individual analog** switches ·Priority order of simultaneous push(Ain>Bin>Cin>Din) ·Prevention of malfunction attributable to pulse noise (Pulse width is discriminated by muting delay time.)
Aout Bout Cout Dout	27, 26, 25, 24		·Output of driver for LED which displays ON state corresponding to individual analog switches ·N channel open drain(Source is connected to V_{EE})
A1,B1, C1,D1 A2,B2, C2,D2 COM1 COM2	10,11, 12,13 19,18, 17,16 14 15		·A to D: Audio signal input pins ·COM: Audio signal output pins ·Signal inputs (A to D)conduct according to signal inputs(Ain to Din) as follows: COM output: An Bn Cn Dn Specified input: Ain 1 0 0 0; Bin * 1 0 0; Cin * * 1 0; Din * * * 1 *: Don't care
TMin	6		·Input pin for specifying tape monitor mode ON/OFF ·Rise of input signal is detected; monitor mode ON/OFF are inverted to monitor mode OFF/ON respectively.
TMCTL	22		·Output pin for controlling external analog switch (LC4966) for tape monitor ·Source of N channel transistor of complementary buffer output is connected to V_{EE}.
$\overline{\text{TMout}}$	23		·Output pin for driver for LED which displays tape **monitor state as well as for control of external switch (LC4966) for tape monitor.** ·$\overline{\text{TMout}}$ is opposite in polarity to TMCTL.
$\overline{\text{MUTEin}}$	8		·Input pin for forcing audio muting control signal (MUTE) to be triggered externally ·If fixed at'L' level,MUTE output becomes'H'level.
MUTE	21		·Output pin for audio muting control signal ·Signal with pulse width to be determined by external constant at CR pin is outputted at the time of function switchover or $\overline{\text{MUTEin}}$ input.
CR	1		·CR time constant pin for determining time interval of audio muting control signal ·Time lag(muting delay) between muting signal rise and analog switch switchover depends on C·R_S time constant **at the time of transistor ON. CR parallel connection also usable.**
$\overline{\text{RESET}}$	7		·Input pin for turning OFF all analog switches and resetting tape monitor flip-flop('L' level active)

Absolute Maximum Ratings at Ta=25±2°C

				unit
maximum Supply Voltage	V_{DD} max		V_{SS}-0.3 to V_{EE}+40	V
	V_{EE} max		V_{DD}-40 to V_{SS}+0.3	V
Output Current	I_{OUT}	$\overline{Aout}$,$\overline{Bout}$,$\overline{Cout}$, $\overline{Dout}$,$\overline{TMout}$	30	mA
Output Voltage	V_{OUT}	" "	V_{EE}-0.3 to V_{DD}+0.3	V
Voltage Difference at analog switch ON	ΔV_{on}	Switch ON	0.5	V
Allowable Power Dissipation	Pd max	Ta≦85°C	350	mW
OPerating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Ranges at Ta=-40 to +85°C

		Pin No.	Conditions	min	typ	max	unit
Supply Voltage	V_{DD1}	V_{DD}(28)	V_{EE}≦V_{SS}-4.5	V_{SS}+4.5		V_{EE}+37	V
	V_{EE}	V_{EE}(20)	V_{DD}≧V_{SS}+4.5	V_{DD}-37		V_{SS}-4.5	V
	V_{DD2}	V_{DD}(28)	Backup V_{EE}≦V_{SS}	V_{SS}+3		V_{SS}+37	V
'H' Level Input Voltage	V_{IH1}	Ain(2) to Din(5), $\overline{RESET}$(7),$\overline{MUTE}$ in(8)		0.75V_{DD}		V_{DD}	V
	V_{IH2}	TMin(6)		0.8V_{DD}		V_{DD}	V
'L' Level Input Voltage	V_{IL1}	Ain(2) to Din(5) $\overline{RESET}$(7),$\overline{MUTE}$ in(8)		V_{SS}		0.25V_{DD}	V
	V_{IL2}	TMin(6)		V_{SS}		0.2V_{DD}	V
Analog Switch Input Voltage	V_{IN}	A1(10) to D1(13), A2(19) to D2(16)		V_{EE}		V_{DD}	V
External Capacitance for Muting Timer	C	CR(1)				10	uF
External Resistance for Muting Timer	R	CR(1)	V_{DD}-V_{SS}=4.5V	40		100	kohm
			14V>V_{DD}-V_{SS}≧9V	100		300	kohm
			18V>V_{DD}-V_{SS}≧14V	80		300	kohm
			37V>V_{DD}-V_{SS}≧18V	100		300	kohm
Input Receiving Pulse Width	T_{IN}	Ain(2) to Din(5) TMin(6)	V_{DD}=9V, C=3.3uF,R=220kohm	120			ms

Electrical Characteristics at Ta=25±2°C,V_{SS}=0V

		Pin NO.	Conditions	min	typ	max	unit
'H' Level Output Voltage	V_{OH1}	$TMCT_L$(22)	IOH=-0.1mA VDD=4.5 to 37V	0.8V_{DD}		V_{DD}	V
	V_{OH2}	MUTE(21)	IOH=-0.4mA,V_{DD}=4.5V	V_{DD}-1.5		V_{DD}	V
			" ,V_{DD}=9V	V_{DD}-0.5		V_{DD}	V
'L' Level Output Voltage	V_{OL1}	TMCTL(22)	I_{OL}=0.1mA	V_{EE}		0.2x (V_{DD}-V_{EE})	V
	V_{OL2}	MUTE(21)	I_{OL}=0.4mA,V_{DD}=4.5V	0		1.5	V
			" ,V_{DD}≧9V	0		0.5	V
	V_{OL3}	$\overline{AOUT}$(27),$\overline{DOUT}$(24) $\overline{TMOUT}$(23)	I_{OL}=7mA,V_{DD}-V_{EE}=4.5V	V_{EE}		V_{EE}+2	V
			I_{OL}=30mA,V_{DD}-V_{EE}=9V	V_{EE}		V_{EE}+4	V
			" ,V_{DD}-V_{EE}=18V	V_{EE}		V_{EE}+2	V
Analog Switch ON Resistance	Ron	A1(10),B1(11) C1(12),D1(13) COM1(14) A2(19),B2(18) C2(17),D2(16), COM2(15)	I=1mA,V_{DD}-V_{EE}=4.5V		400		ohm
			" ,V_{DD}-V_{EE}=9V		120		ohm
			" ,V_{DD}-V_{EE}=18V		80		ohm
			" ,V_{DD}-V_{EE}=37V		70		ohm

				min	typ	max	unit
Input/Output OFF Leak Current	I_{OFF1}	$\overline{AOUT}$(27) to $\overline{DOUT}$(24) $\overline{TMOUT}$(23)	Output transistor OFF $V_O=V_{EE}+18V$			10	uA
			Output transistor OFF $V_O=V_{EE}+37V$			20	uA
	I_{OFF2}	CR(1)	Output transistor OFF $V_O=V_{SS}+18V$			3	uA
	I_{OFF3}	A1(10) to D1(13), COM1(14), A2(19) to D2(16), COM2(15)	Analog switch OFF $V_{IN}=V_O=V_{EE}$ to $V_{EE}+38V$	-10		10	uA
Total Harmonic Distortion	THD1	COM1(14),COM2(15)	V_{IN}=1Vrms,f=1KHz, $V_{DD}-V_{EE}$=15 to 37V, Refer to Fig.1.		0.01		%
	THD2	" "	V_{IN}=0.1Vrms,f=1KHz, $V_{DD}-V_{EE}$=4.5V, Refer to Fig.1.		0.05		%
Feedthrough (Switch OFF)	FTH	A1(10), D1(13) to COM1(14); A2(19), D2(16) to COM2(15)	$V_{DD}-V_{EE}$=37V,f=10KHz, V_{IN}=0.77Vrms, Refer to Fig.2. RL=47kohm		55		dB
Crosstalk	CT	A1(10), D1(13) to COM2(15); A2(19), D2(16) to COM1(14)	$V_{DD}-V_{EE}$=37V,f=10KHz, V_{IN}=0.77Vrms, Refer to Fig.3. RL=47kohm		75		dB
Muting Time	TM1	MUTE(21)	V_{DD}=9V, Refer to Fig.4. C=3.3uF±20%, R=220kohm±5%	350	580	1000	ms
	TM2	MUTE(21)	V_{DD}=9V, C=3.3uF±0%, R=220kohm±0%	450	580	800	ms
Switch Switchover Delay Time	T_{SWD}	Ain(2) to Din(5) TMin(6)	V_{DD}=9V, Refer to Fig.5. C=3.3uF,R=220kohm	30	50	120	ms
Supply Current	I_{DD1}	V_{DD}(28)	Operating, Refer to Fig.6. $V_{DD}-V_{EE}$=18V			1000	uA
Input Floating Voltage	V_{IF}(1)	Ain(2) to Din(5) TMin(6)	V_{DD}=4.5 to 37V	V_{SS}		0.75	V
	V_{IF}(2)	RESET(7)	V_{DD}=4.5 to 37V	V_{DD}-0.75		V_{DD}	V

Fig. 1 Toatl harmonic distortion

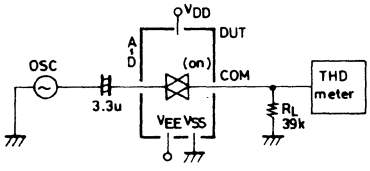
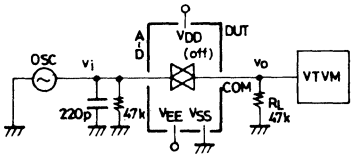


Fig. 2 Feedthrough

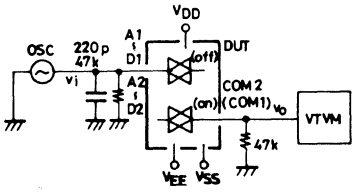


$$FTH=20 \log \frac{V_o}{V_i} (dB)$$

V_i=770mVrms

$V_{DD}-V_{EE}$=38V

Fig. 3 Crosstalk



$CT = 20 \log \frac{Vo}{Vi}$ (dB)

Vi=770mVrms

VDD-VEE=38V

Fig. 4 Muting period

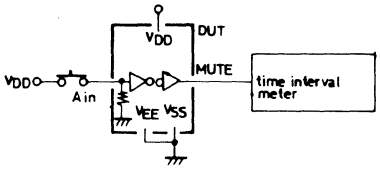
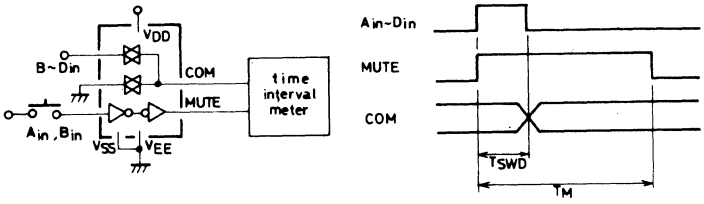
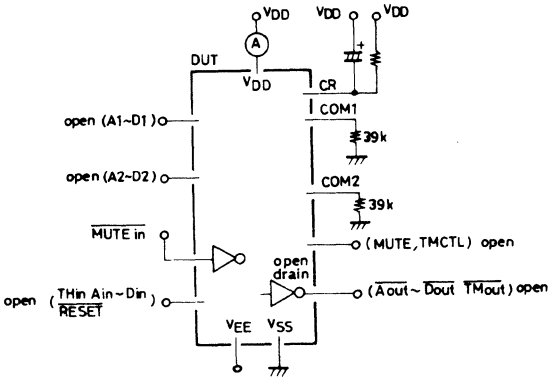


Fig. 5 Switch switchover delay time

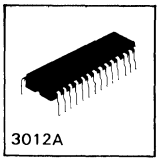


TM: Muting period
TSWD: Switch switchover delay time

Fig. 6 Supply current



LC7817



C MOS IC

2-Pole 4-Position Analog Function Switch

Ⓔ 1359A

The LC7817 is a 2-pole 4-position analog function switch with 2 built-in C-MOS analog switches (LC4066 type). A soft touch of a button enables switchover of the input signal source of an audio amplifier.

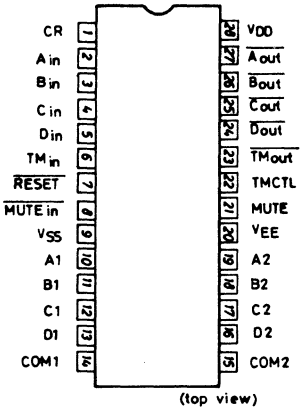
Use:

Function switchover of amplifier, receiver, etc.(2 poles 4 positions)

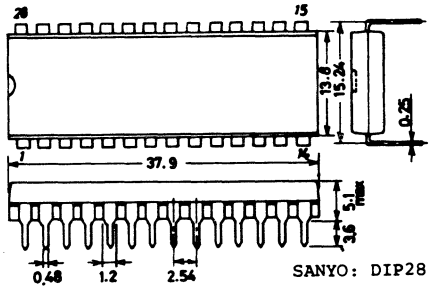
Features:

1. Good distortion characteristic because of built-in analog switches of LC4066 type: Distortion 0.01% max./V_{in}=1V_{rms}, V_{DD}=15 to 37V
2. Capable of outputting audio muting control signal to minimize noise to be generated at the time of switchover
3. Built-in controller for tape monitor switchover (using LC4966 together)
4. Built-in driver for LED which displays function mode, tape monitor mode
5. Since control input can be operated from + supply alone when using dual supplies (+,-), interface with other circuits can be achieved easily.
6. Since audio muting control signal can be triggered independently from external pin ($\overline{MUTE_{in}}$), audio muting at the time of return from backup can be achieved easily.
7. Control input pin ($\overline{RESET}$) to be used for turning OFF all analog switches
8. Backup can be performed easily because of C-MOS structure.(Backup voltage: 3V min.)
9. Operating voltage: 18V/dual supplies
10. Package: DIP-28

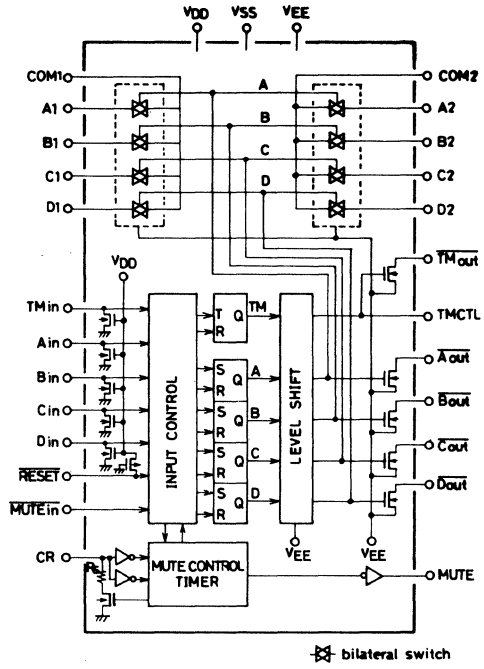
Pin Assignment



Case Outline 3012A-D28IC
(unit:mm)

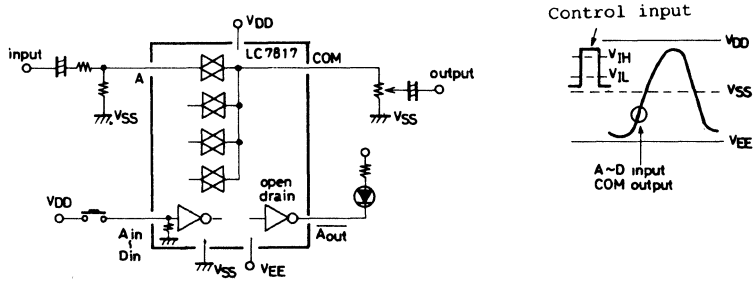


Equivalent Circuit Block Diagram

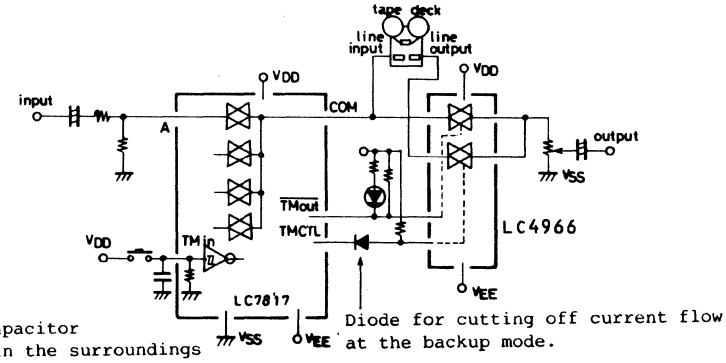


Sample Application Circuits

1. Dual-supply operation/without tape monitor function

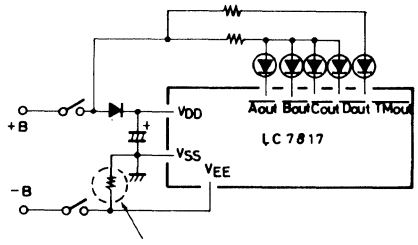


2. Dual-supply operation/with tape monitor function



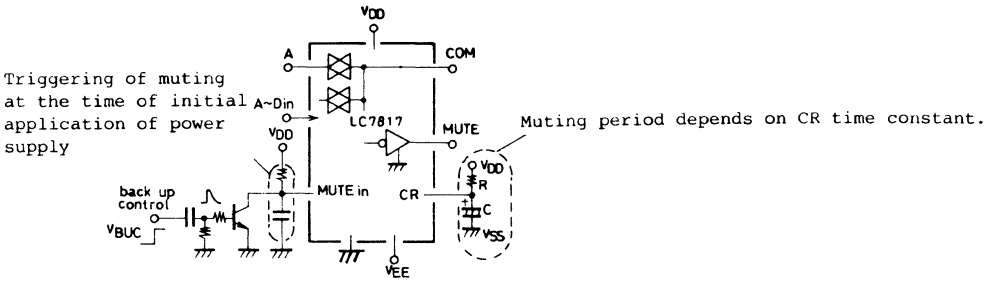
3. Backup

Dual-supply operation



High resistance

4. Muting

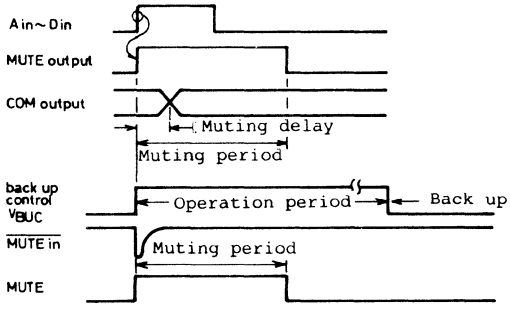


Triggering of muting at the time of initial application of power supply

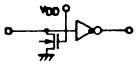
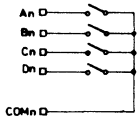
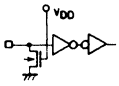
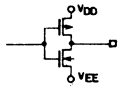
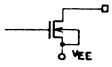
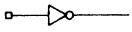
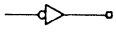
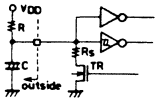
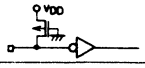
Muting period depends on CR time constant.

Function switchover

Return from backup



Pin Description

Pin Name	Pin No.	Type of Input/Output	Pin Functions
VDD VSS VEE	28 9 20		·Power supply pins Single supply (+): VSS=VEE=GND Dual supplies (+-): VSS=GND, VEE=(-)V
Ain,Bin, Cin,Din	2,3, 4,5		·Specified input pins for turning ON individual analog switches ·Priority order of simultaneous push(Ain Bin Cin Din) ·Prevention of malfunction attributable to pulse noise (Pulse width is discriminated by muting delay time.)
$\overline{Aout}$ $\overline{Bout}$ $\overline{Cout}$ $\overline{Dout}$	27, 26, 25, 24		·Output of driver for LED which displays ON state corresponding to individual analog switches ·N channel open drain(Source is connected to VEE)
A1,B1, C1,D1 A2,B2, C2,D2 COM1 COM2	10,11, 12,13 19,18, 17,16 14 15		·A to D: Audio signal input pins ·COM: Audio signal output pins ·Signal inputs (A to D)conduct according to signal inputs(Ain to Din) as follows: COM output: Specified input — Ain: An 1, Bn 0, Cn 0, Dn 0; Bin: An *, Bn 1, Cn 0, Dn 0; Cin: An *, Bn *, Cn 1, Dn 0; Din: An *, Bn *, Cn *, Dn 1 *: Don't care
TMin	6		·Input pin for specifying tape monitor mode ON/OFF ·Rise of input signal is detected; monitor mode ON/OFF are inverted to monitor mode OFF/ON respectively.
TMCTL	22		·Output pin for controlling external analog switch (LC4966) for tape monitor ·Source of N channel transistor of complementary buffer output is connected to VEE.
$\overline{TMout}$	23		·Output pin for driver for LED which displays tape monitor state as well as external analog switch (LC4966) for tape monitor ·$\overline{TMout}$ is opposite in polarity to TMCTL.
$\overline{MUTEin}$	8		·Input pin for forcing audio muting control signal (MUTE) to be triggered externally ·If fixed at'L' level,MUTE output becomes'H'level.
MUTE	21		·Output pin for audio muting control signal ·Signal with pulse width to be determined by external constant at CR pin is outputted at the time of function switchover or $\overline{MUTEin}$ input.
CR	1		·CR time constant pin for determining time interval of audio muting control signal ·Time lag(muting delay) between muting signal rise and analog switch switchover depends on C·RS time constant at the time of transistor ON.
$\overline{RESET}$	7		·Input pin for turning OFF all analog switches and resetting tape monitor flip-flop('L' level active)

Absolute Maximum Ratings at Ta=25±2°C

				unit
maximum Supply Voltage	V_{DD} max		V_{SS}-0.3 to V_{EE}+40	V
	V_{EE} max		V_{DD}-40 to V_{SS}+0.3	V
Output Current	I_{OUT}	$\overline{Aout}$, $\overline{Bout}$, $\overline{Cout}$, $\overline{Dout}$, $\overline{TMout}$	30	mA
Output Voltage	V_{OUT}	" "	V_{EE}-0.3 to V_{DD}+0.3	V
Voltage Difference at analog switch ON	ΔV_{on}	Switch ON	-0.5 to 0.5	V
Allowable Power Dissipation	Pd max	Ta≦85°C	350	mW
OPerating Temperature	T_{opg}		-40 to +85	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Ranges at Ta=-40 to +85°C

		Pin No.	Conditions	min	typ	max	unit
Supply Voltage	V_{DD1}	V_{DD}(28)	V_{EE}≦V_{SS}-4.5	V_{SS}+4.5		V_{EE}+37	V
	V_{EE}	V_{EE}(20)	V_{DD}≧V_{SS}+4.5	V_{DD}-37		V_{SS}-4.5	V
	V_{DD2}	V_{DD}(28)	Backup V_{EE}≦V_{SS}	V_{SS}+3		V_{SS}+37	V
'H' Level Input Voltage	V_{IH1}	Ain(2) to Din(5), $\overline{RESET}$(7), $\overline{MUTE}$ in(8)		0.75V_{DD}		V_{DD}	V
	V_{IH2}	TMin(6)		0.8V_{DD}		V_{DD}	V
'L' Level Input Voltage	V_{IL1}	Ain(2) to Din(5) $\overline{RESET}$(7), $\overline{MUTE}$ in(8)		V_{SS}		0.25V_{DD}	V
	V_{IL2}	TMin(6)		V_{SS}		0.2V_{DD}	V
Analog Switch Input Voltage	V_{IN}	A1(10) to D1(13), A2(19) to D2(16)		V_{EE}		V_{DD}	V
External Capacitance for Muting Timer	C	CR(1)				10	uF
External Resistance for Muting Timer	R	CR(1)	V_{DD}-V_{SS}=4.5V	40		100	Kohm
			V_{DD}-V_{SS}≧9V	100		300	Kohm
Input Receiving Pulse Width	T_{IN}	Ain(2) to Din(5) TMin(6)	V_{DD}=9V, C=3.3uF, R=220Kohm	120			ms

Electrical Characteristics at Ta=25±2°C, V_{SS}=0V

		Pin NO.	Conditions	min	typ	max	unit
'H' Level Output Voltage	V_{OH1}	TMCTL(22)	IOH=-0.1mA, VDD=4.5 to 37V	0.8V_{DD}		V_{DD}	V
	V_{OH2}	MUTE(21)	IOH=-0.4mA, V_{DD}=4.5V	V_{DD}-1.5		V_{DD}	V
			" , V_{DD}≧9V	V_{DD}-0.5		V_{DD}	V
'L' Level Output Voltage	V_{OL1}	TMCTL(22)	IOL=0.1mA	V_{EE}	0.2x (V_{DD}-V_{EE})		V
	V_{OL2}	MUTE(21)	IOL=0.4mA, V_{DD}=4.5V	0		1.5	V
			" , V_{DD}=9V	0		0.5	V
	V_{OL3}	$\overline{AOUT}$(27), $\overline{DOUT}$(24) $\overline{TMOUT}$(23)	IOL=7mA, V_{DD}-V_{EE}=4.5V	V_{EE}		V_{EE}+2	V
			IOL=30mA, V_{DD}-V_{EE}=9V	V_{EE}		V_{EE}+4	V
			" , V_{DD}-V_{EE}≧18V	V_{EE}		V_{EE}+2	V
Analog Switch ON Resistance	R_{on}	A1(10), B1(11) C1(12), D1(13) COM1(14) A2(19), B2(18) C2(17), D2(16) COM2(15)	I=1mA, V_{DD}-V_{EE}=4.5V		400		ohm
			" , V_{DD}-V_{EE}=9V		120		ohm
			" , V_{DD}-V_{EE}≧18V		80		ohm

				min	typ	max	unit
Input/Output OFF Leak Current	I_{OFF1}	$\overline{AOUT}$(27) to $\overline{DOUT}$(24) $\overline{TMOUT}$(23)	Output transistor OFF $V_O=V_{EE}+37V$			10	uA
	I_{OFF2}	CR(1)	Output transistor OFF $V_O=V_{SS}+18V$			3	uA
	I_{OFF3}	A1(10) to D1(13), COM1(14), A2(19) to D2(16), COM2(15)	Analog switch OFF $V_{IN}=V_O=V_{EE}$ $V_{EE}+37V$	-10		10	uA
Total Harmonic Distortion	THD1	COM1(14),COM2(15)	V_{IN}=1Vrms,f=1KHz, $V_{DD}-V_{EE}$=15 to 37V, Refer to Fig.1.		0.01		%
	THD2	" "	V_{IN}=0.1Vrms,f=1KHz, $V_{DD}-V_{EE}$=4.5V, Refer to Fig.1.		0.05		%
Feedthrough (Switch OFF)	FTH	A1(10), D1(13) → to COM1(14); A2(19), D2(16) → to COM2(15)	$V_{DD}-V_{EE}$=37V,f=10KHz, V_{IN}=0.77Vrms, Refer to Fig.2. RL=47Kohm		55		dB
Crosstalk	CT	A1(10), D1(13) → to COM2(15); A2(19), D2(16) → to COM1(14)	$V_{DD}-V_{EE}$=37V,f=10KHz, V_{IN}=0.77Vrms, Refer to Fig.3. RL=47Kohm		75		dB
Muting Time	TM1	MUTE(21)	V_{DD}=9, Refer to Fig.4. C=3.3uF±20%, R=220Kohm±5%	350	580	1000	ms
	TM2	MUTE(21)	V_{DD}=9V, C=3.3uF±0%, R=220Kohm±0%	450	580	800	ms
Switch Switchover Delay Time	T_{SWD}	Ain(2) to Din(5) TMin(6)	V_{DD}=9V, Refer to Fig.5. C=3.3uF,R=220Kohm	30	50	120	ms
Supply Current	I_{DD1}	V_{DD}(28)	Operating, Refer to Fig.6. $V_{DD}-V_{EE}$=37V			1000	uA

Fig. 1 Toatl harmonic distortion

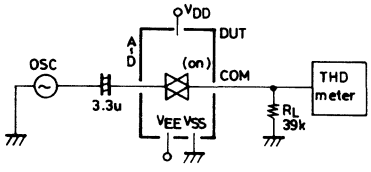
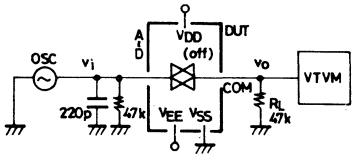


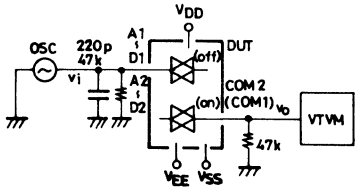
Fig. 2 Feedthrough



$$FTH=20 \log \frac{V_o}{V_i} (dB)$$

Vi=770mVrms
VDD-VEE=37V

Fig. 3 Crosstalk



$$CT=20 \log \frac{V_o}{V_i} (dB)$$

Vi=770mVrms
VDD-VEE=37V

Fig. 4 Muting period

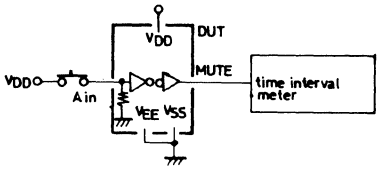
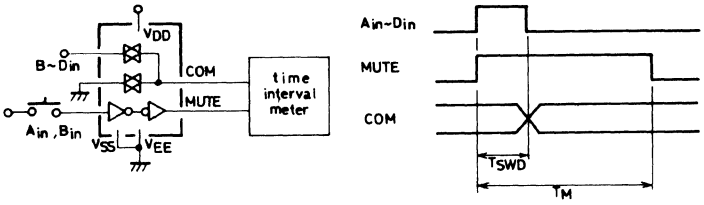
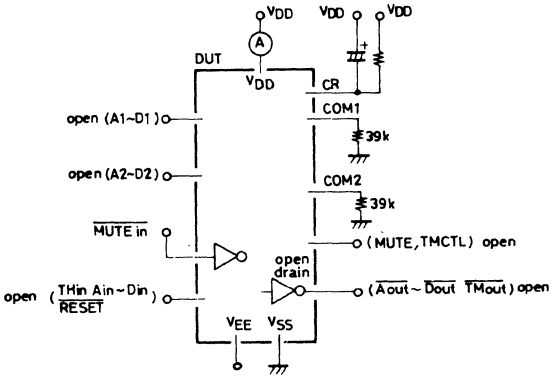


Fig. 5 Switch switchover delay time

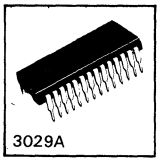


TM: Muting period
TSWD: Switch switchover delay time

Fig. 6 Supply current



LC7820



C MOS IC

2-Pole 4-Position Function Switch

Ⓔ 1514

TENTATIVE

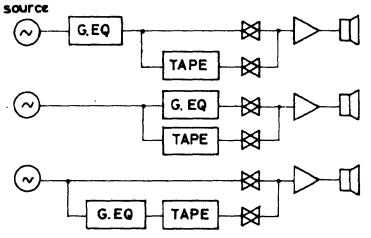
Functions

- 2-pole 4-position function switch of feather touch type
- Tape monitor function, REC equalization (graphic equalizer input/output) function
- Microcomputer-controlled. 2 control lines. Microcomputer-applied mute output and mode display.

Features

(1) Tape monitor with one touch

(2) With a graphic equalizer connected to the REC equalization pins, the following 3 configurations of equalizer connection are available with one touch.

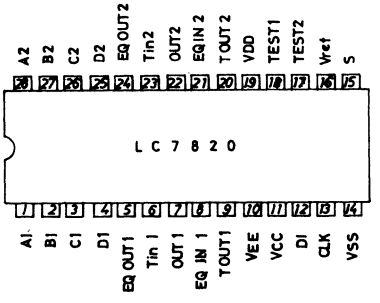


(3) The use of 2 IC's makes it possible to add the functions shown below.
  (1) Dubbing A→B, B→A (A→B: With REC equalization function)
  (2) REC OUT selector (On-the-air program, off-the-air program)

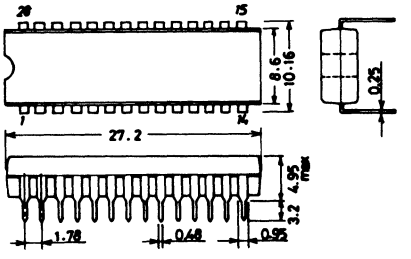
(4) Wide dynamic range due to 40V breakdown voltage

(5) Two control lines can be used in common with other IC (graphic equalizer LC7520).

Case Outline and Pin Assignment

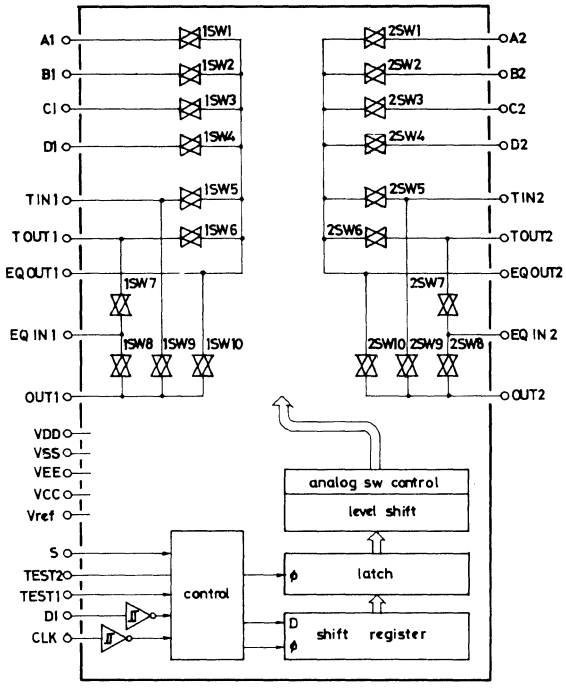


Case Outline 3029A-D28SIC
(unit:mm)



SANYO: DIP28S

Equivalent Circuit Block Diagram

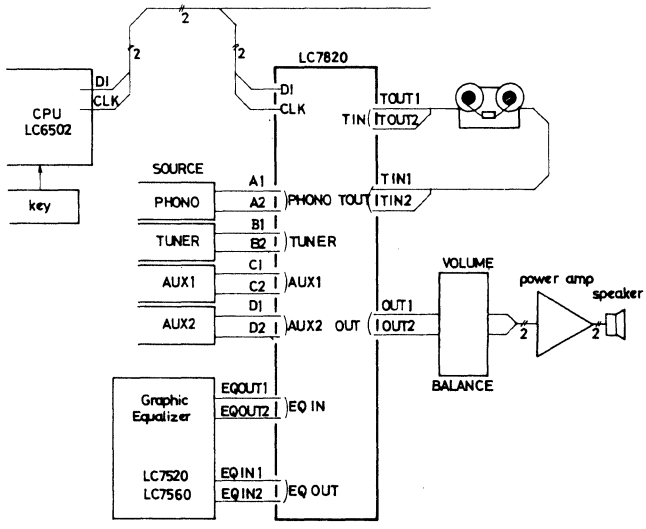


Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V				unit
Maximum Supply Voltage	V_{DD}	$V_{EE} \leq V_{SS}$	$V_{DD}-V_{EE} \leq 40$	V
	V_{EE}		"	V
	V_{CC}		V_{SS} to $V_{SS}+7.0$	V
	V_{ref}	$V_{SS} \leq Vref$	$V_{DD}-Vref \leq 11.0$	V
Input Voltage	V_{I1}	CLK,DI	$V_{SS}-0.3$ to $V_{CC}+0.3$	V
	V_{I2}	A1 to D1,A2 to D2, Tin1,2 EQin1,2	$V_{EE}-0.3$ to $V_{DD}+0.3$	V
Analog SW ON-state Voltage Difference	$\Delta V1$	Between analog SW input and output (ON)	0.6	V
Analog SW OFF-state Voltage Difference	$\Delta V2$	Between analog SW input and output (OFF)	$V_{DD}-V_{EE}$	V
Allowable Power Dissipation	Pdmax	Ta≦75°C	100	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

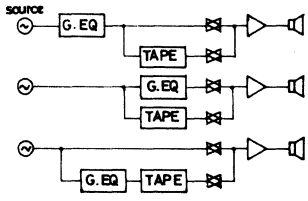
Allowable Operating Ranges at Ta=25°C, V_{SS}=0V				unit
Supply Voltage	V_{DD}	$V_{EE} \leq V_{SS}$, $V_{CC} < DD$	$8 \leq V_{DD}-V_{EE} \leq 37$	V
	V_{EE}	"	"	V
	V_{CC}	"	4.5to(typ5.0)to5.5	V
	Vref	$V_{DD}-Vref \leq 10$	0 to $V_{DD}-4.5$	V
"H" Input Voltage	$V_{IH(1)}$	CLK,DI	$0.8V_{CC}$ to V_{CC}	V
	$V_{IH(2)}$	S	$Vref+0.9(V_{DD}-Vref)$toV_{DD}	V
"L" Input Voltage	$V_{IL(1)}$	CLK,DI	V_{SS} to $0.2V_{CC}$	V
	$V_{IL(2)}$	S	$Vref$to$Vref+0.1(V_{DD}-Vref)$	V
Input Pulse Width	tøw	CLK	min 1	V
Setup Time	t_{setup}	CLK,DI	min 1	V
Hold Time	t_{hold}	CLK,DI	min 1	V
Operating Frequency	fopg	CLK	330	kHz
Analog SW Input Voltage	V_{IN}	A1 to D1,A2 to D2 Tin1,2,EQin1,2	V_{EE} to V_{DD}	V

Electrical Characteristics			min	typ	max	unit
Current Dissipation	I_{DD}				1	mA
	Iref				1	mA
	I_{CC}				1	mA
Analog SW ON-State Resistance	Ron	$I=1mA, V_{DD}-V_{EE}=18V$		80	200	ohm
		$I=1mA, V_{DD}-V_{EE}=23V$		70	180	ohm
		$I=1mA, V_{DD}-V_{EE}=37V$		60	140	ohm
Input/Output OFF-State Leak Current	I_{off}	Analog SW OFF $V_{IN}=Vo=V_{EE}$ to 18V	-10		10	uA
Total Harmonic Distortion	THD1	$V_{IN}=1Vrms, f=1kHz, V_{DD}-V_{EE}=37V$			0.01	%
	THD2	$V_{IN}=0.1Vrms, f=1kHz, V_{DD}-V_{EE}=37V$			0.05	%
Feedthrough (SW OFF-State)	FTH	$V_{DD}-V_{EE}=37V, f=10kHz$ Vin=0dBm, R_L=47kohm		-55		dB
Crosstalk	CT	$V_{DD}-V_{EE}=37V, f=10kHz$ Vin=0dBm, R_L=47kohm		-75		dB

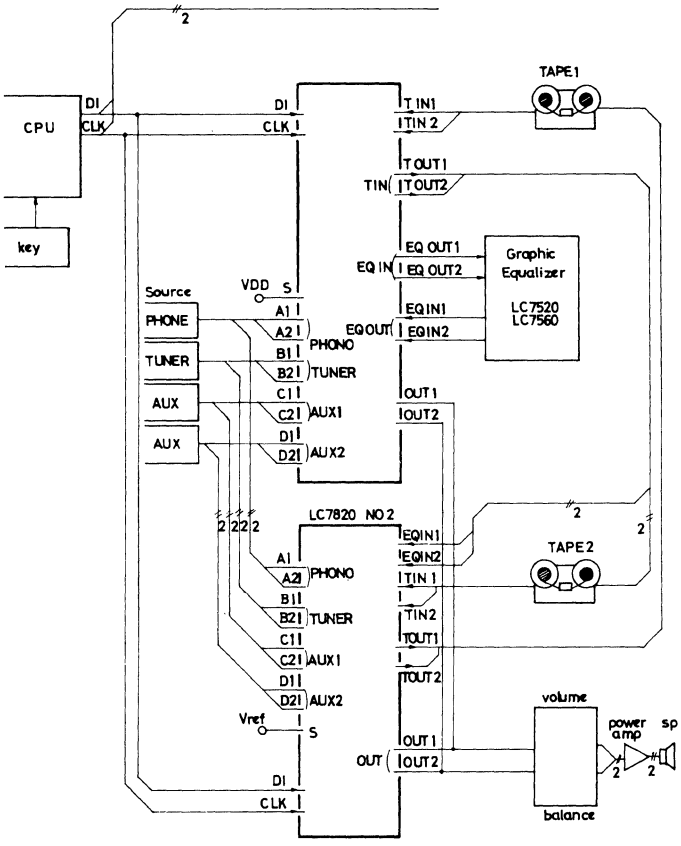
Sample Application Circuit 1 : General Function



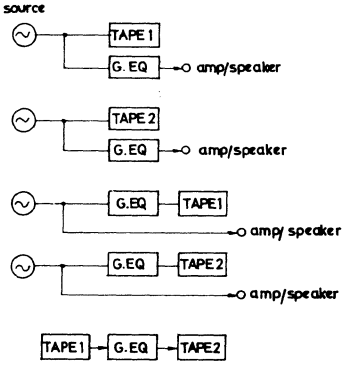
Function (1) 4 inputs (+tape input) 1 selection
(2) Equalizer ON/OFF
(3) Tape monitor ON/OFF
(4) 3 configurations of equalizer connection



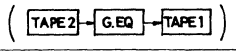
Sample Application Circuit 2 : REC OUT Selector, Dubbing Function (Using 2 IC's)



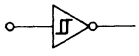
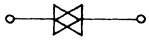
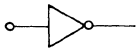
Function (1) 4 inputs (+tape 1,2 input) 1 selection
(2) Equalizer ON/OFF
(3) Tape monitor ON/OFF
} Functions in 1-chip application
(4) REC OUT selector (On-the-air program, off-the-air program)
(5) Dubbing 1→2, dubbing 2→1
(Graphic equalizer connection:1 direction)
(6) 5 confugurations of equalizer connection



The following configuration is unrecommendable.

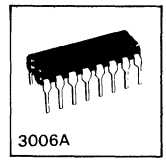


Pin Description

Pin Name	Pin No.	Pin Configuration	Description
V_{DD}	19		Power supply pin, +18V typ., For sound signal.
Vref	16		Power supply pin, V_{DD}-5V typ., For driving internal logic.
V_{SS}	14		Power supply pin, 0V
V_{EE}	10		Power supply pin, -18V typ., For sound signal.
V_{CC}	11		Power supply pin, +5V typ., For input logic
DI	12		. Pin for inputting data from CPU . Schmitt inverter type
CLK	13		. Pin for inputting clock from CPU . Schmitt inverter type
A1,2 B1,2 C1,2 D1,2 Tin1,2 EQin1,2	1,28 2,27 3,26 4,25 6,23 8,21	1,2SWn  A1,2 Tout1,2 B1,2 EQout1,2 C1,2 OUT1,2 D1,2	Sound signal input pin. 1SWn,2SWn: Simultaneous operation.
OUT1,2 Tout1,2 EQout1,2	7,22 9,20 5,24		Sound signal output pin.
S	15		Select pin for using 2 IC's S: 0 → Key code 7D2 S: 1 → Key code 7D3

(Note) The manuals for microcomputer, control data, timing are in preparation.

LC7910



C MOS IC

A/D, D/A Converter

Ⓔ 1335A

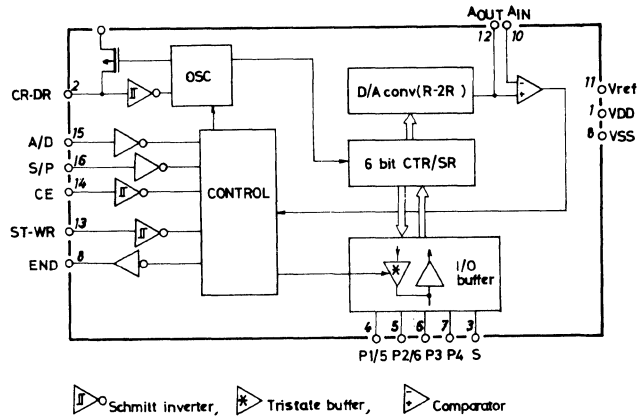
Use:

6-bit 64-step A/D, D/A converter that is applied to control various types of equipment by making serial or parallel transfer of data to and from 4-bit CPU.

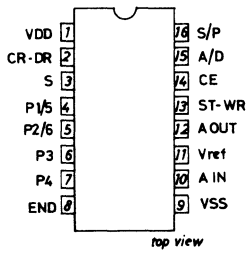
Features:

(1) A/D or D/A conversion function
(2) Serial or parallel data output/input
(3) Single 5V power supply
(4) 6-bit 64-step resolution
(5) Tri-state is available for data output pins according to input on CE pin.

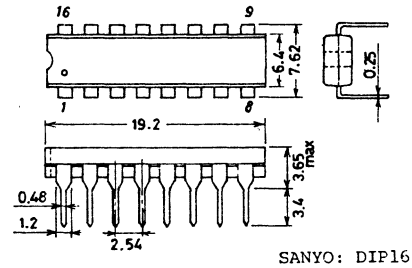
Equivalent Circuit Block Diagram



Pin Assignment



Case outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Absolute Maximum Ratings at Ta=25±2°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DDmax}		-0.3 to +8.0	V
	V_{refmax}	$V_{refmax} \leqq V_{DDmax}$	-0.3 to +8.0	V
Maximum Input Voltage	V_{IN}	A_{IN}	V_{SS} to V_{ref}	V
Maximum Output Voltage	V_{OUT1}	A_{OUT}	V_{SS} to V_{ref}	V
	V_{OUT2}	CR-DR,END,P1/5~4,S	V_{SS} to V_{DD}	V
Maximum Output Current	I_{OUT}	END,P1/5~4,S	-4.0 to +4.0	mA
Maximum Allowable Power Dissipation	P_{dmax}	Ta≦75°C	100	mW
Operating Temperature	T_{opg}		-30 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Ranges at Ta=25±2°C, V_{SS}=0V

				unit
Supply Voltage	V_{DD}		4.5 to 5.5	V
	V_{ref}	$V_{ref} \leqq V_{DD}$	4.5 to V_{DD}	V
Input 'H' Level Voltage	V_{IH1}	A/D,S/P,CE,ST-WR, P1/5~4, (D/A mode)	0.75V_{DD} to V_{DD}	V
	V_{IH2}	CR-DR(D/A mode)	0.85V_{DD} to V_{DD}	V
Input 'L' Level Voltage	V_{IL1}	A/D,S/P,CE,ST-WR, P1/5~4,S(D/A mode)	V_{SS} to 0.25V_{DD}	V
	V_{IL2}	CR-DR(D/A mode)	V_{SS} to 0.25V_{DD}	V
External Resistance	R_{osc}	CR-DR at 5V C=0.01uF(J,K)	6.8 to 100	Kohm

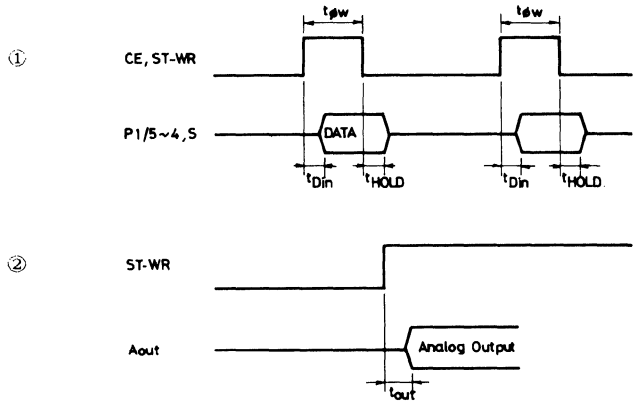
Electrical Characteristics(1) at Ta=25±2°C, V_{SS}=0V

			min	typ	max	unit
Input Pulse Width	$t_{\emptyset w}$	CE,ST-WR	10			us
Data Hold Time	t_{HOLD}	P1/5~4,S(after CE='0')	10			us
Data Input Time	t_{DIN}	P1/5~4,S(after CE='1')	1			us
Output Settling Time	t_{OUT}	A_{OUT}			10	us
Output Active Time	t_{ON}	P1/5~4,S(after CE='1')			10	us
Output Inactive Time	t_{OFF}	P1/5~4,S(after CE='0')			10	us
Output 'H' Level Voltage	V_{OH}	P1/5~4,S,END,I_{OH}=-2mA	0.8V_{DD}		V_{DD}	V
Output 'L' Level Voltage	V_{OL}	" I_{OL}=+2mA	V_{SS}		0.2V_{DD}	V
Output Off Leakage Current	I_{OFF}	P1/5~4,S, CE='0'	-10		10	uA
Input Current	I_{IN1}	A/D,S/P,ST-WR,$V_{SS} \leqq V_{IN} \leqq V_{DD}$	-10		10	uA
	I_{IN2}	A_{IN} $V_{SS} \leqq V_{IN} \leqq V_{ref}$	-10		10	uA
	I_{IN3}	CE $V_{SS} \leqq V_{IN} \leqq V_{DD}$	-10		10	uA
Output impedance	R_{AOUT}	A_{OUT}		10		Kohm
Current Dissipation	I_{DD}	V_{DD} V_{DD}=4.5~5.5V			1	mA
	I_{ref}	V_{ref} V_{DD}=V_{ref}=4.5~5.5V			1	mA
Maximum Conversion Time	t_{conv}	V_{DD}=V_{ref}=V_{in}=4.5~5.5V R_{OSC}=3.3Kohm			3	msec

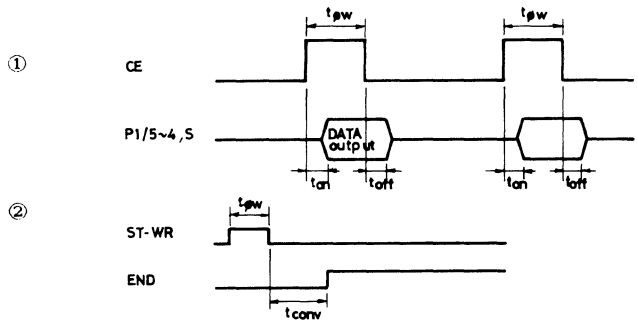
Electrical Characteristics (2) at Ta=25±2°C, V_{DD}=Vref=5V

		min	typ	max	unit
A/D	Resolution		6		bit
	Quantize accuracy	-1/2		+1/2	LSB
	Relative accuracy	-1		+1	LSB
	Offset error	0		2	LSB
D/A	Resolution		6		bit
	Linearity	-1/2		+1/2	LSB

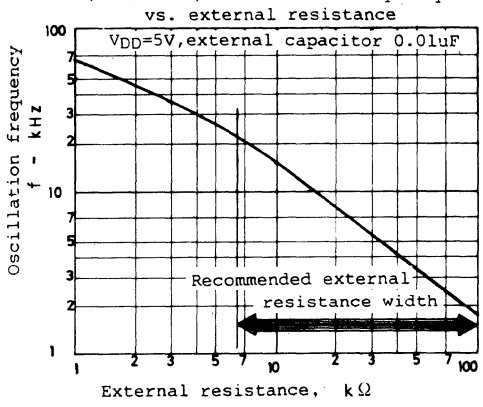
D/A mode



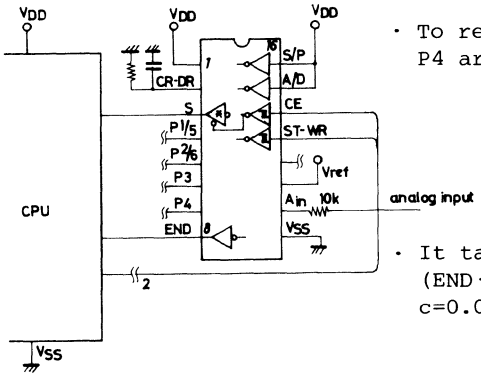
A/D mode



(Reference) Oscillation frequency vs. external resistance

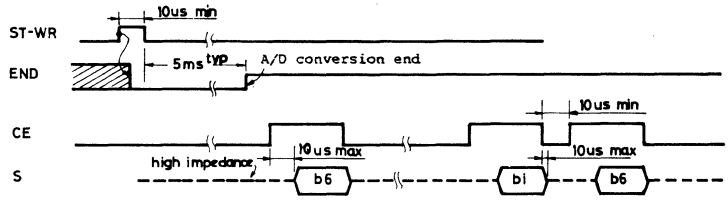


Sample Application (1) A/D converter (Serial output)



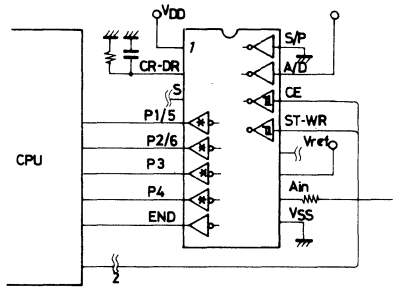
- To reduce current dissipation, P1/5 to P4 are connected to GND/VDD.
- It takes 5ms before conversion ends (END ← 1) at fOSC=13KHz (R=13Kohm, c=0.01uF).

A/D conversion timing (At 5V, f_{OSC}=13KHz)



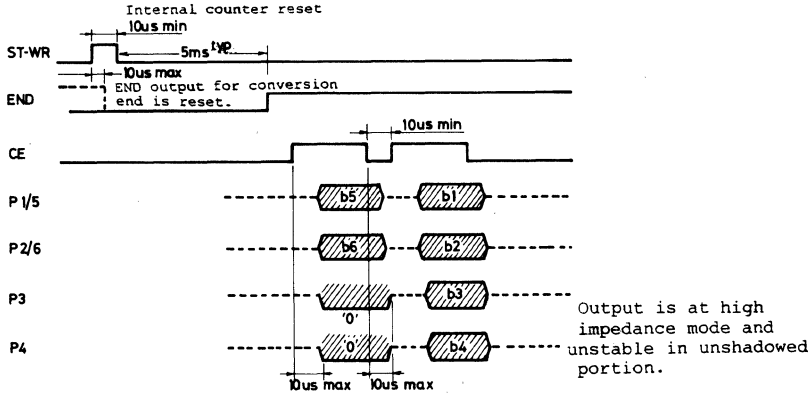
Output data can be strobed 10us after output active CE rise.
b6 is delivered at first CE after END becomes '1'; then b5,b4, ---,b1 are delivered in succession.
b6 is delivered at next CE, and data is delivered endlessly.
(Note 1) If S/P or A/D is changed-over during output transfer, correct data cannot be held.

Sample Application Circuit (2) A/D converter (Parallel output)

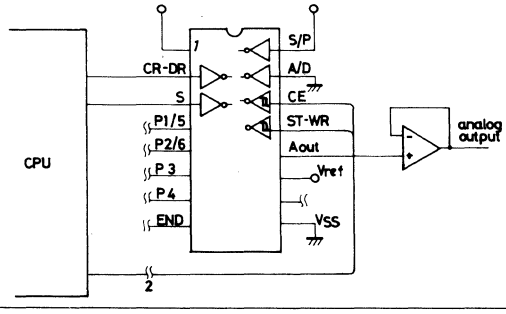


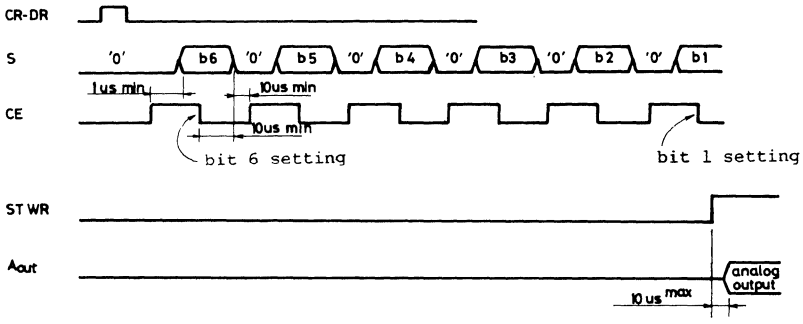
- To reduce current dissipation, S pin is connected to VDD/GND

Conversion timing (At 5V, f_{OSC}=13KHz)

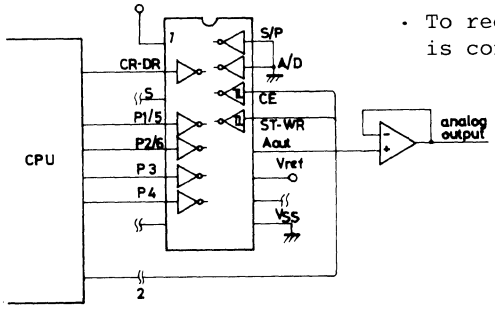


Sample Application Circuit (3) D/A converter (Serial output)



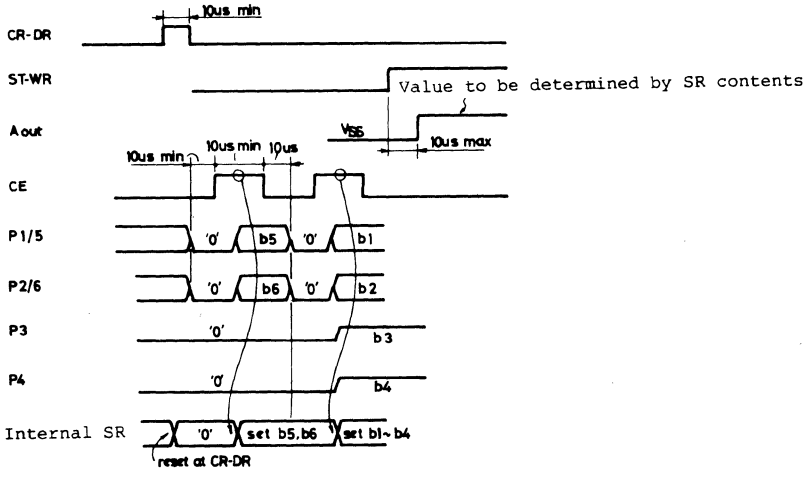


Sample Application Circuit (4) D/A converter (Parallel output)



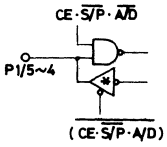
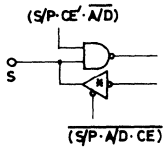
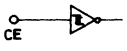
- To reduce current dissipation, S pin is connected to VDD/GND.

Conversion timing



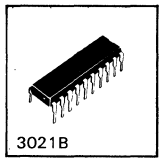
- Note 1: P1/5, P2/6 data must be inputted 1us after CE rise immediately following CR-DR. At this moment P3, P4 must be at '0'.
- Note 2: Data on P pin must be held for at least 10us after CE becomes '0'.
- Note 3: A_{OUT} is delayed 10us max. after ST-WR becomes '1'.

Pin Description

Pin Name	Pin No.	Pin Configuration	Pin Description
P1/5 P2/6 P3 P4	4 5 6 7		1) Output pin at A/D conversion and parallel output mode(A/D pin→'1') When CE is at '1',A/D conversion output is obtained. When CE is at '0'.high impedance mode is entered. Output data (After '1'is delivered at END) 1st CE: P1/5 b5, P2/6 b6, P3 '0', P4 '0' 2nd CE: P1/5 b1, P2/6 b2, P3 b3, P4 b4 3rd CE: P1/5 b5, P2/6 b6, P3 '0', P4 '0' Repeated thereafter '0':'L' level For $A_{IN} \equiv V_{ref}$, 111111=(b6 b5 b4----b1); for $A_{IN} \equiv V_{SS}$, 000000=(b6 b5-----b1) 2) Parallel input pin at D/A conversion mode (A/D pin→'0') Internal shift register fetches data synchronously with CE rise. Data must be inputted 1us after CE rise. Input data (After applying '1' to CR-DR) 1st CE: P1/5 b5, P2/6 b6, P3 '0', P4 '0' 2nd CE: P1/5 b1, P2/6 b2, P3 b3, P4 b4 (note) Since data is set to each bit by OR input, data cannot be set 2 times or more.
S	3		1) Output pin at A/D conversion and serial output mode (A/D pin→'1') When CE is at '1', A/D conversion output is obtained. When CE is at '0', high impedance mode is entered. Output data 1st CE: S b6 2nd CE: S b5 3rd CE: S b4 4th CE: S b3 5th CE: S b2 6th CE: S b1 7th CE: S b6 .... 2) Input pin at D/A conversion serial (input) mode (A/D pin→'0') Pin for loading data into shift register by use of CE signal. Input data 1st CE: S b6 2nd CE: S b5 3rd CE: S b4 4th CE: S b3 5th CE: S b2 6th CE: S b1 (Note) If CE is set to '1' 7 times or more, data of each bit may be destroyed.
ST-WR	13		Schmitt inverter type input pin. No pull-up,pull-down. 1) A/D mode Input pin for resetting internal counter. When ST-WR is at '1',counter is reset; when ST-SR falls, A/D conversion starts. 2) D/A mode Shift register contents are D/A-converted to determine A_{OUT} output timing. If ST-WR is at '0', A_{OUT} outputs V_{SS}.
CE	14		Schmitt inverter type input pin No pull-up,pull-down. 1) A/D mode Each time CE is applied after A/D conversion end (END='1'),A/D conversion data is obtained from P1/5 to P4 or S. 2) D/A mode Control pin for loading data into shift reister.

Pin Name	Pin No.	Pin Configuration	Pin Description
END	8	END	When oscillation stops after A/D conversion ends at A/D conversion mode, '1' is delivered at END pin. END output is reset by ST-WR input and delivers'0' until A/D conversion ends again.
CR-DR	2	CR-DR	1) A/D mode: Open drain type output buffer Oscillation circuit: CR are connected externally. Conversion time: Within 64 times oscillation cycle (T_{osc}) $T_{conv} \leq T_{osc} \times 64$ 2) D/A mode: Schmitt inverter. No pull-up,pull-down. Input pin for applying shift register reset signal at D/A conversion mode. Shift register is reset by '1' input.
VSS	9		Power supply: Biased into most negative potential
S/P	16	S/P	Serial mode/parallel mode selection: '1': serial, '0': parallel. At A/D mode, no selection is allowed until data is read completely after conversion end. At D/A mode, no selection is allowed until data is inputted completely.
A/D	15	A/D	Selection of A/D conversion mode or D/A conversion mode. A/D='1': A/D mode A/D='0': D/A mode
VDD	1		Power supply
Vref	11		$V_{ref} \leq V_{DD}$. 1) Reference voltage at A/D conversion mode For $A_{IN} \geq V_{ref}$, A/D conversion output is (1,1,----,1). For $A_{IN}=0$, A/D conversion output is (0,0,----,0). 2) Reference voltage at D/A conversion mode.
AIN	10		Pin for applying A/D conversion input Allowable applied voltage: $V_{SS} = A_{IN} = V_{ref}$
AOUT	12	Aout R-2R ladder	D/A conversion output Output impedance: 10kohm typ. Output: $V_{SS} \leq V_{OUT} \leq V_{ref}$

LM7000



N MOS LSI

Direct PLL Electronic Tuning System

Ⓔ 1434A

TENTATIVE

Features

(1) High-speed programmable divider capable of direct dividing FM band VCO.
(2) Reference frequency (7 kinds).
100, 50, 25, 10, 9, 5, 1 kHz
(3) Output for band select (3 bits).
(4) Clock output for controller (400kHz).
(5) Time base output for watch (8Hz).
(6) Data input : Serial input (CE, CL, DATA pin).
(7) IF Count Circuit.
FM: ±10kHz MW,SW: ±3kHz LW: ±0.6kHz

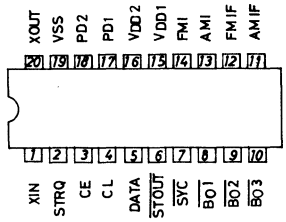
Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$	V_{DD1},V_{DD2}	-0.3 to +8.0	V
Input Voltage	$V_{IN(1)}$	CE,CL,DATA,STRQ	-0.3 to +8.0	V
	$V_{IN(2)}$	Input pins other than $V_{IN(1)}$	-0.3 to V_{DD}+0.3	V
Output Voltage	$V_{OUT(1)}$	$\overline{SYC}$,$\overline{STOUT}$	-0.3 to +8.0	V
	$V_{OUT(2)}$	$\overline{BO1}$,$\overline{BO2}$,$\overline{BO3}$	-0.3 to +15	V
	$V_{OUT(3)}$	Output pins other than $V_{OUT(1)}$,$V_{OUT(2)}$.	-0.3 to V_{DD}+0.3	V
Operating Temperature	Topg		-40 to +85	°C
Storage Temperature	Tstg		-50 to +125	°C

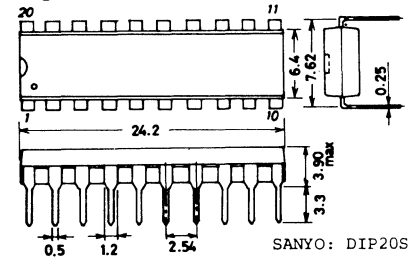
Allowable Operating Ranges at Ta=-40 to +85°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	$V_{DD(1)}$	V_{DD}1:PLL operation	4.5		6.0	V
	$V_{DD(2)}$	V_{DD}2:X'tal OSC time base	3.5		6.0	V
Input "H" Level Voltage	V_{IH}	CE,CL,DATA,STRQ	2.2		6.0	V
Input "L" Level Voltage	V_{IL}	CE,CL,DATA,STRQ	0		0.7	V
Output Voltage	$V_{OUT(1)}$	$\overline{SYC}$,$\overline{STOUT}$	0		6.5	V
	$V_{OUT(2)}$	$\overline{BO1}$,$\overline{BO2}$,$\overline{BO3}$	0		13	V

Pin Assignment



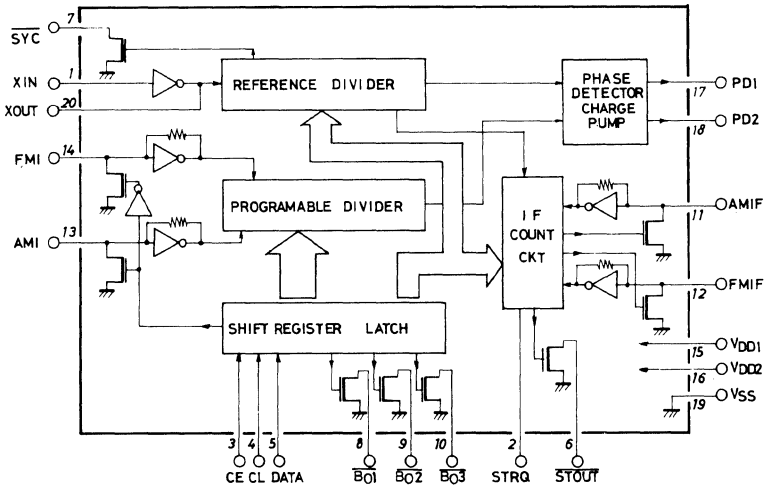
Case Outline 3021B-D20SIC
(unit:mm)



SANYO: DIP20S

			min	typ	max	unit
Input Frequency	$f_{IN(1)}$	XIN:Sine wave,capacitive coupling	1.0	7.2	8.0	MHz
	$f_{IN(2)}$	FMIN: "	5.0		130	MHz
	$f_{IN(3)}$	AMIN: "	0.5		10.0	MHz
	$f_{IN(4)}$	FMIF: "	10.0	10.7	11.5	MHz
	$f_{IN(5)}$	AMIF: "	400	450	500	kHz
Oscillation-Guaranteed Crystal Resonator	X'tal	XIN-XOUT:CI≦40ohm	5.0	7.2	8.0	MHz
Input Amplitude	$V_{IN(1)}$	XIN:Sine wave,capacitive coupling	0.5		1.5	Vrms
	$V_{IN(2)}$	FMIN: "	0.1		1.5	Vrms
	$V_{IN(3)}$	AMIN: "	0.1		1.5	Vrms
	$V_{IN(4)}$	FMIF: "	0.1		1.5	Vrms
	$V_{IN(5)}$	AMIF: "	0.1		1.5	Vrms
External Feedback Resistance	Rf	XIN-XOUT		500		kohm

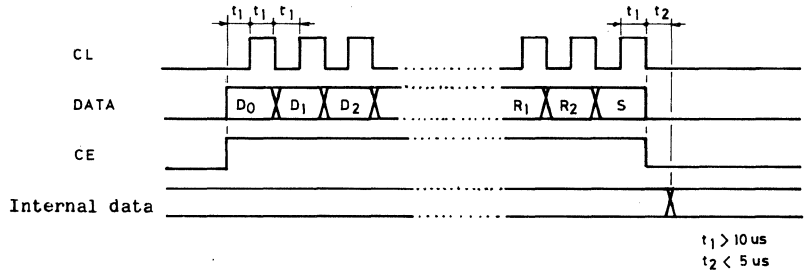
Equivalent Circuit Block Diagram



Pin Description

SYC	: Controller clock (400kHz)
XIN,XOUT	: X'tal OSC (7.2MHz), external feedback resistor
FMI,AMI	: Local oscillation signal input
CE,CL,DATA	: Data input
$\overline{BO1}$,$\overline{BO2}$,$\overline{BO3}$	: Band data output, $\overline{BO1}$ can be also used for time base output (8Hz).
$\overline{STRQ}$	: IF count request input
$\overline{STOUT}$	: Auto search stop signal output
V_{DD1},V_{DD2},V_{SS}	: Power supply (V_{DD2} is for backup.)
AMIF,FMIF	: IF signal input
PD1,PD2	: Charge pump output

Data input



← Inputting starts at D0.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	T0	T1	B0	B1	B2	TB	R0	R1	R2	S

1) D0(LSB) to D13(MSB) : Frequency divisions data
For FMI, use D0 to D13; for AMI, use D4 to D13.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13

1 0 1 0 0 0 0 0 0 1 0 1 1 1 → FMI frequency divisions = 14853
LSB MSB

× × × × 0 0 0 0 0 1 0 1 1 1 → AMI frequency divisions = 928
LSB MSB

2) T0,T1: For LSI test (0, 0)
3) B0 to B2,TB : Band data
Time base data

Input				Output		
B0	B1	B2	TB	$\overline{B01}$	$\overline{B02}$	$\overline{B03}$
0	0	0	0	*	*	*
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	*	*
×	1	0	1	TB	1	0
×	0	1	1	TB	0	1
×	1	1	1	TB	1	1

* : Determined by R0 to R2.
X : don't care.
TB : 8Hz.

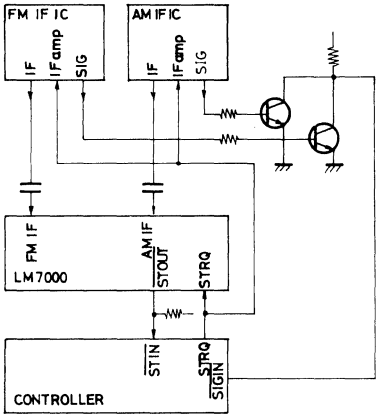
4) R0 to R2 : Reference frequency data

R0	R1	R2	fref	$\overline{B01}$	$\overline{B02}$	$\overline{B03}$	IF Count
0	0	0	100 kHz	1	1	0	10.7 MHz±10 kHz
0	0	1	50	1	1	0	
0	1	0	25	1	1	0	
0	1	1	5	0	0	1	450 kHz±3 kHz
1	0	0	10	1	0	1	
1	0	1	9	1	0	1	
1	1	0	1	0	1	1	450 kHz±0.6 kHz
1	1	1	5	0	0	1	450 kHz±3 kHz

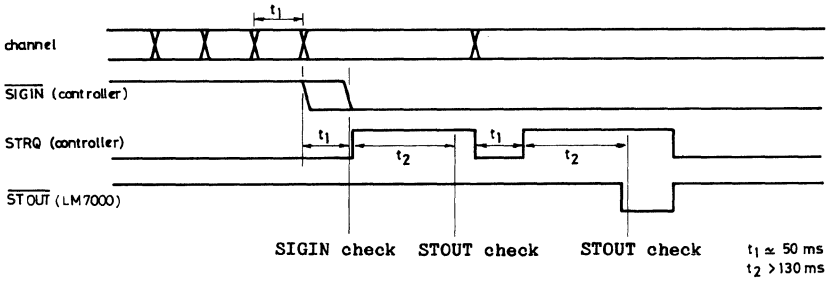
(Note) B0 to B2 = 0

5) S : Divider select data
1 : FMI, 0 : AMI

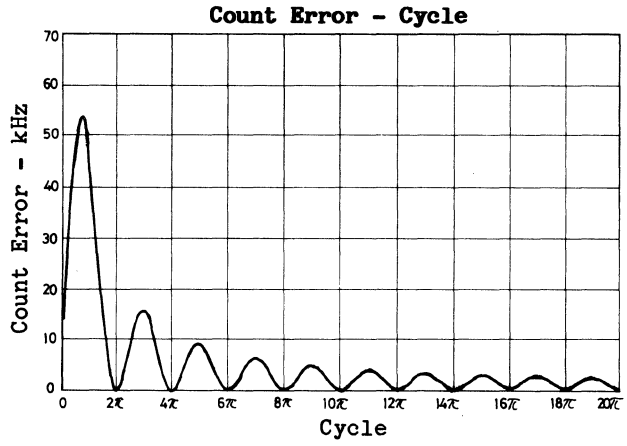
IF count circuit : Circuit to stop auto tuning



- When in the neighborhood of a broadcasting station, "SIG" signal is outputted, setting $\overline{\text{SIGIN}}$ of the controller to "0".
- "STRQ" signal is applied to the LM7000 and IF IC from the controller.
- IF signal is applied to the LM7000 from the IF IC and the LM7000 counts this signal.
- When the specified count value is reached, "$\overline{\text{STOUT}}$" signal is applied to the controller from the LM7000, stopping auto tuning.

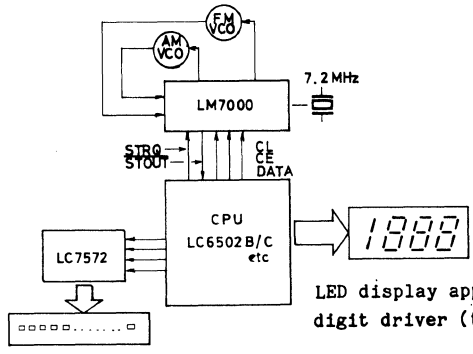


- Counting is performed only at "STRQ"=1.
- The count time is 120msec.
- For FM, the count error is as shown on next page.
  (Example : For 50Hz 100% modulation, the maximum count error is 5kHz.)



Sample Connection to Controller

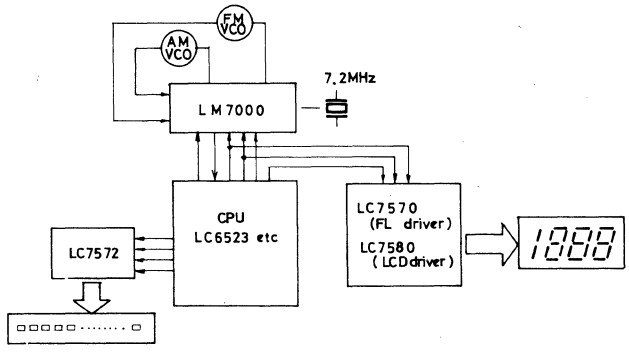
1) FL dynamic display, LED dynamic display applications



LED display application require segment, digit driver (transistor).

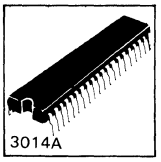
Preset address display (LED)

2) FL static display, LCD display applications



Preset address display (LED)

LM8523



P MOS LSI

Counter for Tape Recorder

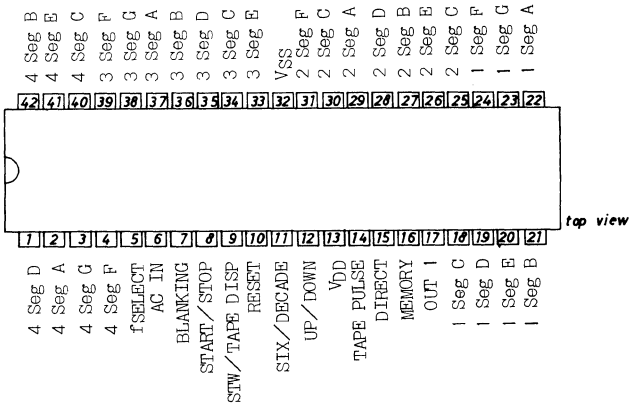
Ⓔ 788A

Use : Tape counter of tape recorder, tape deck, VTR, etc.

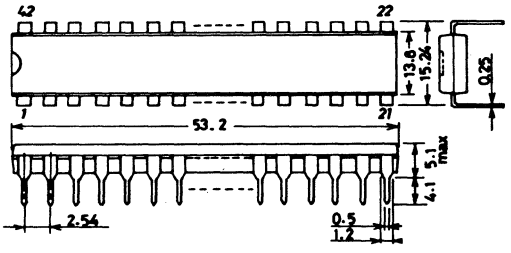
Function : Count and its display, stopwatch.

Features :

1. 1-chip P-channel E/D MOS LSI.
2. Possible to direct drive LED (more than 5mA, cathode common).
3. Possible to direct drive fluorescent display tube (ON voltage : less than 16V) : LM8523H.
4. Wide operating voltage range : -8.5 to -16V.
5. 50Hz or 60Hz available for reference frequency.
6. Blanking pin for blanking display (possible to connect in parallel with other LSI of P-channel open drain output type).
7. TAPEPULSE input part contains 5u sec. chattering preventive circuit.
8. Stopwatch counter countable up to 59 minutes 59 seconds is built in.
9. The moment counter counts down to 0, control pulse is outputted (counter zero stop function).
10. When memory pin is set at 'H', counter content at this moment is memorized, and when counter content coincides with memory, control pulse is outputted (memory stop function).
11. Predivider to divide tape pulse into 1/5 or 1/1 is built in.



Case Outline 3014A-D42IC
(unit:mm)



SANYO: DIP42

Absolute Maximum Ratings at T_a=25°C, V_{SS}=0V

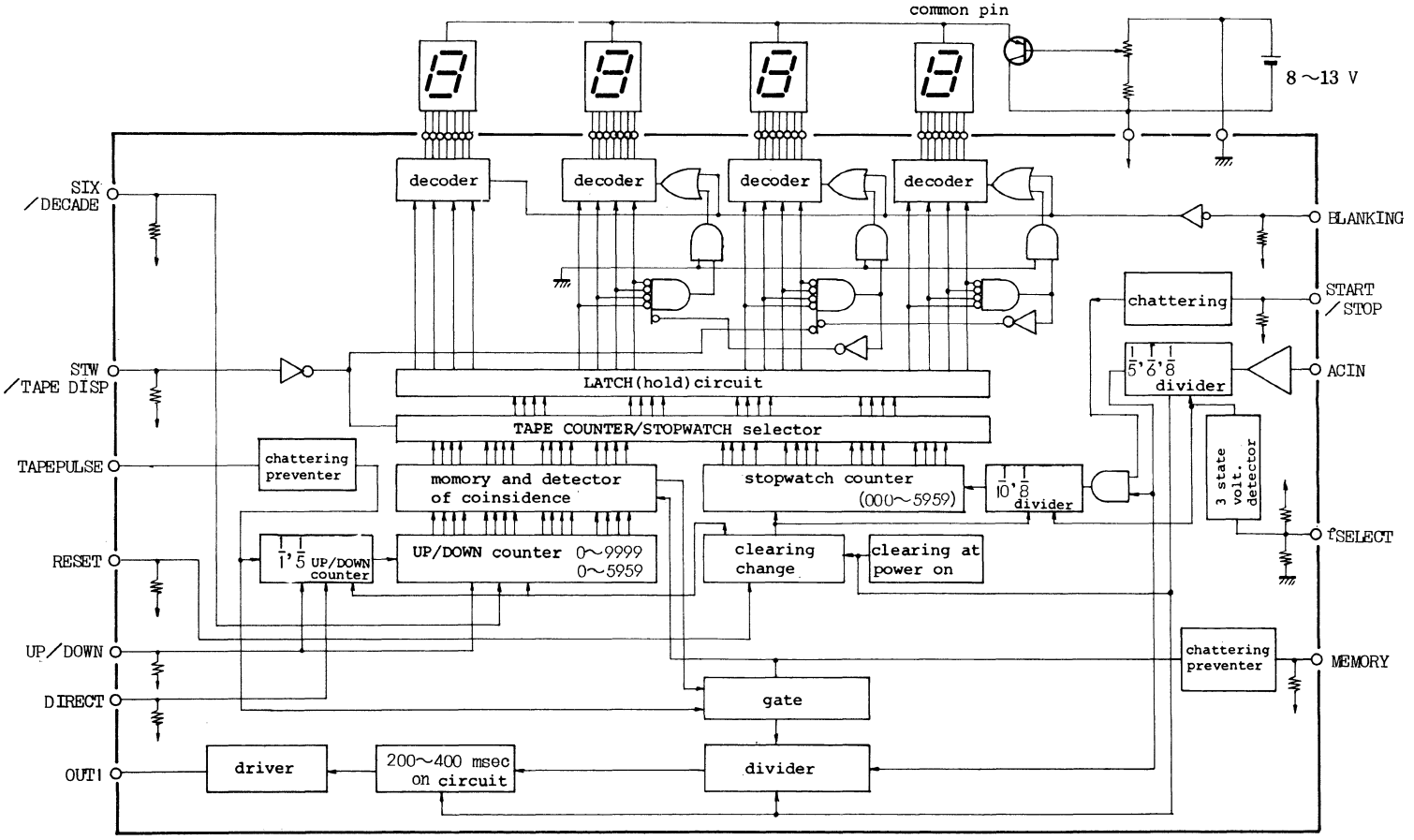
Max. Supply Voltage	$V_{DD}max$		-18 to +0.3	V
Max. Input Voltage	$V_{IN}max$		V_{DD}-0.3 to +0.3	V
Max. Output Voltage	$V_{OUT}max$	Output off	V_{DD}-0.3 to +0.3	V
Allowable Power Dissipation	P_dmax	$T_a \leqq 60°C$	800	mW
		$T_a \leqq 60°C$, Segment output	20	mW
		$T_a \leqq 60°C$, OUT 1	70	mW
Operating Temperature	T_{opg}		-30 to +60	°C
Storage Temperature	T_{stg}	All pins open	-55 to +125	°C

Allowable Operation Condition at T_a=25°C, V_{SS}=0V

Supply Voltage	V_{DD}		-16.0 to -8.5	V
Input'H' Level Voltage	V_{IH}		-8.0	V or more
Input'L' Level Voltage	$V_{IL(1)}$	ACIN, TAPEPULSE	V_{DD}+1.5	V or less
	$V_{IL(2)}$	f_{SELECT}, RESET, BLANKING	V_{DD}+0.8	V or less
	$V_{IL(3)}$	Other than above	V_{DD}+2.0	V or less
Input Frequency	f_{IN}	TAPEPULSE, ACIN, START/STOP, duty cycle 50%	DC to 5k	Hz
V_{DD} Fall Time	t_f	Condition for initial clear	500	msec or less

Electrical Characteristics at T_a=25°C, V_{SS}=0V, V_{DD}=-8.5 to -14.5V

			min	typ	max	unit
Input'H' Level Current	$\|I_{IH(1)}\|$	TAPEPULSE, ACIN, $V_{IN}=V_{SS}$			5	uA
Input'L' Level Current	$\|I_{IH(2)}\|$	f_{SELECT}, $V_{IN}=V_{SS}$	10		350	uA
	$\|I_{IH(3)}\|$	Other than above, $V_{IN}=V_{SS}$	15		350	uA
Input'L' Level Current	$\|I_{IL(1)}\|$	TAPEPULSE, ACIN, $V_{IN}=V_{DD}$			5	uA
	$\|I_{IL(2)}\|$	f_{SELECT}, $V_{IN}=V_{DD}$	10		350	uA
Input Floating Voltage	V_{If}	Input pins excluding TAPEPULSE, ACIN, f_{SELECT}			V_{DD}+0.6	V
Hysteresis Voltage Width	V_{hysw}	ACIN		1.0		V
Output'H' Level Current	$\|I_{OH(1)}\|$	Segment output, V_{DD}=-8.5V, V_{OH}=-2.5V	5			mA
	$\|I_{OH(2)}\|$	OUT 1, V_{DD}=-8.5V, V_{OH}=-6V	9.5			mA
Output Leak Current	$\|I_{OFF(1)}\|$	Segment output, $V_{OL}=V_{DD}$			20	uA
	$\|I_{OFF(2)}\|$	OUT 1, $V_{OL}=V_{DD}$			20	uA
Current Dissipation				20		mA



Equialent Circuit Block Diagram of LM8523

1. Display

1. Count contents and cumulative time are displayed in the following display font by use of 4-digit, 7-segment LED or fluorescent tube.
2. Display Font : 1 2 3 4 5 6 7 8 9 0
3. Lighting System : Static lighting
4. Display Range : Either of the following is selectable with input pin (STW/TAPE DISP).
   - For counter
     0 to 9999 (high-order digit:0 blanking)
     or
     0 to 5959 (high-order digit:0 blanking)
   - For stopwatch
     000 to 5959 (most significant digit only:0 blanking)

2. Input Signal

1. Switch Signal
   Logical "L" --- V_{DD}
   Logical "H" --- V_{SS}
2. TAPEPULSE Input Signal
   - Input signal of V_{SS}-$V_{DD(p-p)}$ sinusoidal wave, square wave.
   - Chattering reject time : 5 usec. min.
3. 50/60 Hz Input Signal
   - V_{SS}-$V_{DD(p-p)}$ sinusoidal wave, square wave.

3. Output System

- Segment output,OUT 1 P-ch open drain system.

4. Description of Pins

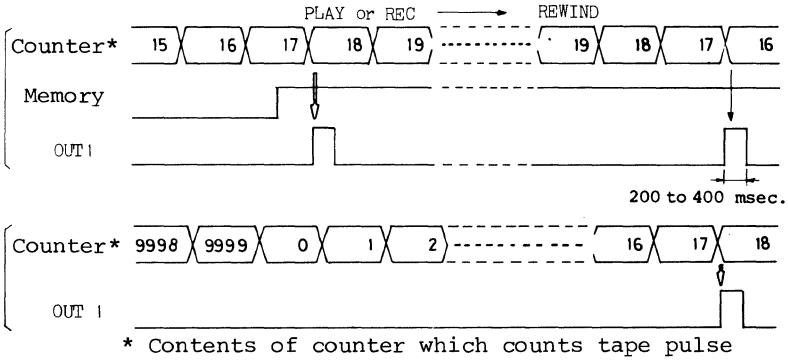
1. Pins for Tape Counter
   UP/DOWN: Input pin for selecting up-count or down-count of tape counter.
   TAPEPULSE: Count pulse input pin for tape counter.
   OUT 1: Output pin for controlling plunger, etc. by detecting coincidence of tape counter contents of all zeros with memory contents.
   MEMORY: Tape counter contents are memorized by applying 'H' level to this input pin. This input pin also signals tape stop output (OUT 1) when memorized contents coincide with tape counter contents.
   DIRECT: Input pin for selecting operation mode of predivider preceding tape counter least significant digit to 1/5 or 1/1.
   SIX/DECADE: Input pin for selecting operation mode of tape counter to base-60 or decimal notation.
2. Common Pins for Tape Counter and Stopwatch
   STW/TAPE DISP:Input pin for selecting display of stopwatch or tape counter.
   RESET : Input pin for resetting tape counter or stopwatch counter to all zeros. Only counter whose display appears is reset.
   BLANKING: Input pin for causing all segment output pins to have high impedance.
3. Pins for Stopwatch
   START/STOP: Instruction input pin for operating or stopping stopwatch counter.
   f_{SELECT}: Input pin for selecting 50Hz or 60Hz as reference input of stopwatch.
   AC IN: Input pin for reference frequency (50/60 Hz) of stopwatch.

5. Logical Functions

1. UP/DOWN (Input)
   For up-count, make 'H'.
   For down-count, make 'L' (or open).
2. TAPEPULSE (Input)
   Display of 0 to 9999, 0 to 5959 is enabled by count pulse. Display is varied ±1 by applying 5 pulses or 1 pulse to TAPEPULSE input.

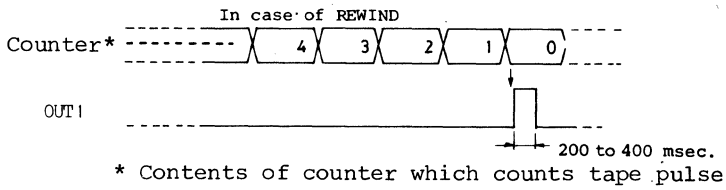
5 usec. chattering prevention circuit is built in this pin.

3. DIRECT (Input)
   Display is varied +1 or -1 by applying 5 pulses to TAPEPULSE pin when this pin is made 'L' (open).
   Display is varied +1 or -1 by applying 1 pulse to TAPEPULSE pin when this pin is made 'H'.
4. SIX/DECADE
   When this pin is made 'L' (open), tape counter becomes decimal counter and display of 0 to 9999 is enabled by count pulse.
   When this pin is made 'H', tape counter becomes base-60 counter and display of 0 to 5959 is enabled by count pulse.
5. Counter All Zeros Detection (OUT 1 Output)
   The moment tape counter contents are changed from 1 to 0, output driver OUT 1 stays "on" for approximately 200 to 400 msec., that is, OUT 1 is 'H'.
6. Memory Stop Detection (OUT 1 Output)
   The moment memory input is made from 'L' to 'H', tape counter contents (N) are memorized. When tape counter counts up as N + 1, N + 2, ----, N + k, and then counts down as N + k - 1, -----, N + 1, and the counter contents coincide with memorized value (N), OUT 1 output immediately stays "on" for approximately 200 to 400 msec., that is, OUT 1 is 'H'.
   When count-down is further started and counter contents are changed from 1 to 0, OUT 1 output immediately stay "on" for approximately 200 to 400 msec., that is, OUT 1 is'H'.
   When count-up is further started as 0, 1, 2, -----, N - 2, N - 1 and counter contents coincide with memorized value (N), OUT 1 output immediately stays "on" for approximately 200 to 400 msec., that is, OUT 1 is 'H'.
   When memory pin is 'L', OUT 1 is "off", that is, OUT 1 remains 'L'.
7. When memory pin is made 'H', operation in Item 6 is performed.
8. OUT 1 Output
   Output pin for generating signal for count pulse zero detection, counter all zeros detection, memory stop detection. Generated pulse stays 'H' for approximately 200 to 400 msec.
   (1) Output timing of OUT 1
   (a) Memory stop (Memory stop detection)



* Contents of counter which counts tape pulse

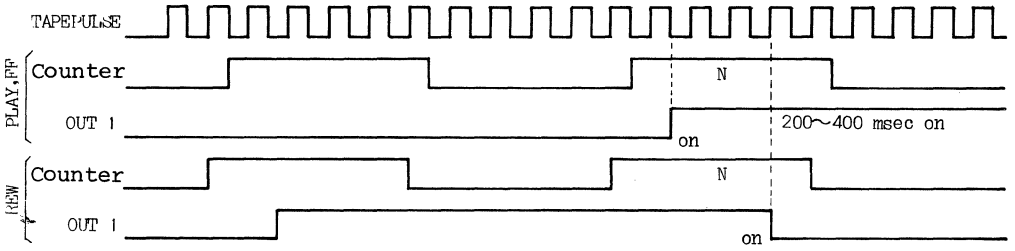
(b) Counter zero stop (Counter all zeros detection)



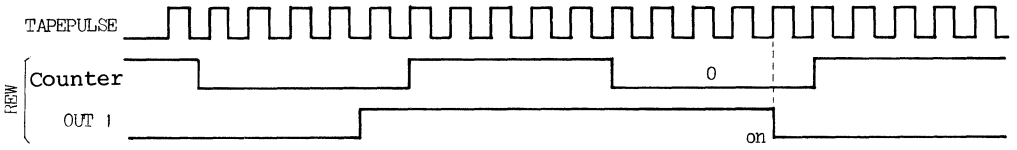
* Contents of counter which counts tape pulse.

(2) Output timing of OUT1 (Detail)

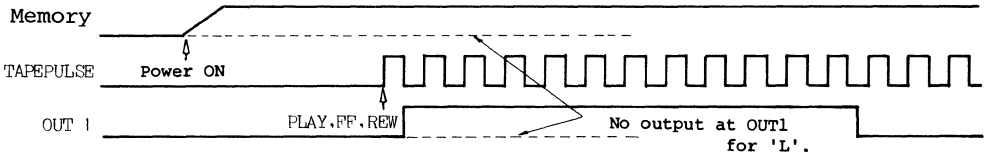
(a) Memory stop (Memory pin 'H', memory contents N)



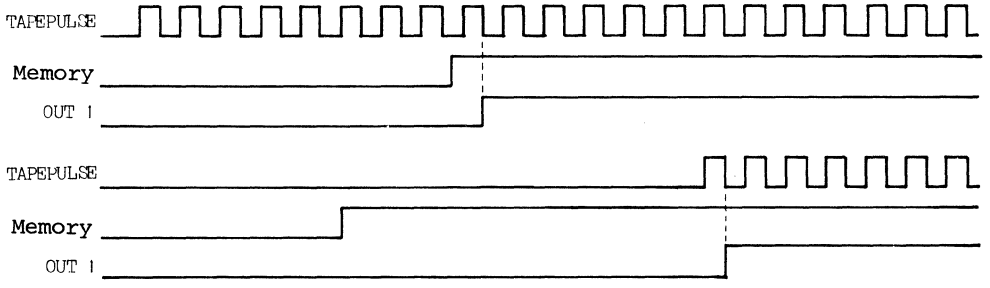
(b) 0 stop TAPEPULSE Counter



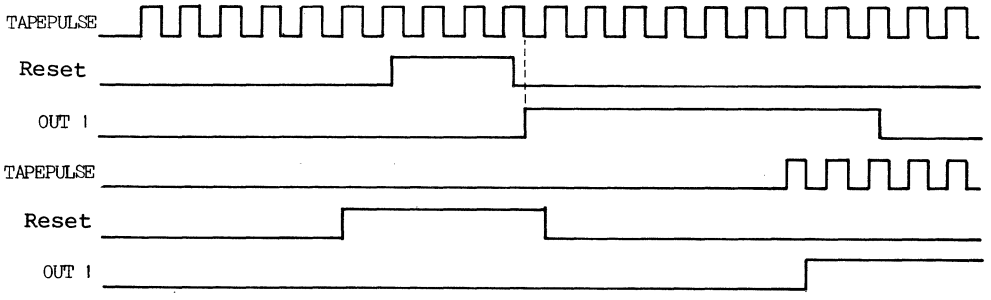
(c) Memory pin 'H' at the time of power ON



(d) Immediately after memory pin 'L' —— 'H'



(e) Reset at the time of memory pin 'H'

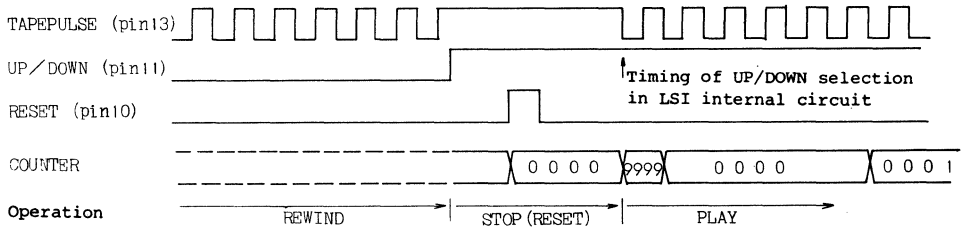


9. STW/TAPE DISP Input
   Stopwatch counter display when this pin is 'H', and tape counter display when 'L' (open).
10. RESET Input
   . Stopwatch counter contents become 0 when STW/TAPE DISP input pin of Item 9 is made 'H' and RESET pin is also made 'H'.
   . Tape counter contents become 0 when STW/TAPE DISP input pin of Item 9 is made 'L' (open) and RESET pin is made 'H'.
   . This RESET pin is made 'L' when opened.
11. Initial Clear Circuit: Counter Reset Function when Power Supply is turned ON.
   Internal reset circuit which turns flip-flop inside LSI such as tape counter, stopwatch counter into initial state the moment voltage is applied to LSI. Counter contents are all 0 at initial state.
12. BLANKING Input
   All segments output is made 'L' by making this BLANKING pin 'L' (open) when display (LED) only is used in common with another LSI, e.g. digital clock. Display is also blanked by making this BLANKING pin 'L' in order to save power dissipation when energizing with battery, etc.
13. START/STOP input
   . When START/STOP pin is made 'H', display is varied +1 per second.
   . When START/STOP pin is made 'L', display stops being varied +1.
   15 to 30 msec. chattering prevention circuit is built in this pin.
14. f_{SELECT} Input
   . Frequency select pin is made 'H' when applying 50Hz to input pin of Item 13.
   . Frequency select pin is made 'L' when applying 60Hz to input pin of Item 13.
15. AC IN Input
   Commercial frequency (50/60 Hz) is applied to this input pin as reference frequency of stopwatch counter. Hysteresis circuit is built in this input pin.

6. Precautions

1. Input level at TAPEPULSE pin at STOP mode
   UP/DOWN select signal is inputted to the internal circuit of LSI only when TAPEPULSE is at "L". Therefore, if operated in the sequence of REWIND ⟶ STOP ⟶ RESET ⟶ PLAY (or F.F.) when TAPEPULSE is at "H" level at STOP mode, the display after RESET counts down once and then starts counting up as 0 ⟶ 9999 ⟶ 1 ⟶ 2 -----. (Refer to Fig. 1.)
   To avoid this operation mode, the TAPEPULSE generator must be designed so that output at STOP mode becomes "L". Fig. 2,3 are the examples of this circuit design.

. TAPEPULSE stops at "H" level.



. TAPEPULSE stops at "L" level.

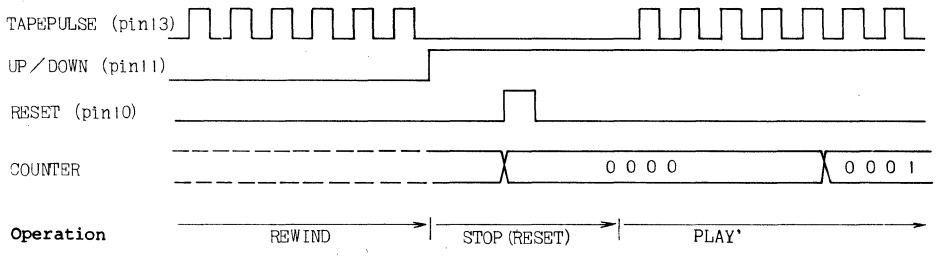
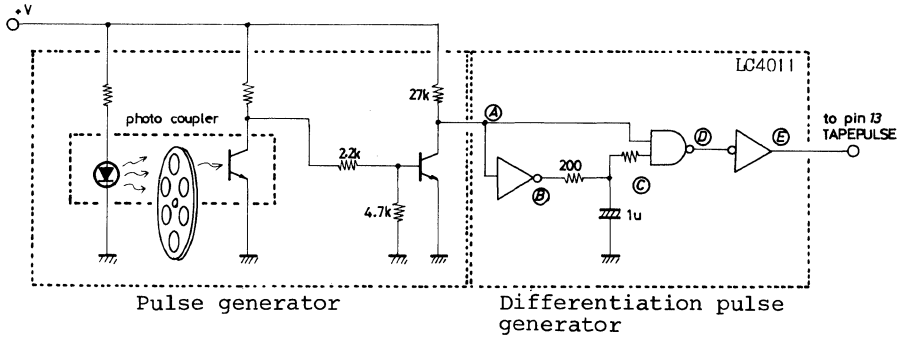


Fig. 1 Timing chart



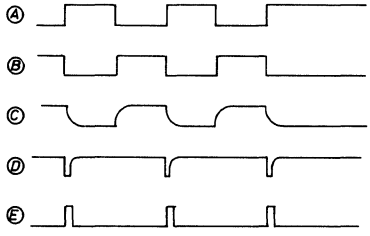
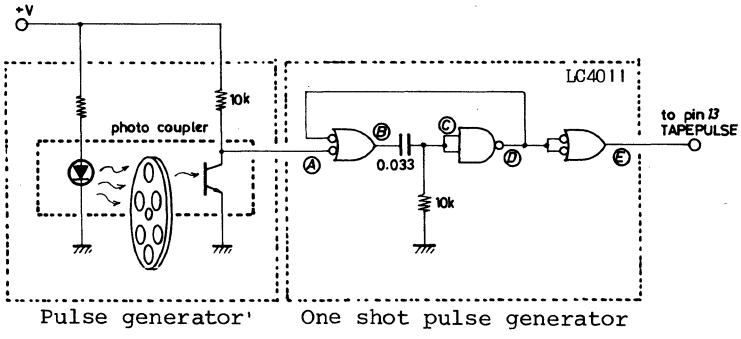


Fig. 2 Example (1) of circuit to make TAPEPULSE "L" level at STOP mode/how to generate.



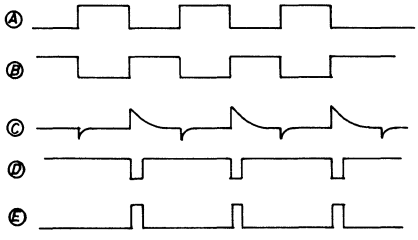
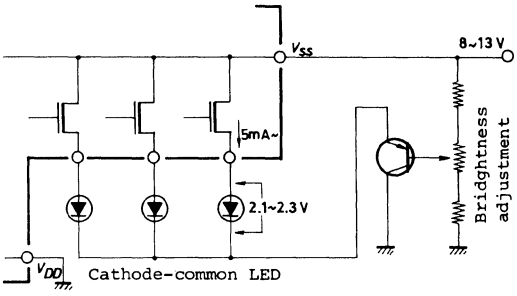
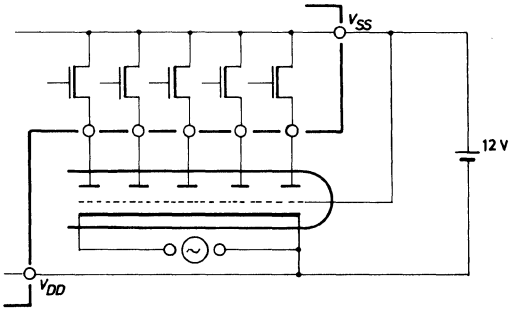


Fig. 3 Example (2) of circuit to make TAPEPULSE "L" level at STOP mode.

7. LED Driver

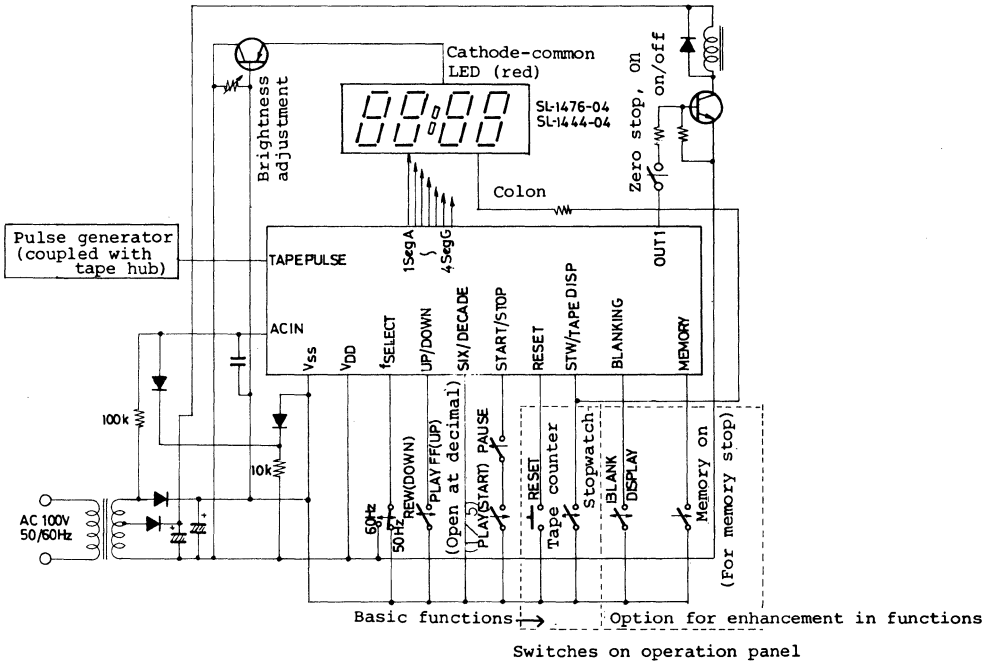


8. Digitron Driver



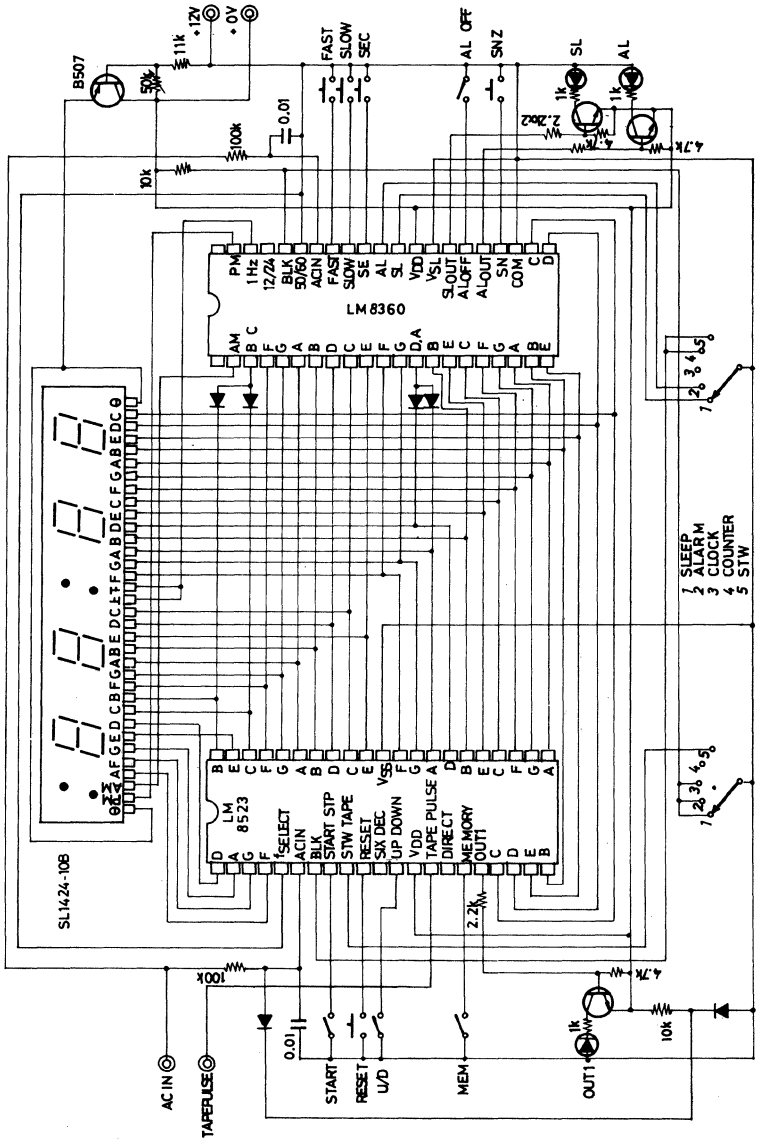
9. Application Circuit (1)

Functions (1) Tape counter
(2) Stopwatch
(3) Zero stop (at REW)
(4) Memory stop (at FF, PLAY REW)



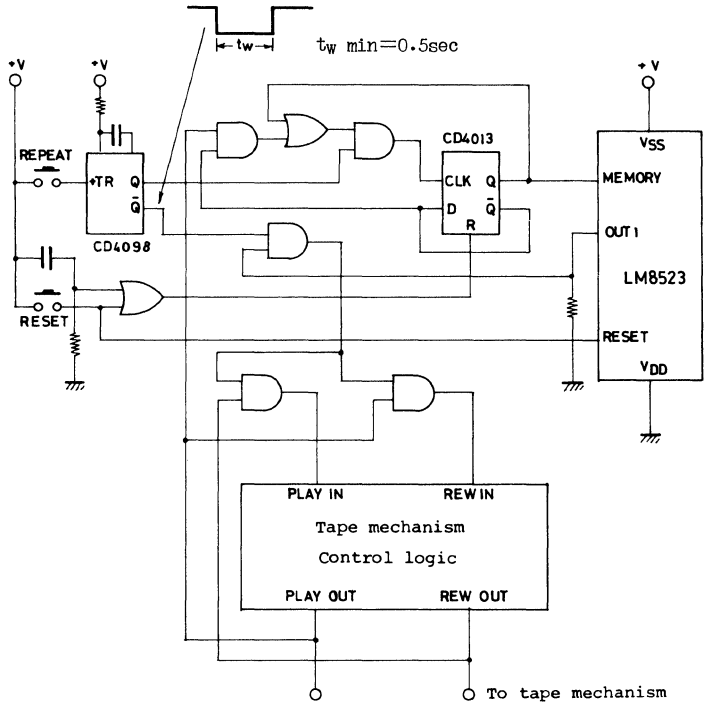
Application (2)

Functions (1) Tape counter
(2) Stopwatch
(3) Clock
(4) Alarm
(5) Sleep timer

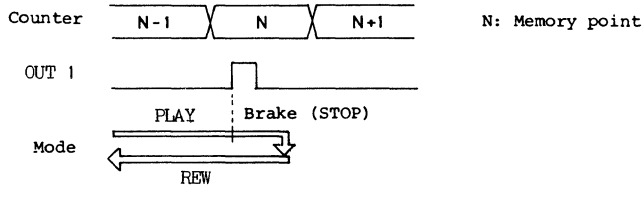


Application (3)

Function : Repeat play (0 $\underset{\text{REW}}{\overset{\text{PLAY}}{\rightleftarrows}}$ memory point)



- If REPEAT switch is turned ON at PLAY mode, REPEAT mode is set, and if REPEAT switch is turned ON again at any operation mode, REPEAT mode is reset.
- If PLAY starts with 0, REPEAT operates normally, but if PLAY starts with memory point, REPEAT does not operate notmally.
- If counter is reset, REPEAT mode is reset.
- After power is turned ON, REPEAT mode is reset.
- PLAY ⟶ REW switchover is designed to occur before the reading of counter becomes memory point +1.

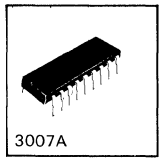


- **Pin Numbering**

When you face the top side (marking side) of the package, numbering starts with ① assigned to the pin located, in a counterclockwise direction, immediately after the index point and turns counterclockwise.

OTHER APPLICATIONS

LC7150



C MOS SI GATE LSI

PLL For Cordless Telephone

Ⓔ 1634

Functions :

- On-chip PLL for transmission/reception
- On-chip digital unlock detector (only PLL for transmission)
- 5.0kHz/4.4kHz output pins for guard tone
- Standby function

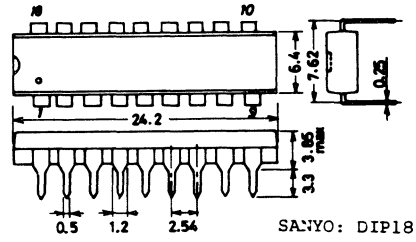
Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		-0.3 to 6.5	V
Maximum Input Voltage	$V_I max$	All input pins	-0.3 to V_{DD}+0.3	V
Maximum Output Voltage	$V_{O1}max$	$\overline{F1}$,$\overline{F2}$ Output OFF	-0.3 to +6.5	V
	$V_{O2}max$	Output pins other than $V_{OUT(1)}$	-0.3 to V_{DD}+0.3	V
Output Current	I_{OUT}	$\overline{F1}$,$\overline{F2}$,LDT	0 to 3.0	mA
Allowable Power Dissipation	Pdmax	Ta≤75°C		mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Conditions at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		3.0		5.5	V
"H"-Level Input Voltage	V_{IH1}	D1 to D4,$\overline{SB}$	0.7V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL1}	"	0		0.3V_{DD}	V
"H"-Level Input Voltage	V_{IH2}	$\overline{R}$/B	0.9V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL2}	"	0		0.1V_{DD}	V
Input Frequency	f_{IN1}	PIT;V_{IN}=0.1Vrms	10		27	MHz
	f_{IN2}	PIR; "	30		42	MHz
	f_{IN3}	XIN;V_{IN}=0.3Vrms	5.0	10.24	11.0	MHz
Input Amplitude	V_{IN1}	PIT;f_{IN}=27MHz	0.1		0.3V_{DD}	Vrms
	V_{IN2}	PIR;f_{IN}=42MHz	0.1		0.3V_{DD}	Vrms
	V_{IN3}	XIN;f_{IN}=11MHz	0.3		0.3V_{DD}	Vrms

Case Outline 3007A-D18IC
(unit:mm)



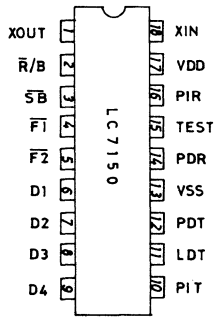
SANYO: DIP18

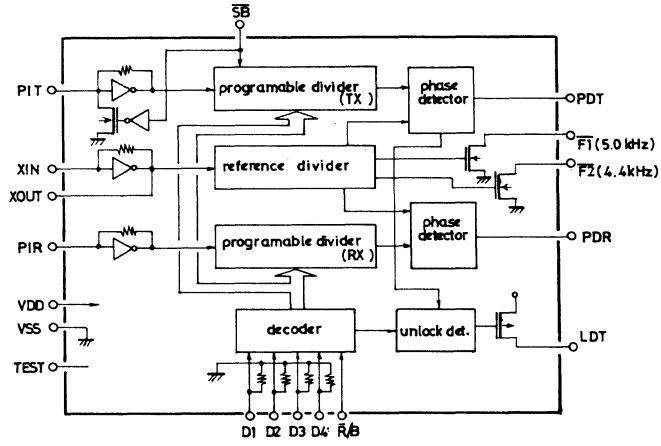
Electrical Characteristics at Ta=25°C, under Allowable Operating Conditions

			min	typ	max	unit
"H"-Level Input Current	I_{IH1}	XIN; $V_I=V_{DD}$			20	uA
"L"-Level Input Current	I_{IL1}	XIN; $V_I=V_{SS}$			20	uA
"H"-Level Input Current	I_{IH2}	PIT,PIR; $V_I=V_{DD}$			40	uA
"L"-Level Input Current	I_{IL2}	PIT,PIR; $V_I=V_{SS}$			40	uA
"H"-Level Input Current	I_{IH3}	$\overline{SB}$,$\overline{R}$/B; $V_I=V_{DD}$			10	uA
"L"-Level Input Current	I_{IL3}	$\overline{SB}$,$\overline{R}$/B; $V_I=V_{SS}$			10	uA
"H"-Level Input Current	I_{IH4}	D1 to D4; $V_I=V_{DD}$	25	130	500	uA
Input Floating Voltage	V_{IF}	D1 to D4; Open			$0.1V_{DD}$	V
Feedback Resistance	R_{f1}	XIN; V_{DD}=4.3V		1.0		Mohm
	R_{f2}	PIT,PIR; "		0.5		Mohm
"H"-Level Output Voltage	V_{OH1}	PDT,PDR; Io=0.5mA	V_{DD}-1.0			V
"L"-Level Output Voltage	V_{OL1}	PDT,PDR; Io=0.5mA			1.0	V
Output OFF Leak Current	I_{off1}	PDT,PDR; Vo=V_{DD}/V_{SS}		0.01	1.0	nA
"H"-Level Output Voltage	V_{OH2}	LDT; Io=1mA	V_{DD}-1.0			V
Output OFF Leak Current	I_{off2}	LDT; Output OFF Vo=V_{SS}			5.0	uA
"L"-Level Output Voltage	V_{OL2}	$\overline{F1}$,$\overline{F2}$; Io=1mA			1.0	V
Output OFF Leak Current	I_{off3}	$\overline{F1}$,$\overline{F2}$; Output OFF Vo=5.5V			5.0	uA
"H"-Level Output Voltage	V_{OH3}	XOUT				V
"L"-Level Output Voltage	V_{OL3}	XOUT				V
Current Dissipation	I_{DD1}	(C3)V_{DD}=3.0V		4		mA
	I_{DD2}	(C3)V_{DD}=4.5V		7		mA
	I_{DD3}	(C3)V_{DD}=5.5V		13		mA
	I_{DD4}	(C2)V_{DD}=3.0V		3		mA
	I_{DD5}	(C2)V_{DD}=4.5V		5		mA
	I_{DD6}	(C2)V_{DD}=5.5V		10		mA

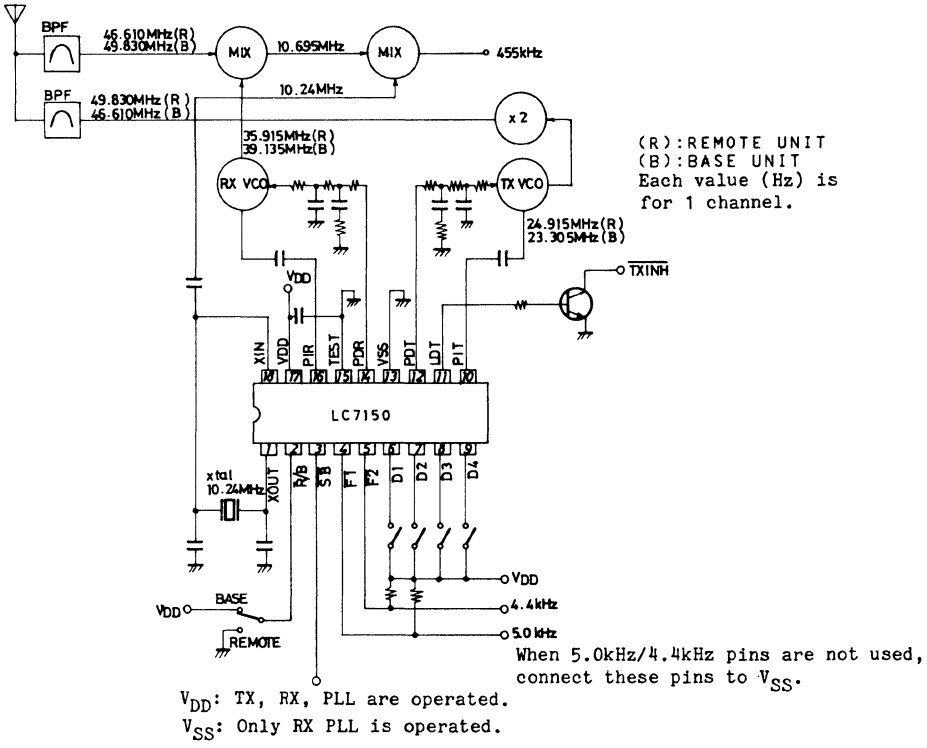
(C3):XIN=10.24MHz,Xtal connected
PIT=27MHz 100mVrms
PIR=42MHz 100mVrms
$\overline{R}$/B=V_{DD},$\overline{SB}$=V_{DD},Other pin open
(C2):XIN=10.24MHz,Xtal connected
PIR=42MHz,
$\overline{R}$/B=V_{DD},$\overline{SB}$=V_{SS},Other pin open

Pin Assignment
Equivalent Circuit Block Diagram





Sample Application Circuit



Pin Description

$\overline{F1}$: 5.0kHz output. When not used, connect to V_{SS}.

$\overline{F2}$: 4.4kHz output(10.24MHz-2304). When not used, connect to V_{SS}.

V_{DD},V_{SS}: Power supply.

XIN,XOUT:Crystal resonator (10.24MHz).

D1 to D4:Channel select pin.

$\overline{R}$/B: Base unit/remore unit select pin.

$\overline{R}$/B="0"(V_{SS}).....Remote unit

$\overline{R}$/B="1"(V_{DD}).....Base unit

SB: Used to stop the TX PLL at the standby mode to minimize current dissipation.

$\overline{SB}$="0"(V_{SS}).....Standby mode. Only the TX PLL is operated. The charge pump enters a high-impedance mode.

$\overline{SB}$="1"(V_{DD})..... The TX, RX PLL are operatd.

PIT: TX programmable divider input pin.

PIR: RX programmable divider input pin.

PDT: TX charge pump output pin.

PDR: RX charge pump output pin.

TEST: LSI test input pin. Connected to V_{SS}.

LDT: TX PLL unlock signal output pin.

When the phase difference becomes t_D(=6.25usec.) or more, 5.6msec. output pulse is delivered at the LDT pin.

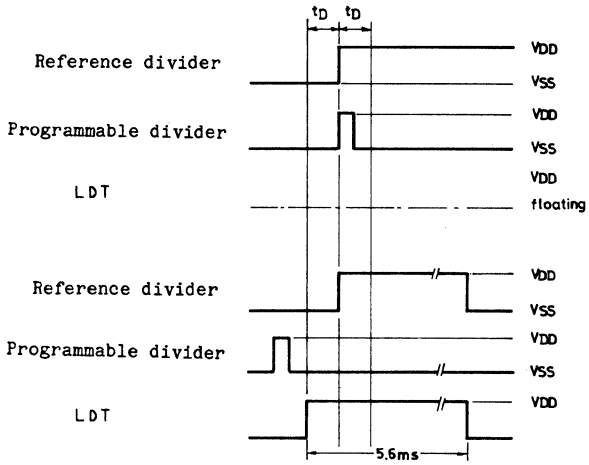
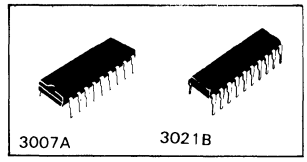


Table of Frequency Division

INPUT				C	REMOTE ($\bar{R}$/B='0')					BASE ($\bar{R}$/B='1')				
					TX(fref=2.5kHz)		RX(fref=5kHz)			TX(fref=2.5kHz)		RX(fref=5kHz)		
				H	fTX (MHz)	fVCO (MHz)	N	fVCO (MHz)	N	fTX (MHz)	fVCO (MHz)	N	fVCO (MHz)	N
D1	D2	D3	D4											
1	0	0	0	1	49.670	24.8350	9934	35.915	7183	46.610	23.305	9322	38.975	7795
0	1	0	0	2	49.845	24.9225	9969	35.935	7187	46.630	23.315	9326	39.150	7830
1	1	0	0	3	49.860	24.9300	9972	35.975	7195	46.670	23.335	9334	39.165	7833
0	0	1	0	4	49.770	24.8850	9954	36.015	7203	46.710	23.355	9342	39.075	7815
1	0	1	0	5	49.875	24.9375	9975	36.035	7207	46.730	23.365	9346	39.180	7836
0	1	1	0	6	49.830	24.9150	9966	36.075	7215	46.770	23.385	9354	39.135	7827
1	1	1	0	7	49.890	24.9450	9978	36.135	7227	46.830	23.415	9366	39.195	7839
0	0	0	1	8	49.930	24.9650	9986	36.175	7235	46.870	23.435	9374	39.235	7847
1	0	0	1	9	49.990	24.9950	9998	36.235	7247	46.930	23.465	9386	39.295	7859
0	1	0	1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1	1	0	1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0	0	1	1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1	0	1	1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0	1	1	1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1	1	1	1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0	0	0	0	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855

LC7350, 7351



C MOS LSI

Pulse Dialer

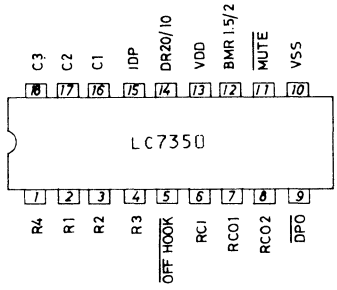
Ⓔ 1529

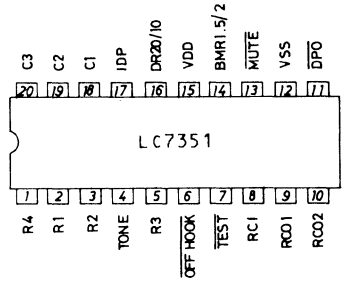
The LC7350(18-pin package)/LC7351(20-pin package) are redial function-provided pulse dialer C-MOS LSI's for use in pushbotton telephones.

Features

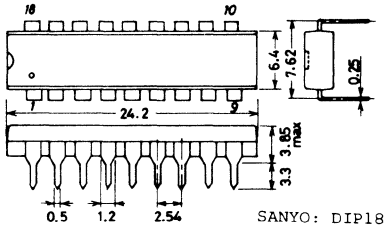
(1) Low voltage C-MOS process for direct operation from telephone line.
(2) Possible to use single contact or standard 2-of-7 key pad.
(3) Contains inexpensive R-C oscillator (f_{OSC}=5kHz typ.).
(4) Two selections of output pulse rate (20pps or 10pps).
(5) Two selections of output pulse break/make ratio (1.5 or 2).
(6) Two selections of inter-digit pause (400ms or 800ms (Note)).
(7) Provides PBX redial mode ("#" key) with access code (2 digits or less).
(8) Contains 20-digit FIFO (First-In-First-Out) buffer memory.
(9) Key touch tone output (1250Hz/625Hz alternating pacifier tone) capability for LC7351(20-pin package).
(10) Supplyvoltage/operatingtemperature ---- V_{DD}=1.5 to 3.5V/Topg=-30 to +70°C
(11) Operating current ---- I_{DD}=100uAmax(V_{DD}=3.5V), I_{DD}=20uAmax(V_{DD}=1.5V) (Note)

Pin Assignment

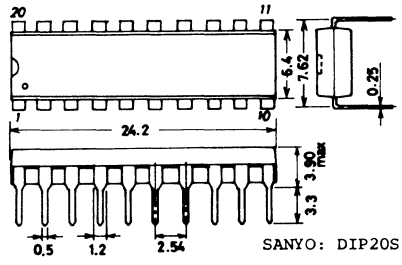




Case Outline 3007A-D18IC
(unit:mm)

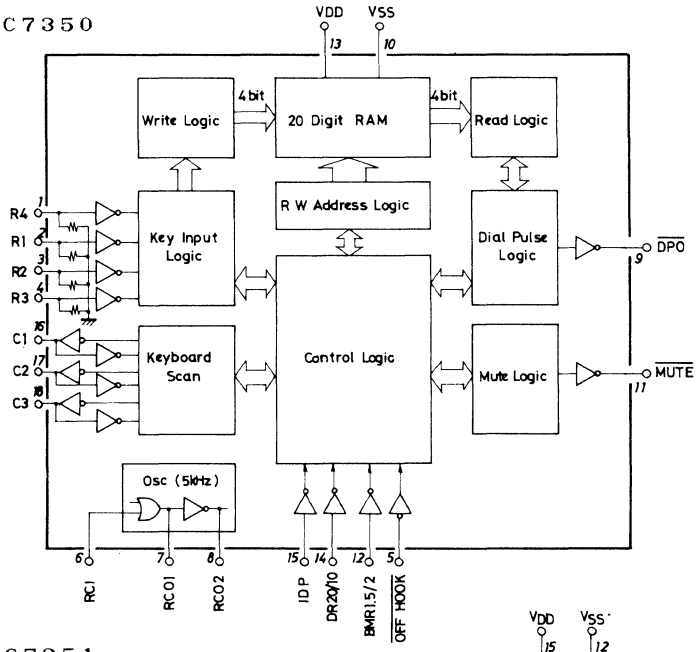


Case Outline 3021B-D20SIC
(unit:mm)

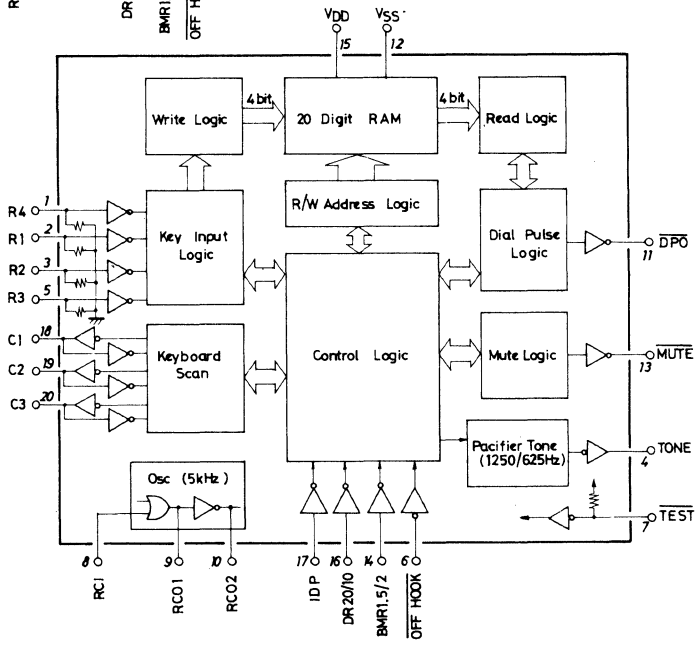


Equivalent Circuit Block Diagram

LC7350



LC7351

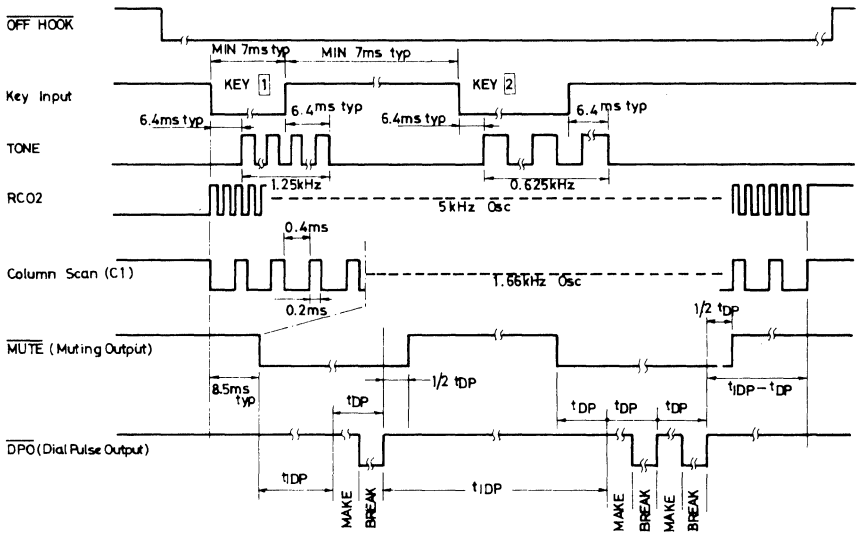


Function Table

(fosc=5kHz)

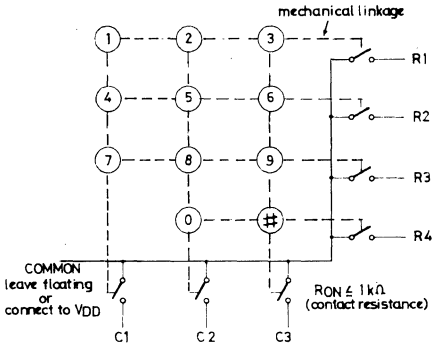
Function	Pin Name	Input Logic Level	Selection
Dial Pulse Rate	DR20/10	V_{SS}	10pps(t_{DP}=100msec)
		V_{DD}	20pps(t_{DP}=50msec)
Make/Break Ratio	BMR 1.5/2.0	V_{SS}	Make=33 1/3(%), Break=66 2/3(%)
		V_{DD}	Make=40(%), Break=60(%)
Inter-Digit Rause	IDP	-	D.P.R=10pps D.P.R=20pps
		V_{SS}	t_{IDP}=800ms t_{IDP}=400msec
		V_{DD}	t_{IDP}=400ms t_{IDP}=200ms

Timing

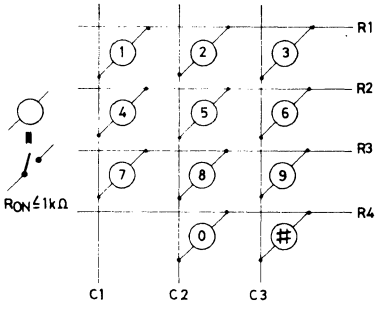


Keyboard Interface

Standard 2 of 7 Keyboard



Single Contact Keyboard

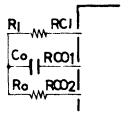


Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +5.5	V
Maxinum Input Voltage	$V_I$max		-0.3 to V_{DD}+0.3	V
Maximum Output Voltage	$V_O$max		-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta--30 to +70°C	150	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=-30 to +70°C, V_{SS}=0V

				min	typ	max	unit
Supply Voltage	V_{DD}			+1.5		+3.5	V
"H"-Level Input Voltage	V_{IH1}	R1,R2,R3,R4,C1,C2,C3		0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{OFF-HOOK}}$,$\overline{\text{TEST}}$(LC7351 only)		0.8V_{DD}		V_{DD}	V
	V_{IH3}	BMR1.5/2.0,DR20/10,IDP		0.9V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL1}	R1,R2,R3,R4,C1,C2,C3		V_{SS}		0.3V_{DD}	V
	V_{IL2}	$\overline{\text{OFF-HOOK}}$,$\overline{\text{TEST}}$(LC7351 only)		V_{SS}		0.2V_{DD}	V
	V_{IL3}	BMR1.5/2.0,DR20/10,IDP		V_{SS}		0.1V_{DD}	V
External Constants for Oscillation Guaratee	R_o		(LC7350)	176	300	360	kohm
			(LC7351)	176	220	360	kohm
	C_o		(LC7350)	243	270	396	pF
			(LC7351)	243	360	396	pF
	R_I		(LC7350)	675	820	1650	kohm
			(LC7351)	675	1200	1650	kohm
Oscillation Frequency	f_{OSC}	RCO2			5.0		kHz
Key Contact Resistance	R_{KI}					1.0	kohm
Keyboard Capacitance	C_{KI}					50	pF

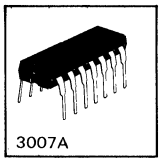


Electrical Characteristics at Ta=25±2°C, V_{SS}=0V *V_{CC}(pin)

			min	typ	max	unit
"H"-Level Input Current	I_{IH1}	V_{IN}=V_{DD},*1.5 to 3.5V,(*)			1.0	uA
	I_{IH2}	" ,*1.5V,(R1,R2,R3,R4)	3.0			uA
		" ,*3.5V,(")			60	uA
"L"-Level Input Current	I_{IL1}	V_{IN}=V_{SS},*1.5 to 3.5V,(*)	-1.0			uA
	I_{IL2}	" ,*1.5V,($\overline{\text{TEST}}$)			-3.0	uA
		" ,3.5V,($\overline{\text{TEST}}$)	-140			uA
"L"-Level Input Floating Voltage	V_{IFL}	Input pin open,*1.5 to 3.5V, (R1,R2,R3,R4)	V_{SS}	0.3V_{DD}	-0.3	V
"H"-Level Output Voltage	V_{OH1}	I_{OH}=20uA,*1.5V,($\overline{\text{DPO}}$,$\overline{\text{MUTE}}$)	V_{DD}-0.5			V
		I_{OH}=125uA,*3.5V,(")	V_{DD}-1.0			V
	V_{OH2}	I_{OH}=20uA,*1.5V,(TONE)	V_{DD}-0.5			V
		I_{OH}=125UA,*3.5V,(")	V_{DD}-1.0			V
"L"-Level Output Voltage	V_{OL1}	I_{OL}=20UA,*1.5V,($\overline{\text{DPO}}$,$\overline{\text{MUTE}}$)			0.4	V
		I_{OL}=125uA,*3.5V,(")			0.4	V
	V_{OL2}	I_{OL}=20uA,*1.5V,(TONE)			0.4	V
		I_{OL}=125uA,*3.5V,(")			0.4	V
Operating Current	I_{DD1}	DR=10pps,*1.5V,(V_{DD})			20	uA
		All output pins:open,*3.5V(V_{DD})			100	uA
Quiescent Current	I_{DD2}	$\overline{\text{OFF-HOOK}}$=$V_{DD}$,All output pins: open,*1.5 to 3.5V,(V_{DD})		0.1	1.0	uA
Frequency Deivation	Δfo/fo	Ro=300kohm,Co=270pF,RI=820kohm 220 , 360 , 1.2Mohm				
		*1.5 to 2.5V,(RCI,RCO1,RCO2)	-3		+3	%
		*2.5 to 3.5V,(")	-3		+3	%
Data Hold Voltage	V_{DR}	($\overline{\text{OFF-HOOK}}$=$V_{DD}$, ($V_{DD}$)	1.0			V
Data Hold Current	I_{DR}	All output pins:open,*1.0V,(V_{DD}))			0.4	uA

(*):$\overline{\text{OFF-HOOK}}$,RCI,DR20/10,BMR1.5/2.0,IDP

LC7352



C MOS LSI

Pulse Dialer

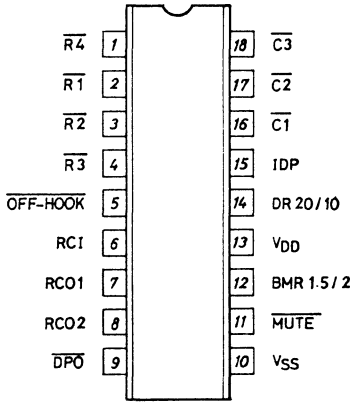
General Description

The LC7352(18-pin package) are redial function-provided pulse dialer C-MOS LSI's for use in pushbutton telephones. (Dial pulse output, mute output : Open drain type / Key Scan Polarity : Low active)

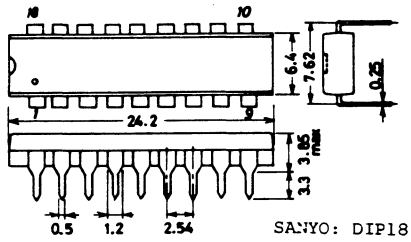
Features

1. Low voltage C-MOS process for direct operation from telephone line.
2. Possible to use single contact or standard 2-of-7 key pad.
3. Contains inexpensive R-C oscillator (f_{OSC}=5kHz typ.).
4. Two selections of output pulse rates (20pps or 10pps).
5. Two selections of output pulse break/make ratios (1.5 or 2).
6. Two selections of inter-digit pause (400ms or 800ms (Note 1)).
7. Provides redial mode ("#" key 3 digits to 20 digits) with access code (2 digits or less) meeting PBX requirements.
8. Contains 20-digit FIFO (First-In-First-Out) buffer memory.
9. Supply voltage/operating temperature --- V_{DD}=1.5 to 3.5V/Topg=-30 to +70°C
10. Operating current --- I_{DD}=100uA max. (V_{DD}=3.5V),I_{DD}=20uA max. (V_{DD}=1.5V).
11. Data hold voltage --- V_{DR}=1.0V, Data hold current I_{DR}=0.4uA (V_{DD}=1.0V)

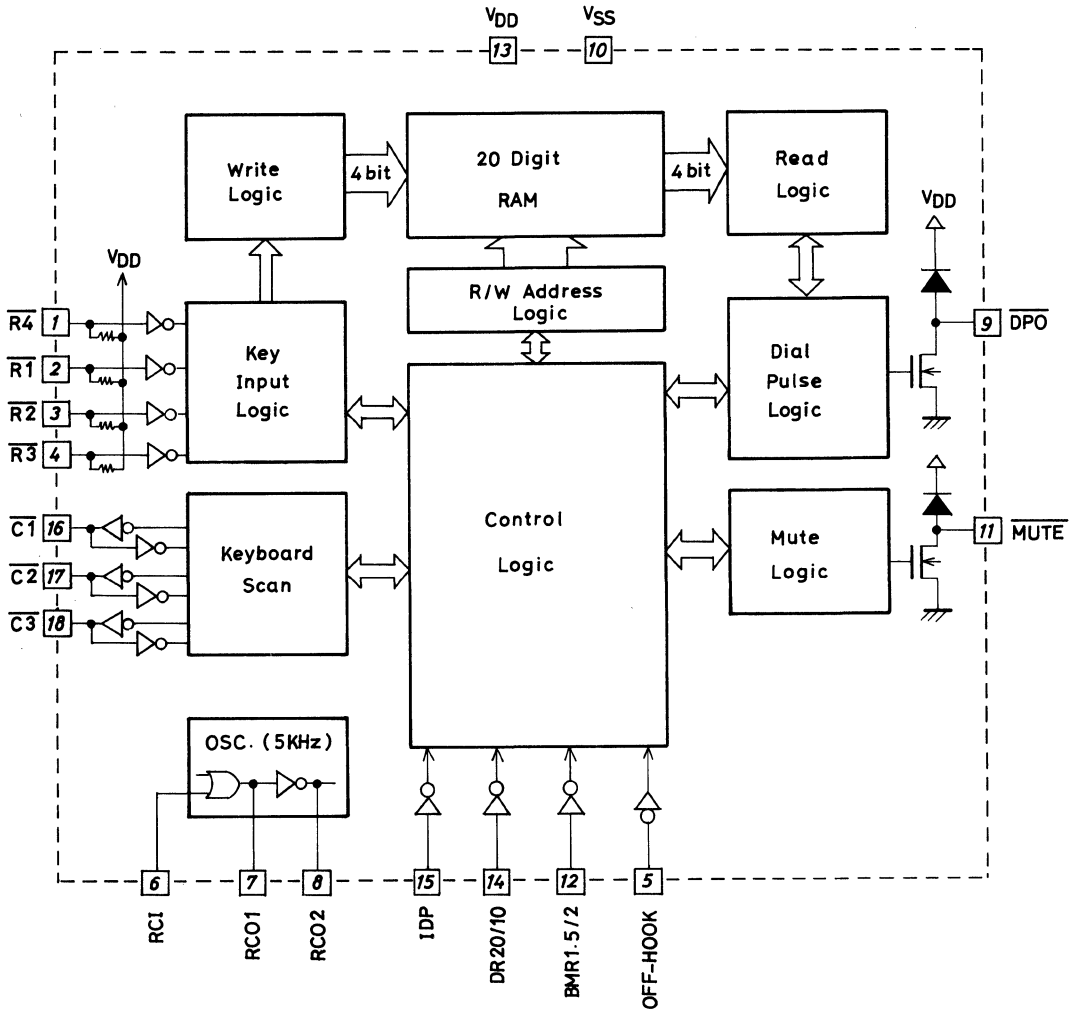
Pin Assignment



Case Outline 3007A-D18IC
(unit:mm)



SANYO: DIP18



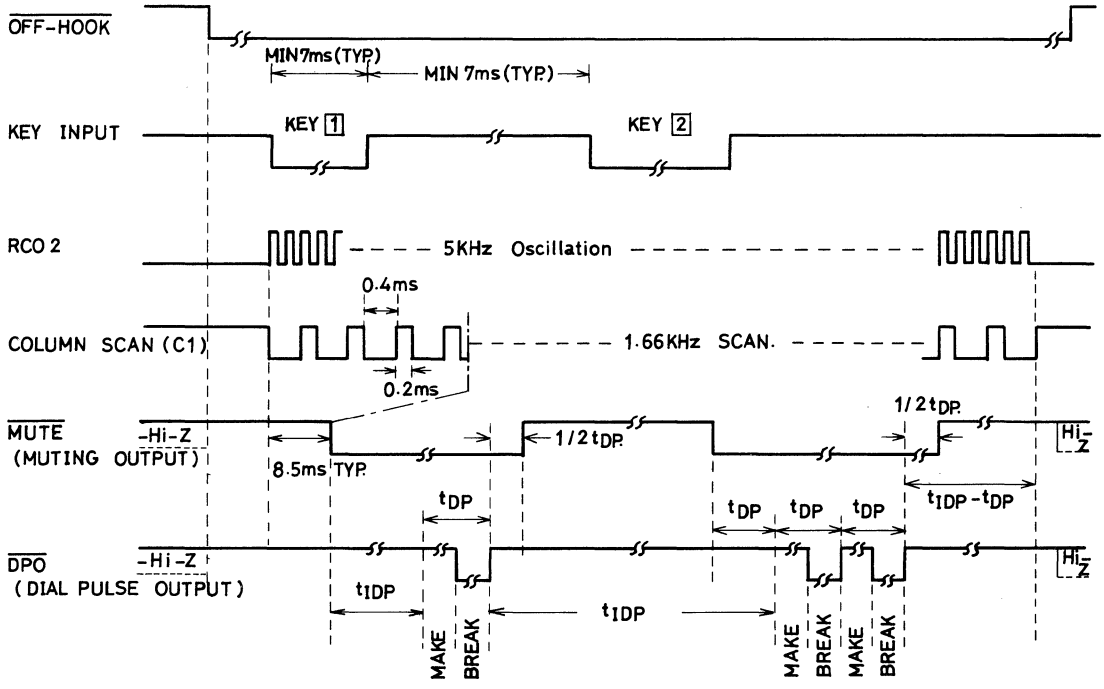
BLOCK DIAGRAM (LC7352)

Function Table

(f_{osc}=5KHz)

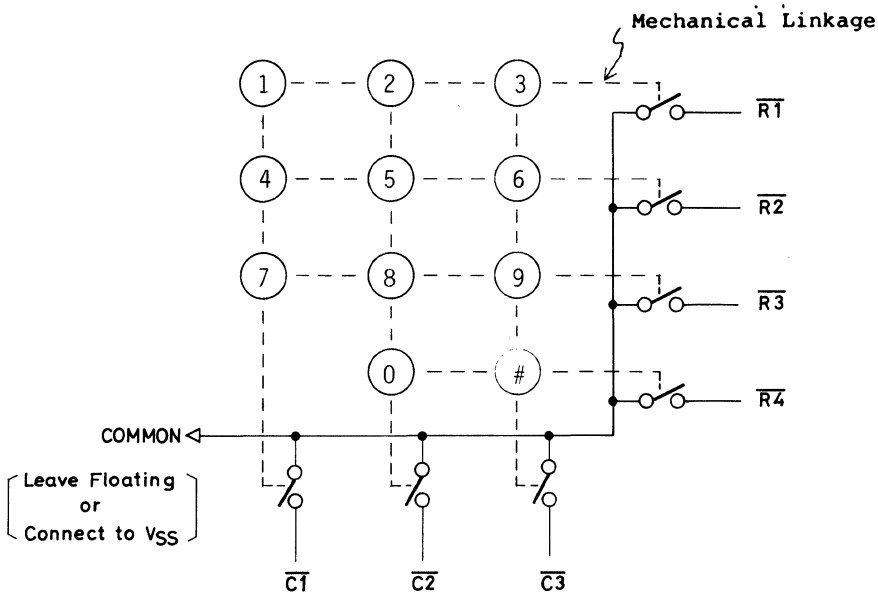
Function	Pin Name	Input Logic Level	Selection	
Dial Pulse Rate	DR20/10	V_{SS}	10PPS (t_{DP}=100ms)	
		V_{DD}	20PPS (t_{DP}=50ms)	
Make Break Ratio	BMR1.5/2	V_{SS}	Make=$33\frac{1}{3}$(%), Break=$66\frac{2}{3}$(%)	
		V_{DD}	Make=40(%), Break=60(%)	
Inter-Digit Pause	IDP		D.P.R=10PPS	D.P.R=20PPS
		V_{SS}	t_{IDP}=800ms	t_{IDP}=400ms
		V_{DD}	t_{IDP}=400ms	t_{IDP}=200ms

TIMING

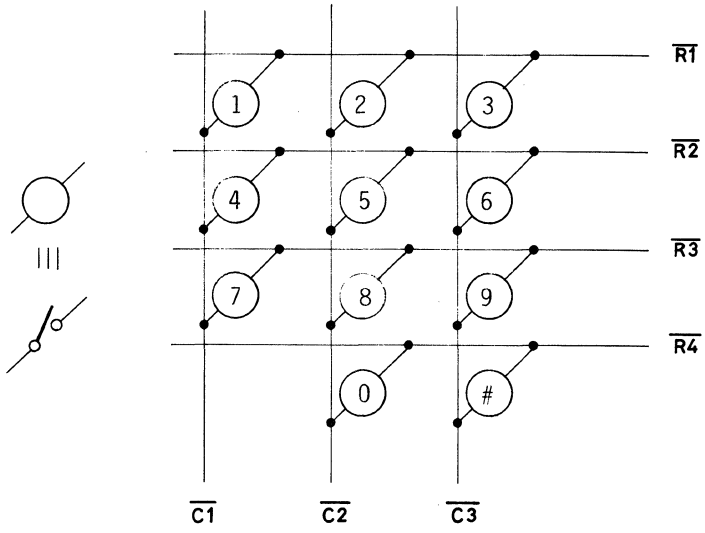


Keyboard Interface

Standard 2 of 7 Keyboard



Single Contact Keyboard



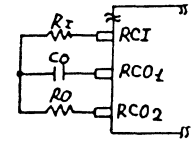
Absolute Maximum Ratings

Ta=25°C±2°C, V_{SS}=0V

Characteristic	Symbol	Conditions	Limits MIN	Limits TYP	Limits MAX	Unit	
Supply Voltage	V_{DD}		-0.3		+5.5	V	
Input Voltage	V_I		-0.3		V_{DD}+0.3	V	
Output Voltage	V_O		-0.3		V_{DD}+0.3	V	
Allowable Power Dissipation	P_D	Ta=-30 to +70°C			150	mW	
Operating Temperature	T_{opg}		-30		+70	°C	
Storage Temperature	T_{stg}		-40		+125	°C	

Allowable Operating Ranges

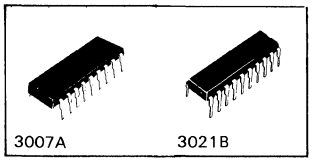
Ta=-30°C~+70°C, V_{SS}=0V

Characteristic	Symbol	Conditions	Limits MIN	Limits TYP	Limits MAX	Unit	Pin Names
Supply Voltage	V_{DD}		+1.5		+3.5	V	
High-Level Input Voltage	$V_{IH(1)}$		0.7V_{DD}		V_{DD}	V	$\overline{R1}$,$\overline{R2}$,$\overline{R3}$,$\overline{R4}$ $\overline{C1}$,$\overline{C2}$,$\overline{C3}$,
	$V_{IH(2)}$		0.8V_{DD}		V_{DD}	V	$\overline{OFF\text{-}HOOK}$
	$V_{IH(3)}$		0.9V_{DD}		V_{DD}	V	BMR1.5/2,DR20/10 IDP
Low-Level Input Voltage	$V_{IL(1)}$		V_{SS}		0.3V_{DD}	V	$\overline{R1}$,$\overline{R2}$,$\overline{R3}$,$\overline{R4}$, $\overline{C1}$,$\overline{C2}$,$\overline{C3}$,
	$V_{IL(2)}$		V_{SS}		0.2V_{DD}	V	$\overline{OFF\text{-}HOOK}$
	$V_{IL(3)}$		V_{SS}		0.1V_{DD}	V	BMR1.5/2,DR20/10 IDP
External Constants for Oscillation Guarantee	R_O		176	300 220	360	KΩ	
	C_O		243	270 360	396	PF	
	R_I		675	820 1200	1650	KΩ	
Oscillation Frequency	f_{OSC}			5.0		KHz	RCO_2

Electrical Characteristics

Characteristic	Symbol	Conditions	V_{DD}	Limits min	Limits typ	Limits max	Unit	Pin Name
High-Level Input Current	$I_{IH}(1)$	$V_{IN}=V_{DD}$	1.5 to 3.5			1.0	uA	$\overline{OFF\text{-}HOOK}$, RCI BMR1.5/2, IDP DR20/10
Low-Level Input Current	$I_{IL}(1)$	$V_{IN}=V_{SS}$	1.5 to 3.5	-1.0			uA	$\overline{OFF\text{=}HOOK}$, RCI, DR20/10, BMR1.5 IDP
	$I_{IL}(2)$	$V_{IN}=V_{SS}$	1.5			-3.0	uA	$\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$
			3.5	-60				
High-Level Input Floating Voltage	V_{IFL}	Input pin open	1.5 to 3.5	$0.7V_{DD}+0.3$		V_{DD}	V	$\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$
Output Off-leak Current	I_{OFF}	Output Tr: OFF $V_O=V_{SS}$ to V_{DD}	1.5 to 3.5			1.0	uA	$\overline{DPO}$, $\overline{MUTE}$
Low-Level Output Voltage	V_{OL}	I_{OL}=20uA	1.5			0.4	V	$\overline{DPO}$, $\overline{MUTE}$
		I_{OL}=125uA	3.5			0.4		
Operating Current	$I_{DD}(1)$	.DR=10PPS .All output pins: No load	1.5			20	uA	V_{DD}
			3.5			100		
Quiescent Current	$I_{DD}(2)$	.$\overline{OFF\text{-}HOOK}$ =V_{DD} .All output pins ---No load	1.5 to 3.5		0.1	1.0	uA	V_{DD}
Frequency Deviation	$\Delta f_O/f_O$	R_O 300 kΩ 220 kΩ	1.5 to 2.5	-3		+3	%	RCI RCO_1 R_{CO2}
		C_O 270 360	2.5 to 3.5	-3		+3	%	
		R_I 820 1200						
Data Hold Voltage	V_{DR}	.$\overline{OFF\text{-}HOOK}$ =V_{DD} .All output pins--- No load		1.0			V	V_{DD}
Data Hold Current	I_{DR}		1.0			0.4	uA	

LC7353, 7354



C MOS LSI

Pulse Dialer

Ⓔ 1585

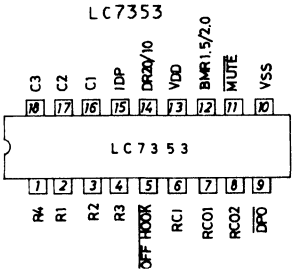
General Description

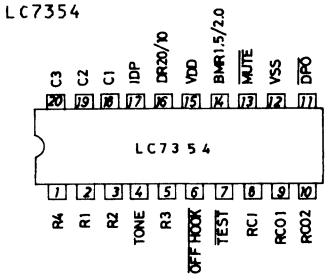
The LC7353(18-pin package)/LC7354(20-pin package) are redial function-provided pulse dialer C-MOS LSI's for use in pushbutton telephones. (Dial pulse output ($\overline{DPO}$), MUTE OUTPUT($\overline{MUTE}$): Open drain type).

Features

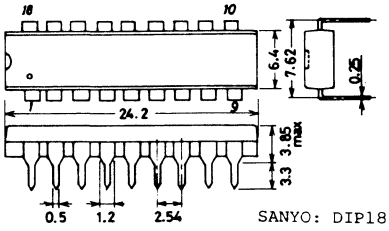
1. Low voltage C-MOS process for direct operation from telephone line.
2. Possible to use single contact or stancard 2-of-7 key pad.
3. Contains inexpensive R-C oscillator (f_{OSC}=5kHz typ.).
4. Two selections of output pulse rate (20pps or 10pps).
5. Two selections of output pulse break/make ratio (1.5 or 2).
6. Two selections of inter-digit pause (400ms or 800ms (DR=10pps).
7. Provides PBX redial function (# key, 3 digits to 20 digits) with access code (2 digits or less).
8. Contains 20-digit FIFO (First-In-First-Out) buffer memory.
9. Key touch tone output (1250Hz/625Hz alternating pacifier tone) capability for LC7354 (20-pin package).
10. Supply voltage: V_{DD}=1.5 to 3.5V, Operating temperature: Topg=-30 to +70°C.
11. Operating Current: I_{DD}max=100uA/V_{DD}=3.5V,
    20uA/V_{DD}=1.5V.
12. Data hold voltage: $V_{DR} \geq$1.0V, Data hold Current: $I_{DR} \leq$0.4uA(V_{DD}=1.0V)

Pin Assignment

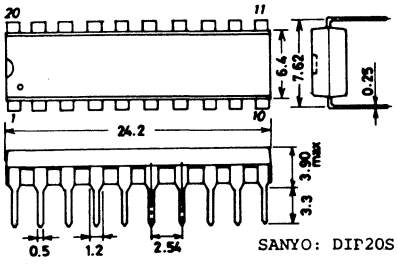




Case Outline 3007A-D18IC LC7353
(unit:mm)

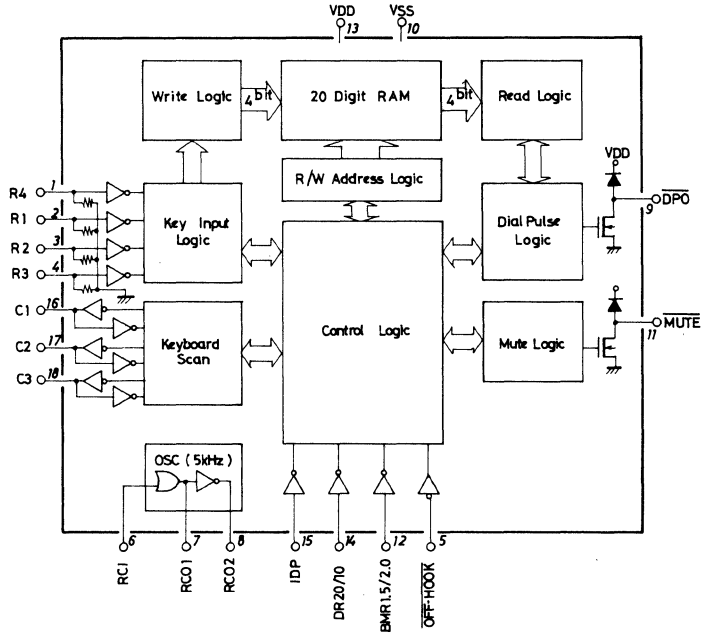


Case Outline 3021B-D20SIC LC7354
(unit:mm)

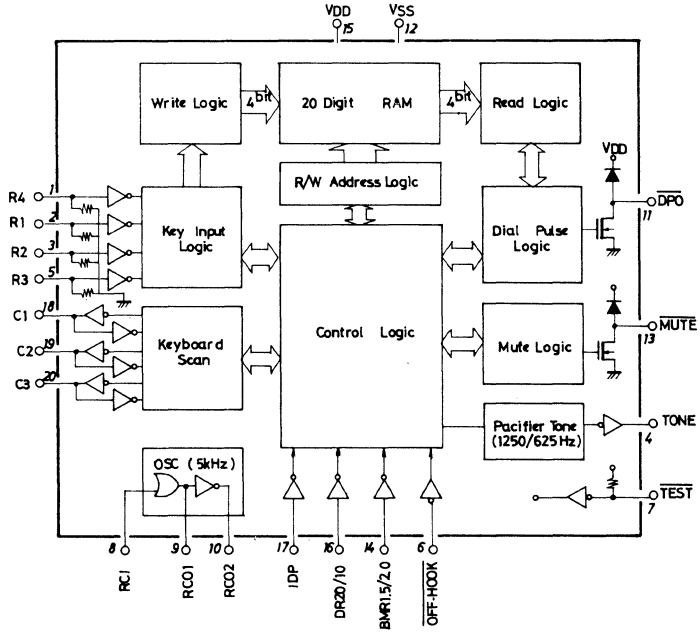


Equivalent Circuit Block Diagram

LC7353



LC7354

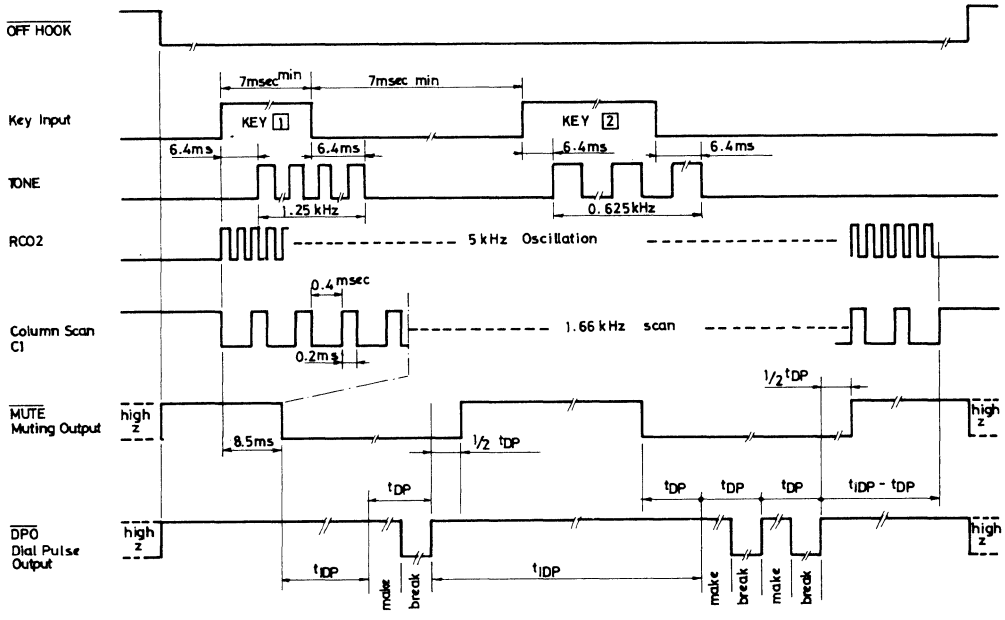


Function Table

(f_{osc}=5KHz)

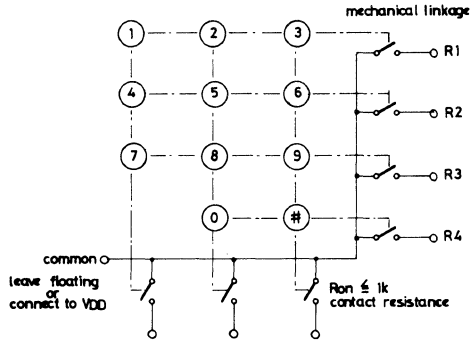
Function	Pin Name	Input Logic Level	Selection	
Dial Pulse Rate	DR20/10	V_{SS}	10PPS(t_{DP}=100ms)	
		V_{DD}	20PPS(t_{DP}=50ms)	
Make Break Ratio	BMR1.5/2	V_{SS}	Make=$33\frac{1}{3}$(%),Break=$66\frac{2}{3}$(%)	
		V_{DD}	Make=40(%),Break=60(%)	
Inter-Digit Pause	IDP		D.P.R=10PPS	D.P.R=20PPS
		V_{SS}	t_{IDP}=800ms	t_{IDP}=400ms
		V_{DD}	t_{IDP}=400ms	t_{IDP}=200ms

Timing

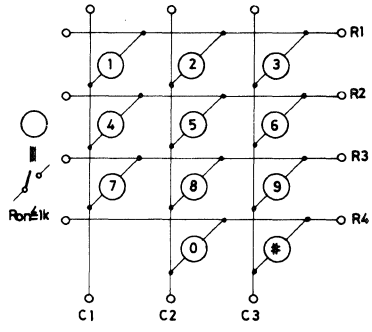


Keyboard Interface

Standard 2 of 7 Keyboard



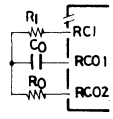
Single Contact Keyboard



Absolute Maximum Ratings at Ta=25±2°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +5.5	V
Maximum Input Voltage	$V_I$max		-0.3 to +V_{DD}+0.3	V
Maximum Output Voltage	$V_O$max		-0.3 to +V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta=-30 to +70°C	150	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C

			min	typ	max	unit
Supply Voltage	V_{DD}		+1.5		+3.5	V
"H" Level Input Voltage	V_{IH1}	R1,R2,R3,R4,C1,C2,C3	0.7V_{DD}		V_{DD}	V
	V_{IH2}	OFF-HOOK,TEST	0.8V_{DD}		V_{DD}	V
	V_{IH3}	BMR1.5/2.0,DR20/10,IDP	0.9V_{DD}		V_{DD}	V
"L" Level Input Voltage	V_{IL1}	R1,R2,R3,R4,C1,C2,C3	V_{SS}		0.3V_{DD}	V
	V_{IL2}	OFF-HOOK,TEST	V_{SS}		0.2V_{DD}	V
	V_{IL3}	BMR1.5/2.0,DR20/10,IDP	V_{SS}		0.1V_{DD}	V
Oscillation Guaranteed External Constants	R_O		176	(300	(220	360 kohm
	C_O		243	270)	or 360)	396 pF
	R_I		675	820)	1200)	1650 kohm

Oscillation Frequency	f_{OSC}	RCO2		5.0		kHz
Key Contant Resistance	R_{KI}				1.0	kohm
Keyboard Capacitance	C_{KI}				50	pF

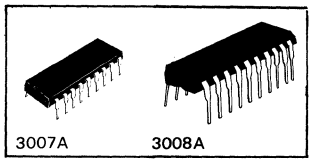
Electrical Characteristics at Ta=25±2°C, V_{SS}=0V, V_{DD}=See a, b, c, d defined below.

					min	typ	max	unit
"H" Level Input Current	I_{IH1}	V_{IN}=V_{DD},	btod	OFF-HOOK,RCI, DR20/10 BMR1.5/2.0,IDP			1.0	uA
	I_{IH2}	V_{IN}=V_{DD},	b	R1,R2,R3,R4	3.0			uA
		"	d	"			60	uA
"L" Level Input Current	I_{IL1}	V_{IN}=V_{SS},	btod	OFF-HOOK,RCI, DR20/10, BMR1.5/2.0,IDP	-1.0			uA
	I_{IL2}	V_{IN}=V_{SS},	b	TEST			-3.0	uA
		"	d	"	-140			uA
"L" Level Input Floating Voltage	V_{IFL}	Input pin open,	btod	R1,R2,R3,R4	V_{SS}	0.3V_{DD}	-0.3	V
"H" Level Output Voltage	V_{OH}	I_{OH}=20uA	b	TONE	V_{DD}-0.5			V
		I_{OH}=125uA	d	"	V_{DD}-1.0			V
Output Off-leak Current	I_{OFF}	Output tr. OFF, Vo=V_{SS}toV_{DD},	btod	DPO,MUTE			1.0	uA
"L" Level Output Voltage	V_{OL1}	I_{OL}=20uA	b	DPO,MUTE			0.4	V
		I_{OL}=125uA	d	"			0.4	V
	V_{OL2}	I_{OL}=20uA	b	TONE			0.4	V
		I_{OL}=125uA	d	"			0.4	V
Operating Current	I_{DD1}	(DR=10pps, All output pins:No load)	b	V_{DD}			20	uA
			d	"			100	uA

					min	typ	max	unit
Quiescent Current	I_{DD2}	OFF-HOOK= V_{DD}, All output pins :No load	btod	V_{DD}		0.1	1.0	uA
Frequency Deviation	$\Delta f_o / f_o$	(kohm/pF) R_o 300 220, C_o 270 360, R_I 820 1200	btoc ctod	RCI,RCO1,RCO2	-3 -3		+3 +3	% %
Data Hold Voltage	V_{DR}	OFF-HOOK= V_{DD}, All output pins :No load		V_{DD}	1.0			V
Data Hold Current	I_{DR}	"	a	V_{DD}			0.4	uA

$\longrightarrow V_{DD}$;a=1.0V,b=1.5V,c=2.5V,d=3.5V

LC7355, 7356



C MOS LSI

Pulse Dialer

Ⓔ 1586

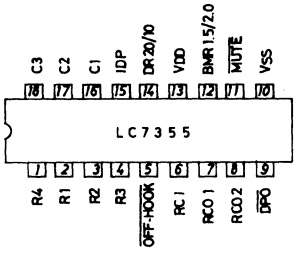
General Description

The LC7355(18-pin package)/LC7356(20-pin package) are redial function-provided pulse dialer C-MOS LSI's for use in pushbutton telephones. (Dial pulse output ($\overline{DPO}$), mute output($\overline{MUTE}$): Open drain type).

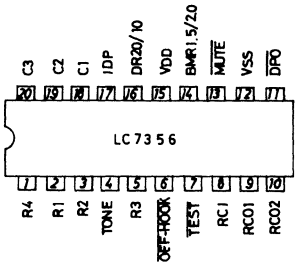
Features

1. Low voltage C-MOS process for direct operation from telephone line.
2. Possible to use single contact or standard 2-of-7 key pad.
3. Contains inexpensive R-C oscillator (f_{OSC}=5kHz typ.).
4. Two selections of output pulse rate (20pps or 10pps).
5. Two selections of output pulse break/make ratio (1.5 or 2).
6. Four selections of inter-digit pause (500/400msec:20pps,1000/800msec:10pps)
7. Redial function (3 digits to 20 digits) available with [#] key.
8. PBX redial function available with access code (2 digits or less).
9. Supply voltage: V_{DD}=1.5 to 3.5V, Operating temperature: Topg=-30 to +70°C.
10. Operating Current: I_{DD}max=100uA/V_{DD}=3.5V,
    20uA/V_{DD}=1.5V.
11. Data hold voltage: $V_{DR} \geq$1.0V, Data hold Current: $I_{DR} \leq$0.4uA(V_{DD}=1.0V)

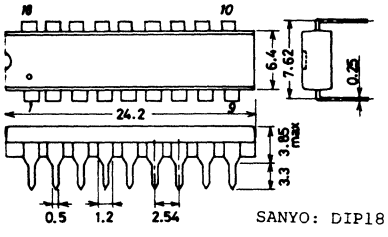
Pin Assignment LC7355



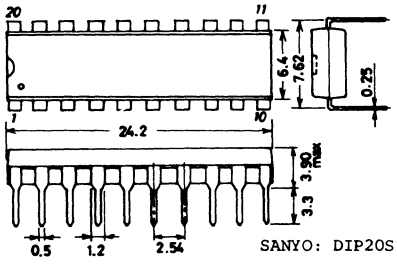
LC7356



Case Outline 3007A-D18IC LC7355
(unit:mm)

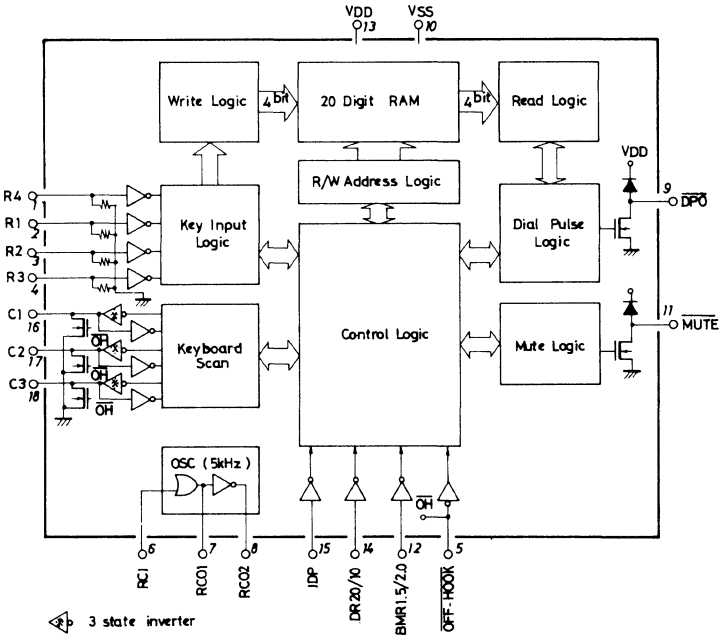


Case Outline 3008A-D20IC LC7356
(unit:mm)

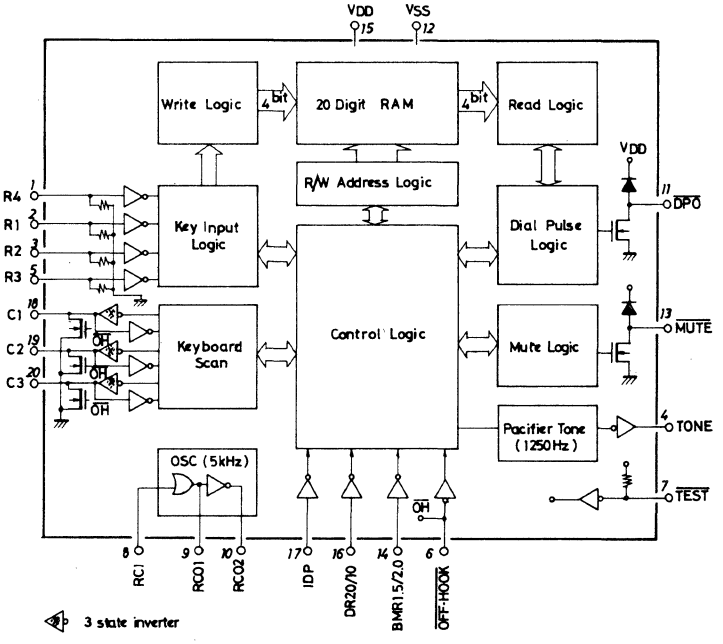


Equivalent Circuit Block Diagram

LC7355



LC7356

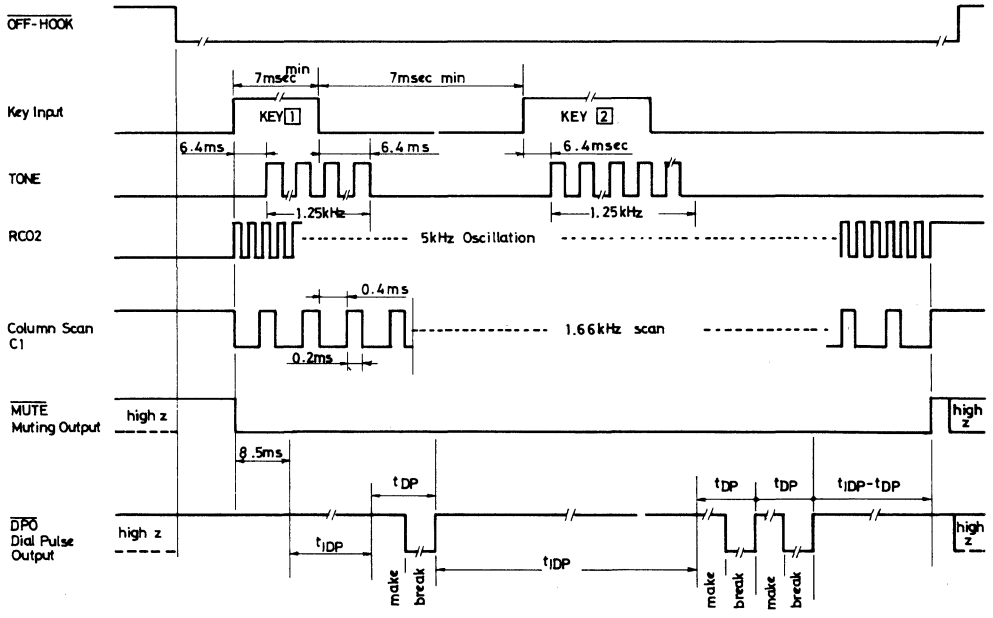


Function Table

(f_{osc}=5KHz)

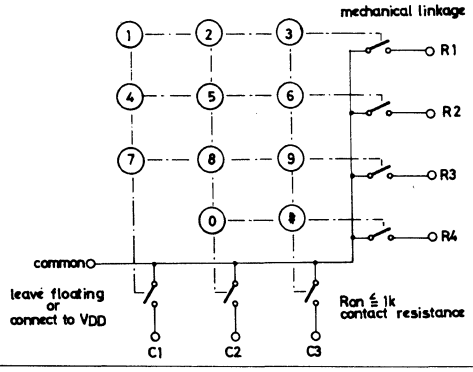
Function	Pin Name	Input Logic Level	Selection	
Dial Pulse Rate	DR20/10	V_{SS}	10PPS (t_{DP}=100ms)	
		V_{DD}	20PPS (t_{DP}=50ms)	
Make Break Ratio	BMR1.5/2	V_{SS}	Make=$33\frac{1}{3}$(%), Break=$66\frac{2}{3}$(%)	
		V_{DD}	Make=40(%), Break=60(%)	
Inter-Digit Pause	IDP		D.P.R=10PPS	D.P.R=20PPS
		V_{SS}	t_{IDP}=800ms	t_{IDP}=400ms
		V_{DD}	t_{IDP}=400ms	t_{IDP}=200ms

Timing

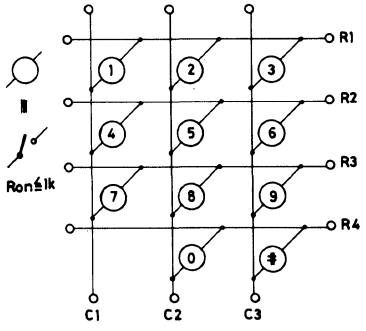


Keyboard Interface

Standard 2 of 7 Keyboard



Single Contact Keyboard



Absolute Maximum Ratings at Ta=25±2°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +5.5	V
Maximum Input Voltage	$V_I$max		-0.3 to +V_{DD}+0.3	V
Maximum Output Voltage	$V_O$max		-0.3 to +V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta=-30 to +70°C	150	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C

			min	typ	max	unit
Supply Voltage	V_{DD}		+1.5		+3.5	V
"H" Level Input Voltage	V_{IH1}	R1,R2,R3,R4,C1,C2,C3	0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{OFF-HOOK}}$,$\overline{\text{TEST}}$	0.8V_{DD}		V_{DD}	V
	V_{IH3}	BMR1.5/2.0,DR20/10,IDP	0.9V_{DD}		V_{DD}	V
"L" Level Input Voltage	V_{IL1}	R1,R2,R3,R4,C1,C2,C3	V_{SS}		0.3V_{DD}	V
	V_{IL2}	$\overline{\text{OFF-HOOK}}$,$\overline{\text{TEST}}$	V_{SS}		0.2V_{DD}	V
	V_{IL3}	BMR1.5/2.0,DR20/10,IDP	V_{SS}		0.1V_{DD}	V
Oscillation Guaranteed External Constants	R_O	RCI	176	300 or 220	360	kohm
	C_O	RCO1	243	270 or 360	396	pF
	R_I	RCO2	675	820 or 1200	1650	kohm
Oscillation Frequency	f_{OSC}	RCO2		5.0		kHz
Key Contant Resistance	R_{KI}				1.0	kohm
Keyboard Capacitance	C_{KI}				50	pF

Electrical Characteristics at Ta=25±2°C, V_{SS}=0V, V_{DD}=See a, b, c, d defined below.

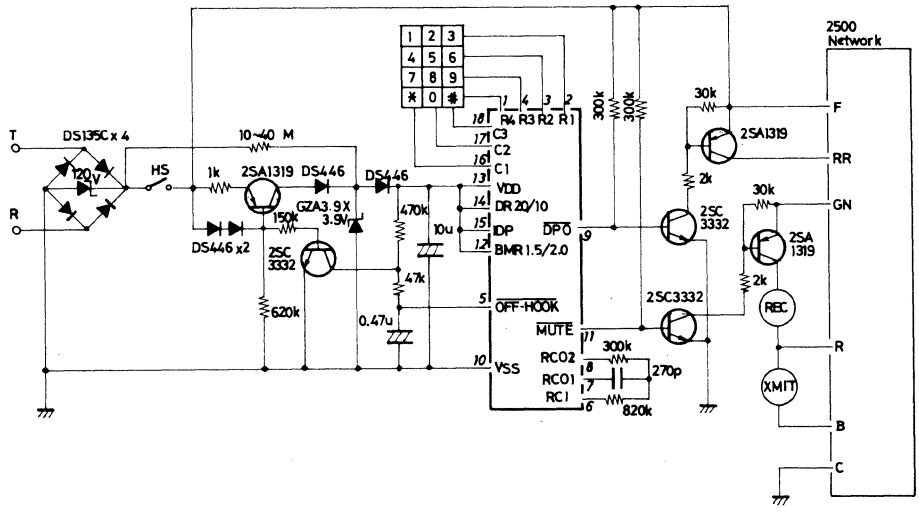
					min	typ	max	unit
"H" Level Input Current	I_{IH1}	V_{IN}=V_{DD},	atob	$\overline{\text{OFF-HOOK}}$,RCI, BMR1.5/2.0,IDP DR20/10			1.0	uA
	I_{IH2}	V_{IN}=V_{DD},	b	R1,R2,R3,R4	3.0			uA
		"	d	"			60	uA
	I_{IH3}	V_{IN}=V_{DD},	b	C1,C2,C3	3.0			uA
		$\overline{\text{OFF-HOOK}}$=$V_{DD}$	d	"			30	uA
"L" Level Input Current	I_{IL1}	V_{IN}=V_{SS},	btod	$\overline{\text{OFF-HOOK}}$,RCI, DR20/10, BMR1.5/2.0,IDP	-1.0			uA
	I_{IL2}	V_{IN}=V_{SS},	b	$\overline{\text{TEST}}$			-3.0	uA
		"	d	"	-140			uA
"L" Level Input Floating Voltage	V_{IFL}	Input pin open,	btod	R1,R2,R3,R4	V_{SS}	0.3V_{DD}	-0.3	V
"H" Level Output Voltage	V_{OH1}	I_{OH}=20uA	b	TONE	V_{DD}-0.5			V
		I_{OH}=125uA	d	"	V_{DD}-1.0			V
Output Off-leak Current	I_{OFF}	Output tr. OFF, Vo=V_{SS}toV_{DD},	btod	$\overline{\text{DPO}}$,$\overline{\text{MUTE}}$			1.0	uA
"L" Level Output Voltage	V_{OL1}	I_{OL}=20uA	b	$\overline{\text{DPO}}$,$\overline{\text{MUTE}}$			0.4	V
		I_{OL}=125uA	d	"			0.4	V
	V_{OL2}	I_{OL}=20uA	b	TONE			0.4	V
		I_{OL}=125uA	d	"			0.4	V

					min	typ	max	unit
Operating Current	I_{DD1}	DR=10pps, All output pins:No load	b	V_{DD}			20	uA
			d	"			100	uA
Quiescent Current	I_{DD2}	$\overline{\text{OFF-HOOK}}$= V_{DD},All output pins :No load	btod	V_{DD}		0.1	1.0	uA
Frequency Deviation	$\triangle f_o / f_o$	(kohm/pF) btoc		RCI,RCO1,RCO2	-3		+3	%
		R_o 300 220 ctod		"	-3		+3	%
		C_o 270 360						
		R_I 820 1200						
Data Hold Voltage	V_{DR}	$\overline{\text{OFF-HOOK}}$= V_{DD},All output pins :No load		V_{DD}	1.0			V
Data Hold Current	I_{DR}	"	a	V_{DD}			0.4	uA

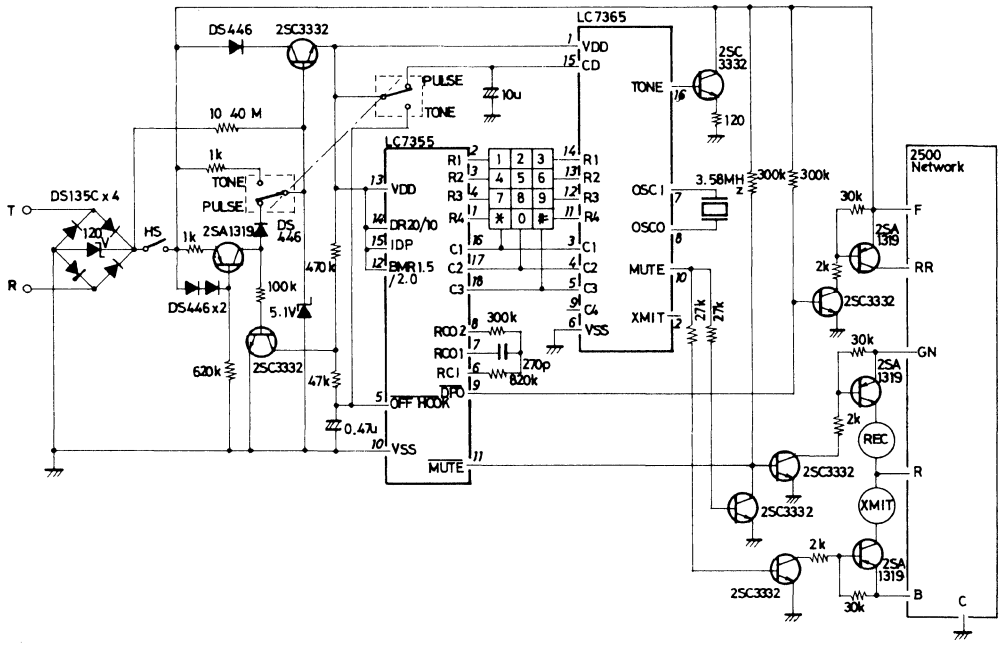
↳ V_{DD};a=1.0V,b=1.5V,c=2.5V,d=3.5V

Sample Application Circuit 1.

(Note) The LC7356 differes in pin assignment.



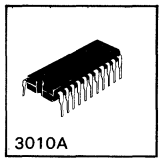
Sample Application Circuit 2. Tone-Pulse Switchable Application



(Note) The LC7356 differs in pin assignment.

- The circuit constants are not intended for a design for the mass production where the error or temperature characteristic of parts must be considered.
- No responsibility is assumed by us for any patents on the Application Circuits.

LC7360



C MOS LSI

Tone/Pulse Switchable Dialer

TENTATIVE

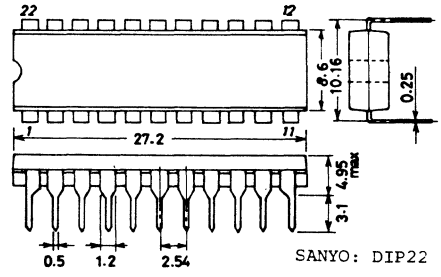
General Description

The LC7360 (22-pin package) is a DTMF/OUT-PULSE dialer C-MOS LSI with redial function for use in pushbutton telephones.

Features

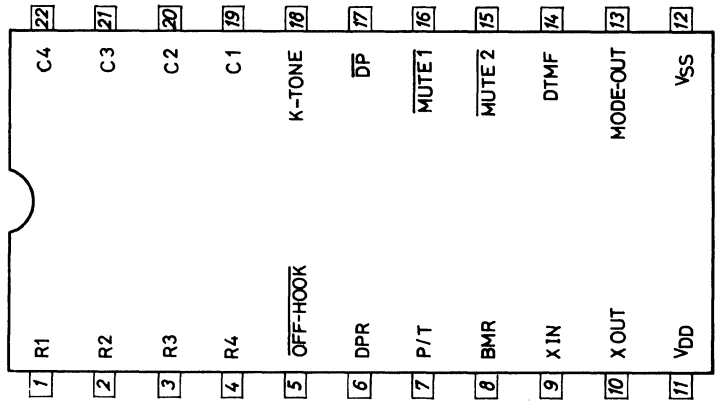
(1) Low voltage C-MOS process for direct operation from telephone line.
(2) Possible to use single contact or standard 2-of-7, 2-of-8 key pad.
(3) Possible to use color-burst crystal resonator for on-chip oscillator (f_{OSC}=3.58MHz).
(4) Possible to use either mode select pin (P/T) or function key (4 x 4 matrix key) to select DTMF mode/OUT-PULSE mode.
(5) Delivers 12 DTMF signals when in DTMF mode.
(6) On-chip 31-digit redial memory.
(7) Possible to provide mix redial (31 digits-PULSE-MC) of DTMF/OUT-PULSE modes.
(8) Either auto pause select (4 sec. x N) or manual release available for mode select standby time during redial operation.
(9) Output pulse make rate of OUT-PULSE mode pin-selectable (33-1/3% or 40%).
(10) Output pulse rate of OUT-PULSE mode pin-selectable (10pps or 20pps).
(11) On-chip circuit to prevent malfunction due to noise pulse caused by key entry.
(12) Key touch tone (pacifier tone) output capability.
DTMF mode : 1250Hz
OUT-PULSE mode : 625Hz
(13) Supply voltage/operating temperature
DTMF mode : V_{DD}=2.5V to 5.5V/Ta=-20°C to +70°C
OUT-PULSE mode : V_{DD}=2.0V to 5.5V/Ta=-20°C to +70°C
(14) Operating current
DTMF mode : $I_{DD(max.)}$=2.0mA at V_{DD}=3.5V
OUT-PULSE mode : $I_{DD(max.)}$=500uA at V_{DD}=3.5V
(15) Data hold voltage/data hold current
$V_{DR} \geq 1.5V / I_{DR} \geq 0.4uA$ (V_{DD}=1.5V)

Case Outline 3010A-D22IC
(unit:mm)



SANYO: DIP22

Pin Assignment



Key Assignment

1	2	3	F	R1
4	5	6	P	R2
7	8	9	RD	R3
*	0	#	MC	R4
C1	C2	C3	C4	

F : Flash

P : Pause

RD : Redial, pause release

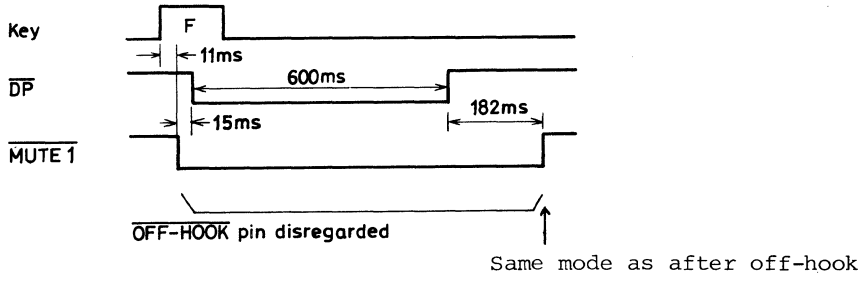
MC : Pulse ⟷ tone select

When in OUT-PULSE mode

* = P

= RD

Timing of flash



. OUT-PULSE/DTMF mode

Pin Name	Input level	Mode
P/T	V_{DD}	OUT-PULSE
	V_{SS}	DTMF

. Dial pulse output

Pin Name	Input level	Dial pulse rate	Interdigit pause	Make rate
DPR	V_{DD}	20PPS	500ms	
	V_{SS}	10PPS	800ms	
BMR	V_{DD}			33-1/3%
	V_{SS}			40%

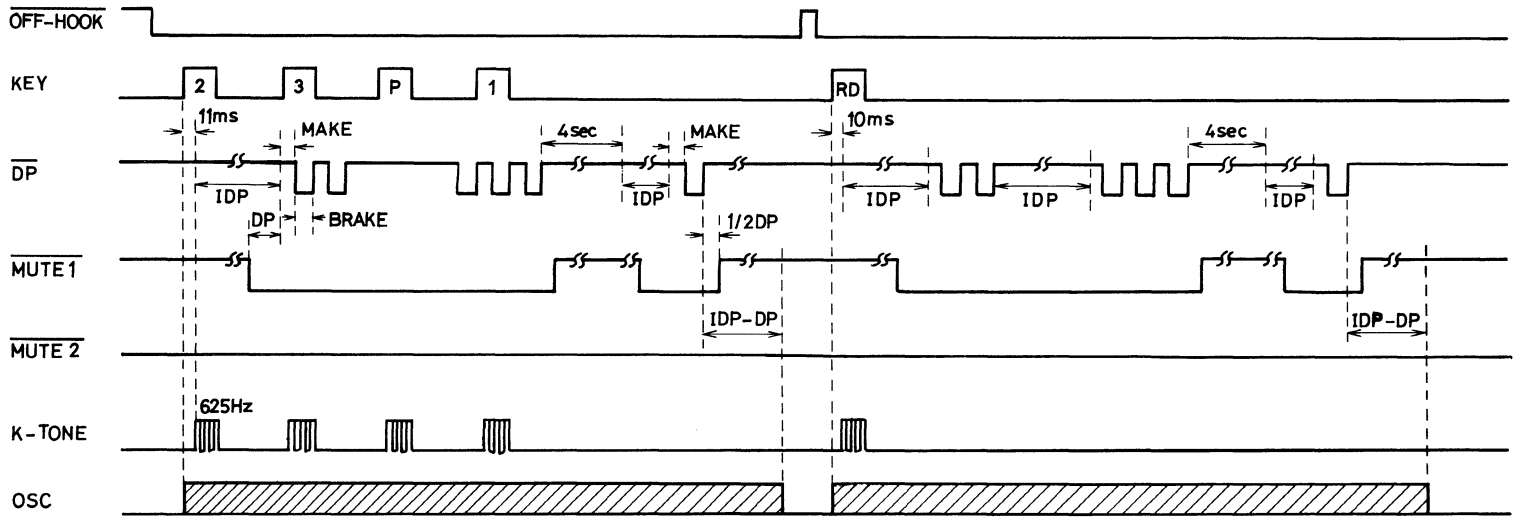
. DTMF Output

Input	Output frequency (Hz)		Deviation (%)
	Standard	LC7360	
R1	697	699.1	+0.30
R2	770	766.2	-0.49
R3	852	847.4	-0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	-0.32
C3	1477	1471.9	-0.35

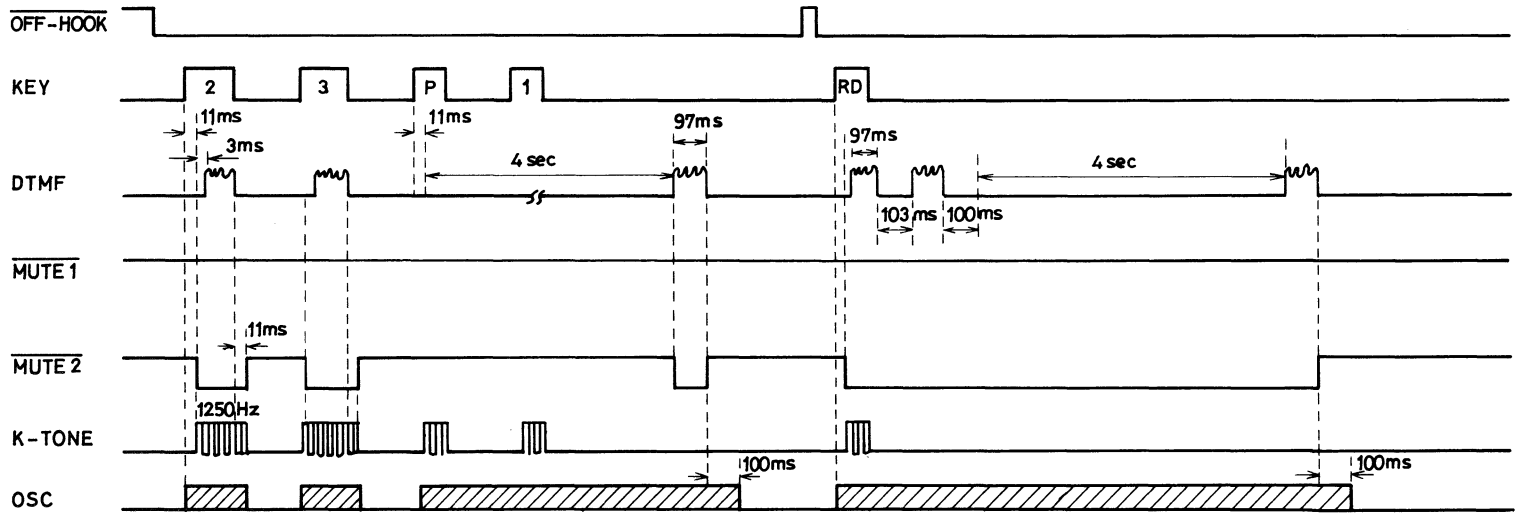
Redial operation

Parameter	Time
DTMF output	97ms
Interdigit pause	103ms
Period	200ms

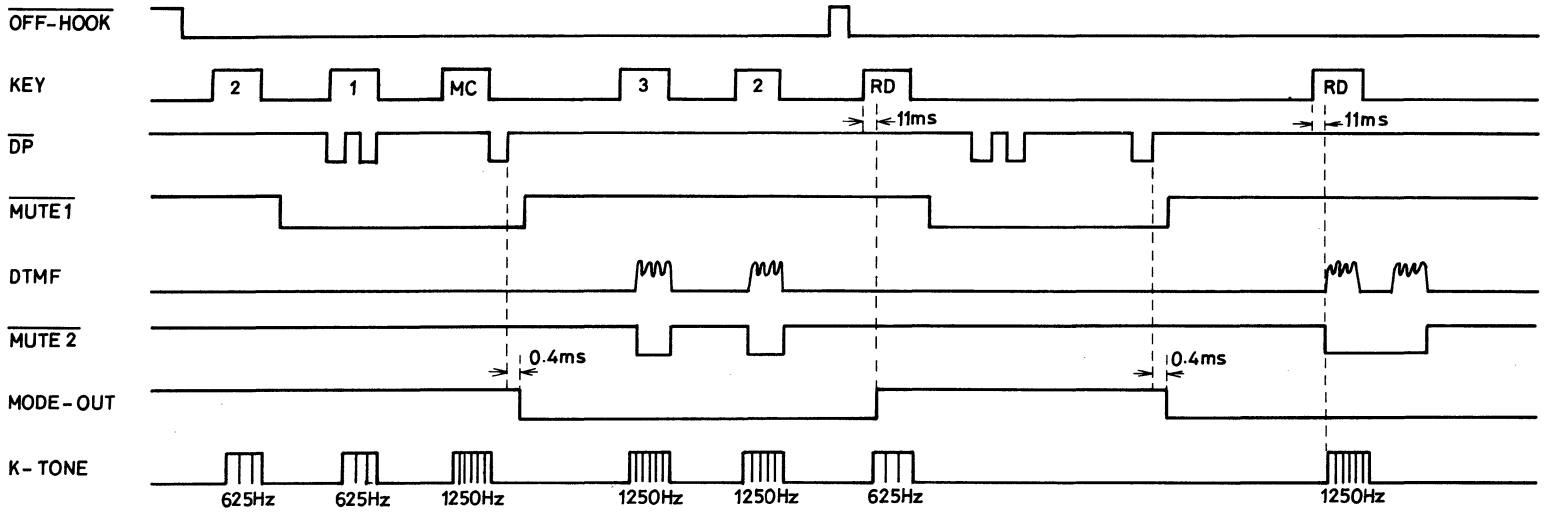
(1) OUT-PULSE



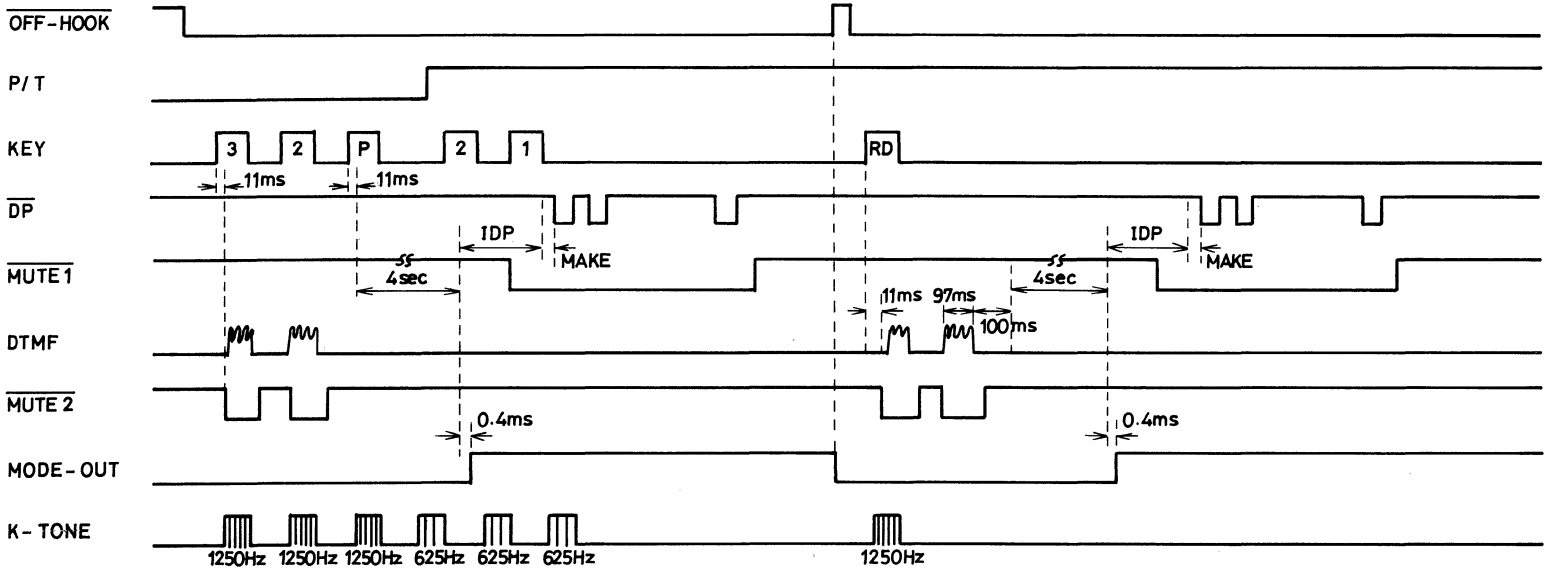
(2) Tone mode



(3) Pulse tone mix (P/T="H")



(4) Tone↔pulse mix



Key operation

1. Normal dial

   Off-hook ⟶ [D1] [D2] ------ [Dn]

   Redial

   Off-hook ⟶ [RD]

2. PBX dial

   Off-hook ⟶ [D0] [P] [D1] [D2] ------ [Dn]

   Redial

   Off-hook ⟶ [RD]

3. Pulse/tone mix

   (1) In case where there is no pause during mode select

   Off-hook ⟶ [D1] [D2] [MC] [D3] [D4] [MC] [D5] [D6] (P/T="H")
   Pulse Tone Pulse

   Redial

   Off-hook ⟶ [RD] D1,D2 [RD] D3,D4 [RD] D5,D6
   Pulse Tone Pulse

   (2) In case where there are pauses during mode select

   Off-hook ⟶ [D1] [D2] [P] [MC] [D3] [D4] [MC] [P] [D5] [D6] (P/T="L")
   Tone Pulse Tone

   Redial

   Off-hook ⟶ [RD] D1,D2 4sec. D3,D4 4sec. D5,D6
   Tone Pulse Tone

(Note)

(1) When in OUT-PULSE mode

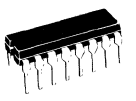
   [P] = [*] [RD] = [#]

(2) Pause: 4 sec./1 push of P, 8 sec./2 pushes of [P], 4 x n sec./n pushes of P

(3) For pause release, push RD. All pauses can be also released by pushing [RD] once.

(4) When selecting pulse mode/DTMF mode, do not use both P/T pin and [MC] key in combination during off-hook.
In applications where both pulse mode and DTMF mode are used, it is desirable that only P/T pin or [MC] key should be used for mode select.

LC7365, 7366


3006A

C MOS LSI

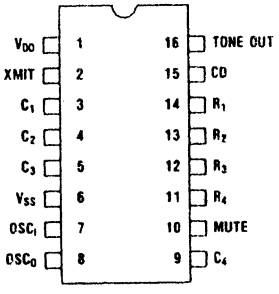
Tone Dialer

TENTATIVE

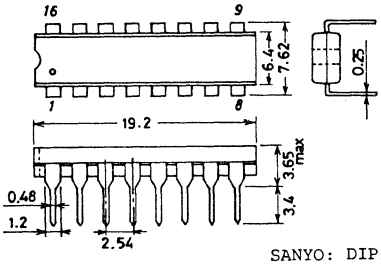
Features

(1) Wide Operating Supply Voltage Range : 2.5 to 10 Volts
(2) Can be Powered Directly from Telephone Line or from Small Batteries.
(3) Use TV Crystal standard (3.58MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability.
(4) Mute and XMIT Drivers On Chip.
(5) Interfaces Directly to a Standard Telephone Push-Botton or Calculator Type X-Y Keyboard.
(6) Low Output Tone Distortion : 7% Max.
(7) Oscillator Bias Resistor and Capacitancies On Chip.
(8) On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range.
(9) Dual tone as well as Single Tone Capability.
(10) Operating Temperature : $-30^{o}C$ to $+70^{o}C$
(11) Operating Current : $I_{DD(max)}$=3mA(V_{DD}=2.5V), 16mA(V_{DD}=10.0V)
(12) Standby Current : $I_{DD(typ)}$=0.3uA(V_{DD}=2.5V), 1uA(V_{DD}=10.0V)
(13) The LC7366 can be interfaced direct to C/MOS logic output.

Pin Assignment



Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Absolute Maximum Ratings at Ta=25°C±2°C, V_{SS}=0V

Characteristic	Symbol	Conditions	Limits min	Limits typ	Limits max	unit	Comment
Supply Voltage	V_{DD}		-0.3		11	V	
Input Voltage	V_I		V_{SS}-0.3		V_{DD}+0.3	V	
Allowable Power Dissipation	Pd	Ta=70°C			450	mW	
Operating Temperature	Topg		-30		70	°C	
Storage Temperature	Tstg		-40		125	°C	

Allowable Operating Ranges at Ta=-30°C to +70°C, V_{SS}=0V

Characteristic	Symbol	Conditions	Limits min	Limits typ	Limits max	unit	Comment
Supply Voltage	V_{DD}	Tone out Mode (Valid Key Depressed)	2.5		10.0	V	
		Non Tone out Mode (No Key Depressed)	1.6		10.0	V	
High-Level Input Voltage	V_{IH}		0.7V_{DD}		V_{DD}	V	
Low-Level Input Voltage	V_{IL}		V_{SS}		0.3V_{DD}	V	
Key Contact Resistance	R_{KI}				1.0	kohm	
Crystal Specification	f	3.579545MHz±0.02%					
	R_S	<100ohm					
	LM	96mH					
	CM	0.02pF					
	CH	5pF					

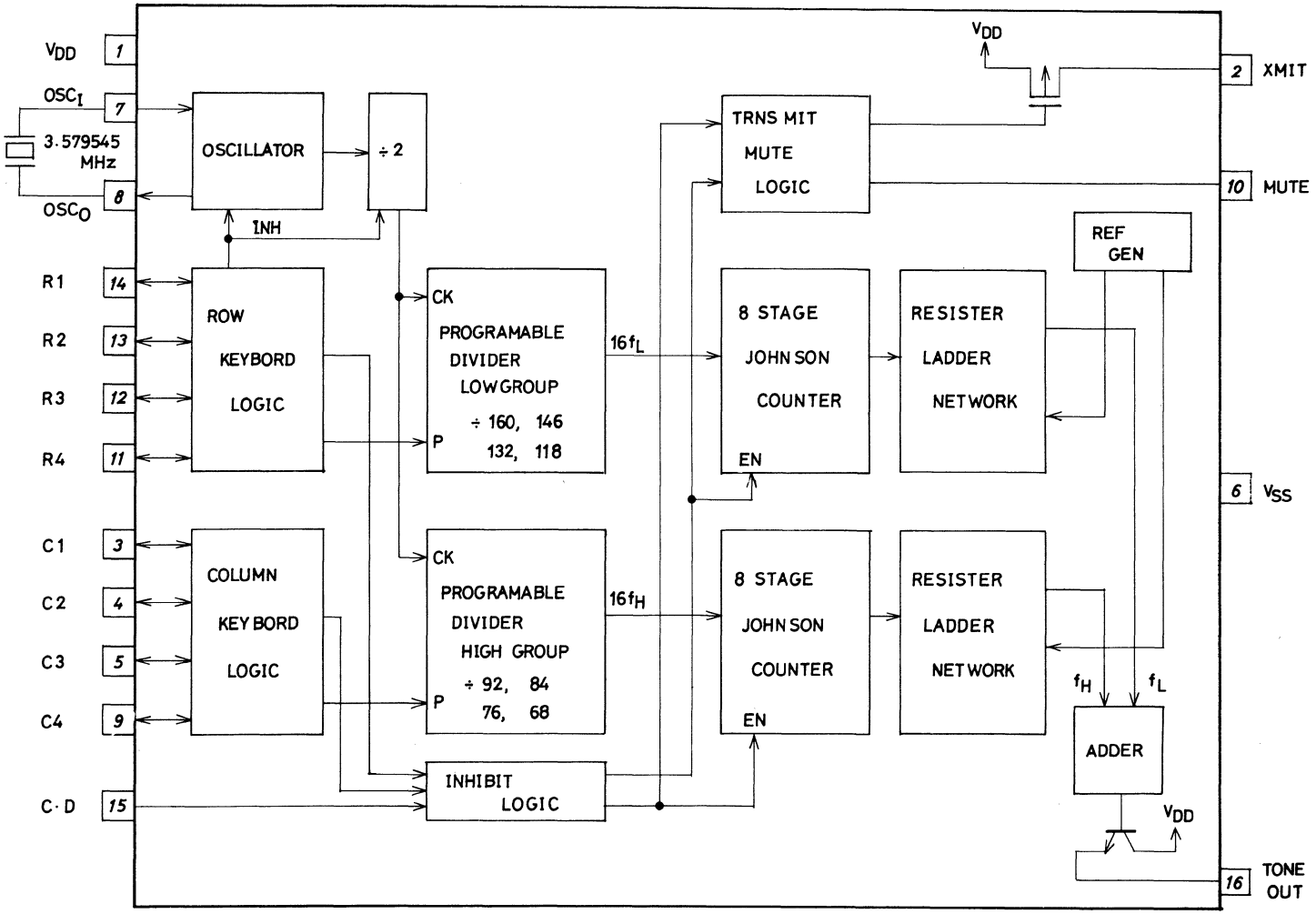
Electrical Characteristics at Ta=25°C±2°C, V_{SS}=0V

Characteristic	Symbol	Conditions	V_{DD} (V)	Limits min	Limits typ	Limits max	unit	Comment
Operating Current	$I_{DD(1)}$	One Key Selected, Tone, XMIT, and MUTE Output Unloaded	2.5		1.5	3.0	mA	V_{DD} Pin
			10.0		8	16	mA	

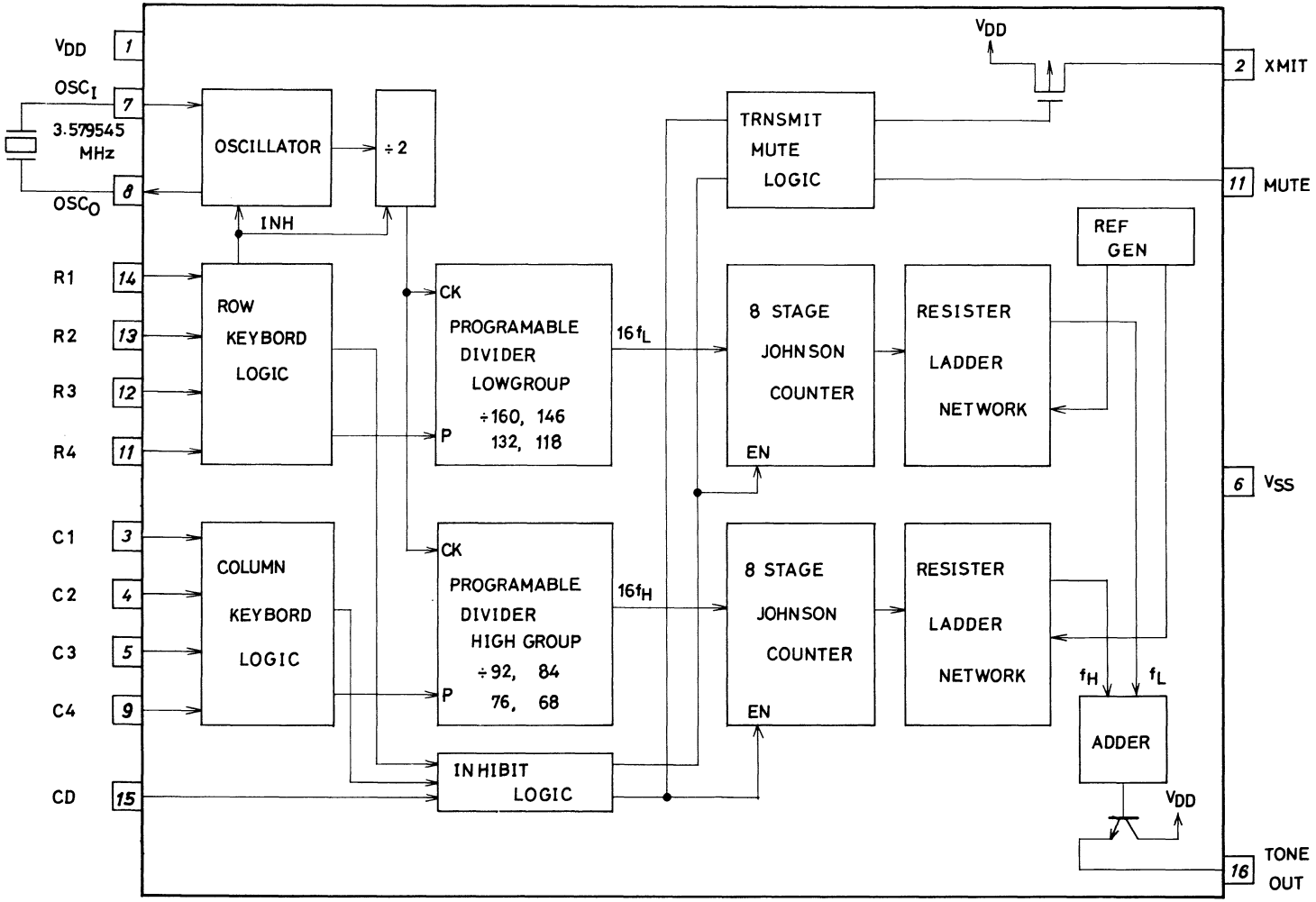
Characteristic	Symbol	Conditions	V_{DD} (V)	Limits min	typ	max	unit	Comment
Quiescent Current	$I_{DD(2)}$	One Key Selected, Tone, XMIT, and MUTE Output Unloaded	2.5		0.3	30	uA	V_{DD} Pin
			10.0		1.0	100	uA	
Single Tone Mode Output Voltage	V_{OR}	Row Tone R_L=390ohm	2.5	135	200	270	mV	Tone out Pin
		R_L=390ohm	5.0	150	220	300	mV	
		R_L=240ohm	10.0	150	220	300	mV	
Ratio of Column to Row Tone	dB_{CR}	Dual Tone Mode	2.5	1.0	2.0	3.0	dB	
			10.0					
Distortion	%DIS		2.5			7	%	
			10.0					
XMIT, Output Voltage High	V_{OH}	No Key Depressed I_{OH}=5mA	2.5	1.5	1.8		V	XMIT Pin
		I_{OH}=50mA	10.0	8.5	8.8			
XMIT, Output Source Leakage Current	I_{OF}	V_{OF}=0V	10.0			100	uA	XMIT Pin
MUTE, Output Voltage Low	V_{OL}	No Key Depressed No Load	2.5		0	0.5	V	MUTE Pin
			10.0		0	0.5		
MUTE, Output Voltage High	V_{OH}	No Key Depressed No Load	2.5	2.25	2.50		V	MUTE Pin
			10.0	9.5	10.0			
MUTE, Output Sink Current	I_{OL}	V_{OL}=0.5V	2.5	0.4	1.0		mA	MUTE Pin
			10.0	2.0	5.3			
MUTE, Output Source Current	I_{OH}	V_{OH}=2.0V	2.5	0.17	0.41		mA	MUTE Pin
		V_{OH}=9.5V	10.0	0.57	1.5			
OSC_O, Output Sink Current	I_{OL}	One Key Selected V_{OL}=0.5V	2.5	0.18	0.40		mA	OSC_O Pin
		V_{OL}=0.5V	10.0	0.80	2.1			
OSC_O, Output Source Current	I_{OH}	One Key Selected V_{OH}=2.0V	2.5	0.13	0.31		mA	OSC_O Pin
		V_{OH}=9.5V	10.0	0.42	1.1			
Oscillator Startup Time	t_{START}		2.5		2	5	ms	
			10.0		0.25	4		
Input/Output Capacitance	$C_{I/O}$		2.5		12	16	pF	OSC_O,OSC_I Pin
			10.0		10	14		
Row & Column Inputs Current	I_{IH}	V_{IH}=2.5V	2.5	4	10		uA	C1~C4, R1~R4 Pin LC7365 only
		V_{IH}=10.0V	10.0	9.2	24			
	I_{OH}	V_{OH}=2.0V	2.5	70	170		uA	
		V_{OH}=9.5V	10.0	280	740			

Characteristic	Symbol	Conditions	V_{DD} (V)	Limits min	typ	max	unit	Comment
Row & Colum Input Leakage Current	I_{IHOF}	V_{IH}=2.5V	2.5			1	uA	C1~C4, R1~R4 Pin LC7366 only
		V_{IH}=10.0V	10.0			2	uA	
	I_{ILOF}	V_{IL}=0V	2.5			1	uA	
		V_{IL}=0V	10.0			2	uA	
Chip Disable Input Current	I_{IH}	V_{IH}=2.5V	2.5	2.5	7.5		uA	CD Pin
		V_{IH}=10.0V	10.0	55	143			
Oscillator Frequency	f_{OSC}		2.5 ~10.0	3.579545∓0.26%			MHz	OSC_O,OSC_I Pin

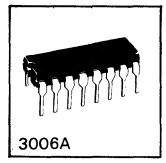
LC7365 Block Diagram



LC7366 Block Diagram



LC7450



C MOS LSI

PLL RF Modulator for CATV

Ⓔ 1481A

Applications

CATV converter, VTR video and audio carrier generator

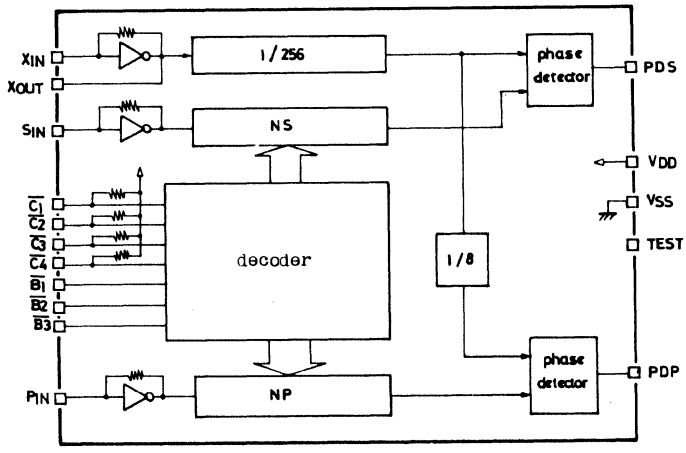
Functions

(1) Video carrier
U.S.A. : 2ch to 13ch, Ach to Hch, with 1/8 prescaler
Japan : 1ch to 12ch, with 1/8 prescaler
Europe : 30ch to 45ch, with 1/64 prescaler

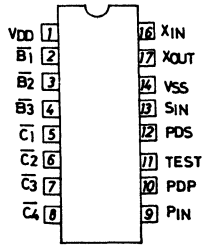
(2) Audio carrier
U.S.A., Japan : 4.5MHz
Europe (1) : 5.5MHz
(2) : 6.0MHz
(3) : 6.5MHz

(3) 8.0MHz oscillator on chip

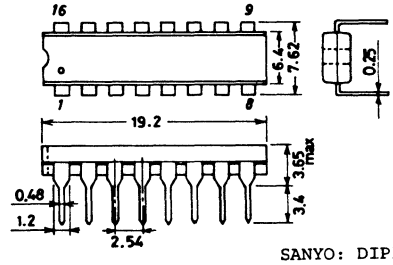
Equivalent Circuit Block Diagram



Pin Assignment



Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	$V_{DD}max$		-0.3 to +9.0	V
Maximum Input Voltage	V_{IN}	Input pin	-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax	Ta≦75°C	250	mW
Operating Temperature	Topg		-30 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		8.5	V
Input "H" Level Voltage	V_{IH}	$\overline{C1}$~$\overline{C4}$, $\overline{B1}$~$\overline{B3}$	0.8V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}	$\overline{C1}$~$\overline{C4}$, $\overline{B1}$~$\overline{B3}$	0		0.2V_{DD}	V
Input Frequency	$f_{IN(1)}$	P_{IN}, V_{IN}=0.7Vp-p	2.0		18	MHz
"	$f_{IN(2)}$	P_{IN}, V_{IN}=1.5Vp-p, V_{DD}≧7.5V	2.0		30	MHz
"	$f_{IN(3)}$	S_{IN}, V_{IN}=0.7Vp-p	0.5		8.0	MHz
"	$f_{IN(4)}$	X_{IN}, V_{IN}=2.0Vp-p	0.5		9.0	MHz
Input Amplitude	$V_{IN(1)}$	P_{IN}, f_{IN}=2.0~18MHz	0.7		0.9V_{DD}	Vp-p
	$V_{IN(2)}$	P_{IN}, f_{In}=2.0~30MHz, V_{DD}≧7.5V	1.5		0.9V_{DD}	Vp-p
	$V_{IN(3)}$	S_{IN}, f_{IN}=0.5~8.0MHz		0.7	0.9V_{DD}	Vp
	$V_{IN(4)}$	X_{IN}, f_{IN}=0.5~0.9MHz	2.0		0.9V_{DD}	Vp-p

Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Input H/L Level Current	$I_{IH}(1)$/ $I_{IL}(1)$	X_{IN}, V_I=V_{DD}/V_{SS}			50	uA
"	$I_{IH}(2)$/ $I_{IL}(2)$	P_{IN}, S_{IN}, V_I=V_{DD}/V_{SS}			100	uA
"	$I_{IH}(3)$/ $I_{IL}(3)$	$\overline{B1}$~$\overline{B3}$, V_I=V_{DD}/V_{SS}			5.0	uA
Input "L" Level Current	$I_{IL}(4)$	$\overline{C1}$~$\overline{C4}$, V_I=V_{SS}	15		300	uA
Input Floating Voltage	V_{IF}	$\overline{C1}$~$\overline{C4}$, V_I=Open	0.9V_{DD}		V_{DD}	V
Feedback Resistance	Rf(1)	X_{IN}, V_{DD}=6.5V		1.0		Mohm
"	Rf(2)	P_{IN}, S_{IN}, V_{DD}=6.5V		0.5		Mohm
Output "H" Level Voltage	V_{OH}	PDP, PDS I_O=0.3mA	V_{DD}-1.0		V_{DD}	V
Output "L" Level Voltage	V_{OL}	PDP, PDS "	0		1.0	V
Output Off-leakage Current	I_{OFF}	PDP, PDS V_O=V_{DD}/V_{SS}		0.01	1.0	nA
Supply Current	I_{DD}	(Note)			20	mA

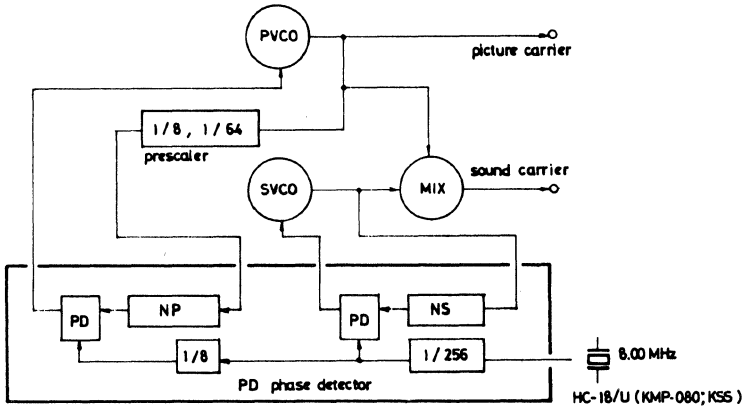
(Note) V_{DD}=8.5V, P_{IN}=30MHz, S_{IN}=8.0MHz
X_{IN}, X_{OUT}=8.0MHz Crystal resonator connected
$\overline{B1}$~$\overline{B3}$=V_{DD} Other pins : open

Frequency Division Table

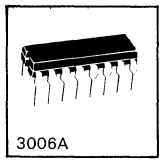
				$\overline{B1}$		1		0		1		0	1
				$\overline{B2}$		1		1		0		0	1
				$\overline{B3}$		1		1		1		1	0
				fsVCO(MHz),NS		4.5, 144		4.5, 144		5.5, 176		6.0, 192	6.5, 208
				PVCO prescaler		1/8		1/8		1/64			
$\overline{C1}$	$\overline{C2}$	$\overline{C3}$	$\overline{C4}$	fPVCO,NP	fPVCO·MHz	NP	fPVCO·MHz	NP	fPVCO·MHz	NP			
1	1	1	1		55·25	1768	91.25	2920	543.25	2173			
0	1	1	1		61.25	1960	97.25	3112	551.25	2205			
1	0	1	1		67.25	2152	103.25	3304	559.25	2237			
0	0	1	1		77.25	2472	171.25	5480	567.25	2269			
1	1	0	1		83.25	2664	177.25	5672	575.25	2301			
0	1	0	1		175.25	5608	183.25	5864	583.25	2333			
1	0	0	1		181.25	5800	189.25	6056	591.25	2365			
0	0	0	1		187.25	5992	193.25	6184	599.25	2397			
1	1	1	0		193.25	6184	199.25	6376	607.25	2429			
0	1	1	0		199.25	6376	205.25	6568	615.25	2461			
1	0	1	0		205.25	6568	211.25	6760	623.25	2493			
0	0	1	0		211.25	6760	217.25	6952	631.25	2525			
1	1	0	0		121.25(A)	3880	145.25(E)	4648	639.25	2557			
0	1	0	0		127.25(B)	4072	151.25(F)	4840	647.25	2589			
1	0	0	0		133.25(C)	4264	157.25(G)	5032	655.25	2621			
0	0	0	0		139.25(D)	4456	163.25(H)	5224	663.25	2653			

f refS=31.25kHz

f refP=3.90625kHz



LC7460



C MOS IC

Remote Control Transmission

Ⓔ 1562

Functions and Features

- Eight functions selectable by 8 switches
- Generates a pulse-train remote control signal corresponding to each function switch.
- On-chip oscillator (ceramic resonator, capacitor: connected externally)
- Operating voltage: V_{DD}=2.0 to 3.6V (Ta=-10 to +75°C)
- Current dissipation: Operating mode ---- I_{DD}(max)=1.0mA
  Standby mode ------ I_{DD}(max)=1.0uA

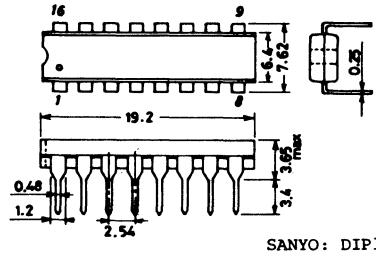
Absolute Maximum Ratings at Ta=25±2°C

				unit
Maximum Supply Voltage	V_{DD} max		-0.3 to +6	V
Input Voltage	V_I		-0.3 to V_{DD}+0.3	
Output Voltage	V_O		-0.3 to V_{DD}+0.3	V
Output Current	I_O	OUT1	20	mA
Allowable Power Dissipation	Pd max	Ta≦75°C	150	mW
Operating Temperature	T_{opg}		-10 to +75	°C
Storage Temperature	T_{stg}		-40 to +125	°C

Allowable Operating Ranges at Ta=-10 to +75°C, V_{SS}=0V

		Pin Name		min	typ	max	unit
Supply Voltage	V_{DD}			2.0	3.0	3.6	V
Input "H"-Level Voltage	V_{IH}	$\overline{K1}$ to $\overline{K8}$		0.8V_{DD}		V_{DD}	V
Input "L"-Level Voltage	V_{IL}	$\overline{K1}$ to $\overline{K8}$		V_{SS}		0.2V_{DD}	V
Oscillating Frequency	f_{osc}	OSC_{IN}, OSC_{OUT}	: Ta=25±2°C C_i=C_o=100pF Ceramic resonator	400	540	600	KHz
External Capacitor Value for Delay	C	C			1.0		uF
External Capacitor Value for Oscillation	ci	OSC_{IN}	Ceramic resonator CSB540E(Murata) or KBR540B(Kyocera)		100		pF
	c_o	OSC_{OUT}	Ceramic resonator CSB540E(Murata) or KBR540B(Kyocera)		100		pF

Case Outline 3006A-D16IC
(unit;mm)



SANYO: DIP16

Electrical Characteristics at Ta=25±2°C, V_{SS}=0V

		Pin Name		min	typ	max	unit
Input Floating Voltage	V_{IF}	$\overline{K1}$ to $\overline{K8}$	V_{DD}=2.0 to 3.6V input pin open	0.8V_{DD} +0.2		V_{DD}	V
Input "L"-Level Current	I_{IL}	$\overline{K1}$ to $\overline{K8}$	V_{DD}=3V, V_{IN}=V_{SS}	-60		-15	uA
Output "H"-Level Voltage	V_{OH}(1)	OUT1	V_{DD}=3V, I_{OH}=-10mA	V_{DD}-2.0		V_{DD}	V
	V_{OH}(2)	OUT2	V_{DD}=3V, I_{OH}=-0.5mA	V_{DD}-1.0		V_{DD}	V
Output "L"-Level Voltage	V_{OL}(1)	OUT1	V_{DD}=3V, I_{OL}=0.1mA			0.4	V
	V_{OL}(2)	OUT2	V_{DD}=3V, I_{OL}=0.1mA			0.4	V
Oscillation Signal Division Delay Time	t_D(DIV)	C, OUT2	V_{DD}=3V, C=1.0uF		13		ms
Oscillation Start Time	t_{st}(osc)	OSC_{IN} OSC_{OUT}	V_{DD}=3V, c_i=c_o=100pF CF:CSB540E(Murata) or KBR540B(Kyocera)		1.0		ms
Oscillation Frequency Variation with Supply Voltage	Δf_V	OSC_{IN} OSC_{OUT}	V_{DD}=2 to 4.5V, c_i=c_o=100pF CF:CSB540E(Murata) or KBR540B(Kyocera) CF:540B(Murata)			±0.2	%
Current Dissipation	I_{DD}(1)	V_{DD}	V_{DD}=3V, Fig. 1			1.0	mA
Quiescent Current	I_{DD}(2)	V_{DD}	V_{DD}=2 to 3V, Fig.2			1.0uA	

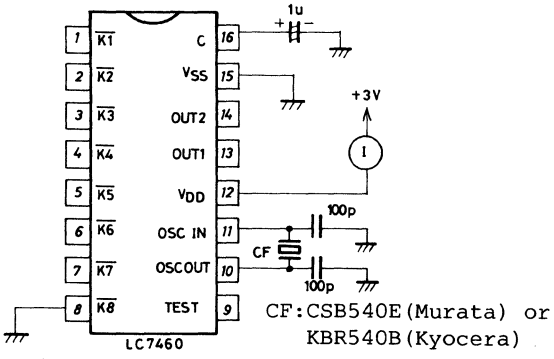


Fig. 1 Current Dissipation Test Circuit

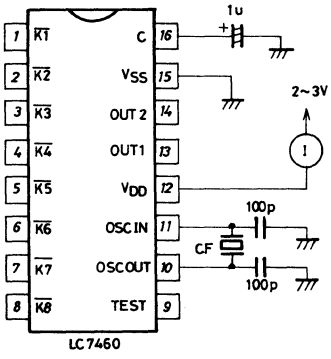
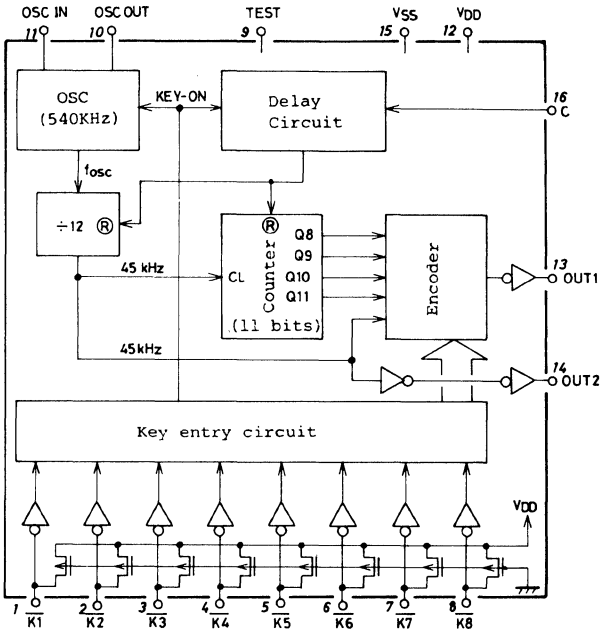


Fig. 2 Quiescent Current Test Circuit

Pin Connection and Pin Assignment

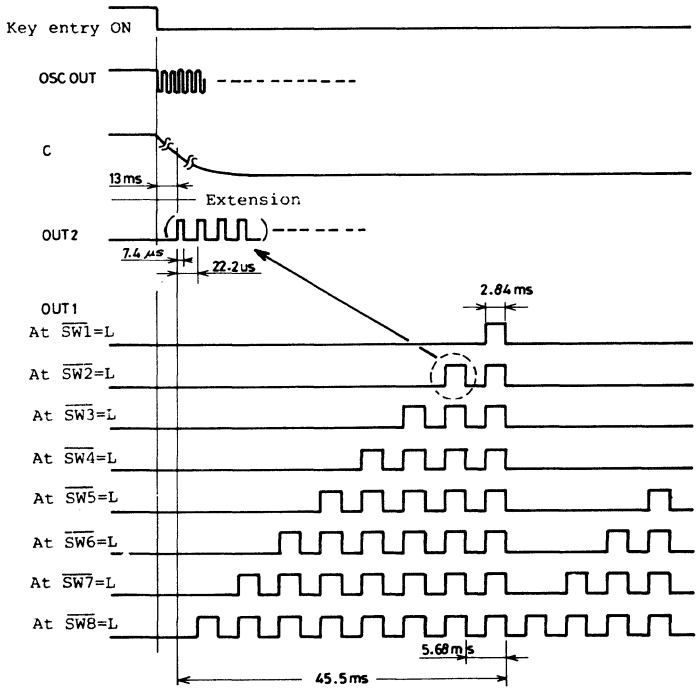
Pin No.	Pin Name	Input/Output	Pin No.	Pin Name	Input/Output
1	$\overline{K1}$	Input	9	TEST	Output
2	$\overline{K2}$	Input	10	OSC_{OUT}	Input/Output
3	$\overline{K3}$	Input	11	OSC_{IN}	Input/Output
4	$\overline{K4}$	Input	12	V_{DD}	-
5	$\overline{K5}$	Input	13	OUT1	Output
6	$\overline{K6}$	Input	14	OUT2	Output
7	$\overline{K7}$	Input	15	V_{SS}	-
8	$\overline{K8}$	Input	16	C	Input/Output

Equivalent Circuit Block Diagram



Timing Chart

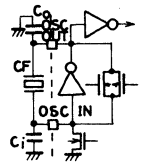
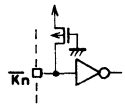
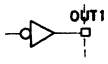
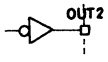
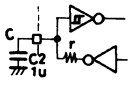
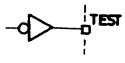
(OSC frequency 540kHz)



Note: Priority order of $\overline{SWn}$ input

$\overline{SW8} > \overline{SW7} > \overline{SW6} > \overline{SW5} > \overline{SW4} > \overline{SW3} > \overline{SW2} > \overline{SW1}$

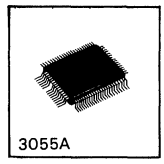
Pin Description

Pin Name	Pin No.	Input/Output Configuration	Functions
V_{DD}	12		Power supply pin V_{DD}=2.0V to 3.6V, V_{SS}=0V
V_{SS}	15		
OSC_{OUT}	10		· Oscillation of reference signal · C-MOS inverter self-bias type amp is contained. · Ceramic resonator (CF), capacitors (Ci, Co) are connected externally. · CF: CSB540E (Murata) or KBR540B (Kyocera) Ci=100pF, Co=100pF
OSC_{OUT}	11		
$\overline{K1}$ to $\overline{K8}$	1 to 8		· Key entry pin used to specify remote control signal · Built-in pull-up resistor causes normal "Hi" level to be set. When "Lo" level input is applied by signal contact type switch, OSC is operated and pulse-train remote control signal corresponding to key entry is delivered. (Refer to Timing Chart on preceding page.)
OUT_1	13		· Output pin of remote control transmit signal (Refer to Timing Chart on preceding page.) · Modulation carrier frequency of pulse-train remote control signal: 45KHz (OSC frequency (f_{OSC}): 540KHz)
OUT_2	14		· Output pin of signal (modulation carrier frequency) for transmit indicator
C	16		· Reset release of division counter is delayed until OSC is stabilized at key-ON mode. · Delay time depends on external capacitor (C), built-in resistor (r).
TEST	9		· $f_{OSC}/3072$ signal is delivered. · Device test pin

Note) Shown below are the carrier frequency and period when the reference OSC frequency (f_{OSC}) is changed

- Carrier frequency: $f_{OSC}/12$ (KHz)
- Period (T) : $T \times \frac{540\ (KHz)}{f_{OSC}\ (KHz)}$

LC7930



C MOS LSI

LCD Driver

Ⓔ 1613

Testimonial

General Description

The LC7930 is a C-MOS LSI containing 2 channels of 20-bit shift register, 20-bit latch, and 20 LCD driver outputs (40 outputs in all).
One (channel 2) of the 2 channels can be used as the back plate driver and the other (channel 1) as the segment driver.
It is especially suited for use as the LCD interface to a microcomputer (4 bits, 8 bits) or a dot matrix controller with a character generator.

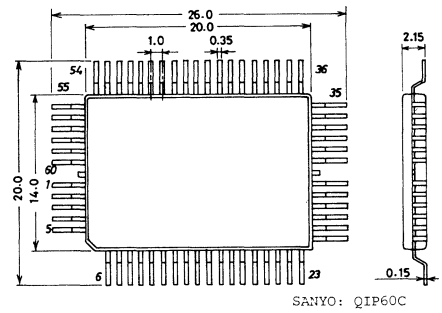
Features

1. 20-output segment driver x 2 channels (40 outputs in all)
2. Capable of being configured as 20-output segment driver + 20-output back plate driver.
3. Its connection to a controller uses 1 serial data line and 3 control signal lines.
4. A plurality of the LC7930 can be connected in series for a display with a large capacity.
5. Bidirectionality of the on-chip shift register permits the shift direction to be selected so that wiring for mounting can be facilitated.
6. Operating voltage/operating temperature range: V_{DD}=4.5 to 5.5V/Topg=-20 to +75°C
7. Operating current dissipation: I_{DD}=1.0mA max (logic 400kHz, LCD 1kHz)
8. Package: 60-pin flat (QIP60)

Absolut Maximum Ratings at Ta=25±2°C

				unit
Supply Voltage	V_{DD}		-0.3 to +7.0	V
	V_{EE}		V_{DD}-13.5 to V_{DD}+0.3	V
Input Voltage	V_I	V1,V2,V3,V4,V5,V6	-0.3 to V_{DD}+0.3	V
			V_{EE} to V_{DD}+0.3	V
Output Voltage	V_O		-0.3 to V_{DD}+0.3	V
		Output transistor:OFF Y1 to Y40	V_{EE} to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax		100	mV
Operating Temperatue	Topg		-10 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Case Outline 3055A-Q60CIC
(unit:mm)



SANYO: QIP60C

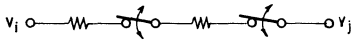
Allowable Operation conditions at Ta=-20 to +75°C, V_{SS}=0V, V_{EE}=-4 to -6V

			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD}	4.5		5.5	V
High-Level Input Voltage	V_{IH}	Note(1)	$0.7V_{DD}$		V_{DD}	V
Low-Level Input Voltage	V_{IL}	Note(1)	V_{SS}		$0.3V_{DD}$	V
Shift Frequency	f_{CL}	CLK_{SR}			400	kHz
High-Level Clock Width	f_{CWH}	CLK_{SR}, CLK_{LA}	800			ns
Low-Level Clock Width	f_{CWL}	CLK_{SR}	800			ns
Data Setup Time	t_{SU}	LDATA1, LDATA2 RDATA1, RDATA2	300			ns
Clock setup Time	t_{SL}	CLK_{SR}, SLK_{LA}: $CLK_{SR} \rightarrow CLK_{LA}$	500			ns
	t_{LS}	" : $CLK_{LA} \rightarrow CLK_{SR}$	500			ns
Clock Rise/Fall Time	t_{ct}	CLK_{SR}, CLK_{LA}			200	ns
Data Hold Time	t_{DH}	LDATA1, LDATA2, RDATA1, RDATA2	300			ns

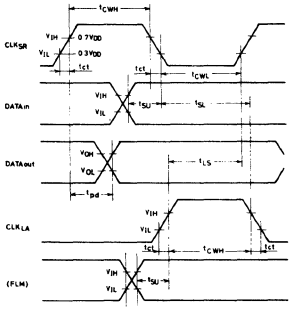
Electrical Characteristics at Ta=-20 to +75°C, V_{DD}=+5V±10%, V_{SS}=0V, V_{EE}=-4 to -6V

			min	typ	max	unit
Input Leakage Current	I_{IH}	Note(1): Vin=V_{DD}			5	uA
	I_{IL}	" : Vin=V_{SS}	-5			uA
Output "H"-Level Voltage	V_{OH}	LDATA1, LDATA2, RDATA1, RDATA2: I_{OH}=-0.4mA	V_{DD}-0.4			V
Output "L"-Level Voltage	V_{OL}	LDATA1, LDATA2, RDATA1, RDATA2: I_{OL}=0.4mA			0.4	V
Voltage Drop between Vi and Yj	Vd1	Y1 to Y40 Note(2): Ion=100uA: One of Yj			1.1	V
	Vd2	Y1 to Y40 Note(2): Ion=50uA: Each Yj			1.5	V
Vi Quiescent Current	I_{VH}	V1 to V6: Output pin: open Vin=V_{DD}			10	uA
	I_{VL}	V1 to V6: Output pin open Vin=V_{EE}	-10			uA
Supply Current	I_{DD}	V_{DD}: Output pin open CLK_{SR}=400kHz			1.0	mA
	I_{EE}	V_{EE}: Output pin open, M=1kHz			10	uA
Output Delay Time	t_{PD}	LDATA1, LDATA2, RDATA1, RDATA2: C_L=15pF			500	ns

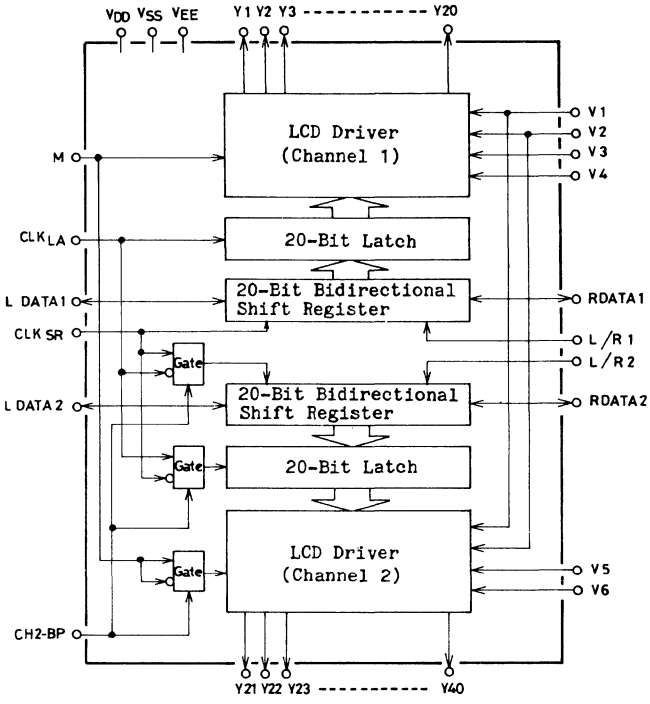
Note(1): CLK_{SR}, CLK_{LA}, LDATA1, RDATA1, LDATA2, RDATA2, M, L/R1, L/R2, CH2-BP
Note(2): Equivalent circuit between Vi and Yj(i=1 to 6, j=1 to 40)



Note(3) Switching Waveform



Internal Equivalent Circuit



Pin Assignment

Pin No.	Pin name	I/O	Pin No.	Pin name	I/O	Pin No.	Pin name	I/O
1	Y30	Output	21	Y14	Output	41	RDATA1	I/O
2	Y31	Output	22	Y13	Output	42	LDATA2	I/O
3	Y32	Output	23	Y12	Output	43	RDATA2	I/O
4	Y33	Output	24	Y9	Output	44	N.C.	-
5	Y34	Output	25	Y10	Output	45	M	Input
6	Y29	Output	26	Y11	Output	46	L/R1	Input
7	Y28	Output	27	Y8	Output	47	L/R2	Input
8	Y27	Output	28	Y7	Output	48	CH2-BP	Input
9	Y26	Output	29	V_{DD}	-	49	V1	Input
10	Y25	Output	30	Y6	Output	50	V2	Input
11	Y24	Output	31	Y5	Output	51	V3	Input
12	Y23	Output	32	Y4	Output	52	V4	Input
13	Y22	Output	33	Y3	Output	53	V5	Input
14	Y21	Output	34	Y2	Output	54	V6	Input
15	Y20	Output	35	Y1	Output	55	Y40	Output
16	Y19	Output	36	V_{EE}	-	56	Y39	Output
17	Y18	Output	37	CLK_{LA}	Input	57	Y38	Output
18	Y17	Output	38	CLK_{SR}	Input	58	Y37	Output
19	Y16	Output	39	V_{SS}	-	59	Y36	Output
20	Y15	Output	40	LDATA1	I/O	60	Y35	Output

Pin Function

<table>
<tr><th>Pin Name</th><th>Function</th></tr>
<tr><td>V_{DD}
V_{SS}
V_{EE}</td><td>Power supply for internal logic. (+5V±5%)
0V
Power Supply for Logic of LCD driver. (-4V to -6V)</td></tr>
<tr><td>Y1 to Y20
Y21 to Y40</td><td>LCD driver outputs of Channel 1.
LCD driver outputs of Channel 2.</td></tr>
<tr><td>V1,V2
V3,V4
V5,V6
L/R1</td><td>Voltage level (selected) inputs for LCD driver.
Voltage level (nonselected) inputs for LCD driver of Channel 1.
Voltage level (nonselected) inputs for LCD driver of Channel 2.
Shift direction select of the shift register of Channel 1.
<table>
<tr><th>L/R1</th><th>LDATA1</th><th>RDATA1</th></tr>
<tr><td>"H"-Level</td><td>Output</td><td>Input</td></tr>
<tr><td>"L"-Level</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>L/R2</td><td>Shift direction select of the shift register of Channel 2.
<table>
<tr><th>L/R2</th><th>LDATA2</th><th>RDATA2</th></tr>
<tr><td>"H"-Level</td><td>Output</td><td>Input</td></tr>
<tr><td>"L"-Level</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>LDATA1
RDATA1</td><td>Data input/output of the shift register of Channel 1.</td></tr>
<tr><td>LDATA2
RDATA2</td><td>Data input/output of the shift register of Channel 2.</td></tr>
<tr><td>M</td><td>AC signal for LCD driver.</td></tr>
<tr><td>CLK_{LA}</td><td>The channel data is latched on the negative transition.
(For CH2-BP="L", the same is also true of Channel 2.)</td></tr>
<tr><td>CLK_{SR}</td><td>The Channel 1 data is shifted on the negative transition.
(For CH2-BP="L", the same is also true of Channel 2.)</td></tr>
<tr><td>CH2-BP</td><td>Mode select of Channel 2.
Exchanges the latch signal and the shift signal of Channel 2 and inverts the M signal. In this mode Channel 2 can be used as the back plate driver.
<table>
<tr><th rowspan="2">CH2-BP</th><th colspan="2">Channel 2</th><th rowspan="2">M</th><th rowspan="2"></th></tr>
<tr><th>Latch</th><th>Shift</th></tr>
<tr><td>"H"</td><td>CLK_{SR} ↗</td><td>CLK_{LA} ↗</td><td>M</td><td>For back plate drive</td></tr>
<tr><td>"L"</td><td>CLK_{LA} ↘</td><td>CLK_{SR} ↘</td><td>M</td><td>For segment plate drive</td></tr>
</table></td></tr>
</table>

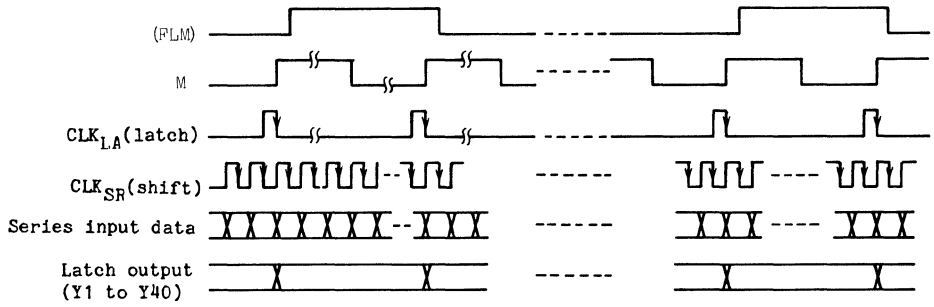
Function Description

The LC7930 is an LCD driver LSI of serial data transfer type.
The data inputted to the DATA pin serially is shifted sequentially by the synchronization clock (CLK_{SR}), and is latched by the latch clock (CLK_{LA}) when shifting is finished.

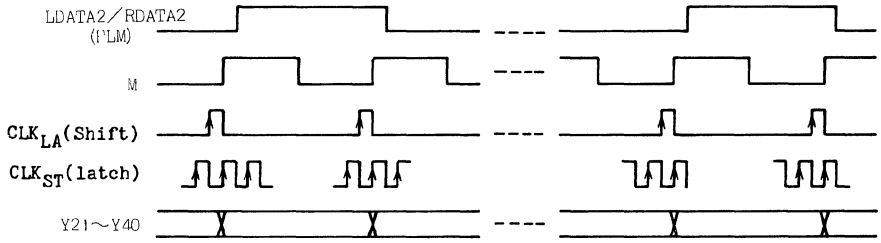
Segment plate
When CH2-BP="L", both the Channel 1 and Channel 2 data are shifted and latched on the negative transtion of CLK_{SR} and CLK_{LA} respectively. The latch data causes the select/nonselect mode.

Back plate
When CH2-BP="H", the Channel 2 data is shifted and latched on the rising transition of CLK_{LA} and CLK_{SR} respectively.
The "FLM" signal inputted as the data provides the back platedriver.

(1) Segment plate drive (CH-BP="L")



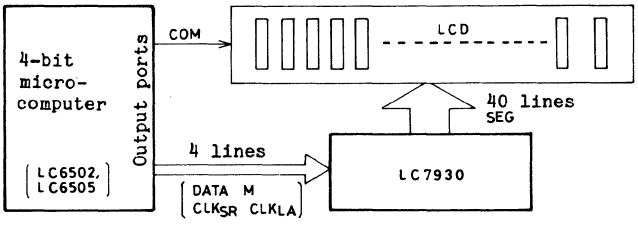
(2) Back plate drive (CH2-BP="H")



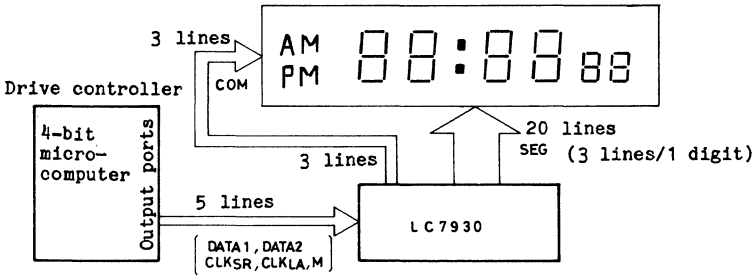
• Y1 to Y40 output of LCD drive voltage (V1 to V6)

CH2-BP	Serial input data	M	Output Y1 to Y20	Output Y2 to Y40
"H"Level (1)	1 (select)	H	V1	V2
		L	V2	V1
	0 (nonselect)	H	V3	V6
		L	V4	V5
"L"Level (0)	1	H	V1	V1
		L	V2	V2
	0	H	V3	V5
		L	V4	V6

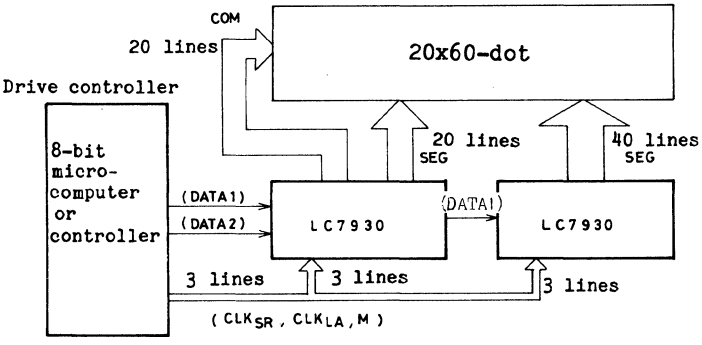
Sample LCD Display Interface
(No LCD voltage divider is illustrated.)
(1) 40-segment bar graph display (static)



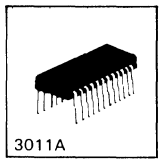
(2) 6-digit 7-segment + sign display (1/3 duty, 1/3 bias)



(3) 20 x 60-dot graphic display (1/20 duty, 1/5 bias)



LM8071



P MOS LSI

Equal Tempered Scale Generator

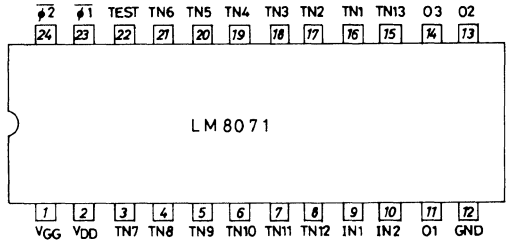
Ⓔ 216E

The LM8071 is a master tone generator of equal tempered scale driven by 2-phase clock pulses generated by a main oscillator. The frequency of 2-phase clock pulses is selected from among 0.25 to 2.2MHz according to an application or purpose for which the LM8071 is used and is divided into 13 different frequencies. Thirteen tones are 12 tones of C_8, $C_8^{\#}$,D, -----, B_8 and C9. The output impedance of the LM8071 is designed to be equal to that of 6-bit divider IC LM3216.
The LM8071 contains a 3-bit TFF that is connected across main oscillator and clock driver and serves to provide 4 selections of octave for the 13-tone range. Thus, the main oscillator requires no more than one crystal to produce 4 different tones.
The 13-tone cent error for 2119.040kHz and a sample main oscillator and clock driver are shown below.

Absolute Maximum Ratings at Ta=25°C			unit
Maximum Voltage Applied to Pin	BV_{PIN}	-20 to +0.3	V
Operating Frequency	Topg	-10 to +60	°C
Storage Temperature	Tstg	-40 to +125	°C

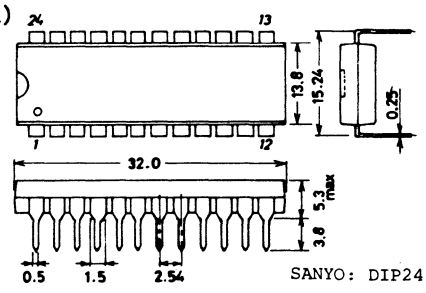
Allowable Operating Ranges at Ta=25°C			unit
Opeerating V_{DD} Voltage	V_{DD}	-11.0 to -9.0	V
Operating V_{GG} Voltage	V_{GG}	-18.7 to -15.3	V

Pin Assignment



In actual applications the TEST pin must be connected to GND.

Case Outline 3011A-D24IC
(unit:mm)



SANYO: DIP24

Allowable Operating Ranges at Ta=25°C, V_{GG}=-17V±10%, V_{DD}=-10V±10%

			min	typ	max	unit
Input "H" Level	V_{IH}		-1.0		0	V
Input "L" Level	V_{IL}		V_{GG}		-8.0	V
Input "H" Level Time	t_{IH}	Fig. 1	150			ns
Input "L" Level Time	t_{IL}	Fig. 1	150			ns
Input Transient Time	t_{If},t_{Ir}	Fig. 1			1	us
Input Frequency	f_I	t_{IL},t_{IH}≧150ns t_{If},t_{Ir}≦50ns Fig. 1	0.1		2.3	MHz
Clock "H" Level	VØH	Fig. 2	-1.0		0	V
Clock "L" Level	VØL	Fig. 2	V_{GG}		V_{GG}+1	V
Clock Pulse Width	tØw	Fig. 2	145			ns
Clock Interval	tØs	Fig. 2	0			ns
Clock Transient Time	tØf,tØr	fØ=2.2MHz tØw=145ns Fig. 2			40	ns
Clock Transient Time	fØf,tØr	tØ=100kHz tØw=145ns Fig. 2			100	ns
Clock Frequency	fØ	tØw≧145ns tØr,tØf≦40ns tØs≧0 Fig. 2	0.1		2.3	MHz

Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Tone Counter Output "H" Level	$V_{OH(1)}$	I_{OH}=-0.5mA V_{GG}=-15.3V V_{DD}-9V Fig. 4	-0.5			V
Tone Counter Output "L" Level	$V_{OL(1)}$	I_{OL}=0.4mA V_{GG}=-15.3V V_{DD}=-9V Fig. 4			-8.0	V
Tone Counter Output Resistance (V_{DD} Side)	$r_{OUT(1)}$	V_{DD}=-9V V_{GG}=-15.3V			2.5	kohm
Tone Counter Output Resistance (GND Side)	$r_{OUT(2)}$	V_{DD}=-9V V_{GG}=-15.3V			1.0	kohm
Tone Counter Output Duty Cycle				50		%
TFF Output "H" Level	$V_{OH(2)}$	I_{OH}=-0.25mA V_{GG}=-15.3V V_{DD}=-9V Fig. 3	-0.5			V
TFF Output "L" Level	$V_{OL(2)}$	I_{OL}=1.6mA V_{GG}=-15.3V V_{DD}=-9V Fig. 3			-5.8	V
TFF Output Resistance (V_{DD} Side)	$r_{OUT(3)}$	V_{DD}=-9V V_{GG}=-15.3V			2	kohm
TFF Output Resistance (GND Side)	$r_{OUT(4)}$	V_{DD}=-9V V_{GG}=-15.3V			2	kohm
Input Resistance	r_{IN}	V_{IN}=-10V	1			Mohm
Clock Resistance	rØ	VØ=-18.7V	1			Mohm
Input Capacitance	C_{IN}	f=1MHz,V_{IN}=0V			10	pF
Clock Capacirance	CØ	f=1MHz,VØ=0V			100	pF

			min	typ	max	unit
V_{GG} Supply Current	I_{GG}	V_{GG}=-18.7V, V_{DD}=-11V			8	mA
V_{DD} Supply Current	I_{DD}	V_{GG}=-18.7V, V_{DD}=-11V			70	mA

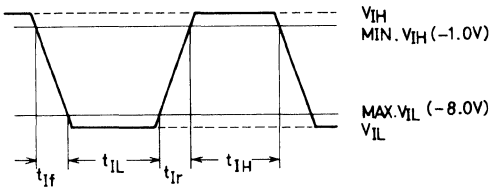


Fig. 1 Input Waveform

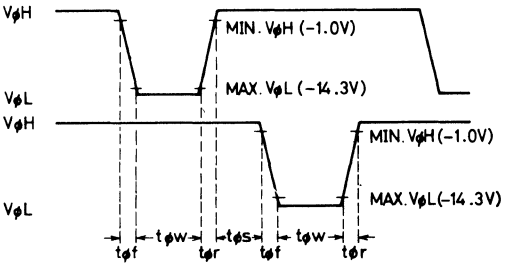


Fig. 2 Clock Waveform

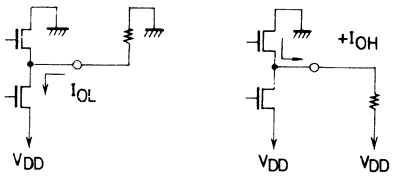


Fig. 3 Output Signal Test Circuit
O_1, O_2, O_3(Pre-TFF Output)

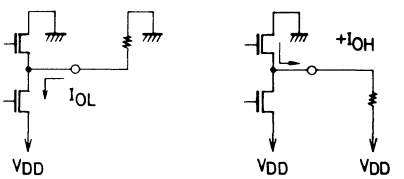
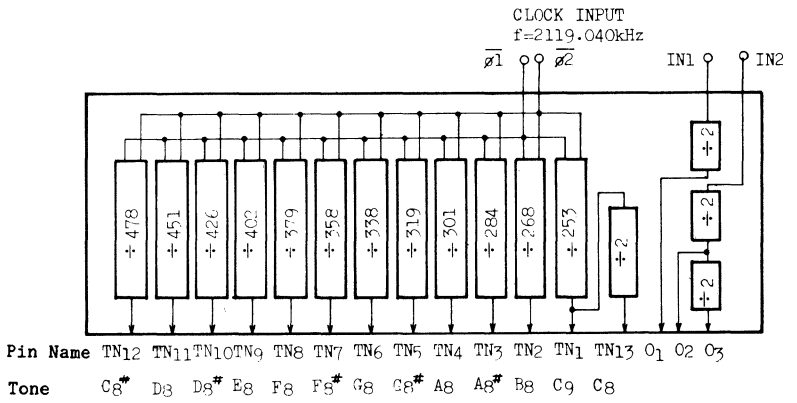


Fig. 4 T_{N1}, T_{N2}-----T_{N13}
(Tone Counter Output)

Equivalent Circuit Block Diagram(C Scale Circuit Function)

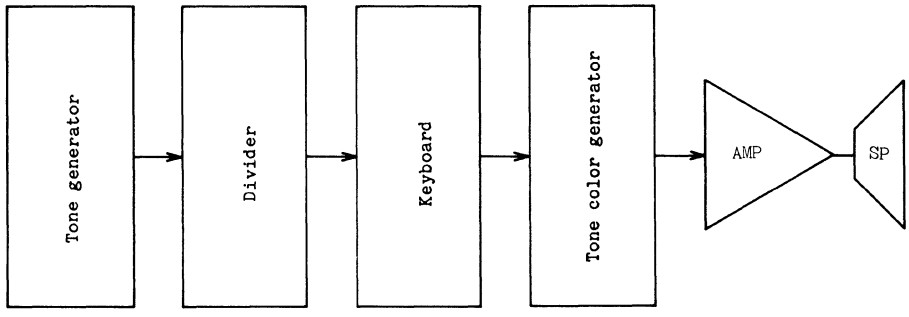


Division	Ratio	(Hz) Output Frequency	(Hz) True Frequency	Cent Error
C_9	253	8375.652	8372.018	+0.751
B_8	268	7906.866	7902.133	+1.037
$A_8^{\#}$	284	7461.408	7458.620	+0.647
A_8	301	7040.000	7040.000	0.000
$G_8^{\#}$	319	6642.759	6644.875	-0.551
G_8	338	6269.349	6271.927	-0.712
$F_8^{\#}$	358	5919.106	5919.911	-0.235
F_8	379	5591.135	5587.652	+1.079
E_8	402	5271.244	5274.041	-0.918
$D_8^{\#}$	426	4974.272	4978.032	-1.308
D_8	451	4698.537	4698.636	-0.036
$C_8^{\#}$	478	4433.138	4434.922	-0.697

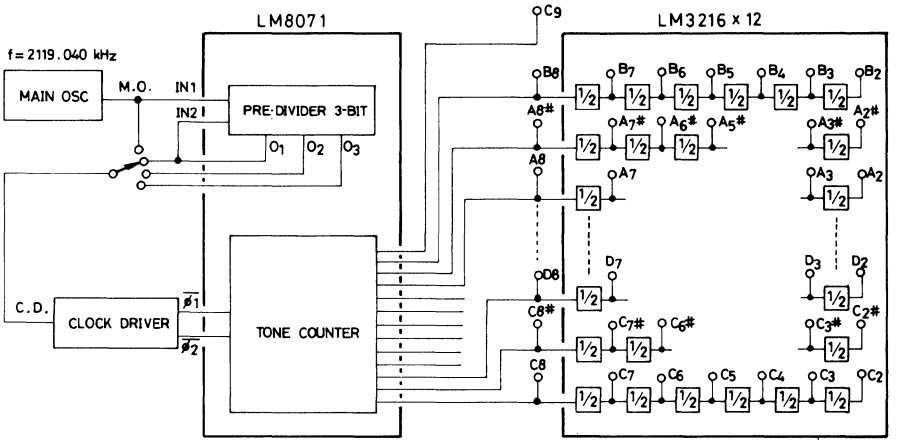
C scale output frequency (clock frequency=2119.040kHz)

Sample Application Circuit

1. Electronic Organ Block Diagram

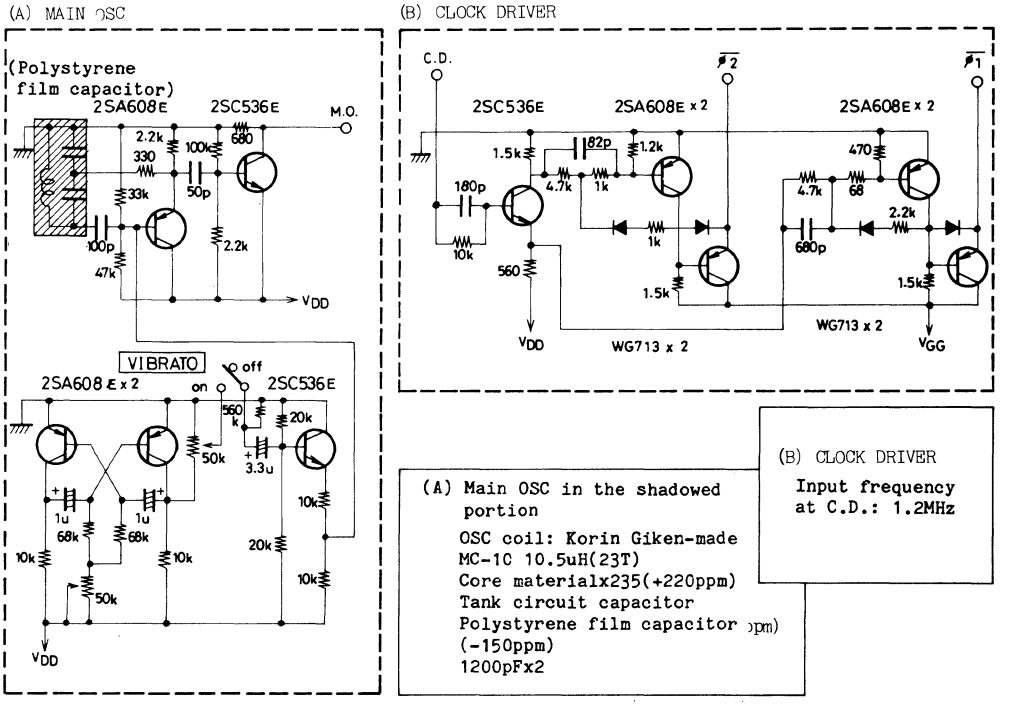


2. Detailed Block Diagram of Tone Generator, Divider



System Diagram

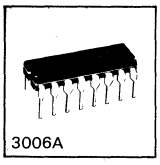
3. Sample Main OSC and Clock Driver



(A) Main OSC in the shadowed portion
OSC coil: Korin Giken-made
MC-10 10.5uH(23T)
Core materialx235(+220ppm)
Tank circuit capacitor
Polystyrene film capacitor ppm)
(-150ppm)
1200pFx2

(B) CLOCK DRIVER
Input frequency at C.D.: 1.2MHz

LM8372



P MOS IC

Rhythm Pattern Generator

Ⓔ 473C

General Description

- Selectable rhythms: 8 rhythms
- Outputs for pattern generation: 6 outputs
- Time: Simple triple time, quadruple time
- Steps: Simple triple time line: 6 steps
  Quadruple time line: 8 steps
- Output pin for tempo lamp (T_L output)

Absolute Maximum Ratings at Ta=25±2°C

				unit
Maximum Supply Voltage	V_{GG}		-20 to +0.3	V
Input Voltage	v_i		-20 to +0.3	V
Output Voltage	v_o	Outut Tr OFF	-20 to +0.3	V
Allowable Power Dissipation	Pdmax	Ta≦60°C	350	mW
Operating Temperature	Topg		-10 to +60	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at ta=25±2°C

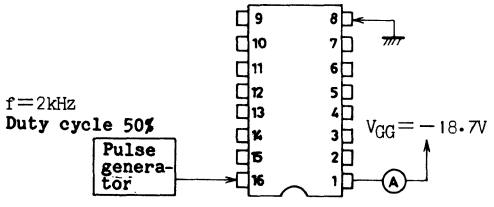
				min	typ	max	unit
Supply Voltage	V_{GG}	1	Ta=-10to+60°C	-18.7	-17	-15.3	V
High-Level Input Voltage	$V_{IH(1)}$	3to7		-0.6		0	V
	$V_{IH(2)}$	2,16		-1.0		0	V
Low-Level Input Voltage	V_{IL}	2to7,16		V_{GG}		-8.0	V
Input Transient Time	t_{Ir}, t_{If}	16				15	usec
Operating Frequency	f_{CLK}	16		DC		100	Hz

Electrical Characteristics at Ta=25±2°C, V_{GG}=-15.3 to 18.7V

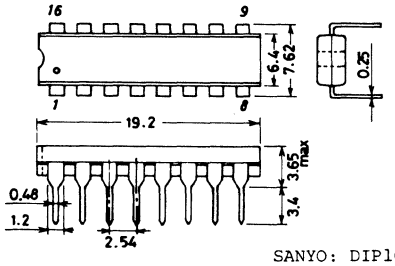
				min	typ	max	unit
High-Level Output Voltage	V_{OH}	9to15	I_{OH}=-0.5mA	-0.5		0	V
Output OFF Leak Current	I_{OL}	9to15	$V_o=V_{GG}+1V$	-20			uA
Input Current	I_I	2to17,16	V_{IN}=-10V	-3			uA
Input Pull-up Resistance	R_{IN}	3to7	V_{IN}=GND	25			kohm
			V_{IN}=6V			750	kohm
Current Dissipation	I_{GG}	1	V_{GG}=-18.7V	-12	-6		mA
			See the Test Circuit below.				

[Note] Current direction: Positive (No sign): Flowing into device
Negative (- sign): Flowing out of device

Current Dissipation Test Circuit

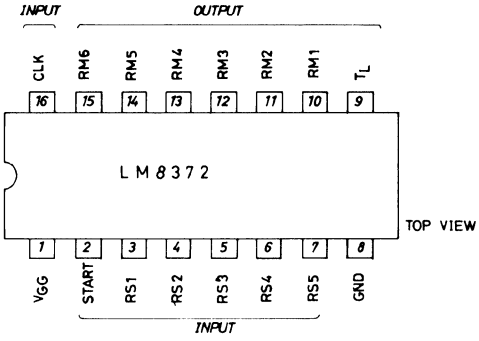


Case Outline 3006A-D16IC
(unit:mm)

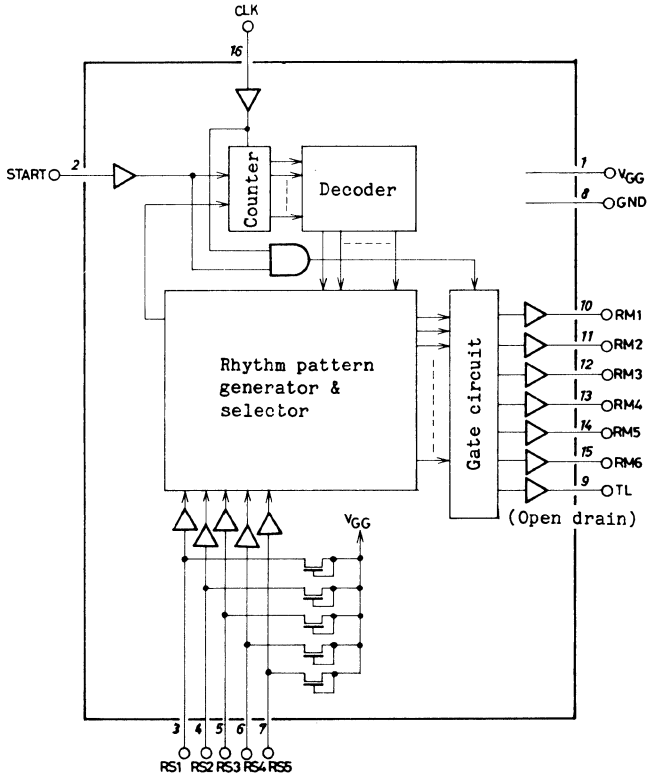


SANYO: DIP16

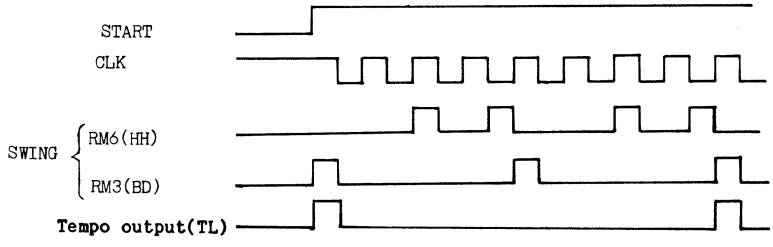
Pin Connection and Pin Assignment



Equivalent Circuit Block Diagram



Input/Output Waveforms

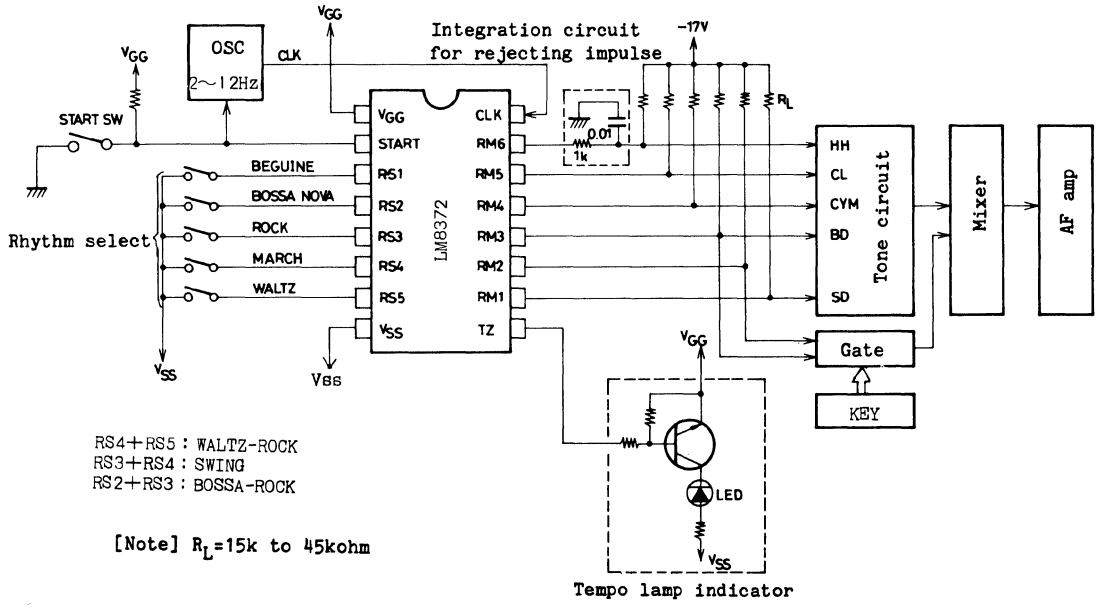


Rhythm Pattern

Rhythm	Rhythm Select Input	Pattern Output	1	2	3	4	5	6	7	8
BEGUINE	RS1="H" Other pin="L"	RM4		○						
		RM6	○	○	○	○	○	○	○	○
		RM1		○		○		○		○
		RM5	○			○			○	
		RM2		○		○		○		○
		RM3	○				○		○	
BOSSA-NOVA	RS2="H" Other pin="L"	RM6	○	○	○	○	○	○	○	○
		RM5	○			○			○	
		RM2	○	○	○	○	○	○	○	○
		RM3	○			○	○			○
ROCK	RS3="H" Other pin="L"	RM6	○	○	○	○	○	○	○	○
		RM1			○				○	
		RM2			○				○	
		RM3	○			○	○			○
MARCH	RS4="H" Other pin="L"	RM4	○				○			
		RM1			○				○	
		RM2			○				○	
		RM3	○				○			
WALTZ	RS5="H" Other pin="L"	RM4	○							
		RM1				○		○		
		RM2				○		○		
		RM3	○							
BOSSA-ROCK	RS2="H" RS3="H" Other pin="L"	RM6	○	○	○	○	○	○	○	○
		RM1			○				○	
		RM5	○			○			○	
		RM2	○	○	○	○	○	○	○	○
		RM3	○			○	○			○
SWING	RS3="H" RS4="H" Other pin="L"	RM4	○				○			
		RM6	○		○		○		○	○
		RM1			○				○	
		RM2			○				○	
		RM3	○				○			
WALTZ-ROCK	RS4="H" RS5="H" Other pin="L"	RM4	○							
		RM1				○		○		
		RM2				○		○		
		RM3	○				○			

RM1 Snare drum
RM2 Auto chord output
RM3 Bass drum
RM4 Cymbal
RM5 Claves
RM6 High hat

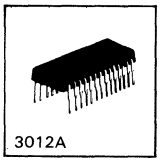
Sample Application Circuit



RS4+RS5 : WALTZ-ROCK
RS3+RS4 : SWING
RS2+RS3 : BOSSA-ROCK

[Note] R_L=15k to 45kohm

LM8471



P MOS LSI

Rhythm Pattern Generator

Ⓔ 456C

The LM8471 is a P-channel MOS LSI designed for use in the auto rhythm section of electronic organs or rhythm instruments.
It is capable of selecting 10 rhythms and driving 9 kinds of percussion instrument. It is also capable of providing 2 kinds of variation on each rhythm. These two kinds of variation can be played automatically. This means that 10 (rhythms) x 2 (variations) = 20 (rhythm patterns) are available. The rhythm tempo indicator (lighted every beat) makes it possible for you to know the rhythm tempo during the pause of playing and to restart playing smoothly.

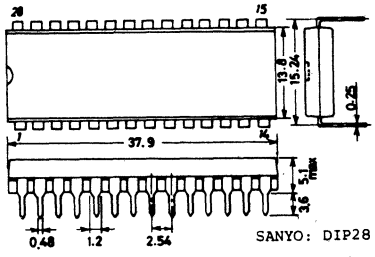
General Description

- Selectable rhythms: 10 rhythms
- Steps: Simple triple time line: 48 steps
  Quadruple time line: 64 steps
- Outputs for tone generator drive: 8 outputs
- Outputs for auto chord: 3 outputs
- Output for tempo indicator: 1 output (Lighted at the beginning of a bar during playing; lighted every beat during pausing)
- On-chip oscillator (External C,R)
- With variation pins (VARI-A, VARI-B)

Absolute Maximum Ratings at Ta=25±2°C

			unit
Maximum Supply Voltage	$V_{DD}max$	-13 to +0.3	V
Maximum Input Voltage	V_I	-13 to +0.3	V
Operating Temperature	Topg	-10 to +60	°C
Storage Temperature	Tstg	-40 to +125	°C

Case Outline 3012A-D28IC
(unit:mm)



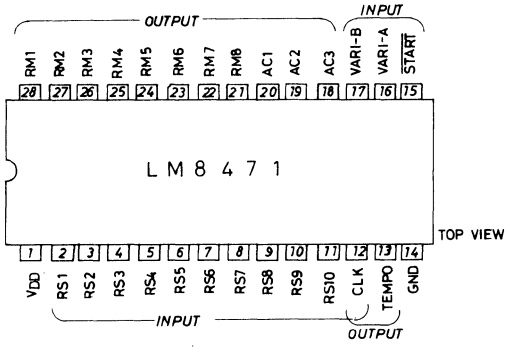
Allowable Operating Ranges at Ta=25±2°C

				min	typ	max	unit
Supply Voltage	V_{DD}		Ta=-10 to +60°C	-11	-10	-9	V
"H"-Level Input	$V_{IH(1)}$	RS1 to RS10		-0.8		0	V
	$V_{IH(2)}$	$\overline{START}$,VARI-A,VARI-B		-1.0		0	V
"L"-Level Input	V_{IL}	RS1 to RS10,$\overline{START}$, VARI-A,VARI-B		V_{DD}		-8.5	V
Input Pulse Rise Time	t_{Ir}	RS1 to RS10,$\overline{START}$, VARI-A,VARI-B				50	ms
Input Pulse Fall Time	$t_{If(1)}$	RS1 to RS10,VARI-A,VARI-B				50	ms
	$t_{If(2)}$	$\overline{START}$		2.0		50	ms
Operating Frequency	f_{CLK}	CLK		10		1000	Hz
External Resistance for OSC	R	CLK		18		600	kohm

Electrical Characteristics at Ta=25±2°C,V_{DD}=-9 to -11V

				min	typ	max	unit
"H"-Level Input	V_{OH}		I_{OH}=-0.5mA	-0.5		0	V
Output Leak Current	I_{OL}		V_{OL}=-10V	-20			uA
Input Current	I_I	$\overline{START}$	V_{IN}=-10V	-3			uA
Input Pull-up Resistance (V_{DD} Side)	$R_{IN(1)}$	RS1toRS10	V_{IN}=GND	15		400	kohm
	$R_{IN(2)}$	VARI-A,VARI-B	V_{IN}=GND	20		600	kohm
Supply Voltage Characteristic of OSC Frequency	△f(V)	CLK				±15	%
Temperature Characteristic of OSC Frequency	△f(Ta)	CLK				±25	%
Current Dissipation	I_{DD}	V_{DD}	V_{DD}=-11V		-5		mA

Pin Assignment and Pin Connection

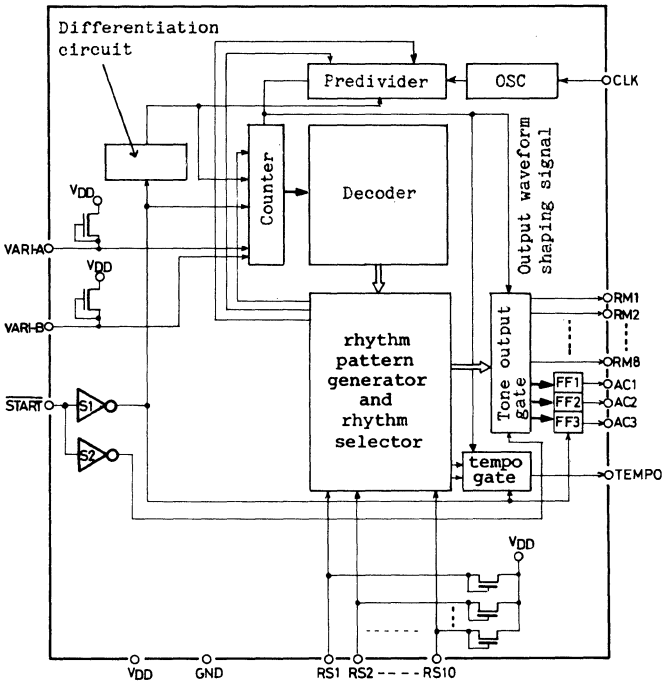


RS1:WALTZ RS2:MARCH RS:TANGO RS4:ROCK
RS5:SWING RS6:MAMBO RS7:BOSSA-NOVA RS8:SLOW-ROCK
RS9:SAMBA RS10:BEGUINE

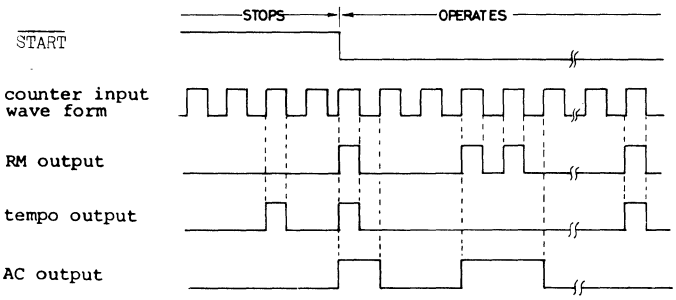
RM1:Cymbal RM2:Low conga(LC) RM3:High conga(HC)
RM4:Snare drum(SD) RM5:High hat(HH) RM6:Claves(CL)
RM7:Bongo(BO) RM8:Maraca(MA) AC2+AC3:Bass drum(BD)

AC1:lower manual AC2:pedal 1 AC3:pedal 5

Internal Block Diagram

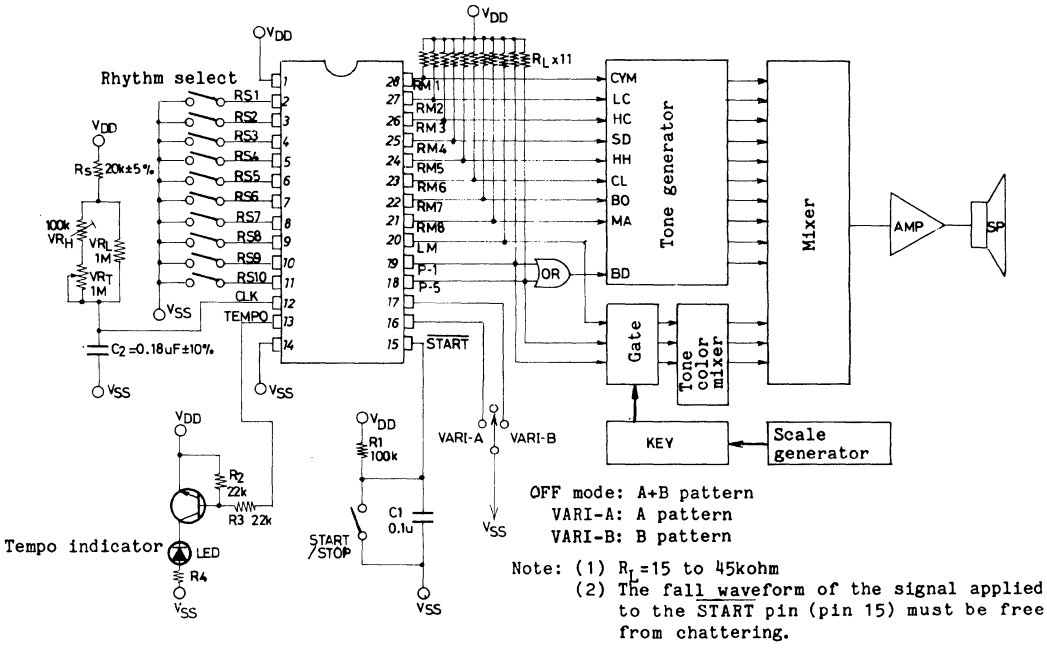


Input/Output Waveforms



Note: Holding input RS1 at "H"(V_{SS}) level delivers RM1 (to RM8) output corresponding to RS1.

Sample Application Circuit



OFF mode: A+B pattern
VARI-A: A pattern
VARI-B: B pattern

Note: (1) R_L=15 to 45kohm
(2) The fall waveform of the signal applied to the START pin (pin 15) must be free from chattering.

LM8972

P MOS IC

Rhythm Pattern Generator

Ⓔ 470A

Use

Radio cassette tape recorders, stereos

(Note) This IC has no auto chord outut because it is intended for use in audio equipment (other than keyboard instruments). For electronic organs, the LM8372 (rhythm pattern generator IC with auto chord output) is available.

The LM8972 is classified into two groups according to supply voltage (V_{GG}).

A rank V_{GG}=-15V to -18.7V(operation from 17V)

B rank V_{GG}=-6V to -15V(operation from 9V, 12V)

General Description

- Selectable rhythms: 8 rhythms
- Outputs for pattern generation: 5 outputs
- Time: Simple triple time, quadruple time
- Steps: Simple triple time line: 6 steps
  Quadruple time line: 8 steps
- Output for tempo lamp (TL output)

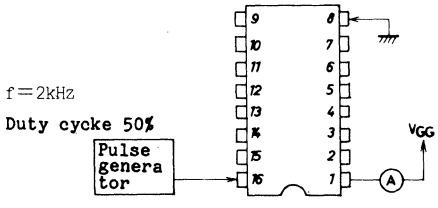
Absolute Maximum Ratings at Ta=25±2°C

				unit
Maximum Supply Voltage	V_{GG}		-20 to +0.3	V
Input Voltage	v_i		-20 to +0.3	V
Output Voltage	v_o	Output Tr OFF	-20 to +0.3	V
Allowable Power Dissipation	Pdmax	Ta≦60°C	350	mW
Operating Temperature	Topg		-10 to +60	°C
Storage Temperature	Tstg		-40 to +125	°C

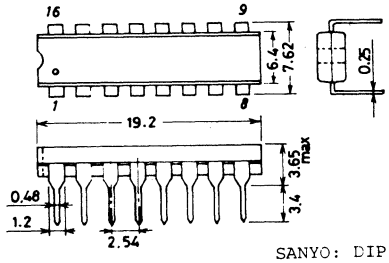
Allowable Operating Ranges at Ta=25±2°C, V_{SS}=0V

				min	typ	max	unit
Supply Voltage	V_{GG}	1	Ta=-10 to 60°C	-18.7		-6.0	V
High-Level Input Voltage	$V_{IH(1)}$	3to7		-0.6		0	V
	$V_{IH(2)}$	2,16		-1.0		0	V
Low-Level Input Voltage	V_{IL}	2to7,16		V_{GG}		-5.5	V
Input Transient Time	t_{Ir},t_{If}	16				15	us
Operating Frequency	$f_{(CLK)}$	16		0.1		100	Hz

Current Dissipation Test Circuit



Case Outline 3006A-D16IC
(unit:mm)



SANYO: DIP16

Electrical Characteristics [LM8972 A] at V_{GG}=-15 to -18.7V,Ta=25°C,V_{SS}=0V

				min	typ	max	unit
High-Level Output Voltage	V_{OH}	9,10,12to15	I_{OH}=-0.5mA	-0.5		0	V
Output OFF Leak Current	I_{OL}	9,10,12to15	Vo=V_{GG}+1V	-20			uA
Input Current	I_I	2to7,16	V_{IN}=-10V	-3			uA
Input Pull-up Resistance	R_{IN}	3to7	V_{IN}=V_{SS}	25k			ohm
(V_{GG} Side)		3to7	V_{IN}=-6V			750k	ohm
Current Dissipation	I_{GG}	1	V_{GG}=-18.7V	-12	-3		mA
			See the Test Circuit below.				

Electrical Characteristics [LM8972 B] at V_{GG}=-10 to -15V,Ta=25°C,V_{SS}=0V

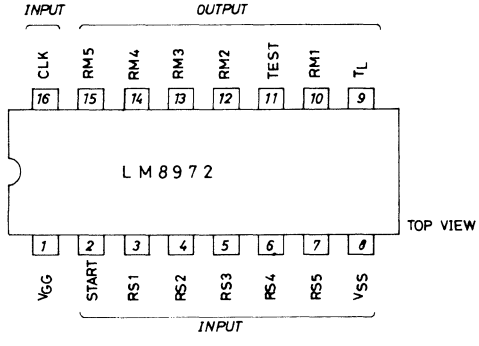
				min	typ	max	unit
High-Level Output Voltage	V_{OH}	9,10,12to15	I_{OH}=-0.5mA	-0.75			V
Output OFF Leak Current	I_{OL}	9,10,12to15	Vo=V_{GG}+1V	-20			uA
Input Current	I_I	2to7,16	V_{IN}=-10V	-3			uA
Input Pull-up Resistance	R_{IN}	3to7	V_{IN}=V_{SS} to V_{GG}	25k			ohm
(V_{GG} Side)							
Current Dissipation	I_{GG}	1	V_{GG}=-15V	-12	-2		mA
			See the Test Circuit below.				

Electrical Characteristics [LM8972 B] at V_{GG}=-6 to -10V,Ta=25°C,V_{SS}=0V

				min	typ	max	unit
High-Level Output Voltage	V_{OH}	9,10,12to15	I_{OH}=-0.5mA	-1.5			V
Output OFF Leak Current	I_{OL}	9,10,12to15	Vo=V_{GG}+1V	-20			uA
Input Current	I_I	2to7,16	V_{IN}=-10V	-3			uA
Input Pull-up Resistance	R_{IN}	3to7	V_{IN}=V_{SS} to V_{GG}	50k			ohm
(V_{GG} Side)							
Current Dissipation	I_{GG}	1	V_{GG}=-10V	-3.0	-1.0		mA
			See the Test Circuit below.				

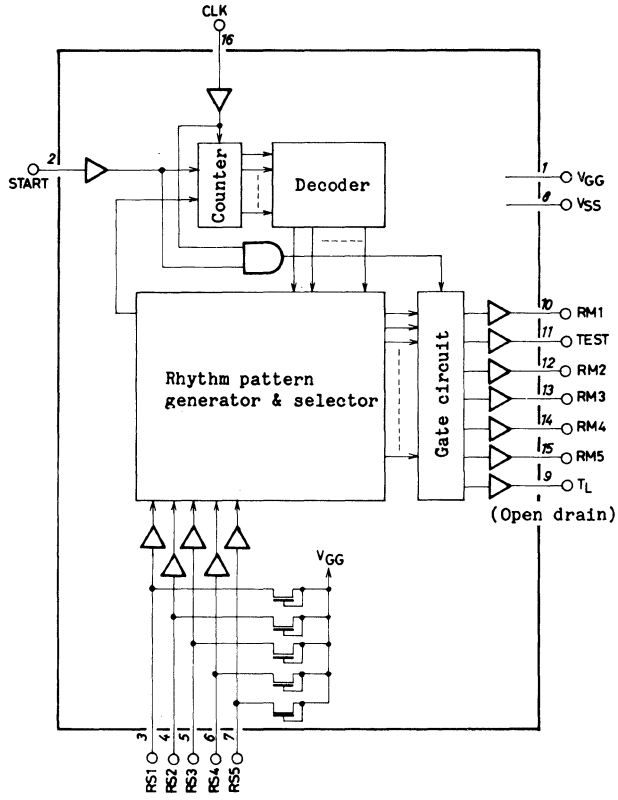
(Note) 1. Current direction: Positive (no sign): Flowing into device
Negative (- sign): Flowing out of device
2. When using the IC at V_{GG} from -6V to -15V, the RS input pins (pins 3 to 7) must not be open.
3. The TEST pin (pin 11) must be connected to V_{SS}.

Pin Assignment and Pin Connection

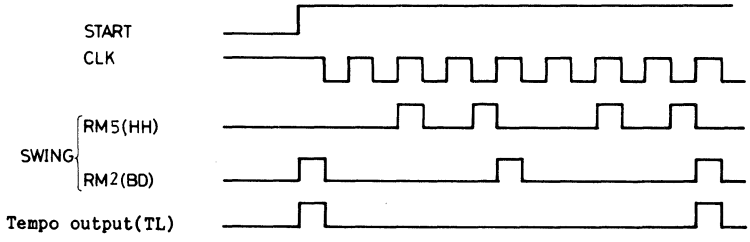


RS1: BEGUINE
RS2: BOSA-NOVA
RS3: ROCK
RS4: MARCH
RS5: WALTZ
RS2+RS3: BOSSA-ROCK
RS3+RS4: SWING
RS4+RS5: WALTZ-ROCK
RM1: Snare drum(SD)
RM2: Bass drum(BD)
RM3: Cymbal(CYM)
RM4: Claves(CL)
RM5: High hat(HH)

Equivalent Circuit Block Diagram



Input/Output Waveforms

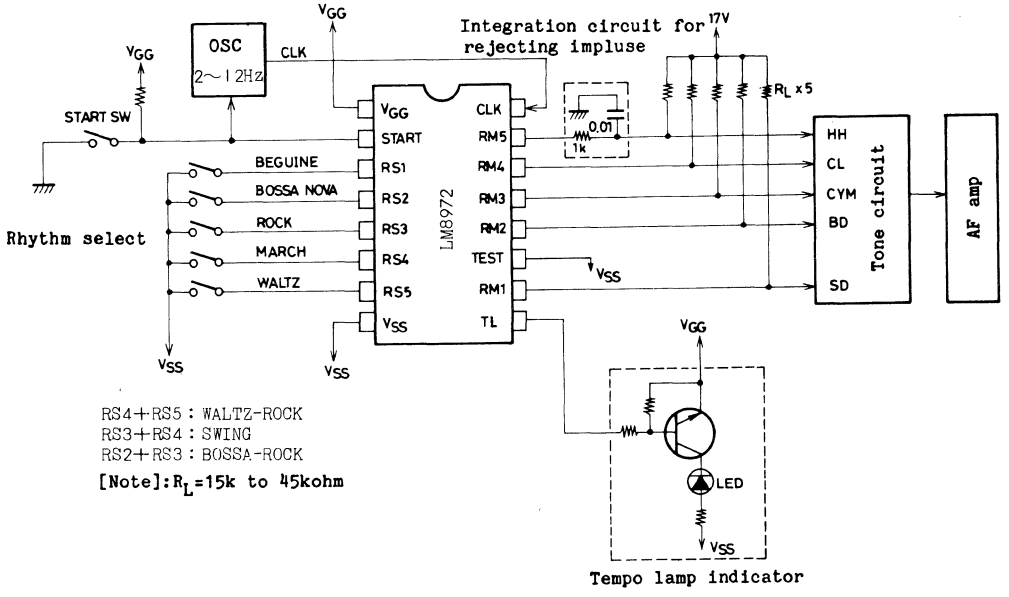


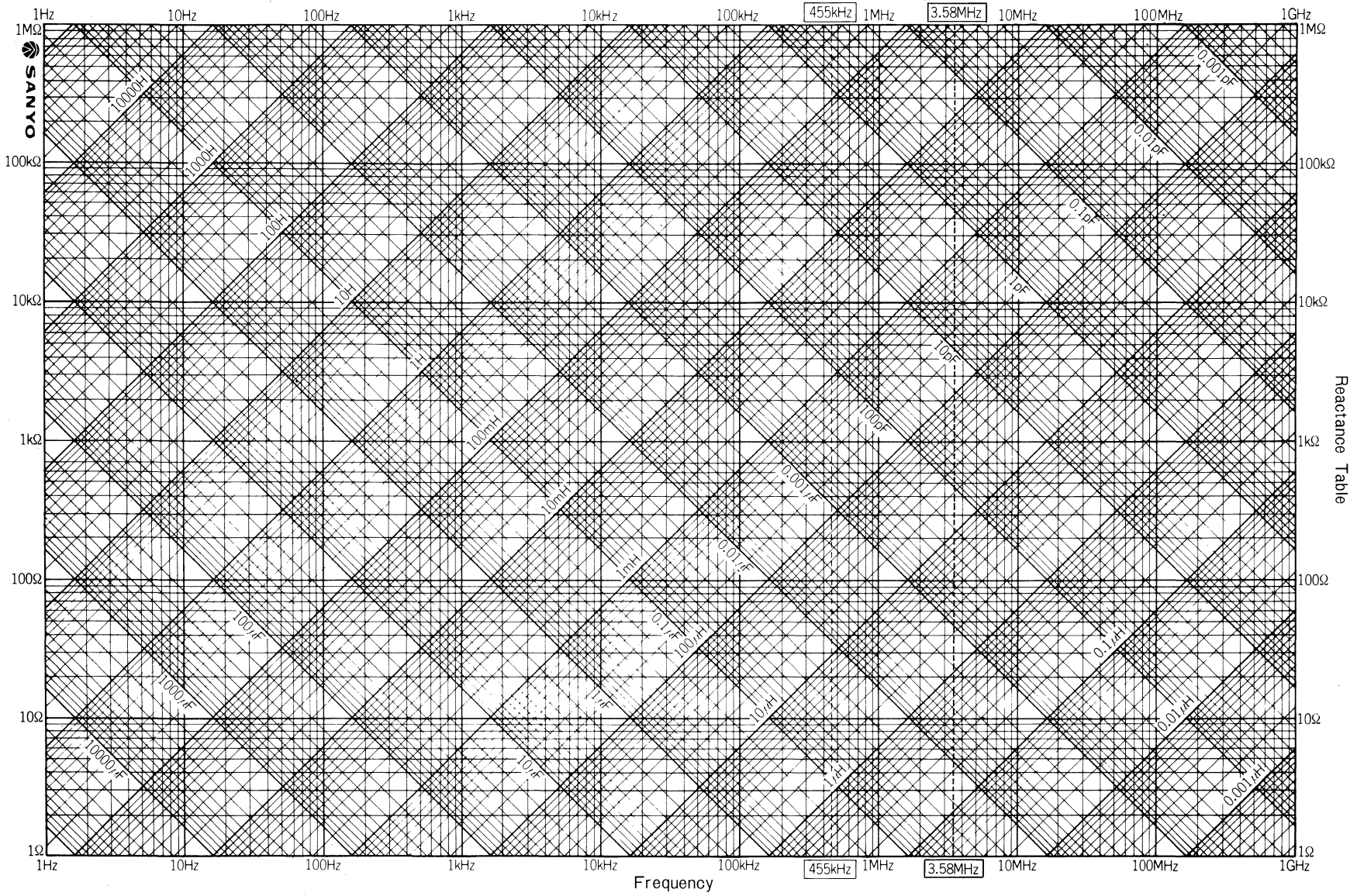
Rhythm pattern generator & selector

Rhythm	Rhythm Select Input	Pattern Output	1	2	3	4	5	6	7	8
BEGUINE	RS1="H" Other pin="L"	RM3		○						
		RM5	○	○	○	○	○	○	○	○
		RM1		○		○		○		○
		RM4	○			○			○	
		RM2	○				○		○	
BOSSA-NOVA	RS2="H" Other pin="L"	RM5	○	○	○	○	○	○	○	○
		RM4	○			○			○	
		RM2	○			○	○			○
ROCK	RS3="H" Other pin="L"	RM5	○	○	○	○	○	○	○	○
		RM1			○				○	
		RM2	○			○	○			○
MARCH	RS4="H" Other pin="L"	RM3	○				○			
		RM1			○				○	
		RM2	○				○			
WALTZ	RS5="H" Other pin="L"	RM3	○							
		RM1				○		○		
		RM2	○							
BOSSA-ROCK	RS2="H" RS3="H" Other pin="L"	RM5	○	○	○	○	○	○	○	○
		RM1			○				○	
		RM4	○			○			○	
		RM2	○			○	○			○
SWING	RS3="H" RS4="H" Other pin="L"	RM3	○				○			
		RM5			○	○			○	○
		RM1			○				○	
		RM2	○				○			
WALTZ-ROCK	RS4="H" RS5="H" Other pin="L"	RM3	○							
		RM1				○		○		
		RM2	○				○			

Pattern output name: RM1 snare drum, RM2 bass drum, RM3 cymbal, RM4 claves, RM5 high hat.

Sample Application Circuit




SANYO
1Hz
10Hz
100Hz
1kHz
10kHz
100kHz
455kHz
1MHz
3.58MHz
10MHz
100MHz
1GHz
1MΩ
100kΩ
10kΩ
1kΩ
100Ω
10Ω
1Ω
Frequency
Reactance Table
10000H
1000H
100H
10H
1H
100mH
10mH
1mH
100μH
10μH
1μH
0.1μH
0.01μH
0.001μH
10000μF
1000μF
100μF
10μF
1μF
0.01μF
0.001μF
100pF
10pF
1pF
0.1pF
0.01pF
0.001pF

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