Ordering number : EN*5240

CMOS LSI

LC895124

CD-ROM Driver with On-Chip SCSI Interface and Subcode Functions

Preliminary

Overview

The LC895124 is the next-generation version of the LC89512 and is a CD-ROM decoder that includes a SCSI interface that supports the high-speed transfers (10 MB/s) of the FAST SCSI standard.

Functions

CD-ROM ECC function, subcode read function, SCSI interface

Features

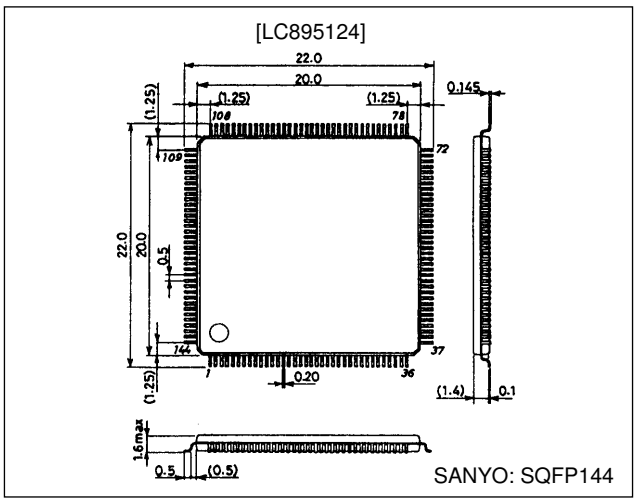
- On-chip SCSI interface (with built-in SCAM selection register)
- Supports 8× playback - Using ×16 80-ns DRAMs
- Supports 4× playback - Using ×16 80-ns DRAMs or ×8 70-ns DRAMs
- Transfer rates: 10 MB/s (synchronous), 5 MB/s (asynchronous) using ×16 80-ns DRAMs*1
- Transfer rates: 8.467 MB/s (synchronous), 4.2336 MB/s (asynchronous) using ×8 70-ns DRAMs*2
- PSRAM can be used, providing 5 MB/s transfers in synchronous mode and 5 MB/s transfers in asynchronous mode .
- Supports the connection of up to 32 Mb of buffer RAM (using DRAM) (Up to 2 Mb when PSRAM is used)
- The user can freely set the CD main channel, C2 flag, and other areas in buffer RAM.
- Batch transfer function (transfers the CD main channel and C2 flag data in a single operation)
- Multi-block transfer function (automatically transfers multiple blocks in a single operation)
- High-speed transfer mode supports a 10-MB/s (synchronous) transfer rate using ×8 80-ns DRAMs
- Subcode ECC function

Note: 1. For speeds up to 8× speed, use a SCSI master clock frequency of 20 MHz.
2. For speeds up to 4× speed, use a SCSI master clock frequency of 16.9344 MHz.

Package Dimensions

unit: mm

3214-SQFP144



Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltages	V_I, V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	450	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering heat resistances (pins only)		10 seconds	260	°C

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Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C

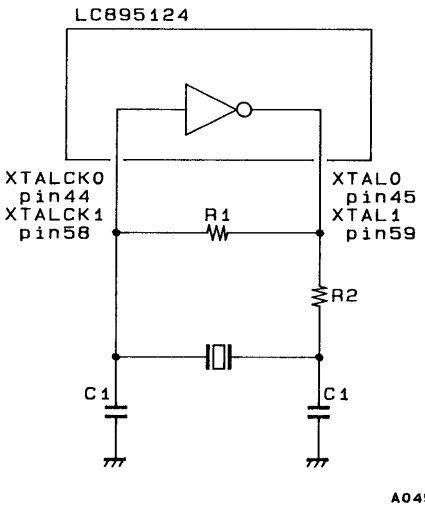
Parameter	Symbol	Applicable Pins	min	typ	max	Unit
Input high level voltage	$V_{IH}1$	All input pins other than (1), (3), and XTALCK	2.2			V
Input low level voltage	$V_{IL}1$				0.8	V
Input high level voltage	$V_{IH}2$	$\overline{RESET}$, IO0 to IO15, D0 to D7, $\overline{RD}$, $\overline{CS}$, $\overline{WR}$, WFCK, SBSO, SCOR (1)	2.5			V
Input low level voltage	$V_{IL}2$				0.6	V
Input high level voltage	$V_{IH}3$	Input pins (3), $\overline{ACK}$, and $\overline{ATN}$	2.0			V
Input low level voltage	$V_{IL}3$				0.8	V
Output high level voltage	$V_{OH}1$	$I_{OH}1$ = –2 mA: All output pins except (2), (3), and XTALCK, IO0 to IO15, and D0 to D7	2.4			V
Output low level voltage	$V_{OL}1$	$I_{OL}1$ = 2 mA: All output pins except (2), (3), and XTALCK, IO0 to IO15, and D0 to D7			0.4	V
Output low level voltage	$V_{OL}2$	$I_{OL}2$ = 2 mA: $\overline{INT1}$, $\overline{INT0}$, and ZSWAIT (open-drain outputs with pull-up resistors) (2)			0.4	V
Output low level voltage	$V_{OL}3$	$I_{OL}3$ = 48 mA: $\overline{DB0}$, to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$, I/O, $\overline{MSG}$, $\overline{SEL}$, $\overline{RST}$, $\overline{REQ}$, C/D (3)			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: All input pins	–25		+25	µA
Pull-up resistance	R_{UP}	IO0 to IO15, D0 to D7, $\overline{INT0}$, $\overline{INT1}$, ZSWAIT	40	80	160	kΩ

Note: The subcode-related pins in group (1) are not provided by the LC895124.

SCSI Pin Input Characteristics

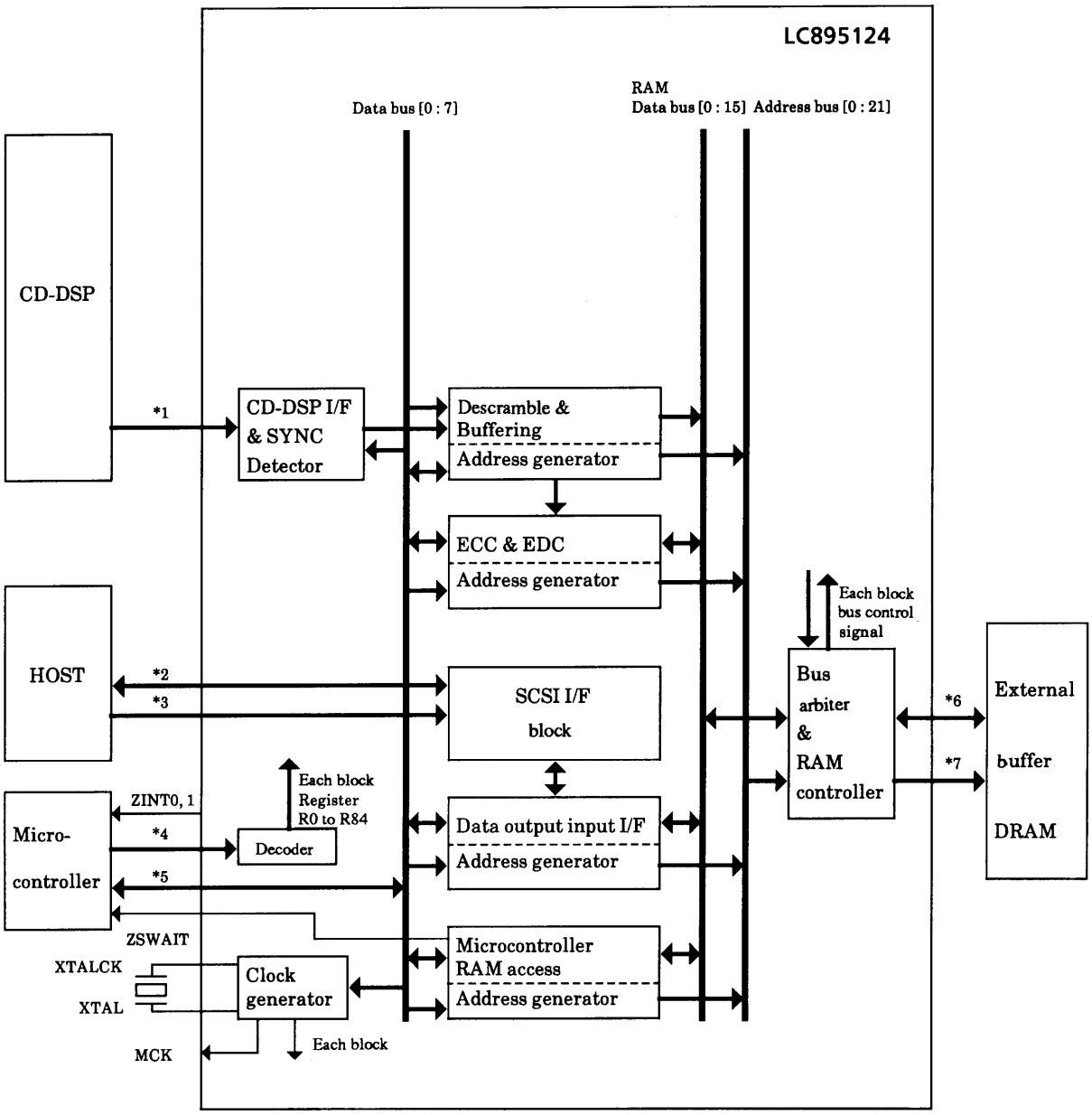
Parameter	Symbol	Conditions	min	typ	max	Unit
Input threshold voltage	V_{t+t1}	V_{DD} = 4.5 to 5.5 V		1.60	2.00	V
	V_{t-t1}		0.80	1.11		V
Hysteresis width	ΔV_{tt1}	V_{DD} = 5.0 V	0.41	0.49		V

Sample Recommended Oscillator Circuit



R1 = 120 kΩ
R2 = 47 Ω
C1 = 30 pF
Crystal oscillator frequencies: XTALCK0 = 16.9344 MHz and XTALCK1 = 20 MHz
or:
R1 = 3.3 kΩ
R2 = None
C1 = 5 pF
Crystal oscillator frequency: XTALCK0 = 33.8688 MHz
If third harmonic overtones appear when using a 33.8688 MHz frequency with the recommended circuit example, consult with the manufacturer of the crystal element, since detailed values of the circuit constants will be influenced by the printed circuit board.

Block Diagram



Note: 1 BCK, SDATA, LRCK, C2PO
2. $\overline{DB0}$ to $\overline{DB7}$, $\overline{DBP}$, $\overline{BSY}$, $\overline{MSG}$, $\overline{SEL}$, $\overline{RST}$, $\overline{REQ}$, I/O, C/D
3. $\overline{ACK}$, $\overline{ATN}$
4. ZRD, ZWR, SUA0 to SUA6, ZCS, CSCTRL
5. D0 to D7
6. IO0 to IO15
7. RA0 to RA16, ZRAS0, ZRAS1, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE

Note: IO8 to IO15 and RA9 to RA16 are the same pins.
Subcode pins are connected to CD-DSP or to V_{SS}.

Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
1	V_{SS0}	P	
2	V_{SS0}	P	
3	V_{SS0}	P	
4	V_{SS0}	P	
5	ZRAS0	O	Buffer RAM RAS signal output pin 0 (Normally, pin 0 is used)
6	ZRAS1	O	Buffer RAM RAS signal output pin 1
7	ZCAS0	O	Buffer RAM CAS signal output pin 0 (Normally, pin 0 is used)
8	ZCAS1	O	Buffer RAM CAS signal output pin 1
9	ZOE	O	Buffer RAM output enable
10	ZUWE	O	Buffer RAM upper write enable
11	ZLWE	O	Buffer RAM lower write enable
12	V_{SS0}	P	
13	RA0	O	Buffer RAM address signal outputs
14	RA1	O	
15	RA2	O	
16	RA3	O	
17	RA4	O	
18	V_{DD}	P	
19	V_{SS0}	P	
20	RA5	O	Buffer RAM address signal outputs
21	RA6	O	
22	RA7	O	
23	RA8	O	
24	RA9 (IO15)	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
25	RA10 (IO14)	B	
26	RA11 (IO13)	B	
27	RA12 (IO12)	B	
28	V_{SS0}	P	
29	RA13 (IO11)	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
30	RA14 (IO10)	B	
31	RA15 (IO9)	B	
32	RA16 (IO8)	B	
33	IO7	B	Buffer RAM data I/O. The pin circuit includes a pull-up resistor.
34	IO6	B	
35	IO5	B	
36	V_{SS0}	P	
37	V_{DD}	P	
38	IO4	B	Address outputs for the buffer RAM or data I/O pins The pin circuits include pull-up resistors.
39	IO3	B	
40	IO2	B	
41	IO1	B	
42	IO0	B	
43	V_{SS0}	P	
44	XTALCK0	I	Crystal oscillator input
45	XTAL0	O	Crystal oscillator output
46	V_{DD}	P	
47	MCK	O	Outputs the XTALCK0 frequency, or that frequency divided by 2.
48	TEST0	I	Test pins. These pins must be connected to V_{SS0}.
49	TEST1	I	
50	TEST2	I	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
51	TEST3	I	Test pins. These pins must be connected to V_{SS0}.
52	TEST4	I	
53	ZRESET	I	LSI reset. The LSI is reset on a 0 input.
54	V_{DD}	P	
55	V_{SS0}	P	
56	CSCTRL	I	Selects active-high or active-low for the microcontroller CS logic.
57	X1EN	I	Selection pin that must be set to 1 when XTALCK1 is used.
58	XTALCK1	I	SCSI block oscillator circuit input. Selected by X1EN.
59	XTAL1	O	SCSI block oscillator circuit output.
60	ZSWAIT	O	WAIT signal output to the microcontroller
61	V_{DD}	P	
62	V_{SS0}	P	
63	D0	B	Microcontroller data signals
64	D1	B	
65	D2	B	
66	D3	B	
67	D4	B	
68	D5	B	
69	D6	B	
70	D7	B	
71	ZRD	I	Microcontroller data read signal input
72	V_{SS0}	P	
73	V_{DD}	P	
74	ZWR	I	Microcontroller data write signal input
75	ZCS	I	Input for the register chip select signal from the microcontroller
76	SUA0	I	Register chip select signal from the microcontoller
77	SUA1	I	
78	SUA2	I	
79	SUA3	I	
80	SUA4	I	
81	SUA5	I	
82	SUA6	I	
83	ZINT0	O	Interrupt request output to the microcontroller (ECC side. Set with a register.)
84	ZINT1	O	Interrupt request output to the microcontroller (SCSI side. Set with a register.)
85		NC	
86		NC	
87		NC	
88		NC	
89		NC	
90	V_{DD}	P	
91	V_{SS1}	P	
92		NC	
93		NC	
94		NC	
95	$\overline{DB0}$	B	SCSI connection
96	V_{SS1}	P	
97	$\overline{DB1}$	B	SCSI connection
98	$\overline{DB2}$	B	
99	V_{SS1}	P	
100	$\overline{DB3}$	B	SCSI connection

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Symbol	Type	Function
101	$\overline{DB4}$	B	SCSI connection
102	V_{SS1}	P	
103	$\overline{DB5}$	B	SCSI connection
104	$\overline{DB6}$	B	
105	V_{SS1}	P	
106	$\overline{DB7}$	B	SCSI connection
107	$\overline{DBP}$	B	
108	V_{SS1}	P	
109	V_{DD}	P	
110	$\overline{ATN}$	B	SCSI connection
111	$\overline{BSY}$	B	
112	V_{SS1}	P	
113	$\overline{ACK}$	B	SCSI connection
114	$\overline{RST}$	B	
115	V_{SS1}	P	
116	$\overline{MSG}$	B	SCSI connection
117	$\overline{SEL}$	B	
118	V_{SS1}	P	
119	C/D	B	SCSI connection
120	$\overline{REQ}$	B	
121		NC	
122		NC	
123		NC	
124	V_{SS1}	P	
125	I/O	B	SCSI connection
126	V_{DD}	P	
127	V_{SS0}	P	
128		NC	
129		NC	
130		NC	
131		NC	
132		NC	
133		NC	
134	V_{SS0}	P	
135	V_{SS0}	P	
136	V_{SS0}	P	
137		NC	
138		NC	
139	C2PO	I	CD-DSP interface
140	SDATA	I	
141	BCK	I	
142	LRCK	I	
143		NC	
144	V_{DD}	P	

Note: 1. NC pins must be left open. Do not connect any signal to these pins.
2. Pin names that start with Z are negative-logic signals.
3. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground.
4. Applications that use DRAM must insert resistors in the CAS and RAS lines, connect capacitors between these lines and ground, and take any other measures necessary to prevent undershoot in the DRAM related circuits.
5. Since these circuits include buffers that sink 48 mA, adequate noise prevention measures must be applied.

Pin Functions

1. SCSI Pins
   - $\overline{\text{BSY}}$, $\overline{\text{ACK}}$, $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{REQ}}$, $\overline{\text{ATN}}$, I/O, C/D (input and output)
     SCSI bus control pins.

   - $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBPB}}$ (input and output)
     These are the SCSI data bus pins.

2. Microcontroller Interface Pins
   - ZCS (input)
     Microcontroller chip select line
   - CSCTRL (input)
     Microcontroller chip select logic selection signal
     High - ZCS is an active low signal.
     Low - ZCS is an active high signal.
   - ZRD, ZWR, SUA0 to SUA6 (input)
     Microcontroller interface control signal
     The SUA0 to SUA6 pins are used for addressing.
   - ZSWAIT (output)
     When the microcontroller accesses RAM, it must wait if this pin is low.
     This is a built-in pull-up resistor open drain output.
   - D7 to D0 (input and output)
     Microcontroller data bus. Pull-up resistors are built in.
   - ZINT0, ZINT1 (output)
     Interrupt request output to the microcontroller. A SCSI-side interrupt can be output from ZINT1 by setting the C register (bit 7 in R11).
     This is a built-in pull-up resistor open drain output.

3. Buffer RAM Pins
   - IO0 to IO15 (input and output)
     Buffer RAM data bus. Pull-up resistors are built in. The IO8 to IO15 pins have shared functions as the RA9 to RA16 pins.
     This means that 16-bit PSRAM cannot be used.
   - RA0 to RA16 (output)
     Buffer RAM address lines. RA9 to RA16 have shared functions as the IO8 to IO15 pins.
     This means that 16-bit PSRAM cannot be used.
   - ZRAS0, ZRAS1, (ZCS0), (ZCS1) (output)
     Buffer DRAM RAS outputs. Normally, ZRAS0 is used. However, when two 1-MB (64k × 16-bit) DRAM chips are used, the respective DRAM RAS pins are connected to ZRAS0 and ZRAS1. Connected to the CS pin if PSRAM is used.
   - ZCAS0, ZCAS1 (output)
     Buffer DRAM CAS outputs. Normally, ZCAS0 is used. However, when two 1-MB (64k × 16-bit) DRAM chips are used, the respective DRAM CAS pins are connected to ZCAS0.
   - ZOE (output)
     Buffer RAM read output signal
   - ZUWE, ZLWE (output)
     Buffer RAM write output signals. Connected to the corresponding pins on the RAM chip.
     Leave ZUWE open if an 8-bit RAM is used.

4. CD DSP Data Pins
   - BCK, SDATA, LRCK, C2PO (input)
     The LC895124 reads in CD-ROM data over these pins connected to a CD DSP.
     C2PO is the C2 flag pin.

5. Other Pins
   - ZRESET (input)
     Reset input to the LC895124. The LC895124 is reset by a low-level input.
     This pin must be held low for a period of at least 1 μs when power is first applied.
   - XTALCK0, XTAL0
     The main clock for the ECC and SCSI blocks. These pins support frequencies from 16.9344 to 25 MHz.
     When a double-frequency input is used, these pins accept frequencies up to 38 MHz.
     Use a double-frequency input when a ceramic oscillator and DRAM are used.
     (This is because the internal clock must have a 50% duty.)
     An external clock may input to the XTALCK pin.
     The SCSI block main clock can also be provided from XTALCK1 and XTAL1 if so specified by the setting of X1EN (pin 89).
   - XTALCK1, XTAL1
     The main clock for the ECC and SCSI blocks. These pins are enabled for oscillator operation by setting X1EN (pin 89). The LC895124 is designed so that the ECC and SCSI blocks can also be operated asynchronously.
     This means that precise 10-MB/s synchronous transfers can be achieved by providing a 20-MHz input to XTALCK1 and XTAL1.
     A ceramic oscillator may be used here since only the rising edge of this signal is used.
     In applications that do not use these pins, XTALCK1 must be tied to V_{SS} and XTAL1 must be left open.
   - X1EN (input)
     Set this pin to 1 to us use XTALCK1 and XTAL1 for the SCSI block main clock.
     Set this pin to 0 to drive both the ECC and SCSI blocks from XTALCK0 and XTAL0.
   - MCK (output)
     Outputs either the XTALCK0 frequency or that frequency divided by 2. This pin's output can also be stopped if desired.