TELECOM PRODUCTS

DATABOOK

TELECOM PRODUCTS

3rd EDITION

INCLUDING AT&T LINEAR BIPOLAR AND HIGH VOLTAGE DEVICES

TELECOM PRODUCTS

3rd EDITION

July 1986

This third edition of the SGS Telecom Products databook contains datasheet for some ninety products — double the number in the previous edition — realized with bipolar, CMOS & NMOS technologies. All of these products are designed specifically for applications in the telecommunications field.

With the addition of the latest devices, SGS now offers solutions for the most important telecom subsystems: telephone sets, digital switching systems and PABXs.

In addition to the original SGS product range, this databook also includes the range of products available from SGS through an agreement with AT&T, which has extended the range of applications covered.

Among the most recently-designed telecom ICs, two highlights are the SGS SLIC, which integrates the ringing function, and a PCM Conference Call chip, both of which are unrivalled of the market in terms of performance and system approach.

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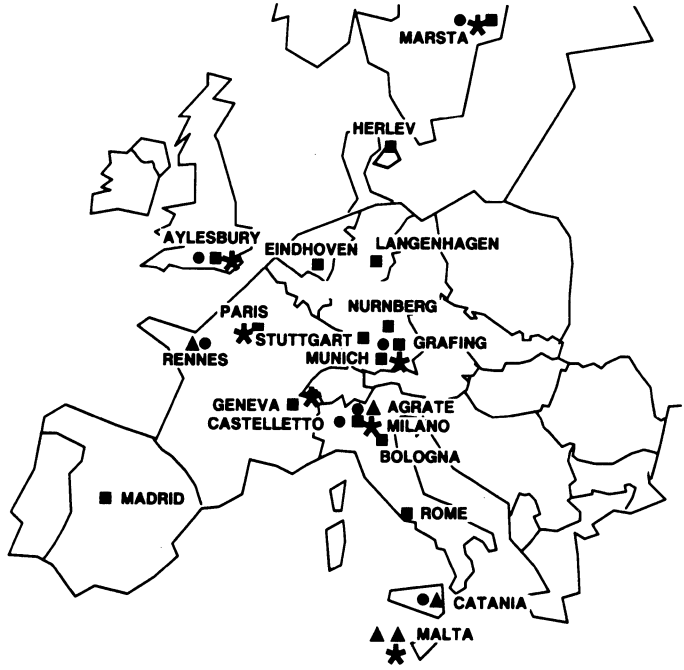
IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with billings over 300 million dollars and employing over 9500 people.

The SGS Group of Companies has now reached a total of 11 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Sweden, Switzerland, United Kingdom and the USA.

To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

SGS IN EUROPE



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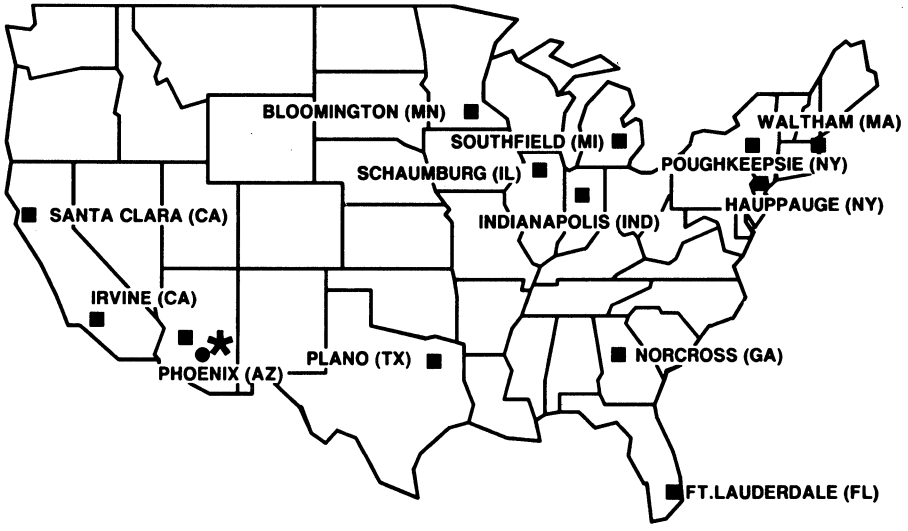

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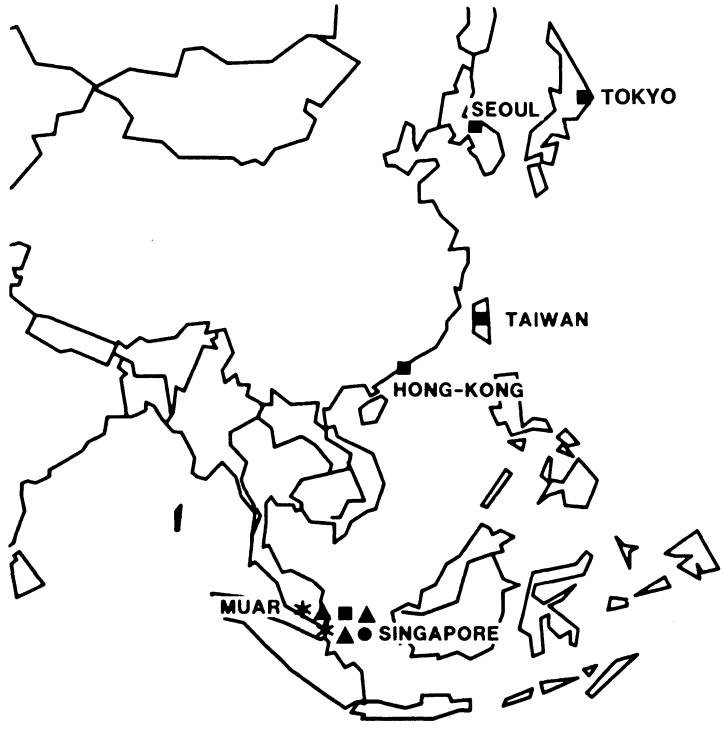

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TELEPHONE SET

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SMALL SIGNAL TRANSISTORS

Polar.	Max ratings			Type	Characteristics				Page
	V_{CEO} (V)	I_C (mA)	P_{tot} (mW)		f_T (MHz)	NF (dB)	and P_G (dB)	@ f (MHz)	
NPN	15	25	200	**BFY90**	1400	4.5	8	800	673
NPN	15	50	200	**2N3600**	1000	3	—	60	677
NPN	15	50	200	**2N918**	900	3.5	22	200	677
NPN	15	50	200	**BFX73**	900	6	—	60	677
PNP	25	50	225	**BFR99A**	2300	3.5	8	800	669
NPN	20	200	600	**2N3137**	750	—	7	250	681
NPN	30	200	800	**BFR36**	1000	4	16	200	665
NPN	20	400	1000	**2N5109**	1400	3	14	200	685

DATASHEETS

L545

ADVANCE DATA

ACTIVE TRUNK TERMINATION CIRCUIT

- TYPICAL APPLICATIONS IN VOICE-BAND MODEMS.
- ON CHIP POLARITY GUARD
- MEET DC LINE CHARACTERISTICS OF EITHER CCITT AND EIA RS 464 SPECS
- PULSE FUNCTION
- HIGH AC IMPEDANCE
- OFF HOOK-STATUS DETECTION OUTPUT
- LOW EXTERNAL COMPONENT COUNT
- MINIDIP DIL PACKAGE
- CIRCUIT DESCRIPTION

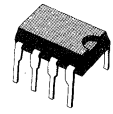
The circuit provides DC loop termination for analog trunk lines.

The V-I characteristics is equivalent to a fixed voltage drop (zener like characteristic) in series with an external resistance that determines the slope of the DC characteristic.

An external low voltage electrolytic capacitor causes the circuit to exhibit a very high impedance to all AC signal above a minimum frequency that is determined by the capacitor itself and by a 50KΩ nominal resistor integrated on the chip.

The off-hook status is detected all the time a minimum of 10mA is flowing into the circuit. In this condition a constant current generator is activated to supply an external device (typically an optocoupler without affecting the AC characteristic of the circuit.

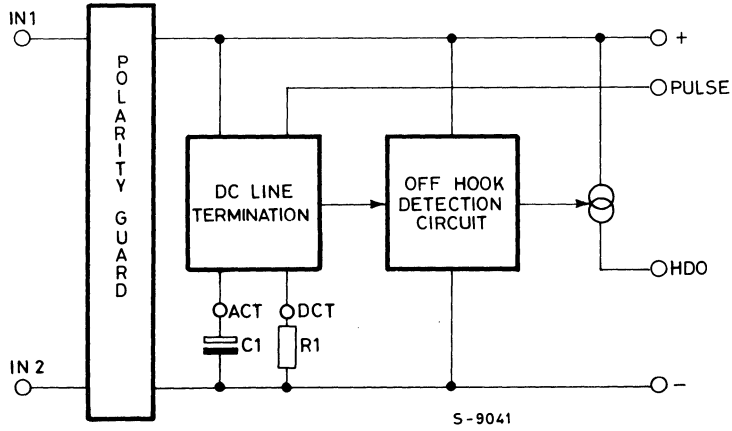
When pulse dialing is required, the PULSE input high causes the device to exhibit a pure resistive impedance characteristic. Levels are TTL compatible.



Minidip Plastic

ORDERING NUMBER: L545

BLOCK DIAGRAM

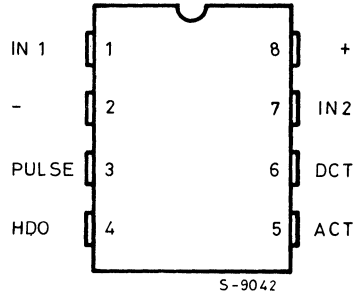


L545

ABSOLUTE MAXIMUM RATINGS

V_1	Max line voltage (pulse duration 10ms max.)	20	V
I_1	Max line current	150	mA
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	800	mW
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

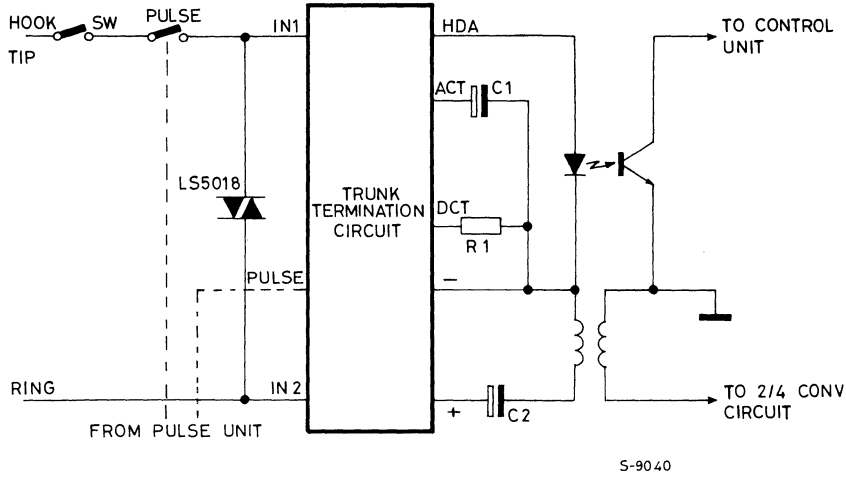
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS
(I_1 = 5 to 100mA; T_{amb} = -25 to +60°C; f = 1KHz; unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_1	Line Voltage	I_1 = 10mA I_1 = 20mA I_1 = 125mA R_1 = 60Ω			4.5 5.1 11.5	V
Z	AC impedance	C_1 = 2.2μF	35			KΩ
I_{ofh}	Off-Hook current detection threshold		10			mA
I_o	Off-Hook output drive current	I_1 = 10mA min. I_1 = 20mA	1 2			mA

APPLICATION INFORMATION

With the use of this circuit it is possible to terminate an analog trunk so that all the DC current component is flowing in the TRUNK TERMINATION CIRCUIT while the AC component is decoupled with a low voltage capacitor and can be used with a small and low cost audio coupler transformer to provide the AC balancing termination and two to four wire conversion. Figure 1 gives the typical application circuit; it is worth to note that the TRUNK TERMINATION CIRCUIT, together with the LS5018 transient suppressor provides a compact and low cost module fully protected against lightning or overvoltages frequently present on telephone lines. The PULSE input, when high, allows the device to show a resistive impedance equal to R1 to the line.



L3100

PRELIMINARY DATA

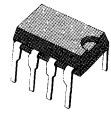
TRANSIENT VOLTAGE / CURRENT SUPPRESSOR

- BREAKOVER VOLTAGE LARGELY INDEPENDENT OF TRANSIENT RISE TIME
- HIGH CURRENT CAPABILITY
- PROGRAMMABILITY BOTH IN VOLTAGE AND CURRENT
- VERY HIGH OFF STATE RESISTANCE
- VERY HIGH ON STATE CONDUCTANCE
- AUTOMATIC RECOVERY
- CHARACTERISTICS LARGELY INDEPENDENT OF AGEING
- FAILSAFE OPERATION
- CAN BE USED ON REMOTE – SUPPLY LINES

The L3100 is a transient overvoltage suppressor/ overcurrent arrester designed to protect sensitive components in electronic telephones and telecommunications equipment against transients caused by lightning, induction from power lines, etc.

The L3100 characteristic, that is its firing voltage and current, can be easily programmed by means of inexpensive external components; more over, since this device recoveres automatically when the surge current falls below a fixed holding current, it may be used on remotely supplied lines. Finally, if destroyed, it becomes a permanent short circuit.

The device is encapsulated in 4 + 4 power minidip with copper frame



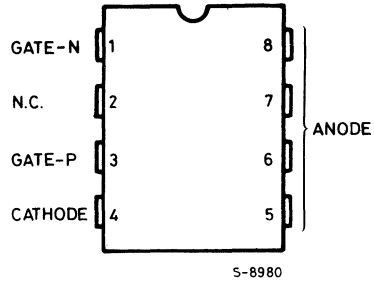
Minidip Plastic

ORDERING NUMBER: L3100B

ABSOLUTE MAXIMUM RATINGS

I_{TS}	Transient current (T1/T2 = 1μs/50μs pulse - see fig. 1a)	250	A
	(T1/T2 = 1μs/1000μs pulse - see fig. 1a)	150	A
I_p	Non repetitive peak current (one sine wave 50 Hz, 30 sec interval - see fig. 1b)	50	A
I_p	Repetitive peak current (50 Hz, 1 sec - see fig. 1c)	20	A
P_{tot}	Total power dissipation at T_{amb} = 50°C (steady state)	1.2	W
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM

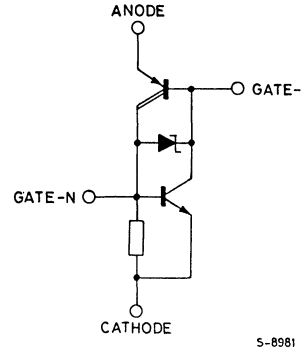


Fig. 1 - Waveforms

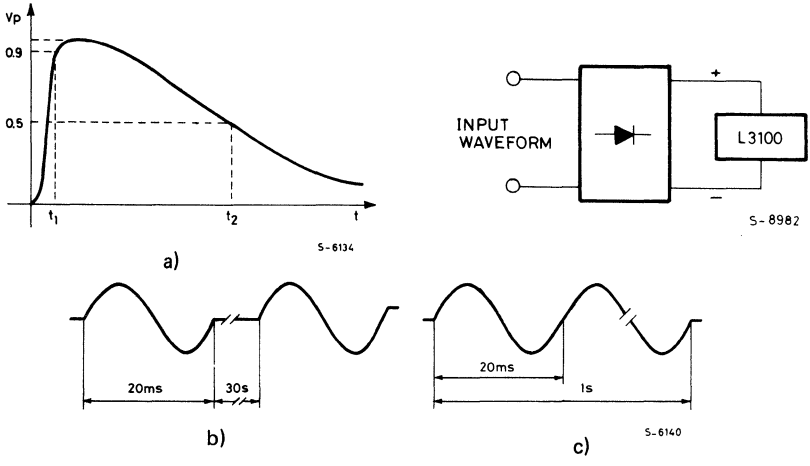
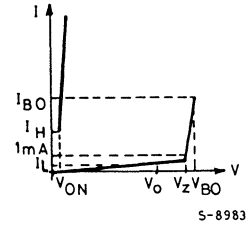


Fig. 2 - Voltage current characteristics (gate not connected)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction temperature	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pin	max	20	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to test circuit and volt/amp characteristics

T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
OPERATION WITHOUT GATE						
I_L	Direct leakage current	V_o = 60V V_o = 250V T_{amb} = 70°C			7 50	μA μA
I_R	Reverse leakage current	V = 0.7V			1	mA
V_Z	Zener voltage	I_Z = 1 mA	265		310	V
I_{BO}	Firing current		200		500	mA
V_{BO}	Static breakover voltage	$I_{A\text{-}C}$ = 1A; 50 Hz half wave			350	V
V_{BOdyn}	Dynamic breakover voltage	$I_{A\text{-}C}$ = 100A; 1/50 μs			400	V
V_{ON}	ON state voltage	I = 1A			3	V
I_H	Holding current	T_{amb} = 55°C; 300 μs pulse	250			mA
R_{ON}	On state diff. resistance	I = 1 to 5A			0.25	Ω
C_{OFF}	OFF state capac.				100	pF
OPERATION WITH GATES						
V_{GP}	Gates voltage	I_G = 200 mA	0.6		1.2	V
V_{RGP}	Reverse gate-P voltage	I_G = -1 mA	0.7			V
I_{GP}	Firing gate-P curr.	$V_{A\text{-}C}$ = 100V			50	mA
I_{GN}	Firing gate-N current	$V_{A\text{-}C}$ = 100V	100		200	mA

CIRCUIT DESCIPTION

- The L3100 is to be connected between the two line wires, in parallel with the protected devices
- As it is mono-directional, it has to be put after a rectifier bridge.
- When the vorking voltage and current are below the threshold values, the device is in OFF state condition and shows a very high impedance with less than 5 microAmp leakage current at 250V and ambient temperature.
- As the thresholds are reached L3100 switches ON in about a hundred nanoseconds and behaves like a short circuit standing transients up to 200A and repetitive sinusoidal peaks to 20A.
- When the transient current falls below the holding current (I_H), the device returns automatically to the OFF state. The holding current is high enough to allow operation on remote feed lines.
- If the device fails it become a short circuit. providing protection and indicating that a failure has occurred.

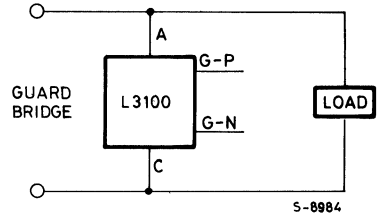
GATES OPERATION

- In the open-gate configuration the breakover level is set at about 280V due to an internal zener.
- Furthermore the threshold voltage can be programmed at any value, below 265V, with a proper zener diode connected to the gates.
- In the gate-controlled configuration the device can operate also as a current transient arrester providing, unique up to now, both series and shunt protection.
  The protected circuit is fed through a resistance connected between the anode (+) and the gate-P. When the voltage across the two leads exceeds 0.8V, depending on line current and resistance values, the device switches ON shorting the line.

TYPICAL APPLICATIONS

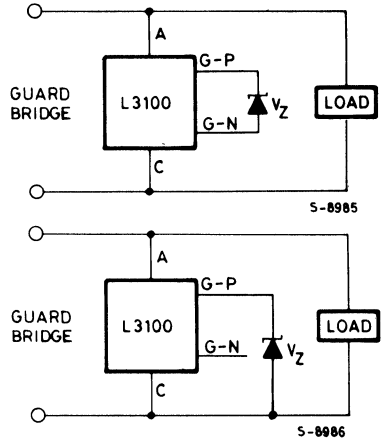
- The L3100 can be used in several configurations.
- In any case, as it is a mono directional device, it must be connected to the line through a rectifier bridge.
- Warning – degradation may occur when polarizing L3100 inversely (more than 10 volts).
- In the basic open gate configuration (fig. 3), it switches on at about 280V.

Fig. 3



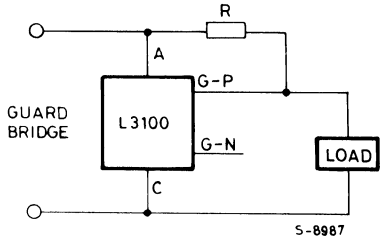
- In the gate controlled operation it can be connected to program either.
- The breakover voltage (figg. 4).
- The maximum load current (fig. 5).
- Both of them (figg. 6)

Figg. 4 - (a and b) ($V_{BO} = V_Z$)

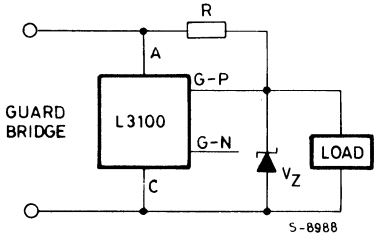


TYPICAL APPLICATIONS (continued)

Fig. 5 - $I_{BO} = \frac{V_{gate}}{R1} + Igate$



Figg. 6



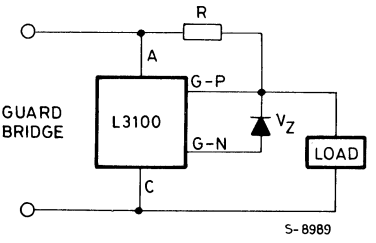
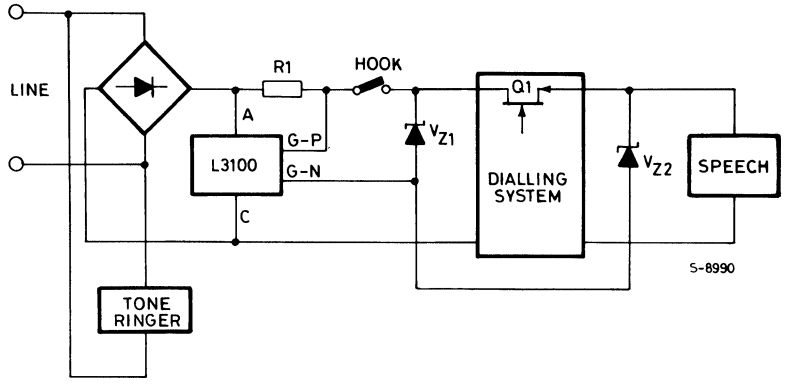


Fig. 7



– A schematic full protection configuration is shown in (fig. 7) where:

a) The internal breakover (280V) protects the tone ringer with the hook on.

b) The breakover of L3100 in dialling operation (Q1 open) is set by V_{Z1}.

c) As in speech operation it's fixed by V_{Z2} (18 to 20V).

d) The current threshold into the load for the L3100 switching on is about

$\frac{V_{gate}}{R} + Igate$ with V_{BE}= 800 mV (typ) and Igate= 50 mA

L3101

PRELIMINARY DATA

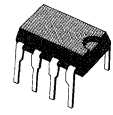
TRANSIENT VOLTAGE/CURRENT SUPPRESSOR

- BREAKOVER VOLTAGE LARGELY INDEPENDENT OF TRANSIENT RISE TIME
- HIGH CURRENT CAPABILITY
- PROGRAMMABILITY BOTH IN VOLTAGE AND CURRENT
- VERY HIGH OFF STATE RESISTANCE
- VERY HIGH ON STATE CONDUCTANCE
- AUTOMATIC RECOVERY
- CHARACTERISTICS LARGELY INDEPENDENT OF AGEING
- FAILSAFE OPERATION
- CAN BE USED ON REMOTE – SUPPLY LINES

The L3101 is a transient overvoltage suppressor/overcurrent arrester designed to protect sensitive components in electronic telephones and telecommunications equipment against transients caused by lightning, induction from power lines, etc.

The L3101 characteristic, that is its firing voltage and current, can be easily programmed by means of inexpensive external components; more over, since this device recoveres automatically when the surge current falls below a fixed holding current, it may be used on remotely supplied lines. Finally, if destroyed, it becomes a permanent short circuit.

The device is encapsulated in 4 + 4 power minidip with copper frame.



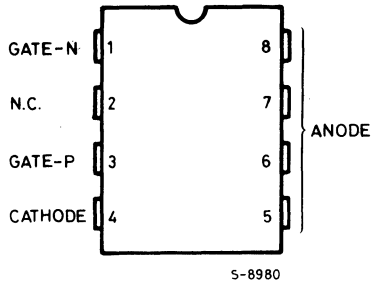
Minidip Plastic

ORDERING NUMBER: L3101

ABSOLUTE MAXIMUM RATINGS

I_{TS}	Transient current (T1/T2 = 1μs/50μs pulse - see fig. 1a)	500	A
	(T1/T2 = 1μs/1000μs pulse - see fig. 1a)	150	A
I_p	Non repetitive peak current (one sine wave 50Hz, 30s interval - see fig. 1b)	50	A
I_p	Repetitive peak current (50Hz, 1s - see fig. 1c)	20	A
P_{tot}	Total power dissipation at $T_{amb} = 50°C$ (steady state)	1.2	W
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM

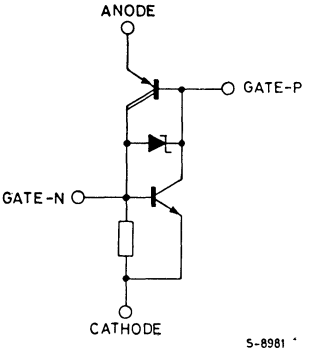


Fig. 1 - Waveforms

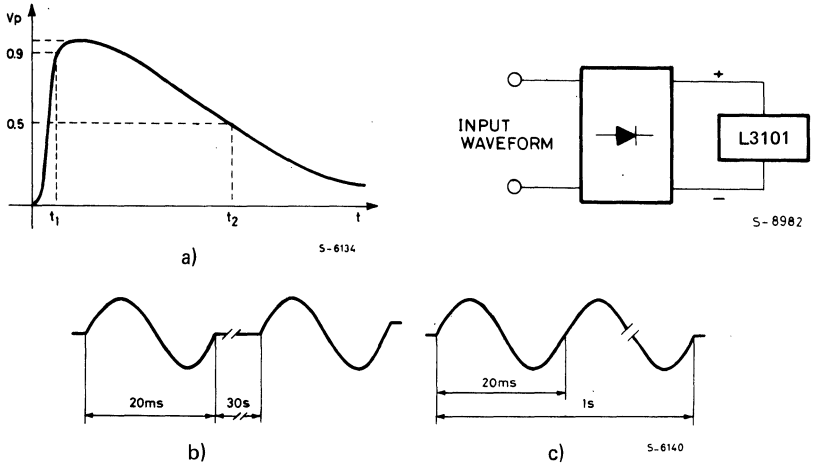
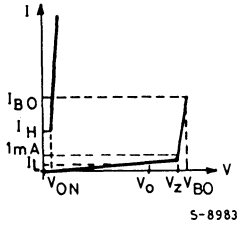


Fig. 2 - Voltage current characteristics (gate not connected)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction temperature	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pin	max	20	°C/W

ELECTRICAL CHARACTERISTICS (Refer to test circuit and volt/amp characteristics T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
OPERATION WITHOUT GATE						
I_L	Leakage current	V_o = 60V V_o = 90V T_{amb} = 70°C			7 10	μA μA
V_Z	Zener voltage	I_Z = 1mA	100	120	150	V
I_{BO}	Firing current		200		500	mA
V_{BO}	Breakover voltage	I = 1A			180	V
V_{ON}	ON state voltage	I = 1A			3	V
I_H	Holding current	T_{amb} = 55°C	150			mA
R_{ON}	ON state diff. resistance	I = 1 to 5A			0.25	Ω
C_{OFF}	OFF state capac.				100	pF
OPERATION WITH GATES						
V_G	Gates voltage	I = 200mA	0.6		1.2	V
I_{GP}	Firing gate-P current	$V_{A\text{-}C}$ = 60V			50	mA
I_{GN}	Firing gate-N current	$V_{A\text{-}C}$ = 60V	100		200	mA

CIRCUIT DESCRIPTION

- The L3101 is to be connected between the two line wires in parallel with the protected devices.
- As it is mono-directional, it has to be put after a rectifier bridge.
- When the working voltage and current are below the threshold values, the device is in OFF state condition and shows a very high impedance with less than 10μA leakage current at 90V and ambient temperature.
- As the thresholds are reached L3101 switches ON in about 100ns and behaves like a short circuit standing transients up to 500A and repetitive sinusoidal peaks to 20A.
- When the transient current falls below the holding current I_H, device returns automatically to the OFF state. The holding current is high enough to allow operation on remote feed lines.
- If the device fails it become a short circuit, providing protection and indicating that a failure has occurred.

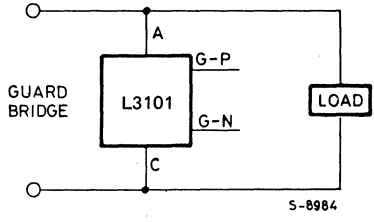
GATES OPERATION

- In the open-gate configuration the breakover voltage level is set at about 120V due to an internal zener.
- Furthermore the threshold voltage can be programmed at any value, below 120V with a proper zener diode added between the gate P and either cathode (-) or gate N.
- In the gate-controlled configuration the device can operate also as a current transient arrester providing, unique up to now, both series and shunt protection.
  The protected circuit is fed through a resistance connected between the anode (+) and the gate-P. When the voltage across the two leads exceeds 0.8V, depending on line current and resistance values, the device switches ON shorting the line.

TYPICAL APPLICATIONS

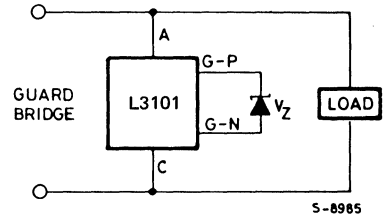
- The L3101 can be used in several configurations.
- In any case, as it is a mono directional device, it must be connected to the line through a rectifier bridge.
- Warning – degradation may occur when polarizing L3101 inversely (more then 10V).
- In the basic open gates configuration (fig. 3), it switches on at about 120V.

Fig. 3



- In the gate controlled operation it can be connected to program either.
- The breakover voltage (figg. 4)
- The maximum load current (fig. 5)

Figg. 4 - (a and b) ($V_{BO} = V_Z$)



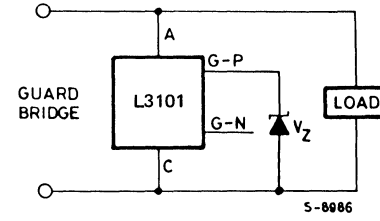
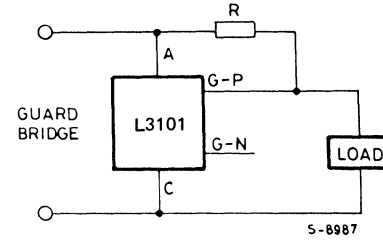


Fig. 5 - $I_{BO} = \frac{V_{gate}}{R} + I\ gate$



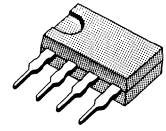
L3121
L3122

PRELIMINARY DATA

FULL FEATURES TRANSIENT SUPPRESSORS

- BREAKOVER VOLTAGE LARGELY INDEPENDENT OF TRANSIENT RISE TIME
- BIDIRECTIONAL OPERATION
- INDEPENDENT/ASYMMETRICAL PROGRAMMABILITY
- PARALLEL OVERVOLTAGE PROTECTION (PROGRAMMABLE)
- SERIAL OVERCURRENT PROTECTION (PROGRAMMABLE)
- VERY HIGH CURRENT CAPABILITY
- VERY HIGH OFF STATE RESISTANCE
- VERY HIGH ON STATE CONDUCTANCE
- AUTOMATIC RECOVERY
- CHARACTERISTIC LARGELY INDEPENDENT AGEING
- FAILSAFE OPERATION
- FOR USE ON REMOTE - SUPPLY LINES

The L3121 and L3122 are bidirectional transient overvoltage/overcurrent protections derived from the programmable L3101 to provide full feature protection for the subscriber line interface (L3121) and for the standard telephone set (L3122).
Full programmability is allowed through access to the triggering gate available on the chips. The L3121 protects the line to ground either against positive or negative transients with external and independent adjustment of the threshold voltages (zener or external battery) in the two directions.
The L3122 provides a parallel and series protection in a four pole configuration ensuring both modes of operation fully programmable below the built in levels.



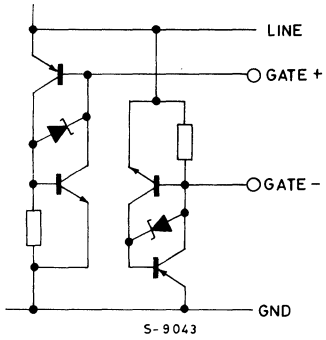
SIP-4

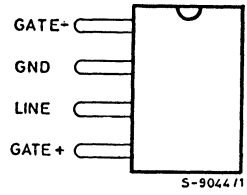
ORDERING NUMBER: L3121
L3122

ABSOLUTE MAXIMUM RATINGS

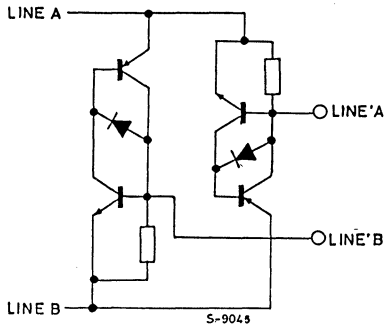
I_{TS}	Transient current (T1/T2 = 1μs/50μs pulse - see fig. 1a)	500	A
	(T1/T2 = 1μs/1000μs pulse - see fig. 1a)	150	A
I_p	Non repetitive peak current (one sine wave 50Hz, 30s interval - see fig. 1b)	50	A
I_p	Repetitive peak current (50Hz, 1s - see fig. 1c)	20	A
P_{tot}	Total power dissipation at $T_{amb} = 50°C$ (steady state)	1.2	W
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK and CONNECTION DIAGRAMS
for L3121





for L3122



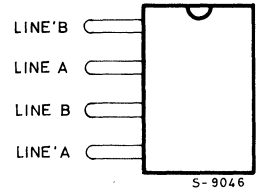
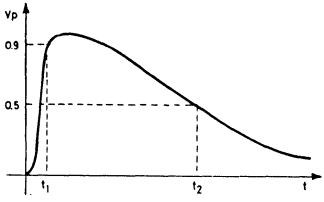
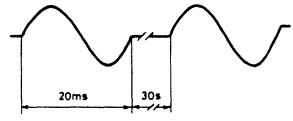


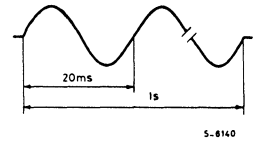
Fig. 1 - Waveforms



(a)

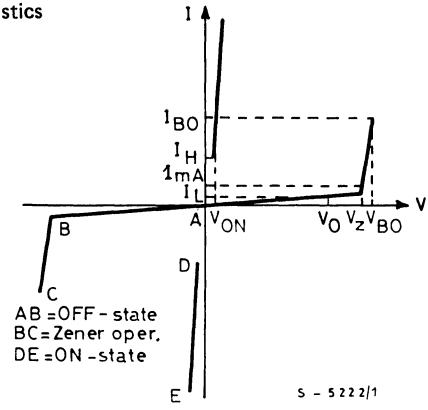


(b)



(c)

Fig. 2 - Voltage current characteristics



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pin	max	20	°C/W

ELECTRICAL CHARACTERISTICS (Refer to test circuit and volt/amp characteristics T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Unit
OPERATION WITHOUT GATE						
I_L	Leakage current	V_o = 60V V_o = 90V T_{amb} = 70°C			7 10	µA µA
V_Z	Zener Voltage	I_Z = 1mA	100	120	150	V
I_{BO}	Firing current		200		500	mA
V_{BO}	Breakover voltage	I = 1A			180	V
V_{ON}	ON state voltage	I = 1A			3	V
I_H	Holding current	T_{amb} = 55°C	150			mA
R_{ON}	ON state diff. resistance	I = 1 to 5A			0.25	Ω
C_{OFF}	OFF state capacitance				100	pF
OPERATION WITH GATES						
V_G	Gates voltage	I = 200mA	0.6		1.2	V
I_{GP}	Firing gate-P current Gate+ (L3121 only)	$V_{LINE\text{-}GND}$ = 60V			50	mA
I_{GN}	Firing gate-N current Gate - (L3121) Both Line ' (L3122)	$V_{LINE\text{-}GND}$ = -60V $V_{LINE\ A\text{-}B}$ = +/- 60V	100		200	mA

L3211

ADVANCE DATA

VERY LOW VOLTAGE SPEECH CIRCUIT WITH DTMF INTERFACE

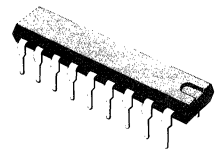
- SPEECH MODE DOWN TO 5mA/1.3V FOR PARALLEL OPERATION
- DTMF MODE DOWN TO 14mA
- A.C. BRIDGE CONFIGURATION ALLOWS ALL IMPEDANCES TO BE CONTROLLED CLOSELY
- DRIVES RECEIVERS OF 150Ω IMPEDANCE FOR REDUCED COST
- ON CHIP DTMF INTERFACE

The L3211 is a monolithic integrated circuit in 18 pin plastic DIP package suitable to replace the hybrid circuit in the telephone set. It works with magnetic capsules in receiving and with electret microphone in sending. With its very low voltage operation the L3211 is particularly suitable to work in parallel with conventional telephone sets.

In addition to speech operation, the L3211 acts as interface for the DTMF for both feeding and signaling functions.

The L3211 basic functions are the following:

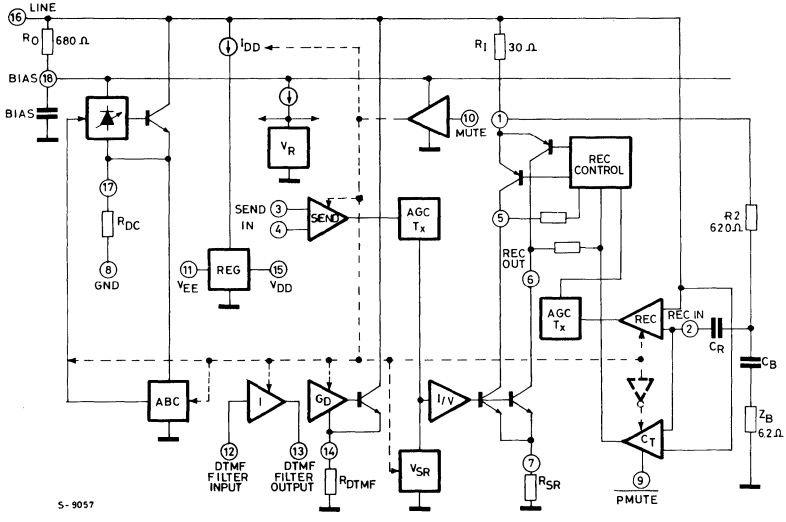
- To present the proper DC path for the line current (particular care has been paid to have very low voltage drop at low line current levels).
- To handle the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing the line current.
- To act as linear interface for the DTMF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated during the signaling.
- To feed with a constant voltage the electret microphone.



DIP-18 Plastic
(0.4)

ORDERING NUMBER: L3211

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

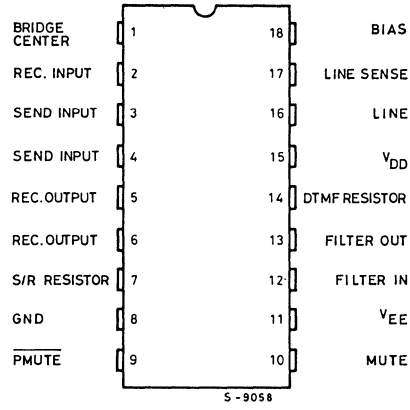
V_L	Line Voltege (3ms pulse duration)	20	V
I_L	Line Current	150	mA
P_{tot}	Total Power dissipation at $T_{amb} = 70°C$	1	W
T_{op}	Operating temperature	-20 to +55	°C
T_{stg}, T_j	Storage and Junction temperature	-60 to +150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

CONNECTION DIAGRAM

(Top view)



Electret Bias (V_{EE})
The electret is biased through a voltage generator at Pin 11.

DC Regulator
This stage provides the path for the DC line current (DC characteristics) through the external resistor R_{DC} to pin 17.

AGC (AGC T_X, AGC R_X)
The Automatic Gain Control is internally fixed for both T_X, and R_X sections. The AGC function is built with low distortion stages.

V_{DD}
A regulated voltage is available at Pin 15 for the bias of the DTMF generator. This stage has the following characteristics:

- When the line voltage drops lower then V_{DD}, the V_{DD} output follows the line voltage.
- The load is fed through a saturated NPN transistor. During pulse dialing when the I_C is disconnected from the line, the capacitor across the V_{DD} output is discharged only by the base-emitter leakage of the NPN transistor. This allows this capacitor to be used for "Keep Alive Memory" in pulse dialing application.

BLOCK DESCRIPTION (continued)

Sending/Receiving Stages
A differential input stage is available in sending. The sending/receiving gains are internally fixed. Nevertheless, sending gain can be adjusted by varying the electret bias and receiving gain can be adjusted by rearranging the external balancing network R_1, R_2, Z_B.

Confidence Level
A confidence level gain stage is built in parallel with the input receiving stage. During DTMF mode the C.L. gain stage is turned on and the input receiving stage is turned off. This permits a fixed amount of DTMF signal when receiving.

DTMF Amplifier and Filter
The DTMF transconductance output amplifier is available between pins 14 and 16. An external resistor at Pin 14 controls the amount of DTMF gain. A buffer stage for filtering an incoming DTMF gain. A buffer stage for filtering an incoming DTMF tone is provided between pin 12 and 13.

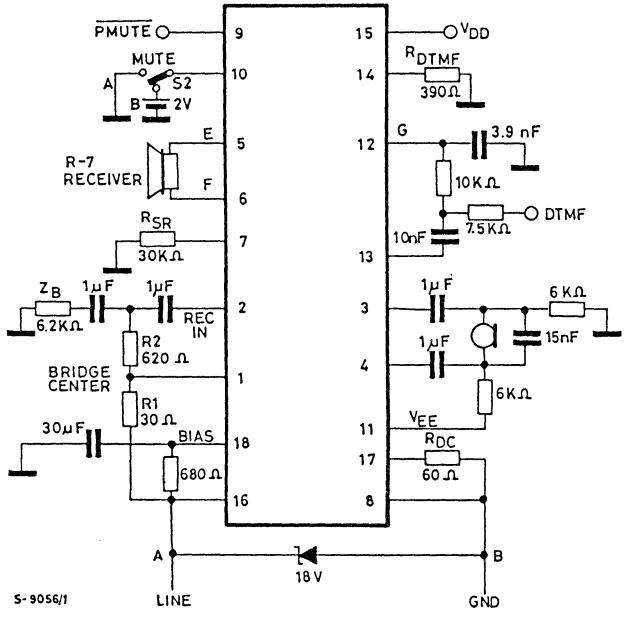
Mute
The functions performed by the mute (active high, pin 10) are:

- Mute of the sending path
- Reduction of the sending/receiving consumption.
- Increase of the source current at the regulated output V_{DD}.
- Increase of the line voltage.
- Switching of the ABC into the high current mode.
- Mute of the first stage in receiving.
- Turn on of the confidence level stage.
- Bias of the DTMF amplifier stage and filter.

$\overline{\text{Pmute}}$

When $\overline{\text{Pmute}}$ (Pin 9) is low the confidence level signal in receiving is muted.

Fig. 1 - Application and test circuit



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, f = 200 to 3400Hz, S2 in position (a) on the test circuit, unless otherwise specified).

Parameter		Test Conditions	Min	Typ	Max	Unit	Fig.
SPEECH OPERATION for I_L = 20mA to 125mA							
V_L	Line Voltage	I_L = 20mA I_L = 125mA			5.1 12	V V	
G_S	Sending Gain	f = 1KHz I_L = 42mA V_{MI} = 3mV I_L = 96mA	39 35		41 37	dB dB	2 2
	Sending Distortion	f = 1KHz V_{SO} = 700mV I_L = 20mA			2	%	2
	Sending Noise	V_{MI} = 0V		-70		dBmp	2
	Micro Input Impedance	V_{MI} = 3V	40			KΩ	
G_R	Receiving gain	V_{RI} = 0.3V I_L = 42mA f = 1KHz I_L = 96mA	-11 -15		-9 -13	dB dB	3 3
	Receiving Distortion	f = 1KHz V_{RO} = 440mV I_L = 20mA			2	%	3
	Receiving Noise	V_{RI} = 0		100		μV	3
	Receiving out impedance	V_{RO} = 50mV		30		Ω	
	Sidetone	f = 1KHz		36		dB	2
Z_{ML}	Line matching impedance	V_{RI} = 0.3V f = 1KHz		600		Ω	3
	Return Loss	V_{RI} = 0.3V f = 1KHz	-14			dB	3
V_{EE}	Electret Bias		2.4			V	
I_{EE}	Electret Supply Current		0.5			mA	
V_{DD}	DTMF Supply Voltage		2.4			V	
I_{DD}	DTMF Stand-by Supply Current		0.5			mA	
SPEECH OPERATION for I_L = 5mA to 20mA							
V_L	Line Voltage	I_L = 5mA			1.3	V	
V_{SO}	Sending dyn. input voltage	I_L = 5mA		100		mV_{rms}	
I_{RO}	Receiving dyn. output current	I_L = 5mA		0.8		mA	
V_{EE}	Electret bias	I_L = 5mA		0.7		V	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min	Typ	Max	Unit	Fig.
DTMF INTERFACE AND OPERATION I_L = 20mA to 125mA							
V_{DD}	DTMF Supply Voltage	S2 in (b)	2.4			V	
I_{DD}	DTMF Supply Current	S2 in (b)	2.5			mA	
V_{PI}	Sinusoidal Input pair level (Pin 12)	V_{DD} = 2.5V		3.4		V_{PP}	5
DTMF	Amplifier Gain	$f_{MF\ in}$ = 1KHz $V_{MF\ in}$ = 80mV	-3.3	-2.3	-1.3	dB	4
DTMF	Transient Voltage				V_L+5	V	
R_I	Input impedance	$V_{MF\ in}$ = 80mV	60			KΩ	
	Signal Tone Dist.	I_L = 14mA		2		%	
	Starting Delay Time				5	ms	
V_{IL}	Mute Input Low				1.0	V	
V_{IH}	Mute Input High		2.0			V	
V_{CL}	Conf. level gain $(20 \log_{10} \frac{V_{RO}}{V_{SO}})$		-24		-30	dB	
	Sending Gain Mute	V_{MI} = 3mV S2 in (b)		-60		dB	2
I_{LEAK} V_{DD}	Leakage	V_{DD} = 2.5V		2		nA	
DTMF INTERFACE AND OPERATION 14mA to 20mA							
I_b	Boost Current (Pin 12)			100		μA	
V_{SO}	Sinusoidal Output Levels	High Low		-9 -11		dBm dBm	
PULSE DIALING OPERATION							
I_{PL}	Input Low Current $\overline{Pmute}$				50	μA	
I_{LEAK}	Input High Current $\overline{Pmute}$				-10	μA	
	Confidence Level	Pmute Low		-40		dB	3

TEST CIRCUITS

Fig. 2

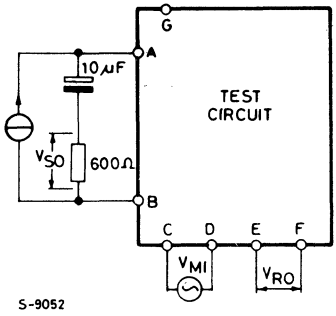


Fig. 3

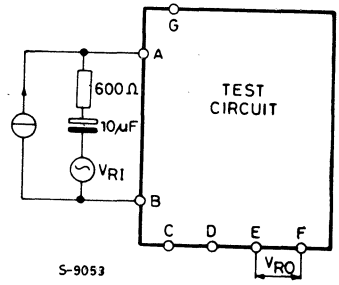


Fig. 4

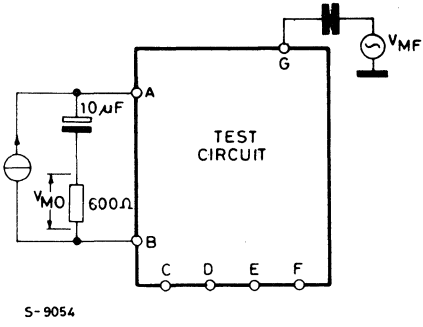
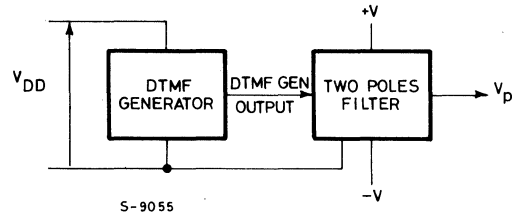


Fig. 5



L3212

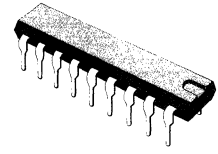
ADVANCE DATA

INTEGRATED TELEPHONE SPEECH TRANSMISSION CIRCUIT WITH DTMF INTERFACE

- ON CHIP DTMF AMPLIFIER/FILTER
- WORKS TO 14mA IN DTMF MODE, HENCE SUITABLE FOR USE ON CARRIER STATION
- DRIVES RECEIVERS OF 150Ω IMPEDANCE
- ON BOARD POWER SUPPLIES FOR ELECTRET POLARISATION AND DIALLER CHIP POWER
- LOOP-COMPENSATION START / STOP POINTS SELECTABLE ENABLING WORKING WITH DIFFERING EXCHANGE BATTERY VOLTAGES AND LINE CHARACTERISTICS
- DURING LONG LOOP DISCONNECT MODES i.e. 600ms FLASH TIMING, V_{DD} REGULATED VOLTAGE OUTPUT BECOMES HIGH IMPEDANCE ENSURING MINIMAL DISCHARGE OF 'KEEP ALIVE MEMORY' CAPACITOR
- WORKS IN SPEECH MODE TO 5mA/1.3V
- ALL IMPEDANCES CAN BE CONTROLLED BY AC BRIDGE CONFIGURATION
- DUAL LEVEL MUTING OF RECEIVER FOR DTMF AND LOOP-DISCONNECT DIALLING
- DTMF GAIN ADJUSTABLE TO SUIT SIGNALLING REQUIREMENTS
- RFL IS REDUCED BY INTERNAL BALANCED AMPLIFIERS
- ADJUSTABLE GAIN FOR SEND/RECEIVE

The L3212 is a monolithic integrated circuit in 18 pin plastic DIP package designed to replace the hybrid circuit in the telephone set. It works with magnetic capsules in receiving and with electret microphone in transmitting. With its very low voltage operation, the L3212 is particularly suitable to work in parallel with conventional telephone sets.

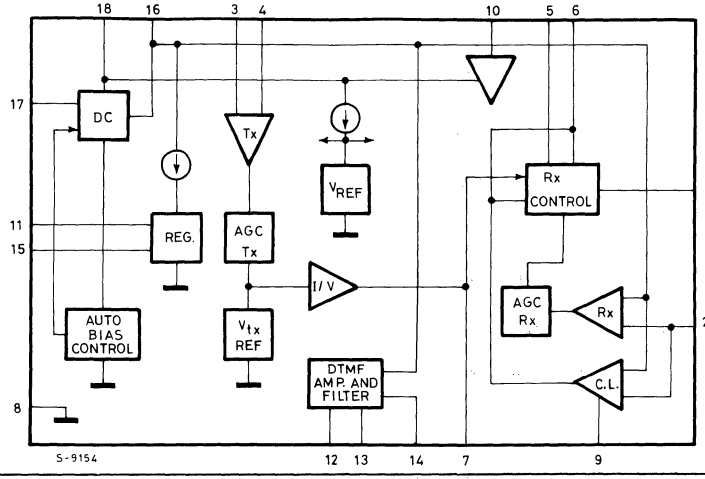
In addition to the speech operation, the L3212 acts as an interface for the DTMF for both feeding and signalling functions.



DIP-18 Plastic
(0.4)

ORDERING NUMBER: L3212

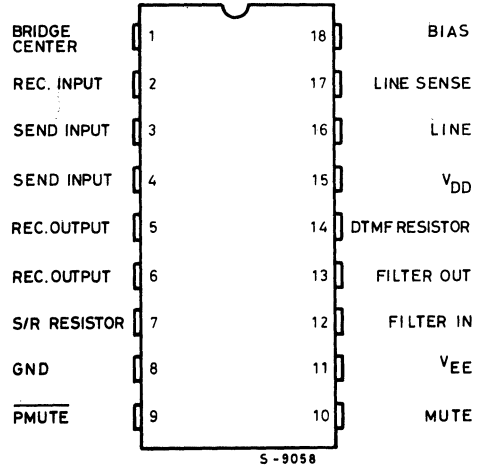
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3ms pulse duration)	20	V
I_L	Line current	150	mA
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	1	W
T_{op}	Operating temperature	-20 to +55	°C
T_{stg}, T_j	Storage and junction temperature	-60 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

FUNCTIONAL PIN DESCRIPTION

Pin Number	Description
1	Reference point of receiver circuit.
2	Receiver input
3 and 4	Send input
5 and 6	Receiver output
7	Send/receive amplifier gain control.
8	Ground
9	Pulse Mute When low, in conjunction with Mute, provide 40dB attenuation of receive signal.
10	Mute, when high, mutes transmitter by 60dB and receiver by 26dB. Also causes power supplies to increase current available.
11	V_{EE} Electret power supply. Voltage source of 2.4V supplying up to 500μA. Used to polarize electret transmitter.
12	DTMF Filter In.
13	DTMF Filter Out.
14	DTMF resistor. Sets DTMF gain
15	V_{DD} Regulated power supply output. Used to power dialing chip.
16	Line input
17	Line sense. A resistor R_{DC} here sets DC resistance and amplifier AGC points.
18	Bias input. Used as bias reference internally.

Fig. 1 - Application and test circuit

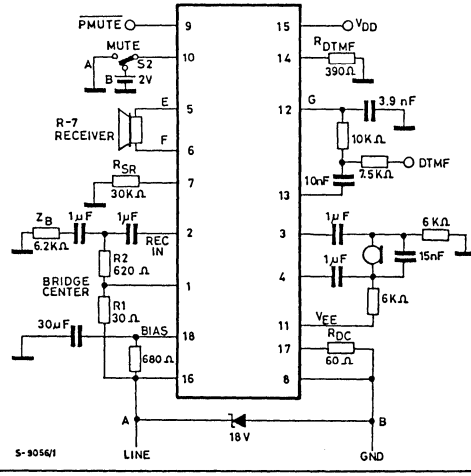


Fig. 2 - Side tone and sending gain

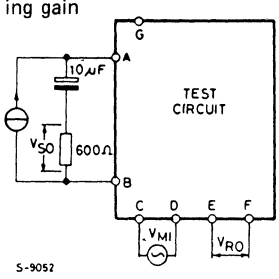


Fig. 3 - Receive gain

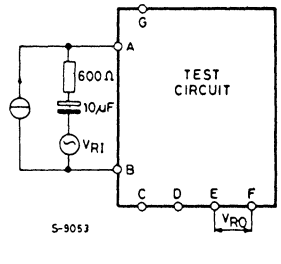
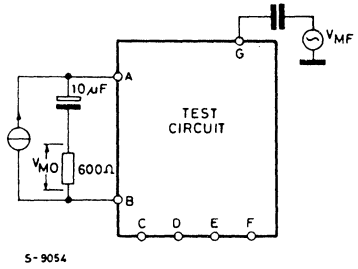


Fig. 4 - DTMF gain



Side tone = $\frac{V_{RO}}{V_{MI}}$ $G_S = \frac{V_{SO}}{V_{MI}}$ $G_R = \frac{V_{MO}}{V_{RI}}$ $G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, f = 200 to 3400Hz, S2 in position (A) on the test circuit, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION FOR I_L = 5mA TO 20mA							
V_L	Line voltage	I_L = 5mA			1.3	V	
V_{so}	Sending dynamic output voltage	I_L = 5mA		100		mV_{rms}	
I_{ro}	Receiving dynamic output current	I_L = 5mA		0.8		mA	
V_{EE}	Electret Bias	I_L = 5mA		0.7		V	
DTMF INTERFACE AND OPERATION: S2 IN POSITION (B)							
V_{DD}	DTMF supply voltage		2.4			V	
I_{DD}	DTMF supply current		2.5			mA	
DTMF	Amplifier gain	f_{MFin} = 1KHz V_{MFin} = 80mV	-3.3		-1.3	dB	4
DTMF	Transient voltage				V_L+5	V	
R_I	Input impedance	V_{MFin} = 80mV	60			KΩ	
DTMF	Tone distortion	I_L > 14mA		2		%	
	Starting delay time				5	ms	
V_{IL}	Mute input LOW				1.0	V	
V_{IH}	Mute input HIGH		2.0			V	
V_{CL}	Conference level gain	V_{RO} / V_{SO}	-24	-27	-30	dB	
	Sending Gain Mute	V_{MI} = 3mV		-60		dB	1
	I_{Leak} V_{DD} leakage	V_{DD} = 2.5V		2		nA	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION FOR I_L = 20mA TO 125mA							
V_L	Line Voltage	I_L = 20mA I_L = 125mA			3 10	V V	
G_S	Sending Gain	f = 1KHz I_L = 42mA V_{MI} = 3mV I_L = 96mA	39 35	40 36	41 37	dB dB	2 2
	Transmitting distortion	f = 1KHz V_{SO} = 700mV I_L = 20mA			2	%	2
	Sending Noise	V_{MI} = 0V		-70		dBmp	2
	Micro input impedance		40			KΩ	
G_R	Receiving gain	V_{RI} = 0.3V f = 1KHz I_L = 42mA I_L = 96mA	 -11 -15	 -10 -14	 -9 -13	 dB dB	 3 3
	Receiving distortion	f = 1KHz V_{RO} = 440mV I_L = 20mA			2	%	3
	Receiving Noise	V_{RI} = 0V		100		μV	3
	Receiving out impedance	V_{RO} = 50mV		30		Ω	
	Sidetone	f = 1KHz		36		dB	2
Z_{ML}	Line matching impedance	V_{RI} = 0.3V f = 1KHz	500	600	700	Ω	3
	Return Loss	V_{RI} = 0.3V f = 1KHz	 -14			 dB	 3
V_{EE}	Electret bias		2.4			V	
I_{EE}	Electret supply current		0.5			mA	
V_{DD}	DTMF supply voltage		2.4			V	
I_{DD}	DTMF stand-by supply current		0.5			mA	
PULSE DIALING OPERATION: S2 IN POSITION (B)							
I_{PL}	Input low current pulse mute				50	μA	
I_{Leak}	Input high current Pulse mute				-10	μA	
	Confidence level gain	Pulse Mute Low		-40		dB	3

L3240

ELECTRONIC TWO-TONE RINGER

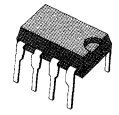
- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS
- BRIDGE OUTPUT CONFIGURATION

L3240 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a trasformer is needed. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across output amplifiers in the transducer; both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect the correct operation of the devices.

The output bridge allows to use a high impedance transducer with acoustical results much better than in a single ended configuration.

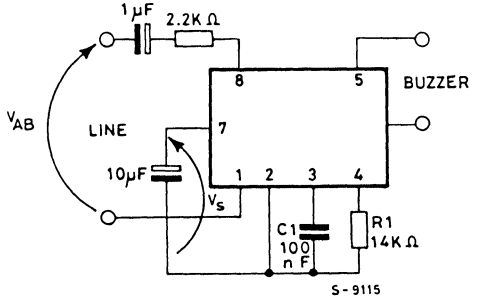
The two outputs can also be connected independently to different converters or actuators (acoustical, opto, logic).



Minidip Plastic

ORDERING NUMBER: L3240

Fig. 1 - Test circuit

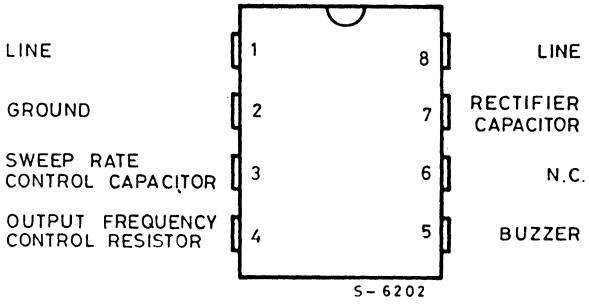


$$f_1 = \frac{3.56 \cdot 10^4}{R1\ (K\Omega)}$$ (see fig. 4) $\qquad f_2 = 0.725\ f_1 \qquad f_{SWEEP} = \frac{750}{C1\ (nF)}$

ABSOLUTE MAXIMUM RATINGS

V_{AB}	Calling voltage (f = 50Hz) continuous	120	V_{rms}
V_{AB}	Calling voltage (f = 50Hz) 5s N/10s OFF	200	V_{rms}
DC	Supply vurrent	30	mA
T_{op}	Operating temperature	-20 to +70	°C
T_{stg}	Storage and junction temperature	-65 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_S	Supply voltage				26	V
I_B	Current consumption without load (Pins 8-1)	V_S = 16.5 to 29.5V		1.5	1.8	mA
V_{ON}	Activation voltage		12		13.5	V
V_{OFF}	Sustaining voltage		7.8		9.3	V
R_D	Differential resistance in OFF condition		6.4			KΩ
V_{OUT}	Output voltage swing			V_S -5		V
I_{OUT}	Short circuit current (Pins 5-6)	V_S = 20V		35		mA
V_S	Voltage drop between Pin 8-1 and Pin 7-2			3		V

AC OPERATION

	Output frequencies fout 1 fout 2	V_S = 26V R_1 = 14KΩ V_S = 0V V_S = 6V	 2 1.4		 2.66 2	KHz
	$\frac{\text{fout 1}}{\text{fout 2}}$		1.33		1.43	Hz
	Programming resistor range		8		56	KΩ
	Sweep frequency	R_1 = 14KΩ C1 = 100nF		10		Hz

Fig. 2 - Typical application with balanced output

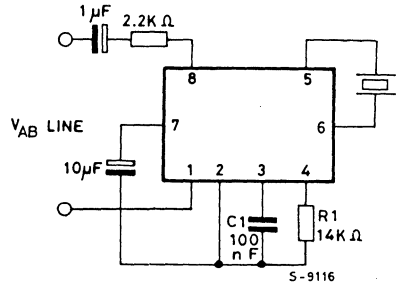


Fig. 3 - Application compatible with LS1240

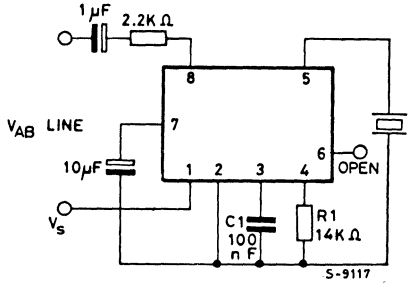
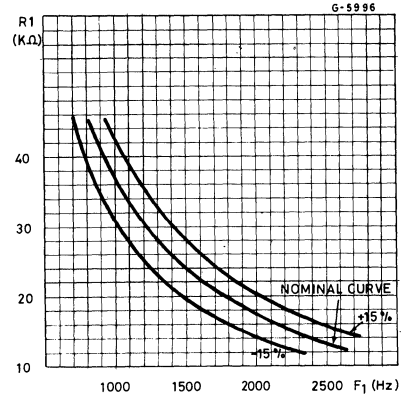


Fig. 4 - F_1 out vs. R_1



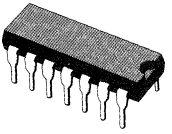
L3280

ADVANCE DATA

LOW VOLTAGE TELEPHONE SPEECH CIRCUIT

- OPERATION DOWN TO 1.3V/5mA
- DTMF & BEEP TONE INPUTS
- EXTERNAL MUTING FOR EARPHONE AND MICROPHONE
- MUTE TURNS ON BEEP TONE & DTMF INPUTS AND TURNS OFF EARPHONE & MICROPHONE
- SUITABLE FOR DYNAMIC OR PIEZO EARPHONES AND PIEZO, DYNAMIC OR ELECTRET MICROPHONES

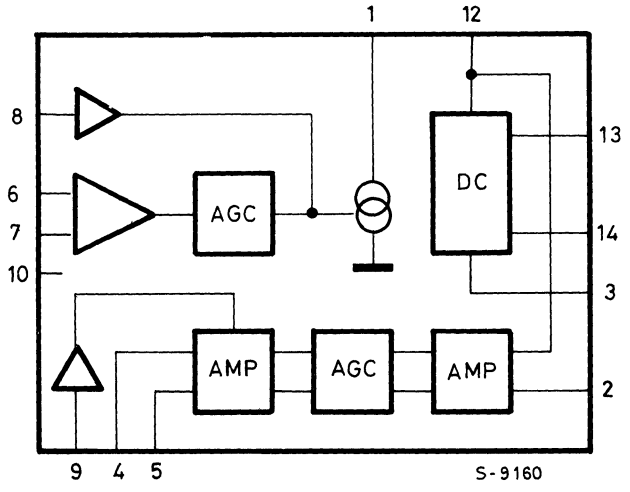
The L3280 is a brand new low voltage speech circuit designed to replace hybrid circuits in telephone sets. It is designed for sets that may be operated in parallel. It feature both DTMF input and Beep tone input; ALC on send and receive and muting input.



DIP-14 Plastic
(0.25)

ORDERING NUMBER: L3280

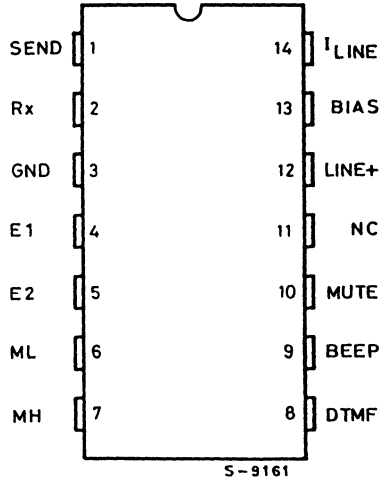
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_L	Line Voltage (3ms pulse)	20	V
I_L	Line Current	150	mA
P_{tot}	Total Power Dissipation, $T_{amb} = 70°C$	1	W
T_{op}	Operating Temperature	-20 to 55	°C
T_j	Junction Temperature	-65 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, f = 200 to 3400Hz)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_L	Line Voltage	I_L = 20mA R_{LINE} = 43Ω I_L = 50mA R_{LINE} = 43Ω I_L = 80mA R_{LINE} = 43Ω			3 6 10	V V V	
G_s	Sending Gain	I_L = 52mA V_{MI} = 2mV	42.5		45.4	dB	3
ΔG_s	Sending Gain Variation $I_{L\ ref}$ = 52mA	V_{MI} = 2mV I_L = 23mA I_L = 80mA	 4 0		 6 -2	 dB dB	3
THD_S	Sending Distortion	f = 1KHz V_{so} = 700mV I_L = 20mA			3	%	3
	Sending Noise	V_{MI} = 0		-70		dBmp	3
	Microphone Input Impedance	V_{MI} = 2mV	40			KΩ	
G_R	Receiving Gain	I_L = 52mA	1.5		4.5	dB	2
ΔG_R	Receiving Gain Variation $I_{L\ ref}$ = 52mA	V_{RI} = 500mV I_L = 23mA I_L = 80mA	 4 0		 6 -2	 dB dB	2
THD_R	Receiving Distortion	f = 1KHz V_{RO} = 630mV I_L = 20mA			3	%	2
	Receiving Noise	V_{RO} = 0		150		μV	2
	Receiving Output Impedance			30		Ω	
Z_{ML}	Line Matching Impedance	V_{RI} = 500mV	500		700	Ω	2
	Return Loss		14			dB	2
	Side Tone			36		dB	3

OPERATION FROM I_L = 5 to 20mA

V_L	Line Voltage	I_L = 5mA			1.3	V	
V_{SO}	Sending Output Voltage	I_L = 5mA		100		mV	
I_{RO}	Receiving Output Current	I_L = 5mA		0.8		mA	
MUTE L	Mute Input Low (Speaking)				1	V	
MUTE H	Mute Input High (Dialing)		2			V	
	DTMF Gain (MUTE H = 2V)	V_d = 3mV	26.5	28	29.5	dB	
	DTMF Input Impedance (MUTE H = 2V)	V_d = 3V		7.5		KΩ	
	DTMF distortion (MUTE H = 2V)	V_d = 25mV			3	%	
	Beeptone Gain (MUTE H = 2V)	V_b = 25mV		9		dB	
	Beeptone Input Impedance (MUTE H = 2V)	V_b = 25mV		14		KΩ	
	Beeptone Distortion (MUTE H = 2V)	V_b = 100mV		3		%	

TEST CIRCUITS

Fig. 1

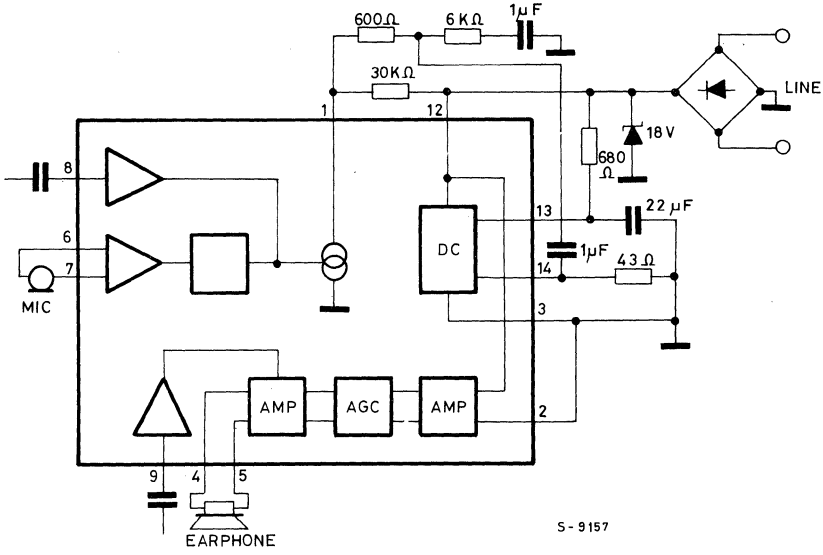
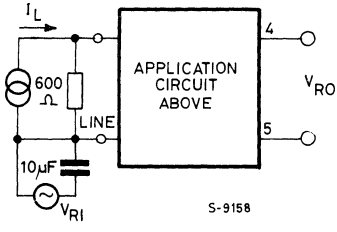


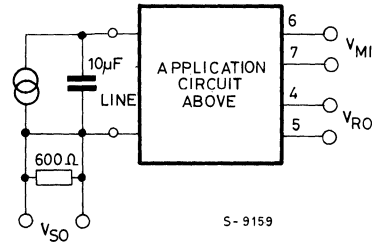
Fig. 2



Receiving gain:

$$G_R = \frac{V_{RO}}{V_{RI}}$$

Fig. 3



Sending gain and sidetone:

$$G_S = \frac{V_{SO}}{V_{MI}} \quad ; \quad ST = \frac{V_{RO}}{V_{MI}}$$

CHARACTERISTIC AT 1KHz

Fig. 4 - Receive characteristic and max output at 2%THD

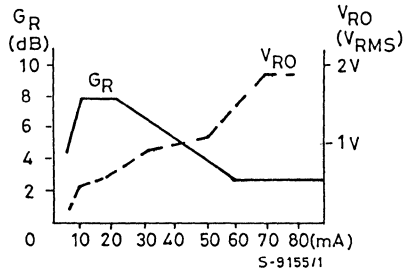


Fig. 5 - Sending ALC characteristic and max output at 2% THD

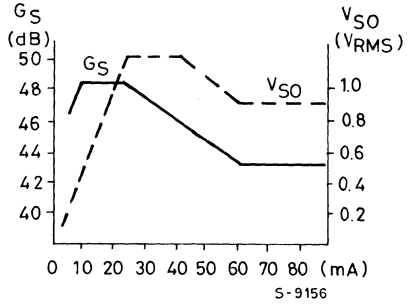
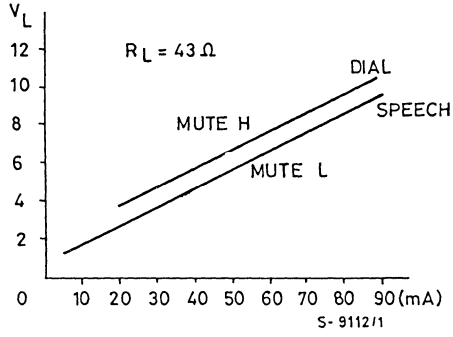


Fig. 6 - DC characteristic measured between line and GND



LOGIC OF MUTE SWITCHING

	DTMF	BEEP	MIC INPUT	RECEIVE INPUT
MUTE H	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	MUTED	MUTED
MUTE L	MUTED	MUTED	ACTIVE	ACTIVE

LB1004

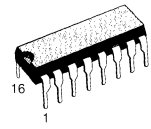
PRELIMINARY DATA

AN AT&T PRODUCT

FULL-FEATURE TELEPHONE TONE RINGER/RINGING DETECTOR

- COMPLETE TELEPHONE BELL REPLACEMENT WITH CAPABILITY OF 32 SWITCH-SELECTABLE ALERTER TONES
- TIGHT OUTPUT FREQUENCY CONTROL (±3%) FOR MAXIMUM ACOUSTIC OUTPUT
- EXTERNAL COMPONENTS: ONLY TWO CAPACITORS AND ONE RESISTOR REQUIRED
- INDEPENDENTLY SELECTABLE AM OR FM MODULATION
- ON-CHIP VOLUME CONTROL RESISTORS PROVIDED
- IMMUNE TO ROTARY DIAL PULSING (BELL TAP)
- MEETS BOTH TYPE A AND B RINGING REQUIREMENTS (40 $V_{RMS} \leq V_{IN} \leq 150V_{RMS}$, $15Hz \leq f_{IN} \leq 68$ HZ) AS SPECIFIED BY EIA RS-470 AND FCC PART 68
- MEETS INPUT IMPEDANCE CRITERIA SPECIFIED BY EIA RS-470 AND AT&T TECH. PUB. 47001
- LOGIC- OR SWITCH-SELECTABLE OUTPUT FREQUENCY AND MODULATION RATE
- INTERNAL POLARITY GUARD PROVIDES 1500V LIGHTNING SURGE PROTECTION WHEN CONNECTED AS IN FIG. 10 AND 11
- RINGER EQUIVALENCY: 1 B WHEN CONFIGURED AS SHOWN IN FIGURES 10 AND 11

The LB1004 is a Full Feature Tone RInger/Ringing Detector integrated circuit which simultaneously provides a ringer-output tone and a "ringing-detected" output signal. The tone ringer portion of the device provides switch-selectable output frequencies of 750, 900, 940, and 1200 Hz at independently selectable modulation rates of 7.5, 10, 15, and 20 Hz. Amplitude or frequency modulation may also be independently selected. These TTL/CMOS logic or switch selectable features, controlling both the type of sound and its duration, provide distinctive ringing capabilities which are useful for a multiphone office environment. The ringer can



DIP-16 B Plastic

ORDERING NUMBER: LB1004AC

be prevented from providing a tone output with a "Ringing Inhibit" function. These functions can be controlled by a microprocessor, allowing various alerting tasks to be performed by appropriate programming. The ringing detector portion of the device provides an output (LED OUT) which can interface with a microprocessor or an opto-isolator (see Applications).

PIN CONFIGURATION

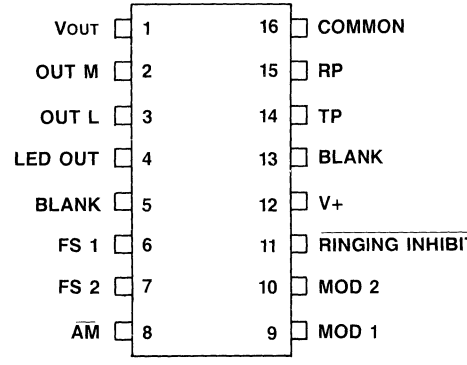
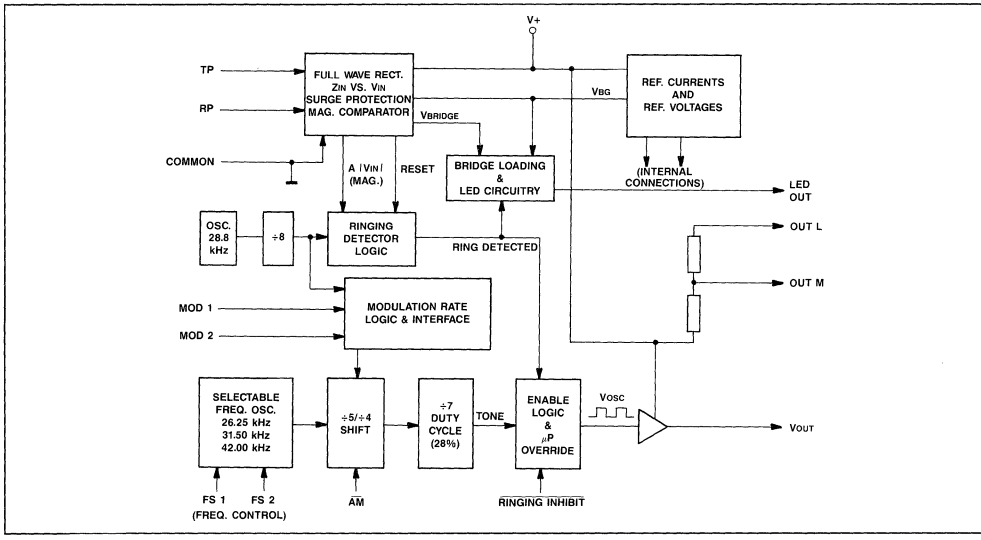


Fig. 1 - Functional Diagram



PIN DESCRIPTION

Pin	Symbol	Name/Function
1	V_{OUT}	Tone ringer output which drives the alerter
2	OUT M	Control option for medium volume output
3	OUT L	Control option for low volume output
4	LED OUT	Sinks current when ringing is detected
5	Blank	This pin may be used as a tie point for external components Voltage applied to this pin should not exceed 30V
6	FS 1	Frequency Select pin (see Table 2)
7	FS 2	Frequency Select pin (see Table 2)
8	$\overline{AM}$	Selects either AM or FM modulation or output ringer tone (see Table 1)
9	MOD 1	Modulation Rate Select pin (see Table 2)
10	MOD 2	Modulation Rate Select pin (see Table 2)
11	$\overline{\text{Ringing Inhibit}}$	The Ringer Inhibit function is a TTL/CMOS-compatible input for logic control of the Tone Ringer output (see Table 1)
12	V+	Internal supply voltage. This voltage is usually derived from the AC signal which is present on the Tip-Ring pair. This pin must have a 10µF capacitor to common for energy storage and "smoothing" purposes. For "stand alone applications", an external voltage may be use to bias this pin.
13	Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 30V
14 15	TP RP	Tip Prime (TP) and Ring Prime (RP) are inputs to this device. AC ringing signals from the telephone line energize the detector circuit
16	Common	Circuit Common (not necessarily physical or system ground)

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Operating Voltage (V+ to Common)	30	V
Operating Voltage (TP-RP)	±30	V
Operating Current (TP-RP)	±100	mA
Output Current (V_{OUT}-Common)	±30	mA
Ambient Operating Temperature Range	−20 to +75	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering, 15 sec)	300	°C
Power Dissipation (Package Limitation)	500	mW

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions		Min	Typ	Max	Unit
Power Supply Current	V+ = 28V	(See Fig. 2)	—	0.76	1.9	mA
Power Supply Current	V+ = 15V	(See Fig. 2)	—	0.73	1.5	
TP Current, No Load(1)	V_{TP-RP} = 8V	(See Fig. 3)	—	0.90	1.2	
RP Current, No Load(1)	V_{TP-RP} = −8V	(See Fig. 3)	—	−0.90	−1.2	
TP Current, No Load(1)	V_{TP-RP} = 20V	(See Fig. 3)	—	0.98	1.55	
RP Current, No Load(1)	V_{TP-RP} = −20V	(See Fig. 3)	—	−1.0	−1.55	
Input Threshold Voltage, TP-RP(2)	V+ = 8V	(See Fig. 4)	6.0	7.0	8.0	V
Input Threshold Voltage, TP-RP(2)	V+ = 25V	(See Fig. 4)	6.0	7.0	8.0	
I_{TP}	V_{TP-RP} = 4V	(See Fig. 5)	—	15	30	μA
I_{RP}	V_{RP-TP} = 4V	(See Fig. 5)	—	15	30	
Clamp Voltage(3)	I_{TP} = 25mA	(See Fig. 6)	22.5	25.7	30	V
Clamp Voltage(3)	I_{TP} = −25mA	(See Fig. 6)	−22.5	−25.7	−30	
Clamp Voltage(3)	I_{TP} = 100mA	(See Fig. 6)	—	3.8	5.5	
Clamp Voltage(3)	I_{TP} = −100mA	(See Fig. 6)	—	−3.8	−5.5	
LED Current Off (Ringing not detected state)		(See Fig. 7)	—	0.43	±10	μA
LED Current On (Ringing detect state)		(See Fig. 8)	310	375	500	
Frequency(4)	V+ = V_{TP} = 15V V_{RP} = 0	(See Fig. 9, Note 1)	1164	1200	1236	Hz
Modulation Rate(4)	V+ = V_{TP} = 15V V_{RP} = 0	(See Fig. 9, Note 2)	16	20	24	
Frequency(5)	I_{TP} = 10mA	(See Fig. 9, Note 1)	1154	1200	1246	
Modulation Rate(5)	I_{TP} = 10mA	(See Fig. 9, Note 2)	16	20	24	

Table 1 - Tone Output Status (see Notes 6 and 7)

Ringing Inhibit	$\overline{AM}$	Tone Output State
Open	Open	Frequency Shift Modulation (at modulation rate)
Low	Don't Care	No output tone
Open	Low	Amplitude Modulation (at modulation rate)

Table 2 - Tone Selection (see Notes 6 and 7)

Frequency Select Pins			Modulation Rate Select Pins		
FS 1	FS 2	Tone Output Frequency	MOD 1	MOD 2	Tone Output Modulation Rate
Open	Open	1200 Hz	Open	Open	20 Hz
Open	Low	940 Hz	Open	Low	15 Hz
Low	Open	900 Hz	Low	Open	10 Hz
Low	Low	750 Hz	Low	Low	7.5 Hz

Notes:

1. The specified current is measured after ringing has been detected (30 to 40 ms).
2. With the proper voltage applied to V+, the threshold voltage is defined as the TP-RP voltage at which the device detects a ringing signal, as seen at the LED OUT pin or the alerter output (V_{OUT}-Common).
3. The potential between TP and RP is measured with the specified current at TP.
4. The output frequency and modulation rate between V_{OUT} and Common are measured with the specified voltages at V+, TP and RP. These measurements are obtained after ringing has been detected (30 to 40 ms).
5. The output frequency and modulation rate are measured with the specified current at TP and after ringing has been detected (30 to 40 ms).
6. Low denotes a connection (switch, wire path, or a transistor) between the appropriate pin and Common (pin 16). Pin 6, 7, 8, 9, 10 are TTL/CMOS-compatible inputs, with internal pull-up provided.
7. Frequency shift modulation generates frequencies f_O and 5/4 f_O. Amplitude modulation generates f_O turned on and off at the modulation rate.

TEST CIRCUITS

Fig. 2

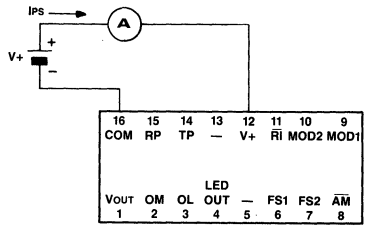
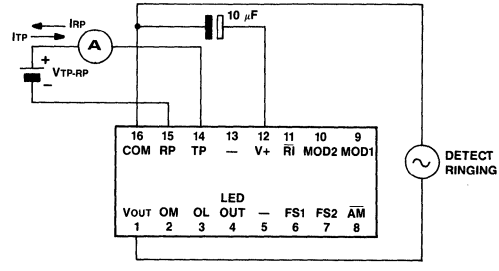


Fig. 3



TEST CIRCUITS (Continued)

Fig. 4

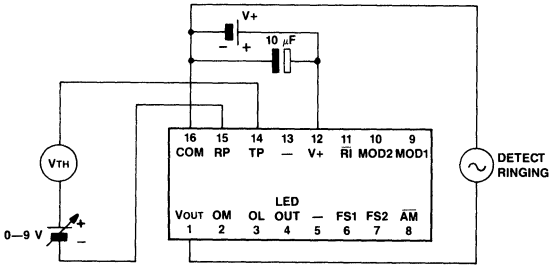


Fig. 5

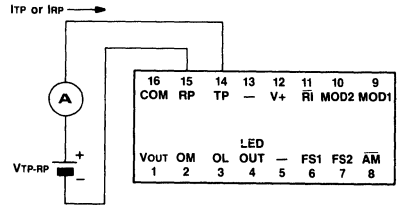


Fig. 6

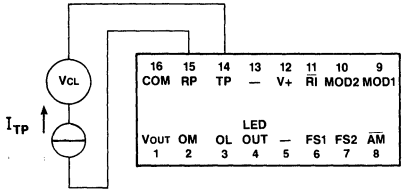


Fig. 7

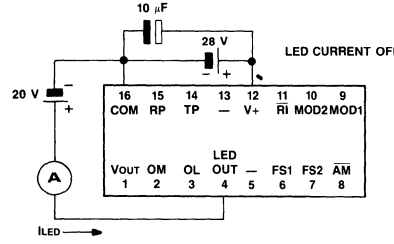


Fig. 8

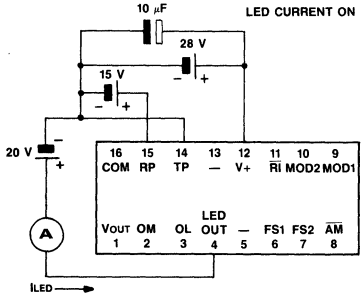
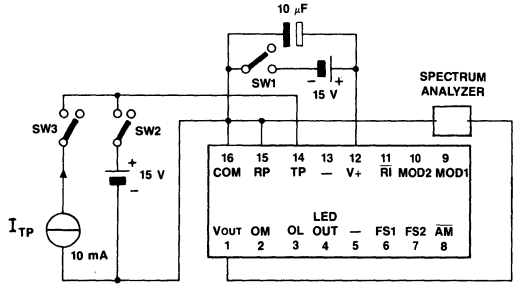


Fig. 9



Note 1: Measure F1 or 1.25 F1 with SW1 and SW2 closed; SW3 open.
Note 2: Measure modulation rate with SW1 and SW2 open; SW3 closed.

APPLICATIONS

The LB1004AC requires only two capacitors, one resistor, and an output transducer to provide tone ringing functions from any standard Tip-Ring telephone pair. These devices operate over varying ringing waveforms (15 to 68 Hz at 40 to 150 V_{RMS}). A tone ringer derives its power by rectifying the AC ringing signals from the Tip-Ring pair of a telephone loop. It uses this power to activate a tone generator and then transfers most of this power to an alerter after ringing is detected. Thus, there is essentially no loading under non-ringing conditions. Selectable on-chip resistors allow the volume of the alerter output to be adjusted (See the application diagram below).

The ringing detector portion of this device has one output (LED OUT). This output will sink current when ringing is detected, and can be connected to either an opto-isolator device or to a logic interface with a microprocessor (see Figures 10 and 11). This device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source V+ will also allow the device to operate in what is described as "stand alone applications".

Fig. 10 - Typical Application For Opto-Isolator Drive

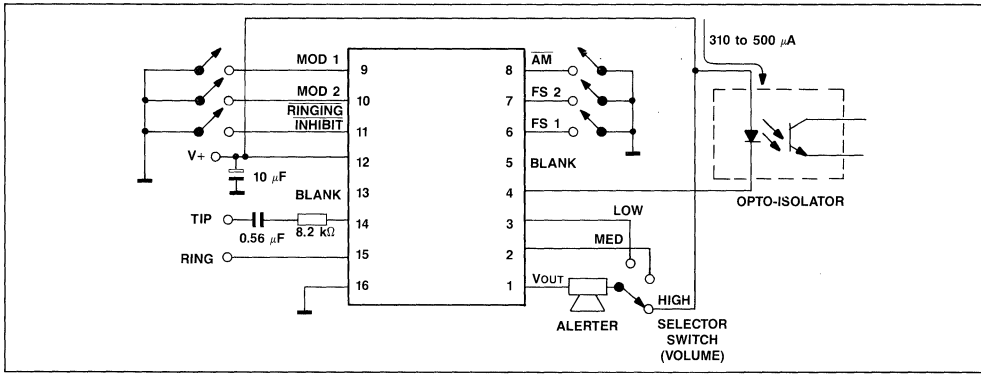
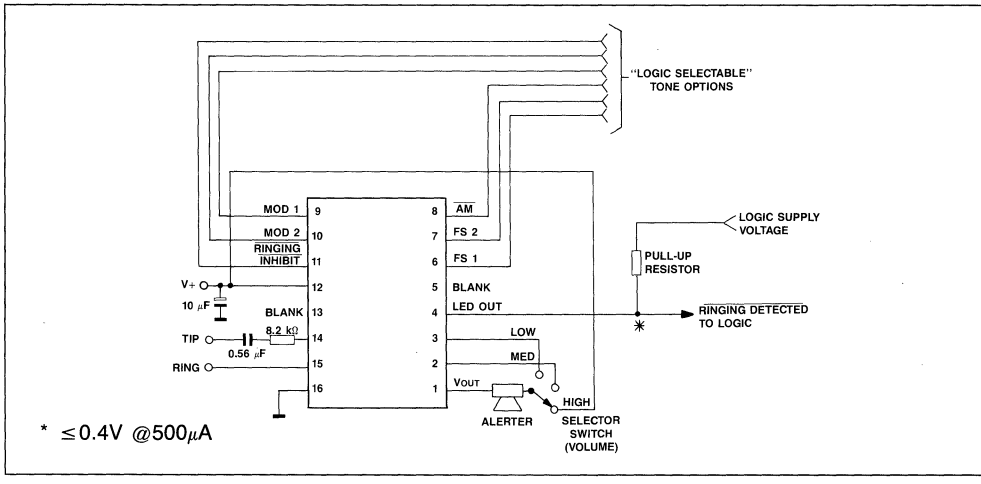


Fig. 11 - Typical Application for Interface Direct to Logic



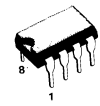
LB1005AB
LB1005BB

PRELIMINARY DATA

AN AT&T PRODUCT

GENERAL-PURPOSE TELEPHONE TONE RINGERS

- TIGHT OUTPUT FREQUENCY CONTROL (±3%) FOR MAXIMUM ACOUSTIC OUTPUT
- EXTERNAL COMPONENTS REQUIRED ARE TWO CAPACITORS AND ONE RESISTOR
- MEETS BOTH TYPE A AND B RINGING REQUIREMENTS (40 V_{RMS} < V_{IN} < 150 V_{RMS}, 15 Hz < f_{IN} < 68 Hz) AS SPECIFIED BY EIA RS-470 ON FCC PART 68
- IMMUNE TO ROTARY DIAL PULSING (BELL TAP)
- MEETS INPUT IMPEDANCE CRITERIA SPECIFIED BY EIA RS-470 AND AT&T TECHNICAL PUBBLICATION 47001
- POLARITY GUARD PROVIDES 2000V LIGHTNING SURGE PROTECTION WHEN CONNECTED AS IN FIG. 8
- ON CHIP VOLUME CONTROL RESISTORS PROVIDED
- PROVIDES ESSENTIALLY NO LOADING UNDER NON-RINGING CONDITIONS
- RINGER EQUIVALENCY: 0.8 B WHEN CONFIGURED AS IN FIG. 8.

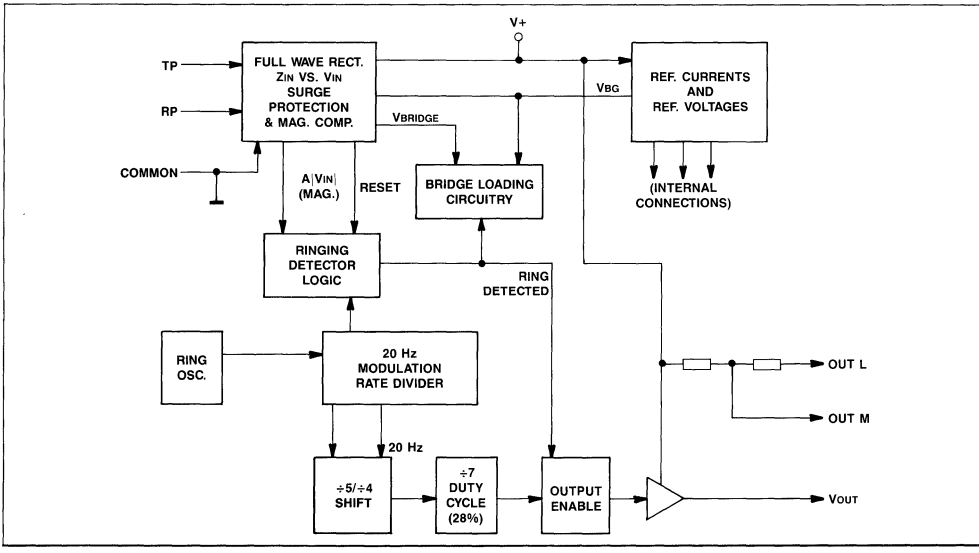


Minidip Plastic

ORDERING NUMBER: LB1005AB (MINIDIP-A)
LB1005BB (MINIDIP-B)

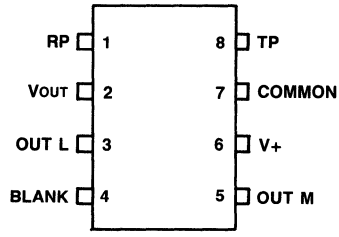
These devices provide a telephone alerter function with an output tone warbling between the base frequency and 1.25 times that of the base frequency, at a 20Hz modulation rate. Both devices meet all known standard criteria for telephone alerters, and also drive piezoelectric transducers directly. The LB1005AB is a tone ringer having an 1800Hz base frequency, and is particularly suited for applications where space for the alerter is at a premium. The LB1005BB is a tone ringer having a 1200Hz base frequency. This device produces a more pleasing tone where required space is available for the alerter.

Fig. 1 - Functional Diagram



LB1005AB
LB1005BB

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Description
1 8	TP RP	Tip Prime (TP) and Ring Prime (RP) are the inputs to the device. AC ringing signals from the telephone line energize the detector circuit.
2	V_{OUT}	Tone ringer output which drives the alerter.
3	OUTL	Control option for lower volume output.
4	Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 30 volts.
5	OUTM	Control option for medium volume output.
6	V+	Internal supply voltage. This voltage is usually derived from the AC signal which is present on the Tip-Ring pair. This pin must have a 10 μF capacitor to common for energy storage and «smoothing» purposes. For «stand alone applications», an external voltage may be used to bias this pin.
7	Common	Circuit Common (not necessarily physical or system ground).

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Operating Voltage (V+ − RP)	30	V
Operating Voltage (V_{OUT} − RP)	30	V
Operating Current (TP or RP)	±100	mA
Output Current (V_{OUT})	±30	mA
Non-Recurrent Peak Surge Current, TP or RP ($t \leq 1ms$)	±500	mA
Ambient Operating Temperature Range	−20 to +75	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering 15 sec)	300	°C
Power Dissipation (Package Limitations)	600	mW

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions		Min	Typ	Max	Unit
Power Supply Current	V+ = 28V	(See Fig. 2)	200	455	900	μA
Power Supply Current	V+ = 15V	(See Fig. 2)	200	450	800	
TP Current, No Load	V_{TP-RP} = 20V[1]	(See Fig. 3)	250	585	850	
RP Current, No Load	V_{TP-RP} = −20V[1]	(See Fig. 3)	−250	−585	−850	
Input Threshold Voltage, TP or RP	V+ = 10V[2]	(See Fig. 4)	6.0	7.4	8.0	V
I_{TP}	V_{TP-RP} = 4.5V	(See Fig. 5)	—	32	65	μA
	V_{TP-RP} = −4.5V	(See Fig. 5)	—	−32	−65	
Clamp Voltage	I_{TP} = 20mA[3]	(See Fig. 6)	22.5	25.8	33	V
Clamp Voltage	I_{TP} = −20mA[3]	(See Fig. 6)	−22.5	−25.8	−33	
Clamp Voltage	I_{TP} = 100mA[3]	(See Fig. 6)	—	3.6	5.5	
Clamp Voltage	I_{TP} = −100mA[3]	(See Fig. 6)	—	−3.6	−5.5	
Frequency	V+ = 15V[4] (See Fig. 7, Note 6)	LB1005AB	1746	1800	1854	Hz
	V_{TP} = 15V V_{RP} = 0	LB1005BB	1164	1200	1236	
Modulation Rate	I_{TP} = 10mA[5]	(See Fig. 7, Note 7)	16	20	24	

NOTES:

1. The specified current is measured after ringing has been detected (30 to 40 ms).
2. With the proper voltage applied to V+, the threshold voltage is defined as the TP-RP voltage at which the device detects a ringing signal, as seen at the LED OUT pin or the alerter output (V_{OUT}-Common).
3. The potential between TP and RP is measured with the specified current at TP.
4. The output frequency and modulation rate between V_{OUT} and Common are measured with the specified voltage at V+, TP and RP. These measurements are obtained after ringing has been detected (30 to 40 ms).
5. The output frequency and modulation rate are measured with the specified current at TP and after ringing has been detected (30 to 40 ms).

TEST CIRCUITS

Fig. 2

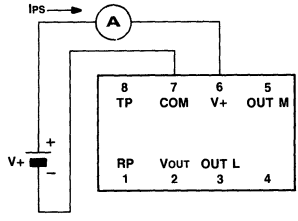
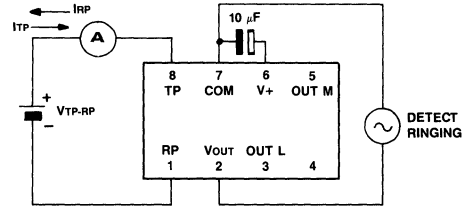


Fig. 3



TEST CIRCUITS (Continued)

Fig. 4

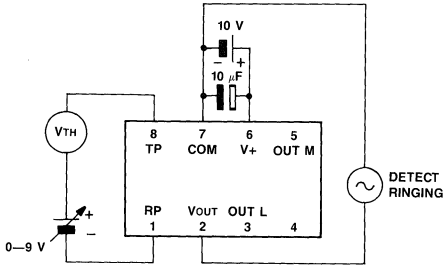


Fig. 5

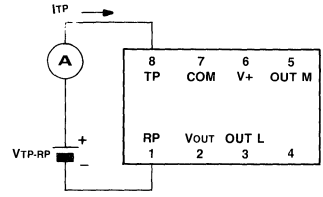


Fig. 6

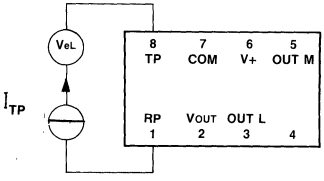
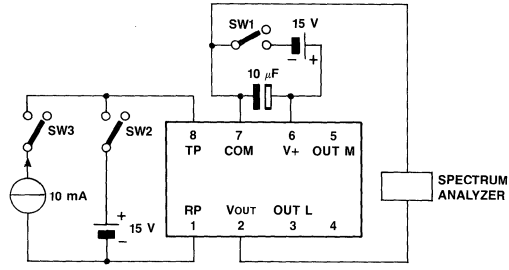


Fig. 7



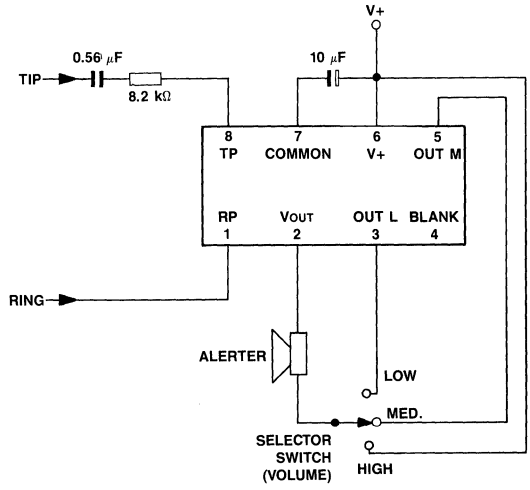
Notes: 6: Measure Frequency with SW1 and SW2 closed; SW3 open.
7: Measure Modulation Rate with SW1 and SW2 open; SW3 closed.

APPLICATION

The LB1005AB or the LB1005BB requires only two capacitors, one resistor, and an alerter to provide tone ringing functions from any standard Tip-Ring telephone pair. These devices operate over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 V_{RMS}). A tone ringer derives its power by rectifying the AC ringing signal from the Tip-Ring pair of a telephone loop. It uses this power to activate a tone generator, and then transfers most of this power to an alerter after the ringing has been detected. There is essentially no loading under non-ringing conditions. Selectable on-chip resistors allow the volume of the alerter output to be adjusted (see application circuit in Fig. 8). This device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the device to operate in what is described as «stand alone applications». The tone generator circuitry includes an oscillator and frequency divider which produce specified tones and the tone modulation rate. The LB1005BB has an output warble frequency range of 1200 to 1500 Hz at a 20 Hz modulation rate. The LB1005AB has an output warble frequency range of 1800 to 2250 Hz at a 20 Hz modulation rate.

APPLICATION (Continued)

Figure 8 - Typical Application



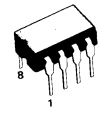
LB1006

PRELIMINARY DATA

AN AT&T PRODUCT

TELEPHONE RINGING DETECTOR

- MEETS BOTH TYPE A AND B RINGING REQUIREMENTS ($40V_{RMS} \leq V_{IN} \leq 150V_{RMS}$, $15Hz \leq F_{IN} \leq 68Hz$
- OPERATES ON LESS THAN 1mA FROM THE TELEPHONE LOOP
- INTERNAL POLARITY GUARD PROVIDES 1500V LIGHTNING SURGE PROTECTION WHEN CONNECTED AS IN FIG. 11 AND 12
- IMMUNE TO ROTARY DIAL PULSING (BELL TAP)

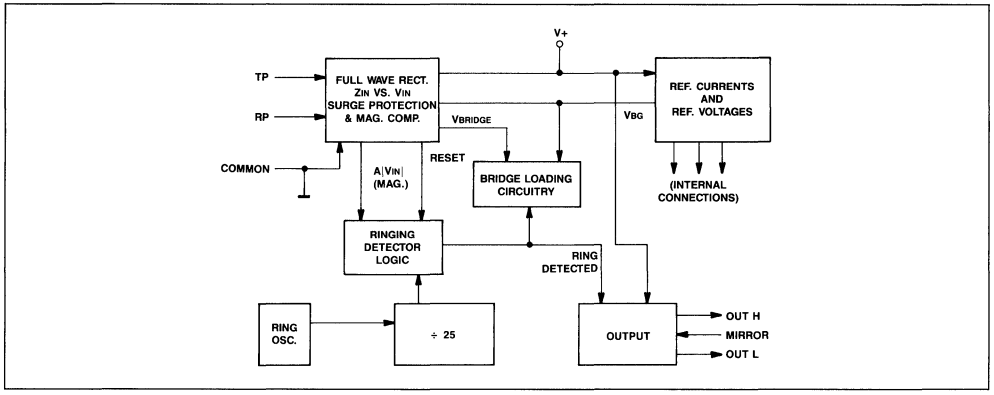


Minidip A Plastic

ORDERING NUMBER: LB1006AB

The LB1006 provides ringing detection functions from the Tip-Ring pair of a telephone loop. This device provides approximately 1mA output current for two types of output drivers. The output can be connected to either an opto-isolator device or to a logic interface with a microprocessor.

Fig. 1 - Functional Diagram

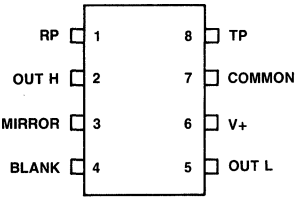


PIN DESCRIPTION

Pin	Symbol	Description
8	TIP	AC input signal from telephone line
1	RING	AC input signal from telephone line
2	OUTH	Sources current when ringing is detected
3	MIRROR	Mirror current from OUTH to activate pin OUTL
5	OUTL	Sinks current when ringin is detected
6	V+	Internal supply voltage. This voltage is usually derived from the AC signal which is present on the Tip-Ring pair. This pin must have a 10 μF capacitor to common for energy storage and «smoothing» purposes. For «stand alone applications», an external voltage may be used to bias this pin.
7	GND	Ground
4	NC	No connection

LB1006

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V+	Supply Voltage (ref to GND)	30	V
OUTH	Supply Voltage (ref to GND)	30	V
OUTL	Supply Voltage (ref to GND)	30	V
TIP	Voltage (Tip-Ring)	±30	V
I_O	Operating Current (Tip-Ring)	±100	mA
I_{MIR}	Mirror Current	2.0	mA
T_A	Ambient Operating Temperature Range	−20 to +75	°C
T_{stg}	Storage Temperature Range	−40 to +125	°C
—	Pin Temperature (Soldering, 15 sec)	300	°C
P_D	Power Dissipation (Package Limitation)	600	mW

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions		Min	Typ	Max	Unit
Power Supply Current	V+ = 28V	(See Fig. 2)	200	365	900	μA
Power Supply Current	V+ = 15V	(See Fig. 2)	200	360	800	
Tip-Ring Current	$V_{TIP-RING}$ = 4.5V	(See Fig. 3)	—	30.4	65	
OUTH Current	V_{TIP} = V+ = 15V	(See Fig. 5)	540	900	1040	
OUTL Current	V_{TIP} = V+ = 15V	(See Fig. 4)	750	—	1400	
Mirror Current	I_{MIRROR} = 1.0mA, V_{OUTL} = 5.0V	(See Fig. 8)	750	1245	1400	
Tip Current, No Load	$V_{TIP-RING}$ = 20V	(See Fig. 7)	0.25	1.410	1.8	mA
Ring Current, No Load	$V_{TIP-RING}$ = −20V	(See Fig. 7)	−0.25	−1.41	−1.8	
Input Threshold Voltage, Tip-Ring	V+ = 10V	(See Fig. 6)	6.0	7.2	8.0	V
Clamp Voltage	I_{TP} = 20mA	(See Fig. 9)	22.5	25.5	30	
	I_{TP} = −20mA	(See Fig. 9)	−22.5	−25.5	−30	
	I_{TP} = 100mA	(See Fig. 9)	—	3.6	5.5	
	I_{TP} = −100mA	(See Fig. 9)	—	−3.6	−5.5	

TEST CIRCUITS

Fig. 2

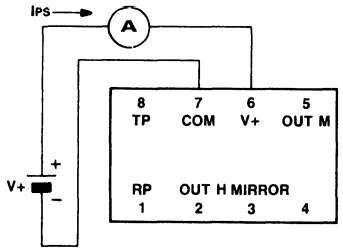


Fig. 3

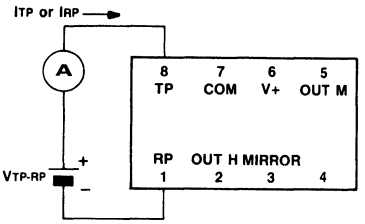


Fig. 4

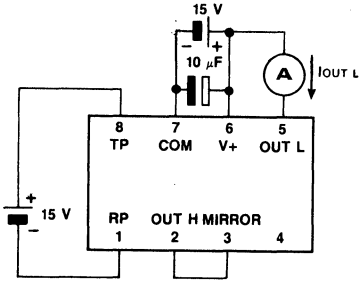


Fig. 5

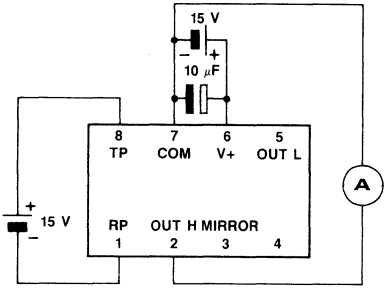


Fig. 6

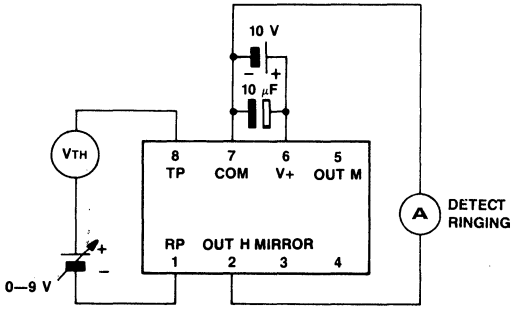
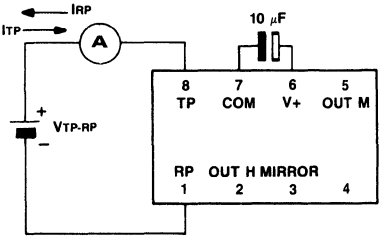


Fig. 7



TEST CIRCUITS (Continued)

Fig. 8

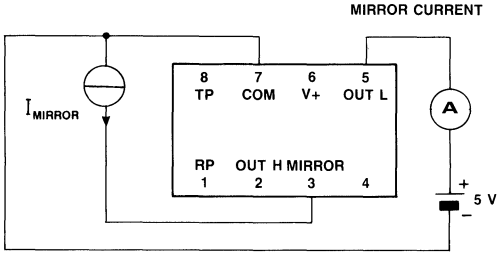
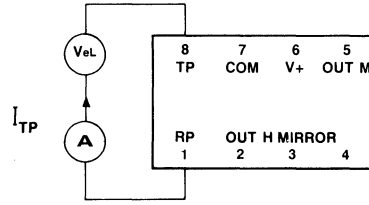


Fig. 9



APPLICATION

The LB1006 detector derives its power by rectifying the AC ringing signal from the Tip-Ring pair of a telephone loop. It operates over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 V_{RMS}). It uses this derived power to activate ringing detector logic, and then transfers most of this power to an output current driver. There is essentially no loading under non-ringing conditions. This device has two outputs, OUTH and OUTL. The OUTH output is used to source output current when ringing is detected. The OUTL output will sink output current when the OUTH output is connected to the mirror input and when ringing is detected (see Application Diagram Figure 11 and 12). The device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V + will also allow the device to operate in what is described as "Stand Alone Applications".

Fig. 10 - Simplified Output Diagram

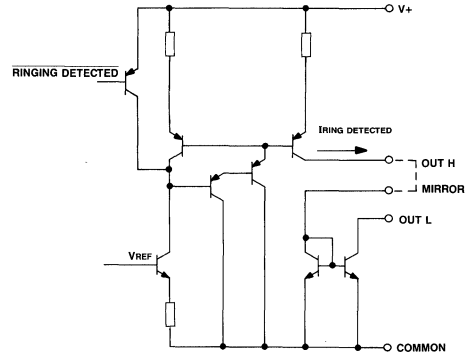
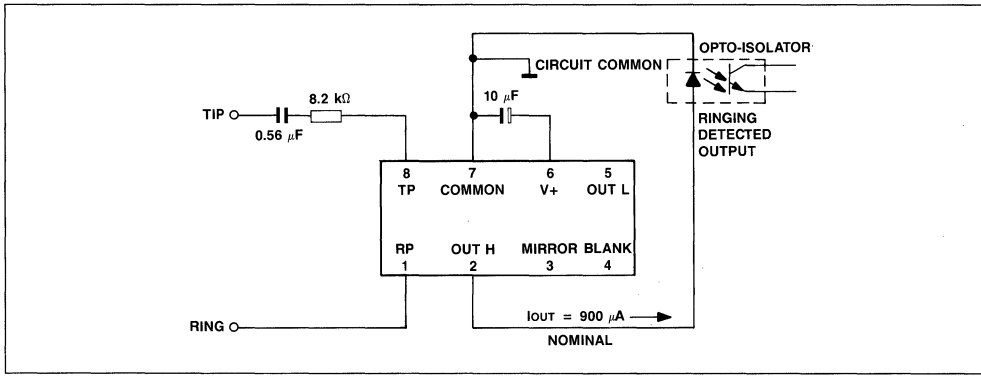
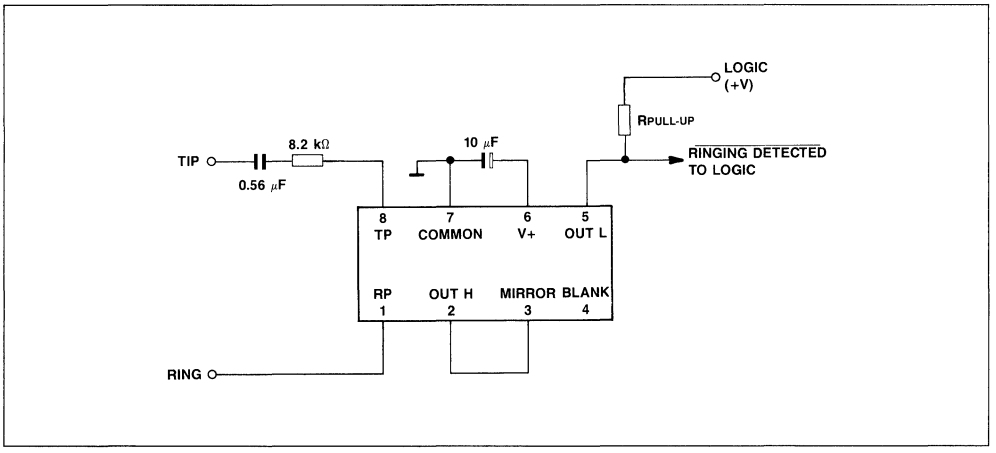


Fig. 11 - Typical Application for Opto-Isolator Drive



APPLICATION (Continued)

Fig. 12 - Typical Application for Interface Direct to Logic

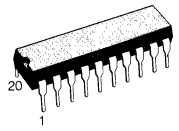


LB1007

ADVANCED DATA
AN AT&T PRODUCT

KEYBOARD CONTROLLED, TOUCH TONE, BASIC SINGLE-CHIP TELEPHONE INTEGRATED CIRCUIT

- BUILT-IN SCHOTTKY POLARITY GUARD
- 1800 Hz/2250 Hz ALERTING SIGNAL
- CAPABLE OF SPEECH TRANSMISSION DOWN TO 3 mA LOOP CURRENT
- DRIVES PIEZOELECTRIC TRANSDUCER FOR ALERTING
- TYPE B RINGER EQUIVALENCY
- SIGNAL GROUND PIN ELIMINATES AN EXTERNAL CAPACITOR FOR DIAL-IN-HANDSET DESIGNS
- REQUIRES 3 CONTACT SWITCH HOOK
- OPERATES FROM POWER SUPPLIED BY THE CENTRAL OFFICE
- USES ELECTRET MICROPHONE WITH PREAMPLIFIER

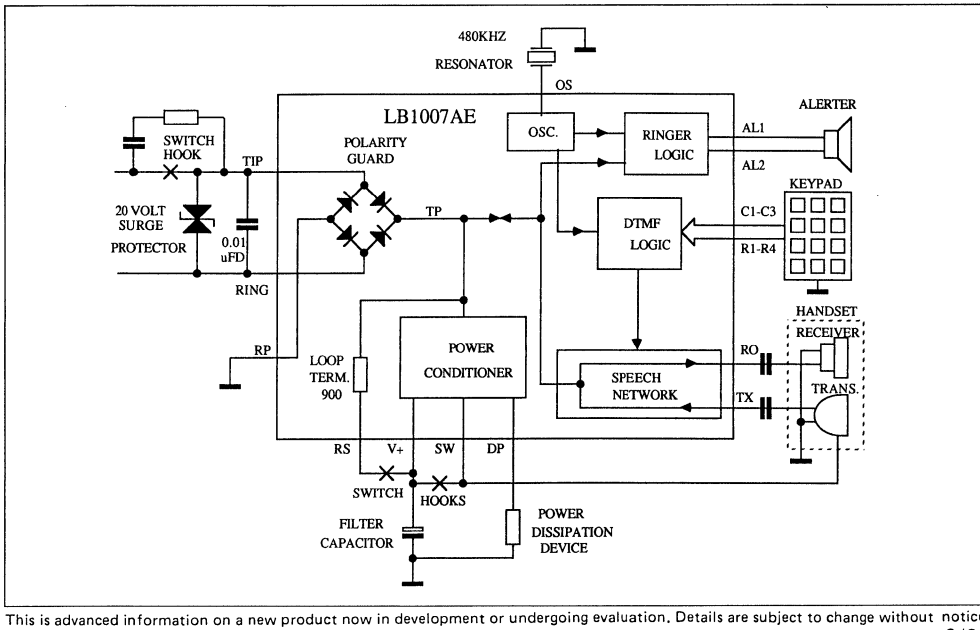


DIP-20 B Plastic

ORDERING NUMBER: LB1007AE

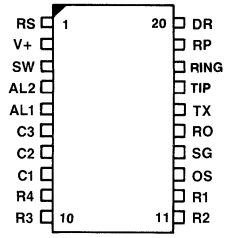
The LB1007 integrated circuit requires only four capacitors, two resistors, a ceramic resonator, and surge protection diode to provide all of the electronic functions. It provides four basic telephone functions as follows: furnishes AC and DC loop termination during the on-hook state; transmits and receives voice signals; provides dual-tone multi-frequency (DTMF) signals to the central office; properly distinguishes between spurious noise and genuine ringing signals providing a distinctive audible alerter output.

Fig. 1 - Functional Diagram



LB1007

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	RS	Provide proper off hook termination impedance when connected through switch hook contact to V+.
2	V+	The most positive DC voltage on the device (must be filtered externally). This voltage is derived from the Tip-Ring inputs and is used to supply internal circuits. No current can be taken from V+ without changing the characteristics as shown in Figure 2.
3	SW	Turns on transmit/receive circuitry when connected through switch hook contact to V+.
4 5	AL2 AL1	Output terminals for driving an alerter. The ringer logic distinguishes between genuine ringing and other noise signals present on the telephone loop, and provides a distinctive audible output. The alerter can be driven differentially or single ended. If the alerter is driven single ended to RP, the second output can be used to drive a visible indicator to RP. Volume can be adjusted by placing a resistor in series with terminals AL1 or AL2.
6 7 8	C3 C2 C1	Keypad inputs for columns 1 through 3. High-frequency touchtone signals are controlled by these inputs. These inputs are disabled when the telephone goes on hook. Single tones are generated when two rows or two columns are activated. Diagonal selections result in no tones. A high frequency and a low frequency tone can be generated by connecting the appropriate column to the desired row pin via the keypad crosspoint switch. An alternative method for generating a single high frequency is to connect the appropriate column to V+ through a 50k resistor.
9 10 11 12	R4 R3 R2 R1	Keypad inputs for rows 1 through 4. Low-frequency touch-tone signals are controlled by these inputs. These inputs are disabled when the telephone goes on hook. Single tones are generated when two rows or two columns are activated. Diagonal selections result in no tones. See note for pins 6,7,8. An alternative method for generating a single low frequency is to connect the appropriate row pin to RP through a 50k resistor.
13	OS	Resonator connection. A 480 kHz ceramic resonator is placed between this pin and RP. This resonator is used to provide the precise frequency required to generate the DTMF tones.
14	SG	Signal ground for use with the receiver output drive. The receive can be placed between this pin and RO without a decoupling capacitor.
15	RO	Receiver output. Optimum receiver impedance is 600 ohms, the circuit will provide 2 dB less power to a 150 ohm receiver. A receiver can be placed between RO and RP or between RO and SG. If the receiver is connected between RO and RP, a decoupling capacitor must be used.
16	TX	Input from transmitter which must be capacitively coupled. This input has a 40k input impedance.
17	TIP	Tip signal input to polarity guard. This signal is supplied by the central office.
18	RING	Ring signal input to polarity guard. This signal is supplied by the central office.
19	RP	The Ring Prime terminal is the logic common or DC ground point.
20	DR	The driver terminal is used to dump extra line current to an external load resistor. This reduces the power consumption in the telephone chip on short loops. The terminal can be used to power an LED if desired.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{TIP}	Circuit Voltage	20	V
I_{TIP}	Circuit Current	120	mA
P_{tot}	Total Power Dissipation	0.5	W
T_{op}	Operating Temperature	0 to 60	°C
T_{stg}, T_j	Storage and Junction Temps.	−45 to 125	°C

THERMAL DATA

R_{TH}	Thermal impedance, junction to ambient	61	°C/W

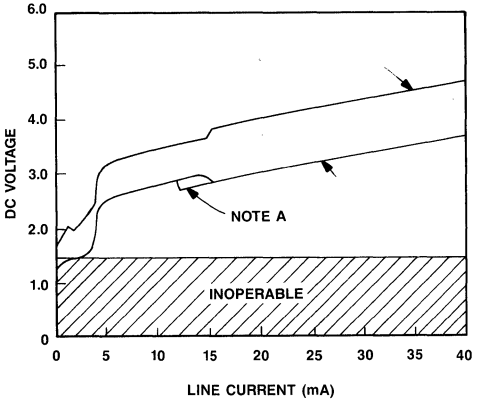
ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
OFF-HOOK DC TESTS					
V_{TIP}	I_{TIP} = 8mA, speech	4.00	—	4.95	V
	I_{TIP} = 20mA, speech	4.80	—	5.90	
	I_{TIP} = 90mA, speech	6.35	—	8.35	
	I_{TIP} = 20mA, dialing	5.10	—	6.16	
V_{V+}	I_{TIP} = 8mA, speech	2.66	—	2.78	
	I_{TIP} = 20mA, speech	2.75	—	3.20	
	I_{TIP} = 90mA, speech	4.50	—	5.60	
$V_{TIP} - V_{V+}$	I_{TIP} = 20mA, dialing	2.00	—	3.15	
I_{DR}	I_{TIP} = 20mA, speech	9.0	—	11.0	mA
	I_{TIP} = 90mA, speech	70.5	—	73.5	
	I_{TIP} = 20mA, dialing	7.5	—	9.7	
	I_{TIP} = 90mA, dialing	69.0	—	72.0	
$I_{TIP,u,s}$	Upper Switch Point, speech	15.5	—	19.5	
$I_{TIP,l,s}$	Lower Switch Point, speech	11.5	—	15.0	
$I_{hys,s}$	$I_{TIP,u,s} - I_{TIP,l,s}$	4.5	—	—	
$I_{TIP,l,d}$	Lower Switch Point, dialing	12.0	—	16.0	
$I_{hys,d}$	$I_{TIP,u,s} - I_{TIP,l,d}$	3.5	—	—	
$V_{RO} - V_{SG}$	I_{TIP} = 20mA, speech	−0.1	—	0.1	V
	I_{TIP} = 20mA, dialing	−0.1	—	0.1	
OFF-HOOK AC TESTS					
$G_{XMIT} = v_{TIP}/v_{TX}$	I_{TIP} = 8mA	2.0	—	4.0	
	I_{TIP} = 20mA, V_{TX} = 0.1Vrms	2.0	—	4.0	
	I_{TIP} = 90mA	2.0	—	4.0	—
$G_{RCV} = V_{RCV}/v_{CO}$	I_{TIP} = 20mA, v_{CO} = 0.5Vrms	0.25	—	0.45	—
	I_{TIP} = 90mA	0.25	0.45		
$R_{TX} = v_{TX}/i_{TX}$	I_{TIP} = 20mA, v_{TX} = 0.1Vrms	—	40K	—	Ω

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
OFF-HOOK AC TESTS (Continued)					
$R_{RO} = v_{RO}/i_{RO}$	I_{TIP} = 20mA v_{RO} = 0.1Vrms	—	600	—	Ω
$R_{TIP} = v_{TIP}/i_{TIP}$	I_{TIP} = 20mA V_{CO} = 0.5Vrms I_{TIP} = 90mA	650 650	— —	950 850	Ω
$G_{SDT} = V_{RCV}/v_{TX}$	I_{TIP} = 8mA I_{TIP} = 20mA v_{TX} = 1Vrms I_{TIP} = 90mA	.4 .4 .4	— — —	.9 .9 .9	—
$V_{TIP,l}$, low group out	I_{TIP} = 20mA	.291	—	—	Vrms
$v_{TIP,h}$, high group out	I_{TIP} = 20mA	.367	—	—	Vrms
$v_{TIP,e}$ Extraneous voice-band signals	I_{TIP} = 20mA, dialing	—	—	.045	Vrms
$v_{TIP,l,h}$ total DTMF, both groups	I_{TIP} = 90mA, dialing	—	—	.869	Vrms
$G_{XMIT} = v_{TIP}/v_{TX}$	I_{TIP} = 20mA, v_{TX} = 0.1Vrms, dialing	—	—	.03	—
ON-HOOK DC TESTS					
I_{TIP}	V_{TIP} = 3V	—	—	35	μA
$V_{TIP,th}$, Thereshold of detection	Ringing detected	5.9	—	6.7	V
I_{TIP}	V_{TIP} = 10V V_{TIP} = 20V	1.5 1.5	— —	2.0 2.5	mA
ON-HOOK AC TESTS					
$v_{AL} = v_{AL2} - v_{AL1}$	V_{TIP} = 10V V_{TIP} = 20V	5.0 15.0	— —	7.0 17.0	V_{p-p}

Fig. 2 - Typical DC V-I Characteristics



Note A: Shown is the hysteresis that occurs in going from the full-feature mode (where dialing can occur in the speech-mode) to the mode where only speeck circuits are active.

APPLICATION

Dual Tone Multi Frequency generation (DTMF)
This circuit is intended to operate with a 3-column, 4-row external keypad. The keypad should be of the type which interconnects the appropriate row and column leads when a key is depressed. The interconnection resistance should be less than 1 kΩ. If two row keys with the same column are depressed, a single frequency corresponding to that column will be generated. In a similar manner, two column keys with the same row will generate that row's fequency. If two keys are depressed which do not have a common row or column, no tones will be generated. The DTMF can also be controlled with a microprocessor by driving the inputs through 50kΩ resistors. A logic "high" on a column input will generate the appropriate column frequency. A logic "low" on a row input will generate the appropriate row frequency. A row and column must be selected to generate a dual frequency tone. The frequencies associated with each row and column pin are shown in Table 1.

Ringing Alerter
The ringing detector determines the presence of a true incoming ringing signal by incrementing an up/down counter depending upon the instantaneous magnitude of the incoming signal. The external series RC network has been selected to optimize discrimination between valid ringing signals and extraneous noise signals. It also provides an on hook type B ringer equivalency. Alerter outputs AL1 and AL2 can be used to drive an external piezoelectric transducer. The load can be applied from AL1 to RP for single ended drive or between AL1 and AL2 for differential push-pull drive (larger amplitude). The volume can be reduced by placing resistors in series with the load. The alerting signal is a square wave alternating between 1800 Hz and 2250 Hz at a 20 Hz repetition rate.

Polarity Guard:
A Schottky diode bridge (on chip) ensures proper voltage polarity on the device, with a 1.2 V drop (at approx. 20 mA) across the bridge rectifier.

Oscillator:
An external 480 kHz ceramic resonator, in conjunction with an internal oscillator control circuit, is used to provide timing functions for the logic circuits, (see Figure 3. Note 4).

Power Conditioner:
This set of circuits provides accurate temperature compensated current and voltage references for the other circuit blocks. It also sets the loop loading and digital reset states for the various types of operation, i.e., on-hook, off-hook, and multiple telephone sets.

Speech Network:
This analog circuit block provides proper transmission levels in both directions. Since the local talker's signal is larger than (on the average) the received signal at the telephone set terminals, an out-of-phase portion of the transmitted signal is also sent to the receiver. This proportion is designed to provide a level in the talker's ear (the "sidetone") between "too hot" and "dead". the DTMF D/A converter is placed in the transmit path during dialing, while the receive-gain path is simultaneously attenuated.

External Components:
As shown in the functional diagram (see Figure 1) the LB1007 IC needs only four capacitors, two resistors, a 480 kHz ceramic alerter, and a surge protection diode to provide basic touch-tone electronic functions. An alerter, a telephone set (containing the transmitter and receiver) and a keypad with a maximum series resistance of 1kΩ are also illustrated.

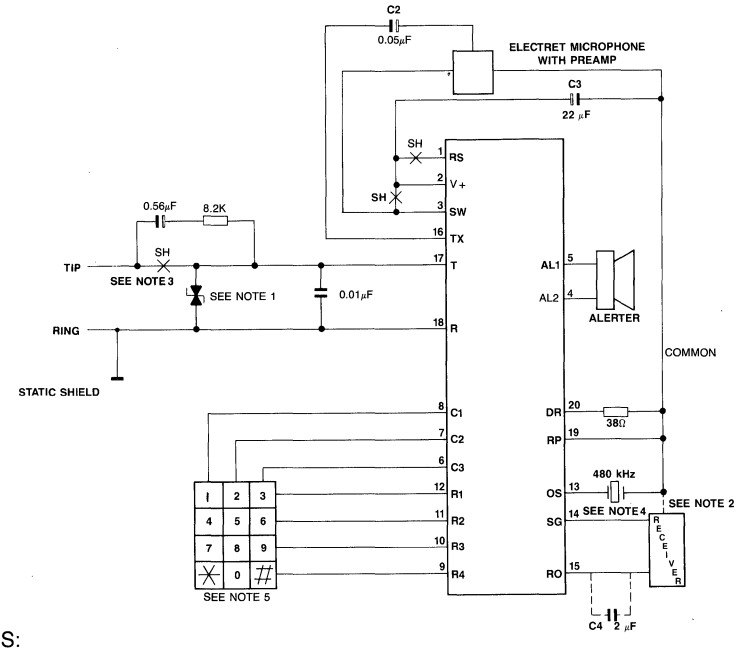
The application diagram (see Figure 3) contains more detailed information. It shows components for connecting to the telephone loop and optional connection components.

APPLICATIONS (Continued)

Table 1

Pin Name	Keypad Input	Tones (Design Value)
R1	Row 1	697 Hz
R2	Row 2	770 Hz
R3	Row 3	852 Hz
R4	Row 4	941 Hz
C1	Column 1	1209 Hz
C2	Column 2	1336 Hz
C3	Column 3	1447 Hz

Fig. 3 - Typical Application Diagram



NOTES:
1. 18V, 150 amp surge protector. (LS5018)
2. For 4-wire interface, pin SG is open and dotted-line options are connected.
3. SH denotes Switch Hook.
4. Ceramic resonator.
5. Keypad inputs can be microprocessor controlled if 50kΩ resistors are placed in series.

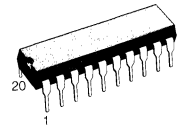
LB1008

ADVANCE DATA

AN AT&T PRODUCT

KEYPAD CONTROLLED, ENHANCED SINGLE-CHIP TELEPHONE INTEGRATED CIRCUIT

- AN ALERTER SELECT OPTION OF 1200 Hz/1500 Hz OR 1800 Hz/2250 Hz
- CAPABLE OF SPEECH TRANSMISSION DOWN TO 3mA LOOP CURRENT
- OPERATES FROM POWER SUPPLIED BY THE CENTRAL OFFICE
- SIGNAL GROUND PIN ELIMINATES AN EXTERNAL CAPACITOR FOR DIAL-IN-HANDSET DESIGNS
- REQUIRES A 2 CONTACT SWITCH HOOK
- COMPATIBLE WITH ELECTRET MICROPHONE
- PROVIDES A POWER PORT FOR DRIVING A LED

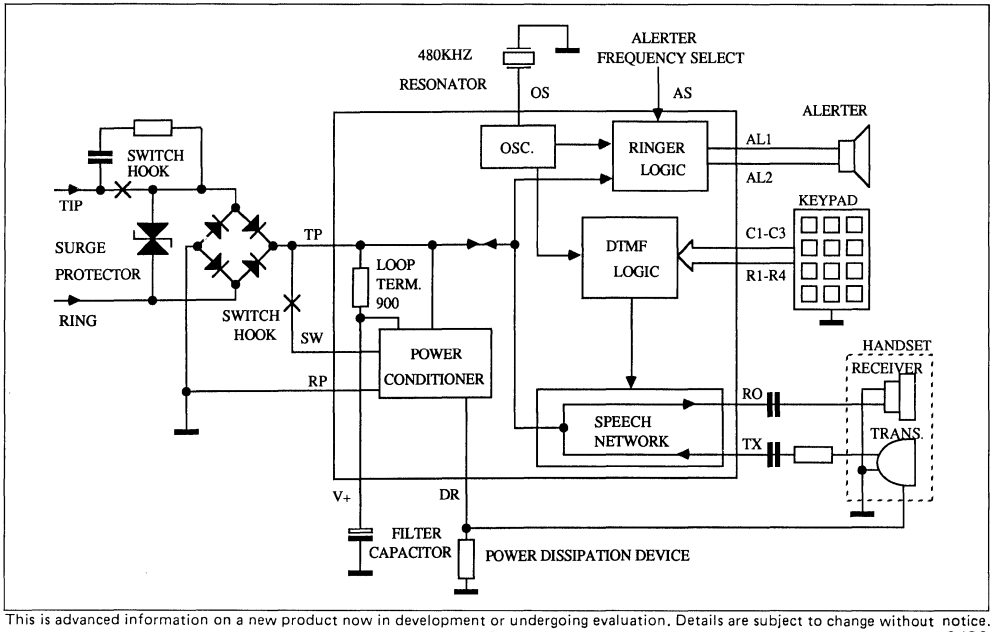


DIP-20 B Plastic

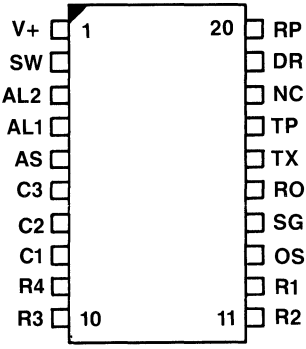
ORDERING NUMBER: LB1008AE

The LB1008 integrated circuit requires only four capacitors, two resistors, a ceramic resonator, a surge protection diode, and a polarity guard to provide all of the touch-tone electronic functions. Four basic telephone functions are accomplished: furnishes AC and DC loop termination diring the on-hook state; transmits and receives voice signals within performance guidelines (including transducer variations); provides dual-tone multi-frequency (DTMF) signals to the Central Office; properly distinguishes between spurious noise and genuine ringing signals providing a distinctive audible alerter output.

Fig. 1 - Functional Diagram



PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	V+	The most positive DC voltage (must be filtered externally). This voltage is derived from the Tip-Ring input and is used to supply internal circuits. No current can be taken from V+ without changing the characteristics as shown in Figure 3.
2	SW	Turns on trasmit/receive circuitry when connected through switch hook contact to V+
3 4	AL2 AL1	Output terminals for driving an alerter. The ringer logic distinguishes between genuine ringing and other noise signals present on the telephone loop, and provides a distinctive audible output. The alerter can be driven differentially or single ended. If the alerter is driven single ended to RP, the second output can be used to drive a visible indicator to RP. Volume can be adjusted by placing a resistor in series with terminals AL1 or AL2.
5	AS	Logic input used to determine alerter frequency. This pin can be programmed via a microprocessor or mechanically set to provide an output frequency of 1200 Hz shifted to 1500 Hz, (AS pin set to logic low or left open), or 1800 Hz frequency shifted to 2250 Hz, (AS pin set to logic high or pulled up to V+ through a 100kΩ resistor).
6 7 8	C3 C2 C1	Keyboard inputs for columns 1 through 3. High frequency touchtone signals are controlled by these inputs. These inputs are disabled when the telephone goes on hook. Single tones are generated when two rows or two columns are activated. Diagonals result in no tones. A high frequency and a low frequency tone can be generated by connecting the appropriate column to the desired row pin via the keypad crosspoint switch. An alternative method for generating a single high frequency is to connect the appropriate column to V+ through a 50k resistor.
9 10 11 12	R4 R3 R2 R1	Keypad inputs for rows 1 through 4. Low frequency touch-tone signals are controlled by these inputs. These inputs are disabled when the telephone is on hook. Single tones are generated when two rows or two columns are activated. Diagonals result in no tones. See note for pins 6, 7, 8. An alternative method for generating a single low frequency is to connect the appropirate row pin to RP through a 50k resistor.
13	OS	Resonator connection. A 480 KHz ceramic resonators is placed between this pin and RP. This resonator is used to provide the precise frequency required to generate the DMTF tones.

PIN DESCRIPTION

Pin	Name	Description
14	SG	Signal Ground for use with the receiver output drive. The receiver can be placed between this pin and RO without a decoupling capacitor.
15	RO	Receiver Output. Optimum receiver impedance is 600Ω, the circuit will provide 2 dB less power to a 150Ω receiver. A receiver can be placed between RO and RP or between RO and SG. If the receiver is connected between RO and RP, a decoupling capacitor must be used.
16	TX	Input from transmitter which must be capacitively coupled. This input has a 40kΩ input impedance.
17	TP	The Tip Prime terminal is the more positive input to the Power Conditioner and Speech Network. It connectes to Tip-Ring on the positive side of the polarity guad.
18	NC	No connection. This pin may not be use as a tie point for external circuitry.
19	DR	The driver terminal is use to dump extra line current to an external load resistor. This reduces the power consumption in the telephone chip on short loops. The terminal can be use to a power an LED if desired.
20	RP	The Ring Prime terminal is the the logic common or DC ground point.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{TP}	Circuit Voltage	20	V
I_{TP}	Circuit Current	120	mA
P_{tot}	Total Power Dissipation	0.5	W
T_{op}	Operating Temperature	0 to 60	°C
T_{stg}, T_j	Storage and Junction Temps.	−45 to 125	°C

THERMAL DATA

R_{TH}	Thermal impedance, junction to ambient	61	°C/W

ELECTRICAL CHARACTERISTICS (at 25°C unless othewise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
OFF-HOOK DC TESTS					
V_{TP}	I_{TP} = 8mA, speech	3.00	—	3.35	
	I_{TP} = 20mA, speech	3.80	—	4.30	
	I_{TP} = 90mA, speech	5.35	—	6.75	
	I_{TP} = 20mA, dialing	4.10	—	4.56	
V_{V+}	I_{TP} = 8mA, speech	2.66	—	2.78	V
	I_{TP} = 20mA, speech	2.75	—	3.20	
	I_{TP} = 90mA, speech	4.50	—	5.60	
$V_{TP} - V_{V+}$	I_{TP} = 20mA, dialing	1.20	—	1.55	
I_{DR}	I_{TP} = 20mA, speech	9.0	—	11.0	
	I_{TP} = 90mA, speech	70.5	—	73.5	
	I_{TP} = 20mA, dialing	7.5	—	9.7	
	I_{TP} = 90mA, dialing	69.0	—	72.0	
$I_{TP,u,s}$	Upper Switch Point, speech	15.5	—	19.5	mA
$I_{TP,l,s}$	Lower Switch Point, speech	11.5	—	15.0	
$I_{hys,s}$	$I_{TP,u,s} - I_{TP,l,s}$	4.5	—	—	

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
OFF-HOOK DC TESTS (Continued)					
$I_{TP,l,d}$	Lower Switch Point, dialing	12.0	—	16.0	
$I_{hys,d}$	$I_{TP,u,s} - I_{TP,l,d}$	3.5	—	—	
$V_{RO} - V_{SG}$	I_{TP} = 20mA, speech I_{TP} = 20mA, dialing	−0.1 −0.1	— —	0.1 0.1	V
OFF-HOOK AC TESTS					
$G_{XMIT} = v_{TP}/v_{TX}$	I_{TP} = 8mA I_{TP} = 20mA v_{TX} = 0.1Vrms I_{TP} = 90mA	4.3 6.2 4.3	— — —	6.2 8.9 6.2	—
$G_{RCV} = v_{RCV}/v_{CO}$	I_{TP} = 20mA I_{TP} = 90mA v_{CO} = 0.5Vrms	0.25 0.25	— —	0.45 0.45	
$R_{TX} = v_{TX}/i_{TX}$	I_{TP} = 20mA v_{TX} = 0.1Vrms	—	25K	—	
$R_{RO} = v_{RO}/i_{RO}$	I_{TP} = 20mA v_{RO} = 0.1Vrms	—	600	—	
$R_{TP} = v_{TP}/i_{TP}$	I_{TP} = 20mA I_{TP} = 90mA v_{CO} = 0.5Vrms	650 650	— —	950 850	
$G_{SDT} = v_{RCV}/v_{TX}$	I_{TP} = 8mA I_{TP} = 20mA v_{TX} = 0.1Vrms I_{TP} = 90mA	1.0 1.0 1.0	— — —	1.5 1.5 1.5	—
$v_{TP,l}$, low group out	I_{TP} = 20mA	0.291	—	—	
$v_{TP,h}$, high group out	I_{TP} = 20mA	0.367	—	—	Vrms
$v_{TP,e}$ Extraneous voice-band signals	I_{TP} = 20mA, dialing	—	—	0.045	
$v_{TP,l,h}$ total DTMF, both groups	I_{TP} = 90mA, dialing	—	—	0.869	
$G_{XMIT} = v_{TP}/v_{TX}$	I_{TP} = 20mA, v_{TX} = 0.1Vrms dialing	—	—	0.03	—
ON-HOOK DC TESTS					
I_{TP}	V_{TP} = 3V	—	—	35	μA
$V_{TP,th}$, Thershold of detection	Ringing detected	5.9	—	6.7	V
I_{TP}	V_{TP} = 10V V_{TP} = 20V	1.5 1.5	— —	2.0 2.5	mA
ON-HOOK AC TESTS					
$v_{AL} = v_{AL2} - v_{AL1}$	V_{TP} = 10V V_{TP} = 20V	5.0 15.0	— —	7.0 17.0	V_{p-p}

Fig. 2 - DC Loop Operation Dial Mode

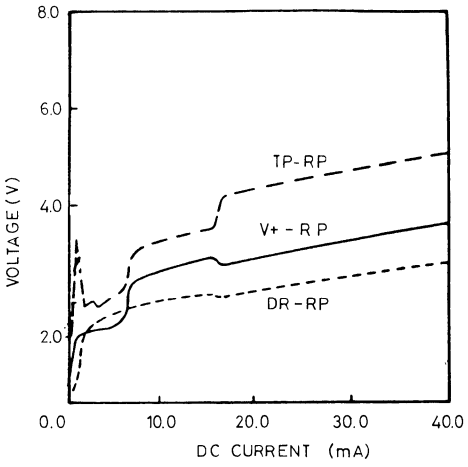
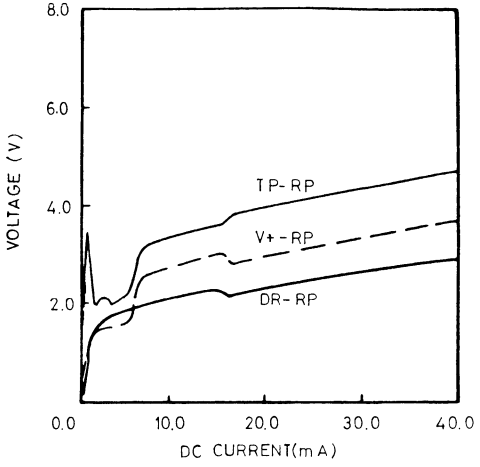


Fig. 3 - DC Loop Operation Speech Mode



APPLICATION

Dual Tone Multi Frequency generation (DTMF)
This circuit is intended to operate with a 3-column, 4-row external keypad. The keypad should be of the type which interconnects the appropriate row and column leads when a key is depressed. The interconnection resistance should be less than 1kΩ. If two row keys with the same column are depressed, a single frequency corresponding to that column will be generated. In a similar manner, two column keys with the same row will generate that row's fequency. If two keys are depressed which do not have a common row or column, no tones will be generated. The DTMF can also be controlled with a microprocessor by driving the inputs through 50k resistors. A logic "high" on a column input will generate the appropriate column frequency. A logic "low" on a row input will generate the appropriate row frequency. A row and column must be selected to generate a dual frequency tone. The frequencies associated with each row and column pin are shown in Table 1.

Ringing Alerter
The ringing detector determines the presence of a true incoming ringing signal by incrementing an up/down counter depending upon the instantaneous magnitude of the incoming signal. The external series RC network has been selected to optimize discrimination between valid ringing signals and extraneous noise signals. It also provides an on hook type B ringer equivalency. Alerter outputs AL1 and AL2 can be used to drive an external piezoelectric transducer. The load can be applied from AL1 to RP for single ended drive or between AL1 and AL2 for differential push-pull drive (larger amplitude). The volume can be reduced by placing resistors in series with the load. The alerting signal is a square wave alternating between 1800 Hz and 2250 Hz (AS high, or 1200 Hz and 1500 with AS low) at a 20 Hz repetition rate.

APPLICATION (Continued)

Polarity Guard:
An external bridge rectifier ensures proper voltage polarity on the device, with a minimum voltage drops across the bridge rectifier.

Oscillator:
An external 480 kHz ceramic resonator, in conjunction with an internal oscillator control circuit, is used to provide timing functions for the logic circuits, (see Figure 4).

Power Conditioner:
This set of circuits provides accurate temperature compensated current and voltage references for the other circuit blocks. It also sets the loop loading and digital reset states for the various types of operation, i.e., on-hook, off-hook, and multiple telephone sets. For loop current greater than 5mA, the DR port can be used to power an electret preamplifier or an external LED.

Speech Network:
This analog circuit block provides proper transmission levels in both directions. Since the local talker's signal is larger than (on the average) the received signal at the telephone set terminals, an out-of-phase portion of the transmitted signal is also sent to the receiver. This proportion is designed to provide a level in the talker's ear (the "sidetone") between "too hot" and "dead". the DTMF D/A converter is placed in the transmit path during dialing, while the receive-gain path is simultaneously attenuated.

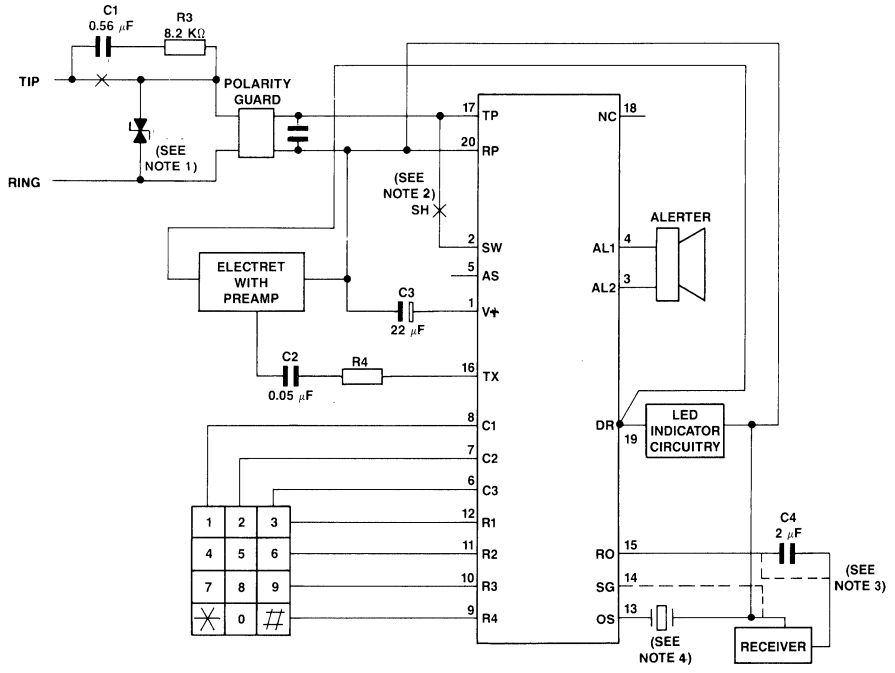
External Components:
As shown in the functional diagram (see Figure 4) the LB1008 needs only four capacitors, an external polarity guard, two resistors, a 480 kHz ceramic alerter, and a surge protection diode to provide basic touch-tone electronic functions. An alerter, a telephone set (containing the transmitter and receiver) and a keypad with a maximum series resistance of 1kΩ are also illustrated.

The application diagram (see Figure 4) contains more detailed information. It shows components for connecting to the telephone loop and optional connection components.

Table 1

Pin Name	Keypad Input	Tones (Design Value)
R1	Row 1	697 Hz
R2	Row 2	770 Hz
R3	Row 3	852 Hz
R4	Row 4	941 Hz
C1	Column 1	1209 Hz
C2	Column 2	1336 Hz
C3	Column 3	1447 Hz

Fig. 4



NOTES:
1. 18V, 150 amp surge protector. (LS5018)
2. SH denotes switch hook.
3. Options for 5-wire handset (eliminating C4) are shown.
4. Ceramic Resonator.

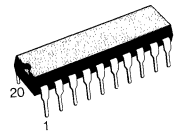
LB1009

PRELIMINARY DATA

AN AT&T PRODUCT

MICROPROCESSOR CONTROLLED, SINGLE-CHIP TELEPHONE INTEGRATED CIRCUIT

- CAPABLE OF SPEECH TRANSMISSION DOWN TO 3mA LOOP CURRENT
- A FEATURE MODE FUNCTION INDICATES POWER PORT (DR) STATUS
- PROVIDES A POWER PORT FOR DRIVING A LED OR A MICROPROCESSOR
- AN ALERTER SELECT OPTION OF 1200 Hz/ 1500 Hz OR 1800 Hz/2250 Hz
- REQUIRES ONLY A 2 CONTACT SWITCH HOOK
- COMPATIBLE WITH ELECTRET MICROPHONES
- OPERATES FROM POWER SUPPLIED BY THE CENTRAL OFFICE

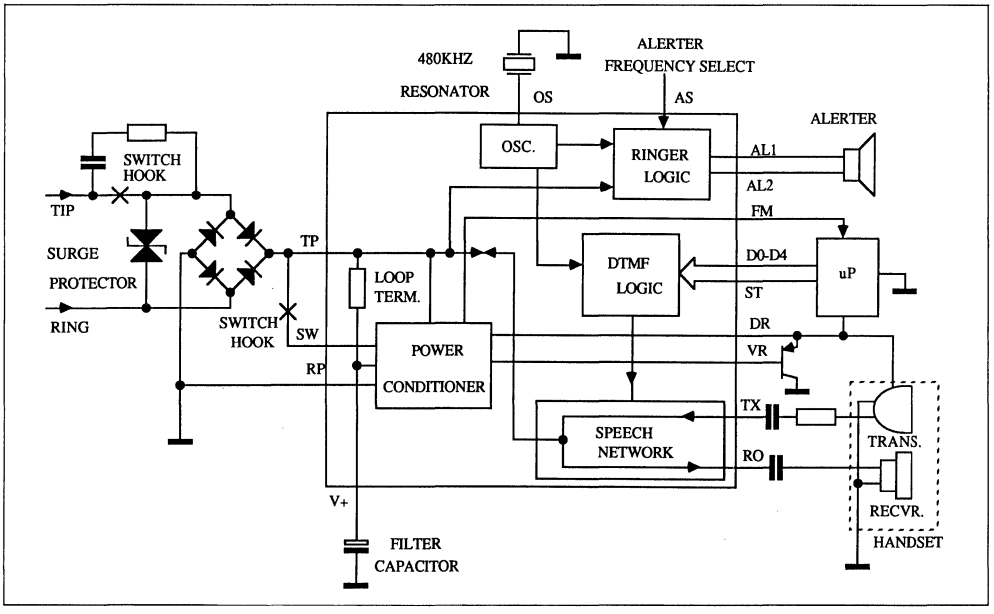


DIP-20 B Plastic

ORDERING NUMBER: LB1009AE

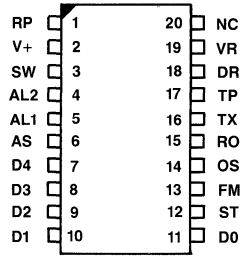
The LB1009 integrated circuit requires only four capacitors, one resistor, a ceramic resonator, a transistor, a surge protection diode, and a polarity guard to provide all of the touch-tone electronic functions. Four basic telephone functions are accomplished: furnishes AC and DC loop termination for both switch hook states; transmits and receives voice signals; provides dual-tone multi-frequency (DTMF) signals to the Central Office; properly distinguishes between spurious noise and genuine ringing signals providing a distinctive audible alerter output.

Fig. 1 - Functional Diagram



LB1009

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	RP	The Ring Prime terminal is the more negative input connected to Tip-Ring on the negative side of the polarity guard bridge. It is also the logic common (ground) point.
2	V+	The most positive DC voltage (filtered) on the device. This voltage is derived from the Tip-Ring inputs. It is used to supply internal circuits.
3	SW	Turns on Transmit/Receive circuitry when connected through switch hook contact to TP.
4 5	AL2 AL1	Output terminals for driving an alerter. The ringer logic distinguishes between genuine ringing and other noise signals present on the telephone loop, and provides a distinctive audible output. The alerter can be driven differentially or single ended. If the alerter is driven single ended to RP, the second output can be used to drive a visible indicator to RP. Volume can be adjusted by placing a resistor in series with terminals AL1 or AL2.
6	AS	Logic input used to determine alerter frequency. This pin can be programmed via a microprocessor or mechanically set to provide an output frequency of 1200 Hz shifted to 1500 Hz, (AS pin set to logic low or left open), or 1800 Hz frequency shifted to 2250 Hz, (AS pin set to logic high or pulled up to V+ through a 100kΩ resistor).
7 8 9 10 11	D4 D3 D2 D1 D0	DTMF signals are controlled by these inputs via a microprocessor. These inputs are disabled when the telephone goes on-hook and in the low power mode (FM open). These inputs are CMOS and TTL compatible (See Table 1)
12	ST	Data Strobe from microprocessor. It loads the DTMF inputs on a rising edge pulse.
13	FM	Feature Mode is an open collector output which shorts to RP when the telephone goes off-hook. Long loops (with two telephones off-hook) can result in a "speech only, low power" mode of operation. FM will "open circuit" under these conditions.
14	OS	Resonator connection. This logic is designed to operate with a some 480 KHz ceramic resonator. The resonator frequency is divided down to perform various synchronous clock tasks.
15	RO	Output to 600Ω receiver, capacitively coupled.
16	TX	Input from the transmitter, capacitively coupled.
17	TP	The Tip Prime terminal is the more positive input to the Power Conditioner and Speech Network. It connects to Tip-Ring on the positive side of the polarity guard bridge.
18	DR	A low impedance regulated port for powering a microprocessor and transmitter. Currents (in the full feature mode) will provide a minimum of 800μA for a maximum of 3.3 volts. Excess set current not used by internal circuits will appear on DR to power external circuits. Current not used by external circuits will be passed to RP via an external PNP transistor.
19	VR	This voltage is a reference when the set is off-hook. When connected to DR via PNP transistor (see Fig. 4), a regulated voltage is produced on DR.
20	NC	No connection. This pin may not be use as a tie point for external circuitry.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{TP}	Circuit Voltage	20	V
I_{TP}	Circuit Current	120	mA
P_{tot}	Total Power Dissipation	0.5	W
T_{op}	Operating Temperature	0 to 60	°C
T_{stg}, T_j	Storage and Junction Temps.	−45 to 125	°C
—	Pin temperature (soldering 15 sec)	300	°C

THERMAL DATA

R_{TH}	Thermal impedance, junction to ambient	61	°C/W

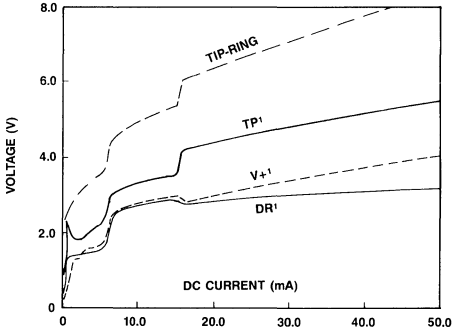
ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
OFF-HOOK DC TESTS					
V_{TP}	I_{TP} = 8mA, speech	3.00	—	3.35	
	I_{TP} = 20mA, speech	3.80	—	4.30	
	I_{TP} = 90mA, speech	5.35	—	6.75	
	I_{TP} = 20mA, dialing	4.10	—	4.56	
V_{V+}	I_{TP} = 8mA, speech	2.66	—	2.78	V
	I_{TP} = 20mA, speech	2.75	—	3.20	
	I_{TP} = 90mA, speech	4.50	—	5.60	
$V_{TP} - V_{V+}$	I_{TP} = 20mA, dialing	1.20	—	1.55	
I_{DR}	I_{TP} = 20mA, speech	9.0	—	11.0	
	I_{TP} = 90mA, speech	70.5	—	73.5	
	I_{TP} = 20mA, dialing	7.5	—	9.7	
	I_{TP} = 90mA, dialing	69.0	—	72.0	
$I_{TP,u,s}$	Upper Switch Point, speech	15.5	—	19.5	
$I_{TP,l,s}$	Lower Switch Point, speech	11.5	—	15.0	mA
$I_{hys,s}$	$I_{TP,u,s} - I_{TP,l,s}$	4.5	—	—	
$I_{TP,l,d}$	Lower Switch Point, dialing	12.0	—	16.0	
$I_{hys,d}$	$I_{TP,u,s} - I_{TP,l,d}$	3.5	—	—	
$V_{RO} - V_{SG}$	I_{TP} = 20mA, speech	−0.1	—	0.1	V
	I_{TP} = 20mA, dialing	−0.1	—	0.1	
OFF-HOOK AC TESTS					
$G_{XMIT} = v_{TP}/v_{TX}$	I_{TP} = 8mA	4.3	—	6.2	
	I_{TP} = 20mA v_{TX} = 0.1Vrms	6.2	—	8.9	
	I_{TP} = 90mA	4.3	—	6.2	—
$G_{RCV} = v_{RCV}/v_{CO}$	I_{TP} = 20mA v_{CO} = 0.5Vrms	0.21	—	0.30	
	I_{TP} = 90mA	0.21	—	0.30	

ELECTRICAL CHARACTERISTICS (Continued)

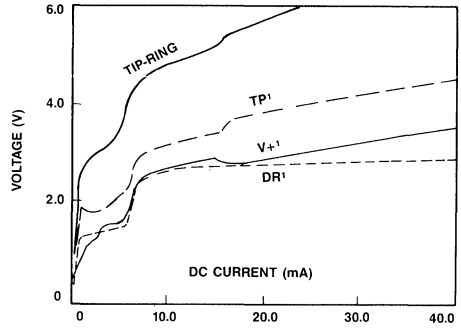
Parameter	Test Conditions	Min	Typ	Max	Unit
OFF-HOOK AC TESTS (Continued)					
$R_{TX} = v_{TX}/i_{TX}$	I_{TP} = 20mA v_{TX} = 0.1Vrms	—	30K	—	Ω
$R_{RO} = v_{RO}/i_{RO}$	I_{TP} = 20mA v_{RO} = 0.1Vrms	—	600	—	Ω
$R_{TP} = v_{TP}/i_{TP}$	I_{TP} = 20mA, v_{CO} = 0.5Vrms I_{TP} = 90mA, v_{CO} = 0.5Vrms	650 650	— —	950 850	Ω
$G_{SDT} = v_{RCV}/v_{TX}$	I_{TP} = 8mA, v_{TX} = 0.1Vrms I_{TP} = 20mA, v_{TX} = 0.1Vrms I_{TP} = 90mA, v_{TX} = 0.1Vrms	0.3 0.3 0.3	— — —	0.6 0.6 0.6	—
$v_{TP,l}$, low group out	I_{TP} = 20mA	0.291	—	—	Vrms
$v_{TP,h}$, high group out	I_{TP} = 20mA	0.367	—	—	Vrms
$v_{TP,e}$ Extraneous voice-band signals	I_{TP} = 20mA, dialing	—	—	0.045	Vrms
$v_{TP,l,h}$ total DTMF, both groups	I_{TP} = 90mA, dialing	—	—	0.869	Vrms
$G_{XMIT} = v_{TP}/v_{TX}$	I_{TP} = 20mA, v_{TX} = 0.1Vrms dialing	—	—	0.03	—
ON-HOOK DC TESTS					
I_{TP}	V_{TP} = 3V	—	—	35	μA
$V_{TP,th}$, Threshold of detection	Ringing detected	5.9	—	6.7	V
I_{TP}	V_{TP} = 10V V_{TP} = 20V	1.5 1.5	— —	2.0 2.5	mA
ON-HOOK AC TESTS					
$v_{AL} = v_{AL2} - v_{AL1}$	V_{TP} = 10V V_{TP} = 20V	5.0 15.0	— —	7.0 17.0	V_{p-p}

Fig. 2 - Typical DC V-I Characteristics (Dial Mode)



Note 1 Voltages measured with respect to Ring Prime (RP)

Fig. 3 - Typical DC V-I Characteristics (Speech Mode)



APPLICATION

(Refer to Functional Diagram, Fig. 1)

Polarity Guard:
An external bridge rectifier (see Figure 4) ensures proper voltage polarity on the device, with a minimum voltage drop across the bridge rectifier.

Oscillator:
An external 480 KHz ceramic resonator, in conjunction with an internal oscillator control circuit, is used to provide timing functions for the logic circuits.

DTMF Generation Logic:
This circuit connects to a microprocessor. The logic circuitry decodes the microprocessor input states to generate accurately timed digital control signals for a D/A converter.

Ringer Logic:
This circuit determines the presence of a true incoming ringing signal by up or down counting, depending upon the instantaneous magnitude of an incoming transient. After a positive decision, the logic provides suitable timed inputs to an external alerter device. Volume can be controlled by placing resistors in series with leads AL1 or AL2. See "AS" pin description for alerter frequency-select capability.

Power Conditioner:
This set of circuits provides accurate temperature compensated current and voltage references for the other circuit blocks. It also sets the loop loading and digital reset states for the various types of operation, i.e., on-hook, off-hook, and multiple telephone sets.

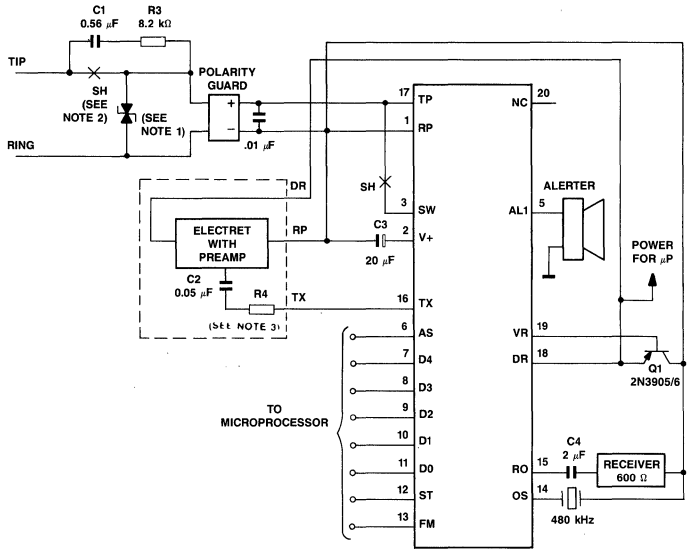
Speech Network:
This analog circuit block provides proper transmission levels in both directions. Since the local talker's signal is normally larger than the received signal at the telephone set terminals, an out-of-phase portion of the transmitted signal is also sent to the receiver. This proportion is designed to provide a level in the talker's ear (the "sidetone") between "too hot" and "dead". The DTMF D/A converter is placed in the transmit path during dialing, while the receive-gain path is simultaneouly attenuated. Transmit mute is provided independently of receive mute and is under control of the microprocessor. Transmit mute is not functional in the speech only mode (telephone set current is below approximately 16mA). When transmit mute is functional, it provides a minimum of 40 dB attenuation.

Driver (DR) and Voltage Regulator (VR) Ports: (see Pin Description Key)

External Components:
Only two switch hook contacts are required with this device. In going off-hook, the contact connected to the SW pin should open simultaneously with, or before the other switch hook contact. As shown in the functional diagram (see Figure 1), the LB1009 needs only four capacitors, one resistor, a ceramic resonator, a transistor, a surge protection diode, and a polarity guard to provide all of the basic touch-tone electronic functions. An alerter, a telephone handset (containing the transmitter and receiver), and a microprocessor are also illustrated.

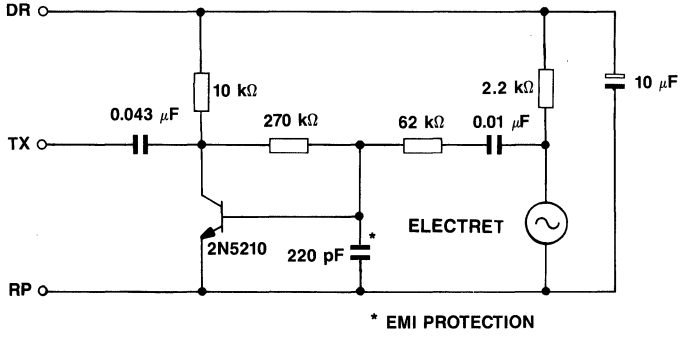
The application diagram (see Figure 4) contains detailed information. The LB1009 can be used in a 4-wire handset application.
A preamplifier circuit which can be used with a microphone is shown in Fig. 5.

Fig. 4 - Typical Application Diagram



NOTES:
1. 18 volt, 150 amp surge protector. (LS5018)
2. SH denotes switch hook.
3. Value of R4 adjusts transmit gain for various applications.

Fig. 5 - Electret Interface Circuitry



NOTE: This interface circuit may be used for some commercially available electrets.

Table 1 - Microprocessor Control Logic table.

DTMF Signal Inputs					Mode of Operation	Tones (Design Value)	
D4	D3	D2	D1	D0			
1	0	0	0	*	Dial	L1 (697 Hz)	Single Tones
1	0	1	0	*	Dial	L2 (770 Hz)	
1	1	0	1	0	Dial	L3 (825 Hz)	
1	1	1	1	0	Dial	L4 (941 Hz)	
1	1	*	0	0	Dial	H1 (1209 Hz)	
1	1	*	0	1	Dial	H2 (1336 Hz)	
1	0	*	1	0	Dial	H3 (1477 Hz)	
0	0	0	0	0	Dial	H1, L1	DTMF Tones
0	0	0	0	1	Dial	H2, L1	
0	0	0	1	0	Dial	H3, L1	
0	0	1	0	0	Dial	H1, L2	
0	0	1	0	1	Dial	H2, L2	
0	0	1	1	0	Dial	H3, L2	
0	1	0	0	0	Dial	H1, L3	
0	1	0	0	1	Dial	H2, L3	
0	1	0	1	0	Dial	H3, L3	
0	1	1	0	0	Dial	H1, L4	
0	1	1	0	1	Dial	H2, L4	
0	1	1	1	0	Dial	H3, L4	
*	0	0	1	1	Speech, Transmit Mute		Special Functions
*	0	1	1	1	Speech		
*	1	0	1	1	Dial, No Tone		

* = Don't Care

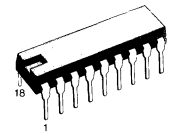
LB1010

PRELIMINARY DATA

AN AT&T PRODUCT

OCTAL LINE PROTECTOR

- BI-DIRECTIONAL CLAMPING
- CLAMP THRESHOLD TRACKS SUPPLY VOLTAGE TO 7.0 VOLTS
- PROTECTS 8 LINES
- INPUT STAND-OFF VOLTAGE UP TO 65 VOLTS (AFTER ON-CHIP FUSE OPENS)

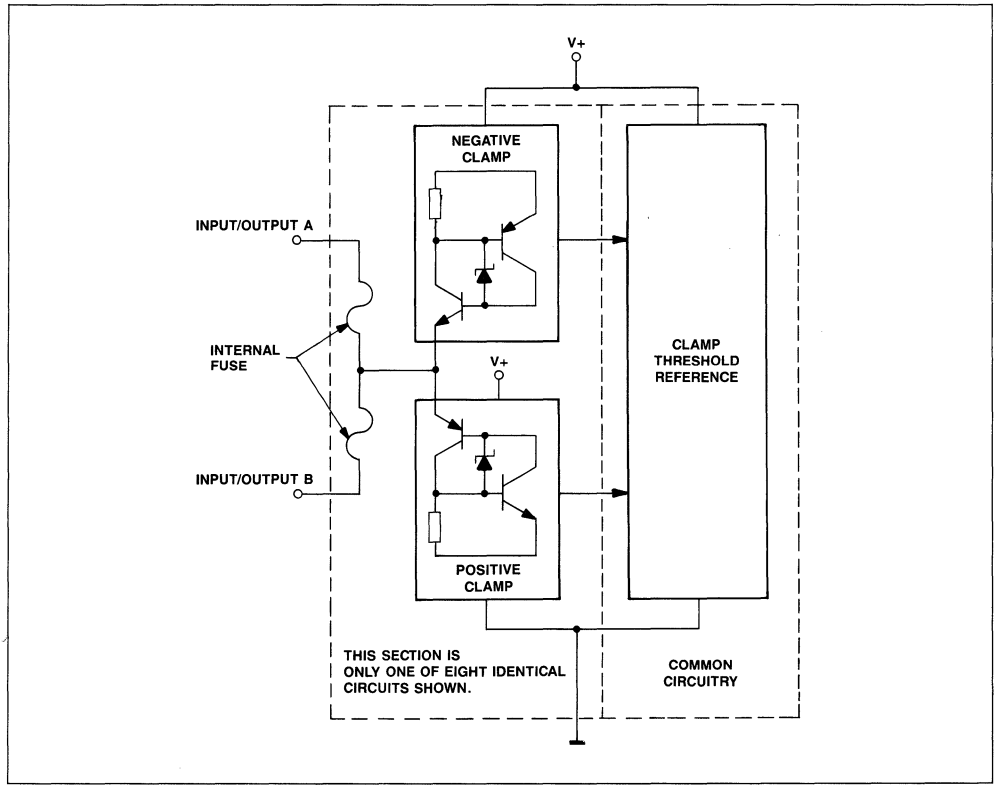


DIP-18 C Plastic

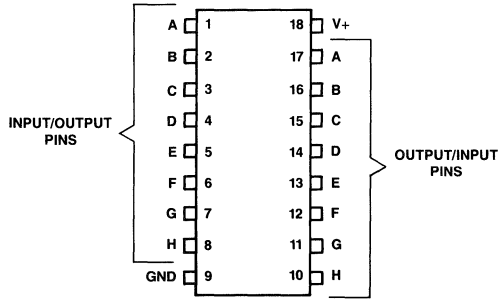
ORDERING NUMBER: LB1010AD

The LB1010 integrated circuit is a bi-directional over-voltage/over-current limiting device that protects up to eight digital lines. This circuit contains 16 on-chip fuses, 8 voltage/current clamps, and a threshold reference which tracks the power supply. In operation, transient on-line surges (within specified limits) are clamped to a safe level. However, if an extraordinarily high current fault is detected (on the order of 1 amp), an on-chip fusing component will open, protecting your electronic circuits.

Fig. 1 - Functional Diagram



PIN CONFIGURATION



COMPLEMENTARY INPUT/OUTPUT LEADS MAY BE INTERCHANGED FOR BIDIRECTIONAL OPERATION.

PIN DESCRIPTION

Pin	Symbol	Description
1-8	Input/Output (A-H)	Input/Output (I/O) pins A through H, respectively. The LB1010 device consists of eight independent protector sections (Figure 1) designated by the letters A through H. Each protector section has two leads that may be used either as an input terminal or as an output terminal.
9	GND	Circuit common. This pin should be connected to system ground.
10-17	Output/Input (H-A)	Output/Input (O/I) pins H through A, respectively. For reference purposes, pins 1 through 8 are designated as I/O pins, while complementary pins 10 through 17 are designated as O/I pins. Unused I/O and O/I pins may float when not being used.
18	V+	External positive supply voltage pin range is 2.5 to 7.0 volts.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (soldering, 15 sec)	300	°C
Input Stand-off Voltage (after on-chip fuse opens)*	65	V
Input Current Continuous, (each I/O and O/I pin)	±15	mA
Input Current 1% duty cycle (each I/O and O/I pin)	±500	mA
Input Current 50% duty cycle (each I/O and O/I pin)	±50	mA
Voltage (V+ to GND)	7.0	V

* Rating applies from each I/O pin to its complementary O/I pin and vice versa.

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{PS+}	Power Supply Current	(See Fig. 2)	6.0	—	22	mA
I_{BO+}	Positive Breakover Current (1)	(See Fig. 5)	100	—	200	
I_{BO-}	Negative Breakover Current (1)	(See Fig. 5)	−100	—	−250	
I_{REL+}	Positive Release Current (2)	(See Fig. 6)	100	—	350	
I_{REL-}	Negative Release Current (2)	(See Fig. 6)	−75	—	−300	
I_L	Leakage Current	V+ = 3.0V, V_{in} = 0 (See Fig. 3)	—	—	±1.0	
I_L	Leakage Current	V+ = 3.0V, V_{in} = 2.7V (See Fig. 3)	—	—	±10	μA
V_{BO+}	Positive Breakover Voltage	V+ = 3.0V; I = I_{BO+} (See Fig. 5)	3.2	—	4.8	V
V_{BO+}	Positive Breakover Voltage	V+ = 5.0V; I = I_{BO+} (See Fig. 5)	5.3	—	6.6	
V_{BO-}	Negative Breakover Voltage	I = I_{BO-} (See Fig. 5)	−0.3	—	−2.5	
V_{ON+}	Positive On-state Voltage	(See Fig. 5)	1.0	—	2.0	
V_{ON-}	Negative On-State Voltage	(See Fig. 5)	0.5	—	2.0	
V+	Power Supply Voltage		2.5	—	7.0	
R	Built in Fuse Resistance	(See Fig. 4)	1.0	2.5	5.0	Ω
C_L	Line Capacitance	V+ = 5.0V, V_{IN} = 0.3 to 4.7V	—	12.0	—	pF
R+	Positive ON-State Resistance	(See Fig. 5)	—	0.7	—	Ω
R−	Negative ON-State Resistance	(See Fig. 5)	—	0.8	—	
T_T	Fusing Time	I_{surge} = 1.0A	—	6.0	—	μsec

Notes
1 Breakover current is that value of current applied to the specified pin at which the Breakover Voltage peak occurs (Figure 7).
2 A bias current, 1% duty cycle force the device into a low impedance on-state condition. Reduce the current (as specified in the following sentences) and measure the voltage on the pin to which the bias is applied (Figure 8).
The Positive Release Current is recorded when the voltage on the specified pin equals V+.
The Negative Release Current is recorded when the voltate on the specified pin equals zero.

TEST CIRCUITS

Fig. 2

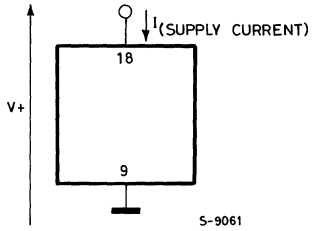


Fig. 3

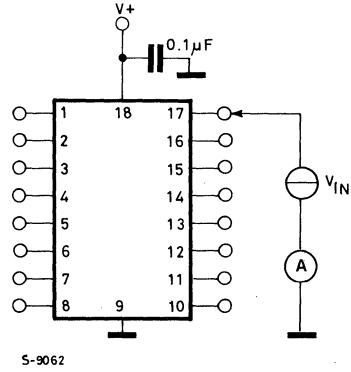


Fig. 4

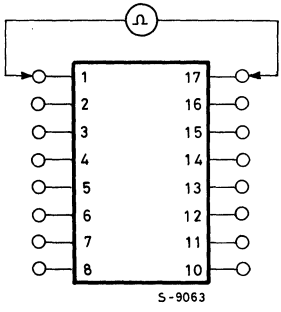
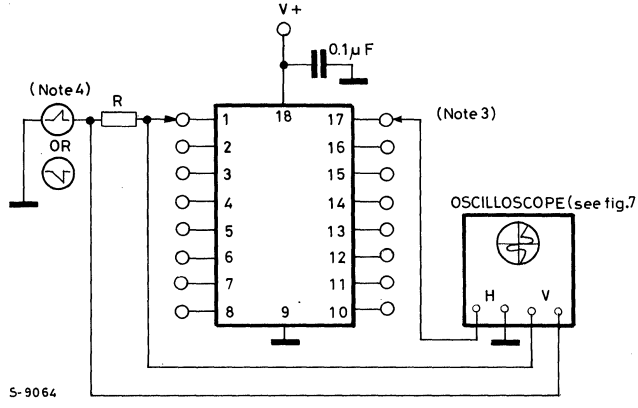
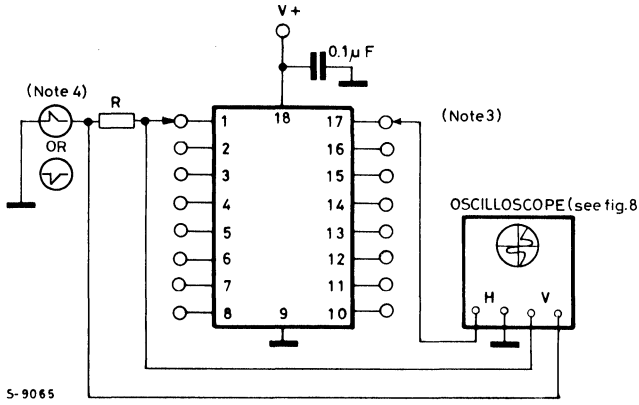


Fig. 5



TEST CIRCUITS (Continued)

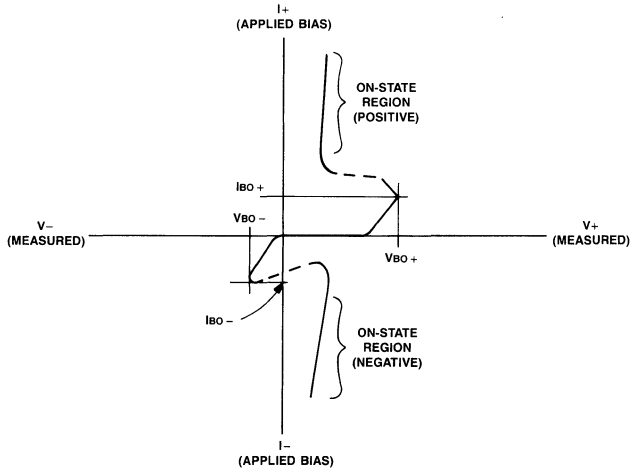
Fig. 6



Note 3: This test applies to each I/O and O/I pin.
4: A ramped bias current (1% duty cycle) is applied to the appropriate I/O or O/I pin. Breakover voltage is measured as the peak magnitude of voltage which occurs as the bias current is increased in magnitude form zero to value which forces the device into the low impedance on-state region of its characteristic (Figure 3). Polarity designations should be observed with respect to GND.

CHARACTERISTIC CURVES

Fig. 7 - Symbology For Test Characteristics



CHARACTERISTIC CURVES (Continued)

Fig. 8 - Release Current Characteristics

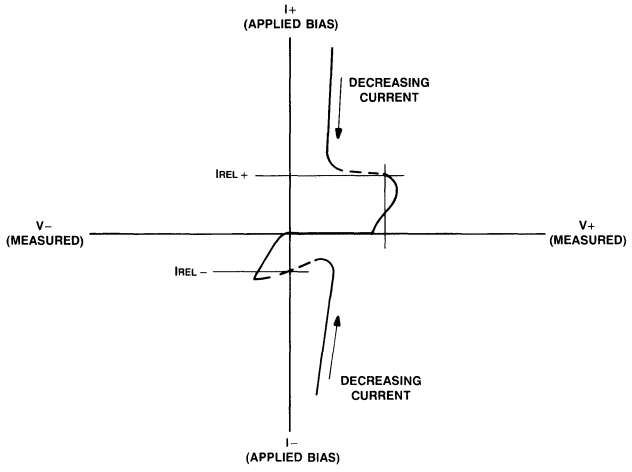


Fig. 9 - Typical Operating Characteristics

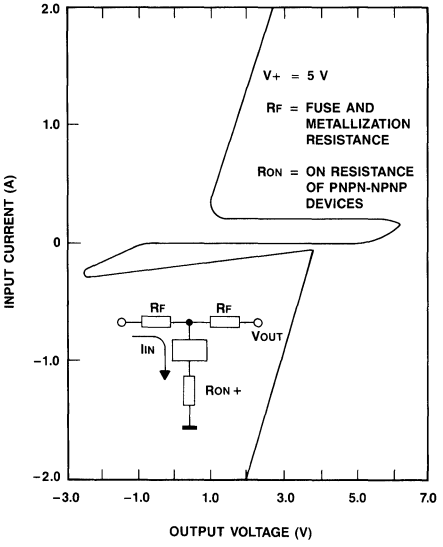
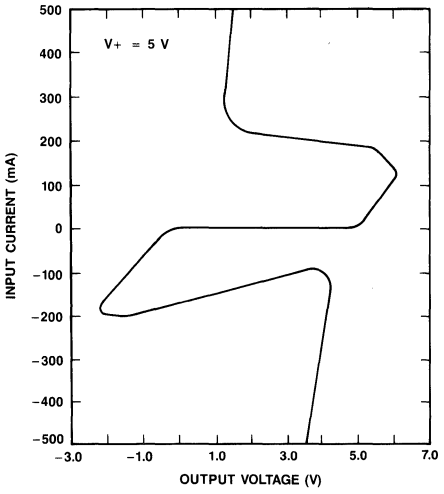
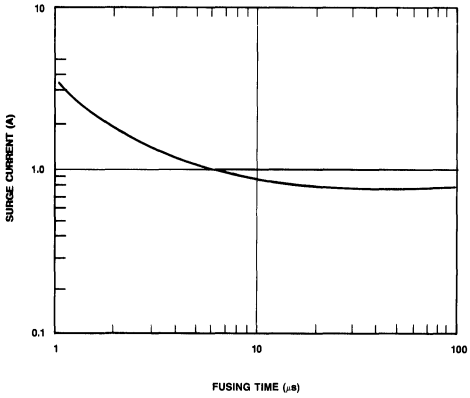


Fig. 10 - Typical Operating Characteristics



CHARACTERISTIC CURVES (Continued)

Fig. 11 - Typical Fusing Characteristics



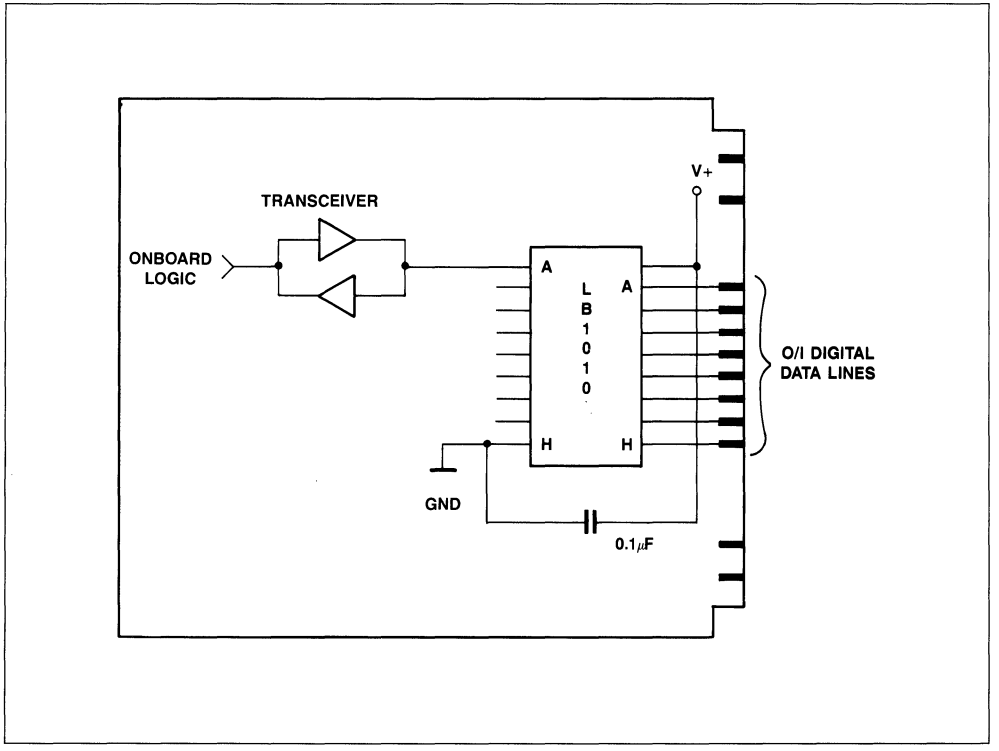
APPLICATION

Figure 5 illustrates the connection for line protection applications. No additional circuitry is needed with the LB1010 other than an 0.1μF ceramic bypass capacitor as close as possible between device leads 9 and 18.

The threshold reference circuit sets the potential above which the positve/negative clamps (see Figure 1) will begin to clamp the data lines. Since the threshold voltage is a function of the external power supply voltage, this device can be used with a variety of logic families up to 7 volts.

If the resulting line current, during a clamped condition, exceeds the values shown in Figure 4 the associated on-chip fuse will "open", permanently disconnecting the affected signal lines until a new LB1010 is installed. The maximum voltage which may be applied to an "open" input line is 65 volts.

Fig. 12 - Octal Line Protector Application Diagram



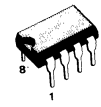
LB1011

PRELIMINARY DATA

AN AT&T PRODUCT

BATTERY FEED

- BASIC BATTERY FEED FUNCTION AT A LOW COST
- HIGH AC IMPEDANCE CHARACTERISTICS FOR BALANCED LINE, DIFFERENTIAL-MODE, VOICE-BAND SIGNALS
- FULL INTERNAL LIGHTNING SURGE PROTECTION UP TO 4 AMPS.
- DC VOLTAGE DROPS CAN BE ADJUSTED TO ACCOMODATE DIFFERENT PEAK SIGNAL LEVELS

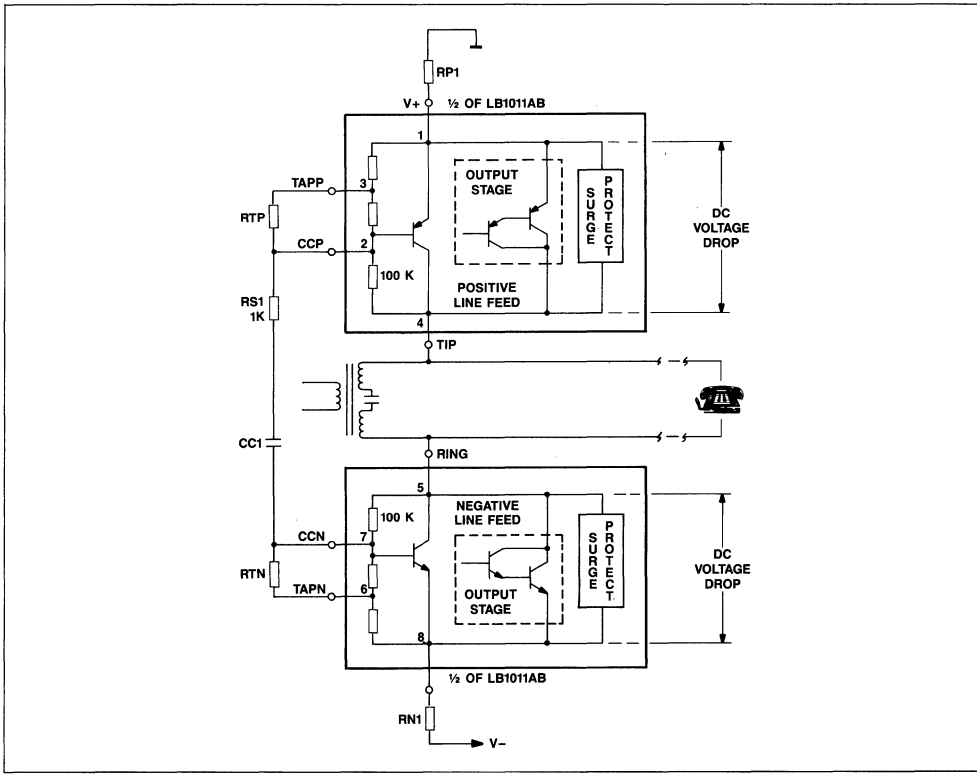


Minidip-A Plastic

ORDERING NUMBER: LB1011AB

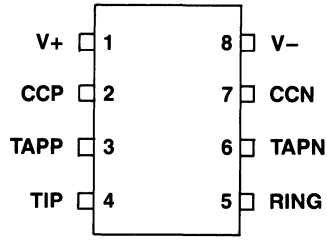
The LB1011 is an electronic battery feed circuit which supplies DC currents to a telephone line with minimal loading on the AC signals. The LB1011 is integrated as two complementary chips to supply DC currents of both negative and positive polarities to either balanced or unbalanced lines. In the balanced line application, this device helps to suppress undesirable common-mode signals.

Fig. 1 - Functional Diagram



LB1011

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	V+	This pin connects to the "most positive" external power supply (in some cases this is ground) through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the "Positive Line Feed" output.
2 7	CCP CCN	"Cross-Coupling", Positive and Negative respectively. A capacitor between these two pins (for balanced line applications) creates a high AC impedance between TIP and RING. Since full Tip-to-Ring voltage appears across these pins, it is recommended that a 1k ohm resistor be placed in series with the cross-coupling capacitor for surge protection purposes. Unbalanced line applications should connect the cross-coupling capacitor to ground so that the common-mode impedance of the output is greatly increased.
3 6	TAPP TAPN	Resistor tap pins. These terminals are used to adjust the "DC VOLTAGE DROP" across the "Positive Line Feed" and the "Negative Line Feed" respectively. The nominal "DC VOLTAGE DROP" is 3 volts when no resistors are connected between pins 2-to-3 or pins 6-to-7 respectively. A short circuit between these same pins will produce a nominal voltage drop of 4 volts. Resistors connected between these pins will produce voltage drops varying between 3 and 4 volts. A higher "DC VOLTAGE DROP" (greater than 3 volts) may be desirable for high operating temperatures, or when the peak value of the AC signals exceed 2.5 volts.
4	TIP	Output of the "Positive Line Feed Supply".
5	RING	Output of the "Negative Line Feed Supply".
8	V–	This pin connects to the "most negative" external power supply through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the "Negative Line Feed" output.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	−20 to + 70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C

ELECTRICAL CHARACTERISTICS: ($T_A = 25°C$ unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Voltage Drop, Positive Line Feed	$I_{V+} = 50mA$ (See Fig. 3)	2.50	—	3.50	V
DC Voltage Drop, Positive Line Feed, High-Level Mode	$I_{V+} = 50mA$ (See Fig. 4) TAPP shorted to CCP	3.75	—	4.85	V
DC Voltage Drop, Negative Line Feed	$I_{V-} = -50mA$ (See Fig. 3)	−2.50	–	−3.50	V
DC Voltage Drop, Negative Line Feed, High – Level Mode	$I_{V-} = -50mA$ (See Fig. 4) TAPN shorted to CCN	−3.60	–	−4.00	V
Shunt Impedance	(See Fig. 14)	18	—	—	KΩ
Common Mode (Longitudinal) Rejection	$V_{IN} = 1.0$ Vrms, f = 1kHz (See Fig. 12) RP1 = RN1 (see fig. 5)	45	–	–	dB
Common Mode (Longitudinal) Rejection, High-Level Mode	TAP shorted to CC (See Fig. 12) $V_{IN} = 1.0$ Vrms, f = 1kHz RP1 = RN1 (see fig. 5)	45	—	—	dB
Distortion	V(TIP to RING) = 1.0 Vrms (See Fig. 13)	—	—	2.0	%
Distortion, High-Level-Mode	TAP shorted to CC (See Fig. 13) V(TIP to RING) = 2.0 Vrms	—	—	2.0	%

TEST SPECIFICATION ($T_A = 25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{BEP}	PNP Base-Emitter Voltage	$I_{PNP} = 50mA$ (See Fig. 2)	−2.0	−1.0	V
ΔV_{BEP}	PNP Base-Emitter Voltage Change	(See Fig. 2) $\Delta V_{BEP} = V_{BEP}(100mA) - V_{BEP}(50mA)$	−250	−25	mV
V_{BEN}	NPN Base-Emitter Voltage	$I_{NPN} = 50mA$ (See Fig. 2)	1.2	2.0	V
ΔV_{BEN}	PNP Base-Emitter Voltage Change	(See Fig. 2) $\Delta V_{BEN} = V_{BEN}(100mA) - V_{BEN}(50mA)$	+25	+250	mV
V_{CEP}	PNP Collector-Emitter Voltage	(See Fig. 3)	2.5	3.5	V
V_{CEN}	NPN Collector-Emitter Voltage	(See Fig. 3)	−3.5	−2.5	V
V_{BF}	BF Total Volts	$I_1 = 50mA$ (See Fig. 4) S1, S2 Open	5.0	6.8	V
ΔV_{BF}	BF Total Voltage Difference	$I_1 = 100mA$ (See Fig. 4) S1, S2 Open $\Delta V_{BF} = V_{BF}(100mA) - V_{BF}(50mA)$	−400	+600	mV
V_{BF}	BF Total Volts (High Level Mode)	$I_1 = 50mA$ (See Fig. 4) S1, S2 Closed	7.2	9.4	V
ΔV_{BF}	BF Total Voltage Difference (High Level Mode)	$I_1 = 100mA$ (See Fig. 4) S1, S2 Closed $\Delta V_{BF} = V_{BF}(100mA) - V_{BF}(50mA)$	−400	+600	mV
V_F	Forward Voltage	$I_T = 200mA$ (See Fig. 5)	—	1.4	V

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_F	Forward Voltage	$I_T = 200mA$ (See Fig. 6)	—	1.4	
		$I_T = 75mA$ (See Fig. 7)	—	1.4	
		$I_T = 75mA$ (See Fig. 8)	—	1.4	
		$I_T = 75mA$ (See Fig. 9)	—	1.4	
		$I_T = 75mA$ (See Fig. 10)	—	1.4	V
V_{BO}	PNPN Breakdown Voltage	$I_T = 35mA$ (See Fig. 5)	−10	−8	
V_S	PNPN Sustain Voltage	$I_T = 200mA$ S1 Closed (See Fig. 6)	−5	−2	
V_{BO}	PNPN Breakdown Voltage	$I_T = -35mA$ S1 Closed (See Fig. 6)	−10	−8	
V_S	PNPN Sustain Voltage	$I_T - 200mA$ S1 Closed (See Fig. 6)	−5	−2	
Z_S	Shunt Impedance	S1, S2 Open (See Fig. 11) Z_S(in ohms) = 100/V_M(in volt)	18	—	KΩ
Z_S	Shunt Impedance	S1, S2 Closed (See Fig. 11) Z_S(in ohms) = 100/V_M(in volt)	18	—	KΩ
L_B	Longitudinal Balance	S1, S2 open (See Fig. 12) $L_B = Log[V_M/V_{IN}]$ (in dB)	−45	—	dB
L_B	Longitudinal Balance	S1, S2 Closed (See Fig. 12) $L_B = Log[V_M/V_{IN}]$ (in dB)	−45	—	dB
T_{HD}	Distorsion Test	S1, S2 Open $V_{IN} = 1V$ rms (See Fig. 13)	—	2	%
T_{HD}	Distorsion High	S1, S2 Closed $V_{IN} = 2V$ rms (See Fig. 13)	—	2	%

TEST CIRCUITS

Fig. 2

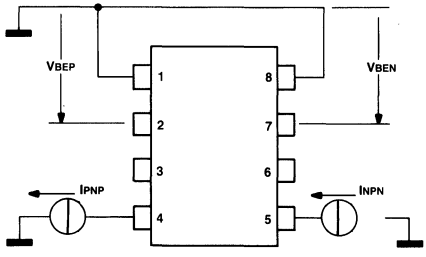
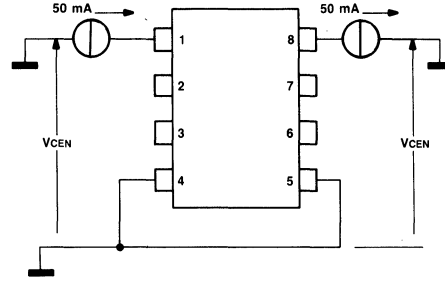


Fig. 3



TEST CIRCUITS (Continued)

Fig. 4

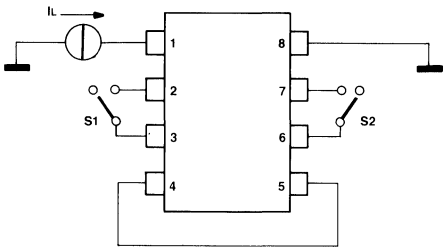


Fig. 5

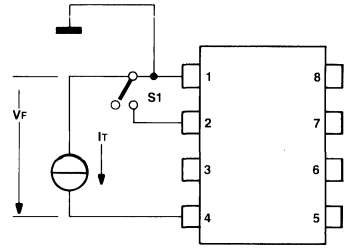


Fig. 6

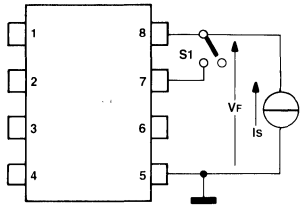


Fig. 7

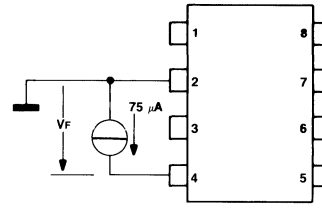


Fig. 8

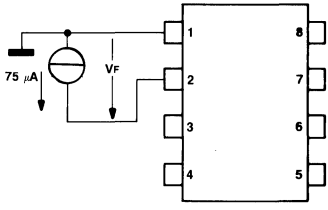
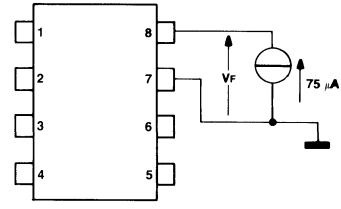


Fig. 9



TEST CIRCUITS (Continued)

Fig. 10

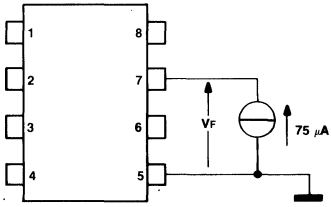


Fig. 11

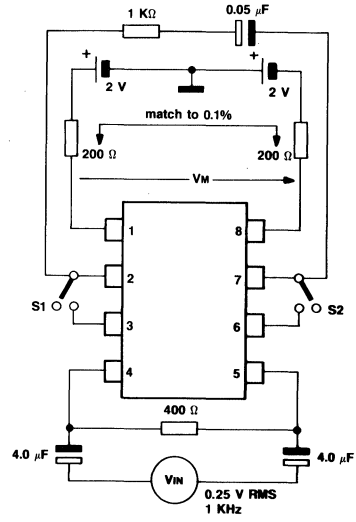


Fig. 12

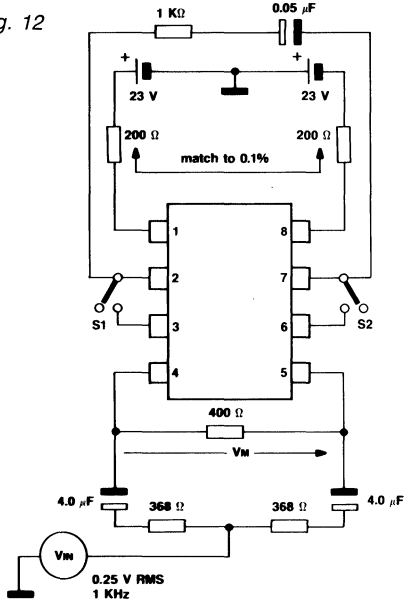


Fig. 13

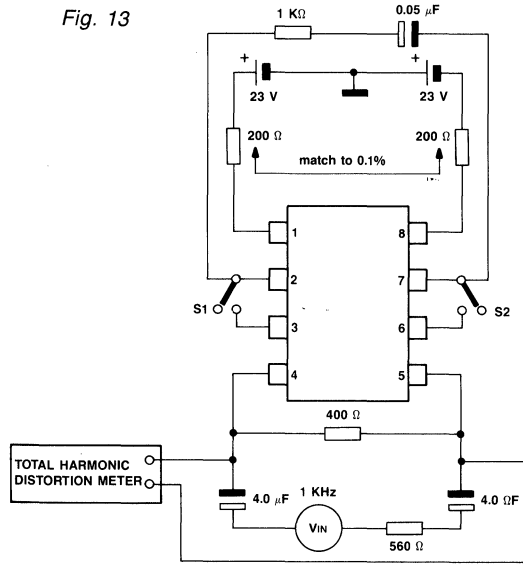
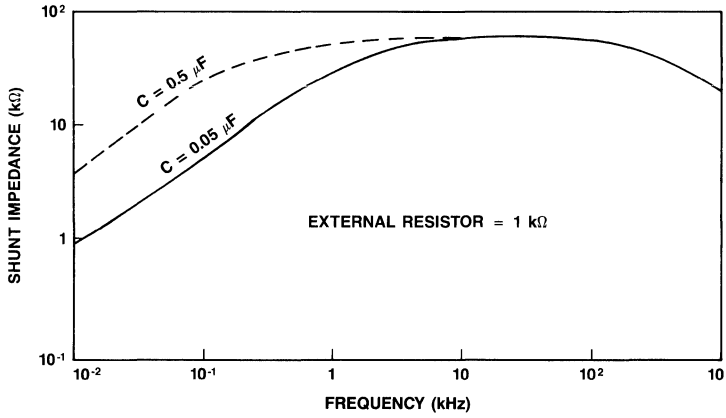


Fig. 14



SURGE PROTECTION CHARACTERISTICS

Internal surge protection circuitry (see Figure 1) in conjunction with external resistors, provides protection against forward voltage surges. Reverse surges are dissipated through large internal diodes bridged across each "Line Feed" section. Forward surge protection consists of a composite PNPN device. This composite PNPN device can withstand surges as shown in Figure 15. It has a breakover point (V_{BO}) of about 9 volts as shown in Figure 16. After breakover, the output is clamped at less than 2 volts as long as the surge source supplies more than 150 mA. When the surge source drops below 150 mA, the PNPN device recovers and normal operation resumes.

Fig. 15 - Maximum Applied Forward Surge Limits (PNPN Composite Device)

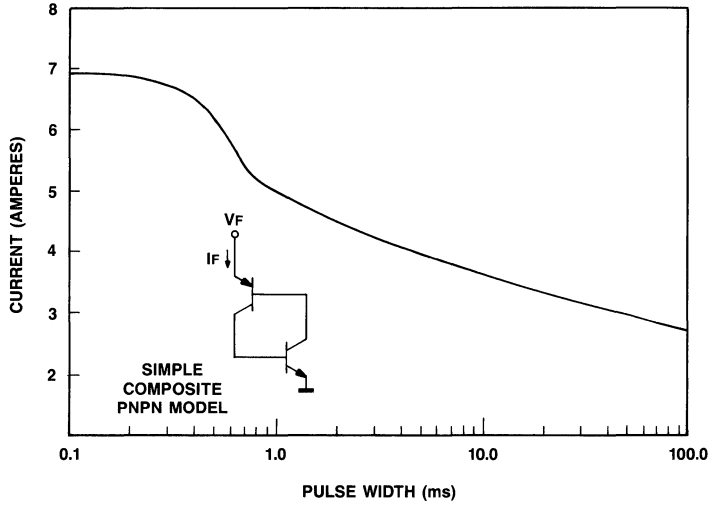
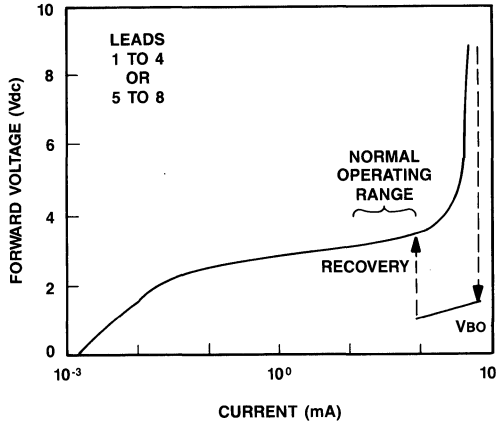


Fig. 16 - Typical Voltage vs Current (PNPN Composite)



APPLICATION

Figure 17 shows the LB1011 in a balanced line configuration. The complementary Positive and Negative Line Feeds are capacitively cross-coupled. Differential signals on the balanced line (TIP-RING) do not disturb the AC ground at the center of the cross-coupled connection. Therefore, both circuits act as constant current sources which present a high shunt impedance of approximately 50K ohms. The cross coupling does not affect feedback for either DC or common-mode signals. Therefore, for common-mode noise, the two complementary power supplies act as low impedance paths to ground through the resistors connected to V+ and V−. Common-mode rejection depends on the degree of matching between resistors RP1 and RN1.
Figure 18 illustrates the LB1011 in a single-ended configuration in which it exhibits a very low DC impedance and a very high AC impedance. In some applications, where DC current needs to flow and AC Current should be blocked, this LB1011 configuration can replace an inductor. It does not, however, have the phase and amplitude vs frequency characteristics of a true inductor or RL network. The TAPP connection (pin 2) permits an external resistor (RTAP) to change the "DC Voltage Drop" (see Figure 1). RTAP can be selected to raise the voltage from 3V (normal operating value) to as high as 4V. This voltage may be desirable for high operating temperature, or if the peak voltage of the AC signal exceeds 2.5V.
Since the "DC Voltage Drop" is relatively constant, the current supplied to the line is controlled by the supply voltage, the external resistor to the supply, and the resistance shunting the line. For AC signals, however, the capacitively-coupled "ground" causes the LB1011 to operate as a constant-current source with an impedance of approximately 25 Kohms.

Fig. 17 - LB1011 Battery Feed Application Diagram (Balanced Configuration)

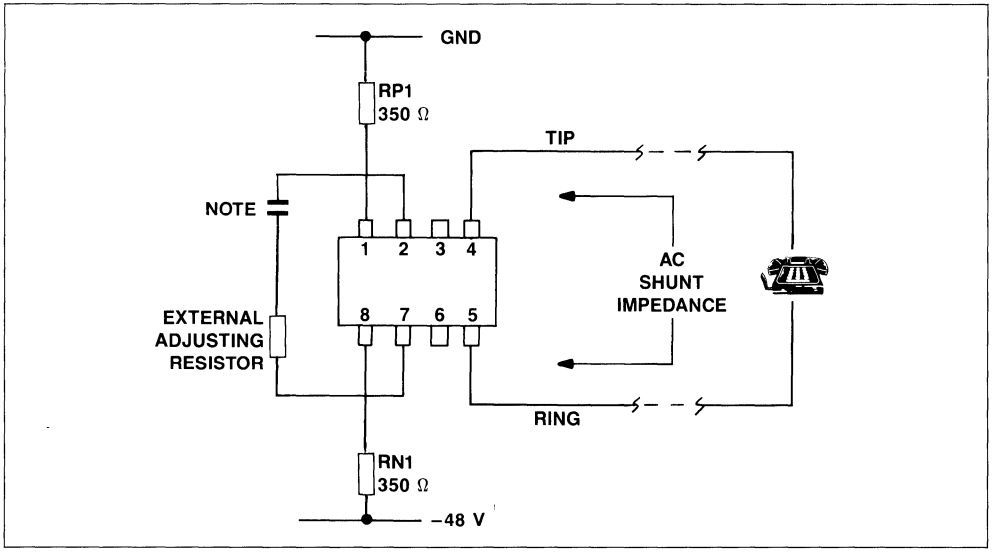
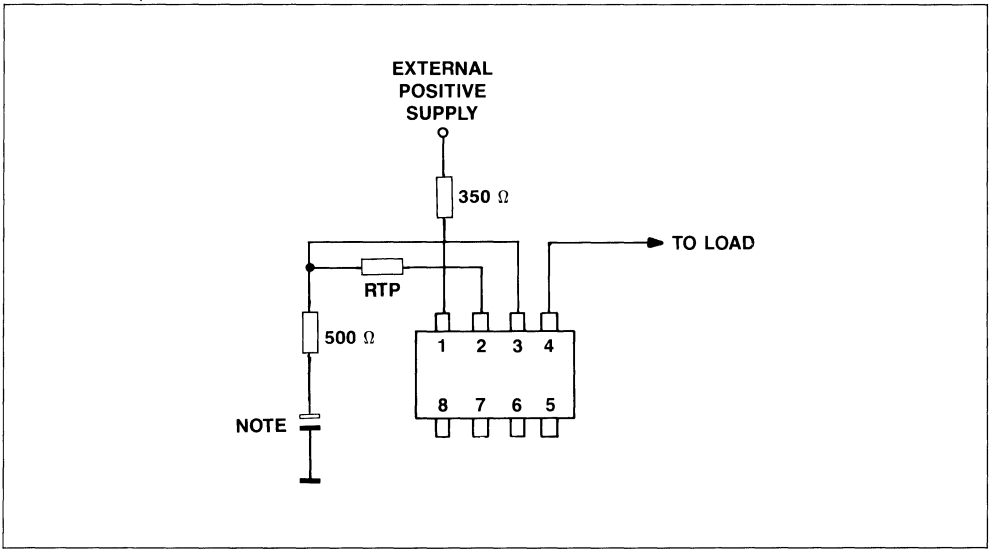


Fig. 18 - LB1011 AC Blocking, DC Current Feed Application



Note 1: Value of capacitor selected based on frequency requirements.

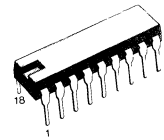
LB1012

PRELIMINARY DATA

AN AT&T PRODUCT

BATTERY FEED

- CAN DRIVE LOOP LENGTHS UP TO 1300 OHMS
- COMMON-MODE REJECTION (LONGITUDINAL BALANCE) BETTER THAN 60 dB.
- LONGITUDINAL BALANCE AND AMPLIFIER GAINS ARE LASER TRIMMED
- TTL COMPATIBLE "HOOK STATUS" INDICATOR
- PROPER LINE MATCHING CAN BE PROVIDED WITH A 50:1 SCALED NETWORK; I.E., 30K OHMS PROVIDES A 600 OHM TERMINATION
- SOON AVAILABLE IN MULTIWATT 15
- 18-PIN PLASTIC POWER DIP

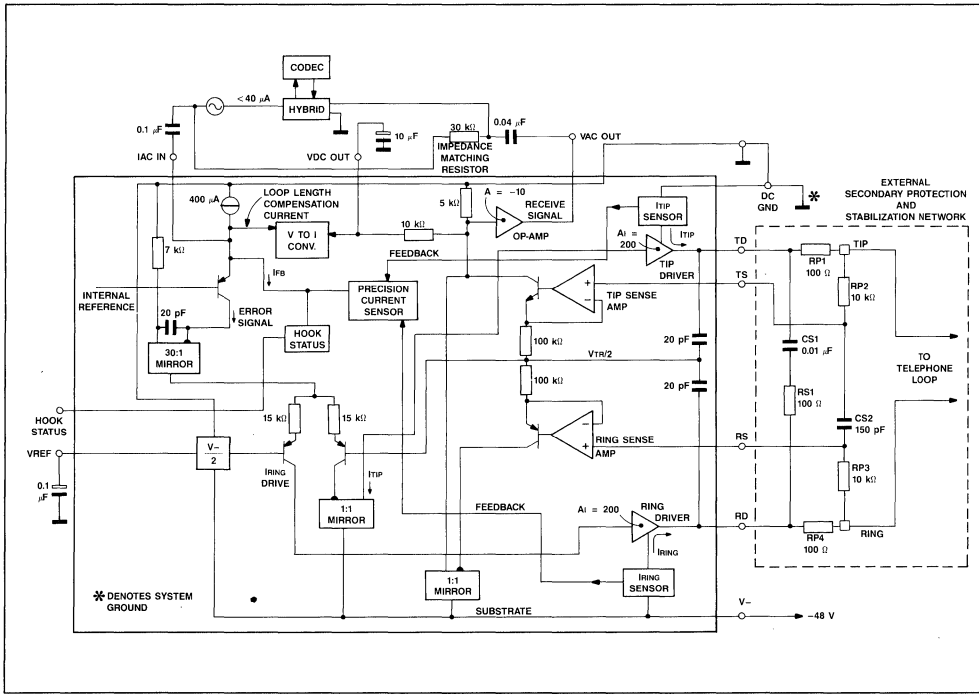


DIP-18 A Plastic

ORDERING NUMBER: LB1012AD

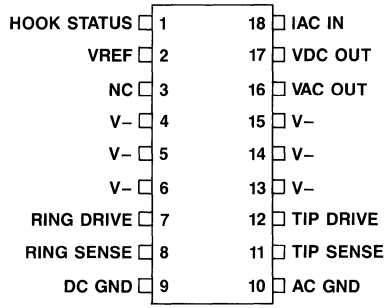
The LB1012 is an electronic battery feed circuit which supplies a controlled DC current to the Tip-Ring pair of a telephone system. The battery feed circuitry presents a low impedance to DC, while presenting a high impedance to AC signals. This device contains input and output ports for voice-frequency signals, and a hook status output signal. The hook status output can be connected to an appropriate LED indicator or to a microprocessor.

Fig. 1 - Functional Diagram



LB1012

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	HOOK STATUS	Hook status output. When DC loop current exceeds 14mA, this terminal sinks 1mA to ground and requires an external 5K pull-up resistor to +5 volts for TTL compatibility. Logic HIGH indicates an "on-hook" condition, while logic LOW indicates an "off-hook" condition.
2	VREF	This pin is an output from an internal reference voltage (approximately one-half of the V– voltage). A by-pass capacitor should be connected from this pin to signal ground to maximize power supply rejection characteristics.
3	NC	No connection. This pin should not be used as an external tie point.
4,5 6,13 14,15	V–	The most negative external supply voltage is connected to these pins. Pins 4, 5 and 6 are physically connected together with a large metal area internal to the package. This same statement is true for pins 13, 14 and 15. All of these pins should be connected to the external V– supply and to a large plated area on its printed circuit board for heat dissipation.
7	RING DRIVE	Output of Ring Drive Amplifier (RD). A protective resistor should go between this pin and the RING side of the active load (see Figure 1).
8	RING SENSE	Input to Ring Sense Amplifier (RS). This pin should be connected through a resistor to the RING side of the active load (see Figure 1). The separation of RING DRIVE and RING SENSE allows the use of a low-cost protective RC network (RP1 thru RP4 in Figure 1).
9	DC GND	High-current DC ground. This is the main source of TIP DC current. This pin connects directly to system ground. This pin is the most positive power supply connection.
10	AC GND	AC (signal) ground. All signal by-pass capacitors and the hybrid/CODEC ground should be connected directly to this pin. This AC GND pin should be connected directly to the DC GND pin.
11	TIP SENSE	Input to Tip Sense Amplifier (TS). This pin should be connected through a resistor to the TIP side of the active load (Figure 1). The separation of TIP DRIVE and TIP SENSE allows the use of a low-cost protective RC network (RP1-RP4 in Figure 1).
12	TIP DRIVE	Output of Tip Drive Amplifier (TD). A protective resistor should go between this pin and the TIP side of the active load (Figure 1).
16	VAC OUT	Low impedance output of op-amp (see Figure 1). A differential Tip-Ring signal input is converted to a single-ended output and is referenced to signal ground. This AC signal is −0.5 times (AC voltage from Tip-to-Ring). The DC bias on this pin is −3 volts. This pin requires a DC blocking capacitor.

PIN DESCRIPTION (Continued)

Pin	Name	Description
17	VDC OUT	This pin is an output from a loop length compensation path. A by-pass capacitor must be connected from this pin to signal ground so that a "DC only signal" is present in the loop length compensation path. The voltage on this pin is directly proportional to loop length (approximately 0.05 of the DC voltage from Tip-to-Ring). This pin could be used to control optional loop length functions.
18	IAC IN	This is the primary AC input signal (very low impedance) from the hybrid. It requires a DC voltage blocking capacitor. The DC bias on this pin is −1.35 volts. The maximum AC signal is 40 μArms. This produces a signal level of approximately +7dBm in a 600 ohm loop, without causing signal clipping. The AC component of Tip-to-Ring signal current is 100 times (IAC IN signal).

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Power Dissipation (see Outline Drawing)*	2.0	W
Voltage (GND to V−)	52	V
Voltage (HOOK STATUS to V−)	57.5	V
Current (TIP DRIVE)	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* Care in mounting and proper environment conditions are required to keep the operating temperature acceptably low. The package of this device has a thermal resistance of approximately 12 C/W to its mounting plane. The remainder of its environment (thermal resistance of wiring board mounting plane to ambient) should not exceed an additional 30 C/W. Forced air circulation over the IC or high thermal conducivity wiring boards may be needed.

Thermal impedance between the package and the connecting mounting path may be minimized by connecting the V− pins to as large a thermal conductive land area as is practical to place on the mounting board. See the V− pin description for additional information.

ELECTRICAL CHARACTERISTICS: (T_A + 25°C unless otherwise specified, default test circuit is in Fig. 2)

Parameter	Test Conditions	Min	Max	Unit
Power Supply Current (OFF-HOOK)	V− = −53 to −60 V (R_{loop} = 275 Ω) (See Fig. 4)	44	49.5	mA
Power Supply Current (ON-HOOK)	Loop = Open Circuit (See Fig. 2)	—	3.5	
Ringing Current Capability	RING Lead Open (See Fig. 4)	100	—	
TIP Current for Power Gate Threshold	(See Fig. 7)	3.0	8.0	
Loop Current for Hook Status Threshold	(Loop = 500 Ω) (See Fig. 8)	10	18	
Loop Current	150Ω (See Fig. 6)	38.3	41.3	
	500Ω (See Fig. 4)	38.5	41.5	
	800Ω (See Fig. 4)	30.5	34.5	
	1.300Ω (See Fig. 4)	19	23	
Transmit Loop Current Gain	IAC IN to TIP-RING (See Fig. 9)	95.5	101	—
Receive Voltage Gain	TIP-RING to VAC OUT (See Fig. 9)	0.476	0.506	
Longitudinal Balance	$I_{COMMON\ MODE}$ <10mA (See Fig. 9)	60	—	dB
Power Supply Rejection	Loop = 400Ω (See Fig. 6)	53	—	
Noise Voltage TIP, RING	Loop = 500Ω (See Fig. 15)	—	8.0	dBmC
IAC IN Input Resistance	(See Fig. 10)	—	100	Ω
VAC OUT Output Resistance	With 2.0 kΩ between VAC OUT & GND (See Fig. 13)	—	50	
Longitudinal Resistance	(See Fig. 14)	50	100	
TIP-RING Shunt Resistance	ΔLoop = 150 − 400Ω (See Fig. 12)	30	—	kΩ
IAC IN-Input Current	Maximum Without Clipping (See Fig. 9)	100	—	μAPP
VAC OUT Output Voltage	(See Fig. 6)	3.0	—	VPP

TEST SPECIFICATION

Symbol	Parameter	Test Conditions V_S = 53V unless otherwise stated	Min	Max	Unit
ΔV_{BG}	Tip-Ring Voltage Balance	Measure $V_{B\text{-}G}$ at R_{load} = 400Ω and R_{load} = 275Ω. Let ΔV_{BG} = the difference of these two readings (See Fig. 3)	—	±75	mV
I_{PS}	Power Supply Current	Measure current in VS power supply lead R_{loop} = 275Ω (See Fig. 4)	−43	−49.5	mA
I_{PS}	60 V Power Supply Current	Measure current in VS power supply lead R_{loop} = 275Ω VS = 60V (See Fig. 4)	−43	−49.5	
I_{PS}	On-Hook Poewr Supply Current	Measure current in VS power supply lead (See Fig. 2)	−0.2	−3.5	

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions $V_S = 53V$ unless otherwise stated	Min	Max	Unit
V_{BG}	$\frac{V_{TIP} + V_{RING}}{2}$	$R_{loop} = 400\Omega$ (See Fig. 3)	−26.2	−28.3	
V_{CM}	$V_{COMMON\text{-}MODE}$	$R_{loop} = 400\Omega$ (See Fig. 3)	−26.2	−28.3	V
ΔV	Longitudinal Loop Error	$R_{LOOP} = 400\Omega$ (See Fig. 3)	—	±1.0	
$V_{A,g}$	Input Voltage	Open VS power supply lead (See Fig. 5)	390	470	mV
$V_{A,g}$	Bandgap Voltage	$R_{load} = 150\Omega$ $V_{CM} = 26.5V$ (See Fig. 5)	−1.2	−1.48	
$V_{T\text{-}R}$	Tip-Ring Voltage	$R_{load} = 150\Omega$ $V_{CM} = 26.5V$ (See Fig. 6)	5.75	6.2	
$V_{16,G}$	VAC Out DC Level	$V_{CM} = -26.5V$ $R_{load} = 150\Omega$ (See Fig. 6)	−2	−4	
$V_{16,G}$	VAC Out DC Level	$V_{CM} = -26.5V$ $R_{load} = 500\Omega$ (See Fig. 6)	−2	−4	
ΔV	VAC Out DC Shift	$V_{CM} = -26.5V$, $R_{LOAD} = 500\Omega$ (See Fig. 6)	—	±0.4	V
$V_{16,G}$	$V_{AG,GND}$ Power Gate OFF	$I_{TIP} = 3mA$ (See Fig. 7)	0	−1	
$V_{16,G}$	$V_{AC,\ GND}$ Power Gate ON	$I_{TIP} = 8mA$ (See Fig. 7)	—	−5	
V_{HS}	Hook Status OFF Voltage	Set I_{ADJ} so that $I_L = 11mA$ (See Fig. 8)	4	5	
V_{HS}	Hook Status ON Voltage	Set I_{ADJ} so that $I_L = 19mA$ (See Fig. 8)	—	±0.2	
A_I	Current Gain, $I_{AC\ (IN)}$ to I_{loop}	Measure $V_{T\text{-}R}$ at $I_A = +0.05mA$, $-0.05mA$ $A_I = \frac{\Delta V_{T\text{-}R}/500\Omega}{0.1mA}$ (See Fig. 9)	95.5	101	dB
A_V	Voltage gain, $V_{T\text{-}R}$ to V_{AC}	Measure $V_{T\text{-}R}$ and V_{AC} at $I_A = +0.05mA$ and at $I_A = -0.05mA$. $A_V = \Delta V_{AC}/\Delta V_{T\text{-}R}$ (See Fig. 9)	0.476	0.505	—
$\Delta V_{T\text{-}R}$	Longitudinal Balance	Measure $V_{T\text{-}R}$ at $I_D = +10mA$, $I_D = -10mA$ (See Fig. 9)	—	±25	mV
I_{loop}	Loop Current	$R_{loop} = 500\Omega$ (See Fig. 4)	38.5	41.5	
I_{loop}	Loop Current	$R_{loop} = 800\Omega$ (See Fig. 4)	30.5	34.5	mA
I_{loop}	Loop Current	$R_{loop} = 1300\Omega$ (See Fig. 4)	19	23	
ΔV	I_{AC} Input Resistance	Measure V_{AC} at $I_{AC} = -50\mu A$, $+50\mu A$ and compute difference (See Fig. 10)	—	±10	mV
$V_{T\text{-}G}$	Tip-Ring Current Capability	$I_{TIP} = 100mA$ for 0.5 seconds minimum (See Fig. 11)	−12	−25	V
$\Delta V_{T\text{-}G}$	Tip-Ring Voltage Change	$V_{CM} = 26.5V$ Measure $V_{T\text{-}G}$ at 150Ω and at 400Ω and calculate difference (See Fig. 12)	—	±20	mV
R_{AC}	AC Out Source Resistance	Measure V_{AC} at R_{VAC} open and at $R_{VAC} = 2000\Omega$. Then: $R_{AC} = \frac{2000(V[open] - V[2000])}{V[2000]}$ (See Fig. 13)	—	50	Ω
$\Delta V_{T\text{-}G}$	Power Supply Rejection	$R_{load} = 400\Omega$. Measure $V_{T\text{-}G}$ at $V_S = -53V$, $V_{CM} = -26.5V$ and at $V_S = -45V$, $V_{CM} = -22.5V$ (See Fig. 6)	—	±20	mV
$\Delta V_{T\text{-}G}$	Longitudinal Resistance	Measure $V_{T\text{-}G}$ at $I_D = +10mA$ and at $I_D = -10mA$, and calculate difference (See Fig. 14)	−1	−2	V
Noise	Short Loop Noise	$R_{load} = 500\Omega$ (See Fig. 15)	—	8	dBrnc
Noise	Long Loop Noise	$R_{load} = 1000\Omega$ (See Fig. 15)	—	25.0	

TEST CIRCUITS

Fig. 2 - Basic Test Circuit

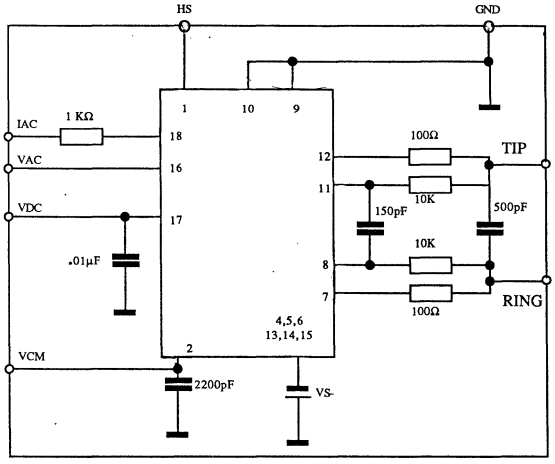


Fig. 3

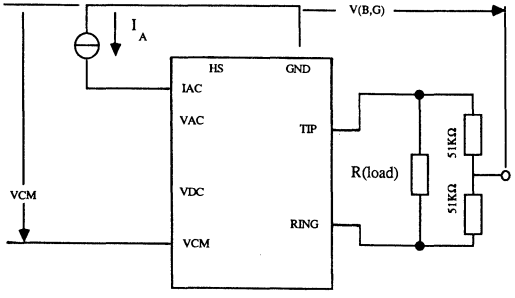
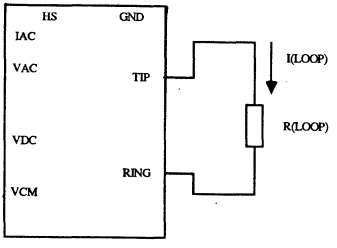


Fig. 4



TEST CIRCUITS (Continued)

Fig. 5

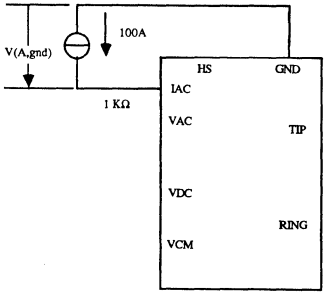


Fig. 6

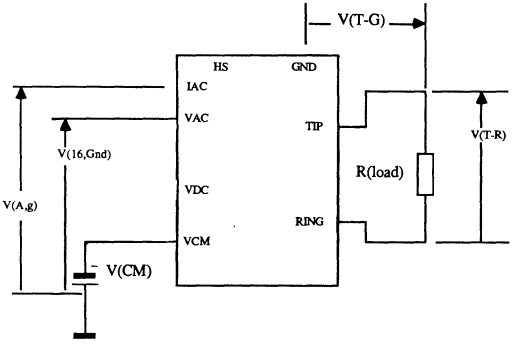


Fig. 7

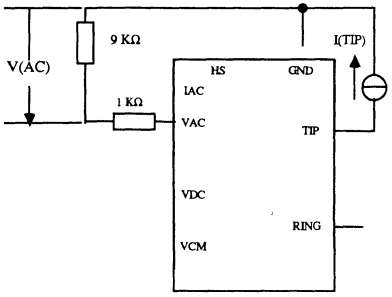
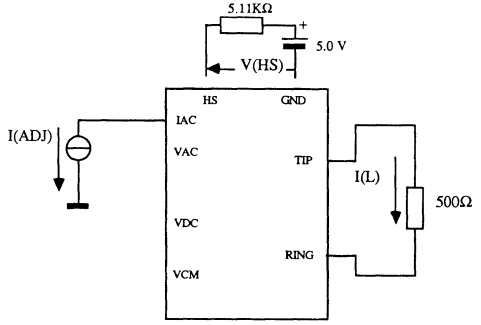
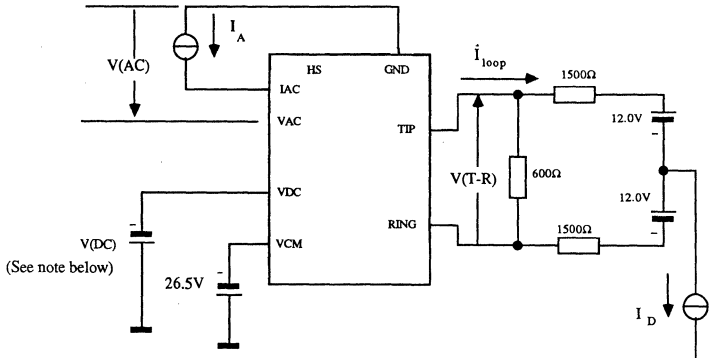


Fig. 8



TEST CIRCUITS (Continued)

Fig. 9



Note: With VDC open, set I(A)=0 and measure the voltage at VDC. Set V(DC) to this value

Fig. 10

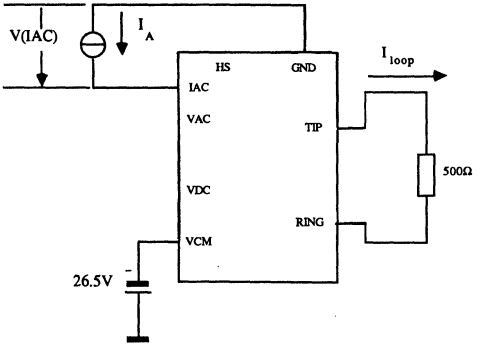
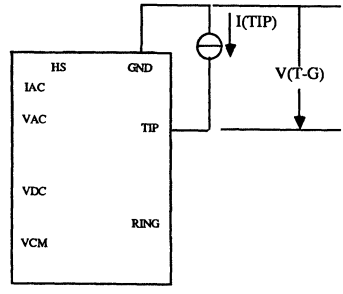


Fig. 11



TEST CIRCUITS (Continued)

Fig. 12

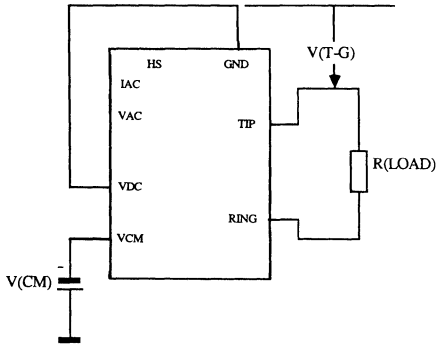


Fig. 13

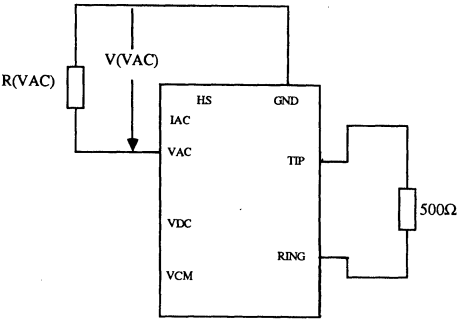


Fig. 14

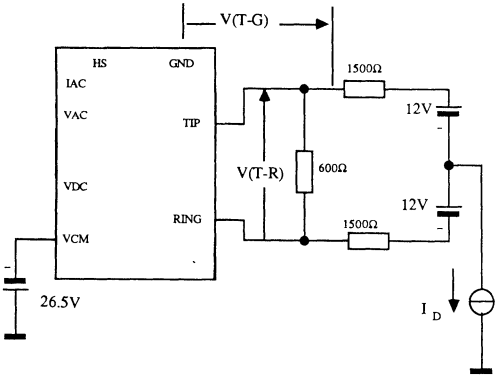
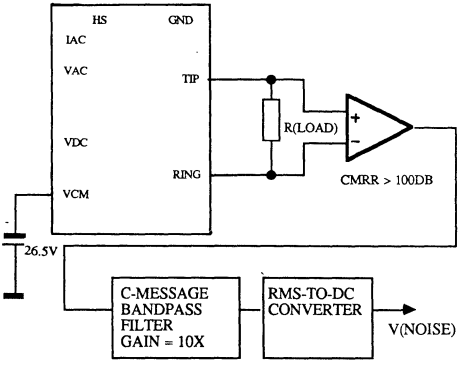


Fig. 15



CHARACTERISTIC CURVES

Fig. 16 - Typical Loop Current versus Loop Resistance

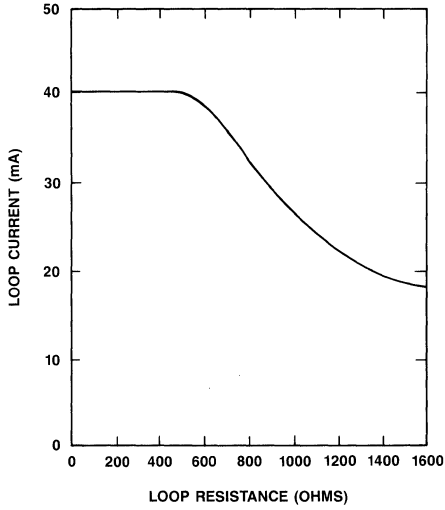
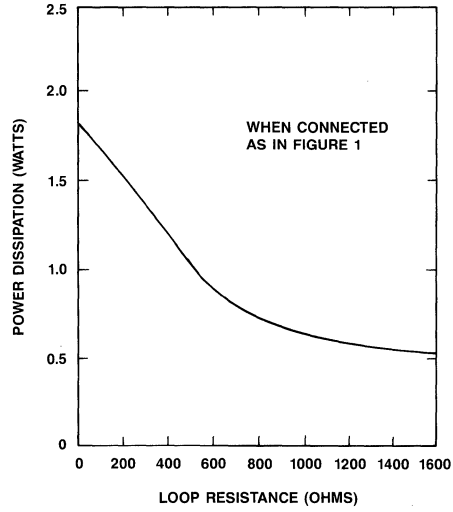


Fig. 17 - Typical Power Dissipations versus Loop Resistance



FUNCTIONAL DESCRIPTION

(see Figures 1, 18 and Note 1):

The LB1012 Battery Feed device supplies a controlled DC current from its own external V– power supply to a customer loop Tip-Ring pair (40 mA on loops up to approximately 600 ohms, decreasing to approximately 21 mA for 1300 ohm loops). Two precisely trimmed audio interface ports are provide: IAC IN, with a current gain of 100 to the Tip-Ring pair and the "TIP SENSE-to-RING SENSE" input with a voltage gain of –0.50 to VAC OUT. These gains make it possible to control the loop termination with impedances scaled 50-to-1 (i.e., 30K ohms connected between VAC OUT and IAC IN looks like 600 ohms across Tip-to-Ring) as shown in Figure 18. A common-mode cancellation feature provides 75 ohms loading for common-mode Tip-Ring currents, with peak values less than the loop currents.

The LB1012 features very good "common-mode to differential" signal rejection (and vice versa), high Tip-to-Ring termination impedance and good power supply noise rejection. Internal thermal shutdown circuitry protects against overload currents. An ON-CHIP over temperature protection circuit temporarily shunts down circuit operation at a case temperature of 112°C.

Lightning surge protection is acheived with esternal diodes and resistors (see Applications). The power gating circuitry is designed to minimize "on-hook" current down. The TIP-DRIVE output provides "ringing Current" capability when the RING DRIVE output is opencircuited. Both TIP DRIVE and RING DRIVE are clamped to their respective power supplies while "on-hook".

The LB1012 is designed for use with supply voltages of +5 volts, ground and a negative voltage supply (V–). The device is tested at V– values between –52 and –60 volts, can work at voltages as low as –30 volts (provided the loop resistance is low enough to prevent signals clipping).

Note 1:

Common-mode signals are frequently referred to as "longitudinal" in the telephone industry. Likewise, differential voltages are frequently referred to as "metallic" voltages.

APPLICATION:

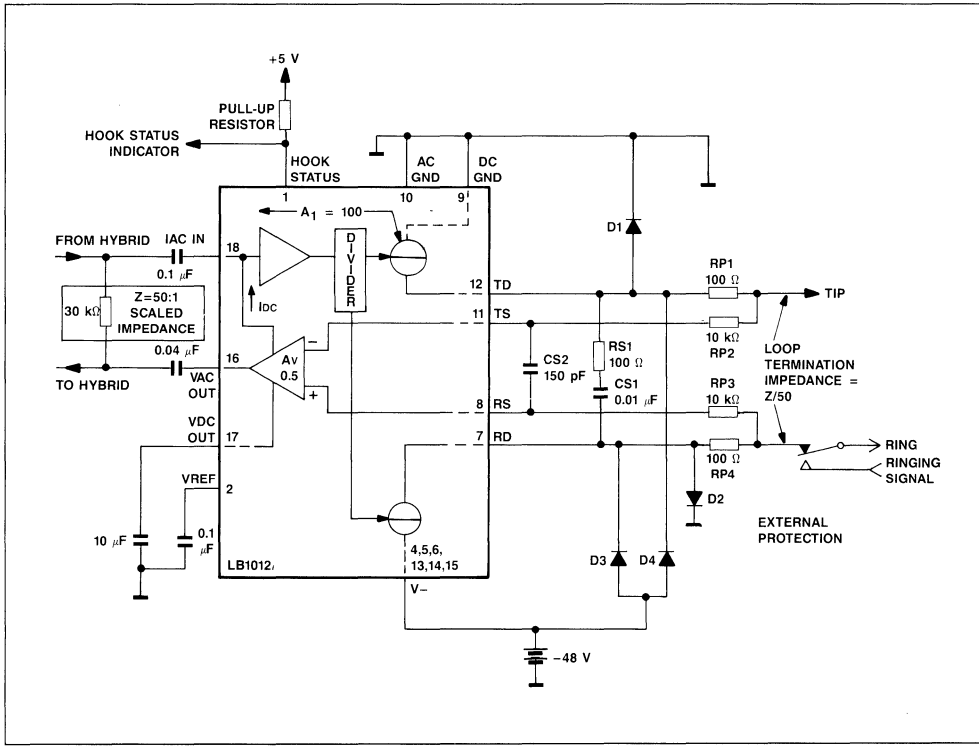
Each LB1012 Battery Feed integrated circuit feeds an individual customer loop. It moderates the flow of DC current from its external V– power supply to the loop system. Simultaneous to supplying the DC current, it serves as a signal path between the hybrid (input/output in Central Office) and the customer loop system (input/output to a telephone set). The LB1012 must respond to "ringing signals" and to "off-hook" conditions. Moreover, since the battery feed circuit must work in a potentially harsh environment (due to power line crossing and lightning surges), there must be some protective provisions for the possibility of overvoltage.

Figure 18 shows a method for correctly connecting the LB1012 device to the Tip and Ring connections of a telephone loop system. Careful grounding procedures will assure good common-mode and power supply noise rejection characteristics. The AC GND pin should be connected directly to the DC GND pin, while all by-pass capacitors should be connected directly to signal ground (AC GND).

A R-C network (RS1 and RS2) should be placed between TIP DRIVE ad RING DRIVE, while a capacitor (CS2) should be placed between TIP SENSE and RING SENSE. This assures stable operation under widely varying load conditions.

An external network of 4 resistors (RP1 through RP4) and 4 surge protection diodes (D1 through D4) are required to protect the LB1012 device against electrical transients, including lightning surges. The 4 diodes connected between Tip, Ring, system ground and V– must be able to withstand secondary lightning surges (15 amps peak, 10μsec risetime, 1000 μsec decay to half-peak amplitude). The resistor on the HOOK STATUS pin and the capacitors on IAC IN, VAC OUT and VREF have already been discussed under Pin Description.

Fig. 18 - LB1012 Battery Feed Application Diagram



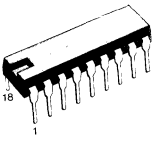
LB1013

PRELIMINARY DATA

AN AT&T PRODUCT

85V DUAL OP-AMP

- OPERATES FROM 5 TO 85V
- BIAS IS SET EXTERNALLY
- AUDIO BAND OPERATION; TYPICAL ft = 2 MHz gain = 60 db at 3 kHz
- HANDLES OUTPUT CURRENT OF UP TO 40 mA
- DUAL OR SINGLE POWER SUPPLY OPERATION

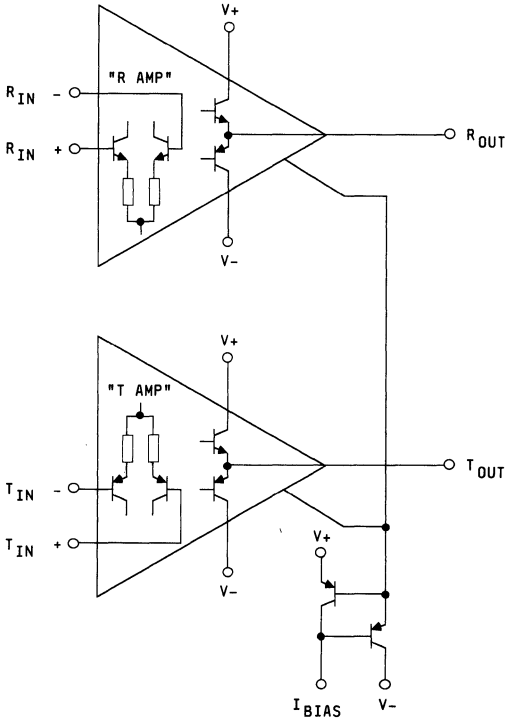


DIP-18 A Plastic

ORDERING NUMBER: LB1013AD

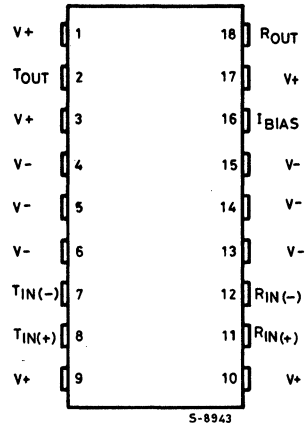
The LB1013 HIGH-VOLTAGE OP-AMP operates off of a single power supply from 5 to 85 volts. The amplifiers are internally compensated and are designed to operate in the audio band. This device is powered up with a 40 μA current supplied to the IBIAS pin.

Fig. 1 - High Voltage Dual Op-Amp Diagram



LB1013

PIN CONFIGURATION



PIN DESCRIPTION

Name	Description
V+ V−	There are two basic supply-voltage pins, V+ and V− (although either of these pins can be connected to ground). The more positive supply-voltage is connected to the five pins designated as V+. The more negative supply-voltage is connected to six pins designated as V−.
$R_{IN}(+)$ $R_{in}(-)$	These pins are the non-inverting and the inverting inputs respectively for the "R" Amplifier.
$T_{IN}(+)$ $T_{IN}(-)$	These pins are the non-inverting and the inverting inputs respectively for the "T" Amplifier.
R_{OUT} T_{OUT}	These pins are the Op-Amp outputs for the "R" Amplifier and the "T" Amplifier respectively.
IBIAS	A current source or suitable value resistor to V− can be connected to this pin. A negative current flow must be present before the device becomes operational.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	−20 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering Time = 15 sec.)	300	°C
Power Dissipation (see note under Outline Drawing)	2	W
Voltage (V+ to V−)	85	V

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($T_A = 25$ C, $V+ = 25V$, $V- = 25V$, IBIAS connects through 1.25MΩ to $V-$ unless otherwise specified)

Parameter	Test Condition		Min.	Typ.	Max.	Unit
Open Loop Gain	f = 100 Hz		75	—	—	dB
	f = 1 KHz		55	—	—	dB
Input Offset Voltage			—	—	±5.0	mV
Input Current (Inverting and Non-Inverting Pins)			—	—	±1.0	μA
Input Offset Current			—	—	±1.0	μA
Common Mode Rejection Ratio	$V- = -30V$, $V_{CM} = \pm 20V$		80	—	—	dB
Output Voltage Swing ("T" Amplifier)	$V+ = 38V$; $V- = -38V$ Non-Inverting Input = GND; $R_L = 1k\Omega$ ΔV (Inverting Input = ±0.5V) V_{HIGH} V_{LOW}		 —	 —	 36.8 34.6	V
Output Voltage Swing ("R" Amplifier)	$V+ = 38V$; $V- = -38V$ Non-Inverting Input = GND; $R_L = 1k\Omega$ ΔV (Inverting Input = ±0.5V) V_{HIGH} V_{LOW}		 —	 —	 36.0 34.6	V
Power Supply Currents (Amplifiers activated under no-load conditions)	Test Circuit (See Figure 2) $V+ = 42.5V$; $V- = -42.5V$ I_{V+} I_{V-}		 —	 —	 1.1 −1.1	mA
Power Supply Leakage Current (Amplifier Off)	Test Circuit (See Figure 2) $V+ = 35V$; $V- = -35V$; IBIAS = (open) I_{V+} I_{V-}		 —	 —	 ±10 ±10	μA
Output Leakage Currents (Amplifier Off)	Test Circuit (See Figure 3) $V+ = 35V$; $V- = -35V$ IBIAS = (open) $V_{LOAD} = +30V$ $V_{LOAD} = -30V$		 —	 —	 ±10 ±10	μA
T_{OUT} to $V+$ Fault Current	Test Circuit (See Figure 4) $V+ = 35V$; $V- = -35V$; t = 100ms	$V_{LOAD} = +35V$	41	—	47	mA
T_{OUT} to $V-$ Fault Current		$V_{LOAD} = -35V$	−41	—	−47	
R_{OUT} to $V+$ Fault Current		$V_{LOAD} = +35V$	41	—	47	
R_{OUT} to $V-$ Fault Current		$V_{LOAD} = -35V$	−41	—	−47	

Fig. 2 - Power Supply Current, Test Circuit
(For This test, connect both op-amps as shown above)

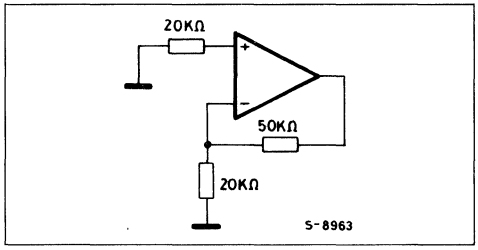


Fig. 3 - Output Leakage Current, Test Circuit
(The current through this 10 K resistor is the "Leakage Current")

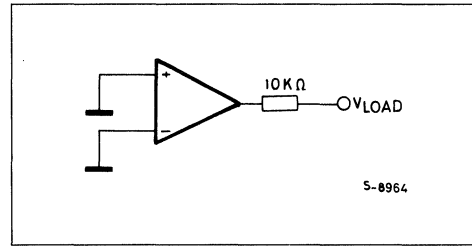
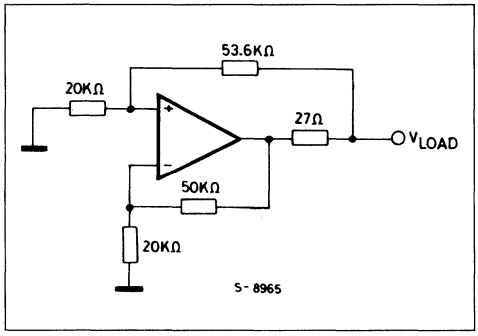


Fig. 4 - Fault Current Test Circuit



APPLICATION

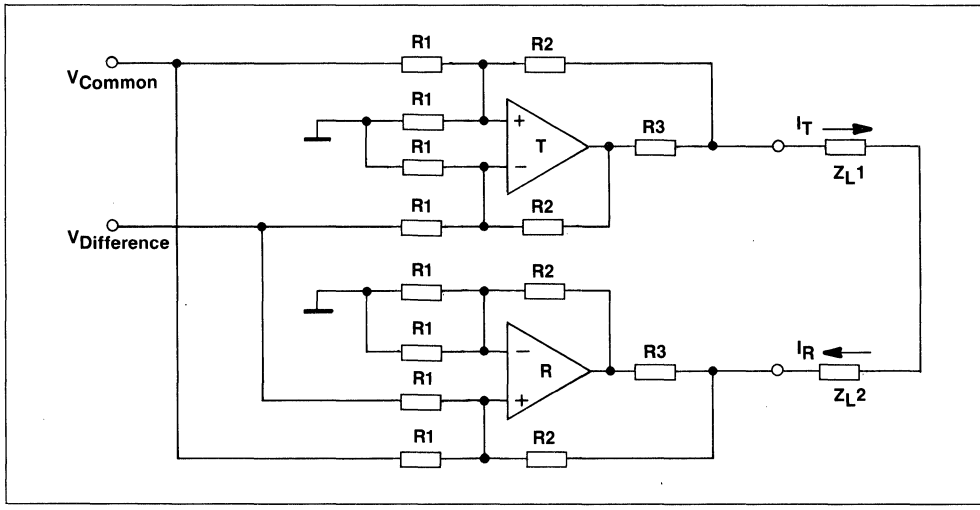
The simplified schermatic shown below illustrates an application as a transconductance amplifier for telephone line drive applications. Other applications include high voltage/power voltage followers, audio amplifiers and circuits where high-voltage, high-power op-amp capability are required.
The equations relating to the circuit shown below are as follows:

For R1 & R2 > > R3

$$I_T = \frac{V_C - V_D}{R1} \cdot \frac{R2}{R3}$$

$$I_R = -\frac{V_C + V_D}{R1} \cdot \frac{R2}{R3}$$

Fig. 5 - Simplified Line Feed Operation



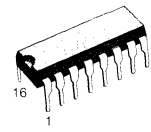
LB1017

PRELIMINARY DATA

AN AT&T PRODUCT

HIGH-SPEED DUAL ANALOG SWITCH

- LOW "ON" RESISTANCE (9 TO 15 OHMS) FOR SIGNAL UP TO ±4V AND 100kHz
- CHARACTERIZED FOR THE AUDIO RANGE; CAPABLE OF HANDLING SMALL-SIGNAL ANALOG INPUTS TO THE MHz RANGE
- SWITCHING TIME <50 NSEC
- ±4V COMMON-MODE RANGE
- LOW INJECTED CHARGE (<50 pC)
- HIGH OPEN-SWITCH ISOLATION (−70 dB) AT 1.0 kHz
- LOW LEAKAGE CURRENT (<100 nA) in "OFF" STATE
- LOW CROSS-TALK (−50 dB) BETWEEN SWITCHES
- LOW HARMONIC DISTORSION
- SWITCHES HAVE SINK/SOURCE CURRENT CAPABILITIES GREATER THAN 16 mA.
- LOW FEEDTHROUGH CAPACITANCE (<0.3 pF).

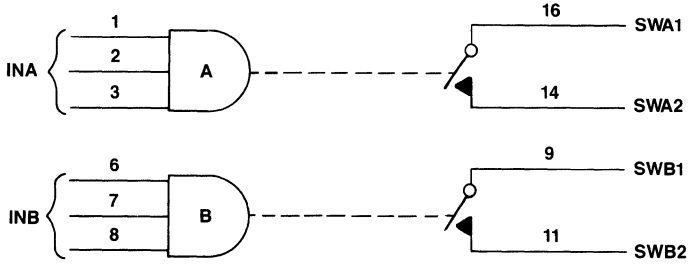


DIP-16 A Plastic

ORDERING NUMBER: LB1017AC

The LB1017 high-speed analog switch contains two channels in one package. Each channel consists of a driver circuit controlling a SPST switch. The drivers interface with TTL logic input signals for applications such as multiplexing, commutating and D/A converter applications. These drivers enable a low-level input (0.8 to 2.0 volts) to control the ON-OFF condition of each switch. In the ON state, each switch will conduct equally well in either direction. In the OFF state, the switch will block voltages up to ±5V. Positive logic "1" will turn each switch ON, and logic "0" will turn it OFF.

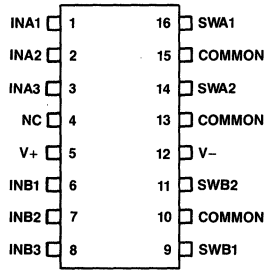
Fig. 1 - Functional Diagram



Logic	Switch
111	ON
000 001 010 011 100 101 110	OFF

LB1017

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1 2 3 6 7 8	INA1 INA2 INA3 INB1 INB2 INB3	TTL compatible logic input pins for switching channels "A" and "B" respectively (see Figure 1). A channel switch is normally closed if all of its inputs are logic HIGH. A logic LOW on any input pin will open the switch.
4	NC	No connection. This pin should not be used as a tie point for external circuitry.
5	V+	Connection for "most positive" external power supply.
9 16	SWB1 SWA1	One side of the switch output (designated as side number 1) for channels "B" and "A" respectively.
10 13 15	COMMON	Ground or circuit common (not necessarily physical or system ground). All of these pins should be externally connected to one common point.
11 14	SWB2 SWA2	One side of the switch output (designated as side number 2) for channels "B" and "A" respectively.
12	V–	Connection for "most negative" external power supply.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Supply Voltage (V+ to COMMON)	9.5	V
Supply Voltage (V− to COMMON)	−9.5	V
Switch Voltages (SWA or SWB to COMMON)	±5.0	V
Input Voltages (INA or INB to COMMON)	±5.5	V

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Each Channel): $T_A = 25°C$, $V+ = 9V$, $V- = -9V$, V_{IN} = Pins 1, 2, 3, 6, 7 and 8

Parameter	Test Conditions	Min	Typ	Max	Unit
Switch ON Resistance	$V_{IN} = 2.4V$, $V_{SW1} = V_{SW2} = 0$, f = 1KHz (See Fig. 3)	9	—	15	Ω
Switch Leakage Current, ON Condition	$V_{IN} = 2.4V$, $V_{SW1} = V_{SW2} = 0$ (See Fig. 4) $V_{IN} = 2.4V$, $V_{SW1} = V_{SW2} = -5V$ $V_{IN} = 2.4V$, $V_{SW1} = V_{SW2} = +5V$	—	—	±1.5	mA
Switch Source Current	$V_{IN} = 2.4V$, $V_{SW1} = 1.5V$, $V_{SW2} = 0$ (See Fig. 5)	−16	—	−30	mA
Switch Sink Current	$V_{IN} = 2.4V$, $V_{SW1} = -1.5V$, $V_{SW2} = 0$ (See Fig. 5)	16	—	30	mA
Logic Input Current "HIGH"	$V_{IN} = 5.5V$ (See Fig. 6)	—	—	1	μA
Logic Input Current "LOW"	$V_{IN} = 0.4V$ (See Fig. 6)	−0.4	—	−1.2	mA
Switch Leakage Current, OFF Condition	$V_{IN} = 0.8V$, $V_{SW1} = +4.5V$, $V_{SW2} = -4.5V$ $V_{IN} = 0.8V$, $V_{SW1} = -4.5V$, $V_{SW2} = +4.5V$ (See Fig. 7)	—	—	±100	nA
Positive Supply Current	Switch in OFF Condition (See Fig. 8)	—	7.7	13	mA
Negative Supply Current	Switch in OFF Condition (See Fig. 8)	—	−3	−10	mA
Positive Power Supply Rejection Ratio	(See Fig. 9)	38	—	—	dB
Negative Power Supply Rejection Ratio	(See Fig. 10)	38	—	—	dB
Switch OFF Isolation	$V_{IN} = 0.4V$; (See Fig. 11)	−70	—	—	dB
Crosstalk Between Switches	$V_{IN} = 2.4V$; (See Fig. 12)	−50	—	—	dB
Second Harmonic Distorsion	$V_{IN} = 2.4V$; $V_{SOURCE} = 250mVrms$ at 1KHz; (See Fig. 13 and Note 2)	—	—	250	μVrms
Third Harmonic Distorsion	$V_{IN} = 2.4V$; $V_{SOURCE} = 250mVrms$ at 1KHz; (See Fig. 13 and Note 3)	—	—	140	μVrms
Switch Offset Voltage, No load (See Note 3)	V_{IN} (Pins 2, 7, 1 and 8) = 2.4V V_{IN} (Pins 3 and 6) = Pulsed (See Note 4) $V_{SET} = -5V$ $V_{SET} = 0$ $V_{SET} = +5V$ (See Fig. 14)	— — —	— — —	±25 ±25 ±25	mV mV mV
Switch Offset Voltage, 400Ω load (See Note 1)	V_{IN} (Pins 2, 7, 1 and 8) = 2.4V V_{IN} (Pins 3 and 6) = Pulsed (See Note 4) $V_{SET} = -5V$ $V_{SET} = +5V$ (See Fig. 16)	— —	+165 +165	±300 ±300	mV mV

Note 1: The "Switch Offset Voltage" is defined as the difference in voltage ($\Delta V = V_{GEN} - V_{OUT}$) during the last 200 nanonseconds of the positive portion of the pulse described in Note 4.

Note 2: Second harmonic distorsion is defined as the amplitude of a 2KHz signal at V_{OUT} ($V_{SOURCE} = 250mVrms$ at 1KHz)

Note 3: Third harmonic distorsion is defined as the amplitude of a 3KHz signal at V_{OUT} ($V_{SOURCE} = 250mVrms$ at 1KHz)

SWITCHING CHARACTERISTICS (Each Channel): $T_A = 25°C$, $V+ = 9V$, $V- = -9V$, V_{IN} = Pins 1, 2, 3, 6, 7 and 8

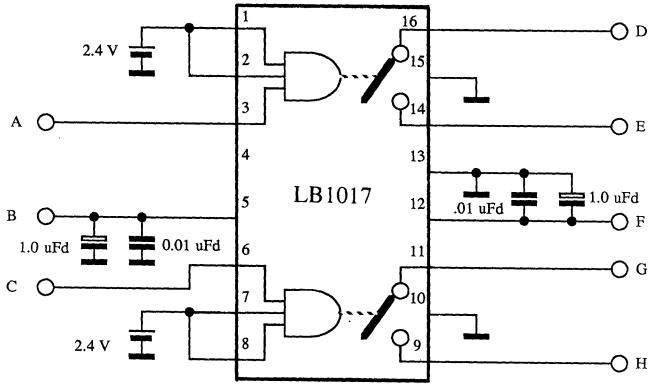
Parameter	Test Conditions	Min	Typ	Max	Unit
Turn-on Time	V_{IN} (Pins 2, 7, 1, and 8) = 2.4V V_{IN} (Pins 3 and 6) = Pulsed (see Note 4) $R_{LOAD} = 400\Omega$				
	$V_{SET} = -5V$	20	—	50	ns
	$V_{SET} = +5V$ (See Fig. 16, 17)	20	—	50	
Turn-Off Time	V_{IN} (Pins 2, 7, 1 and 8) = 2.4V V_{IN} (Pins 3 and 6) = Pulsed (see Note 4) $R_{LOAD} = 400\Omega$				
	$V_{SET} = -5V$	10	—	40	ns
	$V_{SET} = -5V$ (See Fig. 16, 17)	10	—	40	
Injected Charge (see Note 5)	$V_{IN} = 2.4V$				
	$V_{SW1} = -4.5V$	—	±50	±5	pC
	$V_{SW1} = 0$	—	±5	±50	
	$V_{SW1} = +4.5V$ (See Fig. 15)	—	±5	±50	

Note 4: Positive pulses with a 400 nsec width and a 2.5 volta amplitude are applied a repetition rate of 60 μsec. Rise and fall times of this applied pulse are ≤ 5 nsec.

Note 5: Injected charge is defined as the amount of excess charge transferred to a 1000pF load capacitor (connected to the SW2 side of each channel switch) during the time interval associated with the turn-off of the switch.

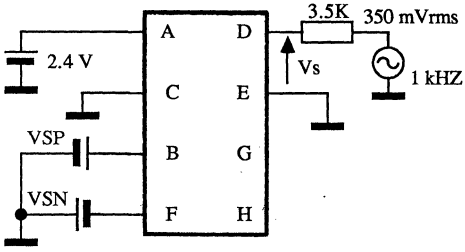
TEST CIRCUITS

Fig. 2



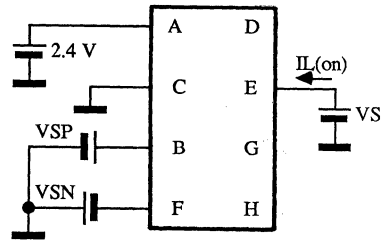
TEST CIRCUITS (Continued)

Fig. 3



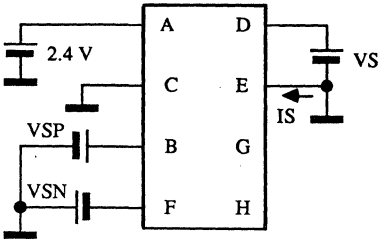
Resistance = Vs/0.001

Fig. 4



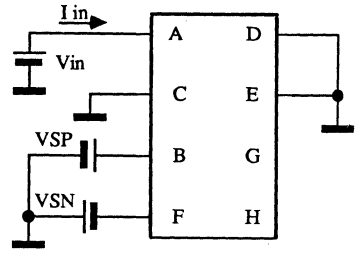
Switch leakage current (on)

Fig. 5



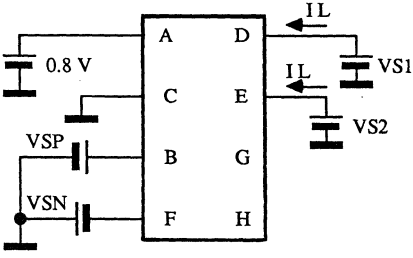
Source/Sink current

Fig. 6



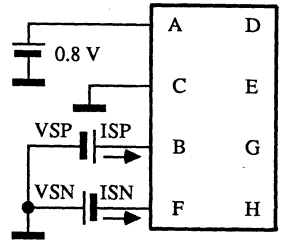
Logic input current

Fig. 7



Switch leakage (off)

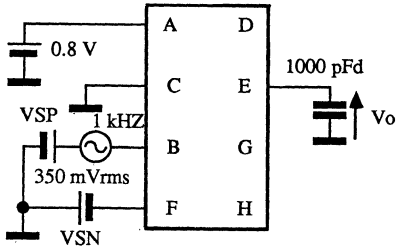
Fig. 8



Power supply current

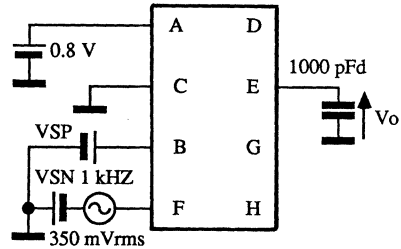
TEST CIRCUITS (Continued)

Fig. 9



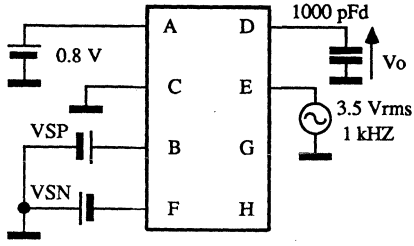
PSRR = 20 log(0.35/Vo)

Fig. 10



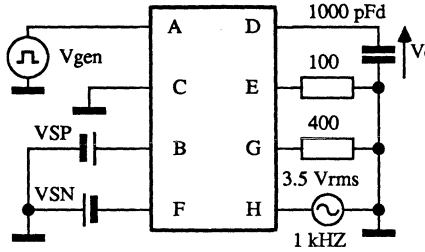
PSRR = 20 log(0.35/Vo)

Fig. 11



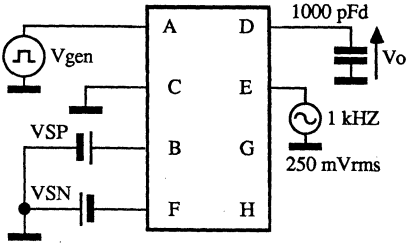
Voltage feedthrough

Fig. 12



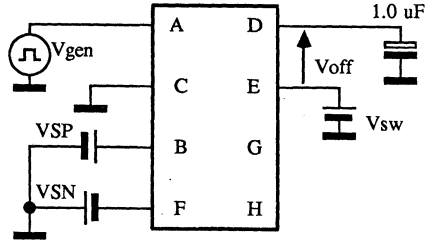
Crosstalk = 20 log(Vo/3.5)

Fig. 13



Harmonic distortion

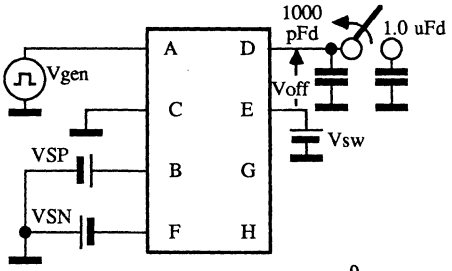
Fig. 14



Offset voltage

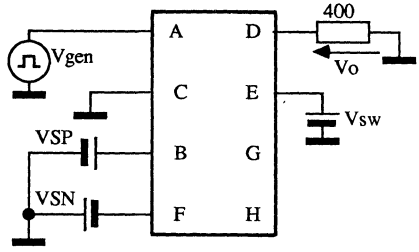
TEST CIRCUITS (Continued)

Fig. 15



Injected charge = ΔVoff x 10 $^{-9}$ pC

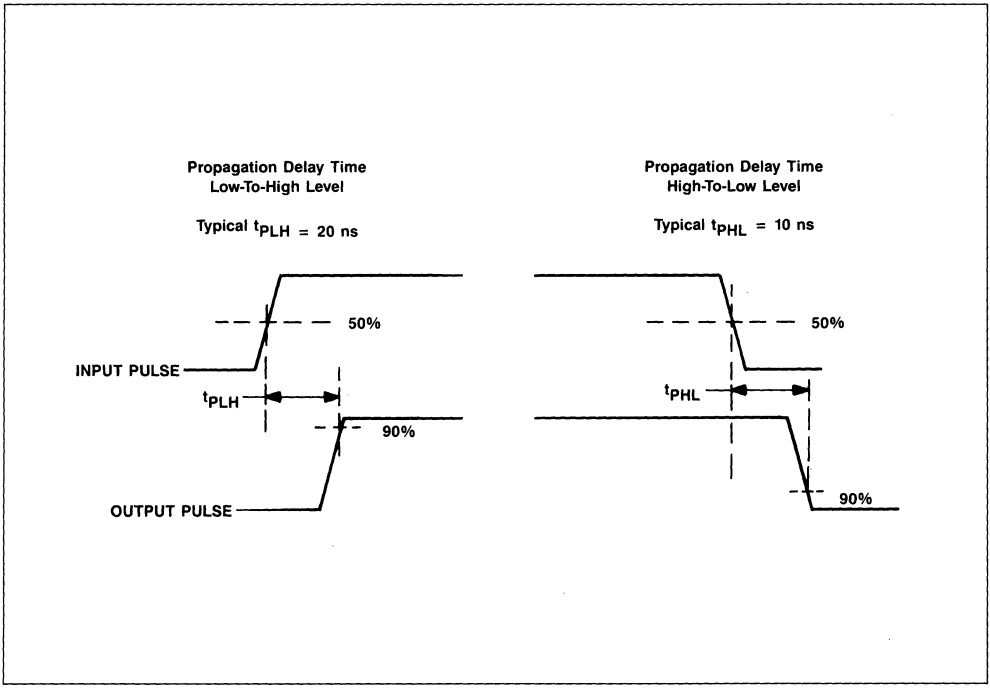
Fig. 16



Turn on / Turn off time

CHARACTERISTIC CURVES

Fig. 17



CHARACTERISTIC CURVES (Continued)

Fig. 18 - Typical Offset Voltage vs Common Mode Voltage

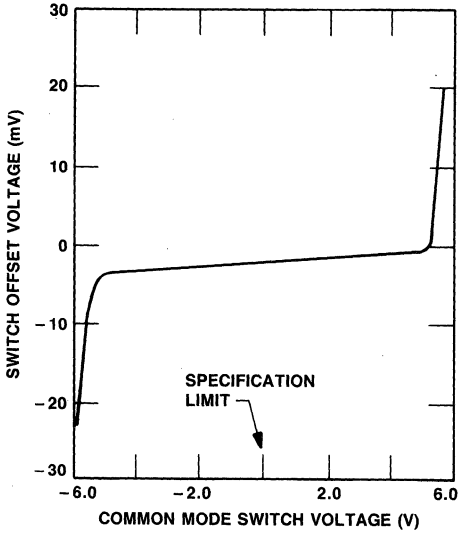


Fig. 19 - Typical leakage Current vs Common Mode Voltage

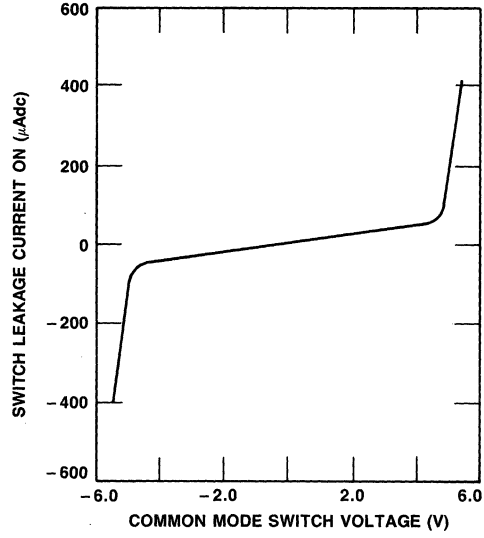


Fig. 20 - Typical Injected Charge vs Common Mode Voltage

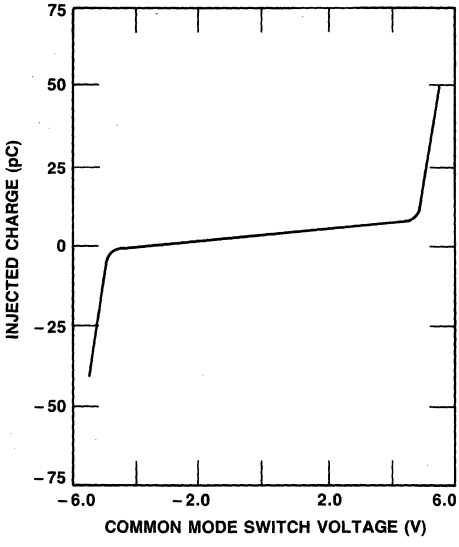
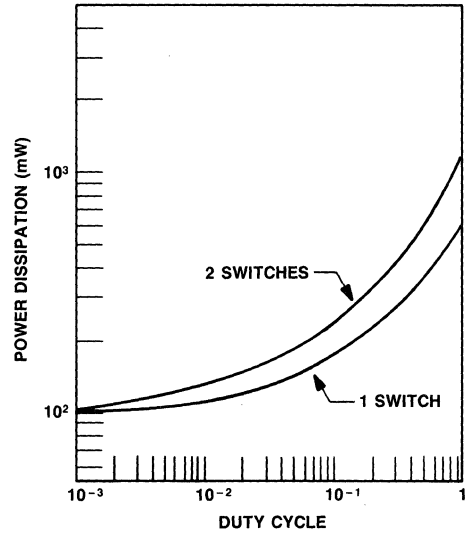


Fig. 21 - Typical Power Dissipation vs Duty Cycle



CHARACTERISTIC CURVES (Continued)

Fig. 22 - Typical Power Supply Ripple Rejection vs Temperature

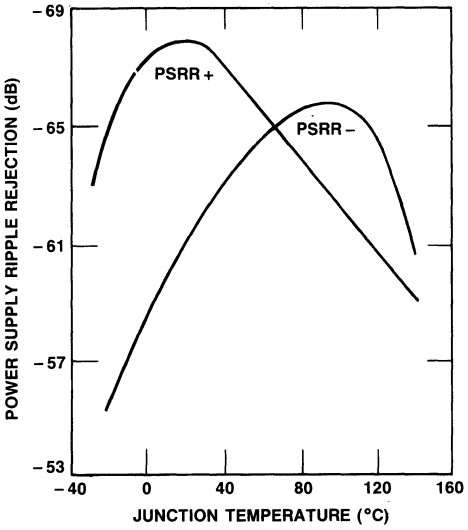


Fig. 23 - Typical Power Supply Current vs Temperature

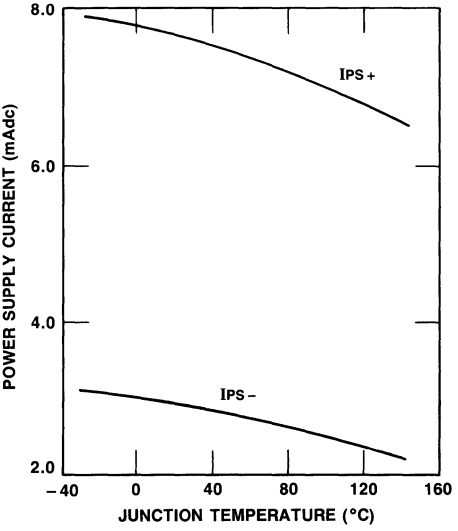


Fig. 24 - Typical Input Logic Current "Low" vs Temperature

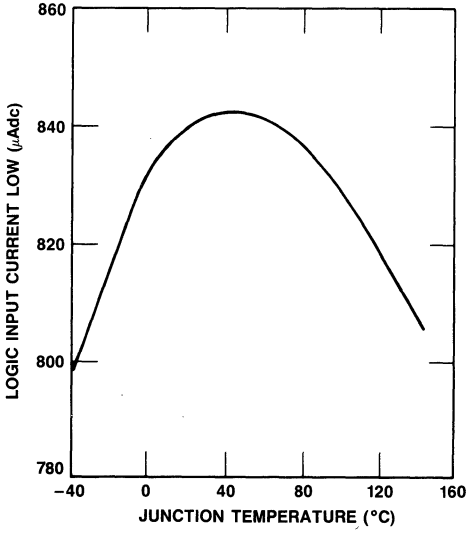
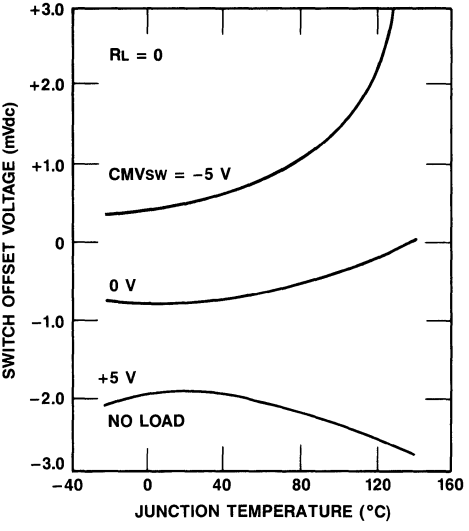


Fig. 25 - Typical Switch Offset Voltage vs Temperature



CHARACTERISTIC CURVES (Continued)

Fig. 26 - Typical Switch Offset Voltage vs Temperature

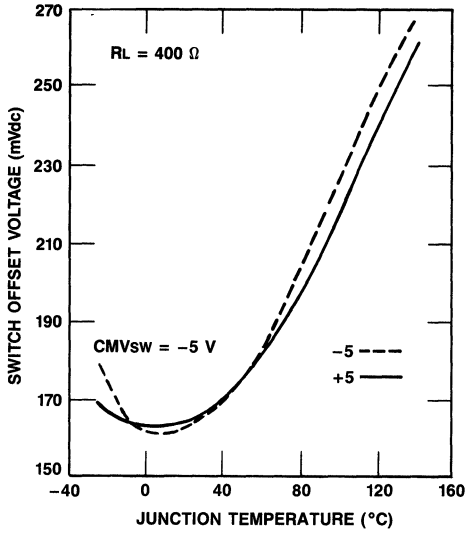


Fig. 27 - Typical Switch Leakage Current "ON" vs Temperature

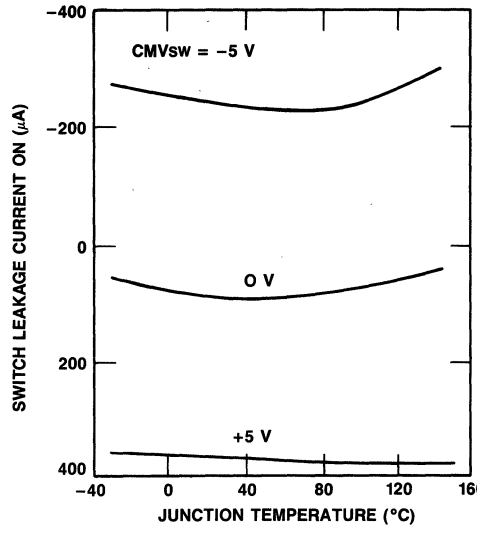


Fig. 28 - Typical Injected Charge vs Temperature

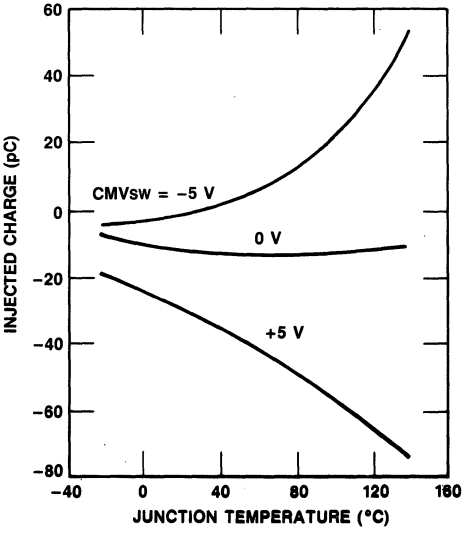
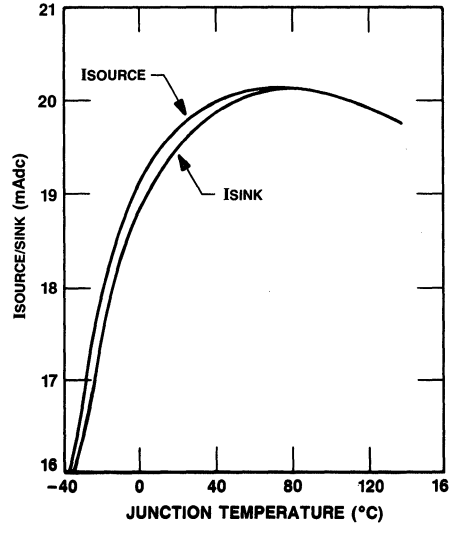
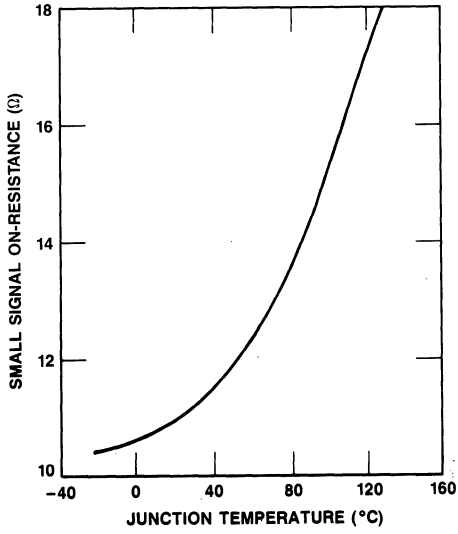


Fig. 29 - Typical Source and Sink Current vs Temperature



CHARACTERISTIC CURVES (Continued)

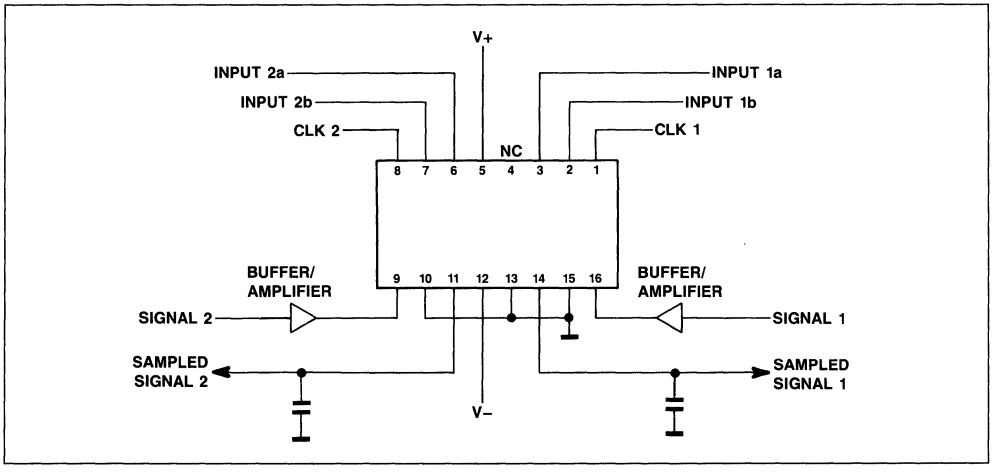
Fig. 30 - Typical On-Resistance vs Temperature



APPLICATION

The LB1017 is a High-Speed Dual Analog Switch with low "ON" resistances and control inputs which are TTL compatible.
Figure 21 shows a diagram of the LB1017 as used in a sampling application. The design of this device incorporates high-speed current amplifiers. Therefore, it is important that proper high-frequency bypassing of power supplies is used, and that proper grounding designs are incorporated.

Fig. 31 - LB1017 High-Speed Dual Analog Switch Sampling Application

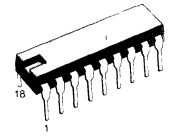


LB1018

PRELIMINARY DATA
AN AT&T PRODUCT

4 x 8 PNPN CROSSPOINT ARRAY

- JUNCTION-ISOLATED FOR LOW COST
- LOW ON STATE RESISTANCE (< 13 Ω)
- HIGH OFF STATE RESISTANCE (> 200 MΩ)
- 40mA DC CURRENT CAPABILITY
- 30 VOLT OFF-STATE CAPABILITY
- EXCELLENT TRANSIENT IMMUNITY (> 300V/μS)
- LOW SIGNAL LOSS TO SUBSTRATE (> − 48dB)

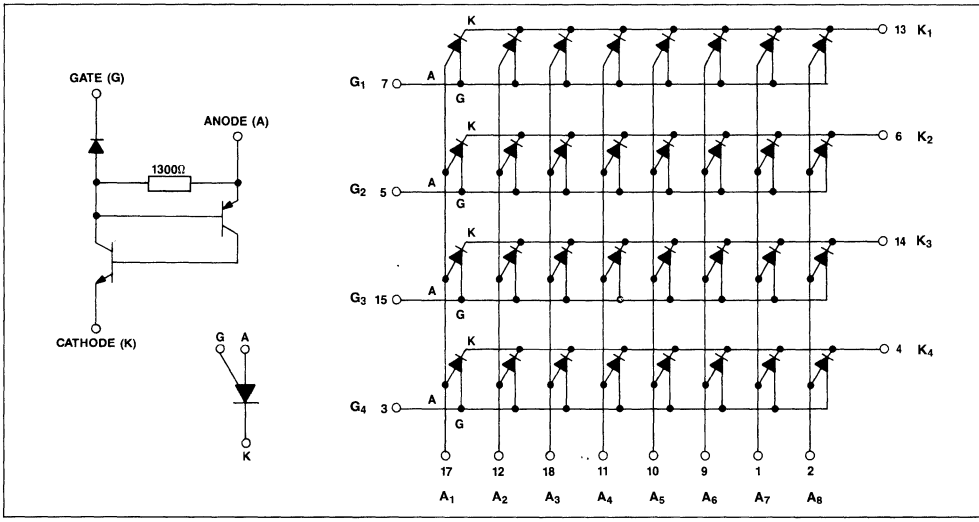


DIP-18 A Plastic

ORDERING NUMBER: LB1018AD

The LB1018 Crosspoint Array integrated circuit is a high density, high performance, bipolar switch. It is organized as a 4 x 8 array with crosspoints consisting of 32 SCR devices. Each crosspoint is a nearly ideal switch, capable of switching analog signals with an intersection impedance of less than 13 ohms. It is useful as a high reliability replacement for metallic relays in switching networks.

Fig. 1 - Schematic Diagram

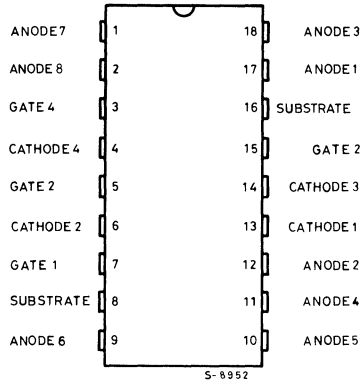


ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	− 0 to 70	°C
Storage Temperature Range	− 40 to + 125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Voltage (Anode to Cathode)	± 30	V
Voltage (Cathode to Substrate)	30	V
Voltage (Anode to Substrate)	30	V

LB1018

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS ($T_A = -40$ to $+70°C$)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{AK}	Forward Voltage	$I_{AK} = 10mA$	(See Fig. 2)	0.7	0.9	1.1	V
$\frac{dis}{diak}$	Substrate Crosstalk	$I_{AK} = 10mA$ $I_{AK} = 10mApp$ $V_{AS} = 20V$	(See Fig. 2)	—	—	4	$\frac{\mu A}{mA}$
R_{ON}	On Resistance	$I_{AK} = 10mA$	(See Fig. 2)	5.4	—	13.4	Ω
I_{LKS}	Cathode-Substrate Leakage Current	$V_{KS} = 30V$	(See Fig. 3)	—	0.22	10	μA
I_{EN}	Enable Current		(See Fig. 4)	0.2	—	1.0	mA
V_{EN}	Enable Voltage		(See Fig. 4)	−0.8	—	−1.7	V
I_{LAK}	Forward Leakage Current	$V_{AK} = 30V$	(See Fig. 5)	—	0.004	1.0	μA
I_{LKA}	Reverse Leakage Current	$V_{KA} = 30V$	(See Fig. 5)	—	0.012	1.0	
I_{LGA}	Gate-Anode Leakage Current	$V_{GA} = 30V$	(See Fig. 6)	—	—	1.0	
I_{HOLD}	Holding Current		(See Fig. 7)	0.3	—	1.8	mA
dV/dt	Transient Immunity	0-30V Ramp		—	300	—	V/μs
V_{STEP}	Step Voltage Immunity			—	5.0	—	V
C_{AK}	Anode Line to Cathode Line Capacitance	$V_{AK} = 30V$		—	1.0	2.0	pF

TEST CIRCUITS

Fig. 2

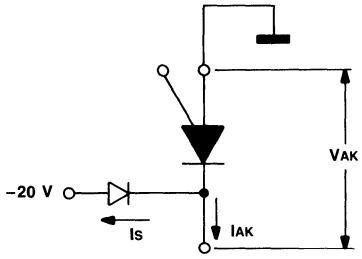


Fig. 3

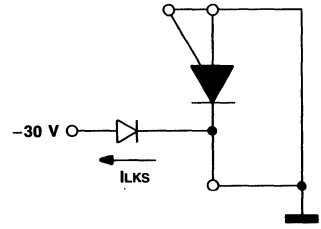


Fig. 4

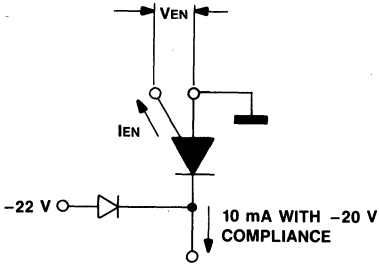


Fig. 5

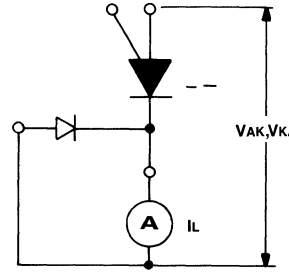
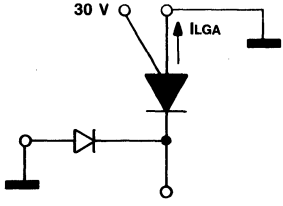


Fig. 6



CHARACTERISTIC CURVES

Fig. 7

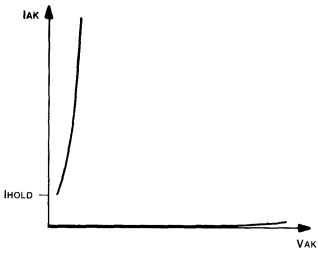


Fig. 8

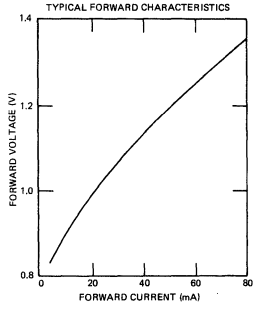


Fig. 9

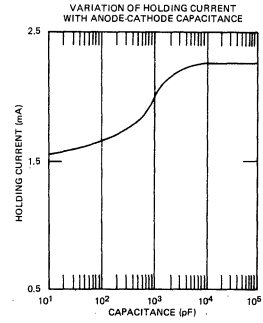


Fig. 10

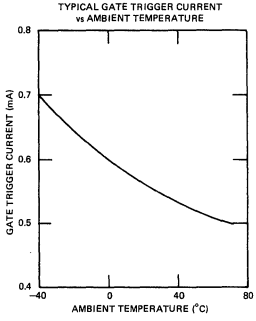


Fig. 11

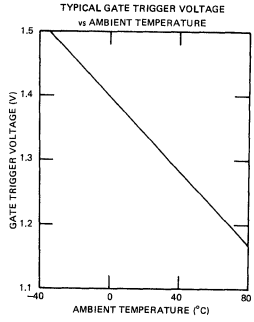


Fig. 12

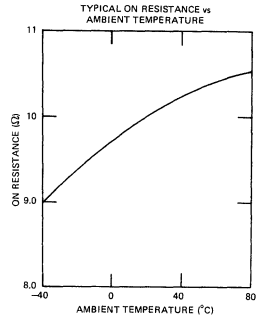


Fig. 13

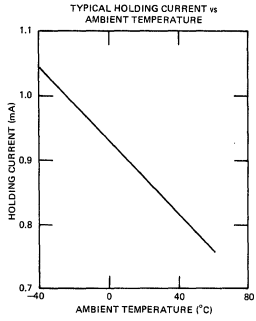


Fig. 14

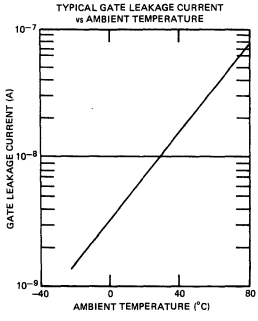
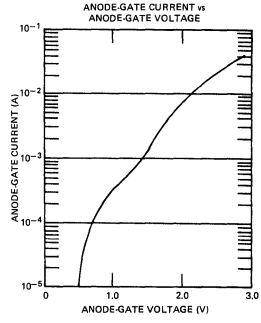


Fig. 15



CHARACTERISTIC CURVES (Continued)

Fig. 16

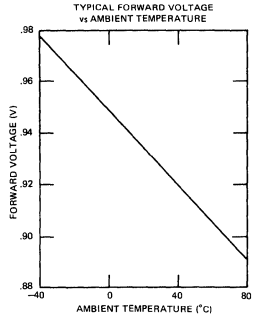


Fig. 17

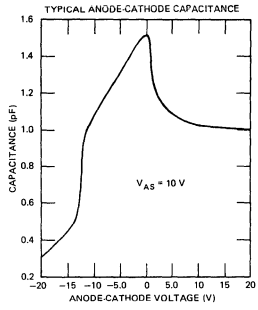


Fig. 18

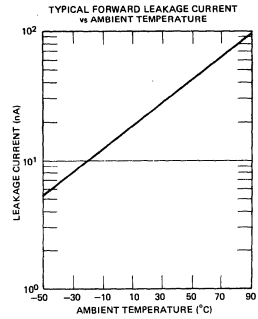


Fig. 19

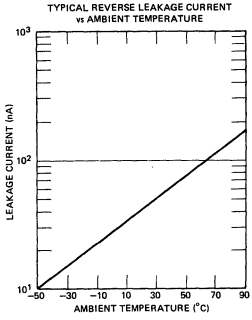
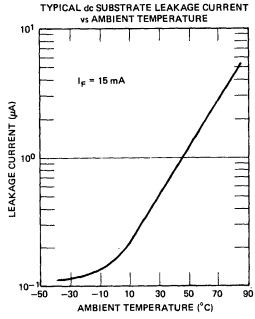


Fig. 20



APPLICATION

The LB1018 Crosspoint Array is designed to provide a low-loss analog switching element for telephony signals.

Applications indicate that the minimum holding current is a function of the anode cathode capacitance placed in parallel with a PNPN element. The form of the variation is shown in Figure 3. When the device is placed in a circuit where active inductance is present, the holding current may be depressed slightly. The values of holding current given in the electrical characteristics table correspond to measurements made with very small anode/cathode capacitance, such as when the device is connected to a curve tracer with short wires.

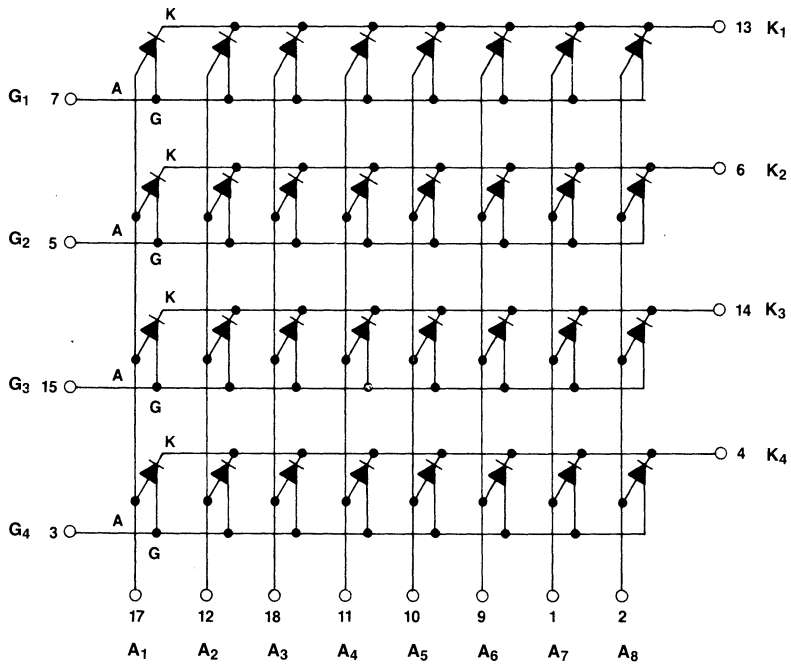
The "ON" resistance of PNPN elements vary for different paths through the matrix. A total variation of ±1 ohm may occur around the mean value.

The forward and reverse leakages given in the electrical characteristics are measured from anode to cathode with the substrate held at the same potential as the cathode. Leakage to the substrate (via all the other parts of the device not under tests) will be diverted into the voltage source controlling the substrate potential. If the substrate is allowed to float, the leakage is collected by the cathode of the PNPN element under test. Thus, the leakage measured at the one cathode is greatly increased (typically to 350 nanoamps at room temperature).

The LB1018 is designed to conduct continuous forward current up to 42 mAdc provided that the junction temperature is not greater than 120 C. However, it is also designed to be able to survive infrequent fault conditions where up to 100 mAdc flows for intervals up to 1 hour. Typical devices have been observed to be destroyed by forward current surges of 750 mA.

APPLICATION (Continued)

Fig. 21 - Crosspoint Array Schematic



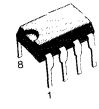
LB1019

PRELIMINARY DATA

AN AT&T PRODUCT

POWER CONTROLLER

- DIGITALLY CONTROLLED POWER SWITCH
- CONTROLS −48V POWER TO TELEPHONE SETS OR OTHER LOADS
- POWER CAN BE TURNED ON AND OFF USING $\overline{ON}$ INPUT
- CURRENT LIMITING DURING A FAULT CONDITION
- THERMAL SHUTDOWN DURING EXTENDED FAULT CONDITIONS
- ISOLATION OF THE LOAD FROM THE POWER SUPPLY UNTIL THE POWER SUPPLY'S MAGNITUDE EXCEEDS −33 VOLTS (TYPICALLY)
- INTERRUPTION OF POWER TO THE LOAD WHEN THE POWER SUPPLY'S MAGNITUDE FALLS BELOW −30.5V (TYPICALLY)
- INDICATES AN OVERCURRENT CONDITION WHEN THE LOAD CURRENT EXCEEDS 300mA (TYPICALLY)
- INQUIRE ABOUT AVAILABILITY OF DEVICES WITH 200, 450, 600 mA (±15%) OF OVERCURRENT THRESHOLD
- INDICATES CURRENT FLOW TO CONFIRM CIRCUIT CONTINUITY
- EO INPUT ALLOWS SMOOTH POWER UP SEQUENCE
- SMALL 8-PIN DUAL-IN-LINE PACKAGE



Minidip-A Plastic

ORDERING NUMBER: LB1019AB

The LB1019 integrated circuit provides control functions and maintenance monitoring for −48-volt power supplied via a single output to a telephone set or other load. It is able to turn the power on and off under manual control, indicate a 300mA overcurrent condition on the circuit, and provide an indication that some current is flowing to confirm circuit continuity. The device includes two safety features: an output current limit to protect against large current surges on a direct short-circuit and thermal shutdown of the chip if an overload persists without being manually turned off.

An "EO" input is provided to allow for smooth power-up sequences. This lead is connected to an RC network (R from +5.0V to EO and C from EO to ground) and holds the circuit in an off state for a predetermined amount of time after the +5.0V is applied.

Power will not be applied to the controlled circuit unless the nominally −48-volt supply is more negative than −33 volts and power will be interrupted to the load when the power supply is more positive than −30.5 volts.

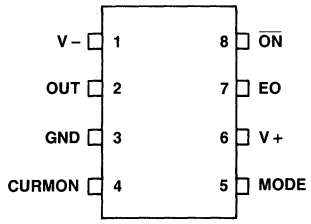
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	−20 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (r = 15 sec.)	300	°C
Power Dissipation (Package Limitation)	1	W
Power Instantaneous ($T \leq 2\mu$sec)	50	W
Operating Voltage V+	+5.5	V
Operating Voltage V−	−54	V

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

LB1019

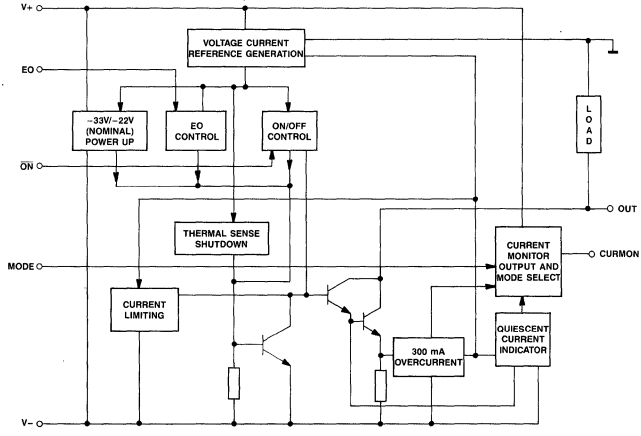
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	V–	Connection for "most negative" external power supply.
2	OUT	The output pin supplies a "controlled" voltage to a telephone set or other types of loads.
3	GND	Ground or circuit common (not necessarily physical or system ground).
4	CURMON	Current monitor. CURMON is a TTL compatible output signal. It indicates whether the output load current is either less than of greather than a predetermined threshold reference level.
5	MODE	Mode is an LSTTL-Compatible input signals (Table 1). A logic HIGH sets the CURMON thresold reference level to a typical level of 300mA. A logic LOW sets the CURMON threshold level to a typical level of 3mA (Table 2).
6	V+	Connection for the "most positive" external power supply.
7	EO	EO is a high impedance input used to force the chip to ignore all other inputs and hold the –48-volt output off until the voltage on EO exceeds 3.0 volts. This input can be used to eliminate logic power-up "sanity" problems by use of an external R-C network, as shown in the Block Diagram (Fig. 1). This input has substantial hysteresis (1.0 ± 0.5 volts) to prevent noise problems since the voltage may ramp up slowly. A diode is included on the chip between EO and +5.0Vdc to insure quick discarge of the capacitor upon power down. The leakage current into or out of EO is tested to be less than 5.0μA under all conditions.
8	$\overline{ON}$	This terminal is an LSTTL compatible input. When held LOW, it turns on power to the –48V load as long as EO is HIGH and LB1019 is not in a thermal overload condition.

Fig. 1 - Functional Diagram



ELECTRICAL CHARACTERISTICS (At 25°C and with V+ = 5.0V, V− = −48V unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{PS}	Power Supply Current	V+ = 5.5V, V− = −48V (See Fig. 4)	—	—	4.4	mA
		V+ = 5.5V, V− = −54V (See Fig. 5)	—	—	2.8	
		V+ = Open, V− = −54V (See Fig. 6)	—	—	3.0	
$V_{\overline{THON}}$	V− Turn-On Thereshold	(See Fig. 7)	−26.0	−33	−37	V
$V_{\overline{THOFF}}$	V− Turn-Off Thereshold	(See Fig. 7)	−27.5	−30.5	−35.2	
V_{DROP}	Output Voltage Drop	I_{OUT} = 300mA (See Fig. 8)	—	—	2.0	
EO_{THON}	EO Turn-On Threshold	(See Fig. 9)	1.5	2.0	2.5	
EO_{THOFF}	EO Turn-Off Threshold	(See Fig. 9)	2.5	3.0	3.5	
I_{THLO}	Low Output Current Threshold	(See Fig. 10)	1.5	3.0	7.0	mA
	Low Output Current Threshold	T_j = 100°C (See Fig. 10)	1.5	—	10	
I_{THHI}	High Output Current Threshold	(See Fig. 10)	258	300	340	
I_{LIM}	Output Current Limit	(See Fig. 11)	0.6	0.8	1.1	A

Table 1 - TTL-Compatible Input/Output Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{IL}	Single LSTTL input: ($\overline{ON}$ & MODE)	V_{IN} = 0.4V, V+ = 5.5V	—	—	−400	μA
I_{IH}		V_{IN} = 2.7V, V+ = 5.5V	—	—	20	
V_{OL}	TTL Output: (CURMON)	I_{OL} = 1mA V+ = 4.5V	—	—	0.45	V
V_{OH}		I_{OH} = −250μA V+ = 4.5V	2.4V	—	—	
V_I	Input Clamp Diode (see EO Pin Description)	I_I = −18mA V+ = 4.5V	—	—	1.5	V

Fig. 2 - Output Characteristics at 25°C

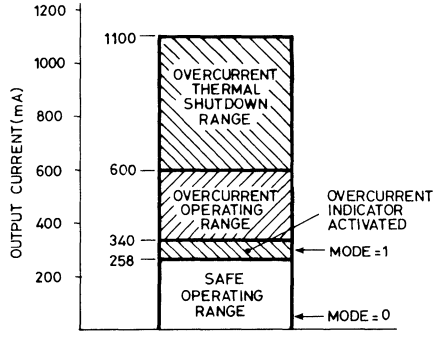


Fig. 3 - Logical Diagram

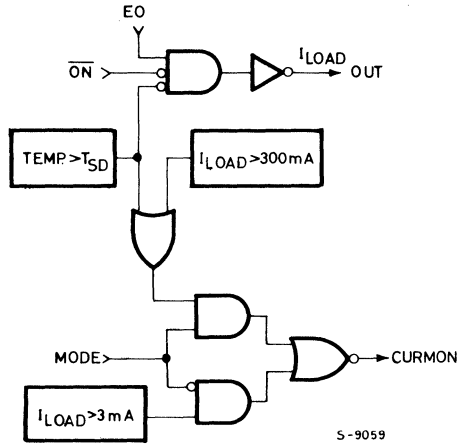


Table 2 - Output Status Logic Table

E_O	$\overline{ON}$	Thermal Shutdown	OUT
0	X	X	OFF
X	X	1	OFF
1	1	0	OFF
1	0	0	ON

Table 3 - Current Monitor Status Logic Table

MODE	I_{LOAD} >3mA	I_{LOAD} >300mA	Thermal Shutdown	CURMON
0	0	X	X	1
0	1	X	X	0
1	X	0	0	1
1	X	X	1	0
1	X	1	0	0

TEST CIRCUITS

Fig. 4 - Power Supply Current

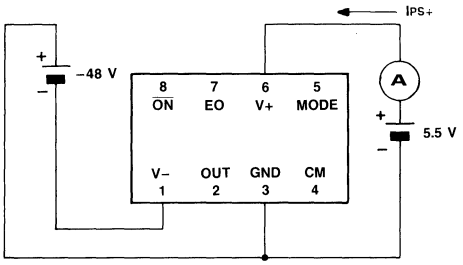


Fig. 5 - Power Supply Current

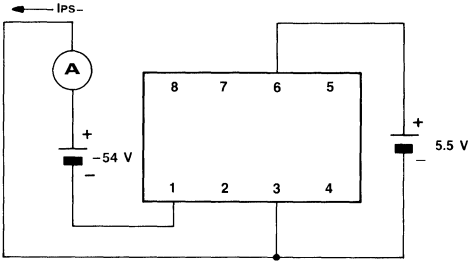


Fig. 6 - Power Supply Current

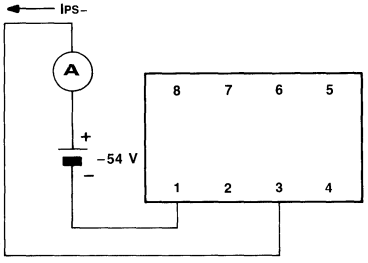


Fig. 8 - Output Voltage Drop (V_{OUT})

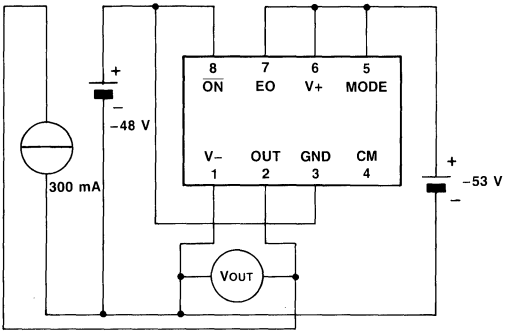
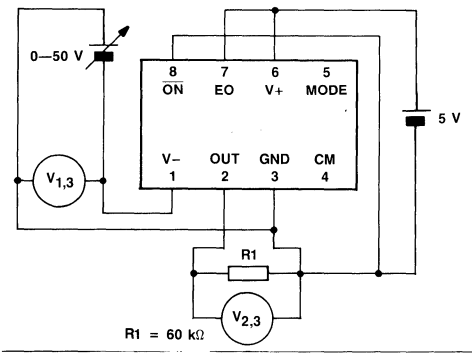
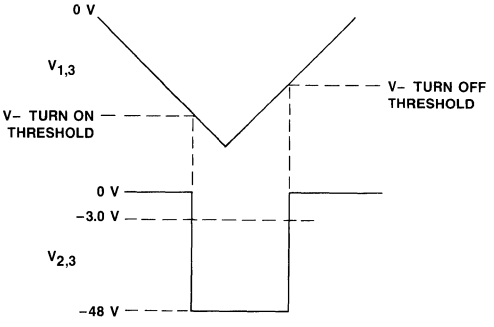


Fig. 7 - V-Turn ON & V-Turn OFF Threshold





TEST CIRCUITS (Continued)

Fig. 9 - EO Turn ON & EO Turn OFF Threshold

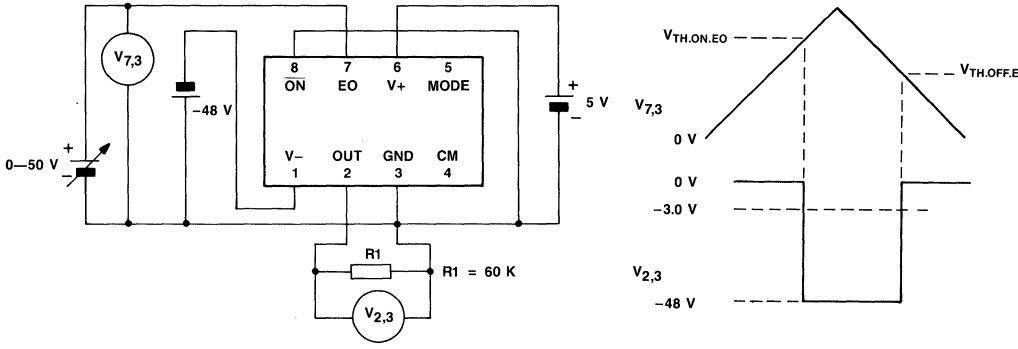


Fig. 10 - Low Output Current Threshold (I_2)

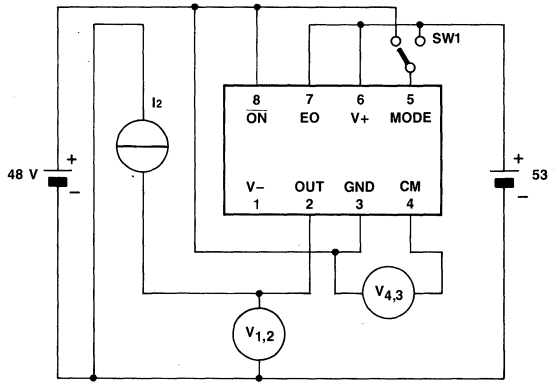
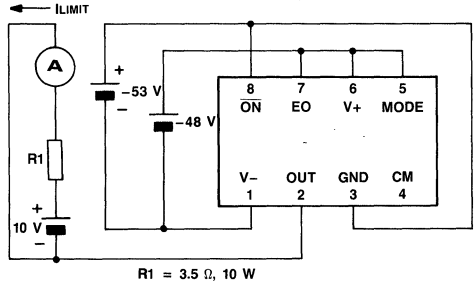


Fig. 11 -Output Current Limit (I_{LIMIT})



APPLICATION

Power will not be applied to the load which is connected to the output of the LB1019 Power Controller unless the V– supply is more negative than a nominal –33 volts. This condition is described as the V– turn-on threshold. Conversely, power will be interrupted to an operating load when the V– supply becomes more positive than a nominal –30.5 volt. This condition is described as the V– Turn-OFF threshold. The LB1019 Power Controller has been designed to operate with a nominal power supply of –48 volts.

Table 4 is a summary of the device operation. Specifically, the device may be interrogated (either with a microprocessor or with manual control) to determine the status of the load connected to the output of the LB1019. Voltage on the EO pin should be greather than +3.5 volts for the interrogation process.

If the LB1019 Power Controller is overloaded for a significant period of time and is in danger of destruction due to thermal runaway, the internal shutdown mechanism will act to protect the device and remove power from the load. An indication of this is that CURMON will be a logic LOW when MODE is a logic HIGH.

If desired, the user can differentiate between an overcurrent indication and thermal shutdown by examining CURMON with MODE being a logic HIGH and $\overline{ON}$ being a logic LOW. Then force $\overline{ON}$ to a logic HIGH and examine CURMON again. If CURMON remains LOW under both conditions, the device is in thermal shutdown and no current is flowing. If the state of CURMON changes under this test, the device was not shutdown, but was in an overcurrent condition.

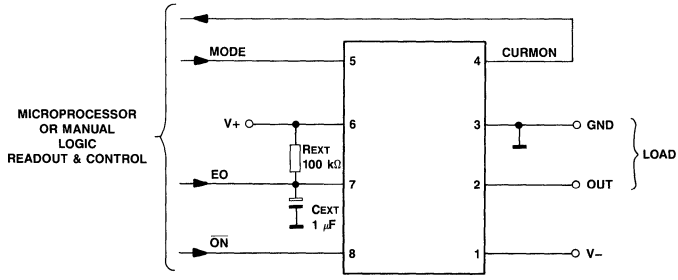
Another special interrogation feature is the quiescent current indicator (MODE is set to zero). This feature indicates that the output of the controller is connected to the load.

Table 4 - Device Operation Summary

EO (in)	$\overline{ON}$ (in)	MODE (in)	CURMON (out)	DEVICE STATE
0	X	X	1	Disabled, output turned OFF
1	1	X	1	Output OFF, device not in thermal Shutdown
1	1	1	0	Output OFF, device in thermal shutdown from previous overload
1	0	0	1	Output ON, connection from controller output to the load is open
1	0	0	0	Output ON, load is connected to the controller output
1	0	1	1	Output ON, current less than overload thereshold
1	0	1	0	Output ON, current greater than overload thereshold, device may be in danger of going into thermal shutdown, or is in thermal shutdown

The application diagram shown in Figure 12 illustrates the connections and external components which are necessary for the basic operation of the LB1019 Power Controller. The RC network (R_{EXT} and C_{EXT}) holds the device in an OFF-state condition for a predetermined amount of time after V+ is applied.

Fig. 12 - Power Controller Application Diagram



LB1020
LB1021

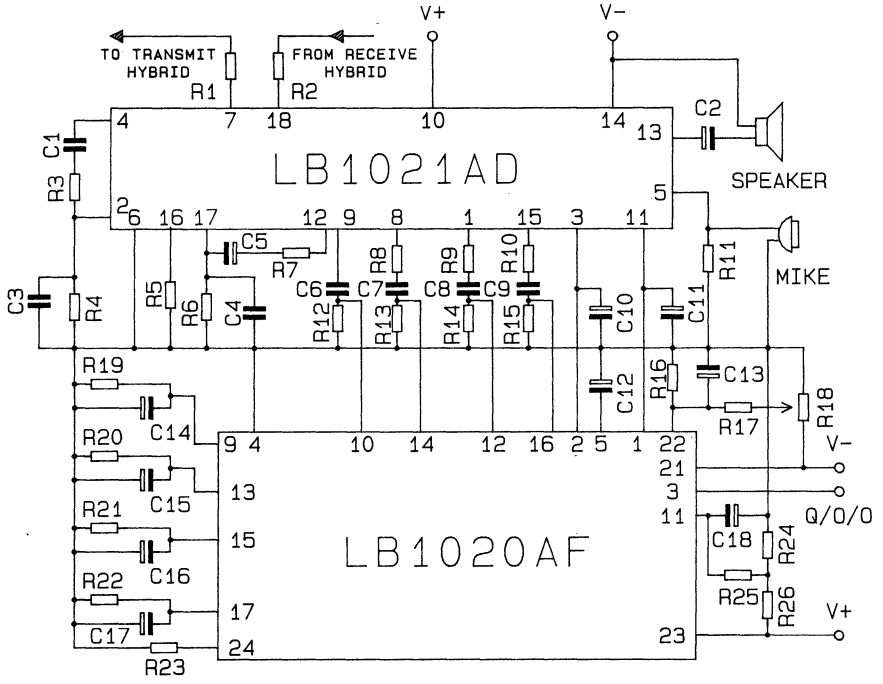
PRELIMINARY DATA

AN AT&T PRODUCT

SPEAKERPHONE KIT LB1020AF VOICE PATH SWITCH AND LB1021AD SPECIAL AMPLIFIER

This kit consists of two integrated circuits which form the basis of a high-performance speakerphone.
The system works in "half-duplex" and is powered from a single 12 V source.
The LB1020 performs the switching function needed for Speakerphone operation by accepting transmit and receive signals as input and providing transmit and receive variolosser control signals as output. Timing of the various switching functions is selectable using external RC components.
The LB1020 also provides a noise guard feature which permits steady background noise to be ignored in making the transmit/receive switching decision.
The LB1021 provides the linear amplification for the speakerphone system, including switchable, controllable gain for the transmit and receive voice paths, speaker and line drive capabilities, and switchguard/talkdown gain. It also provides a stable, low-noise signal reference from the 12 V supply.

Speakerphone Kit application diagram

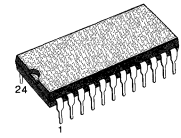


Note: Refer to last page of this data sheet for values of resistences and capacitors

LB1020

VOICE PATH SWITCH FOR SPEAKERPHONE APPLICATIONS (See Application at the end of the chapter)

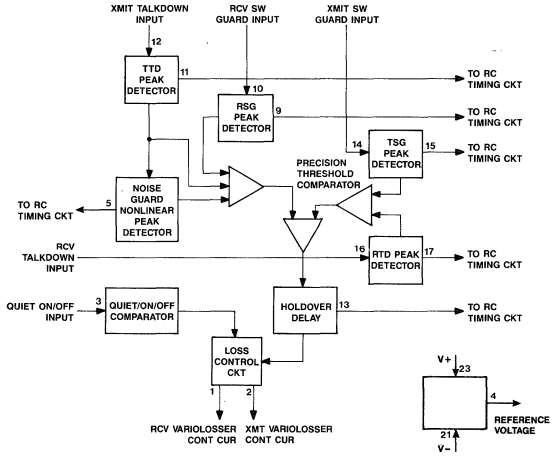
- SINGLE POWER SUPPLY
- DETERMINES TRANSMIT/RECEIVE MODE.
- HALF-DUPLEX OPERATION, RECEIVE IN DEFAULT
- ALL TIMING, CONTROLLABLE WITH EXTERNAL COMPONENTS
- PROVIDES SWITCHING UNAFFECTED BY BACKGROUND NOISE



DIP-24 C Plastic

ORDERING NUMBER: LB1020AF

Fig. 1 - Block Diagram

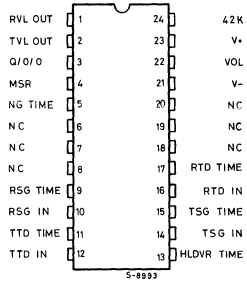


ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Power Dissipation	1000	mW
Operating Voltage	15	V
Storage Temperature Range	−40 to +125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	RVL OUT	This is the control current which regulates the attenuation of the receive variolosser on the LB1021AD. In transmit it is nominally 100 μA. In receive it lies between zero and 100 μA, depending on the volume control voltage.
2	TVL OUT	This is the current which regulates the attenuation of the transmit variolosser. In transmit, it is close to zero, while in receive it is nominally 100 μA.
3	Q/O/O	(Quiet-on-off). Quiet corresponds to >2V, off to <-2V, and on is nominally OV.
4	MSR	Input for the midsupply voltage generated on the LB1021AD, this voltage is used as the signal ground and is not intended to be tied to system ground.
5	NG TIME	(Noise guard timing node). To this is connected the capacitor (usually large) which sets the time over which the background noise guard signal is averaged.
6,7,8 18,19,20	No connection	
9	RSG TIME	To this is connected the RC circuit whose time constant determines the response of the noise guard peak catcher when the noise guard signal falls.
10	RSG IN	This is the input to the receive switch guard peak detector. It is coupled to pin 9 of the LB1021AD through an RC voltage divider. The ratio of this divider sets the relative weight of this particular signal.
11	TTD TIME	The RC circuit at this point sets the time constant of the peak detector for the transmit talkdown signal.
12	TTD IN	This is the input to the transmit talkdown peak detector.
13	HLDVR TIME	The RC pair at this point sets the timing of the transition back to the receive state when an idle condition is preceeded by transmit. It has little effect on the timing of the forced receive transition.
14	TSG IN	Input to the transmit switch guard peak catcher.
15	TSG TIME	The RC pair at this point sets the dynamics of the transmit switch guard peak detector.
16	RTD IN	Input to the receive talkdown peak detector.
17	RTD TIME	Sets the time constant associated with the receive talk down peak detector.
21	V−	The negative power supply connection.
22	VOL	(Volume control input). Goes from −4V (minimum volume) to 0V (maximum volume)
23	V+	The positive power supply connection.
24	42K	A 42.2K 1% resistor is connected from this point to midsupply reference.

ELECTRICAL SPECIFICATIONS (At 25°C)

INPUT-OUTPUT TABLE

STATUS	3 Q/O/O	12 TTD IN	13 HLD TIME	16 RTD IN	22 VOL	1 RVL OUT (μA)		2 TVL OUT (μA)	
						MIN	MAX	MIN	MAX
Normal receive				−1V		−6.5	+6.5	92	110
Normal transmitt		+1V				92	108	−2	+6
Receive with low volume				−1V	−4V	93	107	−6	+10
Transmitt with low volume		+1V			−4V	93	108	−2.2	+6
Off	−4V					150	650	150	650
Quiet	+4V					−6	+6	150	650
Transmit with low volume			+5.5V		−4V	93	108	—	—
Low Volume			−4V	—	—	−6	+10		
Quiet with transmission	+4V	+1V				−6	+6	150	620
Quiet with high level transmission	−4V	+2V				−6	—	150	620

For RSG, RTD, TSG, TTD:	
Timing Discharge Current	440 μA Min.
Timing Leakage Current	1.5 μA Max.
Input Leakage Current	1.5 μA Max.
Power-Supply Current @ ±6V	3.0 − 9.0 mA

TEST SPECIFICATION (For all Tests, V+ = 6V, V− = −6V, and all other voltages are measured with respect to pin 4 (MSR); $T_A = 25°C$)

Symbol	Parameter	Test Conditions	Min	Max	Unit
$I_{(PS)}$	Power Supply Current	Measure current in positive and negative supply leads (see Fig. 2)	3	6	mA
$V_{(13,4)}$	Holdover Voltage, Idle	(See Fig. 2)	2.6	3.4	V
$V_{(13,4)}$	Holdover Voltage, High	$V_{(TTD)} = +2V$ (see fig. 3)	4.3	—	V
$V_{(13,4)}$	Holdover Voltage, Low	$V_{(RTD)} = -2V$ (see fig. 4)	0	1.6	V
$I_{(RVL)}$	Receive Variolosser Current Out, RCV Max Volume	$V_{(VOL)} = 0$ $V_{(RTD)} = -1.0V$ $V_{(QT)} = 0$ (See Fig. 5)	−6.5	+6.5	μA
$I_{(RVL)}$	Receive Variolosser Current Out, RCV Min Volume	$V_{(VOL)} = -4V$ $V_{(RTD)} = -1.0V$ $V_{(QT)} = 0$ (See Fig. 5)	93	107	μA
$I_{(TVL)}$	Transmit Variolosser Current Out, RCV Min Volume	$V_{(VOL)} = -4V$ $V_{(RTD)} = -1.0V$ $V_{(QT)} = 0$ (See Fig. 5)	−6	+10	μA
$I_{(TVL)}$	Transmit Variolosser Current Out, RCV Max Volume	$V_{(VOL)} = 0V$ $V_{(RTD)} = -1.0V$ $V_{(QT)} = 0$ (See Fig. 5)	92	110	μA
$I_{(RVL)}$	Receive Variolosser Current Out, Transmit Max Volume	$V_{(VOL)} = 0V$ $V_{(RTD)} = +1.0V$ $V_{(QT)} = 0$ (See Fig. 6)	92	108	μA
$I_{(TVL)}$	Transmit Variolosser Current Out, Transmit Max Volume	$V_{(VOL)} = 0V$ $V_{(RTD)} = +1.0V$ $V_{(QT)} = 0$ (See Fig. 6)	−2	+6	μA

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions	Min	Max	Unit
$I_{(RVL)}$	Receive Output Variolosser Current, Transmit Min Volume	$V_{(VOL)} = -4V$ $V_{(RTD)} = 0$ $V_{(TTD)} = +1V$ $V_{(QT)} = 0$ (See Fig. 7)	93	108	
$I_{(TVL)}$	Transmit Output Variolosser Current, Transmit Min Volume	$V_{(VOL)} = -4V$ $V_{(RTD)} = 0$ $V_{(TTD)} = +1V$ $V_{(QT)} = 0$ (See Fig. 7)	−2.2	+6	
$I_{(RVL)}$	RCV Variolosser Output Current QUIET/ON/OFF = OFF	$V_{(QT)} = -4V$ (See Fig. 8)	150	650	
$I_{(TVL)}$	Trans. Variolosser Output Current, QUIET/ON/OFF = OFF	$V_{(QT)} = -4V$ (See Fig. 8)	150	650	μA
$I_{(RVL)}$	RCV Variolosser Output Current RCV Quiet	$V_{(QT)} = +4V$ (See Fig. 8)	−6	+6	
$I_{(TVL)}$	Trans Variolosser Output Current, RCV Quiet	$V_{(QT)} = +4V$ (See Fig. 8)	150	650	
$I_{(RVL)}$	Transmit-Volume Interaction Current	$V_{(HLDVR)} = +5.5V$ (See Fig. 9)	−6	+6	
$I_{(TVL)}$	Receive-Volume Interaction Current	$V_{(HLDVR)} = 0$ (See Fig. 9)	−6	10	
$V_{(NG)}$	Noise Guard Timing Offset	(See Fig. 2)	0	620	mV
$I_{(RVL)}$	Transmit State Quiescent Current	$V_{(QT)} = +4V$ $V_{(TTD)} = +1V$ $V_{(RTD)} = 0$ (See Fig. 10)	−6	+6	
$I_{(TVL)}$	Transmit Talkdown Current Transmit Quieting	$V_{(QT)} = +4V$ $V_{(TTD)} = +1V$ $V_{(RTD)} = 0$ (See Fig. 10)	150	620	
$I_{(RVL)}$	Receive Talkdown Current Transmit Off	$V_{(QT)} = -4V$ $V_{(TTD)} = 0V$ $V_{(RTD)} = -2V$ (See Fig. 10)	150	620	μA
$I_{(TVL)}$	Transmit Talkdown Current Transmit Off	$V_{(QT)} = -4V$ $V_{(TTD)} = +2V$ $V_{(RTD)} = 0$ (See Fig. 10)	150	620	
$I_{(13)}$	Noise Guard Action Leakage	(See Fig. 11)	−1.3	+1.3	
$VTH_{(13,4)}$	Transmit Talkdown Voice Switch Threshold	$I_{(HLDVR)} = -24\mu A$ $V_{(RSG)} = 0$ $V_{(TSG)} = 0$ (See Fig. 12)	27.5	40	
$VTH_{(12,4)}$	Transmit Talkdown Voice Switch Threshold, RSG Signal	$I_{(HLDVR)} = -200\mu A$ $V_{(RSG)} = -1V$ $V_{(TSG)} = 0$ (See Fig. 12)	946	1121	mV
$VTH_{(16,4)}$	Receive Talkdown Voice Switch Threshold, RSG Signal	$I_{(HLDVR)} = +65\mu A$ $V_{(RSG)} = 0$ $V_{(TSG)} = 0$ (See Fig. 12)	−27.5	−42.5	
$VTH_{(16,4)}$	Receive Talkdown Switch Threshold, TSG Signal	$I_{(HLDVR)} = +65\ \mu A$ $V_{(RSG)} = 0$ $V_{(TSG)} = +1V$ (See Fig. 12)	−1375	−1633	
$I_{(10)}$	Receive Switch Guard Input Leakage	$V_{(RSG)} = V_{(TTD)} = V_{(RTD)} = V_{(TSG)} = 0$ S1 closed, S2-5 open (See Fig. 13)	−1.5	+1.5	
$I_{(12)}$	Transmit Talkdown Input Leakage	$V_{(RSG)} = V_{(TTD)} = V_{(RTD)} = V_{(TSG)} = 0$ S2 closed, S1,3,4,5 open (See Fig. 13)	−1.5	+1.5	
$I_{(14)}$	Transmit Switch Guard Input Leakage	Close S3 (See Fig. 13)	−1.5	+1.5	μA
$I_{(16)}$	Receive Talkdown Input Leakage	Close S4 (See Fig. 13)	−1.5	+1.5	
$I_{(16)}$	Receive Talkdown Timing Leakage Current	Close S4 and S5 $V_{(RTD)} = +1.0V$ (See Fig. 13)	−1.5	+1.5	

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions	Min	Max	Unit
$I_{(16)}$	Receive Talkdown Timing Discharge Current	Close S4 and S5. $V_{(RTD)} = -1.0V$ (See Fig. 13)	440	—	
$I_{(15)}$	Transmit Switch Guard Time Leakage Current	Close S3 and S6 $V_{(TSG)} = -1.0V$ (See Fig. 13)	−1.5	+1.5	
$I_{(15)}$	Transmit Switch Guard Time Discharge Current	Close S3 and S6. $V_{(TSG)} = +1.0V$ (See Fig. 13)	—	−440	
$I_{(11)}$	Transmit Talkdown Time Leakage Current	Close S2 and S7. $V_{(TTD)} = -1.0$ V (See Fig. 13)	−1.5	+1.5	
$I_{(11)}$	Transmit Talkdown Time Discharge Current	Close S2 and S7. $V_{(TTD)} = +1.0V$ (See Fig. 13)	—	−440	
$I_{(9)}$	Receive Switch Guard Time Leakage Current	Close S1 and S8 $V_{(RSG)} = +1.0V$ (See Fig. 13)	−1.5	+1.5	
$I_{(9)}$	Receive Switch Guard Time Discharge Current	Close S1 and S8. $V_{(RSG)} = -1.0V$ (See Fig. 13)	440	—	
$I_{(22)}$	Volume Control Leakage Current	S1,2,3,4 open. S5,S6 closed. $V_{(VOL)} = -4V$ $V_{(TTD)} = 0$ $V_{(Q00)} = 0$ $V_{(HLDVR)} = 0$ (See Fig. 14)	−1.5	+1.5	
$I_{(13)}$	Holdover Timing Leakage Current	S1,2,3,4,5 open. S6 closed $V_{(VOL)} = 0$ $V_{(TTD)} = 0$ $V_{(Q00)} = 0$ $V_{(HLDVR)} = +4.0V$ (See Fig. 14)	−1.5	+1.5	μA
$I_{(5)}$	Noise Guard Timing Leakage Current	S1,4,5,6 open. S2,S3 closed. $V_{(VOL)} = 0$ $V_{(TTD)} = +1V$ $V_{(Q00)} = 0$ $V_{(HLDVR)} = = 0V$ (See Fig. 14)	4.5	21	
$I_{(5)}$	Noise Guard Drive Leakage Current	S1,4,5,6 open. S2,S3 closed. $V_{(VOL)} = 0$ $V_{(TTD)} = -3V$ $V_{(Q00)} = 0$ $V_{(HLDVR)} = 0V$ (See Fig. 14)	—	350	
$I_{(3)}$	Q/0/0 High Leakage Current	S1,2,3,4,6 open. S5 closed. $V_{(VOL)} = 0$ $V_{(TTD)} = 0$ $V_{(Q00)} = +4.0V$ $V_{(HLDVR)} = 0$ (See Fig. 14)	−12	+12	
$I_{(3)}$	Q/0/0 Low Leakage Current	S1,2,3,4,6 open. S5 closed $V_{(VOL)} = 0$ $V_{(TTD)} = 0$ $V_{(Q00)} = -4.0V$ $V_{(HLDVR)} = 0$ (See Fig. 14)	−12	+12	
$VTH_{(16,4)}$	Receive Talkdown Threshold	$VTH_{(16,4)}$ is the Voltage between pins 16 and 4 at which $V_{(13,4)}$ makes the transition from >1.2V to <1.2V (See Fig. 15)	−24	−46	mV
$VTH_{(13,4)}$	Holdover Timing Threshold Voltge	$VTH_{(13,4)}$ is the voltage between the pins 13 and 4 at which $I_{(TTD)}$ lies between 10 and 90 μA. (See Fig. 16)	.915	1.16	V

TEST CIRCUITS

Fig. 2

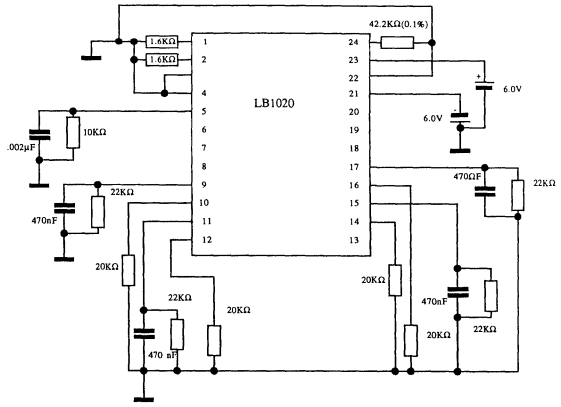


Fig. 3 - Remove load normally connected to pin 12

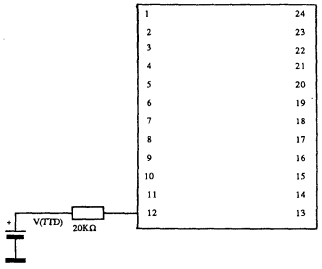


Fig. 4 - Remove load normally connected to pin 16

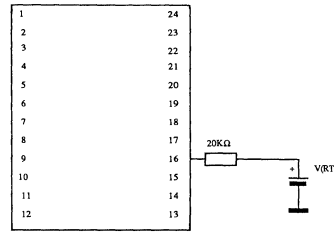


Fig. 5 - Remove load normally connected to pins 1,2,3 and 16

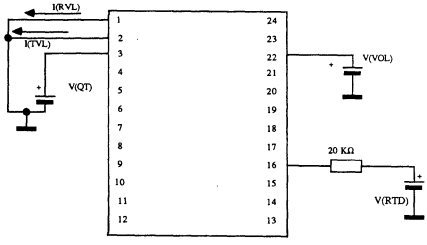
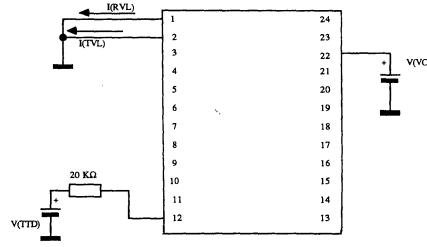


Fig. 6 - Remove load normally connected to pins 1,2,12 and 22.



TEST CIRCUITS (Continued)

Fig. 7 - Remove load normally connected to pins 1,2,12,16 and 22

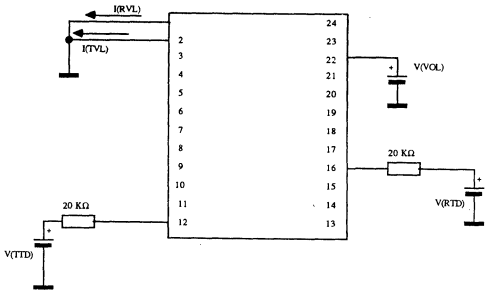


Fig. 8 - Remove load normally connected to pin 3

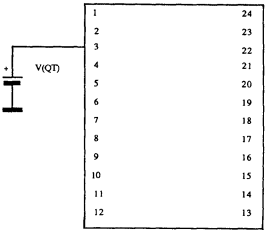


Fig. 9 - Remove load normally connected to pins 1,2,12,16, and 22

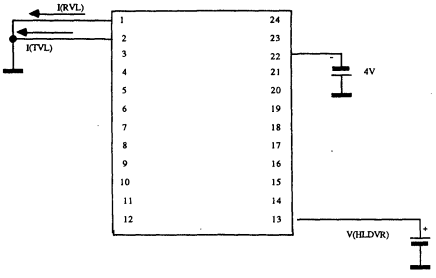


Fig. 10 - Remove load normally to 1,2,12 and 16. $V_{(NG)}$ = voltage measured at test # 19

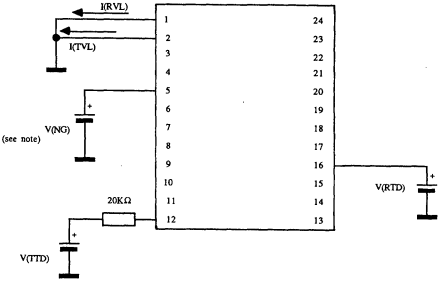


Fig. 11 - Remove load normally connected to pin 12

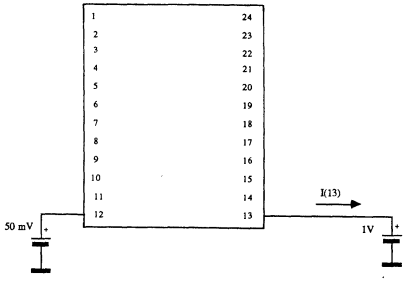
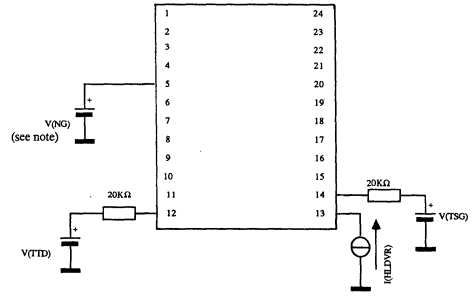


Fig. 12 - Remove load normally to 12 and 14. $V_{(NG)}$ = voltage measured at test # 19



TEST CIRCUITS (Continued)

Fig. 13 - Disconnect load normally to pins 10,12,14, and 16

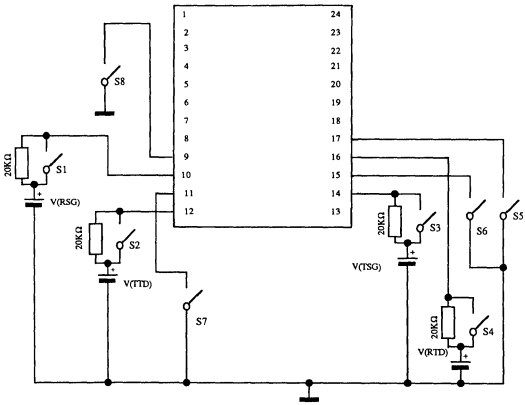


Fig. 14 - Remove normal load from pin 12. Disconnect load normally to pins 10,12,14, and 16

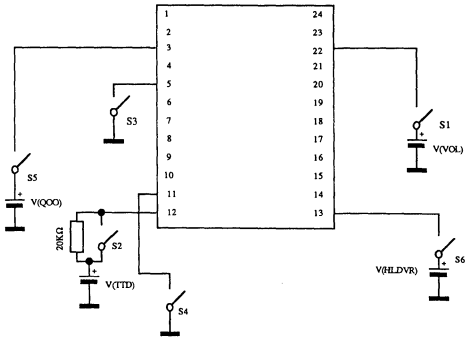


Fig. 15 - $V_{(NG)}$ = voltage measured at test # 19

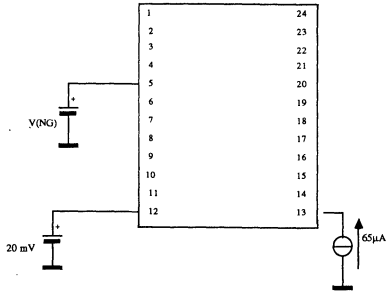
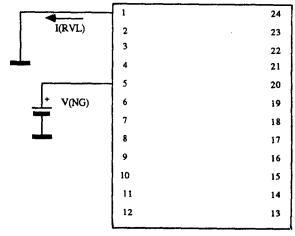


Fig. 16 - $V_{(NG)}$ = voltage measured at test # 19

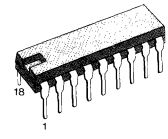


LB1021

SPECIAL AMPLIFIER FOR SPEAKERPHONE APPLICATION

(See Application at the end of the chapter)

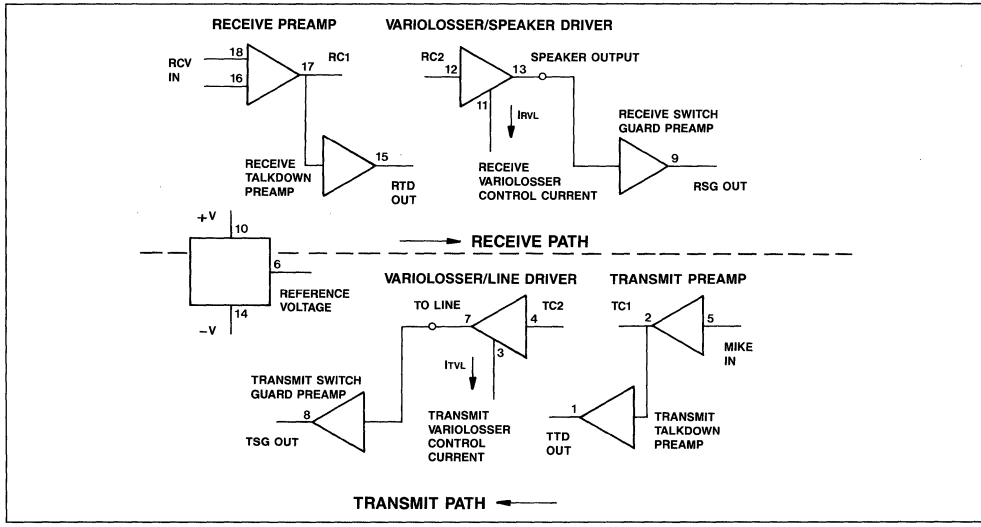
- PROVIDES ALL VOICE PATH AMPLIFICATION
- HIGH-GAIN RECEIVE PREAMPLIFIER ACCOMMODATES VARIETY OF MICROPHONES
- 78 mA SPEAKER DRIVE CAPABILITY
- GAIN, SWITCHING CONTROLLABLE BY 0-100 μA CONTROL CURRENTS



DIP-18 A Plastic

ORDERING NUMBER: LB1021AD

Fig. 1 - Block Diagram

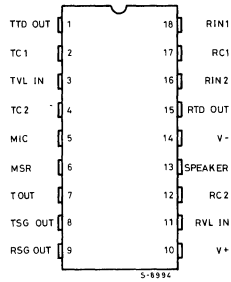


ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Power Supply Voltage	15	V
Power Dissipation	900	mW
Storage Temperature Range	−40 to +125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	TTD OUT	Output of the transmit talkdown amplifier. This is a voltage which is proportional to the output of the microphone.
2	TC1	This is the output of the transmit preamplifier which drives the transmit variolosser. There are two outputs of both the transmit and receive preamplifiers: one to drive the variolosser, the other to drive the talkdown circuits. It should be remembered that these outputs are currents, not voltages.
3	TVL IN	Transmit variolosser control current input.
4	TC2	Transmit variolosser signal current input. This is connected to pin 2 via an RC circuit.
5	MIC	Microphone input. Self-explanatory. There is sufficient gain to handle low-level microphones. Higher-output microphone types may need a resistive pad. The return path to the mike is the mid-supply reference.
6	MSR	Midsupply voltage generated on the chip; this voltage is used as the signal ground and is not intented to be tied to system ground.
7	T OUT	Transmit output, which drives the line in the transmit mode.
8	TSG OUT	Transmit switch guard output. This is a voltage intended to drive the TSG peak detector; it is proportional to the transmitted signal.
9	RSG OUT	Receive switch guard output. Proportional to the voltage which drives the speaker, it is an input to the RSG peak detector.
10	V+	Positive power supply input.
11	RVL IN	Receive variolosser control current input, from the loss control circuit of the LB1020AF.
12	RC2	The signal current input to the receive variolosser.
13	SPEAKER	The return path from the speaker, is the V− supply, not the midsupply reference. The MSR is the output of an operational amplifier, and cannot supply the currents needed to drive the speaker. The speaker is capacitively coupled.
14	V−	Negative power supply input.
15	RTD OUT	Receive talkdown output, proportional to the receive input signal.
16	RIN2	One of the two receive input connections. When the receive signal source is single-ended, this pin is tied to midsupply reference.
17	RCI	The output of the receive preamplifier which drives the variolosser.
18	RIN1	The other receive input (together with RIN2, pin 16)

ELECTRICAL SPECIFICATIONS (For all Tests, V+ = 6V, V− = −6V, and all other voltages are measured with respect to pin 4 (MSR); $T_A = 25°C$)

Parameters	Test Conditions	Min	Nom	Max	Unit
Receive Preamplifier Gain		8.5	12	15	dB
Total Receive Path Gain	$R_{(IN)} = 4$ Kilohms	35	38	41	dB
Receive Max Gain/Min Gain		46	50	53	dB
Transmit Path Gain	(Microphone to $T_{(OUT)}$)	25	28	31	dB
Transmit Max Gain/Min Gain		47	52	56	dB
Receive Variolosser Transimpedance		60.8	74	86	kΩ
Speaker Output Swing	$V_{ps} = \pm 5.5V$, $R_{Speaker} = 45\Omega$	±3.5	—	—	V
Power Supply Current		8.0	22	34	mA
$T_{(OUT)}$ drive current	±3V	±800			μA
Transmit Path quieting		−70			dB

TEST SPECIFICATION (For all Tests, V+ = 6V, V− = −6V, and all other voltages are measured with respect to pin 4 (MSR); $T_A = 25°C$)

Symbol	Parameter	Test Conditions	Min	Max	Unit
$I_{(PS)}$	Power Supply Current	Measure current into VS+ lead (See Fig. 2)	10	30	mA
V_{OS}	MID-Supply Voltage Offset	$V_{OS} = V_{(6)} - \frac{V_{(10)} + V_{(14)}}{2}$ (See Fig. 2)	−100	+100	mV
$V_{(13,6)}$	Speaker Offset Voltage	Ramp current out of lead 11 from 0 to 100 μA. Measure positive and negative excursions of $V_{(13,6)}$ (See Fig. 3)	−80	+80	
$\Delta V_{(13,6)}$	Receive Switch Offset Voltage	Calculate difference between maximum and minimum value of $V_{(13,6)}$ during current ramp of test 3 (See Fig. 3)	—	150	mV_{P-P}
$V_{(9,6)}$	Receive Switch Guard Offset	Ramp current out of lead 11 from 0 to 100 μA. Measure positive and negative excursions of $V_{(9,6)}$ (See Fig. 3)	−0.5	+1.0	V
$V_{(15,6)}$	Receive Talkdown Offset	(See Fig. 2)	−0.5	+0.5	
$I_{(RPRE)}$	Receive Preamp Offset Current	(See Fig. 4)	−70	+70	μA
$V\pm_{(MS)}$	MID Supply Current Source and Sink Capability	VS+ = +5.5V VS− = −5.5 Vary $I_{(MSR)}$ from −10 mA to +10mA Measure $V_{(6)}$ referenced to power supply ground. (See Fig. 5)	−600	+600	mV
$IOS_{(RPA)}$	Receive Preamp Swing, High	$V_{(RIN1)} = +400mV$ $V_{(RC1)} = +2.0V$, Remove normal load from 17 (See Fig. 6)	—	−500	μA
$IOS_{(RPA)}$	Receive Preamp Swing, Low	$V_{(RC1)} = -2.0V$, remove normal load from 17 (See Fig. 6)	+500	—	

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions	Min	Max	Unit
$VOS_{(RTD)}$	RTD Swing, High	$V_{(RIN1)} = -200$ mV (See Fig. 7)	+4.5	—	V
$VOS_{(RTD)}$	RTD Swing, Low	$V_{(RIN1)} = -200$ mV (See Fig. 7)	—	−4.5	
$VOS_{(RSG)}$	RSG Swing, High	$I_{(RC2)} = -200$ mA (See Fig. 8)	+4.5	—	
$VOS_{(RSG)}$	RSG Swing, Low	$I_{(RC2)} = -200$ mA (See Fig. 8)	—	−4.5	
$VOS_{(SPR)}$	Speaker Swing, Positive	$I_{(RC2)} = -500$ μA (See Fig. 9)	+3.3	—	
$VOS_{(SPR)}$	Speaker Swing, Negative	$I_{(RC2)} = -500$ μA (See Fig. 9)	—	−3.3	
$ARCM_{(RP)}$	Receive Preamp Common Mode Rejection	$ARCM_{(RP)} = \frac{V_{(RC1)}}{V_{(RIN1)}}$ (See Fig. 10)	—	0.08	—
$Z01_h$	Receive Path Transimpedance, High	$IAC_{(RC2)} = 10\mu A$ rms, $I_{(RVLM)} = 0\mu A$, $Z01_h = V_{(SPKA)}/I_{(RVLIN)}$ (See Fig. 11)	54.1	93.3	kΩ
$Z01_l$	Receive Path Transimpedance, Low	$IAC_{(RC2)} = 180\mu A$ rms, $I_{(RVLIN)} = 100\mu A$, $Z01_l = V_{(SPKA)}/IAC_{(RC2)}$ (See Fig. 11)	94.4	428	Ω
AV	Receive Variolosser Range	$AV = Z01_h/Z01_l$ (See Fig. 11)	46	54	dB
$Z01_{(RSG)}$	Receive Switch Gaurd Transimpedance	$I_{(RVLIN)} = 0\mu A$ $IAC_{(RC2)} = 4\mu A$ rms $Z01_{(RSG)} = V_{(RSGOUT)}/IAC_{(RC2)}$ (See Fig. 11)	400	665	kΩ
$AI_{(RTD)}$	Receive Talkdown Current Gain	$I_{(RVLM)} = 0\mu A$ $IAC_{(RM1)} = 10\mu A$ $AI_{(RTD)} = V_{(RTDOUT)}/(20.5K\Omega \times 10\mu A)$ (See Fig. 12)	11	13	dB
$AI_{(PRE)}$	Receive Preamp Current Gain	$I_{(RVLIN)} = 0\mu A$ $IAC_{(RM1)} = 30\mu A$ $AI_{(PRE)} = V_{(RC1)}/(2K\Omega \times 30\mu A)$ (See Fig. 12)	7.7	16	
$AT_{(RP)}$	Overall Receive Path Gain	$VAC_{(RIN1)} = 20$ mV (See Fig. 13) $AT_{(RP)} = V_{(SPKR)}/VAC_{(RIN1)}$	38	47	
$V_{(TOUT)}$	Transmit Output Offset	Vary $I_{(TVL)}$ from 0 to 100μA while observing maximum and minimum values of $V_{(TOUT)}$ (See Fig. 14)	−88	+88	mV
$V_{(TOUT)}$ (RANGE)	Transmit Switch Offset	In test 26, $V_{(OUT)(RANGE)} = V_{(TOUT)(MAX)} - V_{(TOUT)(MIN)}$ (See Fig. 14)	—	88	
$V_{(TSG)}$	Transmit Switch Gaurd Offset	Vary $I_{(TVL)}$ fro 0 to 100μA while observing minimum and maximum values of $V_{(TSG)}$ (See Fig. 14)	−550	+280	
$V_{(1,6)}$	Transmit Talkdown Offset	(See Fig. 2)	−550	+550	
$I_{(TC1)}$	Transmit Talkdown Offset	S1 open $V_{(TC1)} = 0$ (See Fig. 15)	−77	+77	μA
$I_{(TC1)}$	Transmit Preamp Swing, Negative	S1 closed $V_{(TC1)} = +2V$ $V_{(MIC)} = +0.3V$ (See Fig. 15)	—	−360	
$I_{(TC1)}$	Transmit Preamp Swing, Positive	S1 closed. $V_{(TC1)} = -2V$ $V_{(MK)} = -0.12V$ (See Fig. 15)	+450	—	

TEST SPECIFICATION (Continued)

Symbol	Parameter	Test Conditions	Min	Max	Unit
$V_{(TTD)}$	Transmit Talkdown Swing, Positive	$I_{(TTD)} = -50\mu A$ $V_{(MK)} = +0.12V$ (See Fig. 16)	3.2	—	V
$V_{(TTD)}$	Transmit Talkdown Swing Negative	$I_{(TTD)} = -50\mu A$ $V_{(MK)} = +0.12V$ (See Fig. 16)	—	1.1	
$V_{(TSG)}$	Transmit Switch Guard Output, Positive	$I_{(TC2)} = +300\mu A$ dc S1 closed $I_{(TVLM)} = 0$ (See Fig. 17)	3.2	—	
$V_{(TSG)}$	Transmit Switch Guard Output, Negative	$I_{(TC2)} = -300\mu A$ dc S1 closed $I_{(TVLIN)} = 0$ (See Fig. 17)	—	−3.2	
$V_{(TRAN)}$	Transmit Voltage Swing, Positive	S1 open $I_{(TC2)} = -800\mu A$ dc $I_{(TVLM)} = 0$ (See Fig. 17)	—	—	
$V_{(TRAN)}$ dc	Transmit Output Swing Negative	S1 open, $I_{(TVLN)} = 0$ $I_{(TC2)} = +800\mu A$ dc (See Fig. 17)	—	−2.7	
$Z_{(TRAN)}$	Transmit Path Trans Impedence Max	S1 open $I_{(TVLN)} = 0$, $I_{(TC2)} = 180\mu A$ rms $Z_{(TRAN)} = V_{(TRAN)}/I_{(TC2)}$ (See Fig. 17)	11.1	22	kΩ
$Z_{(TRAN)}$	Transmit Path Impedence Min	S1 open $I_{(TVLIN)} = 100\mu A$, $I_{(TC2)} = 180$ μA rms $Z_{TRAN} = V_{(TRAN)}/I_{(TC2)}$ (See Fig. 17)	25	88	Ω
$AV_{(TRAN)}$	Transmit Loss Range	$AV_{(TRAN)} = ZTRAN_{(test\ 39)}/ZTRAN_{(test\ 40)}$ (See Fig. 17)	46	57	dB
$A_{(TTD)}$	Transmit Talkdown Voltage Gain	$I_{(TVLM)} = 0$ $V_{(MIC)} = 20$ mV rms $ATTD = V_{(TTD)}/V_{(MIC)}$ (See Fig. 18)	32.7	38.4	
$G_{(TPRE)}$	Transmit Preamp Transconductance	$I_{(TVL)} = 0\mu A$ dc $V_{(MIC)} = 20$ mV rms $G_{(TPRE)} = I_{(TVL)}/10K\Omega/V_{(MIC)}$ (See Fig. 19)	3.0	8.3	ms
$AV_{(TRAN)}$	Transmit Voltage Gain	$I_{(TVL)} = 0$ $V_{(MIC)} = 20\Omega A$ rms $AV_{(TRAN)} = V_{(TRAN)}/V_{(MIC)}$ (See Fig. 18)	22.5	34	dB
ACT	MIC-RSG Crosstalk, High Gain	$I_{(TVL)} = 100\mu A$ $V_{(MIC)} = 120$ mV rms $ACT = V_{(RSG)}/V_{(MIC)}$ (See Fig. 18)	—	3.0	
ACT	MIC-RSG Crosstalk, Low Gain	$I_{(TVL)} = 0$ $V_{(MIC)} = 120$ mV rms $ACT = V_{(RSG)}/V_{(MIC)}$ (See Fig. 18)	—	3.0	
ACT	RIN-TSG Crosstalk	$ACT = V_{(TSG)}/20$ mV (See Fig. 20)	—	10	
$V_{(NOISE)}$	Noise Output	(See Fig. 21)	—	10	mVrms

TEST CIRCUITS

Fig. 2 - Default Test Connection

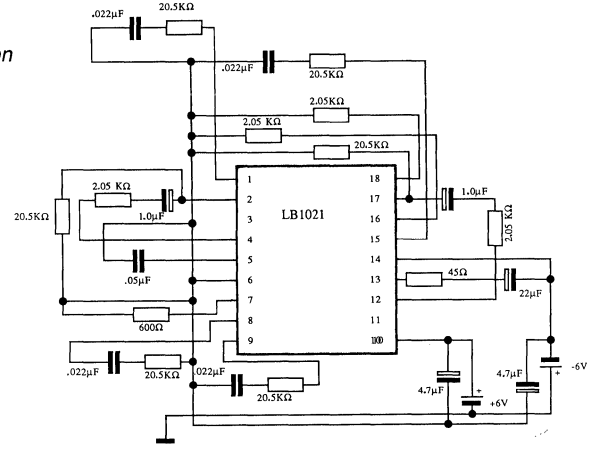


Fig. 3

Fig. 4

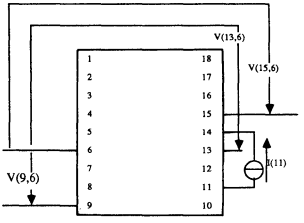


Fig. 5

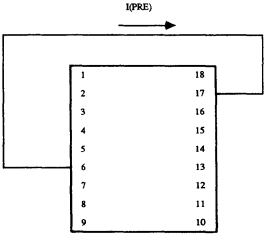
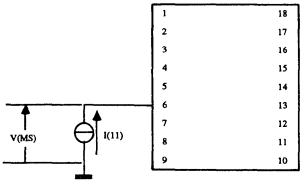
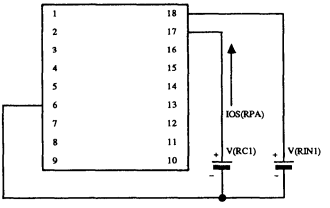


Fig. 6





TEST CIRCUITS (Continued)

Fig. 7 - Remove normal load from pin #15

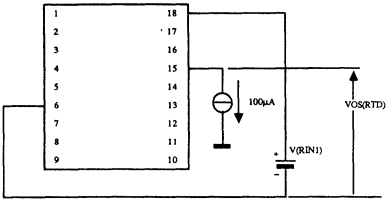


Fig. 8 - Remove normal load from pin #9

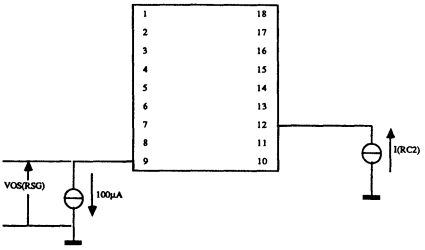


Fig. 9 - Remove normal load from pin #13

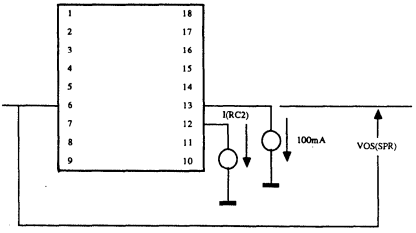


Fig. 10 - Remove normal load from pin numbers 16, 17, and 18

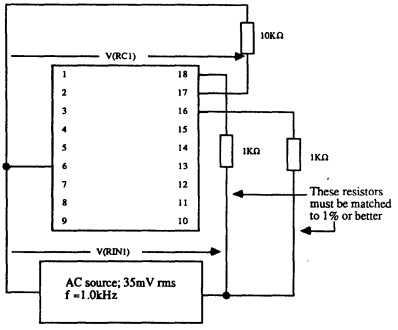


Fig. 11

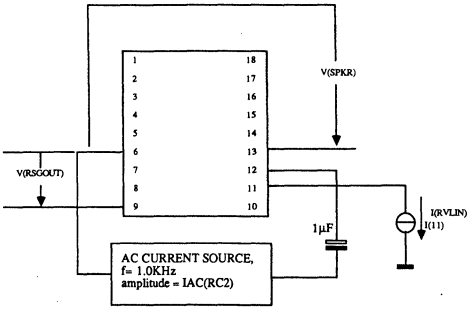
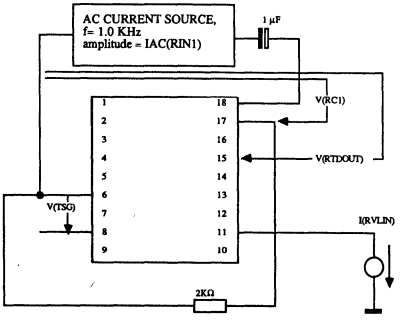


Fig. 12 - Remove normal load from pin 17



TEST CIRCUITS (Continued)

Fig. 13 - Remove mormal load from pin 18

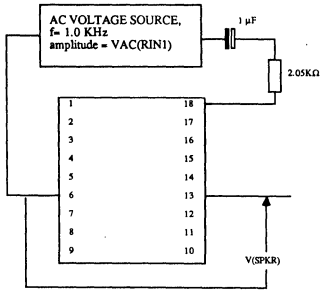


Fig. 14

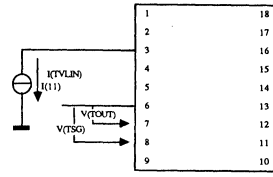


Fig. 15 - Remove normal load from pins 1 and 5

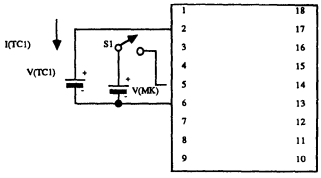


Fig. 16 - Remove normal load from pins 2 and 5

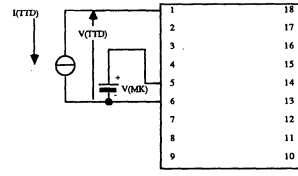


Fig. 17

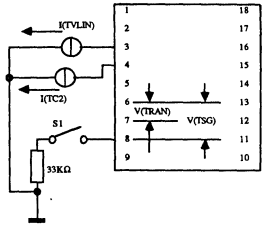
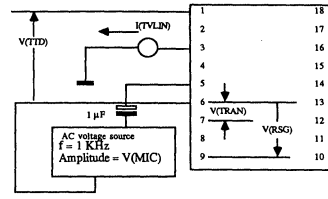


Fig. 18



TEST CIRCUITS (Continued)

Fig. 19 - Disconnect normal load from pin 2

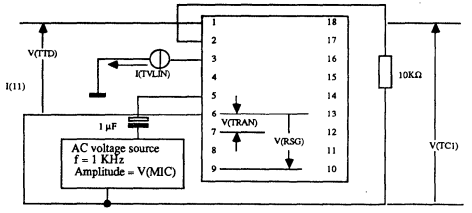


Fig. 20

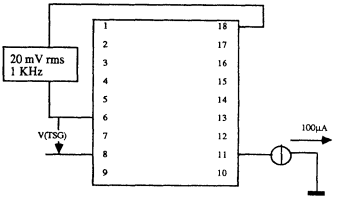
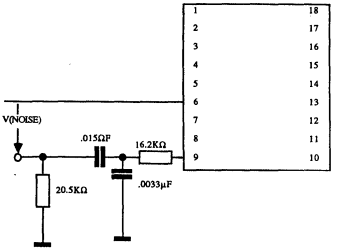


Fig. 21



APPLICATIONS

I. INTRODUCTION

This document is intended to provide background material for the application of two devices, the LB1021AD Speakerphone Voice Path IC and the LB1020AF Speakerphone Switching Circuit IC, in Speakerphone and Speakerphone-like applications. Since the two ICs were designed to be used together, the entire discussion will relate to composite of the pair embedded in a typical Speakerphone circuit.

II. SPEAKERPHONE TUTORIAL

The easiest way to understand the functioning of this (or any) Speakerphone configuration is to consider the problems with which any speakerphone must deal:

1. It must amplify an outgoing (transmit) signal from the microphone to a level high enough to meet transmit specifications.
2. It must amplify an incoming (receive) signal to a high enough power level to drive a speaker.
3. It must prevent the instability that would occur if the received signal fed back to the microphone and became the amplified transmitted signal.

In the realization under discussion here, we solve problem (3) by switching the receive and transmit path in such a manner they are never both on at once. We are, in effect, always breaking one part or the other of the feedback path. This approach is termed "half-duplex" operation, as contrasted to "duplex" operation in which both transmit and receive paths can function at once. As might be imagined, the problem of suppressing oscillation in duplex operation of a speakerphone, which must work in a rather broad range of acoustic environments, can become quite complicated.

For the rest of this tutorial, we shall use the term "Speakerphone Circuit" to refer to the particular half-duplex realization employing the LB1021AD/LB1020AF.

We shall also, for the rest of the discussion, assume that the problem of splitting the communication channel into separate receive and transmit channels has been accomplished. In ordinary telephone applications this is usually done with a hybrid; in principle it could be done with a four-wire transmission line, or by the internal electronics of a CODEC or radiotelephone.

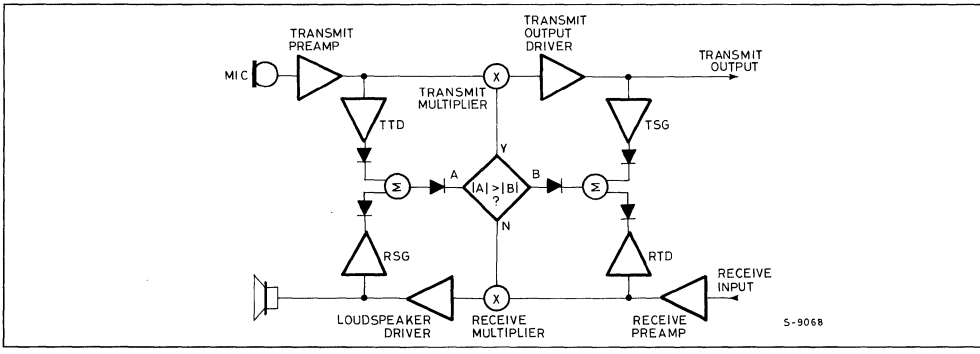
For our circuit, we may now break the Speakerphone into three main elements:

1. A relatively simple transmission path which amplifies the microphone signal and drives the transmission channel. It can be switched on or off.
2. A simple receive path which amplifies the received signal and drives a loudspeaker, it also is switchable.
3. A complex switching circuit which decides between the receive and transmit configuration, based on the nature and relative amplitudes of the receive signal coming in over the line and that generated at the microphone.

Fig. 1 illustrates a fairly primitive speakerphone which illustrates the basic switching scheme employed. The diodes shown on the outputs of some of the amplifiers indicate that the signals at these points are rectified, and either the positive or negative peak values appear.

If we first consider the transmit and receive paths, the most notable feature is that we have elected to do our switching by changing gains rather than by some binary ON-OFF scheme. There is no switching at all in the strict sense; the undesired signal is reduced to a very low level rather than being in-

Fig. 1 - Simplified Speakerphone Circuit



APPLICATION (Continued)

terrupted. We shall not further add to the length of this paper by discussing the pros and cons of alternate approaches, other than to note that they exist.
The switching portion of Figure 1 illustrates the basic approach to switching. Four signals are sampled:

1. Transmit Talkdown (TTD), proportional to the signal from the microphone.
2. Transmit Switch Guard (TSG), proportional to the signal transmitted down the line.
3. Receive Talkdown (RTD), proportional to the received signal.
4. Receive Switch Guard (RSG), proportional to the signal driving the speaker.

In general, switch guard signals tend to prevent a change of configuration, while talkdown signals promote a change.
To see how the system works, suppose the system is in a transmit configuration, and someone is speaking into the microphone. The TTD output is high, and its positive peaks are being held; RSG is low. There is therefore a large positive signal at A, which passes through to the A > B? comparison circuit. TSG is high also, and its positive peaks are held, while RTD is low. B is high and positive, but the diode prevents it from getting through to the comparator. A therefore dominates the switching, and the circuit is held in transmit mode.
Now suppose that the person on the other end of the line wishes to interrupt, and begins to speak more loudly than the person who has the line. RTD increases, and, assuming the person who wants the line is speaking loudly enough, it becomes greater than TSG. B then becomes large and negative. RSG has not changed, since switching has not yet occurred, so A is unchanged. When the magnitudes of the receive input signal relative to the microphone signal becomes great enough, the circuit will switch into receive.
At this point TSG drops low and RSG increases. This causes A to decrease in magnitude, or even change sign; B remains negative and its magnitude increases. This drives the circuit even deeper into the receive configuration. Even if the microphone signal were to increase slightly, or the receive signal were to decrease slightly, the configuration would not drop back into transmit. This hysteresis prevents the distracting rapid switching back and forth that would otherwise occur when the two signal levels were very close to one another.

Although this simplified circuit provides the hysteresis necessary to prevent switching instabilities at near-identical signal levels, it would have numerous other distracting shortcomings.
The largest set of shortcomings derives from the fact that the circuit, as shown, has no built-in delays or time constants. In the transmit mode, for example, the system could be switched by a small signal, or even by noise, every time the speaker paused. Indeed, it could be easily switched during the small time intervals between words.
Moreover, Figure 1 gives no indication that the switching of the circuit is done over a time interval. However, if background noise, speech, and any dc offsets in the system are switched intantaneously, the hearer is aware of a popping sound. Switching must therefore be done by ramping volume over a well-controlled time interval. This time interval must be short when speech is being switched, since clipping of the initial syllable must be avoided. In the present speakerphone system, the line always falls back to receive when no one is speaking. In this case, the primary source of pop is noise and d.c. offset, and there is no speech to mask it, and the gain rampup time can and should be longer.
If a simple speakerphone is used in an environment where there is a steady noise in the background, that noise can easily dominate the switching, so that the speakerphone would tend always to fall back into the transmit state. A feature that automatically subtracted out a constant, or at least a slowly varying, background noise before making the switching decision wuold be useful in many applications.
Finally, we have not yet considered user-controlled features that would normally be needed: volume control, muting (so that transmission can be cut off during a side conversation) and, of course, on-off controls.

III. Speakerphone Block Diagram

Figure 2 is a diagram of the whole speakerphone configuration realized with LB1020AF and LB1020AD pair.
Let us begin with the transmit gain path. This consists of:

Transmit Preamplifier This takes the incoming voltage signal from the microphone, amplifies it, and converts it to two proportional currents. (The multiplication step which follows is more easily accom-

APPLICATION (Continued)

plished working with currents). One current goes to the transmit multiplier, the other to transmit talkdown (TTD) amplifier.

Transmit Multiplier, which attenuates the current output of the transmit preamplifier by a factor proportional to the TVL current from the loss control circuit.

Transmit output driver. At this point the current is converted back to a voltage; the voltage at this point is the transmitted voltage.

The receive amplifier chain is very similar to the transmit chain:

Receive preamplifier This amplifies the received signal from the line and converts it to two currents. One current drives the receive multiplier, the other is the input to the receive talkdown (RTD) amplifier. Notice that, unlike the transmit preamplifier, this preamplifier has a differential input: that's the way telephone signals often come.

Receive Multiplier attenuates the current from the receive preamplifier by a factor proportional to the RVL output of the loss control circuit.

Loudspeaker Driver Converts the current from the receive multiplier, and provides sufficient power to drive a 45 ohm speaker.

The decision of whether to be in transmit or receive mode is based on samples of the power levels at four points: microphone, receive input, speaker, and transmit output. The circuitry which performs the decision function is driven by four voltage inputs. Four preamplifiers are necessary to provide voltages proportional to the four signals. These are:

Transmit Talk Down The reason for the nomenclature is covered in the preceeding section and will not be repeated here. Since we must convert a current to a voltage, this is a transresistance amplifier, and provides a voltage proportional to the microphone signal level.

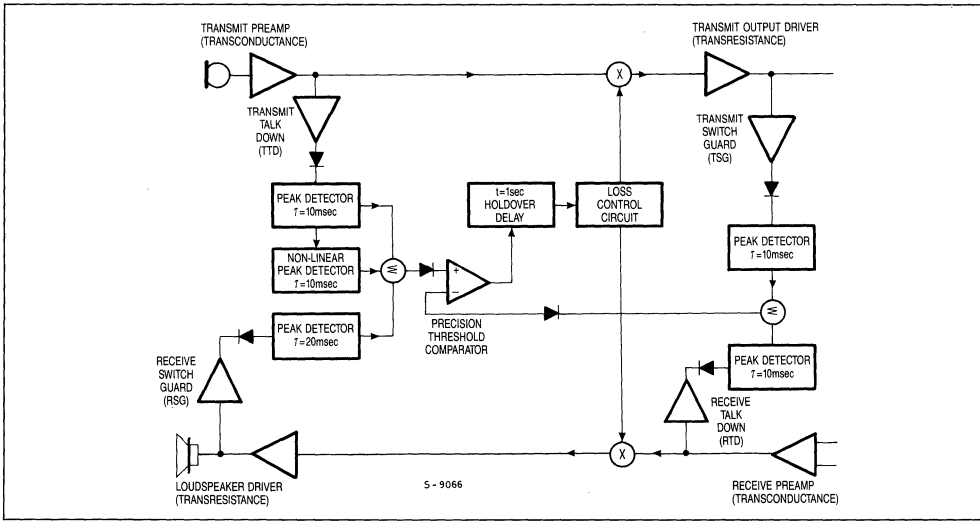
Transmit Switch Guard This is a voltage amplifier, and samples the transmitted voltage.

Receive Talk Down A transresistance amplifier whose output is proportional to the received signal.

Receive Switch Guard A voltage amplifier whose output is proportional to the speaker drive level.

The outputs of these four amplifiers are a.c. coupled to peak catcher circuits via external RC circuits. This external coupling circuit can be selected to vary the characteristic time constants of the peak catchers. Figure 3 illustrates the block diagram of a typical peak catcher circuit.
This might be a good place to point out that the

Fig. 2 - Functional block diagram

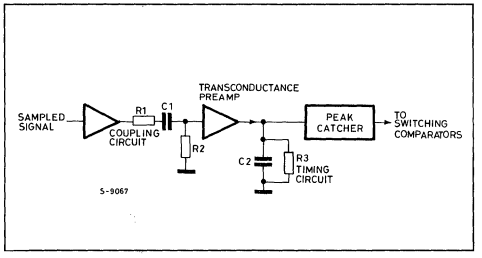


APPLICATION (Continued)

ground signal, where shown, refers to a voltage midway between the positive and negative voltages. The power supply is often single-ended, and generating a mid-supply reference (MSR) voltage provides the stable signal reference which is critical in a circuit which employs high gains, as this one does.

There are two RC circuits involved in the structure: one is the coupling circuit feeding the peak catcher, the other is a timing circuit within the catcher. Of course, the coupling circuit can in principle influence the time constant, but normally the values of R1,R2, and C1 will be selected so that the $(R1 + R2)C1 \ll R3 \times C2$. The purpose of R1 and R2 is not to set timing, but rather to set the relative weighting factors of RSG, RTD, TTD, TSG, and NG. The voltage input to the peak catcher is converted to a current, and drives a circuit which has a fast attack time, but a decay time set by an external $R3 \times C2$ circuit. The fast attack time assures that the circuit will respond quickly enough that initial syllables will not be lost. The long decay time constant assures that the peak catcher will bridge short gaps in the conversation.

Fig. 3 - Block diagram of typical peak character



The sense of rectification of the peak catchers is selected so that a positive-going output tends towards a decision for transmit, while a negative-going waveform corresponds to receive. Thus the TTD and TSG peak detectors put out a positive waveform, while the RSG and RTD peak detectors put out negative waveforms.

There is a fifth circuit lumped in with the peak detectors, called the noise guard. Its input is the (positive) output of the transmit talk down peak detector. The noise guard is a quick-decay, slow attack inverting circuit with a very long (10 second) time constant. Its effect is therefore to subtract out that component of the TTD signal which is the time-averaged minimum of the TTD waveform. Such a factor would be significant if there were a steady noise in the background from air conditioning, fans, factory, machinery, etc.

The outputs of the five peak catcher circuits (to be really precise, we would have to call the noise guard a valley catcher) are fed into a precision threshold comparator. This portion of the circuit is more than a simple comparator. Basically, it recognizes three states: forced transmit, forced receive, and idle. The idle state corresponds to the situation where neither the microphone nor the incoming receive signals are high enough to force the configuration. In this case, the default state is receive.

However, as was explained in section II, switching under such a condition can give rise to an audible pop. Moreover, there is no hurry to switch to the default condition, and we would therefore like to make the switching time constant long compared to that of forced switching.

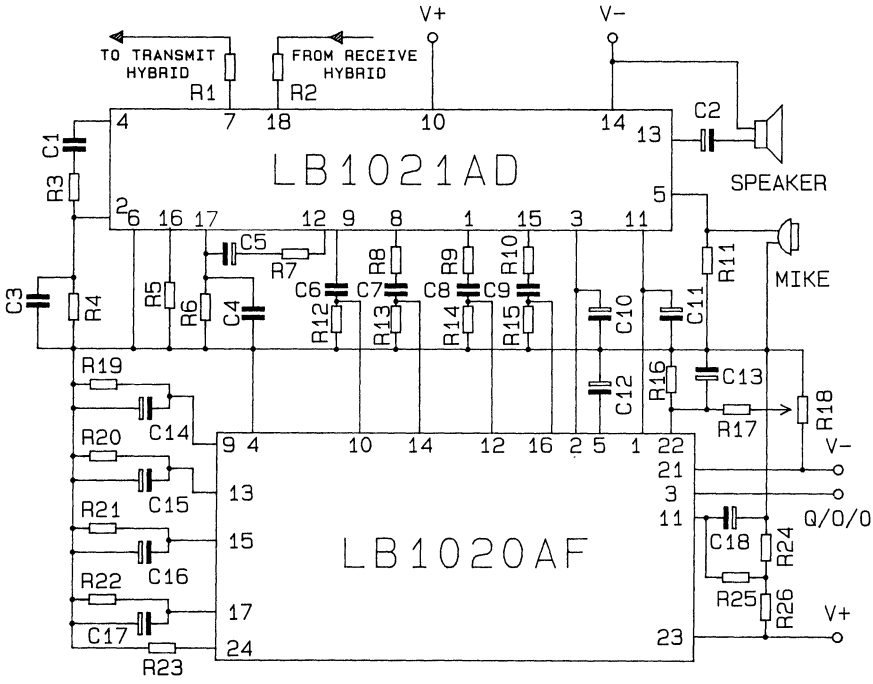
The circuit therefore has two switching time constants, set by the parallel external RC combination called the holdover timing network. The switching time during forced switching is set by the capacitor only, which is driven by 500 μA during a forced switching condition. Switching corresponds to a 5V change accross the capacitor, so forced swiching time is 5C/500 μA; it would be about 5 milliseconds for a 47 μF capacitor.

The switching time for idle state switching is set by the time for the voltage of 5.8 volts, which is the normal transmit state voltage, to decay to zero. Since no currents are being forced under this condition, the time is set by the time constant of the RC circuit. For reasonable values of R, this is on the order of a second or two.

As has been noted before, the switching action is implemented by having the loss control circuit generate two control currents, receive variolosser (RVL) and transmit variolosser (TVL) currents. These currents control the attenuation of the two amplifier path multipliers. The nominal range of these control currents is from 0 to 100 μA. Zero current corresponds to minimum attenuation, while 100 μA is maximum attenuation. The two currents track; this is necessary to prevent overall loop gain from ever getting high enough to cause feedback and instability. Receive variolosser control current is modified by the setting on the volume control input, so that, in the receive mode, the RVL control current, instead of being a nominal zero, is a function of the volume control voltage. -4 volts on the volume control input lead corresponeds to minimum volume, 0 volts is maximum volume.

APPLICATION (Continued)

In addition to the volume control, there is a quiet-on-off control. When the voltage at this point goes above +2V with respect to midsupply, the system is locked out of the transmit configuration. This is useful if one wants to have a side conversation without the person being called overhearing. The phone is forced into an "off" state when the voltage is pulled below −2V with respect to midsupply. With the voltage at midsupply, the normal "on" conditions prevail.



R1 = 3.01 KΩ
R2 = 2.05 KΩ
R3 = 2.05 KΩ
R4 = 2.05 KΩ
R5 = 2.05 KΩ
R6 = 196 KΩ
R7 = 3.15 KΩ
R8 = 1.87 KΩ
R9 = 59 KΩ
R10 = 78.7 KΩ
R11 = 10 KΩ
R12 = 7.87 KΩ
R13 = 2.05 KΩ
R14 = 38.3 KΩ
R15 = 18.7 KΩ
R16 = 205 KΩ
R17 = 100 KΩ
R18 = 100 KΩ
R19 = 21.5 KΩ
R20 = 3 MΩ
R21 = 21.5 KΩ
R22 = 21.5 KΩ
R23 = 42.2 KΩ
R24 = 100 Ω
R25 = 21.5 KΩ
R26 = 10 KΩ
C1 = 68nF
C2 = 20μF
C3 = 10nF
C4 = 47nF
C5 = 0.22μF
C6 = 10nF
C7 = 2.2nF
C8 = 4.7nF
C9 = 4.7nF
C10 = 1μF
C11 = 1μF
C12 = 47μF
C13 = 0.1μF
C14 = 0.47μF
C15 = 0.47μF
C16 = 0.47μF
C17 = 0.47μF
C18 = 0.47μF

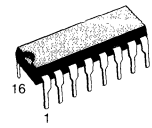
LB1022AC
LB1022BC

PRELIMINARY DATA

AN AT&T PRODUCT

QUAD LINE RECEIVERS

- MEETS EIA RS-422A/423A SPECIFICATIONS
- FOUR INDEPENDENT RECEIVERS WITH COMMON STROBE TTL COMPATIBLE INPUT
- ELECTROSTATIC DISCHARGE PROTECTION ON RECEIVER INPUTS
- REQUIRES ONLY A SINGLE 5V (±10%) POWER SUPPLY
- INPUT SENSITIVITY:
  LB1022AC ±200 mV
  LB1022BC ±500 mV
- MINIMUM INPUT HYSTERESIS:
  LB1022AC ±15 mV
  LB1022BC ±30 mV
- INTERNAL FAIL-SAFE FORCES THE OUTPUT HIGH FOR AN OPEN INPUT CONDITION
- TYPICAL PROPAGATION DELAY OF 17 ns

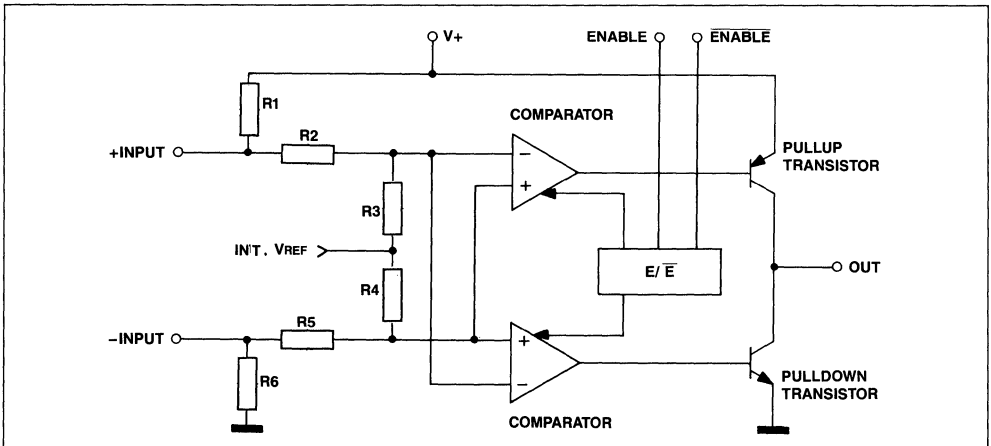


DIP-16 B Plastic

ORDERING NUMBER: LB1022AC
LB1022BC

The LB1022AC and LB1022BC Quad Line Receivers are general purpose quad line receivers for balanced and unbalanced data transmission. A TTL compatible Enable, $\overline{\text{Enable}}$ is common to all four receivers in the device package. The Enable, $\overline{\text{Enable}}$ allows the output to assume a high impedance state for output busing. These devices are encapsulated in a 16-pin plastic dual in-line package (DIP) and designed to meet industry standard EIA RS-422A specifications for the LB1022AC and EIA RS-423A specifications for the LB1022BC. They are pin compatible replacements for devices 26LS32 and 26LS33, respectively.

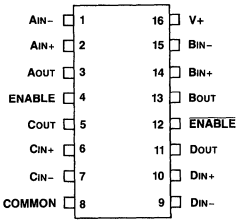
Figure 1 - Functional Diagram



NOTES: R1 and R6 are fail safe resistors.
R2,R3,R4,R5 form an Input Divider.
With the internal reference VREF, these components set the input characteristics.
One of four identical circuits shown.

LB1022AC
LB1022BC

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Name	Pin	Symbol	Name
1	$A_{IN}-$	Neg. Input, Rec'r A	9	$D_{IN}-$	Neg. Input, Rec'r D
2	$A_{IN}+$	Pos. Input, Rec'r A	10	$D_{IN}+$	Pos. Input, Rec'r D
3	A_{OUT}	Output, Rec'r A	11	D_{OUT}	Output, Rec'r D
4	ENABLE	Enable Input	12	$\overline{\text{ENABLE}}$	$\overline{\text{Enable}}$ Input
5	C_{OUT}	Output, Rec'r C	13	B_{OUT}	Output, Rec'r B
6	$C_{IN}+$	Pos. Input, Rec'r C	14	$B_{IN}+$	Pos. Input, Rec'r B
7	$C_{IN}-$	Neg. Input, Rec'r C	15	$B_{IN}-$	Neg. Input, Rec'r B
8	COMMON	Circuit common (not necessarily physical or system ground).	16	V+	Supply Voltage, External

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Supply Voltage (V+)	7.0	V
Control Input Voltage (Enable, $\overline{\text{Enable}}$)	7.0	V
Input Common Mode Range	±25	V
Input Differential Voltage	±25	V
Storage Temperature Range	−40 to 125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
Supply Voltage (V+)	4.5 to 5.5	V
Operating Ambient Temperature Range	0 to 85	°C
Input Common Mode Range LB1022AC LB1022BC	 ±7.0 ±15	 V V

ELECTRICAL CHARACTERISTICS ($0 \leq T_A \leq 85°C$, $4.5 \leq V+ \leq 5.5$, unless otherwise specified)

Parameter	Test Conditions		Min	Max	Unit
Differential Input Thereshold Voltage	$I_O = -0.4mA$, $V_{OH} \geq 2.7$ (See Fig. 4) LB1022AC $-7V < V_{CM} < 7V$ LB1022BC $-15V < V_{CM} < 15V$		— —	0.2 0.5	V
	$I_O = 4mA$, $V_{OL} \leq 0.5$ (See Fig. 4) LB1022AC $-7V < V_{CM} < 7V$ LB1022BC $-15V < V_{CM} < 15V$		— —	−0.2 −0.5	
Dynamic Input Resistance	$-15V < V_{CM} < 15V$ (See Fig. 5) One input AC GND		6	—	kΩ
Input Current	$V_{IN} = 15V$ (See Fig. 6) $V_{IN} = -15V$		— —	2.3 −2.8	mA
Input Hysteresis Voltage	$V+ = 5V$; $T_A = 25°C$ LB1022AC $V_{CM} = \pm 7V$ LB1022BC $V_{CM} = \pm 15V$		−15 −30	+15 +30	mV
High Level Output Voltage	$V+ = 4.5V$ (See Fig. 7) $V_{\overline{ENABLE}} = 0.8V$; $I_{OH} = -440\mu A$		2.7	—	V
Low Level Output Voltage	$V+ = 5.5V$ (See Fig. 7) $V_{ID} = -0.8V$ $V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 4mA$	—	0.4	
		$I_{OL} = 8mA$	—	0.45	
Output Short Circuit Current	$V_O = 0V$, $V+ = 5.5V$ (See Fig 8) $V_{ID} = 1V$		−15	−85	mA
Off State Output Current (High Z)	$V+ = 5.5V$, $V_O = 2.4V$ (See Fig. 9)		—	20	μA
	$V+ = 5.5V$, $V_O = 0.4V$		—	−20	
Power Supply Current	$V+ = 5.5V$ (See Fig. 10) All Inputs GND, Output Disabled		—	70	mA
Input Low State Voltage[1]	$V+ = 5.5V$, $V_{IN} = 0V$		—	0.8	V
Input High State Voltage[1]			1.8	—	
Low State Current[1]	$V+ = 5.5V$, $V_{IN} = 2.7V$		—	−360	μA
High State Current[1]			—	20	
High Voltage Current[1]	$V+ = 5.5V$, $V_{IN} = 5.5V$		—	100	μA
Input Clamp Voltage[1]	$V+ = 4.5V$, $I_{IN} = -18mA$		—	1.5	V

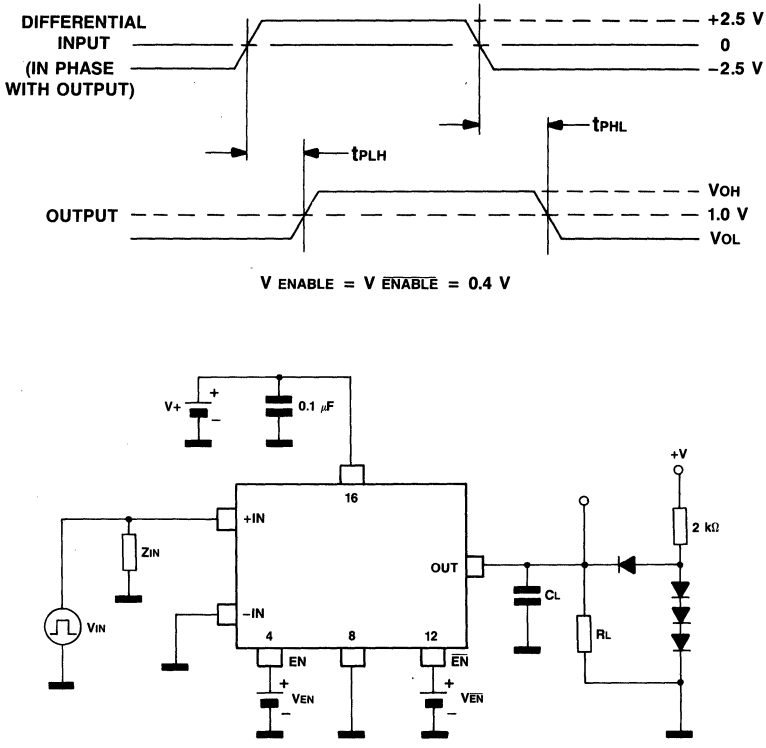
Note 1. These specifications refer only to Enable and $\overline{\text{Enable}}$ inputs (pin 4 and 12 respectively).

TIMING CHARACTERISTICS

Characteristic and Conditions				Min	Max	Unit
Propagation Delay Time	$T_A = 25°C$ $V+ = 5.0V$ $C_L = 20pF$	$R_L = 5.0$ kΩ (See Fig. 2)	t_{PLH}	—	25	ns
			t_{PHL}	—	25	
		$R_L = 1.67$ kΩ (See Fig. 3)	t_{PLZ}	—	30	
			t_{PHZ}	—	27	
		$R_L = 5.0$ kΩ (See Fig. 3)	t_{PZL}	—	22	
			t_{PZH}	—	24	

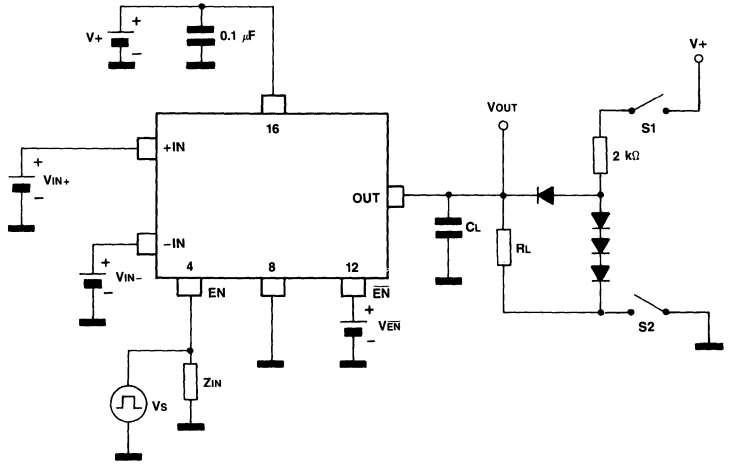
TEST CIRCUITS

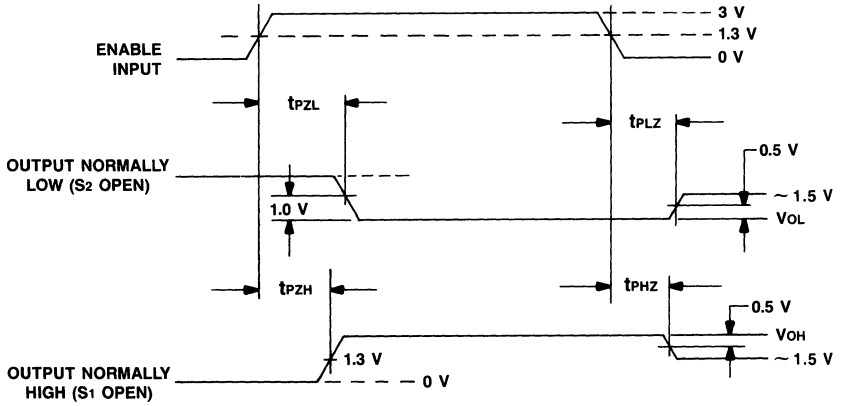
Fig. 2 - Signal Propagation Delay Time



TEST CIRCUITS (Continued)

Fig. 3 - Enable/Disable Delay time





Notes: S_1 and S_2 of Load Circuit are Closed Except as Noted Above, and $V_{\overline{ENABLE}}$ = 1.8 V
Pulse Generator: Rate ≤ 1.0 MHz, Z_O = 50 Ω, tr ≤ 15 ns, tf ≤ 6 ns

TEST CIRCUITS (Continued)

Fig. 4

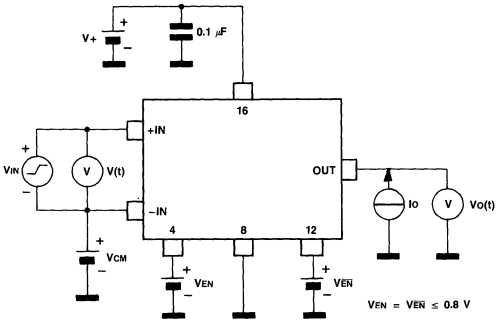


Fig. 5

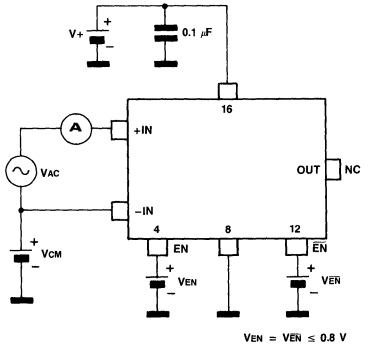
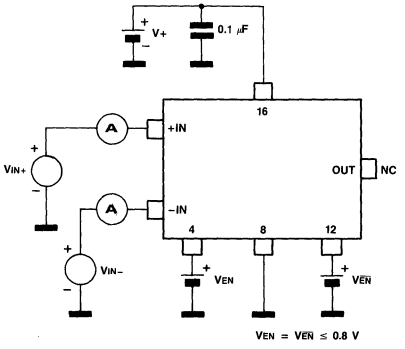


Fig. 6



TEST CIRCUITS (Continued)

Fig. 7

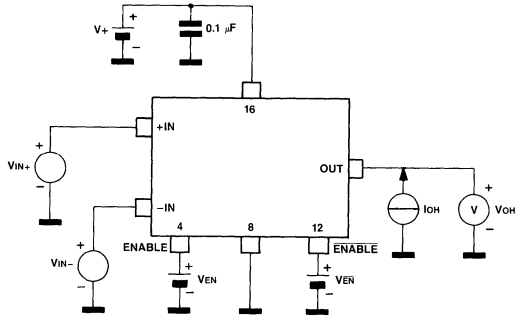


Fig. 8

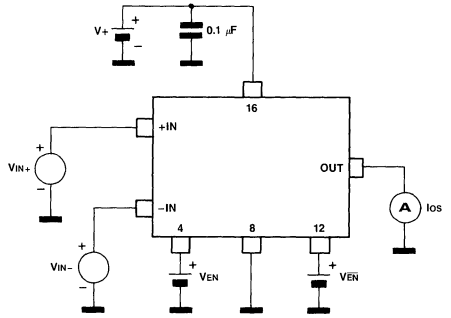
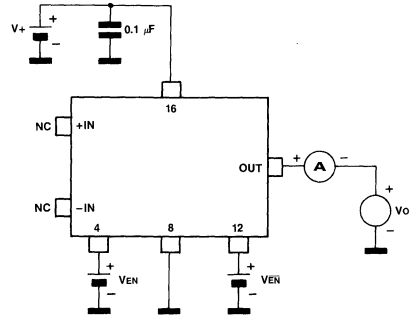
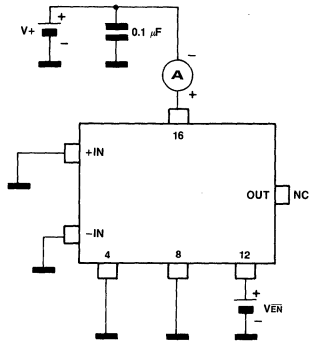


Fig. 9



TEST CIRCUITS (Continued)

Fig. 10

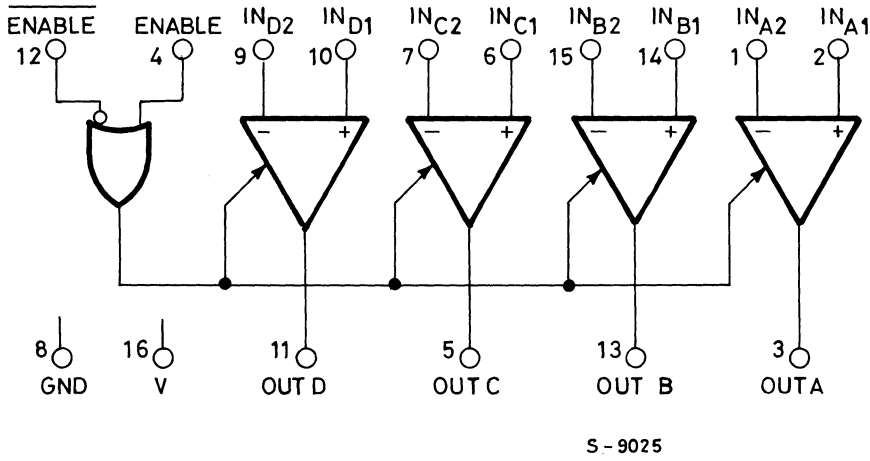


TRUTH TABLE FOR ENABLE, $\overline{\text{ENABLE}}$ Inputs

E	$\overline{E}$	Output
0	0	Enabled
1	0	Enabled
0	1	Disabled
1	1	Enabled

0 = low state ($V_{in} \leqslant 0.8V$)
1 = high state ($V_{in} \geqslant 2.0V$)

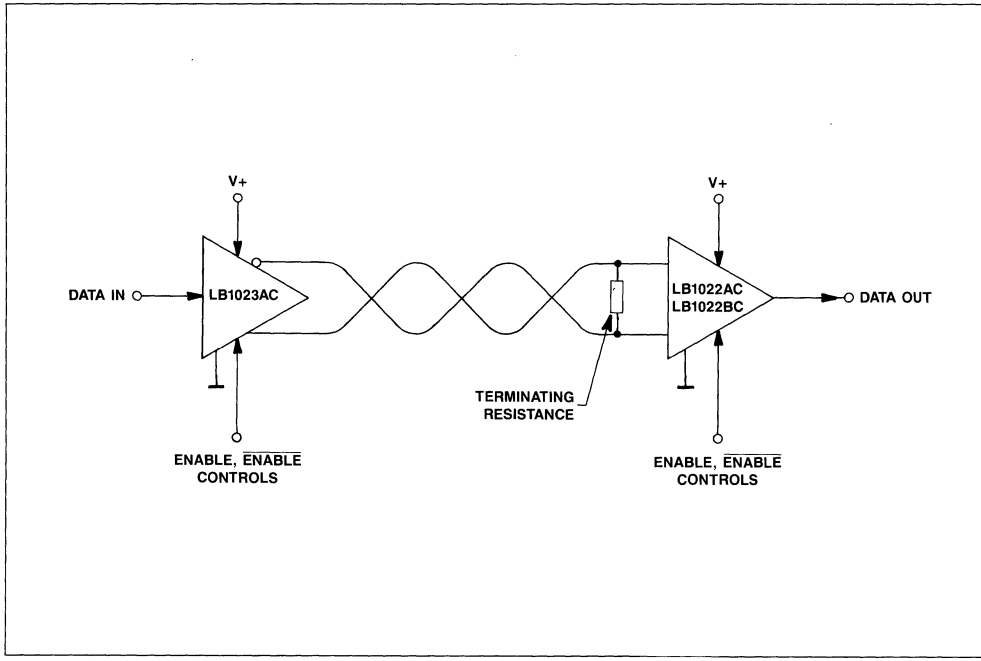
Fig. 11 - Block Diagram



APPLICATION

The following Truth Table shows the ENABLE, and $\overline{\text{ENABLE}}$ conditions which must be met to provide specific "Receiver Output States".
The following diagram illustrates basic information for application of the LB1022A and B line receiver devices in a Two-Wire Balanced RS-422A System. This particular diagram shows the LB1022A Line receivers interfacing with the LB1023AC Line Driver.

Fig. 12 - Quad Line Receiver Application Diagram



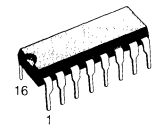
LB1023

PRELIMINARY DATA

AN AT&T PRODUCT

QUAD LINE DRIVER

- MEETS EIA RS-422A REQUIREMENTS
- PROPAGATION DELAY IS LESS THAN 20 ns
- ENABLE OR $\overline{\text{ENABLE}}$ TO OUTPUT DELAY IS LESS THAN 40 ns
- TTL COMPATIBLE ENABLE AND $\overline{\text{ENABLE}}$ INPUTS
- POWER SUPPLY CURRENT IS REDUCED TO LESS THAN 40 mA WHEN DEVICE IS DISABLED
- OUTPUT SKEW (TIME DELAY BETWEEN DIRECT OUTPUT AND INVERSE OUTPUT) TYPICALLY 2 ns

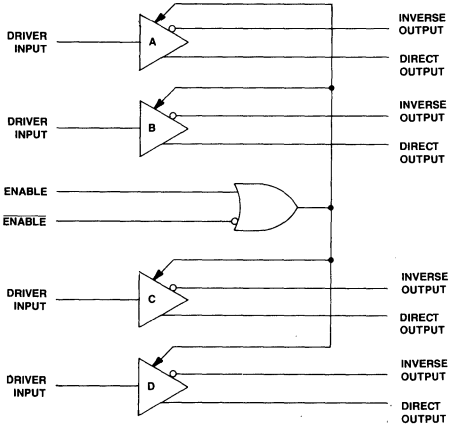


DIP-16 A Plastic

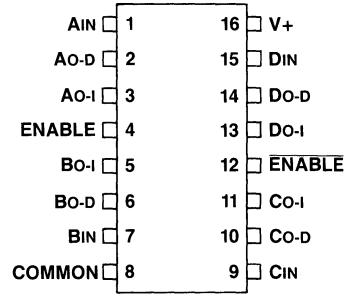
ORDERING NUMBER: LB1023AC

The LB1023 Quad Line Driver is an integrated circuit consisting of four independent line drivers with a common control for both ENABLE and $\overline{\text{ENABLE}}$. It provides high speed differential drive to transmission lines having an impedance of at least 100 ohms. Each of the four drivers has a complementary tristate output. The LB1023 requires only a single 5 volt supply ($\pm$10%) for operation.

Fig. 1 - Functional Diagram



PIN CONFIGURATION



PIN DESCRIPTION

Name	Description
A_{IN} B_{IN} C_{IN} D_{IN}	TTL compatible inputs for Line Drivers A through D respectively
A_{OD} B_{OD} C_{OD} D_{OD}	Non-inverting Line Driver outputs for drivers A through D respectively.
A_{OI} B_{OI} C_{OI} D_{OI}	Inverting Line Driver outputs for drivers A through D respectively.
ENABLE	Logic-High-Enable, TTL compatible input. See Truth Table under Applications for logic programming of this pin.
$\overline{\text{ENABLE}}$	Logic-Low-Enable, TTL compatible input. See Truth Table under Applications for logic programming of this pin.
V+	Connection for external power supply.
COMMON	Circuit common (not necessarily physical or system ground).

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Power Supply Voltage (V+)	7.0	V
Input Operating Voltages, V+, Driver Inputs, ENABLE and $\overline{\text{ENABLE}}$	5.5	V
Driver Output Current	±35	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING CHARACTERISTICS (T_A = 25°C, V+ = 5V, See Fig. 7)

Symbol	Characteristics	Min.	Typ.	Max.	Unit
T_{THL} or T_{TLH}	Transition time; (see Figure 2)	—	—	20	ns
T_{PHL} or T_{PLH}	Propagation Delay Time; (see Figure 3)	—	—	20	ns
T_{SKEW}	V_{OD} to V_{OI} Time Difference; (see Figure 2)	—	±2.0	±6.0	ns
$\frac{V_{peak}-V_+}{V_+}$	Overshoot, (see Figure 3)	—	—	10	%

TIMING CHARACTERISTICS (Continued)

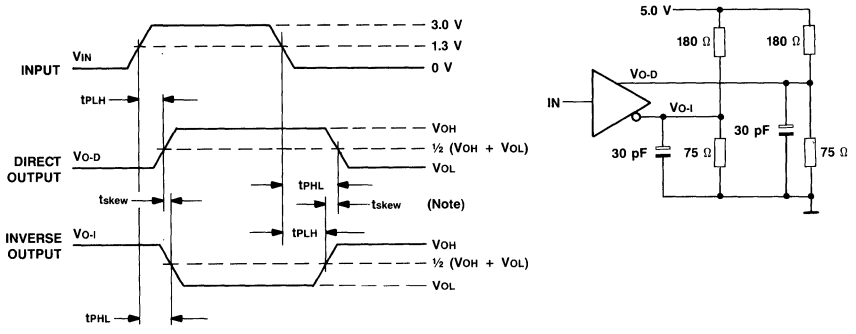
Driver Disable and Enable Times (see Figures 4, 5 and 6)

Symbol	Characteristics	Min.	Typ.	Max.	Unit
	Output $\overline{\text{ENABLE}}$ Times (See Fig. 5 and Note 1):				
t_{HZ}	Output high to "high impedance"	—	—	40	ns
t_{LZ}	Output low to "high impedance"	—	—	40	ns
	Output Enable Times (See Fig. 4 and Note 1)):				
t_{ZH}	"High impedance" to output high;	—	—	30	ns
t_{ZL}	"High impedance" to output low	—	—	30	ns

NOTE 1: The device is disabled when ENABLE = LOW and $\overline{\text{ENABLE}}$ = HIGH. All other conditions of ENABLE and $\overline{\text{ENABLE}}$ will allow the device to operate (see Truth Table under Applications).

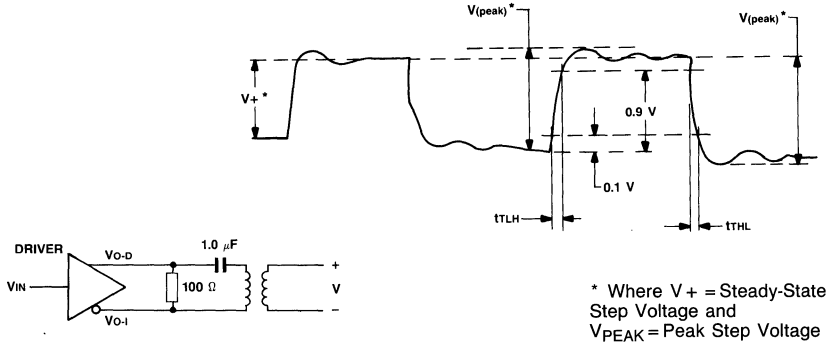
TIMING DIAGRAMS

Fig. 2 - Propagation Delay and t_{SKEW} Diagram and Associated Load Schematic



Note: t_{skew} is defined as the absolute time difference between the average voltage of the input and its complement. The average voltage is ½ ($V_{OH} + V_{OL}$. Either output, V_{O-D} or V_{O-I} may occur first.

Fig. 3 - Overshoot Diagram and Associated Load Schematic



* Where V+ = Steady-State Step Voltage and V_{PEAK} = Peak Step Voltage

TIMING DIAGRAMS

Fig. 4 - Enable and Output Waveforms

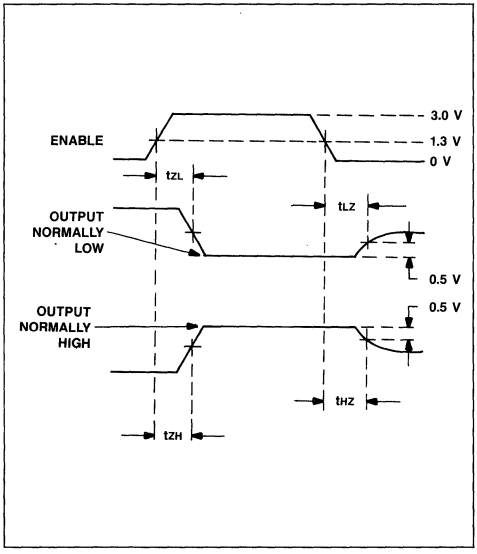


Fig. - 5 $\overline{Enable}$ and Output Waveforms

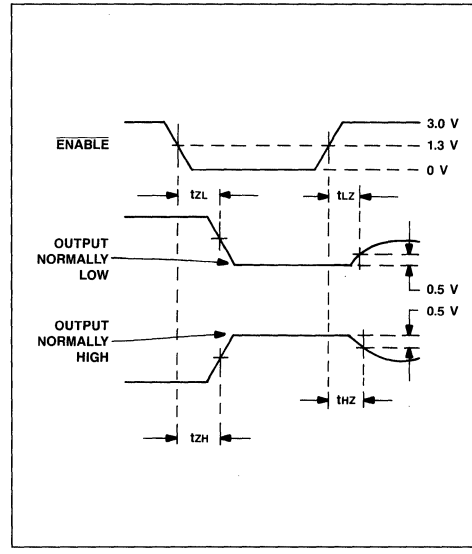


Fig. 6 - Associated Enable, $\overline{Enable}$ Loading Diagrams

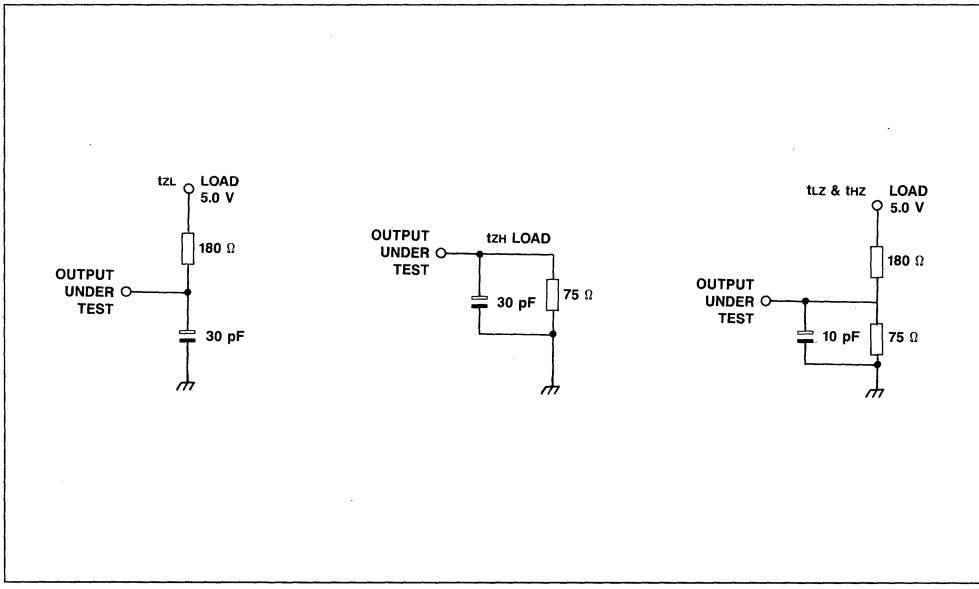
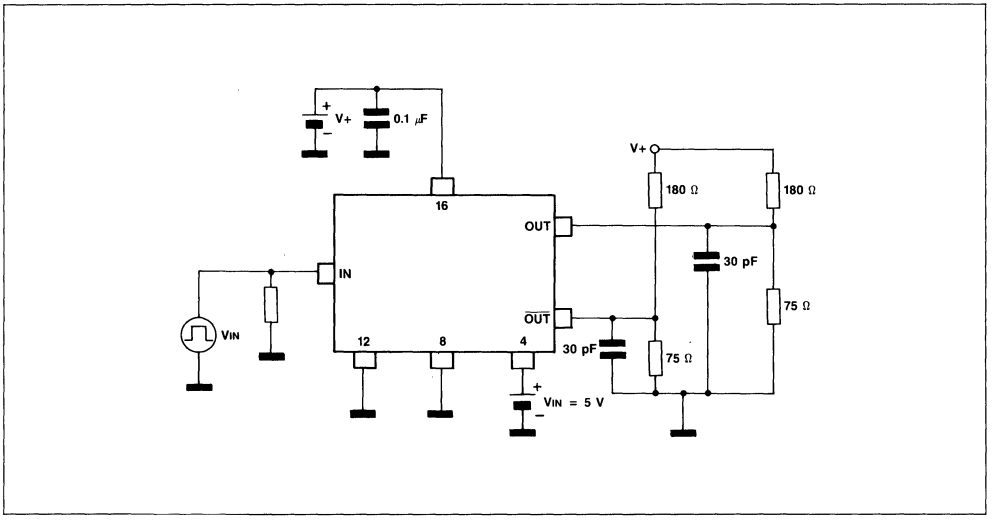


Fig. 7 - Switching Time Test Configuration



ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified)

Parameter	Test Conditions		Min	Typ	Max	Unit
Power Supply Operating Voltage	(See Fig. 8)		4.5	—	5.5	V
Output Voltage	$V+ = 4.5V$, $I_O = 20mA$, (See Fig. 8)	High	2.5	—	3.5	V
	$V_{IH} = 2.0V$, $V_{IL} = 0.8V$ (See Fig. 8)	Low	0.05		0.5	V
Input Clamp Voltage	$V+ = 4.5V$, $I_{IN} = -18mA$	(See Fig. 9)	0	—	−1.5	V
Power Supply Current	$V+ = 5.5V$, $V_{IN} = 0$ (See Fig. 10)	No Load	45	—	90	mA
	$V+ = 5.5V$, $V_{IN} = 2.0V$ (See Fig. 10)	Disabled	20	—	40	mA
Output Current	$V_O = 0.5$ or $2.5V$ (See Fig. 11)	Disabled	—	—	±20	μA
	$V_O = -0.25$ or $6.0V$ (See Fig. 12)	Power Off	—	—	±100	μA
	$V+ = 5.5V$ (See Fig. 13)	Short-Circuit	—	—	−150	mA
Input Current	$V_{IN} = 0.4V$ (See Fig. 14)	Low	0	—	−0.36	mA
	$V_{IN} = 2.7V$ (See Fig. 14)	High	—	—	±20	μA
	$V_{IN} = 7.0V$ (See Fig. 14)	Reverse	0	—	0.1	mA

TEST CIRCUITS

Fig. 8 - Output Voltage (High) (Low)

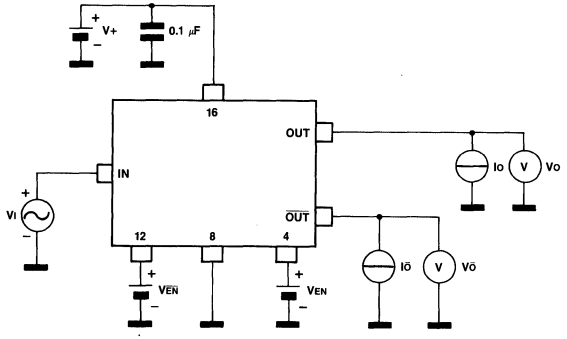


Fig. 9 - Input Clamp Voltage

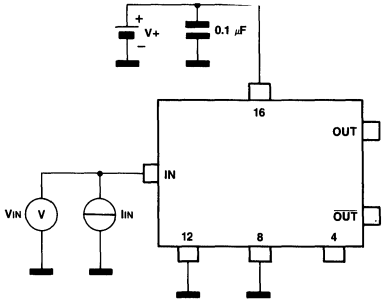


Fig. 10 - Power Supply Current No Load & Disabled

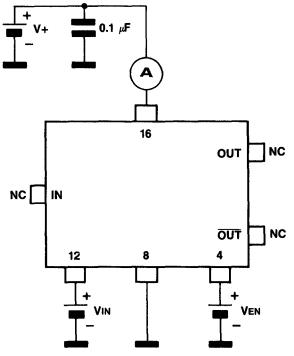


Fig. 11 - Output Current (Disabled)

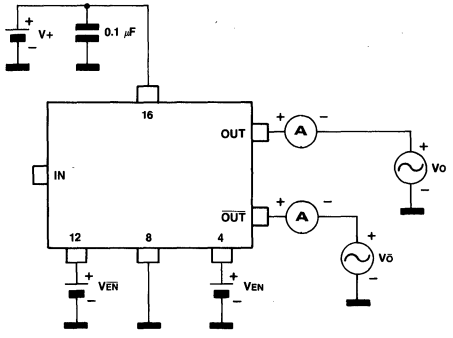
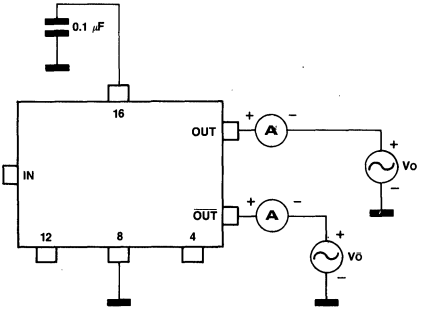


Fig. 12 - Output Current (Power OFF)



TEST CIRCUITS (Continued)

Fig. 13 - Output Current, Short Circuit

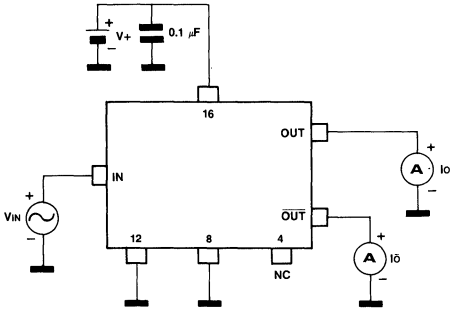
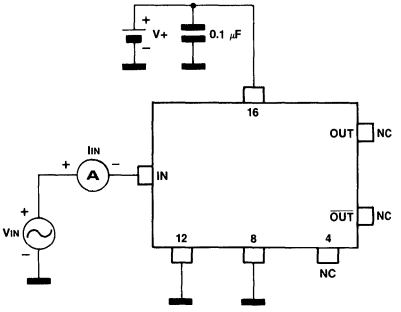


Fig. 14 - Input Current (Low) (High) (Reverse)



APPLICATION

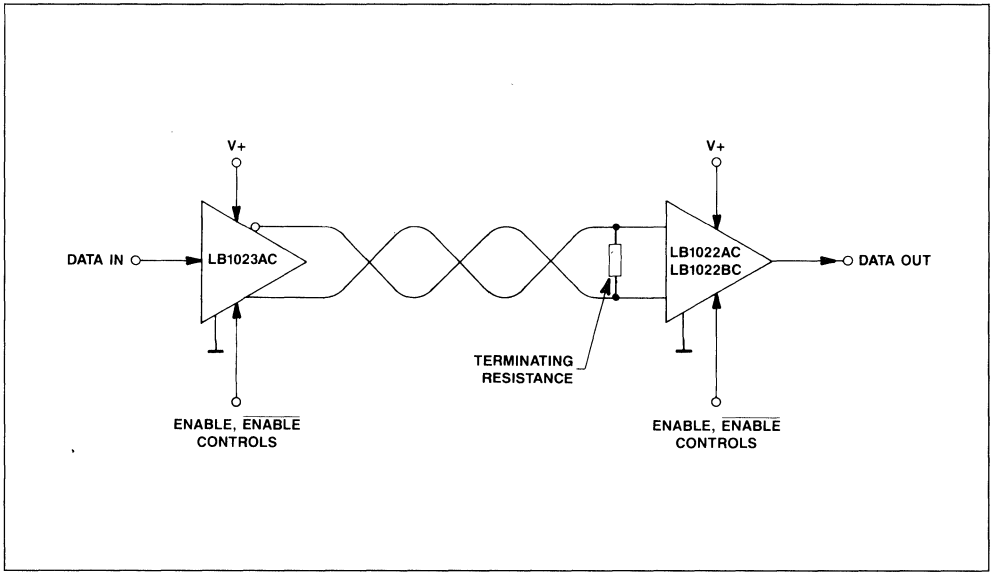
The following Truth Table shows the V+, ENABLE, $\overline{\text{ENABLE}}$ and "Data In" conditions which must be met to provide specific "Driver Output States" (both direct and inverse outputs).
Figure 15 illustrates basic information for application of the LB1023 line driver devices in a Two-Wire Balanced RS-422A System. This particular diagram shows the LB1023 Line Driver interfacing with the LB1022A type Line Receivers.

TRUTH TABLE

Condition [1]	Data In [1]	Direct Output	Inverse Output
Enable is High	High	High	Low
Enable is High	Low	Low	High
$\overline{\text{Enable}}$ is Low	High	High	Low
$\overline{\text{Enable}}$ is Low	Low	Low	High
Enable is Low AND $\overline{\text{Enable}}$ is High	Don't Care	High Impedance	High Impedance
V+ is Low (≤ 0.5V)	Don't Care	High Impedance	High Impedance

NOTE 1: High and Low levels for Enable, $\overline{\text{Enable}}$ and Data In are TTL levels ($V_{IH} \geq$ 2.0V, $V_{IL} \leq$ 0.8V).

Fig. 15 - LB1023 Quad Line Driver Application Diagram



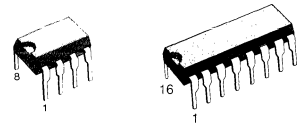
LB1024AB
LB1024BC

PRELIMINARY DATA

AN AT&T PRODUCT

DIGITAL-SIGNAL TRANSCEIVERS

- TRANSMITTED OUTPUT OF CURRENT-LIMITED, COMPLEMENTARY VOLTAGE PULSES
- POSITIVE – AND NEGATIVE – RECEIVED SIGNALS ARE DETECTED SEPARATELY
- TTL COMPATIBLE INPUTS AND OUTPUTS
- HIGH INPUT IMPEDANCE ALLOWS TRANSCEIVER TO BE DRIVEN BY EITHER TTL OR CMOS
- 40 kHz OPERATION
- CAN BE POWERED BY A SINGLE 5V POWER SUPPLY
- ENABLE INPUTS (DRIVE AND RECEIVE) ARE TIED TOGETHER (LB1024AB ONLY)
- ENABLE INPUTS (DRIVE AND RECEIVE) MAY BE OPERATED INDEPENDENTLY OR TIED TOGETHER
- MINIDIP PLASTIC; LB1024AB
- 16-PIN PLASTIC DIP; LB1024BC

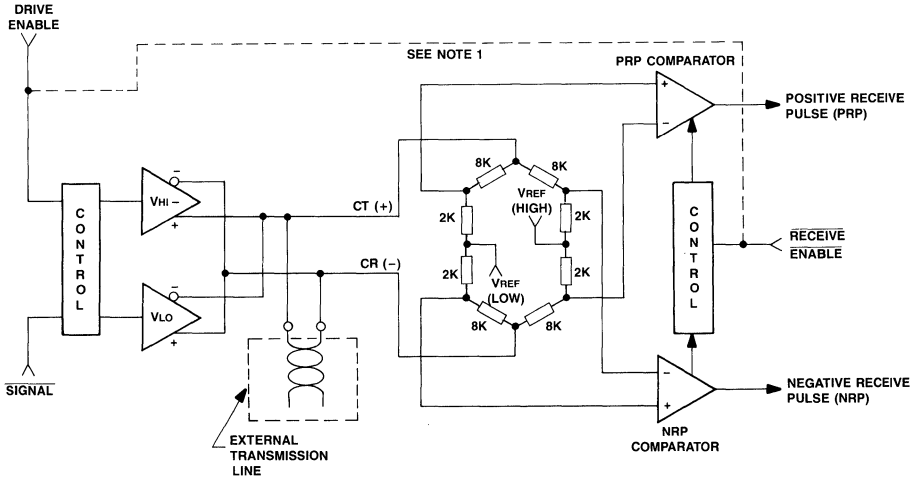


Minidip A DIP-16 A Plastic

ORDERING NUMBER: LB1024AB
LB1024BC

Each transceiver receives or transmits on a "one pair" transmission line. The outputs are current limited to prevent damage from faults to ground, faults to the positive supply, or faults from line to line. Transmission radiation is minimized by having one driver that raises the voltage (approximately 0.7V) on one line of a wire pair, while another driver lowers the voltage (approximately 0.7V) on the other line. Thus, the DC level of the pair remains constant. Two receive comparators sense differential voltage on the wire pair. Both outputs are low when the differential voltage is below a set threshold value. The PRP comparator goes HIGH for positive signals and the NRP comparator goes HIGH for negative signals.

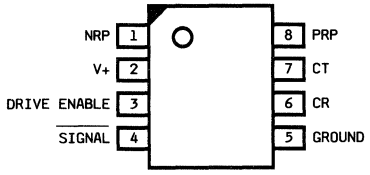
Fig. 1 Functional Diagram



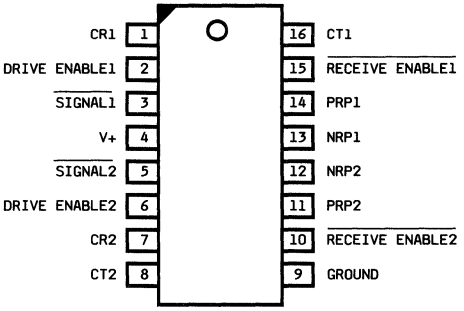
NOTE 1: The DRIVE and RECEIVE ENABLE pins are internally tied together for the LB1024AB device only.

LB1024AB
LB1024BC

PIN CONFIGURATION



LB1024AB



LB1024BC

PIN DESCRIPTION

NOTE (For the LB1024BC dual version device only). A designator (either 1 or 2 following the pin name) means that this terminal is part of either transceiver section 1 or 2 respectively.

Name	Description
CR CR1, CR2	Line Driver/Receiver (negative output/input terminal). This pin interfaces with an external transmission line.
CT CT1, CT2	Line Driver/Receiver (positive output/input terminal). This pin interfaces with an external transmission line.
NRP NRP1, NRP2	Logic output terminal for the Negative Receive Pulse comparator. This output is HIGH for negative input pulses.
PRP PRP1, PRP2	Logic output terminal for the Positive Receive Pulse comparator. This output is HIGH for the positive input pulses.
DRIVE ENABLE DRIVE ENABLE1 DRIVE ENABLE2	A logic HIGH on this terminal activates the "transmit" function for the LB1024BC device. The "drive enable" and "$\overline{\text{receive enable}}$" functions are internally tied to the DRIVER ENABLE pin for the LB1024AB device. Thus, with a logic HIGH or logic LOW on this pin, the LB1024AB is either in a "transmit" or "receive" mode respectively.
$\overline{\text{RECEIVE ENABLE1}}$ $\overline{\text{RECEIVE ENABLE2}}$	A logic low on this terminal activates the "receive" function for the LB1024BC device. The LB1024AB devices has no external pin for this function. In the LB1024AB device, the "receive enable" function and the "drive enable" function are both tied to the DRIVE ENABLE pin. The comparator outputs are disabled when the receiver section is disabled. The comparator outputs are a logic LOW when the differential voltage of CT minus CR is below a set threshold value.
$\overline{\text{SIGNAL}}$	Input for line driver signals.
V+	Connection for external power supply
GROUND	Circuit common (not necessarily physical or system ground).

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Power Supply Voltage	6.0	V
Line Driver/Receiver Voltage (CT or CR to V+); LB1024AB	+3.9	V
Line Driver/Receiver Voltage (CT or CR to V+); LB1024BC	+1.0	V
Line Driver/Receiver Voltage (CT or CR to GROUND); LB1024AB	−1.0	V
Line Driver/Receiver Voltage (CT or CR to GROUND); LB1024BC	−4.3	V
Inputs (DRIVE ENABLE, CT or CR to GROUND)	−1.0	V
Inputs (DRIVE ENABLE, SIGNAL or RECEIVE ENABLE TO V+)	+1.0	V
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unles otherwise specified)

Parameter	Test Condition			Min	Max	Unit
Power Supply Current (Comparators Enabled-Voltage Drivers Disabled)		LB1024AB		1.87	3.13	mA
		LB1024BC		3.15	5.29	
Input Signal Range		LB1024AB		0	8.9	V
		LB1024BC		−4.3	5	
LINE DRIVER						
Output Voltage	Differential			1.3	1.7	V
	High-Level	150Ω Load		2.8	5.0	
	Low-Level		(See Fig. 2)	0	1.8	
	Driver Off	Open Circuit	(See Fig. 3)	2.24	2.46	
Differential Output Voltage	Driver Off	Open Circuit	(See Fig. 3)	—	±0.01	
Short-Circuit Output Current	High-Level		(See Fig. 4)	−17	−26	mA
	Low-Level		(See Fig. 4)	17	26	
LINE RECEIVER						
Ouptut Voltage	High-Level (ΔV_{in} = ±1.0V)		(See Fig. 5)	2.5	5.0	V
	Low-Level (ΔV_{in} = ±1.0V)		(See Fig. 5)	0	0.4	
	Small-Signal (ΔV_{in} = ±0.2V)		(See Fig. 5)	0	0.4	
Input Voltage	Receive Mode Range			See Table 1		
Output Leakage Current	High State, Disabled Mode, V_{out} = 0V (See Fig. 3)			0	−1.0	μA
	Low-State, Disabled Mode, V_{out} = 5.0V (See Fig. 3)			0	1.0	
LOGIC INPUTS						
Input Voltage	Maximum Low-Level			—	0.8	V
	Minimum High-Level			2.0	—	

TEST CIRCUITS

Fig. 2 - V_{OUT} Voltage

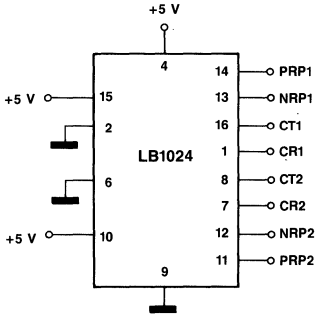


Fig. 3 - Driver Output Voltage

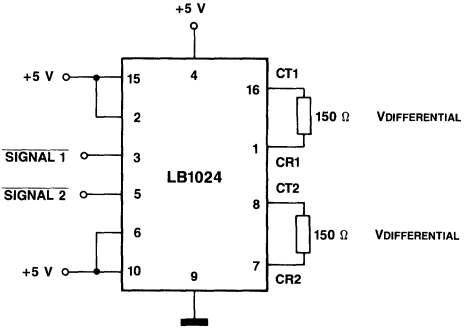


Fig. 4 - Driver Short Circuit Output Current

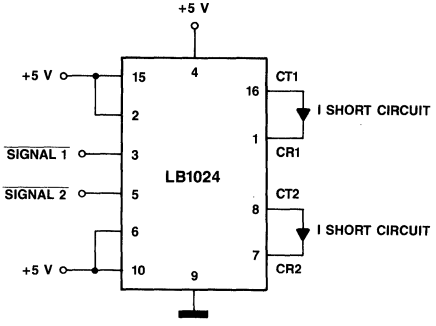
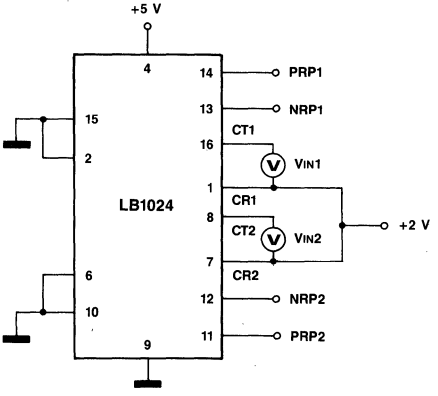


Fig. 5 - Receiver Output Voltage



APPLICATION

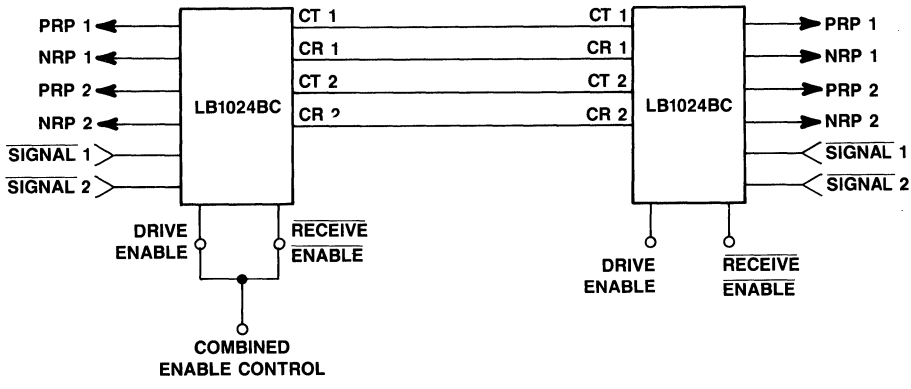
Table 1 gives the logic information necessary for the operation of the LB1024 type Transceivers. Figure 6 is a typical application of the Dual Transceiver device. This diagram illustrates two types of "enable control" operation: combined and independent control.

Table 1 - LB1024AB, LB1024BC Operation Table

	Logic Inputs			Line		Logic Outputs	
Mode	**Drive Enable**	**$\overline{\text{Receive Enable}}$**	**$\overline{\text{Signal}}$**	**Output (Transmit) CT-CR**	**Input (Receive) CT-CR**	**PRP**	**NRP**
Transmit Mode	H	H	L	+1.3 to +1.7V	—	T	T
	H	H	H	−1.7 to −1.3V	—	T	T
Receive Mode	L	L	X	—	≥ +1.0V	1	0
	L	L	X	—	≤ −1.0V	0	1
	L	L	X	—	−0.2V to +0.2V	0	0

T = Tristated (disabled) output
X = Don't care

Fig. 6 - LB1024BC Dual Digital-Signal Transceiver Application Diagram



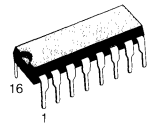
LB1025

PRELIMINARY DATA

AN AT&T PRODUCT

QUAD BUS TRANSCEIVER

- FOUR INDEPENDENT TRANSCEIVERS
- LOW OUTPUT CAPACITANCE (< 6pF TO BUS)
- SIMULTANEOUS RECEIVE/TRANSMIT ENABLING OF ALL TRANSCEIVERS
- TTL COMPATIBLE INPUTS
- TRISTATE RECEIVER OUTPUTS
- RECEIVER INPUT HYSTERESIS
- DRIVER OUTPUT HIGH IS 75mA
- 5V SUPPLY VOLTAGE



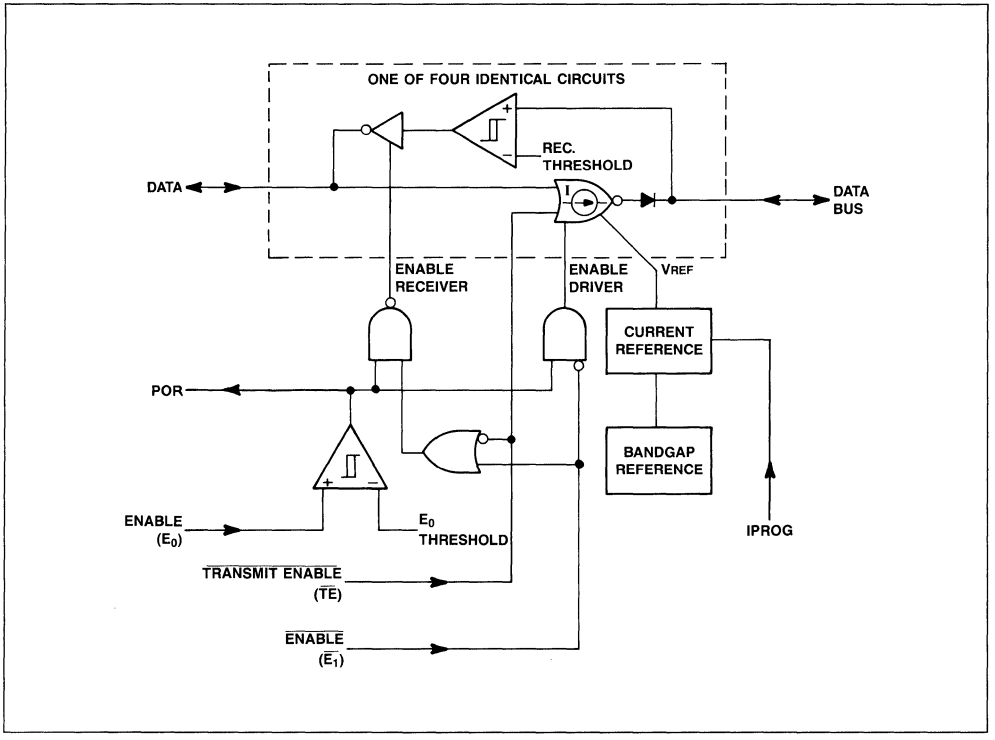
DIP-16 A Plastic

ORDERING NUMBER: LB1025AC

Each transceiver will interface a tristate bus with a large, low-impedance party-line bus. It has current source drive to the party-line bus and maintains tains a high-impedance load to this bus under all conditions.

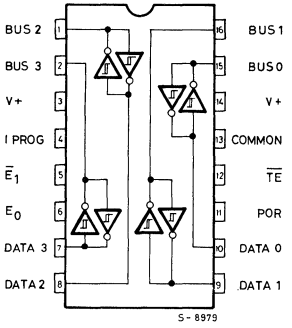
All receivers have tristate outputs and therir inputs have built-in hysteresis to improve noise control. Fail-safe design ensures that transmit is disabled when the enable pins are open.

Fig. 1 - Functional Diagram



LB1025

PIN CONFIGURATION



PIN DESCRIPTIONS

Description	Name
Data 1 Data 2 Data 3 Data 4	Data inputs/outputs. These pins connect to the input/output terminals of user defined equipment (computers and computer peripherals, instrumentation equipment, etc.).
Bus 0 Bus 1 Bus 2 Bus 3	Bus transmission line inputs/outputs. These pins are the inputs for the "receive" operation and the outputs for the "transmit" operation.
V+	External supply voltage (+4.75V to 5.25V). The supply voltage pins (3 and 14) are internally connected together.
COMMON	Circuit common (not necessarily physical or system ground).
E_0 $\overline{E}_1$	Enable (zero) and Enable (one). See TABLE 1 for logic programming of these pins.
$\overline{TE}$	Transmit/Receive control input. See TABLE 1 for logic programming of this pin.
POR	Power on reset. A non-inverting buffered signal of the E_0 input may be obtained from this pin.
IPROG	This pin can be programmed to vary driver output currents for test purposes only. This pin should be connected to V+ for all applications.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Operating Voltage (all pins)	5.5	V

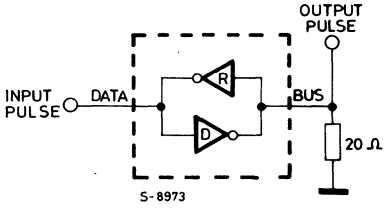
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified)

	Parameters	Test Conditions		Min	Typ	Max	Unit
Driver Section	Input Voltage		High-level	2.0	—	—	V
			Low-Level	—	—	0.8	
	Input Current		High-Level	—	−0.03	−40	μA
			Low-Level	—	−0.05	−0.2	mA
	Output Current		High-Level	−67.5	−75	−82.5	
			Low-Level	—	−20	−40	μA
Receiver Section	Input Threshold Voltage		High-to-Low	0.3	0.48	0.6	V
			Low-to-High	0.5	0.76	1.1	
	Hysteresis Voltage			200	270	500	mV
	Output Voltage		High-Level	2.4	4.05	—	V
			Low-Level	—	0.35	0.4	
	Input Current		High-Level	—	−7.0	−40	μA
			Low-Level	—	−20	−40	
	Output Current		Short-Circuit, Low-Level	15	50	150	mA
			Short-Circuit, High-Level	−15	−40	−150	
Logic Section	Input Voltage		$\overline{TE}$ High-Level	2.0	—	—	V
			$\overline{TE}$ Low-Level	—	—	0.8	
			E_0 Low-to-High	2.75	2.96	3.5	
			E_0 High-to-Low	1.75	2.1	2.5	
	Hysteresis Voltage		E_0 Input	0.5	0.85	1.5	
	Input Current	$V_{IN} = 3.0V$	$\overline{TE}$ High-Level	—	−0.03	−20	μA
			$\overline{E}_1$ High-Level	—	−0.01	−20	
			E_0 High-Level	—	−0.1	−5.0	
		$V_{IN} = 0.4V$	$\overline{TE}$ Low-Level	—	−0.07	−0.4	mA
			$\overline{E}_1$ Low-Level	—	—	−0.4	
		$V_{IN} = 0.2V$	E_0 Low-Level	—	−1.4	−4.0	μA
Propagation Delay Time	Driver	See Figures 2 and 4	Low-to-High	—	9.0	40	ns
			High-to-Low	—	16	40	
	Receiver	See Figures 3 and 5	Low-to-High	—	30	45	
			High-to-Low	—	16	40	
	$\overline{TE}$ to Driver		High-to-Low	—	20	50	
			High-to-Low	—	28	50	
	$\overline{TE}$ to Receiver		Low-to-High	—	40	60	
Power Supply	Current (Maximum)			—	380	500	mA
	Current (Quiescent, Idle)			—	65	90	

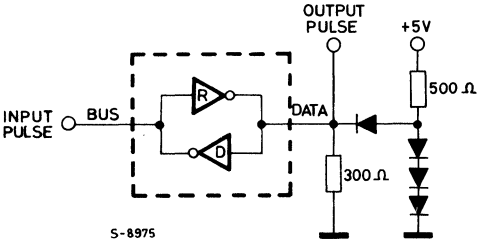
TEST CIRCUITS

Fig. 2 - Driver Test Circuit



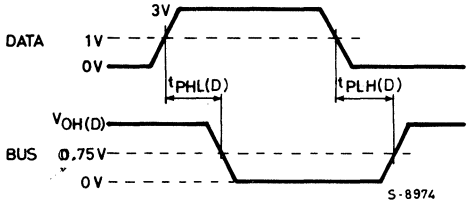
$\overline{T_E} = L$
$\overline{E_I} = L$
$E_O = H$
$V+ = +5V$

Fig. 3 - Receiver Test Circuit



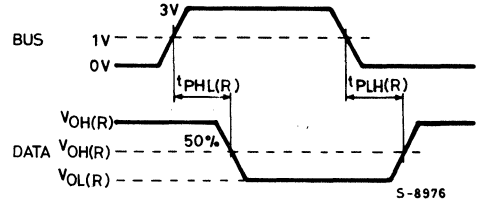
$\overline{T_E} = H$
$\overline{E_I} = L$
$E_O = H$
$V+ = +5V$

Fig. 4 - Driver Timing Waveform



$t_r = t_f = 10ns$
Pulsewidth = 100ns

Fig. 5 - Receiver Timing Waveform



$t_r = t_f = 10ns$
Pulsewidth = 100ns

APPLICATION

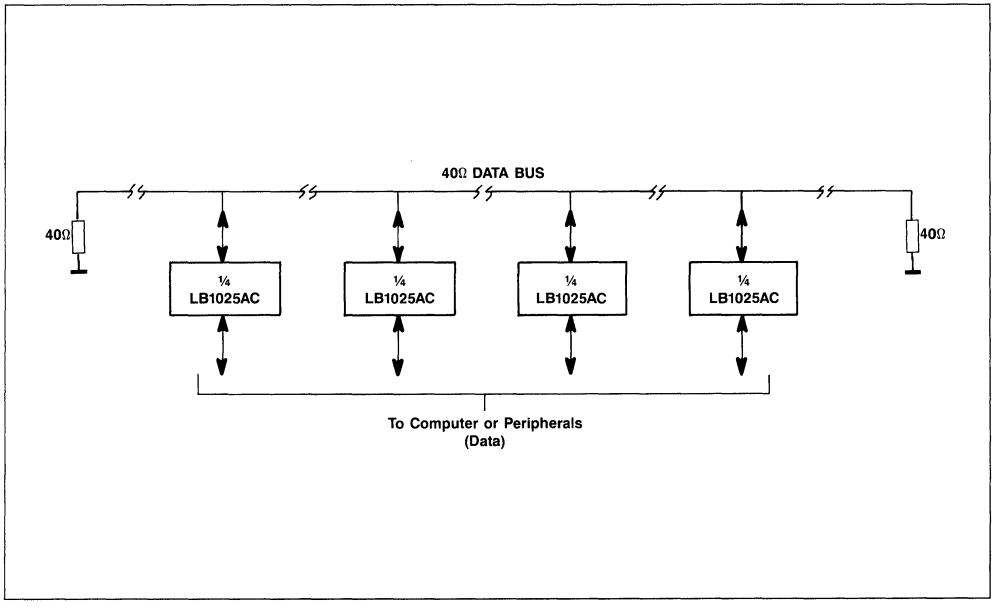
Table 1 gives the logic information necessary for the operation of the LB1025AC Transceiver. Figure 8 is typical application of the Quad Bus Transceiver. This diagram ilustrates the device when used as an interface between a 40 ohm party line bus and a computer or peripherals.

Table 1 - LB1025AC Truth Table

$\overline{TE}$	E_0 (note 1)	$\overline{E}_1$	Information Flow	Operation
0	0	0	Bus-Data	Receive
1	0	0	Bus-Data	Receive
0	1	0	Data-Bus	Normal Transmit
1	1	0	Bus-Data	Normal Receive
0	0	1	Bus-Data	Receive
1	0	1	Bus-Data	Receive
0	1	1	Isolate	Disable Device
1	1	1	Isolate	Disable Device

Note 1. E_0 is generally low only during the power-on-state. During the power-on-state, the transceiver default into the "Receive" state until the voltage at E_0 exceeds 3 volts.

Fig. 6 - LB1025AC Quad Bus Transceiver Application Diagram



LB1026

PRELIMINARY DATA
AN AT&T PRODUCT

LEVEL EXPANDER

- REDUCES BACKGROUND NOISE DURING PAUSE IN CONVERSATION
- LB1026AA SUPPLIED WAFER FORM
- LB1026AB SUPPLIED IN MINIDIP

The LB1026 functions as a voice-frequency level expander that is used to condition amplified signals from electret-type microphones. A characteristic of this level expander is to attenuate low-level signals from the microphone that typically originate from background room noise, while passing normal amplitude speech at unity gain. The end effect of using this device is that the quality of the conversation is enhanced, for both the talker (via receiver sidetone) and listener, by reducing background sounds that might be heard during periods when the talker is silent.
This device operates from a single 2 to 15 V power supply and must be ac-coupled at the input and output. In addition, a 1.0μF response-time control capacitor must be provided by the user if the specified attack and release times are to be obtained. The LB1026 may be supplied in wafer form to the customer who is then responsible for subsequent processing to obtain the usable device. Each chip has six pads for wire bond attachment (see outline drawing).

Minidip-A Plastic

ORDERING NUMBERS: LB1026AA
LB1026AB

PIN CONFIGURATION

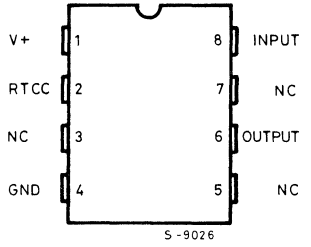
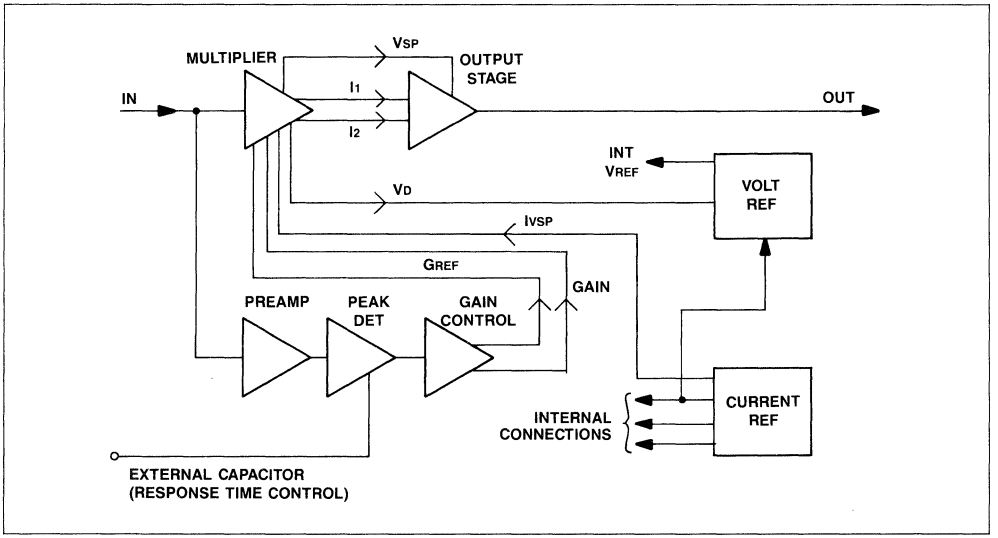


Fig. 1 - Block Diagram



PAD & PIN DESCRIPTION

Pad	Pin	Symbol	Description
1	1	V+	Connection for the power supply voltage.
6	2	RTCC	Response Time Control Capacitor.
	3	NC	No Connection, should not be used as a tie point.
15	4	GND	Ground.
	5	NC	No Connection, should not be used as a tie point.
16	6	OUTPUT	Device output.
22	7	GND	This pin can be connected to ground. This connection is not to be considered the ground terminal for this device.
21	8	INPUT	Device input.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Voltage (on Pads 1, 15, 22)	25	V
Storage Temperature Range	−40 to +125	°C
Ambient Operating Temperature Range	0 to 50	°C
Pin Temperature (Soldering 15 sec)	300	°C

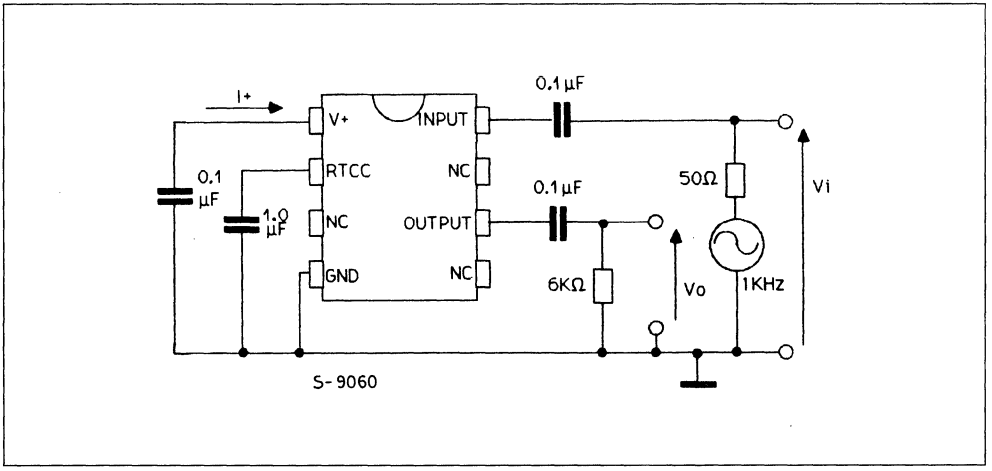
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (At 25°C unless otherwise specified see test fig. 2)

Parameter	Test Conditions	Min	Max	Unit
Power Supply Voltage		2.0	15	V
Power Supply Current	V+ = 15V	—	1.0	mA
Power Supply Current	V+ = 3.0V	—	700	μA
Output Voltage	R_L = 6KΩ	—	1.0	V_{PP}(1)
Maximum Input Gain Ratio(3)	Input = 388mVrms	0.94	1.15	
High-Level Gain Ratio(3)	Input ≥ 50mVrms	0.94	1.1	
Mid-Level Gain Ratio(3)	Input = 12.5mVrms	0.38	0.6	
Low-Level gain Ratio(3)	Input = 1.0mVrms	0.19	0.28	
Attack Time		10.5	17.5	ms(2)
Decay Time		105	175	

1. Maximum undistorted sine-wave.
2. Attack and decay times are defined as the time required for the output to settle to within 90% of the values shown in Figure 2 after the input is instantaneously changed from 3.16mV_{RMS} respectively. For this specific response, a 1.0μF capacitor must be connected from lead number 6 of the device to ground in addition to the normal input, output and supply connections. These response times are not directly measured, but are guaranteed by desing.
3. Gain Ratio are defined as V_O/V_I

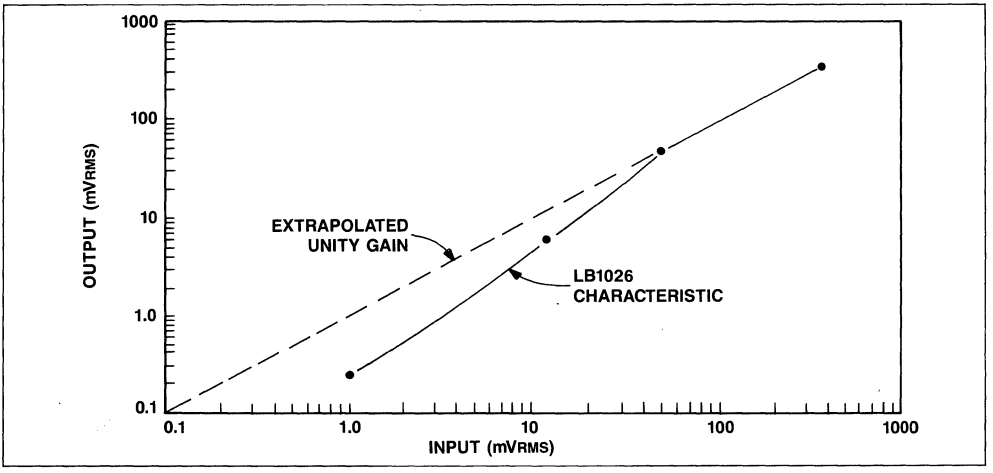
Fig. 2 - Test Circuit



APPLICATIONS

The following information summarizes the basic operation of a voice frequency level expander in electret-type microphone applications.

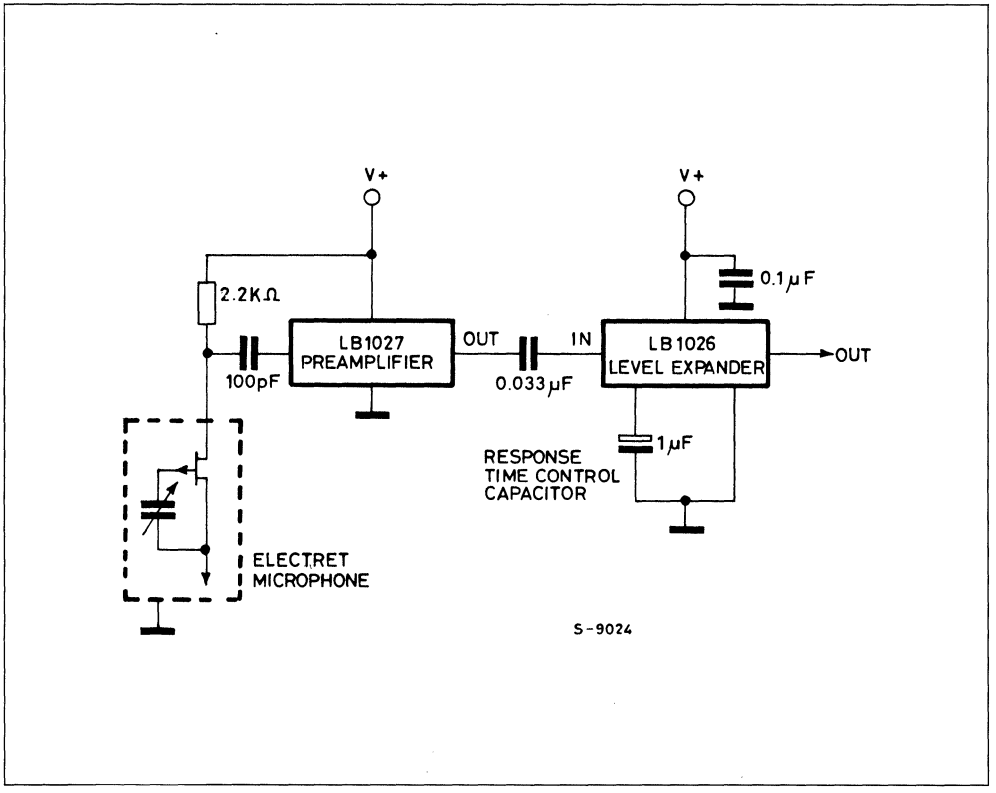
Fig. 3 - Typical Expander Characteristics



Attack and decay times are defined as the time required for the output (V_O) to settle within 90% of the valued (output mVrms, Figure 3) after the input is istantaneously changed from 3.16 mVrms to 31.6 mVrms or from 31.6 mVrms to 3.16 mVrms, respectively. For this specific response, a 1.0 μF capacitor mus be connected from pin 2 of the device to ground in addition to the normal input, output, and supply connections.

APPLICATIONS (Continued)

Fig. 4

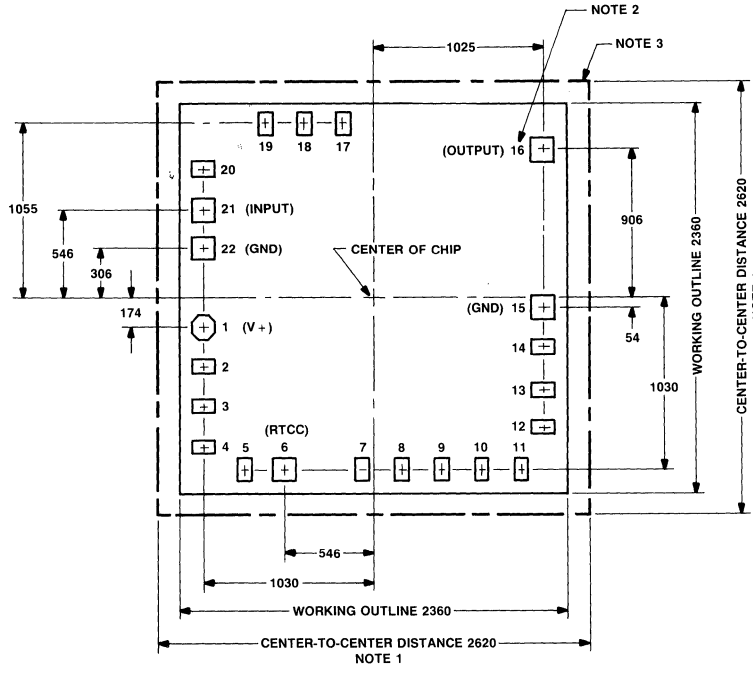


MOUNTING AND CONNECTION

Epoxy bonding is the preferred method of attaching the chip to the substrate.
Thermo-compression bonding is the preferred method of attaching gold wire to the device contact.

Use minimum pressure during bonding. Bonding temperature shall not exceed 340°C
Care shall be taken during wire-to-contact bonding so as not to damage the device.

OUTLINE DRAWING



NOTES:

All dimensions are reference dimensions and are shown in micrometers.

1. The actual chip size equals the center-to-center dimensions less the saw kerf width, typically 50 to 70 micrometers
2. Chip pad location numbers are for reference only and do not appear on the chip. The complete metallization pattern is not shown.
3. The thickness may vary as determined by the wafer diameter used in fabrication. However, the thickness dimension will be in the range of 480 micrometers (.0189 inches) minimum and 700 micrometers (.0275 inches) maximum.

LB1027

PRELIMINARY DATA

AN AT&T PRODUCT

ELECTRET PREAMPLIFIER

- INPUT IMPEDANCE OF 125MΩ (IN PARALLEL WITH 2.5 pF)
- LOW QUIESCENT CURRENT (< 327 μA at 4V)
- AC VOLTAGE GAIN OF 18 dB
- 600 mV PEAK-TO-PEAK OUTPUT VOLTAGE SWING
- TYPICAL OUTPUT RESISTANCE OF 50Ω
- AVAILABLE IN WAFER FORM
- INQUIRE ABOUT 8-PIN DIP AVAILABILITY

The LB1027 is a voice-frequency preamplifier specifically designed for electret microphone applications. This device operates from a supply voltage of 15 volts down to 1.1 volts (with some performance reduction below 1.6 volts).
The LB1027 is supplied in wafer form to the customer who is then responsible for subsequent processing to obtain a usable chip. Each chip has four pads for wire-bond attachment (see outline drawing).

ORDERING NUMBER: LB1027AA

Fig. 1 - Simplified Schematic

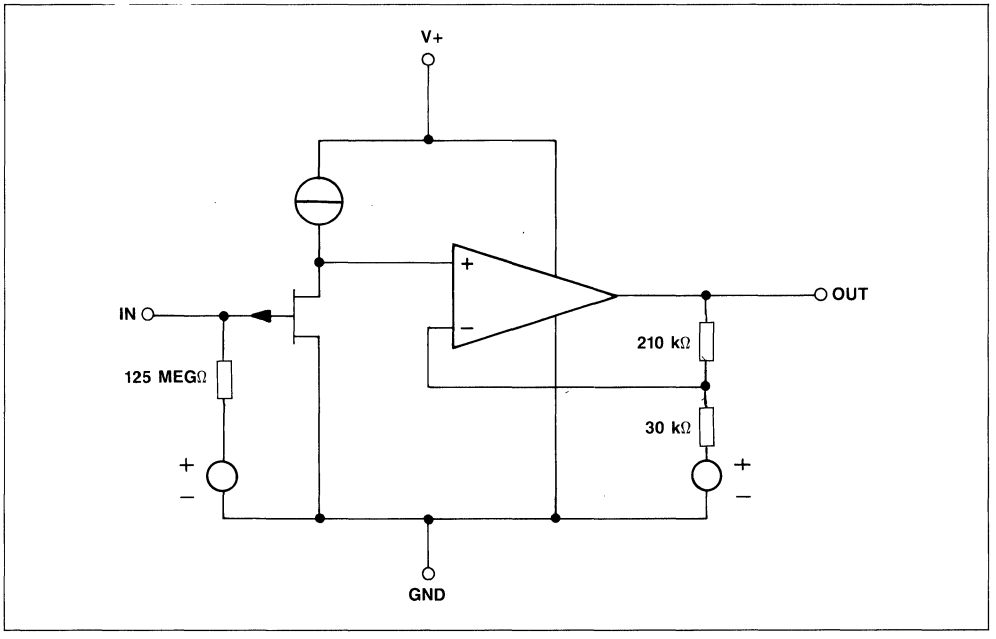
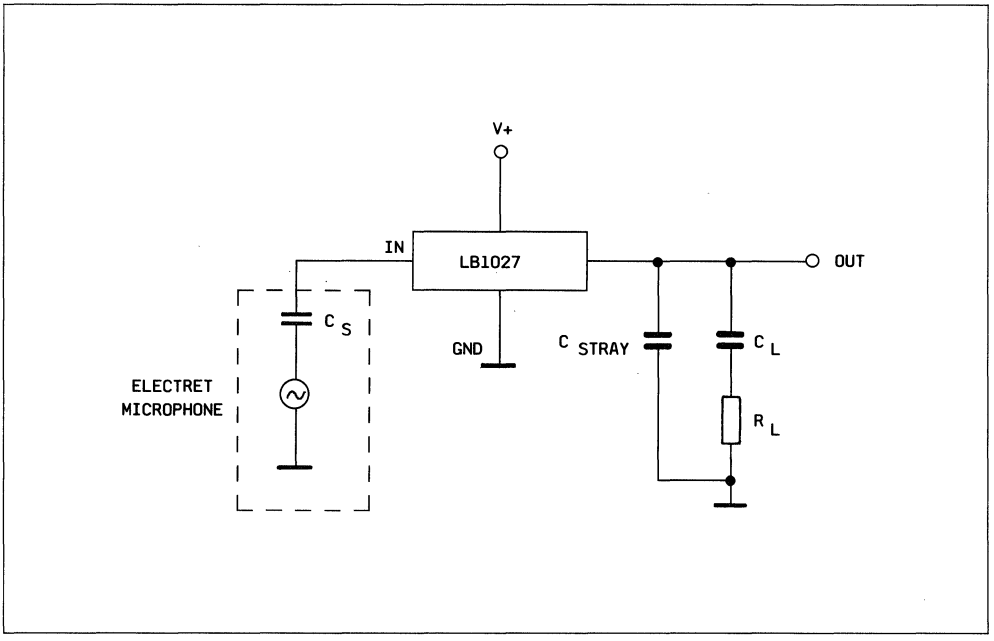


Fig. 2 - Simplified Diagram, Source and Load Requirements



PAD DESCRIPTION *(Refer to Fig. 11)*

Pad N°	*Name*	*Description*
2	*V+*	*Positive-Supply Voltage*
4	*GND*	*Ground*
3	*IN*	*Input (See Source Requirements below)*
1	*OUT*	*Output (See Load Requirements below)*

Source Requirements (See Figure 2)
The LB1027 is optimized (for PSRR) where $C_S = 12$ pF, but will work with any value consistent with its input impedance. The low-frequency roll-off point is determined by C_S. Direct current into the input should be ± 20 pA. The LB1027 is designed for ac input signals less than 20 mV peak-to-peak (low-frequency response may degrade with larger input peaks). Signals greater than 70 mV peak-to-peak may be asymmetrically clipped.

Load Requirements (See Figure 2)
C_L can be any value consistent with the desired output low-frequency roll-off characteristics. Values of C_S, R_L, maximum signal frequency and output voltage swing must be chosen so as not to exceed the LB1027 output drive current capability (+80 μA, −250 μA).
The LB1027 will output a 600 mV p-p signal to >4 kHz without clipping or slew-rate limiting (when $R_L = 10k$ and $C_{STRAY} \leqslant 5000$ pF). It is recommended that C_{STRAY} not exceed 5000 pF in any event.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	−20 to +70	°C
Storage Temperature Range	−40 to +125	°C
Power Dissipation	100	mW
Voltage (V+ to GND)	18	V
Input Current	±10	μA
Output Current	±1	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply Current	V+ = 1.5V	160	—	350	μA
	V+ = 4.0V	160	230	327	
	V+ = 15V (See Fig. 3)	160	—	350	
DC Output Currents	Positive Drive; V_{IN} = 1.5V, V+ = 4.0V	80	110	—	μA
	Negative Drive; V_{IN} = 0.9V, V+ = 4.0V (See Fig. 4)	−250	−430	—	
DC Quiescent Output Voltage	V+ = 1.6V	0.32	0.40	0.9	V
	V+ = 4.0V	0.35	0.55	1.05	
	V+ = 15V (See Fig. 5)	0.35	0.80	1.20	
DC Output Voltages	Positive Swing; V_{IN} = 1.5V, V+ = 4.0V	1.5	—	—	V
	Negative Swing; V_{IN} = 0.9V, V+ = 4.0V (See Fig. 6)	—	—	0.1	
AC Voltage Gain	f = 1KHz, C_{IN} = 1000pF, V_{IN} = 14mVrms NOTE: Circuit frequency response is flat to within ±0.5dB (DC to 10KHz) (See Fig. 7)	16.8	18.0	19.3	dB
Input Impedance	Resistive	—	125	—	MΩ
	Capacitive (Capacitive source = 12pF)	—	2.5	—	pF
Output Resistance		—	50	—	Ω
Low Frequency Response (−3 dB point)	Capacitive Source = 12pF (See Fig. 8)	—	80	—	Hz

RECOMMENDED OPERATING CHARACTERISTICS (at 25°C)

Max Supply Voltage (V+)	15	V
Min Supply Voltage (V+)	1.1	V

TEST CIRCUITS

Fig. 3 - Power Supply Current

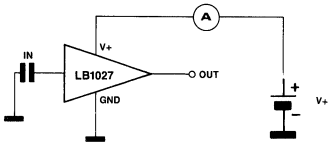


Fig. 4 - DC Output Current Drive

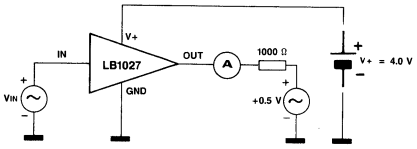


Fig. 5 - DC Quiescent Output Voltage

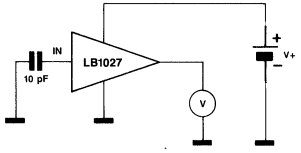


Fig. 6 - DC Output Voltage Swing

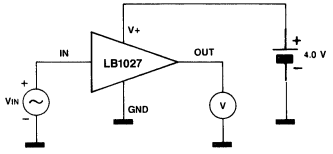


Fig. 7 - AC Voltage Gain

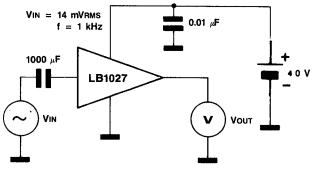
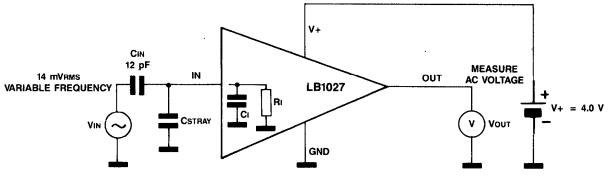
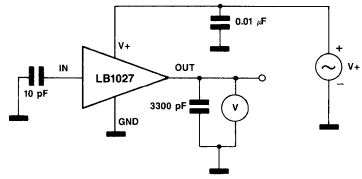


Fig. 8 - Low Frequency −3 dB Point



TEST CIRCUITS (Continued)

Fig. 9 - Stability Check. With V+ = 1.5, 4.0 and 15.0 V, measure AC output voltage with 3dB bandwidth ⩾500 KHz. No oscillation should be detected.



APPLICATIONS

The following simplified diagram summarizes the requirements for optimized operation of the LB1027AA electret preamplifier.

Fig. 10 - Electret Preamplifier Application Diagram

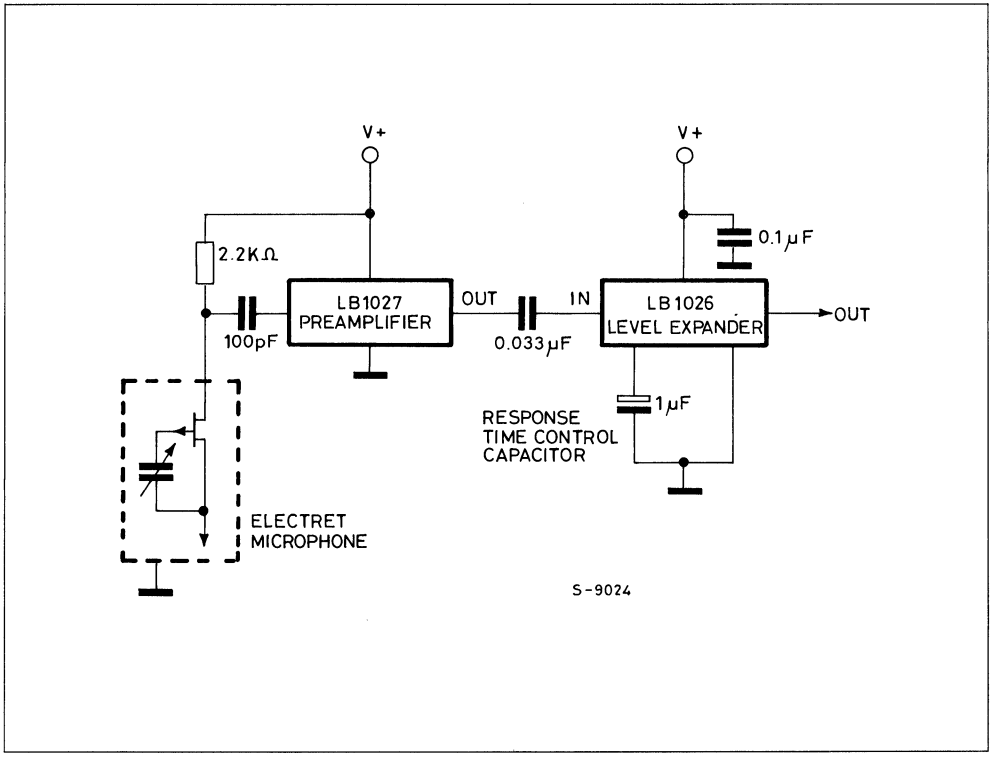
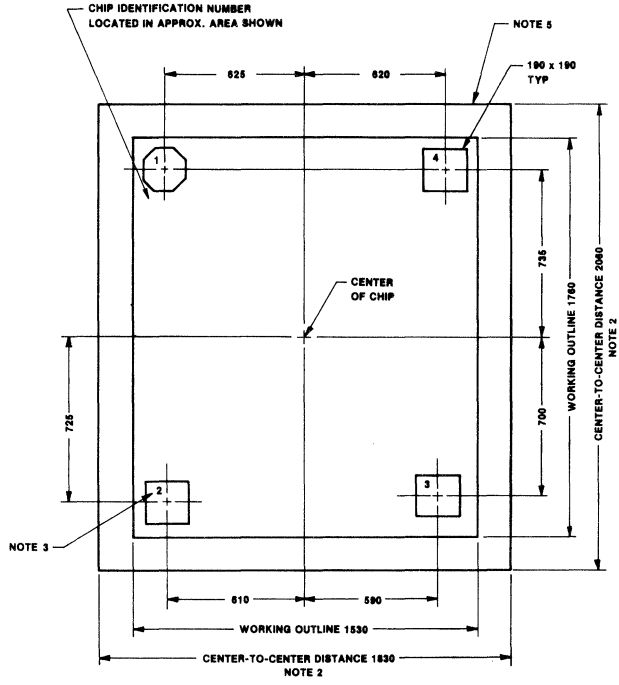


Fig. 11 - Outline Drawing



1. All dimensions are reference dimensions and are shown in micrometers
2. The actual chip size equals the center-to-center dimension less the saw kerf width. Typically 50 to 70 micrometers
3. Chip pad numbers are for reference only and do not appear on the chip
4. The complete metallization pattern is not shown.
5. The thickness may vary as determined by the wafer diameter used in fabrication. However, the thickness dimension will be in the range of 480 micrometers (.0189 inches) minimum and 700 micrometers (.0275 inches) maximum.

MOUNTING AND CONNECTIONS

This device is susceptible to damage as the result of electrostatic discharge. Proper precautions should be taken to eliminate exposure to electrostatic charge during handling by individuals and/or in automatic equipment.
Epoxy bonding is the preferred method of attaching the chip to the substrate.

Thermo-compression bonding is the preferred method of attaching gold wire to the device contact. Use minimum pressure during bonding. Bonding temperature shall not exceed 340°C.
Care shall be taken during wire-to-contact bonding so as not to damage the device.

LBR Family

PRELIMINARY DATA

AN AT&T PRODUCT

VOLTAGE REGULATOR CIRCUIT FAMILY

VOLTAGE REGULATOR

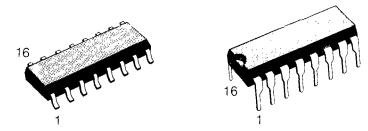
- FIXED VALUES BETWEEN 2V & 24V
- LESS THAN 1% CHANGE OVER COMBINED TEMPERATURE AND POWER SUPPLY VOLTAGE RANGES:
- POWER SUPPLY VOLTAGE MUST BE AT LEAST 2V GREATER THAN REGULATOR OUTPUT VOLTAGE

PRECISION LOW-VOLTAGE REFERENCE

- 1.25 (±1%) OVER ENTIRE POWER SUPPLY RANGE
- TEMPERATURE COEFFICIENT <50ppm/°C (−40 TO +100°C)
- 4 VOLT MINIMUM POWER SUPPLY
- DRIVE UP TO 100 pF
- OUTPUT CURRENT UP TO 10mA
- 40 dB PSRR @ 1 MHz
- FAST START-UP TIME

HIGH-SPEED COMPARATOR

- REFERENCED TO 1.25V
- PROPAGATION DELAY <150 nsec
- INPUT OFFSET <5mV
- OUTPUT CURRENT TO 5mA



16 Pin Surface Mount. DIP-16 C Plastic

8 Pin Surface Mount. Minidip C Plastic

The Regulation Control Circuit Family consists of integrated circuits which provide three main functions in the same package: a voltage regulator, a precision 1.25V reference, and a high-speed comparator. Each device accepts an unregulated DC supply voltage ranging from 4V to 26V and provides two fixed outputs: a 1.25V reference voltage, common to each device code in this family; and a customer specified regulation voltage, ranging from 2V to 24V, fixed at time of manufacture. Refer to Ordering Information (last page) for a detailed listing of existing codes. Other codes for regulation voltages within the specified limits are available upon request.

Fig. 1 - Functional Diagram - 16 Pin DIP - 16 Pin Surface Mount

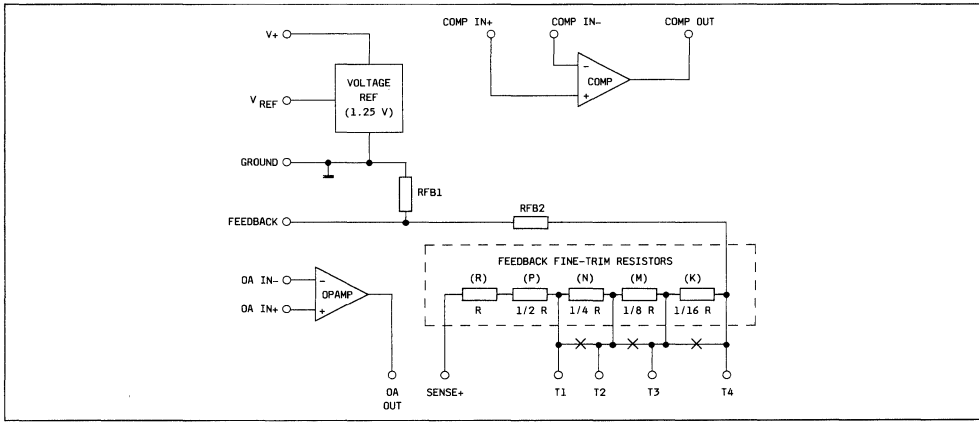
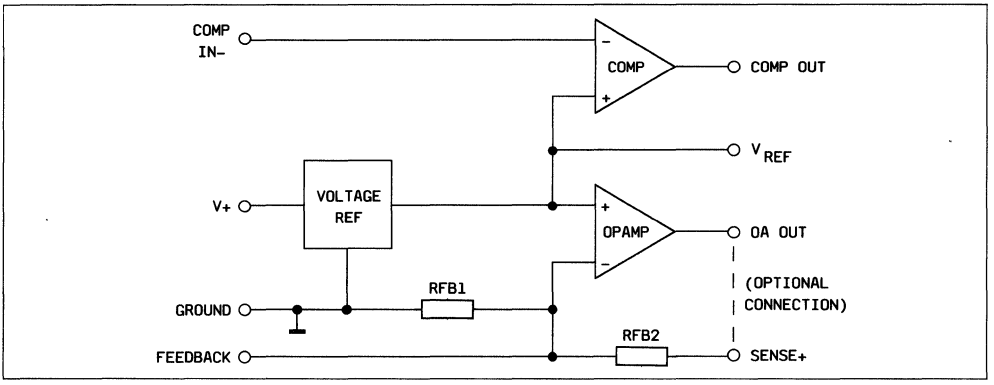
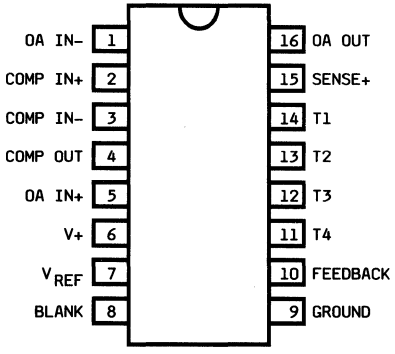


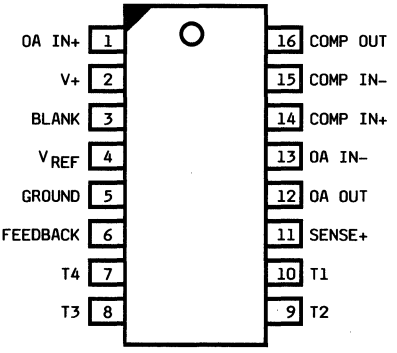
Fig. 2 - Functional Diagram - Minidip - 8 Pin Surface Mount



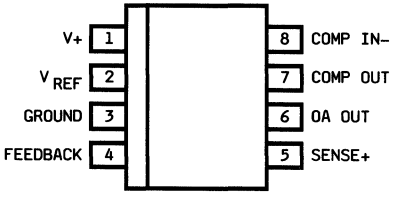
PIN CONFIGURATION



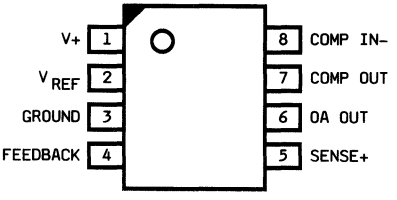
16 Pin Surface Mount



16 Pin Plastic DIP



8 Pin Surface Mount



Minidip Plastic

PIN DESCRIPTION

Name	Description
V+	Supply Voltage (4 to 26V)
BLANK	This pin may be used as a tie-point for external components. Maximum Voltage = 30V
GROUND	Circuit common (not necessarily system or physical ground).
V_{REF}	1.25 V Reference Output.
COMP IN−	Inverting Comparator Input.
COMP IN+	Non-Inverting Comparator Input. Connected to V_{REF} on 8-Pin Packages.
COMP OUT	Comparator Output, Open Collector. Requires Pull-up resistor.
OA IN−	Inverting Op-Amp Input. Connected to FEEDBACK on 8-Pin Packages.
OA IN+	Non-Inverting Op-Amp input. Connected to V_{REF} on 8-Pin Packages.
OA OUT	Op-Amp Output.
FEEDBACK	Connection to feedback resistors. Connected to inverting Op-Amp input on 8-Pin Packages.
SENSE+	Positive Sense Node. Normally connected to inverting Op-Amp Out in regulator applications.
T1 T2 T3 T4 (See Fig. 1)	These trim links are normally factory trimmed as required to provide the desired voltage regulator output. Howerver, some applications may require additional fine-turned trimming to account for offset voltages in customer systems. Devices can be ordered which are trimmed to a value withing several millivolts of a customer's desired value. The customer is then responsible for final trimming. (This option not available in 8-Pin Packages).

ABSOLUTE MAXIMUM RATINGS (At 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V+	Supply Voltage	30	V
T_A	Ambient Operating Temperature Range	−40 to 100	°C
T_{stg}	Storage Temperature Range	−55 to 125	°C
—	Pin Temperature (Soldering, 15 Sec.)	300	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS* ($T_A = 25°C$ unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Standby Current Drain	V+ = 26V (See Fig. 3)	—	3.7	4.5	mA
V_{REF}, Set Point	I_{REF} = 10mA (See Fig. 3)	1.238	1.250	1.262	V
ΔV_{REF} (Load Regulation)	S2 switched from A to B (See Fig. 3)	—	±3	±8	mV
ΔV_{REF} (Line Regulation)	V+ = Default; V+ = 26V (See Fig. 3)	—	±3	±6	
ΔV_{REF} (Temperature Regulation)	T_A = −40°C to +25°C (See Fig. 3)	—	±3	—	
ΔV_{REF} (Temperature Regulation)	T_A = +25°C to 100°C (See Fig. 3)	—	±3	—	
V_{REF}, Power Supply Rejection Ratio	DC 1 MHz	— —	70 40	— —	dB
V_{REF}, Transient Start-Up Times	I_{REF} = 1mA I_{REF} = 5mA I_{REF} = 10mA	— — —	2 15 150	— — —	μsec
Comparator, Input Offset Voltage	T_A = 25°C	—	±1	±5	mV
Comparator, Output (LOW)	V_{BIAS} = 1.350V (See Fig. 3)	—	235	500	
Comparator, Output (HIGH)	V+ = 26V (See Fig. 3)	25	—	26	V
Comparator, Transient Response Times	Turn-on Time Turn-Off Time Rise Time Fall Time	— — — —	105 25 20 50	— — — —	nsec
Op-Amp, Input Offset Voltage	T_A = 25°C	—	±1	±5	mV
Op-Amp, PSRR	DC	—	100	—	dB
V_{SENSE}, Voltage Tolerance	V_{SENSE} Reference = Manufacturer's Coded Value (See Fig. 3)	−1	—	+1	%
ΔV_{SENSE} (Load Regulation)	S1 switched from A to B (See Fig. 3)	—	±0.05	±0.2	

* Conditions, as shown in the appropriate test Circuit Figure, are referred to as "Default" conditions.

Notes:

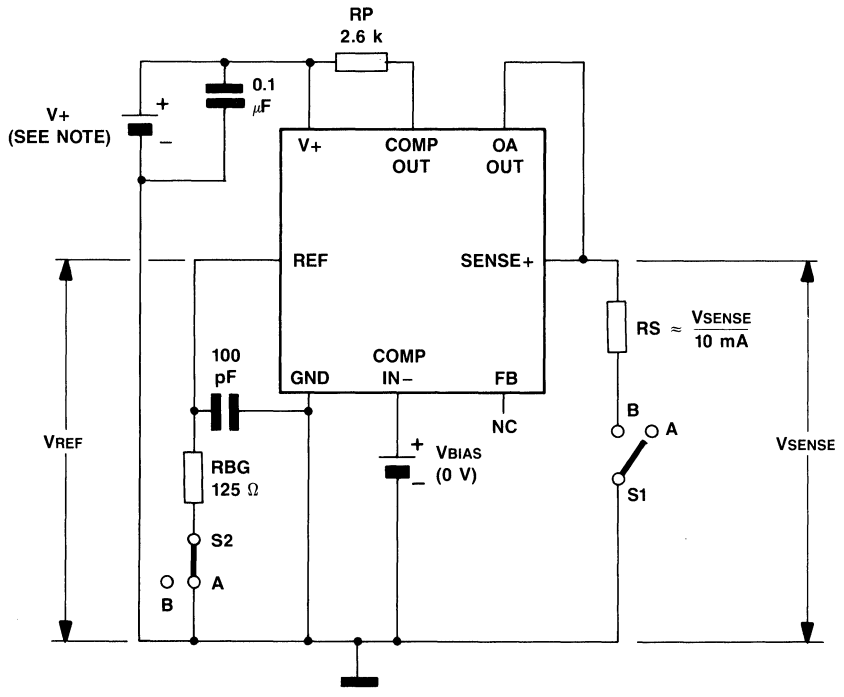
1. When certain pins are not being used, they should be connected as follows for the 8-Pin devices:
   a. COMP IN− to GND (when comparator is not used)
   b. OA OUT to FEEDBACK (when Op-Amp is not used)
   c. SENSE+ should float (when Op-Amp is not used)
2. When certain pins are not used, they should be connected as follows for the 16-Pin devices:
   a. When the comparator is not used, connect COMP IN+ to V_{REF} and COMP IN− to GND.
   b. When the Op-Amp is not used, connect OA OUT to OA IN− and OA IN+ to V_{REF}.
3. This characteristic excludes the current flowing in the feedback resistors. Feedback current must be calculated for each voltage regulator value.
4. Specific available V_{SENSE} output levels are listed with Ordering Information on the last page.
5. OA OUT is connected to SENSE+.
6. OA OUT is disconnected from SENSE+.
7. This is the minimum supply voltage which is required to assure that V_{REF} has stabilized at any specific temperature within the specified temperature range.
8. Supply voltage (V+) minus a nominal 2.5V yelds high CMVR.

RECOMMENDED OPERATING LIMITS (−40 to 100°C)

Parameter	Value	Unit
V_{REF} Current Load, Maximum	10	mA
V+ Voltage Minimum	4	V
V+ Voltage Maximum	26	V
Comparator Output Sink Current, Maximum	10	mA
Op-Amp Output Source Current, Maximum	30	mA
Op-Amp Output Sink Current, Maximum	30	mA

TEST CIRCUITS

Fig. 3



NOTE: V+ should be set to V_{SENSE} (manufacturer's coded value) plus an additional 3 volts. All voltages and switch positions as shown in circuit above are referred to as "Default Conditions".

CHARACTERISTIC CURVES

Fig. 4 - Precision Low-Voltage Reference Start-Up Characteristics

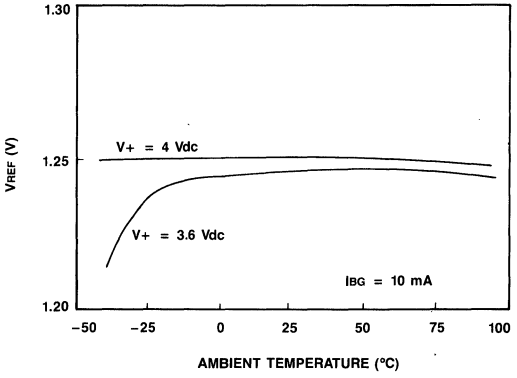


Fig. 5 - Precision Low-Voltage Reference Power Supply Rejection Ratio Frequency Characteristics

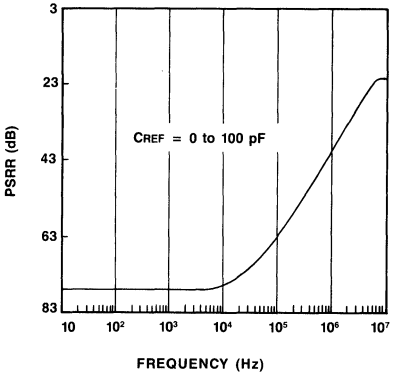


Fig. 6 - Precision Low-Voltage Reference Temperature Characteristics

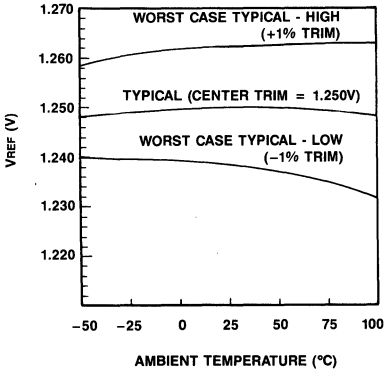
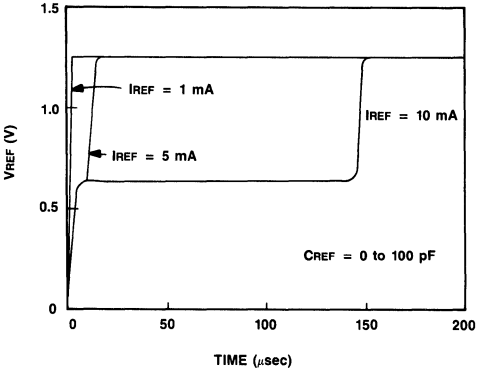


Fig. 7 - Precision Low-Voltage Reference Transient Start-Up Time



CHARACTERISTIC CURVES (Continued)

Fig. 8 - Typical Comparator DC Transfer Characteristics vs Temperature

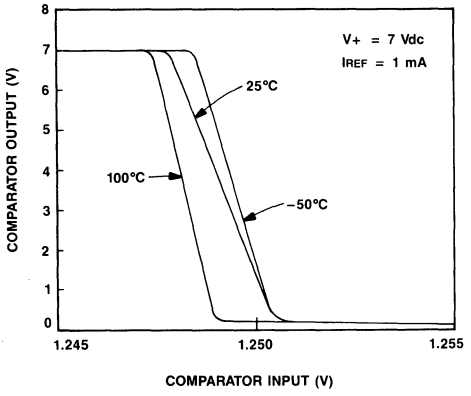


Fig. 9 - Typical Temperature Characteristics Comparator-Output Voltage vs Comparator Input Overdrive of 10mV

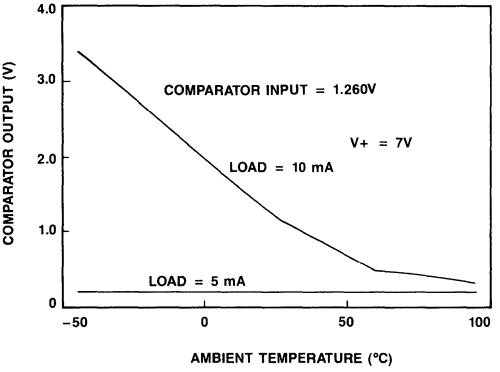


Fig. 10 - Typical Temperature Characteristics Comparator-Output Voltage vs Comparator Input Overdrive of 100mV

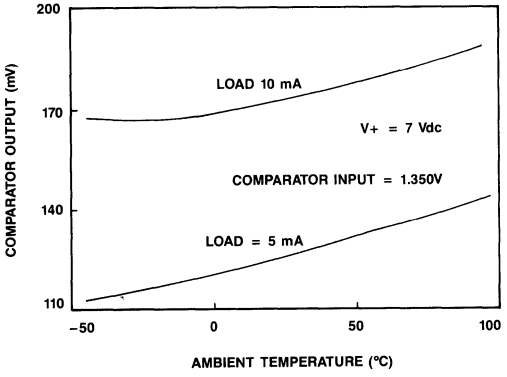
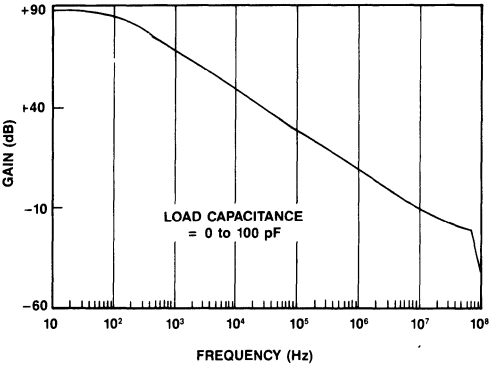


Fig. 11 - Op-Amp Open Loop Gain



APPLICATION

The Regulation Control Devices are used in power supply applications where the simultaneous use of all three functions (Voltage Regulator, High Speed Comparators, Precision Low-Voltage Reference) is a common practice. Application diagrams are shown below.

Fig. 12 - Regulation Control General Application Diagram

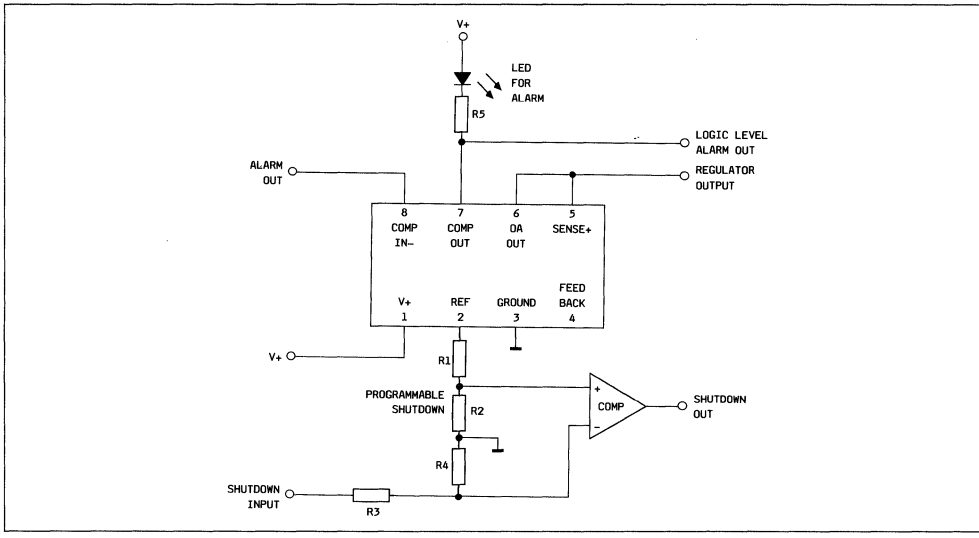
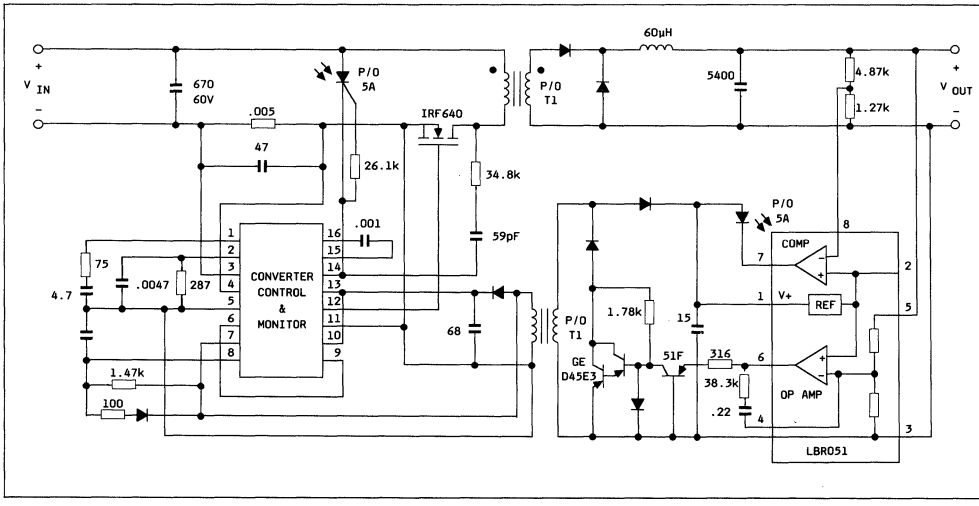
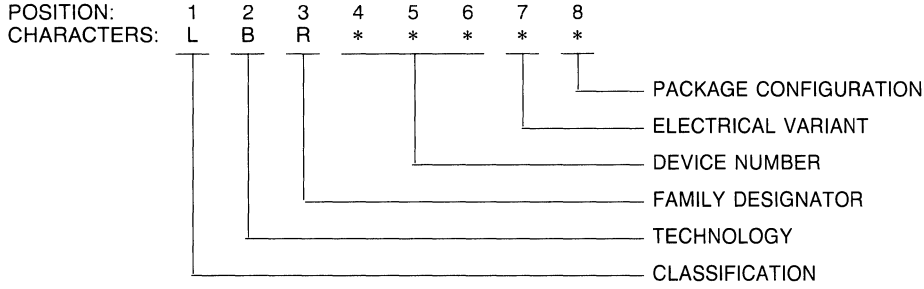


Fig. 13 - LB1001BB (5.1V Regulated Output) Used in DC-DC Converter Application (48V to 5V, 20A) (High Voltage Shutdown and Current Limiting)



ORDERING INFORMATION

The Regulation Control Circuit Family is coded as follow:



Classification (Position 1): L = Linear

Technology (Position 2): B = Complementary Bipolar Integrated Circuit (CBIC)

Family Designator (Position 3): Regulation Control Circuit Family.

Device Number (Positions 4, 5, 6): The device number is also the voltage value of the regulator function for this device. A decimal point shall be understood to exist between positions 5 and 6.

Example: 022 = 2.2V
220 = 22.0V

Electrical Cariants (Position 7) A = ±1% Regulator Voltage[1]
B = ±1.5% Regulator Voltage
C = ±2% Regulator Voltage

Package Variations (Position 8): A = Wafer ((8-Pad Chip)
B = Minidip
C = 16-Pin DIP
K = 16-Pin SOJ (Surface Mount)
S = 8-Pin SOIC (Surface mount)
X = Wafer (16-Pad Chip)

1. Regulator voltage output is SENSE + connected to OA OUT.

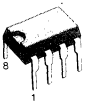
LH1016

ADVANCE DATA

AN AT&T PRODUCT

HIGH-VOLTAGE SOLID-STATE AC/DC RELAY

- HIGH-VOLTAGE MONOLITHIC INTEGRATED CIRCUIT FABRICATED IN A DIELETRIC ISOLATION PROCESS
- CAN SWITCH LOADS UP TO 400V AT CURRENTS UP TO 200mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- NO ELECTROMAGNETIC INTERFERENCE
- 3750V I/O ISOLATION (OPTICALLY COUPLED)
- GOOD dV/dT CAPABILITY
- HIGH-SURGE CAPABILITY
- NOISE-FREE OPERATION
- LOW-POWER CONSUMPTION

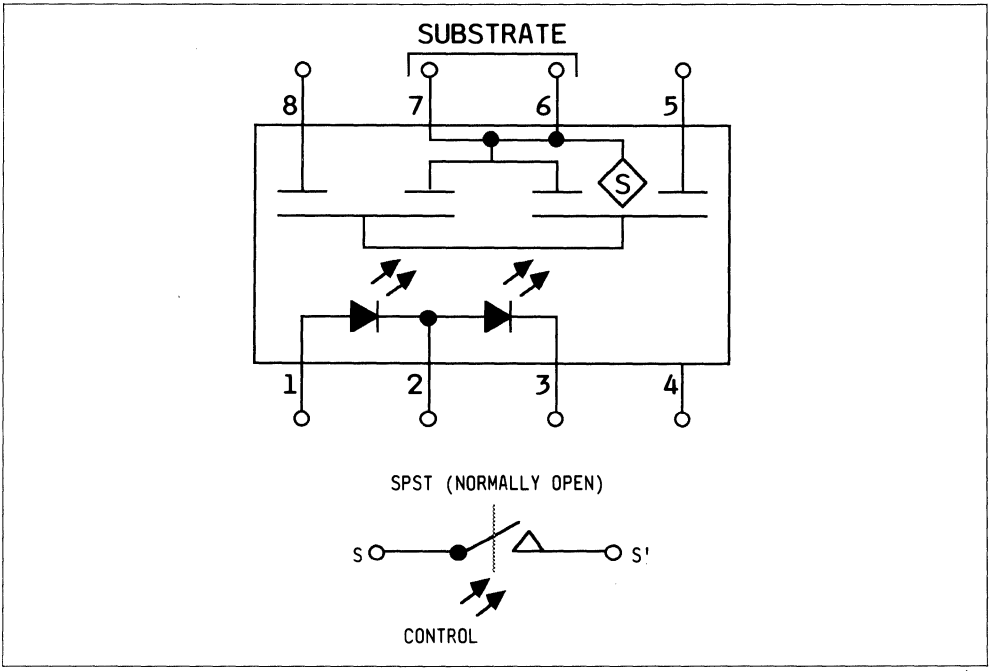


MINIDIP-D Plastic

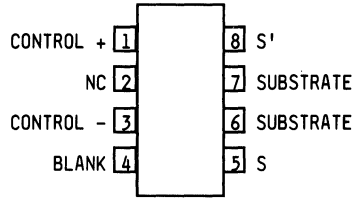
ORDERING NUMBER: LH1016AB

This solid-state device is a high-performance, optically controlled, AC/DC Relay. The LH1016 consists of two GaAlAs light-emitting diodes (LEDs) which optically couples the ON/OFF control signal to a dielectrically isolated high-voltage integrated circuit. The integrated circuit contains the high-voltage DMOS transistors and photosensitive drive circuitry. The optical isolation ensures excellent noise immunity with up to 3750 volts of isolation between input and output, while the LED control currents can be as low as 5.0mA. This makes the LH1016 suitable for logic control. Equivalent relay diagrams for this device is shown in Figure 1.

Fig. 1 - Functional and Equivalent Diagram



PIN CONFIGURATION



PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S, S',	These pins are the outputs.
NC	This pin is connected internally for test purposes. It should NOT be used as a tie-point for external components.
Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 150V.
Substrate	This pin should be left unconnected.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	–40 to +100	°C
Pin Soldering Temperature (t = 15 s max)	300	°C
Input/Output Voltage Isolation	3750	V
LED INPUT		
Continuous Forward Current	25	mA
Peak Forward Surge Current	250	mA
[Pulse width = 4.0ms, 10 pulses/s cycle (4%)]		
Reverse Voltage	20	V
OUTPUT, Continuous Current (RMS)	200	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Unit
OUTPUT POLE						
ON Resistance $R_{ON} = V_M/50mA$		$I_{LED} = 5mA$, $I_{LOAD} = \pm 50mA$ (See Fig. 2)	—	35	40	Ω
ON Voltage		$I_{LED} = 5mA$, $I_{LOAD} = \pm 200mA$ (See Fig. 2)	—	2.0	2.5	V
Breakdown Voltage		$I_{LED} = 0mA$, $I_{LOAD} = \pm 50\mu A$ (See Fig. 2)	400	—	—	
Surge Current		Non-Recurrent 1.0ms square wave $I_{LED} = 5.0mA$ (See Fig. 2)	4.0	—	—	A
Leakage Current		$V_{LOAD} = 400V$ $I_{LED} = 0mA$ (See Fig. 3)	—	—	20	μA
		$V_{LOAD} = 100V$ $I_{LED} = 0mA$ (See Fig. 3)	—	0.5	—	
Switching Time	TURN ON	$V_M = \pm 150V$ $R_L = 15K\Omega$ (See Fig. 4)	—	—	1.2	msec
	TURN OFF	$V_M = \pm 150V$ $R_L = 15K\Omega$ (See Fig. 4)	—	—	0.8	
INPUT CONTROL						
LED Forward Voltage		Forward Current = 10mA	1.17	—	1.43	V
LED Breakdown Voltage		Reverse Current = 10μA	10	—	—	
LED Reverse Leakage Current		Reverse Voltage = 10V	—	—	10	μA
LED Continuous Forward Current:			(See Absolute Maximum Rating)			
Recommended Forward Current for ON-State Operation:			—	5.0	—	mA

TEST CIRCUITS

Fig. 2 - R_{ON}, ON Voltage and Breakdown Voltage

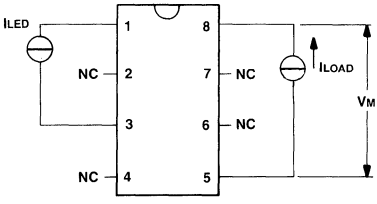


Fig. 3 - Leakage Current

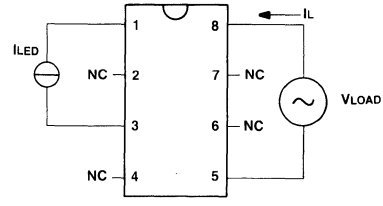
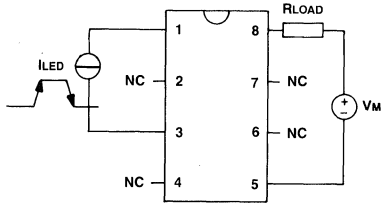
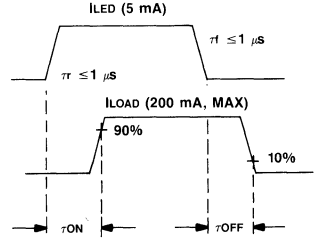


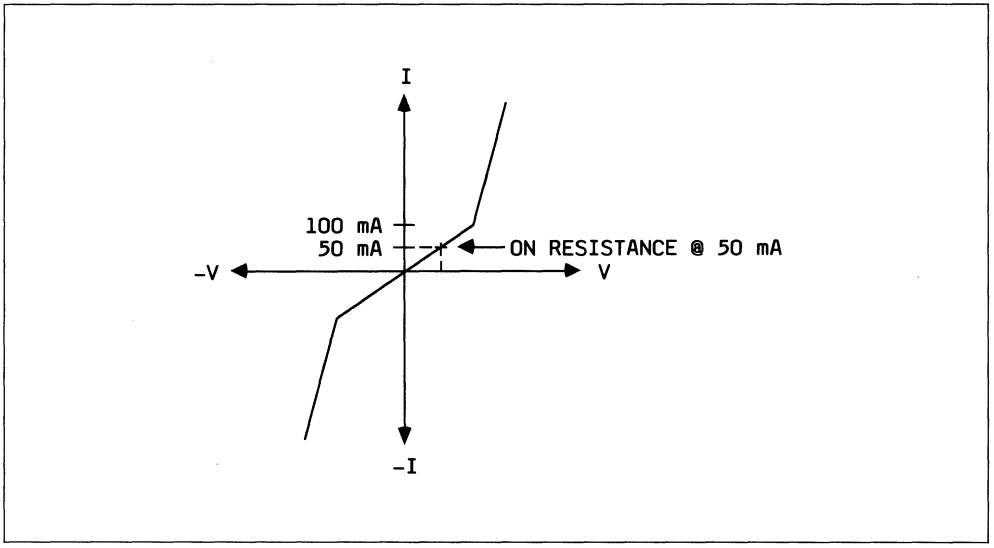
Fig. 4 - $\tau ON/\tau OFF$ Test Circuit and Waveform





CHARACTERISTIC CURVES

Fig. 5 - ON-State Characteristics of Output Poles (Illustrating Bidirectional V-I Characteristics)



DEVICE OPERATION

In the OFF-state, this device can withstand its rated voltage at leakage currents less than 20 μA. In the ON-state, this device exhibits a bidirectional resistive characteristic for currents less than 100 mA (see Figure 5 for ON-state characteristics). This device can switch up to 400 volts at currents up to 200mA.
This one-pole relay offers one of the highest voltage capabilities for a device in its class. Rated at 400 volts, it is particularly suitable for 240 Vrms loads which appear widely in many industrial applications. Despite the higher voltage rating, this device still features ON resistance of only 40Ω maximum. This device will pass surge current up to 4A for 1ms.

APPLICATION

This device has been optimized to meet the demands of switching high voltages at moderate current levels in applications such as telecommunications, instrumentation, and medium-power switching. It is ideally suited for applications where high performance, noise-free switching of ac and dc signals is desirable.
The operational range of this device includes low-power commercial voltage applications where milampere control signals and low ON-resistance are required. The speed, reliability, and linearity of this switch makes it well suited for those applications which are beyond the range of mechanical relays, thyristors, and triacs. For lower ON resistance, higher voltages, or greater current capability, the LH1016 can be easily combined in parallel or series arrangements, as required, with their control LEDs simply driven in series.
The low ON-resistance and low-noise features are beneficial in instrumentation applications. The optical coupling provides isolation of the switch from the control signals in high-voltage and high-frequency applications.
The fabrication of high-voltage, monolithic ICs in a unique dielectric isolation process provides high reliability and the solid-state contruction eliminates problems associated with mechanical relays such as sensitivity to shock and vibration.

Fig. 6 - Typical Application as a Triac Predriver

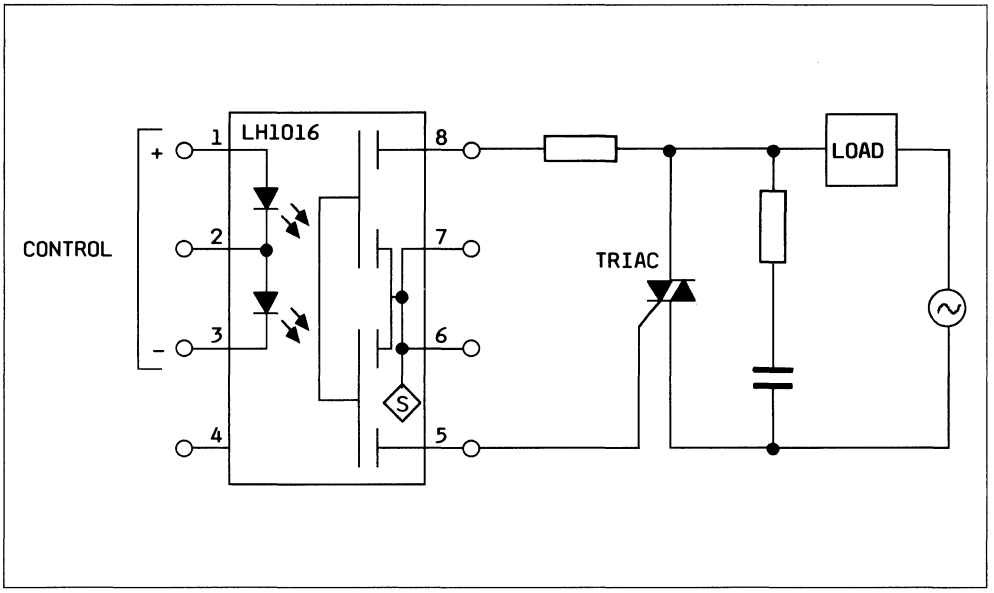
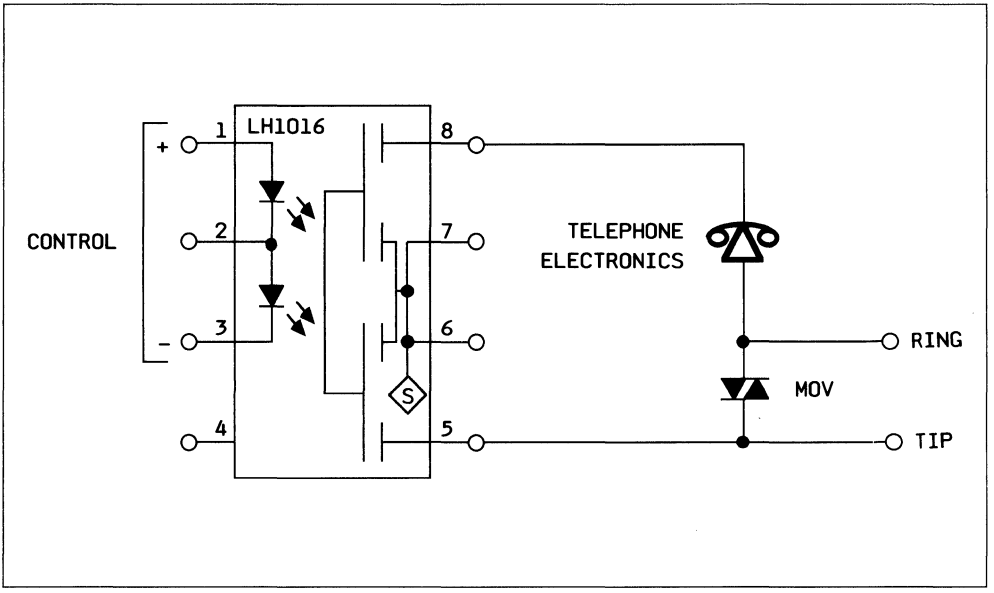


Fig. 7 - Single-Line Switchhook Application



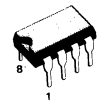
LH1028

PRELIMINARY DATA

AN AT&T PRODUCT

TELEPHONE INTERFACE CIRCUIT

- WITHSTANDS TELEPHONE LOOP VOLTAGES TO 140V
- OPERATES AT LOW TIP-RING VOLTAGES (TYPICALLY AS LOW AS 2.7V)
- POLARITY GUARD HAS LOW INTERNAL VOLTAGE DROPS
- MONOLITHIC SOLID-STATE CONSTRUCTION GIVES COMPETITIVE EDGE IN PHYSICAL AREA CONSERVATION AND RELIABILITY

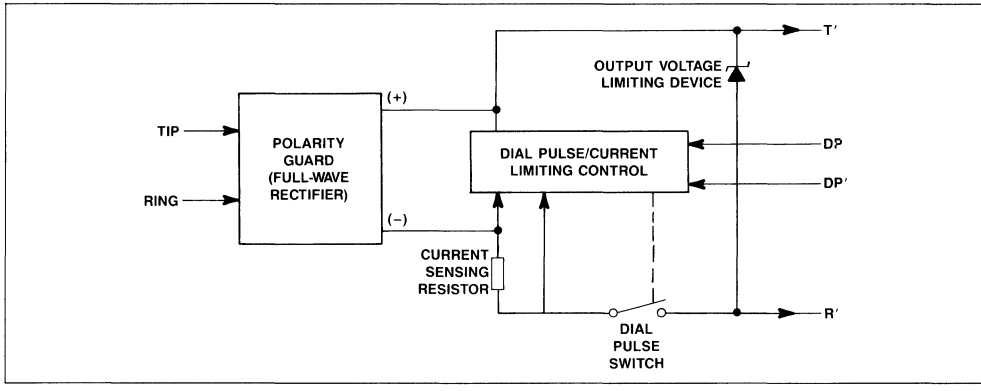


Minidip Plastic

ORDERING NUMBER: LH1028BB

Dielectric isolation and a monolithic high-voltage DMOS technology are used to fabricate the LH1028 Telephone Interface Circuit (TIC). This integrated circuit performs the following basic functions: high-voltage dial pulse switching, protection against reversal of Tip-Ring polarity from the Central Office, and overvoltage/overcurrent protection of telephone circuits.

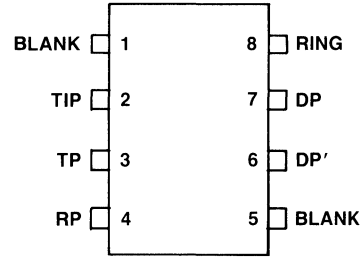
Fig. 1 - Functional Diagram



PIN DESCRIPTION

Pin	Symbol	Description
2	Tip	Tip Input
8	Ring	Ring Input
3	T Prime (T')	Positive output of polarity guard
7	DP	Control for internal dial pulse switch
6	DP Prime (DP')	Control for internal dial pulse switch
4	R Prime (RP')	Negative output of polarity guard
1	NC	No connection; may be used as tie points
5	NC	No connection; may be used as tie points

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{TR}	Voltage (Tip-Ring)	140	V
T_A	Ambient Operating Temperature Range	0 to 50	°C
T_{stg}	Storage Temperature Range	−40 to +125	°C
	Pin Temperature (Soldering, 15 Sec)	300	°C
P_D	Power Dissipation (Package Limitation)	750	mW

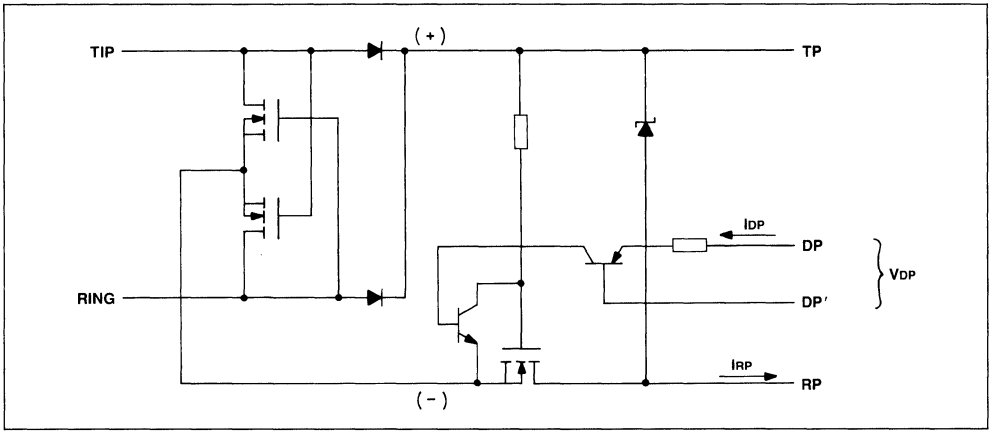
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (See Figure 2)

(T_A = 4 to 49°C for Min and Max value) (T_A = 25°C for Typical value)

Parameter	Test Conditions	Min	Typ	Max	Unit
Breakdown Voltage (Tip-Ring)	V_{DP} = 3.35V Increase V_{TR} until I_{TR} = 3mA (See Fig. 3)	140	175	—	V
Dial Pulse Control Voltage, V_{DP}	V_{TR} = 78.8V Decrease V_{DP} until I_{TR} = 1.75mA (See Fig. 3)	—	1.7	3.35	V
Dial Pulse Control Current	V_{TR} = 78.8V; V_{DP} = 3.35V (See Fig. 3)	—	25	77	μA
Off-State Leakage Current	V_{TR} = 78.8V; V_{DP} = 3.35V (See Fig. 3)	—	0.4	1.57	mA
Tip-Ring Operating Voltage	Increase V_{TR} until V_{OUT} = 1.6V R = 400Ω (See Fig. 4) I_{RP} = −4mA	—	2.7	2.9	V
ON-State Voltage V_{TR} = 6V	R = 235Ω; I_{RP} = −20mA Measure $V_{TR} - V_{OUT}$ (See Fig. 4)	—	1.05	1.3	V
Output Voltage, V_{TR} = 140V peak	Measure V_{OUT} peak (See Fig. 5)	—	26	30	V
Turn-on Time	DP initially at +5V (See Fig. 6)	—	20	1000	μs
Turn-off Time	DP initially shorted to DP' (See Fig. 7)	—	20	1000	μs

Fig. 2 - Simplified Schematic Illustrating Characteristic Symbology



TEST CIRCUITS

Fig. 3

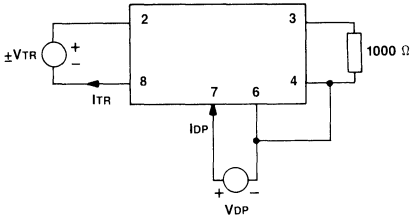


Fig. 4

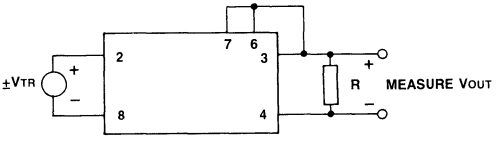
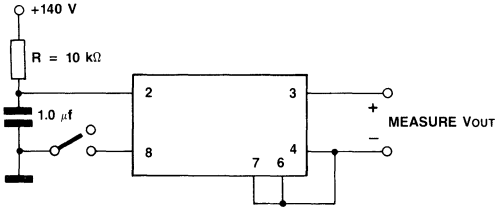


Fig. 5



CHARACTERISTIC TIMINGS

Fig. 6 - Turn-on Time Test Method

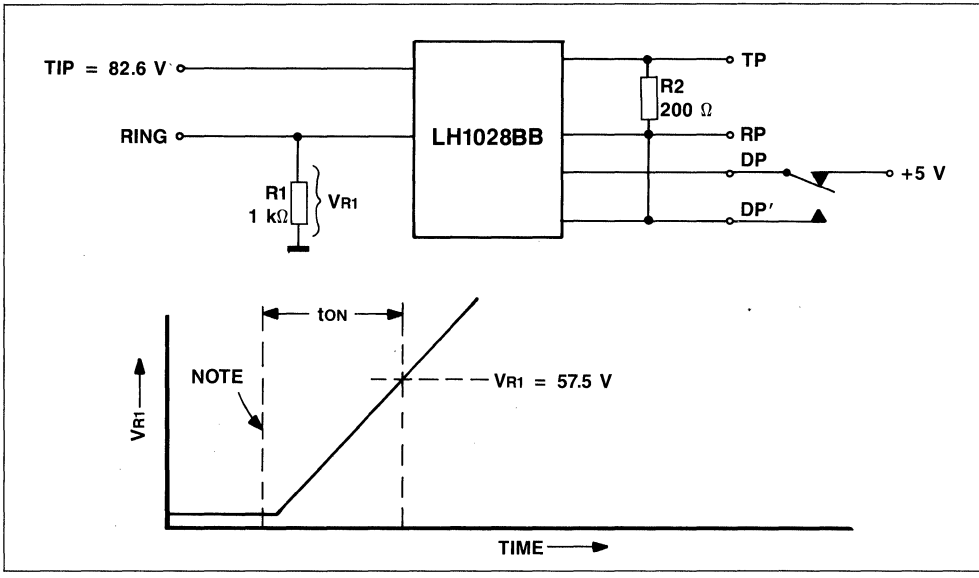


Fig. 7 - Turn-off Time Test Method

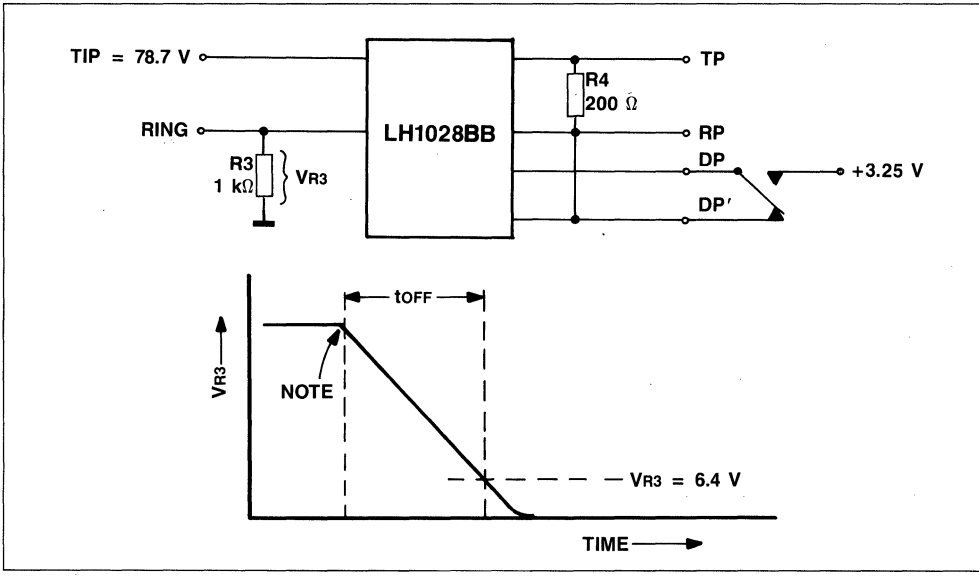
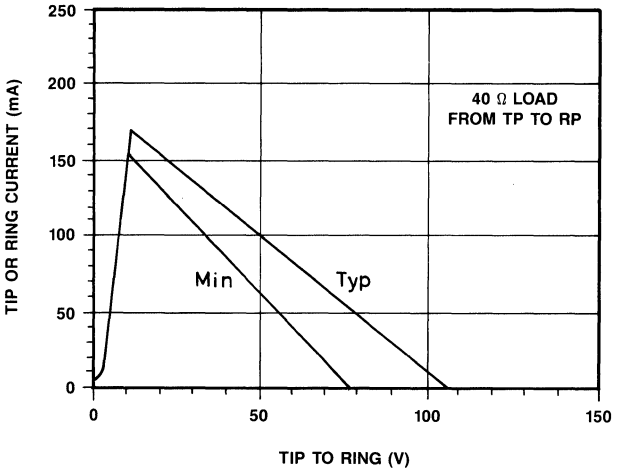


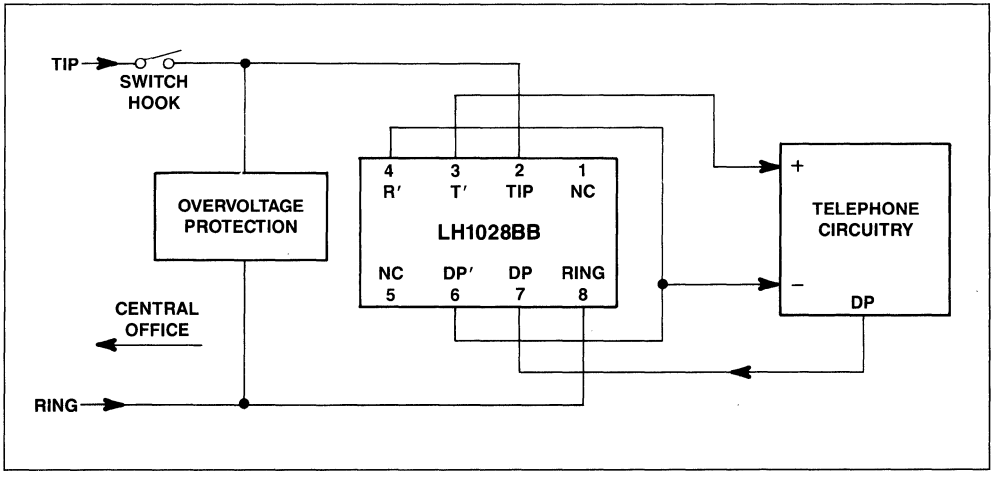
Fig. 8 - Current Limiting Characteristics



APPLICATION

The LH1028 device can be connected in the following manner to perform telephone interface functions. An overvoltage metal-oxide-varistor or other similar type of device shunts the Tip-Ring input terminal of the LH1028 TIC and limits the voltage across these terminals to less than 140V (the maximum voltage rating of the LH1028). The output terminals of the LH1028 TIC are TPRIME (T') and RPRIME (R'). T' and R' are the positive and negative sides of the TIC polarity guard, respectively. R' is connected to the telephone circuitry through a switch which is internal to the LH1028 TIC. This internal switch opens when a dial pulse voltage is applied between terminal DP (Dial Pulse) and DP' (Dial Pulse Prime).

Fig. 9 - Typical Telephone Set Configurations



LH1056

PRELIMINARY DATA

AN AT&T PRODUCT

MSR HIGH-VOLTAGE SOLID-STATE RELAY

- HIGH VOLTAGE MONOLITHIC IC FABRICATED IN A DIELECTRIC ISOLATION PROCESS
- CAN SWITCH LOADS UP TO 350V AT CURRENTS UP TO 100mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- 3750V INPUT/OUTPUT ISOLATION (OPTICALLY COUPLED)
- GOOD dV/dT CAPABILITY
- HIGH-SURGE CAPABILITY
- LOW-POWER CONSUMPTION
- NOISE FREE OPERATION
- NO ELECTROMAGNETIC INTERFERENCE

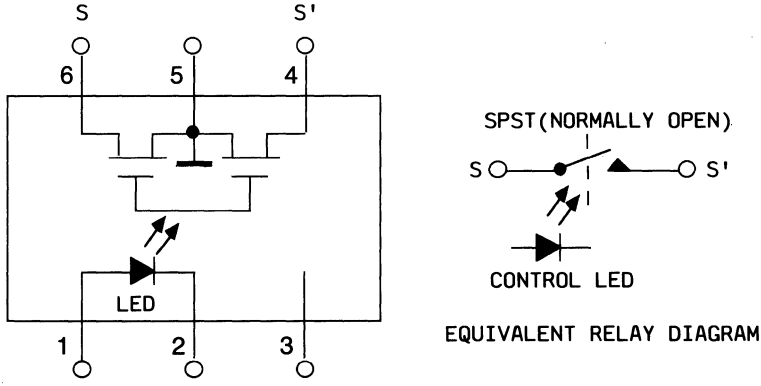
The LH1056 (Multipurpose Solid-State Relay) is a low-cost, bi-directional, SPST switch which can replace mechanical relays in many applications. Its output is rated at 350 volts and can handle loads up to 100 mA. The MSR is packaged in a 6-pin plastic DIP and provides up to 3750 volts of input/output-isolation. The MSR will switch both AC and DC loads.

DIP-6 Plastic

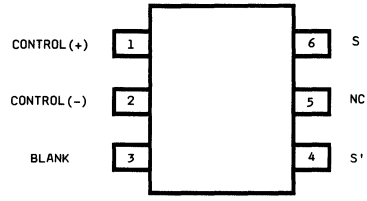
ORDERING NUMBER: LH1056AT

Each device consists of one GaAlAs LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25 mA, and is exceptionally linear up to 50 mA. Beyond 50 mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1056 also has internal current limiting which clamps the load current to 150 mA to insure that the device will survive during power surges. The MSR wil survive FCC, lightning test number 68-302 when it is properly protected.

Fig. 1 - Functional and Equivalent Relay Diagrams



PIN CONFIGURATION



PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S S'	These pins are the outputs. The pin designated as S represents one side of a relay pole. The pin designated as S' (S Prime) is the complementary side of a relay pole. This relay pole is normally open unless sufficient control current is flowing.
Blank	This pin may be used as a tie-point for external components. Voltage on this pin should not exceed 300 volts.
NC	This pin is connected to internal circuitry. It should **not** be used as a tie-point for external circuitry.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−40 to +100	°C
Pin Temperature (Soldering time = 15 s)	300	°C
Input/Output Voltage Isolation	3750	V
LED Input Ratings		
Continuous Forward Current	20	mA
Reverse Voltage	10	V
Recommeded Maximum Output Operation		
Operating Voltage	350	V
Load Current	100	mA
Surge Voltage ON or OFF State	350	V

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Unit
LED Forward Current for Turn-On		$I_{LOAD} = 25mA$ $V_M = 1.25V$ (See Fig. 2)	1.0	3.5	5.0	mA
ON Resistance $R_{ON} = V_M/25mA$		$I_{LED} = 5mA$ $I_{LOAD} = \pm 25mA$ (See Fig. 2)	20	30	50	Ω
ON Voltage		$I_{LED} = 5mA$ $I_{LOAD} = \pm 100mA$ (See Fig. 2)	—	2.6	—	V
Breakdown Voltage		$I_{LED} = 0mA$ $I_{LOAD} = \pm 50\mu A$ (See Fig. 2)	350	—	—	V
Surge Voltage		1.0ms square wave. $I_{LED} = 5.0mA$ (See Fig. 2)	350	—	—	V
Leakage Current		$V_{LOAD} = 300V$ $I_{LED} = 0mA$ (See Fig. 3)		5	40	μA
		$V_{LOAD} = 100V$ $I_{LED} = 0mA$ (See Fig. 3)	—	0.5	—	
Switching Time	TURN ON	$R_{LOAD} = 10K\Omega$ (See Fig. 4)	—	—	2	msec
	TURN OFF	$R_{LOAD} = 10K\Omega$ (See Fig. 4)	—	—	0.5	

TEST CIRCUITS

Fig. 2 - R_{ON}- ON Voltage and Breakdown Voltage

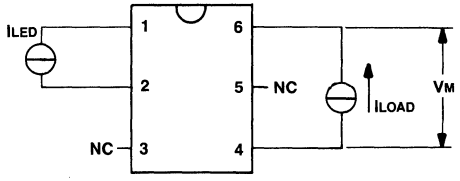


Fig. 3 - Leakage Current

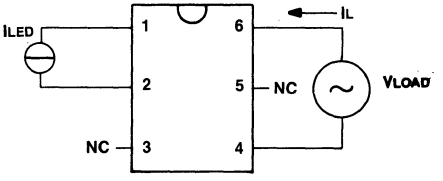


Fig. 4 - $\tau ON/\tau OFF$ Test Circuit and Waveform

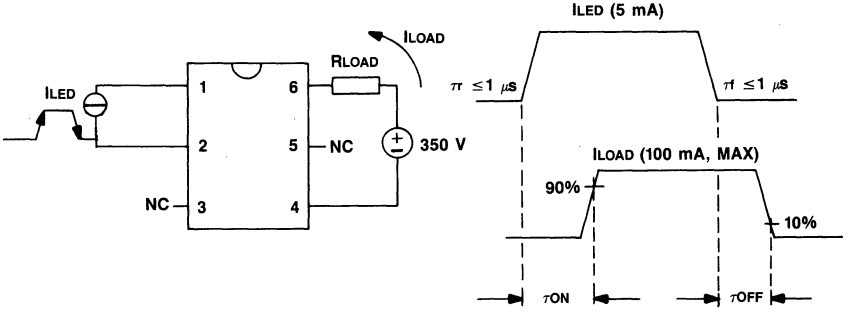


Fig. 5 - MSR Solid-State Relay Typical ON Characteristics

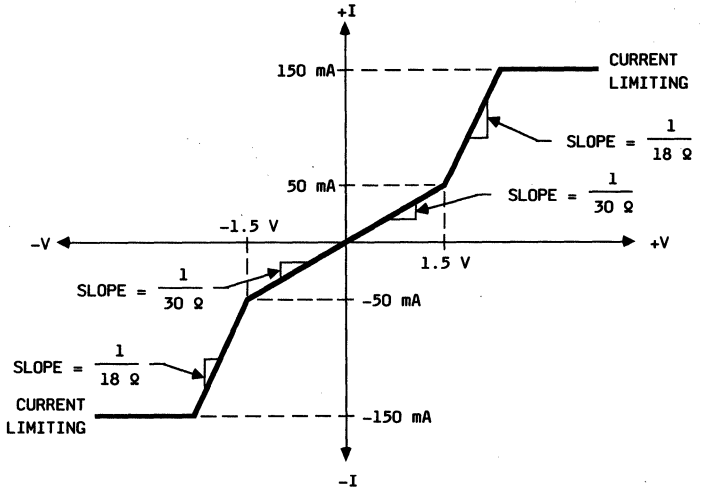


Fig. 6 - Triac Predriver

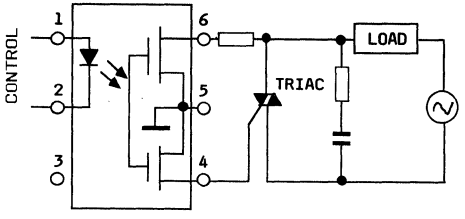
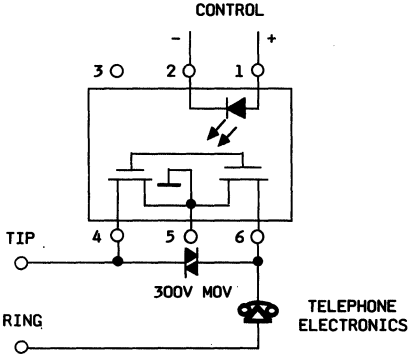


Fig. 7 - Telephone Switchhook



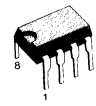
LH1061

ADVANCE DATA

AN AT&T PRODUCT

HIGH-VOLTAGE SOLID-STATE AC/DC RELAY

- HIGH-VOLTAGE MONOLITHIC INTEGRATED CIRCUIT FABRICATED IN A DIELETRIC ISOLATION PROCESS
- CAN SWITCH TWO LOADS UP TO 200 VOLT AT CURRENTS UP TO 200mA
- LOW ON-RESISTANCE
- CLEAN, BOUNCE-FREE SWITCHING
- NO ELECTROMAGNETIC INTERFERENCE
- 3750V I/O ISOLATION (OPTICALLY COUPLED)
- GOOD dV/dT CAPABILITY
- HIGH-SURGE CAPABILITY
- NOISE-FREE OPERATION
- LOW-POWER CONSUMPTION

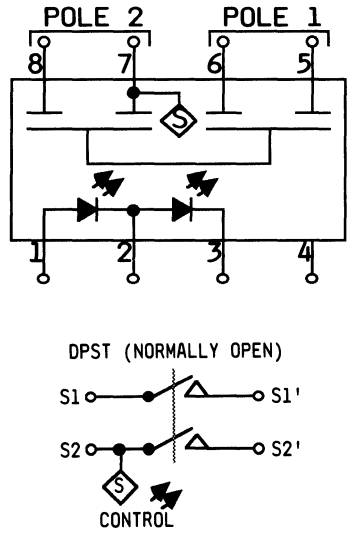


Minidip-D Plastic

ORDERING NUMBER: LH1061AB

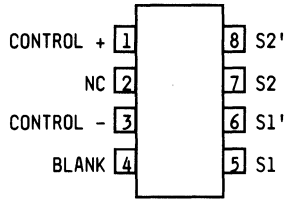
This solid-state device is a high-performance, optically controlled, AC/DC Relay. The LH1061 consists of two GaAlAs light-emitting diodes (LEDs) which optically couples the ON/OFF control signal to a dielectrically isolated high-voltage integrated circuit. The integrated circuit contains the high-voltage DMOS transistors and photosensitive drive circuitry. The optical isolation ensures excellent noise immunity with up to 3750 volts of isolation between input and outputs, while the LED control currents can be as low as 5.0mA. This makes the LH1061 suitable for logic control. Equivalent relay diagrams for this device is shown in Figure 1. The LH1061 also has internal current limiting which clamps the load current to 300mA to ensure that the device will survive during power surges.

Fig. 1 - Functional and Equivalent Diagram



LH1061

PIN CONFIGURATION



PIN DESCRIPTION

Name	Description
Control + Control –	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
S1, S1' S2, S2'	These pins are the outputs. The pins designated as S represents one side of a relay pole. The pins designated as S' are the complementary side of a relay pole. Note that S2 is connected to the substrate.
NC	This pin is connected internally for test purposes. It should NOT be used as a tie-point for external components.
Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 150V.

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	–40 to +100	°C
Pin Soldering Temperature (t = 15 s max)	300	°C
Input/Output Voltage Isolation	3750	V
LED INPUT		
Continuous Forward Current	25	mA
Peak Forward Surge Current	250	mA
[Pulse width = 4.0ms, 10 pulses/s cycle (4%)]		
Reverse Voltage	20	V
OUTPUT, Continuous Current (RMS)		
One Pole (S1, S1' or S2, S2')	300	mA
Each Pole (two poles operating simultaneously)	200	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Parameter (Each Pole)		Test Conditions	Min	Typ	Max	Unit
OUTPUT POLE						
ON Resistance $R_{ON} = V_M/50mA$		$I_{LED} = 5mA$, $I_{LOAD} = \pm 50mA$ (See Fig. 2)	—	15	20	Ω
ON Voltage		$I_{LED} = 5mA$, $I_{LOAD} = \pm 200mA$ (See Fig. 2)	—	2.0	2.5	V
Breakdown Voltage		$I_{LED} = 0mA$, $I_{LOAD} = \pm 20\mu A$ (See Fig. 2)	200	—	—	V
Surge Voltage		1.0ms square wave $I_{LED} = 5.0mA$ (See Fig. 2)	200	—	—	V
Leakage Current		$V_{LOAD} = 200V$ $I_{LED} = 0mA$ (See Fig. 3)	—	—	20	μA
		$V_{LOAD} = 50V$ $I_{LED} = 0mA$ (See Fig. 3)	—	0.5	—	μA
Switching Time	TURN ON	$V_M = \pm 150V$ $R_L = 15K\Omega$ (See Fig. 4)	—	—	2	msec
	TURN OFF	$V_M = \pm 150V$ $R_L = 15K\Omega$ (See Fig. 4)	—	—	0.5	msec
INPUT CONTROL						
LED Forward Voltage		Forward Current = 10mA	1.17	—	1.43	V
LED Breakdown Voltage		Reverse Current = 10μA	10	—	—	V
LED Reverse Leakage Current		Reverse Voltage = 10V	—	—	10	μA
LED Continuous Forward Current:			(See Absolute Maximum Rating)			
Recommended Forward Current for ON-State Operation:			—	5.0	—	mA

TEST CIRCUITS

Fig. 2 - R_{ON}, ON Voltage and Breakdown Voltage

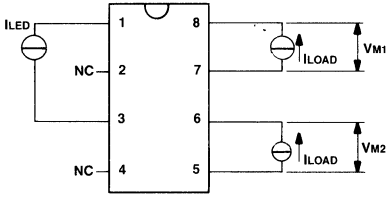


Fig. 3 - Leakage Current

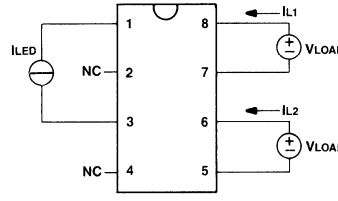
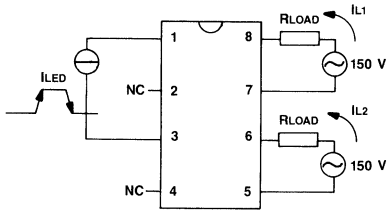
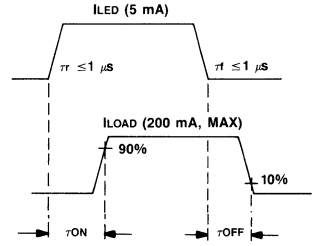


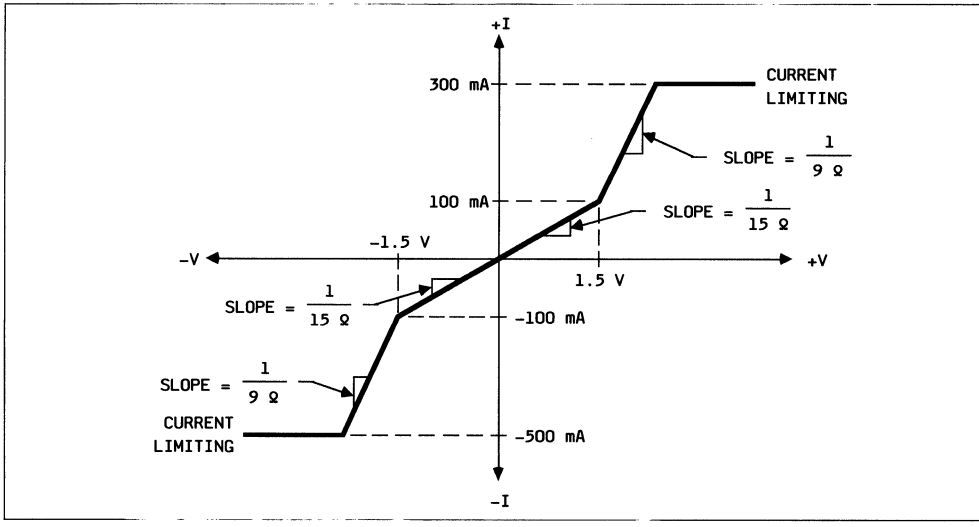
Fig. 4 - $\tau ON/\tau OFF$ Test Circuit and Waveform





CHARACTERISTIC CURVES

Fig. 5 - ON-State Characteristics of Output Poles (Illustrating Bidirectional V-I Characteristics)



DEVICE OPERATION

In the OFF-state, this device can withstand its rated voltage at leakage currents less than 20 μA. In the ON-state, this device exhibits a bidirectional resistive characteristic for currents less than 100 mA (see Figure 5 for ON-state characteristics).
The LH1061 consists of two independent poles, each capable of simultaneously switching up to 200 volts at currents up to 200mA with a maximum ON resistance of 20 ohms. (See Figure 1)
The two-pole, single-throw operation of this switch is advantageous in applications where line balance is an important consideration. The two poles offer 800 volts of pole-to-pole isolation. These switches can also be stacked for higher voltage capability, or paralleled for lower ON resistance.
This device can withstand voltage surges up to 200V (each pole) in both the on and off conditions.

APPLICATION

This device has been optimized to meet the demands of switching high voltages at moderate current levels in applications such as telecommunications, instrumentation, and medium-power switching. It is ideally suited for applications where high performance, noise-free switching of ac and dc signals is desirable.
The operational range of this device includes low-power commercial voltage applications where millampere control signals and low ON-resistance are required. The speed, reliability, and linearity of this switch makes it well suited for those applications which are beyond the range of mechanical relays, thyristors, and triacs. For lower ON resistance, higher voltages, or greater current capability, the LH1061 can be easily combined in parallel or series arrangements, as required, with their control LEDs simply driven in series.
The low ON-resistance and low-noise features are beneficial in instrumentation applications. The optical coupling provides isolation of the switch from the control signals in high-voltage and high-frequency applications.
The fabrication of high-voltage, monolithic ICs in a unique dielectric isolation process provides high reliability and the solid-state contruction eliminates problems associated with mechanical relays such as sensitivity to shock and vibration.

Fig. 6 - Balanced Switchhook Application

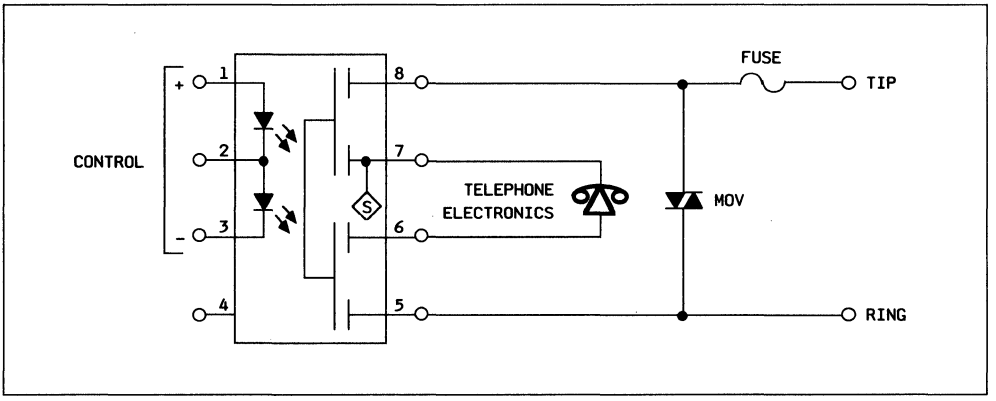
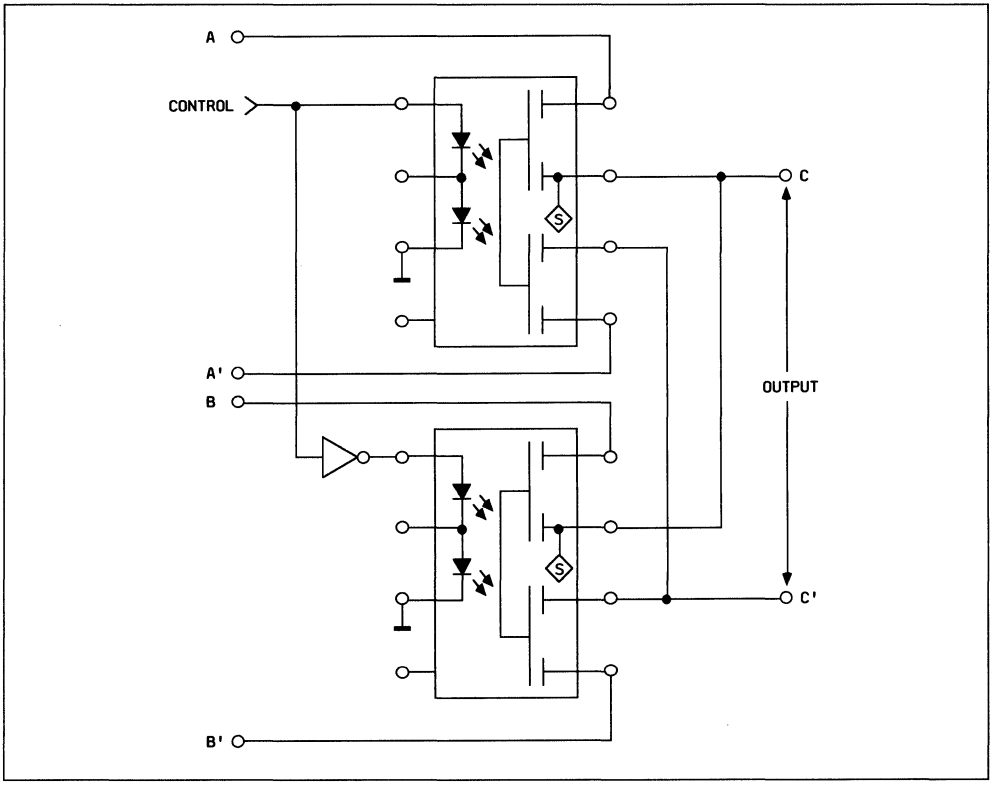


Fig. 7 - Balanced Two-Line Multiplexer Application

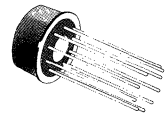


LS025

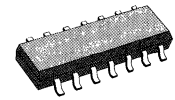
BALANCED MODULATOR

- SINGLE OR DUAL SUPPLY OPERATION
- LOW POWER CONSUMPTION
- LOW CARRIER LEAKAGE
- LOW DISTORTION
- LOW NOISE

The LS025 is a low noise linear integrated circuit, intended for use as a channel modulator and demodulator in FDM telephone equipments and as analogue AC and DC multiplier in industrial and professional applications. It features low quiescent power consumption, low distortion and intermodulation. It shows a typical carrier leakage better than 85dB throughtout the audio bandwidth. The LS025 is available in TO-100 metal case, while the hermetic gold chip (8000 series) is available in SO-14 (14-lead plastic micropackage). This last version is particularly suitable for professional and telecom applications wherever very high MTBF are required.

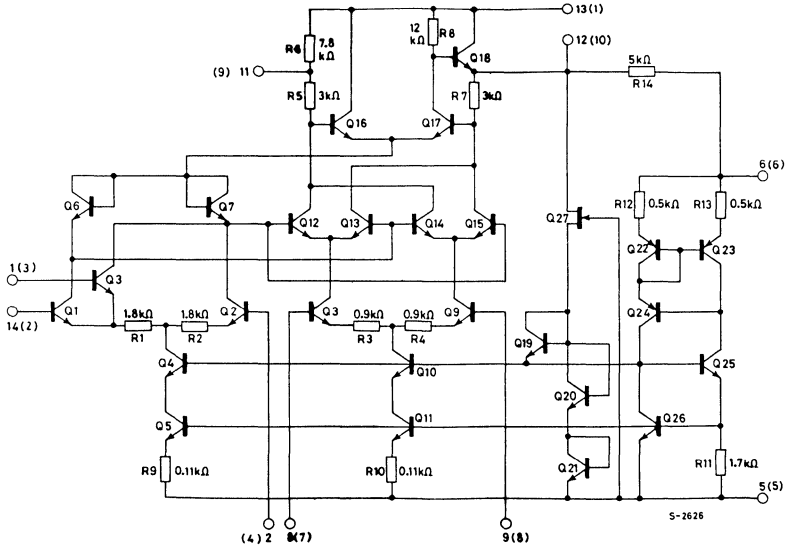


TO-100



SO-14

SCHEMATIC DIAGRAM (The pin numbers refer to the μpackage version, while the numbers in brackets refer to the TO-100 version)

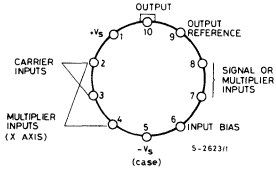


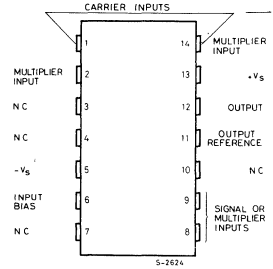
LS025

ABSOLUTE MAXIMUM RATINGS		TO-100	μpackage
V_s	Supply voltage	30 V	
ΔV_i	Differential input voltage	± 5 V	
T_{op}	Operating temperature	-25 to 85 °C	
P_{tot}	Power dissipation at T_{amb} = 70 °C	520 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C

CONNECTION DIAGRAMS AND ORDERING NUMBERS

(top views)





Type	TO-100	SO-14
LS 025	LS 025T	LS025M
LS 8025		LS 8025M

THERMAL DATA

			TO-100	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	155 °C/W	200* °C/W

* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

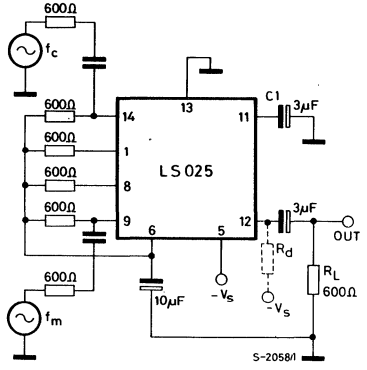
ELECTRICAL CHARACTERISTICS (Referred to the circuit of fig. 1; T_{amb}= 25°C unless otherwise specified. The pins correspond to the μpackage version)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		-12		-30	V
I_s	Supply current			2	2.5	mA
I_b	Input bias current	Pins 14-1 Pins 14-2 Pins 8-9		0.7 0.7 1.4	2 2 4	μA μA μA
ΔI	Input offset current	Pins 14-1 Pins 14-2 Pins 8-9		50 70 100		nA nA nA
	Positive input common mode voltage			4.5		V
	Negative input common mode voltage			-8		V
V_o	DC output voltage (pin 12)		-3.2	-3.8	-4.6	V
ΔV_o	Differential output voltage (pins 11-12)			25	100	mV
V_{ref}	Input biasing reference voltage (pin 6)			-7.5		V
R_i	Input resistance	Pins 14-1 Pins 14-2 Pins 8-9		30 300 150		kΩ kΩ kΩ
R_o	Output resistance	f = 1 kHz		3	10	Ω
V_o	Output voltage swing		1	1.3		Vpp
CMR	Common mode rejection	CM signal (pins 14-1) V = 700 mVrms f_1= 10 kHz Diff. signal (pins 8-9) V = 350 mVrms f_2= 40 kHz		98		dB
		CM signal (pins 14-2) V = 700 mVrms f_1= 10 kHz Diff. signal (pins 8-9) V = 350 mVrms f_2= 40 kHz		86		dB
		CM signal (pins 8-9) V = 350 mVrms f_1= 10 kHz Diff. signal (pins 14-1) V = 175 mVrms f_2= 40 kHz		80		dB
SVR	Positive supply voltage rejection	f = 1 kHz		33		dB
SVR	Negative supply voltage rejection			80		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
K	Scale factor			3.2		V^{-1}
G_c	Conversion gain		4.5	5	5.5	dB
ΔG_c	Conversion gain change	T_{amb}= 10 to 50°C		± 0.1		dB
	Carrier leakage	V_m= 0	-35	-50		dBv
$\frac{V_{fm}}{V_{(f_c \pm f_m)}}$	Modulating signal leakage		-35	-50		dBmo
$\frac{V_{(2f_m)}}{V_{(f_c \pm f_m)}}$	2nd harmonic modulating signal leakage			-75		dBmo
$\frac{V_{(f_c \pm 2f_m)}}{V_{(f_c \pm f_m)}}$	2nd harmonic distortion		-60	-75		dBmo
$\frac{V_{2(f_c \pm f_m)}}{V_{(f_c \pm f_m)}}$	2nd harmonic distortion		-55	-80		dBmo
$\frac{V_{(f_c \pm 3f_m)}}{V_{(f_c \pm f_m)}}$	3rd harmonic distortion		-60	-79		dBmo
	Low frequency thermal noise	V_m= 0 f = 1 kHz B = 100 Hz	-115	-125		dBv
	High frequency thermal noise	V_m= 0 f = 30 kHz B = 100 Hz		-127		dBv

Fig. 1 - Test and application circuit of modulator with single supply voltage



Working conditions

V_s = -20V
f_c = 130 kHz
f_m = 25 kHz
V_o = -15 dBv ($f_c \pm f_m$)
V_c = -13 dBv
$R_L \equiv$ 600 Ω

Fig. 2 - Carrier leakage vs. modulation signal input offset

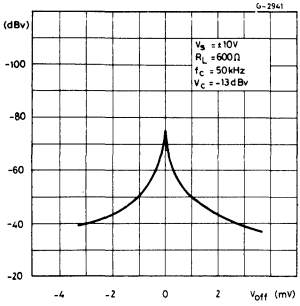


Fig. 3 - Conversion gain vs. frequency

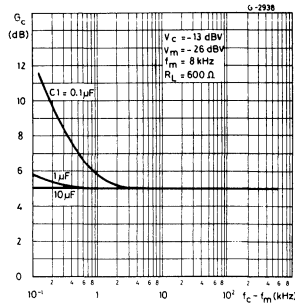


Fig. 4 - Distortion vs. output level

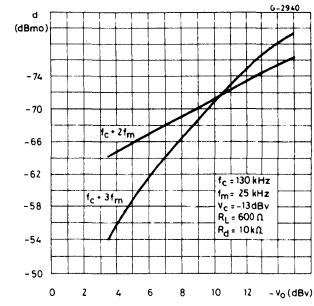


Fig. 5 - Carrier leakage adjustment circuit for system with two supply voltages

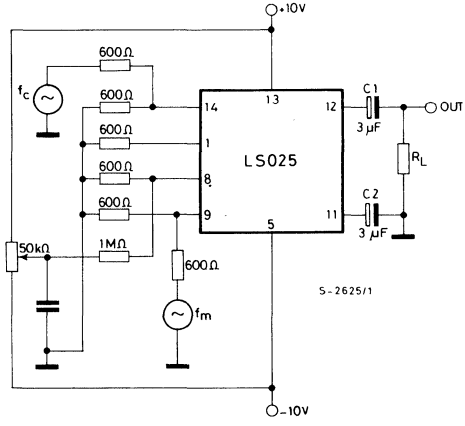
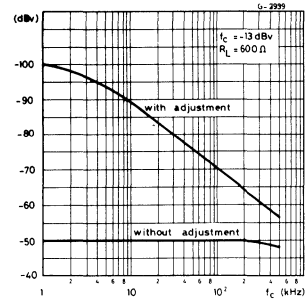
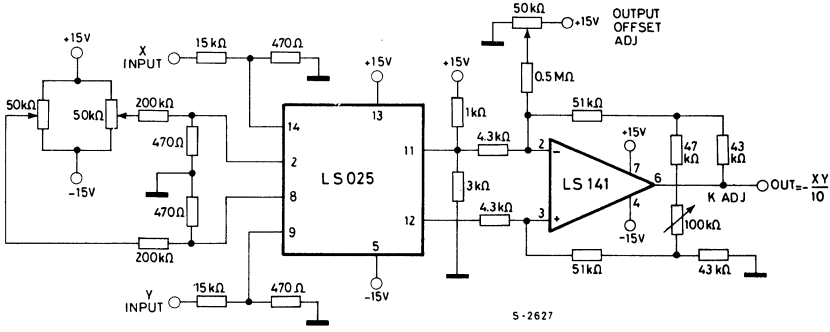


Fig. 6 - Carrier leakage vs. frequency



APPLICATION INFORMATION

Fig. 7 - DC multiplier



Application diagram of DC multiplier, have a scale factor K = 0.1. Typical linearity and leakage errors are less than 1%.
The input voltage range is ± 10V.

Definition of units

dBm : power level ($10 \lg \frac{P_2}{P_1}$) is expressed in dBm when P_1 is 1 mW, therefore 0 dBm= 1 mW.

dBmo : the power is expressed in dBmo when referred to an established power level in the circuit, generally the output signal level.
e.g.: if the output level is -15 dBm and this level is chosen as reference, then 0 dBmo = -15 dBm; if another signal, i.e. the distortion measured at the same point of the circuit, is -90 dBm, then the distortion is -75 dBmo.

dBv : $20 \lg \frac{V_2}{V_1}$ when V_1= 775 mVrms.

Definition of terms

Common mode rejection ratio : $CMR = 20 \lg \frac{V_{CM}\, G}{V_o}$

with G = Conversion gain with specified circuit conditions
V_{CM} = Common mode signal level
V_o = Output signal level at frequency = $f_2 \pm f_1$

Scale factor : $K = \frac{V_o}{V_x \cdot V_y}$

with V_x = voltage input (pins 14 - 2)
V_y = voltage input (pins 8 - 9)

APPLICATION INFORMATION (continued)

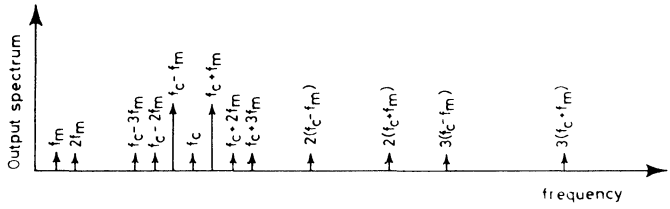
Conversion gain : $G_c = 20 \lg \frac{V_o (f_c \pm f_m)}{V_i (f_m)}$

Carrier leakage : is defined as the output voltage at carrier frequency with only the carrier applied to the input (modulating voltage = 0)

Modulating signal leakage : is defined as the output voltage, at modulating frequency, referred to fundamental carrier sidebands

$$M.S.L. = 20 \lg \frac{V_o (f_m)}{V_o (f_c \pm f_m)}$$

Output spectrum vs. frequency



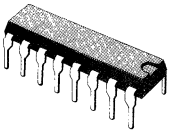
f_c = carrier fundamental (leakage)
f_m = mod. sig. (leakage)
nf_m = harmonic modulating signal (leakage)
$f_c \pm f_m$ = fundamental carrier sidebands
$f_c \pm nf_m$ = fundamental carrier sideband harmonics
$n (f_c \pm f_m)$ = carrier harmonic sidebands

LS156

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

The LS156 is a monolithic integrated circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transdurcers for both transmitter and receiver (typically piezoceramic capsules, but the device can work also with dynamic ones). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS156 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer). The LS156 basic functions are the following:

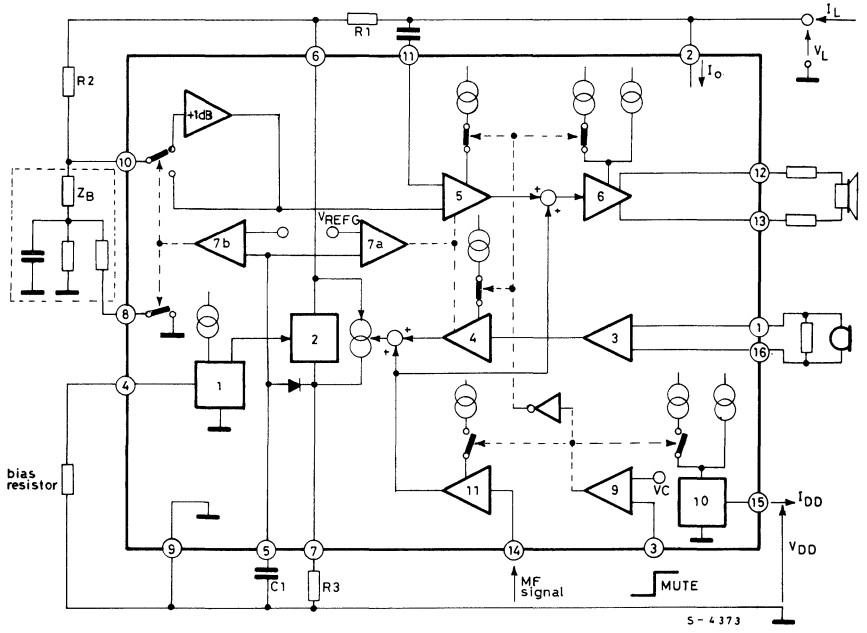
- It presents the proper DC path for the line current.
- It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing the line length through the line current.
- It acts as linear interface for MF, supplying a stabilized to the digital chip and delivering to the line the MF tones generated by the M761.



DIP-16 Plastic
(0.4)

ORDERING NUMBER: LS156B

BLOCK DIAGRAM



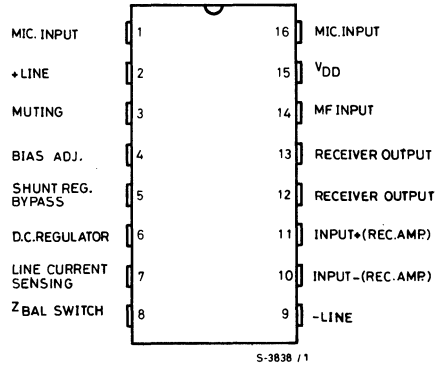
LS156

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM

(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUITS

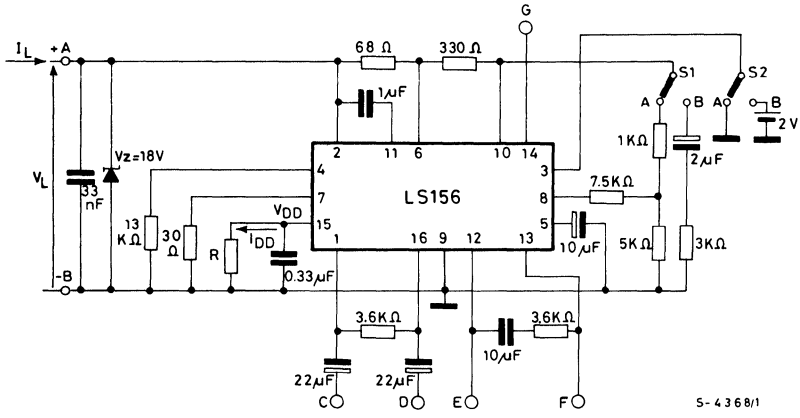
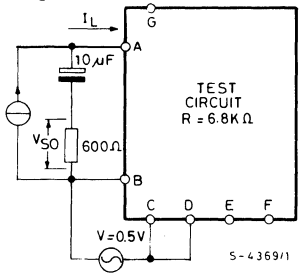
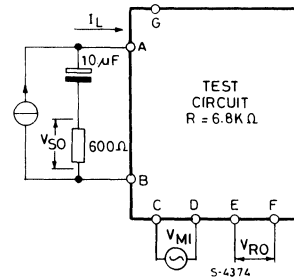


Fig. 1



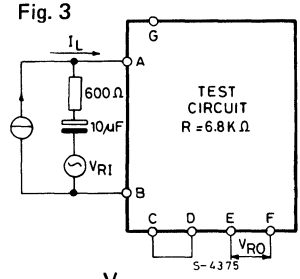
V = 0,5V; CMRR

Fig. 2



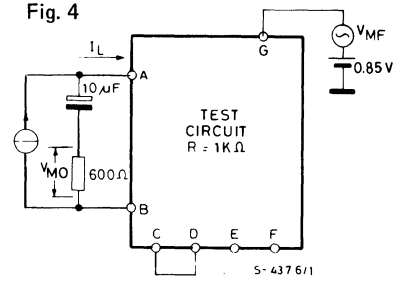
Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_s = \frac{V_{SO}}{V_{MI}}$

Fig. 3



$G_R = \frac{V_{RO}}{V_{RI}}$

Fig. 4



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, S1 and S2 in (a), T_{amb}= -25 to +50°C, f = 200 to 3400 Hz, unless otherwise specified)

Parameter		Test condition		Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION								
V_L	Line voltage	T_{amb}= 25°C	I_L= 12 mA I_L= 20 mA I_L= 80 mA	3.9		4.7 5.5 12.2	V	–
CMRR	Common mode rejection	f = 1 KHz	I_L= 12 to 80 mA	50			dB	1
G_s	Sending gain	T_{amb}= 25°C f = 1 KHz V_{MI}= 2 mV	I_L= 52 mA I_L= 25 mA	44 48	45 49	46 50	dB	2
	Sending gain flatness	V_{MI}= 2 mV	f_{ref}= 1 KHz I_L= 12 to 80 mA			± 1	dB	2
	Sending distortion	f = 1 KHz I_L= 16 to 80 mA	V_{so}= 1V V_{so}= 1.3V			2 10	%	2
	Sending noise	V_{MI}= 0V	I_L= 40 mA		-70		dBmp	2
	Microphone input impedance pin 1-16	V_{MI}= 2 mV	I_L= 12 to 80 mA	40			KΩ	
	Sending loss in MF operation	V_{MI}= 2 mV S_2 in (b)	I_L= 52 mA I_L= 25 mA	-30 -30			dB	2
G_R	Receiving gain	V_{RI}= 0.3V f = 1 KHz T_{amb}= 25°C	I_L= 52 mA I_L= 25 mA	3 7	4 8	5 9	dB	3
	Receiving gain flatness	V_{RI}= 0.3V	f_{ref}= 1 KHz I_L= 12 to 80 mA			± 1	dB	3
	Receiving distortion	f = 1 KHz	I_L= 12 mA V_{RO}= 1.6V I_L= 12 mA V_{RO}= 1.9V I_L= 50 mA V_{RO}= 1.8V I_L= 50 mA V_{RO}= 2.1V			2 10 2 10	%	3
	Receiving noise	V_{RI}= 0V	I_L= 12 to 80 mA		150		μV	3
	Receiver output impedance pin 12-13	V_{RO}= 50 mV	I_L= 40 mA			100	Ω	
	Sidetone	f = 1 KHz T_{amb}= 25°C S_1 in (b)	I_L= 52 mA I_L= 25 mA			36 36	dB	2
Z_{ML}	Line matching impedance	V_{RI}= 0.3V	f = 1 KHz I_L= 12 to 80 mA	500	600	700	Ω	3

ELECTRICAL CHARACTERISTICS (continued)

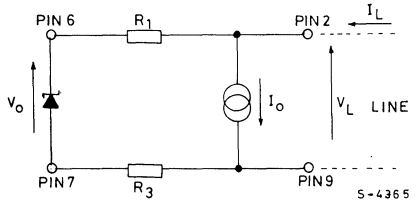
Parameter		Test condition	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF supply voltage (Standby and operation)	I_L= 12 to 80 mA	2.4	2.5		V	–
I_{DD}	MF supply current Stand by Operation	 I_L= 12 to 80 mA I_L= 12 to 80 mA; S_2 in (b)	 0.5 2			mA	–
	MF amplifier gain	I_L= 12 to 80 mA $f_{MF\ in}$= 1 KHz $V_{MF\ in}$= 80 mV	15		17	dB	4
V_i	DC input voltage level (pin 14)	$V_{M\ Fin}$= 80 mV		.3V_{DD}		V	–
R_i	Input impedance (pin 14)	$V_{M\ Fin}$= 80 mV	60			KΩ	–
d	Distortion	$V_{M\ Fin}$= 110 mV I_L= 12 to 80 mA			2	%	4
	Starting delay time	I_L= 12 to 80 mA			5	ms	–
	Muting threshold voltage (pin 3)	Speech operation			1	V	–
		MF Operation	1.6			V	–
	Muting stand by current (pin 3)	I_L= 12 to 80 mA			-10	μA	–
	Muting operating current (pin 3)	I_L= 12 to 80 mA S_2 in (b)			+10	μA	–

CIRCUIT DESCRIPTION

1. DC characteristic

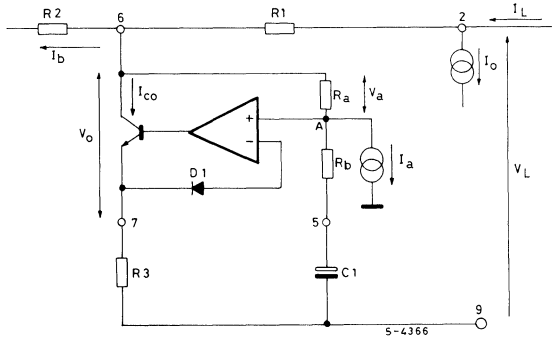
In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristics V_L, I_L.
The DC characteristic of the LS 156 it is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3. The equivalent circuit of the total system is shown in fig. 5.

Fig. 5 - Equivalent DC load to the line



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit.
The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).
The recommended minimum of I_o is 7.5 mA.
The voltage $V_o \cong 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Fig. 6 - Circuit configuration of the shunt regulator



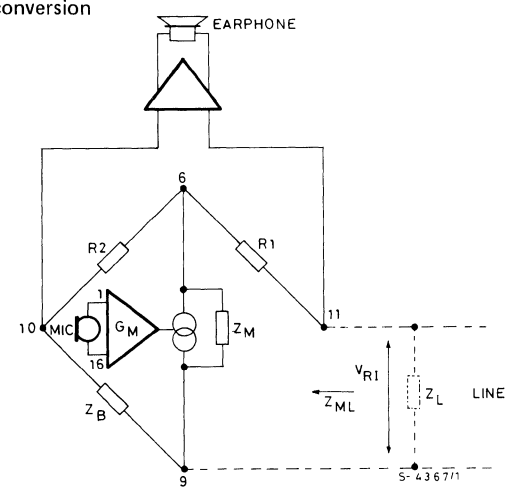
CIRCUIT DESCRIPTION (continued)

The difference $I_L - I_o$ flows through the shunt regulator being I_b negligible.
I_a is an internal constant current generator; hence $V_o = V_{BED1} + I_a \cdot R_a \cong 3.8V$. The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.
It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_{BED1} \cong (I_L - I_o) R_3 + V_{BED1}$).

2. 2/4 wires conversion

The LS156 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 7).

Fig. 7 - Two to four wires conversion



For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B \gg Z_L$); the main part is sent to the line via R_1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$.

From fig. 6, considering C_1 as a short circuit for AC signal, any variation ΔV_6 generates a variation.

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

CIRCUIT DESCRIPTION (continued)

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R_3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R_1 + Z_M \,//\, (R_2 + Z_B)$$

By choosing $Z_M \gg R_1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R_1 (of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must be always valid).

The received signal is related to R_1 value according to the approximated relationship

$$V_R = 2 \cdot V_{RI} \frac{R_1}{R_1 + Z_M}$$

Note that by changing the value of R_1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. Automatic gain control

The LS156 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation by sensing the line length through the line current.
The line current is sensed across R_3 (see fig. 6) and transferred to pin 5 by the regulator.

$$V_5 = V_{BED1} + V_7 \cong V_{BED1} + (I_L - I_o) \cdot R_3.$$

The pin 5 V_5 voltage, after a comparison with an internal reference V_{REFG} (see the block diagram) is used to modify the gain of the amplifiers (4) and (5) on both the sending and receiving path.
The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.
Minimum gain is reached for a line current of about 52 mA for the same drain current $I_o = 7.5$ mA.
When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.
Automatic switching of the balance network Z_B for a better sidetone is performed by the LS156 through V_5 information. This information, proportional to the line length, drives the comparator (7b) (see the block diagram).
For long lines, the impedance level of Z_B is high (pin 8 open) and the additional +1 dB gain is added to the receiving amplifier chain.

CIRCUIT DESCRIPTION (continued)

For short lines, the impedance level of Z_B is automatically switched to a lower value (pin 8 shorted to ground) and the additional +1 dB block is bypassed by the received signal.
A built in hysteresis circuit avoids uncertain operation of the comparator.

4. Transducers interfacing

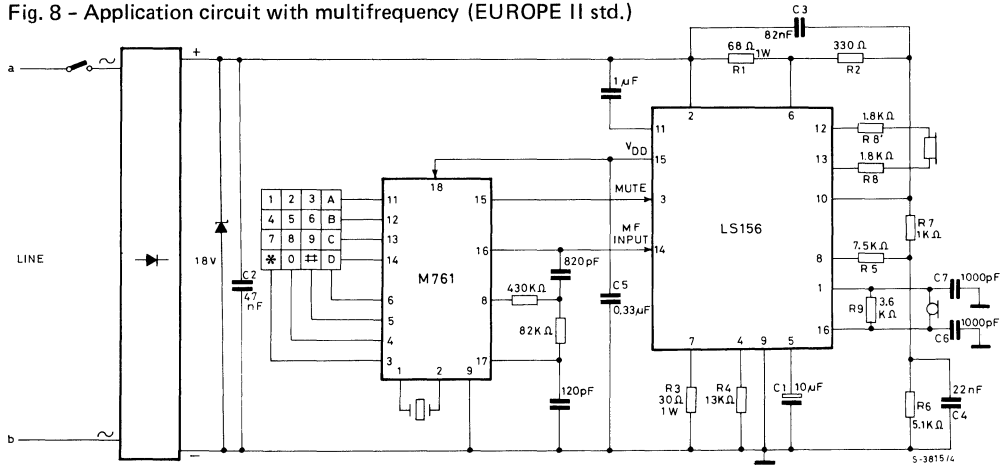
The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistors without affecting the sending gain. The receiving output stage (6) is particularly intended to drive piezoceramic capsules. [Low output impedance (100Ω max); high voltage swing (close to V_L); current capability of 1.8 mAp].
When a dynamic capsule is used, it is useful to decrease the receiving gain by decreasing R_1 value (see the relationship for V_R).
With very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency interfacing

The LS156 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.
When no key of the keyboard is pressed the mute state is low and the LS156 feeds the M761 through pin 15 with low current (standby operation of the M761). The oscillator of the M761 is not operating. When one key is pressed, the M761 sends a "high state" mute condition to the LS156. A voltage comparator (9) of LS156 drives internal electronic switches: the current delivered by the voltage supply (10) is increased to allow the operation of the oscillator. This extra current is diverted by the receiving and sending section of the LS156 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.
A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber; the MF amplifier (11) delivers the dial tones to the sending paths.
The application circuit shown in fig. 9 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm), an external divider must be used (fig. 11).
The mute function can be used also when a temporary inhibition of the output signal is requested.

APPLICATION INFORMATION

Fig. 8 - Application circuit with multifrequency (EUROPE II std.)



APPLICATION INFORMATION (continued)

Fig. 9 - Application circuit with multifrequency (EUROPE I std.)

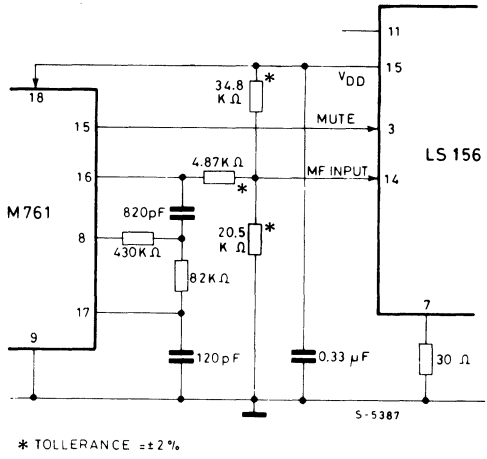


Fig. 10 - External mute function

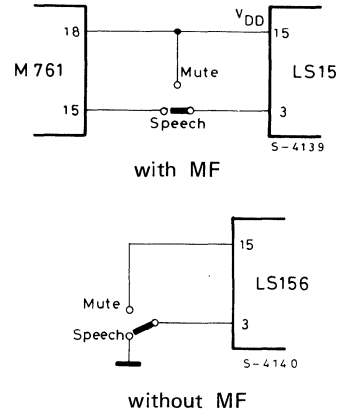
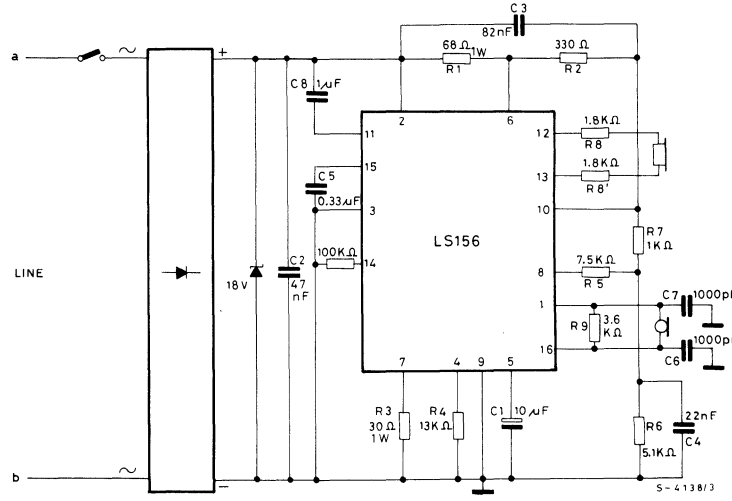


Fig. 11 - Application circuit without multifrequency.



The circuits shown in fig. 8 and fig. 11 are referred to the Italian standard. The fig. 10 shows the connection for mute function (inhibition of the output stage when it is requested) by using an external switch at pin 3.

Different values for the external components can be used in order to satisfy different requirements. The following table can help the designer.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
R_1	68 Ω	Bridge Resistors	R_1 controls the receiving gain. The ratio R_2/R_1 fixes the amount of signal delivered to the line. R_1 helps in fixing the DC characteristic (see R_3 note).
R_2	330 Ω		
R_3	30 Ω	Line current sensing. Fixing DC characteristic.	The relationships involving R_3 are: • $Z_{ML} = (20\ R_3 \,//\, Z_B) + R_1$ • $G_s = K \cdot \frac{Z_L \,//\, Z_{ML}}{R_3}$ • $V_L = (I_L - I_o)(R_3 + R_1) + V_o$; $V_o = 3.8V$. Without any problem it is possible to have a Z_{ML} ranging from 500 up to 900 Ω.
R_4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R_4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (See fig. 12).
R_5	7.5 KΩ	Balance Network	The balance network has two possible impedance levels, selected by the circuit referring to the line current (i.e. to the line length) in order to optimize the sidetone. It's possible to change R_5, R_6, R_7 values in order to improve the matching to different lines; in any case: $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ with the two possible values for Z_B: $Z_{B(1)} = R_7 + R_6 \,//\, C_4$ (long lines) $Z_{B(2)} = R_7 + (R_6 \,//\, R_5) \,//\, C_4$ (short lines) (see fig. 13).
R_6	5.1 KΩ		
R_7	1 KΩ		
$R_8 - R_8'$	1.8 KΩ	Receiver impedance matching	R_8 and R_8' must be equal; the suggested value is good for matching to piezoceramic capsule; there is no problem in increasing and decreasing (down to 0 Ω) this value, but when low resistance levels are used a DC decoupling must be inserted to stop the current due to the receiver output offset voltage (max 400 mV).
R_9	3.6 KΩ	Microphone impedance matching	The suggested value is typical for a piezoceramic microphone, but it is possible to choose R_9 in a wide range.
C_1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency.
C_2	47 nF	Matching to a capacitive line	C_2 changes with the characteristics of the transmission line.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
C_3	82 nF	Receiving gain flatness.	C_3 depends on balancing and line impedance versus frequency.
C_4	22 nF	Balance network.	See note for R_7, R_6, R_5.
C_5	0.33 μF	DC filtering	The C_5 range is from 0.1 μF to 0.47 μF. The lowest value is ripple limited, the higher value is starting up time limited.
C_6 - C_7	1000 pF	RF bypass.	
C_8	1 μF	DC decoupling for receiving input.	

Fig. 12 - Sending and receiving gain vs. line current

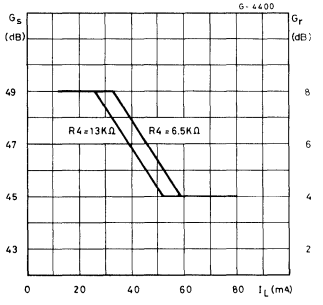
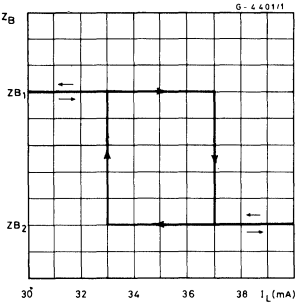


Fig. 13 - Balance network impedance vs. line current

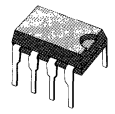


LS188

MICROPHONE AMPLIFIER

- VERY FEW EXTERNAL COMPONENTS NEEDED
- BUILT IN PARTIAL BRIDGE
- HIGH IMMUNITY AGAINST EMI
- ACCURATE GAIN CONTROL
- NO CAPACITOR REQUIRED
- WIDE OPERATING VOLTAGE AND CURRENT RANGE
- PROGRAMMABLE DC CHARACTERISTICS

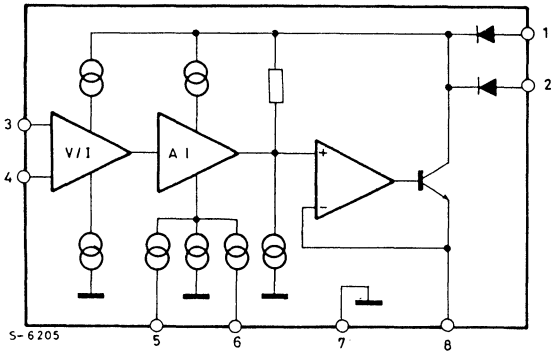
The LS188B/LS188CB monolithic microphone amplifiers are designed to be used with several kinds of transducers. They can replace the carbon microphone in telephones and may also be used in cassette recorder, walky talkies, or infrared receiver applications. The circuits are assembled in a 8-pin Dual in Line Package. The LS188B/LS188CB consist of a differential input amplifier, internal reference and a current modulator stage enabling the device to send the amplifier speech to the line.



Minidip Plastic

ORDERING NUMBER: LS188B
LS188CB

BLOCK DIAGRAM

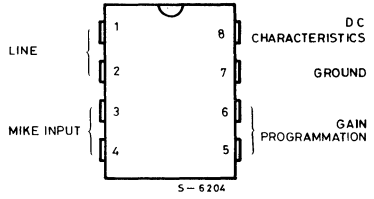


LS188

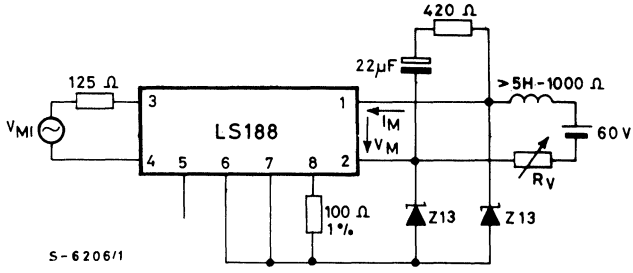
ABSOLUTE MAXIMUM RATINGS

V_M	Microphone voltage (3ms duration)	20	V
I_M	Microphone current	150	mA
P_{tot}	Power dissipation	600	mW
T_{op}	Operating temperature	-30 to 70	°C

CONNECTION DIAGRAM
(Top view)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit at 25°C with f = 300Hz to 3400 Hz unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
G_S	Sending gain for B type for CB type	V_{MI} = 1mV f = 1KHz Pin 5 floating I_M = 15mA Pin 5 floating	 41.5 39.5	 42.5 40.5	 43.5 41.5	dB
G	Gain spread vs. temperature	-25°C T_{amb} +60°C			± 1	dB
G	Gain spread vs. polarity	I_M = ± 15mA			± 0.3	dB
G	Gain spread vs. line current	V_{MI} = 1mV f = 1KHz I_M = 7 to 60mA I_{ref} = 15mA			± 1	dB
V_{1-7}	Microphone voltage	I_M = 7mA I_M = 15mA I_M = 40mA		4.5	 5.9 8.65	V V V
	Differential resistance and output impedance	I_M = 7 to 60mA		120	200	Ω
	Frequency response	I_M = 15mA			± 1	dB
	Sending noise	V_{MI} = 0			-67	dBmp
	Input impedance for B type for CB type	I_M = 7 to 60mA	 10 7.3	 15 9.75	 20 12.2	KΩ
	Distortion	f_{ref} = 1KHz I_M = 7 to 15mA V_o = 0.4V I_M = 15 to 60mA V_o 1.25V			 2 7	 % %
I_q	Quiescent current			1		mA

Gain versus pin 5/6 connection for LS188B

pin 6 / pin 5	Floating	Grounded
Floating	42.5dB	50dB
Grounded	48dB	53dB

Gain versus pin 5/6 connection for LS188CB

pin 6 / pin 5	Floating	Grounded
Floating	40.5dB	48dB
Grounded	46dB	51dB

Intermediate values of G_S are obtained by right resistors at pins 5 or 6.

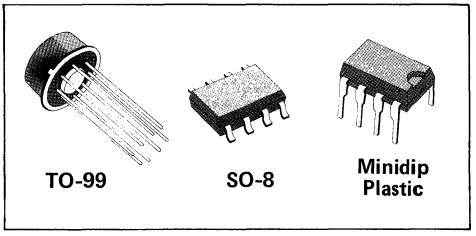
LS204

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

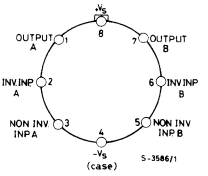
The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc). The LS204 series is available with hermetic gold chip (8000 series).

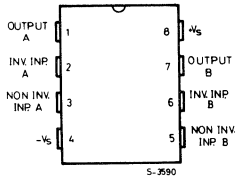


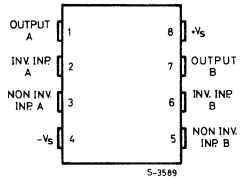
ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	μpackage
V_s	Supply voltage		± 18V	
V_i	Input voltage		$\pm V_s$	
V_i	Differential input voltage		$\pm (V_s - 1)$	
T_{op}	Operating temperature for **LS 204**		-25 to 85°C	
	LS 204A		-55 to 125°C	
	LS 204C		0 to 70 °C	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	665 mW	400 mW
T_j	Junction temperature	150°C	150°C	150°C
T_{stg}	Storage temperature	-65 to 150°C	-55 to 150°C	-55 to 150°C

LS204

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

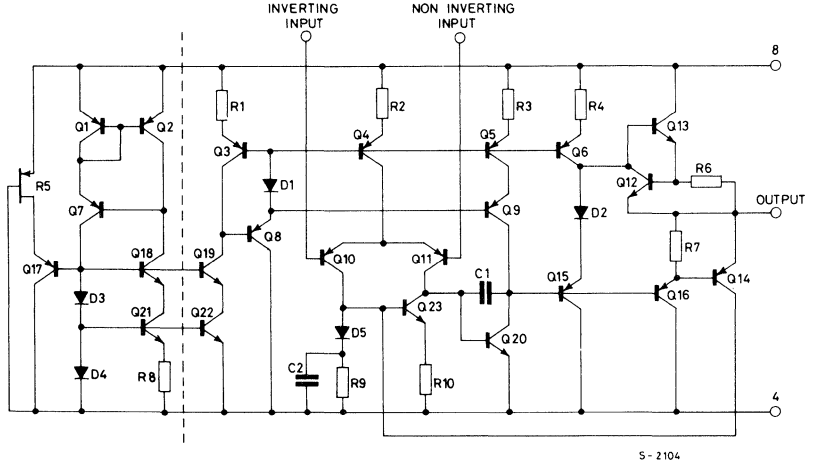






Type	TO-99	Minidip	SO-8
LS 204	LS 204 TB	—	LS 204 M
LS 204 A	LS 204 ATB	—	—
LS 204 C	LS 204 CTB	LS 204 CB	LS 204 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200 °C/W

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	LS 204/LS204A			LS 204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			0.7	1		0.8	1.5	mA
I_b	Input bias current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input resistance	f = 1 KHz		1			0.5		MΩ
V_{os}	Input offset voltage	$R_g \leqslant 10$ KΩ		0.5	2.5		0.5	3.5	mV
		$R_g \leqslant 10$ KΩ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$		5			5		µV/°C
I_{os}	Input offset current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	$T_{min} < T_{op} < T_{max}$ R_L= 2KΩ V_s= ±15V V_s= ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20 KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1 KHz R_g = 50Ω R_g = 1 KΩ R_g = 10 KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	G_v= 20 dB R_L= 2KΩ V_o= 2 Vpp f = 1 KHz		0.03	0.1		0.03	0.1	%
V_o	DC output voltage swing	R_L= 2KΩ V_s= ±15V V_s= ± 4V	±13	±3		±13	±3		V
V_o	Large signal voltage swing	R_L= 10 KΩ f = 10 KHz		28			28		Vpp
SR	Slew rate	unity gain R_L= 2KΩ	0.8	1.5			1		V/µs
CMR	Common mode rejection	V_i= 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply voltage rejection	V_i= 1V f = 100 Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel separation	f = 1 KHz	100	120			120		dB

Note:

	LS 204	LS 204A	LS 204C
$T_{min.}$	-25°C	-55°C	0°C
$T_{max.}$	+85°C	+125°C	+70°C

Fig. 1 - Supply current vs. supply voltage

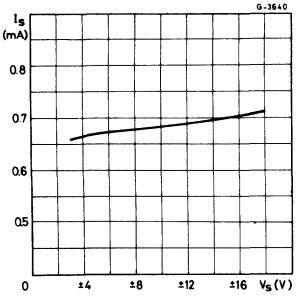


Fig. 2 - Supply current vs. ambient temperature

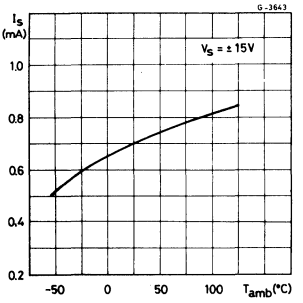


Fig. 3 - Output short circuit current vs. ambient temperature

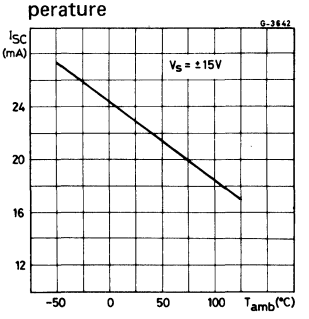


Fig. 4 - Open loop frequency and phase response

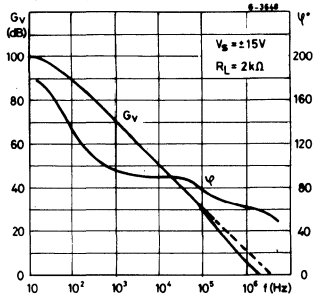


Fig. 5 - Open loop gain vs. ambient temperature

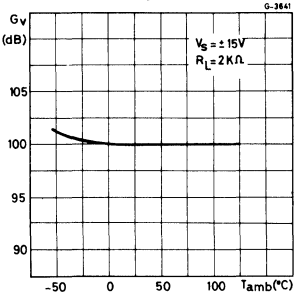


Fig. 6 - Supply voltage rejection vs. frequency

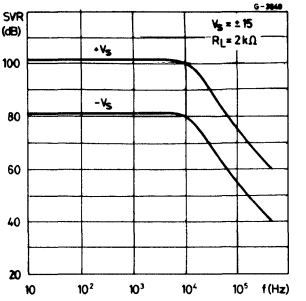


Fig. 7 - Large signal frequency response

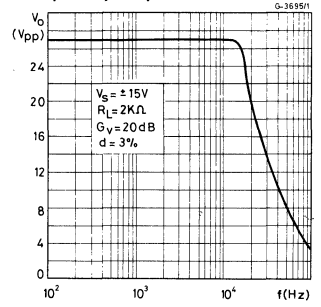


Fig. 8 - Output voltage swing vs. load resistance

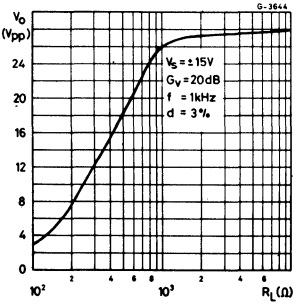
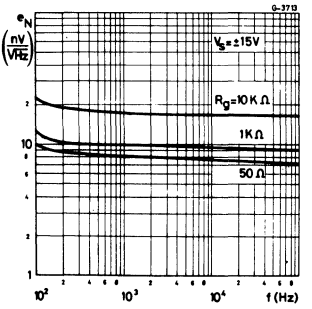


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

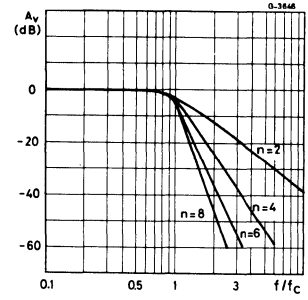
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband

Fig. 10 - Amplitude response



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

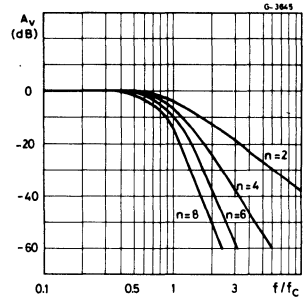
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs
- Fast rise time.

Fig. 11 - Amplitude response

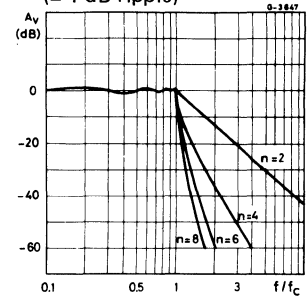


CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from ± 0.2 dB to ± 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

Fig. 12 - Amplitude response (± 1 dB ripple)



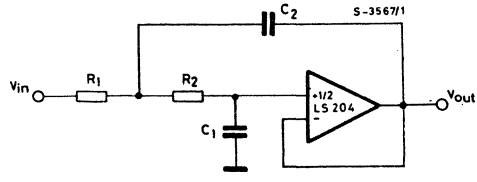
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1\ f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	-
	4	18	$3.0/f_c$	$5.4/f_c$	-
	6	21	$5.9/f_c$	$10.4/f_c$	-
	8	23	$8.4/f_c$	$16.4/f_c$	-
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	-
	4	28	$4.8/f_c$	$8.4/f_c$	-
	6	32	$8.2/f_c$	$16.3/f_c$	-
	8	34	$11.6/f_c$	$24.8/f_c$	-

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\,\xi\,\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:
$\omega_c = 2\pi\ f_c$ with f_c= cutoff frequency

ξ = damping factor.

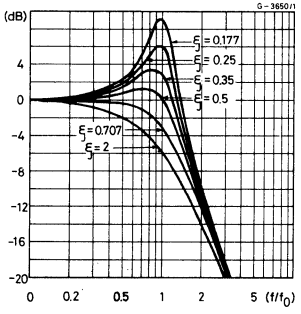
APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter: the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.
The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Tab. I

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_V= -3 dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

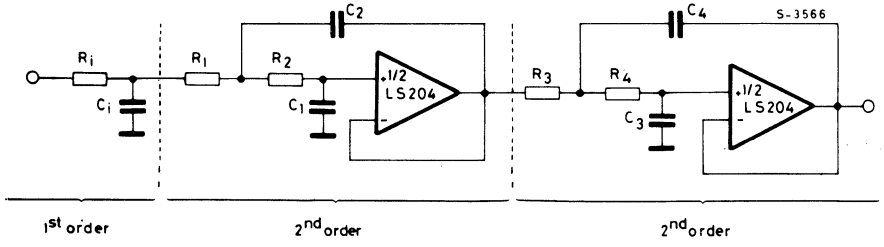
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1\ nF$ we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

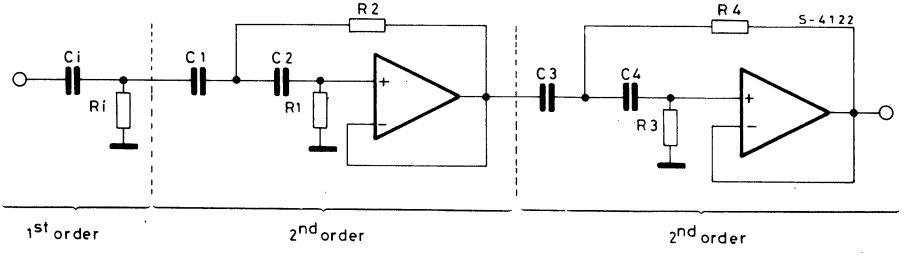
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.

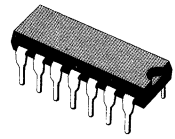


LS285

TELEPHONE SPEECH CIRCUITS

The LS285 is monolithic integrated circuits for replacement of the hybrid circuit (2-4 wire interface) in conventional telephones interfacing the two transducers to the line and providing a controlled amount of sidetone.
The same type of transducer can be used for both transmitter and receiver, usually a 350Ω dynamic type.
By sensing the line current, LS285 adjusts the gain in both directions to compensate for line attenuation.
Output impedance can be matched to the line, independent of transducer impedance.

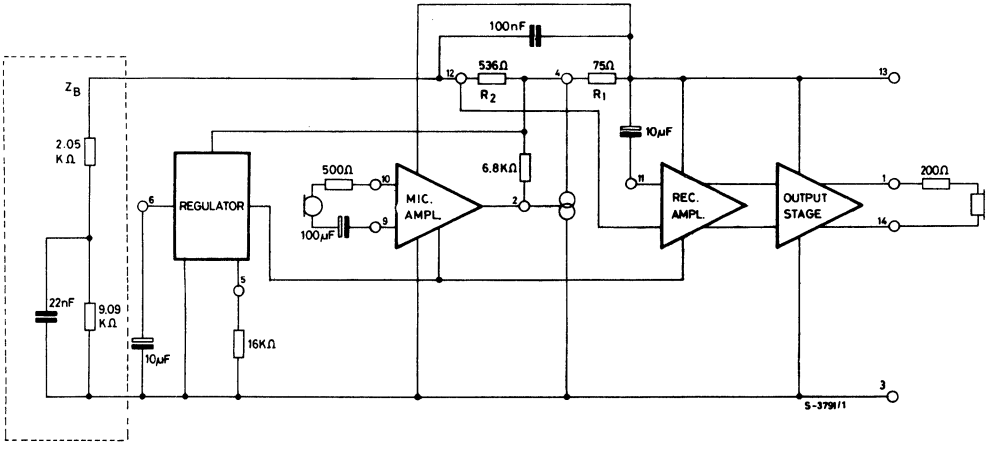
The LS285 is packaged in a 14 lead dual in-line plastic package.



DIP-14 Plastic
(0.4)

ORDERING NUMBER: U37070

BLOCK DIAGRAM

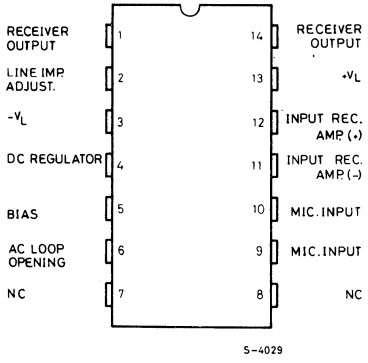


LS285

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward current	120	mA
I_L	Reverse current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{stg}	Storage and junction temperature	-55 to 150	°C
T_{op}	Operating temperature	-40 to 70	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

DESCRIPTION

The LS285 is based on a bridge configuration.
They contain a regulator block, a sending amplifier and a receiver amplifier.
The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length. It provides DC characteristics in line with CEPT standards.
The transmit/receiver amplifiers are connected to the line via an external bridge to provide sidetone attenuation.
The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line lenght. When he is hearing, the signal level on the receiver capsule is constant.
The amplifiers can also be matched to different transducers simply by varying external components. Gain variation over the operating temperature range is less than ± 1 dB.
The impedance to the line can be adjusted; without any change in circuit parameters; by changing an external resistor (6.8 KΩ at pin 2).

Basic circuit configuration

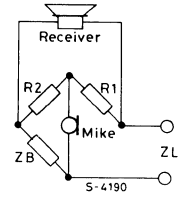


Fig. 1 - Test circuit

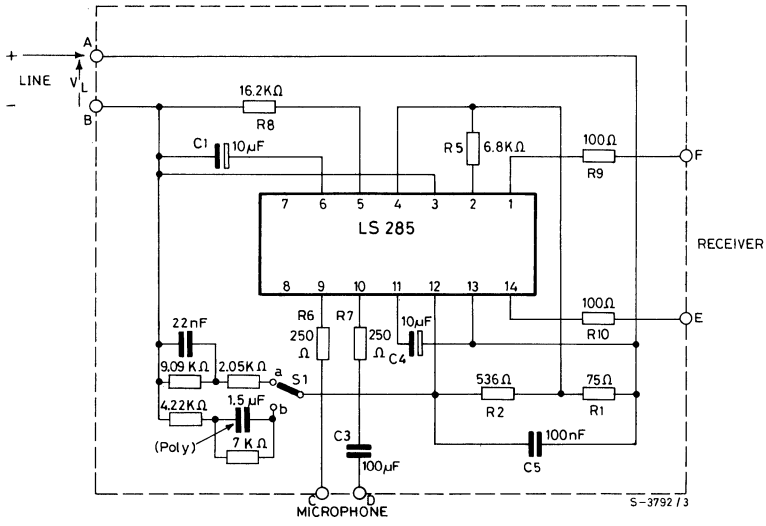
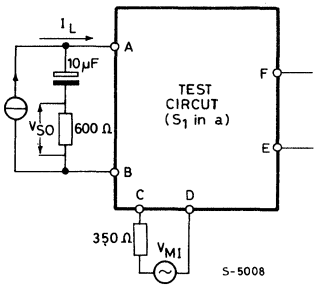
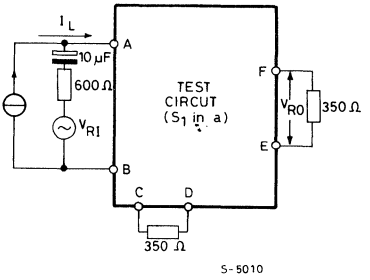


Fig. 2 - Sending gain



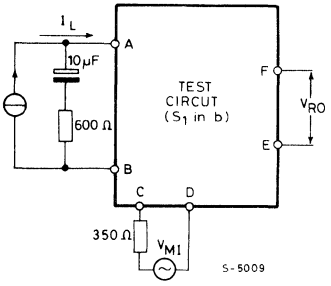
$$G_S = \frac{V_{SO}}{V_{MI}}$$

Fig. 3 - Receiving gain



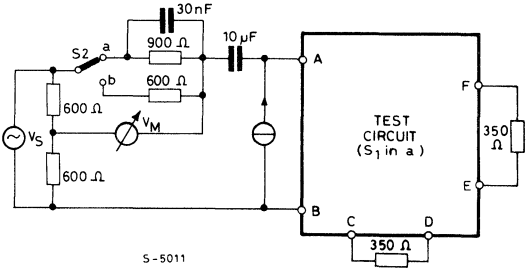
$$G_R = \frac{V_{RO}}{V_{RI}}$$

Fig. 4 - Sidetone



$$\text{Sidetone} = \frac{V_{RO}}{V_{MI}}$$

Fig. 5 - Return loss



$$R_L = \frac{V_s}{2\,V_M}$$

ELECTRICAL CHARACTERISTIC (Refer to the test circuit, T_{amb}= 25°C, f=300 Hz to 3400 Hz, S1, S2 in "a" unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_L	Line voltage	-15°C < T_{amb} < +45°C I_L= 80 mA I_L= 20 mA I_L= 10 mA	 10 5 3.8		 11.5 5.8 4.6	V	1
G_s	Sending gain	f = 1 KHz I_L= 15 mA I_L= 30 mA I_L= 60 mA I_L= 80 mA	 47.5 46.4 41.7 41		 51.5 50.5 45.1 44.3	dB	2
G_s	Sending gain variation vs. temp.	-15°C < T_{amb} < +45°C		0.8		dB	2
	Sending gain flatness	I_L= 10 to 80 mA f_{ref}= 1 KHz S1, S2 in (b)			± 0.5	dB	2
	Sending distortion	-15°C < T_{amb} < +45°C I_L= 10 to 15 mA V_{so}= 0.7V_p			2	%	2
		-15°C < T_{amb} < +45°C I_L= 15 to 80 mA V_{so}= 1 V_p			2	%	
	Sending noise	V_{MI}= 0V I_L= 60 mA		-73		dBmp	2
	Microphone amplifier impedance (pin 9-10)		95			Ω	1
	Max sending output (°)	I_L = 10 to 80 mA V_{MI}= 1V			3	V_p	2
G_R	Receiving gain	f = 1 KHz I_L= 15 mA I_L= 30 mA I_L= 60 mA I_L= 80 mA	 -13.6 -13.6 -18 -19		 -9.9 -10.6 -14.9 -16	dB	3
Δ G_R	Receiving gain variation vs. temperature	-15°C < T_{amb} < +45°C		0.25		dB	3
	Receiving gain flatness	f_{ref}= 1 KHz I_L= 10 to 80 mA S1, S2 in (b)			± 0.5	dB	3

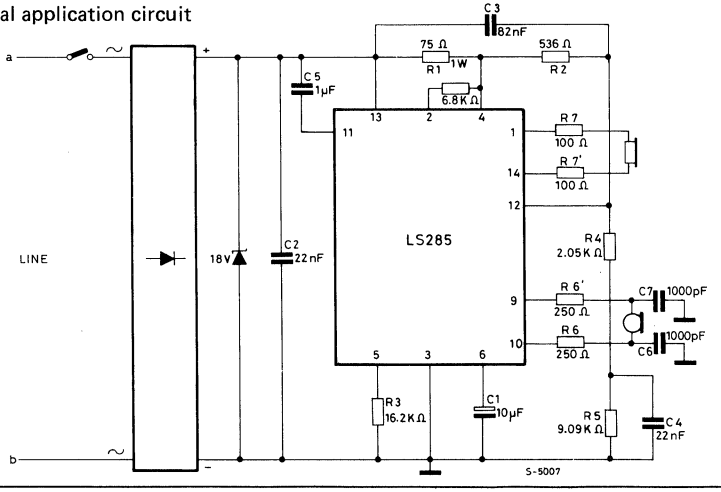
(°) This output is limited to allow for input overvoltages.

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
Receiving distorsion		I_L = 10 to 15 mA V_{RO} = 350 mV_p			2	%	3
	-15°C< T_{amb} < +45°C	I_L = 15 to 80 mA V_{RO} = 500 mV_p			2		
Receiving amplifier output impendance (pin 1-14)				110		Ω	1
Receiving noise	V_{RI} = 0 V psophometric	I_L = 60 mA		80		μV	3
Max receiving output current	I_L = 80 mA V_{RI} = 10V				3.6	mAp	3
Sidetone	f = 1 KHz	I_L = 20 mA		7		dB	4
		I_L = 80 mA		0		dB	
Return loss	S3 in (a)			14		dB	5
	S3 in (b)			14		dB	

(°) This output is limited to allow for input overvoltages.

Fig. 6 - Typical application circuit



APPLICATION INFORMATION

The following table shows the recommended values for the typical application circuit of fig. 6. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R1	75 Ω	Bridge resistors	The ratio R2/R1 fixes the amount of the signal delivered to the line. (see fig. 7)
R2	536 Ω		
R3	16.2 KΩ	Bias resistor	Changing R3 value it is possible to shift the gain characteristics. The value can be chosen from 15 KΩ to 20 KΩ. The recommended value assures the maximum swing (see fig. 9).
R4	2.05 KΩ	Balance network	In order to optimize the sidetone it is possible to change R4 and R5 values. In any case: $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ where Z_B= R4 + R5//C4.
R5	9.09 KΩ		
R6 and R6′	250 Ω	Microphone impedance matching	R6 and R6′ must be equal; 250Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to: $\Delta G_s = 20 \log \frac{Rx}{850\Omega}$ where Rx = R6 + R6′ + R_{mike}. The trend of ΔG_s as a function of Rx value is shown in fig. 8.
R7 and R7′	100 Ω	Receiver impedance matching	R7 and R7′ must be equal; 100Ω is a typical value for dynamic capsules
C1	10 μF	AC loop opening	Ensures a high regulator impedance for AC signals (≅ 20 KΩ). This capacitor should not be higher than 10 μF in order to have a short response time of the system.
C2	22 nF	Matching to a capacitive line	C2 changes with the characteristics of the transmission line.
C3	82 nF	High frequency roll-off	C3 determines the high frequency response of the circuit. It also acts as RF bypass.
C4	22 nF	Balance network	See note for R4 and R5.
C5	1 μF	DC decoupling for receiving input	
C6 and C7	1000 pF	RF bypass	

APPLICATION INFORMATION (continued)

Fig. 7 - Receiving gain variation vs. R1 value (with fixed R1/R2 ratio)

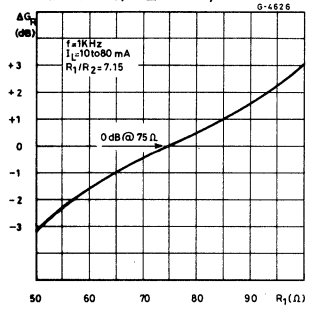


Fig. 8 - Sending gain variation vs. Rx value (see note for R6 and R6')

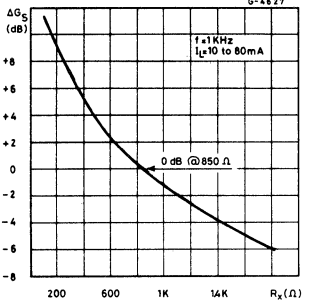
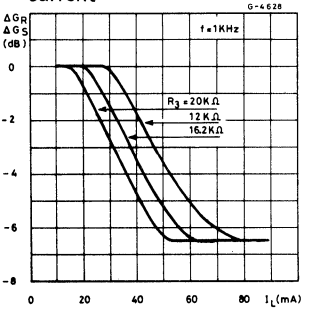


Fig. 9 - Sending and receiving gain variation vs. line current

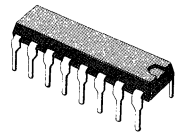


LS288

PROGRAMMABLE TELEPHONE SPEECH CIRCUIT

The LS288 is a monolithic integrated circuit in 16-lead dual in-line plastic package. Designed as a replacement for the hybrid circuit in telephone sets it performs all the functions previously carried out by this circuit.
With the LS288 it is possible to select the operating mode (fixed or variable gain). The device works with both piezoceramic and dynamic transducers and therefore its gain, both in sending and receiving paths, can be preset by means of two external resistors. This feature can also be obtained in AGC operating mode, when the device automatically adjusts the Rx/Tx gains to compensate for the line attenuation by sensing the line current.

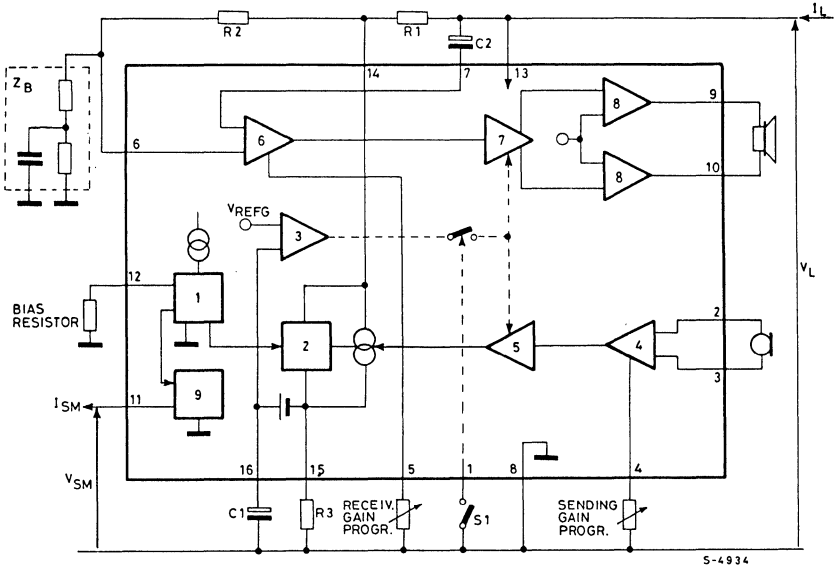
The LS288 can supply the decoupling FET when working with an electret microphone. Output impedance can be matched to the line independently of transducer impedance.



DIP-16 Plastic
(0.4)

ORDERING NUMBER: LS288B
LS288AB

BLOCK DIAGRAM

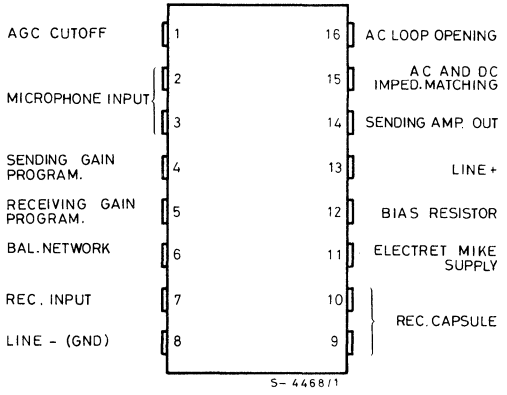


LS288

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM
(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUITS

Fig. 1 - Test Circuit

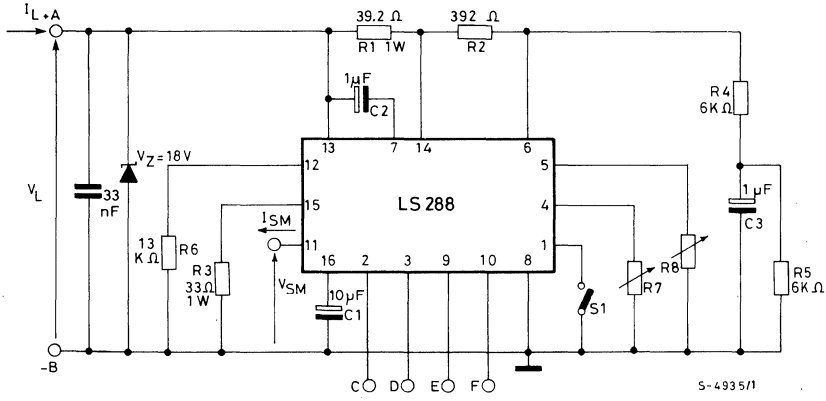
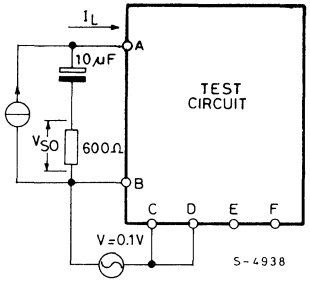
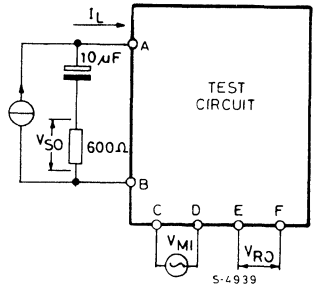


Fig. 2



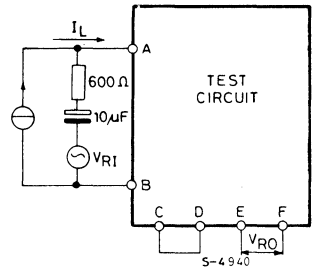
CMRR

Fig. 3



Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_s = \frac{V_{SO}}{V_{MI}}$

Fig. 4



$G_R = \frac{V_{RO}}{V_{RI}}$

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_{amb} = -25 to 50°C, f = 200 to 3400Hz, I_L = 12 to 120mA, unless otherwise specified)

Parameter		Test Conditions		Min	Typ	Max	Unit	Fig.
AGC off (pin 1 floating)								
V_L	Line voltage	T_{amb} = 25°C	I_L = 15mA I_L = 22mA I_L = 60mA I_L = 120mA	4.1	4.5	4.9 5.4 10 14	V	1
CMR	Common mode rejection	f = 1KHz		50			dB	2
G_S *	Sending gain (for B type)	I_L = 60mA T_{amb} = 25°C f = 1KHz R8 = 14.5KΩ V_{MI} = 2mV	 R7 = 8.9KΩ R7 = 31.1KΩ	 26 40.5		 28 43.5	dB	3
G_S *	Sending gain (for AB type)	I_L = 60mA T_{amb} = 25°C f = 1KHz R8 = 14.5KΩ V_{MI} = 2mV	 R7 = 8.9KΩ R7 = 31.1KΩ	 25 40		 29 44	dB	3
ΔG_S	Sending gain flatness (vs. freq.) for B type	V_{MI} = 2mV f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 0.5	dB	3
ΔG_S	Sending gain flatness (vs. freq.) for AB type	V_{MI} = 2mV f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 1	dB	3
ΔG_S	Sending gain flatness (vs. current) for B type	V_{MI} = 2mV f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 0.5	dB	3
ΔG_S	Sending gain flatness (vs. current) for AB type	V_{MI} = 2mV f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 1	dB	3
d_s	Sending distortion for B type	f = 1KHz R7 = 31.1KΩ R8 = 14.5KΩ	V_{so} = 450mV V_{so} = 775mV			2 5	%	3
d_s	Sending distortion for AB type	f = 1KHz R7 = 31.1KΩ R8 = 14.5KΩ	V_{so} = 450mV V_{so} = 775mV			4 5	%	3
	Sending noise for B type	R7 = 31.1KΩ R8 = 14.5KΩ	V_{MI} = 0 I_L = 12mA		-70		dBmp	3
R_{2-3}	Microphone input impedance pin 2-3	V_{MI} = 2mV f = 1KHz		11	16		KΩ	3
G_R *	Receiving gain for B type	I_L = 60mA T_{amb} = 25°C f = 1KHz R7 = 31.1KΩ V_{RI} = 0.3V	 R8 = 14.5KΩ R8 = 17.1KΩ	 0 3		 2 5	dB	4
G_R *	Receiving gain for AB type	I_L 60mA T_{amb} = 25°C f = 1KHz R7 = 31.1KΩ V_{RI} = 0.3V	 R8 = 14.5KΩ R8 = 17.1KΩ	 -1 2		 3 6	dB	4

(*) The sending and receiving gains are not completely indipendent but the variation in sending gain over the whole range of receiving gain (and vice-versa) is less then 0.5dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min	Typ	Max	Unit	Fig.
ΔG_R	Receiving gain flatness (vs. freq.) for B type	V_{RI} = 0.3V f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 0.5	dB	4
ΔG_R	Receiving gain flatness (vs freq.) for AB type	V_{RI} = 0.3V f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 1	dB	4
ΔG_R	Receiving gain flatness (vs. current) for B type	V_{RI} = 0.3V f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 0.5	dB	4
ΔG_R	Receiving gain flatness (vs. current) for AB type	V_{RI} = 0.3V f_{ref} = 1KHz	$I_{L\ ref}$ = 60mA			± 1	dB	4
d_R	Receiving distortion for B type	f = 1KHz R8 = 14.5KΩ R7 = 31.1KΩ	V_{RI} = 570mV V_{RI} = 1.1V			2 5	%	4
d_R	Receiving distortion for AB type	f = 1KHz R8 = 14.5KΩ R7 = 31.1KΩ	V_{RI} = 570mV V_{RI} = 1.1V			4 5	%	4
	Receiving noise for B type	R8 = 14.5KΩ V_{RI} = 0	I_L = 12mA R7 = 31.1KΩ		250		μV	4
R_{9-10}	Receiver output impedance (Pin 9 and 10)	V_{RO} = 50mV			30		Ω	
	Sidetone	f = 1KHz R7 = 31.1KΩ R8 = 14.5KΩ	V_{MI} = 2mV I_L = 12mA		22		dB	3
Z_{ML}	Line matching impedance	V_{RI} = 0.3V	f = 1KHz	650	750	850	Ω	4
	Max receiving output (click suppressor)	V_{RI} = 2V R8 = 14.5KΩ	I_L = 30mA R7 = 31.1KΩ		2.3		V_p	4
V_{SM}	Microphone supply voltage (Pin 11)	I_{SM} = 0.8mA		1.9		2.2	V	1

AGC on (pin 1 ground)

ΔG_S and ΔG_R **	Sending and receiving gain variation	T_{amb} = 25°C $I_{L\ ref}$ = 12mA f = 1KHz	I_L = 25mA I_L = 50mA I_L = 100mA	-1 -6 -7		1 -4 -5	dB	3-4

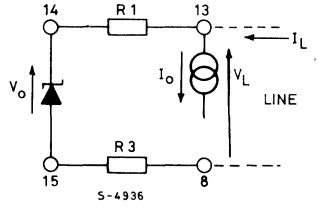
(**) Referred to any value fixed by means of R7 and R8.

CIRCUIT DESCRIPTION

1. DC Characteristic

In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristic V_L, I_L.
The DC characteristics of the LS288 is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3 (see the block diagram). The equivalent circuit is shown in fig. 5.

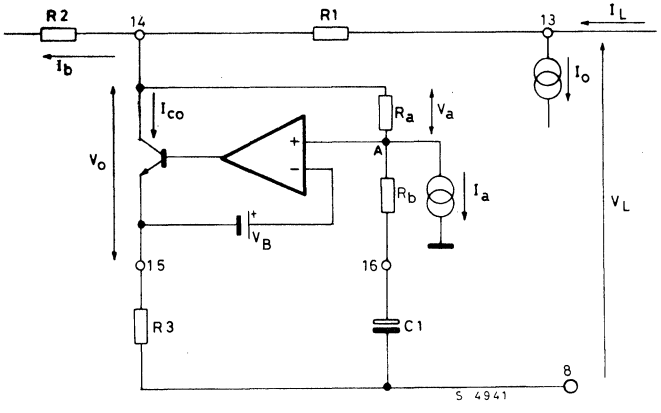
Fig. 5 - Equivalent DC load to the line



A fixed amount, I_o, of the total available current, I_L, is drained to allow the circuit to operate correctly. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 12.

The recommended minimum value of I_o is 7.5 mA with R pin 12 = 13 KΩ.
The voltage $V_o \cong 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (block 2) is controlled by a temperature compensated voltage reference (block 1). Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Fig. 6 - Circuit configuration of the shunt regulator



CIRCUIT DESCRIPTION (continued)

The difference $I_L - I_o$ flows through the shunt regulator since I_b is negligible.
I_a is an internal constant current generator; hence $V_o = V_B + I_a \cdot R_a = 3.8V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series with a battery.
It is important to note that the DC voltage at pin 16 is proportional to the line current $V_{16} = V_{15} + V_B = (I_L - I_o)\, R_3 + V_B$.

2. Two to four wires conversion

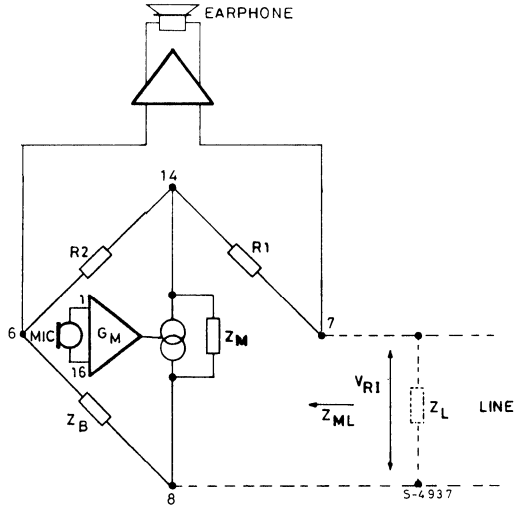
The LS288 performs the two wire (line) to four wire (microphone, earphone) conversion by means of a Wheatstone bridge configuration thus obtaining the proper decoupling between sending and receiving signals (see fig. 7).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 8 and 14). A small percentage of the signal power is lost on Z_B (since $Z_B \gg Z_L$); the main part is sent to the line via R_1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 6 and 7). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator which also acts as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{(14-8)}}{\Delta I_{(14-8)}}$.

Fig. 7 - Two to four wires conversion



CIRCUIT DESCRIPTION (continued)

From fig. 6, considering C_1 as a short circuit to the AC signal, any variation in ΔV_{14} generates a variation as follows:

$$\Delta V_{15} = \Delta V_A = \Delta V_{14} \frac{R_b}{R_a + R_b}$$

The corresponding current change is:

$$\Delta I = \frac{\Delta V_{15}}{R_3}$$

therefore

$$Z_M = \frac{\Delta V_{14}}{\Delta I} = R_3 (1 + \frac{R_a}{R_b})$$

The total impedance across the line connections (pin 13 and 8) is given by

$$Z_{ML} = R_1 + Z_M // (R_2 + Z_B)$$

By choosing $Z_M \gg R_1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R_3 (1 + \frac{R_a}{R_b})$$

The amplitude of the signal received across pins 6 and 7 can be changed using different values of R_1. (Of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must always be valid).

The received signal is related to the value of R_1 according to the approximated relationship:

$$V_R = V_{RI}\ 2 \frac{R_1}{R_1 + Z_M}$$

Note that if the value of R_1 is changed the transmission signal current is not changed, since the microphone amplifier is a transconductance amplifier.

3. Input and output amplifiers

The microphone amplifier (4) has a differential input stage with high impedance (min 11 KΩ) so allowing a good matching to the microphone by means of an external resistor without affecting the sending gain.
The receiving output stage (8) is intended to drive both piezoceramic and dynamic capsules. It has low output impedance, a maximum voltage swing greater than 2 V_p and a peak current of 2 mA.
With very low impedance transducers, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

4. Gain Control

It is possible to set the LS288 gain characteristics by means of one pin (pin 1).
When the pin 1 is floating, the gains of the sending and receiving amplifiers do not depend on the line current (AGC off). When the pin 1 is grounded the LS288 automatically changes the gain to compensate for line attenuation (AGC on).

DESCRIPTION CIRCUIT (continued)

4.1. AGC OFF

In this conditions, as already mentioned, both the sending and the receiving gain are fixed. Their values are determined, independently for the two paths, by the two external resistors R_7 (for T_x, between pin 4 and ground) and R_8 (for R_x, between pin 5 and ground). R_7 values ranging from 8 KΩ up to 50 KΩ giving sending gains from 26 dB to 51 dB. R_8 values range from 8 KΩ to 23 KΩ giving receiving gains from -6 dB to +14 dB (see fig. 9 and 10).
This allows the LS288 to be used with a variety of different transducers.

Fig. 9 - Sending gain vs. R_7 value (AGC off)

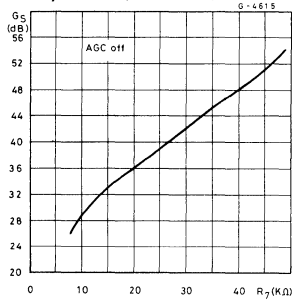
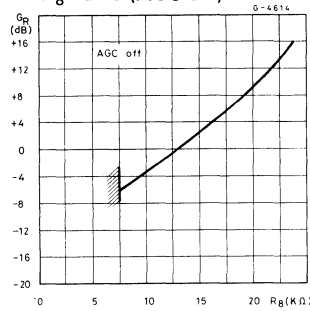


Fig. 10 - Receiving gain vs. R_8 value (AGC off)



4.2. AGC ON

Starting from any couple of gain values, fixed by the appropriate values of R_7 and R_8, the LS288 can automatically change the sending and receiving gains depending on the line current.
The line current is sensed across R_3 (see fig. 7) and transferred to pin 16 by the regulator.

$$V_{16} = V_B + V_{15} = V_B + (I_L - I_o) \cdot R_3$$

Following comparison with an internal reference V_{REFG} (see the block diagram) the voltage at pin 16 is used to modify the gain of the amplifiers (5) and (7) on both the sending and receiving paths.
The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.
The external resistors R_7 and R_8 fix the maximum value for the gains.
Minimum gain is reached for a line current of about 110 mA when the same drain current I_o of 7.5 mA is used.
When I_o is increased by means of the external resistor connected to pin 12 the two above mentioned line current values for the starting point and for the minimum gain increase accordingly.

5. DC Shunt Regulator

The LS288 has built into the chip a DC shunt regulator intended to supply the coupling FET when an electret microphone is used. It delivers 1 mAp current with a voltage of 2 Volts (typ) regardless of the line current.

CIRCUIT DESCRIPTION (continued)

Fig. 11 - Typical application circuit (piezoceramic transducers)

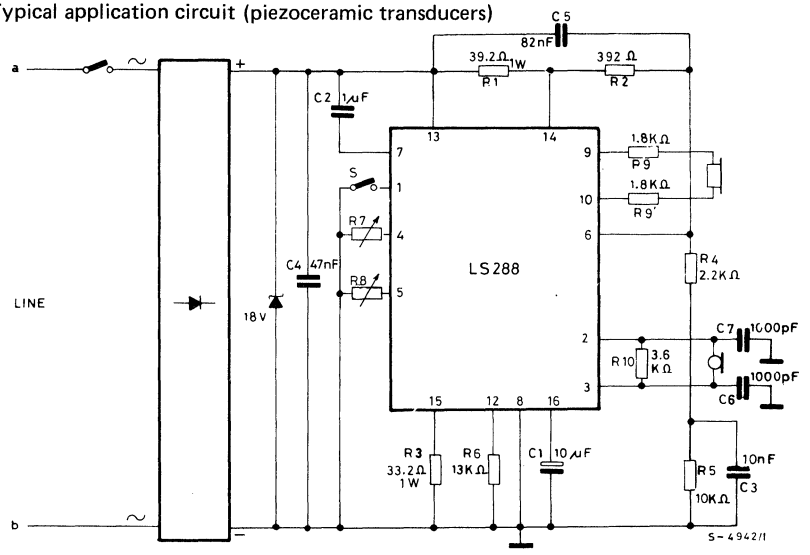
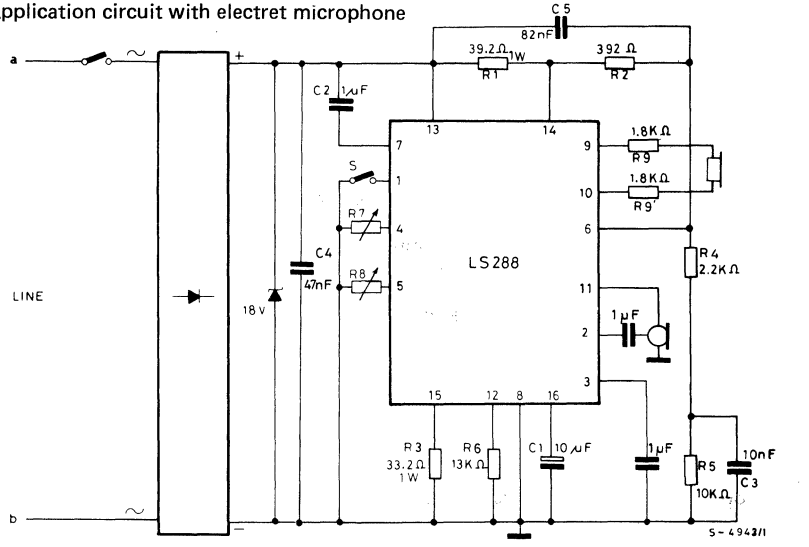


Fig. 12 - Application circuit with electret microphone



The following table can be helpful to the designer when choosing different values for the external components; it refers to the typical application circuit of fig. 11.

Component	Value	Function	Note
R_1	39.2 Ω	Bridge Resistors	R_1 controls the receiving gain. The ratio R_2/R_1 fixes the amount of signal delivered to the line. R_1 helps in fixing the DC characteristic (see R_3 note)
R_2	392 Ω		
R_3	33.2 Ω	Line current sensing Fixing DC characteristic	The relationships involving R_3 are: $- Z_{ML} = (25\ R_3 // Z_B) + R_1$ $- G_s = K \cdot \frac{Z_L // Z_{ML}}{R_3}$ $- V_L = (I_L - I_o)\ (R_3 + R_1) + V_o$ $[\ V_o = 3.8V\ ]$ Values of Z_{ML} ranging from 650 up to 850Ω are easily obtainable.
R_4	2.2 KΩ	Balance Network	In order to optimize the sidetone it is possible to change R_4 and R_5 values; in any case the following relationship applies: $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ where $Z_B = R_4 + R_5 // X_{C3}$
R_5	10 KΩ		
R_6	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current.
R_7	8 to 50 KΩ	Sending gain programming Resistor	
R_8	8 to 23 KΩ	Receiving gain programming Resistor	
R_9, R_9	1.8 KΩ	Receiver impedance matching	R_9 and R_9' must be equal; the suggested value is good for matching to piezoceramic capsule; there is no problem in increasing and decreasing (down to 0Ω) this value, but when low resistance levels are used DC decoupling must be inserted to stop the current due to the receiver output offset voltage (max 400 mV).
R_{10}	4 KΩ	Microphone impedance matching	The suggested value is typical for a piezoceramic microphone, but it is possible to choose R_{10} from a wide range of values: $R_{Mike} = R_{10} // R_{pin\ 2-3}$.

APPLICATION INFORMATION (continued)

Component	Value	Function	Note
C_1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low line current. A lower value gives an alteration of the AC line impedance at low frequency.
C_2	1 μF	DC decoupling for receiving input	
C_3	10 nF	Balance network	See note for R_4 and R_5.
C_4	47 nF	Matching to a capacitive line	C_4 must be chosen according to the characteristics of the transmission line.
C_5	82 nF	Receiving gain flattness	C_5 depends on balancing and line impedance versus frequency.
C_6, C_7	1000 pF	RF bypass	

LS346

POLARITY GUARD WITH VERY LOW VOLTAGE DROP FOR TELEPHONE APPLICATION

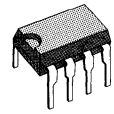
The LS346 is a monolithic integrated circuit designed to work as polarity guard, particularly in telephone applications where a very low voltage drop is required, and DTMF dialling system is used.

Typically it exhibits a total drop of 150mV with a flowing current of 10mA increasing to 700mV with 100mA.

A small amount of the total current: is drained by the LS346 to operate.

In addition to LS346 limits the voltage at the polarized side to 16V so replacing the zener diode usually palced before the electronic telephone speech circuit.

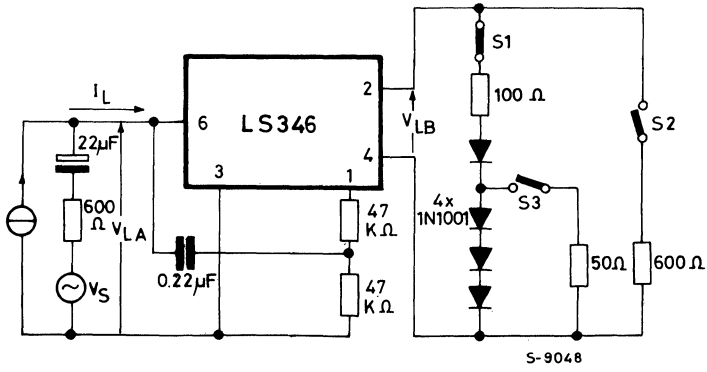
The device is assembled in a standard plastic minidip.



Minidip

ORDER NUMBER: LS346

TEST CIRCUIT

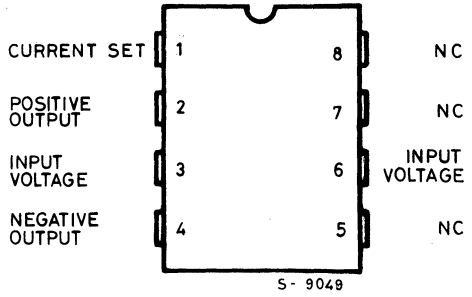


LS346

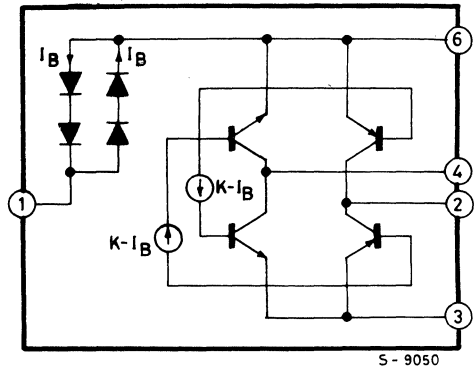
ABSOLUTE MAXIMUM RATINGS

I_{in}	Input current (steady state)	150	mA
V_{in}	Max input voltage	22	V
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}	Storage and junction temperature	-55 to 150	°C

CONNECTION DIAGRAM
(Top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, S1 closed, S2 and S3 open, T_{amb} = 25°C, f = 200 to 3400Hz unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Current consumption	I_L = 10mA I_L = 50mA I_L = 100mA		1 3 5	1.35 4.5	mA
Voltage drop (DC) ($V_{6\text{-}2}$ + $V_{3\text{-}4}$)	I_L = 10mA I_L = 50mA I_L = 100mA		0.15 0.4 0.7	0.25 0.7	V
Voltage drop (AC) 20 Log (V_{LB}/V_{LA})	S1 open S2 closed I_L = 10 to 100mA f = 1KHz		0.25	0.5	dB
Parallel input imp.	I_L = 10 to 100mA		20		KΩ
Operating voltage (DC) V_{LA}	I_L = 5mA S1, S3 closed - S2 open	1.4			V
Flatness vs. frequency	f_{rlf} = 1KHz		0.4		dB

APPLICATION CIRCUIT

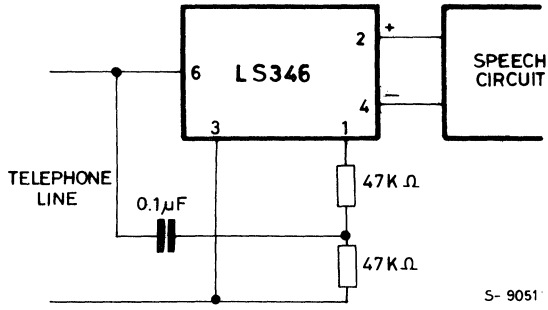


Fig. 1 - Drop voltage line current

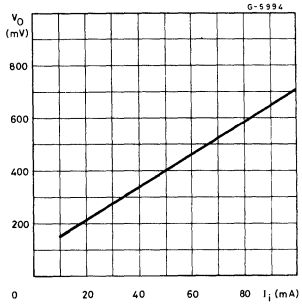
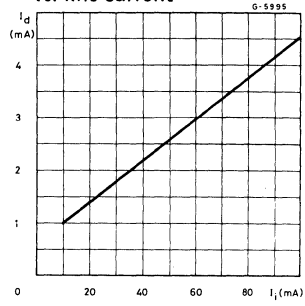


Fig. 2 - Current consumption vs. line current

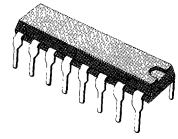


LS356

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

The LS356 is a monolithic circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typical dynamic capsules, but the device can also work with **piezoceramic ones**). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS356 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer). The LS356 basic functions are the following:

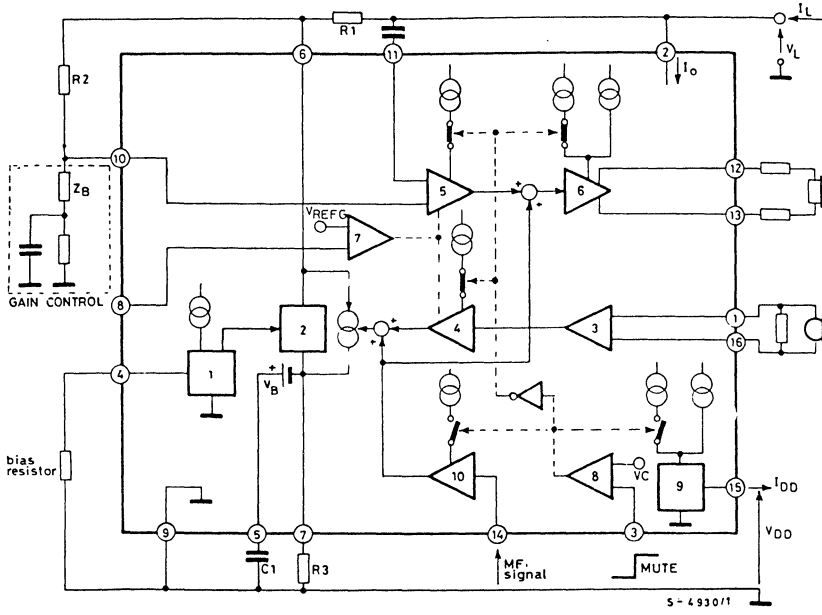
- It presents the proper DC path for the line current.
- It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing either the line current or the line voltage. **In addition, the LS356 can also work in fixed gain mode.**
- It acts as linear interface for MF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated by the M761.



DIP-16 Plastic
(0.4)

ORDERING NUMBER: LS356B
LS356AB

BLOCK DIAGRAM



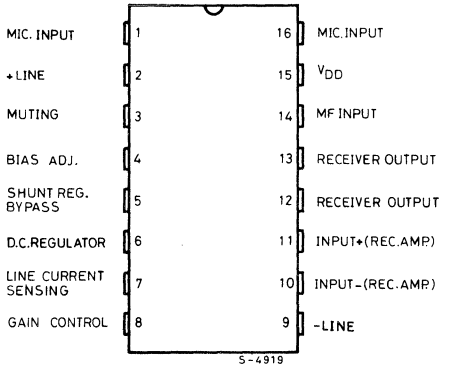
LS356

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM

(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUITS

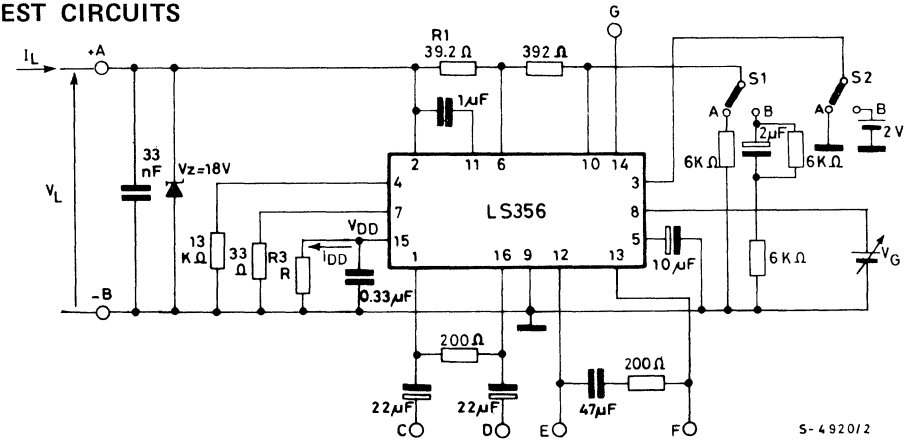
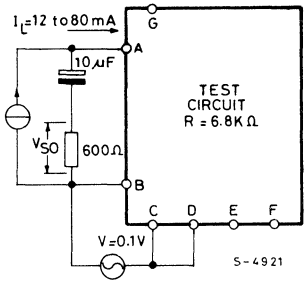
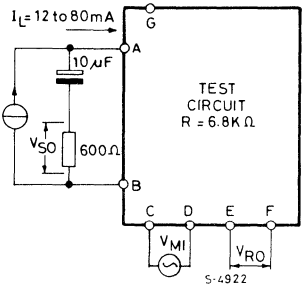


Fig. 1



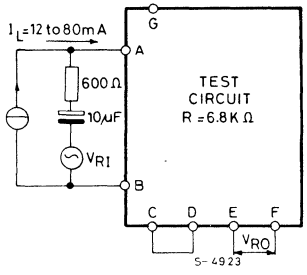
CMRR

Fig. 2



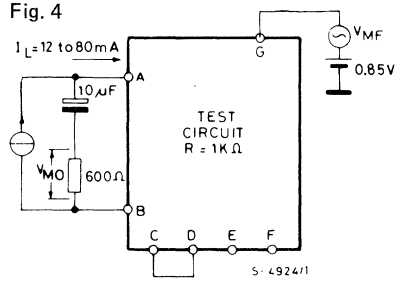
Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_s = \frac{V_{SO}}{V_{MI}}$

Fig. 3



$G_R = \frac{V_{RO}}{V_{RI}}$

Fig. 4



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_G= 1 to 2V, I_L= 12 to 80 mA, S1 and S2 in (a), T_{amb}= -25 to +50°C, f = 200 to 3400 Hz, unless otherwise specified).

Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION						
V_L Line voltage	T_{amb}= 25°C I_L= 12 mA I_L= 20 mA I_L= 80 mA	3.65		4.5 5 10	V	–
CMR Common mode rejection	f = 1 KHz	50			dB	1
G_s Sending gain for B type	T_{amb}= 25°C f = 1 KHz V_G= 2V V_{MI}= 2 mV V_G= 1V	44.5 48.5		46.5 50.5	dB	2
G_s Sending gain for AB type	T_{amb}= 25°C f = 1 KHz V_G= 2V V_{MI}= 2 mV V_G= 1V	44 48		47 51	dB	2
Sending gain flatness (vs. frequency)	V_{MI}= 2 mV f_{ref}= 1 KHz			± 1	dB	2
(*) Sending gain flatness for B type (vs. current)	V_G= 2V I_{ref}= 50 mA			± 0.5	dB	2
(*) Sending gain flatness for AB type (vs. current)	V_G= 2V I_{ref}= 50 mA			± 1	dB	2
Sending distortion for B type	f = 1 KHz V_{so}= 775 mV I_L= 16 mA V_{so}= 900 mV			2 10	%	2
Sending distortion for AB type	f = 1 KHz V_{so}= 775 mV I_L= 16 mA V_{so}= 900 mV			3 10	%	2
Sending noise for B type	V_{MI}= 0V V_G= 1V		-71	-69	dBmp	2
Sending noise for AB type	V_{MI}= 0V V_G= 1V			-65	dBmp	2
Microphone input impedance (pin 1-16)	V_{MI}= 2 mV	40			KΩ	–
Sending gain in MF operation	V_{MI}= 2 mV S2 in (b)	-30			dB	2
G_R Receiving gain for B type	V_{RI}= 0.3V V_G= 2V f = 1 KHz T_{amb}= 25°C V_G= 1V	-5 -0.5		-3 +1.5	dB	3
G_R Receiving gain for AB type	V_{RI}= 0.3V V_G= 2V f = 1 KHz T_{amb}= 25°C V_G= 1V	-5.5 -1.0		-2.5 +2.0	dB	3
Receiving gain flatness (vs. frequency)	V_{RI}= 0.3V f_{ref}= 1 KHz			± 1	dB	3
(*) Receiving gain flatness for B type (vs. current)	V_G= 2V I_{ref}= 50 mA			± 0.5	dB	3
(*) Receiving gain flatness for AB type (vs. current)	V_G= 2V I_{ref}= 50 mA			± 1	dB	3
Receiving distortion for B type	f = 1 KHz V_{RO}= 400 mV V_{RO}= 450 mV			2 5	%	3

* Fixed gain mode.

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
	Receiving distortion for AB type	f = 1 KHz V_{RO}= 400 mV V_{RO}= 450 mV			3 5	%	3
	Receiving noise for B type	V_{RI}= 0V		100	200	μV	3
	Receiving noise for AB type	V_{RI}= 0V			300	μV	3
	Receiver output impedance (pin 12-13)	V_{RO}= 50 mV		30		Ω	–
	Sidetone	f = 1 KHz T_{amb}= 25°C S1 in (b)			36	dB	2
Z_{ML}	Line matching impedance	V_{RI}= 0.3V f = 1 KHz	500	600	700	Ω	3
I_8	Input current for gain control (pin 8)				-10	μA	–

MULTIFREQUENCY SYNTHESIZER INTERFACE

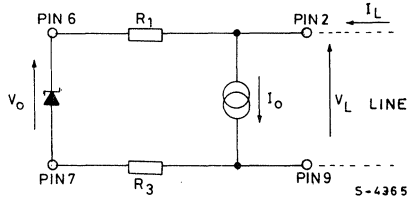
V_{DD}	MF supply voltage (Standby and operation)	S2 in (b)	2.4	2.5	2.7	V	–
I_{DD}	MF supply current Standby Operation	S2 in (b)	0.5 2			mA	–
	MF amplifier gain	$f_{MF\ in}$= 1 KHz $V_{MF\ in}$= 80 mV	15		17	dB	4
V_I	DC input voltage level (pin 14)	$V_{MF\ in}$= 80 mV		0.3 V_{DD}		V	–
R_I	Input impedance (pin 14)	$V_{MF\ in}$= 80 mV	60			KΩ	–
d	Distortion for B type	$V_{MF\ in}$= 110 mV			2	%	4
d	Distortion for AB type	$V_{MF\ in}$= 110 mV			4	%	4
	Starting delay time				5	ms	–
	Muting threshold voltage (pin 3)	Speech operation			1	V	–
		MF operation	1.6			V	–
	Muting standby current (pin 3)				-10	μA	–
	Muting operating current (pin 3)	S2 in (b)			+10	μA	–

CIRCUIT DESCRIPTION

1. DC characteristic

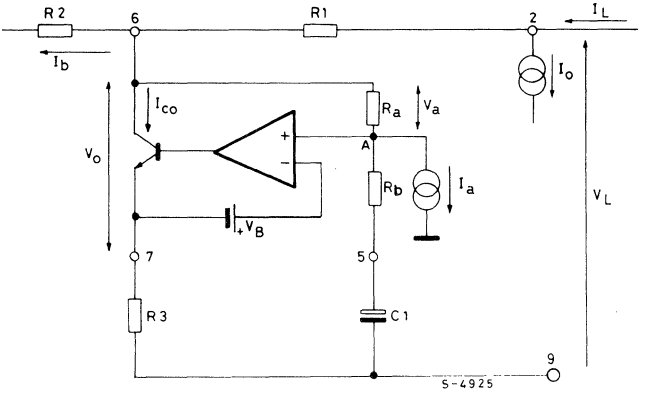
The fig. 5 shows the DC equivalent circuit of the LS356.

Fig. 5 - Equivalent DC load to the line



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).
The minimum value of I_o is 7.5 mA.
The voltage $V_o = 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Fig. 6 - Circuit configuration of the shunt regulator



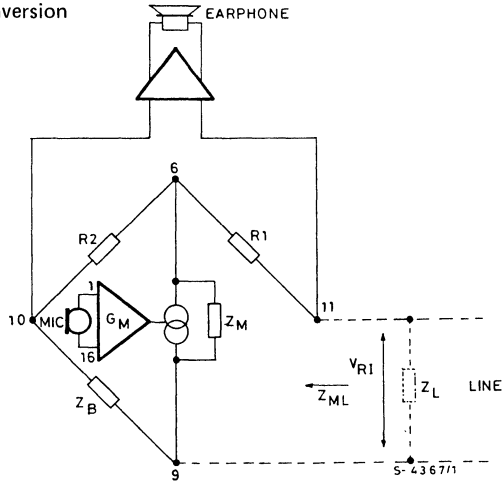
The difference $I_L - I_o$ flows through the shunt regulator being I_b negligible.
I_a is an internal constant current generator; hence $V_o = V_B + I_a \cdot R_a = 3.8V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery. It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).

CIRCUIT DESCRIPTION (continued)

2. Two to four wires conversion

The LS356 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 7).

Fig. 7 - Two to four wires conversion



For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R1}{R2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B \gg Z_L$); the main part is sent to the line via R1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$.

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation:

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3 \left(1 + \frac{R_a}{R_b}\right)$$

CIRCUIT DESCRIPTION (continued)

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R1 + Z_M \,//\, (R2 + Z_B)$$

By choosing $Z_M \gg R1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R3\,(1 + \frac{R_a}{R_b})$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).
The received signal is related to R1 value according to the approximated relationship:

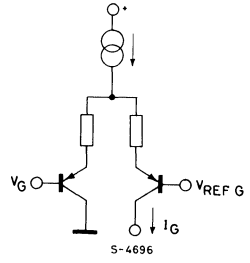
$$V_R = 2\,V_{RI}\,\frac{R1}{R1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. Automatic gain control

The LS356 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.
This function is performed by the circuit of fig. 8.

Fig. 8



The differential stage is progressively unbalanced by changing V_G in the range 1 to 2V (V_{REFG} is an internal reference voltage, temperature compensated).
It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken:

a) from the LS356 itself (both in variable and in fixed mode) and

b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain characteristic depending on the current.
In fact (see fig. 6):

$$V_5 = V_B + V_7 \cong V_B + (I_L - I_o)\,R3$$

The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.

CIRCUIT DESCRIPTION (continued)

Minimum gain is reached for a line current of about 52 mA for the same drain current $I_o = 7.5$ mA. When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.
It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too; for example using a division 1:1 (50K/50K) the AGC starting point shifts to about $I_L = 40$ mA, and the minimum gain is obtained at $I_L = 95$ mA.
In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain values (Rx, Tx) independently of the line conditions.
For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.
This type of operation meets for istance the requirements of the French standard. (See the application circuit of fig. 12).

4. Transducers interfacing

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain.
The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance, 100 Ω max; high current capability, 3 mAp).
When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).
With very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency interfacing

The LS356 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.
When no key of the keyboard is pressed the mute state is low and the LS356 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.
When one key is pressed, the M761 sends a "high state" mute condition to the LS 356. A voltage comparator (8) of LS356 drives internal electronic switches: the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.
This extra current is diverted by the receiving and sending section of the LS356 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.
A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber; the MF amplifier (10) delivers the dial tones to the sending paths.
The application circuit shown in fig. 9 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm) an external divider must be used (fig. 10).
The mute function can be used also when a temporary inhibition of the output signal is requested.

APPLICATION INFORMATION

Fig. 9 - Application circuit with multifrequency (EUROPE II STD)

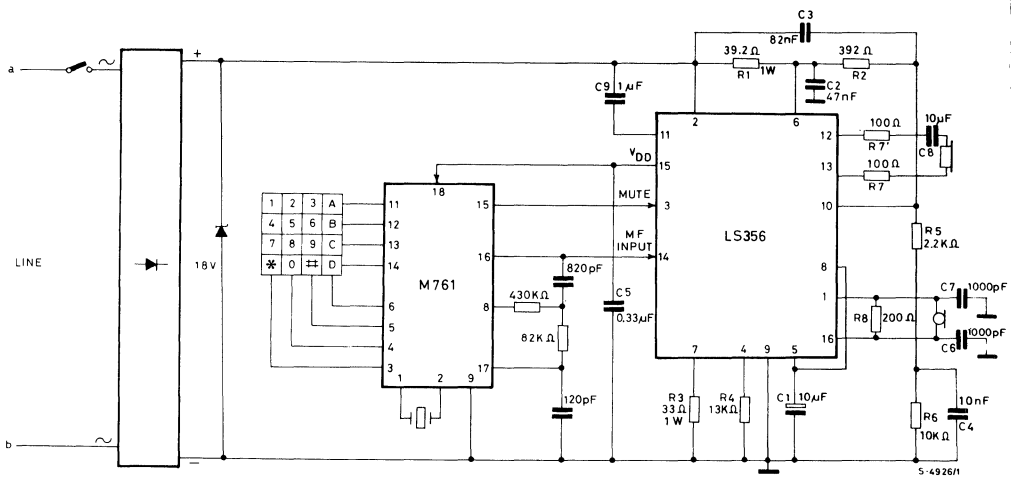
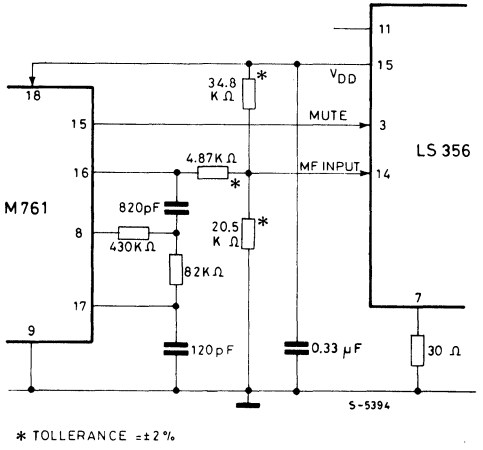


Fig. 10 - Application circuit with multifrequency (EUROPE I)



* TOLLERANCE ±2%

APPLICATION INFORMATION (continued)

Fig. 11 - Sending and receiving gain vs. line current (application circuit of fig. 13)

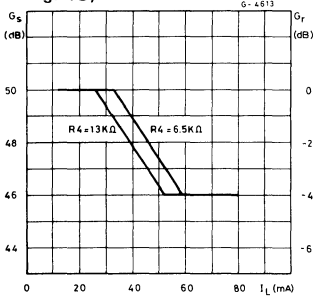


Fig. 12 - Application circuit without multifrequency

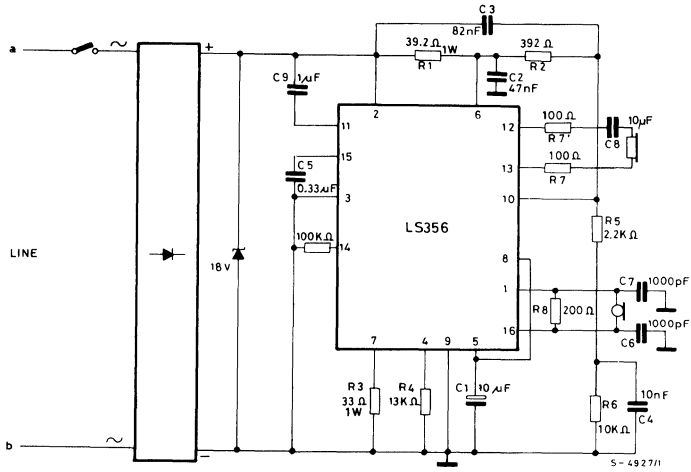
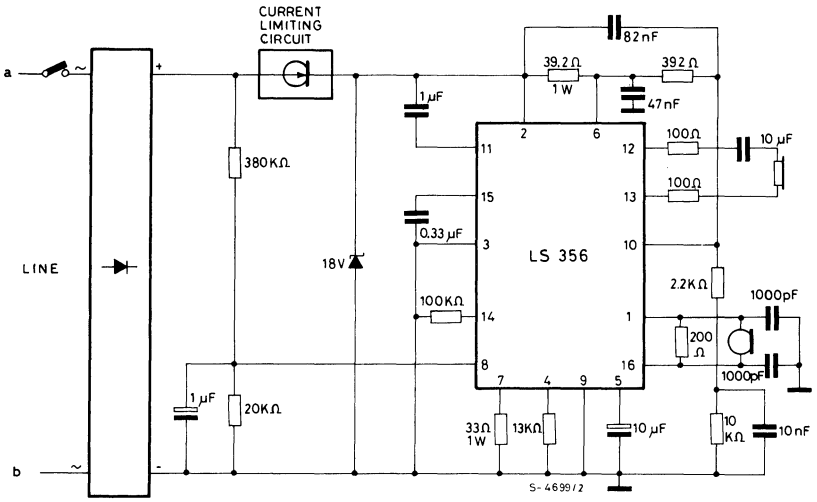
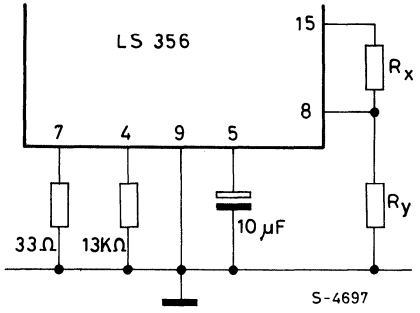


Fig. 13 - Application circuit with gain controlled by line voltage (French standard)



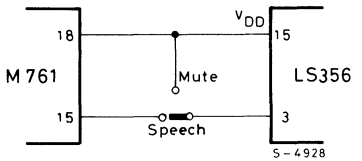
APPLICATION INFORMATION (continued)

Fig. 14 - Application circuit with fixed gain operation

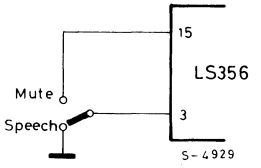


$R_y = 0$ Max gain condition
$R_x = 0$ Min gain condition

Fig. 15 - External mute function



a) with multifrequency



b) without multifrequency

In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.
The following table (refer to the application circuit of fig. 9) can help the designers.

Component	Value	Purpose	Note
R1	39.2 Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1W. The ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristic (see R3 note).
R2	392 Ω		
R3	33 Ω	Line current sensing. Fixing DC characteristic	The relationships involving R3 are: – $Z_{ML} = (20\ R3//Z_B) + R1$ – $G_s = K \cdot \frac{Z_L//Z_{ML}}{R3}$ – $V_L = (I_L - I_o)(R3 + R1) + V_o$; $V_o = 3.8V$. Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900 Ω. As far as the power dissipation is concerned, see R1 note.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
R4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point.
R5	2.2 KΩ	Balance Network	It is possible to change R5 and R6 values in order to improve the matching to different lines; in any case: $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ $Z_B = R5 + R6//X_{C4}$
R6	10 KΩ		
R7-R7'	100 Ω	Receiver impedance matching	R7 and R7' must be equal; the suggested value is good for matching to dynamic capsule; there is no problem in increasing and decreasing (down to 0 Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop the current due to the receiver output offset voltage (max 200 mV).
R8	200 Ω	Microphone impedance matching	The suggested value is typical for a dynamic microphone, but it is possible to choose R8 in a wide range.
C1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47 nF	Matching to a capacitive line	C2 changes with the characteristics of the transmission line.
C3	82 nF	Receiving gain flatness	C3 depends on balancing and line impedance versus frequency
C4	10 nF	Balance, network	See note for R5, R6
C5	0.33 μF	DC filtering	The C5 range is from 0.1 μF to 0.47 μF. The lowest value is ripple limited, the higher value is starting up time limited.
C6-C7	1000 pF	RF bypass	
C8	10 μF	Receiving output DC decoupling	See note for R7, R7'.
C9	1 μF	Receiving input DC decoupling	

LS388

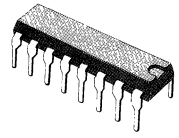
LOW CONSUMPTION TELEPHONE SPEECH CIRCUIT

The LS388 ia a monolithic integrated circuit in 16 lead dual-in-line plastic package, designed as a replacement for the hybrid circuit in telephone sets. It performs all the functions previously carried out by this circuit. The LS388 contains the following main functions:

- It presents the proper DC path for the line current, particular care being paid to have low voltage drop and a very low current consumption; the LS388 is fully operating at 6.5mA
- It handles the voice signal, performing the 2/4 wire interface and, when working with Automatic Gain Control, changing the gain on both sending and receiving amplifiers to compensate for line attenuation.

With the LS388 it is possible to select the operating mode (fixed or variable gain). The device work with both piezoceramic and dynamic transducers because of the programmability ot its gains, that can be preset by means of two external resistors.

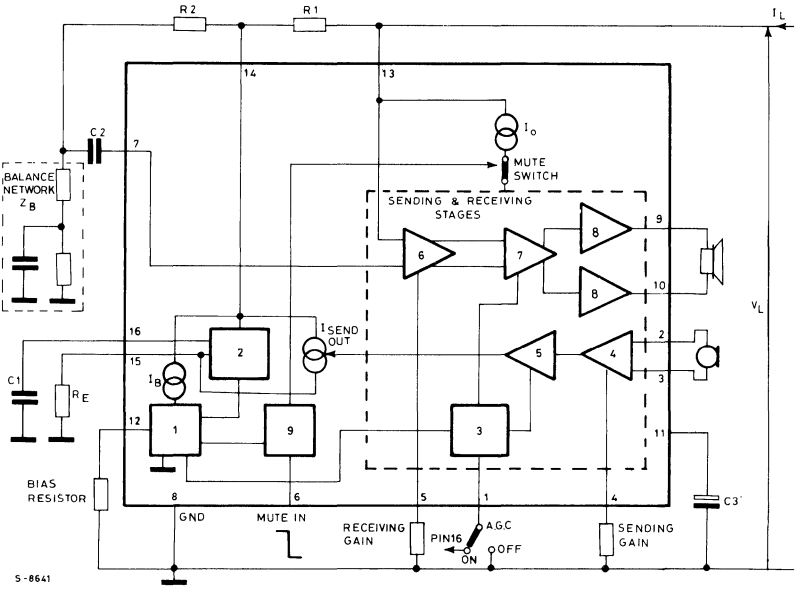
In addition, the LS388 can be set in power down state, where the device displays a very low current consumption (about 2mA) but still maintains DC and AC impedances to the line (for parallel operation with a DTMF generator).



DIP-16 Plastic (0.4)

ORDERING NUMBER: LS388B

BLOCK DIAGRAM

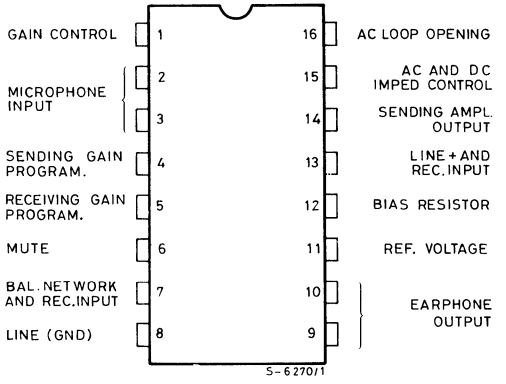


LS388

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUITS

Fig. 1

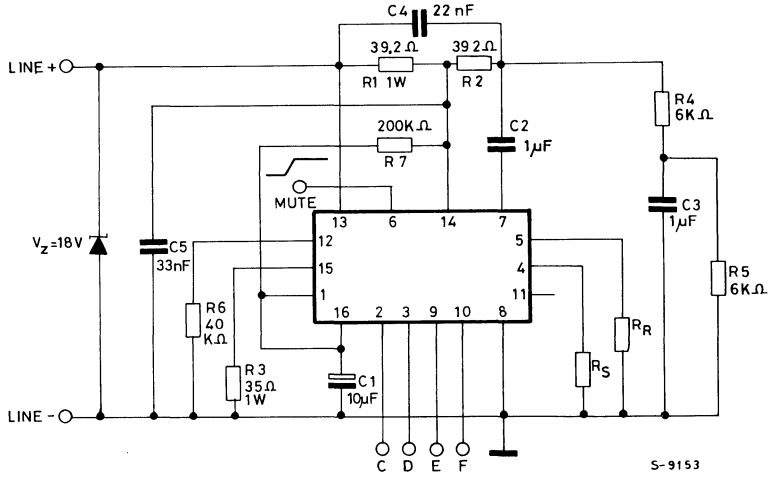


Fig. 2

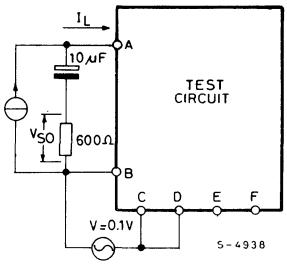


Fig. 3

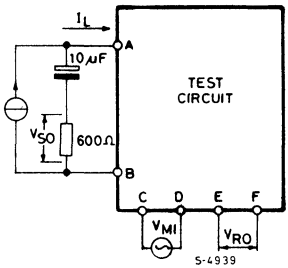
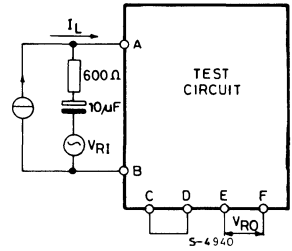


Fig. 4



ELECTRICAL CHARACTERISTICS (Refer to test circuits; T_{amb} = +25°C; F = 1KHz; I_L = 50mA; R_S = 71.5KΩ; R_R = 27.4KΩ; unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_L	Line voltage	I_L = 6.5mA I_L = 25mA I_L = 50mA I_L = 74mA	3.2	3.5 4.5 6.4 7.9	3.8	V	1
CMRR	Common mode rejection ratio	f = 1KHz	50			dB	2
G_S	Sending gain	V_{MI} = 0.5V	52.0		55.0	dB	3
ΔG_S	Sending gain variation vs. current	I_{ref} = 50mA, I_L = 25mA	4.0		6.0	dB	3
		I_{ref} = 50mA, I_L = 75mA	-1.5		+0.5	dB	
	vs. frequency	200Hz < f < 3.4KHz f_{ref} = 1KHz	-0.5		+0.5	dB	
	vs. R_S	ΔR_S = -1KΩ		-0.5		dB	
THD_s	Sending distortion	I_L = 6.5mA, V_{so} = 100mV			5	%	3
		I_L = 22mA, V_{so} = 850mV			5	%	
N_S	Sending noise	V_{MI} = 0mV		-65		dBm	3
Z_{MI}	Microphone impedance	V_{MI} = 0.5mV	11	15		KΩ	3
G_R	Receiving gain	V_{RI} = 570mV	5.0		8.0	dB	4
ΔG_R	Receiving gain variation vs. current	I_{ref} = 50mA, I_L = 25mA	4.0		6.0	dB	4
		I_{ref} = 50mA, I_L = 75mA	-1.5		0.5	dB	
	vs. frequency	200Hz < f < 3.4KHz f_{ref} = 1KHz	-0.5		0.5	dB	
	vs. R_R	ΔR_R = -1KΩ		-1		dB	
THD_r	Receiving distortion	I_L = 12mA, V_{RI} = 870mV			3	%	4
N_R	Receiving noise	V_{RI} = 0mV		-72		dBm	4
Z_{RO}	Receiving output impedance	V_{RO} = 50mV		30		Ω	4
	Sidetone	V_{MI} = 0.5mV		30		dB	3
Z_{ML}	Line matching impedance	V_{RI} = 100mV 12mA < I_L < 74mA	650		850	Ω	4

LS404

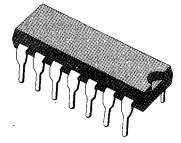
HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

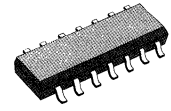
The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is partucularly intended for professional and telecom applications (active filters, etc.).

The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.

The LS404 is available with hermetic gold chip (8000 series).



DIP-14 Plastic
(0.25)



SO-14

ABSOLUTE MAXIMUM RATINGS

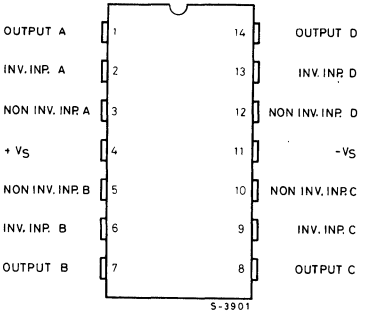
V_s	Supply voltage		± 18	V
V_i	Input voltage	(positive)	$+ V_s$	
		(negative)	$-V_s - 0.5$	V
V_i	Differential input voltage		$\pm (V_s - 1)$	
T_{op}	Operating temperature	**LS 404**	-25 to + 85	°C
		LS 404C	0 to + 70	°C
P_{tot}	Power dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage temperature		-55 to + 150	°C

LS404

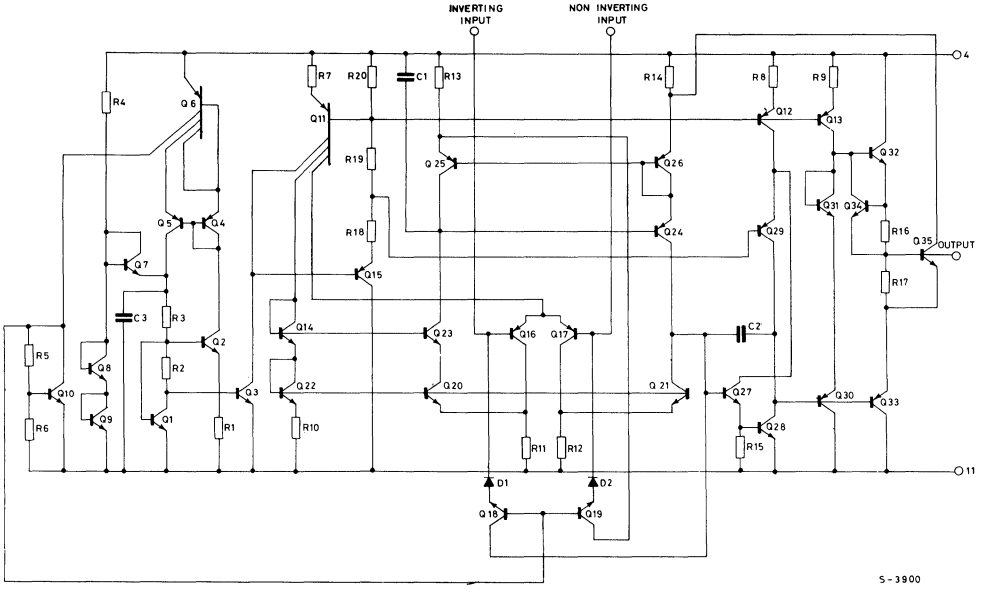
CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)

Type	DIP 14	SO-14
LS 404 LS 404C	— LS 404CB	LS 404M LS 404CM



SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			DIP 14	SO-14
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 12V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	LS 404			LS 404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			1.3	2		1.5	3	mA
I_b	Input bias current			50	200		100	300	nA
R_i	Input resistance	f = 1KHz		0.7			0.5		MΩ
V_{os}	Input offset voltage	R_g = 10KΩ		1	2.5		1	5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input offset current			10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	R_L = 2KΩ V_s = ±12V V_s = ±4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	unity gain R_L = 2KΩ f = 1 KHz V_o = 2Vpp f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC output voltage swing	R_L = 2KΩ V_s = ± 12V V_s = ± 4V	± 10	± 3		± 10	± 3		V
V_o	Large signal voltage swing	f = 10KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		Vpp
SR	Slew rate	unity gain R_L = 2KΩ	0.8	1.5			1		V/μs
CMR	Comm. mode rejection	V_i = 10V	90	94		80	90		dB
SVR	Supply voltage rejection	V_i = 1V f = 100Hz	90	94		86	90		dB
CS	Channel separation	f = 1KHz	100	120			120		dB

Fig. 1 - Supply current vs. supply voltage

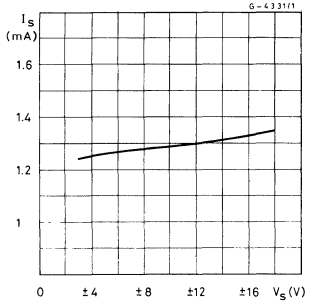


Fig. 2 - Supply current vs. ambient temperature

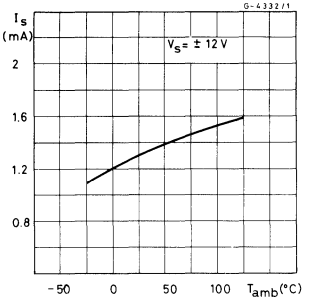


Fig. 3 - Output short circuit current vs. ambient temperature

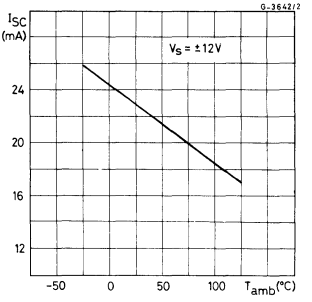


Fig. 4 - Open loop frequency and phase response

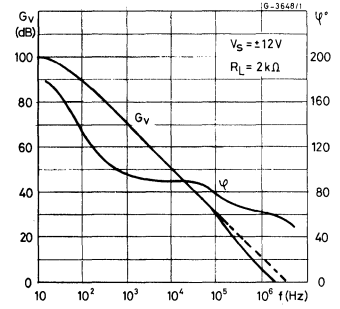


Fig. 5 - Open loop gain vs. ambient temperature

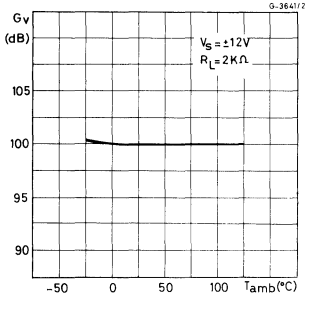


Fig. 6 - Supply voltage rejection vs. frequency

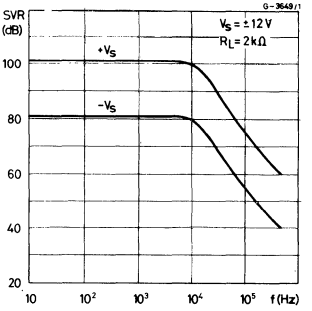


Fig. 7 - Large signal frequency response

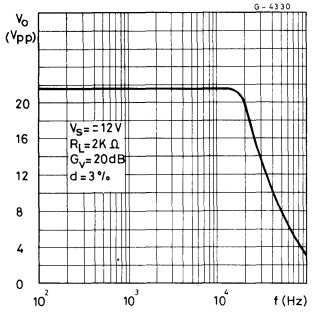


Fig. 8 - Output voltage swing vs. load resistance

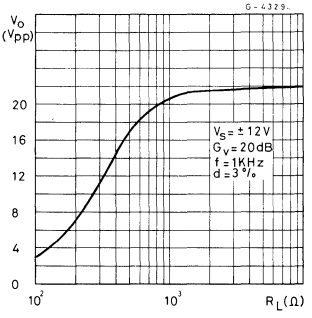
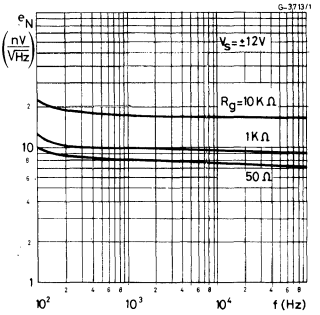


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

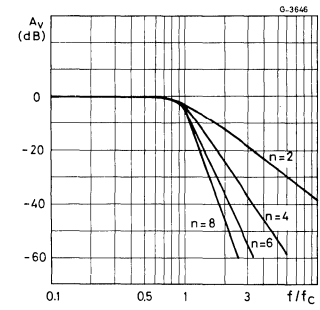
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Fig. 10 - Amplitude response



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

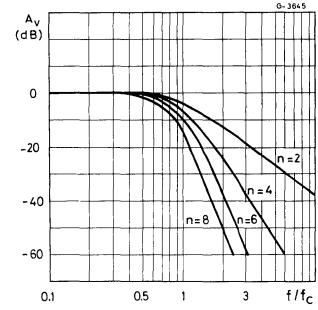
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs
- Fast rise time.

Fig. 11 - Amplitude response

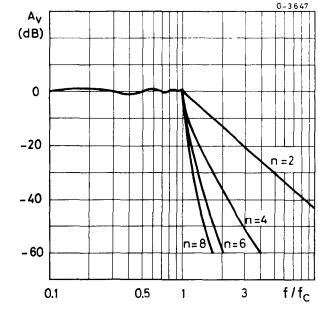


CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs.

Fig. 12 - Amplitude response (± 1 dB ripple)



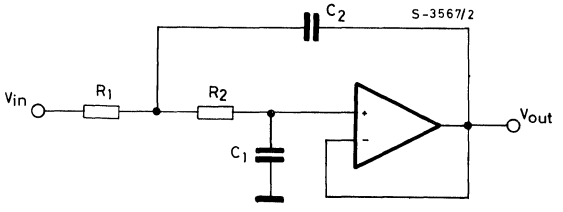
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filter to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

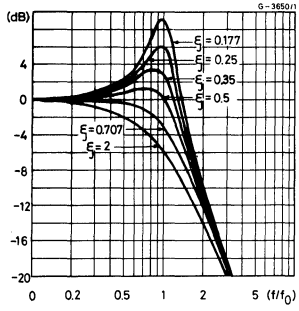
Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required. The choice of 'ξ' (or Q-factor) determines the filter response (see table).

TAB. 1

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v = -3 dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

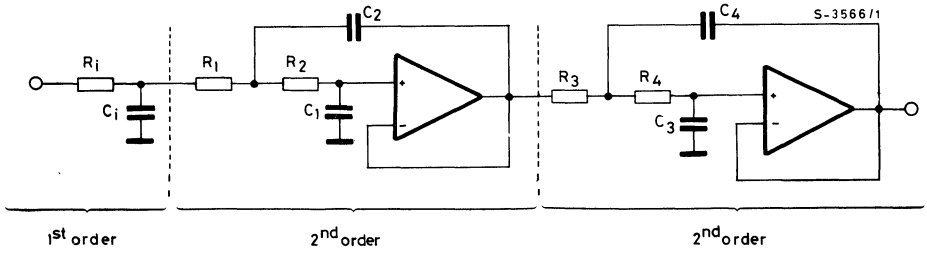
$$C_1 = \frac{1}{R} \frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R} \frac{1}{\xi \omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

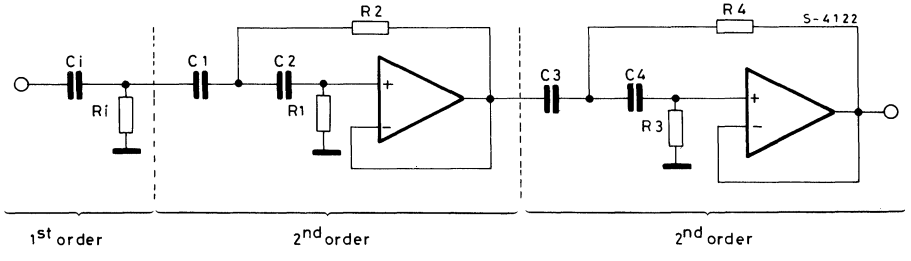
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

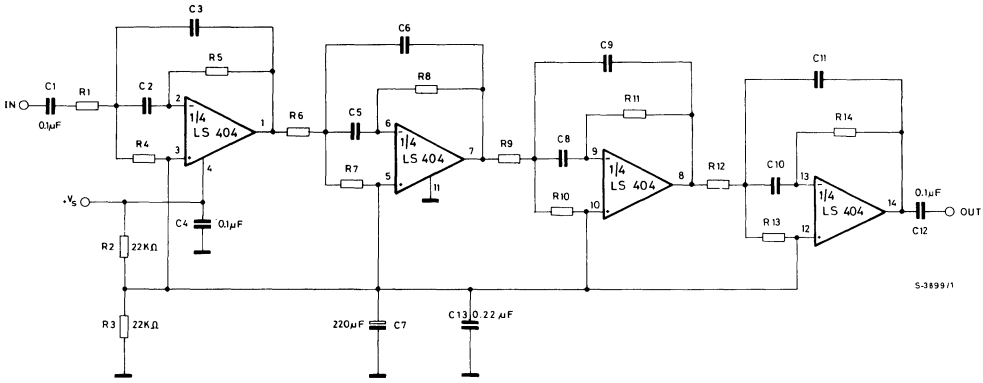
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

Fig. 17 - Multiple feedback 8-pole bandpass filter.



f_c = 1.180Hz; A = 1; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF;
$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ; $R_5 = R_8 = R_{11} = R_{14}$ = 330KΩ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3KΩ

Fig. 18 - Frequency response of band-pass filter

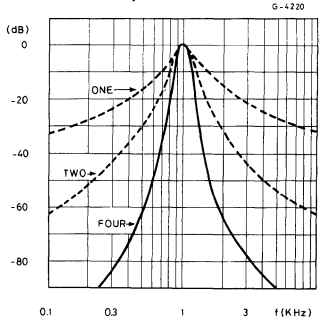
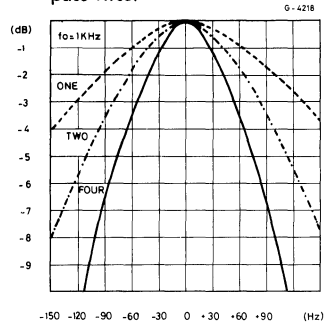
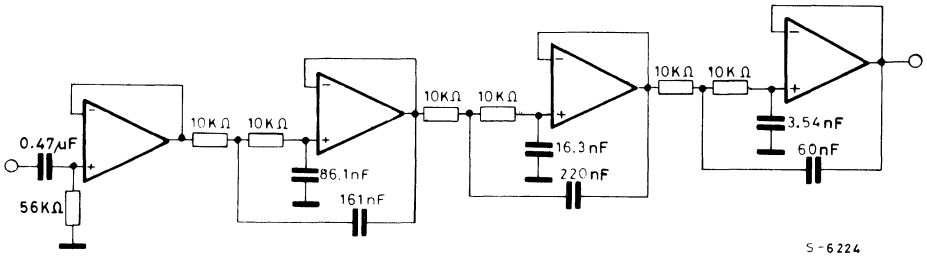


Fig. 19 - Bandwidth of band-pass filter



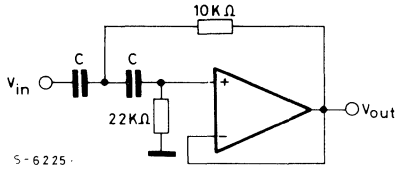
APPLICATION INFORMATION (continued)

Fig. 20 - Six-pole 355 Hz low-pass filter (Chebychev type)



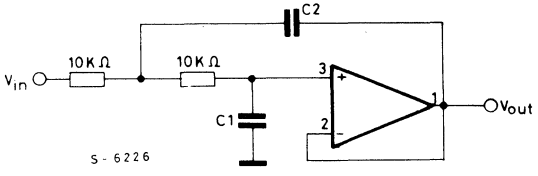
This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Fig. 21 - Subsonic filter (G_v = 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Fig. 22 - High cut filter (G_v = 0 dB)



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

LS496

QUAD RELAY DRIVER

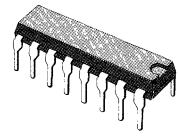
The LS496 is a monolithic integrated circuit for driving four mechanical bipolar relays. In addition to the four medium-power three state output stages, the LS496 contains also the necessary logic circuitry.

Each of the four channels has a data input, a disable input and the output. Furthermore a common disable input is provided. The outputs are in the high impedance state if the corresponding disable input or the common disable input gets the high (H) level. Otherwise, the logic level on the data input appears at the output. This logic behaviour is illustrated in the truth table next page.

The logic signals on the inputs are related to the signal ground (V_M) while the output level depends on the positive (V_{S1} = H) respectively the negative (V_{S2} = L) supply voltage. The output stage is protected via clamping diodes against voltage spikes generated by inductive loads.

The inputs can be supplied from logic signals with small power rating (e.g. C-MOS circuits). All inputs are protected against overvoltage and voltage smaller than the signal ground V_M.

In order to increase reliability, the LS496 contains a thermal shut-down circuit: for junction temperatures above 150°C, all outputs are switched in the high impedance state. With the built-in hysteresis the outputs become active again after a temperature decrease below 110°C. With the aid of current limiters the four output stages are short-circuit protected.



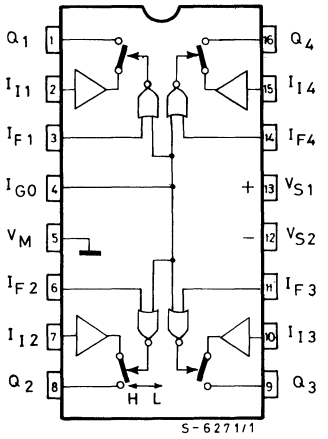
DIP-16 Plastic
(0.25)

ABSOLUTE MAXIMUM RATINGS

V_{S1}-V_{S2}	Supply voltage	-0.5 to 36	V
V_I-V_M	Input voltage	-0.5 to 20	V
	Voltage between two inputs	-0.5 to 20	V
I_O	Output current	± 100	mA
V_O	Maximum output voltage	V_{S2} to V_{S1}	V
T_{amb}	Ambient temperature	0 to 70	°C
T_j	Operating junction temperature	150	°C
P_{tot}	Total power dissipation	600	mW
T_{stg}	Storage temperature	-55 to +125	°C

LS496

CONNECTION AND LOGIC DIAGRAM
(top view)



Truth Table

I_{GO}	I_{Fi}	I_{Ii}	Q_i
L	L	L	L
L	L	H	H
H	X	X	S
X	H	X	S

L : Low Level
H : High Level
S : High Impedance Output (third state)
X : Don't care

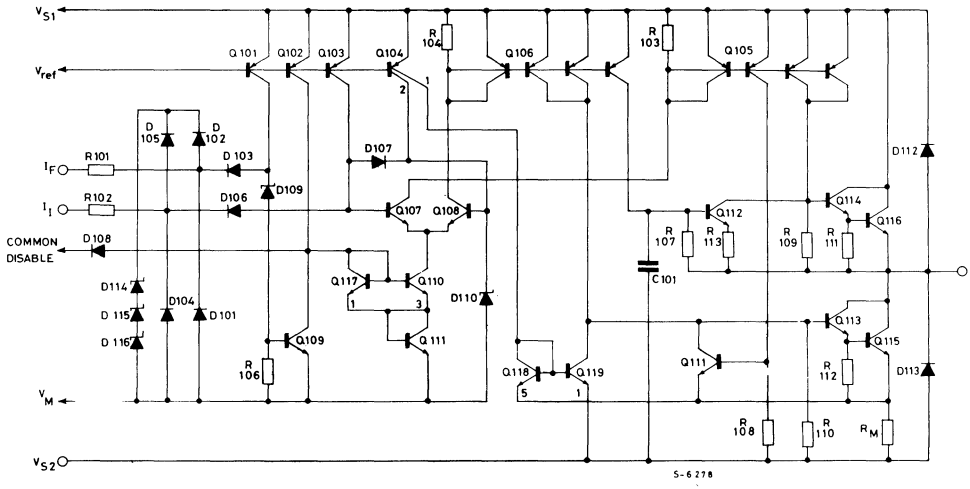
I_{GO} : Common Disable Input
I_{Fi} : Single Stage Disable Input
I_{Fi} : Data Input
Q_i : Output

THERMAL DATA

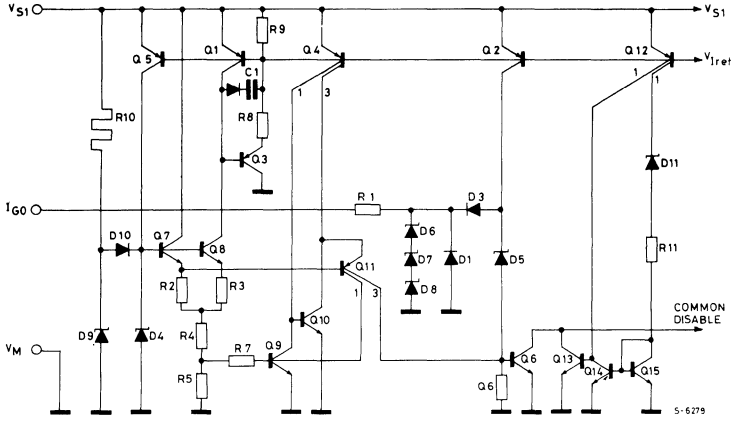
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

SCHEMATIC DIAGRAMS

Channel 1-4



Common part



DC ELECTRICAL CHARACTERISTICS (V_{S1}= +15V, V_{S2}= -15V, V_M = 0, T_{amb}= 45°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{S1}-V_M$ $V_{S2}-V_M$ $V_{S1}-V_{S2}$	Operating supply voltage	(the three conditions need to be fulfilled simultaneously, (see Fig. 1)	9 -27 9		36 0 36	V V V
I_{S1} I_{S2}	Quiescent supply current	I_{GO}= H-level (> 8V) (Q1, Q2, Q3, Q4: high impedance state)		2 -50	6 -200	mA μA
I_{S1} I_{S2}	Quiescent supply current	I_{GO}, I_{F1}-I_{F4}= L-level (< 5V) I_{I1}-I_{I4}: don't care No load on Q1-Q4		5 -3	16 -10	mA mA
I_{S1} I_{S2}	Quiescent supply current	I_{GO}, I_{F1}-I_{F4}= L-level (< 5V) I_{I1}-I_{I4} : don't care Load (> 150 Ω) on Q1-Q4		I_{QH}+5 I_{QL}-3	I_{QH}+16 I_{QL}-10	mA mA
$-V_{IL}$ V_{IL} V_{IH}	Input voltages I_{GO}, I_{F1}-I_{F4}, I_{I1}-I_{I4}	$-I_{IL}$= 1 mA range for low-level (L) range for high-level (H)	1 -0.5 8		2 5 V_{S1}	V V V
I_{IL} I_{IH}	Input currents	V_{IL}= V_M (L-level) V_{IH}= V_{S1} (H-level)		-100	-150 1	μA μA
V_{QL} V_{QH}	Output voltage	I_{QL}= -70 mA (I_{GO}= L, I_{Fi}= L, I_{Ii}= L) I_{QH}= 70 mA (I_{GO}= L, I_{Fi}= L, I_{Ii}= H)	V_{S2}+0.6 V_{S1}-2.3		V_{S2}+1.3 V_{S1}-1.5	V V
I_{QL} I_{QH}	Output currents	V_{QL} (I_{GO}= L, I_{Fi}= L, I_{Ii}= L) V_{QH} (I_{GO}= L, I_{Fi}= L, I_{Ii}= H)			-100 100	mA mA
I_{QS} I_{QS}	Output leakage current	V_Q= V_{S1} (I_{GO}= H or I_{Fi}= H) V_Q= V_{S2} (I_{GO}= H or I_{Fi}= H)		0.1 -0.1	1 -1	μA μA
V_{QVS1} V_{QVS2}	Output saturation voltage of clamping diodes	I_Q = -1 mA I_Q = 1 mA	V_{S1}+0.3 V_{S2}-0.9		V_{S1}+0.9 V_{S2}-0.3	V V
T_{sd}	Thermal shut-down:	all channels change to the high impedance slate reestablishing of the logic behav.		150 110		°C °C
I_{QL} I_{QH}	Short circuit protection:	V_{QL} (I_{GO}= L, I_{Fi}= L, I_{Ii}= L) V_{QH} (I_{GO}= L, I_{Fi}= L, I_{Ii}= H)	-150 no protection			mA

DYNAMIC ELECTRICAL CHARACTERISTICS

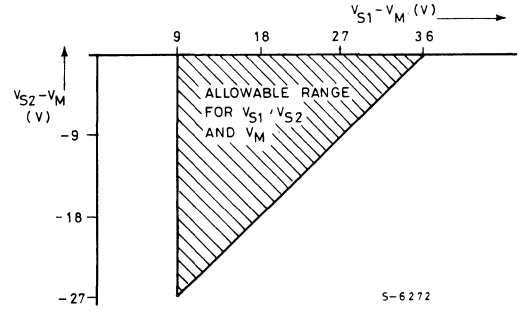
Test conditions : $V_{S1} = +12V$, $V_{S2} = -12V$, $V_M = 0V$, $R_{LOAD} = 180\ \Omega$
Clock : $f_c = 100$ kHz, duty cycle = 50% rise and fall time t_{THL}, $t_{TLH} = 50$ ns

Parameter		Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Propagation delay time (data, see Fig. 2c, 3a)		600 500		ns ns
t_{PSL} t_{PLS} t_{PSH} t_{PHS}	Propagation delay time (disable and common disable, see Fig. 2a, b, 3a)		300 400 500 700		ns ns ns ns
t_{TLH} t_{THL}	Transition time (data, see Fig. 2c, 3b)		250 350		ns ns
t_{TSH} t_{THS} t_{TSL} t_{TLS}	Transition time (disable and common disable, see Fig. 2a, b, 3b)		150 100 40 100		ns ns ns ns
f_c	Clock frequency			200	kHz

Use of L496 as relay driver

If the L496 is used as a relay driver the voltages $V_{S1} = 15V$, $V_{S2} = -15V$ and $V_M = 0V$ are provided Further combinations are possible, if the maximum ratings for the voltages V_{S1}, V_{S2} and V_M are not exceeded.
A graphic illustration of these conditions is seen in Fig. 1.

Fig. 1 - Allowed range of the voltage V_M, V_{S1} and V_{S2}



TEST CIRCUITS

Fig. 2a - Propagation delay time and transition time (disable input I_{F1}-I_{F4})

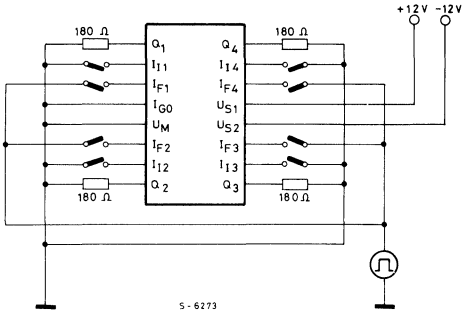


Fig. 2b - Propagation delay time and transition time (common disable input I_{GO})

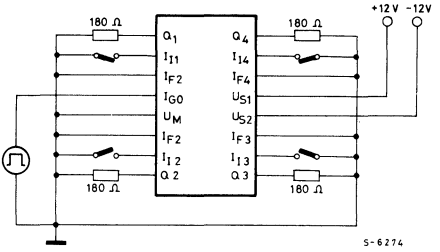


Fig. 2c - Propagation delay time and transition time (data input I_{I1}-I_{I4})

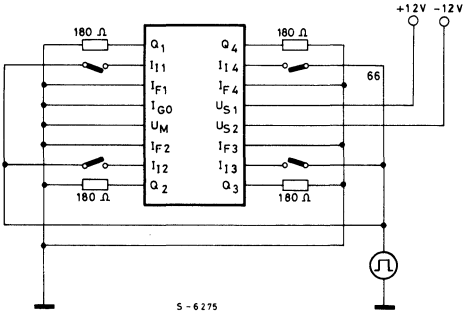


Fig. 3a - Propagation delay time

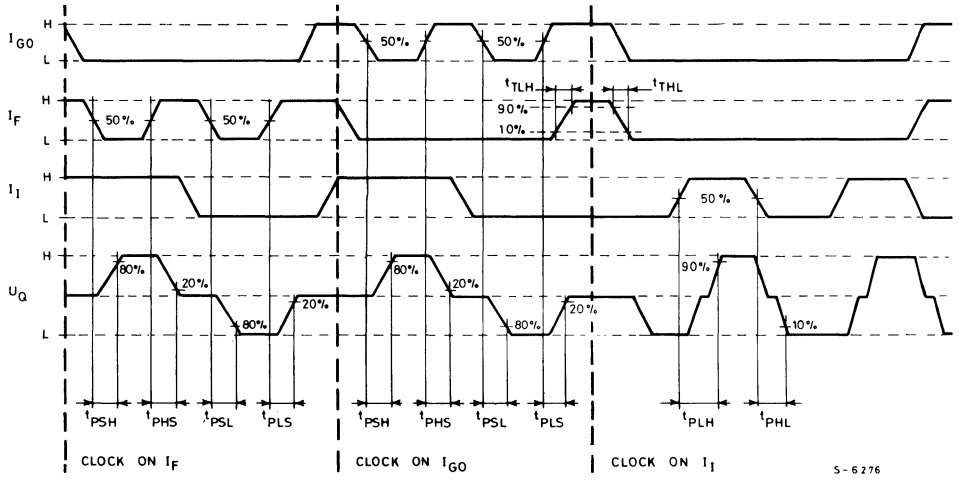
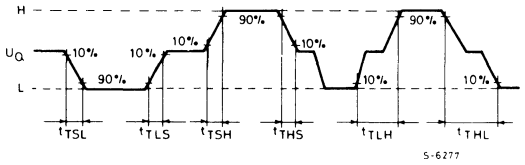


Fig. 3b - Transition time

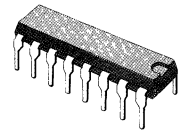


LS588

PRELIMINARY DATA

PROGRAMMABLE TELEPHONE SPEECH CIRCUIT

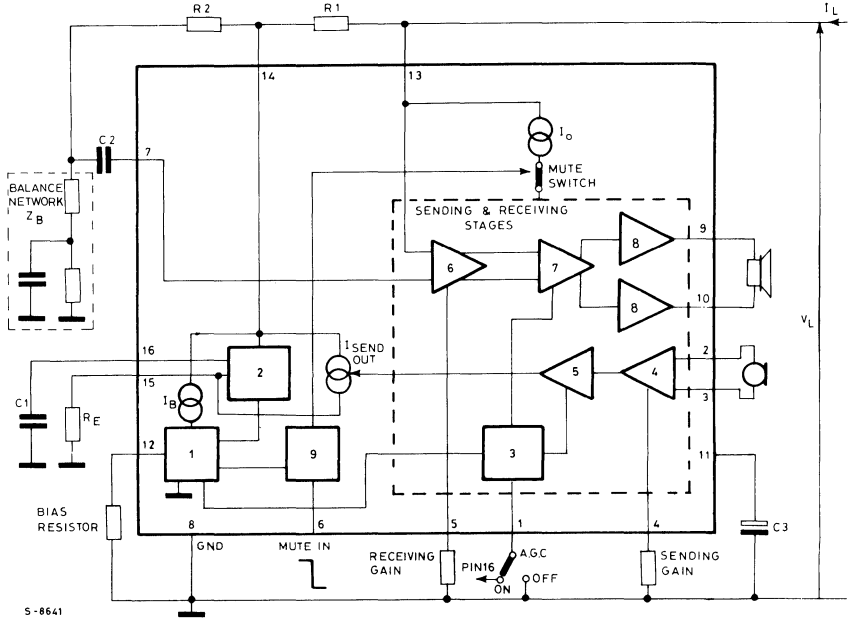
The LS588 is a monolithic integrated circuit in 16 lead dual in-line plastic package. Designed as a replacement for the hybrid circuit in telephone sets it performs all the functions previously carried out by this circuit.
With the LS588 it is possible to select the operating mode (fixed or variable gain). The device works with both piezoceramic and dynamic transducers and therefore its gain, both in sending and receiving paths, can be preset by means of two external resistors. This feature can also be obtained in AGC operating mode, when the device automatically adjusts the Rx/Tx gains to compensate for the line attenuation by sensing the line current.
The LS588 can supply the decoupling FET when working with an electret microphone. Output impedance can be matched to the line independently of transducer impedance.
In addition, the LS588 can be set in power down state, where the device displays a strow decrease of the current consumption (about 8 mA), still maintains DC and AC impedances to the line (for parallel operation with a DTMF generator).



DIP-16 Plastic
(0.4)

ORDERING NUMBER: LS588FB

BLOCK DIAGRAM

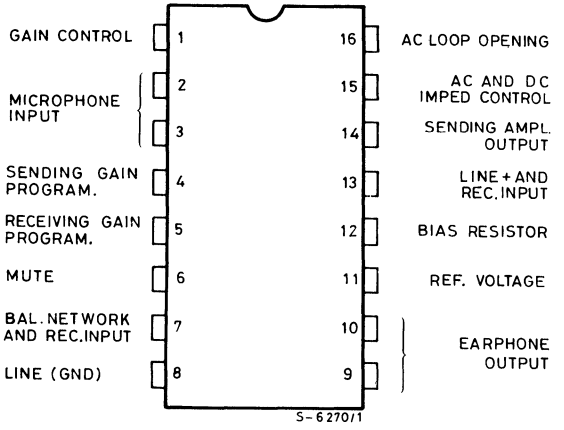


LS588

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

TEST CIRCUITS

Fig. 1

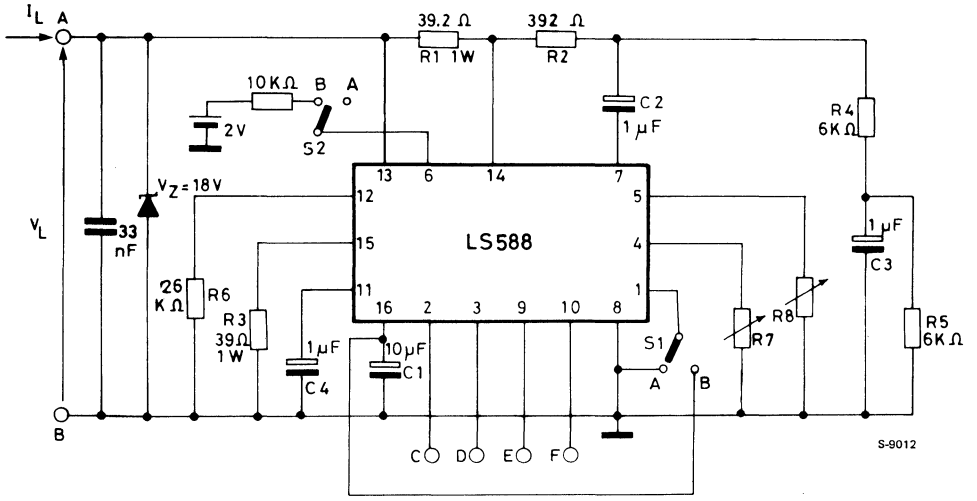


Fig. 2

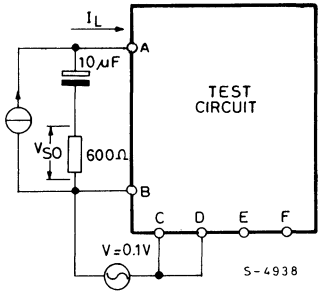


Fig. 3

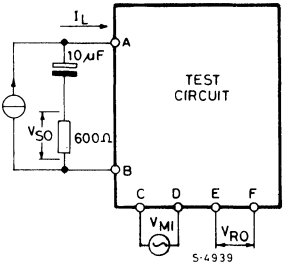
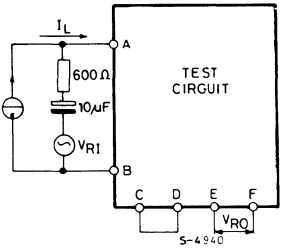


Fig. 4



LS588

ELECTRICAL CHARACTERISTICS (Refer to test circuits, T_{amb} = -25 to +50°C, f = 200 to 3400Hz, I_L = 15 to 100mA, R7 = R8 = 17.4KΩ, S1 in B S2 in A, unless otherwise specified)

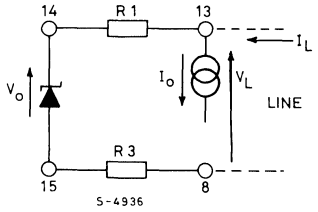
Parameter		Test Conditions		Min.	Typ.	Max.	Unit	Fig.
A.G.C. On								
V_L	Line voltage	I_L = 15mA I_L = 25mA I_L = 50mA I_L = 120mA	T_{amb} = 25°C	4.1	4.5 5.2 7	4.9 5.6 7.8 14	V	1
CMR	Common mode rejection	f = 1KHz		50			dB	2
G_s	Sending gain	I_L = 50mA f = 1KHz	T_{amb} = 25°C V_{MI} = 3mV	33.5		35.5	dB	3
ΔG_s	Sending gain variation vs. current	I_{ref} = 50mA T_{amb} = 25°C	I_L = 25mA	4.5		6	dB	3
			I_L = 100mA	-1.5		0	dB	
	vs. frequency	f_{ref} = 1KHz		-0.5		0.5	dB	3
	vs. R7	ΔR7 = -10KΩ			-9		dB	
THD_s	Sending distortion	I_L = 15 to 25mA V_{so} = 450mV	f = 1KHz			2	%	3
		I_L = 25 to 100mA V_{so} = 1.6V	f = 1KHz			5	%	
N_s	Sending noise	V_{MI} = 0mV			-70		dBm	3
Z_{MI}	Microphone impedance	V_{MI} = 3mV		11	15		KΩ	3
G_R	Receiving gain	I_L = 50mA f = 1KHz	T_{amb} = 25°C V_{RI} = 570mV	-3		-1	dB	4
ΔG_R	Receiving gain variation vs. current	I_{ref} = 50mA T_{amb} = 25°C	I_L = 25mA	4.5		6	dB	4
			I_L = 100mA	-1.5		0		
	vs. frequency	f_{ref} = 1KHz		-0.5		0.5		
	vs. R8	ΔR8 = -3KΩ			-3			
THD_R	Receiving distortion	V_{RI} = 570mV				2	%	4
		V_{RI} = 1.1V				5		
N_R	Receiving noise	V_{RI} = 0mV				250	μV	4
Z_{RO}	Receiving output impedance	V_{RO} = 50mV			50		Ω	4
	Sidetone	f = 1KHz			15		dB	3
Z_{ML}	Line matching impedance	V_{RI} = 0.3V	f = 1KHz	650		850	Ω	4
	Max receiving output (click suppression)	V_{RI} = 4V		3.9		4.7	V_{pp}	4
V_{SM}	Microphone supply	R_{load} = 2.2KΩ		1.9		2.1	V	1
MUTE OPERATION								
	Mute threshold voltage (pin 6)		Speech condition			0.8	V	–
			Mute condition	1.5			V	–
	Muting operation curr. (pin 6)	S2 in B)		50			μA	–
	Line dynamic in mute condition	S2 in B) THD = 2%	I_L = 3.5mA I_L = 4mA I_L = 5mA	600 850 1100			mV	–
	Line voltage in mute condition	S2 in B)	I_L = 3.5mA I_L = 4mA I_L = 5mA		3.6 4.2 4.6		V	–

CIRCUIT DESCRIPTION

1. DC Characteristic

In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristic V_L, I_L.
The DC characteristics of the LS588 is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3 (see the block diagram). The equivalent circuit is shown in fig. 5.

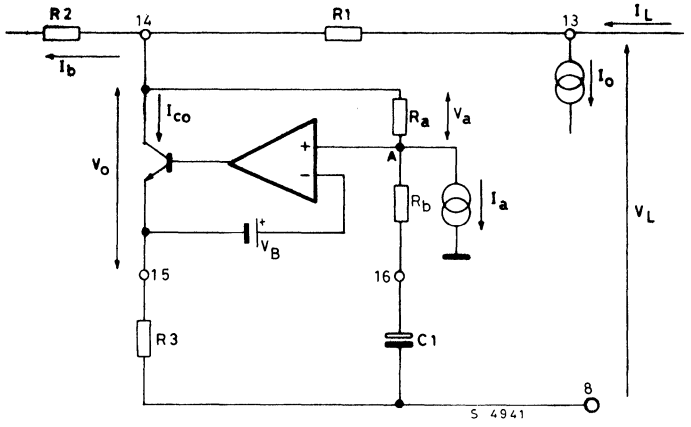
Fig. 5 - Equivalent DC load to the line



A fixed amount, I_o, of the total available current, I_L, is drained to allow the circuit to operate correctly. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 12.

The recommended minimum value of I_o is 7.5 mA with R pin 12 = 26KΩ.
The voltage $V_o \cong 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (block 2) is controlled by a temperature compensated voltage reference (block 1).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.
The difference I_L-I_o flows through the shunt regulator since I_b is negligible.
I_a is an internal constant current generator;hence $V_o = V_B + I_a \cdot R_a = 3.8V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series with a battery.
It is important to note that the DC voltage at pin 16 is proportional to the line current $V_{16} = V_{15} + V_B = (I_L - I_o)\, R_3 + V_B$.

Fig. 6 - Circuit configuration of the shunt regulator



CIRCUIT DESCRIPTION (continued)

2. Two to four wires conversion

The LS588 performs the two wire (line) to four wire (microphone, earphone) conversion by means of a Wheatstone bridge configuration thus obtaining the proper decoupling between sending and receiving signals (see fig. 7).

For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$.

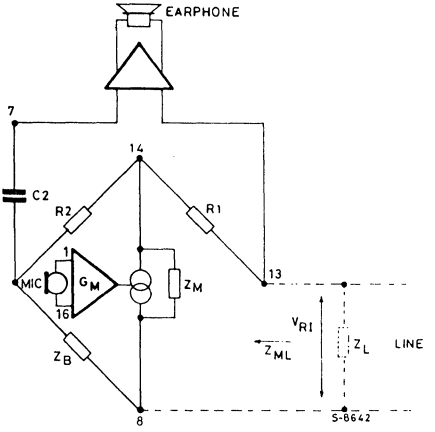
The AC signal from the microphone is sent to one diagonal of the bridge (pin 8 and 14). A small percentage of the signal power is lost on Z_B (since $Z_B \gg Z_L$); the main part is sent to the line via R_1.

In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 7 and 13). After amplification it is applied to the receiving capsule.

The impedance Z_M is simulated by the shunt regulator which also acts as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{(14-8)}}{\Delta I_{(14-8)}}$

Fig. 7 - Two to four wires conversion



From fig. 6, considering C_1 as a short circuit to the AC signal, any variation in ΔV_{14} generates a variation as follows:

$$\Delta V_{15} = \Delta V_A = \Delta V_{14} \frac{R_b}{R_a + R_b}$$

The corresponding current change is:

$$\Delta I = \frac{\Delta V_{15}}{R_3}$$

therefore

$$Z_M = \frac{\Delta V_{14}}{\Delta I} = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 13 and 8) is given by

$$Z_{ML} = R_1 + Z_M \,//\, (R_2 + Z_B)$$

By choosing $Z_M \gg R_1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The amplitude of the signal received across pins 13 and 7 can be changed using different values of R_1. (Of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must always be valid).

The received signal is related to the value of R_1 according to the approximated relationship:

$$V_R = V_{RI}\, 2 \frac{R_1}{R_1 + Z_M}$$

Note that if the value of R_1 is changed the transmission signal current is not changed, since the microphone amplifier is a transconductance amplifier.

CIRCUIT DESCRIPTION (continued)

3. Input and output amplifiers

The microphone amplifier (4) has a differential input stage with high impedance (min 11 KΩ) so allowing a good matching to the microphone by means of an external resistor without affecting the sending gain.
The receiving output stage (8) is intended to drive both piezoceramic and dynamic capsules. It has low output impedance, a maximum voltage swing greater than 2 V_p and a peak current of 2 mA.
With very low impedance transducers, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

4. Gain Control

It is possible to set the LS588 gain characteristics by means of one pin (pin 1).
When the pin 1 is grounded, the gains of the sending and receiving amplifiers do not depend on the line current (AGC off). When the pin 1 is connected to pin 15 the LS588 automatically changes the gain to compensate for line attenuation (AGC on).

4.1. AGC OFF

In this conditions, as already mentioned, both the sending and the receiving gain are fixed. Their values are determined, independently for the two paths, by the two external resistors R_7 (for T_x, between pin 4 and ground) and R_8 (for R_x, between pin 5 and ground), in a wide range (see fig. 8 and 9).

Fig. 8 - Sending gain vs. R_7 value (AGC OFF)

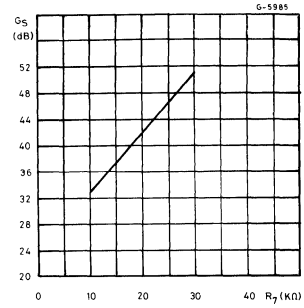
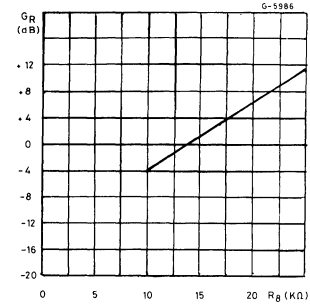


Fig. 9 - Receiving gain vs. R_8 value (AGC OFF)



4.2. AGC ON

Starting from any couple of gain values, fixed by the appropriate values of R_7 and R_8, the LS588 can automatically change the sending and receiving gains depending on the line current.
The line current is sensed across R_3 (see fig. 7) and transferred to pin 16 by the regulator.

$$V_{16} = V_B + V_{15} = V_B + (I_L - I_o) \cdot R_3$$

Following comparison with an internal reference (block 1) the voltage at pin 1 is used to modify (block 3) the gain of the amplifiers (5) and (7) on both the sending and receiving paths.
The starting point of the automatic level control is obtained at $I_L = 25$mA when the drain current $I_o = 7.5$ mA.
The external resistors R_7 and R_8 fix the maximum value for the gains.
Minimum gain is reached for a line current of about 100 mA when the same drain current I_o of 7.5 mA is used.

5. DC Shunt Regulator

The LS588 has built into the chip a DC shunt regulator intended to supply (pin 11) the coupling FET when an electret microphone is used. It delivers 1 mAp current with a voltage of 2 Volts (typ) regardless of the line current.

CIRCUIT DESCRIPTION (continued)

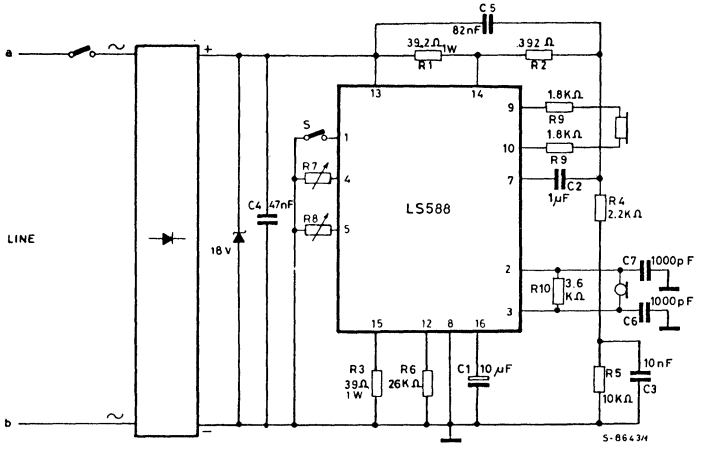
6. Mute condition and multifrequency interfacing

– A logical control (mute) at pin 6 allows operation in parallel with a proper DTMF generator connectable to the line (ex: PBD 3535).

– When pin 6 is set high (more than 1.8 Volt) the mute logic circuit (block 9) switches off both sending and receiving stages (mute switch) and reduces (1) the bias current, to save about 10 mA, available for the paralleled DTMF generator.
In this condition the LS588 still shows to the line the specified AC impedance (650 to 850 Ω) not provided by the DTMF generator which acts as a current generator.
Fig. 12 offers a complete application circuit for LS588 and PBD3535 where C_1 is reduced to 4.7 μF to optimize the DTMF start up without affecting the operation in speech condition.

The following table can be helpful to the designer when choosing different values for the external components, it refers to the typical application circuit of fig. 10.

Fig. 10 - Typical application circuit (piezoceramic transducers)



Component	Value	Function	Note
R_1	39.2 Ω	Bridge	R_1 controls the receiving gain. . The ratio R_2/R_1 fixes the amount of signal delivered to the line. R_1 helps in fixing the DC characteristic (see R_3 note)
R_2	392 Ω	Resistors	
R_3	39 Ω	Line current sensing Fixing DC characteristic	The relationships involving R_3 are: $-Z_{ML} = (21\ R_3 // Z_B) + R_1$ $-G_s = K \cdot \frac{Z_L // Z_{ML}}{R_3}$ $-V_L = (I_L - I_o)\ (R_3 + R_1) + V_o$ $[\ V_o = 3.8V\ ]$ Values of Z_{ML} ranging from 650 up to 850Ω are easily obtainable. .

CIRCUIT DESCRIPTION (continued)

Component	Value	Function	Note
R_4	2.2 KΩ	Balance Network	In order to optimize the sidetone it is possible to change R_4 and R_5 values; in any case the following relationship applies: $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ where $Z_B = R_4 + R_5 // X_{C3}$
R_5	10 KΩ		
R_6	26 KΩ	Bias Resistor	The suggested value assures the optimum operating current. It is possible to increase (decrease) the supply current by decreasing (Increasing) R_6 (they are inversely proportional), in order or achieve the shifting of the AGC starting point. This affects also the absolute gains, requiring different values for R_7 and R_8.
R_7	10 to 50 KΩ (Fig. 8)	Sending gain programming Resistor	
R_8	10 to 23 KΩ (Fig. 9)	Receiving gain programming Resistor	
R_9, R_9'	1.8 KΩ	Receiving impedance matching	R_9 and R_9' must be equal; the suggested value is good for matching to piezoceramic capsule; there is no problem in increasing and decreasing (down to 0Ω) this value, but when low resistance levels are used DC decoupling must be inserted to stop the current due to the receiver output offset voltage (max 400 mV).
R_{10}	3.6 KΩ	Microphone impedance matching	The suggested value is typical for a piezoceramic microphone, but it is possible to choose R_{10} from a wide range of values: $R_{Mike} = R_{10} // R_{pin\ 2\text{-}3}$.
C_1	10 μF	Regular AC bypass	A value greater than 10 μF gives a system start time too high for low line current. A value lower than 3.3 μF gives an alteration of the AC line impedance at low frequency.
C_2	1 μF	DC decoupling for receiving input	
C_3	10 nF	Balance network	See note for R_4 and R_5.
C_4	47 nF	Matching to a capacitive line	C_4 must be chosen according to the characteristics of the transmission line.
C_5	82 nF	Receiving gain flattness	C_5 depends on balancing and line impedance versus frequency.
C_6, C_7	1000 pF	RF bypass	

APPLICATION INFORMATION

Fig. 11 - Application circuit with electret microphone

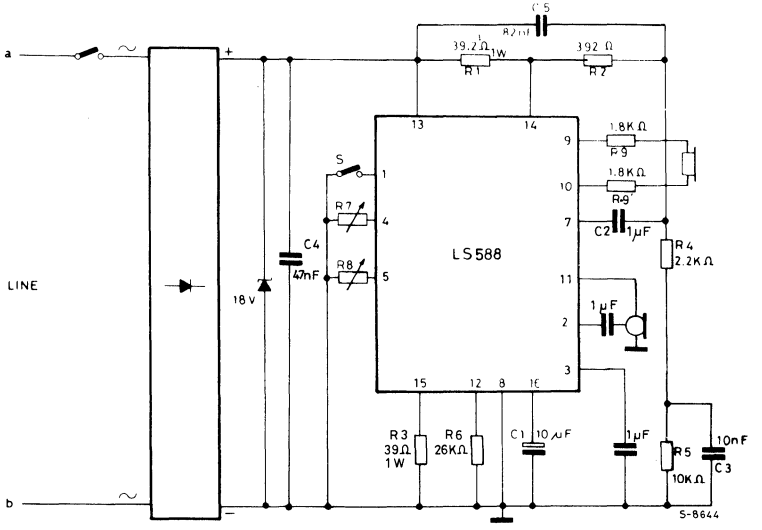
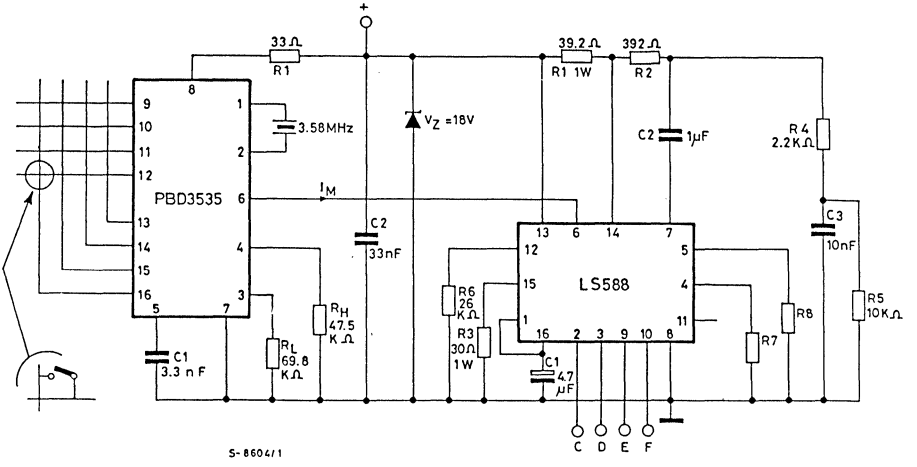


Fig. 12 - LS588 application with PBD3535

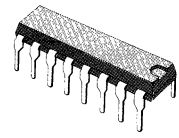


LS656

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

The LS656 is a monolithic integrated circuit in 16-lead plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically dynamic capsules). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS656 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer). The LS656 basic functions are the following:

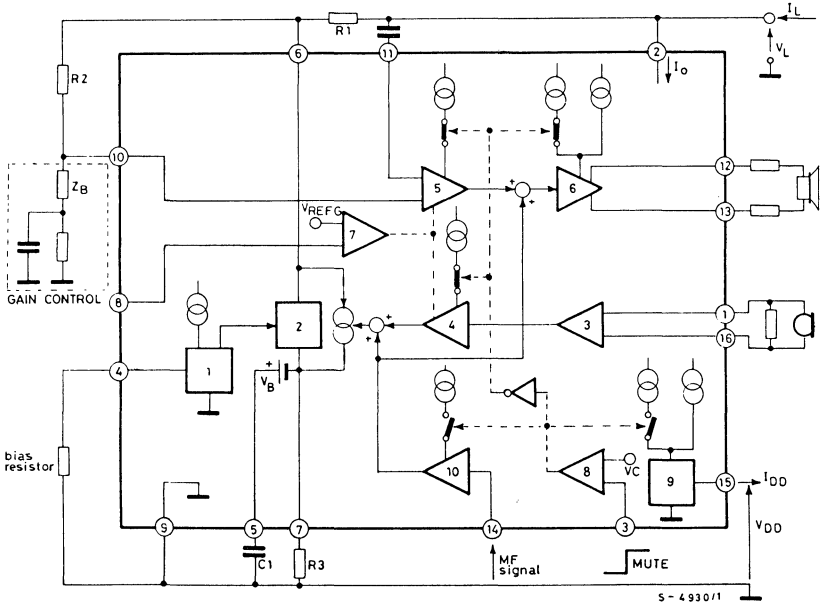
- It presents the proper DC path for the line current, **particular care being paid to have low voltage drop.**
- It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing either the line current or the line voltage. **In addition, the LS656 can also work in fixed gain mode.**
- It acts as linear interface for MF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated by the M761.



DIP-16 Plastic
(0.4)

ORDERING NUMBER: LS656B
LS656AB

BLOCK DIAGRAM

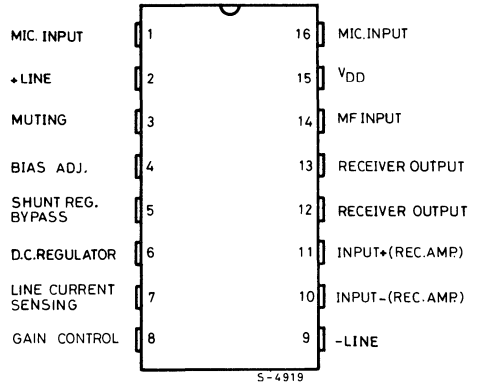


LS656

ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
i_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb}= 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM
(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max * 80	°C/W

TEST CIRCUITS

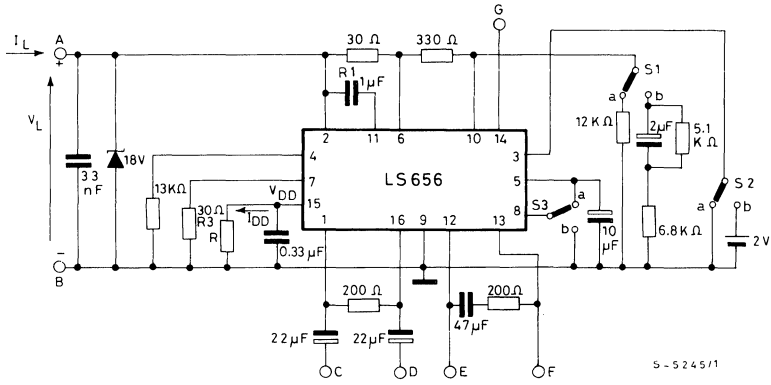
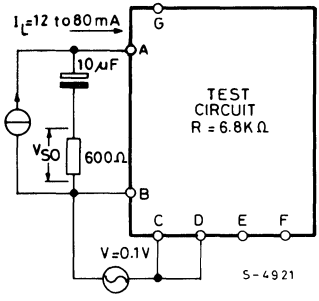
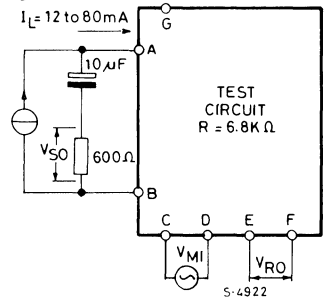


Fig. 1



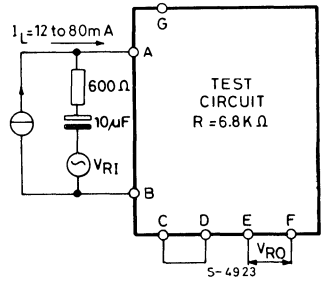
V = 0,1V CMR

Fig. 2



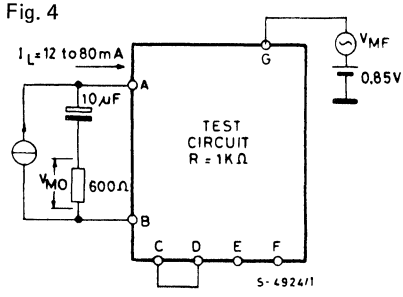
Side tone = $\frac{V_{RO}}{V_{MI}}$ Gs = $\frac{V_{SO}}{V_{MI}}$

Fig. 3



$G_R = \frac{V_{RO}}{V_{RI}}$

Fig. 4



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_G= 1 to 2V, I_L= 12 to 80 mA, S1, S2 and S3 in (a), T_{amb}= -25 to +50°C, f = 200 to 3400 Hz, unless otherwise specified).

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line voltage	T_{amb}= 25°C I_L= 12 mA I_L= 30 mA I_L= 60 mA	3.4		3.9 5.1 6.9	V	–
CMR	Common mode rejection	f = 1 KHz	50			dB	1
G_s	Sending gain for B type	T_{amb}= 25°C f = 1KHz I_L= 25 mA V_{MI}= 2mV I_L= 50 mA	48.5 44.5		50.5 46.5	dB	2
G_s	Sending gain for AB type	T_{amb}= 25°C f = 1 KHz I_L= 25 mA V_{MI}= 2 mV I_L= 50 mA	48 44		51 47	dB	2
	Sending gain flatness for B type (vs. freq.)	V_{MI}= 2 mV f_{ref}= 1 KHz			± 0.5	dB	2
	Sending gain flatness for AB type (vs. freq.)	V_{MI}= 2 mV f_{ref}= 1 KHz			± 1	dB	2
(*)	Sending gain flatness for B type (vs. current)	V_{MI}= 2 mV I_{ref}= 50 mA S3 in (b)			± 0.5	dB	2
	Sending gain flatness for AB type (vs. current)	V_{MI}= 2 mV I_{ref}= 50 mA S3 in (b)			± 1	dB	2
	Sending distortion for B type	f = 1 KHz V_{so}= 775 mV I_L= 16 mA V_{so}= 900 mV			2 10	% %	2
	Sending distortion for AB type	f = 1 KHz V_{so}= 775 mV I_L= 16 mA V_{so}= 900 mV			3 10	% %	2
	Sending noise for B type	V_{MI}= 0V; V_G= 1V		-71	-69	dBmp	2
	Sending noise for AB type	V_{MI}= 0V; V_G= 1V			-65	dBmp	2
	Microphone input impedance (pin-16)	V_{MI}= 2mV	40			KΩ	–
	Sending gain in MF operation	V_{MI}= 2mV S2 in (b)	-30			dB	2
G_R	Receiving gain for B type	V_{RI}= 0.3V I_L= 25 mA f = 1 KHz T_{amb}= 25°C I_L= 50 mA	-5.5 -10.5		-3.5 -8.5	dB	3
G_R	Receiving gain for AB type	V_{RI}= 0.3V I_L= 25 mA f = 1 KHz T_{amb}= 25°C I_L= 50 mA	-6 -11		-3 -8	dB	3
	Receiving gain flatness for B type (vs. freq.)	V_{RI}= 0.3V f_{ref}= 1 KHz			± 0.5	dB	3
	Receiving gain flatness for AB type (vs. freq.)	V_{RI}= 0.3V f_{ref}= 1 KHz			± 1	dB	3
	Receiving gain flatness for B type (vs. current)	V_{RI}= 0.3V I_{ref}= 50 mA S3 in (b)			± 0.5	dB	3
	Receiving gain flatness for AB type (vs. current)	V_{RI}= 0.3V I_{ref}= 50 mA S3 in (b)			± 1	dB	3
	Receiving distortion for B type	f = 1 KHz V_{RO}= 400 mV I_L= 15 mA V_{RO}= 450 mV			2 10	% %	3

* Fixed gain mode.

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
	Receiving distortion for AB type	f = 1 KHz V_{RO}= 400 mV I_L= 15 mA V_{RO}= 450 mV			3 10	% %	3
	Receiving noise for B type	V_{RI}= 0V; V_G= 1V		150	200	μV	3
	Receiving noise for AB type	V_{RI}= 0V; V_G= 1V			300	μV	3
	Receiving output impedance (pin 12-13)	V_{RO}= 50 mV		30		Ω	—
	Sidetone	f = 1 KHz T_{amb}= 25°C S1 in (b)			36	dB	2
Z_{ML}	Line matching impedance	V_{RI}= 0.3V f = 1 KHz	500	600	700	Ω	3
I_8	Input current for gain control (pin 8)				-10	μA	—

MULTIFREQUENCY SYNTHESIZER INTERFACE

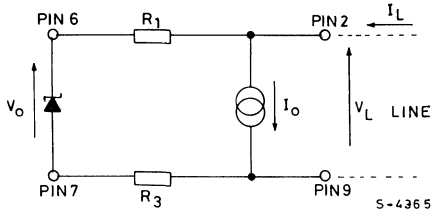
V_{DD}	MF supply voltage Stand by and Operation	S2 in (b)	2.4	2.5	2.7	V	—
I_{DD}	MF supply current Stand by Operation	S2 in (b)	 0.5 2			 mA mA	 — —
	MF amplifier gain	$f_{MF\ in}$= 1 KHz $V_{MF\ in}$= 80 mV	15		17	dB	4
V_I	DC input voltage level (pin 14)	$V_{MF\ in}$= 80 mV		V_{DD} 0.3		V	—
R_i	Input impedance (pin 14)	$V_{MF\ in}$= 80 mV	60			KΩ	—
d	Distortion for B type	$V_{MF\ in}$= 150 mVp I_L > 17 mA			2	%	4
d	Distortion for AB type	$V_{MF\ in}$= 150 mVp I_L > 17 mA			4	%	4
	Starting delay time				5	ms	—
	Muting threshold voltage (pin 3)	Speech operation			1	V	—
		MF operation	1.6			V	—
	Muting stand by current (pin 3)				-10	μA	—
	Muting operating current (pin 3)	S2 in (b)			+10	μA	—

CIRCUIT DESCRIPTION

1. DC characteristic

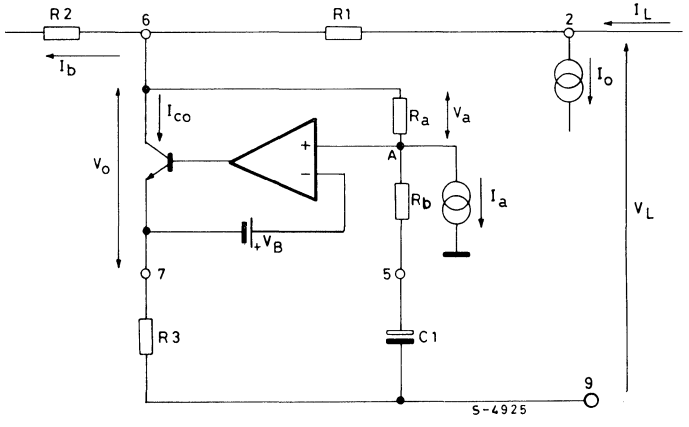
The fig. 5 shows the DC equivalent circuit of the LS656.

Fig. 5 - Equivalent DC load to the line



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).
The minimum value of I_o is 7.5 mA.
The voltage V_o= 37V of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

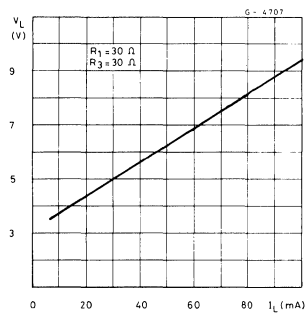
Fig. 6 - Circuit configuration of the shunt regulator



The difference I_L-I_o flows through the shunt regulator being I_b negligible. I_a is an internal constant current generator; hence $V_o = V_B + I_a \cdot R_a = 3.7V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.

It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).
The DC characteristic of the LS656 is shown in fig. 7.

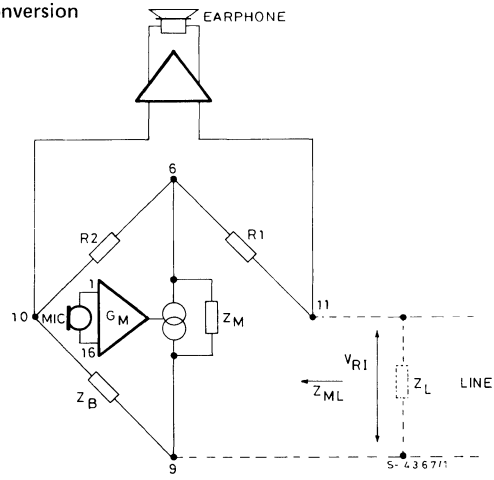
Fig. 7 - DC characteristic



2. Two to four wires conversion

The LS656 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 8).

Fig. 8 - Two to four wires conversion



For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R1}{R2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B \gg Z_L$); the main part is sent to the line via R1. In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

APPLICATION INFORMATION (continued)

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$.

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation:

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3\,(1 + \frac{R_a}{R_b})$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R1 + Z_M // (R2 + Z_B)$$

By choosing $Z_M \gg R1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R3\,(1 + \frac{R_a}{R_b})$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).
The received signal is related to R1 value according to the approximated relationship:

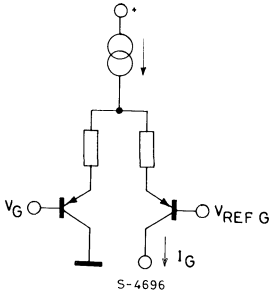
$$V_R = 2\,V_{RI}\,\frac{R1}{R1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. Automatic gain control

The LS656 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.
This function is performed by the circuit of fig. 9.

Fig. 9



The differential stage is progressively unbalanced by changing V_G in the range 1 to 2V (V_{REFG} is an internal reference voltage, temperature compensated).
It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken:

a) from the LS656 itself (both in variable and in fixed mode) and.

b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain characteristic depending on the current.
In fact (see fig. 6)

$$V_5 = V_B + V_7 \cong V_B + (I_L - I_o)\, R3$$

The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.
Minimum gain is reached for a line current of about 50 mA for the same drain current $I_o = 7.5$ mA.
When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.
It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too; for example using a division 1:1 (50K/50K) the AGC starting point shifts to about $I_L = 40$ mA, and the minimum gain is obtained at $I_L = 95$ mA.
In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain values (Rx, Tx) independently of the line conditions.
For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.
This type of operation meets the requirements of the French standard. (See the application circuit of fig. 13).

4. Transducer interfacing

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain.
The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance (100Ω max); high current capability 3 mAp).
When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).
Whit very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency interfacing

The LS656 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.
When no key of the keyboard is pressed the mute state is low and the LS656 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.

When one key is pressed, the M761 sends a "high state" mute condition to the LS656. A voltage comparator (8) of LS656 drives internal electronic switches; the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.
This extra current is diverted by the receiving and sending section of the LS656 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.
A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber; the MF amplifier (10) delivers the dial tones to the sending paths.
The mute function can be used also when a temporary inhibition of the output signal is requested.
The application circuit shown in fig. 10 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm) an external divider must be used (see fig. 11).

APPLICATION INFORMATION

Fig. 10 - Application circuit with multifrequency (EUROPE II STD)

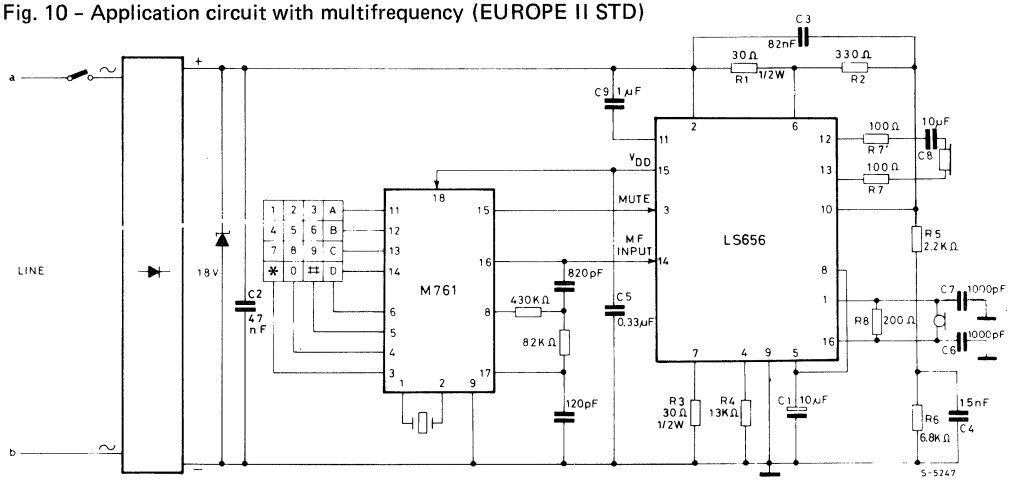
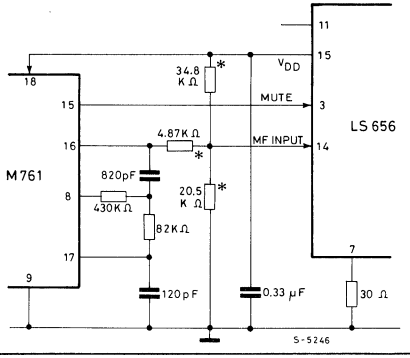


Fig. 11 - Application circuit with multifrequency (EUROPE I STD)



APPLICATION INFORMATION (continued)

Fig. 12 - Sending and receiving gain vs. line current (application circuit of fig.10)

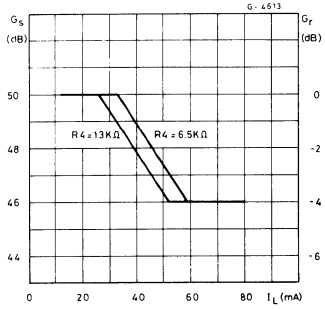


Fig. 13 - Application circuit without multifrequency

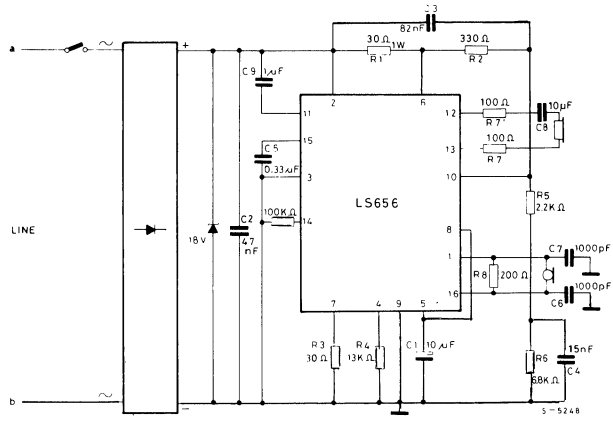
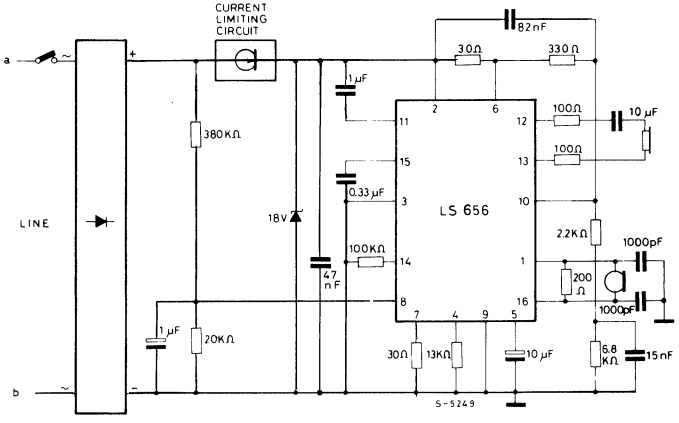
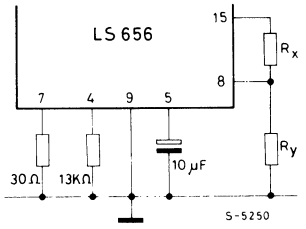


Fig. 14 - Application circuit with gain controlled by line voltage (French standard)



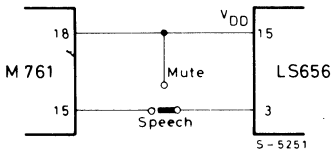
APPLICATION INFORMATION (continued)

Fig. 15 - Application circuit with fixed gain operation

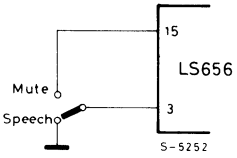


R_y= 0 Main gain condition
R_x= 0 Main gain condition

Fig. 16 - External mute function



a) with multifrequency



b) without multifrequency

In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.
The following table (refer to the application circuit of fig. 10) can help the designers.

Component	Value	Purpose	Note
R1	30 Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1W. The ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristics (see R3 note).
R2	330 Ω		
R3	30 Ω	Line current sensing. Fixing DC characteristic.	The relationships involving R3 are: – Z_{ML}= (20 R3//Z_B) + R1 – $G_s = K \cdot \frac{Z_L//Z_{ML}}{R3}$ – $V_L = (I_L - I_o)$ (R3 + R1) + V_o; V_o= 3.7V. Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900Ω. As far as the power dissipation is concerned, see R1 note.
R4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (See fig. 16). After R4 changement, some variations could be found also in other parameters, i.e. line voltage.

Component	Value	Purpose	Note
R5	2.2 KΩ	Balance Network	It's possible to change R5 and R6 values in order to improve the matching to different lines; in any case: $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ $Z_B = R5 + R6//X_{C4}$
R6	6.8 KΩ		
R7-R7'	100 Ω	Receiver impedance matching	R7 and R7', must be equal; the suggested value is good for matching to dynamic capsule; there is no problem in increasing and decreasing (down to 0Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop the current due to the receiver output offset voltage (max 200 mV).
R8	200 Ω	Microphone impedance matching	The suggested value is typical for a dynamic microphone, but it is possible to choose R8 in a wide range.
C1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47 nF	Matching to a capacitive line	C2 changes with the characteristics of the transmission line.
C3	82 nF	Receiving gain flatness	C3 depends on balancing and line impedance versus frequency.
C4	15 nF	Balance network	See note for R5, R6.
C5	0.33 μF	DC filtering	The C5 range is from 0.1 μF to 0.47 μF. The lowest value is ripple limited, the higher value is starting up time limited.
C6-C7	1000 pF	RF bypass	
C8	100 μF	Receiving output DC decoupling	See note for R7, R7.
C9	1 μF	Receiving input DC decoupling	

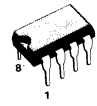
LS1014

PRELIMINARY DATA

AN AT&T PRODUCT

60-VOLT DUAL RELAY DRIVER

- TTL COMPATIBLE INPUT
- EACH OUTPUT CAN HANDLE ANY LOAD FROM 2 TO 30mA.
- DESIGNED TO OPERATE FROM 5V (V+) AND −48V (V−).
- TESTED FOR 60V OPERATION.
- PROTECTION DIODE AT EACH OUTPUT FOR OPTIONAL CONNECTION



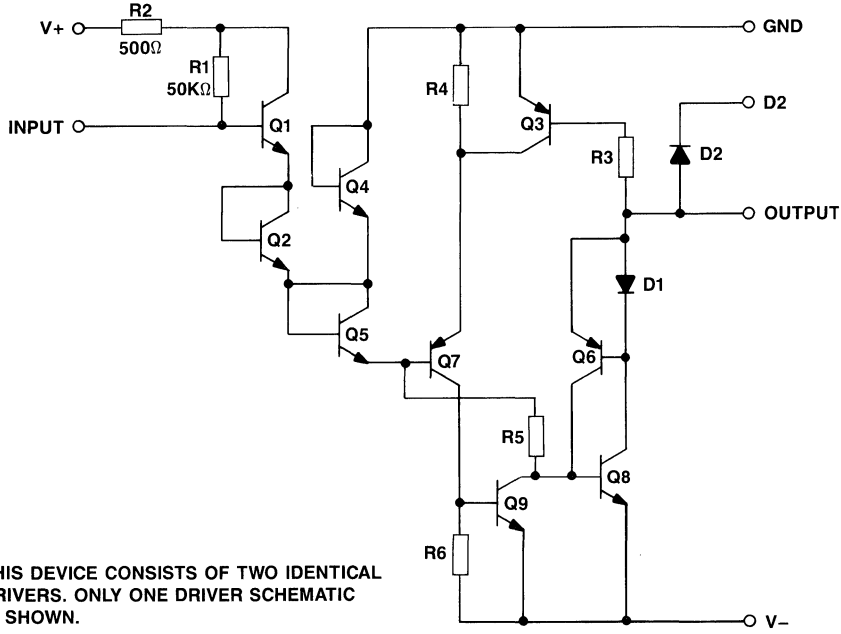
Minidip A Plastic

ORDERING NUMBER: LS1014AB

The LS1014 integrated curcuit consists of two independent relay drivers and is intended for use in high voltage relay applications.

Each driver is controlled by TTL Logic. A logical "1" on the input activates a relay.

Fig. 1 - Basic Schematic Diagram



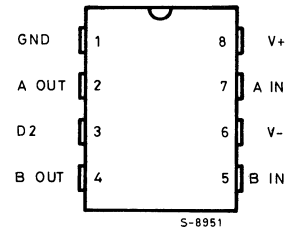
THIS DEVICE CONSISTS OF TWO IDENTICAL DRIVERS. ONLY ONE DRIVER SCHEMATIC IS SHOWN.

LS1014

PIN DESCRIPTION

PIN NUMBER	CONNECTION
1	Ground
2	Output Driver A
3	Diode D2
4	Output Driver B
5	Input Driver B
6	V−
7	Input. Driver A
8	V+

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Voltage (V+ to V−)	70	V
Voltage (V− to GND)	6.25	V
Current (Each Driver Output)	−30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_{PS}	Power Supply Current	$R_L = 1.5k\Omega$	ON	0.1	—	2.4	mA
			OFF	0.1	—	1.6	
I_L	Output Leakage Current			—	—	1.0	μA
I_{PSL}	Logic Supply Current	$R_L = 4.7k\Omega$	ON	100	—	1000	
			OFF	10	—	500	
I_{IH}	Logic Input Current		ON	−4.0	—	−75	
I_{IL}			OFF	−5.0	—	−250	
V_{IH}	Input Switching Voltage		ON	1.8	—	—	V
V_{IL}			OFF	—	—	0.8	
V_{OH}	Output Voltage	$R_L = 820\Omega$	ON	0.6	—	1.6	
V_{OL}			OFF	—	—	10	mV

Fig. 2 - Output Voltage vs Temperature

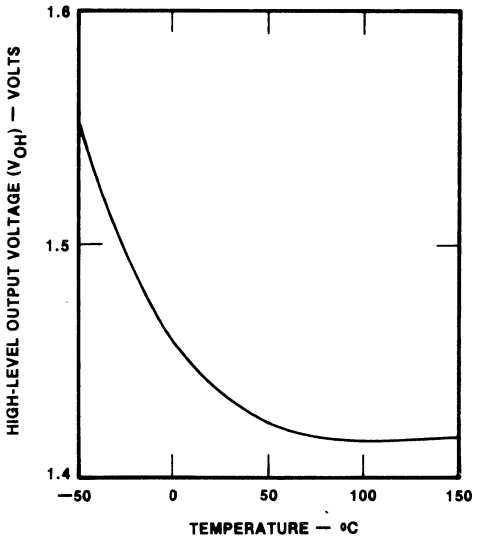


Fig. 3 - Output Leakage Current vs Temperature

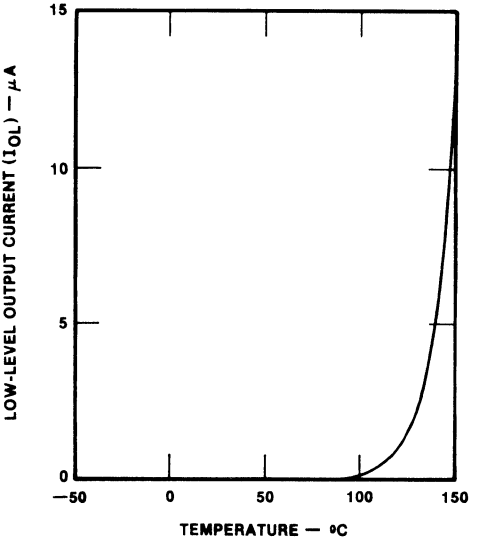


Fig. 4 - Supply Current vs Temperature

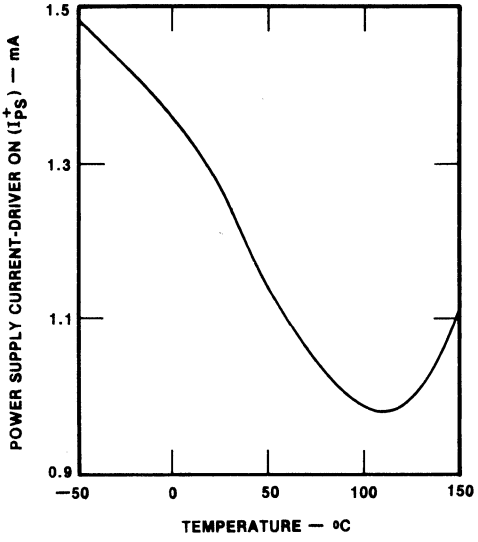
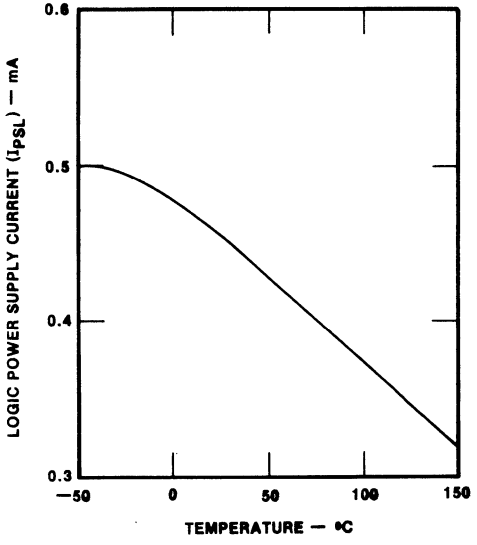


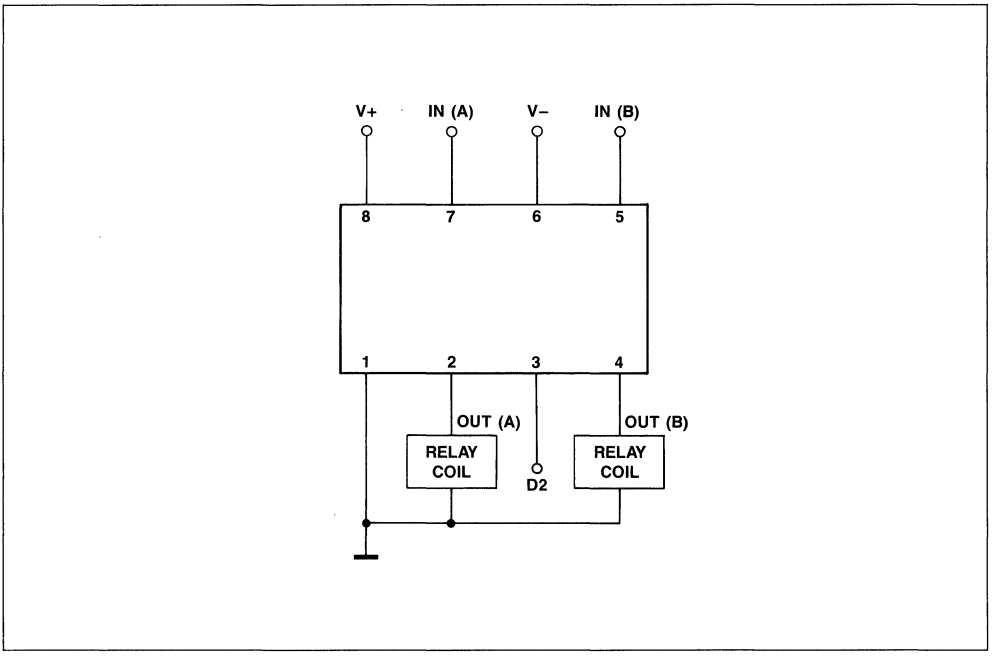
Fig. 5 - Logic Supply Current vs Temperature



APPLICATION

Figure 6 illustrates the relay-to-ground method of driving a relay using the LS1014 device. A surge protection diode can be placed across the relay coils by connecting pin 3 to ground (see Figure 1 for the internal surge protection diode connections).

Fig. 6 - Relay-to-Ground Applications Diagram



LS1240
LS1240A

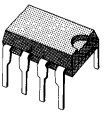
PRELIMINARY DATA

ELECTRONIC TWO – TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS

LS1240 and LS1240A are monolithic integrated circuits designed to replace the mechanical bell in telephone sets in connection with an electro-acoustical converter. Both devices can drive directly a piezoceramic converter (buzzer).
The output current capability of LS1240A is higher than LS1240. For driving a dynamic loudspeaker LS1240 needs a transformer, while LS1240A, needs a decoupling capacitor.
No current limitation is provided on the output stage of LS1240A, so a minimum load DC of 50Ω is adviced.

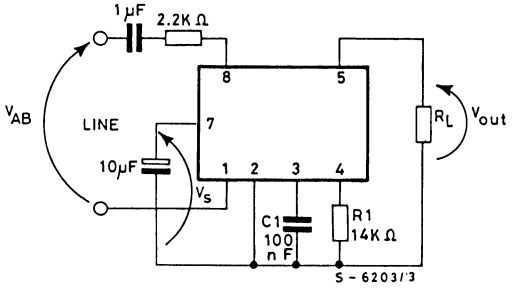
The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker, both tone frequencies and the switching frequency can be externally adjusted. The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect correct operation of the device.



Minidip Plastic

ORDERING NUMBERS: LS1240
LS1240A

Fig. 1 - Test circuit



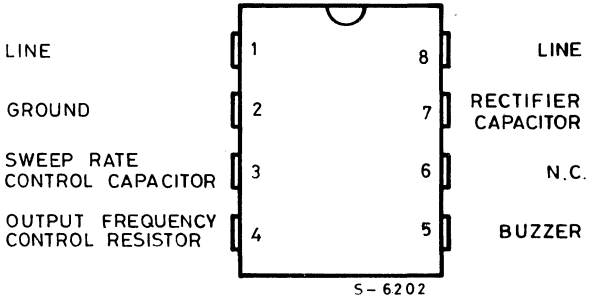
$$f_1 = \frac{2.72 \cdot 10^4}{R\ (K\Omega)} \qquad f_2 = 0.725\ f_1 \qquad f_{SWEEP} = \frac{750}{C_1\ (nF)}$$

LS1240
LS1240A

ABSOLUTE MAXIMUM RATINGS

V_{AB}	Calling voltage (f = 50Hz) continuous	120	V_{rms}
V_{AB}	Calling voltage (f = 50Hz) 5s ON/10s OFF	200	V_{rms}
DC	Supply current	30	mA
T_{op}	Operating temperature	-20 to +70	°C
T_{stg}	Storage and junction temperature	-65 to +150	°C

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_S	Supply voltage				26	V
I_B	Current consumption without load	V_S = 9.3 to 25V		1.5	1.8	mA
V_{ON}	Activation voltage LS1240 LS1240A		12.2 12		13.2 13.5	V V
V_{OFF}	Sustaining voltage LS1240 LS1240A		8 7.8		9 9.3	V V
R_D	Differential resistance in OFF condition		6.4			KΩ
V_{OUT}	Output voltage swing			V_S -5		V
I_{OUT}	Short circuit current LS1240 LS1240A	V_S = 20V R_L = 0Ω R_L = 250Ω		35 70		mA mA

AC OPERATION

	Output frequencies fout 1 fout 2 LS1240	V_S = 26V R_1 = 14KΩ V_3 = 0V V_3 = 6V	1.65 1.15		2.53 1.9	KHz
	fout 1 fout 2 LS1240A	V_3 = 0V V_3 = 6V	1.55 1.08		2.53 1.9	KHz
	$\frac{\text{fout 1}}{\text{fout 2}}$		1.33		1.43	Hz
	Programming resistor range		8		5.6	KΩ
	Sweep frequency	R_1 = 14KΩ C_1 = 100nF	5.25	7.5	9.75	Hz

Fig. 2 - Typical Application for LS1240

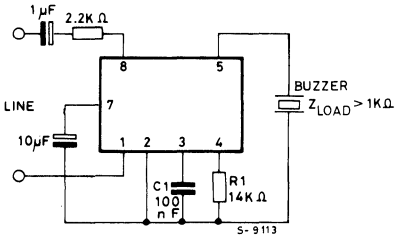
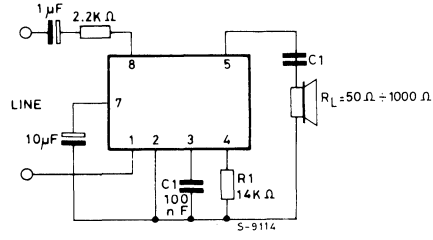


Fig. 3 - Typical Application for LS1240A



C_1 such that $|Z_{LOAD}| > 1K\Omega$

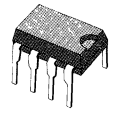
LS1241

PRELIMINARY DATA

ELECTRONIC TWO – TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF A DEVICE
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVER VOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS

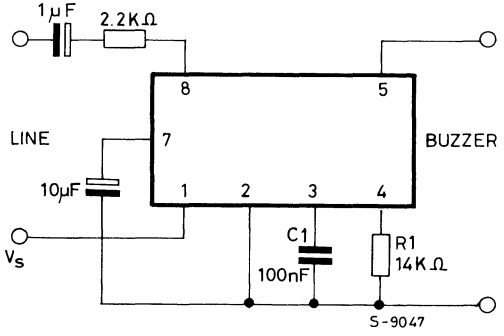
LS1241 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a transformer is needed. The two tone frequencies generated are switched by an output amplifier in the loudspeaker; both tone frequencies and the switching frequency can be externally adjusted.
The supply voltage is obtained from the AC ring signal and the circuit is designed to that noise on the line or variations of the ringing signal cannot affect correct operation of the device.



Minidip Plastic

ORDERING NUMBER: LS1241

Fig. 1 - Test and Application Circuit



$$f_1 = \frac{1.93 \cdot 10^4}{R_1\ (K\Omega)} \qquad f_2 = \frac{4}{5} f_1 \pm 4\% \qquad f_{sweep} = \frac{750}{C_1\ (nF)}$$

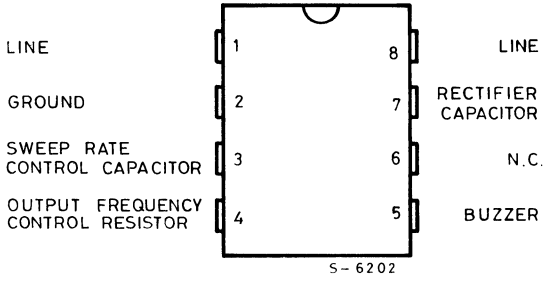
LS1241

ABSOLUTE MAXIMUM RATINGS

V_{AB} *	Calling voltage (f = 50Hz) continuous	90	V_{rms}
V_{AB} *	Calling voltage (f = 50Hz) 1.8s ON/3.6s OFF	130	V_{rms}
DC	Supply current	30	mA
T_{op}	Operating temperature	-20 to +70	°C
T_{stg}	Storage and junction temperature	-65 to +150	°C

* See test circuit of fig. 1

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = applied between pins 7-2 unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage				26	V
I_B	Current consumption without load	V_s = 9 to 25V		1.5	1.8	mA
V_{on}	Activation voltage		12.2		13.2	V
V_{off}	Sustaining voltage		8		9	V
R_D	Differential resistance in OFF condition (pins 8-1)		6.4			KΩ
V_{OUT}	Output voltage swing			V_s-5		V
I_{out}	Short circuit current (pins 5-2)	V_s = 26V		35		mA

AC OPERATION

	Output frequencies $f_{out\ 1}$ $f_{out\ 2}$	V_s = 26V R_1 = 14KΩ V_3 = 0V V_3 = 6V	1.23 0.94		1.8 1.5	KHz
	$\frac{fout\ 1}{fout\ 2}$		1.2		1.3	Hz
	Programming resistor range		12		50	KΩ
	Sweep frequency	R_1 = 14KΩ C_1 = 100nF	5.25	7.5	9.75	Hz

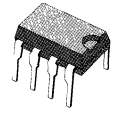
LS5018
LS5060
LS5120

TRANSIENT VOLTAGE SUPPRESSION

- BREAKOVER VOLTAGE INDEPENDENT OF TRANSIENT RISE TIME
- HIGH CURRENT CAPABILITY
- VERY HIGH OFF STATE RESISTANCE
- VERY HIGH ON STATE CONDUCTANCE
- AUTOMATIC RECOVERY
- CHARACTERISTICS LARGELY INDEPENDENT OF AGEING
- FAILSAFE OPERATION
- CAN BE USED ON REMOTE-SUPPLY LINES

The LS5018, LS5060 and LS5120 are bidirectional transient overvoltage suppressors designed to protect sensitive components in electronic telephones and telecommunications equipment against transients caused by lightning, induction from power lines etc.

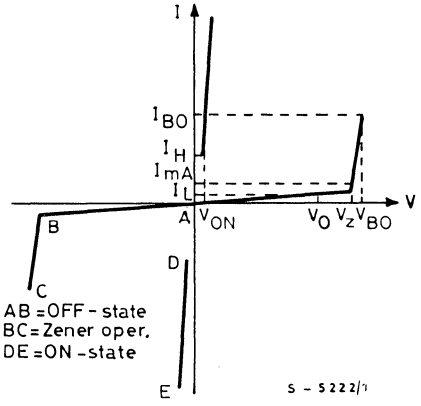
An ideal replacement for gas discharge tubes, these suppressors feature stable characteristics, better reliability, lower overall protection cost and failsafe operation — if destroyed, they become permanent short circuits. Moreover, since these devices recover automatically when the ON state current falls below a 250mA holding current, they may be used on remotely supplied lines.



Minidip Plastic

ORDERING NUMBERS: LS5018
LS5060
LS5120

Fig. 1 - Voltage-current characteristics



LS5018
LS5060
LS5120

ABSOLUTE MAXIMUM RATINGS

I_{TS}	Transient current (t_1/t_2 = 1/50 μs pulse see fig. 2a)	500	Ap
	(t_1/t_2 = 1/1000 μs pulse see fig. 2a)	150	Ap
I_p	Non repetitive peak current (one sine wave 50 Hz, 30 sec interval - see fig. 2b)	50	A
I_p	Repetitive peak current (50 Hz, 1 sec - see fig. 2c)	20	A
P_{tot}	Total power dissipation at T_{amb} = 50°C (steady state)	1.2	W
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(top view)

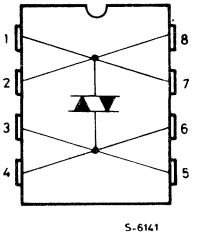
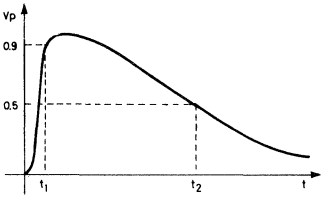
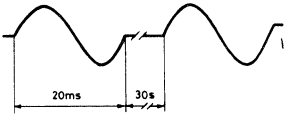


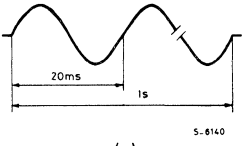
Fig. 2 - Waveforms



(a)



(b)



(c)

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ – see voltage-current characteristics)

Parameter		Test conditions	LS 5018			LS 5060			LS 5120			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Leakage current	V_o = 16V			5							μA
		V_o = 50V						10				
		V_o = 100V									20	
V_Z	Zener voltage	I_L = 1 mA	17			60			120		150	V
I_Z(*)	Maximum OFF state current (BC range)			500			500		500			mA
I_{BO}	Minimum firing current			1300			1000				1250	mA
V_{BO}(**)	Breakover voltage	Max $\Delta V/\Delta t$= 10 KV/μsec			22			85			180	V
V_{ON}	ON state voltage	I = 1A		2			2			2		V
I_H	Holding current			200			200		250			mA
R_{ON}	ON state resistance	$t_{ON} < 100\ \mu s$			0.4			0.4			0.4	Ω
		$t_{ON} > 100\ \mu s$			0.25			0.25			0.25	
C_{OFF}	OFF state capacitance	V = 0		150			150			150		pF

(*) These devices are not designed to function as zeners; consequently continuous operation in the BC range of the characteristic will damage them.

(**) Since the firing current, I_{BO}, is inversely proportional to the temperature, while the Zener voltage V_Z is directly proportional, the breakover voltage V_{BO} is rather independent of temperature.

Fig. 3 - Normalized leakage current vs. temperature

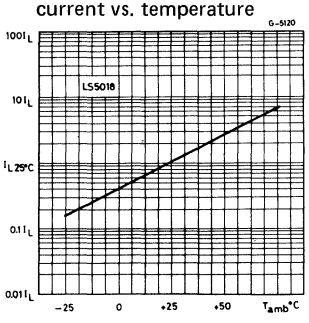


Fig. 4 - Normalized leakage current vs. temperature

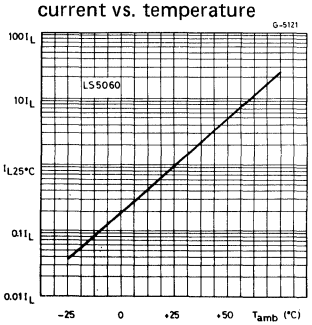


Fig. 5 - Normalized leakage current vs. temperature

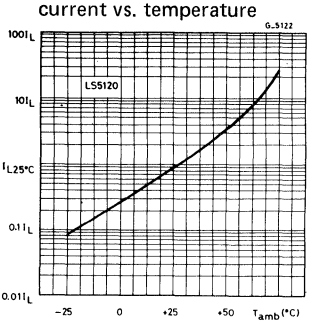


Fig. 6 - ΔI_H vs. temperature

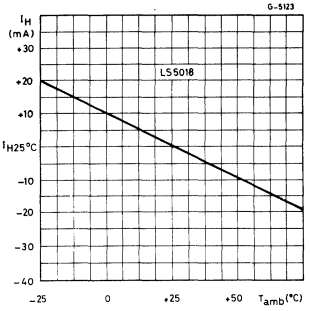


Fig. 7 - ΔI_H vs. temperature

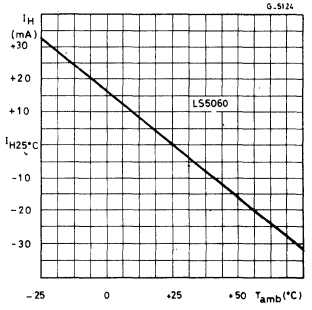


Fig. 8 - ΔI_H vs. temperature

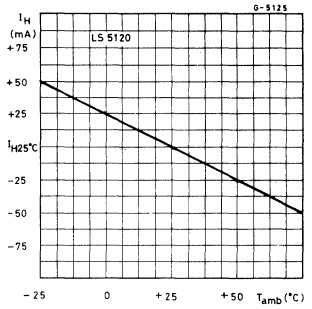


Fig. 9 - ΔV_z vs. temperature

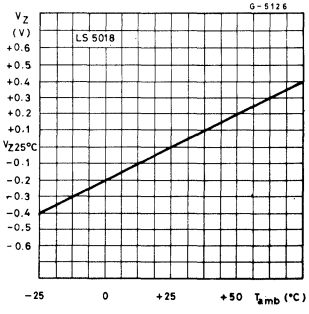


Fig. 10 - ΔV_z vs. temperature

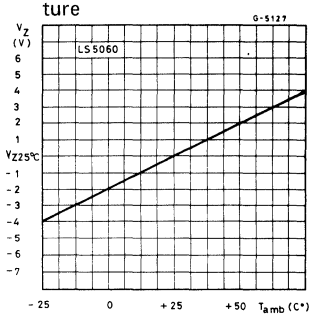
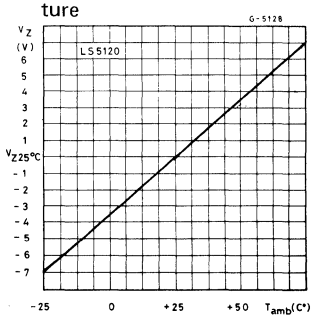


Fig. 11 - ΔV_z vs. temperature



DC TEST CIRCUITS

Fig. 12 - Leakage current

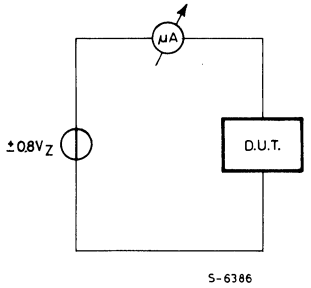


Fig. 13 - Zener voltage

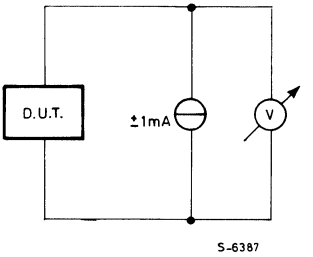


Fig. 14 - Breakover voltage

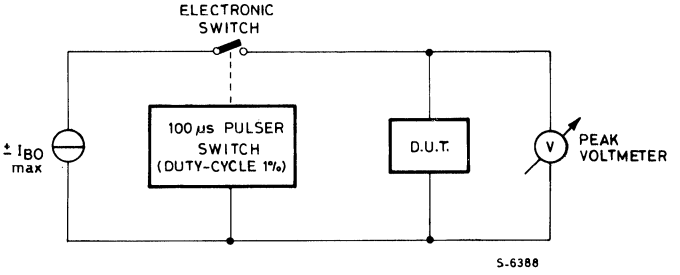
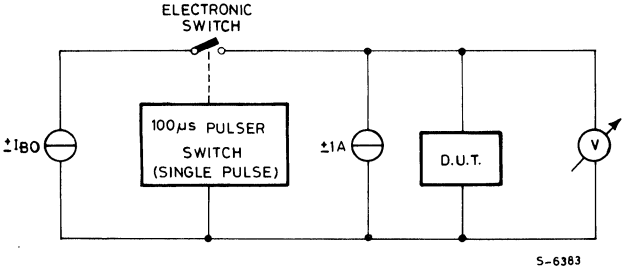
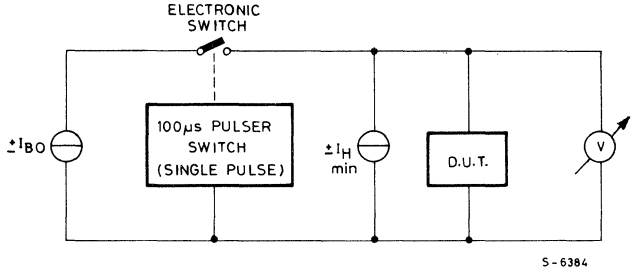


Fig. 15 - V_{on} voltage at 1A



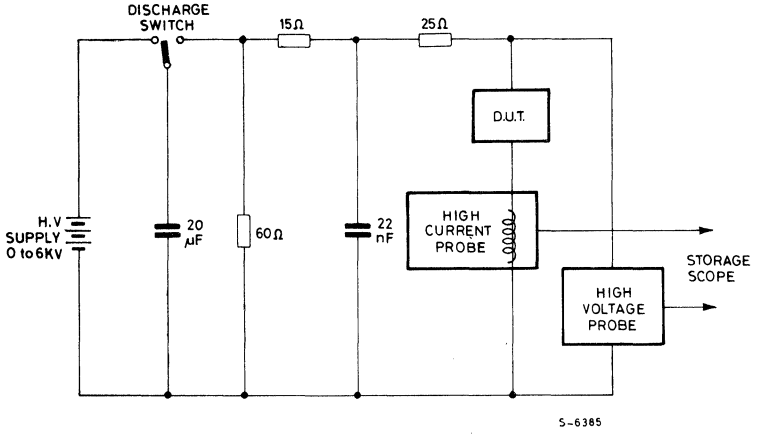
DC TEST CIRCUITS (continued)

Fig. 16 - Holding current



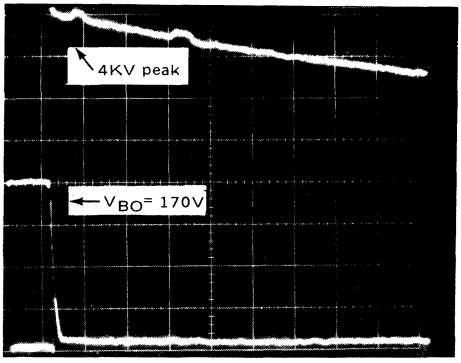
DYNAMIC TEST CIRCUITS

Fig. 17 - High voltage pulse test (according to CCITT vol. IX – Rec. K17)



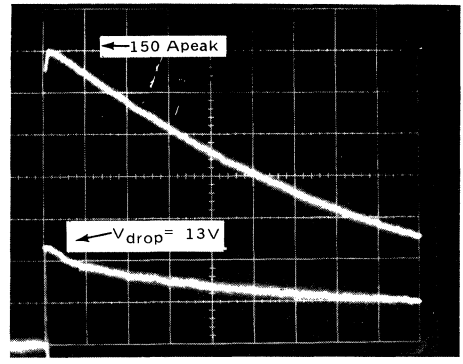
DYNAMIC TEST CIRCUITS (continued)

Fig. 18 - Upper trace (pulse voltage without device)
Lower trace (Intervention of LS5120)



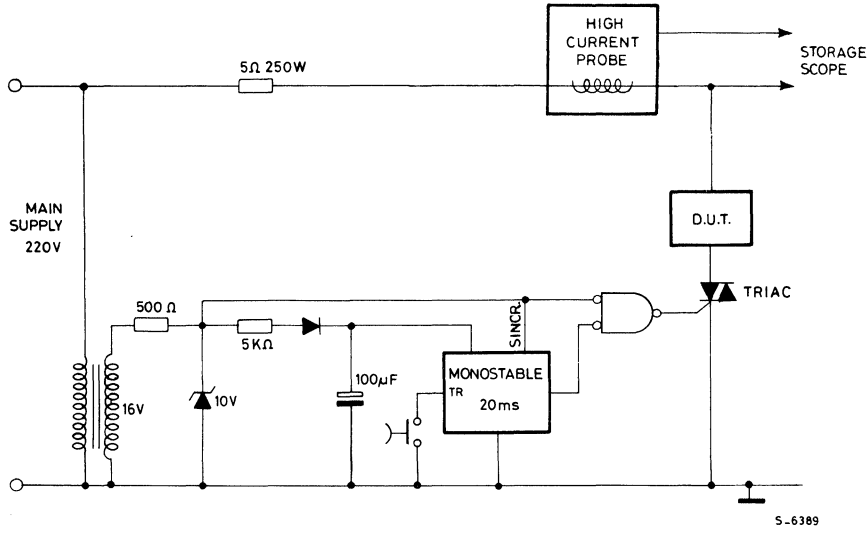
Time base = 50 μs/div.

Fig. 19 - Upper trace (current pulse in device)
Lower trace (Voltage drop across device)



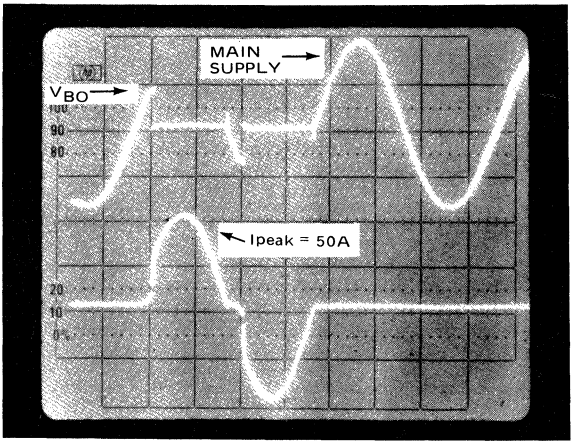
Time base = 50 μs/div.

Fig. 20 - Non repetitive peak current test



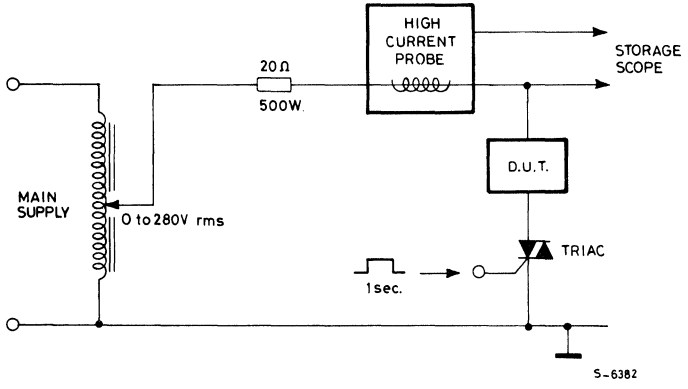
DYNAMIC TEST CIRCUITS (continued)

Fig. 21 - Upper trace (Mains supply used in tests. The intervention of the suppressor is clearly visible)
Lower trace (Current in the device during operation).



Time base = 5 ms/div

Fig. 22 - Repetitive peak current test



CIRCUIT DESCRIPTION

The LS5000 family of transient suppressors are innovative solid state devices designed for crowbar-type applications in electronic telephones and telecom equipment. They protect voltage sensitive components against overvoltages caused by lightning, induction from power lines and power line short circuits.

Qualitatively these devices behave like gas discharge tubes – they zero transients, rather than clamping them – but they offer a substantial improvement in performance, increased reliability and lower cost.

Breakover voltage is virtually independent of transient risetime, the off state leakage is very low and the characteristics are unaffected by ageing. A further advantage is that LS5000 suppressors are failsafe. If they are damaged by an extremely high current peak they become permanent short circuits, providing continuing protection and drawing attention to the need for replacement.

LS5000 series suppressors are bidirectional devices and are connected between the two points to be protected. They behave as a virtual open circuit with a very high resistance and low capacitance until the voltage across the therminals exceeds the rated breakover voltage. At this point the device fires, becoming a virtual short circuit and handling very high current peaks.

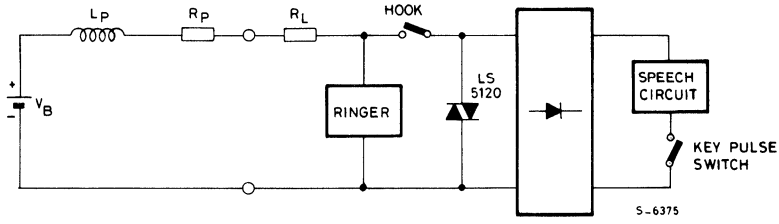
When the transient has been dissipated and the current falls below the 250 mA holding level, LS5000 suppressors turn off and return automatically to the normal open circuit state. The relatively high holding current level allows these devices to be used on remote-supplied lines such as telephone exchange links.

The three breakover voltages offered by the LS5000 family are designed to address specific problems in electronic telephones and telecom equipment. With a breakover voltage of ± 18V, the LS5018 is designed to protect the integrated circuits in multifrequency tone dialling telephones. It connects across the line between the hook switch and the polarity guard bridge (fig. 26). No secondary protection is needed.

For electronic telephones with loop disconnect dialling chips or rotary dials a higher breakover voltage is necessary to avoid suppression of the dialling pulses. The ± 120V LS5120 is designed for this application and, like the LS5018, connects across the line between the hook switch and the polarity guard bridge (figs. 23, 24, 25).

The ± 60V LS5060 is designed for use with the SGS SLIC (fig. 27) and balanced ringer applications.

Fig. 23 - Protection of an electromechanical bell telephone



CIRCUIT DESCRIPTION (continued)

Fig. 24 - Protection of an electronic ringer telephone

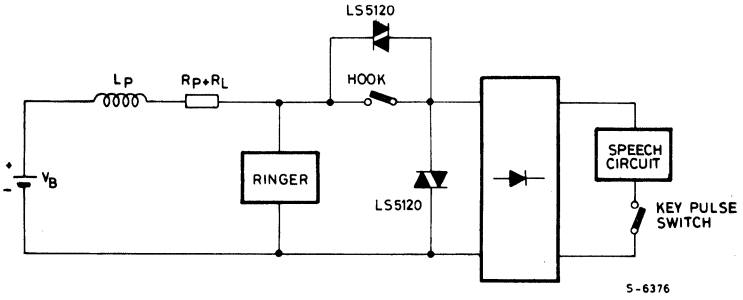


Fig. 25 - Protection of a discrete component SLIC

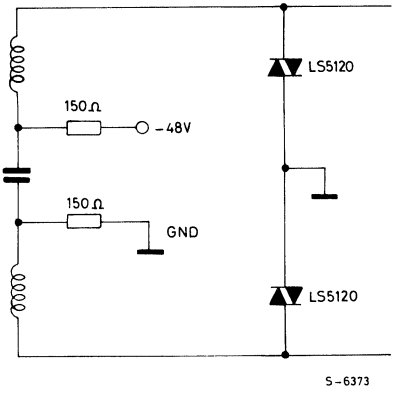
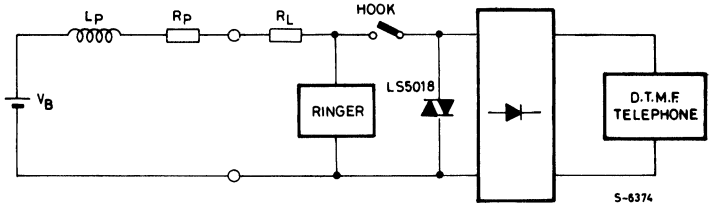


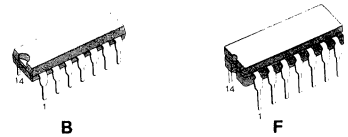
Fig. 26 - Protection of a DTMF telephone



M079

N-CHANNEL 2 x 2 x 2 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE: 18Ω
- INTERNAL CONTROL LATCHES
- 5.5 V_{PP} ANALOG SIGNAL CAPABILITY
- LESS THAN 1% TOTAL DISTORTION AT 0dbm
- LESS THAN -90db CROSS-TALK AT 1.6KHz 2V_{rms}



B
DIP-14 Plastic

F
DIP-14 Ceramic

ORDERING NUMBERS: M079B1
M079F1

DESCRIPTION

The SGS M079 consists of a 2x2x2 crosspoint array and 4 memory cells. Connection between two paths is determined by the status of the corresponding memory elements. If the latch is ON the paths are connected, if OFF disconnected.

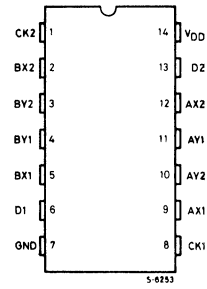
Every memory configuration can be inputted by reading the two D inputs using the two clocks. "1" on D determines the ON status and 0 the OFF status. The clock enters the Data input, on the high level. The correspondent switch is influenced at once. Data is then latched on falling edge of CK input. Thus storage is defined when CK goes down (see fig. 6, 7). CK and D levels are TTL compatible. The power on reset puts the memory elements into OFF status disconnecting the switches.

The M079 is available in 14 pin dual in-line plastic and ceramic packages.

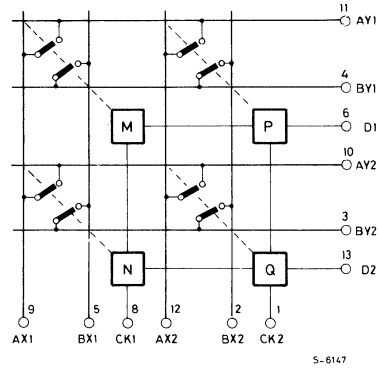
TRUTH TABLE

Logic Input D1	D2	CK1	CK2	Analog Connections Involved				Memory Status
1	X	1	0	AX1	BX1	AY1	BY1	Mon
0	X	1	0	AX1	BX1	AY1	BY1	Moff
X	1	1	0	AX1	BX1	AY2	BY2	Non
X	0	1	0	AX1	BX1	AY2	BY2	Noff
1	X	0	1	AX2	BX2	AY1	BY1	Pon
0	X	0	1	AX2	BX2	AY1	BY1	Poff
X	1	0	1	AX2	BX2	AY2	BY2	Qon
X	0	0	1	AX2	BX2	AY2	BY2	Qoff

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage range	-0.5 to 14	V
V_i	Input voltage range (CK1, CK2, D1, D2)	V_{DD} + 0.5	V
V_{IN}, V_{OUT}	Differential voltage between the two ends of every crosspoint in "OFF" status	14	V
P_{tot}	Power dissipation	600	mW
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-55 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions to extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{DD} at 12V ± 5%, V_{EE} = 3V)

	Parameter	Test Conditions*	Min.	Typ.	Max.	Unit
Crosspoint	αN (Cross Talk) Diaphony Attenuation Beetween each couple (Fig. 2)	V_{IN} = 2V_{rms} 1.6KHz	90			dB
	αN Longitudinal Attenuation (Fig. 3)	V_{IN} = 2V_{rms} 1.6KHz			0.15	dB
	RD Differential Impedance Between AXi and BXi (on AYm and BYm)	V_{IN} = 2V_{rms} 1.6KHz	200			KΩ
	RT Total Longitudinal Resistance*(Fig.3)				18	Ω
	CP Attenuation in off Status	V_{IN} = 2V_{rms} 1.6KHz	100			dB
	$\Delta \frac{RT}{2}$ Resistance Difference Related to one CP				1	Ω
	Total Distortion	V_{IN} = 0dBm 1.6KHz			1	%
Control Logic	V_{INH} Di and CKi High Level Input		2.4			V
	V_{INL} Di and CKi Low Level Input				0.8	V
	I_{INH} Di and CKi High Level Input	VCK = 2.7V V_D = 2.7V			1	μA
	I_{INL} Di and CKi Low Level Input Current	VCK = 0.4V V_D = 0.4V			1	μA
	I_{DD} Supply Current: N0 CP "ON" 1 CP "ON" 2 CP "ON"				 3 2.5 2	 mA mA mA
	I_{AL} Analog Input Leakage (when switches off)	V_{IN} = 0 to 12V			1	μA

* This is the sum of 2-switch resistance: the single switch is tested at 9Ω and its typical value is 5Ω

AC CHARACTERISTICS (T_{amb} = 25°C V_{DD} = 12V)

Parameter	Refert to figure	Min.	Typ.	Max	Unit
f Clock	Fig. 5		–	0.7	MHz
t Turn-on	Fig. 6	–	300	500	ns
t Turn-off	Fig. 6	–	330	700	ns
t_S Setup	Fig. 7	300		–	ns
t_H Hold	Fig. 7	300		–	ns
t_W clock pulse width		300	–		ns

Supply voltage must rise in more than 5ms					

Fig. 2 - Cross Talk Measurement

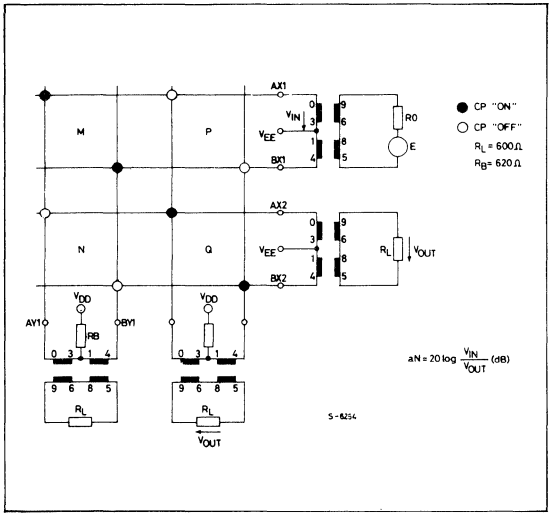


Fig. 3 - Equivalent Circuit of an Activated Phonic Connection

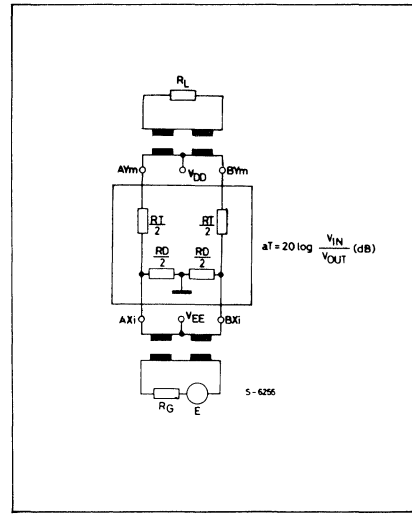


Fig. 4 - Equivalent Circuit an Unactivated Phonic Connection

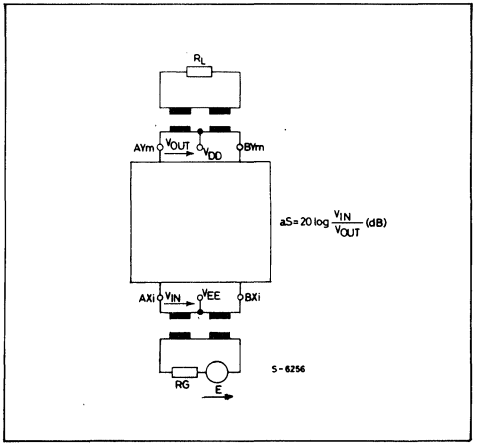


Fig. 5 - Circuit for Turn-on/Turn-off measurement.

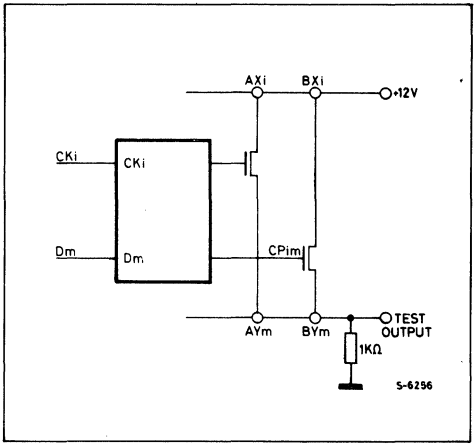


Fig. 6 - Switch Turn-on/Turn-off measurement

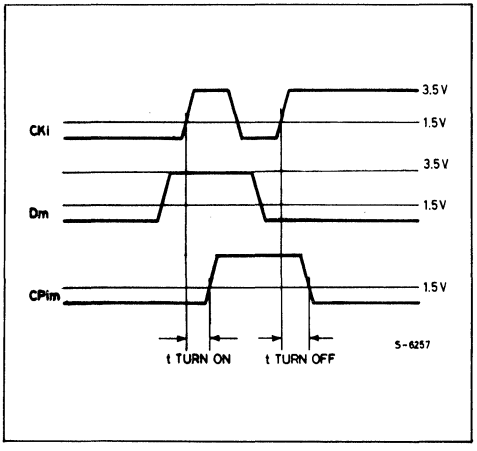
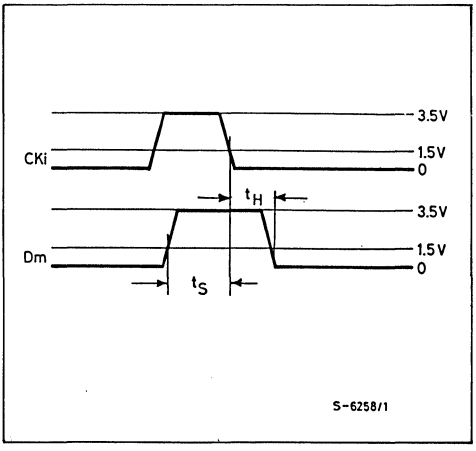


Fig. 7 - $t_{Set\text{-}up}$ / t_{Hold} measurement



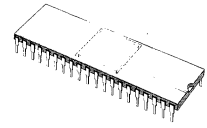
M088

DIGITAL SWITCHING MATRIX

- 256 INPUT AND 256 OUTPUT CHANNEL DIGITAL SWITCHING MATRIX
- BUILDING BLOCK DESIGNED FOR LARGE CAPACITY ELECTRONIC EXCHANGES, SUBSYSTEMS AND PABX
- NO EXTRA PIN NEEDED FOR NOT-BLOCKING SINGLE STAGE AND HIGHER CAPACITY SYNTHESIS BLOCKS (512 OR 1024 CHANNELS)
- EUROPEAN TELEPHONE STANDARD COMPATIBLE (32 SERIAL CHANNELS PER FRAME)
- PCM INPUTS AND OUTPUTS MUTUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- 6 MAIN "FUNCTIONS" OR "INSTRUCTIONS" AVAILABLE
- TYPICAL BIT RATE: 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE: 8KHz (TIME FRAME IS 125μs)
- 5V POWER SUPPLY WITH INTERNALLY GENERATED BIAS VOLTAGE
- MOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- CONSTRUCTED WITH SGS N-CHANNEL SILICON GATE HIGH DENSITY MOS PROCESS

Main istructions controlled by the microprocessor interface

- CHANNEL CONNECTION/DISCONNECTION
- CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/DISCONNECTION
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CHANNEL CONTROL WORD
- TRANSFER TO THE MICROPROCESSOR OF A SELECTED 0 CHANNEL PCM INPUT DATA



DIP-40 Ceramic

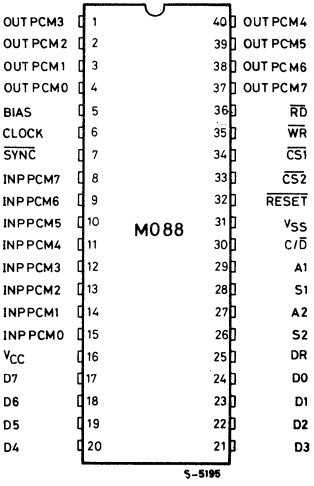
ORDERING NUMBER: M088 D1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 7	V
V_I	Input voltage	-0.3 to 7	V
V_O	Off state output voltage	7	V
P_{tot}	Total package power dissipation	1.5	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

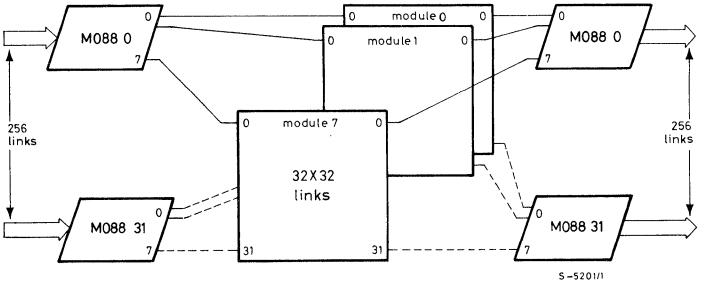
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS

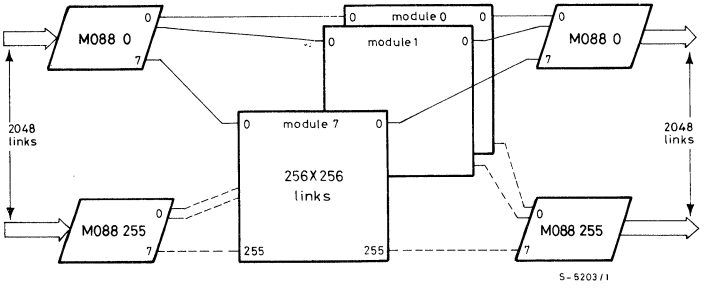


EXCHANGE NETWORKS APPLICATIONS

256 PCM links network (160 or 192 DSM): the 32 x 32 link module shown on the next page

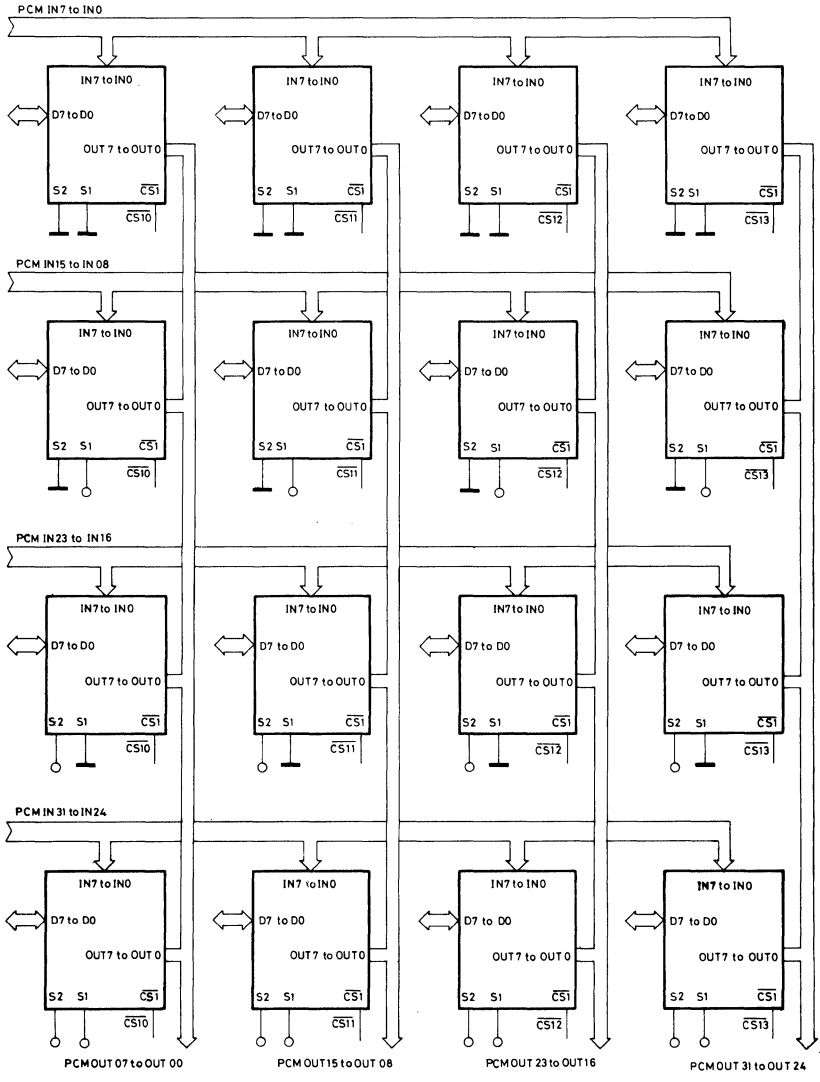


2048 PCM links network (1792 or 2048 DSM): the 256 x 256 link network is shown above



EXCHANGE NETWORKS APPLICATIONS (continued)

Single stage/sixteen devices configuration (32 by 32 links or 1024 channels)

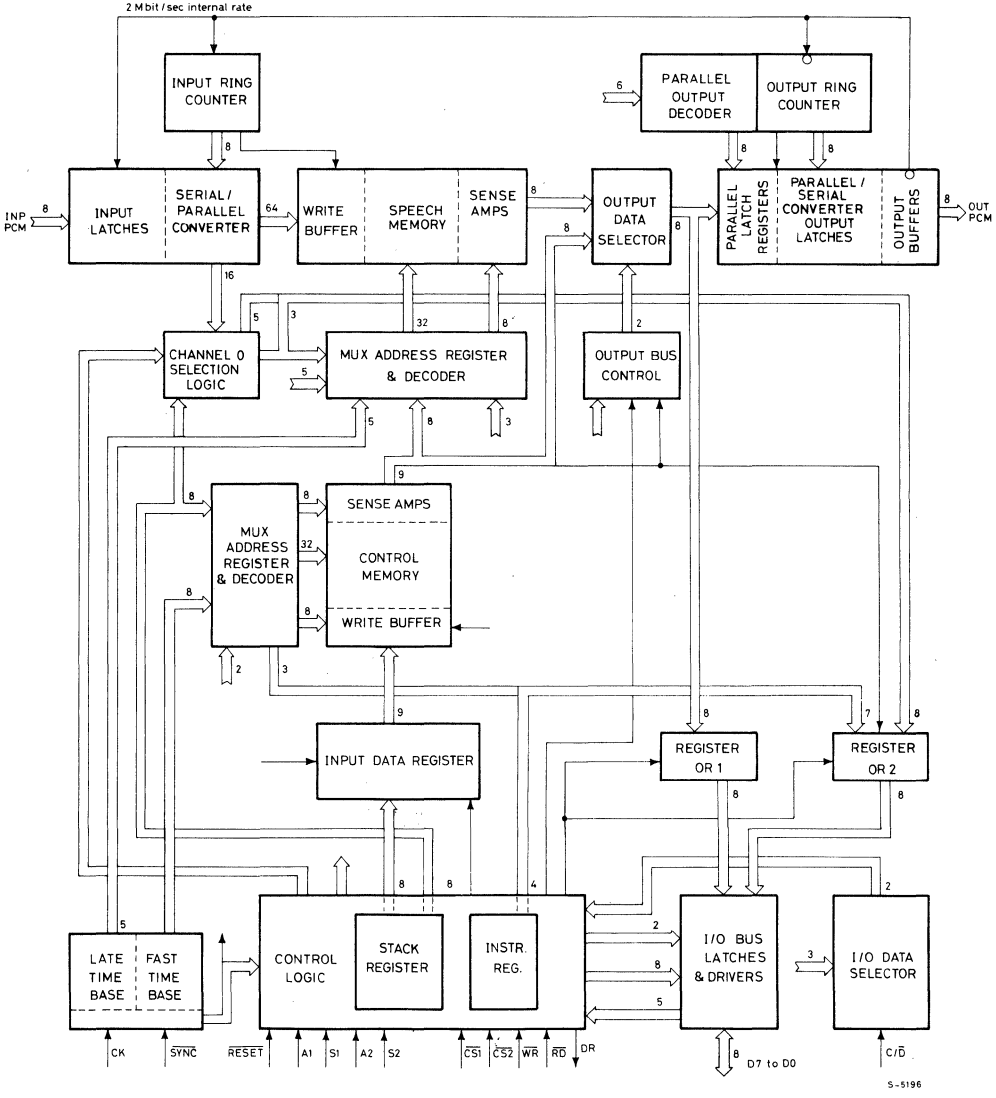


: HARDWARE CONNECTIONS RESPECTIVELY TO V_{CC}/V_{SS}

COMMON INPUT/OUTPUT PINS: C/$\overline{D}$; A1; A2; $\overline{RD}$; $\overline{WR}$; $\overline{CS2}$; D7 to D0; $\overline{RESET}$; CLOCK; $\overline{SYNC}$

FOUR DIFFERENT CHIP SELECT PINS ARE NEEDED

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
V_I	Input voltage	0 to 5.25	V
V_O	Off state output voltage	0 to 5.25	V
CLOCK freq.	Input clock frequency	4.096	MHz
$\overline{SYNC}$ freq.	Input synchronization frequency	8	KHz
T_{op}	Operating temperature	0 to 70	°C

CAPACITANCES (Measurement freq. = 1 MHz; T_{op} = 0 to 70°C; unused pins tied to V_{SS})

Parameter		Pins	Min.	Typ.	Max.	Unit
C_I	Input capacitance	6 to 15; 26 to 30; 32 to 36			5	pf
$C_{I/O}$	I/O capacitance	20 to 24			15	pf
C_O	Output capacitance	1 to 4; 17 to 19; 25; 37 to 40			10	pf

D.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)

All D.C. characteristics are valid 250 μs after V_{CC} and clock have been applied.

Parameter		Pin	Test conditions	Min.	Typ.	Max.	Unit
V_{ILC}	Clock input low level	6		-0.3		0.8	V
V_{IHC}	Clock input high level	6		2.0		V_{CC}	V
V_{IL}	Input low level	7 to 15 20 to 24 26 to 30 32 to 36		-0.3		0.8	V
V_{IH}	Input high level	7 to 15 20 to 24 26 to 30 32 to 36		2.0		V_{CC}	V
V_{OL}	Output low level	17 to 25	I_{OL} = 1.8 mA			0.4	V
V_{OH}	Output high level	17 to 25	I_{OH} = 250 μA	2.4			V
V_{OL}	PCM output low level	1 to 4 37 to 40	I_{OL} = 2.0 mA			0.4	V
I_{IL}	Input leakage current	6 to 15 26 to 30 32 to 36	V_{IN} = 0 to V_{CC}			10	μA
I_{DL}	Data bus leakage current	17 to 24	V_{IN} = 0 to V_{CC} V_{CC} applied; pins 35 and 36 tied to V_{CC}, after device initialization			± 10	μA
I_{CC}	Supply current	16	Clock freq. = 4.096 MHz		100		mA

A.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)

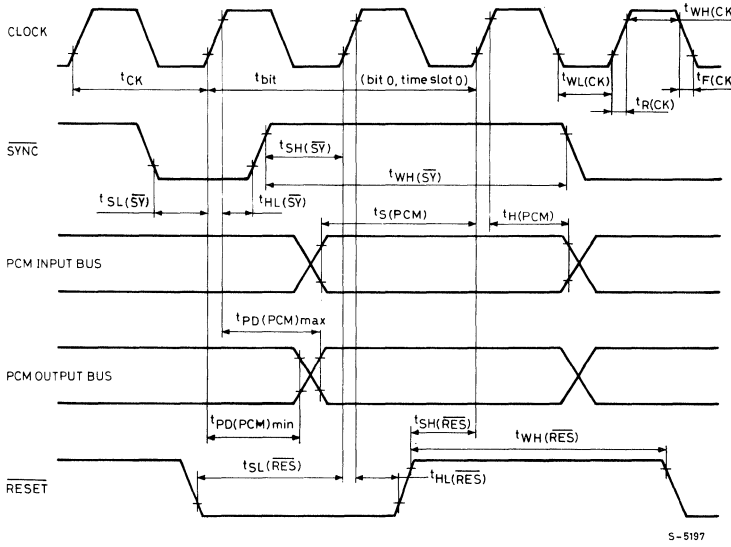
All A.C. characteristics are valid 250 μs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

Signal		Parameter	Test conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock period		230			ns
	t_{WL}	Clock low level width		100			ns
	t_{WH}	Clock high level width		100			ns
	t_R	Rise time				25	ns
	t_F	Fall time				25	ns
$\overline{SYNC}$	t_{SL}	Low level setup time		80			ns
	t_{HL}	Low level hold time		40			ns
	t_{SH}	High level setup time		120			ns
	t_{WH}	High level width		t_{CK}			ns
PCM input busses	t_S	Setup time		-40			ns
	t_H	Hold time		80			ns
PCM output busses	$t_{PD\ min}$	Propagation time referred to CK low level	C_L= 50 pf, R_L= 2 KΩ	80		180	ns
	$t_{PD\ max}$	Propagation time referred to CK high level	C_L= 50 pf, R_L= 2 KΩ	80		180	ns
$\overline{RESET}$	t_{SL}	Low level setup time		100			ns
	t_{HL}	Low level hold time		50			ns
	t_{SH}	High level setup time		90			ns
	t_{WH}	High level width		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low level width		150			ns
	t_{WH}	High level width		t_{CK}			ns
	t_{REP}	Repetition interval between active pulses	t_{REP}= 40 + 2 t_{CK} + + $t_{WL(CK)}$ + + $t_{R(CK)}$	see formula			ns
	t_{SH}	High level setup time to active read strobe		0			ns
	t_{HH}	High level hold time from active read strobe		20			ns
	t_R	Rise time				60	ns
	t_F	Fall time				60	
$\overline{RD}$	t_{WL}	Low level width		180			ns
	t_{WH}	High level width		t_{CK}			ns
	t_{REP}	Repetition interval between active pulses	t_{REP}= 40 + 2 t_{CK} + + $t_{WL(CK)}$ + + $t_{R(CK)}$	see formula			ns
	t_{SH}	High level setup time to active write strobe		0			ns
	t_{HH}	High level hold time from active write strobe		20			ns
	t_R	Rise time				60	ns
	t_F	Fall time				60	ns

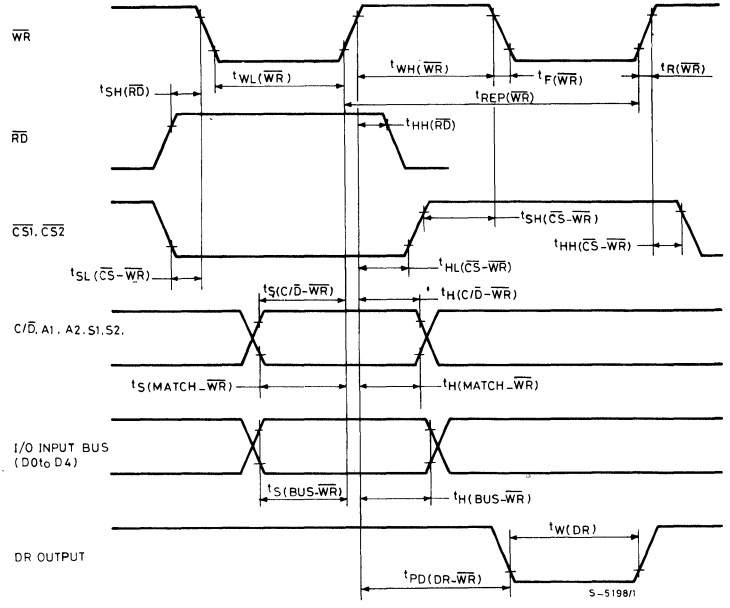
A.C. ELECTRICAL CHARACTERISTICS (continued)

Signal	Parameter		Test conditions	Min.	Typ.	Max.	Unit
$\overline{CS1}$, $\overline{CS2}$	$t_{SL(\overline{CS}-\overline{WR})}$	Low level setup time to $\overline{WR}$ falling edge	active case	0			ns
	$t_{HL(\overline{CS}-\overline{WR})}$	Low level hold time from $\overline{WR}$ rising edge	active case	0			ns
	$t_{SH(\overline{CS}-\overline{WR})}$	High level setup time to $\overline{WR}$ falling edge	inactive case	0			ns
	$t_{HH(\overline{CS}-\overline{WR})}$	High level hold time from $\overline{WR}$ rising edge	inactive case	0			ns
	$t_{SL(\overline{CS}-\overline{RD})}$	Low level setup time to $\overline{RD}$ falling edge	active case	0			ns
	$t_{HL(\overline{CS}-\overline{RD})}$	Low level hold time from $\overline{RD}$ rising edge	active case	0			ns
	$t_{SH(\overline{CS}-\overline{RD})}$	High level setup time $\overline{RD}$ falling edge	inactive case	0			ns
	$t_{HH((\overline{CS}-\overline{RD})}$	High level hold time from $\overline{RD}$ rising edge	inactive case	0			ns
C/$\overline{D}$	$t_{S(C/\overline{D}-\overline{WR})}$	Setup time to write strobe end		130			ns
	$t_{H(C/\overline{D}-\overline{WR})}$	Hold time from write strobe end		25			ns
	$t_{S(C/\overline{D}-\overline{RD})}$	Setup time to read strobe start		20			ns
	$t_{H(C/\overline{D}-\overline{RD})}$	Hold time from read strobe end		25			ns
A1, S1, A2, S2 (match inputs)	t_S(match-$\overline{WR}$)	Setup time to write strobe end		130			ns
	t_H(match-$\overline{WR}$)	Hold time from strobe end		25			ns
	t_S(match-$\overline{RD}$)	Setup time to read strobe start		20			ns
	t_H(match-$\overline{RD}$)	Hold time from read strobe end		25			ns
DR (data ready)	t_W	Low state width	instructions 5 and 6			$2 \cdot t_{CK}$	ns
	t_{PD}	DR output delay from write strobe end (active command)	instruction 5, C_L= 50 pf	$5 \cdot t_{CK}$		$14 \cdot t_{CK}$	ns
D0 to D7 (interface bus)	$t_{S(BUS-\overline{WR})}$	Input setup time to write strobe end		130			ns
	$t_{H(BUS-\overline{WR})}$	Input hold time from write strobe end		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling edge of read strobe	CL= 200 pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising edge of read strobe to high impedance state				80	ns

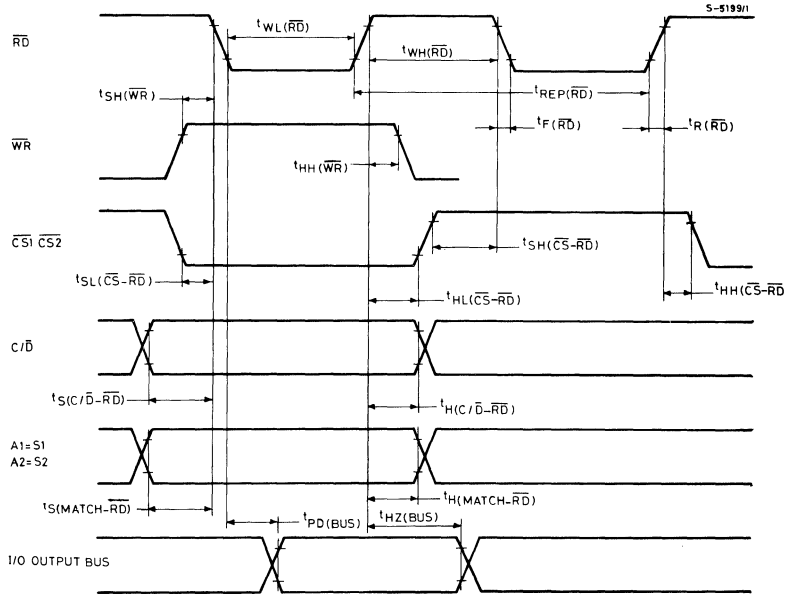
PCM TIMING, $\overline{\text{RESET}}$



WRITE OPERATION TIMING



READ OPERATION TIMING



GENERAL DESCRIPTION

The M088 is intended for large telephone switching systems, mainly central exchanges, digital line concentrators and private branch exchanges where a distributed microcomputer control approach is extensively used. It consists of a speech memory (SM), a control memory (CM), a serial/parallel and a parallel/serial converter, an internal parallel bus, an interface (8 data lines, 11 control signals) and dedicated control logic. By means of repeated clock division two timebases are generated. These are preset from an external synchronisation signal to two specific count numbers so that sequential scanning of the bases give synchronous addresses to the memories and I/O channel controls. Different preset count numbers are needed because of processing delays and data path direction. The timebase for the input channels is delayed and the timebase for output channels is advanced with respect to the actual time. Each serial PCM input channel is converted to parallel data and stored in the speech memory at the beginning of any new time slot (according to first timebase) in the location determined by input pin number and time slot number. The control memory CM maintains the correspondences between input and output channels. More exactly, for any output pin/output channel combination the control memory gives either the full address of the speech memory location involved in the PCM transfer or an 8-bit word to be supplied to the parallel/serial output converter. A 9th bit at each CM location defines the data source for output links, low for SM, high for CM.

The late timebase is used to scan the output channels and to determine the pins to be serviced within each channel; enough idle cycles are left to the microprocessor for asynchronous instruction processing. Two 8-bit registers OR1 and OR2 supply feedback data for control or diagnostic purposes; OR1 comes from internal bus i.e. from memories, OR2 gives an opcode copy and additional data to the microcomputer. A four byte-five bit stack register and an instruction register, under microcomputer control, store input data available at the interface.

Dedicated logic, under control of the microprocessor interface, extracts the 0 channel content of any selected PCM input bus, using spare cycles of SM.

PIN DESCRIPTION

D7 to D0 (pins 17 to 24)

Data bus pins. The bidirectional bus is used to transfer data and instructions to/from the microprocessor. D0 is the least significant digit. The output bus is 8 bits wide; input is only 5 bits wide.
The bus is tristate and cannot be used while $\overline{\text{RESET}}$ is held low.
The meaning of input data, such as bus or channel numbers, and of expected output data is specified in detail by the instruction description.

C/$\overline{\text{D}}$ (pin 30)

Input control pin, select pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data, while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. In a read operation OR1 is selected by C/$\overline{\text{D}}$ = 0, OR2 by C/$\overline{\text{D}}$ = 1.

A1, S1, A2, S2 (pins 26 to 29)

Address select or match pins. In a multi-chip configuration (e.g. a single stage matrix expansion), using the same $\overline{\text{CS}}$ pins, the match condition (A1 = S1 and A2 = S2) leaves the command instruction as defined; on the contrary the mismatch condition modifies the execution as follows: instructions 1 and 3 are reversed to channel disconnection, instruction 5 is unaffected, instructions 2-4-6 are cancelled (not executed).
Bus reading takes place only on match condition, instruction flow is in any case affected.
Each pins couple is commutative: in a multichip configuration pins S1 and S2 give a hard-wired address selection for individual matrixes, while in single configuration S1 and A1 or S2 and A2 are normally tied together.

$\overline{\text{CS1}}$, $\overline{\text{CS2}}$ (pins 33, 34)

Commutative chip select pins. They enable the device to perform valid read/write operations (active low). Two pins allow row/column selection with different types of microprocessors; normally one is tied to ground.

$\overline{\text{WR}}$ (pin 35)

Pin $\overline{\text{WR}}$, when $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are low, enables data transfer from microprocessor to the device. Data or opcode and controls are latched on $\overline{\text{WR}}$ rising edge. Because of internal clock resynchronization one single additional requirement is recommended in order to produce a simultaneous instruction execution in a multichip configuration: $\overline{\text{WR}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

$\overline{\text{RD}}$ (pin 36)

When $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are low and match condition exists, a low level on $\overline{\text{RD}}$ enables a register OR1 or OR2 read operation, through the bidirectional bus.
In addition, the rising edge of $\overline{\text{RD}}$ latches C/$\overline{\text{D}}$ and the match condition pins in order to direct the internal flow of operations. Because of internal clock resynchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multichip configuration: the $\overline{\text{RD}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

DR (pin 25)

Data ready. Normally high, DR output pin goes low to tell the microprocessor that:

a) the instruction code was found to be invalid;

b) executing instruction 5 an active output channel was found in the whole matrix array, that is a CM word not all "ones" was found in a configuration of devices sharing the same $\overline{\text{CS}}$ pins;

c) executing instruction 6 "0 channel extraction" took place and OR2 was loaded with total number of messages inserted on 0 time slot.

DR is active about two clock cycles in case **b** and **c**; in case **a** it is left low until a valid instruction code is supplied.

PIN DESCRIPTION (continued)

$\overline{\text{RESET}}$ (pin 32)

$\overline{\text{RESET}}$ control pin is normally used at the very beginning to inizialize the device or the network. Any logical status is reset and CM is set to all "ones" after $\overline{\text{RESET}}$ going low.
The internal initialization routine takes one time frame whatever the $\overline{\text{RESET}}$ width on low level (minimum one cycle roughly), but it is repeated an integer number of time frames as long as $\overline{\text{RESET}}$ is found low during 0 time slot.
Initialization pulls the interface bus immediately to a high impedance state. After the CM has been set to all "ones" the PCM output channels are also set to high impedance state (that is pulled to "ones").

CLOCK (pin 6)

Input master clock. Typical frequency is 4.096 MHz. First division gives an internal clock controlling the input and output channels bit rate.

$\overline{\text{SYNC}}$ (pin 7)

Input synchronization signal is active low. Typical frequency is 8 kHz.
Internal time bases are forced by synchronism to an assigned count number in order to restore channels and bit sequential addressing to a known state. Count difference between the bases is 32, corresponding to two time slots, that is the minimum PCM propagation time, or latency time.

INP PCM 7 to INP PCM 0 (pins 8 to 15)

PCM input busses or pins; they accept a standard 2 Mbit/s rate. Bit 1 (sign bit) is the first of the serial sequence; in a parallel conversion it is left adjusted as the most significant digit.

OUT PCM 7 to OUT PCM 0 (pins 37 to 40 and 1 to 4)

PCM output busses or pins; bit rate and organization are the same as input pins.
Output buffers are open drain type in order to simplify wired-or connections and minimize current spike problems in multichip configuration systems.
The device drives the output channels theoretically one bit time before input channels are needed by specifications: this feature allows inputs and outputs to be tied together cancelling any analog delay of digital outputs up to

$$t_{DEL\ max} = t_{bit} - \overline{t_{PD\,(PCM)max}} + \underline{t_{PD\,(PCM)min}}$$

BIAS (pin 5)

Internally generated bias voltage (-2.5 to -3.0V for V_{CC} in the operating range). A max. 220 pf capacitor connected to pin 5 provides improved filtering.

MIXED $\overline{\text{RD}}$ & $\overline{\text{WR}}$ OPERATIONS

In principle $\overline{\text{RD}}$ and $\overline{\text{WR}}$ operations are allowed in any order within specification constraints.
In practive, only one control pin is low at any given time when $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are enabled.
If by mistake or hardware failure both $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins are low, the interface bus is internally pushed to tristate condition as long as $\overline{\text{WR}}$ is held low and input registers are protected.
Registers OR1 and OR2 can be read in any order with a single $\overline{\text{RD}}$ strobe using C/$\overline{\text{D}}$ as multiplexing control; never the less this procedure is not recommended because the device is directed for instruction flow only according to data latched by $\overline{\text{RD}}$ rising edge.
Multiple $\overline{\text{RD}}$ operations of the same kind are allowed without affecting the instruction flow: only "new" OR1 or OR2 read operations step the flow.
Input and output registers are held for sure in the previous state for the first 3 cycles following an opcode or an OR2 read.

FUNCTIONAL DESCRIPTION OF SPECIFIC MICROPROCESSOR OPERATIONS

The device, under microprocessor control, performs the following instructions:

1 CHANNEL CONNECTION/DISCONNECTION
2 CHANNEL DISCONNECTION
3 INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/CHANNEL DISCONNECTION)
4 TRANSFER OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
5 TRANSFER OF A SINGLE OUTPUT CHANNEL CONTROL WORD
6 TRANSFER OF A SELECTED 0 CHANNEL PCM INPUT DATA ACCORDING TO AN 8-BIT MASK PREVIOUSLY STORED IN THE "EXPECTED MESSAGES" REGISTER.

The instruction flow is as follows.

Any input protocol is started by the microprocessor interface loading the internal stack register with 2 bytes (4 bytes for instructions 1 and 3) qualified as data bytes by $C/\overline{D} = 0$ and a specific opcode qualified by $C/\overline{D} = 1$ (match condition is normally needed).

After the code is loaded in the instruction register it is immediately checked to see whether it is acceptable and if not it is rejected. If accepted the instruction is also processed as regards match condition and is appended for execution during the memories' spare cycles.

Four cases are possible:

a) the code is not valid; execution cannot take place, the DR output pin is reset to indicate the error; all registers are saved;
b) the code is valid for types 2, 4 and 6 but it is unmatched; execution cannot take place, DR is not affected.
c) the code is valid for types 1 and 3 and it is unmatched; the instruction is interpreted as a channel disconnection.
d) the code is valid and is either matched or of type 5; the instruction is processed as received.

Validation control takes only two cycles out of a total execution time of 5 to 13 cycles; the last operation is updating of the content of registers OR1 and OR2.

During a very long internal operation (device initialization after $\overline{\text{RESET}}$ going high or execution of instruction 6) a new set of data bytes with a valid opcode is accepted while a wrong code is rejected. At the end of the current routine execution takes place in the same way as described before.

At the end of an instruction it is normally recommended to read one or both registers. To enable instruction 6, however, it is necessary to read register OR2. This is because instruction 6, used between other short instructions of type 1 to 5, must have a lower priority and can be enabled only after the short instructions have been completed. Instruction 6 normally has a long process and a special flow which is described below.
First a not-all-zero mask is stored in the "expected messages" register and in another "background" register. This operation starts the second phase of instruction 6 which is called "channel 0 extraction" and is repeated at the beginning of any new time frame. At the beginning of the time frame a new copy of activated channels to be extracted is made from the "background register" and put in the "expected messages" register. In addition the latter register is modified to indicate the exact number of messages that have arrived. The term messages covers any input 0 channel data with starting sequence different from the label 01. So using this label the number of expected messages can be reduced to correspond to the number of effective messages. If and only if the residual number is different from zero will the device start the extraction protocol at the end of the current routine.
The procedure is as follows: the DR output is pulsed low as a two cycle interrupt request and OR2 is loaded with the total number of active channels to be extracted.

FUNCTIONAL DESCRIPTION (continued)

The transfer of OR2 content to the microprocessor continues the extraction which consists of repeated steps of OR1 and OR2 loading, indicating respectively the message and the incoming bus number. Reading the registers in the order OR1, OR2 must be continued until completion or until the time frame runs out.
With a new time frame a new extraction process begins, resuming the copy operation from the background register.

During extraction the active channels are scanned from the highest to the lowest number (from 7 to 0). While extraction is being carried out the time interval requirements between active rising edges of $\overline{RD}$ are minimum 5 to 13 t_{CK} for sequence OR2 - OR1 and minimum 3 times t_{CK} for sequence OR1 - OR2. More details are given in the following tables.

INSTRUCTION TABLES

The most significant digits of OR2 A7, A6, A5 are a copy of the PCM selected output bus; the least significant digits of OR2 are the opcode, C8 is the control bit. In any case parentheses ( ) define actual register content.

INSTRUCTION 1 : CHANNEL CONNECTION/DISCONNECTION

CONTROL SIGNALS					DATA BUS								NOTES
match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bi_2	Bi_1	Bi_0	1st data byte: selected input bus
X	0	0	0	1	X	X	X	Ci_4	Ci_3	Ci_2	Ci_1	Ci_0	2nd data byte: selected input channel
X	0	0	0	1	X	X	X	X	X	Bo_2	Bo_1	Bo_0	3rd data byte: selected output bus
X	0	0	0	1	X	X	X	Co_4	Co_3	Co_2	Co_1	Co_0	4th data byte: selected output channel
yes/no	1	0	0	1	X	X	X	X	0	0	0	1	instruction opcode
yes	0	0	1	0	C7 (1 (Bi_2	C6 1 Bi_1	C5 1 Bi_0	C4 1 Ci_4	C3 1 Ci_3	C2 1 Ci_2	C1 1 Ci_1	C0 1) Ci_0)	OR1: CM content copy, that is for mismatch condition for match condition
yes	1	0	1	0	A7 (Bo_2 (Bo_2	A6 Bo_1 Bo_1	A5 Bo_0 Bo_0	C8 1 0	0 0 0	0 0 0	0 0 0	1 1) 1)	OR2: that is for mismatch condition for match condition

INSTRUCTION 2 : OUTPUT CHANNEL DISCONNECTION

CONTROL SIGNALS					DATA BUS								NOTES
match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	B_{O2}	B_{O1}	B_{O0}	1st data byte: selected output bus
X	0	0	0	1	X	X	X	C_{O4}	C_{O3}	C_{O2}	C_{O1}	C_{O0}	2nd data byte: selected output channel
yes	1	0	0	1	X	X	X	X	0	0	1	0	instruction opcode
yes	0	0	1	0	1	1	1	1	1	1	1	1	OR1: CM content copy (output channel is inactive)
yes	1	0	1	0	A7 (B_{O2}	A6 B_{O1}	A5 B_{O0}	1 1	0 0	0 0	1 1	0 0)	OR2: that is

INSTRUCTION 3 : LOADING A MICROPROCESSOR BYTE

CONTROL SIGNALS					DATA BUS								NOTES
match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	C_{i7}	C_{i6}	C_{i5}	1st data byte: most significant digits to be inserted
X	0	0	0	1	X	X	X	C_{i4}	C_{i3}	C_{i2}	C_{i1}	C_{i0}	2nd data byte: least significant digits to be inserted
X	0	0	0	1	X	X	X	X	X	B_{O2}	B_{O0}	B_{O1}	3rd data byte: selected output bus
X	0	0	0	1	X	X	X	C_{O4}	C_{O3}	C_{O2}	C_{O1}	C_{O0}	4th data byte: selected output channel
yes/no	1	0	0	1	X	X	X	X	0	1	0	0	instruction opcode
yes	0	0	1	0	C7 (1 (C_{i7}	C6 1 C_{i6}	C5 1 C_{i5}	C4 1 C_{i4}	C3 1 C_{i3}	C2 1 C_{i2}	C1 1 C_{i1}	C0 1) C_{i0})	OR1: CM content copy, that is for mis match condition for match condition
yes	1	0	1	0	A7 (B_{O2}	A6 B_{O1}	A5 B_{O0}	1 1	0 0	1 1	0 0	0 0)	OR2: that is

INSTRUCTION 4 : TRANSFER OF A SINGLE PCM SAMPLE

CONTROL SIGNALS					DATA BUS								NOTES
match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo_2	Bo_1	Bo_0	1st data byte: selected output bus
X	0	0	0	1	X	X	X	Co_4	Co_3	Co_2	Co_1	Co_0	2nd data byte: selected output channel
yes	1	0	0	1	X	X	X	X	1	0	1	1	instruction opcode
yes	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1: CM content copy if C8 = 1; or SM content sample if C8=0
					S7	S6	S5	S4	S3	S2	S1	S0	
yes	1	0	1	0	A7	A6	A5	C8	1	0	1	1	OR2: that is
					(Bo_2	Bo_1	Bo_0	C8	1	0	1	1)	

Note: S7 . . . S0 is a parallel copy of a PCM data, S7 is the most significant digit and the first of the sequence.

INSTRUCTION 5 : TRANSFER OF AN OUTPUT CHANNEL CONTROL WORD

CONTROL SIGNALS					DATA BUS								NOTES
match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo_2	Bo_1	Bo_0	1st data byte: selected output bus
X	0	0	0	1	X	X	X	Co_4	Co_3	Co_2	Co_1	Co_0	2nd data byte: selected output channel
X	1	0	0	1	X	X	X	X	1	0	0	0	instruction opcode
yes	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1: selected CM word copy
yes	1	0	1	0	A7	A6	A5	C8	1	0	0	0	OR2: that is
					(Bo_2	Bo_1	Bo_0	C8	1	0	0	0)	

INSTRUCTION 6 : CHANNEL 0 SELECTION MASK STORE/DATA TRANSFER

CONTROL SIGNALS					DATA BUS								NOTES
match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Mi7	Mi6	Mi5	1st data byte: most sign. digits of selection mask
X	0	0	0	1	X	X	X	Mi4	Mi3	Mi2	Mi1	Mi0	2nd data byte: least sign. digits of selection mask
yes	1	0	0	1	X	X	X	X	1	1	1	0	instruction opcode
MASK STORE CONTROL													
yes	0	0	1	0	(previous content)								OR1: register is not affected
yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see below
FIRST DATA TRANSFER (after DR going low)													
yes	0	0	1	0	(previous content)								OR1: register is not affected
yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see below
REPEATED DATA TRANSFER (after first OR2 transfer)													
yes	0	0	1	0	S7	S6	S5	S4	S3	S2	S1	S0	OR1: expected message stored in SM
yes	1	0	1	0	P2	P1	P0	Fn	1	1	1	0	OR2: see below

Notes: 1) About mask bits Mi0 to Mi7 a logic "0" level means disabling condition, a logic "1" level means enabling condition.
2) A null mask or a $\overline{RESET}$ pulse clear the mask and the deep background mask registers and disable channel 0 extraction function.
3) Reading of OR2 is optional after mask store or redefinition, because function is activated only by not-null mask writing.
4) After mask store (N2 N1 N0) is the sum of activated channels, after DR is the sum of active channels; Tn= 1/0 means activation/suppression of the function after store while after DR only Tn= 1 can appear to tell a not-null configuration to be extracted.
5) Reading of OR2 is imperative after DR in order to step the data transfer; reading of OR1 is also needed to scan in descending order the priority register. Relevant messages only are considered, that means only messages with a MSD label different from 0 1.
6) (P2 P1 P0) is the PCM bus on which the message copied in OR1 was found; Fn is a continuation bit telling respectively on level 1/0 for any more/no more extraction to be performed.

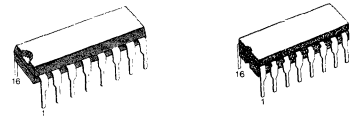
M089

2x8 CROSSPOINT MATRIX

- VERY LOW ON RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE ISOLATION
- SERIAL SWITCH ADDRESSING, μ-PROCESSOR COMPATIBLE

DESCRIPTION

The M089 is a 2x8 crosspoint matrix consisting of 16 N-channel MOS transistors.
The device has been specially designed to provide switches with low cross-talk, high off-state isolation (both better than -90dB) and low on-resistance.

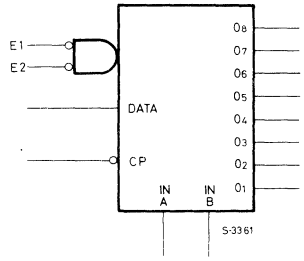


B
Plastic

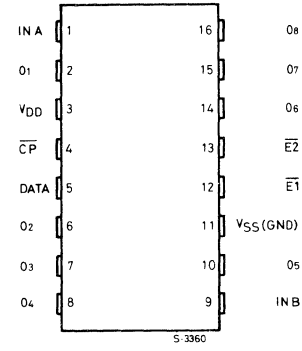
F/D
Ceramic Frit-seal
Ceramic Metal-seal

ORDERING NUMBERS: M089 B1
M089 F1
M089 D1

LOGIC DIAGRAM



PIN CONFIGURATION

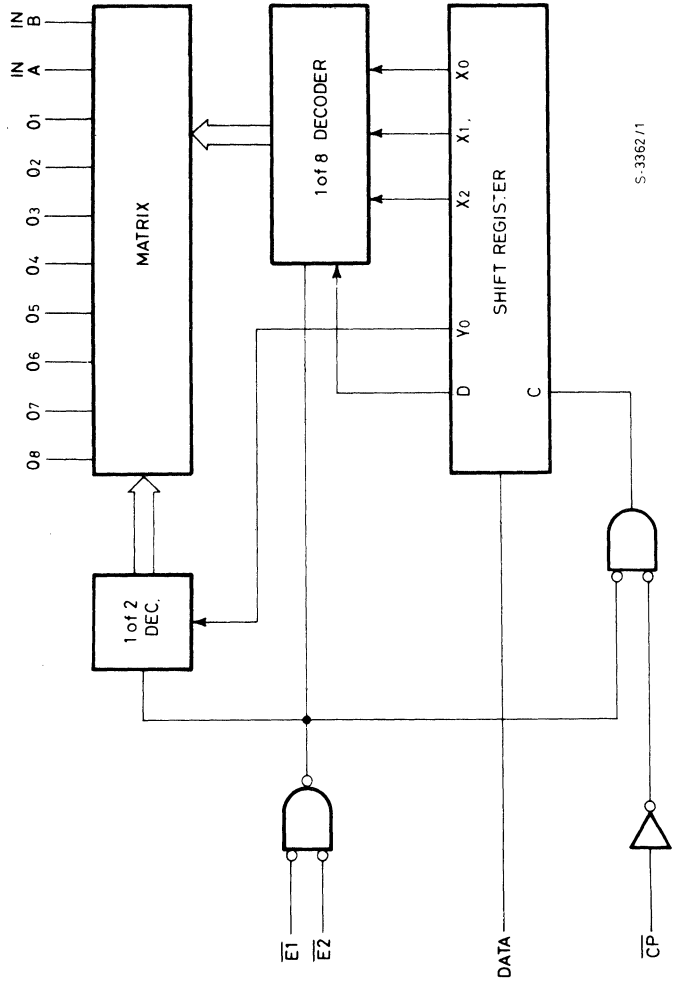


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to 17	V
V_I	Input voltage pins 4, 5, 12, 13	-0.5 to 17	V
$V_{IN} - V_{OUT}$	Differential voltage across any disconnected switch	10	V
P_{tot}	Total power dissipation	640	mW
T_{op}	Operating temperature range : for plastic for ceramic	0 to 70 -40 to 70	°C °C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The M089 is capable of forming any combination of switch conditions in an 8x2 matrix. Each switch is individually set and a latch maintains it in its set condition.
The switch address and control bits are loaded serially into an internal shift register (5 bit for M089, when inputs E_1, and E_2 are low. The address bits consist of: 3 input selection bits (X_0-X_2) and a single output selection bit (Y_0). A fifth (control) bit (D) defines whether the chosen switch is to be opened or closed.
During normal selection the R bit must be a 1.

D	Y_0	X_2	X_1	X_6

M089 Shift Register Bit Allocation

Data bits are clocked into the shift register on the high to low transition of the clock input (CP). If more than 5 clock transmission are applied during loading of the shift register the last 5 data bits are loaded into it. The status of the switch addressed changes on the low to high transition of one or both enable inputs.

ENABLE INPUTS TRUTH TABLE

$\overline{E}_1$	$\overline{E}_2$	FUNCTION
		Data Load
L	L	addressed switch changed
⌐	L	
L	⌐	
⌐	⌐	

DATA BIT TRUTH TABLE

Data	Switch status after enable transition
L	disconnect
H	connect

DATA BITS TRUTH TABLE FOR SWITCH SELECTION

	O_1 Y_0 X_2 X_1 X_0	O_2	O_3	O_4	O_5	O_6	O_7	O_8
IN A	1111	1011	1101	1001	1110	1010	1100	1000
IN B	0111	0011	0101	0001	0110	0010	0100	0000

For example to address the switch connecting IN A to O_5 the shift register must be loaded with the code:

	D Y_0 X_2 X_1 X_0
to connect	11110
to disconnect	01110

ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C for M089 B1; -40 to 70°C for M089 F1, D1; V_{DD} = 14V to 16V unless otherwise specified)

Parameter			Test conditions	Min.	Typ.	Max.	Unit
R_{ON}*	ON-resistance		T_{amb}= 25°C $V_{i\ (A,\ B)}$= 3.5V V_{DD}= 14V $I_{D(min)}$= 10 mA		10	15	Ω
ΔR_{ON}	ON-resistance variation in any package		T_{amb}= 25°C V_i= 3.5V V_{DD}= 14V I_D= 10 mA			± 2	%
I_{DD}	Supply current					7	mA
I_{LI}	Input leakage	pins 4, 5 12, 13	V_i= 5V			1	μA
		pins 1, 9	V_{iA}, V_{iB}= 4.5V V_{O1}, V_{O8}= 1.5V			0.2	μA
			V_{iA}, V_{iB}= 6V V_{O1}, V_{O8}= 1.5V			1	μA
I_{LO}	Output leakage	pins 2, 6, 7 8, 10, 14 15, 16	V_{O1}, V_{O8}= 4.5V V_{iA}, V_{iB}= 1.5V			0.2	μA
			V_{O1}, V_{O8}= 6V V_{iA}, V_{iB}= 1.5V			1	μA
V_{low}	Logic 0 input level		All inputs	-0.3		0.8	V
V_{high}	Logic 1 input level		All inputs	4.5		V_{DD}	V
CT	Cross-talk attenuation		See fig. 4	90	95		dB
I_O	Off isolation		See fig. 5	90	95		dB
f_{CL}	Maximum clock input frequency		See fig. 6 for M089			1	MHz
T_{LG}	Lag time			100			ns
T_{LD1}	Lead time			400			ns
T_{LD2}				150			
T_{WR}	Write time					3	μs
t_W	Clock pulse width			0.4		100	μs

* See fig. 1 and 2 for R_{ON} variation with temperature and V_{BIAS}.

Fig. 1 - R_{ON} derating vs. temperature typ.

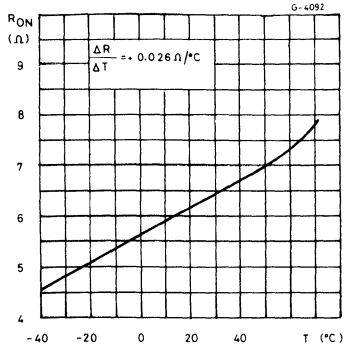
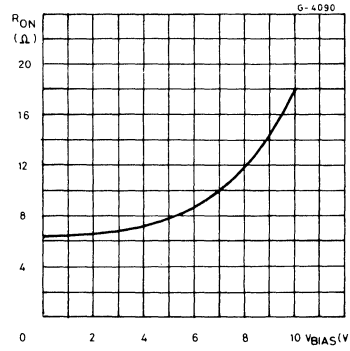


Fig. 2 - R_{ON} derating vs. V_{BIAS}.



TEST CIRCUITS

Fig. 3 - R_{ON} measurement

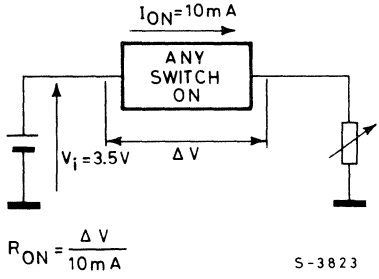


Fig. 4 - Crosstalk measurements

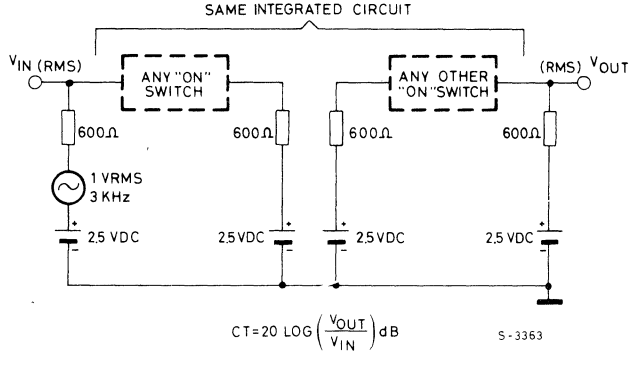
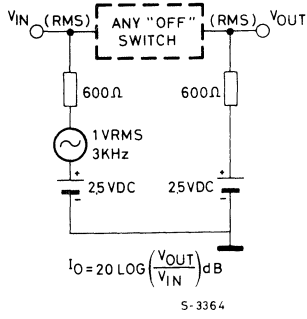
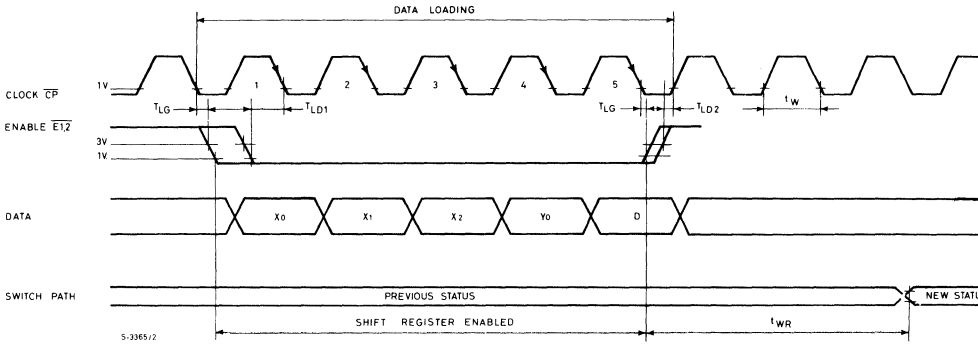


Fig. 5 - Off isolation measurement



TIMING DIAGRAMS

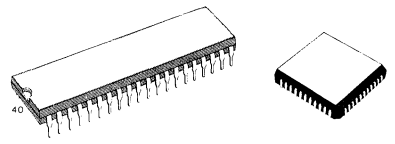
Fig. 6



N-CHANNEL 12 x 8 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE (TYP. 35Ω AT V_{DD} = 14V)
- INTERNAL CONTROL LATCHES
- 2 V_{PP} ANALOG SIGNAL CAPABILITY
- LESS THAN 1% TOTAL DISTORTION AT 0dBm
- LESS THAN -95dB CROSS-TALK AT 1KHz 1V_{PP}

The SGS M093 contains a 12x8 array of cross-point together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one.
The M093 is available in a 40 lead dual in-line plastic, or 44 lead plastic chip carrier packages. Logic inputs are TTL compatible.

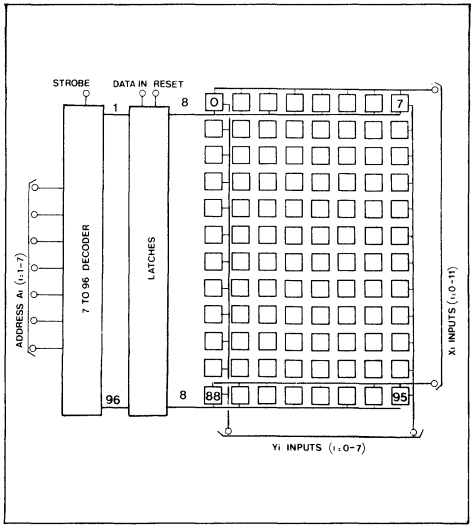


B
DIP-40 Plastic

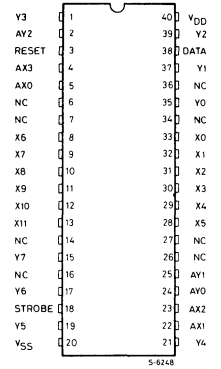
C
Plastic Chip Carrier

ORDERING NUMBER: M093B
M093C

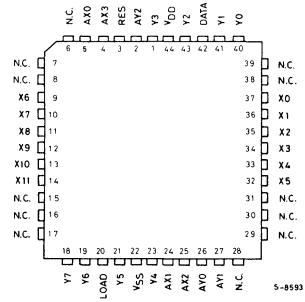
BLOCK DIAGRAM



PIN CONFIGURATION



CHIP CARRIER



THRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
address not allowed 0	1	1	0	0	0	0	no connection
address not allowed 1	1	1	0	0	0	0	no connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
address not allowed 0	1	1	1	0	0	0	no connection
address not allowed 1	1	1	1	0	0	0	no connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	0	X11 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	1	X11 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to 18	V
V_{IN}	Input Voltage Range	-0.5 to V_{DD} +0.5	V
I_{IN}	DC Input Current (Analog Input)	± 10	mA
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-50 to 125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

V_{DD}	Supply voltage	10	to 16	V
T_{op}	Operating Temperature	0	to 70	°C
V_{IN}	(Logic signal)	0	to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = 14V)

Parameter	Test Condition	Min.	Typ.	Max.	Unit
CROSSPOINT					
Operating Current	f_o = 100KHz			35	mA
On Resistance	V_{IDC} = 6.75V V_{ODC} = 6.5V (see fig. 1)		35	75	Ω
ΔR on between any 2 switch			6	10	Ω
Off Leakage *	All switches off $V_{OS} = V_{IS}$ = 0 to V_{DD}			± 3	μA
CONTROLS					
V_{IL}				0.8	V
V_{IN}		2.4			V
Input Leakage *	V_{IN} = 0 to V_{DD}			± 3μA	nA

* There limits are valid on the total temperature range: 0-70°C at 25°C these limits become ±100nA.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF all input square wave rise and fall times = 20ns, V_{DD} = 14V)

Parameter		Test Conditions					Values			Unit
		Note	f_i (KHz)	R_L (KΩ)	V_{is} (V_{PP})	V_{DC} (V)	Min.	Typ.	Max.	
CROSSPOINTS										
t_{PHL}, t_{PLH}	Propagation delay time (Switch ON) signal input to output	Fig. 2		1	2	5		30	100	ns
	Frequency response (Any switch ON) (20 log (V_{OS}/V_{IS}) = -3dB	C_L = 3pF		0.091	2	5		50		MHz
	Sine wave distortion		1000	0.091	2	5			1	%
	Feedthrough (All switches OFF)	Fig. 3	10	1	2	5	-90			dB
	Frequency for signal crosstalk Attenuation of 40dB Attenuation of 110dB	Fig. 4		1	2	5	1 5			MHz KHz
C	Capacitance Xn to ground							15		pF
	Yn to ground		1000		0.1	5		15		
	Feedthrough							0.4		
C	Capacitance Logic input to ground		1000		0.1	5		5		pF

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	See Fig.	V_{DD} (V)	Value Min.	Value Typ.	Value Max.	Unit
CONTROLS								
t_{PSN}	Propagation delay time Strobe to Output (Switch Turn-ON)	$R_L = 1K\Omega$ $C_L = 50pF$ $t_r, t_f = 20ns$	5	14V			400	ns
t_{PZH}	Data-In to Output (Turn-ON to High Level)		6	14V			500	ns
t_{PAN}	Address to Output (Turn-ON to High Level)		7	14V			400	ns
t_{PSF}	Propagation delay time Strobe to Output (Switch Turn-OFF)		5	14V			300	ns
t_{PZL}	Data-In to Output (Turn-ON to Low Level)		6	14V			500	ns
t_{PAF}	Address to Output (Turn-OFF)		7	14V			300	ns
t_{SS}	Set-Up time Data-In to Strobe		5	14V	120			ns
t_{SH}	Hold time Data-In to Strobe		5	14V	200			ns
t_{AS}	Set-Up time Data-in to Address		7	14V	160			ns
t_{AH}	Hold time Data-In to Address		7	14V	100			ns
f_ϕ	Switching frequency			14V		1		MHz
t_W	Strobe Pulse Width			14V	100			ns
	Control crosstalk Data-In, Address, or Strobe to Output	Square wave input $t_r, t_f = 20ns$ $V_{IN} = 3V$ $R_L = 10K\Omega$	8	14V		75		mV
t_W	Reset Pulse Width	$R_L = 1K\Omega$ $C_L = 50pF$ $t_r, t_f = 20ns$	9	14V	100			ns
t_{PHZ}	Reset Turn-OFF Delay		9	14V			260	ns

TEST CIRCUITS

Fig. 1 - R_{ON} measurement

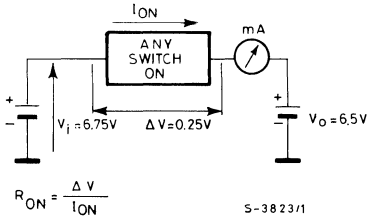


Fig. 2 - Propagation delay time and waveforms (signal input to signal output, switch ON)

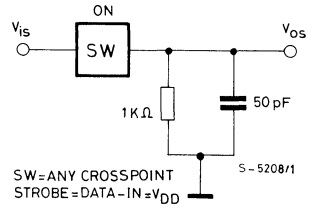
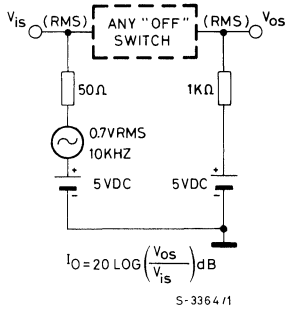


Fig. 3 - Off isolation measurement (Feed through)



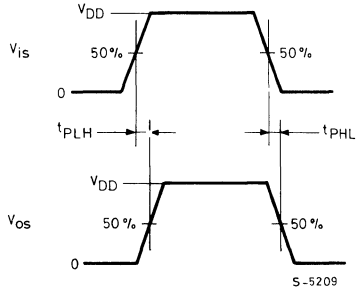


Fig. 4 - Crosstalk measurements

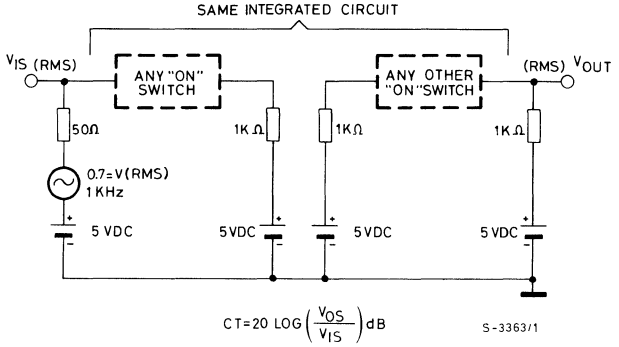


Fig. 5 - Propagation delay time and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF

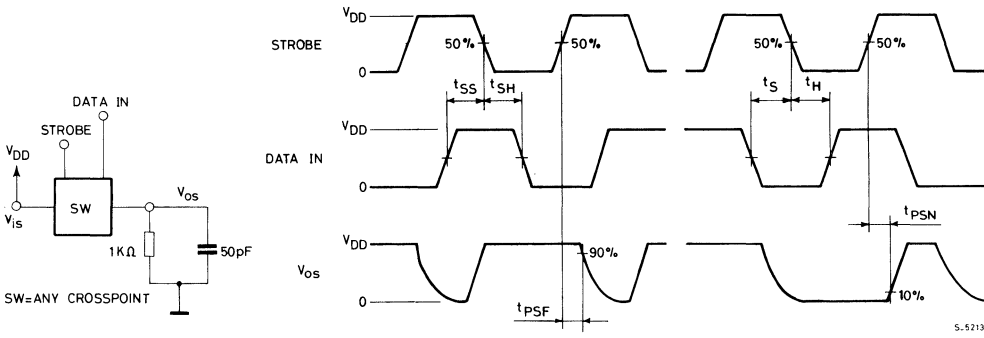


Fig. 6 - Propagation delay time and waveforms (data-in signal output, switch Turn-ON to high or low level)

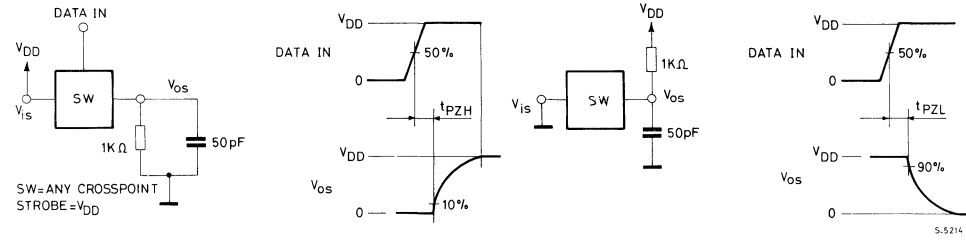


Fig. 7 - Propagation delay time and waveforms (address to signal output switch Turn-ON or Turn-OFF)

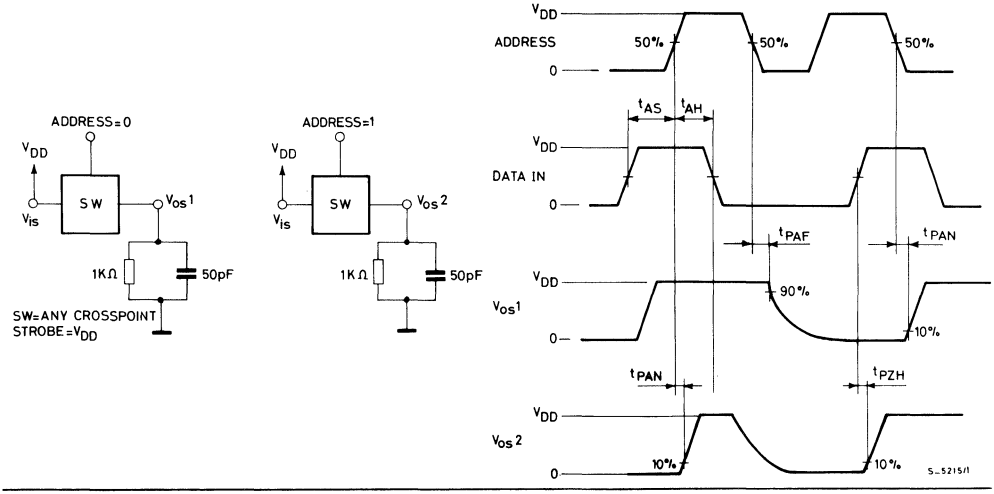


Fig. 8 - Waveforms for crosstalk (control input to signal output)

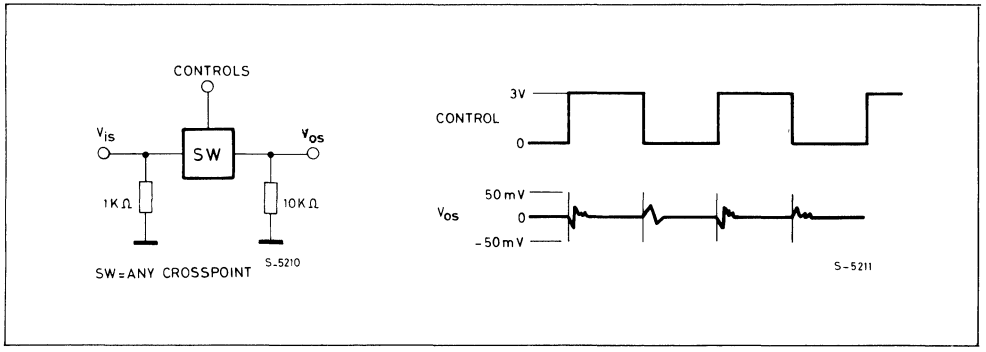
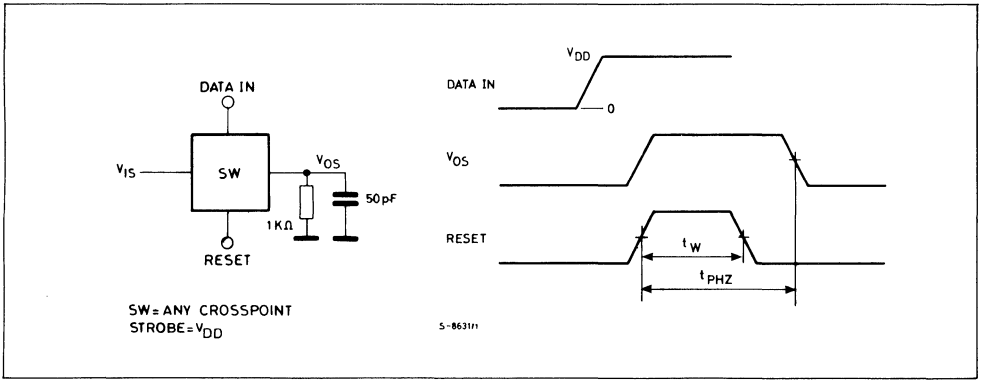
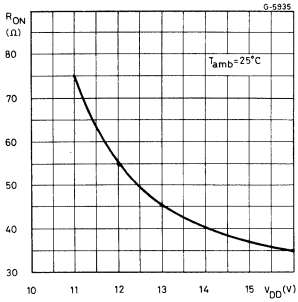


Fig. 9 - Propagation delay time and waveforms (Reset to Output Delay)

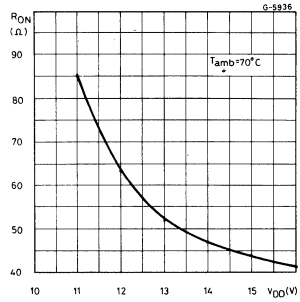


NOTE: Data latch can be performed either by the strobe falling edge a by the address change (with strobe at high level). Advised operation is to move data/address with strobe input at 0, then latching with a strobe pulse.

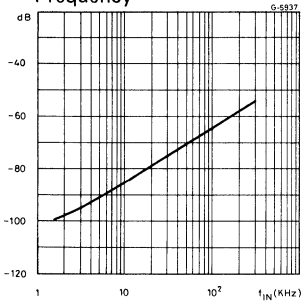
Typical ON Resistance vs. V_{DD}



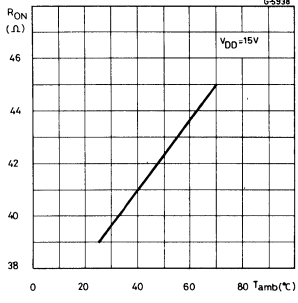
Typical ON Resistance vs. V_{DD}



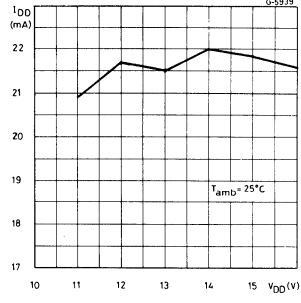
Typical Crosstalk between two CROSS-POINT vs. Input Frequency



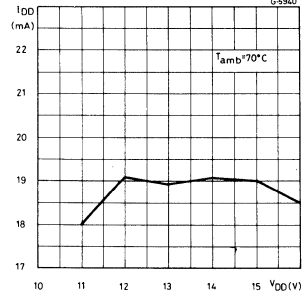
Typical ON Resistance vs. Temperature



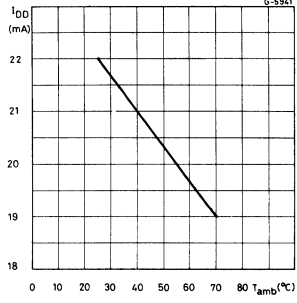
Typical Maximum I_{DD} vs. V_{DD}



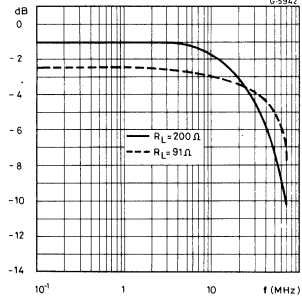
Typical Maximum I_{DD} vs. V_{DD}



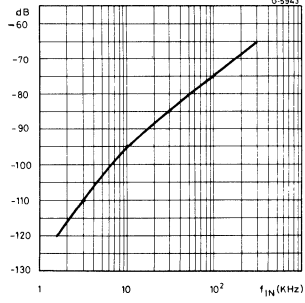
Typical Maximum I_{DD} vs. Temperature



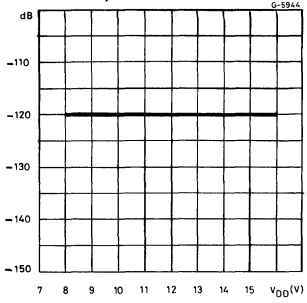
BANDWIDTH Insertion Loss vs. Frequency



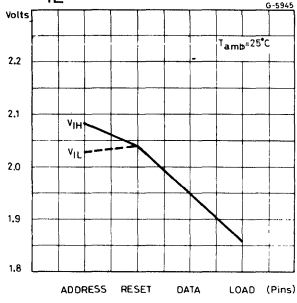
Typical Crosstalk Switches vs. Signal Frequency



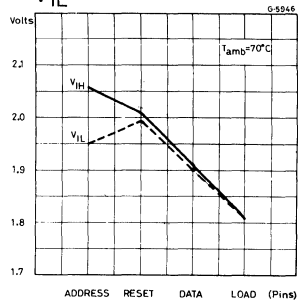
Crosstalk vs. Power Supply at Every Switch



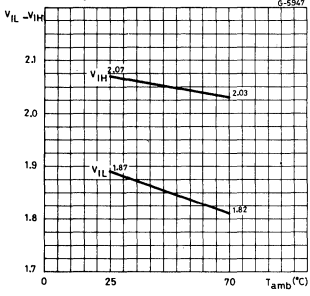
Pin Dependence V_{IH} and V_{IL}



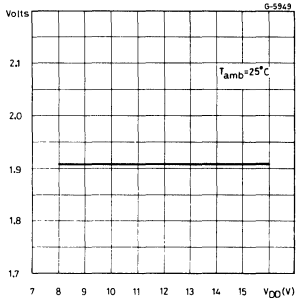
Pin Dependance V_{IH} and V_{IL}



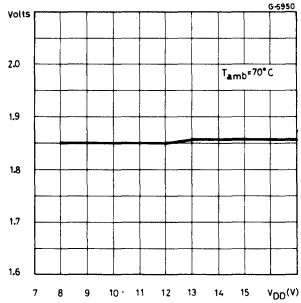
Typycal V_{IL} and V_{IH} vs. Temperature



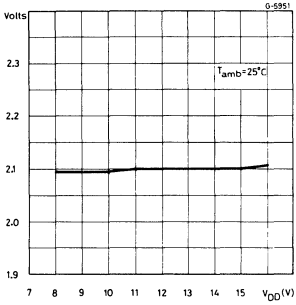
Typical V_{IL} vs. V_{DD}



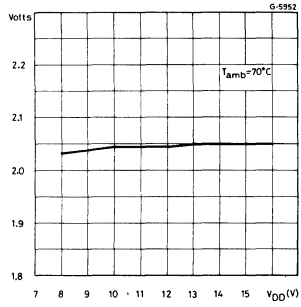
Typical V_{IL} vs. V_{DD}



Typical V_{IH} vs. V_{DD}



Typical V_{IH} vs. V_{DD}

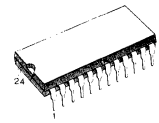


M116

ADVANCE DATA

PCM CONFERENCE CALL AND ATTENUATION / NOISE SUPPRESSION CIRCUIT

- 32 MAXIMUM CONFERENCED CHANNELS IN ANY COMBINATION FROM 10 CONFERENCES OF 3 CHANNELS TO 1 CONFERENCE OF 32 CHANNELS
- 3 TO 32 SERIAL CHANNELS PER FRAME (CONTROLLED BY $\overline{\text{SYNC}}$ SIGNAL PERIOD)
- TWO OPERATION MODES AVAILABLE (CONFERENCE AND TRANSPARENT MODES)
- TYPICAL BIT RATES: 1536/1544/2048 Kbit/s
- COMPATIBLE WITH ALL KINDS OF PCM BYTE FORMAT
- MU AND A LAWS AVAILABLE (PIN PROGRAMMABLE)
- EQUAL PRIORITY TO EVERY CHANNEL
- ONE FRAME (AND ONE CHANNEL) DELAY FROM SENDING TO RECEIVING CHANNELS
- OVERFLOW INFORMATION FOR EACH CONFERENCE SENT OUT BY PINS $\overline{\text{OS}}$ (OVERFLOW SIGNALLING) AND ON DATABUS ON MPU REQUEST
- TONE OUTPUT FOR MASKABLE CONFERENCED CHANNELS. THE DURATION AND FREQUENCY ARE CONTROLLED BY EXTERNAL PINS (TD AND TF)
- INSTRUCTION SET COMPATIBLE WITH THE SGS M088
- PROGRAMMABLE ATTENUATION (0/3/6dB) ON EACH INPUT CHANNEL (BOTH IN CONFERENCE OR TRANSPARENT MODE)
- PROGRAMMABLE NOISE SUPPRESSION FOR EACH OUTPUT CHANNEL ACTING ON FOUR DIFFERENT LEVELS.
- 5V POWER SUPPLY
- MOS AND TTL COMPATIBLE INPUT/OUTPUT LEVELS
- MAIN INSTRUCTIONS CONTROLLED BY THE MICROPROCESSOR INTERFACE:
  - Channel connection to a conference
  - Channel attenuation and/or noise suppression in transparent mode
  - Channel disconnection from both conference and transparent modes
  - Overflow status
  - Operating mode
  - Channel status



B
DIP-24 Plastic

ORDERING NUMBER: M116 B1

DESCRIPTION

The M116 is a product specifically designed for applications in connection with PCM digital exchanges. It is able to handle up to 32 channels in any conference combination, from 3 people (max number of conferences is 10) to 32 people (only one conference).

The parties to be conferenced must previously be allocated through the Digital Switching Matrix (M088) in a single serial wire at the M116 PCM input (IN PCM pin).

Each channel is converted inside the chip from PCM law to linear law (14 bits). Then it is added to the sum of its conference, from which was previously subtracted its information from the previous frame. In this way a new sum signal is generated.

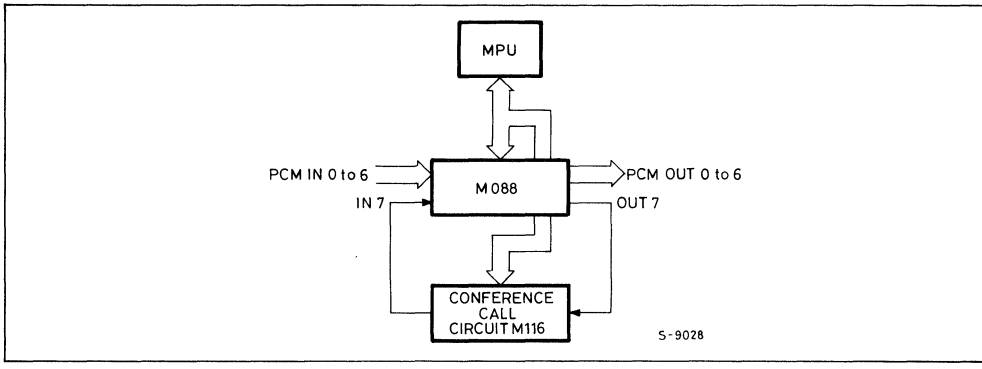
The channel output signal will contain the information of all the other channels in its conference except its own.

After the PCM encoding, the data is serialized by the M116 in the same sequence as the PCM input frame, with one frame (plus one channel) delay and will be reallocated by the DSM (M088/ at the final channel and bus position.

A programmable attenuation as well as a programmable noise suppression threshold can be inserted in any channels connected in conference mode or in transparent mode.

M116 is realized with SGS N-Channel technology and packaged in a 24 pin DIL package.

Fig. 1 - PCM Conference Call Insertion Scheme

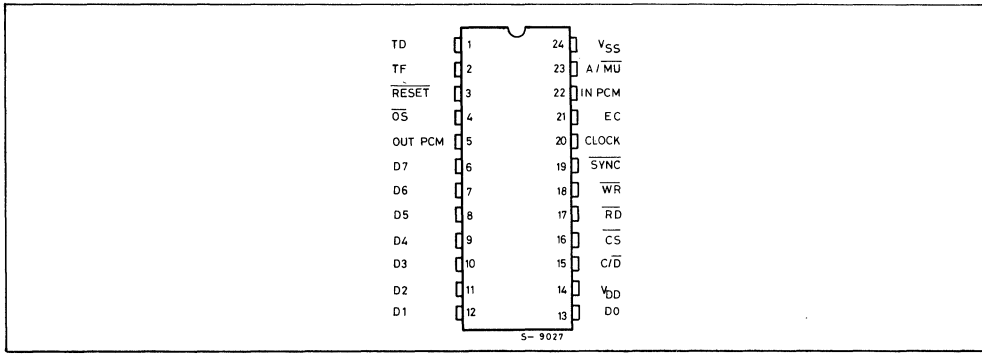


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7	V
V_I	Input Voltage	-0.3 to 7	V
V_O	Off State Output Voltage	7	V
P_{tot}	Total Package Power Dissipation	1	W
T_{op}	Operating Temperature	-0 to 70	°C
T_{stg}	Storage Temperature	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



PIN DESCRIPTION

TD (Pin 1)
Tone Duration input pin. When TD = 1, a PCM coded tone is sent out to all channels of the enabled conferences instead of PCM data. TD is latched by the SYNC signal so that all channels have the same tone during the same number of frame. TD = 0 for normal operation.

TF (Pin 2)
Tone Frequency input pin. When TF = 1, the tone's amplitude is high. When TF = 0, the tone's amplitude is low. TF is latched by the SYNC signal so that all channels have the same tone frequency during the same number of frame. The PCM coded tone levels correspond to the 1/10 of the full scale.

$\overline{\text{RESET}}$ (Pin 3)
Master reset input pin. Reset must be used at the very beginning after power up to initialize the device or when switching from A Law to Mu Law. The internal initialization routine takes two time frames starting from the rising edge of $\overline{\text{RESET}}$. During this initialization time, all databus and PCM output are pulled to a high impedance state.

$\overline{\text{OS}}$ (Pin 4)
Overflow Signalling output pin. When $\overline{\text{OS}}$ = 0 one conference is in overflow. This signal is delayed a little over half time slot with respect to the input channel involved in the conference in overflow, see Fig. 9. Ex: if input channel 3 is one of the parties of one conference in overflow, OS = 0 during the second half of the time slot corresponding to input channel 4.

OUT PCM (Pin 5)
PCM output pin. The bit rate is 2048 Kbit/s max. The sign bit is the first bit of the serial sequence. The output buffer is open drain to allow for multiple connections.

D0 to **D7** (Pins 6 through 13)
Bidirectional Data bus pins. Data and instructions are transferred to or from the microprocessor. D0 is the Least Significant Bit. The bus is tristate when RESET is low and/or CS is high.

C/$\overline{\text{D}}$ (Pin 15)
Control input pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. In a read operation, the overflow information of the first eigh conferences is selected by C/$\overline{\text{D}}$ = 0, the overflow of the last two conferences and the status by C/$\overline{\text{D}}$ = 1.

$\overline{\text{CS}}$ (Pin 16)
Chip select input pin. When $\overline{\text{CS}}$ = 0, data and instructions can be transferred to or from the microprocessor and when $\overline{\text{CS}}$ = 1 the data bus is in tristate.

$\overline{\text{RD}}$ (Pin 17)
Read control input pin. When $\overline{\text{RD}}$ = 0, read operation is performed. When match conditions for the opcode exist, data is transferred to the microprocessor on the falling edge of $\overline{\text{RD}}$.

$\overline{\text{WR}}$ (Pin 18)
Write control input pin. Instructions and opcode from the microprocessor are latched on the rising edge of $\overline{\text{WR}}$ when match conditions exist.

$\overline{\text{SYNC}}$ (Pin 19)
Synchronization input pin. When $\overline{\text{SYNC}}$ rises to logic 1, the internal counter is reset so that a new frame can start. The frame format can vary from three (three is the minimum number of parties required to form a conference) to thirty two and this number is selected by $\overline{\text{SYNC}}$. When PCM frames of 1544 Kbit/s are used, the rise edge of the $\overline{\text{SYNC}}$ signal must correspond to the Extra bit (193th). In the other case it must correspond to the first bit of the first channel.

CLOCK (Pin 20)
Master clock input pin. Max frequency is 4096KHz.

EC (Pin 21)
External clock output pin. This pin provides the master clock for the DSM (M088/M044). Normally is the same signal as applied to CLOCK input (pin 20). When you select, by Instruction 5, Extra bit operating mode, the first two period of the master clock are cancelled, see fig. 8, in order to allow the operation of the M116 and DSM with PCM frame with Extra bit (ex. 193 bit/frame with PCM I/O of 1544 Kbit/s).

PIN DESCRIPTION (continued)

IN PCM (Pin 22)
PCM input pin. The max bit rate is 2048 Kbit/s. The first bit of the first channel is found with the rising edge of the SYNC signal if operating mode with Extra bit is not inserted. The Extra bit is found with the rising edge of the SYNC signal if operating mode with Extra bit is inserted.

A/$\overline{MU}$ (Pin 23)
A Law or MU Law select pin. When A/$\overline{MU}$ = 1. A Law is selected. When A/$\overline{MU}$ = 0, MU Law is selected. The law selection must be done before initializing the device using the $\overline{RESET}$ pin.

Fig. 2 - Insertion scheme of M116 in a 448x448 Non-Blocking Digital Switching Matrix

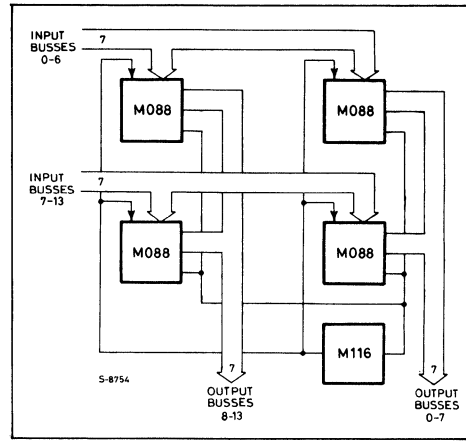
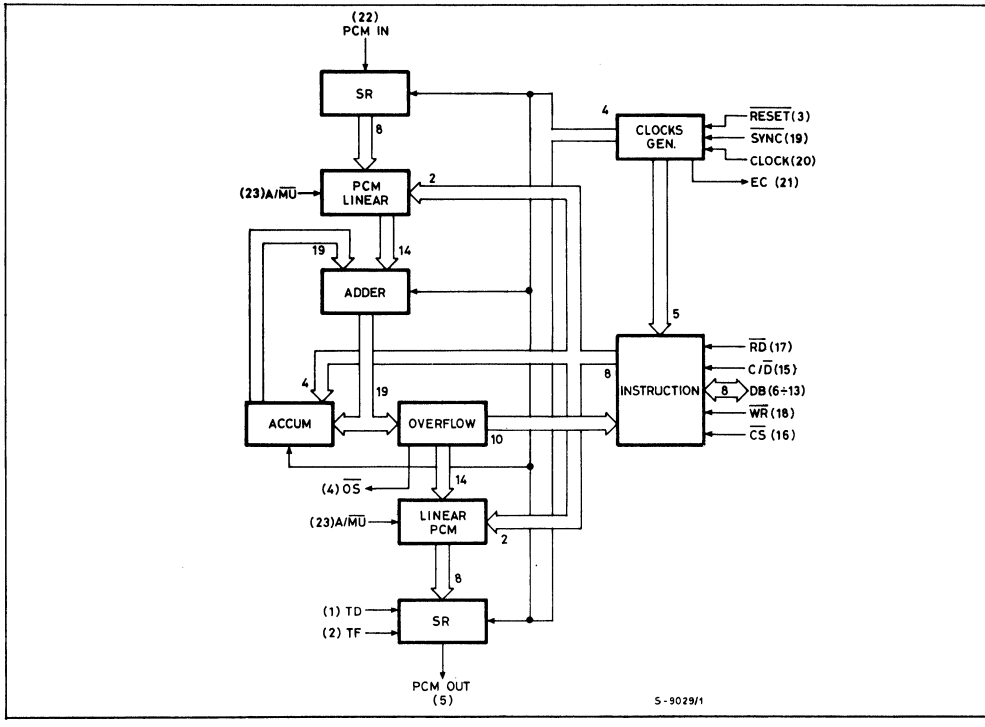


Fig. 3 - Block Diagram



CIRCUIT DESCRIPTION

Through a protocol, the MPU sends the M116 connecting information for each party: the conference number, the conference start bit, the tone insertion enable bit, the number, the attenuation and the noise suppression value for that party.

When a party has to be disconnected the information needed is the disconnection code together with the channel to be disconnected.

The information of channel-N, frame M is added during the first half of channel-N+1, frame M and subtracted during the second half of channel N-1 frame M+1.

After the Linear to PCM conversion, the subtraction result goes to the parallel-in serial-out Shift Register appearing at the output with one frame plus one channel delay with respect to the corresponding sending information of the specific party.

When many channel are to be conferenced, an attenuation can be desired for each specific party and this is obtained from the PCM to Linear conversion ROM.

If the sum of the channels involved in one conference exceeds the full scale value a saturation appears and the device M116 can signal this overflow condition.

The overflow information, sent out to the databus on MPU request, tells specifically which conference is in overflow at the moment requested.

The number of the channel creating the overflow or in the conference already in overflow, can also be extracted from the $\overline{OS}$ pin, correlating this signal with the $\overline{SYNC}$ signal.

The $\overline{OS}$ signal is low during the second half of a generical input channel slot time if the previous input channel is in overflow, see Fig. 9.

This information can be used in the selection of the attenuation value, and the channel to be attenuated.

If noise suppression is desired, four thresholds are available.

When you insert in a channel this function, all the PCM output bytes which are related to this channel and which are at a level less than the selected threshold, are converted into PCM bytes corresponding to the minimum level.

The four thresholds available correspond to the first, the fifth, the ninth and the sixteenth step of the first segment.

These thresholds correspond respectively to 1/4096, 5/4096, 9/4096, 16/4096 respect to the full scale if A-law is selected and to 1/8159, 5/8159, 9/8159, 16/8159 respect to the full scale if MU-law is selected.

The instruction 5 (operating mode) allows the device M116 to be compatible with any kind of PCM byte format, see Table 1, and to work also with PCM frames with Extra bit (ex. 193 bit/frame at 1544 Kbit/s).

The EC pin (External Clock) provides the output clock signal to be applied to the DSM (M088/M044).

This signal is usually the same as the one applied to the input CLOCK pin, only with a little delay (40ns typ.).

When you select, by instructions 5, operating mode with Extra bit, the output clock signal at pin EC has two periods "frozen" in order to allow the DSM (M088/M044) to work also with this kind of PCM frame, see Fig. 8.

The M116 can also operate in transparent mode.

In this case a channel of PCM information can be sent through the M116 and it will appear at the output after one frame (and one channel) delay.

This is useful for a stand/alone system or if the attenuation and noise suppression features are desired without conference.

A tone can be outputted instead of PCM information by using the two tone programming pins (TD/TF).

This tone is a square wave with the same frequency of the signal applied to pin TF, a level corresponding to 1/10 of the full scale value and it is outputed only when pin TD = 1.

Only channels connected in a conference with insertion tone bit (IT) active will have the PCM coded tone at their output.

This feature allows the system to remind the users that they are in conference, or send information of a new party connection and so on.

The chip select pin ($\overline{CS}$) allows several M116 to be connected in parallel on the same databus and access only a particular one.

For testing and diagnostic purposes, a status instruction has been added that provides (for each channel requested) its conference location, the noise suppression threshold level and the attenuation value. This information will appear on the data-bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.75 to 5.25	V
V_I	Input voltage	0 to 5.25	V
V_O	Off state output voltage	0 to 5.25	V
CLOCK freq.	Input clock frequency	4.096	MHz
SYNC freq.	Input synchronization frequency	8	KHz
T_{op}	Operating temperature	0 to 70	°C

CAPACITANCES (Measurement freq. = 1MHz; T_{op} = 0 to 70°C; unused pins tied to V_{SS})

Parameter		Pins	Min.	Typ.	Max.	Unit
C_I	Input capacitance	1 to 3; 15 to 20; 22 to 23			5	pF
$C_{I/O}$	I/O capacitance	6 to 13			15	pF
C_O	Output capacitance	4, 5, 21			10	pF

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)

All DC characteristica are valid 250μs after V_{CC} and clock have been applied.

Parameter		Pins	Test Conditions	Min.	Typ.	Max	Unit
V_{IL}	Input low level	1 to 3 6 to 13 15 to 20 22 to 23		-0.3		0.8	V
V_{IH}	Input high level	1 to 3 6 to 13 15 to 20 22 to 23		2.0		V_{CC}	V
V_{OL}	Output low level	4, 6 to 13	I_{OL} = 1.8mA			0.4	V
V_{OH}	Output high level	4, 6 to 13	I_{OH} = 250μA	2.4			V
V_{OL}	Output low level	5, 21	I_{OL} = 5.0mA			0.4	V
I_{IL}	Input leakage current	1 to 3 6 to 13 15 to 20 22 to 23	V_{IN} = 0 to V_{CC}			10	μA
I_{OL}	Data bus leakage current	6 to 13	V_{IN} = 0 to V_{CC} $\overline{CS}$ = V_{CC}			± 10	μA
I_{CC}	Supply current	14	Clock freq. = 4.096MHz			100	mA

AC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)

All AC characteristics are valid 250μs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

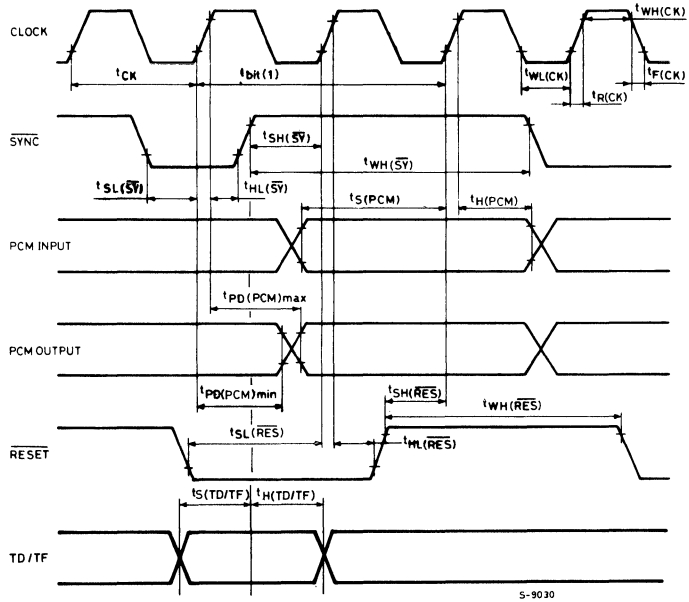
Signal	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock period		230			ns
	t_{WL}	Clock low level width		100			ns
	t_{WH}	Clock high level width		100			ns
	t_R	Rise time				25	ns
	t_F	Fall time				25	ns
$\overline{SYNC}$	t_{SL}	Low level set-up time		80			ns
	t_{HL}	Low level hold time		40			ns
	t_{SH}	High level set-up time		120			ns
	t_{WH}	High level width	See note 1	t_{CK}			ns
PCM input	t_S	Set-up time		20			ns
	t_H	Hold time		80			ns
PCM Output	$t_{PD\ min}$	Propagation time referred to CK high level	C_L = 50pF R_L = 1KΩ	40		80	ns
	$t_{PD\ max}$	Propagation time referred to CK high level	C_L = 50pF R_L = 1KΩ See note 2	90		130	ns
$\overline{RESET}$	t_{SL}	Low level set-up time		100			ns
	t_{HL}	Low level hold time		50			ns
	t_{SH}	High level set-up time		90			ns
	t_{WH}	High level set-up time		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low level width		150			ns
	t_{WH}	High level width		200			ns
	t_{REP}	Repetition interval between active pulses		500			ns
	t_{SH}	High level set-up time to active read strobe		0			ns
	t_{HH}	High level hold time from active read strobe		20			ns
	t_R	Rise time				60	ns
	t_F	Fall time				60	ns
$\overline{RD}$	t_{WL}	Low level width		180			ns
	t_{WH}	High level width		200			ns
	t_{REP}	Reception interval between active pulses		500			ns
	t_{SH}	High level set-up time to active write strobe		0			ns
	t_{HH}	High level hold time strobe		20			ns
	t_R	Rise time				60	ns
	t_F	Fall time				60	ns

NOTE: 1. With Extra Bit Operating Mode insert this time become 3 t_{CK}.
2. With Extra Bit Operating Mode insert these times are 80ns longer.

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$\overline{CS}$	t_{SL} ($\overline{CS}$-$\overline{WR}$)	Low level set-up time to $\overline{WR}$ falling edge	Active case	0			ns
	t_{HL} ($\overline{CS}$-$\overline{WR}$)	Low level hold time from $\overline{WR}$ rising edge	Active case	0			ns
	t_{SH} ($\overline{CS}$-$\overline{WR}$)	High level set-up time to $\overline{WR}$ falling edge	Inactive case	0			ns
	t_{HH} ($\overline{CS}$-$\overline{WR}$)	High level hold time from $\overline{WR}$ rising edge	Inactive case	0			ns
	t_{SL} (CS-RD)	Low level set-up time to $\overline{RD}$ falling edge	Active case	0			ns
	t_{HL} ($\overline{CS}$-$\overline{RD}$)	Low level hold time from $\overline{RD}$ rising edge	Active case	0			ns
	t_{SH} ($\overline{CS}$-$\overline{RD}$)	High level set-up time $\overline{RD}$ falling edge	Inactive case	0			ns
	t_{HH} ($\overline{CS}$-$\overline{RD}$)	High level hold time from $\overline{RD}$ rising edge	Inactive case	0			ns
C/$\overline{D}$	t_S (C/$\overline{D}$-$\overline{WR}$)	Set-up time to write strobe end		130			ns
	t_H (C/$\overline{D}$-$\overline{WR}$)	Hold time from write strobe end		25			ns
	t_S (C/$\overline{D}$-$\overline{RD}$)	Set-up time to read strobe start		20			ns
	t_H (C/$\overline{D}$-$\overline{RD}$)	Hold time from read strobe end		25			ns
$\overline{OS}$	t_{PD} ($\overline{OS}$)	Propagation time from rising edge of CK	C_L = 50pF			100	ns
EC	t_{PD} (EC)	Propagation time referred to CK edges	C_L = 50pF			80	ns
TD/TF	t_S	Set-up		80			ns
	t_H	Hold time		40			ns
D0 to D7 (interface bus)	t_S (BUS-$\overline{WR}$)	Input set-up time to write strobe end		130			ns
	t_H (BUS-$\overline{WR}$)	Input hold time from write strobe end		25			ns
	t_{PD} (BUS)	Propagation time from (active) falling edge of read strobe	C_L = 200pF			120	ns
	t_{HZ} (BUS)	Propagation time from (active) rising edge of read strobe to high impedance state				80	ns

Fig. 4 - SYNC, PCM I/O, RESET, TD/TF Timings



(1) t_{bit} corresponds to bit 0, channel 0 or Extra Bit

Fig. 5 - WRITE Operating Timing

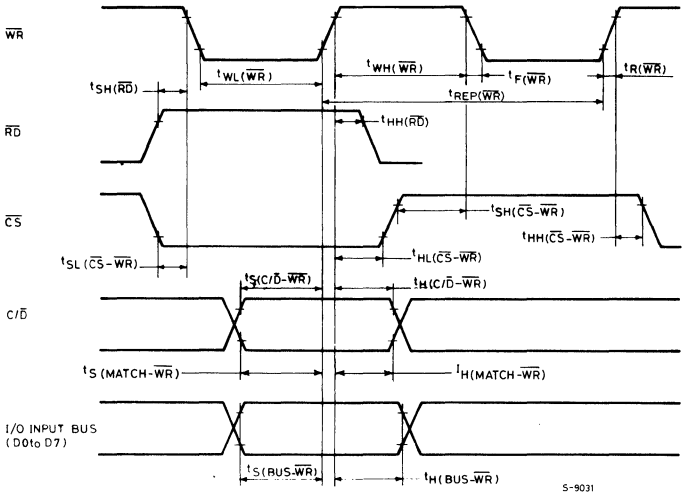


Fig. 6 - READ Operating Timing

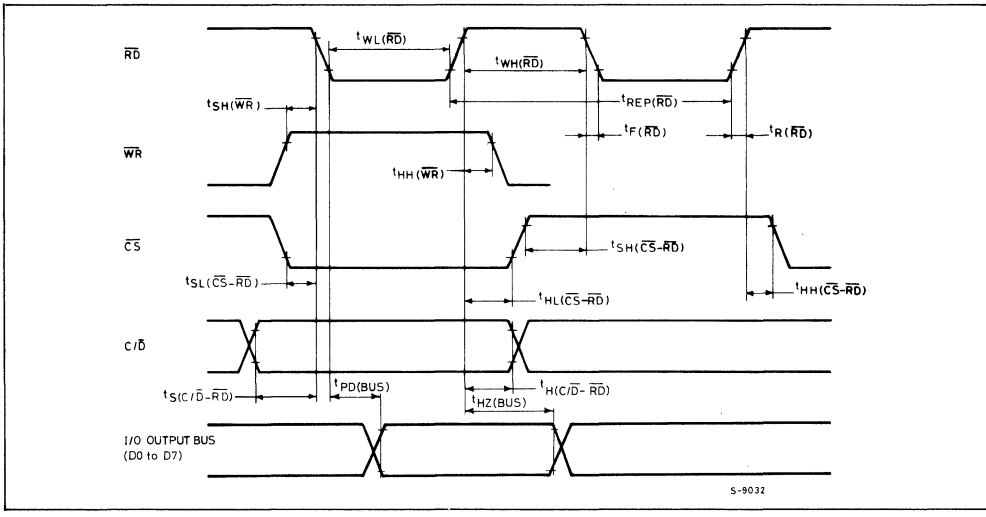


Fig. 7 - EC (External Clock) and $\overline{OS}$ (Overflow Signalling) Timings

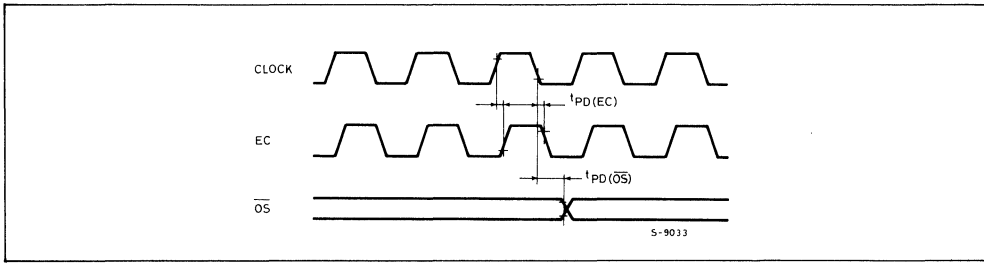


Fig. 8 - EC Timing with Extra Bit Operating Mode Insert

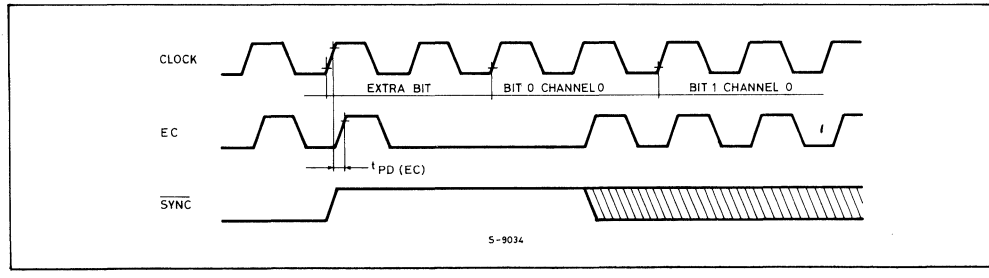


Fig. 9 - $\overline{OS}$ Timing with input PCM channel (u + 1) in overflow

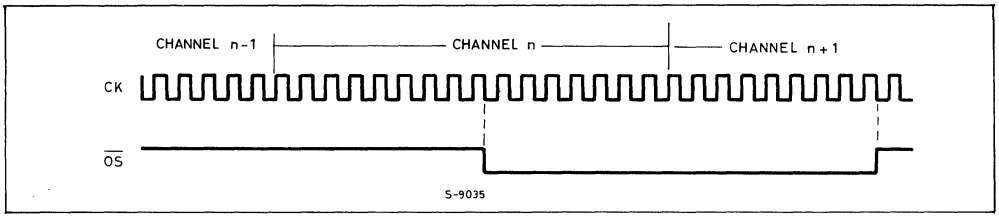
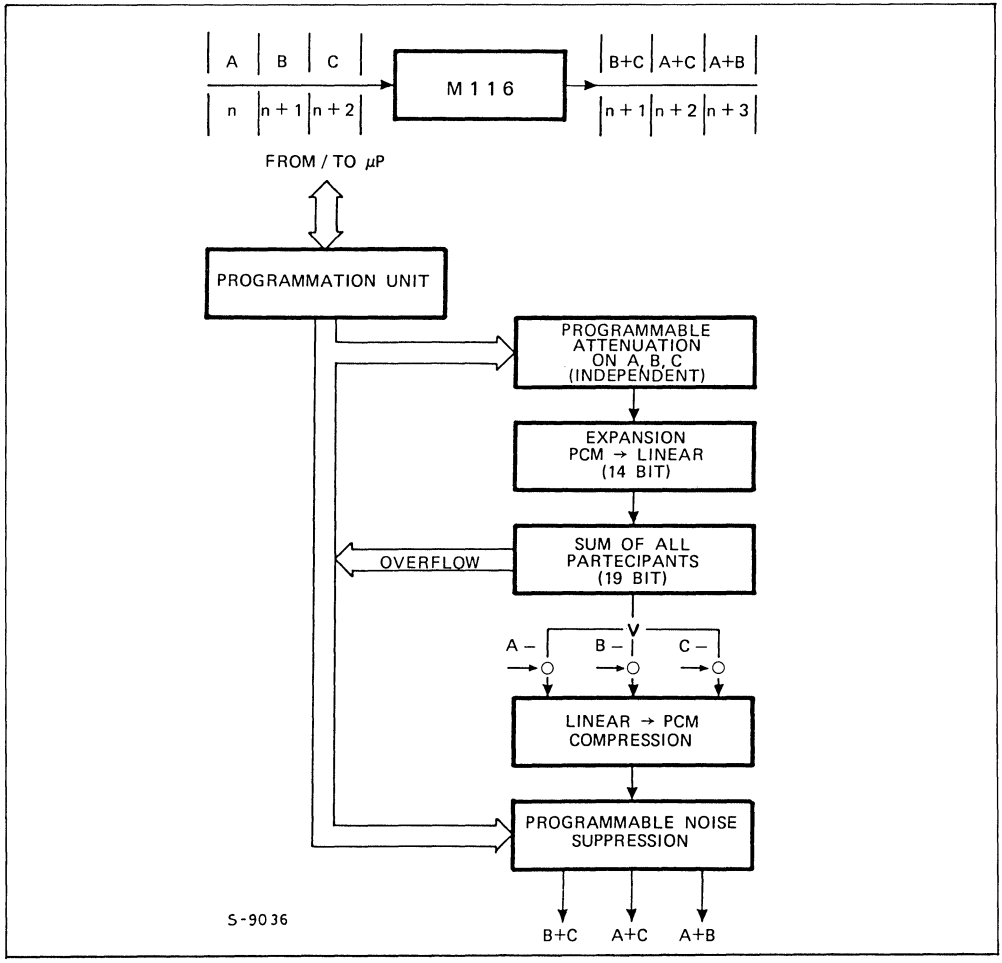


Fig. 10 - Simplified Operating Procedures



INSTRUCTION SET

• INSTRUCTION 1: CHANNEL CONNECTION IN CONFERENCE MODE

Three byte are needed:

1) the first byte contains the conference number (bits D0-D3) and the Start bit S (bit D4). When S = 1, all registers of the conference will be cleared. S = 1 is only required in the instruction 1 set of the first channel connected to a new conference.
2) The second byte contains in the bits (D0-D4) the number of the channel to be connected and the Insert Tone Enable bit IT (D5). When bit IT = 1 all the channels belonging to that conference are enabled using insert tone function if it's active (TD = 1)
3) The third byte contains information about the attenuation level and the noise suppression level to be applied to that channel and the opcode (0111).

INSTRUCTION 1 FORMAT

CONTROL SIGNAL			
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$
0	1	0	0
0	1	0	0
0	0	1	0

DATA BUS							
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	S	P3	P2	P1	P0
X	X	IT	C4	C3	C2	C1	C0
A1	A0	T1	T0	0	1	1	1

S : Conference Start bit
P3 - P0 : Conference number (1-10)
IT : Insertion Tone function enable (IT=1)
C4 - C0 : Channel number (0-31)
A1 - A0 : Channel attenuation
00 = -0dB
01 = -3dB
10 = -6dB

T1 - T0 : Noise suppression decision value (referred to PCM coding, 128+128 steps)
00 = no noise suppression
01 = fifth step, first segment
10 = ninth step, first segment
11 = sixteen step, first segment

• INSTRUCTION 2: CHANNEL CONNECTION IN TRANSPARENT MODE

Two bytes are needed:

1) the first byte contains the number of the channel.
2) The second byte contains information about the attenuation level and the noise suppression level to be applied to that channel and the opcode (0011).

PCM data of this channel is not added to any conference and it is transferred to the PCM output. It is not affected by the tone control pins.

INSTRUCTION 2 FORMAT

CONTROL SIGNAL			
$\overline{CS}$	$\overline{AD}$	C/$\overline{D}$	$\overline{WR}$
0	1	0	0
0	1	1	0

DATA BUS							
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	C4	C3	C2	C1	C0
A1	A0	T1	T0	0	0	1	1

INSTRUCTION SECTION (continued)

• INSTRUCTION 3: CHANNEL DISCONNECTION

Two bytes are needed:

1) the first word contains the number of the channel to be disconnected.

2) The second word contains the opcode (1111).

One time frame must exist between disconnection and connection of the same channel.

INSTRUCTION 3 FORMAT

CONTROL SIGNAL			
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$
0	1	0	0
0	1	1	0

DATA BUS							
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	C4	C3	C2	C1	C0
X	X	X	X	1	1	1	1

• INSTRUCTION 4: OVERFLOW INFORMATION

Two bytes are needed to know the status of all 10 conferences: C/$\overline{D}$ = 0 reads the first byte (first 8 conferences) and C/$\overline{D}$ = 1 reads the second byte (the last 2 conferences). A conference is in overflow when the corresponding bit is high.

INSTRUCTION 4 FORMAT

CONTROL SIGNAL			
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$
0	0	0	1
0	0	1	1

DATA BUS							
D7	D6	D5	D4	D3	D2	D1	D0
CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1
X	X	X	X	X	X	CF10	CF9

CF10 - CF1 : Conference in overflow when high

nb: as long as $\overline{RD}$ remains low, the overflow status of the conference selected by C/$\overline{D}$ can be monitored in real time.

• INSTRUCTION 5: OPERATING MODE

The single byte needed contains the Extra bit E (D6), the format bits F1-F0 (D5-D4) and the opcode (0101).

The E bit must be E = 1 when the PCM frame contains a number of bit multiple of eight plus one bit (ex. PCM frame at 1544 Kbit/s). Normally E = 0.

The bits F1-F0 select the kinds of PCM format bytes according Table 1. After Reset the default values correspond to F1 = 0, F0 = if 1 A-law is selected and F1 = 1, F0 = 1 if Mu-law is selected.

All channels must be disconnected when the Operating Mode Instruction is sent. They must remain disconnected for at least two time frames after the instruction was sent.

We recommende to use this instruction right after the RESET (see pin $\overline{RESET}$ description).

INSTRUCTION SECTION (continued)

INSTRUCTION 5 FORMAT

CONTROL SIGNAL			
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$
0	1	1	0

DATA BUS							
D7	D6	D5	D4	D3	D2	D1	D0
X	E	F1	F0	0	1	0	1

E : Extra bit insertion (active when E=1)
F1 - F0 : PCM byte Format selection (see also Table 1)
00 = no bit inverted
01 = even bit (B0-B2-B4-B6) inverted
10 = odd bit (B1-B3-B5) inverted
11 = all bit (B0-B1-B2-B3-B4-B5-B6) inverted

• INSTRUCTION 6: STATUS

Three bytes are needed :

1) the first byte contains the number of the channel;
2) the second byte contains the opcode (0110);
3) by a reading cycle you extract from the third byte the information about the operating mode of the channel (no connection or transparent mode or number of the conference, bits D4-D7); the attenuation (D2-D3) and noise suppression values (D0-D1) eventually inserted.

INSTRUCTION 6 FORMAT

CONTROL SIGNAL			
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$
0	1	0	0
0	1	1	0
0	0	1	1

DATA BUS							
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	C4	C3	C2	C1	C0
X	X	X	X	0	1	1	0
P3	P2	P1	P0	A1	A0	T1	T2

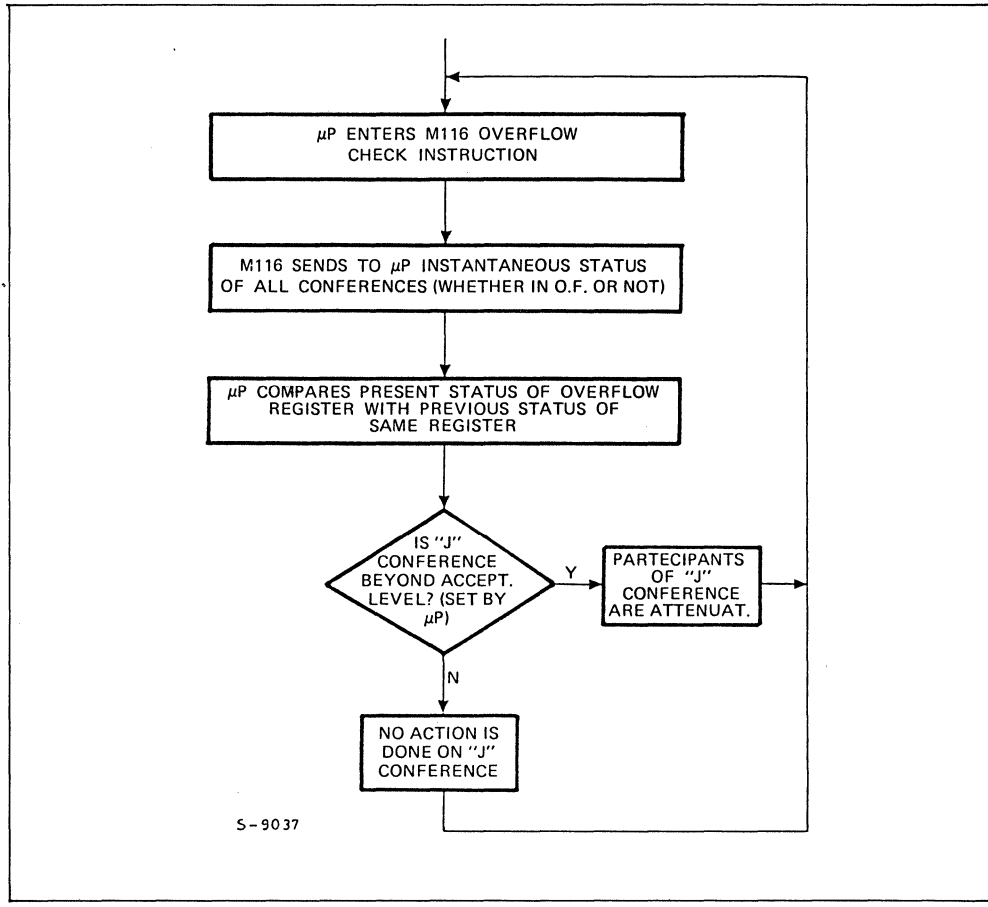
P3 - P0 : channel mode operation information
0000 = no connection
1111 = transparent mode
1010 - 0001 = conference mode, P3-P0 give the number of the conference.

nb: the Instruction 6 enables the data bus to read the status until reset by C/$\overline{D}$ = 0 and $\overline{WR}$ = 1.

Table 1: PCM Byte Format. B7 (sign-bit) is the MSB and B0 is the LSB. F1-F0 corresponds to D5-D4 in the byte of the Operating Mode Instruction (Instruction 5).

F1	F0		B7	B6	B5	B4	B3	B2	B1	B0
0	0	+ FULL SCALE	1	1	1	1	1	1	1	1
		MIN LEVELS	1	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	0
		− FULL SCALE	0	1	1	1	1	1	1	1
0	1	+ FULL SCALE	1	0	1	0	1	0	1	0
		MIN LEVELS	1	1	0	1	0	1	0	1
			0	1	0	1	0	1	0	1
		− FULL SCALE	0	0	1	0	1	0	1	0
1	0	+ FULL SCALE	1	1	0	1	0	1	0	1
		MIN LEVELS	1	0	1	0	1	0	1	0
			0	0	1	0	1	0	1	0
		− FULL SCALE	0	1	0	1	0	1	0	1
1	1	+ FULL SCALE	1	0	0	0	0	0	0	0
		MIN LEVELS	1	1	1	1	1	1	1	1
			0	1	1	1	1	1	1	1
		− FULL SCALE	0	0	0	0	0	0	0	0

Fig. 11 - Overflow Control with μP interactive procedure

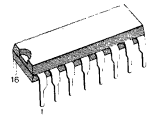


M761E
M761EA

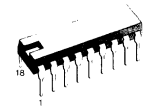
PRELIMINARY DATA

DUAL TONE MULTIFREQUENCY GENERATOR

- 2.4 TO 5V SUPPLY RANGE
- VERY LOW POWER CONSUMPTION
- INTERNAL PULL-UP OR PULL-DOWN RESISTOR WITH DIODE PROTECTION ON ALL KEYBOARD INPUTS
- ON-CHIP CRYSTAL CONTROLLED OSCILLATOR (f_o = 4.433619MHz) WITH INTEGRATED FEEDBACK RESISTOR AND LOAD CAPACITORS
- LOW HARMONIC DISTORTION ($\leqslant$ 2%)
- FIXED PRE-EMPHASIS ON HIGH-GROUP TONES
- FAST START-UP TIME
- LOW POWER CONSUMPTION IN STAND-BY MODE
- MUTE OUTPUT (M761E ONLY)
- ONE CONTACT PER KEY



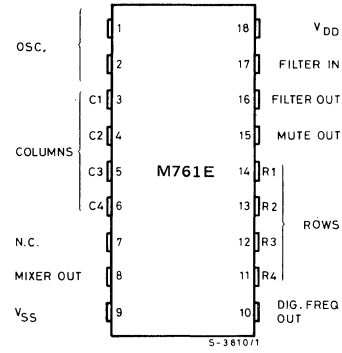
B/F
DIP-16 Plastic and Ceramic

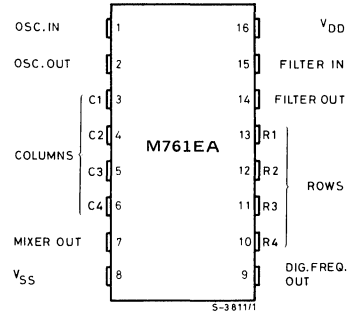


B/F
DIP-18 Plastic and Ceramic

ORDERING NUMBERS: M761EB1
M761EAB1
M761EF1
M761EAF1

PIN CONFIGURATION





DESCRIPTION

The M761E-M761EA provides all the tone frequency pairs required for a DTMF Dialling System. Tones are obtained from an inexpensive TV crystall (f_o = 4,433619MHz) followed by two independent programmable dividers. The dividing ratio is controlled by the selected key. Keyboard format is 4 rows x 4 columns and a key is valid when a column and a row are connected together.

Internal logic prevents the transmission of illegal tones when more than one key is pressed. If no key is selected the oscillator turns off and the linear parts are strobed to decrease the total power consumption.

As any buttom is pressed row and column inputs are scanned internally, to identify the activated ones. Electrically, row and column inputs are activated on high level voltage.

Single tone output cannot be emitted by a "1" an a row or column only. For single tone emission see "Single tone procedure".

A debounce output is available, for M761E only, to indicate that a key has been selected. D/A conversion is accomplished by a capacitive network allowing very low power consumption, very low

M761E
M761EA

DESCRIPTION (continued)

distortion and an exceptional stability of tone level against temperature variations.

The tones are mixed in a resistive network; a unity gain amplifier is provided to realize a two pole active filter with only four external passive components.

SGS has also developed the LS342, DTMF line interface which provides the stabilized supply for the M761E-M761EA from the telephone line and amplifies the output tones to the standardized levels. The M761E can also be interfaced with the LS156 speech circuit with MF interface avoiding the need of the common spring set.

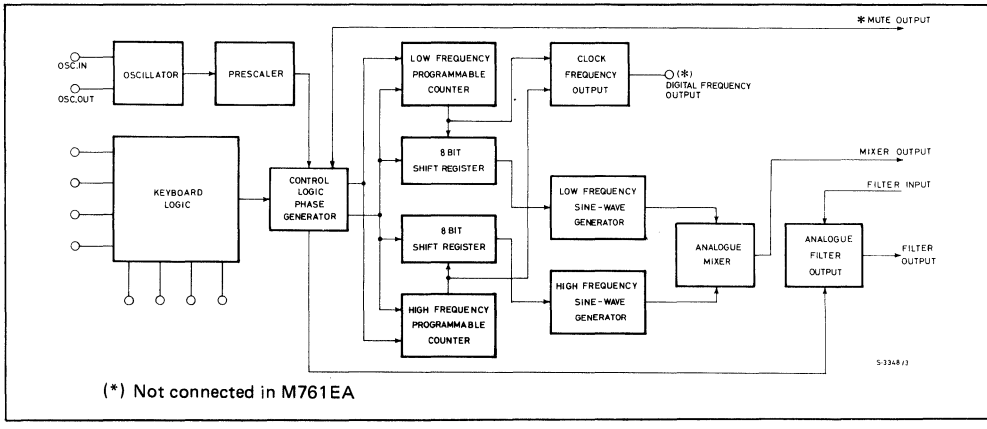
The M761E utilizes low voltage CMOS technology and is available in 18 pin dual in-line plastic ceramic package; the M761EA is available in 16 pin dual in-line package.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to + 5.5	V
V_I	Input voltage	-0.3 to V_{DD} +0.5	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	-25 to +70	°C
T_{stg}	Storage temperature range	-55 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device realibility.

BLOCK DIAGRAM



(*) Not connected in M761EA

ELECTRICAL CHARACTERISTICS (All parameters are tested at $T_{amb} = 25°C$)

	Parameter		Test Conditions (see note 1)		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS								
Supply	V_{DD}	Voltage Supply Voltage			2.4	3	5	V
	I_{DD}	Operating Supply Current	V_{DD} = 2.4V				1.8	mA
	I_{DDO}	Stand-by Supply Current	V_{DDO} = 2.55V				0.3	mA
Row and Column Inputs		Input Voltage Levels						
	V_{IH}	Logical "1"				80% of (V_{DD}-V_{SS})	V_{DD} + 0.3	V
	V_{IL}	Logical "0"				V_{SS} -0.3	20% of (V_{DD}-V_{SS})	V
	C_{IN}	Input Capacitance Any Pin					7.5	pF
Oscillator	I_{IH}	High Level Input Current	V_{DD} = 2.5V	V_{IN} = 2.5V			1	µA
	I_{IL}	Low Level Input Current	V_{DD} = 2.5V	V_{IL} = 0V			1	µA
	I_{OH}	High Level Output	V_{DD} = 2.5V	V_{OH} = 2V	-100	-500		µA
	I_{OL}	Low Level Output Current	V_{DD} = 2.5V	V_{OL} = 0.5V	100	500		µA
Digit. Freq. Outp.	I_{OL}	Low Level Output Current (open drain output)	V_{DD} = 2.5V	V_{OL} = 1V	100			µA
Filter	V_O	Output DC Voltage Without Tones	V_{DD} = 2.5V				200	mV
	V_O	Output DC + AC Voltage With 2 Tones	V_{DD} = 2.5V	(see note 2) (see fig. 1)	0.63	0.84	1.05	V
Mute Output	I_{OH}	Output Drive Current	V_{DD} = 2.5V	V_{OH} = 1.5V	-100			µA
	I_{OL}	Output Sink Current	V_{DD} = 2.5V	V_{OL} = 1V	20			µA
AC CHARACTERISTICS								
Oscillator	R_F	Feedback Oscillator Resistance			4	4.5		MΩ
	C_I	Input Capacitance to V_{DD}				9.5	10.5	pF
	C_O	Output Capacitance to V_{DD}				10.5	11.5	pF
Mixer	Z_{01}	Output Dynamic Impedance with 2 tones	V_{DD} = 2.5V			10		KΩ
Filter	Z_{02}	Output Dynamic Impedance with 2 Tones	V_{DD} = 2.5V			2.5		KΩ
Tone characteristics	$\frac{\Delta F}{F}$	Max. Output Tone Deviration from standard R1 697Hz R2 770Hz R3 852Hz R4 941Hz C1 1209Hz C2 1336Hz C3 1477Hz C4 1633Hz	At crystal frequency f = 4.433619MHz				 +0.5 -0.2 +0.5 -0.6 +0.6 -0.4 -0.3 +1.1	 % % % % % % % %
	V_{LF}	Low Frequency Tones Amplitude at Filter Out	V_{DD} = 2.5V	(see note 3) (see fig. 2)	124		148	mVpp
	V_{HF}	High Frequency Tones Amplitude at Filter Out	V_{DD} = 2.5V	(see note 3) (see fig. 2)	157		187	mVpp

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions (see note 1)	Min.	Typ.	Max.	Unit
Tone characteristics	Pre-emphasis		1.25	2	2.75	dB
	Unwanted Frequency Components at f = 3.4KHz at f = 50KHz				 -33 -80	 dBm dBm
	Total Harminic Distortion for a Single Frequency	V_{DD} = 2.5V			5	%
t_s	Start-up Time	V_{DD} = 2.5V (see fig. 4) (see fig. 5)		3	5	ms
t_r	Supply Voltage Rise Time	V_{DD} = 2.5V			250	ms

Note 1: This device has been designed to be connected to LS342 MF tone dialler line interface, from which it takes a V_{DD} = 2.4V min. therefore many parameters are tested at this value.

Note 2: The value of DC output component at two different conditions of supply voltage, with two tones activated, can be related as follows:

$$V_{DC'} = V_{DC} \frac{V_{DD'}}{V_{DD}}$$

Note 3: The value of AC output components (V_{LF}, V_{HF}) at two different conditions of supply voltages can be related as follows:

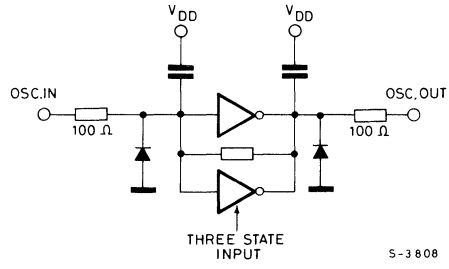
$$V_{LF'} = V_{LF} \frac{V_{DD'}}{V_{DD}} \qquad V_{HF'} = V_{HF} \frac{V_{DD'}}{V_{DD}}$$

The values are measured with two tone at the output.

FUNCTIONAL DESCRIPTION

OSCILLATOR (OSC. IN – OSC. OUT)

The oscillator circuit has been designed to work with a 4.433619MHz crystal ensuring both fast start-up time and low current consumption.
When V_{DD} is applied and a key is activated two inverters are paralleled (see fig. below) to decrease the total r_{ON} resistance.
After oscillations have started one of the two buffers is switched off and the current consumption is reduced to 2/3 of the initial value.
Feedback resistance and load capacitances are integrated on the chip ensuring good temperature performance.
When the device is supplied but no key is activated, the oscillator is in the stand-by mode to minimize power consumption.



FUNCTIONAL DESCRIPTION (continued)

KEYBOARD INPUTS
(C1, C2, C3, C4 – R1, R2, R3, R4)

Each keyboard input has an internal protection circuit; when a button is pressed, the oscillator starts and dynamic scanning of keyboard is realised.

This allows to the detection of which button has been pressed.

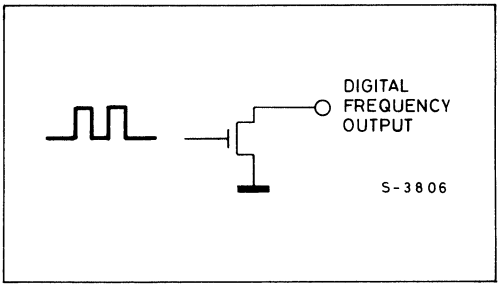
When two or more column or row inputs are activated no tone is generated.

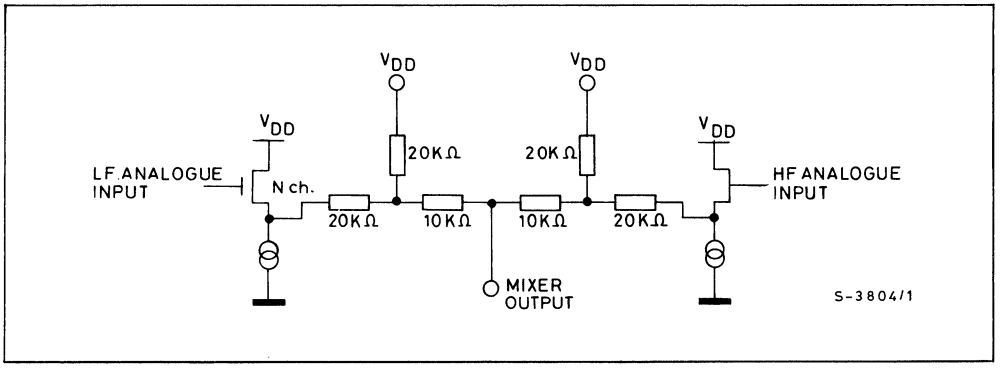
DIGITAL FREQUENCY OUTPUT

This output is intended for testing only; when a single tone is activated, at this output is available a digital signal whose frequency is 16 times the selected output tone frequency. This output is an open collector N-channel transistor.

MIXER OUTPUT

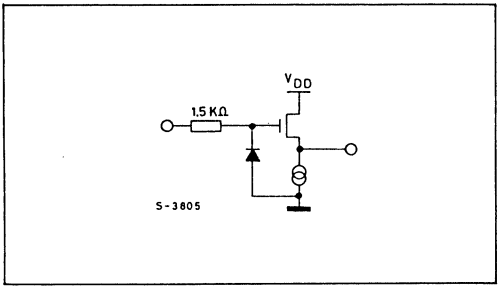
The two reconstructed sine waves are buffered then mixed in a resistive array network that also restores the DC output level.





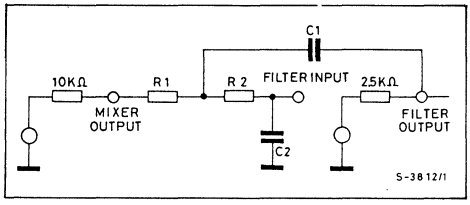
FILTER (Filter Input, Filter Output)

A unity gain amplifier is available to realize a two pole active filter (see fig. below). The output of this amplifier is held low until tones are valid, it than rises to about 0.85V at $V_{DD} = 2.5V$. Tones are superimposed on this DC.
The output DC component is very precise and stable to allow DC coupling with the LS342 DTMF line interface and LS156 speech circuit with MF interface.
The output dynamic impedance of the filter is about 2.5KΩ.



FUNCTIONAL DESCRIPTION (continued)

The following equivalent circuit should be applied during filter design:



It is evident that R1 and R2 should be kept high to avoid undue influence of Mixer and Filter output impedances.

The following values are suggested:

R1 = 430KΩ ± 2%
R2 = 82KΩ ± 2%
C1 = 820pF ± 10%
C2 = 120pF ± 10%

MUTE OUTPUT

Mute output becomes active when a key is activated eliminating keyboard bounces and remains active for all the duration of tone transmission.
If the key is released before the oscillator produces the correct control signals, mute output is disabled.

SINGLE TONE PROCEDURE

This is accomplished through the following steps:

1) Activate simoultaneously 1, A, D inputs, appling logic 1'S. This implies the use of logic level sources. The single contact keyboard does not allow this procedure.
2) The device enters the "test mode" Now any single row or column frequency (or both) can be activated at out put applying logic "1" to correspondant input (inputs).
3) To get out from "test mode" reply 1, A, D activation (or though) power off power on.

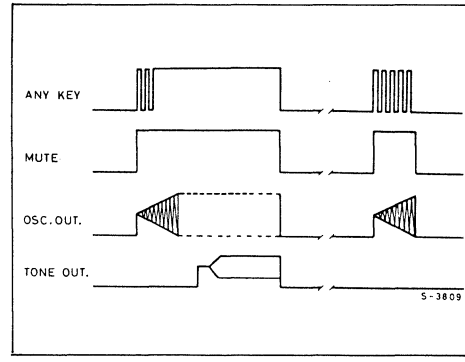
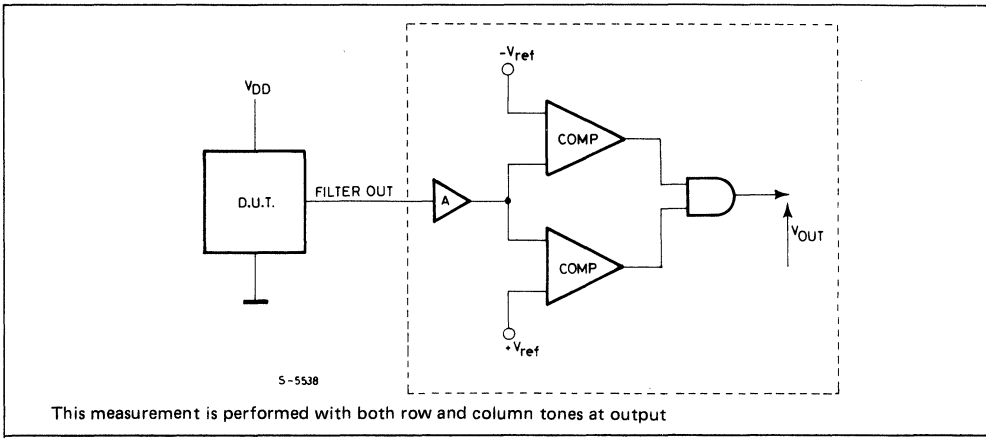


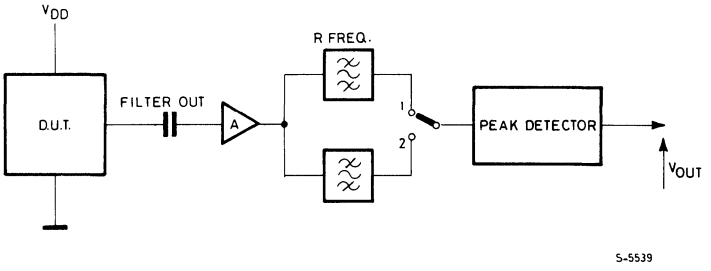
Fig. 1 – DC + AC out level measurement test set



This measurement is performed with both row and column tones at output

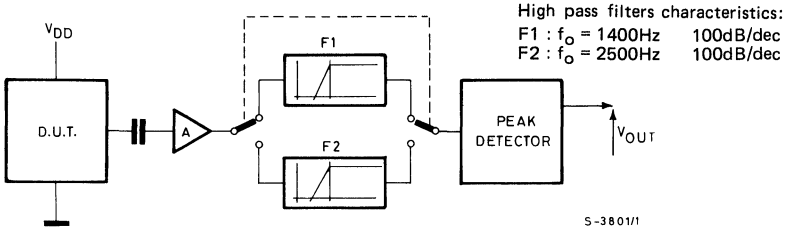
FUNCTIONAL DESCRIPTION (continued)

Fig. 2 – Out tone level measurement test set



This measurement is performed with both row and column tones at output.

Fig. 3 – THD measurement test set



THD measurement is made by sensing the level of harmonic components after suppression of the fundamental. Two different high pass filters are used for low and high frequency tones.

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 – Start-up time measurement test set

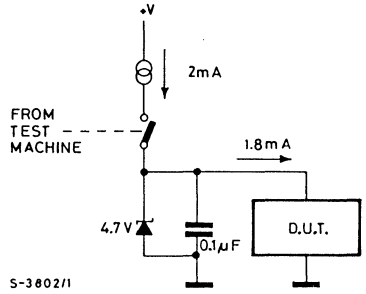
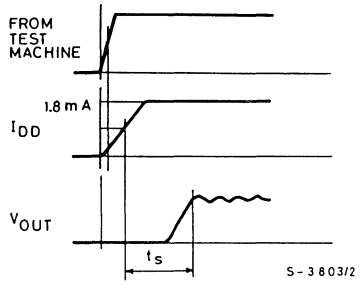
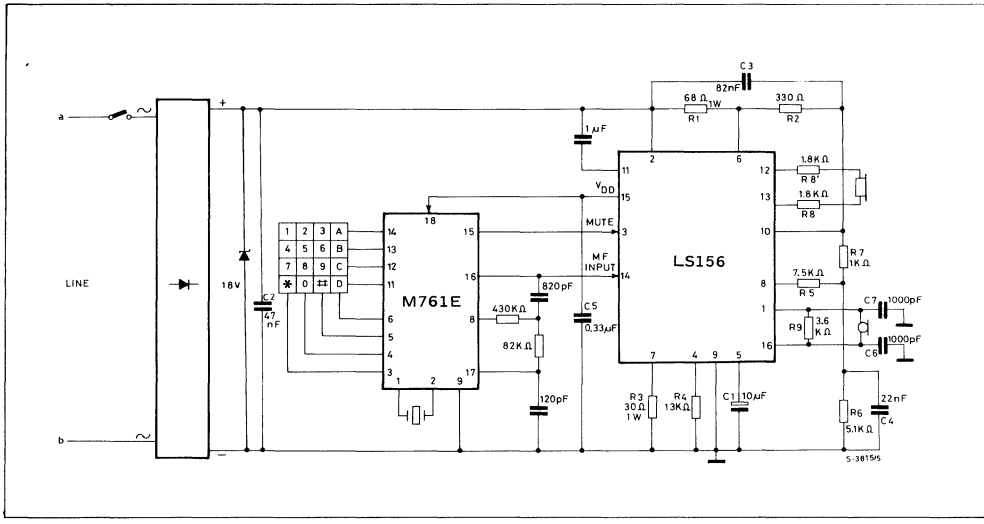


Fig. 5 – Start-up time definition

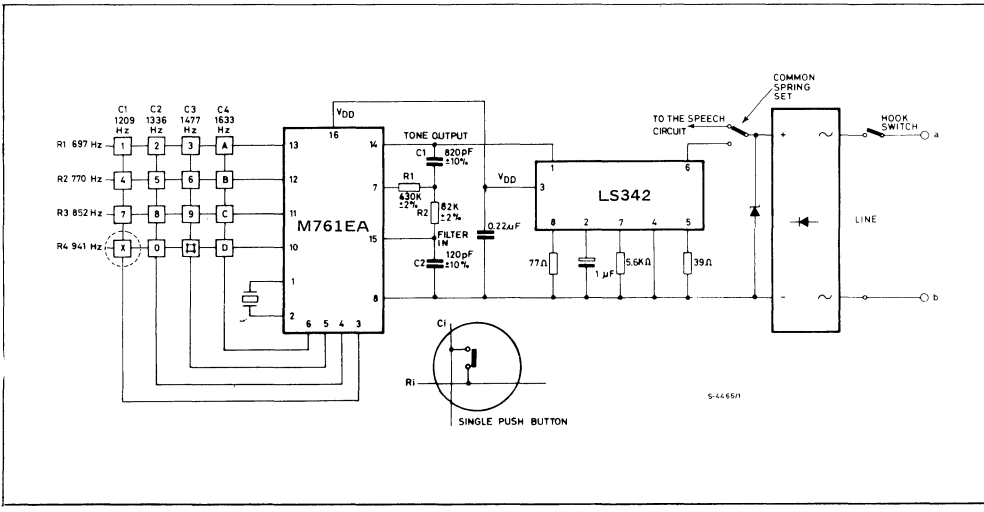


TYPICAL APPLICATIONS

M761E application circuit with electronic speech circuit



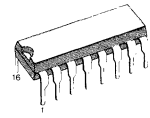
M761EA application circuit with LS342 line interface



M764A

TONE RINGER

- WIDE OUTPUT TONE SELECTION
- DIRECT DRIVE FOR PIEZOCERAMIC OR DYNAMIC TRANSDUCERS
- BUILT IN BAND PASS FILTER (20 TO 60Hz)
- μP CONTROL INPUT
- CMOS TECHNOLOGY



B
DIP-16 Plastic (0.25)

ORDERING NUMBER: M764A B1

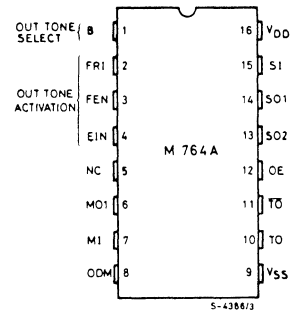
DESCRIPTION

The M764A is a high performance electronic ringer suitable for application in standard and parallel connection telephones; it can also be used as an alarm indicador. An incorporated bandpass filter prevents spurious ringing caused by transients and dialling pulses. Pin-selectable options permit three, two and single tone sequences.

The output stage allows direct drive of both piezoceramic and dynamic transducers. The output tone level can be externally programmed to increase gradually during the first three bursts. Output tone stability and the bandpass filter corner frequencies are guaranteed by a crystal controlled oscillator.

The M764A is available in 16 pin dual in-line plastic.

PIN CONFIGURATION

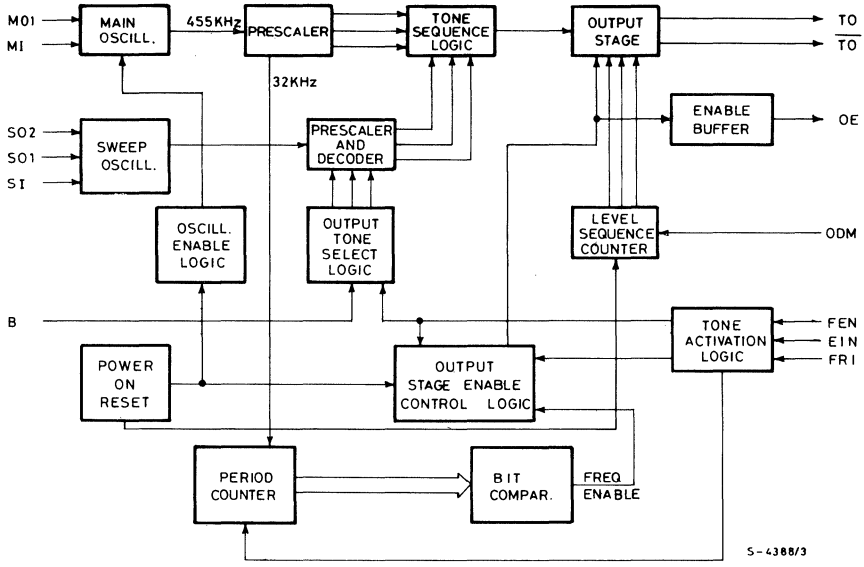


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5V to +17	V
V_I	Input voltage	-0.3 to V_{DD} +0.5	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	-25 to 70	°C
T_{stg}	Storage temperature range	-55 to 125	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (All parameters are tested at $T_{amb} = 25°C$)

	Parameter		Test conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS								
Supply	V_{DD}	Voltage supply			6		17	V
	V_{TH}	Power on/off reset threshold			4.5		5.5	V
	V_{TH}	Sequence logic power on/off reset			1.8		2.8	V
	I_{DD}	Operating supply current	V_{DD}= 15V OE = 1				0.75	mA
	I_{DDO}	Stand-by supply current	V_{DD}= 15V				0.15	mA
Main oscillator	MI	Main oscillator input	I_{IH} V_{IH}= 15V	V_{DD}= 15V			+5	µA
			I_{IL} V_{IL}= 0V				-1	
	MO1	Main oscillator output 1	I_{OH} V_{OH}= 13V	V_{DD}= 15V	-250			µA
			I_{OL} V_{OL}= 1V		+250			

ELECTRICAL CHARACTERISTICS (continued)

Parameter			Test conditions		Min.	Typ.	Max.	Unit
Sweep oscillator	SI	Sweep oscillator input	I_{IH} V_{IH}= 15V	V_{DD}=15V			+1	µA
			I_{IL} V_{IL}= 0V				-1	
	SO1	Sweep oscillator output 1	I_{OH} V_{OH}= V_{DD}-1V	V_{DD}=15V	-90			µA
			I_{OL} V_{OL} V_{DD}13V		+90			
	SO2	Sweep oscillator output 2	I_{OH} V_{OH}= V_{DD}-1V	V_{DD}=15V	-90			µA
			I_{OI} V_{OL} V_{DD}13V		+90			
Control pins	EIN FEN ODM	Enable input Filter enable input Output drive mode	I_{IH} V_{IH} = 15V			0.1	+1	µA
			I_{IL} V_{IL} = 0V			-0.1	-1	
	A B C *	Output sequence selection pins	I_{IH} V_{IH} = 15V			0.1	5	µA
			I_{IL} V_{IL} = 2V			1		mA
Freq. input	FRI	Frequency input	I_{IL} V_{IL}= 0V				1	µA
			I_{IH} V_{IH}= 4V		4	20	40	
			V_{TH}		2		4	V
Output enable	OE		I_{OH} V_{DD}= 15V V_O = 13V		10			mA
			I_{OL} V_{DD}= 15V V_O = 1V		1			
Tone outputs	TO	Output	I_{OH} V_{DD} 15V V_O 13V		10			mA
			I_{OL} V_{DD} = 15V V_O 1V		10			
	$\overline{TO}$	Inverted output	I_{OH} V_{DD} 15V V_O 13V		10			mA
			I_{OL} V_{DD} 15V V_O 1V		10			

* Input resistor of 1.5KΩ is active until V_{TR} of input inverter is reached

AC CHARACTERISTICS

Main oscillator	t_{SM}	Start up time	V_{DD}= 6V f_o= 455 KHz			10		ms
			R_F= 1 MΩ C_I= C_O= 100 pF	see tables 1-2				
Sweep oscill.	t_{SS}	Start up time	V_{DD}= 6V f = 1140 to 11400 Hz (*)			5		ms

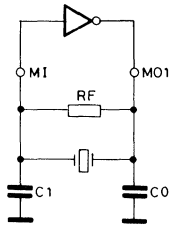
(*) R > 50 KΩ
C > 100 pF

FUNCTIONAL DESCRIPTION

Main Oscillator

The main oscillator has been designed to be driven either by an external RC network or by a ceramic resonator (see fig. 1):

Fig. 1 - a) Crystal controlled oscillator



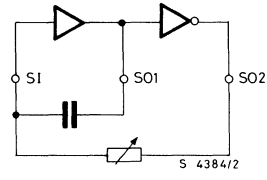
The accuracy of the output tones and of the band-pass filter characteristics are determined by the accuracy of the main oscillator frequency.
The crystal guarantees good performance over the whole temperature range with no external trimmer.
The main oscillator as well as the sweep oscillator are maintained in a stand-by condition or forced to run according to table 1.

Sweep Oscillator

The sweep oscillator (fig. 2) controls the repetition rate of the output tone sequence. The output repetition period is given by

$$T_{rep} = \frac{384}{F_{sweep\ oscill.}}$$

Fig. 2

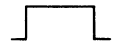
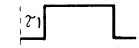
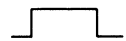
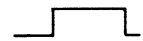
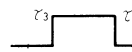
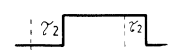
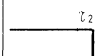
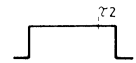
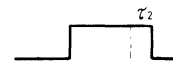


Output Tone Activation (pins FEN, EIN, FRI)

The output stage is enabled by the signal OE (output enable) under control of pins FEN, EIN, FRI as shown in table 1, and fig. 3.
Pin FEN and EIN are standard C-MOS inputs.
Pin FRI has a pull-down resistor of approximately 300 KΩ.

FUNCTIONAL DESCRIPTION (continued)

Table 1

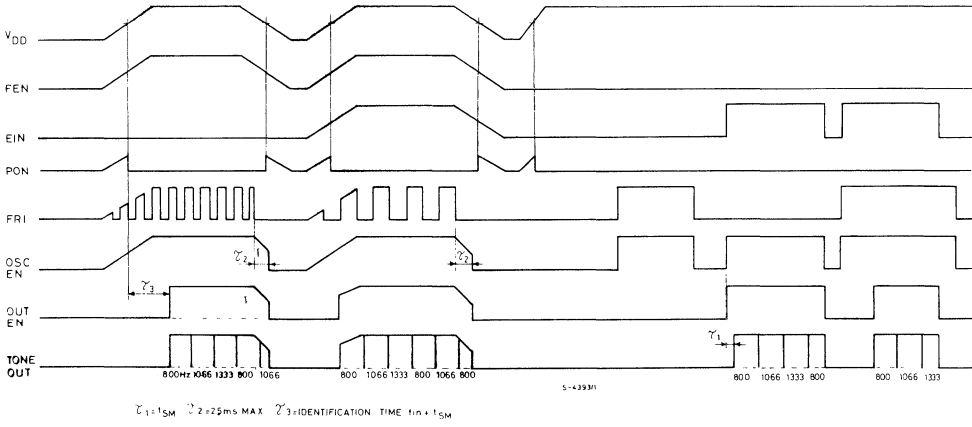
FEN	EIN	FRI	OSC. EN.	OUT. EN.	TONE OUT
0	0	0	0	0	0
0	0	1	1	0	0
0		0			
0		1	1		
1	0				
1	1				

IF f > fmin

S-4392/1

$\tau_1 = t_{SM}$ $\tau_2 = 25ms$ MAX τ_3 = IDENTIFICATION TIME fin + t_{SM}

Fig. 3 - Timing diagram

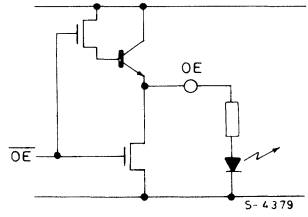


FUNCTIONAL DESCRIPTION (Continued)

Output Enable (OE)

The output enable pin (OE) can be used in special application to drive a LED or any external circuit to indicate that an incoming ringing signal has been detected by the tone ringer as in automatic responders. OE timing diagrams are shown in table 1.
The OE output stage configuration is shown in fig. 4.

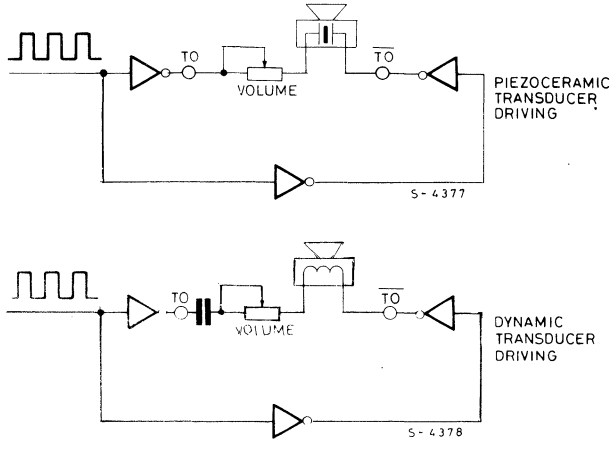
Fig. 4



Tone Outputs (TO, $\overline{TO}$)

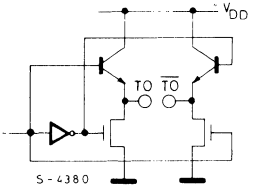
Two complementary outputs are provided to drive in a bridge configuration both piezoceramic and dynamic transducers (see fig. 5).

Fig. 5



The configuration of the output buffer is shown in fig. 6.

Fig. 6



The output waveform is a square wave with 50% duty cycle.
The generated tone level can be constant or can be gradually increased up to the max. level during the detection of the first three ring signals.
This function has been implemented controlling the output voltage swing that can be V_{DD} for max. output level, 0.4 V_{DD} for the intermediate output level and 0.1 V_{DD} for the lowest output level.

Output Drive Mode (ODM)

The output level is constant if this pin is a logical 0: it gradually increases to the max, level if this pin is a logical 1: the sequence can take place if after the first ring signal during the ring tone pause period the supply does not fail below the power on reset threshold (5.5V) and always starts from the lowest level.

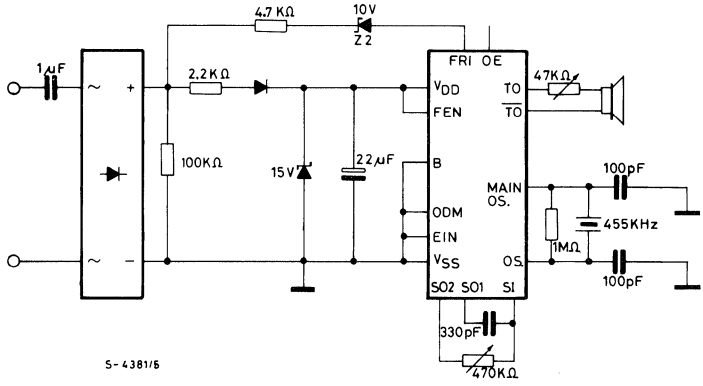
Output Tone Selection (B)

Table 2 **B** Output tone sequences and frequencies $f_{max\ oscill.}$ = 455KHz

0	800	1066	1333
1	800	1066	

TYPICAL APPLICATIONS

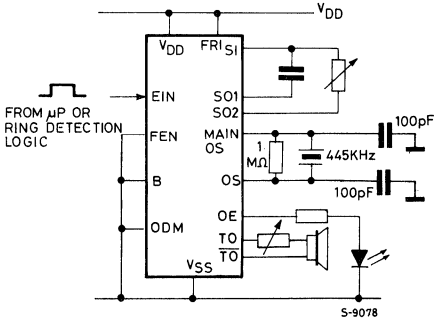
a) **Tone ringer for standard telephone applications**



If pin EIN is connected to V_{DD} the ringer is activated by frequencies upper than 20Hz.

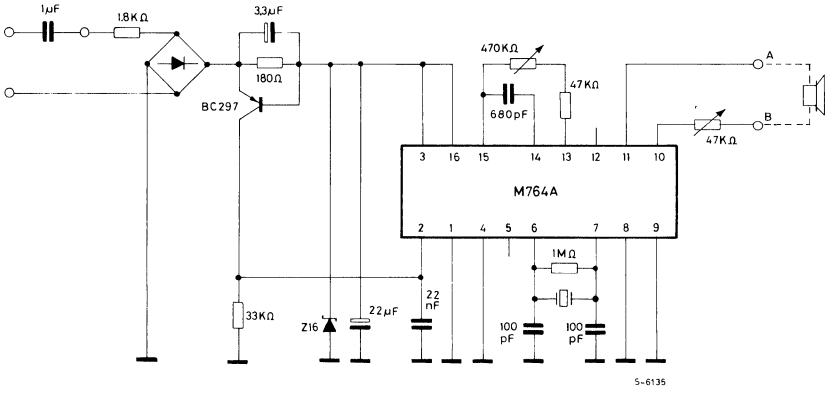
- In both cases the volume potentiometer can be avoided connecting the ODM to V_{DD} allowing the gradually increase of the ringer volume in three steps.
- The number of the output available tones and their frequencies are controlled by ABC pins according to table 2.

b) **Tone ringer for alarm, buzzer or ring tone detection in centralized equipments.**



Anti Tapping Application

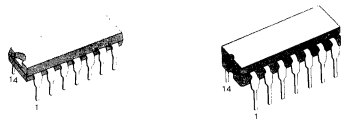
In the anti-tapping application an input current threshold is established.



M774

TONE RINGER

- WIDE OUTPUT TONE SELECTION
- DIRECT DRIVE FOR PIEZOCERAMIC OR DYNAMIC TRANSDUCER
- BUILT IN BAND PASS FILTER (14 TO 66Hz)
- BUILT IN DIODE BRIDGE



B
DIP-14 Plastic (0.25)

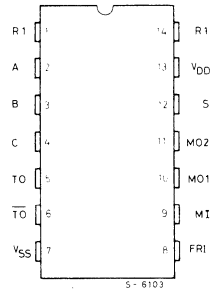
F
Ceramic Frit-seal (0.25)

ORDERING NUMBER: M774 B1
M774 F1

DESCRIPTION

The M774 is a high performance electronic ringer suitable for application in standard telephone sets. An incorporated band pass filter prevents spurious ringing caused by transients and dialling pulses. Pin selectable options permit three and two tone sequences with different sweep rate. The ouput stage allows direct drive of both piezoceramic and dynamic transducers.
The M774 is available in a 14 lead dual in-line plastic and ceramic package.

PIN CONFIGURATION

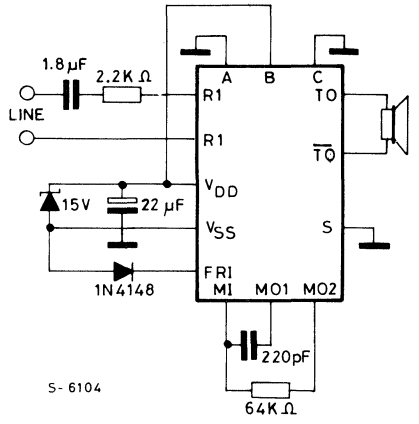


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	-0 to 70	°C
T_{stg}	Storage temperature range	-55 to 80	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS (All parameters are tested at $T_{amb} = 25°C$)

Parameter		Test condition	Min.	Typ.	Max	Unit
DC CHARACTERISTIC						
V_{DD}	Voltage Supply		7		16.0	V
V_{TH}	Power on/off Reset Threshold		4.0		5.5	V
I_{DD}	Operating Supply Current	$V_{DD} = 15V$			0.75	mA
I_{DDO}	Stand-by Supply	$V_{DD} = 15V$			0.15	mA
MI	Main Oscillator Input	I_{IH} $V_{IH} = 15V$ I_{IL} $V_{IL} = 0V$			+5 −1	µA µA
MO1	Main Oscillator Output 1	I_{OH} $V_{OH} = 13V$ $V_{DD} = 15V$ I_{OL} $V_{OL} = 2V$	+250			µA
MO2	Main Oscillator Output 2	I_{OH} $V_{OH} = 13V$ $V_{DD} = 15V$ I_{OL} $V_{OL} = 2V$	+250			µA
TO	Output	I_{OH} $V_{DD} = 15V$ $V_O = 13.5V$ I_{OL} $V_{DD} = 15V$ $V_O = 1V$	10 10			mA
TO	Inverted output	I_{OH} $V_{DD} = 15V$ $V_O = 13.5V$ I_{OL} $V_{DD} = 15V$ $V_O = 1V$	10 10			mA

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test condition	Min.	Typ.	Max	Unit
AC CHARACTERISTICS						
t_S	Start Up time	V_{DD} = 6V f_O = 32kHz		10		ms
f_{min}	Low frequency limit	f_O = 32kHz		14		Hz
f_{max}	High frequency limit	f_O = 32kHz		66		Hz
t_{OS}	Stop time	f_O = 32kHz			36	ms
Z_{in}	Small signal stand by impedance	Z_{in} = 1.5Vr ms a 1kHz	100			KΩ

FUNCTIONAL DESCRIPTION

Ringing input (IRI)

This input is connected the telephone line according to the application circuit shown.
The tone output is enabled only if the ringing signal frequency is between 14 Hz and 66 Hz.

Output tone selection

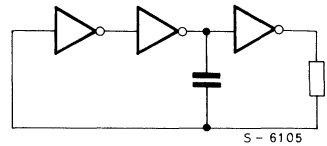
Different output tone sequences are selectable as shown in table 1.

Table 1 (f_{osc} = 32kHz)

A	B	C	Frequencies output		
0	0	1	233	382	446
0	1	0	800	1066	1333
0	1	1	400	533	666
1	0	0		1000	1250
1	1	0		1172	1333
0	0	0	466	764	892
1	0	1		500	625
1	1	1		586	666

Oscillator (MI, MO1, MO2)

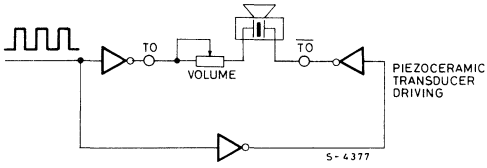
M774 uses an inexpensive RC oscillator.

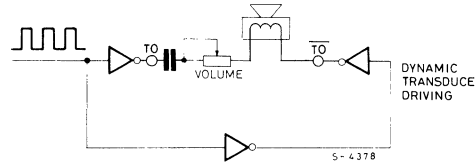


The good stability against supply voltage of this configuration ensures good bandpass filter performance.

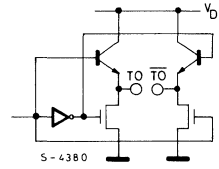
Tone outputs (TO, TO)

Two complementary outputs are provided to drive in bridge configuration both piezoceramic and dynamic transducers see fig.





The configuration of the output buffer is shown in fig.



The output waveform is a square wave with 50% duty cycle.

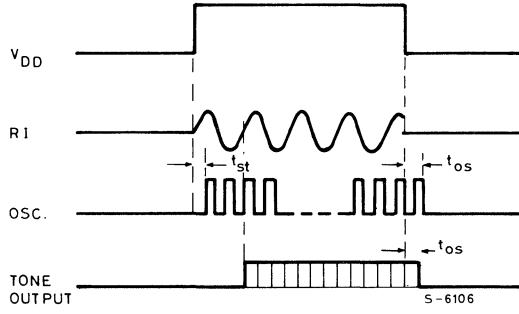
Sweep rate selection

With the M774 it's possible to select two different sweep rates of the output tones according to tab. 2

Table 2

S	Sweep rate
0	10 Hz
1	20 Hz

TIMING DIAGRAM



M1094

ADVANCE DATA

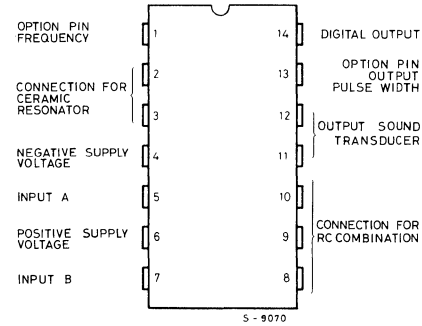
THREE-TONE RINGER

- ON-CHIP RECTIFIER BRIDGE AND TRANSIENT PROTECTION
- DIRECT DRIVE OF PIEZOCERAMIC OR DYNAMIC TRANSDUCERS
- NOISE SUPPRESSION BY DIGITAL FREQUENCY FILTER AND LEVEL DETECTOR
- USES LOW COST CERAMIC RESONATOR FOR MAIN OSCILLATOR
- REPETITION RATE OF TONE SEQUENCE ADJUSTABLE BY RC TIME CONSTANT

B
DIP-14 Plastic

ORDERING NUMBER: M1094 B1

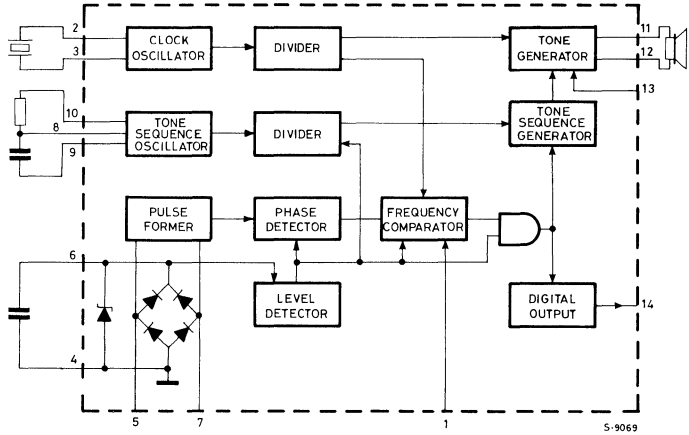
PIN CONFIGURATION



DESCRIPTION

The M1094 replaces the electromechanical telephone bell and calls the subscriber by a melodic tone sequence. It derives its power supply by rectifying the ac ringing signal, requires only a minimum of additional components and is compatible with the conventional telephone network.

Fig. 1 - Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Supply Current	I5, I7 = ± 25	V
V_I	Input Voltage	V_I V_{SS} -0.3 to V_{DD} +0.3	V
	Output Current	I 11, I12, I14 = ± 10	mA
T_{op}	Operating Ambient Temperature	-25 to +60	°C
T_{stg}	Storage Temperature	-40 to + 125	°C
	Furthermore, the conditions of section 9 are applicable		

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock Oscillator Frequency	–	455	–	KHz
	Power Supply (See Functional Description)	–	–	–	–

ELECTRICAL CHARACTERISTICS (at V6-4 = 10V; f_C = 455KHz; T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I5, I7	Current consumption, outputs without load.		1.4	1.8	mA
f_{IN}	Frequency range of the ac input current into pins 5 and 7 which gives an output signal at pins 11 and 12; (Test Circuit - Fig. 7). a) Pin 1 unconnected b) Pin 1 connected to pin 4 = V_{SS} c) Pin 1 connected to pin 6 = V_{AD} dc operation (See section 3)	 23 12		 54 54	 Hz Hz
f_{IN}	Frequency ranges of the ac input current into pins 5 and 7 which do not produce output signals at pins 11 and 12; (Test circuit - Fig. 8). a) Pin 1 unconnected	 0 60		 18 ∞	 Hz Hz
R_{ON}	On-resistance of outputs: pin 11, pin 12, at I_{OL} = 5mA or I_{OH} = -5mA pin 14, at I_{OL} = 5mA pin 14, at I_{OH} = -5mA			 90 500 300	 Ω Ω Ω
f_{01} f_{02} f_{03}	Frequency of the output signal at pin 11, pin 12		813 1083 1354		
	Start-up time of clock oscillator			10	ms
V6-4	Internal supply voltage limitation at I5, I7 = 10mA	15		18	V
V6-4 ON V6-4 OFF	Switching levels of voltage level detector: Turn-on level Turn-off level	 6 3		 7.5 4.5	 V V

GENERAL DESCRIPTION

The M1094 replaces the customary electromechanical telephone bell and calls the subscriber by a melodic tone sequence, using a small magnetic or piezoceramic sound transducer. The melody ringer circuit, together with its transducer is powered by the ringing current from the exchange. This makes it compatible with the conventional telephone network and, in addition, no battery or mains connections are needed (Fig. 2). It is also possible to apply a DC signal instead of the AC ringing signal (Fig. 3). As shown in Fig. 2 and 3 the amount of additional components is reduced to a minimum.

FUNCTIONAL DESCRIPTION OF THE TONE RINGER CIRCUIT

POWER SUPPLY

The tone ringer circuit (Fig. 2) derives the power required for its operation from the ringing AC supplied by the exchange via linea a and b. Together with the loop resistance, the specified 1μF isolating capacitor and a 2.2KΩ resistor is needed to ensure a minimum impedance.

The supplied alternating current is fed to pins 5 and 7 of the tone ringer and is rectified by means of an integrated bridge circuit in the M1094. The rectified current charges the electrolytic capacitor at pin 4 and 6. The direct voltage V6-4 generated across this capacitor is the supply for the internal circuitry. It mainly depends on the loop resistance and on the ringing frequency. Its maximum value is limited by an internal Zener diode to about 16V.

CLOCK SIGNAL GENERATION

The clock oscillator, integrated in the M1094 tone ringer I_C requires only an inexpensive ceramic resonator connected to pins 2 and 3, for example the 455KHz type Murata CSB 455E. The frequency of this oscillator is used to derive the three output tone frequencies and the clocks for the input frequency comparator.

MONITORING THE INPUT RINGING FREQUENCY

The frequency f_{IN} of the ringing AC supplied to the inputs pins 5 and 7 is monitored in the M1094 by a frequency comparator. The result of the frequency comparison is used as one criterion for activating the tone generator (see section 4 for the other criterion). The circuit generates output tones only if the input ringing signal is inside a specified frequency band. Three different modes can be selected by the option pin 1.

a) Pin 1 unconnected:
In this mode a frequency f_{IN} from 23 to 54Hz will be accepted for producing the output tone sequence.

b) Pin 1 connected to pin 4 = 0
In this mode a frequency f_{IN} from 12 to 54Hz will be accepted. Due to this option, the M1094 can also be employed in telephone systems having a ringing frequency below 20Hz.

c) Pin 1 connected to pin 6 = 1
In this mode the result of the frequency comparison has no influence. A DC signal can be applied to the M1094 at pins 4 and 6 or pins 5 and 7 for producing the output tone sequence.

A digital noise suppression circuit in the M1094 ensures that noise signals in the range from 0Hz to 20KHz and with a maximum amplitude of 9V RMS will not affect the correct function of the M1094 if the input ringing signal applied to the terminals and b of Fig. 2 has an amplitude of 50V RMS and a frequency in the range specified for producing an output signal.

VOLTAGE LEVEL DETECTOR

The voltage level V6-4 is monitored in the M1094 and used as another criterion for activating the tone generator. The tone sequence will be started when V6-4 increases to a level around 6V. The tone sequence will be ended when V6-4 decays to a level around 3V.

TONE SEQUENCER

The ringing signal produced by the M1094 is a sequence which is determined by the external RC network of the tone sequence oscillator and by the ratio of the frequency divider. The relationship between repetition rate f_R and oscillator frequency f_{OS} is:

$$f_R = \frac{f_{OS}}{3 \cdot 32}$$

The repetition frequency can be adjusted from 2.4Hz ± 0.2Hz to 25Hz ± 3.5Hz using the connection scheme of Fig. 4 and the following component values:

C = 4.7nF
R3 = 43KΩ
R4 = 0 to 600KΩ

FUNCTIONAL DESCRIPTION (continued)

The repetition frequency can be calculated using the formula:

$$f_R\ (Hz) = \frac{10^6}{134.4 \cdot C \cdot (20 + R)}$$

with C(nF) = capacitance between pins 8 and 9, R(KΩ) = resistance between pins 8 and 10.

The repetition frequency depends slightly on the supply voltage V6-4. The variation is equal or less than +4% per 1V.

TONE GENERATOR

The ringing signal is a sequence of three tones. Their frequencies are derived from the clock frequency at division rates of 560, 420 and 336. Depending of the clock frequency f_C the tone frequencies are:
813Hz, 1083Hz, 1354Hz for f_C = 455KHz or
800Hz, 1067Hz, 1333Hz for f_C = 448KHz

This is a harmonic ratio of 3:4:5. The sequence will be started if two conditions are fulfilled: The input ringing signal f_{IN} has to be inside a specified frequency band and the supply voltage V6-4 has to be increased to the turn-on level. The sequence always starts with the lowest tone. The sequence ends, if f_{IN} departs from the specified frequency band or if V6-4 is lowered to the turn-off level.

TONE OUTPUT

The output amplifier of the M1094 tone ringer is a push pull bridge circuit. It supplies two square wave signals of opposite phase at pin 11 and pin 12. The high value of the signal equals the potential of pin 6 and the low value equals the potential of pin 4, if no load is connected to the outputs. Optionally, the pulsewidth of the squarewave output signal can be limited to 0.2ms internally, in order to save the components of an external limiting circuit containing a capacitor. The shorter pulse-width is of advantage in the case of an electromagnetic transducer being used which will operate with increased efficiency in this case. The connection of pin 13 determines the mode: when connected to pin 4, the pulse-width is not affected. If pin 13 is left unconnected, the pulsewidth will be 0.2ms. The waveform of the current through the load is shown for both cases in Fig. 5.

DIGITAL OUTPUT

The digital outuput pin 14 can be used for connecting a supplementary load to the supply terminals pins 4 and 6 when the tone generation is deactivated. Without the supplementary load the voltage V6-4 may decrease significantly upon activation of the tone generation.
The digital output is at the voltage level of pin 6 as long as the two conditions (f_{IN} and V6-4) for the tone generation are not fulfilled. A supplementary load current can then be drawn through an external resistor between pins 14 and 4. As soon as the conditions for the tone generation are fulfilled, the digital output switches to the voltage level of pin 4.

OVERLOAD PROTECTION

The M1094 can withstand an alternating voltage of 110V at a frequency of 50Hz across terminals a and b of Fig. 2 for 15 seconds.

The circuit will not be damaged by a transient voltage test with the following test conditions:

Voltage across the charge capacitor	2KV
Pulse timing	10/700μs
Pulse sequence	30s
Number of transients	16
Polarity change after	5 transients
Test circuit	Fig. 4

Fig. 2 - M1094 with power supplied by the AC ringing signal

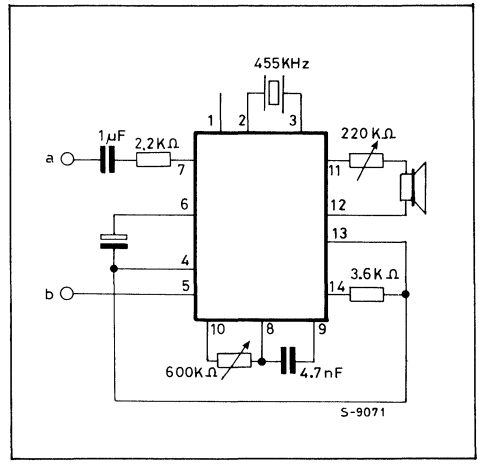


Fig. 3 - M1094 with power supplied by DC

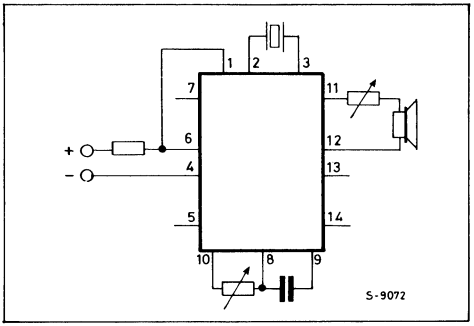
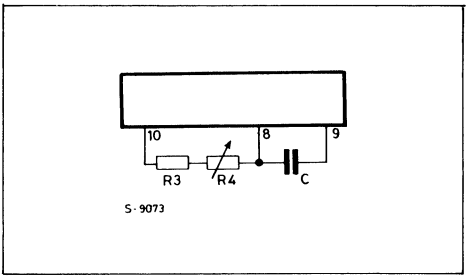


Fig. 4 - Circuit connection scheme for repetition frequency adjustment described in section 5



Figg. 5a/5b - Diagram of output current through a load between pins 11 and 12

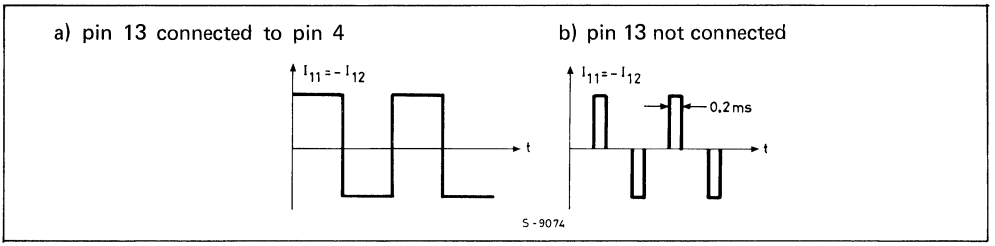


Fig. 6 - Circuit for transient voltage test described in section 9

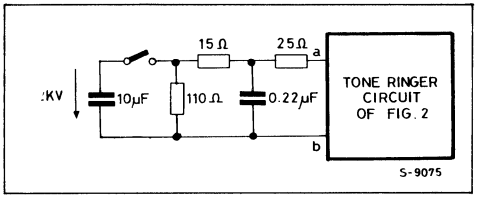


Fig. 7 - Test circuit which activates the output signal generator (see also frequency specification)

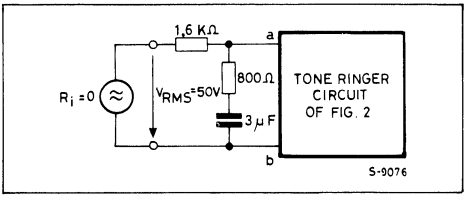
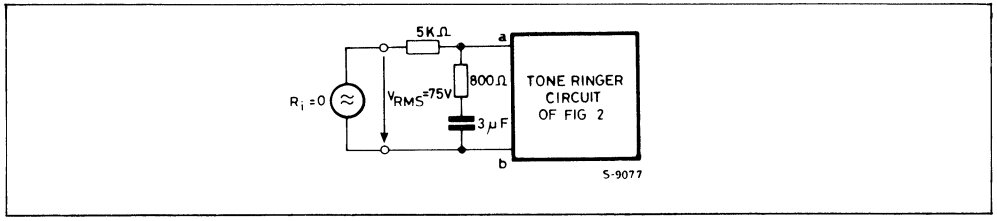


Fig. 8 - Test circuit which does not activate the output signal generator (see also frequency specification)

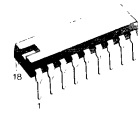


M2560A

DECADIC PULSE DIALLER

- R-C OSCILLATOR GENERATES ALL TIMING WITH AN ACCURACY BETTER THAN ± 5% OVER COMPLETE TEMPERATURE RANGE
- DIALLING SPEED CAN BE REGULATED VIA OSCILLATOR FREQUENCY
- TWO MARK/SPACE RATIONS: $33\frac{1}{3}$ / $66\frac{2}{3}$ OR 40/60
- AVAILABILITY OF REDIAL WITH TWENTY DIGIT MEMORY WHICH ALSO FUNCTIONS AS BUFFER DURING DIALLING
- CMOS PROCESS
- IGNORES MULTY KEY ENTRIES

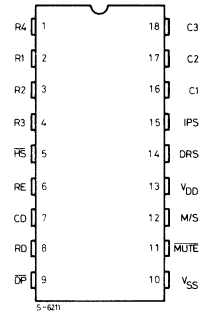
The M2560 converts the key press signals into a series of digital pulses similar to those generated by a mechanical dialler.
The M2560A is available in 18-lead dual in-line plastic package.



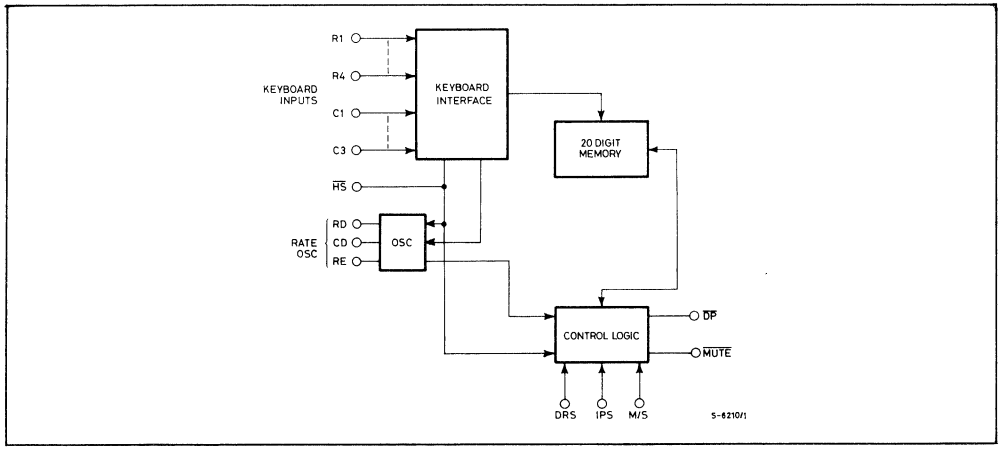
B
DIP-18 Plastic

ORDERING NUMBER: M2560NB1

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Specifications apply over the operating temperature and $1.5V \leq V_{DD}$ to $V_{SS} \leq 3.5V$ unless otherwise specified.

Parameter		$V_{DD}-V_{SS}$ (V)	Test Conditions	Min.	Max.	Units
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current (Sink)	3.5	$V_{OUT}=0.4V$	125		μA
I_{OHDP}	$\overline{DP}$ Output High Current (Source)	1.5 3.5	$V_{OUT}=1V$ $V_{OUT}=2.5V$	20 125		μA μA
I_{OLM}	$\overline{MUTE}$ Output Low Current (Sink)	3.5	$V_{OUT}=0.4V$	125		μA
I_{OHM}	$\overline{MUTE}$ Output High Current (Source)	1.5 3.5	$V_{OUT}=1V$ $V_{OUT}=2.5V$	20 125		μA μA
V_{DR}	Data Retention Voltage		"On Hook" $\overline{HS}=V_{DD}$ Keyboard open, all other input pins to V_{DD} or V_{SS}	1.0		V
I_{DD}	Quiescent Current	1.0			750	nA
I_{DD}	Operating Current	1.5 3.5	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}=V_{SS}$("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above		100 500	μA μA
fo	Oscillator Frequency	1.5			10	kHz
Δ fo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	Fixed R-C oscillator components $50K\Omega \leq RD \leq 750K\Omega$; $100pF \leq CD^* \leq 1000pF$; $750k\Omega \leq RE \leq 5M\Omega$; * 300pF most desirable value for CD	−3 −3	+3 +3	% %
	Input Voltage Levels					
V_{IH}	Logical "1"			80% of $(V_{DD}-V_{SS})$	V_{DD} +0.3	V
V_{IL}	Logical "0"			V_{SS} −0.3	20% of $(V_{DD}-V_{SS})$	V
C_{IN}	Input Capacitance Any Pin				7.5	pF

Note: To prevent excessive dissipation, which could damage the device, V_{DD} must always be applied before any input is applied. In addition the following conditions must be maintained: $V_{SS} <= V_i <= V_{DD}$.
To ensure correct device reset, H_S = 1 should be valid (on Hook condition)when V_{DD} is applied.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	+ 5.5	V
V_{IN}	Voltage at any Pin	V_{SS} -0.3V to V_{DD} + 0.3	V
T_{stg}	Storage Temperature Range	-65 to + 150	°C
T_{op}	Operating Temperature Range	-25 to + 70	°C
	Lead Temperature (Soldering, 10 sec)	300	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

OSCILLATOR

An R-C oscillator, with external RC components (2 resistors and a capacitor), supplies all device timing.
This oscillator is operational only while a number is being dialler and dialling pulses are being transmitted. Under all other conditions, including the "On Hook" condition, the oscillator is inoperative.
Typical oscillator frequency, for 10 pps, is 2400Hz, obtained with two external 750KΩ resistors and a 270pF capacitor. A tolerance of less than ± 1% can be obtained using resistors with 5% tolerance and capacitors with a tolerance of ± 5%.

KEYBOARD INTERAFACE

The M2560 scans the keyboard to establish key state (open or closed)

OFF HOOK OPERATION

In the Off-Hook condition, the M2560A is supplied via a 150KΩ resistor. The DP output is normally high, holding the transistor, which replaces the mechanical dial contact, in the on condition. This transistor causes the line disconnects corresponding to the key pressed.
Table 2 shows the various possible operating modes as a function of the programming pins. Obviously modifying the master clock frequency gives a proportional modification of the DIAL RATE and Inter Digit Pause. The chip also includes an anti-bounce delay of 20ms minimum.

FIRST DIAL AND REDIAL

The digit enter rate is approximately 50ms per digit with a daialling rate in the range 7 to 20 pps. The last dialled number is held in memory for subsequent redialling. Interdigit pause can be inserted during the first dial phase by pressing the "# " key, however the total number of digits pulse pause should not excedd 20.

Redial is obtained by lifting the handset and pressing the "# " key which causes the number to be automatically sent to the line. If a pause is detected the line pulsing is suspended untill the "# " key is pressed.

PIN DESCRIPTION

Keyboard Keys (R1, R2, R3, R4, C1, C2, C3) Pins 1, 2, 3, 4, 16, 17, 18

The key contact resistance must be less then or equal to 1KΩ.

Hook Switch ($\overline{HS}$) - Pin 5

Detects the On-Hook/Off-Hook condition with a low level corresponding to the Off-Hook condition.

Oscillator (RE, CD, RD) - Pins 6, 7, 8

Connections to the external components for the RC oscillator.

Pulse Output ($\overline{DP}$) - Pin 9

Supplies the dial pulses to the line disconnect transistor.

FUNCTIONAL DESCRIPTION (Continued)

Mute Output ($\overline{\text{MUTE}}$) - Pin 11
Drives the external receiver muting transistor.

Mark Space Selection (MS) - Pin 12
See relative table.

Dial Rate Selection (DRS) - Pin 14
See relative table

Inter Digit Pause Selection (IPS) - Pin 15)
See relative table. (Note an interdigit pause is also sent before the first digit pulses are sent to the line)

V_{DD} - Pin 13

V_{SS} - Pin 10

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	RD (kΩ)	RE (kΩ)	CD (pF)	Dial Rate (pps)		IDP (ms)	
					*DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
(f_d/240) (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\left(\frac{1920}{f_i}\times 10^3\right)$	$\left(\frac{960}{f_i}\times 10^3\right)$

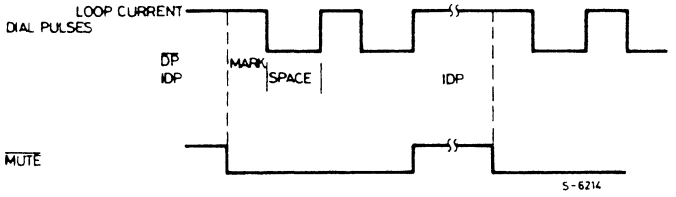
Note: IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10 pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14 pps, and IDP of either 1142ms or 571ms can be selected.
* DRS status scales of a factor 2.

Table 3.

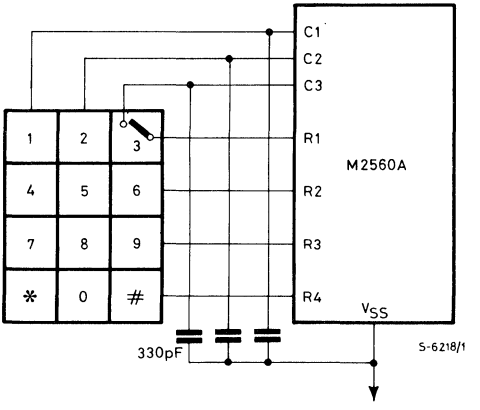
Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240) pps (f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33-1/3/66-2/3 40/60
On Hook/Off Hook	$\overline{\text{HS}}$	V_{DD} V_{SS}	On Hook Off Hook

Note: f is the oscillator frequency.

Timing



Switch Matrix Interface

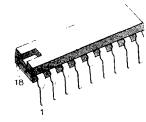


M3326

ADVANCE DATA

CMOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

- OPERATION FROM 2.5V TO 6V SUPPLY
- STATIC STANDBY OPERATION DOWN TO 1.8V
- LOW CURRENT CONSUMPTION; TYP. 40μA
- LOW STATIC STANDBY CURRENT; TYP. 1μA
- ON-CHIP OSCILLATOR FOR 3.58MHz CRYSTAL
- 23-DIGIT CAPACITY, INCLUDING ACCESS PAUSES
- DIALLING PULSE FREQUENCY: 10Hz, (932Hz FOR TEST)
- DIALLING PULSE MARK/SPACE RATIO SELECTABLE: 1.5:1 OR 2:1
- CIRCUIT RESET FOR LINE POWER BREAKS (LONGER THEN 270ms)
- ACCESS PAUSE GENERATION AUTOMATICALLY OR VIA THE KEYBOARD
- ACCESS PAUSE RESET: AUTOMATICALLY, VIA THE KEYBOARD, WITH EXTERNAL TONE RECOGNISER
- MAXIMUM DURATION OF ACCESS PAUSE SELECTABLE: 3s OR 6s
- MAXIMUM NUMBER OF ACCESS PAUSES SELECTABLE: 0, 1 OR 2
- ALL INPUTS WITH PULL-UP/PULL-DOWN (EXCEPT CE)

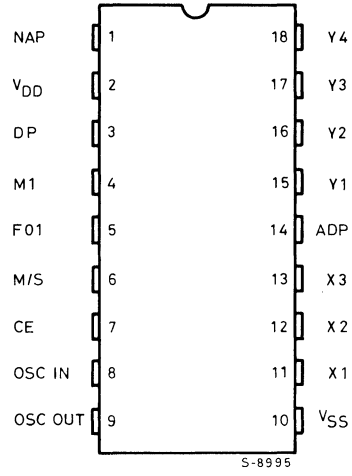


B

DIP-18 Plastic (0.25)

ORDERING NUMBER: M3326 B1

PIN CONFIGURATION



DESCRIPTION

The M3326 is a single chip silicon-gate CMOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3x4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. Access pauses can be stored automatically or via the keyboard.
The M3326 is available in 18 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

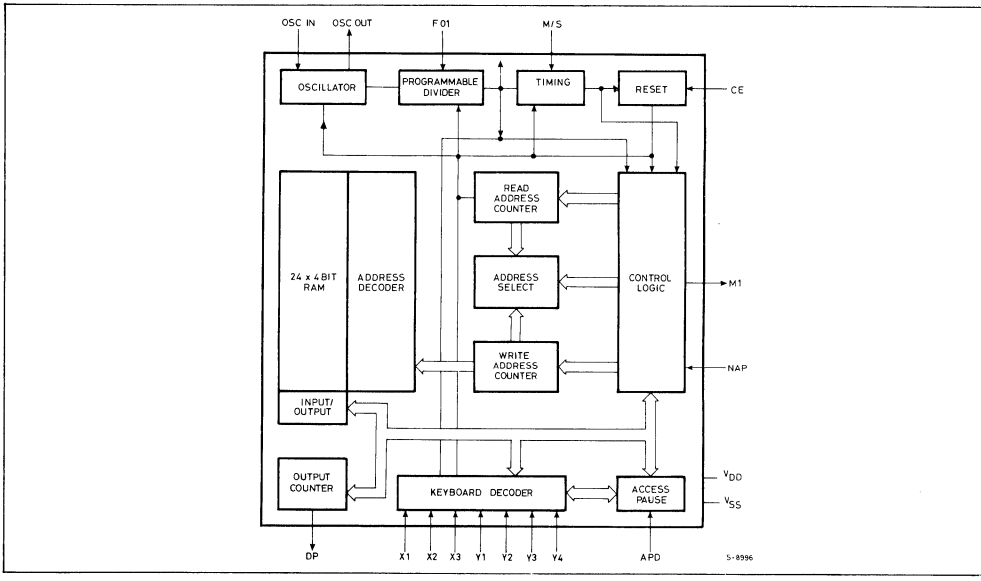
V_{DD}	Supply voltage	-0.3 to 8	V
V_I	Voltage on any pin	V_{SS} -0.3 to V_{DD} +0.3	V
T_{op}	Operating temperature range	-25 to +70	°C
T_{stg}	Storage temperature range	-55 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stresses ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions to extended periods may be affect device reliability.

PIN DESCRIPTION

Symbol	Function
SUPPLY	
V_{DD}	Positive supply.
V_{SS}	Negative supply.
INPUTS	
APD	Access Pause Delay; selects the maximum duration of an access pulse.
NAP	Number of Access Pauses; senses three input states: V_{DD}, $V_{DD/2}$, V_{SS}; limits the number of automatically stored access pause to 0, 1 or 2; if switched to V_{SS} it terminates an automatic or manual access pause.
M/S	Controls the mark-to-space ratio of the line pulses.
CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
X1, X2, X3	Column keyboard inputs with pull-down or chip.
Y1, Y2, Y3, Y4	Row keyboard inputs with pull-up on chip.
OUTPUTS	
DP	Dialling Pulse; drive of the external line switching transistor or relay.
M1	Muting; used for muting during the dialling sequence.
OSCILLATOR PINS	
OSC IN	Input of the on-chip oscillator.
OSC OUT	Output of the on-chip oscillator.

Fig. 1 - Block Diagram



TIMING CHARACTERISTICS (V_{DD} = 2.5 to 6V; V_{SS} = 0; f_{osc} = 3.579545MHz)

Symbol	Parameter		Conditions (Note 3)	F01		Unit
				V_{SS}	V_{DD}	
f_{DP}	Dialling pulse frequency	$1/T_{DP}$		9.708	939.2	Hz
T_{DP}	Dialling pulse period	$1/f_{DP}$		102.99	1.073	ms
f_{CL}	Clock pulse frequency	$30 \times f_{DP}$		291.3	27965	Hz
t_B	Break time (note 1)	$3/5 \times T_{DP}$	M/S = NC	61.77	0.644	ms
t_M	Make time (note 1)	$2/5 \times T_{DP}$	M/S = NC	41.21	0.429	ms
t_B	Break time (note 2)	$2/3 \times T_{DP}$	M/S = V_{DD}	68.66	0.715	ms
t_M	Make time (note 2)	$1/3 \times T_{DP}$	M/S = V_{DD}	34.33	0.358	ms
t_{ID}	Inter-digit pause	$8 \times T_{DP}$		824	858	ms
t_{RD}	Reset delay time	$8/3 \times T_{DP}$		275	2.9	ms
t_{AP}	Access pause time	$32 \times T_{DP}$	APD = V_{SS}	3.1	0.034	s
t_{AP}	Access pause time	$64 \times T_{DP}$	APD = NC	6.2	0.069	s
t_D	Delay last digit last pulse to M1 Debounce time	$1/3 \times T_{DP}$		34	0.358	ms
t_E Min.	Min.	$4/30 \times T_{DP}$		13.7	0.143	ms
t_E Max.	Max.	$1/6 \times T_{DP}$		17.2	0.179	ms
t_{ON} Typ.	Clock start-up time		(note 4)	4	–	ms
t_I	Initial data entry time (Typ.)	$t_{ON} + t_E$		19	4	ms

NOTES: 1. Mark-to-space ratio = 1.5 : 1
2. Mark-to-space ration = 2 : 1
3. In the NC (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/ pull-down current
4. After CE: $V_{SS} \rightarrow V_{DD}$. Stray capacitance between pins 8 and 9 < 3pF.

ELECTRICAL CHARACTERISTICS (V_{DD} = 3V; V_{SS} = 0; crystal parameters: f_{osc} = 3.58MHz, R_{SMAX} = 100Ω (note 3); T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating supply voltage	T_{amb} = -25 to +70°C	2.5	3	6	V
V_{DDO}	Standby supply voltage (note 1)	T_{amb} = -25 to +70°C	1.8		6	V
I_{DD}	Operating supply current	CE = V_{DD}; notes 2, 3		40		μA
		CE = V_{DD}; V_{DD} = 6V; notes 2, 3		50	100	μA
I_{DDO}	Standby supply current	CE = V_{SS}; note 2 V_{DD} = 1.8V T_{amb} = -25 to +70°C		1	2 2	μA
V_{IL}	Input voltage LOW	1.8V ⩽ V_{DD} ⩽ 6V			0.3 V_{DD}	
V_{IH}	Input voltage HIGH	1.8V ⩽ V_{DD} ⩽ 6V	0.7 V_{DD}			
I_{IL}	Input leakage current; CE LOW	CE = V_{SS}			50	nA
I_{IH}	HIGH	CE = V_{DD}			50	nA
I_{IL}	Pull-up input current APD NAP	V_I = V_{SS}	30 1.5	100 3	300 6	nA μA
I_{IH}	Pull-down input current F01, M/S NAP	V_I = V_{DD}	30 1.5	100 3	300 6	nA μA

MATRIX KEYBOARD OPERATION

I_K	Keyboard current	X connected to Y CE = V_{DD}		10		μA
R_{KON}	Keyboard "ON" resistance	Contact ON; note 4			500	Ω
R_{KOFF}	Keyboard "OFF" resistance	Contact OFF; note 4	1			MΩ

OTHER KEYBOARD OPERATION

I_{IH}	Input current for X_n "ON"	V_I = 1.5 to 3V			30	μA
I_{IL}	Input current for Y_n "OFF"	V_I = 0 to 2.5V	10			μA
I_I	Input current Y_n	V_I = V_{SS}			0.7	mA
I_{OL}	MI, DP Output Sink current	V_{OL} = 0.5V	0.7	1.5	3.2	mA
I_{OH}	Source current	V_{OH} = 2.5V	0.65	1.3	2.7	mA

NOTES:
1. V_{DDO} = 1.8V only for redial
2. All other inputs and outputs open
3. Stray capacitance between pins 8 and 9 < 3pF
4. Guarantees correct keyboard operation

FUNCTIONAL DESCRIPTION

CLOCK OSCILLATOR

The time base for the M3326 is a crystal controlled on-chip oscillator which is completed only connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01) to provide the normal clock frequency or the higher test frequency. Alternatively, the OSC IN input may be driven from an external clock signal.

CHIP ENABLE (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM. Input pull-up and pull-down devices are switched off.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time trd (see Figs. 4 and 5 and timing data) an internal reset pulse will be generated at the end of the trd period. The system is then in the static standby mode. Short CE pulses which duration is less t_{RD} will not affect the operation of the circuit. No reset pulses are then produced.

DEBOUNCING KEYBOARD ENTIRES

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3x4 single contact keyboard matrix (with or without common contact) as shown in Fig. 2, or to a double contact keyboard with a common left open (see Fig. 3). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted.

Valid inputs are debounced on the leading and trailing edges as shown in Fig. 4. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_E). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Fig. 2 - Single contact keyboard

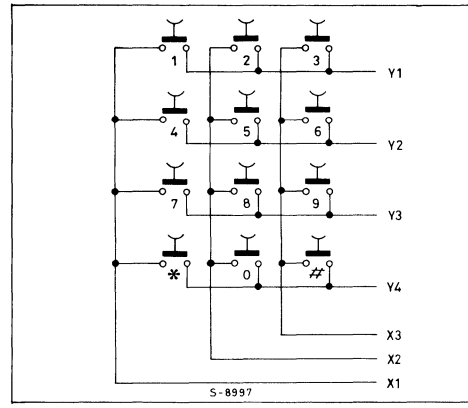
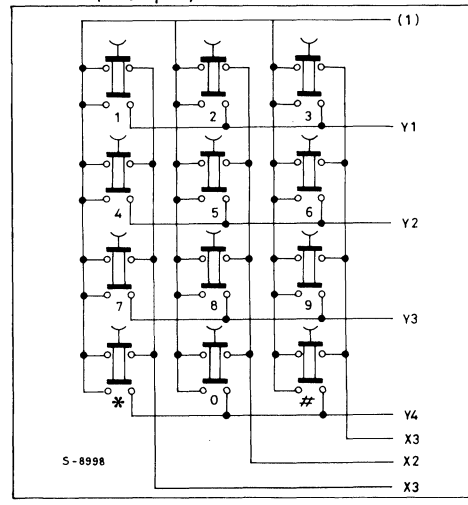


Fig. 3 - Double contact keyboard (1) common (left open)



* Access pause set # Redial

FUNCTIONAL DESCRIPTION (continued)

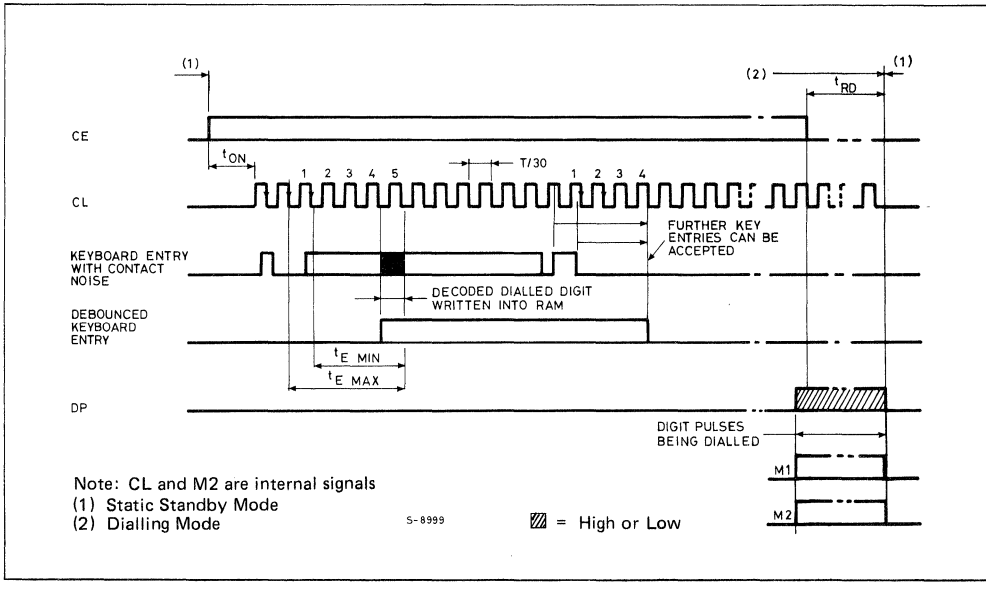
DATA STORAGE AND DATA RETRIEVAL
After each keyboard entry has been debounced and decoded, the keycode is written into the RAM and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM, but not yet converted into line pulses.

If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replaces the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_E, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one to select the next RAM location. Consequently, if the first pushbutton pressed is not redial, the data stored previously in the RAM cannot be redialled any more.

If the first pushbutton is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP.
If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset.
This function will be described later during the description of the access pause system of the M3326. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.

Fig. 4 - Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.



FUNCTIONAL DESCRIPTION (continued)

DIALLING SEQUENCE

The dialling sequence can be initiated under either of the following two conditions:

– The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 5

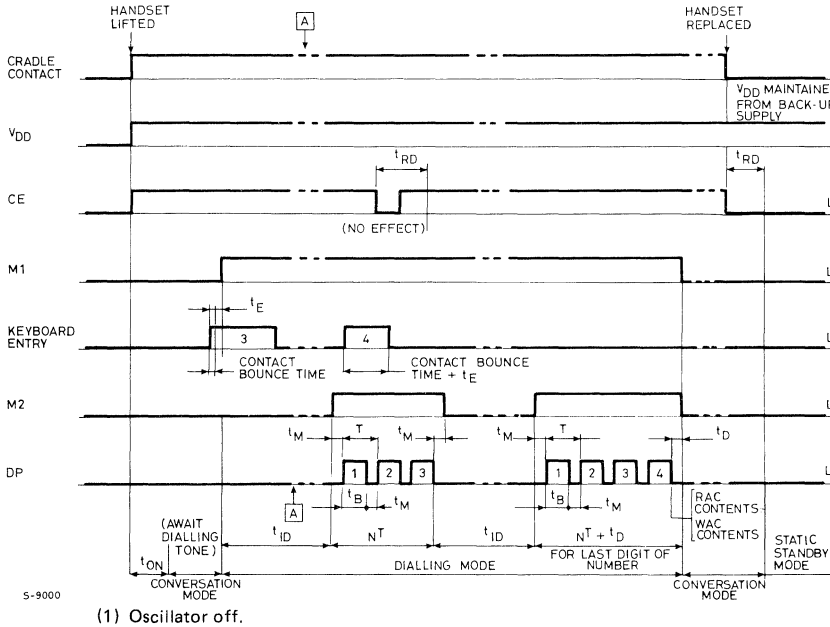
Then, approximately 4ms (t_{ON}) after CE goes HIGH, the clock pulse generator starts and the circuit is in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_E commences.

– The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 6).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4ms (t_{ON}) after CE goes HIGH, the clock pulse generator starts and data entry period t_E commences. After period t_E, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 5. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-difit pause (t_{ID}) ensures. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the

Fig. 5 – Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.



(1) Oscillator off.
All registers except WAC reset.
Keyboard input inhibited.
Number stored in RAM until $V_{DD} < 1.8V$.

FUNCTIONAL DECRIPTION (continued)

register of the output counter which generates the appropriate number of correctly timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time t_{rd} at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1.8V.

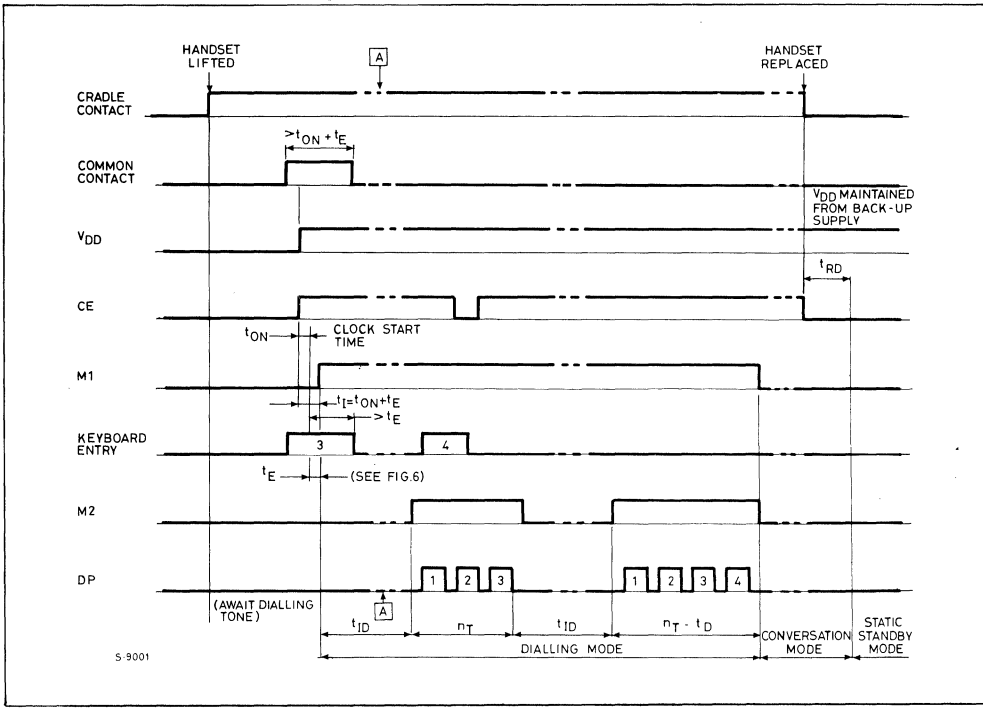
STORAGE AND REGENERATION OF ACCESS PAUSE

A dial sequence may require an extended inter-digit pause, if a dial tone has to be awaited.

During the keyboard entry whenever an access pause is needed a pause code can be stored in the RAM either automatically or via the keyboard for a later redial sequence. When an access pause is regenerated during redialling it can be terminated either automatically after a built-in delay time or via the keyboard or with an external dial tone recognizer circuit.

A pause code takes one position in the RAM like a digit. The number of digits plus the number of access pauses can therefore be up to 23.

Fig. 6 - Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard.
See Fig. 6 for pulse timings after point A. M2 is an internal signal.



FUNCTIONAL DESCRIPTION (continued)

AUTOMATIC PAUSE

An access pause code is stored in the RAM automatically during original entry. When M1 goes LOW after all digits so far entered have been transmitted (see Fig. 5). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is awaited. An access pause code can be stored in this way after any digit. The maximum number of automatic access pause codes that can be stored is limited to two, one or no pause depending on the state of input NAP:

NAP = V_{SS}: no pause
NAP = not connected: 2 pauses
NAP = V_{DD}: one pause

During the redial sequence the access pauses will be automatically regenerated. When an access pause code is read from the RAM, the normal inter-digit pause with a duration t_{ID} is extended by an access pause. There are three methods of terminating a regenerated access pause:

- automatically, if the built-in time t_{AP} expires.
- manually be pressing any key before t_{AP} expires.
- with an external tone recognizer by switching NAP to V_{SS} for shortening an access pause.

The built-in time t_{AP} for automatic termination of the access pause can be set to one of two values with the APD select input (see timing characteristics).

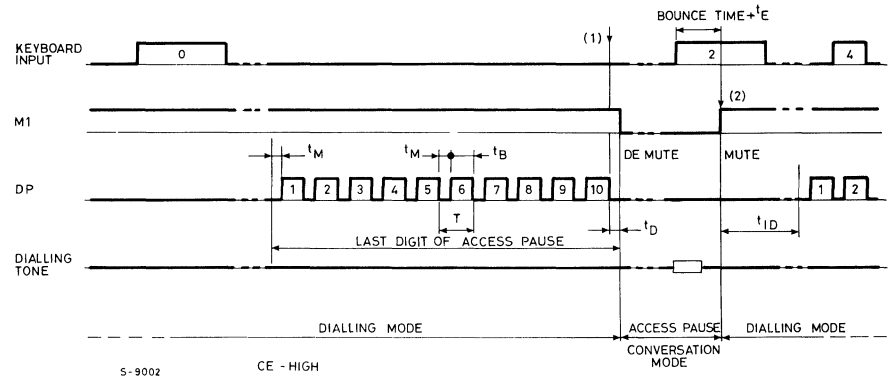
MANUAL PAUSE

Access pause codes can be stored in the RAM at appropriate positions by pressing the access pause key (* key). They can be stored in addition to automatic pause codes. A manual pause code can be stored after any digit. The maximum number of manual pause codes is not limited. The storage of two consecutive manual pause codes is inhibited.

During the redial sequence the manually stored pause codes will automatically generate pause. The duration of the manual pause is unlimited. Whenever a manual pause code is read from the RAM, the normal inter-digit pause is extended until it is terminated by one of two methods:

- manually by pressing any key;
- with an external tone recognizer by switching NAP to V_{SS}

Fig. 7 - Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.



(1) If there are no further key entries before this instant, M1 goes LOW after t_d and an access pause keycode is written into the RAM.
(2) Dialling sequence restarts when another key is pressed.

SUMMARY OF SPECIAL KEYBOARD FUNCTIONS

Key * : Inserts a manual pause code, if activated after a number key.

Key # : Starts the redial sequence, if activated as first key.

Any key: Terminates an automatic or a manual pause if activated during the pause.

STATIC STANDBY OPERATION

CE = LOW turns off the oscillator and resets all internal registers with the exception of the WRITE ADDRESS COUNTER and the RAM. All input pull-up and pull-down devices are switched off. The current consumption is reduced in this conditions such that the supply voltage required to hold the data stored in the RAM can be provided by a capacitor. Data retention of 45 minutes is possible with a capacitor of 2.200μF, it is supplies an initial V_{DD} of 3.5V.

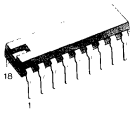
A power-on-reset circuit triggering on the rising slope of V_{DD} ensures that the redial function is inhibited after the supply voltage had decayed to a value at which data retention in the RAM could not be guaranteed any more.

M3327

ADVANCE DATA

CMOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

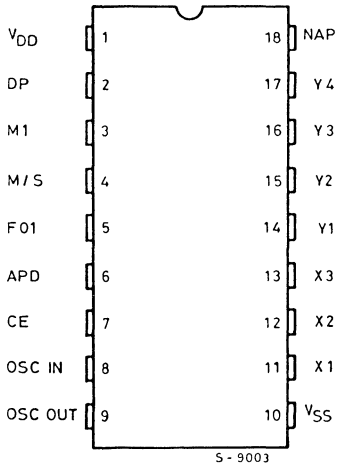
- OPERATION FROM 2.5V TO 6V SUPPLY
- STATIC STANDBY OPERATION DOWN TO 1.8V
- LOW CURRENT CONSUMPTION; TYP. 40μA
- LOW STATIC STANDBY CURRENT; TYP. 1μA
- ON-CHIP OSCILLATOR FOR 455KHz RESONATOR
- LAST NUMBER REDIAL FUNCTION
- 23-DIGIT CAPACITY, INCLUDING ACCESS PAUSES
- DIALLING PULSE FREQUENCY SELECTABLE: 10Hz, 20Hz OR 932Hz
- DIALLING PULSE MARK/SPACE RATIO SELECTABLE: 1.5:1 OR 2:1
- CIRCUIT RESET FOR LINE POWER BREAKS GREATER THAN 270ms.
- ACCESS PAUSE GENERATION AUTOMATICALLY OR VIA THE KEYBORAD
- ACCESS PAUSE RESET: AUTOMATICALLY, VIA THE KEYBOARD, WITH EXTERNAL TONE RECOGNISER
- MAXIMUM DURATION OF ACCESS PAUSE SELECTABLE: 2.7s, 5.5s OR INFINITE
- MAXIMUM NUMBER OF ACCESS PAUSES SELECTABLE: 0, 1 OR 2
- ALL INPUTS WITH PULL-UP/PULL-DOWN (EXCEPT CE AND OSC IN)



B
DIP-18 Plastic (0.25)

ORDERING NUMBER: M3327 B1

PIN CONFIGURATION



S-9003

DESCRIPTION

The M3327 is a single chip silicon-gate CMOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3x4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. Access pauses can be stored automatically or via the keyboard.

The M3327 is available in 18 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

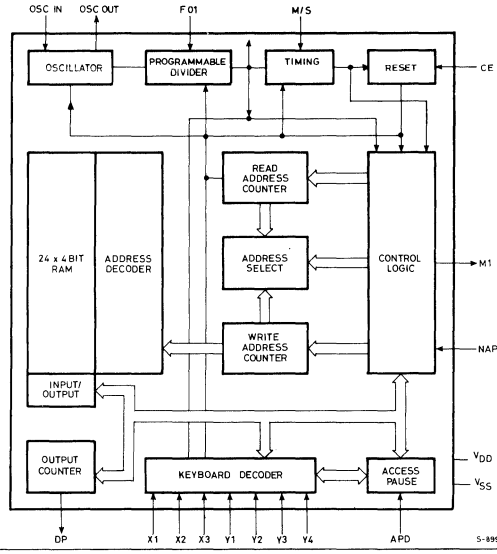
V_{DD}	Supply voltage	-0.3 to 8	V
V_I	Voltage on any pin	V_{SS} -0.3 to V_{DD} +0.3	V
T_{op}	Operating temperature range	-25 to +70	°C
T_{stg}	Storage temperature range	-55 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stresses ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions to extended periods may be affect device reliability.

PIN DESCRIPTION

Symbol	Function
SUPPLY	
V_{DD}	Positive supply.
V_{SS}	Negative supply.
INPUTS	
APD	Access Pause Delay; selects the maximum duration of an access pulse.
NAP	Number of Access Pauses; senses three input states: V_{DD}, $V_{DD/2}$, V_{SS}; limits the number of automatically stored access pauses to 0, 1 or 2; if switched to V_{SS} it terminates an automatic or manual access pause
M/S	Controls the mark-to-space ratio of the line pulses.
F01	Test input; used to speed up all frequencies and timing signals.
CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
X1, X2, X3	Column keyboard inputs with pull-down or chip.
Y1, Y2, Y3, Y4	Row keyboard inputs with pull-up on chip.
OUTPUTS	
DP	Dialling Pulse; drive of the external line switching transistor or relay.
M1	Muting; used for muting during the dialling sequence.
OSCILLATOR PINS	
OSC IN	Input of the on-chip oscillator.
OSC OUT	Output of the on-chip oscillator.

Fig. 1 - Block Diagram



TIMING CHARACTERISTICS (V_{DD} = 2.5 to 6V; V_{SS} = 0; f_{osc} = 455KHz)

Symbol	Parameter		Conditions (note 3)	F01 = V_{SS}	F01 = NC	F01 = V_{DD}	Unit
f_{DP}	Dialling pulse frequency	$1/T_{DP}$		9.874	19.748	947.9	Hz
T_{DP}	Dialling pulse period	$1/f_{DP}$		101.28	50.64	1.055	ms
f_{CL}	Clock pulse frequency	$30 \times f_{DP}$		296.22	592.44	28437	Hz
t_B	Break time (note 1)	$2/3 \times T_{DP}$	M/S = V_{SS}	67.52	33.76	0.703	ms
t_M	Make time (note 1)	$1/3 \times T_{DP}$	M/S = V_{SS}	33.76	16.88	0.352	ms
t_B	Break time (note 2)	$3/5 \times T_{DP}$	M/S = NC	60.77	30.38	0.633	ms
t_M	Make time (note 2)	$2/5 \times T_{DP}$	M/S = NC	40.51	20.26	0.422	ms
t_{ID}	Inter digit pause	$8 \times T_{DP} + t_M$		844	422	8.79	ms
t_{RD}	Reset delay time	$8/3 \times T_{DP}$		270.1	135	2.82	ms
t_{AP}	Access pause time	$27 \times T_{DP} \times t_M$	A_{PD} = V_{SS}	2.768	1.384	0.028	s
t_{AP}	Access pause time	$54 \times T_{DP} + t_M$	A_{PD} = NC	5.503	2.751	0.057	s
t_{AP}	Access pause time	∞	A_{PD} = V_{DD}	∞	∞	∞	s
t_D	Delay last digit last pulse to M1	$1/3 \times T_{DP}$		33.76	16.88	0.352	ms
	Debounce time:						
$t_{E\ min}$	Min.	$4/30 \times T_{DP}$		13.5	6.75	0.141	ms
$t_{E\ max}$	Max.	$1/6 \times T_{DP}$		16.88	8.44	0.176	ms
$t_{ON\ Typ.}$	Clock start-up-time		(note 4)	4	4	4	ms
t_I	Initial data entry time (Typ.)	$t_{ON} + t_E$		19	11	4	ms

NOTES: 1. Mark-to-space ratio = 2:1
2. Mark-to-space ratio = 1.5:1
3. In the NC (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/ pull-down current.
4. After CE: $V_{SS} \rightarrow V_{DD}$. Stray capacitance between pins 8 and 9 < 3pF.

ELECTRICAL CHARACTERISTICS (V_{DD} = 3V; V_{SS} = 0; resonator parameters, f_{osc} = 455KHz, (note 3); T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating supply voltage	T_{amb} = -25 to +70°C	2.5	3	6	V
V_{DDO}	Standby supply voltage (note 1)	T_{amb} = -25 to +70°C	1.8		6	V
I_{DD}	Operating supply current	CE = V_{DD}; notes 2, 3		40		μA
		CE = V_{DD}; V_{DD} = 6V; notes 2, 3		50	100	
I_{DDO}	Standby supply current	CE = V_{SS} note 2 V_{DD} = 1.8V T_{amb} = -25 to +70°C		1	2 2	μA
V_{IL}	Input voltage LOW	1.8V ≤ V_{DD} ≤ 6V			0.3 V_{DD}	
V_{IH}	Input voltage HIGH	1.8V ≤ V_{DD} ≤ 6V	0.7 V_{DD}			
I_{IL}	Input leakage current; CE LOW	CE = V_{SS}			50	nA
I_{IH}	HIGH	CE = V_{DD}			50	nA
I_{IL}	Pull-up input current M/S F01, APD, NAP	V_I = V_{SS} CE = 1	30 1.5	100 3	300 6	nA μA
I_{IH}	Pull-down input current F01, APD, NAP	V_I = V_{DD} CE = 1	1.5	3	6	μA

MATRIX KEYBOARD OPERATION

I_K	Keyboard current	X connected to Y CE = V_{DD}		10		μA
R_{KON}	Keyboard "ON" resistance	contact ON; note 4			500	Ω
R_{KOFF}	Keyboard "OFF" resistance	contact OFF; note 4	1			MΩ

OTHER KEYBOARD OPERATION

I_{IH}	Input current for X_n "ON"	V_I = 1.5 to 3V			30	μA
I_{IL}	Input current for Y_n "OFF"	V_I = 0 to 2.5V	10			μA
I_I	Input current Y_n	V_I = V_{SS}			0.7	mA
I_{OL}	MI, DP Output Sink current	V_{OL} = 0.5V	0.7	1.5	3.2	mA
I_{OH}	Source current	V_{OH} = 2.5V	0.65	1.3	2.7	mA

NOTES:
1. V_{DDO} = 1.8V only for redial
2. All other inputs and outputs open
3. Stray capacitance between pins 8 and 9 < 3pF
4. Guarantees correct keyboard operation

FUNCTIONAL DESCRIPTION

CLOCK OSCILLATOR

The time base for the M3327 is an on-chip oscillator which is completed only by connecting a ceramic resonator between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01) to provide the normal clock frequency or the higher test frequency. Alternatively, the OSC IN input may be driven from an external clock signal.

CHIP ENABLE (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{RD} (see Fig. 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{RD} period. The system is then in the static standby mode. Short CE pulses of less than t_{RD} will not affect the operation of the circuit. No reset pulses are then produced.

DEBOUNCING KEYBOARD ENTRIES

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3x4 single contact keyboard matrix (with or without common contact) as shown (in Fig. 2, or to a double contacts keyboard with a common left open (see Fig. 3). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted.

Valid inputs are debounced on the leading and trailing edges as shown in Fig. 4. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_E). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Fig. 2 - Single Contact Keyboard

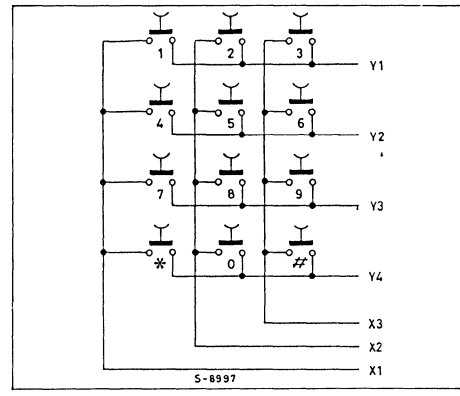
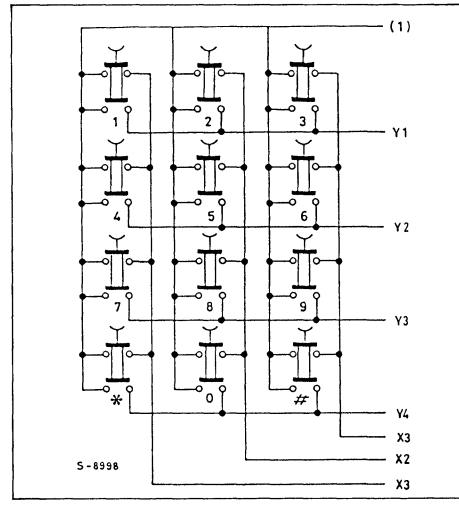


Fig. 3 - Double Contact Keyboard



* Access pause set # Redial

FUNCTIONAL DESCRIPTION (continued)

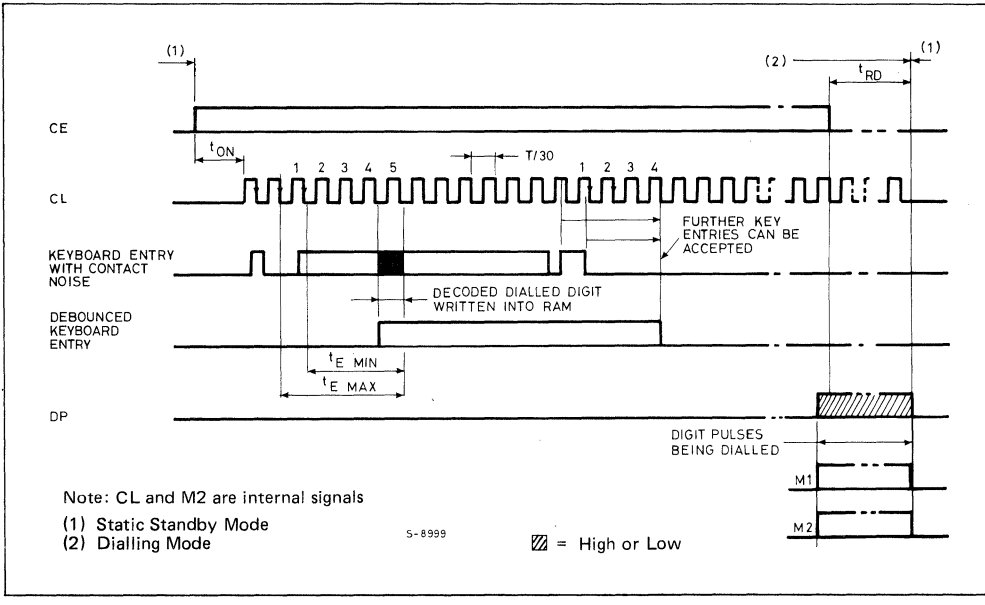
DATA STORAGE AND DATA RETRIEVAL
After each keyboard entry has been debounced and decoded, the keycode is written into the RAM and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM, but not yet converted into line pulses.

If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycodes replace the data in the lower numbered RAM locations. In this event, since an erroneaus number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not Redial (#), the WAC is reset during entry time t_E, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one to select the next RAM location. Consequently, if the first pushbutton pressed is not redial, the data stored previously in the RAM cannot be redialled any more.

If the first pushbutton is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP.
If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the M3327. During redial no keyboard entry will be accepted and stored in the RAM. But, when all numbers stored in the RAM have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.

Fig. 4 - Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.



FUNCTIONAL DESCRIPTION (continued)

DIALLING SEQUENCE

The dialling sequence can be initiated under either of the following two conditions:

– The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 5.

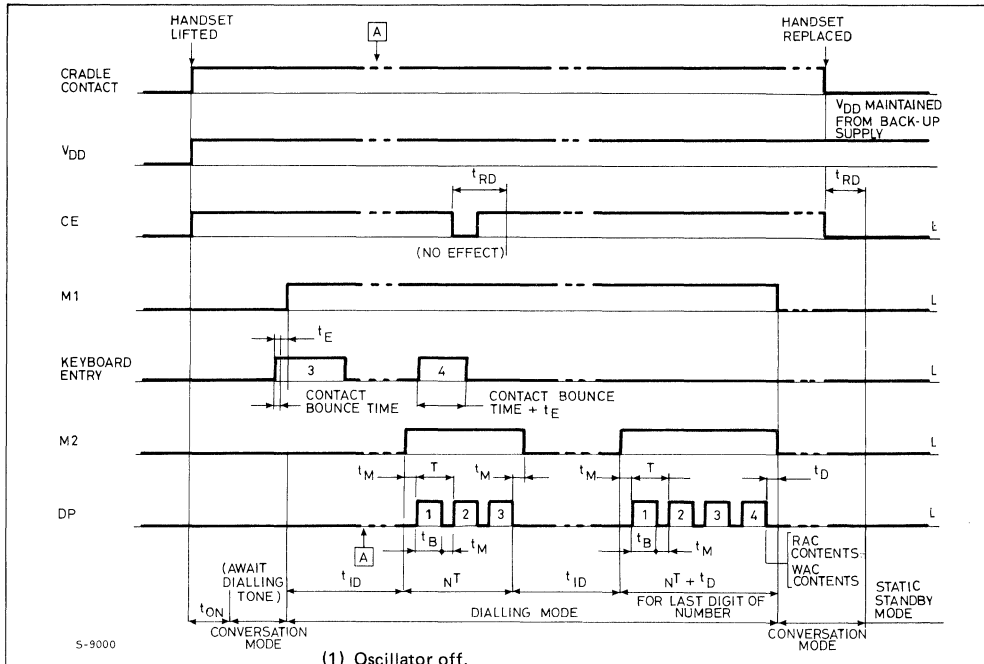
Then approximately 4ms (t_{ON}) after CE goes HIGH, the clock pulse generator starts and the circuit is in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_E commences.

– The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact. (Fig. 6).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4ms (t_{ON}) after CE goes HIGH, the clock pulse generator starts and data entry period t_E commences. After period t_E, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 5. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{ID}) ensured. M2 then goes HIGH (M2 is an internally generated signal used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the

Fig. 5 - Timing diagram of dialling sequence with V_{DD} and CE = HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.



(1) Oscillator off.
All registers except WAC reset.
Keyboard input inhibited.
Number stored in RAM until $V_{DD} < 1.8V$.

FUNCTIONAL DESCRIPTION (continued)

output counter which generates the appropriate number of correctly timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out).

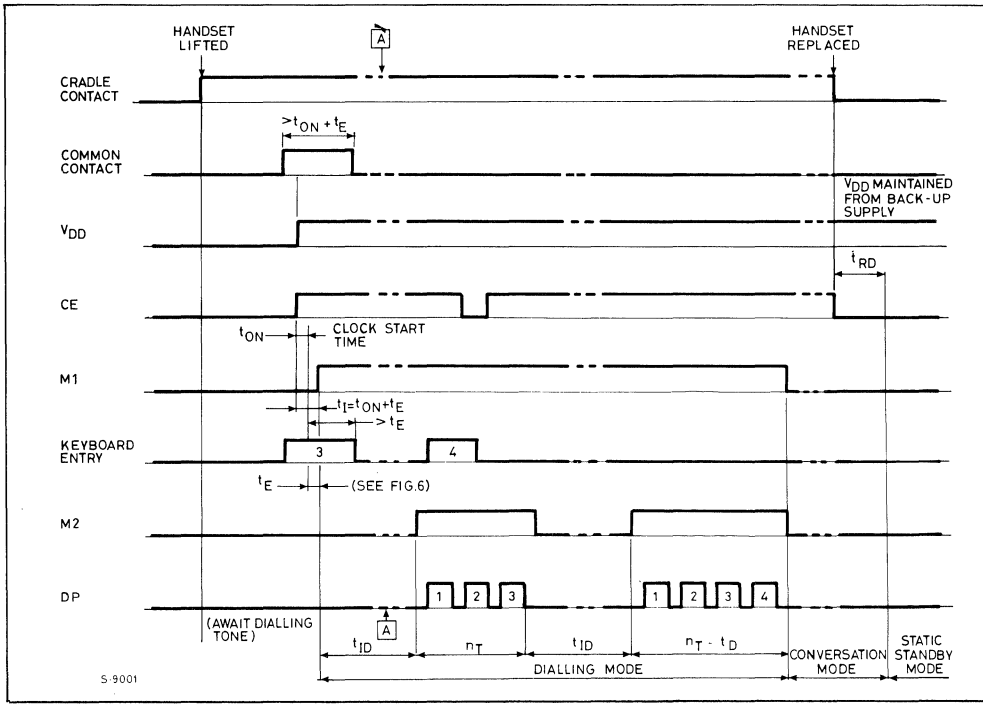
Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more then the reset delay time t_{RD} at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolated CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1.8V.

STORAGE AND REGENERATION OF ACCESS PAUSES

A dial sequence may require an extended inter-digit pause, if a dial tone has to be awaited. During the keyboard entry, whenever an access pause, is needed a pause code can be stored in the RAM either automatically or via the key-board for the later redial sequence. When an access pause is regenerated during radialling it can be terminated either automatically after a built-in delay time or via the keyboard or with an external dial tone recognizer circuit.

A pause code takes one position in the RAM like a digit. The number of digits plus the number of access pauses can therefore be up to 23.

Fig. 6 - Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard.
See Fig. 6 for pulse timings after point A. M2 is an internal signal.



FUNCTIONAL DESCRIPTION (continued)

AUTOMATIC PAUSE

An access pause code is stored in the RAM automatically during original entry, when M1 goes LOW after all digits so far entered have been transmitted (see Fig. 5). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is awaited. An access pause code can be stored in this way after any ditit. The maximum number of automatic access pause codes that can be stored is limited to two, one or no pause depending on the state of input NAP:

NAP = V_{SS} : no pause
NAP = not connected: 2 pauses
NAP = V_{DD} : one pause

During the redial sequence the access pauses will be automatically regenerated. When an access pause code is read from the RAM, the normal inter-digit pause with a duration t_{ID} is extended by an access pause. There are three methods of terminating a regenerated access pause:

- automatically, if the built-in time t_{AP} expires.
- manually by pressing any key before t_{AP} expires.
- with an external tone recognizer by switching NAP to V_{SS} for shortening an access pause.

The built-in time t_{AP} for automatic termination of the access pause can be set to one of two values with the APD select input (see timing characteristics).

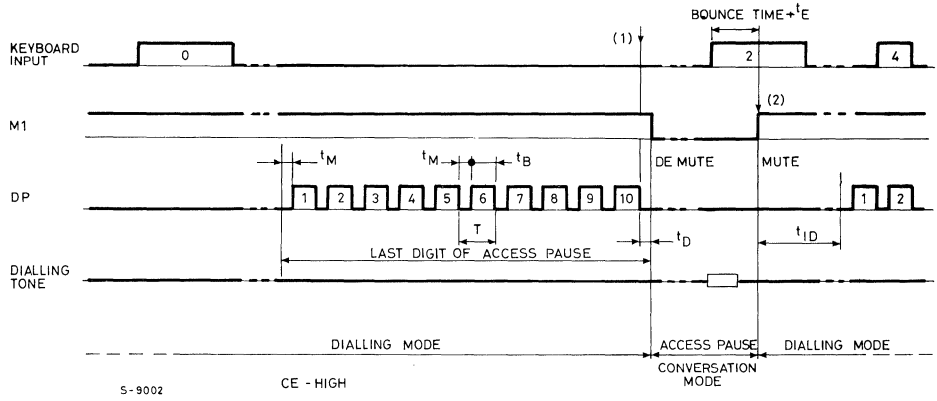
MANUAL PAUSE

Access pause codes can be stored in the RAM at appropriate positions by pressing the access pause key (* key). They can be stored in addition to automatic pause codes. A manual pause code can be stored after any digit. The maximum number of manual pause codes is not limited. Consecutive manual pause codes will generate a single during redial.

During the redial sequence the manually stored pause codes will automatically generate pauses. The duration of the manual pause is unlimited. Whenever a manual pause code is read from the RAM, the normal inter-digit pause is extended until it is teminated by one of two methods:

- manually by pressing any key
- with an external tone recognizer by a negative transition at NAP (n.c. → V_{SS} or V_{DD} → V_{SS}).

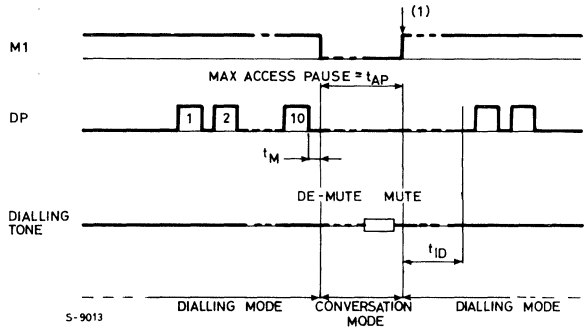
Fig. 7 - Dialling sequence showing how an access pause code si automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.



(1) If there are no further key entries before this instant. M1 goes LOW after t_D and an access pause keycode is written into the RAM.
(2) Dialling sequence restarts when another key is pressed.

FUNCTIONAL DESCRIPTION (continued)

Fig. 8 - Timing diagram showing Access Pause Reset



(1) An automatic access pause:
- expires after t_{AP}
- can be terminated by pressing any key before end of t_{AP}
- can be terminated by switching NAP to V_{SS} before end of t_{AP}

A manual access pause
- can be terminated by pressing any key
- can be terminated by switching NAP to V_{SS}

SUMMARY OF SPECIAL KEYBOARD FUNCTIONAL

Key * : Inserts a manual pause code, if activated after a number key.

Key # : Starts the redial sequence, if activated as first key.

Any key : Terminates an automatic or a manual pause if activated during the pause.

STATIC STANDBY OPERATION

CE = LOW turns off the oscillator and resets all internal registers with the exception of the WRITE ADDRESS COUNTER and the RAM.

All input pull-up and pull-down devices are switched off. The current consumption is reduced in this condition such that the supply voltage required to hold the data stored in the RAM can be provided by a capacitor. Data retention of 45 minutes is possible with a capacitor of 2.200μF, if it supplies an initial V_{DD} of 3.5V.

A power-on-reset circuit triggering on the rising slope of V_{DD} ensures that the redial function is inhibited after the supply voltage had decayed to a value at which data retention in the RAM could not be guaranteed any more.

Fig. 9 - Pull-down input current versus input voltage at V_{DD} = 3V (Input M/S, F01)

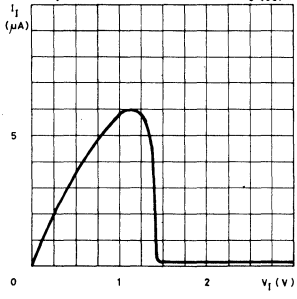


Fig. 10 - Pull-down input current versus supply voltage at $V_I = V_{DD}$, CE = V_{DD} (Input M/S, F01)

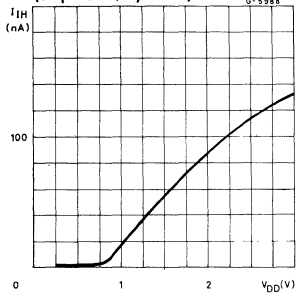


Fig. 11 - Pull-up input current versus input voltage at V_{DD} = 3V (Input APD)

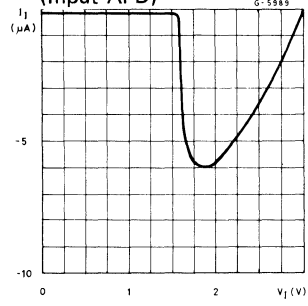


Fig. 12 - Pull-up input current versus supply voltage at $V_{DD} = 3V$, $CE = V_{DD}$ (Input APD)

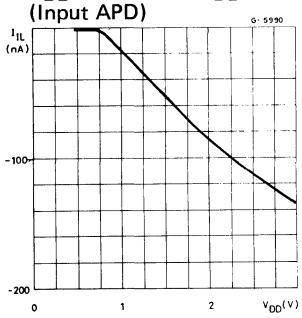


Fig. 13 - Input characteristics for NAP at $V_{DD} = 3V$, $CE = V_{DD}$

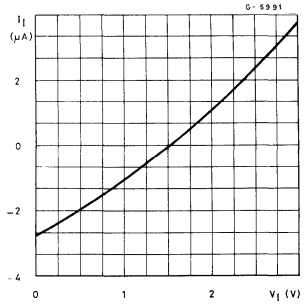


Fig. 14 - Keyboard input characteristics at $CE = V_{DD}$

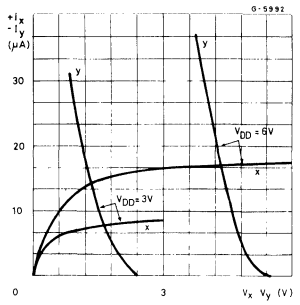
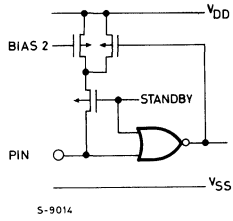
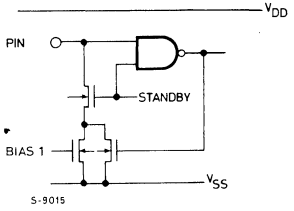


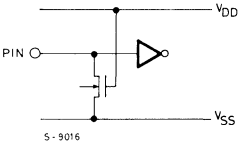
Fig. 15 - Internal input and output configurations. The schematics show the principle of the circuitry. The integrated protection devices are not shown here.
During STANDBY = 1, BIAS1 is switched to V_{SS} and BIAS2 to V_{DD}



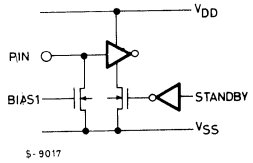
Input APD



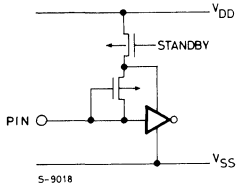
Input M/S



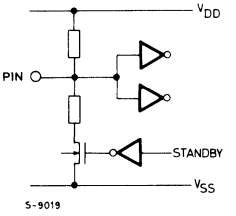
Input F01



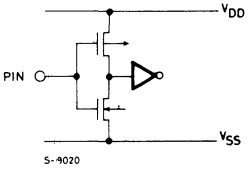
Input X_n



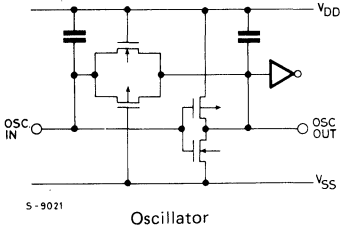
Input Y_n



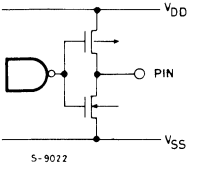
Input NAP



Input CE



Oscillator

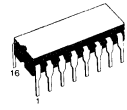


Output DP, M1

M5116

μ-255 LAW COMPANDING CODEC

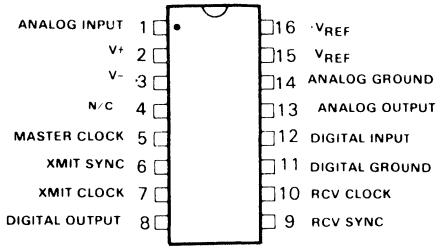
- ± 5V POWER SUPPLY
- LOW POWER DISSIPATION -30mW (TYP.)
- FOLLOWS THE μ-255 LAW COMPANDING CODE
- EXCEEDS D3 CHANNEL BANK TRANSMISSION SPECIFICATIONS
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TIMMING
- SINGLE 16-PIN PACKAGE
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64Kb/s - 2.1 Mb/s AT 8KHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDING PINS REDUCE SYSTEM NOISE PROBLEMS



DIP-16 F Ceramic Frit-seal

ORDERING NUMBERS: M5116 F1

PIN CONFIGURATION



DESCRIPTION

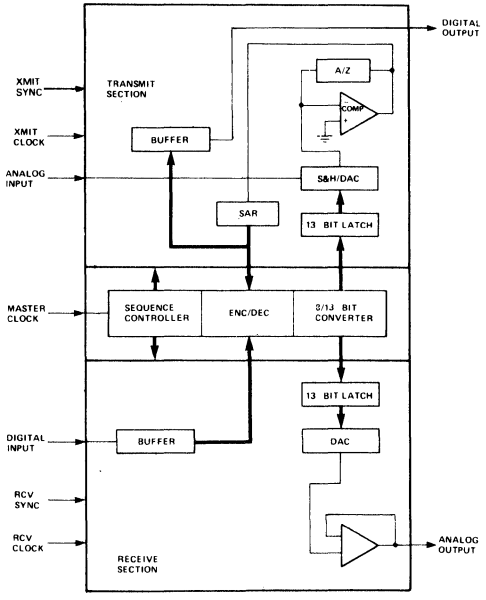
The M5116 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which ahs a transfer characteristic conforming to the μ-255 law companding code and (2) a digital-to-analog converter which also conforms to the μ-255 law code. These two sections form a coder-decoder which is designed to meed the needs of the telecommunications industry for per-channel voice-frequency codecs used in D3 channel bank and PBX systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64KB/s-2.1MB/s rate with analog signal sampling occurring at an 8KHz rate. A sync pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

ABSOLUTE MAXIMUM RATINGS

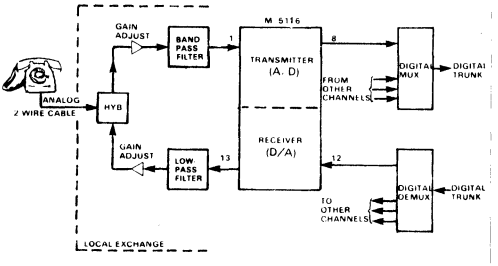
Parameter	Value	Unit
DC Supply Voltage, V+	+ 6	V
DC Supply Voltage, V-	- 6	V
Operating Temperature range	0 to 70	°C
Storage Temperature range	-55 to +125	°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5 \leqslant V_{IN} \leqslant V+$	V
Analog Input	$V- \leqslant V_{IN} \leqslant V+$	V
$+V_{REF}$	$-0.5 \leqslant +V_{REF} \leqslant V+$	V
$-V_{REF}$	$V- \leqslant -V_{REF} \leqslant +0.5$	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permenent damaged to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PCM SYSTEM



POWER SUPPLY REQUIREMENTS

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V-	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

DC CHARACTERISTICS (Test conditions: V+= 5.0V, V-= -5.0V, $+V_{REF}$= 2.5V, $-V_{REF}$= -2.5V)

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	
$V_{OFFSET/I}$	Analog Input Offset Voltage		± 1	± 8	mV	
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$(V_{OFFSET/O})$	Analog Output Offset Voltage		-200	±850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN}= 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN}= 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	± 10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I-	Negative Supply Current		2	6	mA	
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 3 and Figure 4)

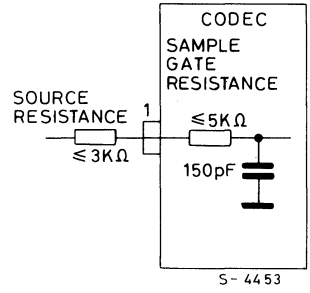
Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of $t_{FC}(t_{RS})$			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay		200		ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50		ns	4
t_{DOR}	Digital Output Rise Time		50		ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of $t_{RC}(t_{FS})$			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	5
t_{RDH}	RCV. Data Hold Time	200			ns	5
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	5
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW-	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 10 and 11)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
S/D	Signal-to-Distortion Ratio	Analog Input = 0 to -30 dBmO Analog Input = -40 dBmO Analog Input = -45 dmO	35 29 24	39 34 29		dB dB dB
GT	Gain Tracking	Analog Input = +3 to -37 dBmO Analog Input = -37 to -50 dBmO Analog Input = -50 to -55 dBmO	-0.4 -0.8 -2.5	± 0.1 ± 0.1 ± 0.2	+0.4 +0.8 +2.5	dB dB dB
N_{IC}	Idle Channel Noise	Analog Input = 0 Volts		10	18	dBrncO
TLP	Transmission Level Point	600 Ω		+4		dB

Notes:
1. $+V_{REF}$ and $-V_{REF}$ must be matched with in ±1% in order to meet system requirements.
2. Sampling is accomplished by changing the internal capacitor to within ½ LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown on the right.
3. The M5116 will I source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with I_{OH}= -100 μA, I_{OL}= 500 μA.
5. The first bit of data is loaded when Sync. and Clock are both "1" during bit time 1 as shown on RCV, timing diagram.
6. This delay is necessary to avoid overlapping Clock and Sync.

EQUIVALENT INPUT RESISTANCE CIRCUIT DURING SAMPLING



FUNCTIONAL DESCRIPTION

Pin 1 – Analog Input

Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to Figure 1). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion.

Pin 5 – Master Clock

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV, CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

FUNCTIONAL DESCRIPTION (continued)

Fig. 1 - A/D, D/A conversion timing

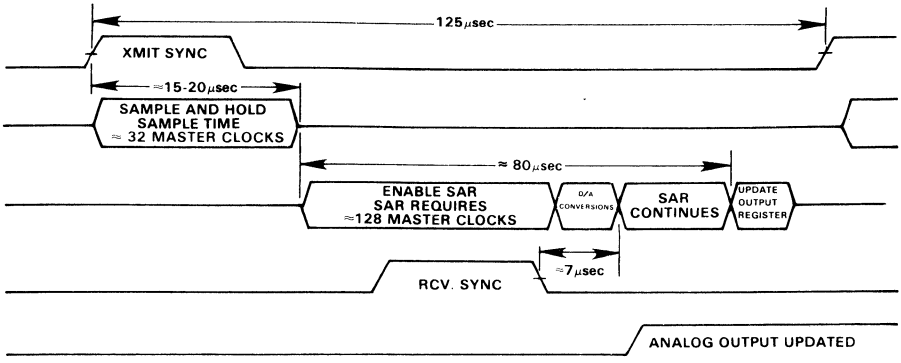
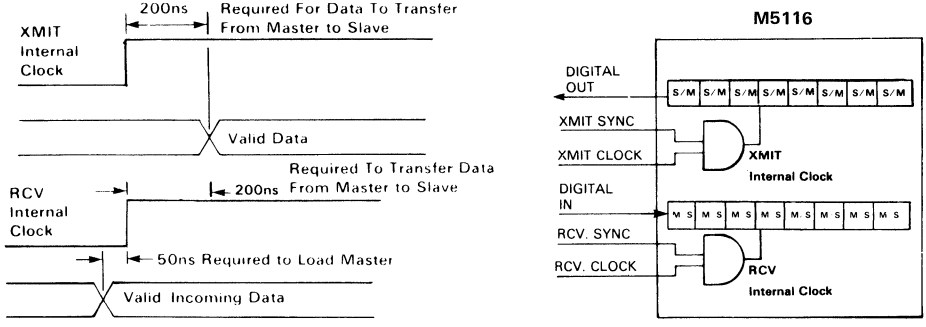


Fig. 2 - Data input/output timing

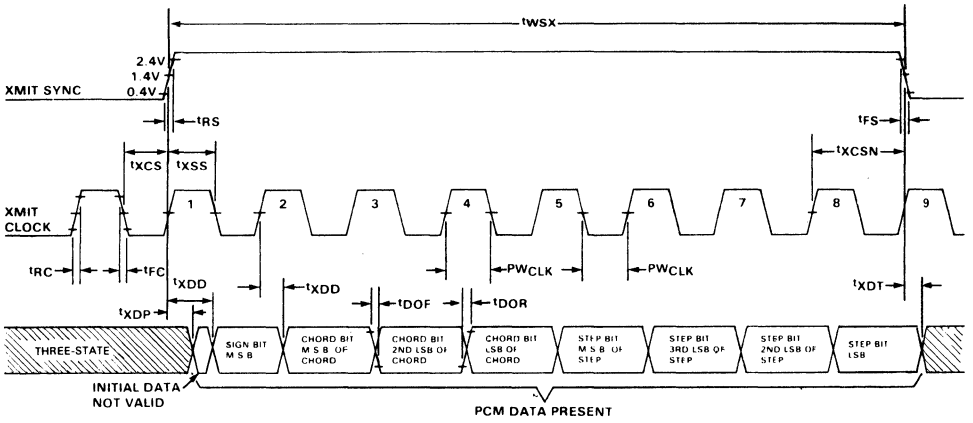


Pin 6 — XMIT SYNC (Refer to Figure 3 for the Timing Diagram)
This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word (Refer to Figure 7).

Pin 7 — XMIT CLOCK (Refer to Figure 3 for the Timing Diagram)
The on-chip 8-bit output shift register of the M5116 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 2). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

FUNCTIONAL DESCRIPTION (continued)

Fig. 3 - Transmitter section timing



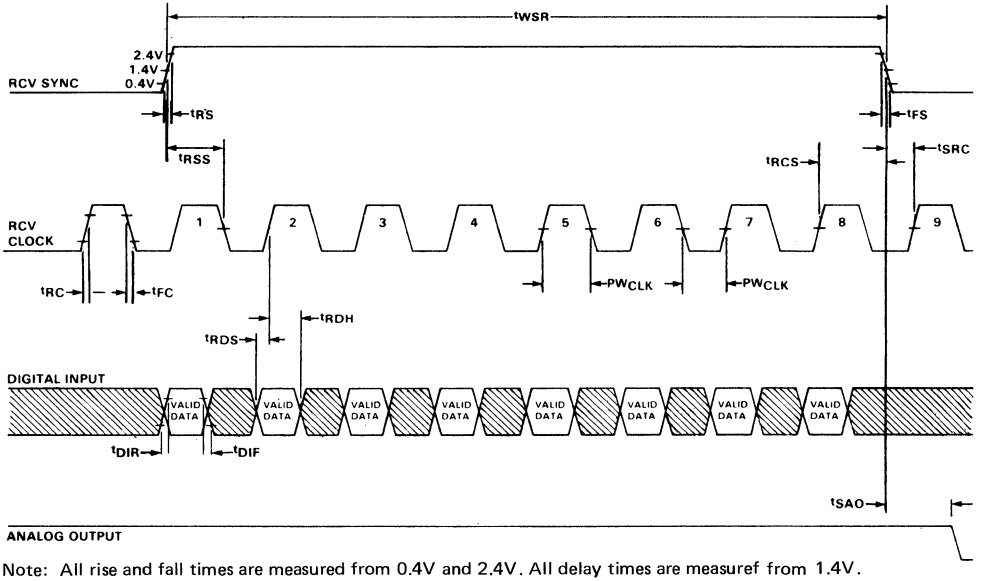
Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Pin 9 — RCV. SYNC (Refer to Figure 4 for the Timing Diagram)
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC. pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 1). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 8).

Pin 10 — RCV. CLOCK (Refer to Figure 4 for the Timing Diagram)
The on-chip 8-bit shift register for the M5116 is loaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 2). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - Receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measuref from 1.4V.

Fig. 5 - A/D converter (μ-Law Encoder) transfer characteristic

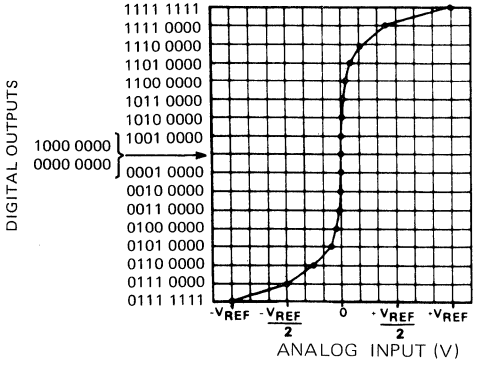
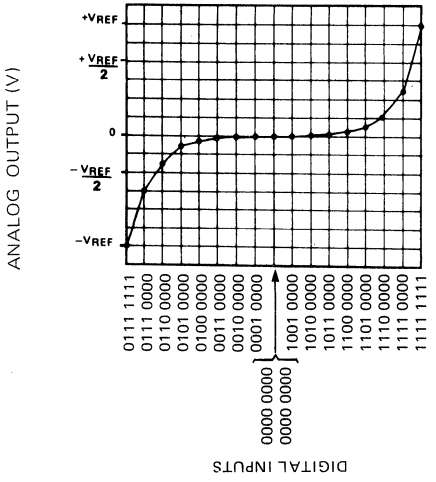


Fig. 6 - D/A converter (μ-Law Decoder) transfer characteristic



FUNCTIONAL DESCRIPTION (continued)

Table 1 - Digital output code: μ-Law

Chord Code	Chord Value	Step Value
1. 000	0.0 mV	0.613 mV
2. 001	10.11 mV	1.226 mV
3. 010	30.3 mV	2.45 mV
4. 011	70.8 mV	4.90 mV
5. 100	151.7 mV	9.81 mV
6. 101	313 mV	19.61 mV
7. 110	637 mV	39.2 mV
8. 111	1.284 mV	78.4 mV

EXAMPLE:

1 011 0010=+70.8 mV+(2x4.90 mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

Pin 8 — Digital Output

The M5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6 mV. In the second Chord, the Stem Bit has a value of 1.2 mV. This doubling of the step value continues for each of the six successive Chords. Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (**Refer to Table 1**). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder)is shown in Figure 5.

Pin 12 — Digital Input

The M5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 4. When RCV. SYNC goes high, the M5116 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 6.

Pin 13 — Analog Output

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

Pins 16 and 15 — Positive and negative reference voltages ($+V_{REF}$ and $-V_{REF}$)

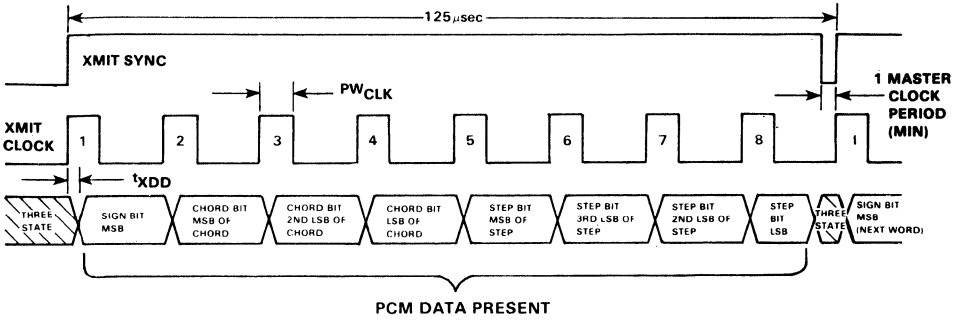
These inputs provide the conversion references for the digital-to-analog converters in the M5116. $+V_{REF}$ and $-V_{REF}$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

OPERATION OF DECODEC WITH 64 kHz XMIT/RCV.

Clock Frequencies

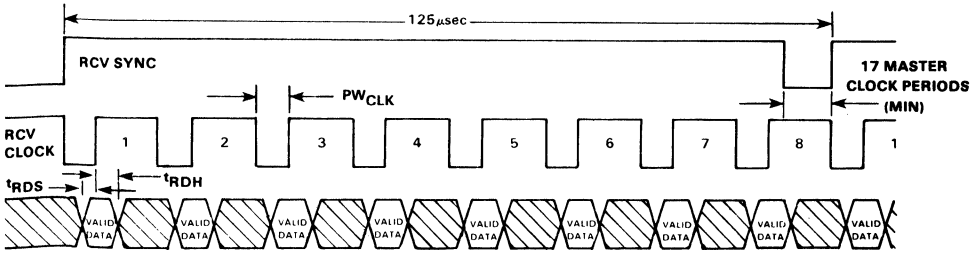
XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figs. 7 and 8).

Fig. 7 - 64 kHz operation, transmitter section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V

Fig. 8 - 64 kHz operation, receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Offset Null

The offset null feature of the M5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

Performance Evaluation

The equipment connections shown in Figure 9 can be used to evaluate the performance of the M5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the M5116. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the M5156 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC.
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.544 MHz.
(2) XMIT SYNC repetition rate = 8 kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods.

When all the above requirements are met, the setup of Figure 9 permits the measurement of synchronous system performance over a wide range of analog inputs.
The data register and ideal decoder provide a means of checking the encoder portion of the M5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the M5116 are shown in Figs. 10 and 11.

Fig. 9 - System characteristics test configuration

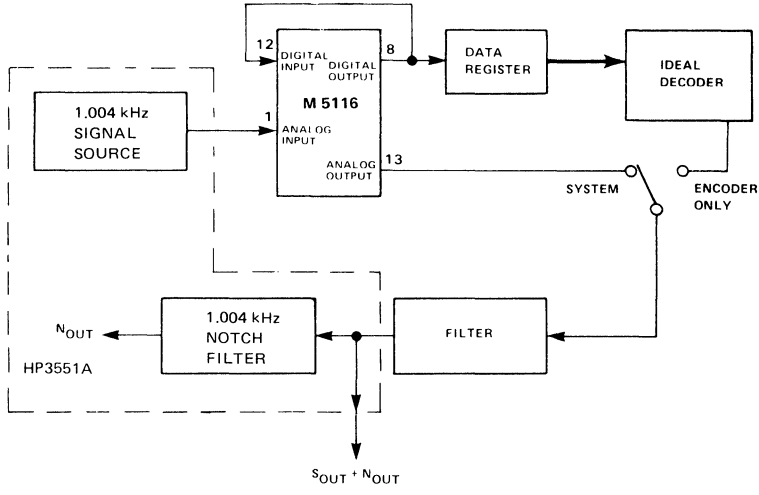


Fig. 10 - S/D ratio vs. input level

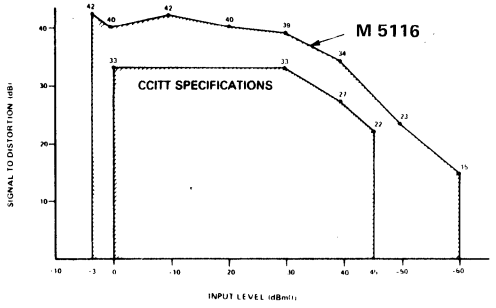
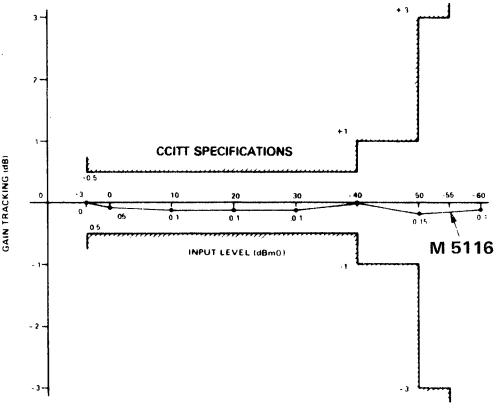


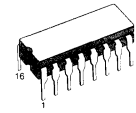
Fig. 11 - Gain tracking performance



M5156

A-LAW COMPANDING CODEC

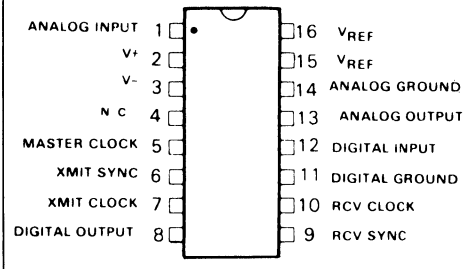
- ± 5V POWER SUPPLY
- LOW POWER DISSIPATION -30mW (TYP.)
- FOLLOWS THE A-LAW COMPANDING CODE
- EXCEEDS CCITT SPECIFICATIONS, INCLUDES EVEN-ORDER-BIT INVERSION
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- SINGLE 16-PIN PACKAGE
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64KB/s-2.1 Mb/s AT 8KHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDING PINS REDUCE SYSTEM NOISE PROBLEMS



DIP-16 F Ceramic Frit-seal

ORDERING NUMBER: M5156 F1

PIN CONFIGURATION



DESCRIPTION

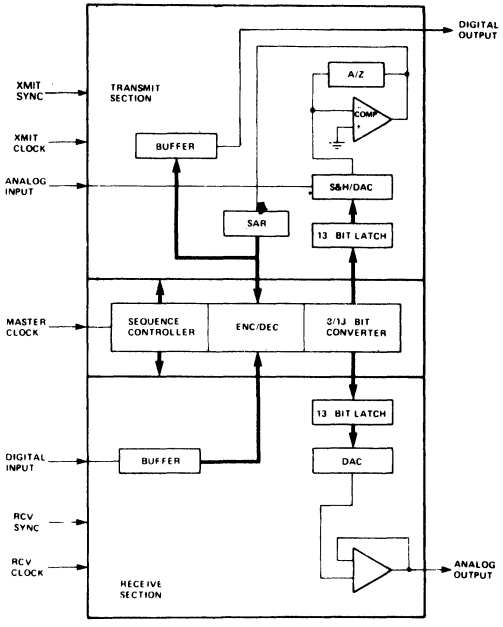
The M5156 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristics conforming to the A-law companding code and (2) a digital-to-analog converter which also conforms to the A-law code. These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64Kb/s-2.1Mb/s rate with analog signal sampling occurring at an 8KHz rate.
A sync pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

ABSOLUTE MAXIMUM RATINGS

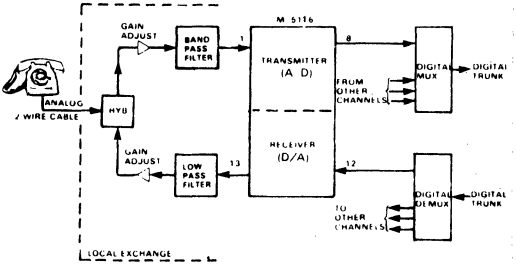
Parameter	Value	Unit
DC Supply Voltage, V+	+ 6	V
DC Supply Voltage, V-	- 6	V
Operating Temperature range	0 to 70	°C
Storage Temperature range	-55 to +125	°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5 \leqslant V_{IN} \leqslant V+$	V
Analog Input	$V- \leqslant V_{IN} \leqslant V+$	V
$+V_{REF}$	$-0.5 \leqslant +V_{REF} \leqslant V+$	V
$-V_{REF}$	$V- \leqslant -V_{REF} \leqslant +0.5$	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permenent damaged to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



PCM SYSTEM



POWER SUPPLY REQUIREMENTS

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V-	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

DC CHARACTERISTICS (Test conditions: V+ = 5.0V, V- = -5.0V, $+V_{REF}$ = 2.5V, $-V_{REF}$ = -2.5V)

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	
$V_{OFFSET/I}$	Analog Input Offset Voltage		± 1	± 8	mV	
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$(V_{OFFSET/O})$	Analog Output Offset Voltage		-200	±850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN}= 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN}= 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	± 10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I-	Negative Supply Current		2	6	mA	
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 3 and Figure 4)

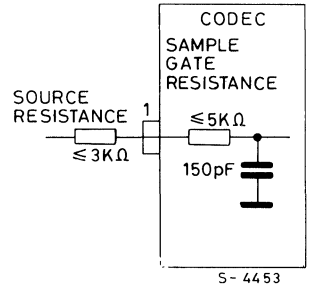
Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of $t_{FC}(t_{RS})$			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay		200		ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50		ns	4
t_{DOR}	Digital Output Rise Time		50		ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of $t_{RC}(t_{FS})$			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	5
t_{RDH}	RCV. Data Hold Time	200			ns	5
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	5
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		$V/\mu s$	
SLEW-	Analog Output Negative Slew Rate		1		$V/\mu s$	
DROOP	Analog Output Droop Rate		25		$\mu V/\mu s$	

SYSTEM CHARACTERISTICS (Refer to Figures 10 and 11)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
S/D	Signal-to-Distortion Ratio	Analog Input = 0 to -30 dBmO Analog Input = -40 dBmO Analog Input = -45 dmO	35 29 24	39 34 29		dB dB dB
GT	Gain Tracking	Analog Input = +3 to -37 dBmO Analog Input = -37 to -50 dBmO Analog Input = -50 to -55 dBmO	-0.4 -0.8 -2.5	± 0.1 ± 0.1 ± 0.2	+0.4 +0.8 +2.5	dB dB dB
N_{IC}	Idle Channel Noise	Analog Input = 0 Volts		-80	--72	dBmOp
TLP	Transmission Level Point	600 Ω		+4		dB

Notes:
1. $+V_{REF}$ and $-V_{REF}$ must be matched with in ±1% in order to meet system requirements.
2. Sampling is accomplished by changing the internal capacitor to within ½ LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown on the right.
3. The M5156 will l source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with I_{OH}= -100 μA, I_{OL}= 500 μA.
5. The first bit of data is loaded when Sync. and Clock are both "1" during bit time 1 as shown on RCV, timing diagram.
6. This delay is necessary to avoid overlapping Clock and Sync.

EQUIVALENT INPUT RESISTANCE CIRCUIT DURING SAMPLING



FUNCTIONAL DESCRIPTION

Pin 1 — Analog Input

Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to Figure 1). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion.

Pin 5 — Master Clock

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV, CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

FUNCTIONAL DESCRIPTION (continued)

Fig. 1 - A/D, D/A conversion timing

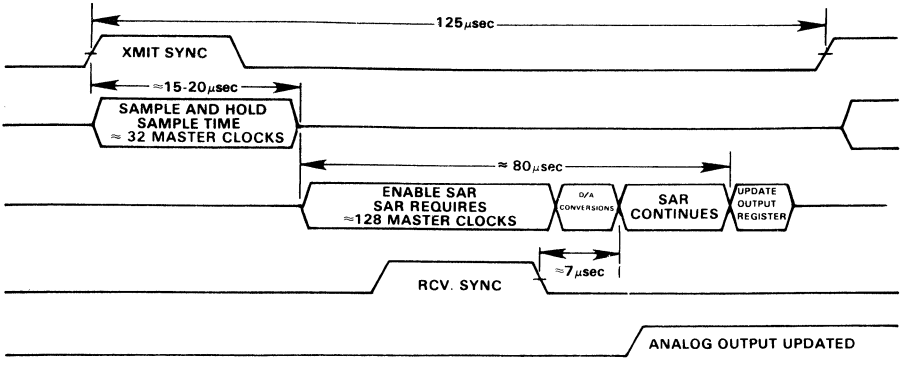
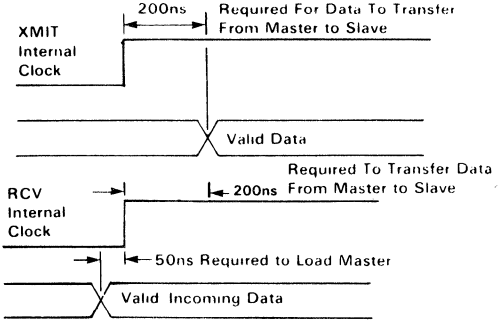
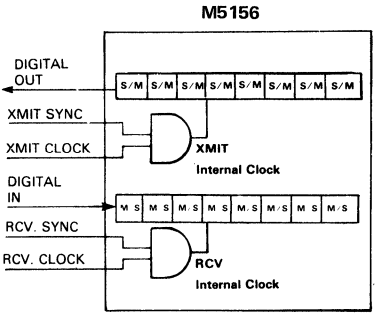


Fig. 2 - Data input/output timing



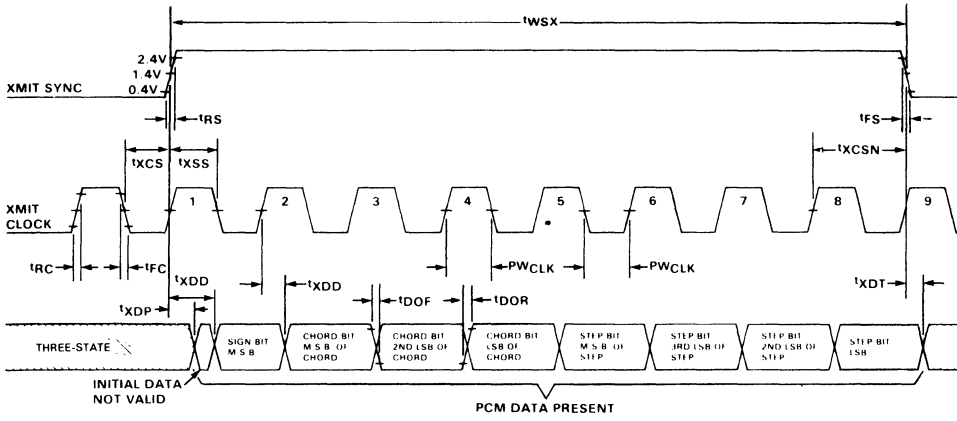


Pin 6 — XMIT SYNC (Refer to Figure 3 for the Timing Diagram)
This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word (Refer to Figure 7).

Pin 7 — XMIT CLOCK (Refer to Figure 3 for the Timing Diagram)
The on-chip 8-bit output shift register of the M5156 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 2). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

FUNCTIONAL DESCRIPTION (continued)

Fig. 3 - Transmitter section timing



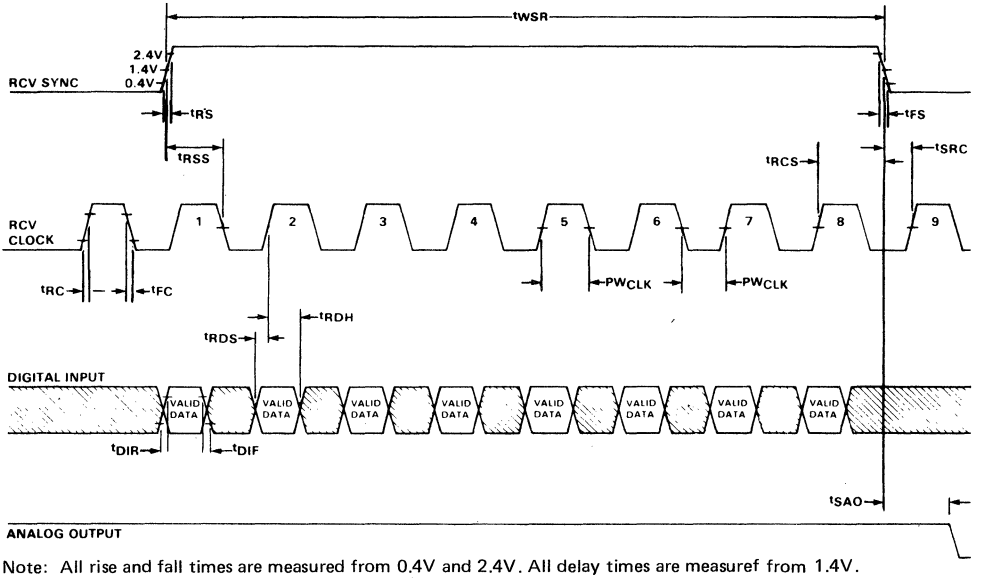
Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Pin 9 — RCV. SYNC (Refer to Figure 4 for the Timing Diagram)
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC. pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 1). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 8).

Pin 10 — RCV. CLOCK (Refer to Figure 4 for the Timing Diagram)
The on-chip 8-bit shift register for the M5156 is loaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 2). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - Receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measuref from 1.4V.

Fig. 5 - A/D converter (A-Law Encoder) transfer characteristic

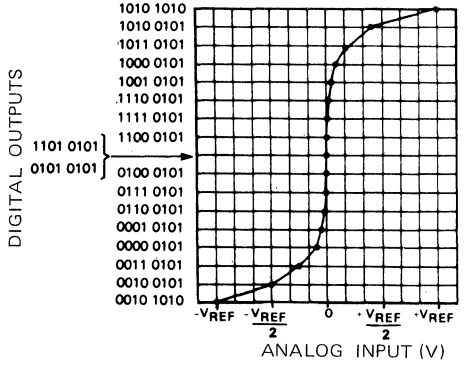
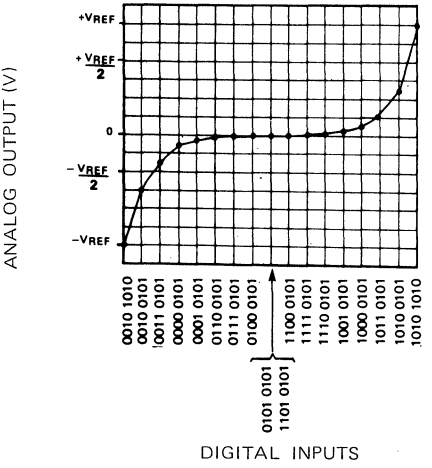


Fig. 6 - D/A converter (A-Law Decoder) transfer characteristic



FUNCTIONAL DESCRIPTION (continued)

Table 1 - Digital output code: A Law

	Chord Code	Chord Value	Step Value
1.	101	0.0 mV	1.221 mV
2.	100	20.1 mV	1.221 mV
3.	111	40.3 mV	2.44 mV
4.	110	80.6 mV	4.88 mV
5.	001	161.1 mV	9.77 mV
6.	000	332 mV	19.53 mV
7.	011	645 mV	39.1 mV
8.	010	1.289 V	78.1 mV

EXAMPLE:

1	110	0111=+80.6mV+(2x4.88mV)
Sign Bit	Chord	Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

Pin 8 — Digital Output

The M5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2 mV. In the third Chord, the Step Bit has a value of 2.4 mV. This doubling of the step value continues for each of the five successive Chords. Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (**Refer to Table 1**). Thus the output, which follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 5.

Pin 12 — Digital Input

The M5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 4. When RCV. SYNC goes high, the M5156 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 6.

Pin 13 — Analog Output

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

Pins 16 and 15 — Positive and negative reference voltages ($+V_{REF}$ and $-V_{REF}$)

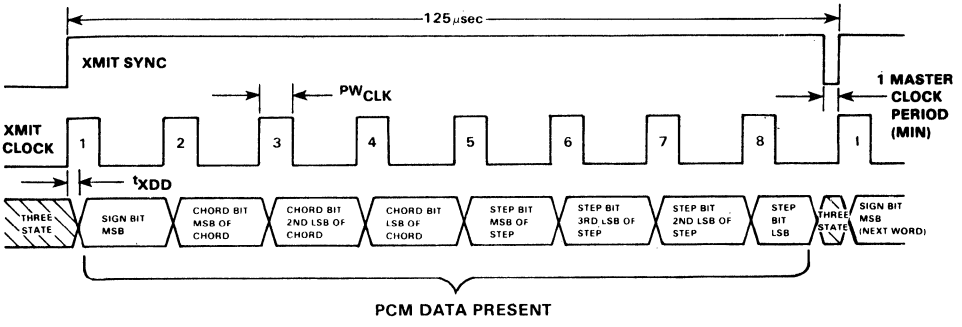
These inputs provide the conversion references for the digital-to-analog converters in the M5156. $+V_{REF}$ and $-V_{REF}$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

OPERATION OF DECODEC WITH 64 kHz XMIT/RCV.

Clock Frequencies

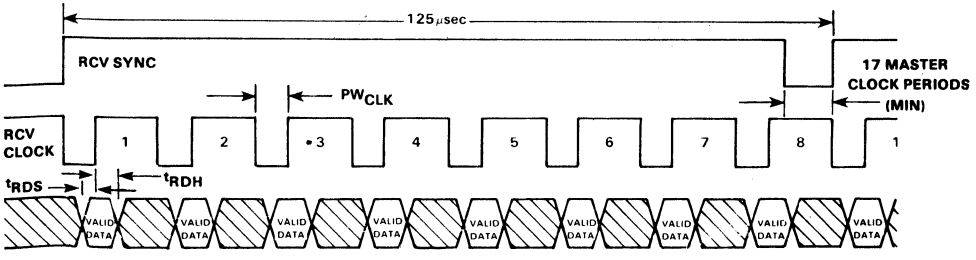
XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figs. 7 and 8).

Fig. 7 - 64 kHz operation, transmitter section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Fig. 8 - 64 kHz operation, receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Offset Null

The offset null feature of the M5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

Performance Evaluation

The equipment connections shown in Figure 9 can be used to evaluate the performance of the M5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the M5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the M5156 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC.
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 2.048 MHz.
(2) XMIT SYNC repetition rate = 8 kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods.

When all the above requirements are met, the setup of Figure 9 permits the measurement of synchronous system performance over a wide range of analog inputs.
The data register and ideal decoder provide a means of checking the encoder portion of the M5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the M5156 are shown in Figs. 10 and 11.

Fig. 9 - System characteristics test configuration

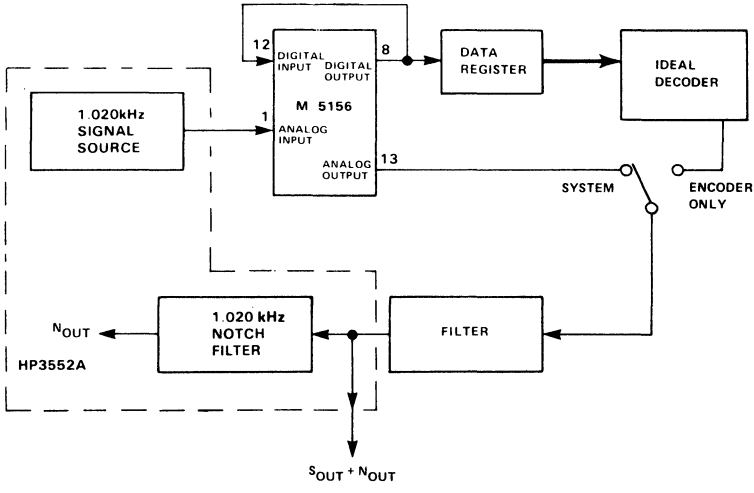


Fig. 10 - S/D ratio vs. input level

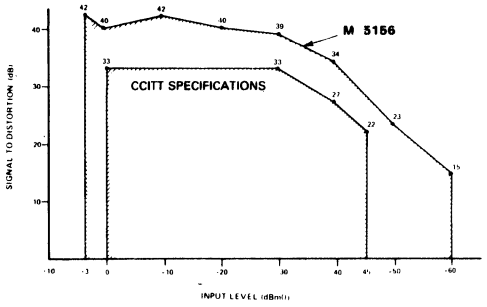
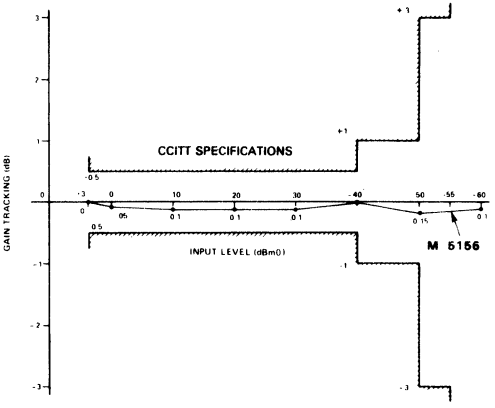


Fig. 11 - Gain tracking performance

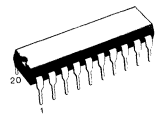


M5913
M5914

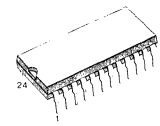
ADVANCE DATA

COMBINED SINGLE CHIP PCM CODEC AND AMPLIFIER

- M5914 ASYNCHRONOUS CLOCKS, 8th BIT SIGNALING, LOOP BACK TEST CAPABILITY
- M5913 SYNCHRONOUS CLOCKS ONLY
- AT&T D3/D4 AND CCITT COMPATIBLE
- TWO TIMING MODES:
  - FIXED DATA RATE MODE: CLOCK OPTIONS: 1.536MHz, 1.544MHz, 2.048MHz
  - VARIABLE DATA MODE: 64kHz-4.096MHz
- PIN SELECTABLE μ-LAW OR A-LAW OPERATION
- NO EXTERNAL COMPONENTS FOR SAMPLE AND HOLD AND AUTO ZERO FUNCTIONS
- PRECISION ON-CHIP VOLTAGE REFERENCES
- LOW POWER DISSIPATION:
  0.5mW POWER DOWN
  70mW TYPICAL OPERATING
- EXCELLENT POWER SUPPLY REJECTION
  - ELIMINATES ON-BOARD REGULATOR



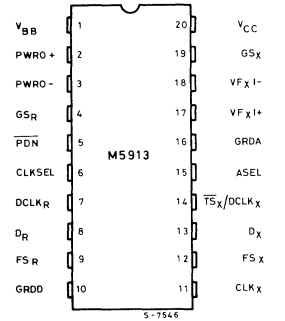
B/F
DIP-20 Plastic and Ceramic

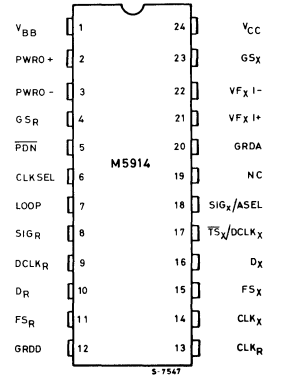


B/F
DIP-24 Plastic and Ceramic

ORDERING NUMBER: M5913B1
M5913F1
M5914B1
M5914F1

PIN CONFIGURATION





DESCRIPTION

The SGS M5913 and M5914 are fully integrated PCM (pulse code modulation) codecs (coder-decoder) and transmit/receive filters fabricated in a highly reliable CMOS silicon gate technology.

The primary applications for the M5913 and M5914 are il telephone systems:

- Switching – M5913-Digital PBX's and Central Office Switching Systems
- Transmission – M5914-D3/D4 Channel Banks
- Concentration – M5913 or M5914-Subscriber Carrier and Concentrators

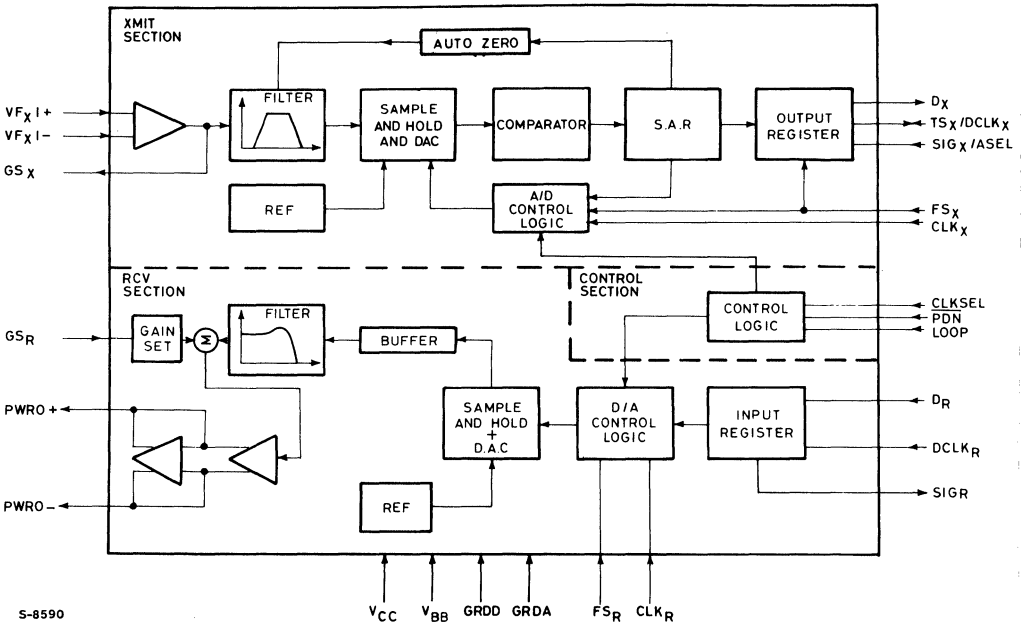
The wide dynamic range of the M5913 and M5914 (78dB) and the minimal conversion time make them ideal products for other applications such as:

- Voice Store and Forward
- Digital Echo Cancellers
- Secure Communications Systems
- Satellite Earth Stations

PIN NAMES

V_{BB}	Power (-5V)	GS_X	Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VF_XI-, VF_XI+	Analog Inputs
GS_R	Gain Setting input for Receive Channel	GRDA	Analog Ground
		NC	No Connect
$\overline{PDN}$	Power Down Select	SIG_X	Transmit Digital Signaling Input
CLKSEL	Master Clock Select	$\overline{ASEL}$	μ or A-law Select
LOOP	Analog Loop Back	$\overline{TS_X}$	Digital Output – Timeslot Strobe
SIG_R	Signaling Bit Output		
$DCLK_R$	Receive Data Rate Clock	$DCLK_X$	Transmit Data Rate Clock
D_R	Receive Channel Input	D_X	Transmit (Digital) Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With respect GRDD, GRDA = 0V	-0.3 to 7	V
V_{BB}	With respect GRDD, GRDA = 0V	+0.3 to -7	V
GRDD, GRDA	In such case: $0 \leqslant V_{CC} \leqslant +7V$, $-7V \leqslant V_{BB} \leqslant 0V$	± 0.3	V
$V_{I/O}$	Analog inputs, analog outputs and digital inputs	V_{BB} -0.3 $\leqslant V_{IN}/V_{OUT} \leqslant V_{CC}$ +0.3	V
$V_{O\ DIG}$	Digital outputs	GRDD -0.3 $\leqslant V_{OUT} \leqslant V_{CC}$ +0.3	V

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Symbol	Function
V_{BB}	Most negative supply, input voltage is -5V ± 5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power applifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power down select. When $\overline{PDN}$ is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} ..... 2.048MHz CLKSEL = GRDD ..... 1.544MHz CLKSEL = V_{CC} 1.536MHz
LOOP	Analog loopback. When this pin is TTL high, the receive output (PWRO +) is internally connected to VF_XI+, GS_R is internally connected to PWRO-, and VF_XI- is internally connected to GS_X. A 0dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
SIG_R	Signaling bit output, receive channel. In fixed data rate mode, SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable date rate mode. In this mode $DCLK_R$, becomes the receive data clock which operates a TTL levels from 64 kB to 4.096 MB data rates.

PIN DESCRIPTION (continued)

Symbol	Function
D_R	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK_R in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8KHz frame synchronization clock input/timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS_R is TTL low for 300 milliseconds.
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode, transmit master clock only in variable data rate mode.
FS_X	8KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS_R. The transmit channel enters the standby state whenever FS_X is TTL low for 300 milliseconds.
D_X	Transmit PCM output PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK_X in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS}_X/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64 KB to 4.096 MB data rates.
SIG_X/ASEL	A dual purpose pin. When connected to V_{BB}. A-law operation is selected. When it is not connected to V_{BB} this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	No connect
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non-inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply, input voltage is $+5V \pm 5\%$.

FUNCTIONAL DESCRIPTION

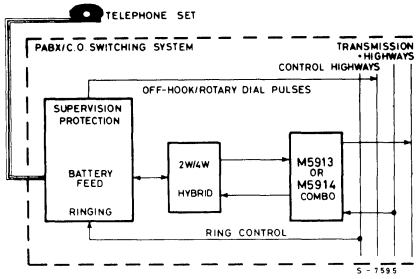
The M5913 and M5914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

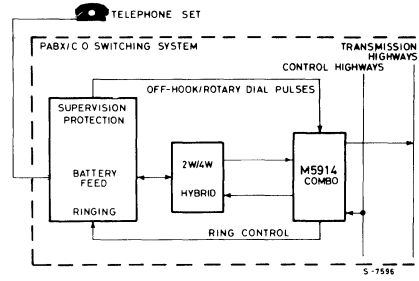
- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

Fig. 3 - Typical Line Terminations

SWITCHING

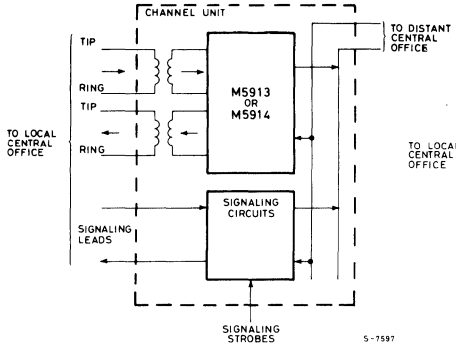


Functional block diagram of a line circuit with separate signaling control highways.

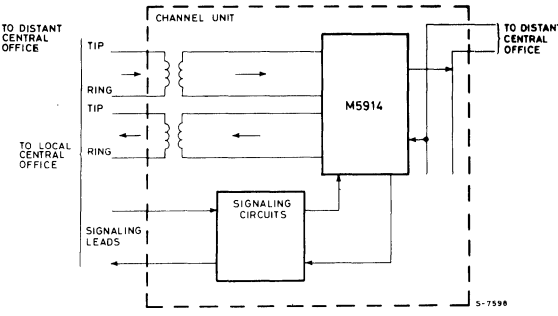


Functional block diagram of a line circuit with borrowed 8th bit signaling.

CHANNEL BANKS



A typical CCITT channel unit.



A typical 4-wire channel unit with signaling using borrowed 8th bit.

GENERAL OPERATION

System Reliability Features

The combochip can be powered up by pulsing FS_X and/or $\overline{FS_R}$ while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The M5913 and M5914 have internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS_X}$ are held in a high impedance state for approximately four frames (500μs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X, $\overline{TS_X}$, and signaling will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit setting time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS_X}$ and D_X will be placed in a high impedance state approximately 20μs after an interruption of CLK_X. Similarly, SIG_R will be held low approximately 20μs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most M5913/M5914 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 0.5 milliwatts. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumptions is reduced to an average of 1 milliwatts. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clocks CLK_X and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS_X}$.

Table 1 — Power-Down Methods

Device Status	Power-Down Method	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS_X}$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10 μs.
Standby Mode	FS_X and FS_R are TTL low	$\overline{TS_X}$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 300 milliseconds after FS_X and FS_R are removed.
Only transmit is on standby	FS_X is TTL low	$\overline{TS_X}$ and D_X are placed in a high impedance state within 300 milliseconds.
Only receive is on standby	FS_R is TTL low	SIG_R is placed in a TTL low state within 300 milliseconds.

CLK_X and CLK_R serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8 kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. $\overline{TS}_X$ is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly on the receive side, data is received on the first eitht falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544, or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

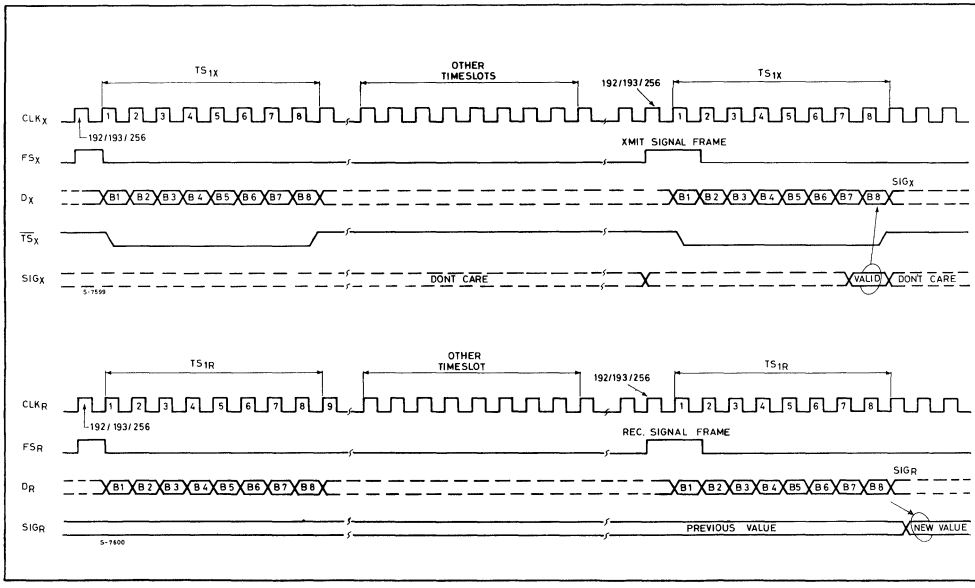
Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employs master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$ and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the M5914, or synchronous in the case of the M5913 from 64 KHz to 4.096 MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Simultarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transition of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125μs frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely,

Fig. 4 - Signaling Timing (Used Only with Fixed Data Rate Mode)



signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Signaling

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode ($DCLK_R = V_{BB}$). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG_X for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG_R lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in Figure 4.

Asynchronous Operation

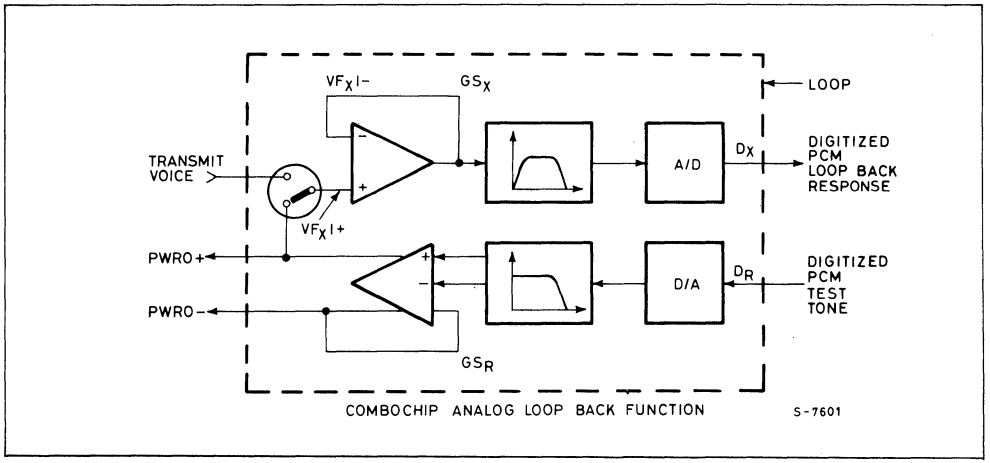
The M5914 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry the design of the SGS M5913/M5914 combochip includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely indipendent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in variable data rate mode the rising edge of CLK_X must occur within t_{FSD} nanoseconds before the rise of FS_X, while the leading edge of $DCLK_X$ must occur within t_{TSDX} nanoseconds of the rise of FS_X. Thus, CLK_X and $DCLK_X$ are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely indepenent of the transmit timing (refer to Variable Data Rate Timing Diagram). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

Analog Loopback

A distinctive feature of the M5914 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in Figure 5, when LOOP is TTL high the receive output (PWRO+) is internally connected to VF_XI+, GS_R in internally connected to PWRO- and VF_XI- is internally connected to GS_X.

Fig. 5 - Simplified Block Diagram of M5914 Combschip in the Analog Loopback Configuration



With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel (D_R) with those generated on the transmit channel (D_X). Due to the difference in transmission levels between the transmit and receive sides, a0 dBm0 code sent into D_R will emerge from D_X as a +3dBm0 code, an implicit gain of 3dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

Precision Voltage Reference

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

Conversion Laws

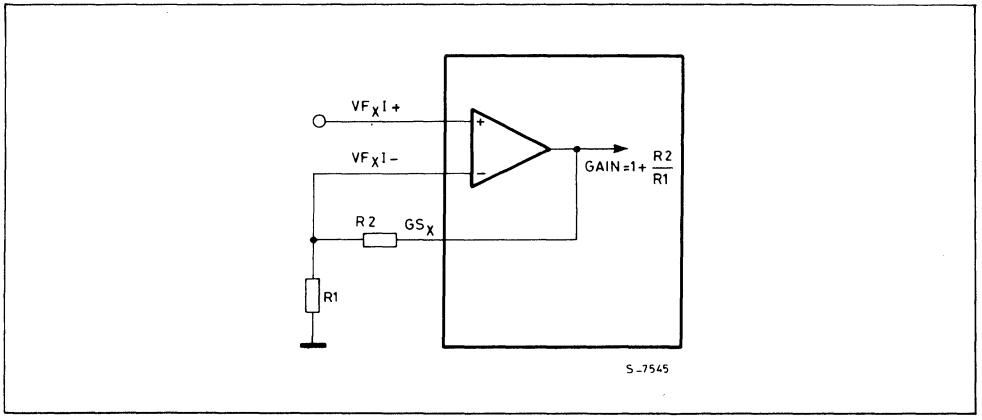
The M5913 and M5914 are designed to operate in both μ-law and A-law systems. The user can select either coversion law according to the voltage present on the SIG_X/ASEL pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for μ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If μ = 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB on the PCM output in signaling frames.

TRANSMIT OPERATION

Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17 volts, a maximum DC offset of 25 mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1MHz. Gain of up to 20dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10 kilohms in parallel with less than 50pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see Figure 6).

Fig. 6 - Transmit Filter Gain Adjustment



A low pass anti-aliasing section is included on-chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT & T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The M5913 and M5914 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in the relative table.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200Hz. This feature allows the use of low-cost transformer hybrids without external components.

Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

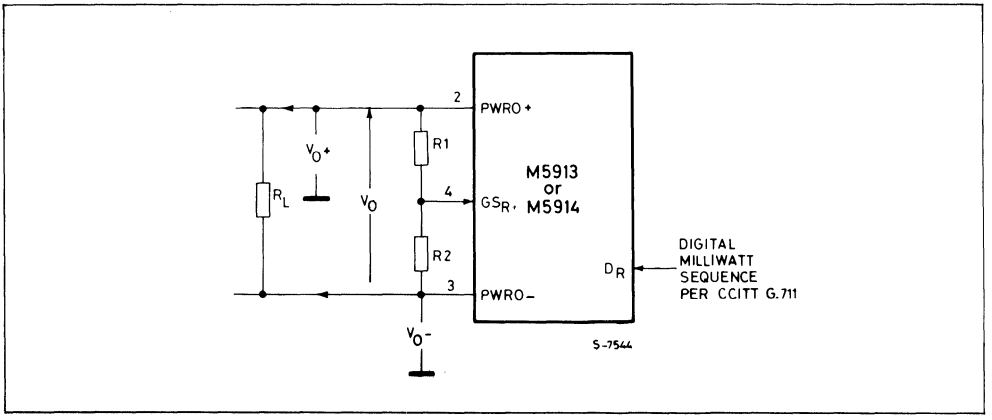
Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT & T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin X)/X response of such decoders. The receive filter characteristics and specifications are shown in the relative table.

Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single

Fig. 7 - Gain Setting Configuration



ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300Ω single ended to a level of 12dBM or 600Ω differentially to a level of 15dBM.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO-, the receive level is maximized; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and -12dB as GS_R is interpolated (with potentiometer) between PWRO- and PWRO+. The use of the output gain set is illustrated in Figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

OUTPUT GAIN SET: DESIGN CONSIDERATIONS

(Refer to Figure 7)

PWRO+ and PWRO- are low impedance complementary outputs. The voltages at the nodes are:

Vo+ at PWRO+
Vo- at PWRO-
Vo = Vo+ − Vo- (total differential response)

R1 and R2 are a gain setting resistor network with the center tap connected to the GS_R input. A value greater than 10KΩ and less than 100K for R1 + R2 is recommended because:

a) The parallel combination of R1 + R2 and R_L sets the total loading.

b) The total capacitance at the GS_R input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

If V_A represents the output voltage without any gain setting resistor network connected, you can have:

$$Vo = AV_A$$

$$\text{where } A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$$

For design purposes, a useful form is R1/R2 as a function of A.

$$R1/R2 = \frac{4A - 1}{1 - A}$$

(Allowable values for A are those which make R1/R2 positive)

Examples are:

If A = 1 (maximum output), then

$R1/R2 = \infty$ or $V(GS_R) = Vo-$;
i.e., GS_R is tied to PWRO-

If A = 1/2, then

$R1/R2 = 2$

If A = 1/4 (minimum output) then
$R1/R2 = 0$ or $V(GS_R) = Vo+$;
i.e., GS_R is tied to PWRO+

DC CHARACTERISTIC (T_{amb} = 0°C to 70°C, V_{CC} = +5 ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, unless otherwise specified) Typical values are for T_{amb} = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level Input Current	GRDD ≤ V_{IN} ≤ V_{IL} (Note[1])			10	μA
I_{IH}	High Level Input Current	V_{IH} ≤ V_{IN} ≤ V_{CC}			10	μA
V_{IL}	Input Low Voltage, except CLKSEL				0.8	V
V_{IH}	Input High Voltage, except CLKSEL		2.0			V
V_{OL}	Output Low Voltage	I_{OL}=3.2mA at D_X $\overline{TS}_X$ and SIG_R			0.4	V
V_{OH}	Output High Voltage	I_{OH}= 9.6mA at D_X I_{OH}= 1.2mA at SIG_R	2.4			V
V_{ILO}	Input Low Voltage, CLKSEL[2]		V_{BB}		V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKSEL		GRDD -0.5		0.5	V
V_{IHO}	Input High Voltage, CLKSEL		V_{CC}-0.5		V_{CC}	V
C_{OX}	Digital Output Capacitance[3]			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

POWER DISSIPATION – All measurements made at f_{DCLK} = 2.048MHz, outputs unloaded.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Operatin Current			8	10	mA
I_{BB1}	V_{BB} Operating Current			-6	-8	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL}; after 10μs		50	300	μA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL}; after 10μs		-50	-300	μA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL}; after 300ms		100	600	μA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL}; after 300ms		-100	-600	μA
P_{D1}	Operating Power Dissipation			70	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL}; after 10μs		0.5	3	mW
P_{ST}	Standby Power Dissipation	FS_X, FS_R ≤ V_{IL}; after 300ms		1	6	mW

NOTES:
1. V_{IN} is the voltage on any digital pin.
2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC}; they are also pinstraps for mode selection when tied to V_{BB} Under these conditions V_{ILO} is the input low voltage requirement.
3. Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pF.

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BX1}	Input Leakage Current VF_XI+, VF_XI-	$-2.17V \leq V_{IN} \leq 2.17V$			100	nA
R_{IXI}	Input Resistance, VF_XI+, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-				25	mV
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	$-2.17 \leq V_{IN} \leq 2.17V$	55			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X		5000			
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	$R_L \geqslant 10k\Omega$	+2.17		-2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ORA}	Output Resistance, PWRO+, PWRO-			1		Ω
V_{OSRA}	Single Ended Output DC Offset, PWRO+, PWRO-	Relative to GRDA		75		mV
C_{LRA}	Load Capacitance, PWRO+, PWRO-				100	pF
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO-, Single-Ended Connection	$R_L \geqslant 300\Omega$ (Note 3) with zero Volt offset	+3.06		-3.06	V
V_{ORA2}	Differential Output Voltage Swing PWRO+, PWRO-, Balance Output Connection	$R_L \geqslant 600\Omega$	-6.12		6.12	V

AC CHARACTERISTICS – TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave[1]. Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration.[2] All output levels are (sin X)/X corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EmW	Encoder Milliwatt Response (Transmit gain tolerance)	T_{amb}=25°C; V_{BB}= -5V; V_{CC}= +5V	-0.15	± 0.04	+0.15	dBm0
EmW_{TS}	EmW variation with Temperature and supplies	± 5% supplies, 0 to 70°C Relative to nominal condition	-0.12		+0.12	dB
DmW	Digital Milliwatt Response (Receive gain tolerance)	T_{amb}= 25°C, V_{BB}= -5V; V_{CC}= 5V	-0.15	± 0.04	+0.15	dBm0
DmW_{TS}	DmW variation with temperature and supplies	± 5% supplies, 0 to 70°C	-0.08		+0.08	dB
$0\,TLP_{1X}$	Zero Transmission Level Point Transmit Channel (0 dBm0) μ-Law	600Ω Load 900Ω Load		+2.76 +1.00		dBm dBm
$0\,TLP_{2X}$	Zero Transmission Level Point Transmit Channel (0 dBm0) A-Law	600Ω Load 900Ω Load		+2.79 +1.03		dBm dBm
$0\,TLP_{1R}$	Zero Transmission Level Point Transmit Channel (0 dBm0) μ-Law	600Ω Load 900Ω Load		+5.76 +4.00		dBm dBm
$0\,TLP_{2R}$	Zero Transmission Level Point Transmit Channel (0 dBm0) A-Law	600Ω Load 900Ω Load		+5.79 +4.03		dBm dBm

Note: 1. 0 dBm0 is defined as the zero reference point of the channel under test (0 TLP). This corresponds to an analog signal input of 1.064 V_{rms} or an output of 1.503 V_{rms} (μ-Law) dual 1.068 V_{rms} or an output 1.516 V_{rms} (A-Law).
2. Unity gain input amplifier: GS_X is connected to VF_XI-, Signal input VF_XI+; Maximum gain output amplifier: GS_R is connected to PWRO-, output to PWRO+.
3. Assuming null Receive gain Tolerance

GAIN TRACKING

Reference Level = -10 dBm0

Symbol	Parameter	Test Conditions	5913-1, 5914-1		5913, 5914		Unit
			Min.	Max.	Min.	Max.	
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law	+ 3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0		± 0.2 ± 0.3 ± 0.65		± 0.25 ± 0.5 ± 1.2	dB dB dB
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law	+ 3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0		± 0.2 ± 0.3 ± 0.65		± 0.25 ± 0.5 ± 1.2	dB dB dB
$GT3_X$	Transmit Gain Tracking Error While Noise Input; A-law	CCITT G.712 Method 1		TBD		TBD	dB
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law	+ 3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0		± 0.2 ± 0.3 ± 0.65		± 0.25 ± 0.5 ± 1.2	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law	+ 3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0		± 0.2 ± 0.3 ± 0.65		± 0.25 ± 0.5 ± 1.2	dB dB dB
$GT3_R$	Receive Gain Tracking Error White Noise Input; A-law	CCITT G. 712 Method 1		TBD		TBD	dB

NOISE

Symbol	Parameter	Test Conditions	2913-1, 2914-1			2913, 2914			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
N_{XC1}	Transmit Noise, C-Message Weighted	VF_XI+ = GRDA, VF_XI- = GS_X			13			15	dBrnc0
N_{XC2}	Transmit Noise, C-Message Weighted with Eighth Bit Signaling	VF_XI+ = GRDA, VF_XI- = GS_X; 6th frame signaling			16			18	dBrnc0
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA, VF_XI- = GS_X			-77			-75	dBm0p
N_{RC1}	Receive Noise, C-Message Weighted: Quiet Code	D_R = 11111111 Measure at PWRO+			8			11	dBrnc0
N_{RC2}	Receiver Noise, C-Message Weighted: Sign bit toggle	Input to D_R is zero code with sign bit toggle at 1 kHz rate			9			12	dBrnc0
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = lowest positive decode level			-82			-79	dBm0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			-50			-50	dBm0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X		-40			-30		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle channel; 200 mV P-P signal on supply; 0 to 50 kHz, measure at D_X		-40			-30		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz		-25			-25		dB
$PSRR_4$	V_{BB} Power Supply Rejection, Receive Channel	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50 kHz		-25			-25		dB
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+=0dBm0,1.02kHz, D_R= lowest positive decode level, measure at PWRO+			-80			-71	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_R = 0dBm0, 1.02 kHz, VF_XI+ = GRDA, measure at D_X			-80			-71	dB

DISTORTION

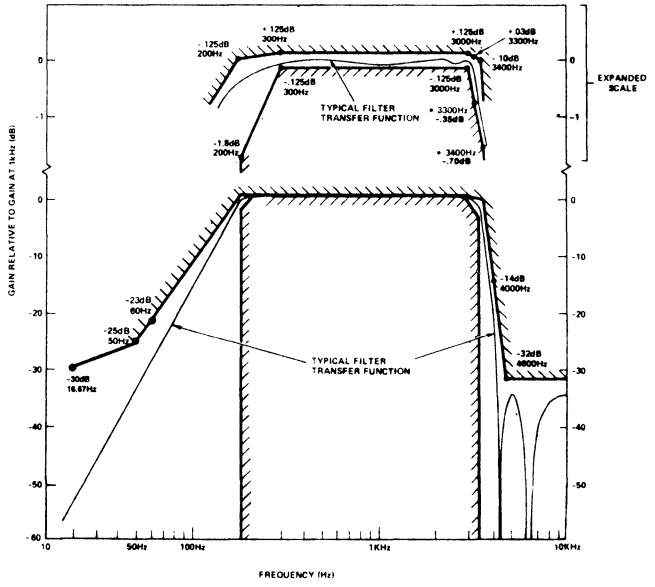
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G,712-Method 2	$0 \leqslant VF_XI+ \leqslant$ -30 dBm0 -40 dBm0 -45 dBm0	36 30 25			dB dB dB
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input CCITT G.712-Method 2	$0 \leqslant VF_XI+ \leqslant$ -30 dBm0 -40 dBm0 -45 dBm0	36 30 25			dB dB dB
$SD3_X$	Transmit Signal to Distortion, A-Law White Noise input; CCITT G.712-Method 1		TBD			
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2	$0 \leqslant VF_XI+ \leqslant$ -30 dBm0 -40 dBm0 -45 dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2	$0 \leqslant VF_XI+ \leqslant$ -30 dBm0 -40 dBm0 -45 dBm0	36 30 25			dB dB dB
$SD3_R$	Receive Signal To Distortion, A-Law While Noise Input; CCITT G.712-Method 1		TBD			
DP_{X1}	Transmit Single Frequency Distortion Products	AT&T Adivisory # 64 (3.8) 0 dBm0 Input Signal			-46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT&T Adivisory # 64 (3.8) 0 dBm0 Input Signal			-46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			-35	dB
IMD_2	Intermodulation Distortion End to End Measurement	CCITT G.712 (7.2)			-49	dB
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			-25	dBm0
SIS	Spurious in Brand Signals, End to End Measurement	CCITT G.712 (9)			-40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048 MHz; 0 dBm0, 1.02 kHz signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed Data Rate, CLK_R = 2.048 MHz; Digital input is DMW codes. Measure at PWRO+		150		μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		10 10 85 110		μs μs μs μs

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, noninverting; maximum gain output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_XI+				
	16.67 Hz				-30	dB
	50 Hz				-25	dB
	60 Hz				-23	dB
	200 Hz		-1.8		-0.125	dB
	300 to 3000 Hz		-0.125		+0.125	dB
	3300 Hz		-0.35		+0.03	dB
	3400 Hz		-0.7		-0.10	dB
	4000 Hz				-14	dB
	4600 Hz and Above				-32	dB

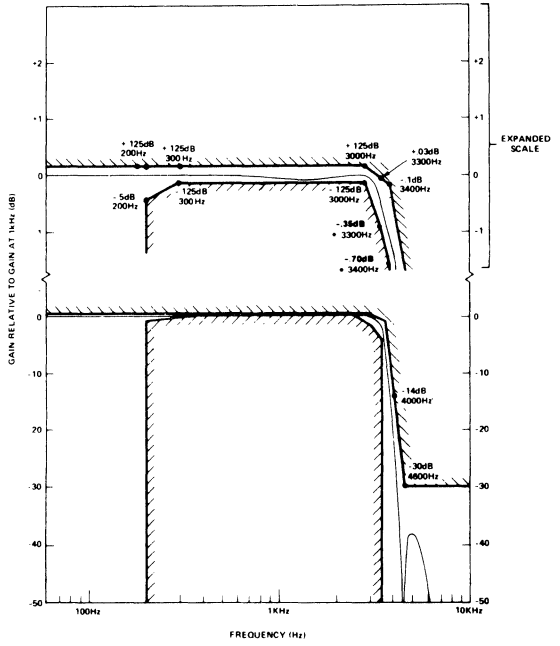
Fig. 8 - Transmit Filter



RECEIVE FILTER TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal input at D_R				
	Below 200 Hz				+0.125	dB
	200 Hz		-0.5		+0.125	dB
	300 to 3000 Hz		-0.125		+0.125	dB
	3300 Hz		-0.35		+0.03	dB
	3400 Hz		-0.7		-0.1	dB
	4000 Hz				-14	dB
	4600 Hz and Above				-30	dB

Fig. 9 - Receive Filter



AC CHARACTERISTICS – TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period, CLK_X, CLK_R	$f_{CLKX} = f_{CLKR} = 2.048$ MHz	488			ns
t_{CLK}	Clock Pulse Width	CLK_X, CLK_R	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	64 kHz $\leq f_{DCLK} \leq$ 2.048 MHz	195			ns
t_{CDC}	Clock Duty Cycle	CLK_X, CLK_R	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns

TRANSMIT SECTION, FIXED DATA RATE MODE[2]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DZX}	Data Enabled on TS Entry	$0 < C_{LOAD} < 100$ pF	0		145	ns
t_{DDX}	Data Delay from CLK_X	$0 < C_{LOAD} < 100$ pF	0		145	ns
t_{HZX}	Data Float on TS Exit	$C_{LOAD} = 0$	60		190	ns
t_{SON}	Timeslot X to Enable	$0 < C_{LOAD} < 100$ pF	0		145	ns
t_{SOFF}	Timeslot X to Disable	$C_{LOAD} = 0$	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SS}	Signal Setup Time		0			ns
t_{SH}	Signal Hold Time		0			ns

RECEIVE SECTION, FIXED DATA RATE MODE

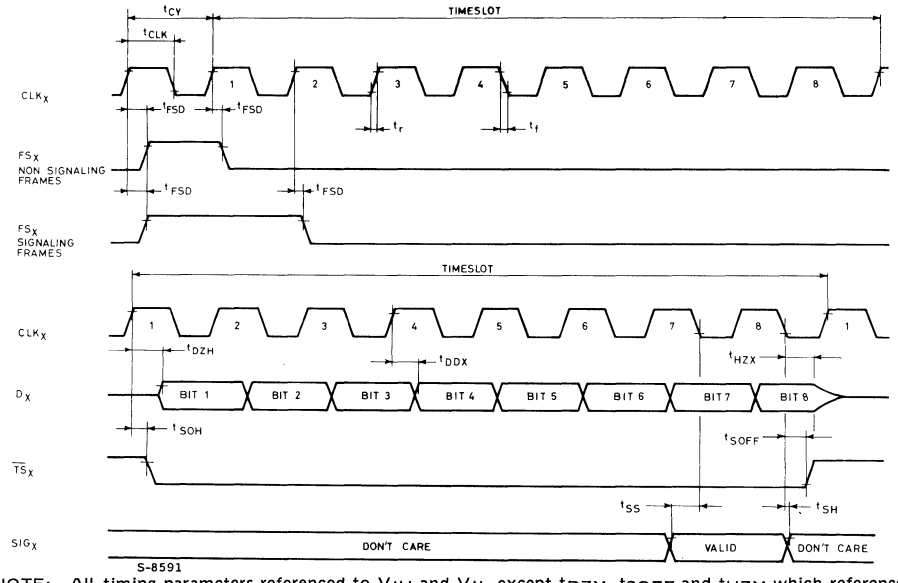
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SIGR}	SIG_R Update		0		2	μs

NOTES:

1. Devices are available which operate at data rates up to 4.096 MHz; the minimum data clock pulse width for these devices is 110 ns.
2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state

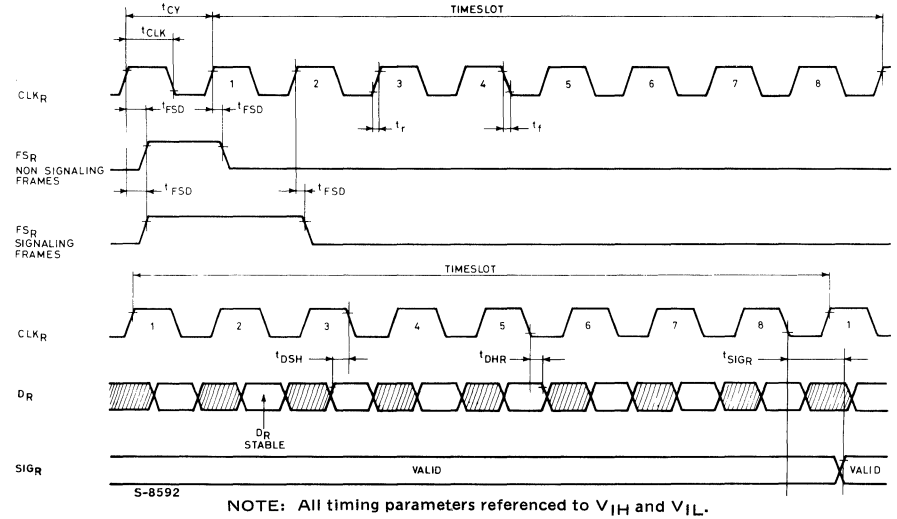
WAVEFORMS

Fixed Data Rata Timing – Transmit Timing



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

Receive Timing



NOTE: All timing parameters referenced to V_{IH} and V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE[1]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDX}	Timeslot Delay from $DCLK_X$		-80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	$0 < C_{LOAD} < 100$ pf	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100$ pf	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100$ pf	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[2]	kHz
t_{DFSX}	Data Delay from FS_X	$t_{TSDX} = 80$ ns	0		140	ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDR}	Timeslot Delay from $DCLK_R$		-80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Data Setup Time		10			ns
t_{DHR}	Data Hold Time		60			ns
f_{DR}	Data Clock Frequency		64		2048[2]	kHz
t_{SER}	Timeslot End Receive Time		0			ns

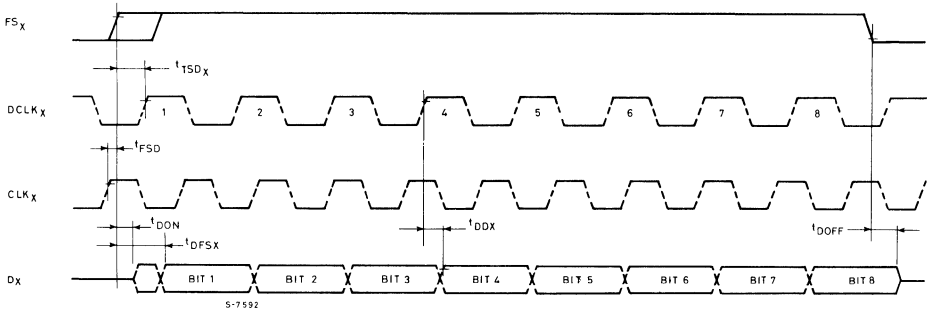
64 KB OPERATION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Minimum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width				10	μs

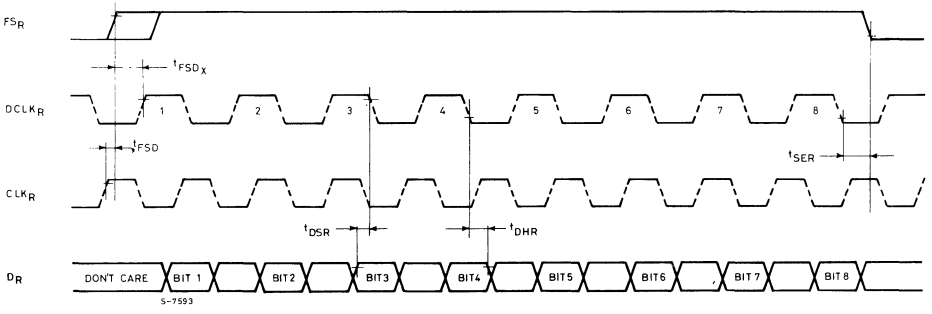
NOTES:
1. Timing parameters t_{DON} and t_{DOFF} are referenced to a high impedance state.
2. Device are available which operate at data rates up to 4.096 MHz.

VARIABLE DATA RATE TIMING

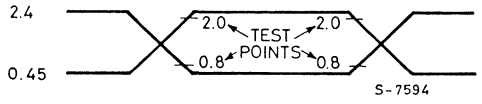
Transmit Timing



Receive Timing



AC Testing Input, Output Waveform

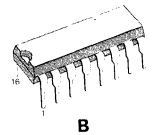


M5916
M5917

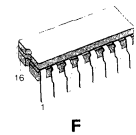
ADVANCE DATA

M5916 AND M5917 PCM COMBO

- **M5916** μ-LAW, 2.048MHz MASTER CLOCK
- **M5917** μ-LAW, 2.048MHz MASTER CLOCK
- INCREASED LINECARD DESTINTIES FROM 16-PIN PACKAGE
- PARTICULARLY USEFUL FOR DIGITAL HEADSET APPLICATIONS
- LOW POWER MODE (3) :
  - 5mW TYPICAL IN POWER DOWN MODE
  - 8mW TYPICAL IN STANDBY MODE
  - 70mW TYPICAL IN OPERATION MODE
- TIMING MODES :
  - VARIABLE 64KHz to 2.048MHz
  - DIRECT 2.048MHz
- COMPATIBLE WITH TTL AND CMOS
- LOW POWER PIN VERSION COMPATIBLE WITH INTEL 2916/2917
- COMPATIBLE WITH AT&T D3/D4 AND CCITT



B
DIP-16 Plastic



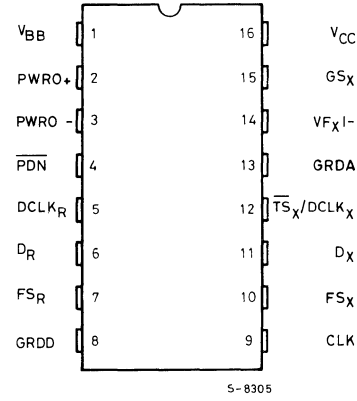
F
DIP-16 Ceramic

ORDERING NUMBER: M5916B1
M5916F1
M5917B1
M5917F1

DESCRIPTION

The M5916 and M5917 make available some of the features found in the M5913 and M5914. Since they are basically low in power and small in package size, they are particularly useful for digital handsets and cellular telephones where these features are particularly desirable. (See pin connection).

PIN CONFIGURATION

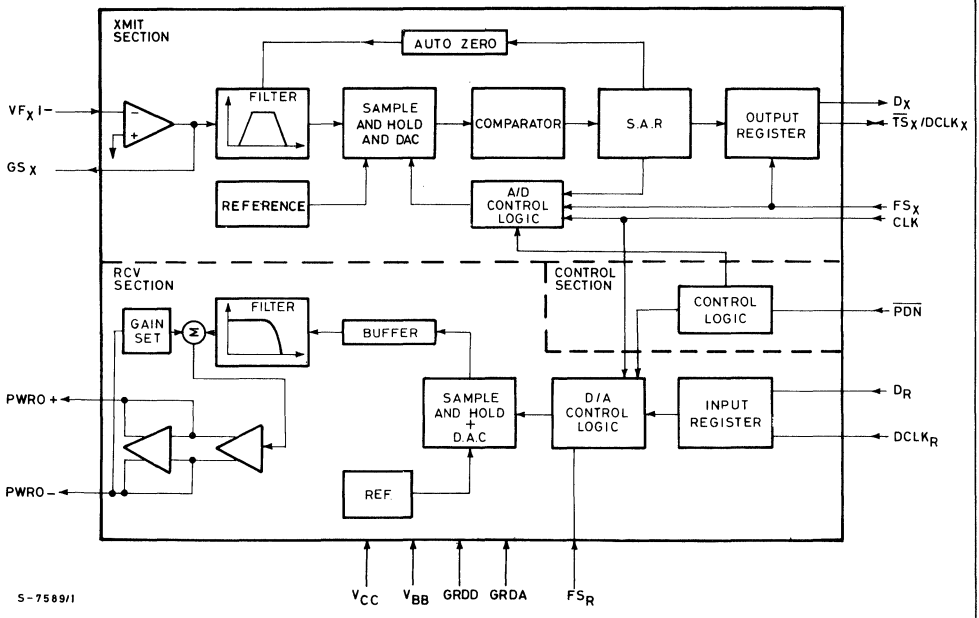


PIN NAMES

V_{BB}	Power (-5V)	VF_XI-	Analog Input
PWRO+, PWRO-	Power Amplifier Outputs	GRDA	Analog Ground
$\overline{PDN}$	Power Down Select	$\overline{TS}_X$	Timeslot Strobe/Buffer Enable
$DCLK_R$	Receive Variable Data Clock	$DCLK_X$	Transmit Variable Data Clock
D_R	Receive PCM Input	D_X	Transmit PCM Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK	Master Clock
GS_X	Transmit Gain Control	V_{CC}	Power (+ SV)

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



S.A.R. = Successive Approximation Register

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
T_{op}	Temperature Under Bias	-10 to +80	°C
T_{stg}	Storage Temperature	-65 to +150	°C
V_{CC}, G_{RDD}	With respect to V_{BB}	-0.3 to 15	V
V_I	All Input/Output Voltage with respect to V_{BB}	-0.3 to 15	V
P_{tot}	Power Dissipation	1.35	W

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Symbol	Function
V_{BB}	Negative supplies: -5V ± 5%.
PWRO+	Power amplifier non-inverting output. Directly drives high impedance loads or hybrids either in single ended or differential configuration.
PWRO-	Power amplifier inverting output. PWRO+'s functional complement.
$\overline{PDN}$	Select for power down. When it is TTL low, power down is effective; when high, the device is active.
$DCLK_R$	Fixed or variable data rate mode select. The fixed data rate mode is selected when DCLK is connected to V_{BB}. If not connected to V_{BB}, the variable data rate mode is effective, and $DCLK_R$ is the receive data clock, operation at TTL levels from 64kB to 4.096 MB level data rates.
D_R	PCM input data receive. Data are clocked in on consecutive receive data clock transitions, with $DCLK_R$ in variable, and CLK in fixed, data rate mode.
FS_R	8KHz frame synchronization clock input/timeslot enable, receive channel. Signal should stay high throughout variable data rate mode timeslot. Whenever FS_R is TTL low for 300ms, receive channel goes into standby.
GRDD	Internal logic circuits' digital ground. No internal link to GRDA.
CLK	Master and data clock for the fixed data rate mode; only master clock in variable data rate mode.
FS_X	8KHz frame synchronization clock input/timeslot enable, transmiit channel. Works like FS_R, but independently. Whenever FS_X is TTL low for 300ms, transmit channel goes into standby.
D_X	Transmit PCM Output. Transmit data clock, clocks them out on 8 consecutive positive transitions. Transmit clock in CLK in fixed data rate mode and $DCLK_X$ in fixed data rate mode.
$\overline{TS}_X/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a 3-state buffer. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 2048 MB data rates.
GRDA	Overall internal voice circuit analog ground return. No internal link to GRDD.
VF_XI-	Uncommitted transmit operational amplifier inverting analog input.
GS_X	On-chip uncomitted op-amp output terminal, serving internally as transmit filter voice signal input.
V_{CC}	+5V ± 5% input voltage; positive supply.

FUNCTIONAL DESCRIPTION

The M5916 and M5917 convert from analog to digital and vice-versa, and provide receive and transmit filtering sufficient for a full duplex 4-wire voice telephone circuit interface, using the PCM highways in a time division multiplexed system (TDM). These are used at the PM line analog termination.

Major functions are as follows:

- Analog signal bandpass filtering before coding and after decoding;
- Voice and call progress information coding and decoding;
- Signalling and supervision information coding and decoding.

GENERAL OPERATION

System Reliability Features

Combochip powering takes place by pulsing FS_X and/or FS_R at the same time as TTL high voltage is applied to $\overline{PDN}$, on condition that all clocks and supplies are connected. The M5916 and M5917 reset internally when power is applied (or when V_{BB} or V_{CC} are re-applied) to ensure digital output validity, so that PCM highway integrity is maintained.

Digital outputs D_X and $\overline{TS}_X$ are maintained in high impedance state for about four frames (500μs) after power, V_{BB} or V_{CC} is applied to the transmit channel.

The result of this delay is that D_X and $\overline{TS}_X$ will take place in the proper timeslot and be functional. Transmit side analog circuits reach equilibrium in about 60ms because of the autozero setting time.

For system reliability enhancement, $\overline{TS}_X$ and D_X are placed in high impedance state about 20μs after CLK interruption.

Power Down and Standby Modes

Two power down modes are available to minimize power consumption; these disable most M5916/M5917 functions. In these modes, only power down, clock and the frame sync. buffers are enabled; these last are needed for power up. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

An external control signal to the $\overline{PDN}$ pin is used in Power Down mode. Reduction of power consumption to 5mW, on the average, is achieved in this mode. When the signal is high, the device is active; when it is low, inactive. If no signal is received, the device remains active continuously, since the $\overline{PDN}$ pin has floated to TTL high.

The user, when employing standby mode, has the option of singly powering down either channel or the entire device by choosing to remove FS_X and/or FS_R. Power consumption is diminished to 12mW, on the average, when both channels are in standby. FS_X should be applied while holding FS_R low, if transmit only operation is wanted. Likewise, FS_R should be applied while holding FS_X low, if receive only is wanted.

Table 3 — Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN}$ = TTL low	5mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 10μs.
Standby Mode	FS_X and FS_R are TTL low	12mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300ms.
Only transmit is on standby	FS_X is TTL low	70mW	$\overline{TS}_X$ and D_X are placed in a high impedance state within 300ms.
Only receive is on standby	FS_R is TTL low	110mW	

Fixed Data Rate Mode

By connecting $DCLK_R$ to V_{BB}, fixed data rate timing is selected. Master clock CLK, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$ are used.

Two uses are made of CLK: master clock for the codec and filter sections; and bit clock controlling data in and out from the PCM highway.

The sampling frequency is set by 8kHz inputs FS_X and FS_R. Gating the PCM word on the PCM highway when an external buffer drives the line is carried out by the timeslot strobe/buffer enable output $\overline{TS}_X$.

Data is received on the highway at D_R on the first eitht falling edges of CLK. Likewise, on the transmit side, data is transmitted on the first eight positive transitions of CLK after the rising edge of FS_X. CLK frequency is 2.048MHz, the only operational frequency allowed in this mode.

Variable Data Rate Mode

By connecting $DCLK_R$ to the bit clock, rather than to V_{BB}, for the receive PCM highway, variable data rate timing is selected. Master clock CLK, bit clocks $DCLK_R$ and $DCLK_X$, and frame synchronization clocks FS_R and FS_X are used.

A flexible data frequency is allowed for variable data rate timing. It is possible to vary the frequency of the bit clocks from 64KHz to 2.048MHz, though the master clock remains restricted to 2.048MHz.

The data clocks for the receive and transmit PCM highways are $DCLK_R$ and $DCLK_X$ in this mode. PCM data from D_X is transmitted onto the highway during the following eight consecutive positive transitions of $DCLK_X$ when FS_X is high. Likewise, each PCM bit from the highway is received by D_R on the next eight consecutive negative transactions of $DCLK_R$ when FS_R is high.

The PCM word is repeated in all remaining timeslots in the 125μs frame on the transmit side wheneever DCLK is pulsed, and FS_X, high. The PCM word can thus be transmitted to the PCM highway as often as desired in each frame; this feature is only available in variable data mode.

Precision Voltage References

The voltage reference function requires no external components with the combochip. On-chip voltage references are generated, and during the manufacturing process, they are calibrated. A difference in subsurface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage characterises this technique. The gain and dynamic range characteristics of the device are determined by these references.

The transmit and receive sections are supplied with separate references; during the manufacturing process, each is trimmed independently. Further trimming in the gain setting op-amps results in the reference value being converted into a final precision value. The combochip can thus reach regulator manufacturing tolerances of ± 0.04dB of half channel absolute gain, giving an important error margin to the user for other board components.

TRANSMIT OPERATION

Transmit Filter

Passband gain adjustment in the input section is provided through use of an on-chip uncommitted operational amplifier. This provides a 2.17V common mode range, a 25mV maximum DC offset, a 5000 minimum voltage gain and a typical 1MHz unity gain bandwidth. Without decreasing filter performance, up to 20dB gain can be set. At amplifier output (GS_X), load impedance to GRDA should be superior to 10KΩ in parallel with less than 50pF. Either AC or DC coupled input signals on lead VF_XI can be used. Use of the input op-amp is limited to the inverting mode shown in Figure 3.

An on-chip low pass anti-aliasing section is included, which normally makes available 35dB sampling frequency attenuation. The necessary anti-aliasing function for the transmit filter switched capacitor section does not require any external components.

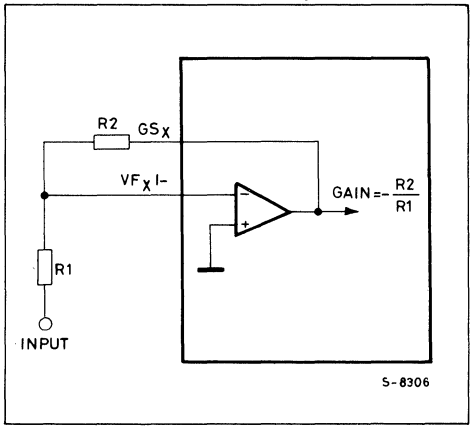
The AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712 are fulfilled by the flatness and stopband attenuation from the passband section. The M5916 and M5917 specifications equal or exceed 5

digital class central office switching norms.

The limits which are shown in Figure 4 apply for transmit filter transfer characteristics and specifications.

To reject low frequency noise from 50 and 60Hz power lines, 17Hz European electric railways, ringing frequencies and their harmonics, and other low frequency noise, a high pass section configuration was selected. The band edge sharpness provides low attenuation at 200Hz even though these frequencies have a high rejection rate. Low cost transformer hybrids without external components can thus be used.

Fig. 3 - Transmit Filter Gain Adjustment



Coding

The coder samples the transmit filter output internally; each sample is held on an internal sample and hold capacitor. An analog to digital conversion on a switched capacitor array is performed by the coder. On the first eight data clock bits of the next frame, digital data representing the sample is transmitted.

DC-offset on the coder input signal is corrected by an on-chip autozero circuit, which uses the sign bit averaging technique. The coder output sign bit is long term averaged and subtracted from the coder input. All DC offset is thus eliminated from the coder input waveform.

RECEIVE OPERATION

Decoding

On the first eight data clock bits of the frame, the D_R load PCM word is serially fetched. The digital word is subjected to a D/A conversion, and an internal sample and hold capacitor is used to hold the corresponding analog sample. The receive filter than takes over the sample.

Receive Filter

Passband flatness and stopband rejection fulfilling both the AT&T D3/D4 specification and CCITT recommendation G.712 are provided by the filter receive section. The required compensation for the (sin x)/x decoder response is contained in the filter. Within the limits shown in Figure 5 will be found the receive filter characteristics and specifications.

Receive Output Power Amplifiers

In order to permit maximum output configuration flexibility, a balanced output amplifier is provided. Single ended loads can be driven by either of the two outputs single endedly (GRDA referenced). Otherwise, a bridged load can be driven directly by the differential output. Loads as low as 300Ω single ended, or 600Ω differentially can be driven by the output stage to levels of 12dBM and 15dBM, respectively.

Transmission levels are specified relative to the receive channel output under digital mW conditions, that is, when the digital input at DR is the 8-code sequence specified in CCITT recommendation G.711.

DC CHARACTERISTICS (T_{amb} = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified)

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	GRDD ≤ V_{IN} ≤ V_{IL} (1)			10	μA
I_{IH}	High Level Input Current	V_{IH} ≤ V_{IN} ≤ V_{CC}			10	μA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA at D_X, $\overline{TS}_X$			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6mA at D_X	2.4			V
C_{OX}	Digital Output Capacitance (2)			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

POWER DISSIPATION – All measurements made at f_{DCLK} = 2.048MHz, outputs unloaded

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Operating Current			6.8		mA
I_{BB1}	V_{BB} Operating Current			7.2		mA
I_{CC0}	V_{CC} Power Down Current	$\overline{PDN}$ ≤ V_{IL}: after 10μs		0.5		mA
I_{BB0}	V_{BB} Power Down Current	$\overline{PDN}$ ≤ V_{IL}: after 10μs		0.5		mA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL}: after 300ms		0.8		mA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL}: after 300ms		0.8		mA
P_{D1}	Operating Power Dissipation (3)			70		mW
P_{D0}	Power Down Dissipation (3)	$\overline{PDN}$ ≤ V_{IL}: after 10μs		5		mW
P_{ST}	Standby Power Dissipation (3)	FS_X, FS_R ≤ V_{IL}: after 300ms		8		mW

NOTES:

1. V_{IN} is the voltage on any digital pin.
2. Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pF.
3. With nominal power supply values.

ANALOG INTERFACE, TRANSMIT CHANNEL INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BX1}	Input Leakage Current, VF_XI-	$-2.17V \leq V_{IN} \leq 2.17V$			100	nA
R_{IXI}	Input Resistance, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI-				25	mV
A_{VOL}	DC Open Loop Voltage Gain, GS_X		5000			
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	$R_L \geqslant 10K\Omega$	-2.17		2.17	V
C_{LXI}	Load Capacitance GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			KΩ

ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{ORA}	Output Resistance, PWRO+, PWRO-			1		Ω
V_{OSRA}	Single-Ended Output DC Offset, PWRO+ PWRO-	Relative to GRDA		75		mV
C_{LRA}	Load Capacitance, PWRO+, PWRO-				100	pF
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO-, Single-Ended Connection	$R_L \geqslant 300\Omega$ with 0V Offset	-3.06		3.06	V
V_{ORA2}	Differential Output Voltage Swing, PWRO+, PWRO- Balanced Output Connection	$R_L \geqslant 600\Omega$	-6.12		6.12	V

AC CHARACTERISTICS - TRANSMISSION PARAMETERS

If not noted otherwise, analog input is 0dBm0, 1020Hz sine wave. Unity gain, inverting setting for input amplifier. Digital input is PCM bit stream generated by passing through and ideal encoder a 0dBm0 1020Hz sine wave. Single-ended receive output measurement. All output levels (sin x)/x corrected.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EmW	Coder Milliwatt Response (Transmit gain tolerance)	Signal input of 1.064 V_{rms} μ-Law Signal input of 1.068 V_{rms} A-Law $T_{amb}=25°C$; $V_{BB}=-5V$; $V_{CC}=+5V$	-0.15	±0.04	+0.15	dBm0
EmW_{TS}	EmW variation with Temperature and supplies	± 5% supplies, 0 to 70°C Based on nominal conditions	-0.12		+0.12	dB
DmW	Digital Milliwatt Response (Receive gain tolerance)	Measured based on OTLPR. Signal input per CCITT Recommendation G.711. Output signal of 100Hz. $T_{amb}=25°C$; $V_{BB}=-5V$; $V_{CC}=+5V$	-0.15	±0.04	+0.15	dBm0
DmW_{TS}	DmW variation with temperature and supplies	± 5% supplies, 0 to 70°C	-0.08		+0.08	dB
$0TLP1_X$	Zero Transmission Level Point Transmit Channel (0dBm0) μ-Law	Referenced to 600Ω Referenced to 900Ω		+2.76 +1.00		dBm dBm
$0TLP2_X$	Zero Transmission Level Point Transmit Channel (0dBm0) A-Law	Referenced to 600Ω Referenced to 900Ω		+2.79 +1.03		dBm dBm
$0TLP1_R$	Zero Transmission Level Point Receive Chennel (0dBm0) μ-Law	Referenced to 600Ω Referenced to 900Ω		+5.76 +4.00		dBm dBm
$0TLP2_R$	Zero Transmission Level Point Receive Channel (0dBm) A-Law	Referenced to 600Ω Referenced to 900Ω		+5.79 +4.03		dBm dBm

NOTES:

1. 0dBm0 is defined as the zero reference point of the channel for μ-Law under test (0TLP). This corresponds to an analog signal input of 1.064 V_{rms} or an output of 1.053 V_{rms}.
2. Unity gain input amplifier, signal input VF_XI-.

GAIN TRACKING
(Reference level = -10dBm0)

Symbol	Parameter	Test Conditions	5916		5917		Unit
			Min.	Max.	Min.	Max.	
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-Law	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0		± 0.25 ± 0.5 ± 1.2			dB dB dB
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-Law	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0				± 0.25 ± 0.5 ± 1.2	dB dB dB
$GT3_X$	Transmit Gain Tracking Error Wite Noise Input; A-Law	CCITT G.712 Method 1				TBD	dB
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-Law	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0		± 0.25 ± 0.5 ± 1.2			dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-Law	+3 to -40dBm0 -40 to -50dBm0 --50 to -55dBm0				± 0.25 ± 0.5 ± 1.2	dB dB dB
$GT3_R$	Receive Gain Tracking Error Wite Noise Input; A-Law	CCITT G.712 Method 1				TBD	dB

NOISE

Symbol	Parameter	Test Conditions	5916			5917			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
N_{XC1}	Transmit Noise, C-Message Weithted	Unity Gain			15				dBrnc0
N_{XP}	Transmit Noise, Psophometrically Weighted	Unity Gain						-75	dBm0p
N_{RC1}	Receive Noise, C-Message Weighted; Quiet Code	D_R = 11111111 Measure at PWRO+			11				dBrnc0
N_{RC2}	Receive Noise, C-Message Weighted: Sign bit toggle	Input to D_R is zero code sign bit toggle at 1kHz rate			12				dBrnc0
N_{RP}	Receive Noise Psophometrically Weighted	D_R = lowest possible decode level						-79	dBm0p
N_{SF}	Single Frequency Noise End to End Measurement	CCITT G.712.4.2.			-50			-50	dBm0
$PSRR_1$	V_{CC} Power Supply Reject., Transmit Channel	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X		-30			-30		dB
$PSRR_2$	V_{BB} Power Supply Reject., Transmit Channel	Idle channel; 200mV P-P signal on supply; 0 to 50kHz, measure at D_X		-30			-30		dB
$PSRR_3$	V_{CC} Power Supply Reject., Receive Channel	Idle channel; 200mV P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50kHz		-25			-25		dB
$PSRR_4$	V_{BB} Power Supply Reject., Receive Channel	Idle channel; 200mW P-P signal on supply; measure narrow band at PWRO+ single ended, 0 to 50kHz		-25			-25		dB
CT_{TR}	Crosstalk, Transmit to Receive Single Ended Output	Input = 0dBm, Unity Gain. 1.02kHz, D_R = lowest positive decode level, measure at PWRO+			-71			-71	dB
CT_{RT}	Crosstalk, Receive to Transmit	D_R = 0dBm0, 1.02kHz, measure at D_X			-71			-71	dB

DISTORTION

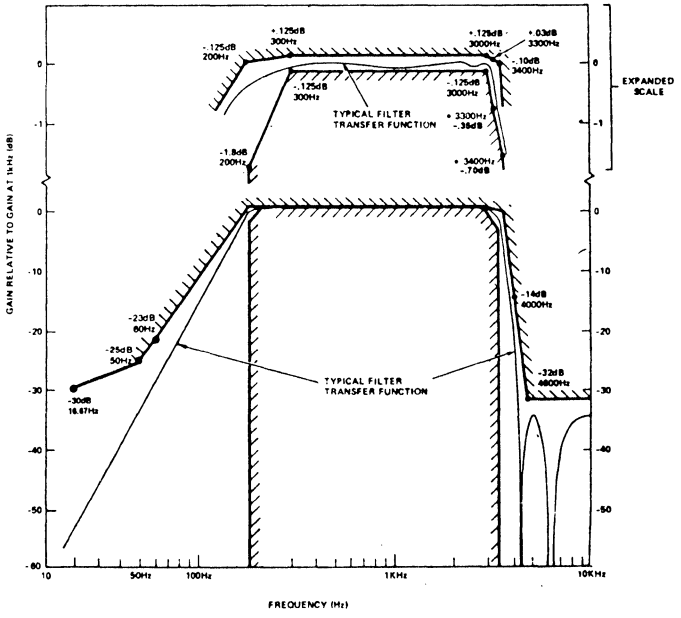
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$SD1_X$	Transmit Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2 (5916)	0 to -30dBm0 -30 to -40dBm0 -40 to -45dBm0	36 30 25			dB dB dB
$SD2_X$	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.712-Method 2 (5917)	0 to -30dBm0 -30 to -40dBm0 -40 to -45dBm0	36 30 25			dB dB dB
$SD3_X$	Transmit Signal to Distortion, A-Law Wite Noise Input; CCITT G.712-Method 1 (5917)		TBD			
$SD1_R$	Receive Signal to Distortion, μ-Law Sinusoidal Input; CCITT G.712-Method 2 (5916)	0 to -30dBm0 -30 to -40dBm0 -40 to -45dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion A-Law Sinusoidal Input; CCITT G.712-Method 2 (5917)	0 to -30dBm0 -30 to -40dBm0 -40 to -45dBm0	36 30 25			dB dB dB
$SD3_R$	Receive Signal to Distortion, A-Law Wite Noise Input; CCITT G.712-Method 1 (5917)		TBD			
DP_{X1}	Transmit Single Frequency Distortion Products	AT&T Advisory # 64 (3.8) 0 dBm0 Input Signal			-46	dBm0
DP_{R1}	Receive Signal Frequency Distortion Products	AT&T Advisory # 64 (3.8) 0 dBm0 Input Signal			-46	dBm0
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			-35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			-49	dBm0
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			-25	dBm0
SIS	Spurious In Band Signals, End to End Measurement	CCITT G.712 (9)			-40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate, CLK_X = 2.048MHz; 0dBm0, 1.02kHz Input Signal, Unity Gain. Measure at D_X		245		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		170 95 45 105		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed Data Rate, CLK = 2.048MHz; Digital Input is DMW codes. Measure at PWRO+		190		μs
D_{DR}	Receive Differential Envelope Delay Relative do D_{AR}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		45 35 85 110		μs μs μs μs

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

Input amplifier is set for unity gain, inverting

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02kHz	0 dBm0 Signal Input at VF_XI-				
	16.67Hz				-30	dB
	50Hz				-25	dB
	60Hz				-23	dB
	200Hz		-18		-0.125	dB
	300 to 3000Hz		-0.125		+0.125	dB
	3300Hz		-0.35		+0.03	dB
	3400Hz		-0.7		-0.10	dB
	4000Hz				-14	dB
	4600Hz and above				-32	dB

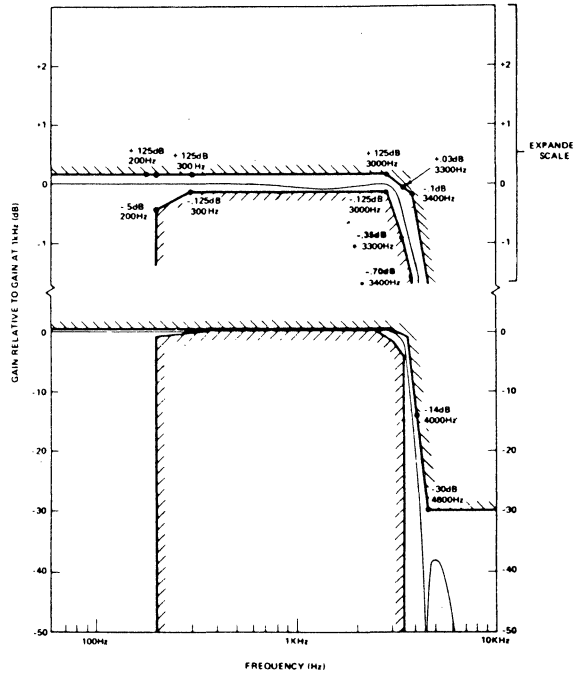
Fig. 4 - Transmit Channel



RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gain at 1.02kHz	0 dBm0 Signal Input at D_R				
	Below 200Hz				+0.125	dB
	200Hz		-0.5		+0.125	dB
	300 to 3000Hz		-0.125		+0.125	dB
	3300Hz		-0.35		+0.03	dB
	3400Hz		-0.7		-0.1	dB
	4000Hz				-14	dB
	4600Hz and above				-30	dB

Fig. 5 - Receive Channel



AC CHARACTERISTICS – TIMING PARAMETERS

CLOCK SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CY}	Clock Period, CLK	f_{CLK} = 2.048MHz	488			ns
t_{CLK}	Clock Pulse Width	CLK	195			ns
t_{DCLK}	Data Clock Pulse Width	64kHz ≤ f_{DCLK} ≤ 2.048MHz	195			ns
t_{CDC}	Clock Duty Cycle	CLK	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns

TRANSMIT SECTION, FIXED DATA RATE MODE (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DZX}	Data Enabled on TS Entry	0 < C_{LOAD} < 100pF	0		145	ns
t_{DDX}	Data Delay from CLK_X	0 < C_{LOAD} < 100pF	0		145	ns
t_{HZX}	Data Float on TS Exit	C_{LOAD} = 0	60		190	ns
t_{SON}	Timeslot X to Enable	0 < C_{LOAD} < 100pF	0		145	ns
t_{SOFF}	Timeslot X to Disable	C_{LOAD} = 0	50		190	ns
t_{FSD}	Frame Sync. Delay		0		120	ns

RECEIVE SECTION, FIXED DATA RATE MODE

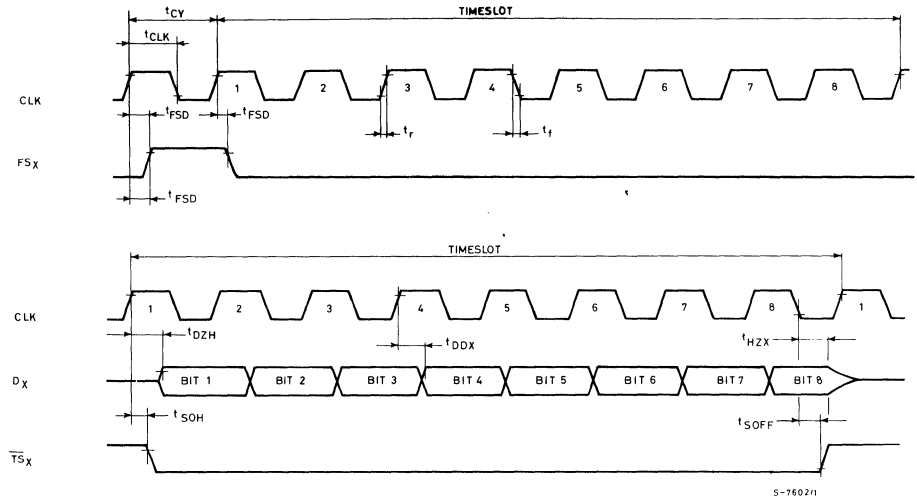
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync. Delay		0		120	ns

NOTES:

1. Timing parameters t_{DZX}, and t_{SOFF} are referenced to a high impedance state.

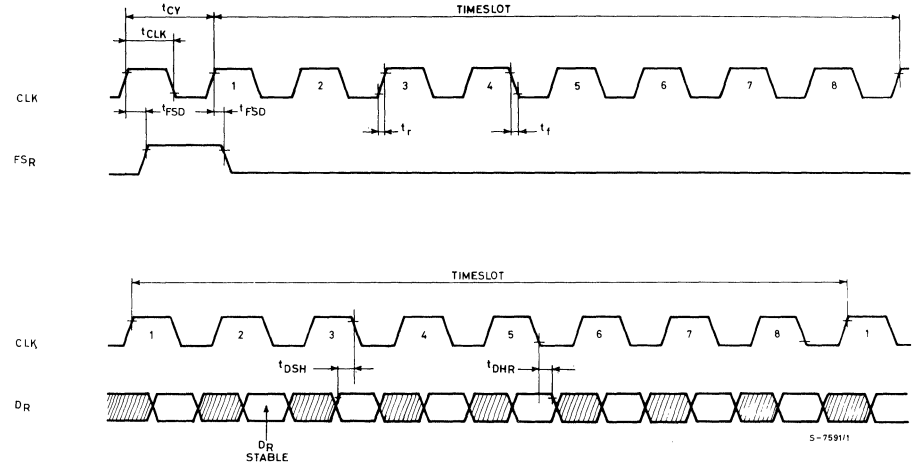
WAVEFORMS

Fixed Data Rate Timing – Transmit Timing



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

Receive Timing



NOTE: All timing parameters referenced to V_{IH} and V_{IL}.

TRANSMIT SECTION, VARIABLE DATA RATE MODE (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDX}	Timeslot Delay from $DCLK_X$		-80		80	ns
t_{DDX}	Data Delay from $DCLK_X$	$0 < C_{LOAD} < 100pF$	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100pF$	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100pF$	0		80	ns
f_{DX}	Data Clock Frequency		64		2048	kHz
t_{DFSX}	Data Delay from FS_X	t_{TSDX} = 80ns	0		140	ns

RECEIVE SECTION, VARIABLE DATA RATE MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TSDR}	Timeslot Delay from $DCLK_R$		-80		80	ns
t_{DSR}	Data Setup Time		10			ns
t_{DHR}	Data Hold Time		60			ns
f_{DR}	Data Clock Frequency		64		2048	kHz
t_{SER}	Timeslot End Receive Time		0			ns

64 KB OPERATION, VARIABLE DATA RATE MODE

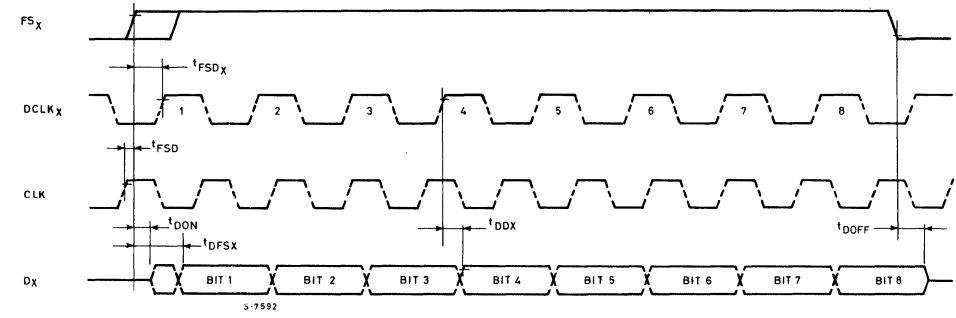
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{FSLX}	Transmit Frame Sync. Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync. Minimum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width				10	μs

NOTES:

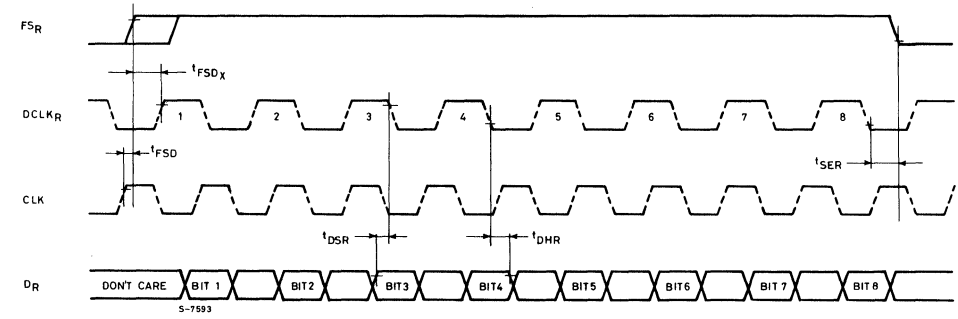
1. Timing parameters t_{DON} and t_{DOFF} are reference to a high impedance state.

WAVEFORMS – Variable Data Rate Timing

Transmit Timing

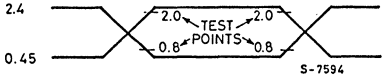


Receive Timing



Note: All Timing Parameters Referenced to V_{IH} and V_{IL} Except t_{DON} and t_{OFF} which Reference a High Impedance State

AC Testing Input, Output Waveform

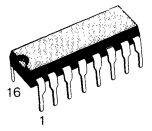


M6569
M6579

ADVANCE DATA

DTMF TRANSMITTER WITH REDIAL AND OUTPUT FLASH

- IT IMPROVES THE DTMF FUNCTION WITH REDIAL AND CALIBRATED OUTPUT TONES
- MEMORY OF 21 DIGITS
- PARALLEL INTERFACE WITH TELEPHONE LINE OR THROUGH SGS ORIGINAL SPEECH CIRCUIT FAMILIES (see Typical Application)
- DISTORSION: BELOW 2% IF USED WITH SGS SPEECH CIRCUIT; IN STAND ALONE LESS THAN 5%
- OUTPUT FLASH AVAILABLE ON M6579 (90ms) OPTION FOR 270ms AVAILABLE ON REQUEST



DIP-16 Plastic (0.25)

ORDERING NUMBER: M6569B1
M6579B1

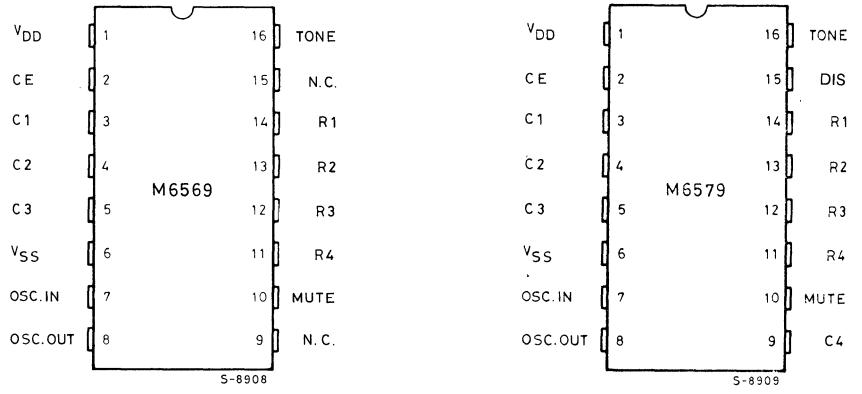
- KEYBOARD INTERFACE WITH 12 (M6569) AND 16 (M6579) BUTTONS.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	+5.5	V
V_{IN}	Voltage at any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V	V
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_{op}	Operating Temperature Range	−25 to +70	°C
	Lead Temperature	300	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS

M6569/M6579 Electrical characteristics: Specification apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.

Symbol	Parameter	Test Condition	(V_{DD}-V_{SS}) Volts	Min	Max	Unit
	SUPPLY VOLTAGE					
V_{DD}	Tone Out Mode (Valide key depressed)			2.5	5	V
	Non Tone Out Mode (no key depressed)			1.5	5	V
V_{DR}	Data Retention Voltage			1.0		V
	SUPPLY CURRENT					
I_{DD}	Standby (No Key Depressed), Tone, Mute and Flash Outputs Unloaded, CE = Low		2.00 5.00		1.0 20.0	μA μA
	Operating (One Key Selected, Tone, Mute and Flash Outputs Unloaded)		3.00		2.5	mA
	Operating During Flash		3.00		300	μA
	TONE OUTPUT					
V_{DR}	Low Group Freq. Voltage	R_L = 390kΩ	5.0	330	690	mVrms
dBcr	Ratio Of Column To Row Tone		2.5 - 5.0	1.0	3.0	dB
%DIS	Distortion		2.5 - 5		*	%
	MUTE AND FLASH OUTPUTS					
I_{OH}	Output Source Current	V_{OH} = 2.7V	3.0	1.0		mA
I_{OL}	Output Sink Current	V_{OL} = 0.3V	3.0	1.0		mA

* 2% - if used with SGS speech circuit, otherwise 7%

Comparisons of Specified vs. Actual Tone Frequencies Generated by M6569/M6579.

Active Input	Output Frequency HZ		% Error
	Specified	Actual	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.58
C2	1339	1331.7	−0.55
C3	1477	1471.9	−0.35

Note: % error does not include oscillator drift.

DESCRIPTION OF M6569/M6579

TONE GENERATION

It is obtained by division of master clock frequency. The cycle of each sinusoid is obtained by digital synthesis and provides a 32-steps approximation. The D/A converter, which performs it, is a resistor network. It is connected to the two reference level V_{DD} and V_{REF}.
V_{REF} is proportional to the supply voltage.
Output amplitude, which is a function of (V_{DD}-V_{REF}), increases with supply.
V_{REF} is chosen so that it is above the V_{BE} drop of the tone output transistor voltage range.
Tone output clipping at low supply voltage is thus eliminated, which improves distorsion performance (2% or 7% according note *).

HOW M6569/M6579 WORKS

Redial memory is filled automatically during first digitation.
Redial is inhibited when more than 21 digit are dialed.
Redial is actuated pushing "*" button, after off hook operation (M6569). In M6579 the Redial is performed pressing the "R" key, as indicated in keyboard configuration table.
During redial keyboard is diseabled. The keyboard is interfaced to a scanning circuitry, whose oscillator is unactivated when keys are not pushed.

When the M6569/M6579 oscillator is not running (key not pushed) the rows show pull down resistors and columns show pull-up resistors: being the resistors realized with active elements, their value depends on V_{DD} as R V_S V_{DD}.

Typical Resistance Values

V_{DD}	Pull-up Resistance (Typ)
2.0V	3.5kΩ
5.0V	1.7kΩ
V_{DD}	**Pull-down Resistance (Typ)**
2.0V	300kΩ
5.0V	30.0kΩ

Keyboard inputs are also drivable by standard CMOS outputs.

CHIP ENABLE

On M6569/M6579 CE pin is active high. When CE is low, TONE output goes to V_{SS}, inhibiting the oscillator and setting "low" MUTE and disconnect outputs.

MUTE OUTPUT

This is a push-pull output. When no key is depressed, MUTE OUT is low, otherwise is high for at least 70msec (duration of tone calibration).

FLASH FUNCTION (available on M6579 only)

DIS output is a push pull buffered output. It is normally High and goes Low when a depression on F key occurs.
DIS output is then activated for 90 msec. (or 270ms on request).

DISCONNECT FUNCTION (M6579 only)

It activates the DIS output, when D key is depressed.
Unlike the F key, D key holds DIS output as long as it is depressed.

PAUSE FUNCTION (M6579 only)

During the redial, this key interrupts the dialling sequence, until any other key is pressed.

DISTORSION PERFORMANCES OF M6569/M6579

(With filtering action through LS656).

The following pictures show the output waveforms, both at the output of M6569/M6579 and at the output of a two pole filter.

KEYBOARD CONNECTION TABLE

M6579

1	2	3	D
4	5	6	P
7	8	9	R
*	0	#	F

M6569

1	2	3
4	5	6
7	8	9
*	0	#

Fig. 1 - Frequency output of single tone emission

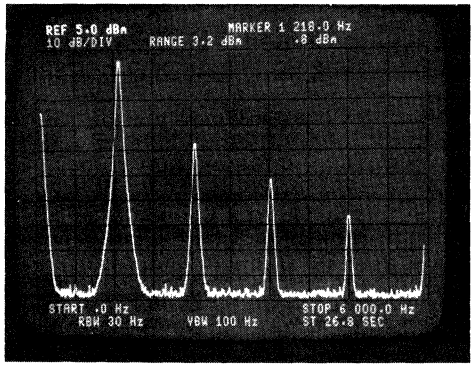


Fig. 2 - Frequency output of dual tone emission

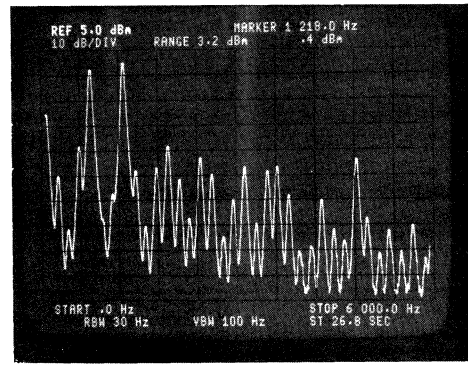


Fig. 3 - Single tone at M6569/M6579 output

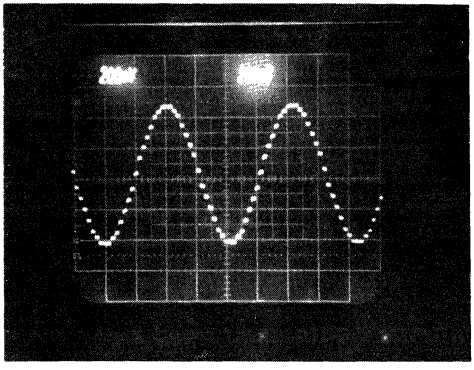


Fig. 4 - Single tone at the two pole filter output

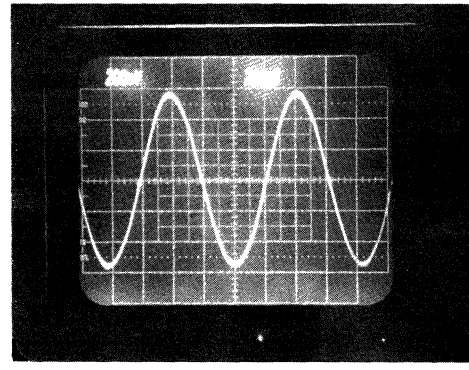


Fig. 5 - Dual tone at M6569/M6579 output

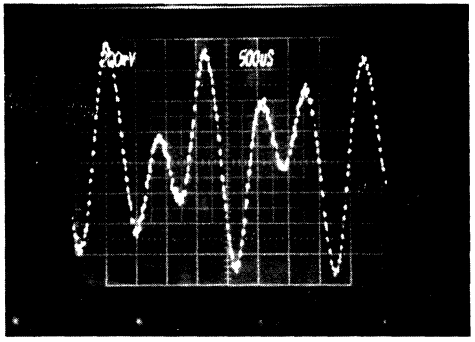


Fig. 6 - Dual tone at the two pole filter output

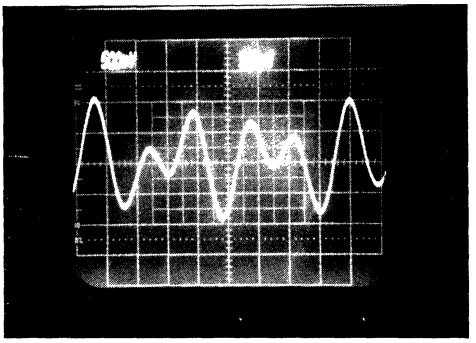
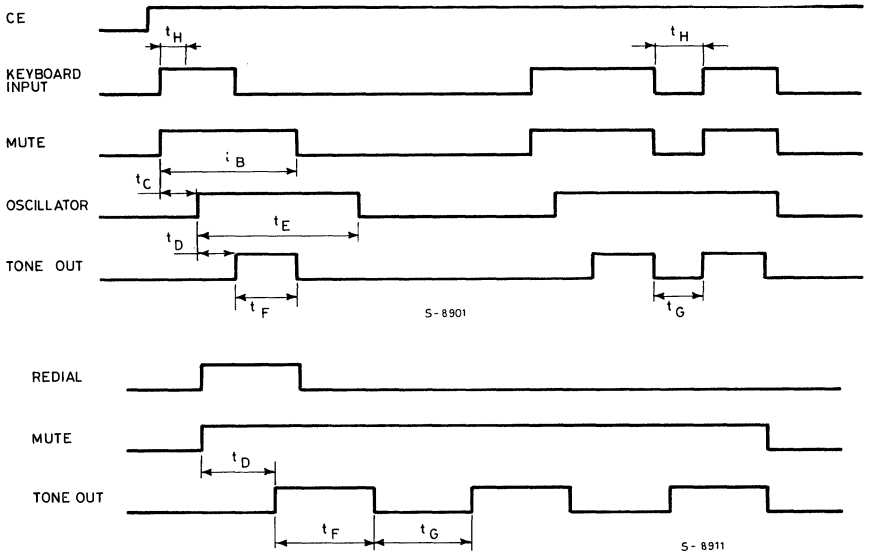
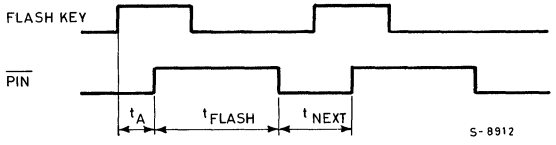


Fig. 7 - Time Diagrams



t_A = DEBOUNCE TIME = 18ms
t_H = KEY RELEASE TIME = 6ms
t_B = MIN. MUTE PULSE WIDTH = 73ms
t_C = OSCILLATOR START UP = 3ms
t_E = OSCILL. MIN ON TIME = 140ms
t_D = TONE OUT DELAY = 21ms
t_F = MINIMUM TONE OUT = 70ms
t_G = MINIMUM OFF TIME = 70ms
t_{FLASH} = 90ms
t_{NEXT} = 50ms



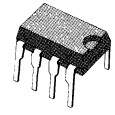
ML8204
ML8205

ADVANCE DATA

TONE RINGER

- DESIGNED FOR TELEPHONE BELL REPLACEMENT
- LOW CURRENT DRAIN
- SMALL SIZE "MINIDIP" PACKAGE
- ADJUSTABLE 2-FREQUENCY TONE
- ADJUSTABLE WARBLING RATE
- BUILT-IN HYSTERESIS PREVENTS FALSE TRIGGERING AND ROTARY DIAL "CHIRPS"
- EXTERNAL TRIGGERING OR RINGER DISABLE (ML8204)
- ADJUSTABLE FOR REDUCED SUPPLY INITIATION CURRENT (ML8205)
- TELEPHONE SET TONE RINGERS
- EXTENSION TONE RINGER MODULES
- ALARMS OR OTHER ALERTING DEVICES

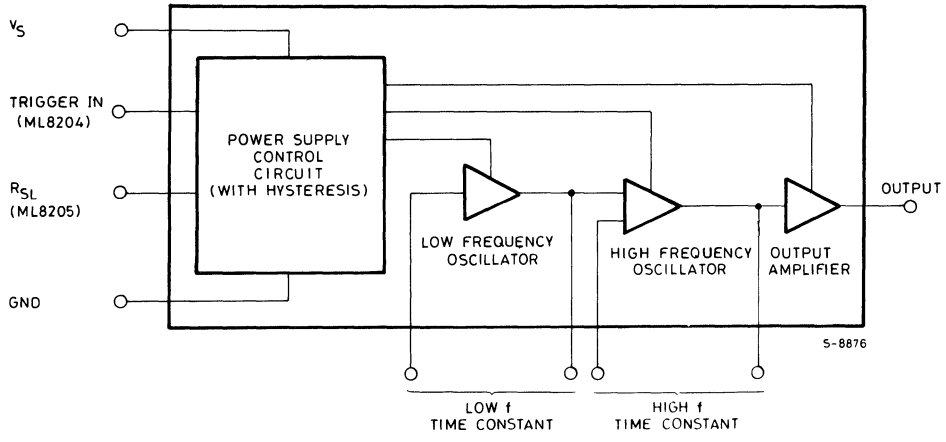
The ML8204/ML8205 tone ringers are monolithic devices, each incorporating two oscillators, an output amplifier and a power supply control circuit. The oscillator frequencies can be adjusted over a wide range by selection of external components. One oscillator, normally operated at a low frequency (f_L), causes the second oscillator to alternate between its nominal frequency (f_{H1}), and a related higher frequency (f_{H2}). The resulting output is a distinctive "warbling" tone. The output amplifier will drive either a transformer coupled loudspeaker or a piezo-ceramic transducer. The device can be powered from a telephone line or a fixed d.c. supply. The power supply control circuit has built-in hysteresis to prevent false triggering and rotary dial "chirps". The ML8204 can be triggered externally under logic control. The ML8205 has provision for adjustment of the power supply initiation current.



Minidip Plastic

ORDERING NUMBERS: ML8204AE
ML8205AE

BLOCK DIAGRAM

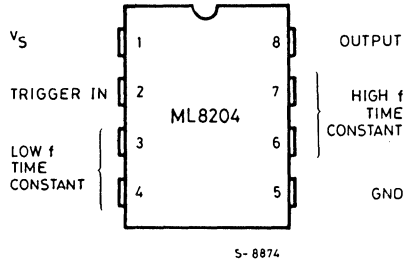


ABSOLUTE MAXIMUM RATINGS *

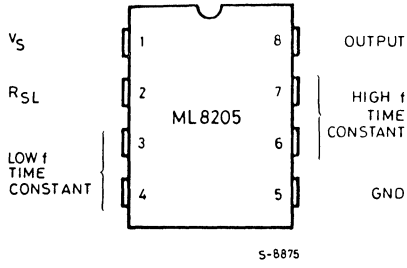
V_S	Supply voltage - GND	30	V
T_{op}	Operating temperature	-45 to 65	°C
T_{stg}	Storage temperature (E package)	-65 to 150	°C
P_{tot}	Total power dissipation (E package)•	400	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
• Derate 6.3mW/°C above 25°C. All leads soldered to PC board.

CONNECTION DIAGRAMS
(Top view)



S-8874



S-8875

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	6.3	mW/°C

ELECTRICAL CHARACTERISTICS (All voltages referenced to GND unless otherwise noted T_{amb} = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating supply voltage				29	V
V_{si}	Supply initiation voltage (1)	Trigger in open circuit (ML8204)	17	19	21	V
V_{sus}	Sustaining voltage (2)		9.7	11	12	V
I_{si}	Supply initiation current	No load $V_s = V_{si}$ R_{SL} = 6.8KΩ (ML8205)	1.4	2.5	4.2	mA
I_{sus}	Sustaining current	No load $V_s = V_{sus}$	0.7	1.2		mA
V_{TR}	Trigger voltage (3)		10.5	11		V
I_{TR}	Trigger current (3)		10	20	1000 (5)	μA
V_{DIS}	Disable voltage (4)			0.4	0.8	V
I_{DIS}	Disable current (4)		-40	-50		μA
V_o	Output voltage	No load V_s = 21V	17	19	21	V
f_o	Oscillator frequency tolerance	Component tolerance excluded			± 7	%

Notes: (1) V_{si} is the value of supply voltage which must be exceeded to trigger oscillation.
(2) V_{sus} is the value of supply voltage required to maintain oscillation.
(3) V_{TR} and I_{TR} are the conditions applied to Trigger In to start oscillation for $V_{sus} \leqslant V_s \leqslant V_{si}$.
(4) V_{DIS} and I_{DIS} are the conditions applied to Trigger In to inhibit oscillation for $V_{si} < V_s$.
(5) Trigger Current must be limited to this value externally.

Fig. 1a - Supply current vs. supply voltage (No load)

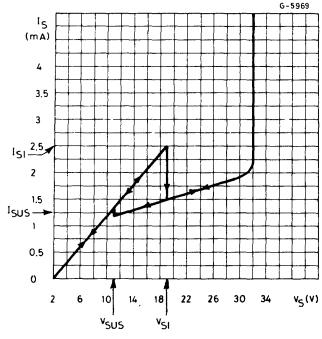
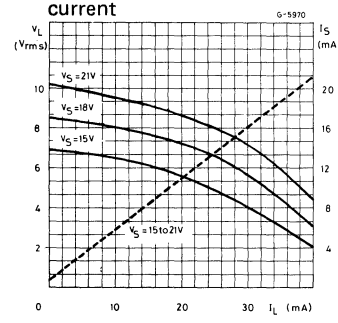


Fig. 1b - Load voltage and supply current vs. load current



FUNCTIONAL DESCRIPTION

The M8204/ML8205 Tone Ringers are primarily intended for use as replacements for the mechanical bell in telephone sets. Each incorporates two oscillators, an output amplifier and a power supply control circuit. The devices can be powered directly from the telephone line using the a.c. ringing voltage, or they may be powered from a separate d.c. supply. The output amplifier is capable of driving a wide range of load impedances when powered from a low impedance supply. The power supply control circuit provides the hysteresis required to ensure positive triggering of the device and to prevent transient triggering due to dial pulsing.

As the power supply voltage to the ML8204/ML8205 is increased up to the supply initiation voltage (V_{si}), the supply current also increases up to I_{si}). When V_{si} is exceeded, oscillation begins and the static power supply current decreases (see Fig. 2a). The low frequency oscillator (LFO) oscillates at a rate (f_L) controlled by an external resistor and capacitor. The frequency can be determined using the relation $f_L = 1/(1.234RC)$ where R is the value of the resistor connected between pins 3 and 4, and C is the value of the capacitor connected between pin 3 and ground.

The output of the LFO is internally connected to the switching threshold circuitry of the high frequency oscillator (HFO). When the output of the LFO is high, the HFO oscillates at its nominal rate (f_{H1}), described by the relation $f_{H1} = 1/(1.515RC)$ where R is the value of the resistor connected between pins 6 and 7, and C is the value of the capacitor connected between pin 6 and ground. When the output of the LFO is low, the HFO oscillates at a higher rate (f_{H2}) described by the relation $f_{H2} = 1.25f_{H1}$. Thus the LFO sets the warbling rate: the rate at which the HFO switches between the two tone frequencies f_{H1} and f_{H2}. Oscillation continues until the supply voltage decreases below the sustaining voltage (V_{sus}). At this point, the power supply current undergoes a step increase (from I_{sus}), and then ramps down in accoardance with the supply voltage.

In normal applications, Trigger in (pin 2) of the ML8204 is left open circuit. This pin allows external triggering of oscillation of the ML8204 at supply voltages in the range $V_{sus} \leqslant V_s \leqslant V_{si}$. To do so, a voltage at least equal to the minimum trigger voltage (V_{TR}) must be applied to pin 2.

Triggering the device is accomplished by sourcing a minimum current (I_{TR}) into pin 2. This current must be limited to prevent damage to the triggering circuit. Tone ringer oscillation may also be inhibited at supply voltages in the range $V_{si} < V_s \leqslant V_{s(max)}$ by applying a maximum disable voltage (V_{DIS}) to pin 2. Disabling is accomplished by sinking a minimum current (I_{DIS}) out of pin 2. (See Applications Section for details on the operation and use of the Trigger in pin.).

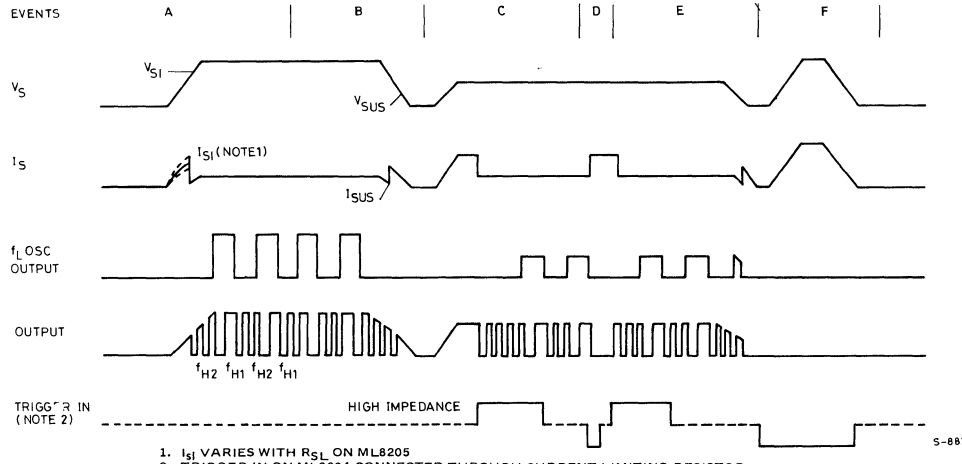
The ML8205 requires the connection of a resistor, R_{SL}, to program the slope of its supply current versus supply voltage characteristic prior to triggering ($V_s \leqslant V_{si}$). This in turn determines the maximum supply initiation current (I_{si} drawn at the initiation voltage (V_{si})). Programming is accomplished by connecting a slope determining resistor, R_{SL}, between pin 2 and ground. The value of I_{si} varies inversely with the value of R_{SL}. This feature can be used to control effective impedance presented to the telephone line by the ringer circuit. (See Applications section for detailed description on the operation and use of the R_{SL} pin.).

The output amplifier of the ML8204/ML8205 is capable of driving a wide range of load impedances when driven from a low source impedance power supply. When the device is powered from a telephone line. load impedance should be kept fairly high (800Ω or greater) to prevent power supply regulation problems. A transformer is thus required for driving loudspeakers as is an output coupling capacitor. Piezo-ceramic transducers may be driven directly. However, the tone frequencies f_{H1} and f_{H2} must normally be set higher (around 2KHz) to ensure that the transducer delivers sufficient acoustic power. (Suitable piezo-ceramic transducers typically have maximum efficiency around 2KHz). It is also necessary to connect a zener diode in parallel with the transducer to limit voltage surges generated by the transducer during mechanical shocks.

TABLE 1

PIN	PIN FUNCTION	DESCRIPTION
1	V_{SS}	Positive power supply.
2	Trigger in	ML8204 - Oscillator external trigger/inhibit pin (Must be connected through a current limiting resistor when used.)
	R_{SL}	ML8205 - Initiation Current (I_{sl}) programming pin. (Must be connected.)
3	Low f Time Constant	Low Frequency Time Constant adjustment pins. Used to set frequency at which high frequency oscillator switches f1 (by connection of appropriate resistor and capacitor. See Fig. 3)
5	GND	Negative power supply.
6	High f Time Constant	High Frequency Time Constant adjustment pins. Used to set nominal tone output frequency (f_{H1}) (by connection of appropriate resistor and capacitor. See Fig. 3)
8	Output	Tone Output. (Must be capacitively coupled for transformer coupled or resistive loads.)

Fig. 2 - ML8204/ML8205 timing diagram



1. I_{sl} VARIES WITH R_{SL} ON ML8205
2. TRIGGER IN ON ML8204 CONNECTED THROUGH CURRENT LIMITING RESISTOR.

A) OSCILLATION TRIGGERED BY $V_s > V_{si}$.
B) OSCILLATION MAINTAINED UNTIL $V_s < V_{sus}$.
C) OSCILLATION TRIGGERED BY TRIGGER IN HIGH FOR $V_{sus} \leq V_s \leq V_{si}$.
D) OSCILLATION STOPPED BY TRIGGER IN LOW FOR $V_s \geq V_{sus}$.
E) OSCILLATION TRIGGERED BY TRIGGER IN HIGH, MAINTAINED UNTIL $V_s < V_{sus}$.
F) OSCILLATION INHIBITED BY TRIGGER IN LOW FOR $V_s > V_{si}$.

APPLICATIONS

Typical Telephone or Extension Tone Ringer Circuit

The circuit shown in Fig. 3 illustrates the use of the ML8204/8205 devices in a typical telephone or extension tone ringer application. The a.c. ringing voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1. C_1 also provides isolation from d.c. voltages on the line. After full wave rectification by the diode bridge BR_1, the waveform is filtered by capacitor C_4 to provide a d.c. supply for the tone ringer chip. As this voltage exceeds the initiation voltage, V_{si}, oscillation starts. With the components shown, the output frequency chops between 512Hz (f_{H1}) and 640Hz (f_{H2}) at a 10Hz (f_L) rate. The loudspeaker load is coupled through a 1300Ω to 8Ω transformer. While the output impedance of the ML8204 is quite low, the load impedance must be kept fairly high. This is to prevent d.c. power supply regulation problems due to high source impedance of the telephone line and coupling components C_1 and R_1. The output coupling capacitor C_5 is required with transformer coupled loads. The value shown (0.22μF) presents a high enough impedance at the nominal ringing frequency to allow connection of fairly low impedance loads without upsetting the supply regulation. If the load impedance is large enough, then the value of this capacitor can be increased to couple more power to the load without upsetting the power supply to the ML8204. Potentiometer P_1, is used to adjust the audio amplitude and resistor R_4 is a current limiting resistor. Resistor R_5 is a quenching resistor used to limit back emf generated by the inductive load when ringing stops. When driving a piezo-ceramic transducer type load, the coupling capacitor C_5 is not required. However, a current limiting resistor is required as is a 29V zener diode in parallel with the transducer. This diode limits the voltage transients than can generated by mechanical shocking of a piezo-ceramic transducer. The electrical characteristics shown in Table 2 indicate typical performance of this circuit. The incoming ringing voltage and frequency are determined by the telephone system.

Fig. 3 - Typical tone ringer circuit

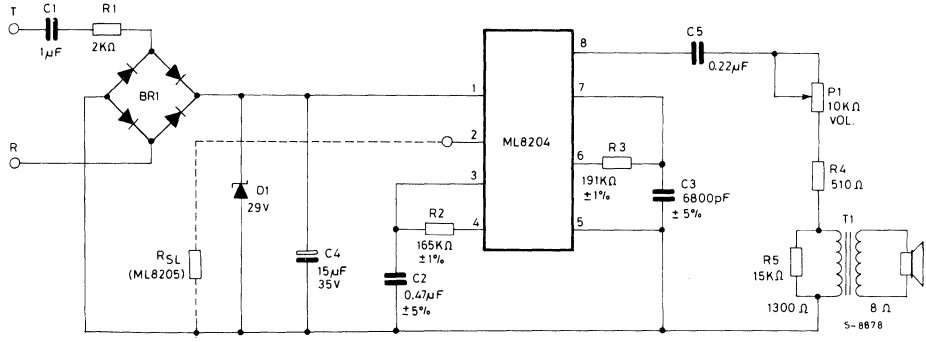


TABLE 2 – TYPICAL ELECTRICAL CHARACTERISTICS OF TONE RINGER CIRCUIT (FIG. 3)

Parameters	Min.	Typ.	Max.	Unit	Parameters	Min.	Typ.	Max.	Unit
Input voltage	75	88	120	V_{rms}	Output frequencies				
					f_L	9	10	11	Hz
Input Frequency	16	20	60	Hz	f_{H1}	461	512	563	Hz
					f_{H2}	576	640	704	Hz
Input Current (when ringing)	–	8	11	mArms					
					Output Voltage (Pin 8 '0' loop)	–	25	–	V_{PP}
Output Power (into 8 transformer coupled load)	–	40	–	mW	Output Sound Pressure	80	85	90	dBA

Use of Trigger In (Pin 2 ML8204)

Pin 2 of the ML8204 may be used to a) externally trigger oscillation for voltages in the range $V_{sus} \leqslant V_s \leqslant V_{si}$, or b) disable ringer operation. The equivalent circuit at pin 2 is shown in Fig. 5. The ringer circuit can only oscillate when Q_1 is conducting. Normally when supply voltage V_s exceeds the supply initiation voltage (V_{si}), base current flows into Q_1, via D_2 and D_1 causing Q_1 to conduct. This continues until V_s is taken below the minimum sustaining voltage (V_{sus}).

The ML8204 can be made to oscillate when powered from supply voltages in the range $V_{sus} \leqslant V_s \leqslant V_{si}$. Oscillation is ensured by forcing a current I_{TR} ($10\mu A \leqslant I_{TR} \leqslant 1mA$) into pin 2 to provide base current to Q_1. This requires the voltage applied to pin 2 to exceed V_{TR} where V_{TR} is the sum of the zener voltage of D_3, the forward voltage drop of D_2 and the V_{BE} of Q_1 (typically 11V). The required current drive can be provided by connecting a resistor R_E between pin 1 and V_s (Fig. 5a); where: $20K\Omega \leqslant R_E \leqslant (V_s - 11)/10M\Omega$. To operate the ML8204 from a d.c. 12V supply, R_E should be typically $50K\Omega$. This mode of operation can also be used to reduce the effective value of the V_{si}, by inserting a zener diode in series with R_E (Fig. 5b). This modifies the initiating voltage to $V_{si(Eff)} = V_{TR} + V_E + 10R_E$ (R_E is in $M\Omega$).

Fig. 4 - Pin 2 input equivalent circuit

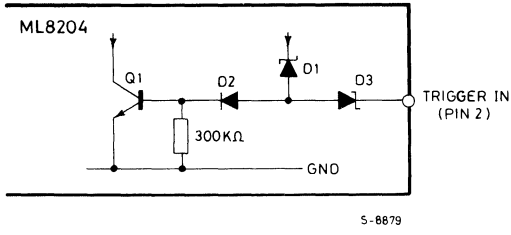


Fig. 5a - Enabling oscillation of the ML8204 for supply voltages less than V_{si}

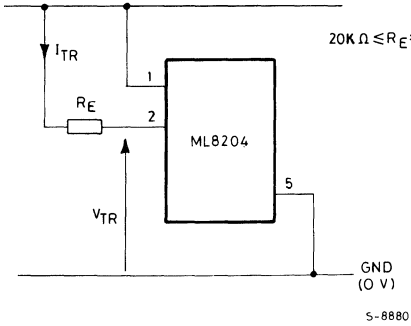
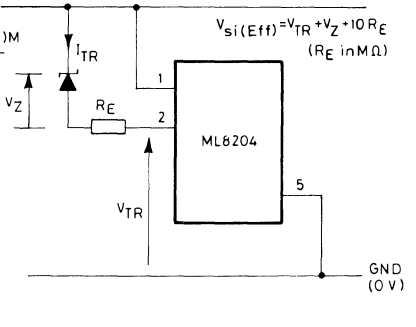


Fig. 5b - Reducing the effective value of V_{si} for the ML8204



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Oscillation of the ML8204 may be inhibited for voltages in the range $V_{si} < V_s \leqslant V_{s(max)}$ by sinking the current from D_1, starving Q_1 of base current. This is achieved by either a) grounding pin 2 (Fig. 6a), or b) applying a voltage V_{INH} via a resistor R_1 to pin 2 (Fig. 6b) to ensure that: $V_{DIS} \leqslant 0.8V$, and $I_{DIS} = \frac{V_{DIS} - V_{INH}}{R_1} \geqslant 40\mu A$.

When driven from a fixed d.c. supply, oscillation of the ML8204 may be gated on or off by CMOS or TTL logic as shown in Fig. 7a and Fig. 7b respectively.

Fig. 6 - Inhibiting oscillation of the ML8204

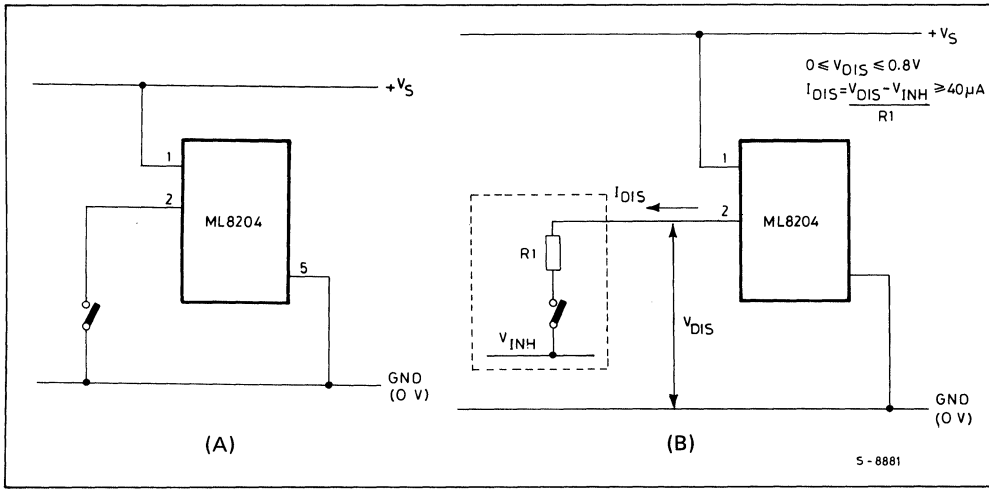


Fig. 7a - Gating the ML8204 from CMOS

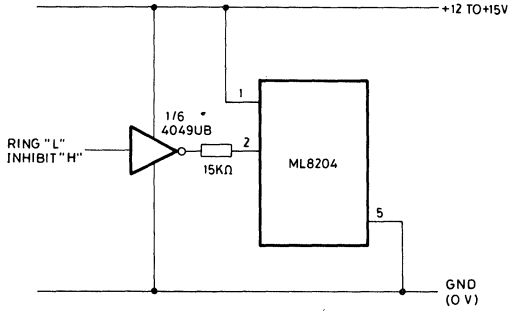
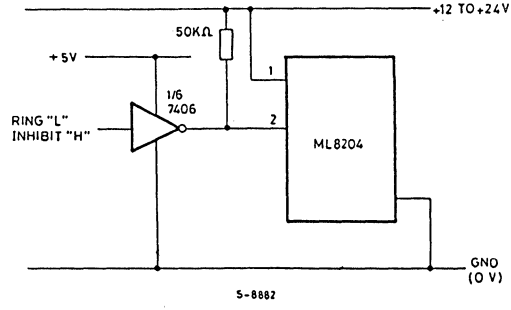


Fig. 7b - Gating the ML8204 from TTL

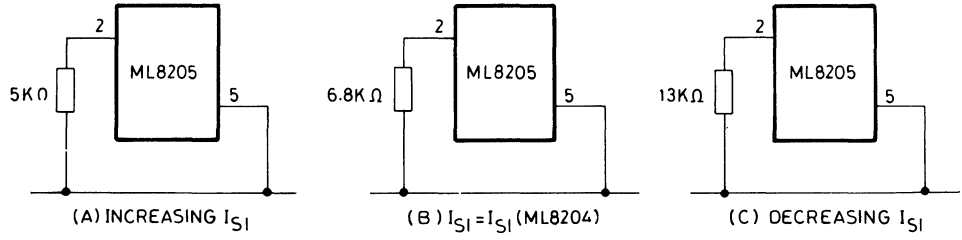


Programming the ML8205 initiation Current

Pin 2 of the ML8205 requires connection of an external resistor R_{SL} (Fig. 8), which is used to program the slope of the supply current vs. supply voltage characteristic, and hence the supply current up to the initiation voltage (V_{si}). This initiation voltage remains constant independent of R_{SL}. The supply initiation current (I_{si}) varies inversely with R_{SL}, decreasing for increasing values of resistance. Thus, increasing the value of R_{SL} will decrease the amount of a.c. ringing current required to trigger the device, As such, longer subscriber loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensate for smaller a.c. line coupling capacitors (providing higher impedance) which can be used alter the ringer equivalence number of a tone ringer circuit.

The graph in Fig. 9a illustrates the variation of supply current with supply voltage of the ML8205. Three curves are drawn to show the change in the slope of the I-V characteristic with R_{SL}. Curve B (R_{SL} = 6.8KΩ) shows the I-V characteristic for the ML8204 tone ringer. Curve A is a plot with R_{SL} = 5.0KΩ and shows an increase in the current drawn up to the initiation voltage V_{si}. The I-V characteristic after initiation remains unchanged. Curve C illustrates the effect of increasing R_{SL} to 13.0KΩ. Initiation current decreases but again current after trigging is unchanged. The variation of I_{si}, with R_{SL} is illustrated in Fig. 9b.

Fig. 8 - Adjusting I_{si} by varying R_{SL}



S-8883

Fig. 9a - I-V slope change due to R_{SL}

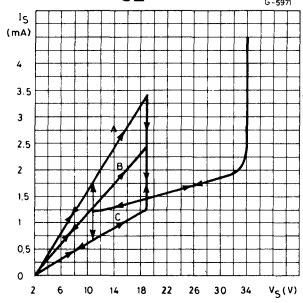
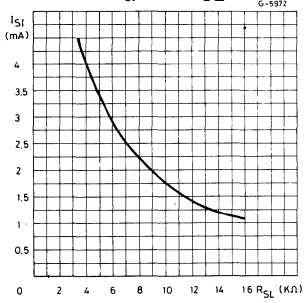


Fig. 9b - Supply initiation current (I_{si}) vs. R_{SL}



Mitel F.C.C. Approved Tone Ringer Module Using ML8205

The Mitel tone ringer module (CM3215) using the Mitel ML8205 tone ringer chip in the circuit below (Fig. 10) has been approved by the F.C.C. (F.C.C. Reg. Number BN285B673550TN). The circuit has been given a ringer equivalence of 0.7 B. This accomplished by increasing the value of R_{SL} to 13KΩ which reduces the supply initiation current (I_{si}). This reduction in I_{si} allows the use of higher line coupling components (R_1 = 8.2KΩ) while ensuring sufficient voltage drop between pins 1 and 5 of the ML8205 for triggering. The 5.1V zener diode D_1 presents a high impedance to low level signals on the telephone line while allowing tone ringer powering from high level rigging voltages.

Transient Overvoltage Testing of the ML8204 Tone Ringer

The following tests were performed to investigate the ability of the ML8204 to withstand transients on its power supply rails. All tests were performed using the circuit shown in Fig. 11 with transient voltage pulses of the form shown in Fig. 12. After each application of a transient pulse, functionality of the device was checked by switching S_1, S_2, and S_3 to the configuration shown in Fig. 11.

Fig. 10 - F.C.C. approved tone ringer circuit

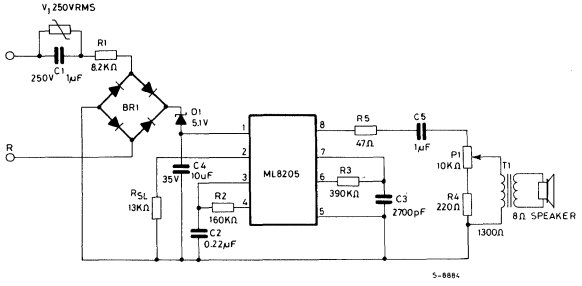
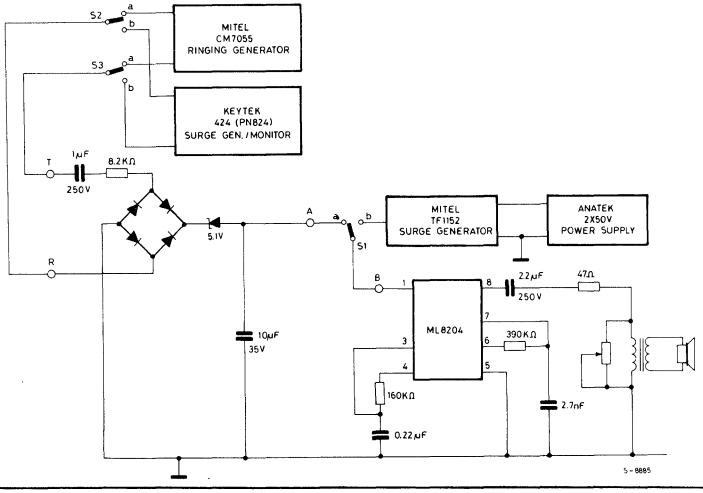


Fig. 11 - ML8204 test circuit (Power supply transients)



The device was tested in two ways by applying pulses: 1) directly into the ML8204 power supply pins, and 2) to the complete ringer circuit TIP and RING inputs. In the first case with S_1 in position "b", a series of pulses with magnitudes (V) from 30V upwards applied from the TF152 until the ML8204 falled to operate. This was repeated for 10 devices. The unloaded value of V at which the devices ceased to operate varied from 84 to 88V (V_{BK}). Subsequently a number of devices were tested by applying 70V pulses to each device. Instability was noted in some devices after 100 pulse applications. All devices ceased to function after 172 to 203 pulse applications. A further set of devices were tested with 64V pulses. All devices withstood 300 pulse applications without any sign of degradation. In the second test, with switches S_2 and S_3 in position "b" and S_1 in position "a", 800 and 1500V pulses were repeatedly applied to the TIP and RING inputs of the circuit. No degradation of the devices' operation was observed.

Fig. 12 - Typical transient test waveform

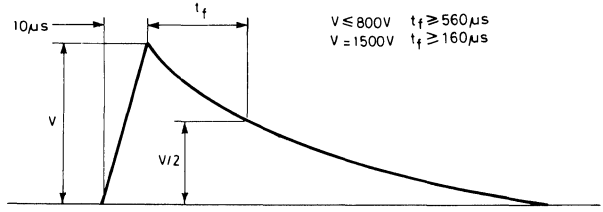
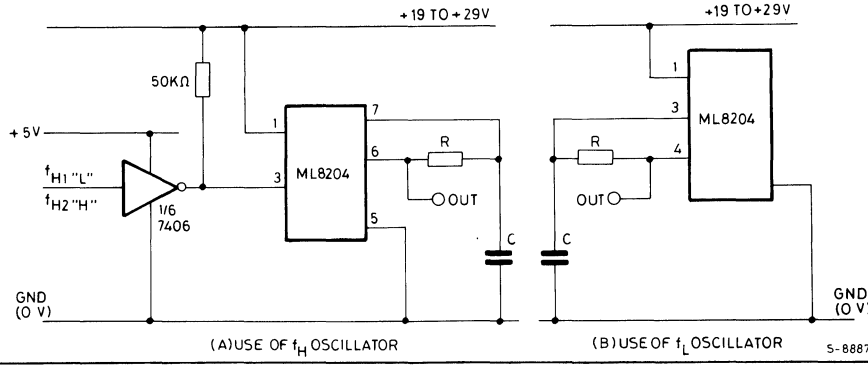


Fig. 13 - Single tone operating of ML8204/ML8205



Single Tone Operation of the ML8204/ML8205

The ML8204/ML8205 can be made to oscillate at one or the other of its output tone frequencies f_{H1} or f_{H2}. To do so, the tone frequency determining components are connected to pins 6 and 7 as normally done. Pin 3 is used as a control input. When pin 3 is connected to V_s, the output (pin 6) will oscillate at the f_{H1} frequency. Conversely, when pin 3 is at ground, the output will oscillate at the f_{H2} frequency. The output can thus be switched between f_{H1} and f_{H2} externally by applying a control signal to pin 3. The low frequency oscillator may also be used separately by connecting the frequency determining components between pins 3 and 4 as normally done. The output is taken from pin 4. However, this is a fairly high impedance output.

Typical Application Circuits for use with a Piezo-electric Transducer

Feedback from a piezo-electric transducer can cause spurious oscillations on the output of a ML8204/5 tone ringer. These oscillations corrupt the normal two-tone output and change as the ringer switches off.

The oscillations occur because the piezo electric transducer resonates at its characteristic frequency. If the resonant amplitude is sufficient to pull pin 8 one bipolar threshold below pin 5 then the tone ringer may give a short spurious pulse.

This effect can be eliminated by using a bypass capacitor across the transducer as shown in Fig. 14. The size of this capacitor is obviously dependent on the piezo-electric transducer used, but a value of 0.1μF is usually sufficient.

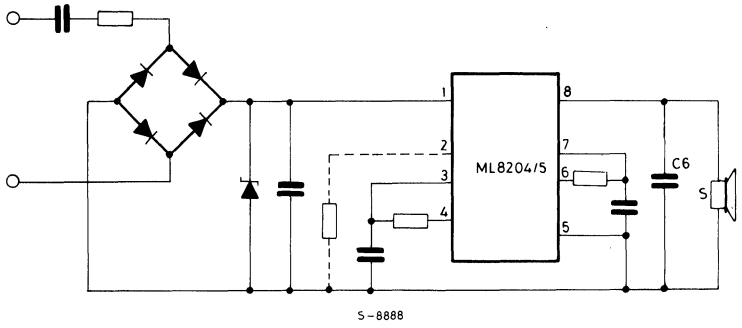
It is possible under specific conditions for a ML8204/5 tone ringer with a piezo-electric load to continue oscillating after the ringing voltage stops.

The ringer can be powered by the smoothing capacitor which is across pins 1 and 5 (see Fig. 14). This causes the device to switch off slowly and since the output frequencies shift by about a musical semitone before oscillation stops, the output can have an unpleasant tail-off.

To eliminate this, a simple monitor can be used which switches the output off when ringing stops. Fig. 16 shows a circuit which works with an ML8204. When ringing voltage is applied from the line, pin 2 is held between 2 and 10V and the device functions normally. When ringing stops, pin 2 is pulled to ground and the ML8204 switches off.

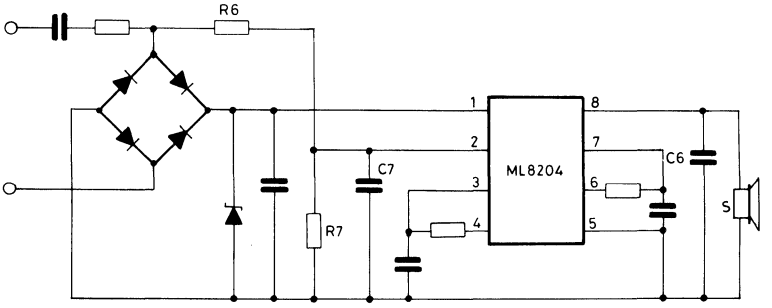
There is no enable on the ML8205 corresponding to pin 2 on the ML8204. Fig. 16 shows a circuit which does not require the enable pin. The output is switched through an NPN transistor instead. During ringing the base of the transistor is forward biased and the load is enabled. When ringing stops the transistor switches off and deactivates the load.

Fig. 14 - Typical application circuit for use with a piezo-electric transducer



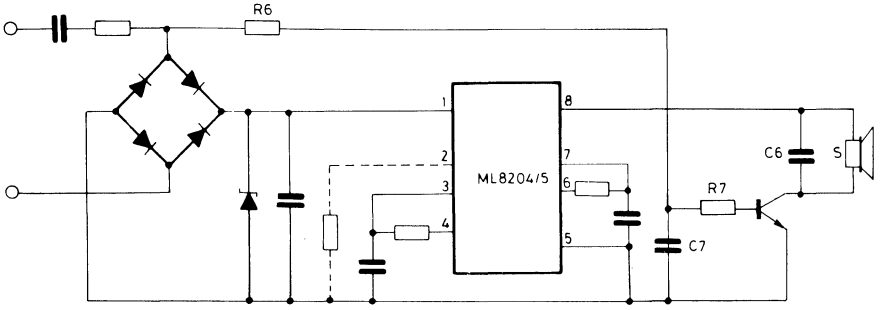
C6 = 0.1μF
S = PIEZO-ELECTRIC TRANSDUCER
OTHER COMPONENTS SAME AS FIGURE 3

Fig. 15 - ML8204 circuit to eliminate tail-off



C6 = 0.1μF
C7 = 4.7μF
R6 = 51KΩ
R7 = 22KΩ
S = PIEZO-ELECTRIC TRANSDUCER
OTHER COMPONENTS SAME AS FIG. 3

Fig. 16 - ML8204/5 circuit to eliminate tail-off



C6 = 0.1μF
C7 = 4.7μF
R6 = 51KΩ
R7 = 22KΩ
S = PIEZO-ELECTRIC TRANSDUCER
OTHER COMPONENTS SAME AS FIG. 3

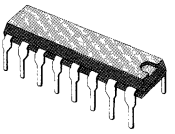
PBD3535

ADVANCE DATA

DTMF GENERATOR

- OPERATES WITH A STANDARD CRYSTAL AT 3.58MHz.
- WIDE OPERATING LINE VOLTAGE AND CURRENT RANGE
- LEVELS FROM THE HIGH AND LOW FREQUENCY GROUP CAN BE ADJUSTED SEPARATELY
- NO INDIVIDUAL LEVEL ADJUSTMENT IS NECESSARY FOR EVERY CIRCUIT
- THE SIGNAL LEVELS ARE STABILIZED AGAINST VARIATIONS IN TEMPERATURE AND LINE VOLTAGE
- SHORT START-UP TIME.
- ALL TONES CAN BE GENERATED SEPARATELY FOR TESTING
- EXTERNAL COMPONENTS ARE MINIMIZED
- EASY PC BOARD LAYOUT; ALL KEYBOARD CONNECTIONS ON ONE SIDE OF THE CHIP
- INTERNAL PROTECTION OF ALL INPUTS
- I^2L PROCESS ENSURES GOOD PARAMETER TOLERANCES

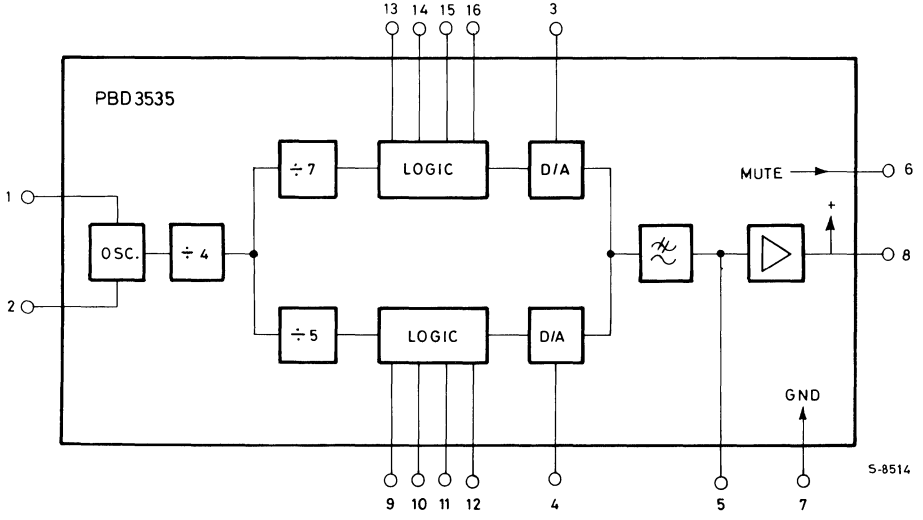
PBD3535 is a monolithic integrated DTMF generator intended for use in a telephone set in parallel with an electronic speech circuit. The DC characteristic to the line is set by the speech circuit. PBD3535 gives a mute signal when sending. The circuit fulfils the CEPT specification. Optional signal levels can be set by resistors. The circuit operates with a single contact matrix keyboard. Interfacing with a computer is also possible.



DIP-16 Plastic (0.4)

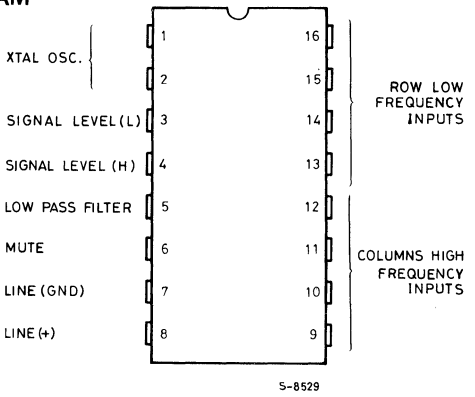
ORDERING NUMBER: PBD 3535

BLOCK DIAGRAM



PBD3535

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Maximum ratings over operating free-air temperature range (unless otherwise stated)

V_L	Max continuous line voltage	15	V
V_L	Peak line voltage pulse time = 2s	20	V
	pulse time = 20 ms	22	V
T_j	Junction temperature	150	°C
T_{amb}	Operating ambient temperature	-20 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

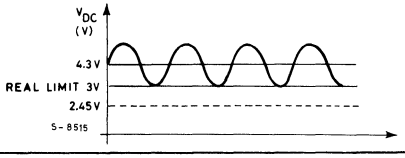
RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Typ.	Max.	Unit
V_L	Line voltage	3		9	V
T_{amb}	Ambient temperature	-20		+70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

Fig. 1 - Min DC level at 1.3V AC signal

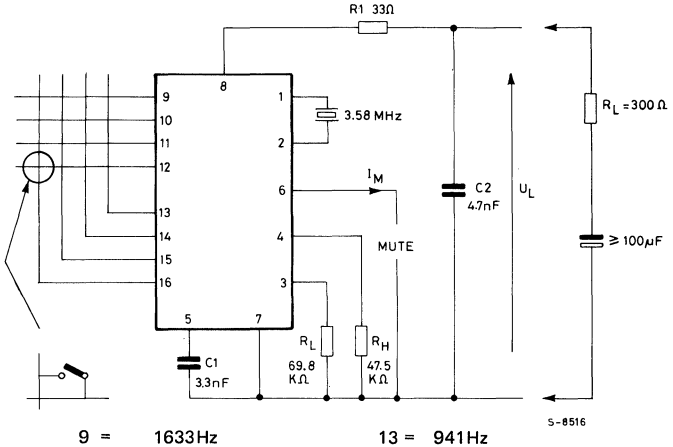


ELECTRICAL CHARACTERISTICS (Electrical characteristics over recommended operating conditions)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_L	Line voltage	Tone generation DC level at 1.3 V_p AC signal	4.3		9	V
V_{DC}	DC voltage below AC voltage	At tone generation	3.0			V
		At tone generation -5°C +45°C	2.45			V
V_L	Line voltage	Stand-by DC level at 2.0 V_p AC signal	4.3		9	V
I_L	Line current	Stand-by: no key pressed V_L = 4.3V			250	μA
I_L	Line current	Operating current V_L = 4.3V			10	mA
I_M	Mute current	One or more keys pressed	125			μA
R_K	Key resistance	Key circuit closed Key open (16 contacts)	 1		1	KΩ MΩ
f_T	Frequency Low	f_{osc} = 3.5795MHz f_1 = 697Hz f_2 = 770Hz f_3 = 852Hz f_4 = 941Hz	 -1 -1 -1 -1	 +0.32 +0.02 +0.03 -0.11	 +1 +1 +1 +1	 % % % %
	Frequency High	f_5 = 1209Hz f_6 = 1336Hz f_7 = 1477Hz f_8 = 1633Hz	-1 -1 -1 -1	-0.03 -0.03 -0.68 -0.36	+1 +1 +1 +1	% % % %
V_H V_L	Signal Level High Signal Level Low	R_H = 47.5KΩ R_L = 69.8KΩ	-11 -13	-9 -11	-7 -9	dBm dBm
V_H V_L V_H V_L		R_H = 33.2KΩ R_L = 48.7KΩ R_H = 26.1KΩ R_L = 39.2KΩ	-8 -10 -6 -8	-6 -8 -4 -6	-4 -6 -2 -4	dBm dBm dBm dBm
$\frac{V_L}{V_H}$	Radio signal level High Freq./Low Freq.		1	2	3	dB
Z_T	Impedance to line	At tone generation	6			KΩ
ZS		At stand-by	50			KΩ
D	Total harmonic distortion	Normal operation Stand-by			-31 -80	dBm dBm
H	Harmonics *	300-3400Hz 3.4-50KHz > 50KHz			-33 -33/-80	dBm dBm
t_s	Start-up time	Output level within 1dB from final level		3	5	ms

* Single tone distortion is less than $(-33 - 12 \times \log \frac{f}{3400})$ dBm

TEST CIRCUIT



9 = 1633Hz
10 = 1477Hz
11 = 1336Hz
12 = 1209Hz
XTAL = 3.5795MHz

13 = 941Hz
14 = 852Hz
15 = 770Hz
16 = 697Hz

FUNCTIONAL DESCRIPTION

Two tones are generated by connecting one input from the high-frequency group and one input from the low-frequency group.

If two or more keys are pressed, no tones other than the basic eight are generated.

All tones can be generated separately. When testing a circuit by connecting one input from the high-frequency group to one input in the low-frequency group plus shorting pin 3 or pin 4 to the ground pin 7, one single tone is generated (low and high frequency, respectively).

The absolute signal level can be adjusted with R_L and R_H, but there is no need for individual adjustment on every circuit. The signal level is stabilized against variations in temperature and line current.

Pause time and signal time are determined externally from the keyboard.

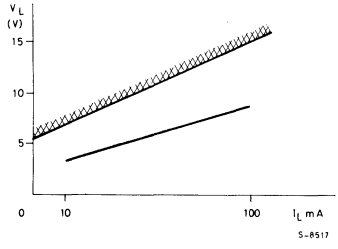
Allowed leakage in keyboard 1MΩ.
Typical threshold is 100KΩ.

The circuit is made to work properly with electronic speech circuits such as PBL 3726.

Component function:

R_1: Protecting resistor;
R_L: Signal level (low);
R_H: Signal level (high);
C_1: Low pass filter;
C_2: Radio frequency suppression (if used together with speech circuit with radio suppression built in, like PBL 3726, C_2 is not necessary.

Fig. 2 - DC characteristics with speech circuit PBL3726/6



To find suitable resistor values for R_H and R_L to get the desired tone levels the following formula can be used for a preliminary calculation. Please note that in R_{LOAD} (f = 1.4KHz) and R_{LOAD} (f = 800Hz) both the impedance of the line and the impedance of the speech circuit are included. V_H and V_L are the desired high and low frequency levels, in dBm.

$$R_H = 56.2 \times R_{LOAD} \ (f = 1.4KHz) \times 10^{-\frac{V_H}{20}}$$

$$R_L = 65.6 \times R_{LOAD} \ (f = 800Hz) \times 10^{-\frac{V_L}{20}}$$

Fig. 3 - Tone level vs. line current

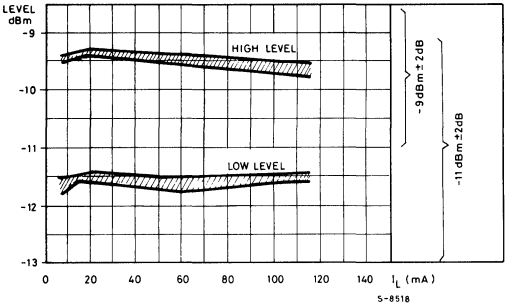
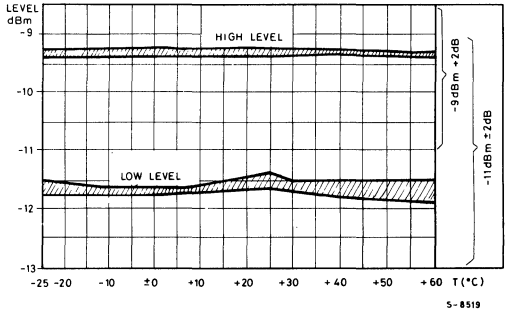


Fig. 4 - Tone level vs. temperature



The current consumption within PBD3535 can be reduced with a resistor connected in parallel with C1 (see fig. 5). If the current reduction is made too large, the output signal can be distorted by clipping.

In applications where a DTMF generator directly powered from the telephone line is wanted (the generator is not working in parallel with any kind of speech network), PBD3535 can be used with a DC regulator as described in fig. 7.

Fig. 5

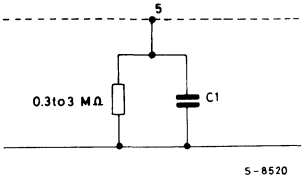
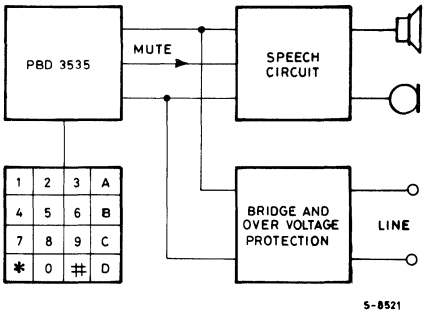
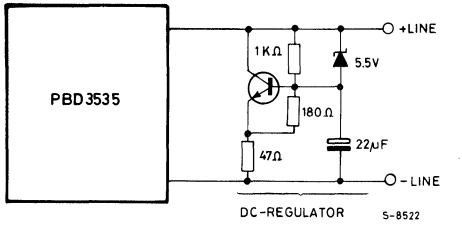


Fig. 6 - Typical application



These schematics give a DC regulator for the range 16-100mA with an output impedance that is a compromise between 600Ω and 900Ω in parallel with 30nF. The zener diode is used to ensure a fast start-up time.

Fig. 7 - DC regulator



For telephone systems with voltage supply instead of current supply) for the telephone line and where the telephone set is supposed to work as a current source, PBD 3535 can be connected with a series regulator as shown in fig. 8.

These schematics are working in the area 5-36V and the output impedance is matched against 600Ω.

PBD 3535 can also be controlled by a microprocessor (see fig. 8). The negative branch of the microprocessor voltage supply is connected to pin 7 of PBD 3535 and the inputs (8) are connected with resistors. For tone-generating one input of the low group (pins 13-16) is connected to the positive voltage and one input of the high group (pins 9-12) is connected to the negative voltage. When an input of the high group (pins 9-12) is connected to the negative voltage, PBD is activated and the mute output is put in high state.

Fig. 8 - DC series regulator

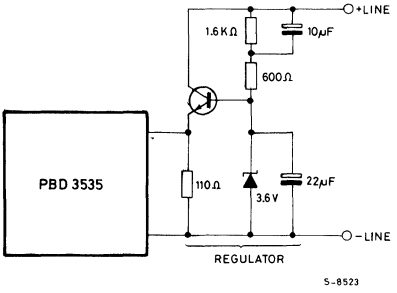
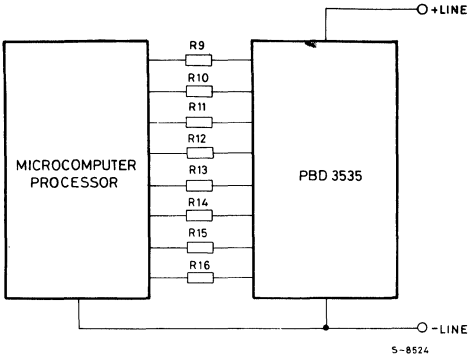


Fig. 9 - Microcomputer interface

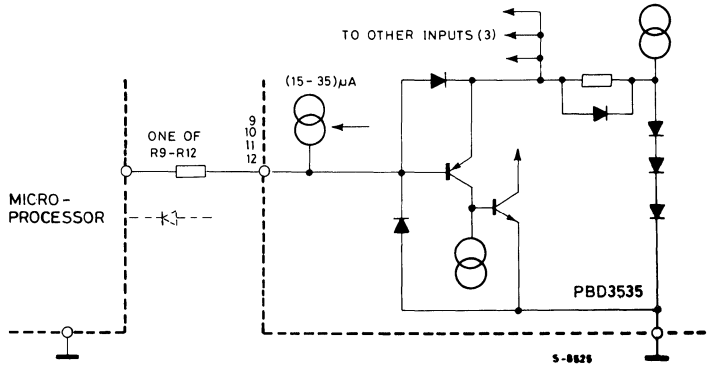


R_9, R_{10}, R_{11} and R_{12}

The resistors have two functions:

- When at low input level, ensure that the input does not get below +0.2V. This must not occur.
- When the input level is high, limit the current. Too high current will interfere with the functions of the other three inputs (the resistors can be exchanged with diodes directly away from PBD 3535).

Fig. 10 - High-frequency group resistors to microcomputer



Example: The logic states very from 0V to +3V. Suitable resistor value is 68KΩ (see fig. 11).

R_{13}, R_{14}, R_{15} and R_{16}

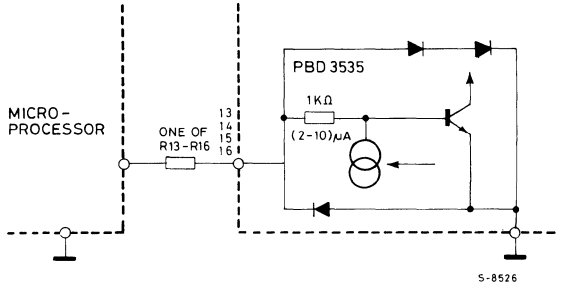
The two functions of the resistors are:

- To raise the OFF/ON Voltage
- To limit the current when the input levels are high

Example: The logic states vary from 0V to +3V. Suitable resistor value is 27KΩ (see fig. 11).

In some telephone instrument designs a click can be heard in the receiver when a button is pressed down for tone signalling. In some applications this has been found desirable as a feedback but in others the effect is not so desirable.

Fig. 11 - Low-frequency group resistors to microcomputer



To suppress the click effect an RC network as seen in fig. 12 can be applied. A capacitor of 47nF halves the loudness of the click and a capacitor of 1.7μF totally cancels the click effect (see fig. 13).

The LS588 speech circuit if specifically developed by SGS for use with the PBD3535 DTMF tone generator. Besides full and independent programmability of both sending and receiving gains when muted the speech circuit reduces its consumption by about 10mA (available to the DTMF circuit), still providing the proper DC and AC (600ohm) impedance to the line.

The external capacitor at pin 16 of LS588 has been reduced from the standard 10μF, usually shown in the SGS application, down to 4.7μF to optimize the DTMF start up without affecting the normal speech operation. (see fig. 14).

Fig. 12 - Click suppression

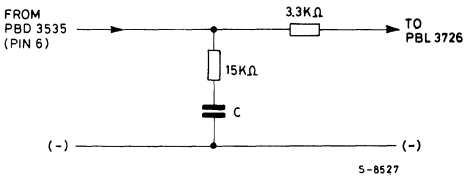


Fig. 13 - Click effect in relative sound pressure

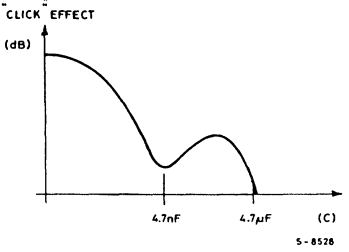
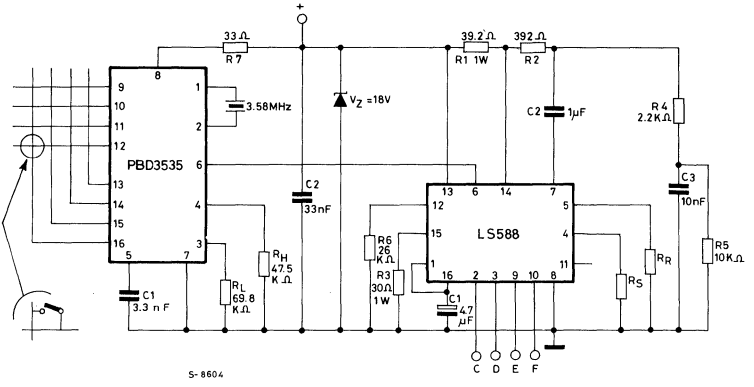


Fig. 14 - PBD3535 application with LS588



PBL3726 Series

PRELIMINARY DATA

MASK-PROGRAMMABLE SPEECH CIRCUITS

Key Options

- MICROPHONE TYPES SUCH AS ELECTRODYNAMIC/MAGNETIC, ELECTRET OR CERAMIC
- POWER SUPPLY FOR EXTERNAL CIRCUITRY
- AGC CIRCUIT
- LINE REGULATION OF TRANSMIT/RECEIVE GAIN FOR CERTAIN TELEPHONE STATION POWER SUPPLIES
- EXTRA POWER SUPPLY INPUTS FOR OUTPUT AMPLIFIER TO BE USED IN HANDS-FREE TELEPHONES
- SPECIAL IMPEDANCE/GAIN REQUIREMENTS
- MUTE OR TRANSMIT/RECEIVE AMPLIFIERS WITH OR WITHOUT CONFIRMATION TONE
- ACOUSTIC SHOCK ARRESTORS
- SIDETONE CANCELLATION CIRCUITRY

Pin Options

- MUTE/NO MUTE FUNCTION
- REGULATION OF SIDETONE WITH LINE LENGTH
- CUT OFF OF ALL LINE REGULATION

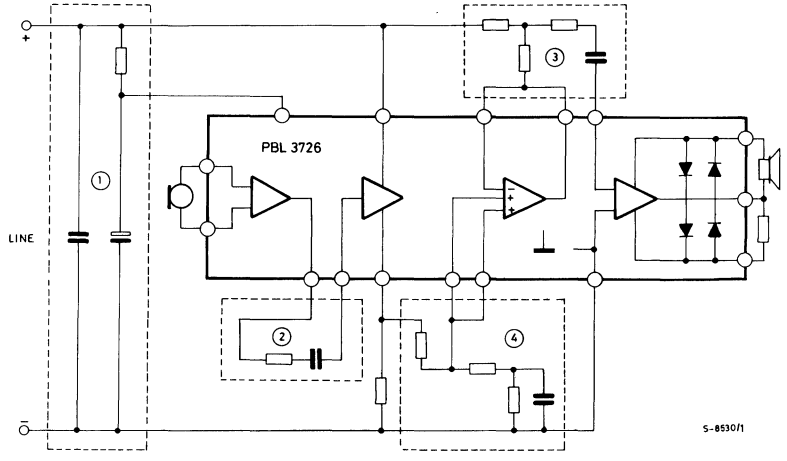
External Components (step by step)

- DC CHARACTERISTICS
- IMPEDANCE
- TRANSMIT GAIN
- TRANSMIT LINEARITY
- RECEIVE GAIN
- RECEIVE LINEARITY
- SIDETONE
- LOW VOLTAGE OPERATION

PBL 3726 is a family of mask-programmable speech circuits intended for various telephone applications. The flexibility of these circuits allows use of versions of PBL 3726 in all telecom markets, whether it be in an ordinary telephone, a hands-free multi-function phone or even as a trunk interface. The versatility is based on three levels:

- Mask options for special requirements
- Pin options on certain functions
- Step-by-step design possibility on the basic telephone functions making it possible to cut down design time to a minimum. This is done by changing the values of a small number of external components.

Fig. 1 - Block diagram and typical application



External RC-networks

① Line impedance and radio interference suppression
② Transmitting amplifier, gain set and frequency adjustment
③ Receiver amplifier, gain set and frequency adjustment
④ Side tone adjustment

PBL3726 Series

ABSOLUTE MAXIMUM RATINGS

Maximum ratings over operating free-air temperature range (unless otherwise stated)

V_{DC}	Line voltage, $t_p = 2s$	22	V
I_{DC}	Continuous operating line current (*)	100	mA
T_j	Junction temperature	+150	°C
T_{amb}	Operating ambient temperature	-40 to +70	°C
T_{stg}	Storage temperature	-55 to +150	°C

(*) Max current increases linearly up to 130 mA with max operating temperature lowered to +55°C

For recommended operating conditions see specific data sheets for different versions of PBL 3726

FUNCTIONAL DESCRIPTION

The gains of the transmitting and receiving amplifiers are continuously and equally changed with the line length. The gain regulation can be cut off externally, and the gain will then be the maximum gain normally used at long lines.

The outputs of the transmitting and receiving amplifiers have internal limitations as to the output amplitudes.

The circuit includes a temperature independent voltage reference used for regulating the DC line current and for regulating the transmitting and receiving gain. The DC voltage quickly settles to its final value with a minimum of overshoot.

The circuit needs few external components. In a normal practical case there are only 5 external capacitors, one of which is an electrolytic/tantalum filter capacitor. The other capacitors are needed for radio interference suppression, to function in the sidetone balancing network, and to provide low frequency cut-off in each of the transmitting and receiving amplifiers.

The circuit has an excellent return loss characteristic against both purely resistive lines such as 600Ω and against complex networks such as 900Ω in parallel with 30nF.

The microphone input is balanced to provide a good CMRR.

It is possible to add a push-button controlled cut-off of the transmitting amplifier of the circuit without disturbing any of the other circuit functions.

A mute input is included to:

1) Cut off the transmitting amplifier (F_1)
2) Reduce gain in the receiving amplifier
3) Reduce current consumption to lower power loss

The DC regulation works independently of the mute function and is not influenced by the mute signal. External mute-control of the circuit from a DTMF generator such as PBD3535 is then possible.

The receiver amplifier is equipped with a high impedance input stage, allowing a less expensive RC network on the input.

Only resistive elements are used to set the receiving gain.

A push-pull power stage in the receiving amplifier provides a high output swing.

The sidetone balance can be set by an RC network without influencing other parameters. An inexpensive solution requires only one capacitor whereas more capacitors may provide better performance. The sidetone can be regulated with respect to line length.

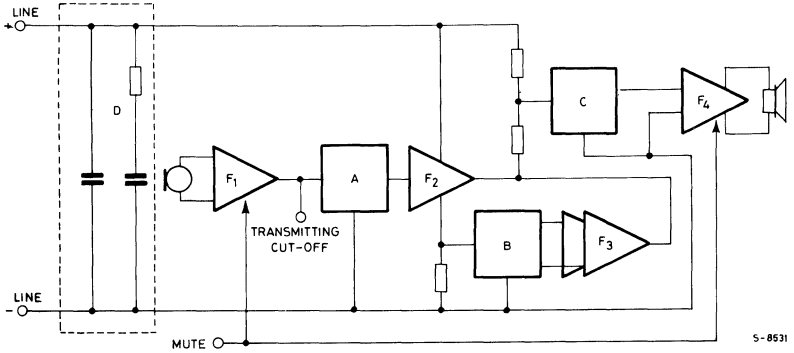
FUNCTIONAL DESCRIPTION (continued)

A separate amplifier stage (F_3) can be used in several different ways, for instance.

1) Separating the sidetone balance network
2) Compensating sidetone level for line length
3) Providing an extra 20dB gain for volume control of the receiving amplifier, etc.

This amplifier has many uses. In the following part only two esamples of its use are given.

Fig. 2



A, B, C and D are RC links with the following functions:

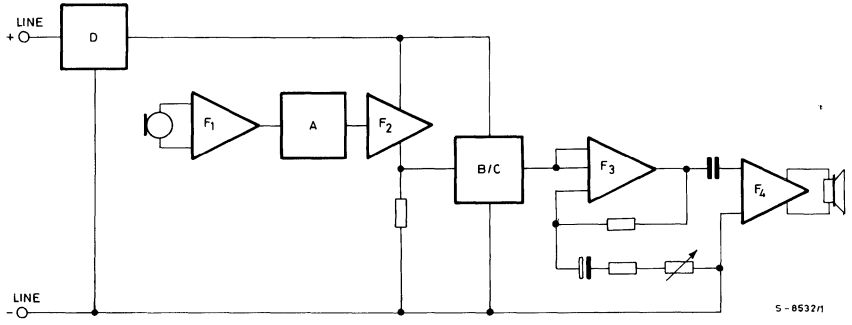
A: To set the gain and frequency response for transmitting

B: To set the sidetone level (regulation with line length is possible)

C: To set the gain and frequency response for receiving

D: For radio interference suppression and to give the correct return loss behaviour

Fig. 3



In this case an extra 20dB amplification is added to the receiving part. A potentiometer provides the possibility of adjusting the gain to the required level.

BASIC EXTERNAL COMPONENTS

R1, R2

These resistors set the starting point for the gain and sidetone regulation.

Input impedance on the regulator is about 52KΩ ± 2%. Only universal versions of PBL 3726 like PBL 3726/6, 3726/9 etc. are equipped with this option. In the data sheets for these versions there is a table showing the R1, R2 values for different central office power supplies. The regulation can also be cut off by leaving R1 open and shorting R2 to -LINE voltage.

For other PBL 3726 versions the regulation is set internally for a specific power supply type.

C1, C2, R3

C1 in series with R3 and these in parallel with C2 determine the impedance to the line from the set.

C2 is normally inserted for radio interference suppression.

The network is optimized with regard to the return loss.

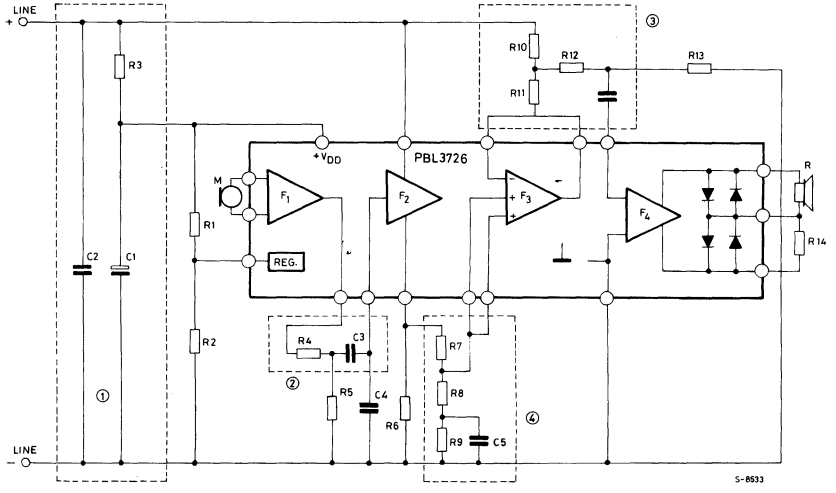
The R3, C1 combination forms a low-pass filter in the DC-feedback loop of the transmitting amplifier. If the R3 C1 time constant is too low there may be distortion at low frequencies.

If R3 is changed this will change the DC characteristics too which is set by the voltage at V_{DD}. The input current at V_{DD} is about 1mA.

R4, R5, C3, C4

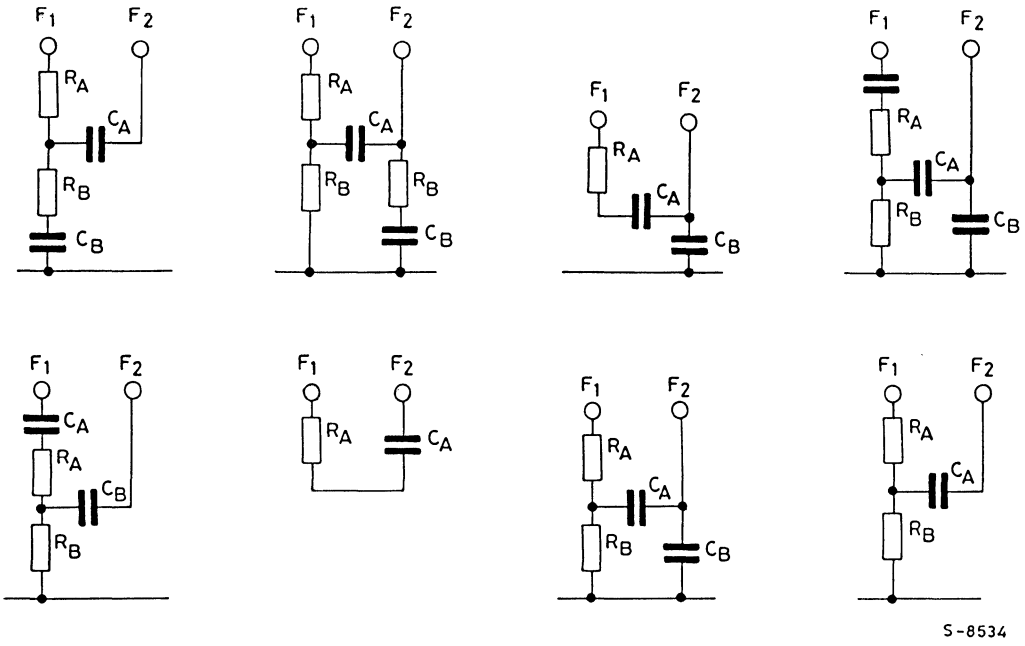
The network gives the amplification and frequency response for the transmitter. R5 is used when a greater reduction of the gain is wanted. Input impedance at F_2 is about 17KΩ with typical variation ± 20%. The DC load on F_1 must be greater than 40KΩ.

Fig. 4 - The PBL3726 and external RC networks



BASIC EXTERNAL COMPONENTS (continued)

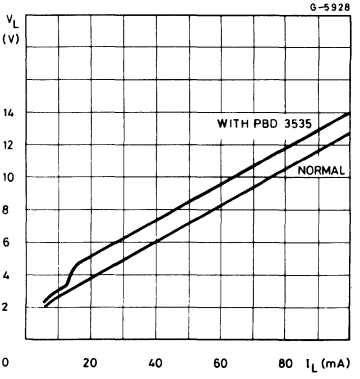
Fig. 5 - Typical filters



R6

Sets the DC Characteristics and dissipates some of the supplied power. The resistor also affects, the transmitter gain, the output amplitude from the transmitter, the gain regulation and the sidetone. Common values are 68Ω to 82Ω.

Fig. 6 - Typical DC characteristics



BASIC EXTERNAL COMPONENTS (continued)

R7, R8, R9, R10, R11, C5

This network sets the sidetone balance. The network in the application is one of many possibilities. R10 and R11 together balance the signals that exit two different ways from the transmitter output stage, one from pin 1 and the other from pin 2. The balance network consists of R8, R9 and C5.

Examples given in the data sheets for different versions of PBL 3726 are not optimized to any specified line; they are given only to show the principle.

Amplifier F_3 has a high input impedance.
Shown in Fig. 7 are some different sidetone networks.

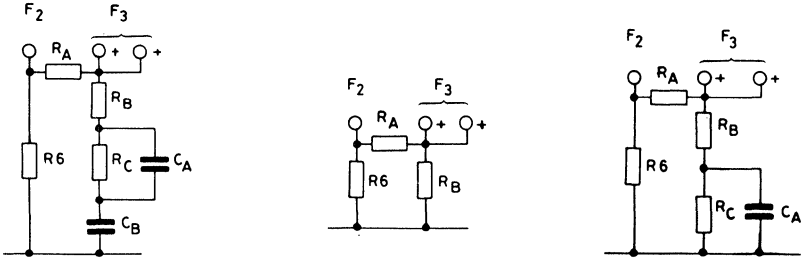
Construction of a sidetone network with regulation according to the above can be done as follows:

The balance impedance A is optimized at a short line where the regulation starts. The balance impedance B is optimized at a long line where the regulation stops. The circuit generates a continuous change between the two balance impedances. R_X insures that no DC voltage shall be between F_3's double positive inputs at the change.

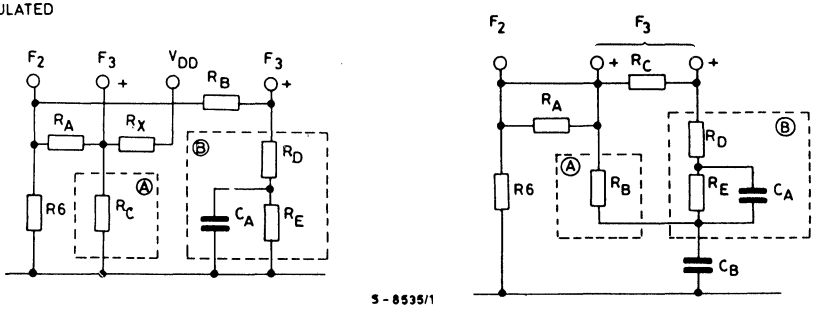
By breaking up between the negative input and output of F_3 it can be used as an amplifier with amplification greater than unit. In Fig. 8 two

Fig. 7 - Sidetone networks

TYPE :UNREGULATED



TYPE : REGULATED



S-8535/1

BASIC EXTERNAL COMPONENTS (continued)

balance networks without F_3 are shown. F_3 can then be used in other applications.

In Fig. 9 a circuit is shown, where F_3 is used as an amplifier with an extra 20 dB gain at receiving and with a volume control.

R12, R13, C6 (R10, R11)

The network gives the gain and frequency response for the receiver.

R13 is used when a greater reduction of the gain is wanted. Input impedance F_4 is about 35KΩ with typical variation ± 20%. For different possibilities for the design of the network, see the network for the transmitter (R4, R5, C3) in Fig. 5.

R14

Generates the output impedance to the magnetic earphone.

If a dynamic earphone is used it should be placed between outer connections. The middle connection is then not used.

This will give about a double output (for the same output current

Rectifier

Rectifier bridge and over-voltage protector. The zener voltage at Fig. 10 should be as low as possible. Common values are between 12V and 16V.

Fig. 9 - 20dB extra amplifier (cannot be used in all version)

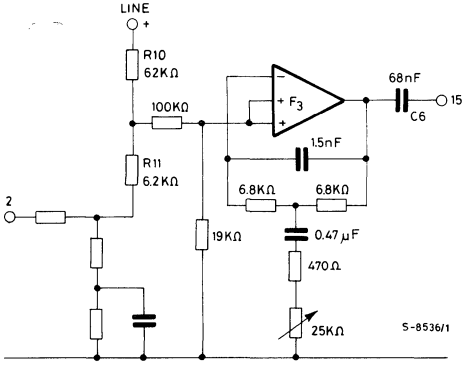


Fig. 8 - Sidetone networks without F_3

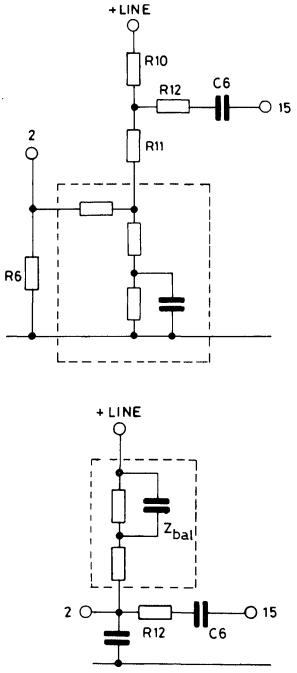
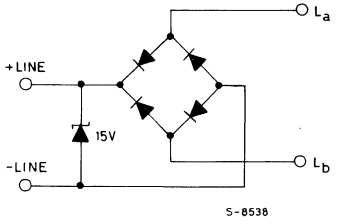


Fig. 10 - Rectifier bridge and overvoltage protection



DESIGN RULES

The following order should always be used when designing telephone parameters.

1) The circuit impedance to the line
2) DC characteristics
3) Gain regulation
4) Transmitter gain and frequency response
5) Receiver gain and frequency response
6) Sidetone

Components usually have to be added to surpress radio interference, especially from the wires up to the handset.

(The circuit can be placed either in the telephone or in the handset.)

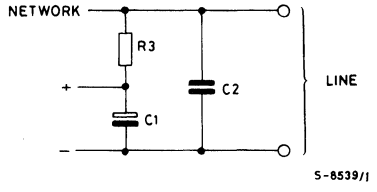
Impedance

This is determined with the components C1, C2, and R3 in most cases. In Fig. 11 a few examples of this are shown. If a more complex impedance is desired as in the example for British Telecom (Fig. 12), this can also be achieved by copying the mathematical model of the desired impedance.

Examples of line impedance matching:

Impedance	R3	C1	C2
600Ω	600Ω	47μF	15nF
900Ω, 30nF	900Ω	47μF	15nF
1.2KΩ,60nF	1.2KΩ	47μF	47nF

Fig. 11 - Typical return loss against 600Ω



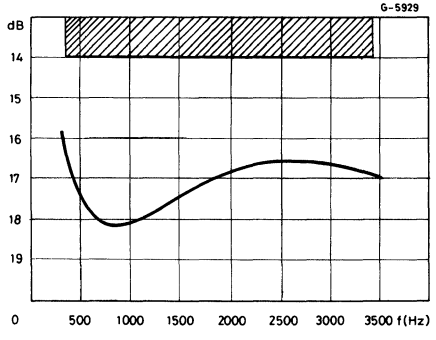
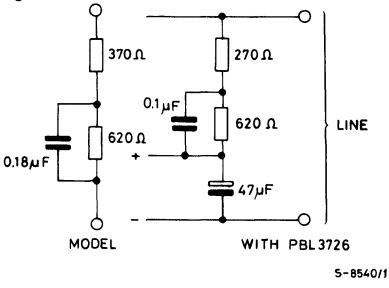


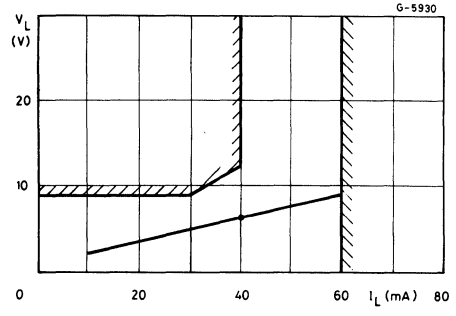
Fig. 12 - Example of complex impedance matching



DC Characteristics

The slope of the DC characteristics is set by the resistor R6 (Fig. 13). The lower value of R6, the flatter the slope. With the steaper slope the

Fig. 13 - Typical DC characteristics



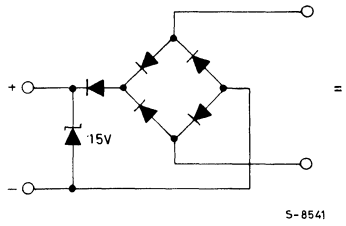
DESIGN RULES (continued)

minimum DC voltage also will go down. It is not recommended, though, to set the PBL 3726 to DC voltages below 2.5V. If in some circumstances the DC characteristics of PBL 3726 is too low, they can be raised by inserting an extra diode in series with the rectifier bridge as in Fig. 14.

Gain regulation

When regulation with line length is used on send and receive gain, this can be set with the resistors R1 and R2. Note that not all versions are equipped with this function. By changing the values of these, the regulation attack can be set to fit any particular need.

Fig. 14 - Rectifier bridge with extra diode



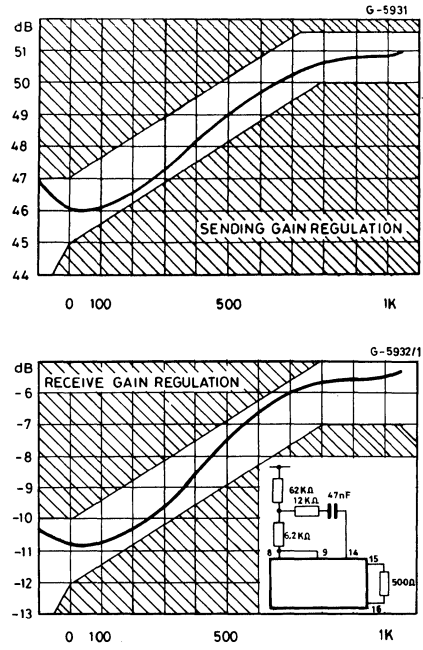
A table in the data sheets shows what values to use for some standard power supply systems. See example in Fig. 15.

Fig. 15 - Examples of line-regulating setting

Line	R1	R2
50V, 2 x 200Ω	18KΩ	47KΩ
50V, 2 x 400Ω	9.1KΩ	4.7KΩ
50V, 2 x 800Ω	0	∞
Unregulated (all lines)	∞	0

Regulation input (pin 6 or PBL 3726/6)

Fig. 16 - Typical gain regulation with line length



Transmitter gain

The resistor R4 sets the gain by attenuating the signal from amplifier F_1. If greater attenuation is needed a resistor (R5) can be connected to the minus line.

To get a frequency response appropriate for the microphone used a filter function as in Fig. 5 can be used. These filters were previously described in this document.

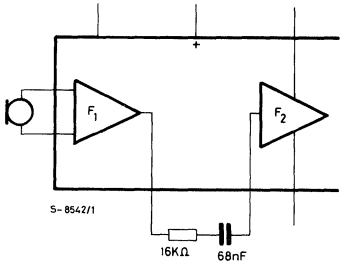
The circuit can be provided with an unbalanced input as in Fig. 18.

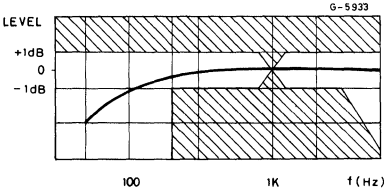
Cut off of the transmitter can be done at F_1 without interfering other functions of the circuit as in Fig. 19.

Also signals other than DTMF signals can be added at input of F_2.

DESIGN RULES (continued)

Fig. 17 - Typical response of PBL 3726 using simple filter





For the version originally developed for electrodynamic/magnetic microphones it is also possible to use electret microphones as shown in Fig. 20.

Receiver gain

In order to get the correct gain on the receive side, resistors R10 - R13 are used. Remember that R10 and R11 also set the rough ratio of the sidetone. R13 is used only in extreme circum-

Fig. 18 -Unbalanced input

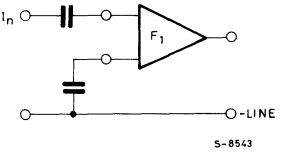


Fig. 19 -Special function

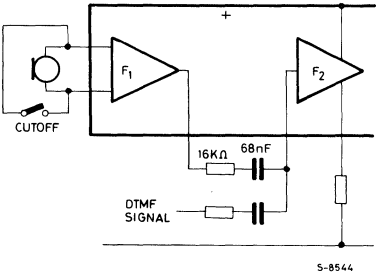
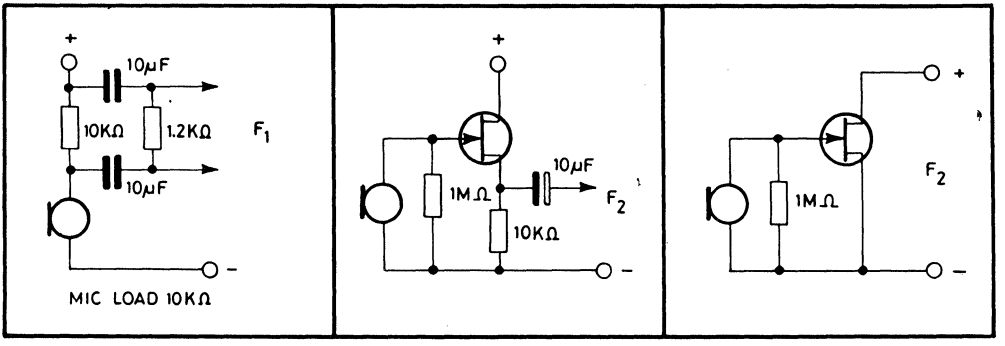


Fig. 20 - Alternative microphones of electromagnetic and electrodynamic types for PBL 3726



a. Electret without source-follower

b. Electret with source-follower 3-lead.

c. Electret with source-follower 2-lead.

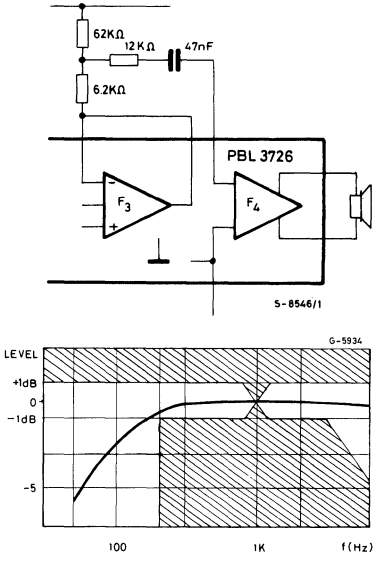
β-8545/1

DESIGN RULES (continued)

stances, where a very high receive gain attenuation is needed. The frequency response can be altered with the same filters used for the send gain (see Fig. 5). To get protection against acoustic shock the diodes provided on some versions after the output of F_4 can be used.

One or two diode pairs can be used. Should this not be enough a resistor can be connected after the diodes (in series). This should be done before the setting of the receive gain.

Fig. 21 - Typical receive gain



Sidetone

$$STMR = -\frac{10}{m} \times 10_{log} \left\{ \sum_{i=1}^{14} 10^{-\frac{m}{10}(W_{ST} + L_E - S_S + S_R + A_{rst})} \right\}$$

The most difficult part of the design work is always to define the sidetone. This should always be done last when designing with PBL 3726. The sidetone is the sound of your own voice fed back into the ear by the handset.

The subjective effect of this is best seen in the formula above for "Side Tone Masking Rating".

Summed at the frequencies $f_i = 0.2$, 0.25 . . . . . 4KHz (see Fig. 22)

W_{ST} = Weighing factor
L_E = Leakage at receiver capsule
S_S = Send sensitivity
S_R = Receive sensitivity
A_{rst} = Hybrid-loss balance

The part that can be alteren by the speech circuit is the A_{rst} value that can be determined by the formula:

$$A_{rst} = 20\ 10_{log} \left[\frac{Z_C + Z_{SO}}{2\,Z_C} \times \frac{Z + Z_C}{Z - Z_{SO}} \right]$$

where:

Z = Impedance of the connected telephone line

Z_{SO} = The balance impedance of the central office (PABX)

Z_C = Impedance of the speech circuit

The sum of Z and Z_{SO} can be called Z_{line}

The principle of the traditional so called active speech circuit has been the wheatstone bridge (Fig. 23). The formula for the minimum sidetone is to balance until:

$$\frac{Z_2}{Z_1} = \frac{Z_{bal}}{Z_{line}}$$

Fig. 22 - CCITT factors

f_i KHz	W_{ST} dB	L_E dB
0.2	86.4	8.4
0.25	81.9	4.9
0.315	78.5	1
0.4	78.2	-0.7
0.5	72.8	-2.2
0.63	67.6	-2.6
0.8	58.4	-3.2
1	49.7	-2.3
1.25	48.0	-1.2
1.6	48.7	-0.1
2	50.7	3.6
2.5	49.8	7.4
3.15	48.4	6.7
4	49.2	8.8

DESIGN ROULES (continued)

The principle of PBL 3726 is more complicated (even if calculation with the bridge in Fig. 23 is possible). With the all-active bridge a method of cancelling the sidetone is a summing amplifier makes it possible to get not only one but two different sidetone optimums for different line lengths (see Fig. 25). The function of the external components in Fig. 7 have previously been described in this document. Fig. 26 shows an example of a sidetone network using the Wheatstone principle with PBL 3726.

Fig. 23 - Balance bridge

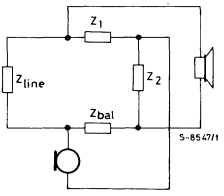
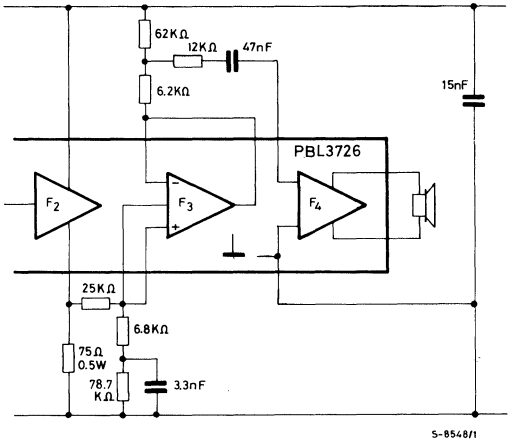
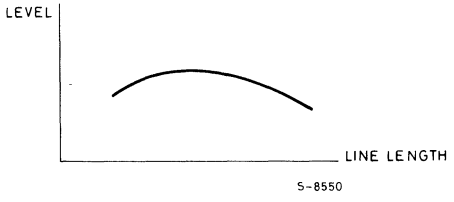
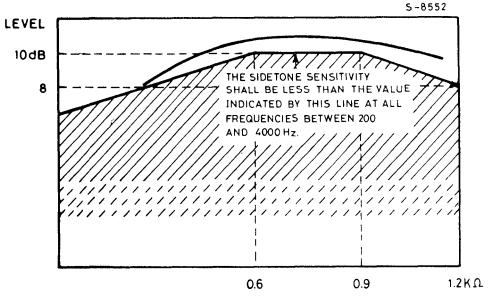


Fig. 24 - Unregulated sidetone network

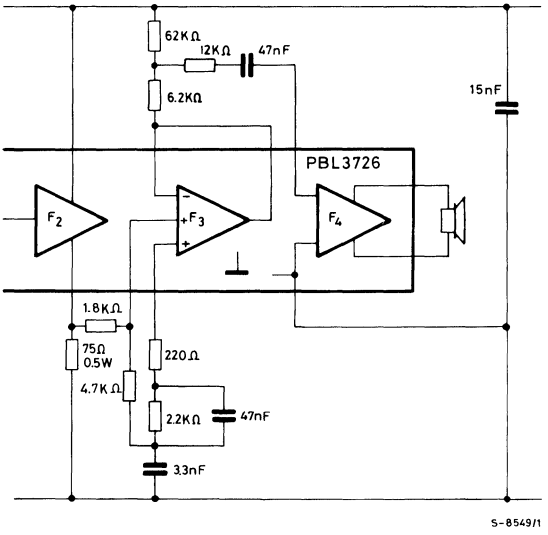


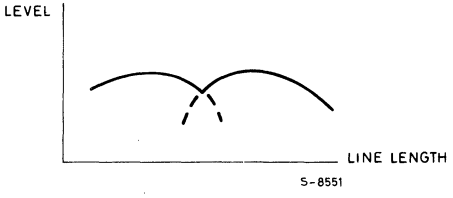


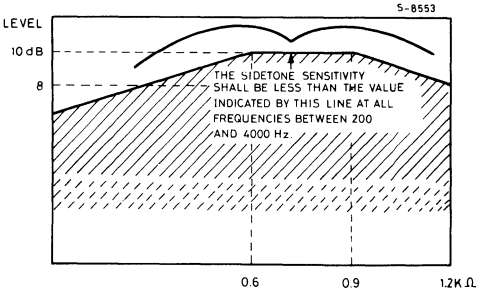


DESIGNE RULES (continued)

Fig. 25 - Regulated sidetone network

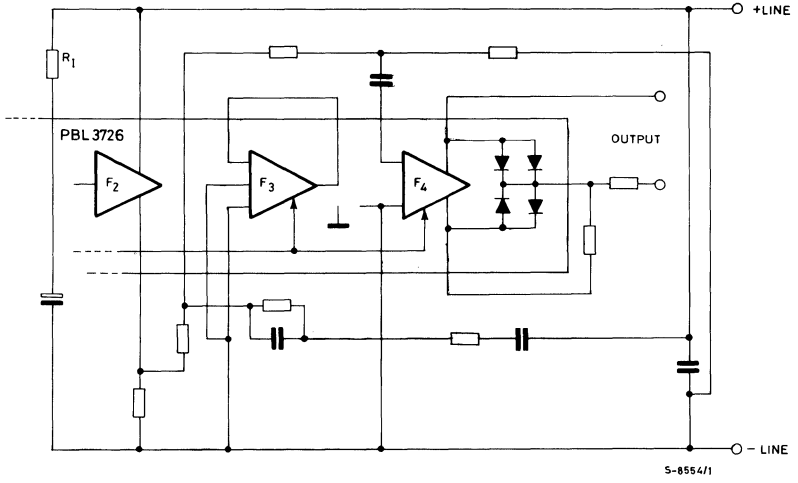






DESIGNE RULES (continued)

Fig. 26 - Wheatstone type sidetone network



PRODUCT SUMMARY

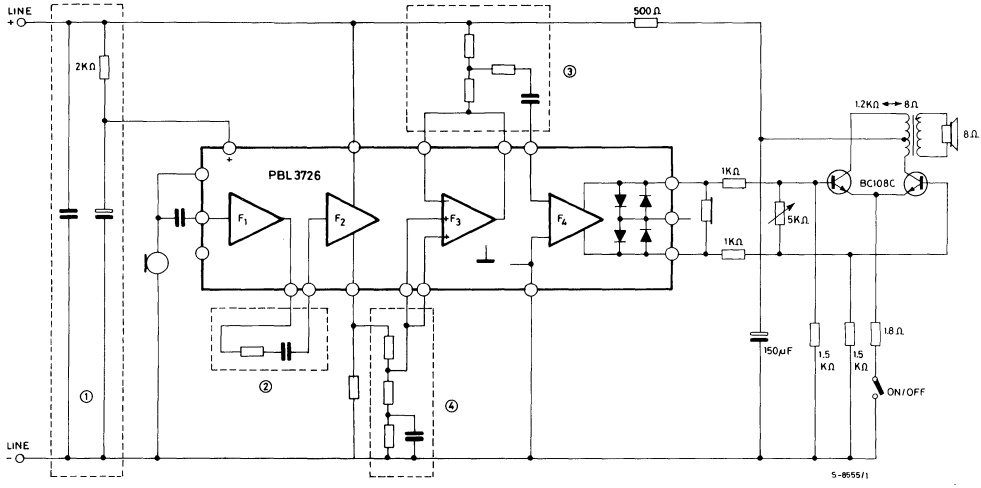
Speech circuit	Microphone				Line	Regulated sidetone	Extra receive amp	Low cost speak phone	Click suppressor	Split power supply for output amp
	Carbon	Electro magnetic	Electro dynamic	Elec tret						
PBL 3726/6		•	•		Adjustable	•	•	•	•	
PBL 3726/8	•			•	36V, 2 x 500Ω 50V, 2 x 800Ω	•	•	•	•	
PBL 3726/9	•			•	Adjustable	•	•	•	•	
PBL 3726/11		•	•			•	•	•	•	
PBL 3726/12		•	•		Adjustable	•	•	•	•	•

APPLICATIONS

To use PBL 3726 in a hands-free telephone with a monitor function the schematics in Fig. 27 can be used. The transformer should be rather efficient. Ordinary transistors can be used.

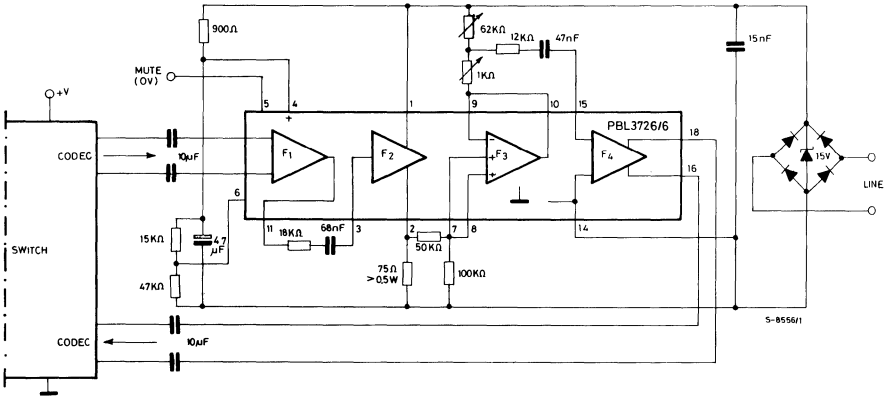
PBL 3726 can also be used as trunk interface in modems, PABX, key systems etc where an analog interface against the telephone line is needed. The balanced inputs and outputs make this possible together with the possibility of regulated sidetone. Examples of both one-way and two-way data/signal communication with PBL 3726/6 are shown in Fig. 28.

Fig. 27 - Monitor loudspeaker



Two - Way communication (send/receive)

Fig. 28 - Trunk interface applications



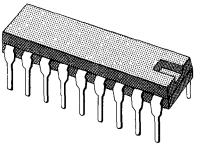
PBL3726/6

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 5 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATING WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATING, DOWN TO 3.3V
- VERY SHORT START-UP TIME

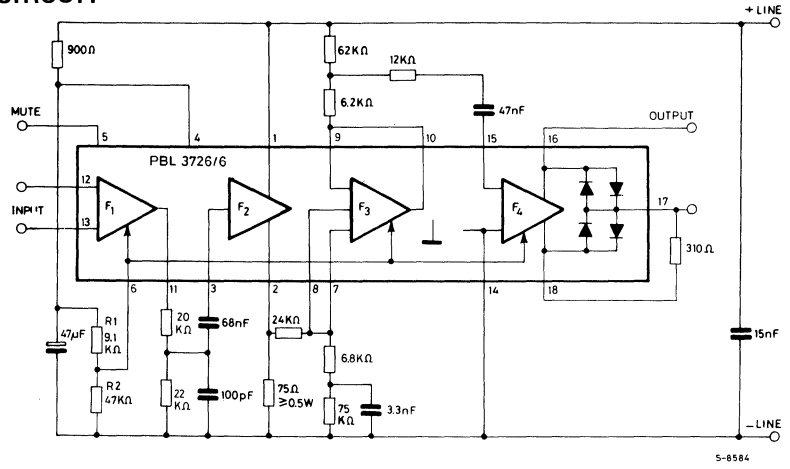
PBL 3726/6 is standard version of the PBL 3726 family of the mask-programmable, monolithic integrated speech circuits for use with a low impedance microphone. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained with external resistor or totally cut off. Typical current feeds as 48V 2 x 200Ω 2 x 400Ω and 36V 2 x 250Ω can be handled.

Application-dependent parameters as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.



DIP-18 Plastic
(0.4)

TEST CIRCUIT



Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table.

Type	R1	R2
No regulation, all feeding systems	∞	0
48V, 2 x 200Ω	16KΩ	47KΩ
48V, 2 x 400Ω	9.1KΩ	47KΩ
36V, 2 x 500Ω	0	∞

ABSOLUTE MAXIMUM RATINGS Maximum ratings over operating free-air temperature range (unless otherwise stated)

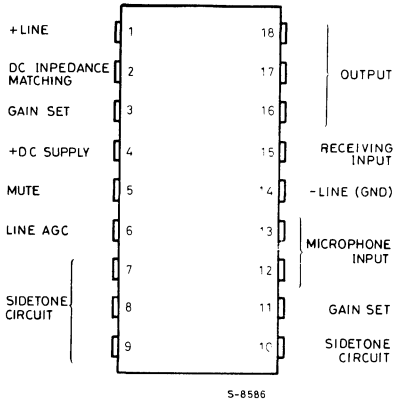
V_{DC}	Line voltage, $t_p = 2s$	22	V
I_{DC} (*)	Continuous operating line current	100	mA
T_j	Junction temperature	150	°C
T_{amb}	Operating ambient temperature	-40 to +70	°C
T_{stg}	Storage temperature	-55 to +150	°C

(*) Max current increases linearly up to 130mA with max operating temperature lowered to +55°C

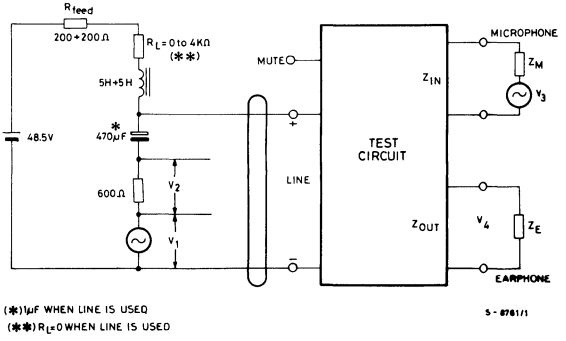
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line Current	15		100	mA

CONNECTION DIAGRAM



Test set-up



THERMAL DATA

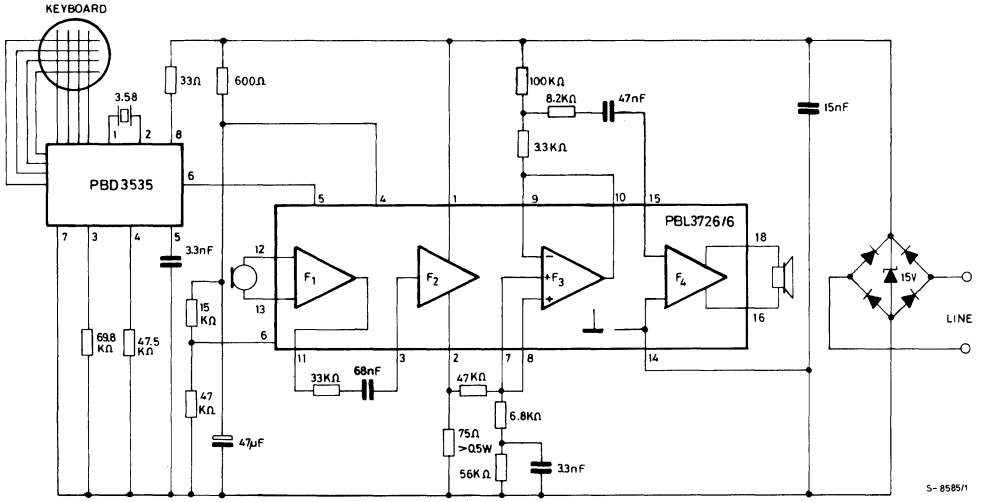
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Electrical characteristics over recommended operating conditions)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal voltage	I_{DC} = 15mA I_{DC} = 100mA	3.3 11	3.7 13	4.1 15	V V
G_T	Transmitting gain *	$20 \cdot \log_{10} (\frac{V_2}{V_3})$ 1KHz R_L = 0 E = E + 10% R_L = 400Ω R_L = 900Ω - 2.2KΩ	 41 43.5 46	 43 45.5 48	 45 47.5 50	 dB dB dB
REG_T	Transmitting range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_T	Transmitting frequency response	200Hz to 3.4KHz	-1		1	dB
G_R	Receiving gain *	$20 \cdot \log_{10} (\frac{V_4}{V_1})$ 1KHz R_L = 0Ω E = E + 10% R_L = 400Ω R_L = 900Ω - 2.2KΩ	 -18.5 -16 -13.5	 -16.5 -14 -11.5	 -14.5 -12 -9.5	 dB dB dB
REG_R	Receiving range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_R	Receiving frequency response	200Hz to 3.4KHz	-1		1	dB
Z_{IN}	Transmitter input impedance	1KHz		1.1		KΩ
V_T	Transmitter dynamic output	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA		1.5		V_p
V_T	Transmitter max output	200Hz - 3.4KHz I_{DC} = 0 - 100mA V_3 = 0 - 1V		3		V_p
Z_{OUT}	Receiver output impedance	1KHz		3 + 310		Ω
	Receiver dynamic output **	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA	0.5	0.55		V_p
V_R	Receiver max output	Measured with line rectifier 200Hz - 3.4KHz I_{DC} = 0 - 100mA V_1 = 0 - 50V		0.9		V_p
N_T	Transmitter output noise	P_{sof}-weighted, REL 1V R_L 0		-75		dB_{psof}
N_R	Receiver output noise	A-weighted, REL 1V, with cable 0-5 Km ϕ 0.5 mm; 0-3 Km ϕ 0.4 mm		-85		dB_A
I_M	Mute input current		0.1			mA
I_{DC}	Extra available current when muted at the same DC-voltage	I_{DC} = 15 - 100mA		10		mA

* Adjustable to both higher and lower values with external components
** The dynamic output can be doubled. See application notes at R14

Fig. 1 - Typical application with DTMF generator PBD 3535



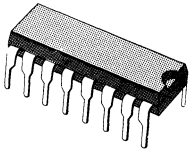
PBL3726/8

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 6 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- CURRENT-SOURCE GENERATOR FOR ACTIVE MICROPHONES

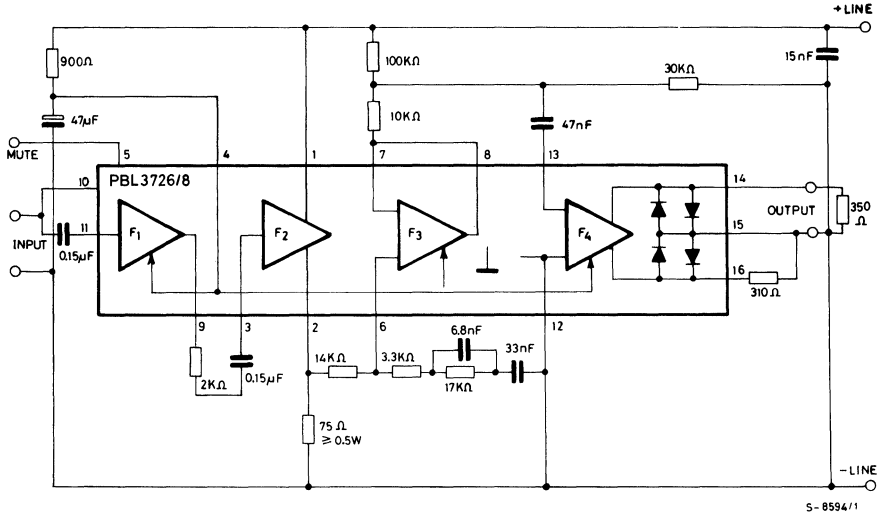
PBL 3726/8 is a standard version of the PBL 3726 family of the mask-programmable, monolithic integrated speech circuits for use in electronic telephones. It is designed for use with a low impedance microphone. Sending and receiving gain is regulated with the line length. Different ranges of amplifier regulation for various current feeds can be obtained by mask programming. Typical current feeds such as 48V 2 x 800Ω, and 36V 2 x 500Ω can be handled.

Application-dependent parameters are line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.



DIP-16 Plastic
(0.4)

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

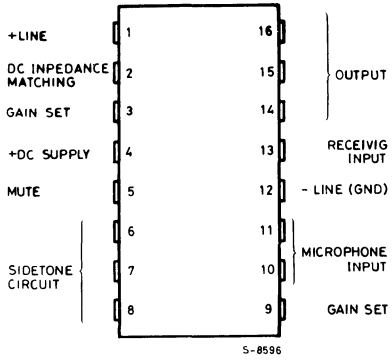
Maximum ratings over operating free-air temperature range (unless otherwise stated)

V_{DC}	Line voltage, t_p = 2s	22	V
I_{DC}	Continuous operating line current	100	mA
T_j	Junction temperature	150	°C
T_{amb}	Operating ambient temperature	-40 to +70	°C
T_{stg}	Storage temperature	-55 to 150	°C

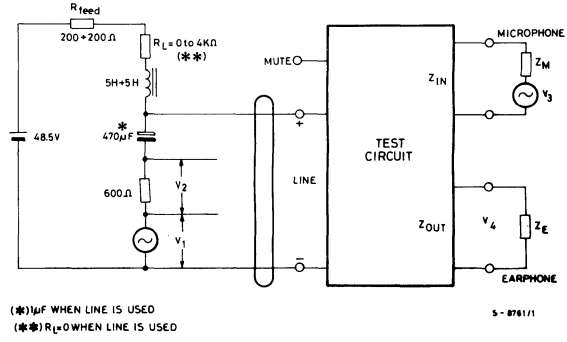
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line current	10		60	mA
T_{amb}	Ambient temperature	-15		45	°C

CONNECTION DIAGRAM



Test set-up



THERMAL DATA

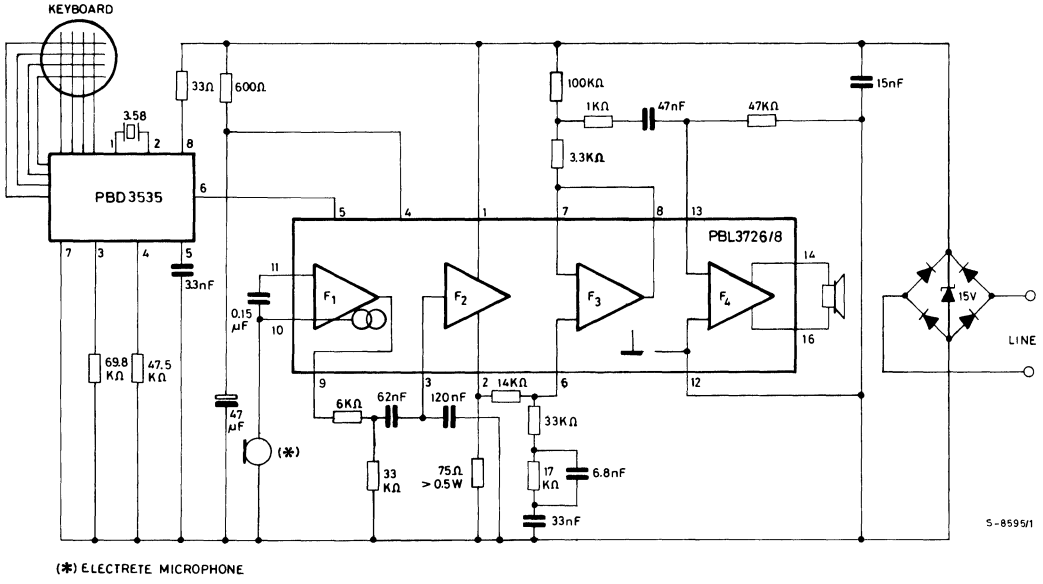
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Electrical characteristics over recommended operating conditions)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal voltage	I_{DC} = 10mA I_{DC} = 60mA	3.0 7	3.5 9	4.0 10.5	V V
G_T	Transmitting gain *	$20 \cdot \log_{10} (\frac{V_2}{V_3})$ 1KHz R_L = 0 E = E + 10% R_L = 400Ω R_L = 900Ω - 2.2KΩ	 33 35.5 38	 34 36.5 39	 35 37.5 40	 dB dB dB
REG_T	Transmitting range of regulation	1KHz R_L = 0Ω, E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_T	Transmitting frequency response	200Hz to 3.4KHz	-1		1	dB
G_R	Receiving gain *	$20 \cdot \log_{10} (\frac{V_4}{V_1})$ 1KHz R_L = 0Ω E = E + 10%	 -17	 -15	 -13	 dB
REG_R	Receiving range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_R	Receiving frequency response	200Hz to 3.4KHz	-1		1	dB
Z_{IN}	Transmitter input impedance	1KHz	17	20		KΩ
V_T	Transmitter dynamic output	200Hz - 3.4Hz ⩽ 2% distortion I_{DC} = 11.25 - 50mA	1.1			V_p
V_T	Transmitter max output	200Hz - 3.4KHz I_{DC} = 0 - 50mA V_3 = 0 - 1V			3	V_p
Z_{OUT}	Receiver output impedance	1KHz		3 + 310		Ω
V_R	Receiver dynamic output **	200Hz - 3.4KHz ⩽ 3% distortion I_{DC} = 11.25 - 50mA	0.4			V_p
V_R	Receiver max output	Measured with line rectifier 200Hz - 3.4KHz I_{DC} = 0 - 50mA V_1 = 0 - 50V			0.9	V_p
N_T	Transmitter output noise	P_{sof}-weighted, REL 1V R_L = 0		-75		dB_{psof}
N_R	Receiver output noise	A-weighted, REL 1V, with cable 0 - 5 Km ϕ 0.5 mm; 0 - 3 Km ϕ 0.4 mm		-85		dB_A
I_M	Mute input current		0.1			mA
V_{DCM}	Minimum DC-line voltage when muted	I_{DC} = 2.5mA I_M = 0.1mA	3.0			V
I_S	Supply current for microphone amplifier	I_{DC} = 11.25 - 50mA	300			μA
I_{DC}	DC voltage for microphone amplifier	I_{DC} = 11.25 - 50mA			2	V

* Adjustable to both higher and lower values with external components
** The dynamic output can be doubled. See application notes at R14

Fig. 1 - Typical application with DTMF generator PBD 3535



(*) ELECTRETE MICROPHONE

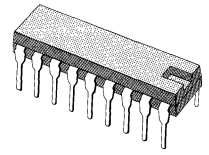
PBL3726/9

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 6 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- INTERNAL CURRENT-SOURCE GENERATOR FOR BUFFER AMPLIFIER OR A SIMILAR DEVICE

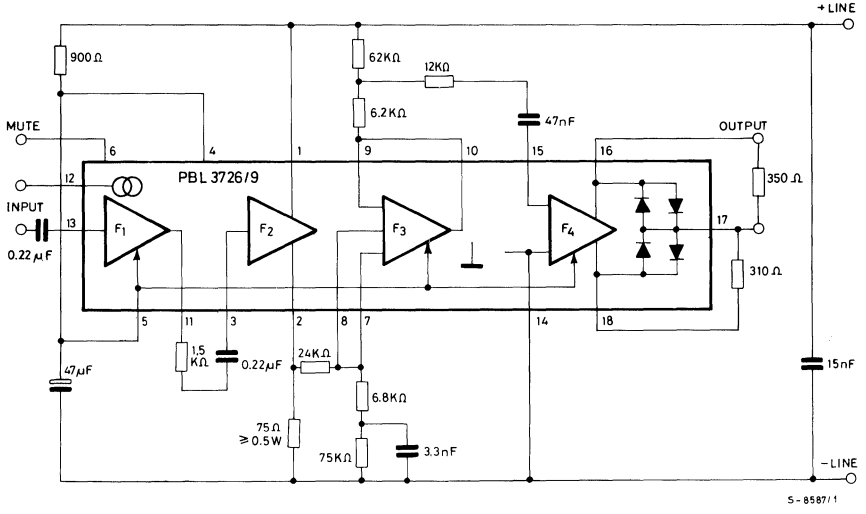
PBL 3726/9 is a standard version of the PBL 3726 family of the mask-programmable, monolithic integrated speech circuit for use in electronic telephones. It is designed for use with electret microphone with a buffer amplifier. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained. Typical current feeds as 48V 2 x 200Ω, 2 x 400Ω and 36V 2 x 250Ω can be handled.

Application-dependent parameters such as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.



DIP-18 Plastic
(0.4)

TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS Maximum ratings over operating free-air temperature range (unless otherwise stated)

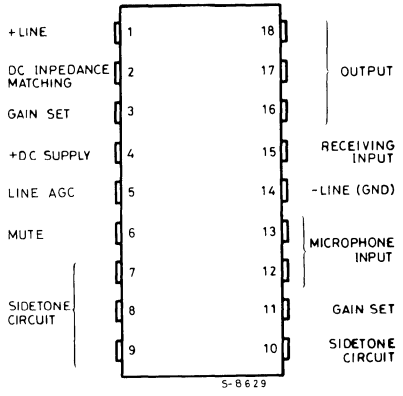
V_{DC}	Line voltage, $t_p = 2s$	22	V
I_{DC} (*)	Continuous operating line current	100	mA
T_j	Junction temperature	150	°C
T_{amb}	Operating ambient temperature	-40 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

(*) Max. current increases linearly up to 130mA with max operating temperature lowered to +55°C

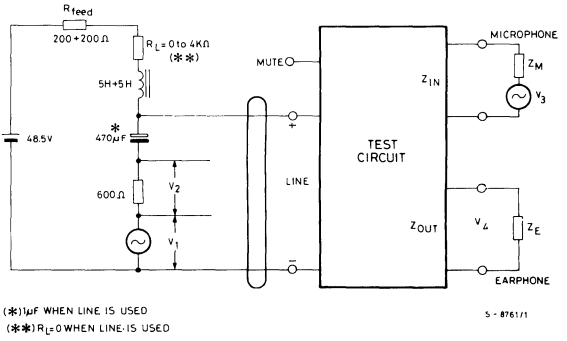
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line current	15		100	mA

CONNECTION DIAGRAM



Test set-up



THERMAL DATA

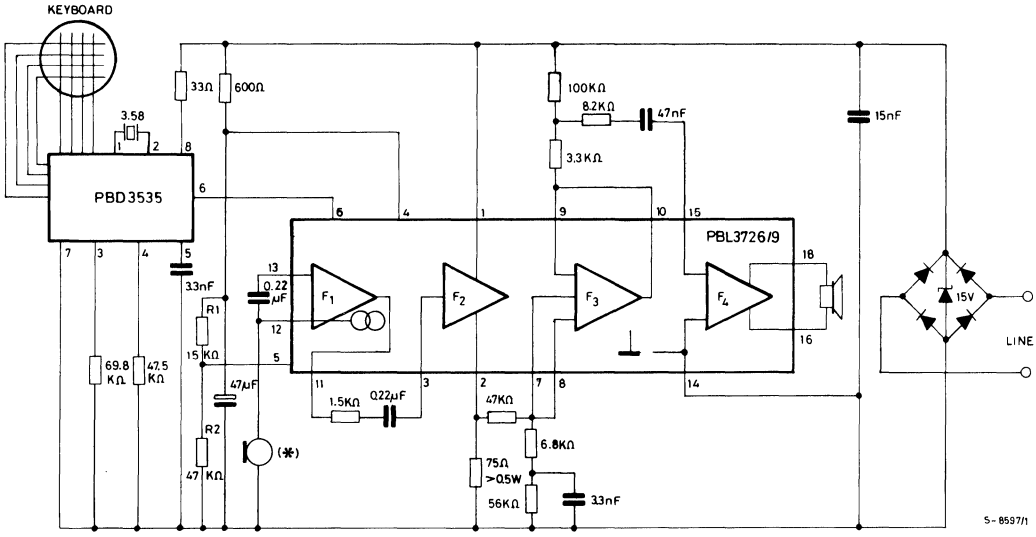
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Electrical characteristics over recommended operating conditions)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal voltage	I_{DC} = 15mA I_{DC} = 100mA	3.5 11	3.9 13	4.3 15	V V
G_T	Transmitting gain *	$20 \cdot \log_{10} (\frac{V_2}{V_3})$ 1KHz R_L = 0 E = E + 10% R_L = 400Ω R_L = 900Ω - 2.2KΩ	 24 26.5 28	 26 28.5 31	 28 30.5 33	 dB dB dB
REG_T	Transmitting range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_T	Transmitting frequency response	200Hz to 3.4KHz	-1		1	dB
G_R	Receive gain *	$20 \cdot \log_{10} (\frac{V_4}{V_1})$ 1KHz R_L = 0Ω E = E + 10% R_L = 400Ω R_L = 900Ω + 2.2KΩ	 -18.5 -16 -13.5	 -16.5 -14 -11.5	 -14.5 -12 -9.5	 dB dB dB
REG_R	Receiving range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_R	Receiving frequency response	200Hz to 3.4KHz	-1		1	dB
Z_{IN}	Transmitter input impedance	1KHz		19		KΩ
V_T	Transmitter dynamic output	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA		1.5		V_p
V_T	Transmitter max output	200Hz - 3.4KHz I_{DC} = 0 - 100mA V_3 = 0 - 1V		3		V_p
Z_{OUT}	Receiver output impedance	1KHz		3 + 310		Ω
V_R	Receiver dynamic output **	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA	0.5	0.55		V_p
V_R	Receiver max output	Measured with line rectifier 200Hz - 3.4KHz I_{DC} = 0 - 100mA V_1 = 0 - 50V		0.9		V_p
N_T	Transmitter output noise	P_{sof}-weighted, REL 1V R_L = 0		-75		dB_{psof}
N_R	Receiver output noise	A-weighted, REL 1V, with cable 0-5 km ϕ 0.5 mm; 0-3 km ϕ 0.4 mm		-85		dB_A
I_M	Mute input current		0.1			mA
I_{DC}	Extra available current when muted at the same DC-voltage	I_{DC} = 15 - 100mA		10		mA
I_S	Supply current for the microphone	R_L = 0 - 800Ω	310			μA

* Adjustable to both higher and lower values with external components
** The dynamic output can be doubled. See application notes at R14

Fig. 1 - Typical application with DTMF generator PBD 3535



(*) ELECTRETE MICROPHONE

Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table

Type	R1	R2
No regulation, all feeding systems	∞	0
48V, 2 x 250Ω	6.8KΩ	48KΩ
48V, 2 x 400Ω	0	∞

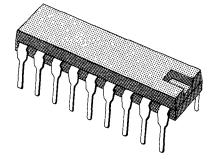
PBL3726/11

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 5 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- SIDETONE DISTORTION CANCELLATION

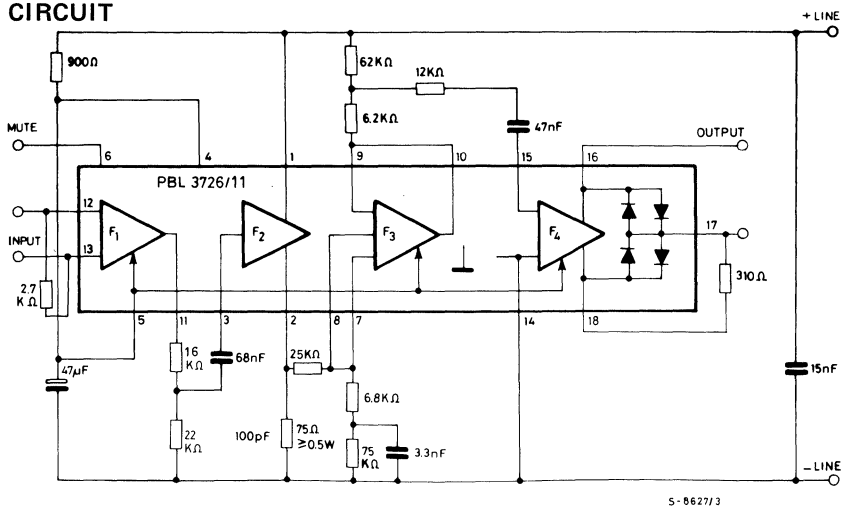
PBL 3726/11 is a standard version of the PBL 3726 family of the mask-programmable, monolithic integrated speech circuits for use in electronic telephones. It is designed for use with a low impedance microphone. Sending and receveing gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained with external resistor or totally cur off. Typical current feeds such as 48V 2 x 200Ω, 2 x 400Ω and 36V 2 x 250Ω can be handled.

Application-dependent parameters such as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market needs. An extra amplifier can be used for various purposes such as active sidetone balance.



DIP-18 Plastic
(0.4)

TEST CIRCUIT



Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table

Type	R1	R2
No regulation, all feeding systems	∞	0
48V, 2 x 200Ω	16KΩ	47KΩ
48V, 2 x 400Ω	9.1KΩ	47KΩ

ABSOLUTE MAXIMUM RATINGS

Maximum ratings over operating free-air temperature range (unless otherwise stated).

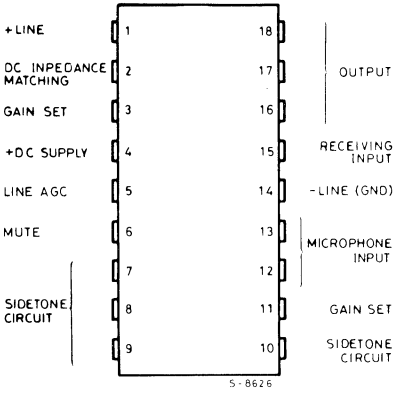
V_{DC}	Line voltage, $t_p = 2s$	22	V
I_{DC} (*)	Continuous operating line current	100	mA
T_j	Junction temperature	150	°C
T_{amb}	Operating ambient temperature	-40 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

(*) Max current increases linearly up to 130mA with max operating temperature lowered to +55°C

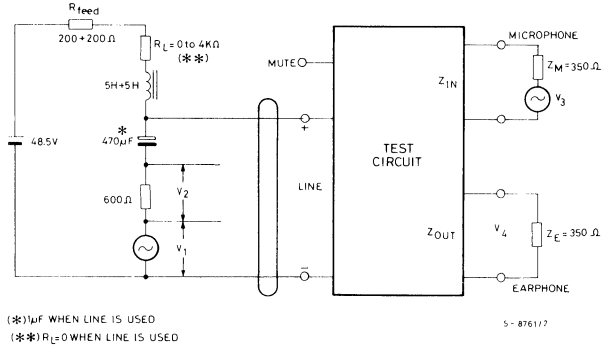
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	TYp.	Max.	Unit
I_L	Line current	15		100	mA

CONNECTION DIAGRAM



Test set-up



THERMAL DATA

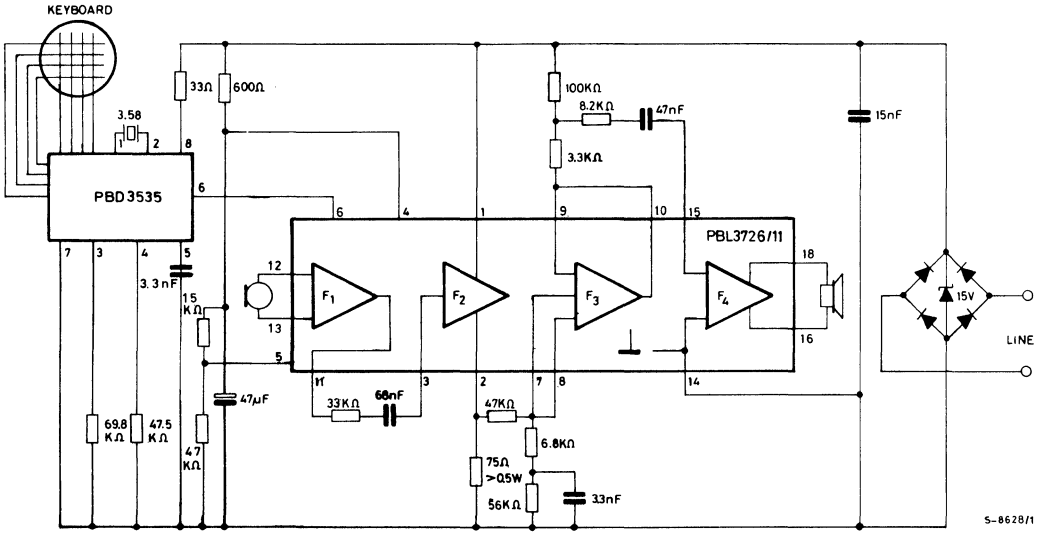
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Electrical characteristics over recommended operating conditions)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_D	Terminal voltage	I_{DC} = 15mA I_{DC} = 100mA	3.3 11	3.7 13	4.1 15	V V
G_T	Transmitting gain *	$20 \cdot \log_{10} (\frac{V_2}{V_3})$ 1KHz R_L = 0 E = E + 10% R_L = 400Ω R_L = 900Ω - 2.2KΩ	 41 43.5 46	 43 45.5 48	 45 47.5 50	 dB dB dB
REG_T	Transmitting range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_T	Transmitting frequency response	200Hz to 3.4KHz	-1		1	dB
G_R	Receive gain *	$20 \cdot \log_{10} (\frac{V_4}{V_1})$ 1KHz R_L = 0Ω E = E + 10% R_L = 400Ω R_L = 900Ω - 2.2KΩ	 -18.5 -16 -13.5	 -16.5 -14 -11.5	 -14.5 -12 -9.5	 dB dB dB
REG_R	Receiving range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_R	Receiving frequency response	200Hz to 3.4KHz	-1		1	dB
Z_{IN}	Transmitter input impedance	1KHz		1050		Ω
V_T	Transmitter dynamic output	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA		1.5		V_p
V_T	Transmitter max output	200Hz - 3.4KHz I_{DC} = 0 - 100mA V_3 = 0 - 1V		3		V_p
Z_{OUT}	Receiver output impedance	1KHz		3 + 310		Ω
	Receiver dynamic output **	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA V_1 = 0 - 50V		0.5		V_p
V_R	Receiver max output	Measured with line rectifier 200Hz - 3.4KHz I_{DC} = 0 - 100mA V_1 = 0 - 50V		0.9		V_p
N_T	Transmitter output noise	P_{sof}-weighted, REL 1V R_L = 0		-75		dB_{psof}
N_R	Receiver output noise	A-weighted, REL 1V, with cable 0-5 Km ϕ 0.5 mm; 0-3 Km ϕ 0.4 mm		-85		dB_A
I_M	Mute input current		0.1			mA
I_{DC}	Extra available current when muted at the same DC-voltage	I_{DC} = 15 - 100mA		10		mA

* Adjustable to both higher and lower values with external components
** The Dynamic output can be doubled. See application notes at R14

Fig. 1 - Typical application with DTMF generator PBD 3535



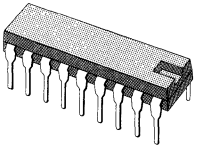
PBL3726/12

SPEECH CIRCUIT

- MINIMUM NUMBER OF INEXPENSIVE EXTERNAL COMPONENTS, 5 CAPACITORS AND 10 RESISTORS
- MUTE FUNCTION FOR PARALLEL OPERATION WITH DTMF GENERATOR OR DECADING IMPULSING
- LOW VOLTAGE OPERATION, DOWN TO 3.3V
- VERY SHORT START-UP TIME
- SEPARATE POWER SUPPLY POSSIBLE FOR OUTPUT AMPLIFIER

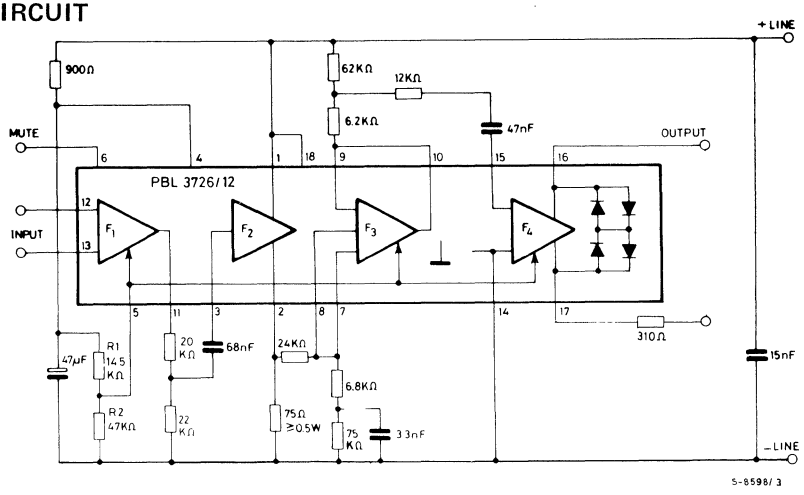
PBL 3726/12 is a standard version of the PBL 3726 family of the mask-programmable, monolithic integrated speech circuits for use in electronic telephones. It is designed for use with a low impedance microphone. Sending and receiving gain is regulated with line length. Different ranges of amplifier regulation for various current feeds can be obtained. Typical current feeds as 48V 2 x 250Ω 2 x 400Ω and 36V 2 x 250Ω can be handled.

Application-dependent parameters such as line balance, sidetone level and frequency response are set by external components. Parameters are set independently which means easy adaptation for various market neeeds. An extra 20dB amplifier can be used for various purposes such as extra receiving gain with volume control or active sidetone balance.



DIP-18 Plastic
(0.4)

TEST CIRCUIT



Some typical values for R1 and R2 for some different supplies from telephone stations are shown in the next table.

Type	R1	R2
No regulation, all feeding systems	∞	0
48V, 2 x 400Ω	14.5KΩ	47KΩ
48V, 2 x 200Ω	18KΩ	47KΩ

ABSOLUTE MAXIMUM RATINGS

Maximum ratings over operating free-air temperature range (unless otherwise stated)

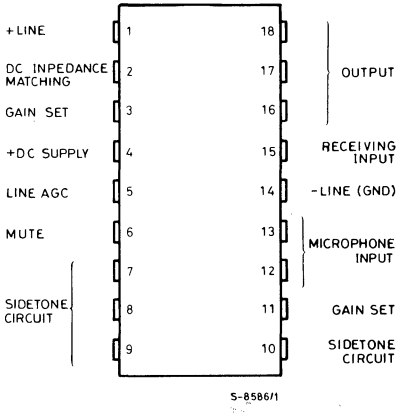
V_{DC}	Line voltage, $t_p = 2s$	22	V
I_{DC} (*)	Continuous operating line current	100	mA
T_j	Junction temperature	150	°C
T_{amb}	Operating ambient temperature	-40 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

(*) Max. current increases linearly up to 130mA with max operating temperature lowered to 55°C

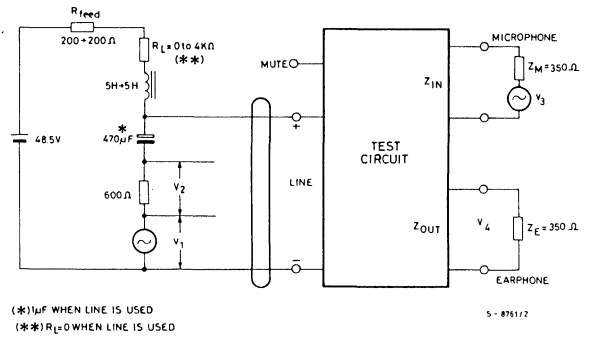
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_L	Line current	15		100	mA

CONNECTION DIAGRAM



Test set-up



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

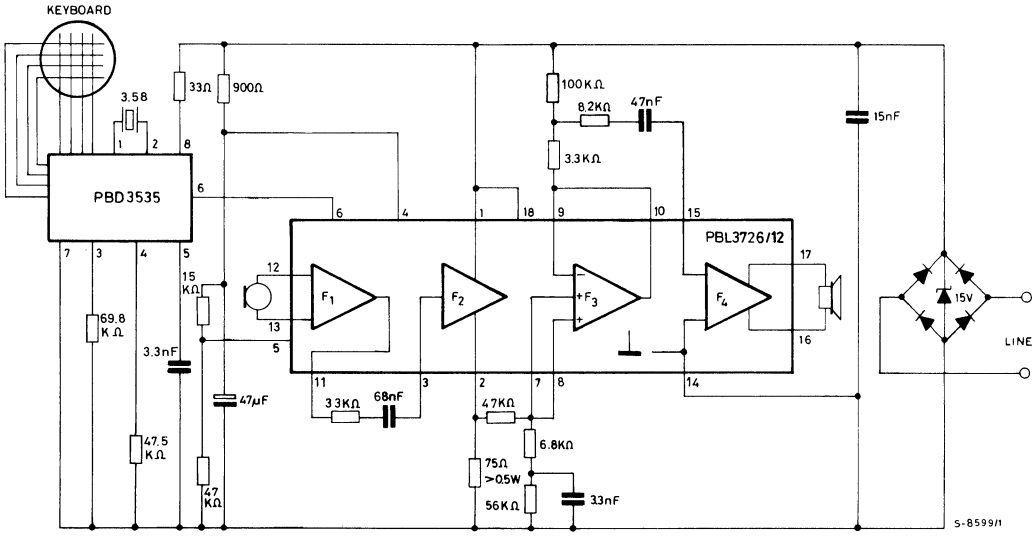
ELECTRICAL CHARACTERISTICS (Electrical characteristics over recommended operating conditions)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{DC}	Terminal voltage	I_{DC} = 15mA I_{DC} = 100mA	3.3 11	3.7 13	4.1 15	V V
G_T	Transmitting gain *	$20 \cdot \log_{10} (\frac{V_2}{V_3})$ 1KHz R_L = 0 E = E + 10% R_L = 900Ω - 2.2KΩ	 38 43	 40 45	 42 47	 dB dB
REG_T	Transmitting range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_T	Transmitting frequency response	200Hz to 3.4KHz	-1		1	dB
G_R	Receiving gain *	$20 \cdot \log_{10} (\frac{V_4}{V_1})$ R_L = 0Ω E = E + 10% R_L = 900Ω - 2.2KΩ	 -18.5 -13.5	 -16.5 -11.5	 -14.5 -9.5	 dB dB
REG_R	Receiving range of regulation	1KHz R_L = 0Ω E = E + 10% to R_L = 900Ω	3	5	7	dB
Lin_R	Receiving frequency response	200Hz to 3.4KHz	-1		1	dB
Z_{IN}	Transmitter input impedance	1KHz		2.5		KΩ
V_T	Transmitter dynamic output	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA		1.4		V_p
V_T	Transmitter max output	200Hz - 3.4KHz I_{DC} = 0 - 100mA V_3 = 0 - 1V		3		V_p
Z_{OUT}	Receiver output impedance	1KHz		3 + 310		Ω
V_R	Receiver dynamic output	200Hz - 3.4KHz ⩽ 2% distortion I_{DC} = 20 - 100mA		0.4		V_p
V_R	Receiver max output	Measured with line rectifier 200Hz - 3.4KHz I_{DC} = 0 - 100mA V_1 = 0 - 50V		0.9		V_p
N_T	Transmitter output noise	P_{sof}-weighted, REL 1V R_L = 0		-75		dB_{psof}
N_R	Receiver output noise	A-weighted, REL 1V, with cable 0-5 Km φ 0.5 mm; 0-3 Km φ 0.4 mm		-85		dB_A
I_M	Mute current		0.1			mA
I_{DC}	Extra available current when muted at the same DC-voltage	I_{DC} = 15-100mA		10		mA

* Adjustable to both higher and lower values with external components

*

Fig. 1 - Typical application with DTMF generator PBD 3535



SLIC

ADVANCE DATA

L3000, L3010, L3121

A KIT OF SOLID STATE DEVICES FOR INTEGRATING THE SUBSCRIBER LINE INTERFACE CIRCUIT

The SGS SLIC is a set of solid state devices designed to integrate all the functions, but testing, needed to interface the telephone line to a telephone exchange.

It consists of four integrated circuits, the L3000 line interface and the L3010 control unit, plus a couple of L3121, solid state transient suppressor.

All together these four devices perform the so-called BORSH, that is:

- BATTERY FEED
- OVERVOLTAGE PROTECTION
- RINGING
- SUPERVISION
- HYBRID

Additional functions, such as battery reversal, extra battery use, line overvoltage sensing and metering-pulse injection are also available from the SGS set of devices; most external characteristics, such as AC and DC impedances are programmable thanks to external components.

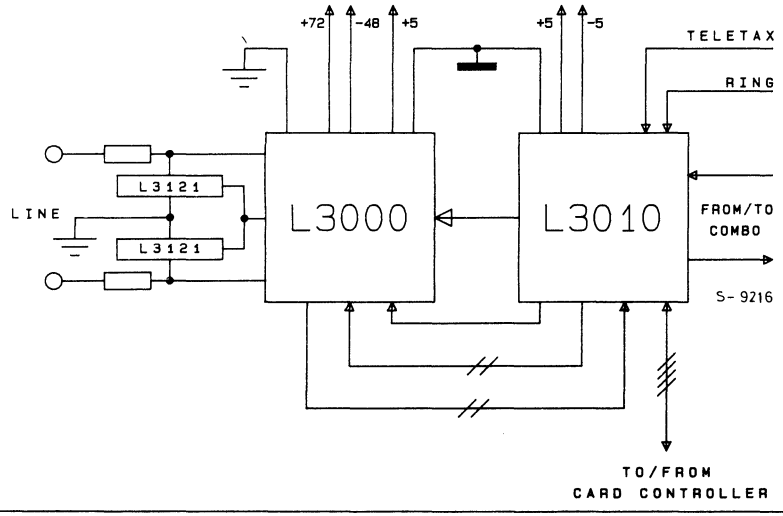
The SGS SLIC injects the ringing current in balanced mode and for that purpose, as well as for the operation in battery boosted condition, a positive supply voltage of +72V shall be available on the subscriber card.

As the right amplification to the ringing signal both in voltage and in current is provided by the SGS SLIC the ring generator shall only provide a low level signal (1 Volt peak).

Intended for use in both public and private networks, the kit is designed using the best technologies available to provide optimal combination of performance and reliability.

In Fig. 1 the block diagram of the SGS SLIC is shown.

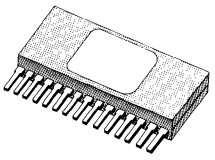
Fig. 1



LINE INTERFACE

The L3000 line interface integrates all those functions which require high voltage or high dissipation, such as Battery Feed and Ringing injection.

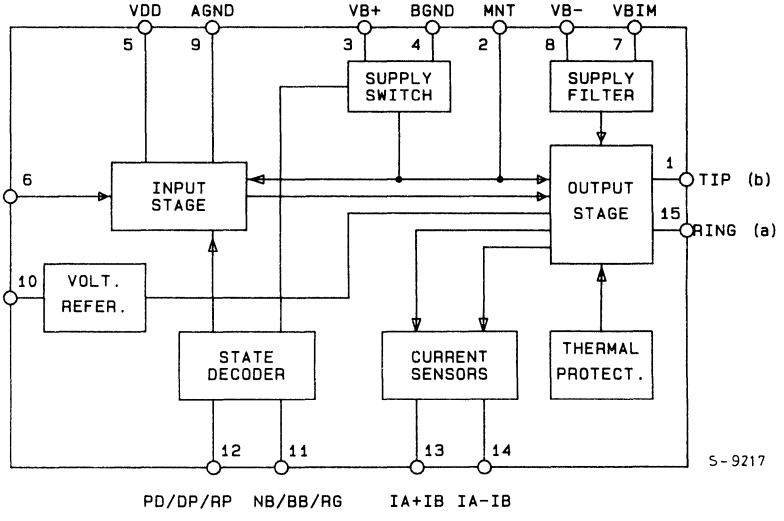
To allow extra feeding for long lines and the integration of the ringing function, this part is designed using a high voltage, junction - isolated bipolar technology ($V_{CEO} > 140V$, $V_{CBO} > 250V$) and housed in a premoulded SIL plastic power package (SILWATT®).



SILWATT®

ORDERING NUMBER: L3000

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$\lvert V_{B-} \rvert$	Voltage of negative battery	80	V
$\lvert V_{B+} \rvert$	Voltage of positive battery	80	V
$\lvert V_{B-} \rvert + \lvert V_{B+} \rvert$	Total battery voltage	140	V
V_{DD}	Supply voltage of analog signal processing	5.5	V
T_{op}	Operating temperature	0 to +70	°C
T_j	Max junction temperature	+140	°C
T_{stg}	Storage temperature	-55 to +150	°C

WARNING: When connecting power supplies to L3000, please be sure that -48 is applied first and +72 last; a reverse sequence shall be followed during disconnection. To prevent wrong operation a shotcky diode may be placed between the battery (-48) and its ground.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

PIN CONFIGURATION

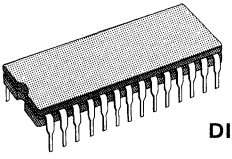
PIN	SYMBOL	FUNCTION
1	TIP	Wire b.
2	MNT	Positive supply voltage monitor.
3	V_{B+}	+72V (+60V).
4	BGND	Battery ground
5	V_{DD}	+5V
6	2 W	Two wire unbalanced terminal.
7	V_{BIM}	Battery image and supply voltage filter.
8	V_{B-}	-48V (-60V).
9	AGND	Analog ground.
10	REF	Bias set.
11	NB/BB/AG	State control signal 1.
12	PD/DP/AP	State control signal 2.
13	$I_A + I_B$	Differential line current
14	$I_A - I_B$	Common mode line current.
15	RING	Wire a.

CONTROL UNIT

Low voltage and control functions are integrated in the L3010 SLIC CONTROL UNIT.

Realized with a high speed 10V technology (MTL3V), which combines analog and digital elements, this chip includes the 2/4 wire interface, impedance matching, on/off hook detection and signalling functions; metering pulse injection (TELETAX) and ground key detection are also present in L3010.

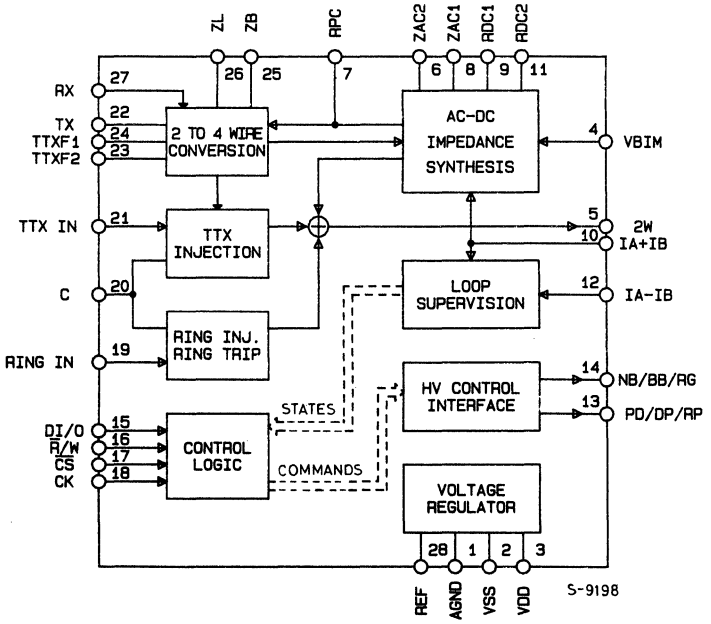
L3010 communicates with the card's control processor via a serial bus; it is encapsulated into a 28 pin ceramic DIL package.



DIP-28 Ceramic (0.25)

ORDERING NUMBER: L3010

BLOCK DIAGRAM



SLIC

SGS L3010

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Positive supply voltage	+5.5	V
V_{SS}	Negative supply voltage	-5.5	V
$\|V_{DD}\| + \|V_{SS}\|$	Total supply voltage	11	V
T_{op}	Operating temperature range	0 to +70	°C
T_j	Max junction temperature	+140	°C
T_{stg}	Storage temperature	-55 to +150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

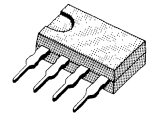
PIN CONFIGURATION

PIN	SYMBOL	FUNCTION
1	AGND	Analog ground.
2	V_{SS}	-5V
3	V_{DD}	+5V
4	V_{BIM}	Battery image input
5	2 W	Two wire unbalanced terminal.
6	Z_{AC2}	AC line synthesis
7	R_{SX}	Protection resistance compensation
8	Z_{AC1}	AC line impedance adjustement.
9	R_{DC1}	DC feeding system
10	$I_A + I_B$	Transversal line current.
11	R_{DC2}	DC feeding system
12	$I_A - I_B$	Longitudinal line current.
13	PD/DP/AP	State contro signal 2.
14	NB/BB/AG	State control signal 1.
15	D I/O	Data in/Data out.
16	$\overline{R}/W$	Read/write.
17	$\overline{CS}$	Chip select.
18	CK	Clock.
19	RING IN	Ring signal input.
20	C	Ring trip detection and TTX shaping.
21	TTX IN	Teletax signal input.
22	TX	Sending output (4W).
23	TTX F1	Teletax filter.
24	TTX F2	Teletax filter.
25	ZB	Balancing network.
26	ZL	Line impedance.
27	RX	Receiving input (4W).
28	REF	Bias set.

OVERVOLTAGE SUPPRESSOR

To protect L3000 and L3010 from overvoltages due to lightning and main induction, a series resistor is located at each line terminal and the special bilateral SCR structure L3121, gate controlled, is connected between each wire and ground. Thanks to gates, the L3121 can easily adapt its breakdown voltage to the actual supply voltage of the L3000.

L3121 is packaged in a S.I.P. 4 plastic minidip.



SIP-4

ORDERING NUMBER: L3121

ABSOLUTE MAXIMUM RATINGS

I_{TS}	Transient current (T1/T2 = 1/50μs pulse	200	AP
	(T1/T2 = 1/1000μs pulse)	150	AP
I_P	Non repetitive peak current (one sine wave 50Hz, 30s interval)	50	A
I_P	Repetitive peak current (50Hz, 1s)	20	A
P_{tot}	Total power dissipationa at $T_{amb} = 50°C$ (steady state)	1.2	W
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

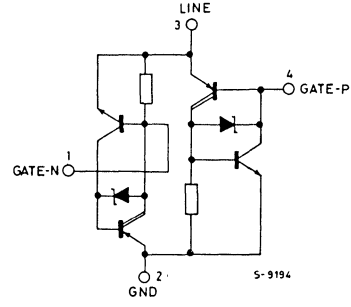
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction temperature	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins 2 and 3	max	20	°C/W

PIN CONFIGURATION

PIN	FUNCTION
1	Gate N
2	Ground
3	Line
4	Gate P

SCHEMATIC DIAGRAM



OPERATION DESCRIPTION

DEFINING PARAMETERS AND CHOOSING EXTERNAL COMPONENT VALUES

To set SGS SLIC in operation, the following parameters have to be defined:

- The DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common values for RFS are 200, 400 or 500Ω).
- The AC impedance at line terminals, ZML. This is the impedance to which the return loss measurement reference. It can be either a pure resistance (typically 600Ω) or a complex impedance.
- The equivalent AC impedance of the line ZB, when evaluating the echo attenuation (2/4 wire conversion). It is usually a complex impedance.
- The frequency of the ringing signal Fr (SGS SLIC can work with this frequency ranging from 16 to 66Hz).
- The metering pulse frequency Ft (two values are possible: 12KHz and 16KHz).
- The value of the two resistors R_P in series with the line terminals; main purpose of the a.m. resistors is to allow primary protection to fire. SGS suggest 30Ω min. for each side.

On these assumptions, the following component lists are defined.

EXTERNAL COMPONENT LIST L3000

COMPONENT		INVOLVED PARAMETER OR FUNCTION
REF	VALUE	
R_{REF}	24.9KΩ	Bias resistance
C_{DVB}	47μF-10VL	Battery voltage rejection
C_{VB+}	0.33μF-100VL	Positive battery filter
C_{VB-}	0.33μF-100VL	Negative battery filter

EXTERNAL COMPONENT LIST L3010

COMPONENT		INVOLVED PAREMETER OR FUNCTION
REF	VALUE (or calculation formula)	
C_{VSS}	0.33μF 15V_L	Negative supply voltage filter.
C_{VDD}	0.33μF 15V_L	Positive supply voltage filter.

EXTERNAL COMPONENT LIST L3010 (continued)

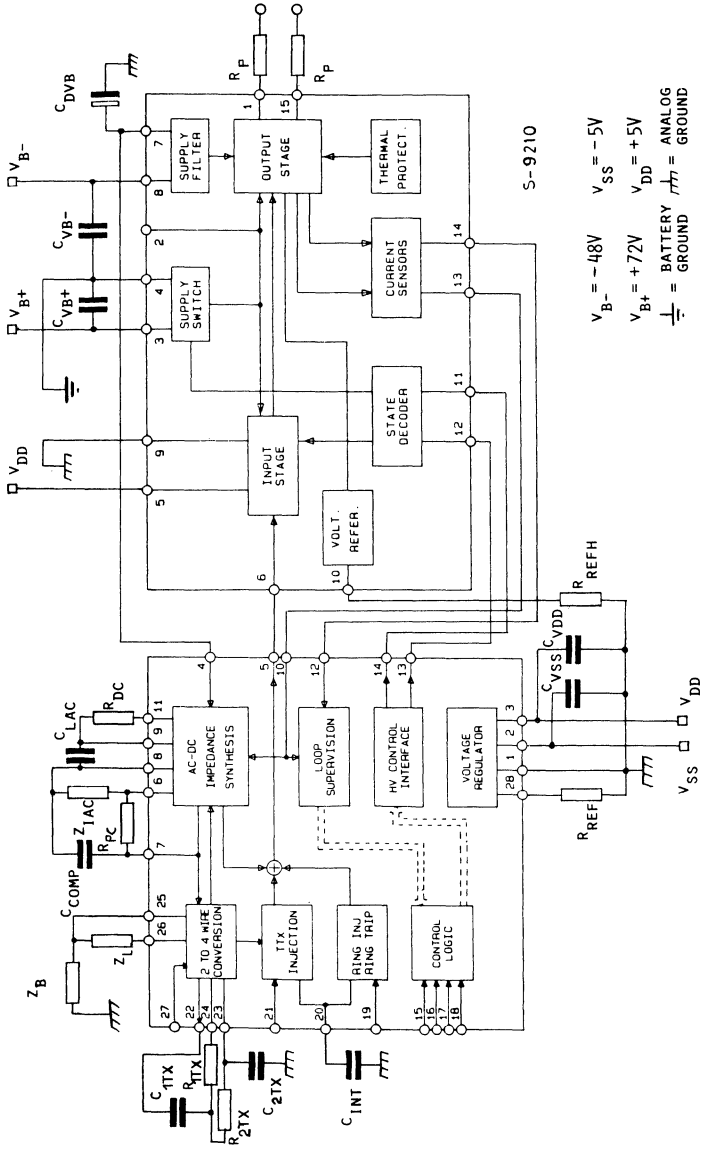
COMPONENT		INVOLVED PARAMETER OR FUNCTION
REF	VALUE (or calculation formula)	
R_{DC}	$\frac{5\ (R_{FS} - R_P)}{4}$	DC Feeding system and AC impedance adjustement
C_{LAC}	$1/(2\pi\ R_{DC} \cdot 30)$	
Z_{IAC}	$\frac{5\ (Z_{ML} - 2R_P)}{4}$	
R_{PC}	$\frac{5\ R_P}{2}$	
C_{COMP}	$1/[2\pi\ (Z_{IAC} + R_{PC})\ .25 \cdot 10^3]$	
R_{REF}	25.5 KΩ	Bias set
Z_B	See note (1)	Line impedance balancing network
Z_L	$K\ \frac{4\ (R_{PC} + Z_{IAC}}{5}\ //\ \frac{1}{K}\ \frac{5\ C_{COMP}}{4}$	Slic impedance balancing network See note (2)
C_{1TX} C_{2TX} R_{1TX} R_{2TX}	15nF 15nF 1.3KΩ 2.21KΩ	Teletaxe filter (12KHz) See note (3)
C_{INT}	See note (4)	Ring trip detection

NOTE (1) : The structure of this network shall copy the line impedance, in case multiplied by a factor K (K= 1. . .10).
(2) : K as fixed at note (1).
(3) : If the teletaxe filter is not used, pin 23 should be shorted with pin 24.

(4)

Ring freq. (Hz)	16/18	18/21	21/26	26/31	31/38	38/46	46/57	57/66
C (nF)	450	390	330	270	220	180	150	120

Fig. 1 - Schematic diagram



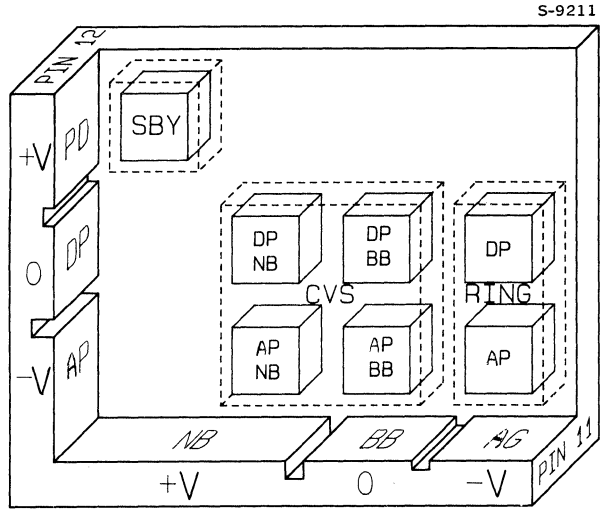
INTERFACING WITH CARD CONTROLLER

In the order to carry out all the functions, inherent to the BORSH operation the SGS SLIC kit has several different working states, each state is defined by the voltage applied by pins 13 and 14 of L3010 respectively to pins 12 and 11 of L3000; three different voltage levels (-3, 0, +3) are available at each connection, so defining six possible states as listed in Tab. 1.

TABLE 1

L3010	V	STATE		V	L3000
Pin 13	+3	Power down	(PD)	+3	Pin 12
	0	Direct polarity	(DP)	0	
	-3	Reverse poalrity	(AP)	-3	
Pin 14	+3	Normal battery	(NB)	+3	Pin 11
	0	Boost battery	(BB)	0	
	-3	Ringing	(AG)	-3	

Fig. 2



Appropriate combinations of two states define the three modes of the SGS SLIC, that are:

A) Stand-by (SBY)
B) Conversation (CVS)
C) Ringing (RING)

The combinations offered by the system are such that in stand-by just one condition is allowed (Normal Battery with Direct Polarity) but four are possible in conversation (Normal Battery or Boost Battery, Direct Polarity or Reverse Polarity) and two in Ringing. (Direct Polarity or Reverse Polarity).

The following picture shows the complete map of SLIC's modes and states.

Inside the conversation mode, two more functions are also available, that do not affect the particular operation where the SLIC is set.

The functions are:

1) Current limiting (with 4 possible levels)
2) Metering pulse injection

Due to the structure of the data transmission from L3010 to 3000, the transition from one state to another is possible only if the two states are somehow contiguous in the map of Fig. 2.

Transitions from not contiguous states always take place passing through the intermediate condition; of course the permanence in such a condition will last just the time needed by the voltage at pin 13 (or 14) to move from +3V to -3V (or viceversa).

Control Interface

The L3000/L3010 states, modes and functions are controlled by the card processor by loading commands serially through a four-wire bus; through the same bus (designed according to the well know SLD architecture) the card processor also reads status information.

The four wires of the bus have the following functions:

1) CLOCK (CK)	Pin 18 of L3010
2) CHIP SELECT ($\overline{CS}$)	Pin 17 of L3010
3) $\overline{READ}$/WRITE ($\overline{RW}$)	Pin 16 of L3010
4) DATA IN / DATA OUT (I/O)	Pin 15 of L3010

The clock frequency is 512KHz max.

The $\overline{CS}$ signal always goes low when I/O data have to flow between the SLIC and its card controller. When $\overline{R}$/W signal is high, data are transferred from the controller into the L3010's I/O register, then copied into a latch for execution; in this phase, a complete 8 bit word shall be loaded into L3010 for system operation, and therefore $\overline{CS}$ shall remain low as long as 8 clock pulses.

$\overline{R}$/W high state shall always last as long as $\overline{CS}$ low state, but it may also start before and end after.

Data are originated by the controller during the trailing edge and loaded into the SLIC during the leading edge of the clock signal.

To determine the line conditions, the card controller periodically reads the contents of the L3010's register and this when both $\overline{CS}$ and $\overline{R}$/W are low.

Output data become available from the SLIC during the loading edge and are received by the controller during the trailing edge of the clock signal.

Only four bits out of the eight available in the I/O register are significative in this phase, therefore $\overline{CS}$ low state may last just four clock pulses; it is also possible for the controller to read only one (or two, or three) bit, and in this case $\overline{CS}$ will remains low just during the bits in which the controller is interested.

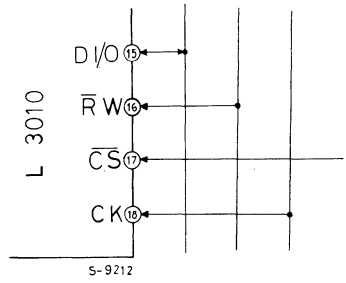
After data have been written into SLIC (or read from the SLIC) two clock pulses are needed before the next phase can start.

The structure of the data bus is shown in Fig. 3 where also the meaning of each bit is displaied. Fig. 4 shows the complete chronogram of a Read/Write operation.

As mentioned before, the L3000/L3010 states and modes are defined by the card controller, and the SLIC moves from one state to another one under external control, as shown in the Table 1; there is just an exception, and is that ringing is suspended autonomously by the SLIC if the loop is closed during a ringing burst.

In this case, without any intervention of the card controller, the SLIC returns to the conversation mode, (normal battery state) by means of the internal logic, and sets the control commands to the new situation.

Fig. 3



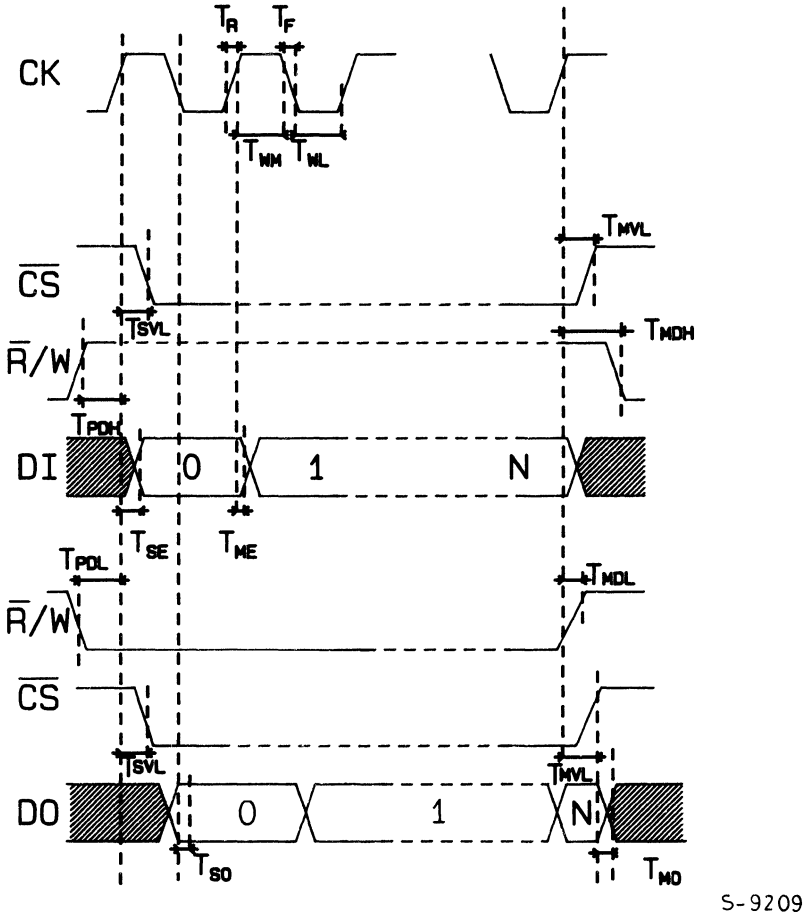
DATA IN

Bit 0 : ACT = ACTIVATION	0 : Stand-by 1 : Operation
Bit 1 : BR = BATTERY POLARITY	0 : Direct polarity (tip to ground) 1 : Reverse polarity (ring to ground)
Bit 2 : RING = RINGING BURST	0 : Ring off 1 : Ring on
Bit 3 : TAX = TELETAX	0 : Teletaxe off 1 : Teletax on
Bit 4 : EXF = EXTRA FEEDING	0 : Normal battery 1 : Boost battery
Bit 5 : LIM0 Bit 6 : LIM1 = CURRENT LIMITING AT: 30mA	]0]0]1]1] 45mA] 60mA] 70mA]]0]1]0]1
Bit 7 : PAR = DISPARITY CONTROL	0 : Σ bit 0-6 = 0DD 1 : Σ bit 0-6 = EVEN

DATA OUT

Bit 0 : LS = LOOP STATE	0 : on hook 1 : off hook
Bit 1 : OVL = OVERLOAD	0 : Differential line current $<$ 65mA 1 : Differential line current $>$ 65mA
Bit 2 : KEY = GROUND KEY	0 : Common mode line current $< I_L/2.5$ 1 : Common mode line current $> I_L/2.5$
Bit 3 : PW = PREVIOUS WORD ACCEPTED	0 : Not accepted 1 : Accepted

Fig. 4 - Chronogram



ELECTRICAL CHARACTERISTICS

Paremeters			Min.	Max.	Unit
CK, $\overline{CS}$, $\overline{R}$/W INPUTS					
H_L	V_H		2	5	V
	I_H			40	μA
L_L	V_L		0	0.8	V
	I_L			200	μA
DATA INPUT					
a) $\overline{R}/W = 1$	$\overline{CS} = 0$ see	CK, $\overline{CS}$, $\overline{R}$/W			
b) $\overline{R}/W = 1$	$\overline{CS} = 1$	I_H		10	μA
		I_L		10	μA
DATA OUTPUT					
c) $\overline{R}/W = 0$	$\overline{CS} = 1$ as b)				
d) $\overline{R}/W = 0$	$\overline{CS} = 0$	V_H	2.4		V
		V_L		0.4	V
CK FREQUENCY			1	512	KHz
TIMING					
T_R, T_F				50	ns
T_{WH}, T_{WL}			800		ns
T_{PDH}, T_{PDL}			1		CKpulse
T_{MDL}			0	100	ns
T_{MDH}			200	600	ns
T_{SVL}, T_{MVL}			0	400	ns
T_{SE}			150	600	ns
T_{ME}			0	200	ns
T_{SO}				300	ns
T_{MO}			100	800	ns

OPERATION MODES OF THE SLIC

Stand-by (SBY)

In this mode, the bias currents of both L3000 and L3010 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them.

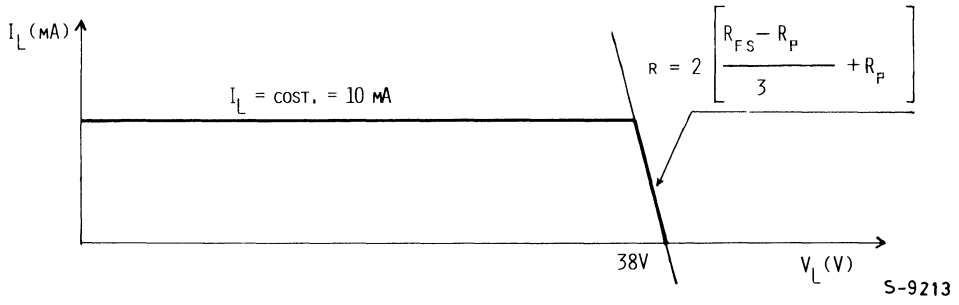
The current supplied to at the line is limited at 10mA, and the DC characteristic depends on the resistance of the feedings system ($2 \times R_{FS}$) as well as on the value of the two external resistors R_{EXT} according to the following formula:

$$\frac{2 \times R_{FS} - 2 \times R_P}{3} + 2 R_P =$$

$$= 2 \left[\frac{R_{FS} - R_P}{3} + R_P \right]$$

The voltage with infinite load is just the battery minus the voltage drop (approx 10V) of the output stage amplifiers (see Fig. 5).

Fig. 5



The AC characteristic is just the resistance the two serial resistors R_P (that is 60Ω).

In stand-by mode the polarity of the battery is just in direct condition, that is the tip wire more positive than the ring one; boost battery is not achievable. There are three possible line conditions where the SLIC is expected to be in stand-by mode.

1) On hook ($I_L < 6mA$) - normal on hook condition
2) Line calling ($I_L > 7.5mA$) - handset unhooked, SLIC waiting for command to activate conversation
3) Malfunction ($6 < I_L < 10mA$) - after the handset has been lifted, but no number dialled, the SLIC should be forced into the stand-by state in order not to waste power; the handset must be replaced, returning to the on-hook condition before another call can be initialized.

When the SGS SLIC is in stand-by mode, the power dissipation of L3000 does not exceed 200mW (from 48V) eventually increased of a certain amount if some current is flowing into the line (for instance during a malfunction condition). Depending on the total loop resistance, this quantity will range from 150mW (total loop resistance = 3.5KΩ) to about 800mW (loop resistance = 140Ω) the total loop resistance includes telephone set and R_P.
The power dissipation of L3010, in the same condition, is limited to 50mW.

Conversation (CVS)

This operation mode is set by the control processor when the off-hook condition has been recognised.

This mode can be set with either standard battery condition (-48V) or in Boost Battery; in this case the L3000 operates between -48 and +72mV.

In any case it is possible to select by the control processor the maximum line current (Bit 5 and Bit 6) and the polarity of the line system ("Direct" or "Reverse" - Bit 1).

Battery reverse can take place either before or during conversation.

As far as the DC characteristic is concerned, three different feeding conditions are preset:

a) Current limiting region: the DC impedance of the SLIC is very high (> 50KΩ) and therefore the system works like a current generator, the current value being set by the contro processor through the interface (4 options are available).

b) Standard feeding system region: the characteristic is equal to a 46V battery (named Apparent Battery, fixed internally by the control unit and indipendent of the actual battery value) in series with two resistors, whose value is set by external components (see external component list of L3010).

c) Low impedance region: the battery value is reduced to 38V, and the serial resistance is reduced to the some value specified in stand-by mode, that is:

$$2\left[\frac{R_{FS} - R_P}{3} + R_P\right]$$

Switching between the three regions is automatic without discontinuity, and depends on the loop resistance.

When the boost battery condition is activated (Bit 4) the low impedance region can never be reached by the system; the Apparent Battery is internally fixed at 95V.

In conversation mode, whatever the condition (normal or boost battery, direct or reverse polarity), it is always possible to inject metering pulses, when request by the control processor (Bit 3).

A patented automatic control system adjusts the level of the metering signal to contain 2 V_{RMS} across the line, regardless of impedance.

Moreover the metering signal is ramped at the beginning and end of each pulse to prevent undesirable clicking noises.

Fig. 6 - DC characteristics (N.B.)

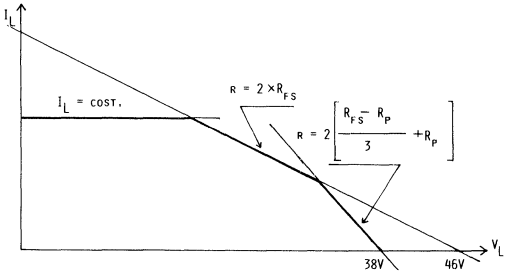
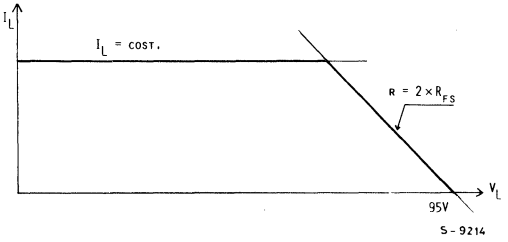


Fig. 7 - DC characteristics (B.B.)



In conversation mode the AC impedance at line terminals, Z_{ML}, is syntetized by the external components Z_{IAC} and R_P, according to the following formula:

$$Z_{ML} = \frac{4}{5} Z_{IAC} + 2 R_P$$

The capacitor C_{COMP} guarantees stability to the system.

Depending on the characteristic of the Z_{IAC} network, Z_{ML} can be either a pure resistance or a complex impedance, so allowing SGS SLIC to meet different standards as far as the return loss is concerned.

The two-to-four wire conversion is achieved by means of a Wheatstone bridge configuration, the sides of which being:

1) The line impedance (Z_{line})
2) The SLIC impedance at line terminals (Z_{ML})
3) The network Z_L connected between pin 25 and pin 26 of 3010, that shall be an image of Z_{ML} (see external component list)
4) The network Z_B between pin 25 and ground; Z_B shall copy the line impedance.

For a perfect balancing, the following equation shall be verified:

$$\frac{Z_L}{Z_B} = \frac{Z_{ML}}{Z_{line}}$$

It is important to underline that Z_L and Z_B are not necessarly equal to Z_{ML} and to Z_{line}, but they both may be multiplied by a certain factor (up to ten) so allowing use of smaller capacitors.

In conversation, the L3000 dissipates about 500mW for its own operation; to that value the dissipation depending on the current supplied to the line shall be added.

Fig. 8A

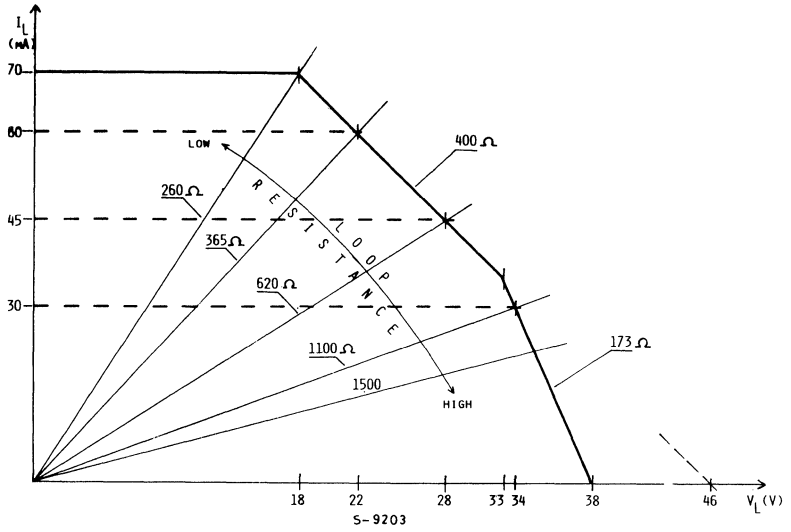
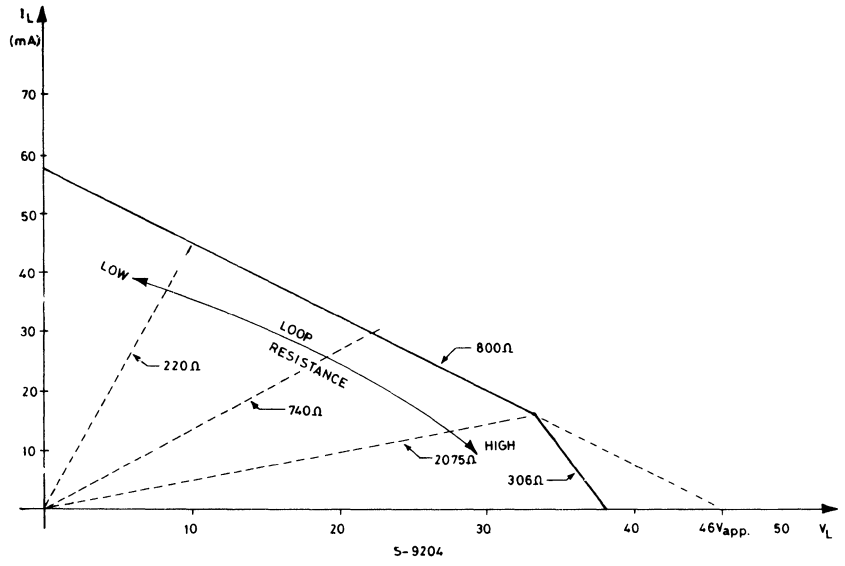

I_L (mA)
70
60
45
30
LOW
400 Ω
260 Ω
365 Ω
620 Ω
1100 Ω
1500
173 Ω
HIGH
LOOP RESISTANCE
18
22
28
33 34
38
46
V_L (V)
S-9203

Fig. 8B


I_L (mA)
70
60
50
40
30
20
10
LOW
LOOP RESISTANCE
220 Ω
740 Ω
2075 Ω
HIGH
800 Ω
306 Ω
10
20
30
40
46 $V_{app.}$
50
V_L
S-9204

To calculate the total power dissipation in a pre-fixed line condition, first of all it is necessary to determine the amount of the current supplied by the SLIC to the line, that amount depending on the max current limit set by the card controller (see Fig. 8A, where a feeding system 2x200 is supposed and Fig. 8B for 2x400). The power dissipated in the L3000 line interface can be evaluated with reference to Fig. 9A and Fig. 9B.

The figure puts in evidence the effect of the current limiting function to reduce the power dissipation.

The equivalent trend of power vs. current is showed in Fig. 10 in case the battery boosted condition is selected.

Fig. 9A

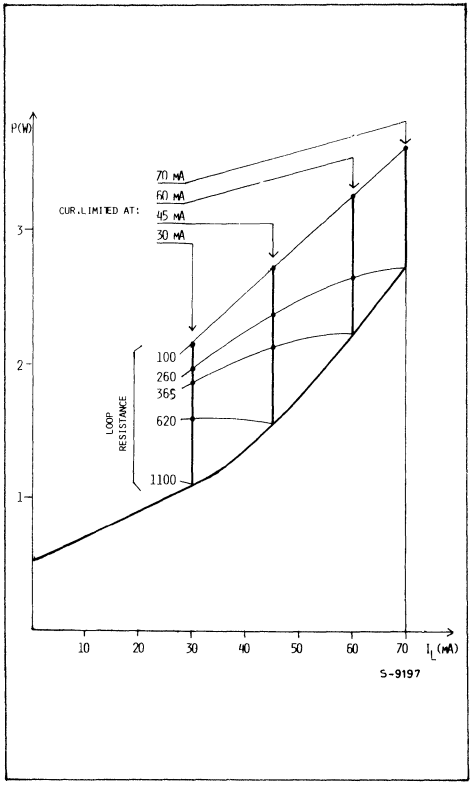


Fig. 9B

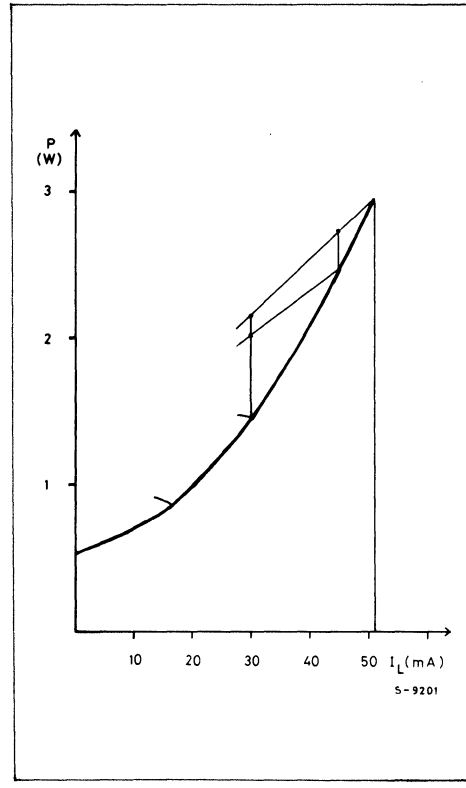
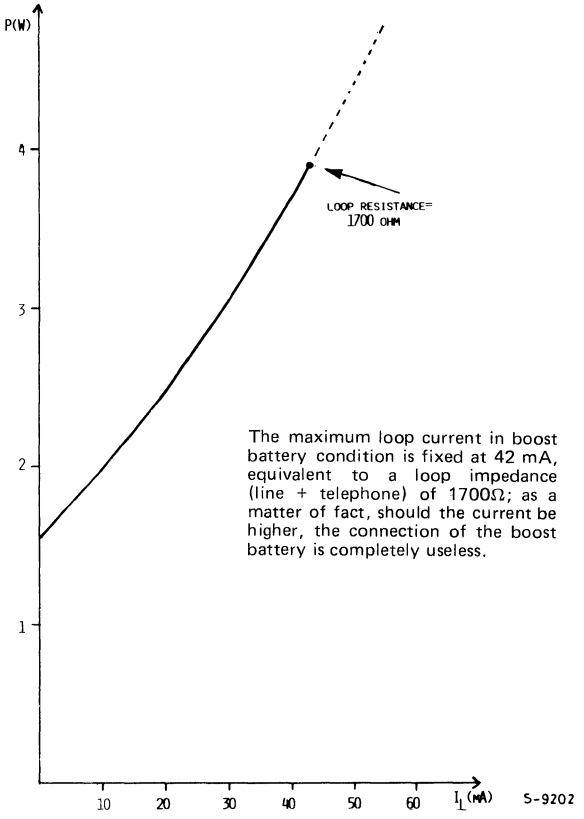


Fig. 10



Ringing

When the ringing function is selected by the control processor, (Bit 2) a low level (1 V_{RMS}) 16-66Hz, permanently applied to one pin of the L3010, is connected to the sending chaine and injected in balanced mode into the line through the L3000 with a superimposed DC voltage of 22V. The first and the last ringing cycles are synchronized by the L3010 so that ringing always starts and stops when the signal crosses zero.

When this mode is activated, the L3000 operates between -48V and the positive +72V battery; the impedance to the line is just the two external resistors and the polarity of the 22V DC component can be either direct or reverse.

Reversal can take place also in presence of the ringing signal.

Ring trip detection is performed autonomously by the SLIC, without waiting for a command from the control processor, using a patented system which allows detection during a ringing burst; when the handset is lifted, the SLIC suspends the ringing signal, returns to the normal battery condition and in this condition checks

that the loop is closed. If the loop closure is confirmed, a flag (BIT in output) is set and the SLIC waits for the control processor to deselect the ringing mode and activate conversation.

In ringing phase, the power dissipation of the H.V. device is about 2.5W (during ring burst), to which the power depending on the ring current shall be added. That contribution is particularly important as the load during ring is generally capacitive; it means that when a high current is flowing from the SLIC, most of the voltage drop is located across the SLIC itself rather than across the load.

As a worst case 3 paralled ringers connected to a null line have been considered, the total load being 1200Ω with a phase of 60°C; time-on is 1 sec and time-off is 4 sec.

Assuming to set SLIC in conversation mode during "time off", and due to the time constant related to the package, in the above mentioned case the average power dissipation about 1.7W.

Of course, in most cases, when one or two ringers are connected, the power dissipation is considerably lower.

On that value the thermal characteristics of the heat sink shall be calculated, assuming an ambient temperature of 70°C.

The power dissipated during the ringing phase can be easily calculated for each condition, when the characteristics of the load are well known.

The load is assumed to include the two resistors R_P, and this in order to put the power dissipation in L3000 in a better, in any case the load will be identified by its impedance module $|Z_{load}|$ and its phase φ

The power delivered to the load by L3000 is:

$$P_{load} = V_{ring} \cdot I_{ring} \cdot \cos\varphi$$

V_{ring} is fixed at 60 V_{RMS}, therefore

$$P_{load} = 60 \cdot \frac{60}{Z_{load}} \cdot \cos\varphi$$

The power drained by L3000 from batteries is

$$P_A = 120 \cdot \frac{60}{Z_{load}} \sqrt{2}\,\frac{2}{\pi}$$

where 120 is the total supply voltage applied to L3000 and $\frac{60}{Z_{load}} \sqrt{2}\,\frac{2}{\pi}$ is the RMS value of the fully rectified ringing current.

The power dissipated inside L3000, P_D, is clearly the difference between the power drained from the batteries and the power delivered to the load.

$$P_A = P_A - P_L$$

The amount of power due to the bias current (2.5W) and to other current proportional to ringing current should be added to this value so obtaining:

$$P_{DTOT} = P_A - P_B + 2.5 + \left(120 \cdot \frac{60}{Z_{load}} \sqrt{2}\,\frac{2}{\pi}\right) \frac{1}{17.6}$$

Of course this power dissipation refers just to the ringing burst, and to know the average value, you have to consider the ring-on and ring-off times by applying:

$$P_{DAV} = \frac{P_{DTOT} \cdot t_{on} + P_{CVS} \cdot t_{off}}{5}$$

P_{CVS} is the power dissipated in L3000 in conversation; t_{on} and t_{off} can change according to different PTT specifications, but $(t_{on} + t_{off})$ is always equal to 5s.

Fig. 11 - Power cycle in ring phase - German/Italian timing

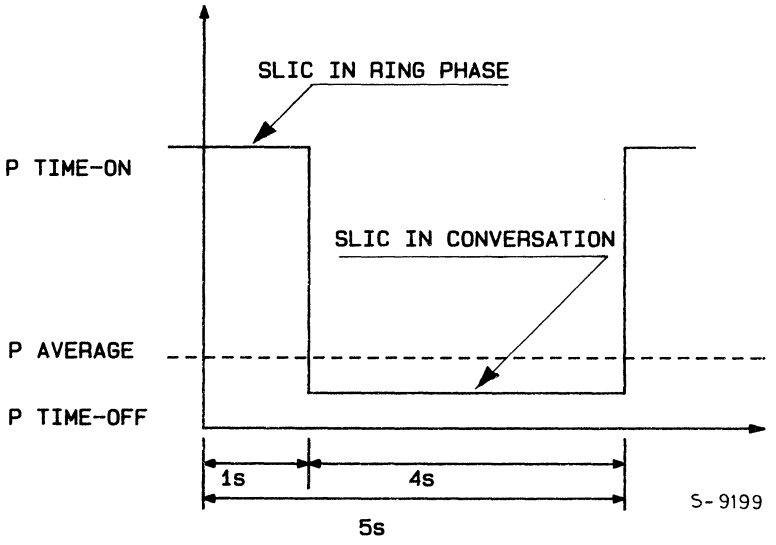
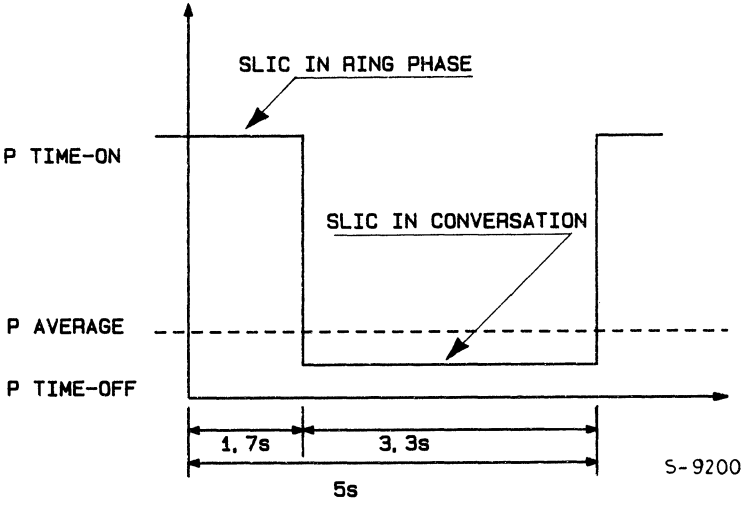


Fig. 12 - Power cycle in ring phase - French timing



APPLICATION INFORMATION

Example

In the following pages a pratical example is considered, and the complete behaviour of the circuit is evaluated.

1) Definition of design parameters

- DC feeding system: 2x200Ω
- AC impedance at line terminals: 600Ω
- Equivalent AC impedance of the line: 600Ω
- Ringing signal frequency: 25Hz
- Teletaxe signal frequency: 12KHz
- Series Resistors R_P : 30Ω

2) Calculation of external components

$$R_{DC} = \frac{5\ (R_{FS} - R_P)}{4} = \frac{5\ (200 - 30)}{4} = 212.5\Omega$$

$$C_{LAC} = \frac{1}{2\pi\ R_{DC} \cdot 30} = \frac{1}{2\pi\ 212.5 \cdot 30} = 25\mu F$$

$$Z_{IAC} = \frac{5\ (Z_{ML} - 2\ R_P)}{4} = \frac{5\ (600 - 60)}{4} = 675\Omega$$

$$R_{PC} = \frac{5}{2}\ R_P = 75\Omega$$

$$C_{COMP} = \frac{1}{2\pi\ (Z_{IAC} + R_{PC}) \cdot 25 \cdot 10^3} = \frac{1}{2\pi\ (675 + 75) \cdot 25 \cdot 10^3} = 9nF$$

$$Z_B = 600\Omega \times 10 = 6K\Omega\ (*)$$

$$Z_L = \frac{4\ (R_{PC} + Z_{IAC}) \cdot 10}{5} \;//\; \frac{5\ C_{COMP}}{4} = \frac{4 \cdot 7050}{5} \;//\; \frac{5 \times 9}{4 \times 10} = 5640\Omega\ //\ 1.1nF\ (*)$$

(*) K = 10

COMPONENT LIST (See fig. 1)

R1 = 30.1 Ω	R8 = 681 Ω	C1 = 0.33μF	C8 = 8.5nF
R2 = 30.1 Ω	R9 = 210 Ω	C2 = 0.33μF	C9 = 47 μF/15V$_L$
R3 = 24.9 KΩ	R10 = 1.33KΩ	C3 = 47 μF/15V$_L$	C9[1] = 47 μF/15V$_L$
R4 = 25.5 KΩ	R11 = 215 KΩ	C4 = 0.33μF	C10 = 100 nF
R5 = 6 KΩ	RRX = 600 Ω	C5 = 0.33μF	C11 = 15 nF
R6 = 5.62KΩ	RTTX = 600 Ω	C6 = 330 nF	C12 = 15 nF
R7 = 75 Ω	RRING = 600 Ω	C7 = 1 nF	D1 = TYPE BAT 49 (Thomson)

All resistors belong to E48 series, 2%, 0.25W, exception made for R1 and R2 that should be at 1%, 0.5W. R3 and R4 - that should be 1%, 0.25W.
All capacitors belong to E12 series exception made for C6, that should have a tolerance of ± 5%.

Fig. 1

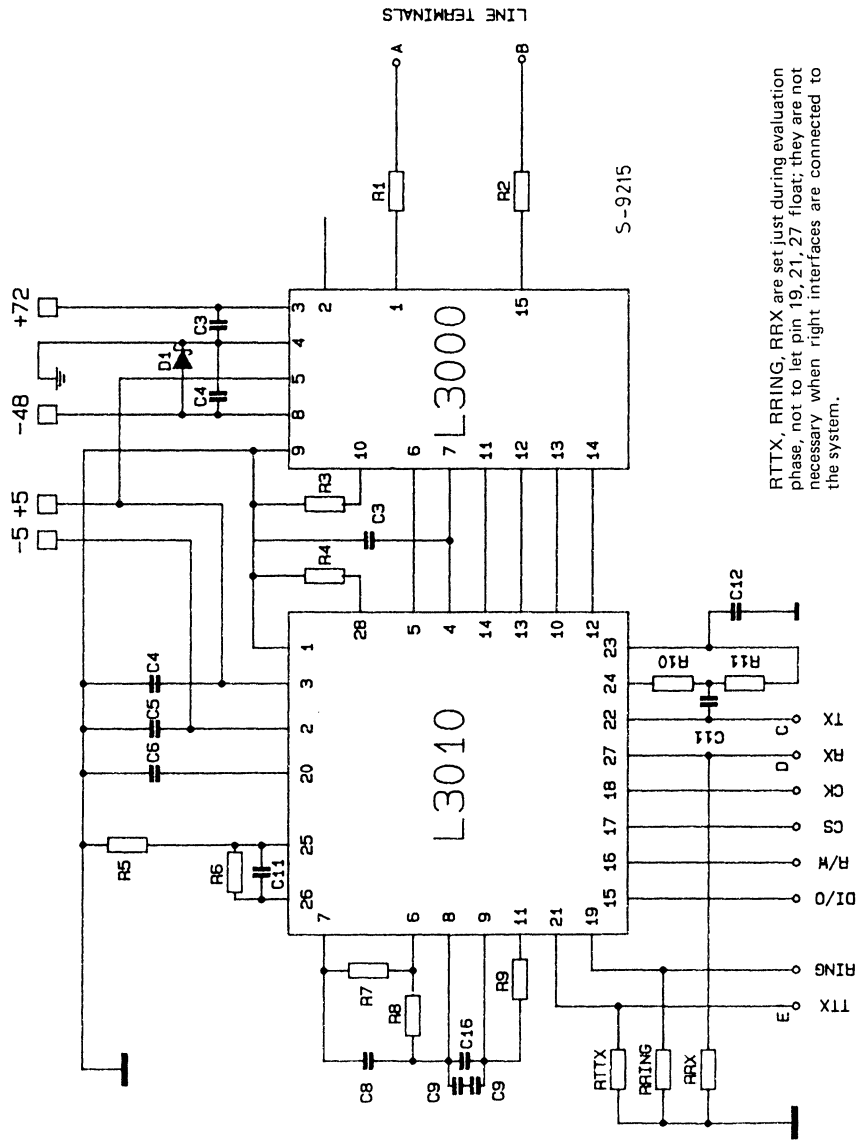
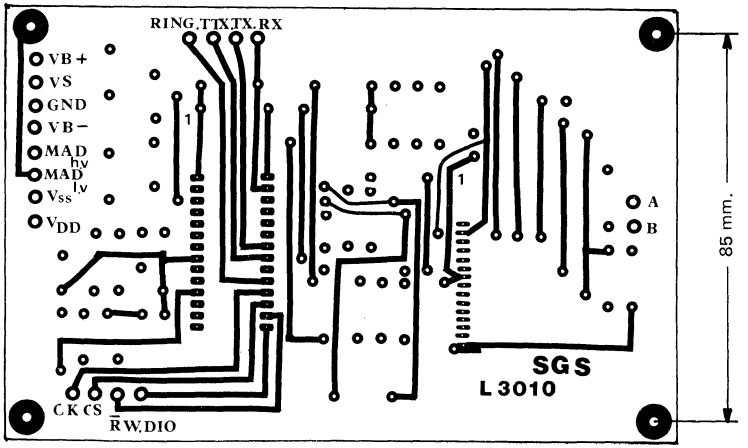
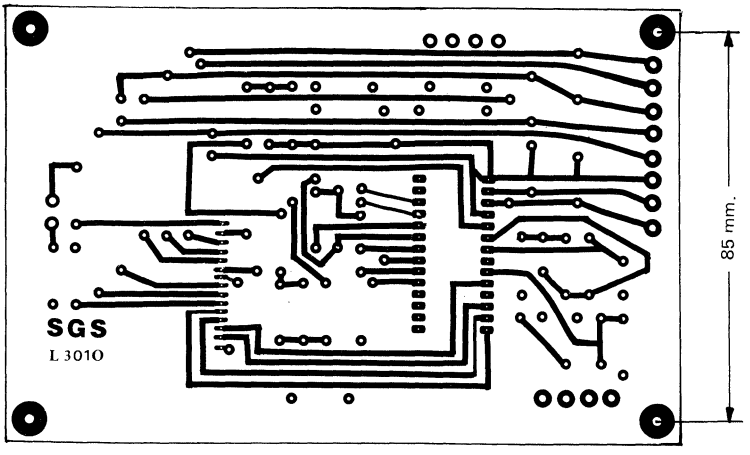

LINE TERMINALS
A
B
R1
R2
S-9215
L3000
L3010
+72
-48
-5
+5
D1
C3
C4
R3
C3
R4
C12
R10
R11
C11
C4
C5
C6
R5
R6
C11
R7
R8
C16
R9
C8
C9
C9
RTTX
RRING
RRX
TX
C
RX
D
CK
CS
R/W
DI/O
RING
TTX
E
RTTX, RRING, RRX are set just during evaluation phase, not to let pin 19, 21, 27 float; they are not necessary when right interfaces are connected to the system.

Fig. 2 - Evaluation P.C.B.

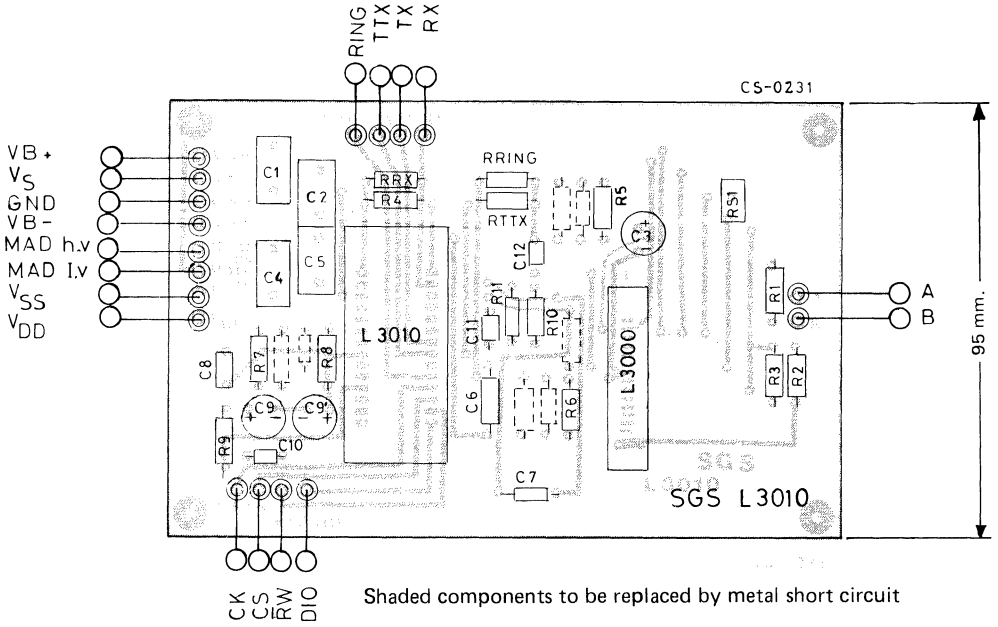


Component Side



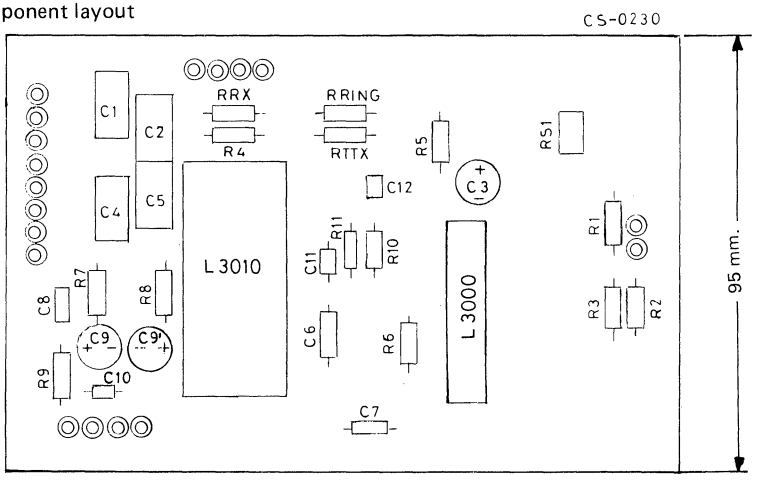
Solder Side

Fig. 3 - P.C. Track and component layout



Shaded components to be replaced by metal short circuit

Fig. 4 - Component layout



ELECTRICAL CHARACTERISTICS

Parameter		Test Condition	Min.	Typ.	Max.	Unit	Fig.
STAND-BY							
V_L	Output voltage						
		I_L = 0mA	37		39	V	
		I_L = 8mA	35.5		37.8	V	
	at line terminals	I_L = 8mA	35.5		37.3	V	
I_{LCC}	Short circuit current				12	mA	
I_O	On-hook detection threshold				6	mA	
I_F	Off-hook detection threshold		7.5			mA	
V_L	Simmetry to ground	I_L = 0mA			750	mV	5
DC OPERATION - NORMAL BATTERY							
V_L	Output voltage						
	at L3000 terminals	I_L = 0mA	37		39	V	
		I_L = 20mA	33.3		42.5	V	
	at line terminals	I_L = 50mA	23		29	V	
I_{LCC}	Short circuit current				75	mA	
I_{LOL}	Overload detection threshold		65			mA	
I_O	On-hook detection threshold		6			mA	
I_F	Off-hook detection threshold				7.5	mA	
I_T	Ground current detection threshold	I_L > 5mA	$I_L/2.5$		$I_L/2$	mA	
DC OPERATION - BOOST BATTERY							
V_L	Output voltage						
	at L3000 termination	I_L = 0mA	92		98	V	
		I_L = 20mA	83		91	V	
	at line termination	I_L = 50mA	70		80	V	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
AC OPERATION							
Z_{TX}	Sending output impedance				10	Ω	
Z_{AX}	Receiving input impedance		100			KΩ	
THD	Distortion at 2W and 4W terminals	V_H = 1.75 V_{peak}			0.5	%	
	Return loss at 2W terminals	f = 300 to 500Hz f = 500 to 3400Hz	16.5 20			dB dB	6
E_S	Echo suppression	f = 500 to 3000Hz f = 300 to 500Hz and 3000 to 3400Hz	24 16			dB dB	7
G_S	Sending Gain	V_{SO}= 0dBm f = 1020Hz	-0.2		+0.2	dB	8
G_S	Sending gain flatness vs. freq.	f = 300/3400Hz freq. = 820Hz without teletax filter with teletax filter	 -0.1 -0.2		 +0.1 +0.2	 dB	
G_S	Gain Accuracy	f = 820Hz $V_{SO\ ref}$ = -10dBm V_{SO} = +4/-40dBm V_{SO} = -40/-60dBm	 -0.1 -0.2		 +0.1 +0.2	 dB dB	
G_R	Receiving gain	V_{RI} = 0dBm f = 1020Hz	-0.2		+0.2	dB	9
G_R	Receiving gain flatness vs. freq.	f = 300/3400Hz freq. = 1020Hz	-0.1		+0.1	dB	
G_R	Gain Accuracy	f = 820Hz V_{RI}= -10dBm V_{RI}= +4/-40dBm V_{RI}= -40/-60dBm	 -0.1 -0.2		 +0.1 +0.2	 dB dB	
N_p	Psophometric noise	TX terminals Line terminals		-75 -75		μV dBmop	
SVRR	Supply voltage rejection	f = 300/3400Hz (both direction)			-40	dB	10
	Longitudinal to transversal conversion	Sending			-49		11
	Transversal to longitudinal conversion	Receiving			-49		12
	Propagation time	Both direction			40	μs	
	Propagation time distortion				25	μs	9
V_{LTTX}	Output signal		1.8		2.2	V_{rms}	9
THD	Harmonic distortion	V_{TTX} = 2V			5	%	9
	Teletax amplifier input impedance		100			KΩ	9
V_R	Residial voltage at TX terminals	with teletax filter			0.6	V_{rms}	13
	Rise time and fall time of teletax signal envelope		10		30	ms	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Condition	Min.	Typ.	Max.	Unit	Fig.
RINGING PHASE							
V_{LR}	Superimposed DC	$R_L = \infty$	18		26	V	
V_{ACR}	Ringing signal amplified	$R_L = \infty$	57		63	V_{rms}	
V_{LR}	Superimposed DC voltage	R_L = 1KΩ	16.8		24.8	V	
V_{ACR}	Ringing signal	Z_L = 1KΩ // 1μF	56.5		62.5	V_{rms}	
I_F	DC off-hook detection threshold			2		mA	
	Current limitation			100		mA_{rms}	
	Ringing current simmetry				2	V_{rms}	14
THD_R	Harmonic distortion				5	%	
	Ringing input impedane		100			KΩ	
	Residual signal at TX output				600	mV_{rms}	
	Ring trip detection time				90	ms	
	Off hook status transmission delay				125	ms	
	Cut off of ringing	Ring trip not confirmed			125	ms	

TEST CIRCUITS

Fig. 5

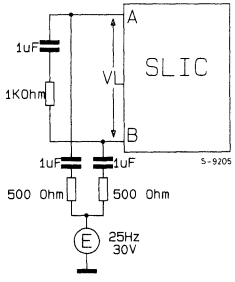
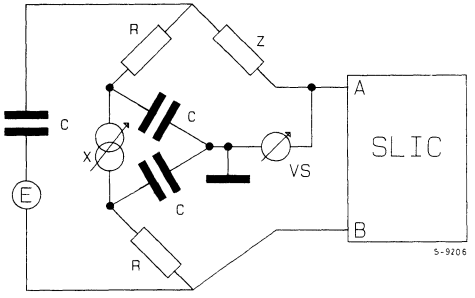


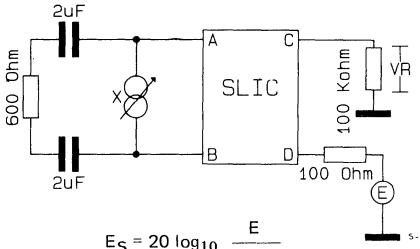
Fig. 6



$$RL = 20 \log \frac{Z_L - Z}{Z + Z_L} = 20 \log \frac{2V_s}{E}$$

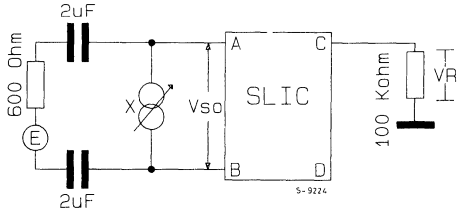
TEST CIRCUITS (continued)

Fig. 7



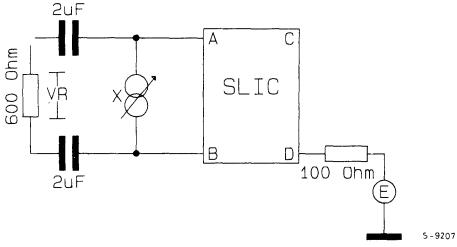
$$E_S = 20 \log_{10} \frac{E}{V_R}$$

Fig. 8



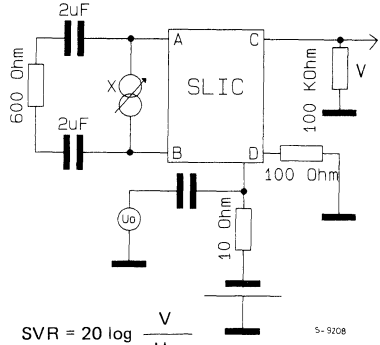
$$G_S = 20 \log_{10} \frac{V_R}{V_{SO}}$$

Fig. 9



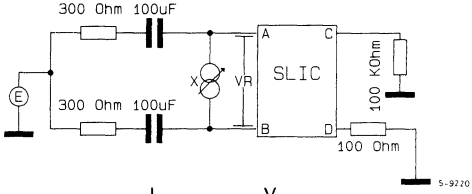
$$G_R = 20 \log_{10} \frac{V_R}{E}$$

Fig. 10



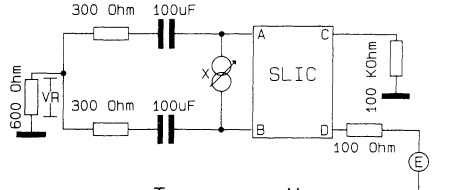
$$SVR = 20 \log \frac{V}{U_O}$$

Fig. 11



$$\frac{L}{T} = 20 \log \frac{V_R}{E}$$

Fig. 12



$$\frac{T}{L} = 20 \log_{10} \frac{V_R}{E}$$

TEST CIRCUITS (continued)

Fig. 13

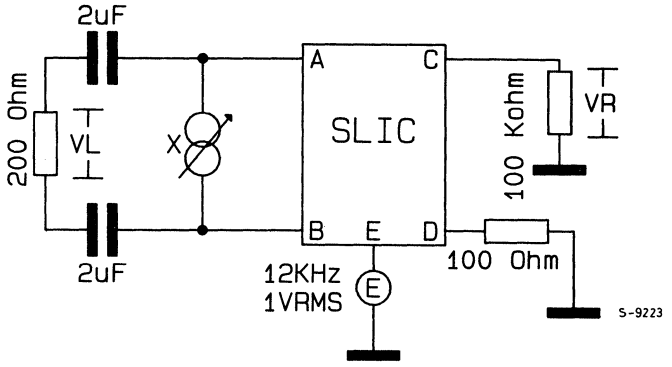
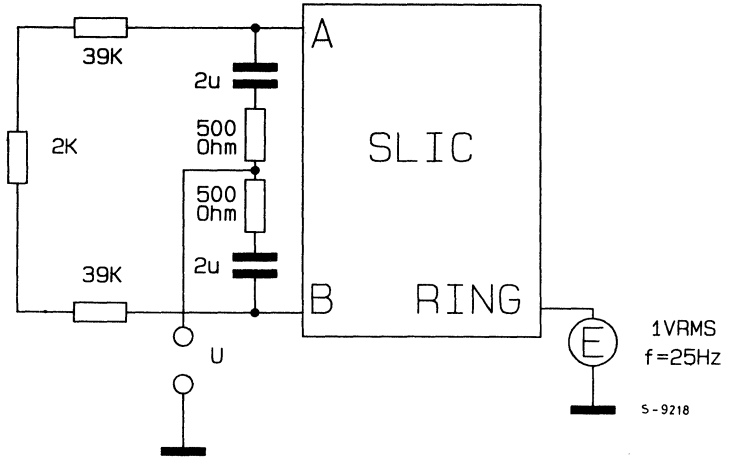


Fig. 14



HOW TO PROTECT SGS SLIC

Terminals Line-A and Line-B of the high voltage line interface L3000 must be protected to ground against overvoltages that might damage the sensitive internal circuitry, causing failure or degradation of SLIC's performance.
Protection must be provided on both line terminations, A and B. and in both directions, positive and negative.

Because of the wide supply voltage range requested in the different countries and application, and due to the broad tolerances on the exchange batteries, a fully programmable suppressor has been developed, to be controlled directly by the external supply.

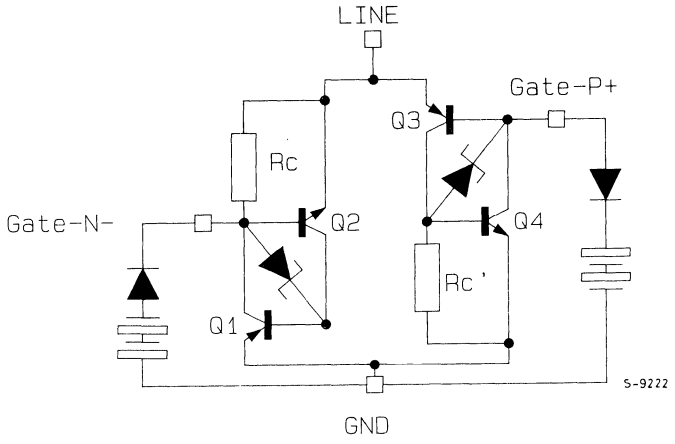
Operation of L3121

The suppressor, Fig. 1, is based on a couple of SCR connected in antiparallel and housed in the same package, which switch to short circuit when the gates are properly triggered, and, due to R_C (a few Ω), recover to high impedance when the current drops below a minimum value (about 200mA).

The L3121 can be controlled either through gate-N- or gate-P+ (Fig. 1).

During overvoltages the peak between line and ground, may overcome by some Volts the value of the triggering reference.

Fig. 1 - L3121 schematic diagram



Application with SLIC against negative overvoltage

When the voltage at line-A (or line-B) decreases about 2V below $-V_{DD}$ ($-V_{DD}-V_{D1}-V_{BE}$), D1 and Q2 start conducting and L3121 switches to short circuit protecting pin 1 (or 15). D1 prevents short circuit between GND and $-V_{DD}$. A resistor of 30Ω is requested at pin 1 (or 15) for a proper operation of the SLIC. This resistance may be splitted in:

- R1 (10Ω), because of some volts overshoot that might occour during fast clamping or L3121, degradating SLIC in case of direct connection;
- R2 (20Ω), to separate L3121 from the external gas-discharge tube, constituting the primary protection.

Application with SLIC against positive overvoltage

As shown in Fig. 2, pin 2 (V_S) is internally connected to pin 4 (GND), through a diode, and to pin 3 ($+V_{CC}$) through a PNP darlington. The darlington, normally off, is switched on in "Boosted Battery" and ringing conditions, to provide requested overfeed (+60 to +72V) for the output stage of the line interface.

A positive overvoltage on the line activates Q3 (base-emitter) and D2, pulling up the supply of the output stage, whichever is the feed condition, and preventing dangerous inversion between V-supply and V-out.

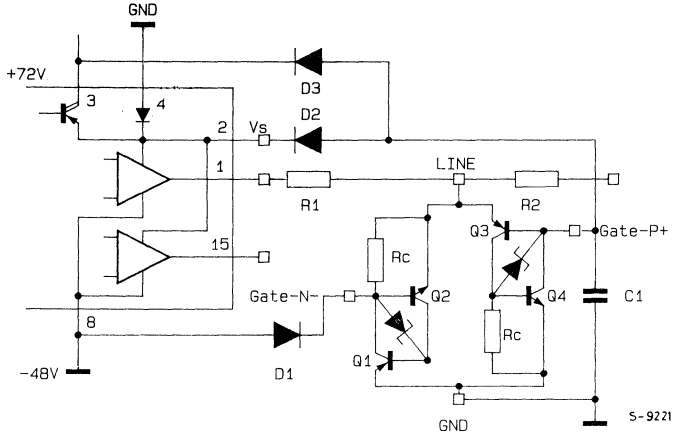
When the line voltage overcomes V_{CC} by about 2V (V_{CC} + V_{BE} + V_{D3}), Q3 and D3 start conducting and switch the L3121 to short circuit, protecting pin 1 (or 15). D2 prevents short circuit between $+V_{CC}$ and GND (through PNP darlington).

In case of very fast rising time, an additional capacitor, C1 - min 10nF is to be added between gate-P and cathode, to speed up Q3.

In conclusion, the L3121, gate controlled transient suppressor, when properly connected and paralleled is able to guarantee a complete protection against positive/negative and static/dynamic overvoltages.

Test performed with a circuit in accordance with the above diagram have given positive results both against lighting stresses and mains inductions.

Fig. 2 - Complete schematic for pulse suppression (The whole circuitry must be duplicated for pin 15)

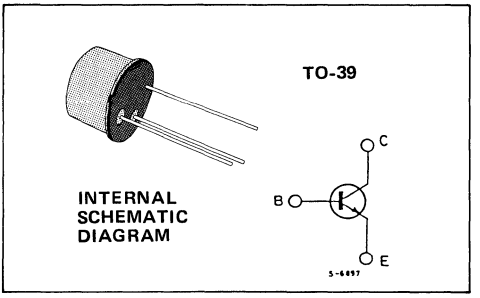


$R_1 + R_2 = R_p$

BFR36

CATV ULTRA-LINEAR HIGH-GAIN TRANSISTOR

The BFR36 is a multi-emitter silicon planar epitaxial NPN transistor in Jedec TO-39 metal case.
It is designed for CATV-MATV amplifier applications over a wide frequency range (40 to 860MHz).
The device features very good intermodulation properties, very low reverse capacitance, high power gain and high power dissipation.



ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	40	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	30	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	3	V
I_C	Collector current	200	mA
I_{CM}	Collector peak current	400	mA
P_{tot}	Total power dissipation at $T_{amb} \leq 40°C$	0.8	W
	at $T_{case} \leq 50°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-55 to 200	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	30	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

BFR36

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = 20V V_{CB} = 20V	 T_{amb} = 150°C			150 20	nA μA
$V_{(BR)\ CBO}$	Collector-base breakdown voltage (I_E = 0)	I_C = 100μA		40			V
$V_{CEO\ (sus)}$ *	Collector-emitter sustaining voltage (I_B = 0)	I_C = 10mA		30			V
$V_{(BR)\ EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = 100μA		3			V
V_{CEK} **	Collector-emitter knee voltage	I_C = 100mA			700	750	mV
V_{BE}	Base emitter voltage	I_C = 70mA	V_{CE} = 5V		750		mV
h_{FE} *	DC current gain	I_C = 70mA I_C = 150mA I_C = 70mA I_C = 150mA	V_{CE} = 5V V_{CE} = 5V V_{CE} = 15V V_{CE} = 15V	60 60 65 65	130		
f_T	Transition frequency	V_{CE} = 15V	f = 100MHz I_C = 70mA I_C = 150mA	1	 1.4 12		 GHz GHz
C_{EBO}	Emitter-base capacitance	I_C = 0 f = 1MHz	V_{EB} = 0.4V		7		pF
C_{CBO}	Collector-base capacitance	I_E = 0 f = 1MHz	V_{CB} = 15V			3	pF
C_{re}	Reverse capacitance	I_C = 0 f = 1MHz	V_{CE} = 15V		1.7	2.2	pF
NF	Noise figure	V_{CE} = 15V f = 200MHz	R_g = 50Ω I_C = 30mA I_C = 70mA		 4 4.5		 dB dB
G_{pe}	Power gain (see test circuit)	I_C = 70mA	V_{CE} = 18V f = 200MHz f = 500MHz f = 800MHz		 16 9.5 6.5		 dB dB dB
P_o (1)	Output power (see test circuit)	I_C = 70mA	V_{CE} = 18V f = 200MHz f = 800MHz	 130 70	 150 90		 mW mW

* Pulsed: pulse duration = 300μs, duty cycle = 1%

** I_B = Value corresponding to I_C = 110mA and V_{CE} = 1V

(1) Output VSWR < 2, d_{im} = -3dB @ f = 2 (f_q-f_p), f_p = 798MHz and f_q = 802MHz

Fig. 1 - RF amplifier circuit for power gain test (f = 200MHz)

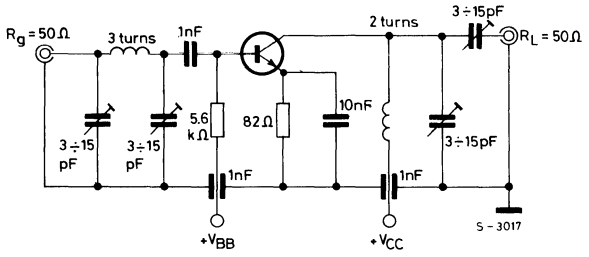


Fig. 2 - Power gain vs. collector current

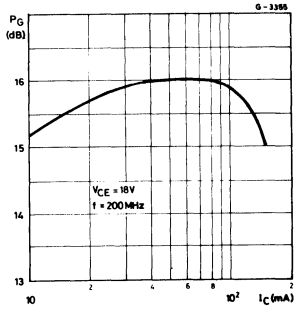


Fig. 3 - High frequency current gain vs. collector curent

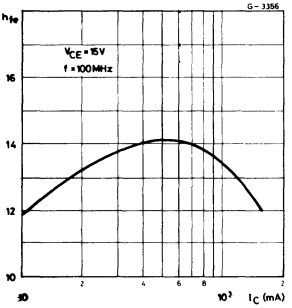


Fig. 4 - Reverse capacitance

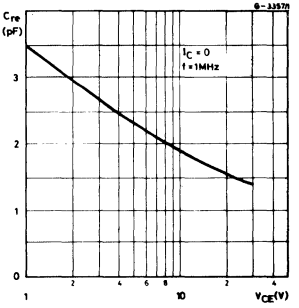


Fig. 5 - Power rating chart

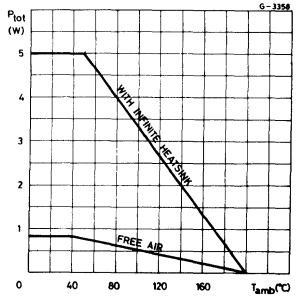


Fig. 6 - Input impedance S_{11e} (normalized 50Ω)

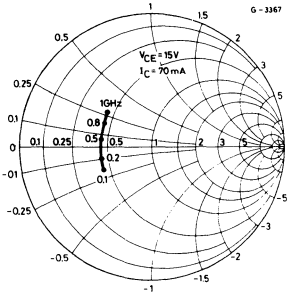


Fig. 7 - Forward transfer coefficient S_{21e}

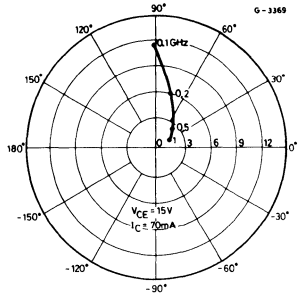


Fig. 8 - Reverse transfer coefficient S_{12e}

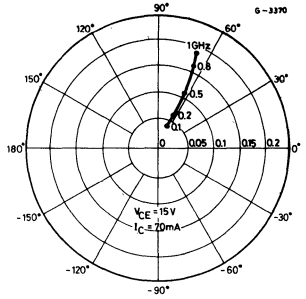


Fig. 9 - Output impedance S_{22e} (normalized 50Ω)

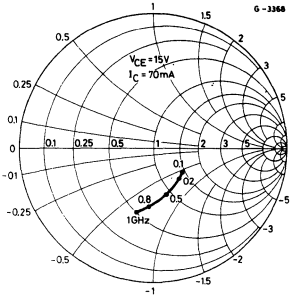


Fig. 10 - CATV - extender line amplifier

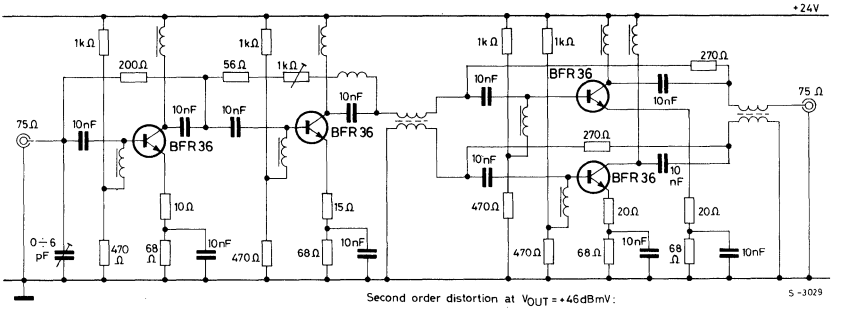
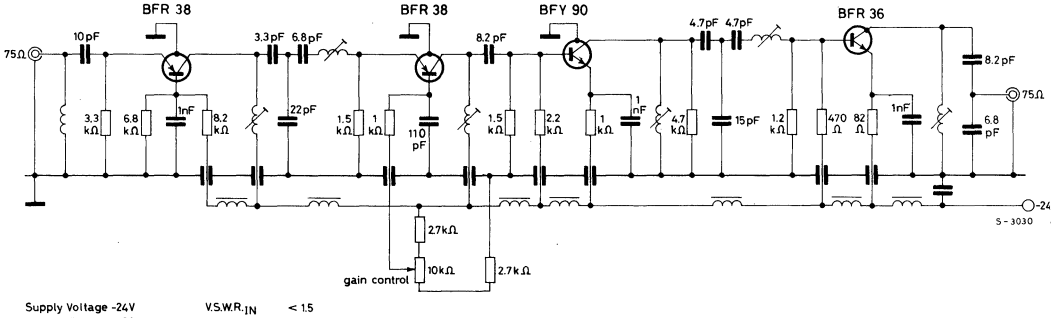


Fig. 11 - MATV - 200MHz channel amplifier



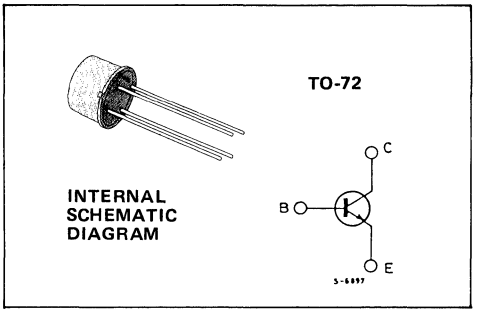
Supply Voltage -24V
Current Drain 100mA
P.G. 70dB
NF 3dB

$V.S.W.R._{IN}$ < 1.5
$V.S.W.R._{OUT}$ < 2
P_{OUT} 120mW at dim -30dB
Gain Control > 30dB

BFR99A

WIDE BAND VHF/UHF AMPLIFIER

The BFR99A is a silicon planar epitaxial PNP transistor in Jedec TO-72 metal case, particularly designed for wide band common-emitter linear amplifier applications up to 1GHz.
It features very high f_T, very low reverse capacitance, very good cross-modulation properties and very low noise. The type is complementary to BFY90.



ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	-25	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	-25	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	-3	V
I_C	Collector current	-50	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 25°C$	225	mW
	at $T_{case} \leqslant 25°C$	360	mW
T_{stg}, T_j	Storage and junction temperature	-55 to 200	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	486	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	777	°C/W

BFR99A

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = -15V			-100	nA
$V_{(BR)\ CBO}$	Collector-base breakdown voltage (I_E = 0)	I_C = -100μA	-25			V
$V_{CEO\ (sus)}$ *	Collector-emitter sustaining voltage (I_B = 0)	I_C = -5mA	-25			V
$V_{(BR)\ EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = -10μA	-3			V
V_{CEK} **	Collector-emitter knee voltage	I_C = -20mA		-0.8		V
V_{BE}	Base-emitter voltage	I_C = -10mA V_{CE} = -10V		-0.75		V
h_{FE} *	DC current gain	I_C = -1mA V_{CE} = -10V I_C = -10mA V_{CE} = -10V I_C = -20mA V_{CE} = -10V	 25 20	75 80		V
f_T	Transition frequency	I_C = -10mA V_{CE} = -15V f = 100MHz	1.4	2.3		GHz
C_{re}	Reverse capacitance	I_C = 0 V_{CE} = -15V f = 1MHz		0.4		pF
NF	Noise figure	I_C = -3mA V_{CE} = -15V R_g = 50Ω f = 200MHz f = 800MHz I_C = -10mA V_{CE} = -15V R_g = 50Ω f = 200MHz f = 800MHz		 2.5 3.5 3 4	 4 5	 dB dB dB dB
G_{pe}	Power gain	I_C = -10mA V_{CE} = -15V f = 800MHz		10		dB
P_o	Output power	I_C = -10mA V_{CE} = -15V f = 800MHz		14		mW
$\lvert S_{21e} \rvert^2$	Transducer power gain	I_C = -10mA V_{CE} = -15V $R_g = R_L$ = 50Ω f = 800MHz		8		dB

* Pulsed: pulse duration = 300μs, duty cycle = 1%

** I_B = value corresponding to I_C = -22mA and V_{CE} = -1V

Fig. 1 - Transition frequency

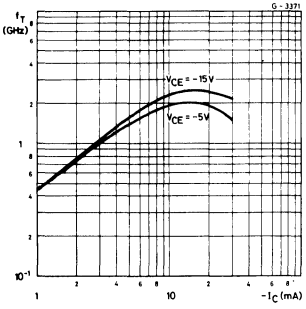


Fig. 2 - Reverse capacitance

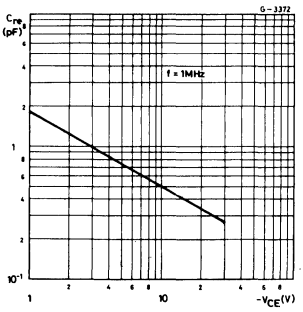


Fig. 3 - Noise figure vs. collector current

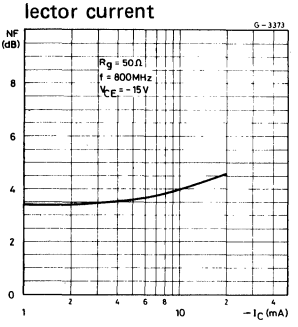


Fig. 4 - Noise figure vs. frequency

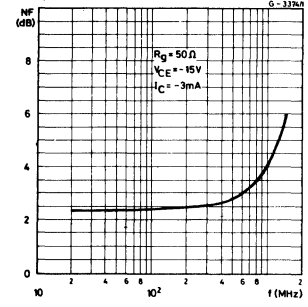


Fig. 5 - Noise figure vs. ambient temperature

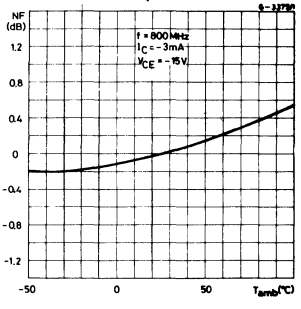


Fig. 6 - Transducer power gain

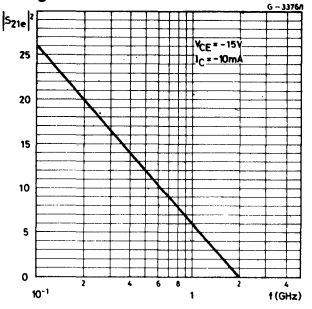


Fig. 7 - Input impedance S_{11e} (50Ω normalized)

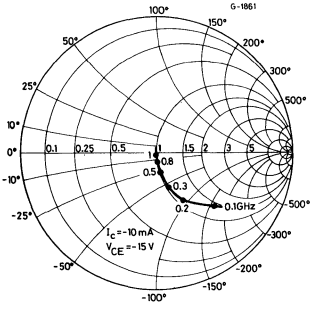


Fig. 8 - Forward transfer coefficient S_{21e}

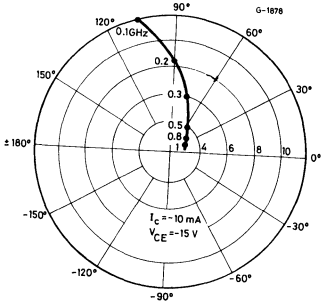


Fig. 9 - Reverse transfer coefficient S_{12e}

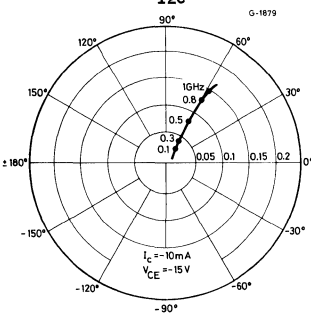


Fig. 10 - Output impedance S_{22e} (50Ω normalized)

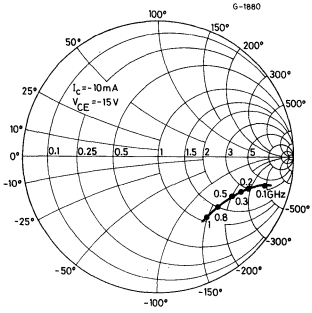
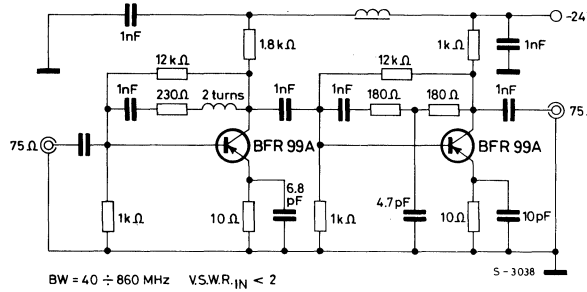
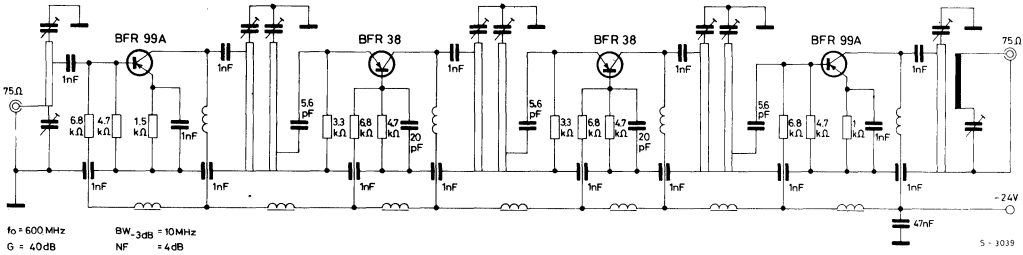


Fig. 11 - Wide band MATV amplifier



BW = 40 ÷ 860 MHz
G = 16 dB
NF < 5dB
V.S.W.R.$_{IN}$ < 2
V.S.W.R.$_{OUT}$ < 2
V_{OUT} = 100mV for 1% Crossmodulation

Fig. 12 - MATV channel amplifier

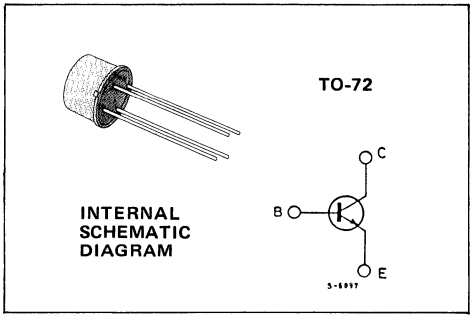


fo = 600 MHz
G = 40dB
V.S.W.R.$_{IN}$ < 1.5
V.S.W.R.$_{OUT}$ < 1.5
BW_{-3dB} = 10MHz
NF = 4dB
P_{OUT} = 15mW @ dim = 30dB

BFY90

WIDE BAND VHF/UHF AMPLIFIERS

The BY90 is a silicon planar epitaxial NPN transistors in Jedec TO-72 metal case, particularly designed for wide band common-emitter linear amplifier applications up to 1GHz.
They feature high f_T, low reverse capacitance, good cross-modulation properties and low noise.



ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	30	V
V_{CER}	Collector-emitter voltage ($R_{BE} \leqslant 50\Omega$)	30	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	15	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	2.5	V
I_C	Collector current	25	mA
I_{CM}	Collector peak current ($f \geqslant 1MHz$)	50	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 25°C$	200	mW
T_{stg}, T_j	Storage and junction temperature	-65 to 200	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	580	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	880	°C/W

BFY90

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = 15V				10	nA
V_{CEK} *	Collector-emitter knee voltage	I_C = 20mA				0.75	V
h_{FE}	DC current gain	I_C = 2mA I_C = 25mA	V_{CE} = 1V V_{CE} = 1V	25 20		150 125	
f_T	Transition frequency	V_{CE} = 5V I_C = 2mA I_C = 25mA	f = 500MHz	 1 1.3	 1.1 1.4		 GHz GHz
C_{CBO} (1)	Collector-base capacitance	I_E = 0 f = 1MHz	V_{CB} = 10V			1.5	pF
C_{re} (2)	Reverse capacitance	I_C = 2mA f = 1MHz	V_{CE} = 5V		0.6	0.8	pF
NF (2)	Noise figure	I_C = 2mA R_g = optimized R_g = optimized R_g = 50Ω R_g = optimized	V_{CE} = 5V f = 100KHz f = 200MHz f = 500MHz f = 800MHz		 2.5 5.5	 4 3.5 5 	 dB dB dB dB
G_{pe} (2)	Power gain (not neutralized)	I_C = 14mA f = 200MHz f = 800MHz	V_{CE} = 10V	 21 	 23 8	 	 dB dB
P_o	Output power	I_C = 14mA d_{im} = -30dB (3) Channel 9 (4) Channel 62	V_{CE} = 10V	 10 	 12 12	 	 mW mW

* I_B = value for which I_C = 22mA at V_{CE} = 1V
(1) Shield lead not grounded
(2) Shield lead grounded
(3) f_p = 202MHz, f_q = 205MHz, $f_{(2q-p)}$ = 208MHz
(4) f_p = 798MHz, f_q = 802MHz, $f_{(2q-p)}$ = 806MHz

Fig. 1 - Power rating chart

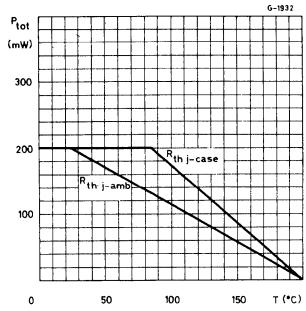


Fig. 2 - Transition frequency

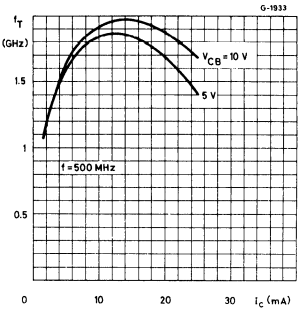


Fig. 3 - Collector-base capacitance

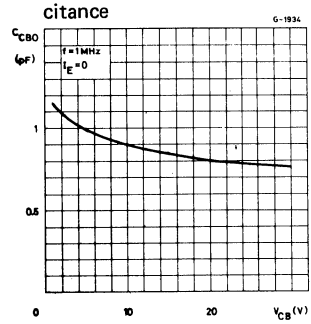


Fig. 4 - Noise figure vs. collector current

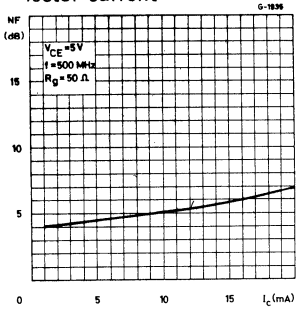


Fig. 5 - Noise figure vs. frequency

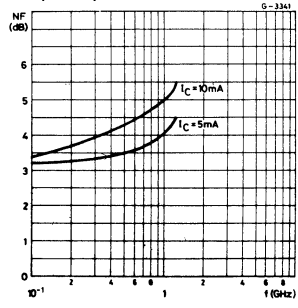
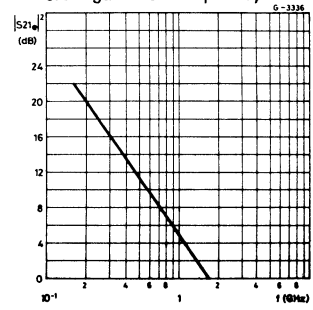


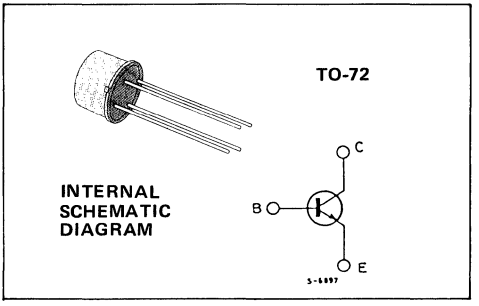
Fig. 6 - Forward transmission gain vs. frequency



BFX73
2N918
2N3600

HIGH-FREQUENCY OSCILLATORS AND AMPLIFIERS

The BFX73, 2N918 and 2N3600 are silicon planar epitaxial NPN transistors in Jedec TO-72 metal case.
They are designed for low-noise VHF amplifiers, oscillators up to 1GHz, non-neutralized IF amplifiers and non-saturating circuits with rise and fall times of less than 2.5ns.



ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	30	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	15	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	3	V
I_C	Collector current	50	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 25°C$	200	mW
	at $T_{amb} \leqslant 25°C$	300	mW
T_{stg}, T_j	Storage and junction temperature	-65 to 200	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	584	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	875	°C/W

BFX73
2N918
2N3600

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = 15V V_{CB} = 15V T_{amb} = 150°C			10 1	nA μA
$V_{(BR)\ CBO}$	Collector-base breakdown voltage (I_E = 0)	I_C = 1μA	30			V
$V_{CEO\ (sus)}$	Collector-emitter sustaining voltage (I_B = 0)	I_C = 3mA	15			V
$V_{(BR)\ EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = 10μA	3			V
$V_{CE\ (sat)}$	Collector-emitter saturation voltage	I_C = 10mA I_B = 1mA			0.4	V
$V_{BE\ (sat)}$	Base-emitter saturation voltage	I_C = 10mA I_B = 1mA			1	V
h_{FE}	DC current gain	I_C = 3mA V_{CE} = 1V for **2N918/BFX73** for **2N3600**	 20 20	50	 150	
f_T	Transition frequency	for **2N918/BFX73** I_C = 4mA V_{CE} = 10V f = 100MHz for **2N3600** I_C = 5mA V_{CE} = 6V f = 100MHz	 600 850	 900 	 1500	 MHz MHz
C_{EBO}	Emitter-base capacitance	I_C = 0 V_{EB} = 0.5V f = 1MHz for **2N918/BFX73** for **2N3600**		 1.4	 2	 pF pF
C_{CBO}	Collector-base capacitance (for **2N918/BFX73** only)	I_E = 0 f = 1MHz V_{CE} = 0 V_{CE} = 10V		1.8 1	3 1.7	pF pF
C_{re}	Reverse capacitance (for **2N3600** only)	I_C = 0 V_{CB} = 10V f = 1MHz			1	pF
NF	Noise figure	I_C = 1.5mA V_{CE} = 6V R_g = 50Ω f = 200MHz for **2N3600** I_C = 1mA V_{CE} = 6V R_g = 400Ω f = 60MHz for **2N918/BFX73** for **2N3600**			 4.5 6 3	 dB dB dB
G_{pe}	Power fain	R_g = 50Ω f = 200MHz for **2N918/BFX73** I_C = 6mA V_{CE} = 12V for **2N3600** I_C = 5mA V_{CE} = 6V	 15 17	 21 	 24	 dB dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min	Typ	Max	Unit
P_o *	Output power	I_C = 12mA f = 500MHz	V_{CB} = 10V				
			for **2N918/BFX73** for **2N3600**	30 20	40		mW mW
η	Collector efficiency (for **2N918/BFX73** only)	I_C = 12mA f = 500MHz	V_{CB} = 10V	25			%
$r_{bb'}$, $C_{b'c}$	Feedback time constant (for **2N3600** only)	I_C = 5mA f = 31.9MHz	V_{CB} = 6V	4		15	ps

* See test circuits

Fig. 1 - DC current gain

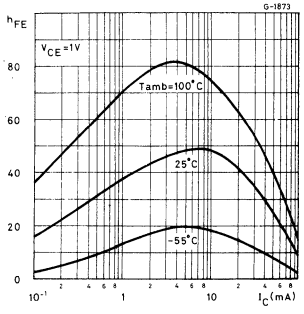


Fig. 2 - Transition frequency

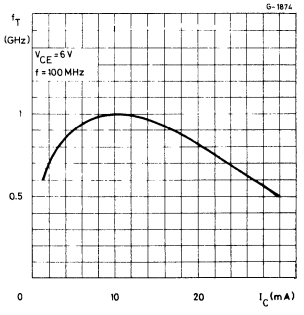
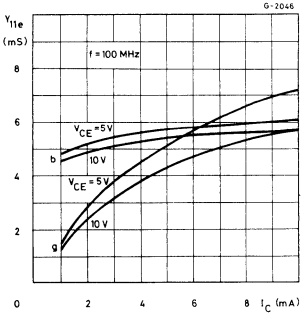


Fig. 3 - Input admittance vs. collector current



BFX73
2N918
2N3600

Fig. 4 - Forward transadmittance vs. collector current

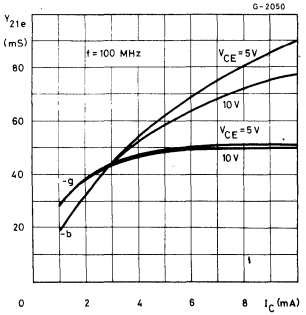


Fig. 5 - Reverse transadmittance vs. collector current

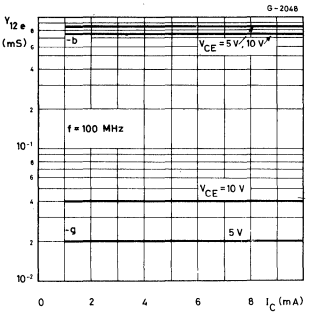


Fig. 6 - Output admittance vs. collector-current

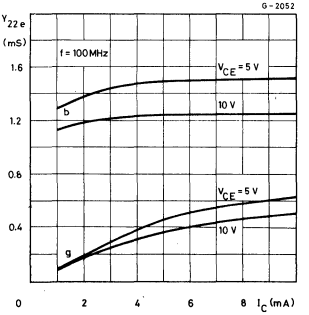


Fig. 7 - Input admittance vs. frequency

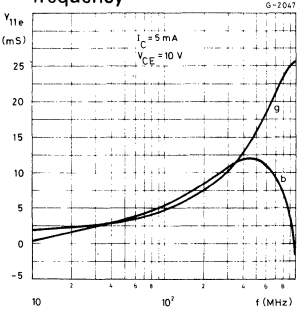


Fig. 8 - Forward transadmittance vs frequency

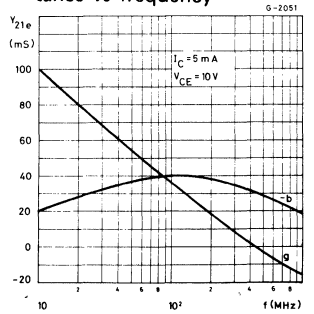


Fig. 9 - Reverse transadmittance vs. frequency

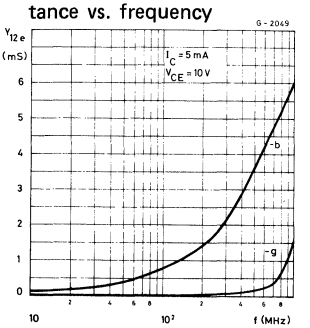


Fig. 10 - Output admittance vs. frequency

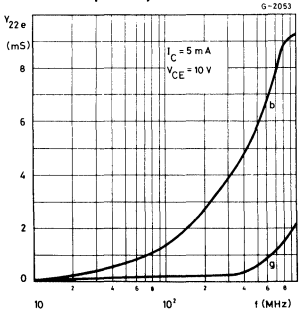
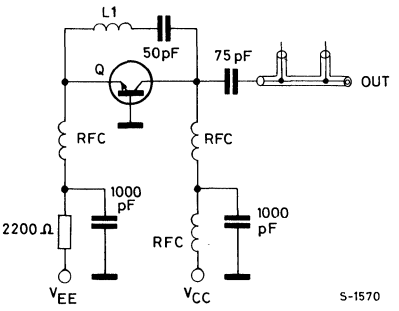


Fig. 11 - 500MHz oscillator test circuit

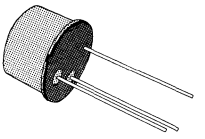


2N3137

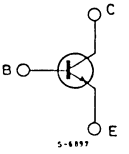
ADVANCE DATA

RF AMPLIFIER

The 2N3137 is a silicon planar epitaxial NPN transistor in a TO-39 metal case. It is primarily designed for application as a Class-C, RF power amplifier.
In addition to the large signal capabilities, the low noise and high transition frequency of the 2N3137 provide excellent performance in a variety of linear amplifier for telecommunication applications.



TO-39



INTERNAL SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	40	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	20	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	4	V
P_{tot}	Total power dissipation at $T_{amb} \leq 25°C$	0.6	W
	at $T_{amb} \leq 25°C$	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 200	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	175	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	292	°C/W

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

2N3137

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = 20V V_{CB} = 20V T_{amb} = 150°C		0.12 0.1	50 50	nA μA
$V_{(BR)\ CBO}$	Collector-base breakdown voltage (I_E = 0)	I_C = 100μA	40			V
$V_{CEO\ (sus)}$ *	Collector-emitter sustaining voltage (I_B = 0)	I_C = 15nA	20			V
$V_{(BR)\ EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = 100μA	4			V
$V_{CE\ (sat)}$	Collector-emitter saturation voltage	I_C = 50mA I_B = 50mA		0.12	0.3	V
h_{FE} *	DC current gain	I_C = 50mA V_{CE} = 5V	20	70	120	
G_{pe}	Power gain (class-C)	V_{CE} = 20V f = 250MHz P_i = 100mW	6	7		dB
NF	Noise figure	V_{CE} = 10V I_C = 30mA f = 200MHz R_g = 50Ω		4		dB
C_{CBO}	Collector-base capacitance	V_{CB} = 10V f = 1MHz		2.8	3.5	pF
f_T	Transition frequency	I_C = 50mA V_{CE} = 10V	500	750		MHz
η	Collector efficiency	V_{CE} = 20V f = 250MHz P_i = 100mW	40	60		%

* Pulsed: pulse duration = 300μs, duty cycle = 1%

Fig. 1 - DC current gain

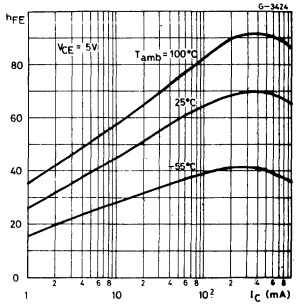


Fig. 2 - Collector-emitter saturation voltage

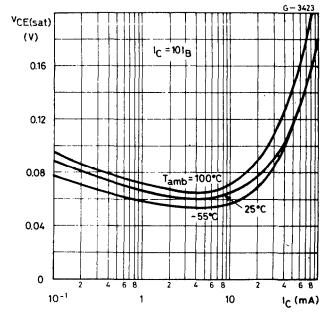


Fig. 3 - Base-emitter saturation voltage

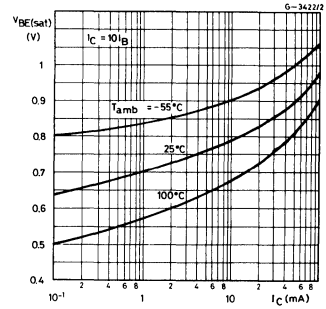


Fig. 4 - Contours of constant transition frequency

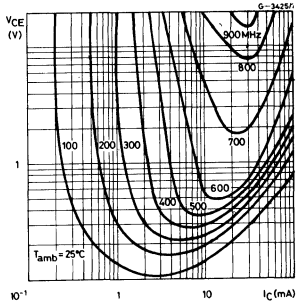


Fig. 5 - Collector-base capacitance

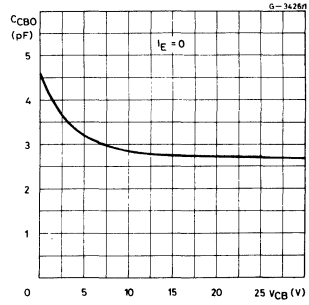
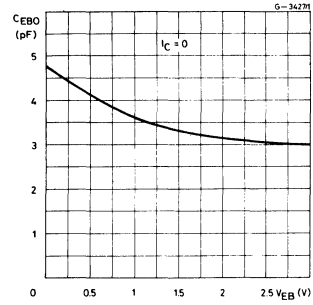


Fig. 6 - Emitter-base capacitance

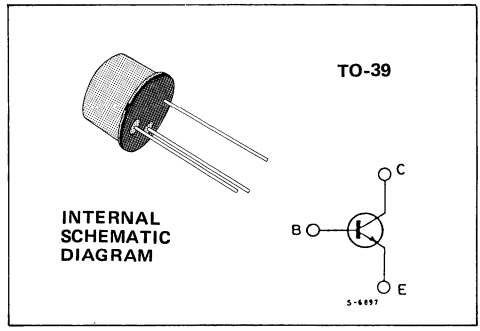


2N5109

ADVANCE DATA

CATV ULTRA-LINEAR HIGH GAIN TRANSISTOR

The 2N5109 is a multi-emitter silicon planar epitaxial NPN transistor in Jedec TO-39 metal case. It is designed for CATV-MATV amplifier applications over a wide frequency range (40 to 860MHz)



ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E = 0$)	40	V
V_{CER}	Collector-emitter voltage ($R_{BE} \leqslant 10\Omega$)	40	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	20	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	3	V
I_C	Collector current	0.4	A
I_B	Base current	0.4	A
P_{tot}	Total power dissipation at $T_{amb} \leqslant 25°C$	1	W
	at $T_{amb} \leqslant 75°C$	2.5	W
T_{stg}, T_j	Storage and junction temperature	-65 to 200	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	175	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

2N5109

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Collector cutoff current (V_{BE} = -1.5V)	V_{CE} = 35V V_{CE} = 15V T_{amb} = 150°C			5 5	mA mA
I_{CEO}	Collector cutoff current (I_B = 0)	V_{CE} = 15V			20	μA
I_{EBO}	Emitter cufoff current (I_C = 0)	V_{EB} = 3V			0.1	mA
$V_{(BR)\ CBO}$	Collector-base breakdown voltage (I_E = 0)	I_C = 0.1mA	40			V
$V_{CE\ (sus)}$ *	Collector-emitter sustaining voltage (R_{BE} = 10Ω)	I_C = 5mA	40			V
$V_{CEO\ (sus)}$	Collector-emitter sustaining voltage (I_B = 0)	I_C = 5mA	20			V
$V_{CE\ (sat)}$	Collector-emitter saturation voltage	I_C = 100mA I_B = 10mA			0.5	V
h_{FE} *	DC current gain	I_C = 50mA V_{CE} = 15V I_C = 360mA V_{CE} = 5V	70 5		210	— —
f_T	Transition frequency	I_C = 50mA V_{CE} = 15V f = 200MHz	1.2			GHz
C_{CBO}	Collector-base capacitance	I_E = 0 V_{CB} = 15V f = 1MHz			3.5	pF
NF	Noise figure	I_C = 10mA V_{CE} = 15V R_g = 50Ω f = 200MHz		3		dB
G_{pe}	Power gain (see test circuit)	I_C = 10mA V_{CE} = 15V f = 200MHz P_i = -10dBm	11			dB

* Pulsed: pulse duration = 300μs, duty cycle = 1%

Fig. 1 - Test circuit for power gain measurement (f = 200MHz)

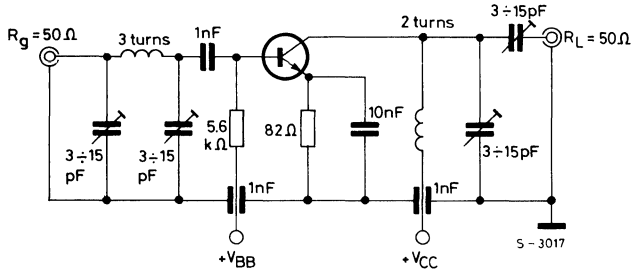


Fig. 2 - High frequency current gain

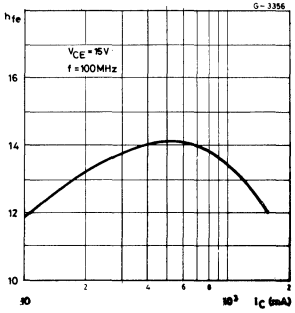


Fig. 3 - Power gain vs. collector current

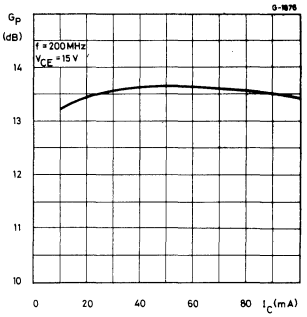


Fig. 4 - Input impedance S_{11e} (normalized 50Ω)

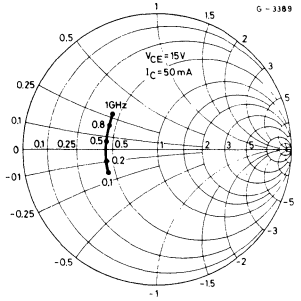


Fig. 5 - Forward transfer coefficient S_{21e}

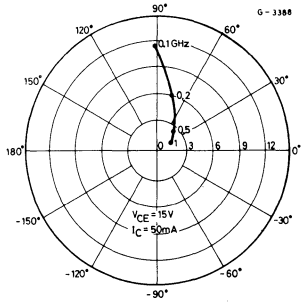


Fig. 6 - Reverse transfer coefficient S_{12e}

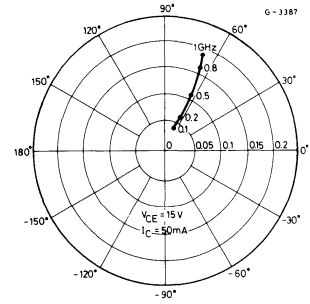
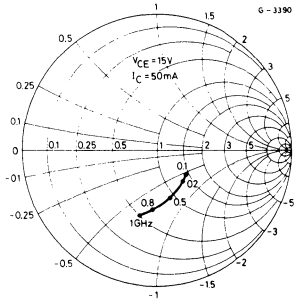
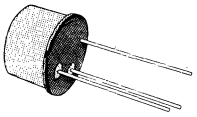


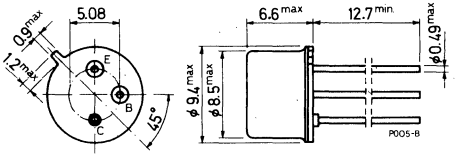
Fig. 7 - Output impedance S_{22e} (normalized 50Ω)



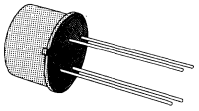
PACKAGES

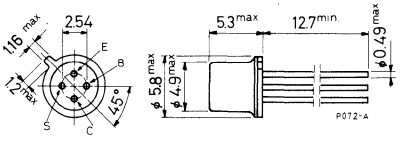
TO-39



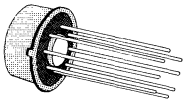


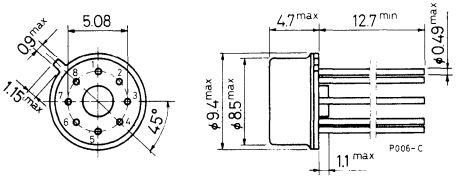
TO-72





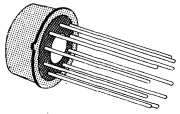
TO-99

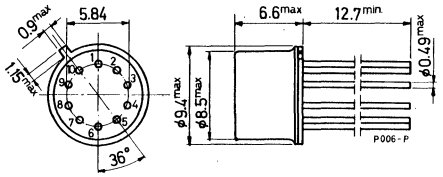




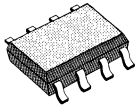
PACKAGES

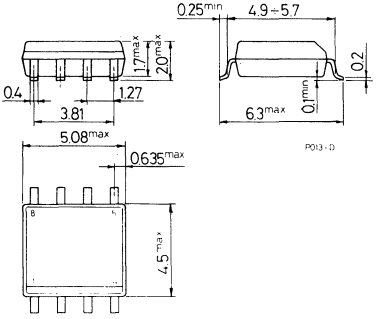
TO-100



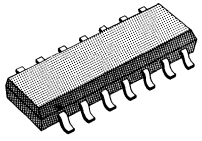


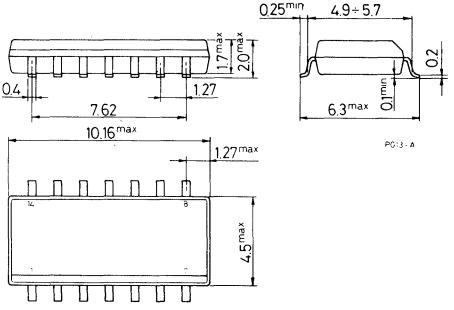
SO-8



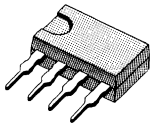


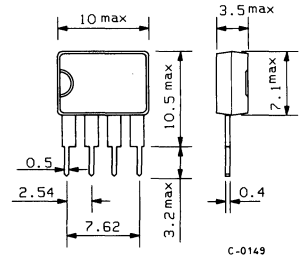
SO-14



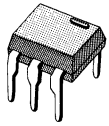


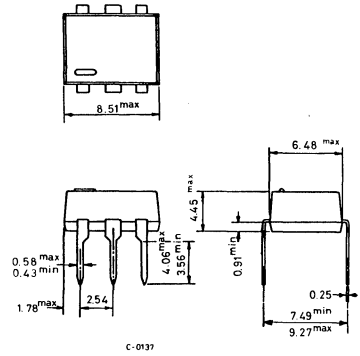
SIP-4



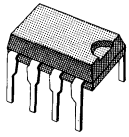


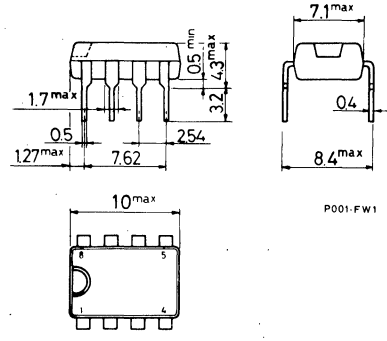
DIP-6





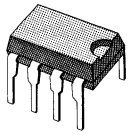
Minidip Plastic

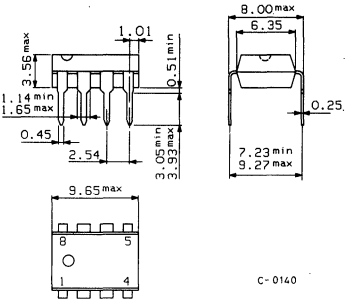




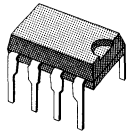
PACKAGES

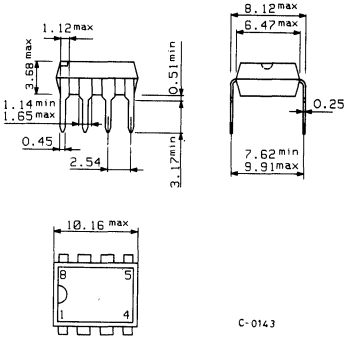
Minidip A Plastic



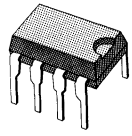


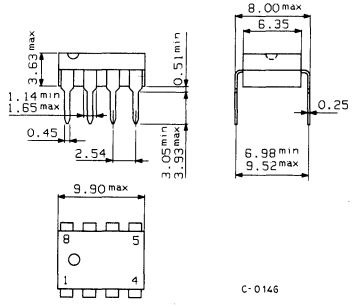
Minidip B Plastic



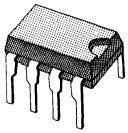


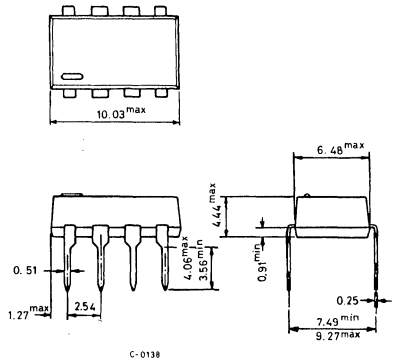
Minidip C Plastic



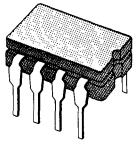


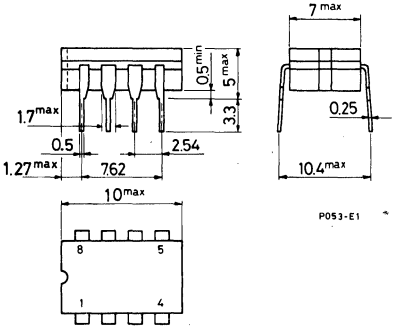
Minidip D Plastic



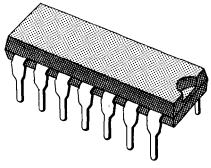


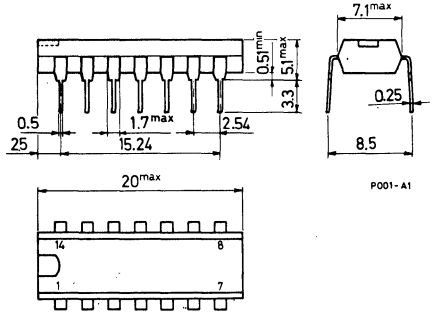
Minidip Ceramic





DIP-14 Plastic (0.25)





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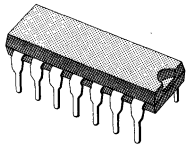
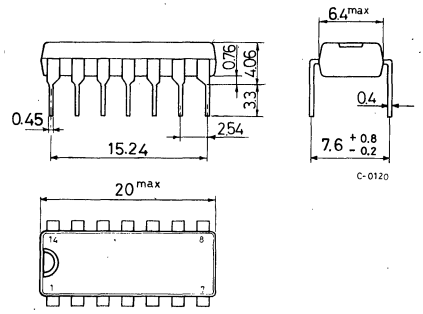
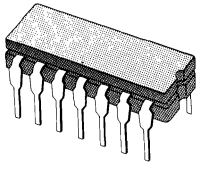
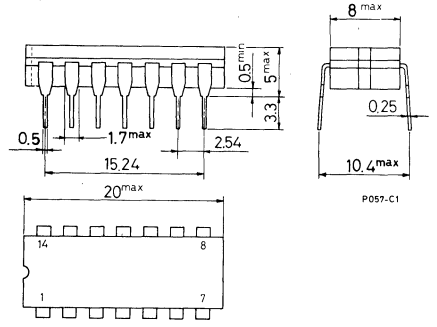
DIP-14 Plastic (0.4)



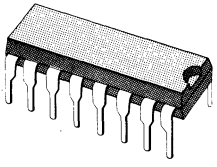


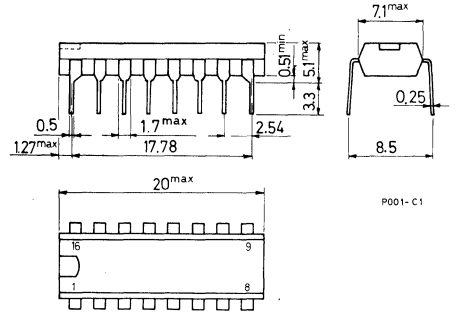
DIP-14 Ceramic (0.25)



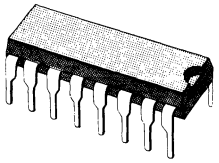


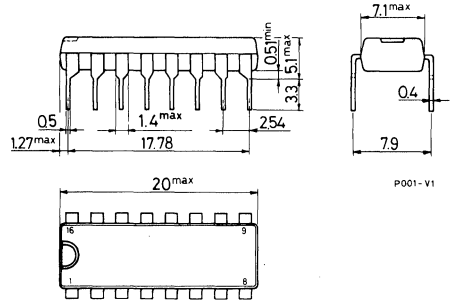
DIP-16 Plastic (0.25)



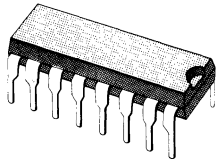


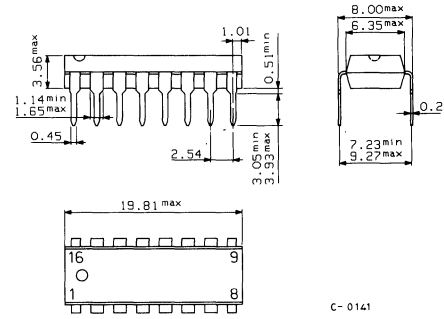
DIP-16 Plastic (0.4)



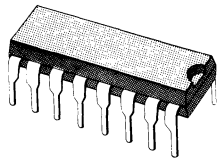


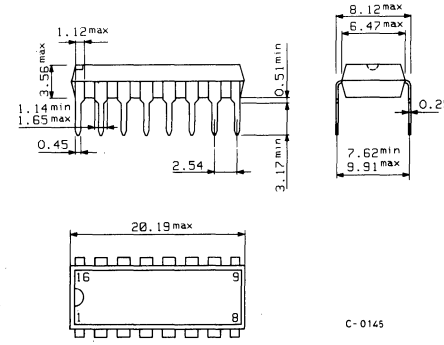
DIP-16 A Plastic





DIP-16 B Plastic





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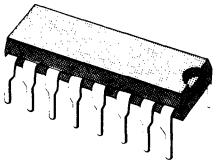
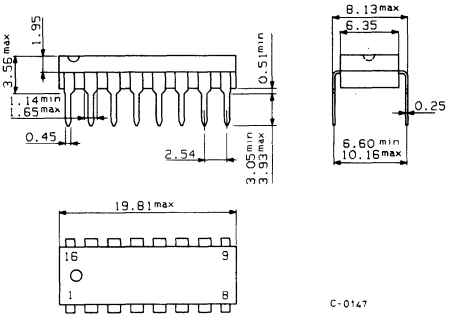
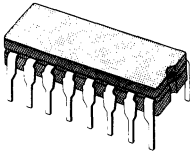
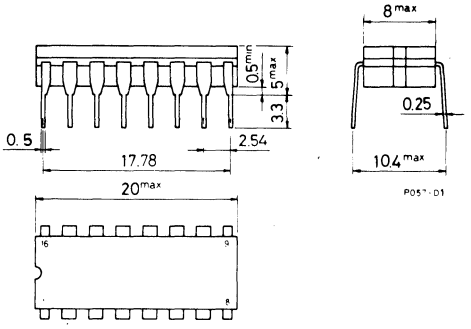
DIP-16 C Plastic



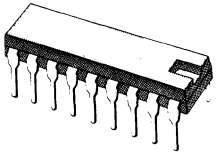


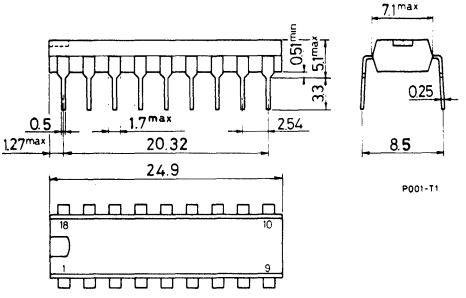
DIP-16 Ceramic (0.25)



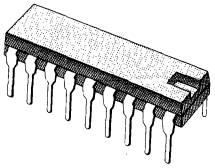


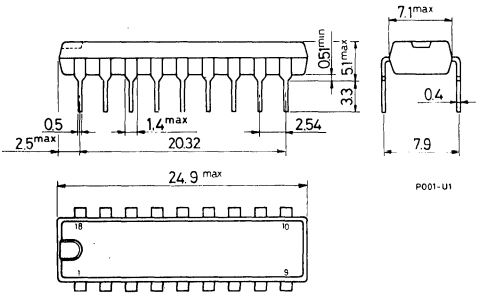
DIP-18 Plastic (0.25)



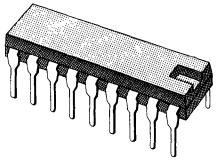


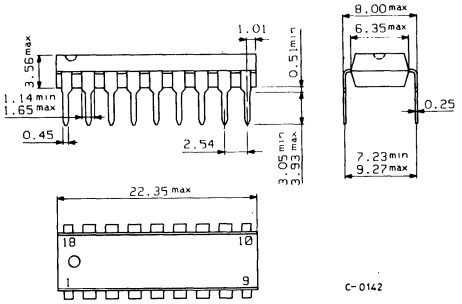
DIP-18 Plastic (0.4)



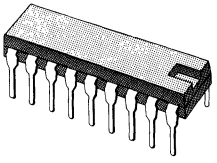


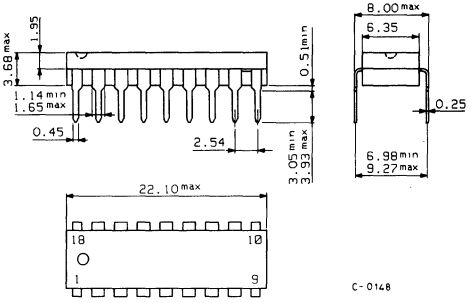
DIP-18 A Plastic





DIP-18 C Plastic





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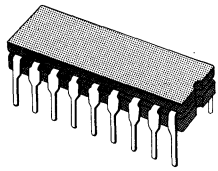
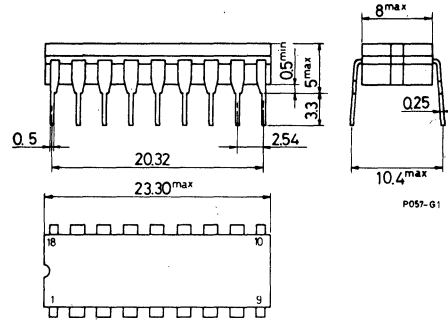
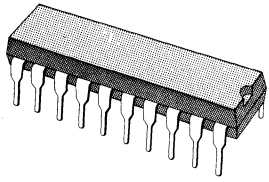
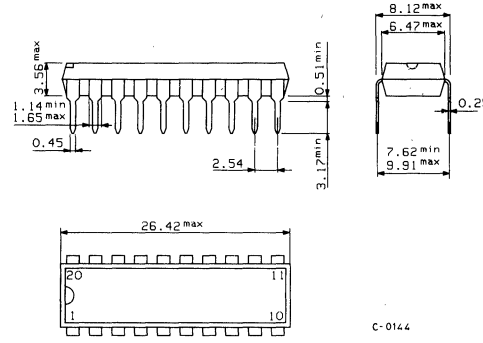
DIP-18 Ceramic (0.25)



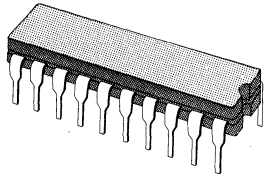


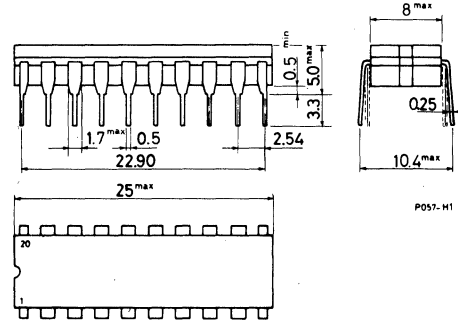
DIP-20 B Plastic



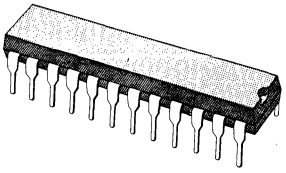


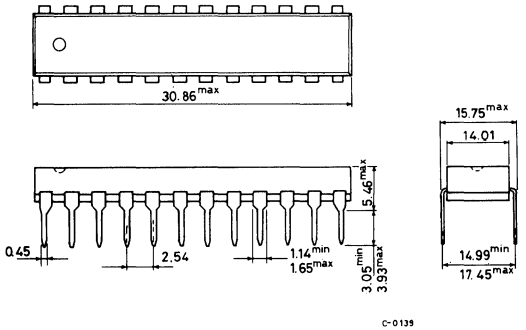
DIP-20 Ceramic (0.25)



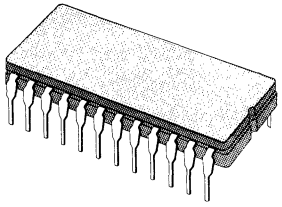


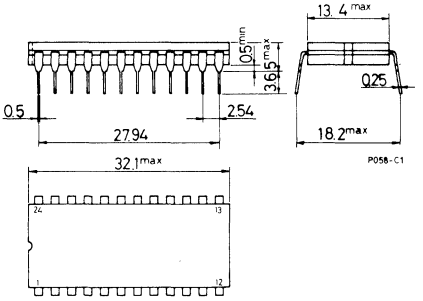
DIP-24 C Plastic



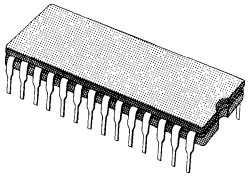


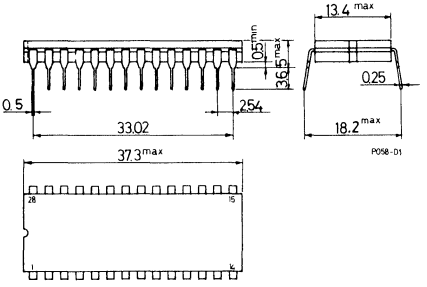
DIP-24 Ceramic (0.25)





DIP-28 Ceramic (0.25)





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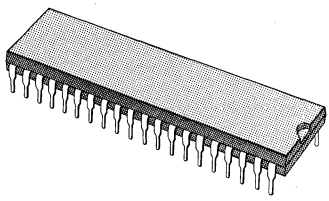
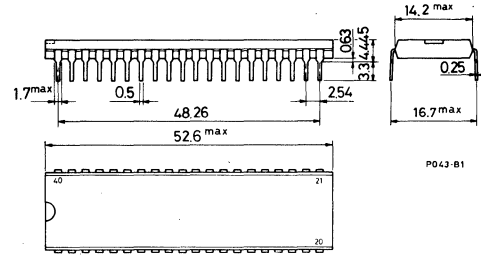
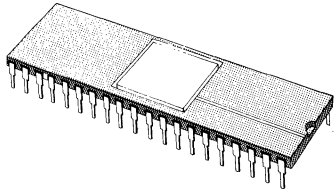
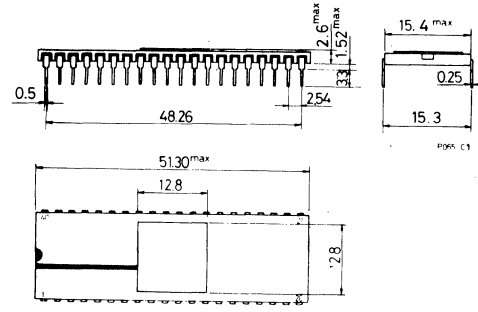
DIP-40 Plastic (0.25)



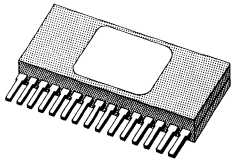


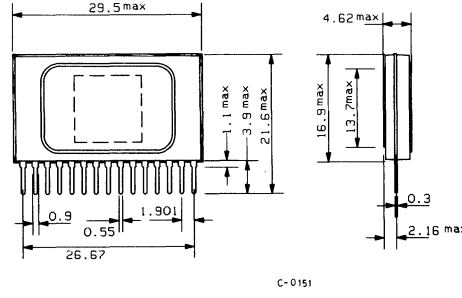
DIP-40 Ceramic (0.25) Side Brazed





SILWATT (In Development)





NOTES

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Fotocomposizione - Servoffset - Milano

Technology and Service

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