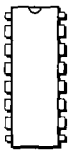
FEATURES

- ☐ Two Clock Generators
- ☐ Eight pre-programmed pin selected pixel clock frequencies
- ☐ One pre-programmed memory clock frequency
- ☐ Programmable pixel clock and memory clock frequencies
- ☐ Power-Down modes for notebook computers
- ☐ On-chip loop filters
- ☐ Maximum frequency–100 MHz
- ☐ Low power CMOS technology
- ☐ IBM VGA Compatible – No additional logic required

16-PIN DIP PACKAGE



SC11412CN

16-PIN SOIC PACKAGE

SC11412CM

GENERAL DESCRIPTION

The SC11412 contains two digitally controlled clock generators capable of generating two independent clock frequencies. The two clock generator outputs may be used to drive the pixel (video dot) clock and memory clock inputs of a typical VGA controller chip. A single crystal or an externally generated system bus clock (14.318MHz) may be used as the input reference frequency.

On power-on reset, the two clock generators default to pre-programmed clock frequencies. The default frequency for Clock Generator No.1 (Pixel Clock) will be one of eight pre-programmed frequencies determined by the configuration of the frequency select pins FS[2:0]. Clock Generator No. 2 (Memory Clock) defaults to a single pre-programmed frequency of 32MHz. In addition to the pre-programmed frequencies, each clock generator can be programmed by the VGA controller, using the serial programming interface, to generate any desired frequency within the VCO frequency range.

Serial programming of the SC11412 by a VGA controller can be accomplished using the VGA controller's three clock select output signals with minimal modification of the Video BIOS routines. Sierra Semiconductor will provide information, including sample routines, to support the modification of the BIOS for programming user defined pixel and memory clock frequencies.

The SC11412 is designed using advanced epi based, double poly, low power CMOS technology. The SC11412 offers a cost effective solution for generating a wide range of pixel and memory clock frequencies. The frequency outputs are compatible with Super VGA, VGA, EGA, MCGA, CGA, MDA and higher frequency applications.

BLOCK DIAGRAM

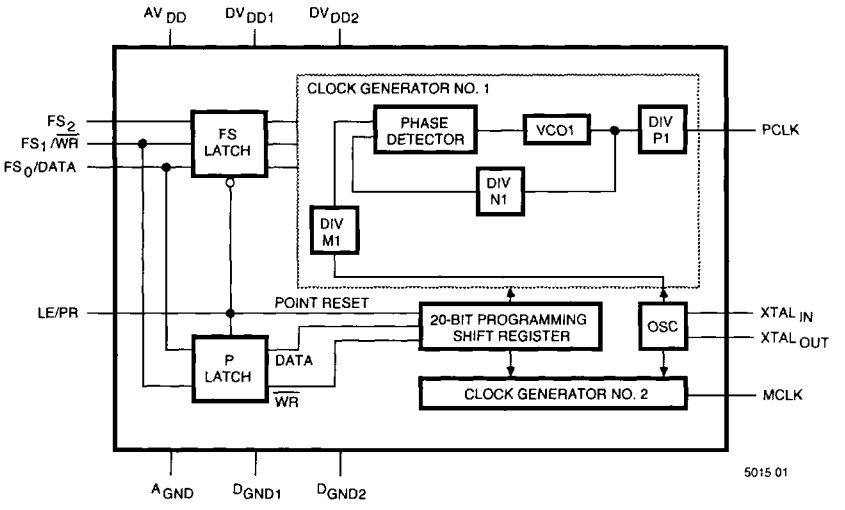
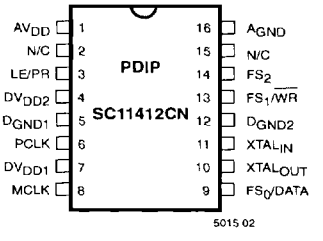


Figure 1.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
A_{GND}	16	Analog ground.
AV_{DD}	1	Analog +5V supply.
D_{GND1}	5	Digital ground for Clock Generator No.1.
D_{GND2}	12	Digital ground for Clock Generator No.2.
DV_{DD1}	7	Digital +5V supply for Clock Generator No.1.
DV_{DD2}	4	Digital +5V supply for Clock Generator No.2.
FS_0/DATA	9	Frequency Select/Data input (TTL compatible). This is a dual purpose pin. When LE/PR is a logic zero, the pin is the FS0 input for Clock Generator No. 1. When LE/PR is a logic one, the pin is the DATA input to the serial programming shift register. Data is shifted into the serial programming shift register on the rising edge of the $\overline{WR}$ signal.
$FS_1/\overline{WR}$	13	Frequency Select/$\overline{WR}$ input (TTL compatible). This is a dual purpose pin. When LE/PR is a logic zero, the pin is the FS1 input for Clock Generator No. 1. When LE/PR is a logic one, the pin is the $\overline{WR}$ input. The rising edge of $\overline{WR}$ is used to shift DATA into the serial programming shift register.
FS_2	14	Frequency Select input (TTL compatible). This pin is the third frequency select input for Clock Generator No. 1.
LE/PR	3	Latch Enable/Pointer Reset (TTL compatible). This is a multi-purpose pin that controls the Frequency Select (FS) and Programming (P) latches as well as the Pointer Reset of the serial programming shift register. When LE/PR is a logic zero, the FS latch is transparent and the P latch is closed. This allows the frequency select inputs FS[2:0] to select one of Clock Generator No.1's eight pre-programmed pixel clock frequencies. When LE/PR is a logic one, the FS latch is closed and the P latch is transparent. This allows the FS0/DATA and FS1/$\overline{WR}$ pins to be used for loading new frequencies into the SC11412. The LE/PR pin is also used to initialize the serial programming pointer (Pointer Reset). Any write operation to the 20-bit serial programming shift register should be preceded by a Pointer Reset. A LOW-to-HIGH transition on the LE/PR pin causes the pointer to be reset to zero.
MCLK	8	Memory Clock output. VCO output of Clock Generator No. 2.
N/C	2, 15	Not connected. These pins should be left unconnected (floating).
PCLK	6	Pixel Clock output. VCO output of Clock Generator No.1.
$XTAL_{IN}$	11	Crystal oscillator input (AC coupled TTL, or a CMOS level signal can be applied). The signal applied to this pin serves as the input reference frequency to the two clock generators. A single crystal or an externally generated system bus clock (14.318 MHz) may be used.
$XTAL_{OUT}$	10	Crystal oscillator output. If a crystal oscillator is used this output should be connected to the crystal through a series damping resistor.

CONNECTION DIAGRAMS



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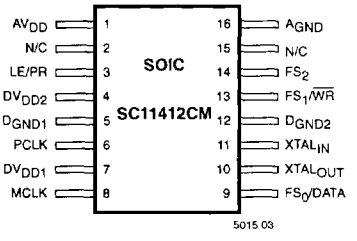

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FUNCTIONAL DESCRIPTION

The SC11412 consists of a crystal oscillator, a serial interface unit and two clock generator blocks (see Figure 1). The two clock generators share a common input reference frequency. Each clock generator block contains two programmable 7-bit dividers and a phase-locked loop circuit.

The output clock frequency is determined by the following equation:

PCLK = (Ni/(Mi*Pi)) * Fosc
and
MCLK = (Ni/(Mi*Pi)) * Fosc

where Mi, Ni, and Pi are the divider values for Clock Generator i, (i=1 for PCLK and i=2 for MCLK) and Fosc = Input Reference Frequency (at $XTAL_{IN}$)

Pi = 1, 2, 4, 8
Mi = 1 to 127
Ni = 1 to 127

NOTE: For Mi and Ni divide ratios of 0 and 1 are divide by 1.

The on-chip loop filters optimize each clock generator for their specified frequency range and eliminate the need for external loop filter components. The on-chip loop filters also increase noise immunity and simplify board layout.

Clock Generator No. 1 is optimized for generating PCLK (pixel clock) frequencies in the range of 45 to 100 MHz. The post scaler divider must be used if an output frequency below 45 MHz is required.

Clock Generator No. 2 is optimized for generating MCLK (memory clock) output frequencies in the range of 32 to 70 MHz. The post scaler divider must be used if any output frequency below 32 MHz is required.

Frequency Selection

The SC11412 supports two frequency program modes: the internal frequency selection mode and the external frequency program mode. In the internal frequency selection mode, the clock generator generates a frequency using pre-programmed M, N, and P values from the SC11412's mask ROM. Clock Generator No. 1 generates one of eight pre-programmed frequencies. This frequency is controlled by the state of frequency select inputs FS[2:0]. Clock Generator No.2 generates a single pre-programmed frequency. The default frequencies for the two clock generators are given in Table 1 assuming a 14.31818 MHz reference input frequency. The set of default frequencies can be altered by a single metal mask option.

In the external frequency program mode, the two clock generators can be programmed independently through the serial programming interface to generate any desired frequency within the VCO range. The external frequency mode is enabled by setting the VCO1 or VCO2 mode control bit (DS3) to a logic zero. Clock Generator No.1's external frequency program mode is selected by setting $FS_0 = FS_2 = 0$, $FS_1 = 1$ and $LE/\overline{PR} = 1$. Other combinations of the frequency select inputs FS[2:0] will select from the seven pre-programmed frequencies shown in Table 1. The pre-programmed frequency for $FS_0 = FS_2 = 0$, $FS_1 = 1$ on Clock Generator No.1 is not available in the external frequency program mode ($LE/\overline{PR} = 1$). In external frequency program mode the user programmed frequency for Clock Generator No.2 is always selected.

A power on reset causes both clock generators to default to the internal frequency selection mode. To ensure that Clock Generator No. 1 is initialized to the desired default frequency, LE/PR should be held at a logic zero during power on reset so that the FS latch is transparent.

Power Down Modes

The SC11412 has two power down modes for each clock generator. Each clock generator has the ability to tristate its output and power down its VCO. These features are controlled by bits DS0–DS3 of the serial programming shift register (see Table 2). Power savings are dependent on the operating frequency and the output load. The power dissipation can be estimated using the following formula:

$P = C \times V^2 \times F$, where:

P is the power in watts
V is the operating voltage in watts
F is the output frequency in Hz

Serial Programming Interface

The serial programming interface allows the user to program the pixel and memory clock frequencies and to select the clock generator and VCO modes. The serial programming interface consists of a 20-bit serial shift register DS[19:0], and the control signals $FS_1/\overline{WR}$, FS_0/DATA, and LE/PR.

Each clock generator can be programmed to generate a desired fre-

FS_2	FS_1	FS_0	Clock Generator No.1 PCLK (MHz)	Clock Generator No. 2 MCLK (MHz)
0	0	0	25.175	32.000
0	0	1	28.321	32.000
0	1	0	40.000	32.000
0	1	1	65.000	32.000
1	0	0	50.000	32.000
1	0	1	44.900	32.000
1	1	0	56.000	32.000
1	1	1	80.000	32.000

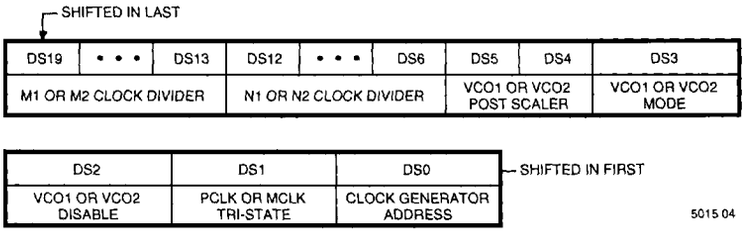
Table 1. Default Clock Generator Frequencies

quency within the VCO's frequency range. The frequency range for VCO 1 is 45 to 100 MHz. The range for VCO2 is 32 to 70 MHz.

A write to the serial programming shift register should be preceded by a pointer reset. The pointer is reset to zero on the rising edge of the LE/PR signal; then one bit of DATA is shifted into the register on every rising edge of $\overline{WR}$ pulse. After the 20-bits are shifted into the serial programming shift register, the data is automatically loaded into the clock generator selected by clock generator address bit (DS0). The pointer is then automatically reset to zero so that the other clock generator may be programmed if necessary.

The 20-bits of the Serial Programming Shift Register are defined as follows:

SERIAL PROGRAMMING SHIFT REGISTER



NAME	DESCRIPTION
DS_0	Clock Generator Address bit. $DS_0 = 1$ Clock Generator 1 is selected for programming. $DS_0 = 0$ Clock Generator 2 is selected for programming.
DS_1	PCLK or MCLK Tri-state bit. $DS_1 = 1$ Tri-states the PCLK or MCLK output driver for the selected clock generator. $DS_1 = 0$ Enables the PCLK or MCLK output driver for the selected clock generator. At power on reset both the clock output drivers are enabled.
DS_2	VCO1 or VCO2 Disable bit. $DS_2 = 1$ Disables the VCO for the selected clock generator. $DS_2 = 0$ Enables the VCO for the selected clock generator. At power on reset, both VCOs are enabled. When the VCO is disabled and DS1 = 0, the clock output is HIGH.
DS_3	VCO1 or VCO2 Mode bit. $DS_3 = 1$ Enables internal frequency selection mode for the selected clock generator. $DS_3 = 0$ Enables external frequency program mode for the selected clock generator. For VCO1, external mode is selected only if $DS_3 = 0$ and $FS_0 = 0$, $FS_1 = 1$, $FS_2 = 0$. For VCO2, the values of FS_0, FS_1 and FS_2 do not affect the mode selection. At power on reset, the internal frequency selection mode is selected for both clock generators.
DS_5–DS_4	VCO1 or VCO2 output auxiliary divider (P). Divides the VCO output of the selected clock generator.
DS_{12}–DS_6	VCO1 or VCO2 clock divider control word (N).
DS_{13}–DS_{19}	Clock Generator No.1 or Clock Generator No.2 reference clock divider control word (M).

DS5	DS4	PCLK	or	MCLK
0	0	VCO_{OUT1}	or	VCO_{OUT2}
0	1	$VCO_{OUT1}/2$	or	$VCO_{OUT2}/2$
1	0	$VCO_{OUT1}/4$	or	$VCO_{OUT2}/4$
1	1	$VCO_{OUT1}/8$	or	$VCO_{OUT2}/8$

Table 2.

INTERFACING THE SC11412 TO VGA CONTROLLERS

The SC11412 is designed to easily interface with standard (IBM compatible) VGA controllers without additional logic components. The interface allows users to program the chip to any desired frequency while maintaining full compatibility with the IBM VGA standard.

The interface to the VGA controller uses the FS_0/DATA, $FS_1/\overline{WR}$, FS_2, and LE/PR pins of the SC11412 and the three clock select pins of the VGA controller (eg. CS[2:0]). If other user programmable outputs (eg. UPOUT) are available from the VGA controller, they may be used to program the SC11412. Figures 2–4 illustrate three possible ways of configuring the SC11412 with a VGA controller.

Configuration 1: In this configuration (Figure 2), LE/PR is tied to a logic zero, and the FS_0/DATA, $FS_1/\overline{WR}$, FS_2 pins are tied to the VGA controller's three clock select pins, CS0, CS1, and CS2. There are nine pre-programmed frequencies available in this configuration, eight for the pixel clock and one for the memory clock.

Configuration 2: Configuration 2 (Figure 3) can access five pre-programmed frequencies and two user-programmable frequencies. In this configuration, FS_2 is tied to a logic zero, and FS_0/DATA, $FS_1/\overline{WR}$, LE/PR pins are tied to the VGA controller clock select pins, CS0, CS1, and CS2. Five pre-programmed frequencies (four for pixel clock and one for memory clock) and two user-programmable frequencies (one for pixel clock and one for memory clock) are available in this configuration.

Configuration 3: This configuration (Figure 4) is applicable only if an additional programmable output pin (eg. UPOUT) is available from the VGA controller. In this configuration, LE/PR is tied to UPOUT, and the FS_0/DATA, $FS_1/\overline{WR}$, FS_2 pins are tied to the VGA controller clock select pins, CS0, CS1, and CS2. Nine pre-programmed frequencies (eight for pixel clock and one for memory clock) and two user-programmable frequencies (one for pixel clock and one for memory clock) are available in this configuration.

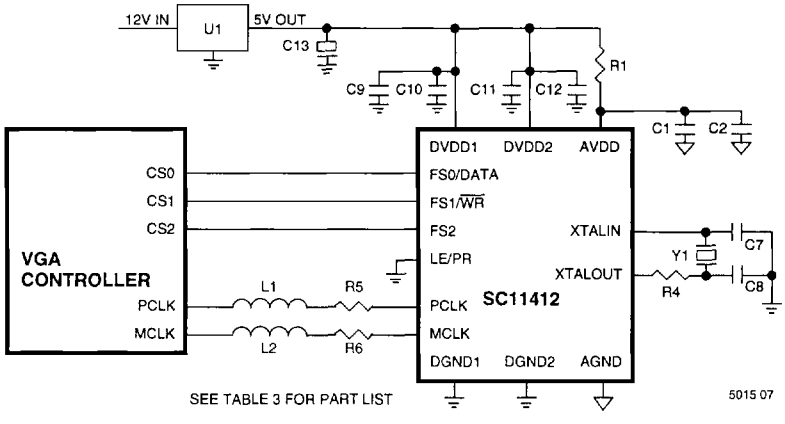


Figure 2. Application Diagram for 9 Pre-Programmed Pixel & Memory Clock Frequencies

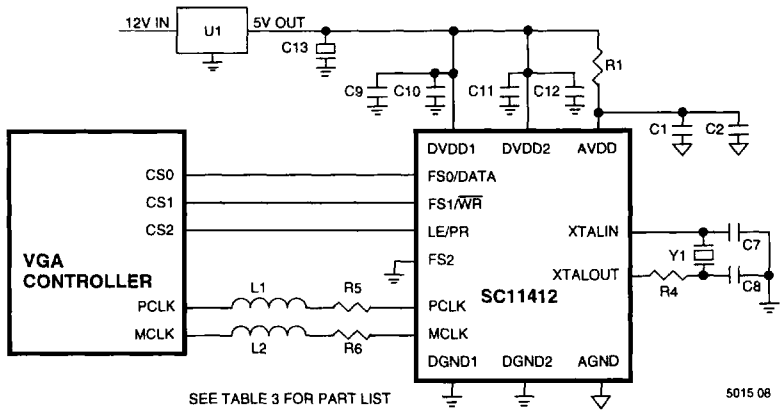


Figure 3. Application Diagram for 5 Pre-Programmed and Two User-Programmable Pixel & Memory Clock Frequencies

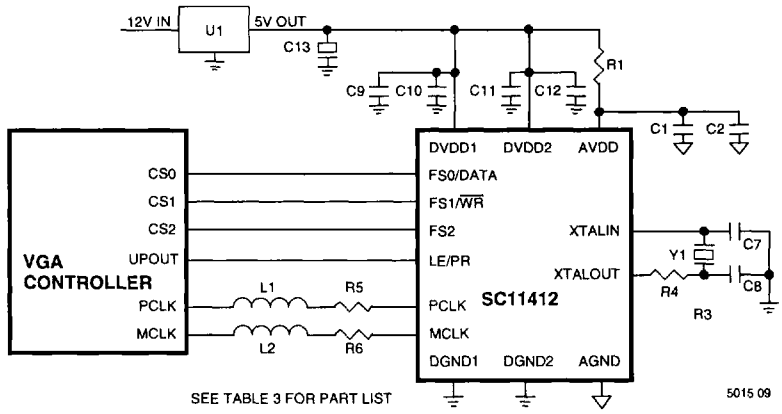


Figure 4. Application Diagram for 9 Pre-Programmmed and Two User-Programmable Pixel & Memory Clock Frequencies

C1, C9, C11	.1µF
C2, C10, C12	.01µF
C7	32pF
C8	32pF
C13	10µF
R1	22Ω
R4	500Ω
R5	47Ω (optional)
R6	47Ω (optional)
L1	Ferrite Bead (optional)
L2	Ferrite Bead (optional)
Y1	14.318MHz series crystal
U1	Voltage Regulator (e.g. 78L05)

Table 3. Part List for Figures 2–4

ABSOLUTE MAXIMUM RATINGS (NOTES 1-3)

Supply Voltage, AV_{DD}, DV_{DD}	6 V
DC Input Voltage	GND - 0.5 to V_{CC} + 0.5 V
Storage Temperature Range	-65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency			14.318	30	MHz
T_R, T_F	Input Rise or Fall Time				50	ns

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Unless otherwise specified, all voltages are referenced to ground.

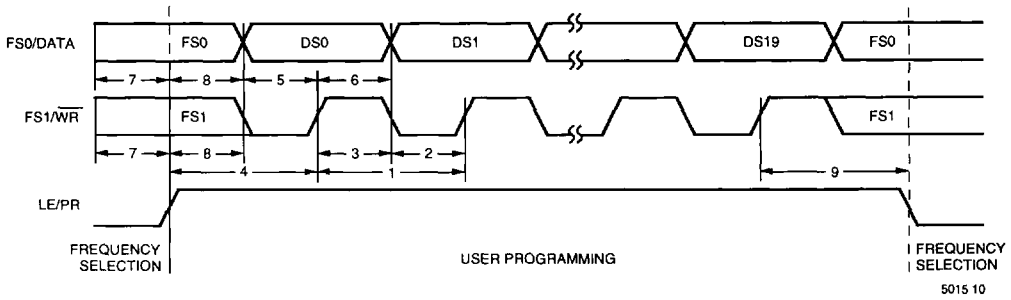
NOTE 3: Power dissipation temperature derating—Plastic package: -12 mW/C from 65°C to 85°C.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ± 10%)

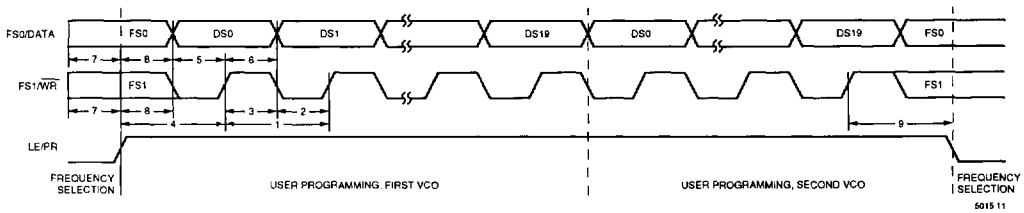
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	AV_{DD} & DV_{DD} Quiescent Current	Normal		50		mA
		VCO1 and VCO2 Powered Down		6		mA
V_{IH}	High Level Input Voltage, All Inputs		2.4			V
V_{IL}	Low Level Input Voltage, All Inputs				0.8	V
V_{OH}	High Level Output, All Outputs Except XTL_{OUT} (I_{OH} = 0.5 mA) (I_{OH} = 100 µA)		 2.4 4.5		 	 V V
V_{OL}	Low Level Output, All Outputs Except XTL_{OUT} (I_{OL} = 1.6 mA) (I_{OL} = 100 µA)				 0.6 0.2	 V V
V_{OH}	High Level Output XTL_{OUT} (I_{OH} = 20 µA)		 4		 	 V
V_{OL}	Low Level Output XTL_{OUT} (I_{OL} = 20 µA)				 0.2	 V

3

SERIAL INTERFACE PROGRAMMING SEQUENCE AND TIMING



Timing for Programming One Clock Generator



Timing for Programming Two Clock Generators

NO.	SYMBOL	PARAMETER	MIN	MAX	UNIT
1	t_{WC}	Write Cycle Time	100		ns
2	t_{WP}	Write Pulse Width	50		ns
3	t_{WR}	Write Recovery Time	50		ns
4	t_{PS}	Point-Reset SetupTime to Rising Edge of $\overline{WR}$	50		ns
5	t_{DS}	DATA Setup Time to Rising Edge of $\overline{WR}$	20		ns
6	t_{DH}	DATA Hold Time from Rising Edge of $\overline{WR}$	20		ns
7	t_{DSL}	FS_0, FS_1 Setup time to Rising Edge of LE/PR	30		ns
8	t_{DHL}	FS_0, FS_1 Hold Time from Rising Edge of LE/PR	20		ns
9	t_{PH}	LE/PR Hold Time from Rising Edge of $\overline{WR}$	50		ns