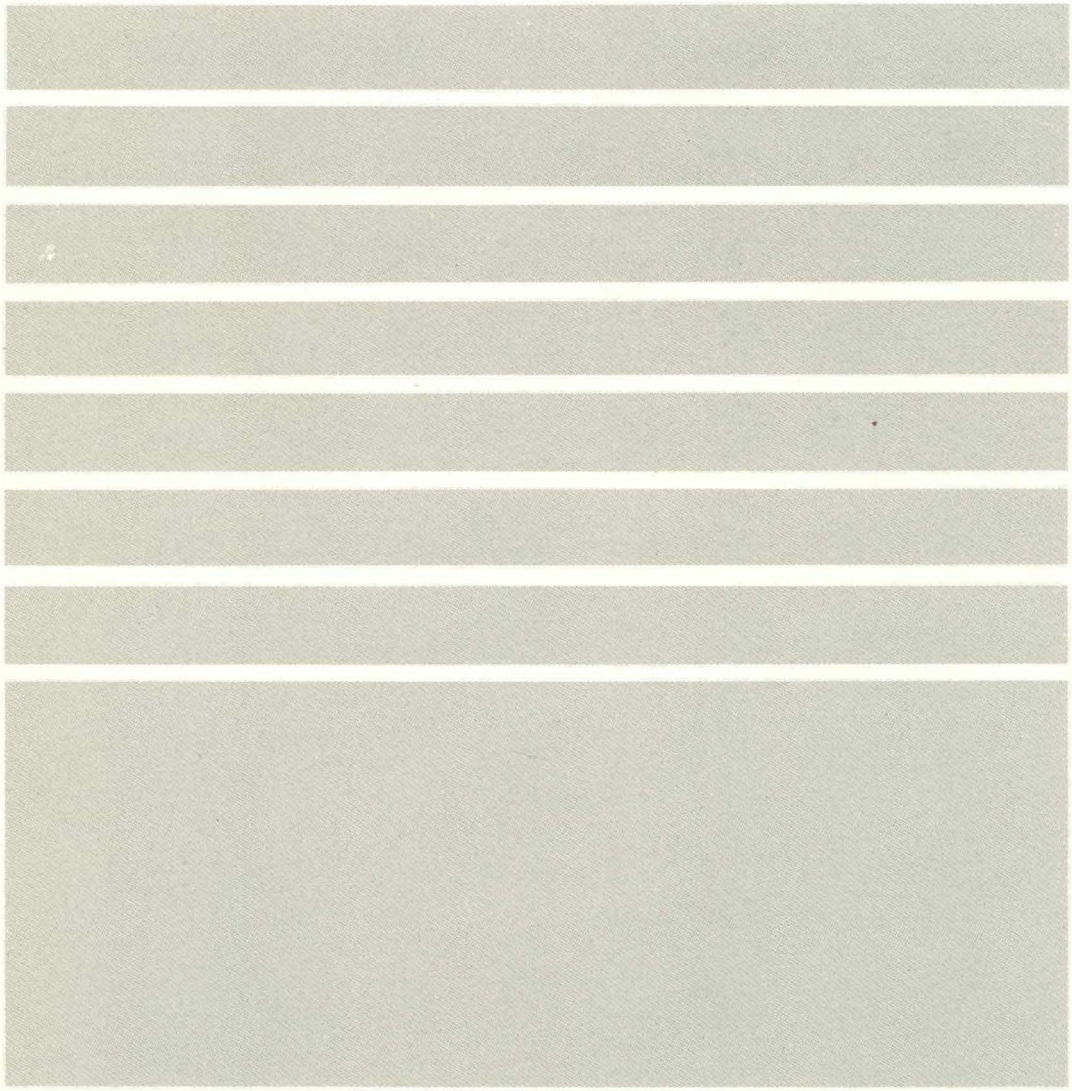
Signetics

Linear Data Manual Volume 3: Video



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Linear Data Manual Volume 3 Video

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Linear Products

1987 Linear Data Manual Volume 3: Video

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Preface

Linear Products

The Linear Division, one of four Signetics product divisions, is a major supplier of a broad line of linear integrated circuits ranging from high performance application specific designs to many of the more popular industry standard devices.

A fifth Signetics division, the Military Division, provides military-grade integrated circuits, including Linear. Please consult the Signetics Military data book for information on such devices.

Employing Signetics' high quality processing and screening standards, the Linear Division is dedicated to providing high-quality linear products to our customers worldwide.

The three 1987 Linear Data and Applications Manuals provide extensive technical data and application information for a broad range of products serving the needs of a wide variety of markets.

Volume 1 — Communications:
Contains data and application information concerning our radio and audio circuits, compandors, phase-locked loops, compact disc circuits, and ICs for RF communication, telephony and modem applications.

Volume 2 — Industrial:
Contains data and application information concerning our data conversion products (analog-to-digital and digital-to-analog), sample-and-hold circuits, comparators, driver/receiver ICs, amplifiers, position measurement devices, power conversion and control ICs and music/speech synthesizers.

Volume 3 — Video:
Contains data and application information concerning our video products. This includes tuning, video IF and audio IF circuits, sync processors/generators, color decoders and encoders, video processing ICs, vertical deflection circuits, Videotex and Teletext ICs and power supply controllers for video applications.

Each volume contains extensive product-specific application information. In addition there are selector guides and product-specific symbols and definitions to facilitate the selection and understanding of Linear products. A functional Table of Contents for each of the three volumes and a complete product and application note listing is also included.

Although every effort has been made to ensure the accuracy of information in these manuals, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in future editions are welcome.

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Signetics

Linear Products

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Signetics

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Cross Reference Guide

Pin-for-Pin Functionally-Compatible*
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Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
AMD	AM6012DC	AM6012F	0 to +70	Ceramic
	DAC-08AQ	DAC-08AF	−55 to +125	Ceramic
	DAC-08CN	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08EN	DAC-08EN	0 to +70	Plastic
	DAC-08EQ	DAC-08EF	0 to +70	Ceramic
	DAC-08HN	DAC-08HN	0 to +70	Plastic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	−55 to +125	Ceramic
	LF198H	LF198H	−55 to +125	Metal Can
	LF198H	SE5537H	−55 to +125	Metal Can
	LF398H	LF398H	0 to +70	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398L	LF398D	0 to +70	SO
	LF398L	NE5537D	0 to +70	SO
	LF398N	LF398N	0 to +70	Plastic
	LF398N	NE5537N	0 to +70	Plastic
Datel	AM-453-2	NE5534/AF	0 to +70	Ceramic
	AM-453-2C	NE5534/AF	0 to +70	Ceramic
	AM-453-2M	SE5534/AF	−55 to +125	Ceramic
	DAC-UP10BC	NE5020N	0 to +70	Plastic
	DAC-UP8BC	NE5018N	0 to +70	Plastic
	DAC-UP8BM	SE5019F	−55 to +125	Ceramic
	DAC-UP8BQ	SE5018F	−55 to 125	Ceramic
Exar	XR-5532/A N	NE5532/AF	0 to +70	Ceramic
	XR-5532/A P	NE5532/AN	0 to +70	Plastic
	XR-L567CN	NE567F	0 to +70	Ceramic
	XR-L567CP	NE567N	0 to +70	Plastic
	XR-5534/A CN	NE5534/AF	0 to +70	Ceramic
	XR-5534/A CP	NE5534/AN	0 to +70	Plastic
	XR-5534/A M	SE5534/AF	−55 to +125	Ceramic
	XR-558CN	NE558F	0 to +70	Ceramic
	XR-558CP	NE558N	0 to +70	Plastic
	XR-558M	SE558F	−55 to +125	Ceramic
	XR-1524N	SG3524F	0 to +70	Ceramic
	XR-1524P	SG3524N	0 to +70	Plastic
	XR-2524P	SG3524N	0 to +70	Plastic
	XR-3524N	SG3524F	0 to +70	Ceramic
	XR-3524P	SG3524N	0 to +70	Plastic
Fairchild	μA080/DA	DAC-08F	0 to +70	Ceramic
	μA0801CDC	MC1408F	0 to +70	Ceramic
	μA0801CPC	MC1408N	0 to +70	Plastic
	μA0801EDC	DAC-08EF	0 to +70	Ceramic
	μA0801EPC	DAC-08AF	0 to +70	Ceramic
	μA1458TC	MC1458N	0 to +70	Plastic
	μA1488DC	MC1488F	0 to +70	Ceramic
	μA1488PC	MC1488N	0 to +70	Plastic
	μA1489/A PC	MC1489/AF	0 to +70	Ceramic
	μA1489/A PC	MC1489/AN	0 to +70	Plastic
	μA198HM	NE5537H	0 to +70	Metal Can
	μA198RM	NE5537N	0 to +70	Plastic

Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
	μA2901DC	LM2901F	−40 to +85	Ceramic
	μA2901PC	LM2901N	−40 to +85	Plastic
	μA311RC	LM311F	0 to +70	Ceramic
	μA324DC	LM324F	0 to +70	Ceramic
	μA324PC	LM324N	0 to +70	Plastic
	μA3302DC	MC3302F	−40 to +85	Ceramic
	μA3302PC	MC3302N	−40 to +85	Plastic
	μA339/ADC	LM339/AF	0 to +70	Ceramic
	μA339/APC	LM339/AN	0 to +70	Plastic
	μA3403DC	MC3403F	0 to +70	Ceramic
	μA3403PC	MC3403N	0 to +70	Plastic
	μA398HC	SE5537H	−55 to +125	Metal Can
	μA398RC	SE5537N	−55 to +125	Plastic
	μA555TC	NE555N	0 to +70	Plastic
	μA556PC	NE556-1N, NE556N	0 to +70	Plastic
	μA723DC	μA723CF	0 to +70	Ceramic
	μA723DM	μA723F	−55 to +125	Ceramic
	μA723HC	μA723CH	0 to +70	Metal Can
	μA723PC	μA723CN	0 to +70	Plastic
	μA733DC	μA733F	0 to +70	Ceramic
	μA733DM	μA733F	−55 to +125	Ceramic
	μA733PC	μA733N	0 to +70	Plastic
	μA741NM	μA741N	−55 to +125	Plastic
	μA741RC	μA741CF	0 to +70	Ceramic
	μA741TC	μA741CN	0 to +70	Plastic
	μA747DC	μA747CF	0 to +70	Ceramic
	μA747PC	μA747CN	0 to +70	Plastic
	μA9667DC	ULN2003F	0 to +70	Ceramic
	μA9667PC	ULN2003N	0 to +70	Plastic
	μA9668DC	ULN2004F	0 to +70	Ceramic
	μA9668PC	ULN2004N	0 to +70	Plastic
Harris	HA-2539	NE5539	0 to +70	Plastic
	HA-2420-2/8B	SE5060F	−55 to +125	Ceramic
	HA-2425N	NE5060N	0 to +70	Plastic
	HA-2425B	NE5060F	0 to +70	Ceramic
	HA1-5102-2	SE5532/AF	−55 to +125	Ceramic
	HA1-5135-2	SE5534/AF	−55 to +125	Ceramic
	HA1-5135-5	NE5534/AF	0 to +70	Ceramic
	HA3-5102-5	NE5532/AN	0 to +70	Plastic
	HA1-5202-5	NE5532/AF	0 to +70	Ceramic
	HA-5320B	NE5060F	0 to +70	Ceramic
Intersil	ADC0803LCD	ADC0803-1 LCF	−40 to +85	Ceramic
	ADC0804	ADC0804-1 CN	0 to +70	Plastic
	ADC0805	ADC0805-1 LCN	−40 to +85	Plastic
Motorola	DAC-08CD	DAC-08CN	0 to +70	Plastic
	DAC-08CQ	DAC-08CF	0 to +70	Ceramic
	DAC-08ED	DAC-08EN	0 to +70	Plastic
	DAC-08EF	DAC-08EF	0 to +70	Ceramic
	DAC-08HQ	DAC-08HF	0 to +70	Ceramic
	DAC-08Q	DAC-08F	−55 to +125	Ceramic

Cross Reference Guide

Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
	LM2901N	LM2901N	-40 to +85	Plastic
	LM311J-8	LM311F	0 to +70	Ceramic
	LM311N	LM311N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM339/A J	LM339/AF	0 to +70	Ceramic
	LM339/A N	LM339/AN	0 to +70	Plastic
	LM358N	LM358N	0 to +70	Plastic
	LM393A/J	LM393/AF	0 to +70	Ceramic
	LM393A/N	LM393/AN	0 to +70	Plastic
	MC1408L	MC1408F	0 to +70	Ceramic
	MC1408P	MC1408N	0 to +70	Plastic
	MC1488L	MC1488F	0 to +70	Ceramic
	MC1488P	MC1488N	0 to +70	Plastic
	MC1489/A L	MC1489/AF	0 to +70	Ceramic
	MC1489/A P	MC1489/AN	0 to +70	Plastic
	MC1496L	MC1496F	0 to +70	Ceramic
	MC1496P	MC1496N	0 to +70	Plastic
	MC3302L	MC3302F	-40 to +85	Ceramic
	MC3302P	MC3302N	-40 to +85	Plastic
	MC3361D	MC3361D	0 to +70	SO
	MC3361P	MC3361N	0 to +70	Plastic
	MC3403L	MC3403F	0 to +70	Ceramic
	MC3403P	MC3403N	0 to +70	Plastic
	MC3410CL	MC3410CF	0 to +70	Ceramic
	MC3410L	MC3410F	0 to +70	Ceramic
		NE5410F	0 to +70	Ceramic
	MC3510L	SE5410F	0 to +70	Ceramic
	NE592F	NE592F-8	0 to +70	Ceramic
	NE592F	NE592F-14	0 to +70	Ceramic
	NE592N	NE592N	0 to +70	Plastic
	NE565N	NE565N	0 to +70	Plastic
	SE592F	SE592F-8	-55 to +125	Ceramic
	SE592F	SE592F-14	-55 to +125	Ceramic
	SE592H	SE592H	-55 to +125	Metal Can
National	ADC0803F	ADC0803-1 LCF	-40 to +85	Ceramic
	ADC0803N	ADC0803-1 LCN	-40 to +85	Plastic
	ADC0805	ADC0805-1 LCN	-40 to +85	Plastic
	ADC0820BCN	ADC0820BNEN	0 to +70	Plastic
	ADC0820CCN	ADC0820CNEN	0 to +70	Plastic
	ADC0820BCD	ADC0820BSAN	-40 to +85	Plastic
	ADC0820CCD	ADC0820CSAN	-40 to +85	Plastic
	ADC0820BD	ADC0820BSEF	-55 to +125	Ceramic
	ADC0820CD	ADC0820CSEF	-55 to +125	Ceramic
	DAC0800LCJ	DAC-08EF	0 to +70	Ceramic
	DAC0800LJ	DAC-08F	-55 to +125	Ceramic
	DAC0800LCN	DAC-08EN	0 to +70	Plastic
	DAC0801LCJ	DAC-08CF	0 to +70	Ceramic
	DAC0801LCN	DAC-08CN	0 to +70	Plastic
	DAC0802LJ	DAC-08AF	-55 to +125	Ceramic
	DAC0802LCJ	DAC-08HF	0 to +70	Ceramic
	DAC0802LCN	DAC-08HN	0 to +70	Plastic
	DAC0806LCJ	MC1408-6F	0 to +70	Ceramic
	DAC0806LCN	MC1408-6N	0 to +70	Plastic
	DAC0807LCJ	MC1408-7F	0 to +70	Ceramic
	DAC0807LCN	MC1408-7N	0 to +70	Plastic
	DAC0808LCJ	MC1408F	0 to +70	Ceramic

Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
	DAC0808LCN	MC1408N	0 to +70	Plastic
	DAC0808LD	MC1408F	0 to +70	Ceramic
	LF198H	SE5537H	-55 to +125	Metal Can
	LF398H	NE5537H	0 to +70	Metal Can
	LF398N	NE5537N	0 to +70	Plastic
	LM13600AN	NE5517N	0 to +70	Plastic
	LM13600N	NE5517N	0 to +70	Plastic
	LM1458N	MC1458N	0 to +70	Plastic
	LM161H	SE529H	-55 to +125	Metal Can
	LM161J	SE529F	-55 to +125	Ceramic
	LM2524J	SG3524F	0 to +70	Ceramic
	LM2524N	SG3524N	0 to +70	Plastic
	LM2901N	LM2901N	-40 to +85	Plastic
	LM2903N	LM2903N	-40 to +85	Plastic
	LM3089	CA3089N	-55 to +125	Plastic
	LM319J	LM319F	0 to +70	Ceramic
	LM319N	LM319N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM324N	LM324N	0 to +70	Plastic
	LM324AD	LM324AD	0 to +70	Plastic
	LM324AN	LM324AN	0 to +70	Plastic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM3524J	SG3524F	0 to +70	Ceramic
	LM3524N	SG3524N	0 to +70	Plastic
	LM358H	LM358H	0 to +70	Metal Can
	LM358N	LM358N	0 to +70	Plastic
	LM361H	NE529H	0 to +70	Metal Can
	LM361J	NE529D	0 to +70	SO
	LM361N	NE529N	0 to +70	Plastic
	LM393/AN	LM393/AN	0 to +70	Plastic
	LM555J	NE555F	0 to +70	Ceramic
	LM555N	NE555N	0 to +70	Plastic
	LM556J	SE556-1F	-55 to +125	Ceramic
	LM556N	SE556-1N	-55 to +125	Plastic
	LM556CJ	NE556-1F	0 to +70	Ceramic
	LM556CN	NE556-1N	0 to +70	Plastic
	LM565CN	NE565N	0 to +70	Plastic
	LM566N	SE566N	-55 to +125	Plastic
	LM566CN	NE566N	0 to +70	Plastic
	LM567CN	NE567N	0 to +70	Plastic
	LM733CN	μA733CN	0 to +70	Plastic
	LM741CJ	μA741CF	0 to +70	Ceramic
	LM741CN	μA741CN	0 to +70	Plastic
	LM741J	μA741F	-55 to +125	Ceramic
	LM741N	μA741N	-55 to +125	Plastic
	LM747CJ	μA747CF	0 to +70	Ceramic
	LM747CN	μA747CN	0 to +70	Plastic
	LM747J	μ747F	-55 to +125	Ceramic
	LM747N	μA747N	-55 to +125	Plastic
	UC3842D	UC3842D	0 to +70	Plastic
	UC3842J	UC3842FE	0 to +70	Ceramic
	UC3842N	UC3842N	0 to +70	Plastic
	UC2842D	UC2842D	0 to +70	Plastic
	UC2842J	UC2842FE	0 to +70	Ceramic
	UC2842N	UC2842N	0 to +70	Plastic
	UC1842J	UC1842FE	-55 to +125	Ceramic
	UC1842N	UC1842N	-55 to +125	Plastic

Cross Reference Guide

Competitor	Competitor Part Number	Signetics Part Number	Temperature Range (°C)	Package
NEC	μPC1571C	NE571N	0 to +70	Plastic
PMI	CMP-05GP	NE5105N	0 to +70	Plastic
	CMP-05CZ	SE5105F	−55 to +125	Ceramic
	CMP-05BZ	SE5105F	−55 to +125	Ceramic
	CMP-05GZ	SA5105N	−40 to +85	Plastic
	CMP-05FZ	SA5105N	−40 to +85	Plastic
	DAC1408A-6P	MC1408-6N	0 to +70	Plastic
	DAC1408A-6Q	MC1408-6F	0 to +70	Ceramic
	DAC1408A-7N	MC1408-7N	0 to +70	Plastic
	DAC1408A-7Q	MC1408-7F	0 to +70	Ceramic
	DAC1408A-8N	MC1408-8N	0 to +70	Plastic
	DAC1408A-8Q	MC1408-8F	0 to +70	Ceramic
	DAC1508A-8Q	MC1408-8F	−55 to +125	Ceramic
	DAC312FR	AM6012F	0 to +70	Ceramic
	OP27BZ	SE5534AFE	−55 to +125	Ceramic
	OP27CZ	SE5534FE	−55 to +125	Ceramic
	PM747Y	μA747N	−55 to +125	Plastic
	SMP-10AY	SE5060F	−55 to +125	Ceramic
	SMP-10EY	NE5060N	0 to +70	Plastic
	SMP-11AY	SE5060F	−55 to +125	Ceramic
	SMP-11EY	NE5060N	0 to +70	Plastic
Raytheon	RC4805DE	NE5105N	0 to +70	Plastic
	RC4805EDE	NE5105AN	0 to +70	Plastic
	RM4805DE	SE5105F	−55 to +125	Ceramic
	RM4805ADE	SE5105AF	−55 to +125	Ceramic
	RC5532/A DE	NE5532/AF	0 to +70	Ceramic
	RC5532/A NB	NE5532/AN	0 to +70	Plastic
	RC5534/A DE	NE5534/AF	0 to +70	Ceramic
	RC5534/A NB	NE5534/AN	0 to +70	Plastic
	RM5532/A DE	SE5532/AF	−55 to +125	Ceramic
	RM5534/A DE	SE5534/AF	−55 to +125	Ceramic
Silicon General	SG3524J	SG3524F	0 to +70	Ceramic
	SG3526N	SG3526N	0 to +70	Plastic
Sprague	UDN6118A	SA594N	−40 to +85	Plastic
	UDN6118R	SA594F	−40 to +85	Ceramic
	ULN8142M	UC3842N	0 to +70	Plastic
	ULN8160A	NE5560N	0 to +70	Plastic
	ULN8160R	NE5560F	0 to +70	Ceramic
	ULN8161M	NE5561N	0 to +70	Plastic
	ULN8168M	NE5568N	0 to +70	Plastic
	ULN8564A	NE564N	0 to +70	Plastic
	ULN8564R	NE564F	0 to +70	Ceramic
	ULS8564R	SE564F	−55 to +125	Ceramic
TI	ADC0803N	ADC0803-1 LCN	−40 to +85	Plastic
	ADC0804CN	ADC0804-1 CN	0 to +70	Plastic
	ADC0805N	ADC0805-1 LCN	−40 to +85	Plastic
	LM111J	LM111F	−55 to +125	Ceramic
	LM311D	LM311D	0 to +70	Plastic
	LM311J	LM311F	0 to +70	Ceramic
	LM311JG	LM311FE	0 to +70	Ceramic
	LM324D	LM324N	0 to +70	Plastic
	LM324J	LM324F	0 to +70	Ceramic
	LM339/AJ	LM339/AF	0 to +70	Ceramic
	LM339/AN	LM339/AN	0 to +70	Plastic
	LM358P	LM358N	0 to +70	Plastic
	LM393/A P	LM393/AN	0 to +70	Plastic
	MC1458P	MC1458N	0 to +70	Plastic
	NE5532/A JG	NE5532/AF	0 to +70	Ceramic
	NE5532/A P	NE5532/AN	0 to +70	Plastic
	NE5534/A JG	NE5534/AF	0 to +70	Ceramic
	NE5534/A P	NE5534/AN	0 to +70	Plastic
	NE555JG	NE555N	0 to +70	Plastic
	NE555P	NE555N	0 to +70	Plastic
	NE556D	NE556N	0 to +70	Plastic
	NE556J	NE556-1F	0 to +70	Ceramic
	NE556N	NE556-1N	0 to +70	Plastic
	NE592	NE592N14	0 to +70	Plastic
	NE592A	NE592F14	0 to +70	Ceramic
	NE592J	NE592F	0 to +70	Ceramic
	NE592N	NE592N-14	0 to +70	Plastic
	SA556D	SA556N	−40 to +85	Plastic
	SE5534/A JG	SE5534/AF	−55 to +125	Ceramic
	SE555JG	SE555N	−55 to +125	Plastic
	SE556J	SE556-1F	−55 to +125	Ceramic
	SE556N	SE556-1N	−55 to +125	Plastic
	SE592	SE592N14	−55 to +125	Plastic
	SE592J	SE592F-14	−55 to +125	Ceramic
	SE592N	SE592N-14	−55 to +125	Plastic
	SN55107AJ	NE521F	0 to +70	Plastic
	SN55108AJ	SE522F	−55 to +125	Ceramic
	SN75107AJ	NE521F	0 to +70	Plastic
	SN75107AN	NE521N	0 to +70	Plastic
	SN75108AJ	NE522F	0 to +70	Ceramic
	SN75108AN	NE522N	0 to +70	Plastic
	SN75188J	MC1488F	0 to +70	Ceramic
	SN75188N	MC1488N	0 to +70	Plastic
	SN75189AJ	MC1489AF	0 to +70	Ceramic
	SN75189AN	MC1489AN	0 to +70	Plastic
	SN75189J	MC1489F	0 to +70	Ceramic
	SN75189N	MC1489A	0 to +70	Plastic
	TL592A	NE592F14	0 to +70	Ceramic
	TL592P	NE592NB	0 to +70	Plastic
	μA723CJ	μA723CF	0 to +70	Ceramic
	μA723CN	μA723CN	0 to +70	Plastic
	μA723MJ	μA723F	−55 to +125	Ceramic
	μA723MU	μA723D	−55 to +125	SO
Unitrode	UC3524J	SG3524F	0 to +70	Ceramic
	UC3524N	SG3524N	0 to +70	Plastic

*THERE MAY BE PARAMETRIC DIFFERENCES BETWEEN SIGNETICS' PARTS AND THOSE OF THE COMPETITION.

Signetics

SO Availability List

Linear Products

PART NUMBER	SMD PACKAGE	DESCRIPTION
ADC0820D	SOL-20	8-Bit CMOS A/D
*DAC08ED	SO-16	8-Bit D/A Converter
*LF398D	SO-14	Sample-and-Hold Amp
LM1870D	SOL-20	Stereo Demodulator
LM2901D	SO-14	Quad Volt Comparator
LM2903D	SO-8	Dual Volt Comparator
LM311D	SO-8	Voltage Comparator
LM319D	SO-14	High-Speed Dual Comparator
LM324AD	SO-14	Quad Op Amp
LM324D	SO-14	Quad Op Amp
LM339D	SO-14	Quad Volt Comparator
LM358AD	SO-8	Dual Op Amp
LM358D	SO-8	Dual Op Amp
LM393D	SO-8	Dual Comparator
*MC1408-8D	SO-16	8-Bit D/A Converter
MC1458D	SO-8	Dual Op Amp
MC1488D	SO-14	Quad Line Driver
MC1489D	SO-14	Quad Line Receiver
MC1489AD	SO-14	Quad Line Receiver
MC3302D	SO-14	Quad Volt Comparator
MC3361D	SOL-16	Low Power FM IF
MC3403D	SO-14	Quad Low Power Op Amp
NE4558D	SO-8	Dual Op Amp
*NE5018D	SOL-24	8-Bit D/A Converter
*NE5019D	SOL-24	8-Bit D/A Converter
*NE5036D	SO-14	6-Bit A/D Converter
NE5037D	SO-16	6-Bit A/D Converter
NE5044D	SO-16	Prog 7-Channel Encoder
NE5045D	SO-16	7-Channel Decoder
NE5090D	SOL-16	Address Relay Driver
NE5105/AD	SO-8	High-Speed Comparator
NE5170A	PLCC-28	Octal Line Driver
NE5180A	PLCC-28	Octal Line Receiver
NE5204D	SO-8	High-Frequency Amp
NE5205D	SO-8	High-Frequency Amp
NE521D	SO-14	High-Speed Dual Comparator
NE5212D8	SO-8	Transimedance Amplifier
NE522D	SO-14	High-Speed Dual Comparator
NE5230D	SO-8	Low Voltage Op Amp
NE527D	SO-14	High-Speed Comparator
NE529D	SO-14	High-Speed Comparator

PART NUMBER	SMD PACKAGE	DESCRIPTION
NE532D	SO-8	Dual Op Amp
*NE544D	SOL-16	Servo Amp
*NE5512D	SO-8	Dual Hi-Perf Op Amp
*NE5514D	SOL-16	Quad Hi-Perf Op Amp
NE5517D	SO-16	Dual Hi-Perf Amp
NE5520D	SOL-16	LVDT Signal Cond Ckt
*NE5532D	SOL-16	Dual Low-Noise Op Amp
*NE5533D	SOL-16	Low-Noise Op Amp
NE5534AD	SO-8	Low-Noise Op Amp
NE5534D	SO-8	Low-Noise Op Amp
NE5537D	SO-14	Sample-and-Hold Amp
NE5539D	SO-14	Hi-Freq Amp Wideband
NE555D	SO-8	Single Timer
NE556D	SO-14	Dual Timer
NE5560D	SO-16	SMPS Control Ckt
NE5561D	SO-8	SMPS Control Ckt
NE5562D	SOL-20	SMPS Control Ckt
NE5568D	SO-8	SMPS Control Ckt
NE558D	SOL-16	Quad Timer
NE5592D	SO-14	Dual Video Amp
NE564D	SO-16	Hi-Frequency PLL
*NE565D	SO-14	Phase Locked Loop
NE566D	SO-8	Function Generator
NE567D	SO-8	Tone Decoder PLL
NE568D	SOL-20	PLL
NE571D	SOL-16	Compandor
NE572D	SOL-16	Prog Compandor
*NE587D	SOL-20	7 Seq LED Driver (Anode)
*NE589D	SOL-20	7 Seq LED Driver (Cath)
NE5900D	SOL-16	Call Progress Decoder
NE592D14	SO-14	Video Amp
NE592D8	SO-8	Video Amp
NE592HD14	SO-14	Hi-Gain Video Amp
NE592HD8	SO-8	Hi-Gain Video Amp
*NE594D	SOL-20	Vac Fluor Disp Driver
NE602D	SO-8	Double Bal Mixer/ Oscillator
NE604D	SO-16	Low Power FM IF System
NE605	SOL-20	FM IF System
NE612D	SO-8	Double Balanced Mixer/Oscillator
NE614D	SO-16	Low Power FM IF System
*PCD3311TD	SO-16	DTMF/Melody Generator

SO Availability List

PART NUMBER	SMD PACKAGE	DESCRIPTION
PCD3312TD	SO-8	DTMF/Melody Generator With ICC
PCD3315TD	SOL-28	Repertory Pulse Dial
PCD3360TD	SO-16	Progress Tone Ringer
PCF2100TD	SOL-28	LCD Duplex Driver (40)
PCF2111TD	VSO-40	LCD Duplex Driver (64)
PCF2112TD	VSO-40	LCD Duplex Driver (32)
PCF8570TD	SO-8	Static RAM (256 × 8)
PCF8571TD	SO-8	1K Serial RAM
PCF8573TD	SO-16	Clock/Timer
PCF8574TD	SO-16	Remote I/O Expander
PCF8576TD	VSO-56	MUX/Static Driver
PCF8577TD	VSO-40	32-/64-Segment LCD Driver
SA5105/AD	SO-8	High-Speed Comparator
SA5230D	SO-8	Low Voltage Op Amp
SA5212D8	SO-8	Transimpedance Amp
SA532D	SO-8	Dual Op Amp
SA534D	SO-14	Dual Op Amp
SA555D	SO-8	Single Timer
SA571D	SOL-16	Compandor
SA572D	SOL-16	Compandor
*SA594D	SOL-20	Vac Fluor Disp Driver
SA602D	SO-8	Double Bal Mixer/ Oscillator
SA604D	SO-16	Lower Power FM IF System
SAA3004TD	SOL-20	R/C Transmitter
SG3524D	SO-16	SMPS Control Circuit
TDA1001BTD	SO-16	Noise Suppressor
TDA1005ATD	SO-16	Stereo Decoder
TDA3047TD	SO-16	IR Preamp
TDA3048TD	SO-16	IR Preamp
TDA5040TD	SO-8	Brushless DC Motor Driver
TDA7010TD	SO-16	FM Radio Circuit
TDA7050TD	SO-8	Mono/Stereo Amp
TDD1742TD	SOL-28	Frequency Synthesizer
ULN2003D	SO-16	Transistor Array
ULN2004D	SO-16	Transistor Array
μA723CD	SO-14	Voltage Regulator
μA741CD	SO-8	Single Op Amp
μA747CD	SO-14	Dual Op Amp

NOTE:
*Non-standard pinout.

UNDER DEVELOPMENT

PART NUMBER	SMD PACKAGE	DESCRIPTION
26LS31D	SO-16	RS-422 Line Driver
26LS32D	SO-16	RS-422 Line Receiver
26LS33D	SO-16	RS-422 Line Receiver
26LS29D	SO-16	RS-423 Line Driver
26LS30D	SO-16	RS-423 Line Receiver

NOTE:
For information regarding additional SO products released since the publication of this document, contact your local Signetics Sales Office.

Ordering Information for Prefixes ADC, AM, CA, DAC, ICM, LF, LM, MC, NE, OP, SA, SE, SG, μA, UC, ULN

Linear Products

Signetics' Linear integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order
$250 per line item per order

Military Product:

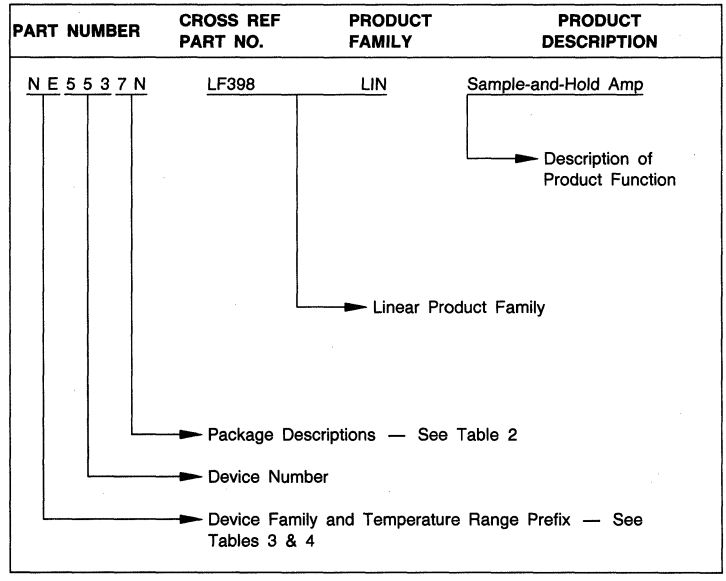
$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that an SE prefix (−55°C to +125°C) indicates only the operating temperature range of a device and *not* its military qualification status. The military qualification status of any Linear product can be determined by either looking in the Military Data Manual and/or contacting your local sales office.

Table 1. Part Number Description



Ordering Information

Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	−55°C to +125°C
SA	−40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
OP	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard
ULN	Linear Industry Standard

Ordering Information for Prefixes HE, OM, MA, ME, PC, PN, SA, TB, TC, TD, TE

Linear Products

Signetics' integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors.

Minimum Factory Order:
Commercial Product:

$ 1000 per order

$ 250 per line item per order

Table 1 provides part number information concerning Signetics/Philips integrated circuits.

Table 2 provides package suffixes and descriptions for all presently existing types. Letters following the device number not used in Table 2 are considered to be part of the device number.

Table 3 provides explanations on the various prefixes employed in the part number descriptions. As noted in Table 3, Signetics/Philips device operating temperature is defined by the appropriate prefix.

OPERATING TEMPERATURE:
The third letter of the prefix, in a three-letter prefix, is the temperature designator.

The letters A to F give information about the operating temperature:

A: Temperature range not specified. See data sheet.
e.g. TDA2541N

B: 0 to +70°C
e.g. PCB8573PN

C: −55°C to +125°C
e.g. PCC2111PN

D: −25°C to +70°C
e.g. PCD8571PN

E: −25°C to +85°C
e.g. PCE2111PN

F: −40°C to +85°C
e.g. PCF2111PN

Table 1. Part Number Description

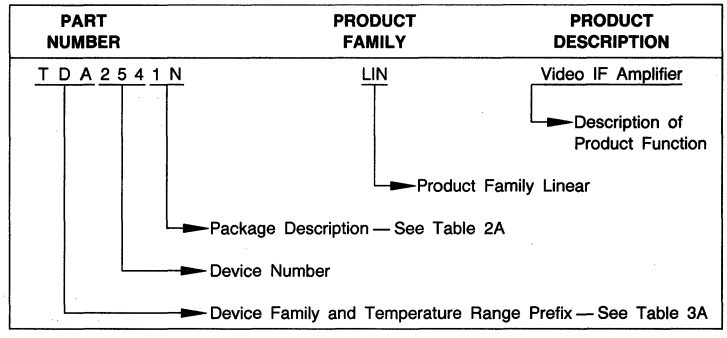


Table 2. Package Description

SUFFIX	PACKAGE DESCRIPTION
PN	8-, 14-, 16-, 18-, 20-, 24-, 28-, 40-lead plastic DIP
TD	Microminiature Package (SO)
DF	14-, 16-, 18-, 22-, 24-lead ceramic DIP
U	Single in-line plastic (SIP) and SIP power packages

Table 3. Device Prefix

PREFIX	DEVICE FAMILY
HEx	CMOS circuit
OM	Linear circuit
MAx	Microcomputer
MEx	Microcomputer peripheral
PCx	CMOS circuit
PNx	NMOS circuit
SAx	Digital circuit
TBx	Linear circuit
TCx	Linear circuit
TDx	Linear circuit
TEx	Linear circuit

Signetics

Linear Products

Section 2
Quality and Reliability

INDEX

"Given the increasingly intense competitive pressures our customers face, they should demand nothing less than zero defects from every IC vendor. We now know that zero defects is an achievable goal. Why should IC customers pay for errors?"

Norman Neumann
President
Signetics Corporation

SIGNETICS' ZERO DEFECTS PROGRAM

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressures. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable — zero defects — is, in fact, achievable.

The IC supplier committed to a standard of zero defects provides a competitive advantage to today's electronics OEM. That advantage can be summed up in four words: *reduced cost of ownership*. As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that the quality-conscious supplier represents a viable cost reduction resource. Consistently high quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures.

REDUCING THE COST OF OWNERSHIP THROUGH TOTAL QUALITY PERFORMANCE

Quality involves more than just IC's that work. It also includes cost-saving advantages that come with error-free service — on-time delivery of the right quantity of the right product at the agreed-upon price. Beyond the product, you want to know you can place an order and feel confident that no administrative problems will arise to tie up your time and personnel.

Today, as a result of Signetics' growing appreciation of the concern with cost of ownership, our quality improvement efforts extend out from the traditional areas of product conformance into every administrative function, including order entry, scheduling, delivery, shipping, and invoicing. Driving this process is a Corporate Quality Improvement Team, comprised of the president and his staff, which oversees the activities of 30 other Quality Improvement Teams throughout the company.

CUSTOMER/VENDOR COOPERATION IS AT THE HEART OF ZERO DEFECTS AND REDUCED COSTS

Working to a zero defects standard requires that emphasis be consistently placed, not on "catching" defects, but on preventing them from ever occurring. This strong preventive focus, which demands that quality be "built-in" rather than "inspected in," includes a much greater attention to ongoing communication on quality-related issues. At Signetics, a focus on this cooperative approach has resulted in better service to all customers and the development of two innovative customer/vendor programs: Ship-to-Stock and Self-Qual.

As a result of their participation in the Ship-to-Stock Program, many of our customers have eliminated costly incoming testing on selected ICs. We will work together with any customer interested to establish a Ship-to-Stock Program, and identify the products to be included in the program and finalize all necessary terms and conditions. From that point, the specified products can go directly from the receiving dock to the assembly line or into inventory. Signetics then provides, free of charge, monthly reports on those products.

In our efforts to continually reduce cost of ownership, we are now using the experience we have gained with Ship-to-Stock to begin developing a Just-in-Time Program. With Just-in-Time, products will be delivered to the receiving dock just as they are needed, permitting continuous-flow manufacturing and eliminating the need for expensive inventories.

Like Ship-to-Stock, our Self-Qual Program employs a cooperative approach based on ongoing information exchange. At Signetics, formal qualification procedures are required for all new or changed materials, processes, products, and facilities. Prior to 1983, we created our qualification programs independently. Our major customers would then test samples to confirm our findings. Now, under the new Self-Qual Program, customers can be directly involved in the prequalification stage. When we feel we have a promising enhancement to offer, customers will be invited to participate in the development of the qualification plan. This eliminates the need to duplicate expensive qualification testing and also adds another dimension to our ongoing efforts to build in quality.

PRODUCT RELIABILITY: QUALITY OVER TIME IS THE GOAL

Our concern with product reliability has developed from communication with many customers. In discussions, these customers have emphasized the high cost of field failures, both in terms of dollars and reputations in the marketplace.

In response to these concerns, we have placed an emphasis on improving product reliability. As a result of this effort, our product reliability has improved more than fourfold in a five-year period (see Figure 1). A key program, SURE (Systematic and Uniform Reliability Evaluation), highlights the significant progress made in this critical area.

SURE was first instituted in 1964 as the core reliability measurement for all Signetics products. In 1980, as a first major step toward improving product reliability, SURE was enhanced by increasing sampling frequency and size and by extending stress tests. As a result of these improvements, most of our major customers now utilize SURE data with no requests for additional reliability testing.

WE WANT TO WORK WITH YOU

At Signetics, we know that our success depends on our ability to support all our customers with the defect-free, higher density, higher performance products needed to compete effectively in today's demanding business environment. To achieve this goal, quality in another arena — that of communications — is vital. Here are some specific ways we can maintain an ongoing dialogue and information exchange between your company and ours on the quality issue:

- Periodical face-to-face exchanges of data and quality improvement ideas between the customer and Signetics can help prevent problems before they occur.
- Test correlation data is very useful. Line pull information and field failure reports also help us improve product performance.
- When a problem occurs, provide us as soon as possible with whatever specific data you have. This will assist us in taking prompt corrective action.

Quality products are, in large measure, the result of quality communication. By working together, by opening up channels through which we can talk openly to each other, we will insure the creation of the innovative, reliable, cost effective products that help insure a competitive edge.

Quality and Reliability

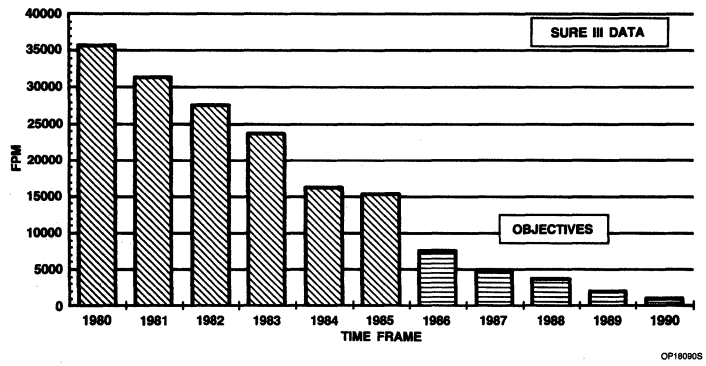


Figure 1

QUALITY AND RELIABILITY ASSURANCE

Signetics' Linear Division Quality and Reliability Assurance Department is involved in all stages of the production of our Linear ICs:

- Product Design and Process Development
- Wafer Fabrication
- Assembly
- Inspection and Test
- Product Reliability Monitoring
- Customer liaison

The result of this continual involvement at all stages of production enables us to provide feedback to refine present and future designs, manufacturing processes, and test methodology to enhance both the quality and reliability of the products delivered to our customers.

LINEAR PRODUCT QUALITY

Signetics has put together a winning process for the manufacturing of Linear Integrated Circuits. The circuits produced by our Linear Division must meet rigid criteria as defined in our design rules and as evaluated through product characterization over the device operating temperature range. Product conformance to specification is measured throughout the manufacturing cycle. Our standard is Zero Defects and our customers' statistics and awards for outstanding product quality demonstrate our advance toward this goal.

Nowhere is this more evident than at our Electrical Outgoing Product Assurance inspection gate. Over the past six years, the measured defect level at the first submission to Product Assurance for Linear products has dropped from over 4000PPM (0.4%) to under 150PPM (0.015%) (see Figure 2). Signetics calls the first submittal to a Product or Quality Assurance gate our Estimated Process Quality or EPQ. It is an internal measure used to drive our Quality Improvement Programs toward our goal of Zero Defects. All product acceptance sampling plans have zero as their acceptance criteria. Only shipments that demonstrate zero defects during these acceptance tests may be shipped to our customers. This is in accordance with our commitment to our Zero Defect policy.

The results from our Quality Improvement Program have allowed Signetics to take the industry leadership position with its Zero Defects Limited Warranty policy. No longer is it necessary to negotiate a mutually acceptable AQL between buyer and Signetics. Signetics will replace any lot in which a customer finds one verified defective part.

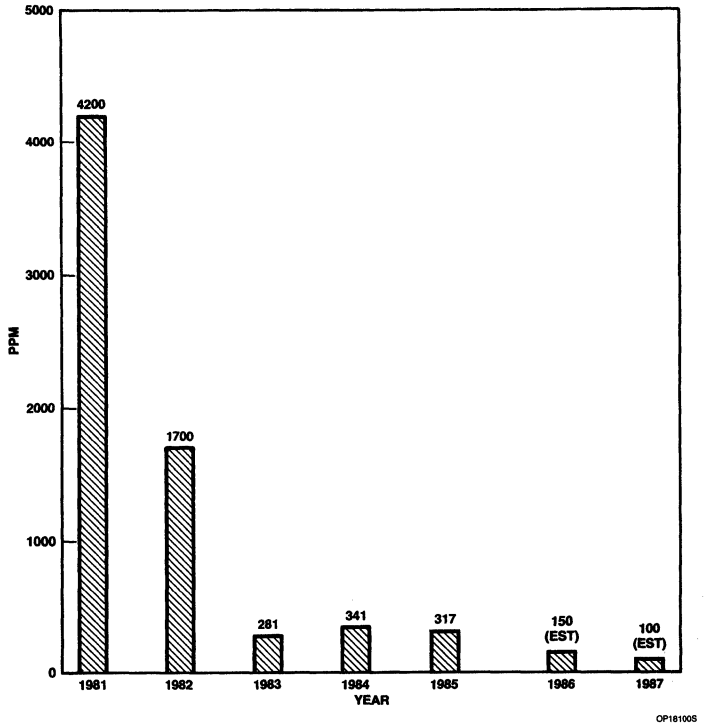


Figure 2. Electrical Estimated Process Quality (EPQ)

QUALITY DATABASE REPORTING SYSTEM — QA05

The capabilities of our manufacturing process are measured and the results are recorded through our corporate-wide QA05 database system. The QA05 system collects the results on all finished lots and feeds this data back to concerned organizations where appropriate corrective actions can be taken. The QA05 reports Estimated Process Quality (EPQ) data which are the sample inspection results for first submittal lots to Quality Assurance inspection for electrical, visual/mechanical, hermeticity, and documentation. Data from this system is available upon request and is distributed routinely to our customers who have formally adopted our Ship-to-Stock program.

SIGNETICS' SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into inventory or to the assembly line from the customer's receiving dock without incoming inspection. This program was developed at the request of several major customers after they had worked with us and had a chance to experience the data exchange and joint corrective action that occurs as part of our quality improvement program.

The key elements of the Ship-to-Stock program are:

- Signetics and customer agree on a list of products to be certified, complete device correlation, and sign a specification.
- The product Estimated Product Quality (EPQ) must be 300ppm or less for the past 3 months.
- Signetics will share Quality (QA05) and Reliability data on a regular basis.
- Signetics will alert Ship-to-Stock customers of any changes in quality or reliability which could adversely impact their product.

Any customer interested in the benefits of the Ship-to-Stock program should contact his local Signetics sales office for a brochure and further details.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 5×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. All circuit designs are computer-checked using the latest CAD software for adherence to design rules. Simulations are performed for functionality and parametric performance over the full operating ranges of voltage and temperature before going to production. These steps allow us to meet device specifications not only the first time, but also every time thereafter.

Quality and Reliability

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees.

PRODUCT QUALIFICATION

Linear products are subjected to rigorous qualification procedures for all new products or redesigns to current products. Qualification testing consists of:

- High Temperature Operating Life: $T_J = 150°C$, 1000 hours, static bias
- High Temperature Storage Life: $T_J = 150°C$, 1000 hours, unbiased
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 15 psig, 121°C, 192 hours, unbiased
- Thermal Shock: −65°C to +150°C, 300 cycles, 5 minute dwell, liquid to liquid, unbiased

Formal qualification procedures are required for all new or changed products, processes, and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

ONGOING RELIABILITY ASSESSMENT PROGRAMS

The SURE Program

The SURE (Systematic and Uniform Reliability Evaluation) program audits products from each of Signetics Linear Division's process families: Low Voltage, Medium Voltage, High Voltage, and Dual-Layer Metal, under a variety of accelerated stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The Audit Program

Samples are selected from each process family every four weeks and are subjected to each of the following stresses:

- High Temperature Operating Life: $T_J = 150°C$, 1000 hours, static bias
- High Temperature Storage Life: $T_J = 150°C$, 1000 hours, unbiased
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static bias
- Pressure Cooker: 20 psig, 127°C, 72 hours, unbiased
- Thermal Shock: −65°C to +150°C, 300 cycles, 5 minute dwell, liquid-to-liquid, unbiased
- Temperature Cycling: −65°C to +150°C, 1000 cycles, 10 minute dwell, air-to-air, unbiased

The Product Monitor Program

In addition, each Signetics assembly plant performs Pressure Cooker and Thermal Shock SURE Product Monitor stresses on a weekly basis on each molded package by pin count per the same conditions as the SURE Program.

Product Reliability Reports

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms, and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request. Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Reliability Engineering

In addition to the product performance monitors encompassed in the Linear SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

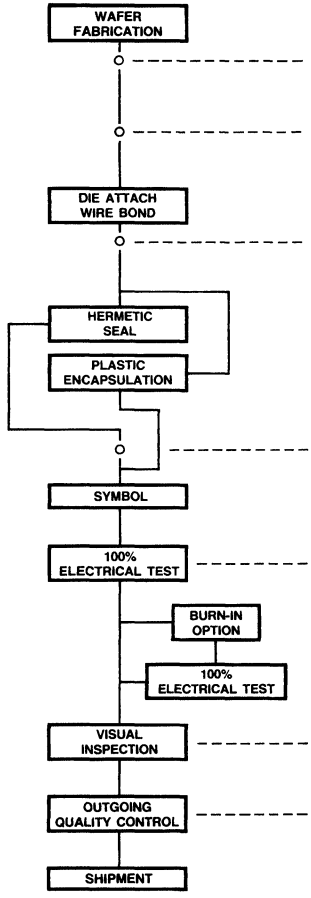
- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in some evaluation programs.

Failure Analysis

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional, and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

LINEAR DIVISION LINEAR PROCESS FLOW



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

DIE ATTACH AND WIRE BONDING

The latest automated equipment is used under statistical process control program.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% and fine gross leak testing.

SYMBOL

Devices are marked with the Signetics logo, device number and period date code of assembly or custom symbol per individual specification requirements.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

BURN-IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum Junction Temperature.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

VISUAL

All products are visually inspected per the requirements specified in Signetics' or customer documents.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees the specified mechanical and electrical AQL's. Every shipment is sealed and identified by QA personnel.

PF00850S

Signetics

Linear Products

Section 3
Small Area Networks

3

INDEX

Introduction to I²C

THE I²C CONCEPT

The Inter-IC bus (I²C) is a 2-wire serial bus designed to provide the facilities of a small area network, not only between the circuits of one system, but also between different systems; e.g., teletext and tuning.

Philips/Signetics manufactures many devices with built-in I²C interface capability, any of which can be connected in a system by simply "clipping" it to the I²C bus. Hence, any collection of these devices around the I²C bus is known as "clips."

The I²C bus consists of two bidirectional lines: the Serial Data (SDA) line and the Serial Clock (SCL) line. The output stages of devices connected to the bus (these devices could be NMOS, CMOS, I²C, TTL, ...) must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C bus can be transferred at a rate up to 100kbits/sec. The physical bus length is limited to 13 feet and the number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

The inherent synchronization process, built into the I²C bus structure using the wired-AND technique, not only allows fast devices to communicate with slower ones, but also eliminates the "Carrier Sense Multiple Access/Collision Detect" (CSMA/CD) effect found in some local area networks, such as Ethernet.

Master-slave relationships exist on the I²C bus; however, there is no central master. Therefore, a device addressed as a slave during one data transfer could possibly be the master for the next data transfer. Devices are also free to transmit or receive data during a transfer.

To summarize, the I²C bus eliminates interfacing problems. Since any peripheral device can be added or taken away without affecting any other devices connected to the bus, the I²C bus enables the system designer to build various configurations using the same basic architecture.

Application areas for the I²C bus include:

- Video Equipment
- Audio Equipment
- Computer Terminals
- Home Appliances
- Telephony
- Automotive
- Instrumentation
- Industrial Control

I²C Bus Specification

INTRODUCTION

For 8-bit applications, such as those requiring single-chip microcomputers, certain design criteria can be established:

- **A complete system usually consists of at least one microcomputer and other peripheral devices, such as memories and I/O expanders.**
- **The cost of connecting the various devices within the system must be kept to a minimum.**
- **Such a system usually performs a control function and does not require high-speed data transfer.**
- **Overall efficiency depends on the devices chosen and the interconnecting bus structure.**

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be resolved to decide which device will be in control of the bus and when. And if different devices with different clock speeds are connected to the bus, the bus clock source must be defined.

All these criteria are involved in the specification of the I²C bus.

THE I²C BUS CONCEPT

Any manufacturing process (NMOS, CMOS, I²L) can be supported by the I²C bus. Two wires (SDA – serial data, SCL – serial clock) carry information between the devices connected to the bus. Each device is recognized by a unique address – whether it is a microcomputer, LCD driver, memory or keyboard interface – and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, while a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually microcomputers, let's consider the case of a data transfer between two microcomputers connected to the I²C bus (Figure 1). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would follow in this way:

1) Suppose microcomputer A wants to send information to microcomputer B
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master transmitter) sends data to microcomputer B (slave receiver)
   - microcomputer A terminates the transfer.
2) If microcomputer A wants to receive information from microcomputer B
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master receiver) receives data from microcomputer B (slave transmitter)
   - microcomputer A terminates the transfer.

Even in this case, the master (microcomputer A) generates the timing and terminates the transfer.

The possibility of more than one microcomputer being connected to the I²C bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event, an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all devices to the I²C bus.

If two or more masters try to put information on to the bus, the first to produce a one when the other produces a zero will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Arbitration and Clock Generation).

Generation of clock signals on the I²C bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow slave

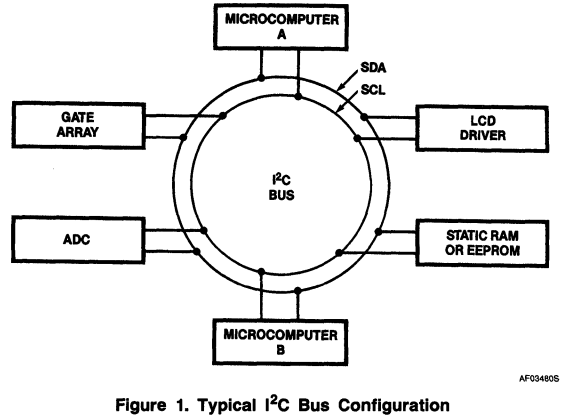


Figure 1. Typical I²C Bus Configuration

I²C Bus Specification

Table 1. Definition of I²C Bus Terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

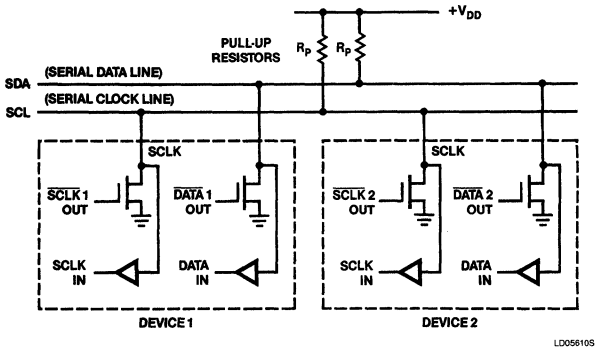


Figure 2. Connection of Devices to the I²C Bus

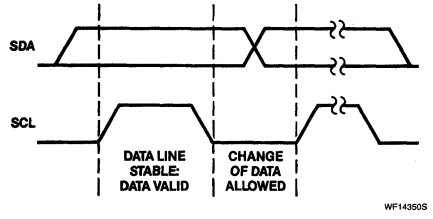


Figure 3. Bit Transfer on the I²C Bus

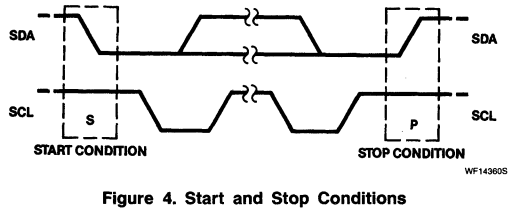


Figure 4. Start and Stop Conditions

device holding down the clock line or by another master when arbitration takes place.

GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 2). When the bus is free, both lines are High. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C bus can be transferred at a rate up to 100kbit/s. The number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, I²L) which can be connected to the I²C bus, the levels of the logical 0 (Low) and 1 (High) are not fixed and depend on the appropriate level of V_{DD} (see Electrical Specifications). One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the High period of the clock. The High or Low state of the data line can only change when the clock signal on the SCL line is Low (Figure 3).

Start and Stop Conditions

Within the procedure of the I²C bus, unique situations arise which are defined as start and stop conditions (see Figure 4).

A High-to-Low transition of the SDA line while SCL is High is one such unique case. This situation indicates a start condition.

A Low-to-High transition of the SDA line while SCL is High defines a stop condition.

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition. This bus free situation will be described later in detail.

Detection of start and stop conditions by devices connected to the bus is easy if they possess the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

TRANSFERRING DATA

Byte Format

Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit.

I²C Bus Specification

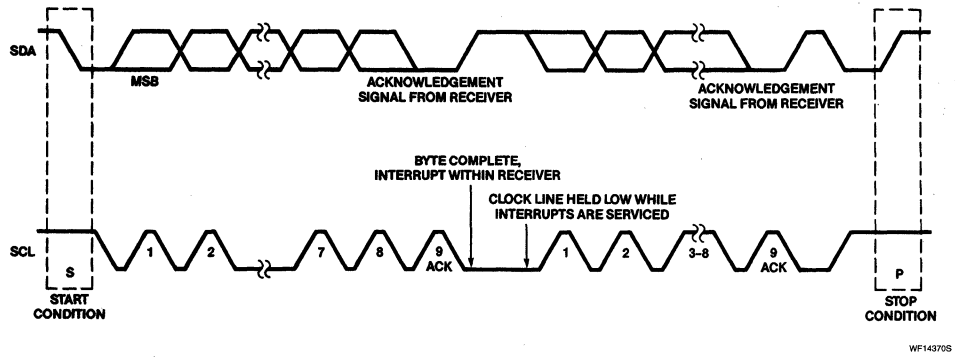


Figure 5. Data Transfer on the I²C Bus

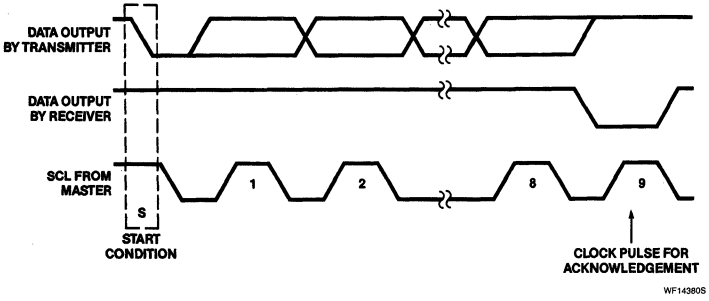


Figure 6. Acknowledge on the I²C Bus

Data is transferred with the most significant bit (MSB) first (Figure 5). If a receiving device cannot receive another complete byte of data until it has performed some other function, for example, to service an internal interrupt, it can hold the clock line SCL Low to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases the clock line SCL.

In some cases, it is permitted to use a different format from the I²C bus format, such as CBUS compatible devices. A message which starts with such an address can be terminated by the generation of a stop condition, even during the transmission of a byte. In this case, no acknowledge is generated.

Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitting device releases the SDA line (High) during the acknowledge clock pulse.

The receiving device has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable Low during the high period of this clock pulse (Figure 6). Of course, setup and hold times must also be taken into account and these will be described in the Timing section.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with a CBUS address.

When a slave receiver does not acknowledge on the slave address, for example, because it is unable to receive while it is performing some real-time function, the data line must be left High by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver does acknowledge the slave address, but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave not generating the acknowledge on the first byte following. The slave leaves the data line High and the master generates the STOP condition.

In the case of a master receiver involved in a transfer, it must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate the STOP condition.

ARBITRATION AND CLOCK GENERATION

Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C bus. Data is only valid during the clock High period on the SCL line; therefore, a defined clock is needed if the bit-by-bit arbitration procedure is to take place.

Clock synchronization is performed using the wired-AND connection of devices to the SCL LINE. This means that a High-to-Low transi-

I²C Bus Specification

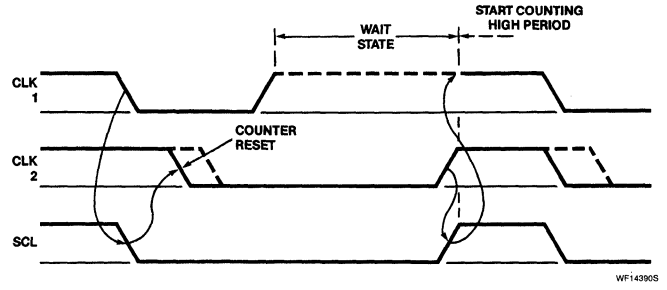


Figure 7. Clock Synchronization During the Arbitration Procedure

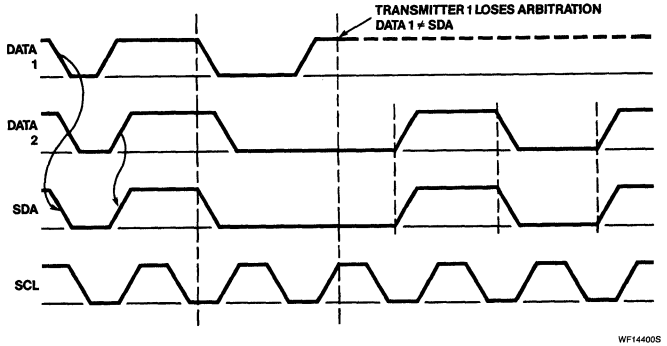


Figure 8. Arbitration Procedure of Two Masters

tion on the SCL line will affect the devices concerned, causing them to start counting off their Low period. Once a device clock has gone Low it will hold the SCL line in that state until the clock High state is reached (Figure 7). However, the Low-to-High change in this device clock may not change the state of the SCL line if another device
clock is still within its Low period. Therefore, SCL will be held Low by the device with the longest Low period. Devices with shorter Low periods enter a High wait state during this time.

When all devices concerned have counted off their Low period, the clock line will be released and go High. There will then be no difference between the device clocks and the state of the SCL line and all of them will start counting their High periods. The first device to complete its High period will again pull the SCL line Low.

In this way, a synchronized SCL clock is generated for which the Low period is determined by the device with the longest clock Low period while the High period on SCL is determined by the device with the shortest clock High period.

Arbitration

Arbitration takes place on the SDA line in such a way that the master which transmits a High level, while another master transmits a Low level, will switch off its DATA output stage since the level on the bus does not correspond to its own level.

Arbitration can carry on through many bits. The first stage of arbitration is the comparison of the address bits. If the masters are each trying to address the same device, arbitration continues into a comparison of the data. Because address and data information is used on the I²C bus for the arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master does lose arbitration during the addressing stage, it is possible that the winning master is trying to address it. Therefore, the losing master must switch over immediately to its slave receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course more may be involved, depending on how many masters are connected to the bus. The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a High output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. As control of the I²C bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Use of the Clock Synchronizing Mechanism as a Handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receiving devices to cope with fast data transfers, either on a byte or bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slave devices can then hold the SCL line Low, after reception and acknowledge of a byte, to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcomputer without a hardware I²C interface on-chip can slow down the bus clock by extending each clock Low period. In this way, the speed of any master is adapted to the internal operating rate of this device.

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FORMATS

Data transfers follow the format shown in Figure 9. After the start condition, a slave address is sent. This address is 7 bits long; the eighth bit is a data direction bit (R/$\overline{W}$). A zero indicates a transmission (WRITE); a one indicates a request for data (READ). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another start condition, and address another slave without first generating a stop condition. Various combinations of read/write formats are then possible within such a transfer.

At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.

The stop condition is generated by the master.

During a change of direction within a transfer, the start condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

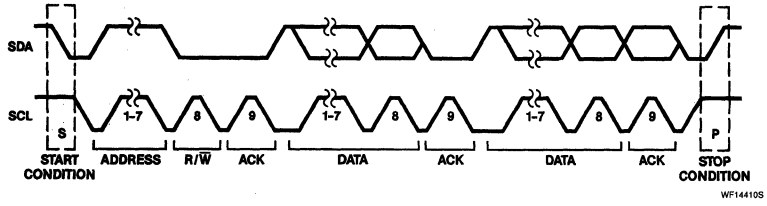
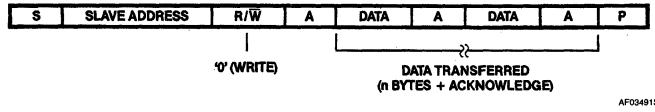


Figure 9. A Complete Data Transfer

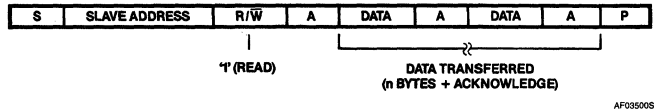
Possible Data Transfer Formats are:

a) Master transmitter transmits to slave receiver. Direction is not changed.

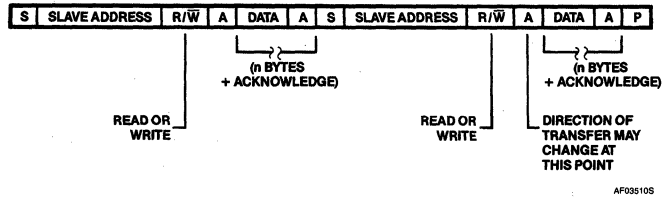
A = ACKNOWLEDGE
S = START
P = STOP



b) Master reads slave immediately after first byte.



c) Combined formats.



NOTES:
1. Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the start condition is repeated, data can then be transferred.
2. All decisions on auto-increment or decrement of previously accessed memory locations, etc., are taken by the designer of the device.
3. Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.
4. I²C devices have to reset their bus logic on receipt of a start condition so that they all anticipate the sending of a slave address.

I²C Bus Specification

ADDRESSING

The first byte after the start condition determines which slave will be selected by the master. Usually, this first byte follows that start procedure. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge, although devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

Definition of Bits in the First Byte

The first seven bits of this byte make up the slave address (Figure 10). The eighth bit (LSB – least significant bit) determines the direction of the message. A zero on the least significant position of the first byte means that the master will write information to a selected slave; a one in this position means that the master will read information from the slave.

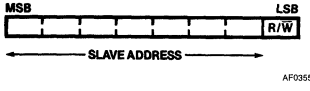


Figure 10. The First Byte After the Start Procedure

When an address is sent, each device in a system compares the first 7 bits after the start condition with its own address. If there is a match, the device will consider itself addressed by the master as a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

The slave address can be made up of a fixed and a programmable part. Since it is expected that identical ICs will be used more than once in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of eight identical devices can be connected to the same bus.

The I²C bus committee is available to coordinate allocation of I²C addresses.

The bit combination 1111XXX of the slave address is reserved for future extension purposes.

The address 1111111 is reserved as the extension address. This means that the addressing procedure will be continued in the next byte(s). Devices that do not use the extended addressing do not react at the reception of this byte. The seven other possibilities in group 1111 will also only be used for extension purposes but are not yet allocated.

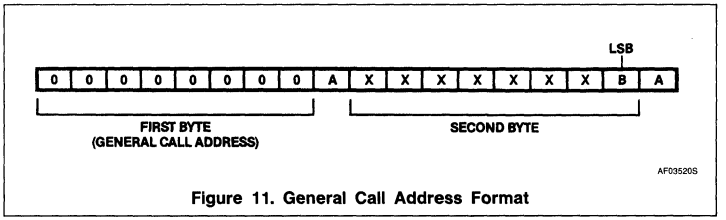


Figure 11. General Call Address Format

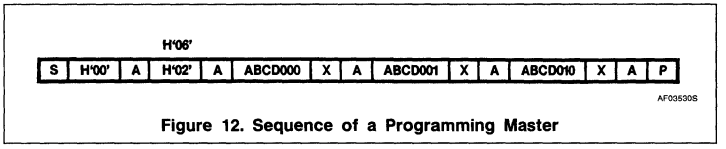


Figure 12. Sequence of a Programming Master

The combination 0000XXX has been defined as a special group. The following addresses have been allocated:

FIRST BYTE			
Slave Address		R/$\overline{W}$	
0000	000	0	General call address
0000	000	1	Start byte
0000	001	X	CBUS address
0000	010	X	Address reserved for different bus format
0000	011	X	To be defined
0000	100	X	
0000	101	X	
0000	110	X	
0000	111	X	

No device is allowed to acknowledge at the reception of the start byte.

The CBUS address has been reserved to enable the intermixing of CBUS and I²C devices in one system. I²C bus devices are not allowed to respond at the reception of this address.

The address reserved for a different bus format is included to enable the mixing of I²C and other protocols. Only I²C devices that are able to work with such formats and protocols are allowed to respond to this address.

General Call Address

The general call address should be used to address every device connected to the I²C bus. However, if a device does not need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If a device does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging.

The meaning of the general call address is always specified in the second byte (Figure 11).

There are two cases to consider:
1. When the least significant bit B is a zero.
2. When the least significant bit B is a one.

When B is a zero, the second byte has the following definition:

00000110 (H'06') Reset and write the programmable part of slave address by software and hardware. On receiving this two-byte sequence, all devices (designed to respond to the general call address) will reset and take in the programmable part of their address.
Precautions must be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

00000010 (H'02') Write slave address by software only. All devices which obtain the programmable part of their address by software (and which have been designed to respond to the general call address) will enter a mode in which they can be programmed. The device will not reset.

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An example of a data transfer of a programming master is shown in Figure 12 (ABCD represents the fixed part of the address).

00000100 (H'04') Write slave address by hardware only. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two-byte sequence. The device will not reset.

00000000 (H'00') This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore these codes.

When B is a one, the two-byte sequence is a hardware general call. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master does not know in advance to which device the message must be transferred, it can only generate this hardware general call and its own address, thereby identifying itself to the system (Figure 13).

The seven bits remaining in the second byte contain the device address of the hardware master. This address is recognized by an intelligent device, such as a microcomputer, connected to the bus which will then direct the information coming from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems an alternative could be that the hardware master transmitter is brought in the slave receiver mode after the system reset. In this way, a system configuring master can tell the hardware master transmitter (which is now in slave receiver mode) to which address data must be sent (Figure 14). After this programming procedure, the hardware master remains in the master transmitter mode.

Start Byte

Microcomputers can be connected to the I²C bus in two ways. If an on-chip hardware I²C bus interface is present, the microcomputer can be programmed to be interrupted only by requests from the bus. When the device possesses no such interface, it must constantly monitor the bus via software. Obviously, the more times the microcomputer monitors, or polls, the bus, the less time it can spend carrying out its intended function.

Therefore, there is a difference in speed between fast hardware devices and the relatively slow microcomputer which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Figure 15). The start procedure consists of:

a) A start condition, (S)
b) A start byte 00000001
c) An acknowledge clock pulse
d) A repeated start condition, (Sr)

After the start condition (S) has been transmitted by a master requiring bus access, the start byte (00000001) is transmitted. Another microcomputer can therefore sample the SDA line on a low sampling rate until one of the seven zeros in the start byte is detected. After detection of this Low level on the SDA line, the microcomputer is then able to switch to a higher sampling rate in order to find the second start condition (Sr) which is then used for synchronization.

A hardware receiver will reset at the reception of the second start condition (Sr) and will therefore ignore the start byte.

After the start byte, an acknowledge-related clock pulse is generated. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the start byte.

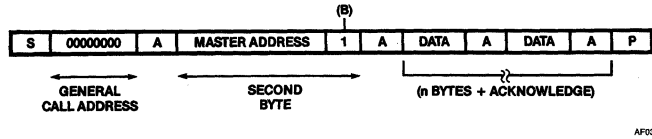
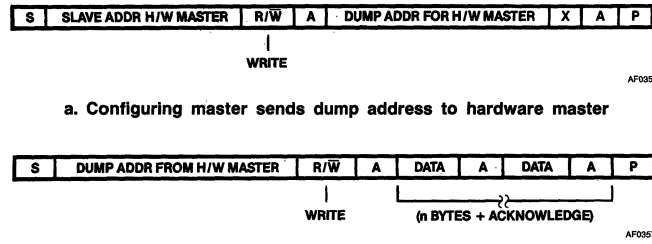


Figure 13. Data Transfer From Hardware Master Transmitter



a. Configuring master sends dump address to hardware master

b. Hardware master dumps data to selected slave device

Figure 14. Data Transfer of Hardware Master Transmitter Capable of Dumping Data Directly to Slave Devices

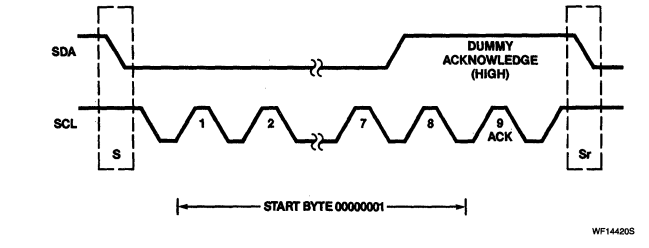


Figure 15. Start Byte Procedure

I²C Bus Specification

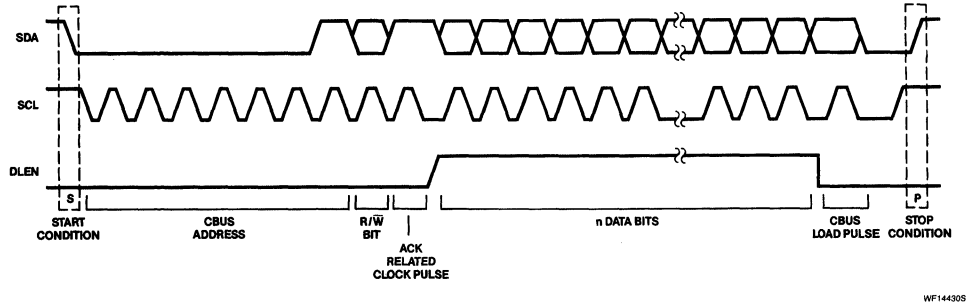


Figure 16. Data Format of Transmissions With CBUS Receiver/Transmitter

CBUS Compatibility

Existing CBUS receivers can be connected to the I²C bus. In this case, a third line called DLEN has to be connected and the acknowledge bit omitted. Normally, I²C transmissions are multiples of 8-bit bytes; however, CBUS devices have different formats.

In a mixed bus structure, I²C devices are not allowed to respond on the CBUS message. For this reason, a special CBUS address (0000001X) has been reserved. No I²C device will respond to this address. After the transmission of the CBUS address, the DLEN line can be made active and transmission, according to the CBUS format, can be performed (Figure 16).

After the stop condition, all devices are again ready to accept data.

Master transmitters are allowed to generate CBUS formats after having sent the CBUS address. Such a transmission is terminated by a stop condition, recognized by all devices. In the low speed mode, full 8-bit bytes must always be transmitted and the timing of the DLEN signal adapted.

If the CBUS configuration is known and no expansion with CBUS devices is foreseen, the user is allowed to adapt the hold time to the specific requirements of device(s) used.

ELECTRICAL SPECIFICATIONS OF INPUTS AND OUTPUTS OF I²C DEVICES

The I²C bus allows communication between devices made in different technologies which might also use different supply voltages.

For devices with fixed input levels, operating on a supply voltage of +5V ± 10%, the following levels have been defined:

V_{ILmax} = 1.5V (maximum input Low voltage)

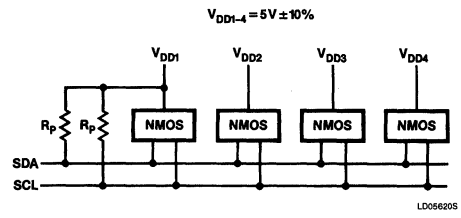


Figure 17. Fixed Input Level Devices Connected to the I²C Bus

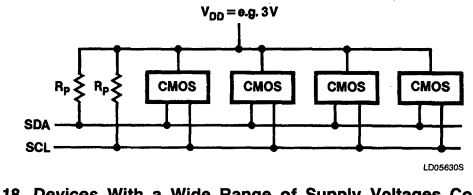


Figure 18. Devices With a Wide Range of Supply Voltages Connected to the I²C Bus

V_{IHmin} = 3V (minimum input High voltage)

Devices operating on a fixed supply voltage different from +5V (e.g. I²L), must also have these input levels of 1.5V and 3V for V_{IL} and V_{IH}, respectively.

For devices operating over a wide range of supply voltages (e.g. CMOS), the following levels have been defined:

$V_{ILmax} = 0.3V_{DD}$ (maximum input Low voltage)

$V_{IHmin} = 0.7V_{DD}$ (minimum input High voltage)

For both groups of devices, the maximum output Low value has been defined:

V_{OLmax} = 0.4V (max. output voltage Low) at 3mA sink current

The maximum low-level input current at V_{OLmax} of both the SDA pin and the SCL pin of an I²C device is −10μA, including the leakage current of a possible output stage.

The maximum high-level input current at $0.9V_{DD}$ of both the SDA pin and SCL pin of an I²C device is 10μA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA pin and the SCL pin of an I²C device is 10pF.

Devices with fixed input levels can each have their own power supply of +5V ± 10%. Pull-up resistors can be connected to any supply (see Figure 17).

However, the devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (see Figure 18).

I²C Bus Specification

When devices with fixed input levels are mixed with devices with V_{DD}-related levels, the latter devices have to be connected to one common supply line of +5V ± 10% along with the pull-up resistors (Figure 19).

Input levels are defined in such a way that:

1. The noise margin on the Low level is 0.1 V_{DD}.
2. The noise margin on the High level is 0.2 V_{DD}.
3. Series resistors (R_S) up to 300Ω can be used for flash-over protection against high voltage spikes on the SDA and SCL line (due to flash-over of a TV picture tube, for example) (Figure 20).

The maximum bus capacitance per wire is 400pF. This includes the capacitance of the wire itself and the capacitance of the pins connected to it.

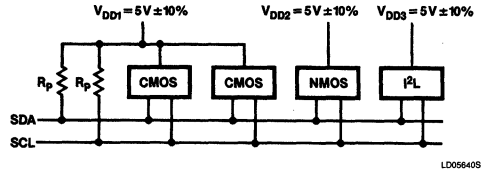


Figure 19. Devices With V_{DD} Related Levels Mixed With Fixed Input Level Devices on the I²C Bus

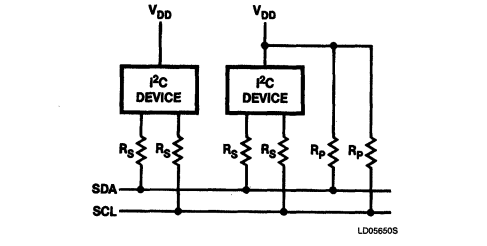


Figure 20. Serial Resistors (R_S) for Protection Against High Voltage

TIMING

The clock on the I²C bus has a minimum Low period of 4.7μs and a minimum High period of 4μs. Masters in this mode can generate a bus clock with a frequency from 0 to 100kHz.

All devices connected to the bus must be able to follow transfers with frequencies up to 100kHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch the Low periods. In the latter case the frequency is reduced.

Figure 21 shows the timing requirements in detail. A description of the abbreviations used is shown in Table 2. All timing references are at V_{ILmax} and V_{ILmin}.

LOW-SPEED MODE

As explained previously, there is a difference in speed on the I²C bus between fast hardware devices and the relatively slow microcomputer which relies on software polling. For this reason a low speed mode is available on the I²C bus to allow these microcomputers to poll the bus less often.

Start and Stop Conditions

In the low-speed mode, data transfer is preceded by the start procedure.

Data Format and Timing

The bus clock in this mode has a Low period of 130μs ± 25μs and a High period of 390μs ± 25μs, resulting in a clock frequency of approx. 2kHz. The duty cycle of the clock has this Low-to-High ratio to allow for more efficient use of microcomputers without an on-chip hardware I²C bus interface. In this mode also, data transfer with acknowledge is obligatory. The maximum number of bytes transferred is not limited (Figure 22).

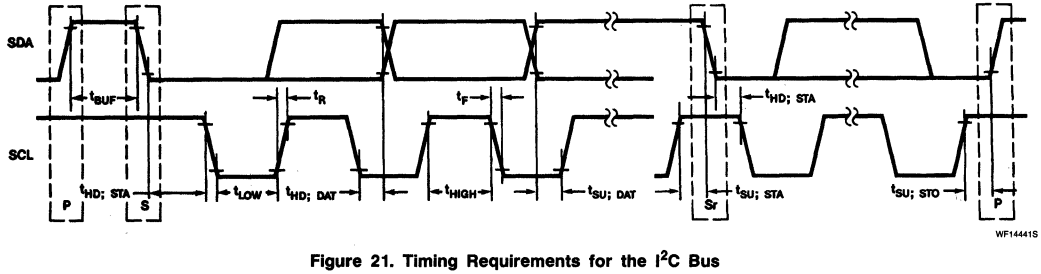


Figure 21. Timing Requirements for the I²C Bus

I²C Bus Specification

Table 2. Timing Requirement for the I²C Bus

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
f_{SCL}	SCL clock frequency	0	100	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		μs
$t_{HD;\ STA}$	Hold time start condition. After this period the first clock pulse is generated	4		μs
t_{LOW}	The Low period of the clock	4.7		μs
t_{HIGH}	The High period of the clock	4		μs
$t_{SU;\ STA}$	Setup time for start condition (Only relevant for a repeated start condition)	4.7		μs
$t_{HD;\ DAT}$	Hold time DATA for CBUS compatible masters for I²C devices	 5 0*		 μs μs
$t_{SU;\ DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	μs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;\ STO}$	Setup time for stop condition	4.7		μs

NOTES:
All values referenced to V_{IH} and V_{IL} levels.
* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

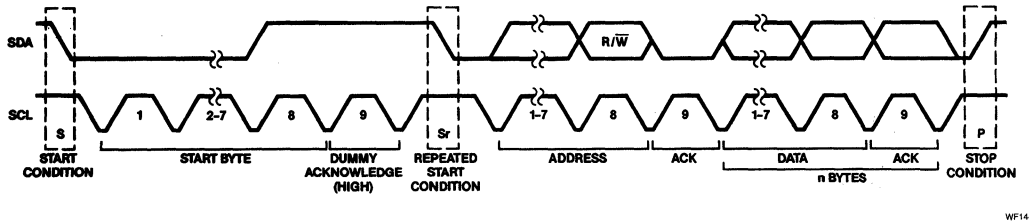


Figure 22. Data Transfer Low-Speed Mode

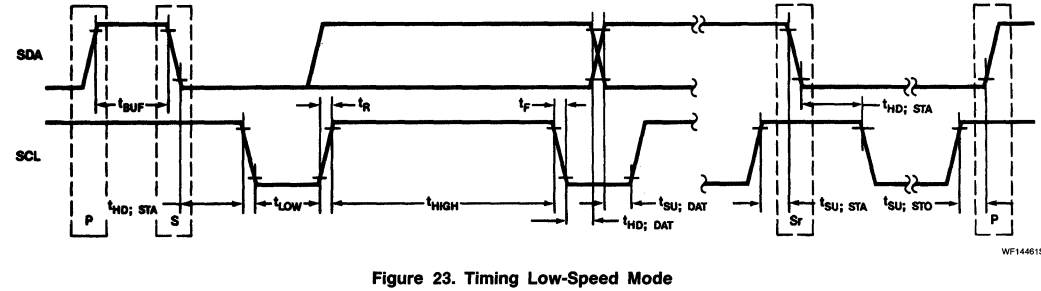


Figure 23. Timing Low-Speed Mode

I²C Bus Specification

LOW SPEED MODE

CLOCK	: $t_{LOW} = 130\mu s \pm 25\mu s$
DUTY CYCLE	: $t_{HIGH} = 390\mu s \pm 25\mu s$: 1:3 Low-to-High (Duty cycle of clock generator)
START BYTE	: 0000 0001
MAX. NO. OF BYTES	: UNRESTRICTED
PREMATURE TERMINATION OF TRANSFER	: NOT ALLOWED
ACKNOWLEDGE CLOCK BIT	: ALWAYS PROVIDED
ACKNOWLEDGEMENT OF SLAVES	: OBLIGATORY

In this mode, a transfer cannot be terminated during the transmission of a byte.

The bus is considered busy after the first start condition. It is considered free again one minimum clock Low period, 105μs, after the detection of the stop condition. Figure 23 shows the timing requirements in detail, Table 3 explains the abbreviations.

Table 3. Timing Low Speed Mode

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{BUF}	Time the bus must be free before a new transmission can start	105		μs
$t_{HD;\ STA}$	Hold time start condition. After this period the first clock pulse is generated	365		μs
$t_{HD;\ STA}$	Hold time (repeated start condition only)	210		μs
t_{LOW}	The Low period of the clock	105	155	μs
t_{HIGH}	The High period of the clock	365	415	μs
$t_{SU;\ STA}$	Setup time for start condition (Only relevant for a repeated start condition)	105	155	μs
$t_{HD;\ DAT}$	Hold time DATA for CBUS compatible masters for I²C devices	 5 0*		 μs μs
$t_{SU;\ DAT}$	Setup time DATA	250		ns
t_R	Rise time of both SDA and SCL lines		1	μs
t_F	Fall time of both SDA and SCL lines		300	ns
$t_{SU;\ STO}$	Setup time for stop condition	105	155	μs

NOTES:
All values referenced to V_{IH} and V_{IL} levels.
* Note that a transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

I²C Bus Specification

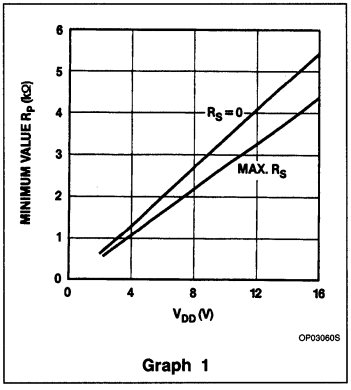
APPENDIX A

Maximum and minimum values of the pull-up resistors R_P and series resistors R_S (See Figure 20).

In a I²C bus system these values depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices (input current + leakage current)

1) The supply voltage limits the minimum value of the R_P resistor due to the specified 3mA as minimum sink current of the output stages, at 0.4V as maximum low voltage. In Graph 1, V_{DD} against R_{Pmin} is shown.

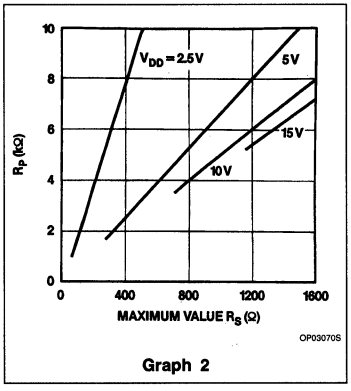


Graph 1

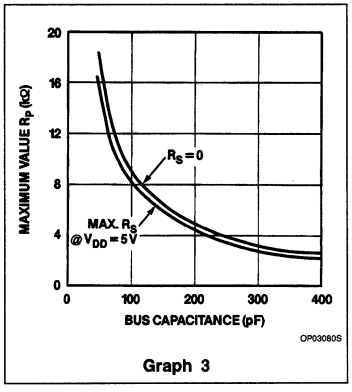
The desired noise margin of 0.1 V_{DD} for the low level limits the maximum value of R_S.

In Graph 2, R_{Smax} against R_P is shown.

2) The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of R_P because of the specified rise time of 1μs.



Graph 2

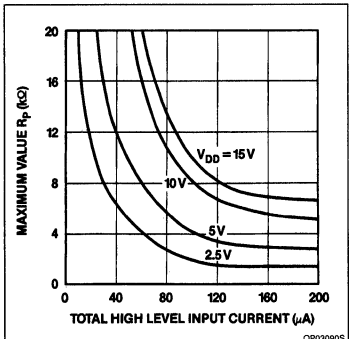


Graph 3

In Graph 3, the bus capacitance – R_{Pmax} relationship is shown.

3) The maximum high-level input current of each input/output connection has a specified value of 10μA max. Due to the desired noise margin of 0.2 V_{DD} for the high level, this input current limits the maximum value of R_P. This limit is dependent on V_{DD}.

In Graph 4 the total high-level input current – R_{Pmax} relationship is shown.



Graph 4

I²C LICENSE

Purchase of Signetics or Philips I²C components conveys a license under the Philips I²C patent rights to use these components in an I²C system, provided that the system conforms to the I²C standard specification as defined by Philips.

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The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

Application Note

Author: Carl Fenger

INTRODUCTION

The I^2C (Inter-IC) bus is becoming a popular concept which implements an innovative serial bus protocol that needs to be understood. On the hardware level I^2C is a collection of microcomputers (MAB8400, PCD3343, 83C351, 84CXX) and peripherals (LCD/LED drivers, RAM, ROM, clock/timer, A/D, D/A, IR transcoder, I/O, DTMF generator, and various tuning circuits) that communicate serially over a two-wire bus, serial data (SDA) and serial clock (SCL). The I^2C structure is optimized for hardware simplicity. Parallel address and data buses inherent in conventional systems are replaced by a serial protocol that transmits both address and bidirectional data over a 2-line bus. This means that interconnecting wires are reduced to a minimum; only V_{CC}, ground and the two-wire bus are required to link the controller(s) with the peripherals or other controllers. This results in reduced chip size, pin count, and interconnections. An I^2C system is therefore smaller, simpler, and cheaper to implement than its parallel counterpart.

The data rate of the I^2C bus makes it suited for systems that do not require high speed. An I^2C controller is well suited for use in systems such as television controllers, telephone sets, appliances, displays or applications involving human interface. Typically an I^2C system might be used in a control function where digitally-controllable elements are adjusted and monitored via a central processor.

The I^2C bus is an innovative hardware interface which provides the software designer the flexibility to create a truly multi-master environment. Built into the serial interface of the controllers are status registers which monitor all possible bus conditions: bus free/busy, bus contention, slave acknowledgement, and bus interference. Thus an I^2C system might include several controllers on the same bus each with the ability to asynchronously communicate with peripherals or each other. This provision also provides expandability for future add-on controllers. (The I^2C system is also ideal for use in environments where the bus is subject to noise. Distorted transmissions are immediately detected by the hardware and the information presented to the software.) A slave acknowledgement on every byte also facilitates data integrity.

An I^2C system can be as simple or sophisticated as the operating environment demands. Whether in a single master or multi-master system, noisy or 'safe', correct system operation can be insured under software control.

CONTROLLERS

Currently the family of I^2C controllers include the MAB8400, and the PCD 3343 (the PCD3343 is basically a CMOS version of the MAB8400). The MAB8400 is based on the 8048 architecture with the I^2C interface built-in. The instruction set for the MAB8400 is similar to the 8048, with a few instructions added and a few deleted. Tables 1 and 2 summarize the differences.

Programs for the MAB8400 and PCD 3343 may be assembled on an 8048-assembler using the macros listed in Appendix A. The serial I/O instructions involve moving data to and from the S0, S1, and S2 serial I/O control registers. The block diagram of the I^2C interface is shown in Figure 1.

SERIAL I/O INTERFACE

A block diagram of the Serial Input/Output (SIO) is shown in Figure 1. The clock line of the serial bus (SCL) has exclusive use of Pin 3, while the Serial Data (SDA) line shares Pin 2 with parallel I/O signal P23 of port 2. Consequently, only three I/O lines are available for port 2 when the I^2C interface is enabled.

Communication between the microcomputer and interface takes place via the internal bus of the microcomputer and the Serial Interrupt Request line. Four registers are used to store data and information controlling the operation of the interface:

- data shift register S0
- address register S0'
- status register S1
- clock control register S2.

THE I^2C BUS INTERFACE: SERIAL CONTROL REGISTERS S0, S1

All serial I^2C transfers occur between the accumulator and register S0. The I^2C hardware takes care of clocking out/in the data, and receiving/generating an acknowledge. In addition, the state of the I^2C bus is controlled and monitored via the bus control register S1. A definition of the registers is as follows:

Data Shift Register S0 — S0 is the data shift register used to perform the conversion between serial and parallel data format. All transmissions or receptions take place through register S0 MSB first. All I^2C bus receptions or transmissions involve moving data to/from the accumulator from/to S0.

Table 1. MAB8400 Family Instructions not in the MAB8048 Instruction Set

SERIAL I/O	REGISTER	CONTROL	CONDITIONAL BRANCH
MOV A,Sn	DEC @Rr	SEL MB2	JNTF addr
MOV Sn,A	DJNZ @Rr,addr	SEL MB3	
MOV Sn,#data			
EN SI			
DIS SI			

Table 2. MAB8048 Instructions not in the MAB8400 Family Instruction Set

DATA MOVES	FLAGS	BRANCH	CONTROL
MOVX A,@R	CLR F0	*JNI addr	ENTOCLK
MOVX @R,A	CPL F0	JF0 addr	
MOVP3 A,@A	CLR F1	JF1 addr	
MOVD A,P	CPL F1		
MPVD P,A			
ANLD P,A		*replaced by	
ORLD P,A		JT0, JNT0	

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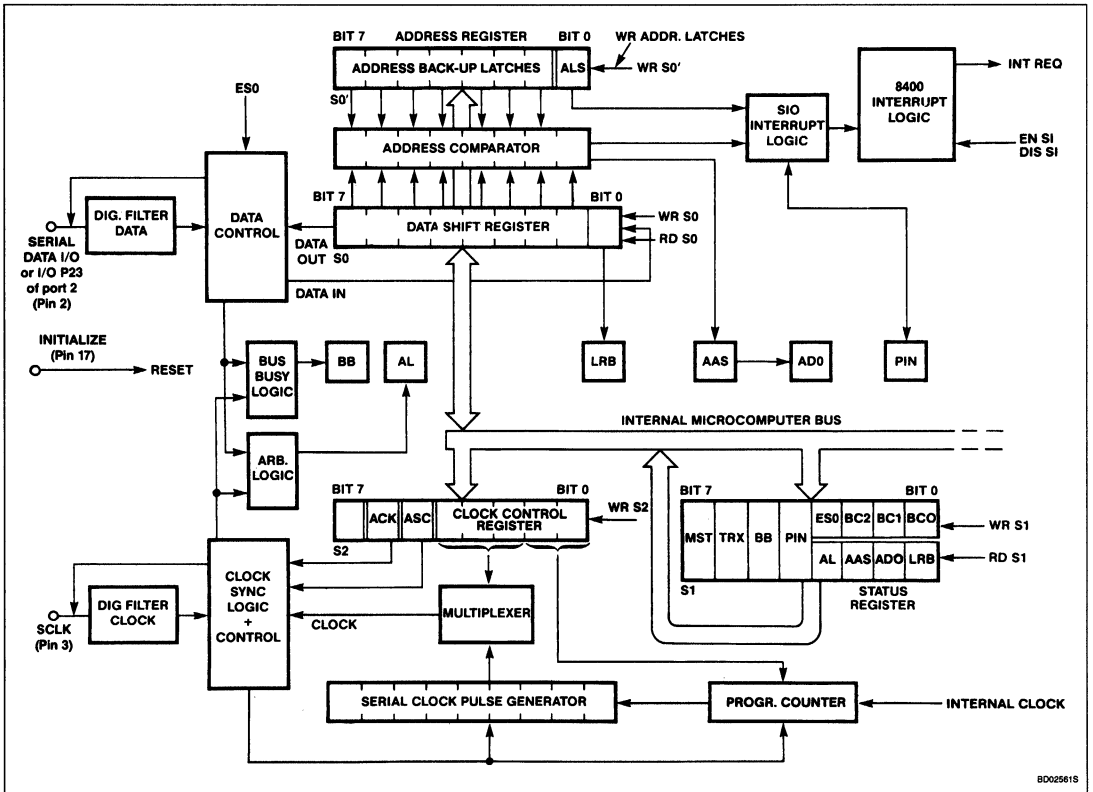

Figure 1. Block Diagram of the MAB8400 SIO Interface

Address Register S0' — In multi-master systems, this register is loaded with a controller's slave address. When activated, (ALS = 0), the hardware will recognize when it is being addressed by setting the AAS (Addressed As Slave) flag. This provision allows a master to be treated as a slave by other masters on the bus.

Status Register S1 — S1 is the bus status register. To control the SIO interface, information is written to the register. The lower 4 bits in S1 serve dual purposes; when written to, the control bits ES0, BC2, BC1, BC0 are programmed (Enable Serial Output and a 3-bit counter which indicates the current number of bits left in a serial transfer). When reading the lower four bits, we obtain the status information AL, AAS, AD0, LRB (Arbitration Lost, Addressed As Slave, Address Zero (the general call has been received), the Last Received Bit (usually the acknowledge bit)). The upper 4 bits are the MST, TRX, BB, and PIN control bits (Master, Transmitter, Bus Busy, and Pending Interrupt Not). These bits define what role the controller has at any particular time. The values of the master and transmitter bits define the controller as either a master or slave (a master initiates a transfer and generates the serial clock; a slave does not), and as a transmitter or receiver. Bus Busy keeps track of whether the bus is free or not, and is set and reset by the 'Start' and 'Stop' conditions which will be defined. Pending Interrupt Not is reset after the completion of a byte transfer + acknowledge, and can be polled to indicate when a serial transfer has been completed. An alternative to polling the PIN bit is to enable the serial interrupt; upon completion of a byte transfer, an interrupt will vector program control to location 07H.

SERIAL CLOCK/ACKNOWLEDGE CONTROL REGISTER S2

Register S2 contains the clock-control register and acknowledge mode bit. Bits S20 – S24 program the bus clock speed. Bit S26 programs the acknowledge or not-acknowledge mode (1/0). The various I^2C bus clock speed possibilities are shown in Table 3.

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

Table 3. Clock Pulse Frequency Control When Using a 4.43MHz Crystal

HEX S20 – S24 CODE	DIVISOR	APPROX. f_{CLOCK} (kHz)
0	Not Allowed	
1	39	114
2	45	98
3	51	87
4	63	70
5	75	59
6	87	51
7	99	45
8	123	36
9	147	30
A	171	26
B	195	23
C	243	18
D	291	15
E	339	13
F	387	11
10	483	9.2
11	579	7.7
12	675	6.6
13	771	5.8
14	963	4.6
15	1155	3.8
16	1347	3.3
17	1539	2.9
18*	1923	2.3
19*	2307	1.9
1A*	2691	1.7
1B*	3075	1.4
1C	3843	1.2
1D	4611	1.0
1E	5379	0.8
1F	6147	0.7

*only values that may be used in the low speed mode (ASC = 1).

These speeds represent the frequency of the serial clock bursts and do not reflect the speed of the processor's main clock (i.e. it controls the bus speed and has no effect on the CPU's execution speed).

BUS ARBITRATION

Due to the wire-AND configuration of the I^2C bus, and the self-synchronizing clock circuitry of I^2C masters, controllers with varying clock speeds can access the bus without clock contention. During arbitration, the resultant clock on the bus will have a low period equal to the longest of the low periods; the high period will equal the shortest of the high periods. Similarly, when two masters attempt to drive the data line simultaneously, the data is 'ANDed', the master generating a low while the other is driving a high will win arbitration. The resultant bus level will be low, and the loser will withdraw from the bus and set its 'Arbitration Lost' flag (S1 bit 3).

The losing Master is now configured as a slave which could be addressed during this very same cycle. These provisions allow for a number of microcomputers to exist on the same bus. With properly written subroutines, software for any one of the controllers may regard other masters as transparent.

I^2C PROTOCOL AND ASSEMBLY LANGUAGE EXAMPLES

I^2C data transfers follow a well-defined protocol. A transfer always takes place between a master and a slave. Currently a microcomputer can be master or slave, while the 'CLIPS' peripherals are always slaves. In a 'bus-free' condition, both SCL and SDA lines are kept logical high by external pull-up resistors. All bus transfers are bounded by a 'Start' and a 'Stop' condition. A 'Start' condition is defined as the SDA line making a high-to-low transition **while the SCL line is high**. At this point, the internal hardware on all slaves are activated and are prepared to clock-in the next 8 bits and interpret it as a 7-bit address and a R/$\overline{W}$ control bit (MSB first). All slaves have an internal address (most have 2 – 3 programmable address bits) which is then compared with the received address. The slave that recognized its address will respond by pulling the data line low during a ninth clock generated by the master (all I^2C byte transfers require the master to generate 8 clock pulses plus a ninth acknowledge-related clock pulse). The slave-acknowledge will be registered by the master as a '0' appearing in the LRB (Last Received Bit) position of the S1 serial I/O status register. If this bit is high after a transfer attempt, this indicates that a slave did not acknowledge, and that the transfer should be repeated.

After the desired slave has acknowledged its address, it is ready to either send or receive data in response to the master's driving clock. All other slaves have withdrawn from the bus. In addition, for multi-master systems, the start condition has set the 'Bus Busy' bit of the serial I/O register S1 on all masters on the bus. This gives a software indication to other masters that the bus is in use and to wait until the bus is free before attempting an access.

There are two types of I^2C peripherals that now must be defined: there are those with only a chip address such as the I/O expander, PCF8574, and those with a chip address plus an internal address such as the static RAM, PCF8570. Thus after sending a start condition, address, and R/$\overline{W}$ bit, we must take into account what type of slave is being addressed. In the case of a slave with only a chip address, we have already indicated its address and data direction (R/$\overline{W}$) and are therefore ready to send or receive data. This is performed by the master generating bursts of 9 clock pulses for each byte that is sent or received. The transaction for writing one byte to a slave with a chip address only is shown in Figure 3.

In this transfer, all bus activity is invoked by writing the appropriate control byte to the serial I/O control register S1, and by moving data to/from the serial bus buffer register S0. Coming from a known state (MOV S1,#18H-Slave, Receiver, Bus not Busy) we first load the serial I/O buffer S0 with the desired

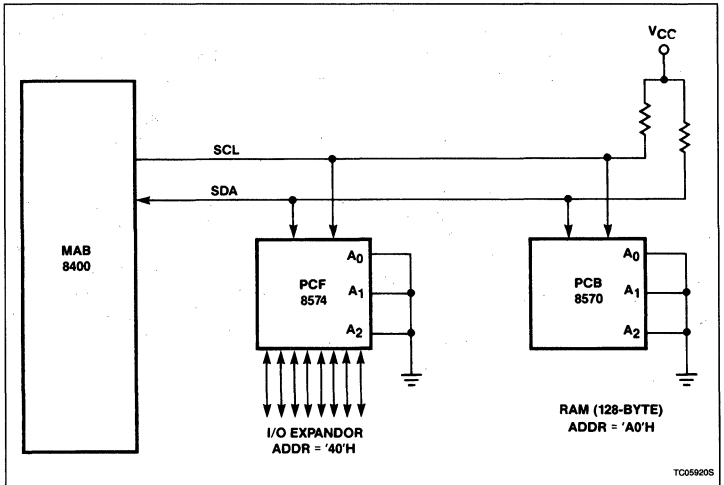

Figure 2. Schematic for Assembly Examples

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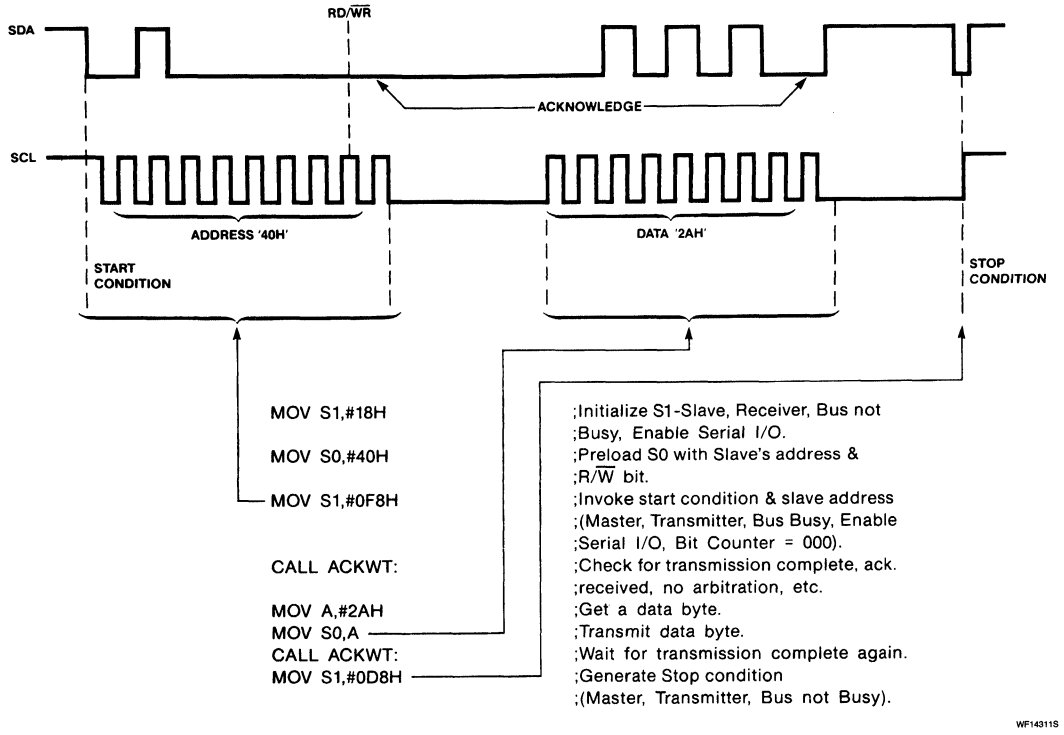

Figure 3

slave's address (MOV S0,#40H). To transmit this preceded by a start condition, we must first examine the control register S1, which, after initialization, looks like this:

MASTER	TRANS	BUS BUSY	PIN	ESO	BC2	BC1	BC0
0	0	0	1	1	0	0	0

To transmit to a slave, the Master, Transmitter, Bus Busy, PIN (Pending Interrupt Not), and ESO (Enable Serial Output) must be set to a 1. This results in an 'F8H' being written to S1. This word defines the controller as a Master Transmitter, invokes the transfer by setting the 'Bus Busy' bit, clears the Pending Interrupt Not (an inverted flag indicating the completion of a complete byte transfer), and activates the serial output logic by setting the Enable Serial Output (ESO) bit.

BIT COUNTER S12, S11, S10

BC2, BC1, and BC0 comprise a bit-counter which indicates to the logic how long the word is to be clocked out over the serial data line. By setting this to a 000H, we are telling it to produce 9 clocks (8 bits plus an acknowledge clock) for this transfer. The bit counter will then count off each bit as it is transmitted. The bit counter possibilities are shown in Table 4.

Thus the bit counter keeps track of the number of clock pulses remaining in a serial transfer. Additionally, there is a not-acknowledge mode (controlled through bit 6 of clock control register S2) which inhibits the acknowledge clock pulse, allowing the possibility of straight serial transfer. We may thus define the word size for a serial transfer (by preloading BC2, BC1, BC0 with the appropriate control number), with or without an acknowledge-related clock pulse being generated. This makes the controller able to transmit serial data to most any serial device regardless of its protocol (e.g., C-bus devices).

CHECKING FOR SLAVE ACKNOWLEDGE

After a 'Start' condition and address have been issued, the selected slave will have recognized and acknowledged its address by

Table 4. Binary Numbers in Bit-Count Locations BC2, BC1 and BC0

BC2	BC1	BC0	BITS/BYTE WITHOUT ACK	BITS/BYTE WITH ACK
0	0	1	1	2
0	1	0	2	3
0	1	1	3	4
1	0	0	4	5
1	0	1	5	6
1	1	0	6	7
1	1	1	7	8
0	0	0	8	9

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pulling the data line low during the ninth clock pulse. During this period, the software (which runs on the processor's 4MHz clock) will have been either waiting for the transfer to be completed by polling the PIN bit in S1 which goes low on completion of a transfer/reception (whose length is defined by the preloaded Bit-counter value), or by the hardware in Serial Interrupt mode. The serial interrupt (vectored to 07H) is enabled via the EN SI (enable serial interrupt) instruction.

At the point when PIN goes low (or the serial interrupt is received) the 9-bit transfer has been completed. The acknowledgement bit will now be in the LRB position of register S1, and may be checked in the routine 'ACKWT' (Wait for Acknowledge) as shown in Figure 4.

This routing must go one step further in multimaster systems; the possibility of an Arbitration Lost situation may occur if other masters are present on the bus. This condition may be detected by checking the 'AL' bit (bit 3). If arbitration has been lost, provisions for reattempting the transmission should be taken. If arbitration is lost, there is the possibility that the controller is being addressed as a Slave. If this condition is to be recognized, we must test on the 'AAS' bit (bit 2). A 'General Call' address (00H) has also been defined as an 'all-call' address for all slaves; bit 1, AD0, must be tested if this feature is to be recognized by a Master.

After a successful address transfer/acknowledge, the slave is ready to be sent its data. The instruction MOV SO,A will now automatically send the contents of the accumulator out on the bus. After calling the ACKWT routine once more, we are ready to terminate the transfer. The Stop condition is created by the instruction 'MOV S1, #0D8H'. This resets the bus-busy bit, which tells the hardware to generate a Stop — the data line makes a low-to-high transition while the clock remains high. All bus-busy flags on other masters on the bus are reset by this signal.

The transfer is now complete — PCF8574 I/O Expandor will transfer the serial data stream to its 8 output pins and latch them until further update.

```
ACKWT:  MOV A,S1        ;Get bus status word
                        ;from S1.
        JB4 ACKWT       ;Poll the PIN bit
                        ;until it goes low
                        ;indicating transfer
                        ;completed
        JBO BUSERR      ;Jump to BUSERR
                        ;routine if acknowledge
                        ;not received.
        RET             ;transfer complete,
                        ;acknowledge received - return.
```

Figure 4

MASTER READS ONE BYTE FROM SLAVE

A read operation is a similar process; the address, however, will be 41H, the LSB indicating to the I/O device that a read is to be performed. During the data portion of a read, the I/O port 8574 will transmit the contents of its latches in response to the clock generated by the master. The Master/Receiver in this case generates a low-level acknowledge on reception of each byte (a 'positive' acknowledge). Upon completion of a read, the master must generate a 'negative' acknowledge during the ninth clock to indicate to the slaves that the read operation is finished. This is necessary because an arbitrary number of bytes may be read within the same transfer. A negative acknowledge consists of a high signal on the data line during the ninth clock of the last byte to be read. To accomplish this, the master 8400 must leave the acknowledge mode just before the final byte, read the final byte (producing only 8 clock pulses), program the bit-counter with 001 (preparing for a one-bit negative acknowledge pulse), and simply move the contents of S0 to the accumulator. This final instruction accomplishes two things simultaneously: it transfers the final byte to the accumulator and produces one clock pulse on the SCL line. The structure of the serial I/O register S0 is such that a read from it causes a double-buffered transfer from the I^2C bus to S0, while the original contents of S0 are transferred to the accumulator. Because the number of clocks produced on the bus is determined by the control number in the Bit Counter, by presetting it to 001, only one clock is generated. At this point in time the slave is still waiting for an acknowledge; the bus is high due to the pull-up, as single clock pulse in this condition is interpreted as a 'negative' acknowledge. The slave has now been informed that reading is completed; a Stop condition is now generated as before. The read process (one byte from a slave with only a chip address) is shown in Figure 5.

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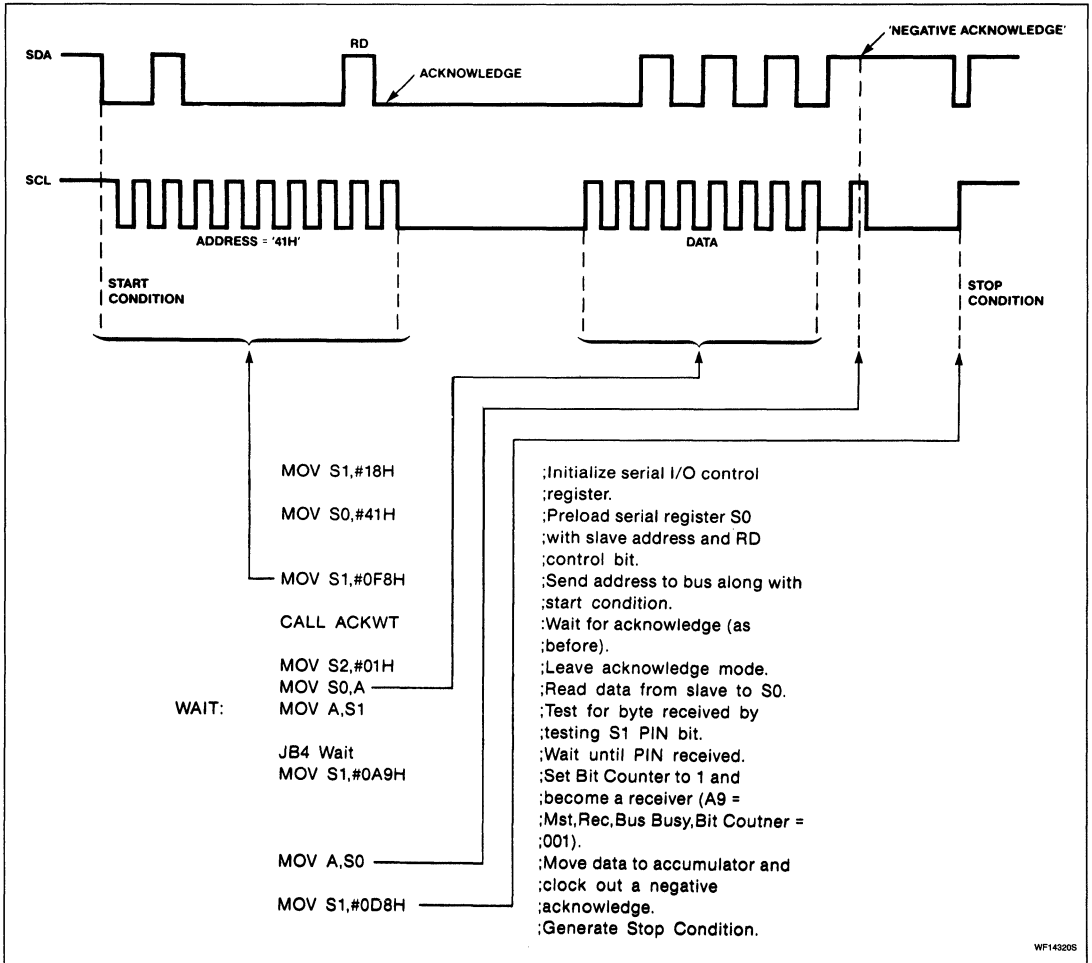

Figure 5

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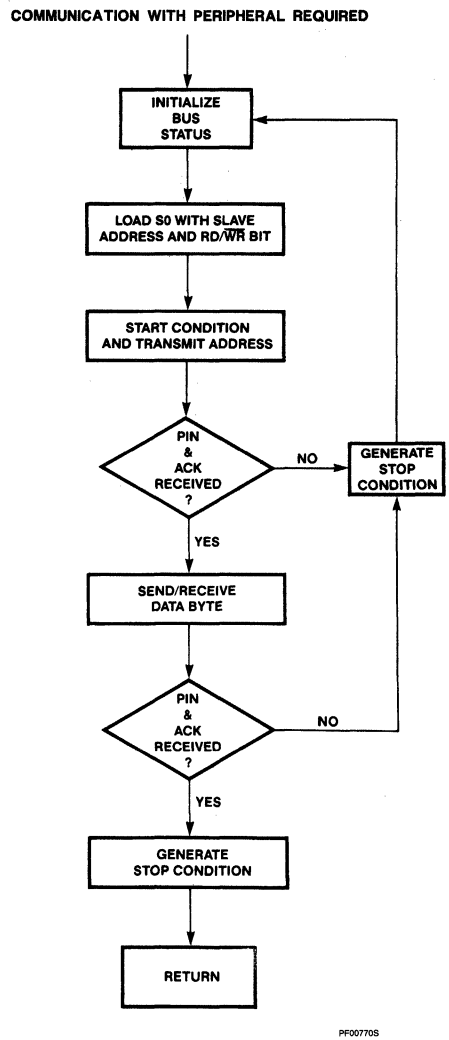

Figure 6. Flowchart for Reading/Writing One Byte to an I^2C Peripheral; Single-Master, Single-Address Slave

```
        MOV S1, #18H      ;Initialize bus-status register
                          ;Master, Transmitter,
                          ;Bus-not-Busy, Enable SIO.
        MOV S0, #0A0H     ;Load S0 with RAM's chip
                          ;address.
        MOV S1, #0F8H     ;Start cond. and transmit
                          ;address.
        CALL ACKWT        ;Wait until address received.
        MOV A,#00H        ;Set up for transmitting RAM
                          ;location address.
        MOV S0,A          ;Transmit first RAM address.
        CALL ACKWT        ;Wait.
        MOV S1, #18H      ;Set up for a repeated Start
                          ;condition.
        MOV A,#0A1H       ;Get RAM chip address & RD bit.
        MOV S0,A          ;Send out to bus
        MOV S1,#0F8H      ;preceded by repeated Start.

        CALL ACKWT        ;Wait.
        MOV A,S0          ;First data byte to S0.
        CALL ACKWT        ;Wait.
        MOV A,S0          ;Second data byte to S0.
                          ;And First data byte to Acc.
        CALL ACKWT        ;Wait.
        MOV R0,A          ;Save first byte in R0.
        MOV A,S0          ;Third data byte to S0
                          ;and second data byte to Acc.
        CALL ACKWT        ;Wait.
        MOV R1,A          ;Save second data byte
                          ;in R1.
        MOV S2,#01H       ;Leave ack. mode.
                          ;Bit Counter=001 for neg ack.
        MOV A,S0          ;Third data byte to acc
                          ;negative ack. generated.
        MOV R2,A          ;Save third data byte in R2.
WAIT1:  MOV A,S1          ;Get bus status.
        JB4 WAIT1         ;Wait until transfer complete.
        MOV S1,#0D8H      ;Stop condition.
        MOV S2,#41H       ;Restore acknowledge mode.
```

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Figure 7

These examples apply to a slave with a chip address — more than one byte can be written/read within the same transfer; however, this option is more applicable to I^2C devices with sub-addresses such as the static RAMs or Clock/Calendar. In the case of these types of devices, a slightly different protocol is used. The RAM, for example, requires a chip address and an internal memory location before it can deliver or accept a byte of information. During a write operation, this is done by simply writing the secondary address right after the chip address — the peripheral is designed to interpret the second byte as an internal address. In the case of a Read operation, the slave peripheral must send data back to the Master after it has been addressed and sub-addressed. To accomplish this, first the Start, Address, and Sub-address is transmitted. Then we have a **repeated** start condition to reverse the direction of the data transfer, followed by the chip address and RD, then a data string (w/ acknowledges). This repeated Start does not affect other peripherals — they have been deactivated and will not reactivate until a Stop condition is detected. I^2C peripherals are equipped with auto-incrementing logic which will automatically transmit or receive data in consecutive (increasing) locations. For example, to read 3 consecutive bytes to PCB8571 RAM locations 00, 01 and 02, we use the following format as shown in Figure 7.

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This routine reads the contents of location 00, 01 and 02 of the PCB8571 128-byte RAM and puts them in registers R0, R1, and R2. The auto-incrementing feature allows the programmer to indicate only a starting location, then read an arbitrary block of consecutive memory addresses. The WAIT 1 loop is required to poll for the completion of the final byte because the ACKWT routine will not recognize the negative acknowledge as a valid condition.

BUS ERROR CONDITIONS: ACKNOWLEDGE NOT RECEIVED

In the above routines, should a slave fail to acknowledge, the condition is detected during the 'ACKWT' routine. The occurrence may indicate one of two conditions: the slave has failed to operate, or a bus disturbance has occurred. The software response to either event is dependent on the system application. In either case, the 'BusErr' routine should reinitialize the bus by issuing a 'Stop' condition. Provision may then be taken to repeat the transfer an arbitrary number of times. Should the symptom persist, either an error condition will be entered, or a backup device can be activated.

These sample routines represent single-master systems. A more detailed analysis of multi-master/noisy environment systems will be treated in further application notes. Examples of more complex systems can be found in the 'Software Examples' manual; publication 9398 615 70011.

The Inter-Integrated Circuit (I^2C) Serial Bus: Theory and Practical Consideration

AN168

APPENDIX A

Only the 8048 assembler is capable of assembling MAB8400 source code when it has at least a "DATA" or "Define Byte" assembler directive, possibly in combination with a MACRO facility.

The new instructions can be simply defined by MACROs. The instructions which are not in the MAB8400 should not be in the MAB8400 source program.

An example of a macro definitions list is given here for the Intel Macro Assembler.

This list can be copied in front of a MAB8400 source program; the new instructions are added to the MAB8400 source program by calling the MACRO via its name in the op-code field and (if required) followed by an operand in the operand field.

MACRO DEFINITIONS

LINE	SOURCE STATEMENT		
1	$MACROFILE		
2	;MACROS FOR 8048 ASSEMBLER RECOGNITION		
3	;OF 8400 COMMANDS		
4	MOVS0A	MACRO	;MOV S0,A
5	DB 3CH		
6	ENDM		
7	MOVAS0	MACRO	;MOV A,S0
8	DB 0CH		
9	ENDM		
10	MOVS1A	MACRO	;MOV S1,A
11	DB 3DH		
12	ENDM		
13	MOVAS1	MACRO	;MOV A,S1
14	DB 0DH		
15	ENDM		
16	MOVS2A	MACRO	;MOV S2,A
17	DB 3EH		
18	ENDM		
19	MOVS0	MACRO L	;MOV S0,#DATA
20	DB 9CH,L		
21	ENDM		
22	MOVS1	MACRO L	;MOV S1,#DATA
23	DB 9DH,L		
24	ENDM		
25	MOVS2	MACRO L	;MOV S2,#DATA
26	DB 9EH,L		
27	ENDM		
28	ENSI	MACRO	;EN SI
29	DB 85H		
30	ENDM		
31	DISSI	MACRO	;DIS SI (Disable serial interrupt)
32	DB	95H	
33	ENDM		
34;			
35;	PORT 0 INSTRUCTIONS:		
36;	INAP0	MACRO	;IN A,P0
37	DB	08H	
38	ENDM		
39;			
40	OUTP0A	MACRO	;OUTL P0,A
41	DB	38H	
42	ENDM		
43;			
44	ORLP0	MACRO L	;ORL P0,#DATA
45	DB	88H,L	
46	ENDM		
47;			
48	ANLP0	MACRO L	;ANL P0,#DATA
49	DB	98H,L	
50	ENDM		
51;			

MACRO DEFINITIONS (Continued)

```
LINE    SOURCE STATEMENT
  52; DATA MEMORY INSTRUCTIONS:
  53                DECARO    MACRO       ;DEC @R0
  54                DB        0C0H
  55                ENDM
  56;
  57                DECAR1    MACRO       ;DEC @R1
  58                DB        OC1H
  59                ENDM
  60;
  61; SELECT MEMORY BANK INSTRUCTIONS:
  62                SELMB2    MACRO       ;SEL MB2
  63                DB        0A5H
  64                ENDM
  65;
  66                SELMB3    MACRO       ;SEL MB3
  67                DB        0B5H
  68                ENDM
  69;
  70; CONDITIONAL JUMP INSTRUCTIONS:
  71                DJNZA0    MACRO L     ;DJNZ @R0,ADDR
  72                DB        0E0H,L AND 0FFH
  73                ENDM
  74;
  75                DJNZA1    MACRO L     ;DJNZ @R1,ADDR
  76                DB        0E1H,L AND 0FFH
  77                ENDM
  78;
  79                JNTF      MACRO L     ;JUMP IF TIMERFLAG IS
                                          NON ZERO
  80                DB        06H,L AND 0FFH
  81                ENDM
  82
  83; END OF MACRO DEFINITIONS
```

THE 8400 INSTRUCTIONS BUILT FROM THE MACRO LIST

LOC/OBJ	LINE	SOURCE STATEMENT		
0000	1	ORG 0		
	2	MOVAS0		;MACRO for MOV A,S0
0000 0C	3 +	DB	0CH	
	4	MOVAS1		;MACRO for MOV A,S1
0001 0D	5 +	DB	0DH	
	6	MOVS0A		;MACRO for MOV S0,A
0002 3C	7 +	DB	3CH	
	8	MOVS1A		;MACRO For MOV S1,A
0003 3D	9 +	DB	3DH	
	10	MOVS2A		;MACRO For MOV S2,A
0004 3E	11 +	DB	3EH	
	12	MOVS0	56H	;MACRO For MOV S0, #56H
0005 9C	13 +	DB	9CH,56H	
0006 56				
	14	MOVS1	9FH	;MACRO for MOV S1, #9FH
0007 9D	15 +	DB	9DH,9FH	
0008 9F				
	16	MOVS2	0E8H	;MACRO for MOV S2, #0E8H
0009 9E	17 +	DB	9EH,0E8H	
000A E8				
	18	ENS1		;MACRO for EN S1
000B 85	19 +	DB	85H	
	20	DISSI		;MACRO for DIS SI
000C 95	21 +	DB	95H	
	22	INAP0		;MACRO for IN A,P0
000D 08	23 +	DB	08H	
	24	OUTP0A		;MACRO for OUTL P0,A
000E 38	25 +	DB	38H	
	26	ORLP0	5AH	;MACRO for ORL P0,A
000F 88	27 +	DB	88H,5AH	
0010 5A				
	28	ANLP0	2FH	;MACRO for ANL P0,A
0011 98	29 +	DB	98H,2FH	
0012 2F				
	30	DECAR0		;MACRO for DEC @R0
0013 C0	31 +	DB	0C0H	
	32	DECAR1		;MACRO for DEC @R1
0014 C1	33 +	DB	0C1H	
	34	SELMB2		;MACRO for SEL MB2
0015 A5	35 +	DB	0A5H	
	36	SELMB3		;MACRO for SEL MB3
0016 B5	37 +	DB	0B5H	
	38	DJNZA0	567H	;MACRO for DJNZ @R0, 567H
0017 E0	39 +	DB	0E0H,567H AND 0FFH	
0019 67				
	40	DJNZA1	0EFEH	;MACRO for DJNZ @R1, 0EFEH
0019 E1	41 +	DB	0E1H,0EFEH AND 0FFH	
001A FE				
	42	JNTF	789H	;MACRO for JNTF 789H
001B 06	43 +	DB	06H, 789H AND 0FFH	
001C 89				
	44	END		

Signetics

Linear Products

Section 4
Tuning Systems

4

INDEX

PCF8570
256 × 8 Static RAM

Product Specification

Linear Products

DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins — A0, A1, and A2 — are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

FEATURES

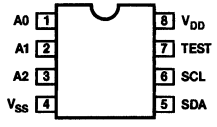
- **Operating supply voltage: 2.5V to 6V**
- **Low data retention voltage: min. 1.0V**
- **Low standby current: max. 5μA**
- **Power saving mode: typ. 50nA**
- **Serial input/output bus (I^2C)**
- **Address by 3 hardware address pins**
- **Automatic word address incrementing**
- **8-lead DIP package**

APPLICATIONS

- **Telephony RAM expansion for stored numbers in repertory dialing (e.g., PCD3343 applications)**
- **Radio and television channel presets**
- **Video cassette recorder**
- **General purpose RAM expansion for the microcomputer families MAB8400 and PCF84C00**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD11900S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address inputs
2	A1	
3	A2	
4	V_{SS}	Negative supply
5	SDA	Serial data line (I^2C bus)
6	SCL	Serial clock line (I^2C bus)
7	TEST	Test input for test speed-up; must be connected to V_{SS} when not in use. (Power saving mode, see Figures 12 and 13)
8	V_{DD}	Positive supply

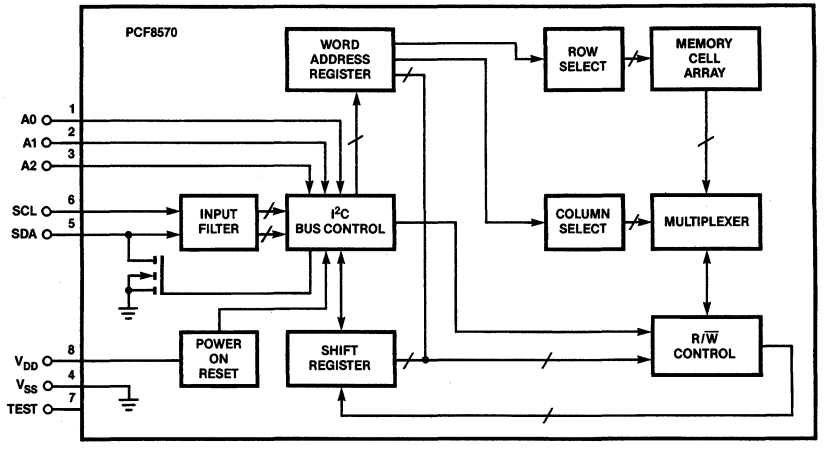
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−40°C to +85°C	PCF8570PN
8-Pin Plastic SO (SO-8L; SOT-176)	−40°C to +85°C	PCF8570TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 8)	−0.8 to +8.0	V
V_I	Voltage range on any input	−0.8 to V_{DD} +0.8	V
$\pm I_I$	DC input current (any input)	10	mA
$\pm I_O$	DC output current (any output)	10	mA
$\pm I_{DD}$; I_{SS}	Supply current (Pin 4 or Pin 8)	50	mA
P_{TOT}	Power dissipation per package	300	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 6V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage	2.5		6	V
	Supply current at f_{SCL} = 100kHz; $V_I = V_{SS}$ or V_{DD}				
I_{DD}	operating			200	μA
I_{DDO}	standby			15	μA
I_{DDO}	standby at T_A = −25 to +70°C			5	μA
V_{POR}	Power-on reset voltage level[1]	1.5	1.9	2.3	V
Input SCL; input/output SDA					
V_{IL}	Input voltage LOW[2]	−0.8		$0.3 \times V_{DD}$	V
V_{IH}	Input voltage HIGH[2]	$0.7 \times V_{DD}$		$V_{DD} + 0.8$	V
I_{OL}	Output current LOW at V_{OL} = 0.4V	3			mA
I_{OH}	Output leakage current HIGH at $V_{OH} = V_{DD}$			250	nA
$\pm I_I$	Input leakage current (A0, A1, A2) at $V_I = V_{DD}$ or V_{SS}			250	nA
f_{SCL}	Clock frequency (Figure 5)	0		100	kHz
C_I	Input capacitance (SCL, SDA) at $V_I = V_{SS}$			7	pF
t_{SW}	Tolerable spike width on bus			100	ns
LOW V_{DD} data retention					
V_{DDR}	Supply voltage for data retention	1		6	V
I_{DDR}	Supply current at V_{DDR} = 1V			5	μA
I_{DDR}	Supply current at V_{DDR} = 1V; T_A = −25 to +70°C			2	μA
Power saving mode					
I_{DDR}	Supply current at T_A = 25°C; TEST = V_{DDR}		50	400	nA

NOTES:

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ±0.5mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

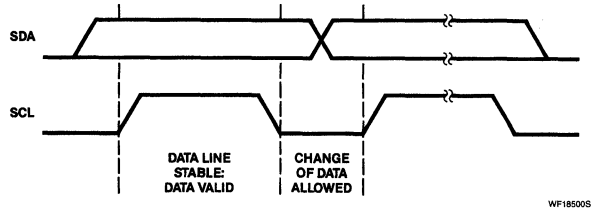


Figure 1. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

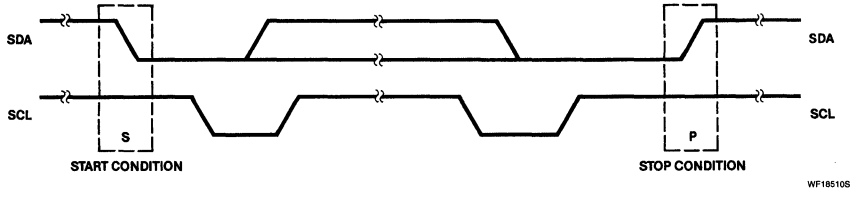


Figure 2. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

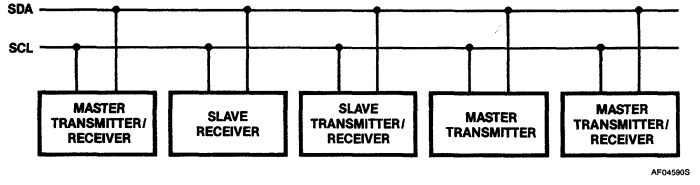


Figure 3. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW. During the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

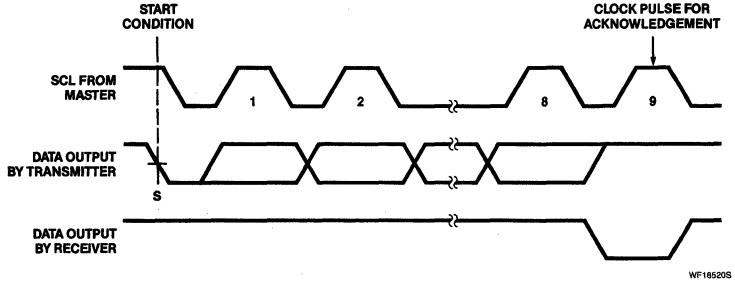


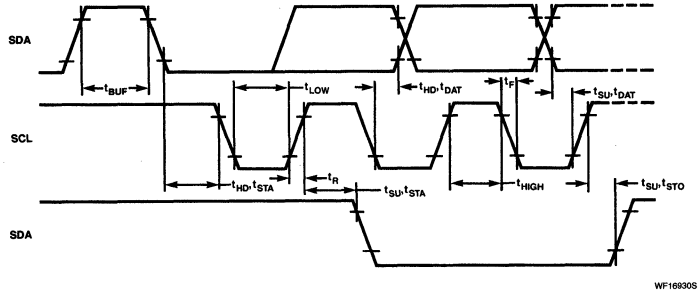
Figure 4. Acknowledge on the I^2C Bus

Timing Specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-Speed Mode

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 5.

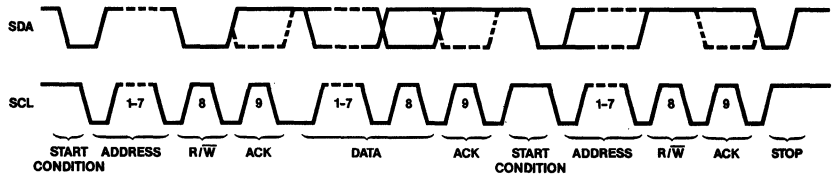


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
$t_{LOWSmin}$	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
$t_{SU;STA}$	$t \geq t_{LOWmin}$	Start condition set-up time; only valid for repeated start code
$t_{HD;DAT}$	$t = 0\mu s$	Data hold time
$t_{SU;DAT}$	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 5. Timing of the High-Speed Mode



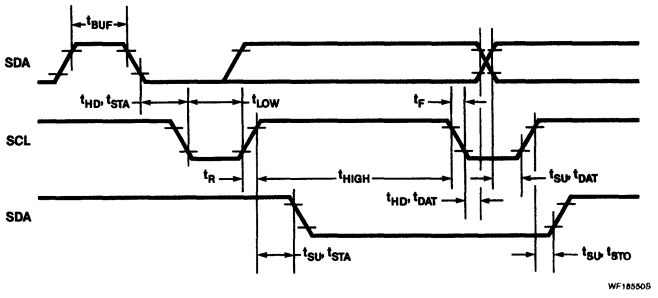
Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 6. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode

Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 7.



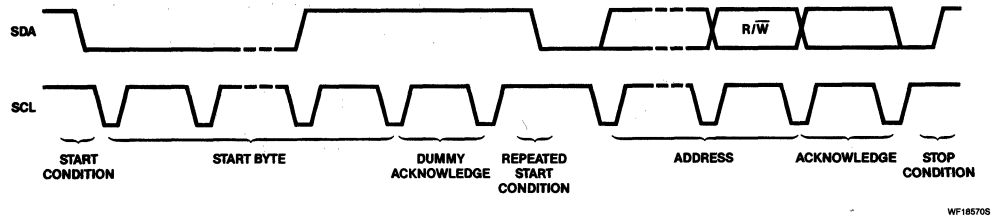
Where:

t_{BUF}	$t \geq 105\mu s$ (t_{LOWmin})
t_{HD}, t_{STA}	$t \geq 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25μs
t_{HIGH}	390 μs ± 25μs
t_{SU}, t_{STA}	130μs ± 25μs*
t_{HD}, t_{DAT}	$t \geq 0\mu s$
t_{SU}, t_{DAT}	$t \geq 250ns$
t_R	$t \leq 1\mu s$
t_F	$t \leq 300ns$
t_{SU}, t_{STO}	130μs ± 25μs

NOTES:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.
For definitions see high-speed mode.

*Only valid for repeated start code.

Figure 7. Timing of the Low-Speed Mode



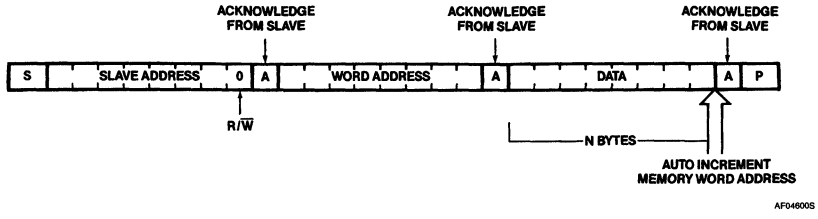
Where:

Clock t_{LOWmin}	130μs ± 25μs
$t_{HIGHmin}$	390μs ± 25μs
Mark-to-space ratio	1:3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	Not allowed
Acknowledge clock bit	Must be provided by master

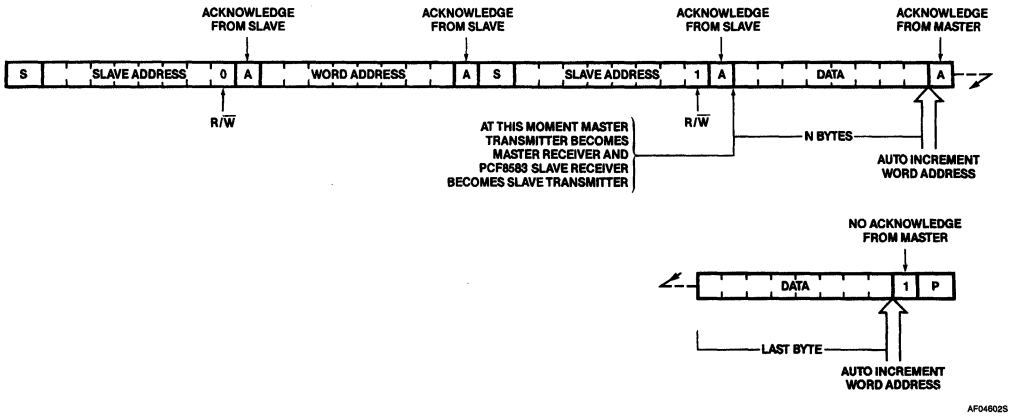
Figure 8. Complete Data Transfer in Low-Speed Mode

Bus Protocol

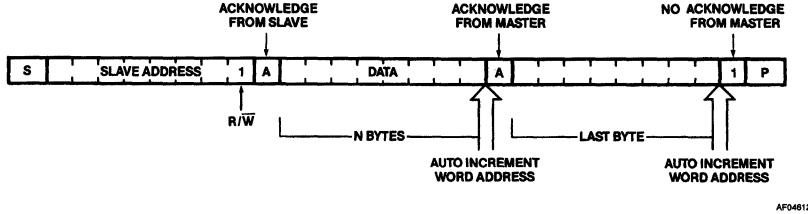
Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I^2C bus configuration for different PCF8570 READ and WRITE cycles is shown in Figure 9.



a. Master Transmits to Slave Receiver (WRITE Mode)



b. Master Reads After Setting Word Address (WRITE Word Address; READ Data)

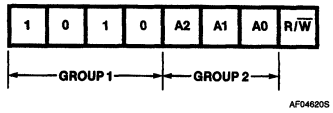


c. Master Reads Slave Immediately After First Byte (READ Mode)

Figure 9

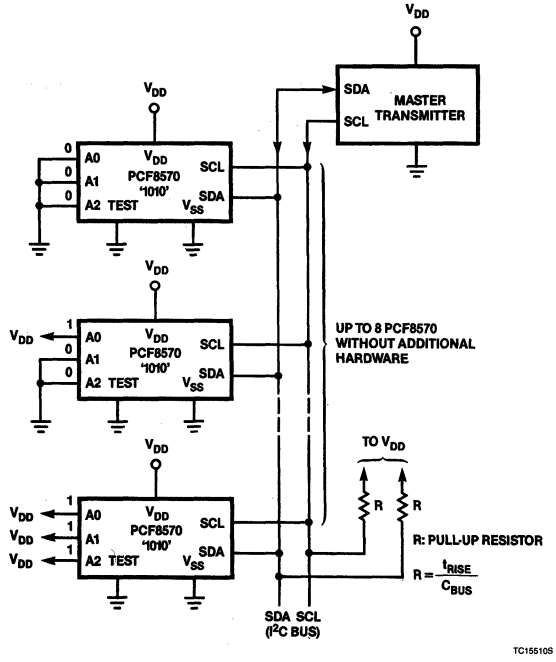
APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Figure 10.)



NOTE:
PCF8570A version: the slave address A0 state is X (don't care); however, the hardware address A0 input must still be connected to V_{SS} or V_{DD}.

Figure 10. PCF8570 Address



NOTE:
A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

Figure 11. PCF8570 Application Diagram

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8570 goes into the power saving mode.

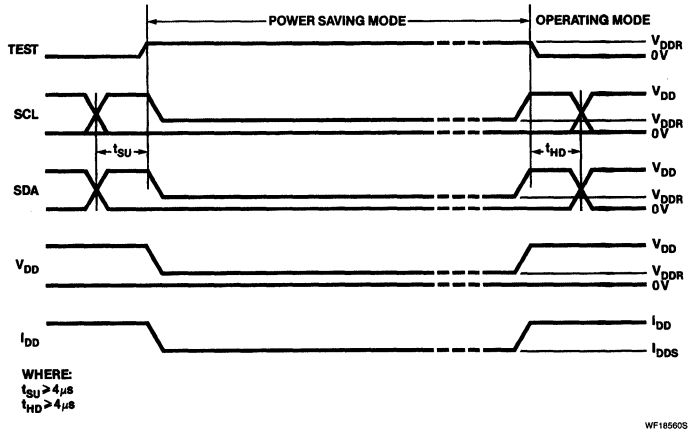
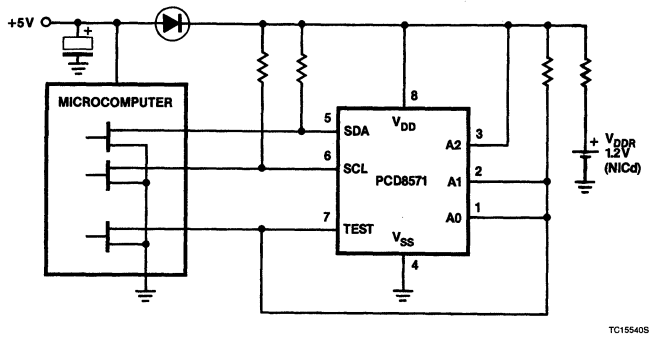


Figure 12. Timing for Power Saving Mode



NOTE:
1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.

Figure 13. Application Example for Power Saving Mode

PCF8571
1K Serial RAM

Product Specification

Linear Products

DESCRIPTION

The PCF8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins — A0, A1, and A2 — are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

FEATURES

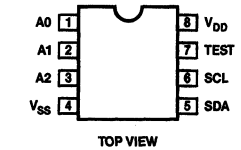
- **Operating supply voltage: 2.5V to 6V**
- **Low data retention voltage: min. 1.0V**
- **Low standby current: max. 5μA**
- **Power saving mode: typ. 50nA**
- **Serial input/output bus (I^2C)**
- **Address by 3 hardware address pins**
- **Automatic word address incrementing**
- **8-lead DIP package**

APPLICATIONS

- **Telephony RAM expansion for stored numbers in repertory dialing (e.g., PCD3340 applications)**
- **Radio and television channel presets**
- **Video cassette recorder**
- **General purpose RAM expansion for the micro-computer families MAB8400 and PCF84C00**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD11900S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address inputs
2	A1	
3	A2	
4	V_{SS}	Negative supply
5	SDA	Serial data line (I^2C bus)
6	SCL	Serial clock line (I^2C bus)
7	TEST	Test input for test speed-up; must be connected to V_{SS} when not in use. (Power saving mode, see Figures 12 and 13)
8	V_{DD}	Positive supply

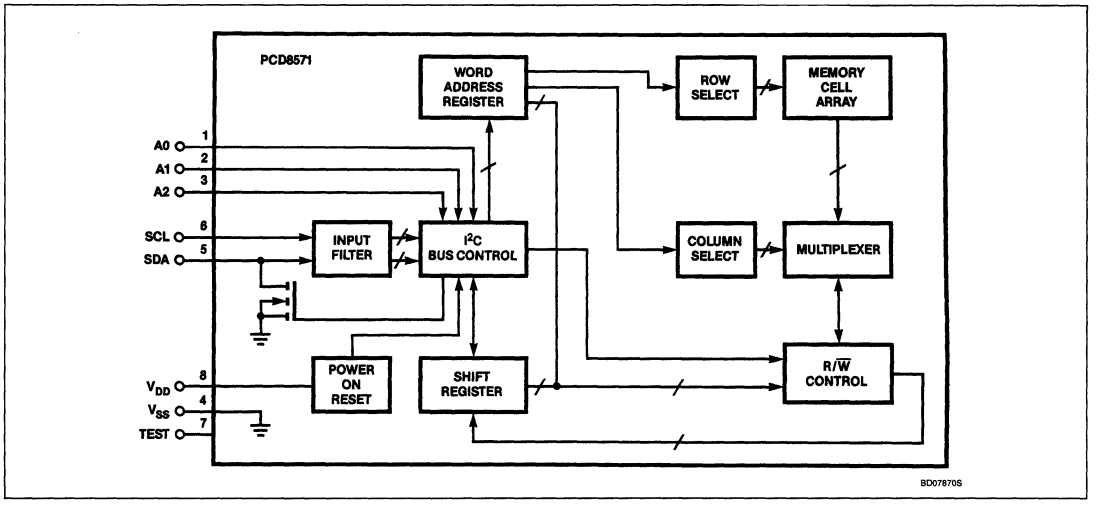
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−25°C to +70°C	PCF8571PN
8-Pin Plastic SO (VSO-8; SOT-176)	−25°C to +70°C	PCF8571TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 8)	−0.8 to +8.0	V
V_I	Voltage range on any input	−0.8 to V_{DD} +0.8	V
$\pm I_I$	DC input current (any input)	10	mA
$\pm I_O$	DC output current (any output)	10	mA
$\pm I_{DD}$; I_{SS}	Supply current (Pin 4 or Pin 8)	50	mA
P_{TOT}	Power dissipation per package	300	mW
P_O	Power dissipation per output	50	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 6V; V_{SS} = 0V; T_A = −25°C to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage	2.5		6	V
	Supply current at f_{SCL} = 100kHz; $V_I = V_{SS}$ or V_{DD}				
I_{DD}	operating			200	μA
I_{DDO}	standby			5	μA
V_{POR}	Power-on reset voltage level at $V_{SCL} = V_{SDA} = V_{DD}$ [1]	1.5	1.9	2.3	V
Input SCL; input/output SDA					
V_{IL}	Input voltage LOW[2]	−0.8		0.3 × V_{DD}	V
V_{IH}	Input voltage HIGH[2]	0.7 × V_{DD}		V_{DD} + 0.8	V
I_{OL}	Output current LOW at V_{OL} = 0.4V	3			mA
I_{OH}	Output leakage current HIGH at $V_{OH} = V_{DD}$			100	nA
$\pm I_I$	Input leakage current (A0, A1, A2) at $V_I = V_{DD}$ or V_{SS}			100	nA
f_{SCL}	Clock frequency (Figure 5)	0		100	kHz
C_I	Input capacitance (SCL, SDA) at $V_I = V_{SS}$			7	pF
t_{SW}	Tolerable spike width on bus			100	ns
LOW V_{DD} data retention					
V_{DDR}	Supply voltage for data retention	1			V
I_{DDR}	Supply current at V_{DDR} = 1V			2	μA
Power saving mode (Figure 12)					
I_{DDS}	Supply current at T_A = 25°C; TEST = A0 = A1 = A2 = V_{DDR}		50	200	nA

NOTES:
1. The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ±0.5mA.

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

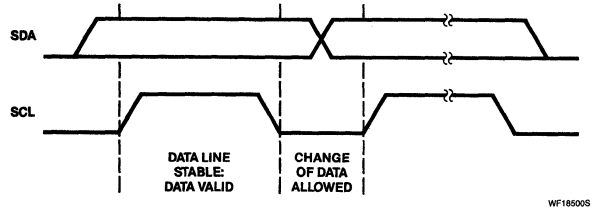


Figure 1. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

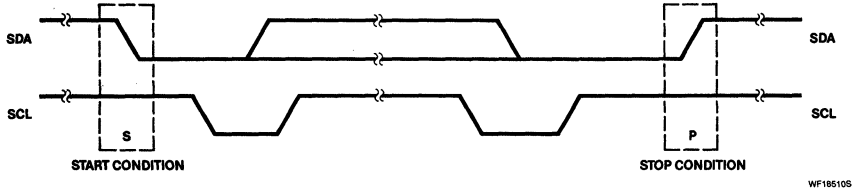


Figure 2. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

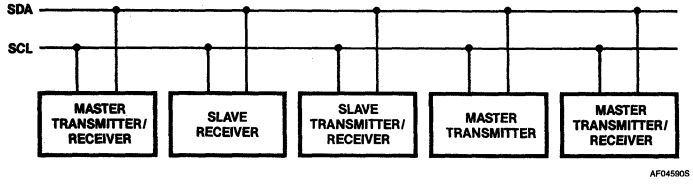


Figure 3. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW. During the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end-of-data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

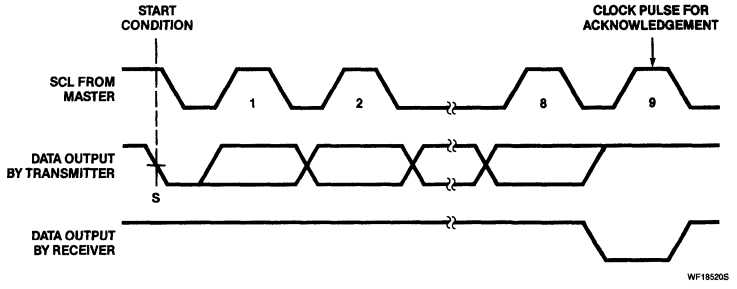


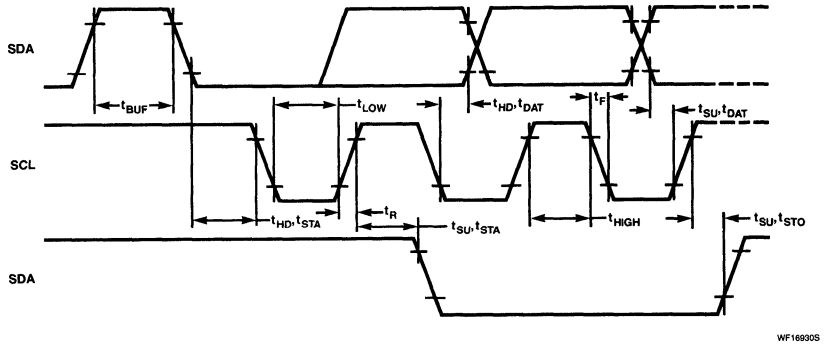
Figure 4. Acknowledgement on the I^2C Bus

Timing Specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8571 operates in both modes and the timing requirements are as follows:

High-Speed Mode

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 5.

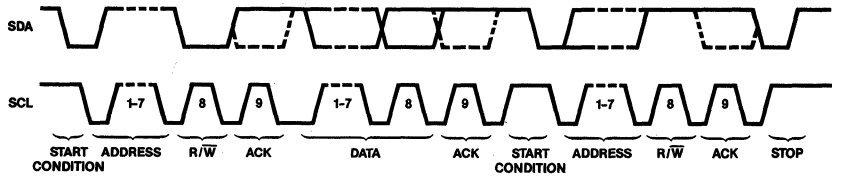


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
t_{HD}, t_{STA}	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
t_{SU}, t_{STA}	$t \geq t_{LOWmin}$	Start condition setup time; only valid for repeated start code
t_{HD}, t_{DAT}	$t \geq 0\mu s$	Data hold time
t_{SU}, t_{DAT}	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
t_{SU}, t_{STO}	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 5. Timing of the High-Speed Mode



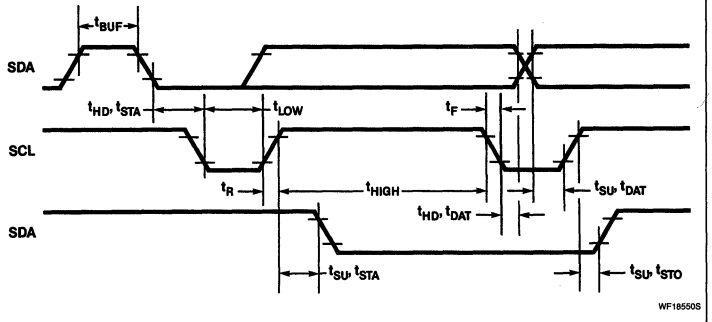
Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 6. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode

Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 7.

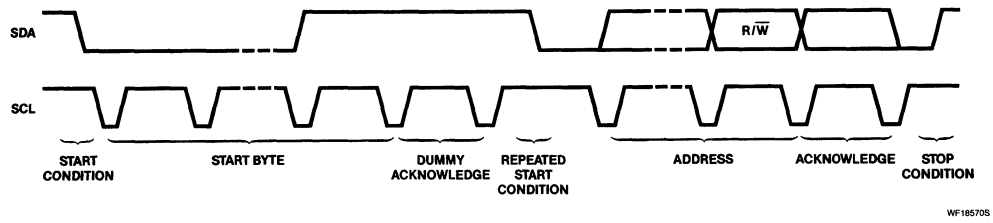


Where:

t_{BUF}	$t \geqslant 105\mu s$ (t_{LOWmin})
t_{HD}, t_{STA}	$t \geqslant 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	130μs ± 25μs
t_{HIGH}	390μs ± 25μs
t_{SU}, t_{STA}	130μs ± 25μs*
t_{HD}, t_{DAT}	$t \geqslant 0\mu s$
t_{SU}, t_{DAT}	$t \geqslant 250ns$
t_R	$t \leqslant 1\mu s$
t_F	$t \leqslant 300ns$
t_{SU}, t_{STO}	130μs ± 25μs

NOTES:
All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.
For definitions see high-speed mode.
*Only valid for repeated start code.

Figure 7. Timing of the Low-Speed Mode



Where:

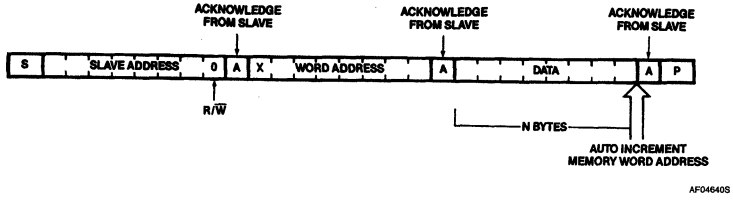
Clock t_{LOWmin}	130μs ± 25μs
$t_{HIGHmin}$	390μs ± 25μs
Mark-to-space ratio	1:3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	Not allowed
Acknowledge clock bit	Must be provided by master

Figure 8. Complete Data Transfer in the Low-Speed Mode

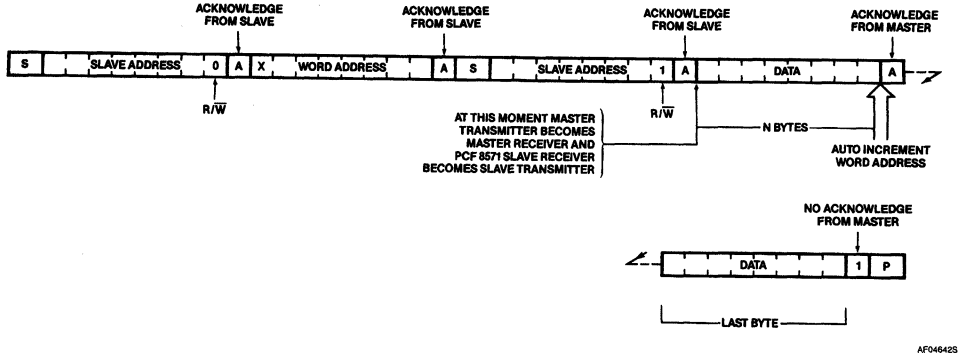
4

Bus Protocol

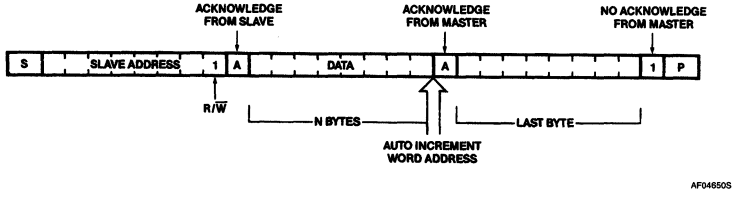
Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I^2C bus configuration for different PCF8571 READ and WRITE cycles is shown in Figure 9.



a. Master Transmits to Slave Receiver (WRITE mode)



b. Master Reads After Setting Word Address (WRITE Word Address; READ Data)



c. Master Reads Slave Immediately After First Byte (READ Mode)

NOTE:
X = don't care bit

Figure 9

APPLICATION INFORMATION

The PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Figure 10).

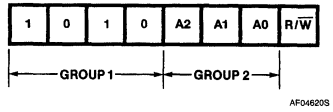
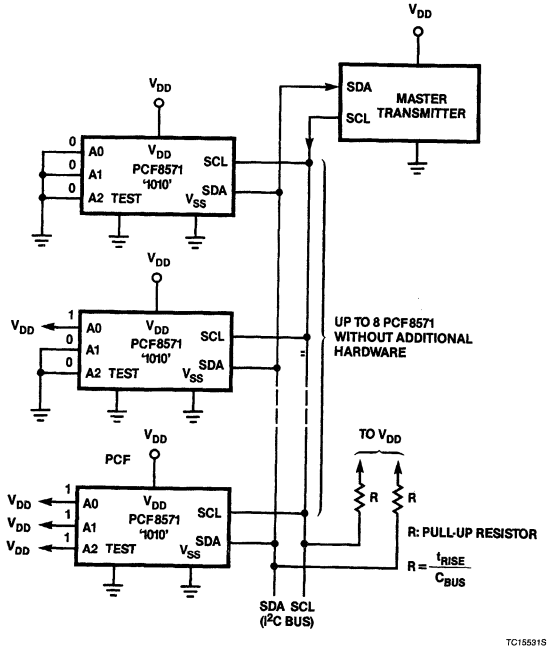


Figure 10. PCF8571 Address

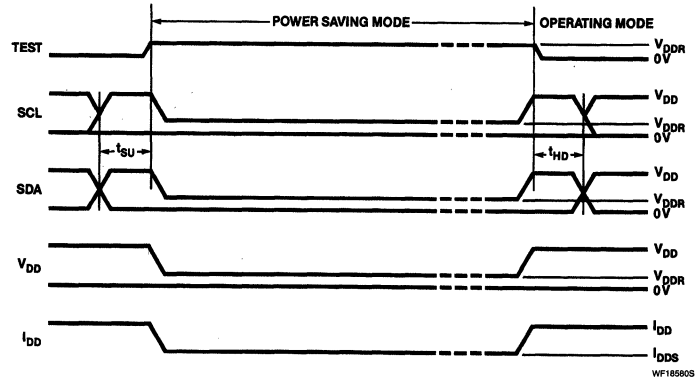


NOTES:
A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

Figure 11. PCF8571 Application Diagram

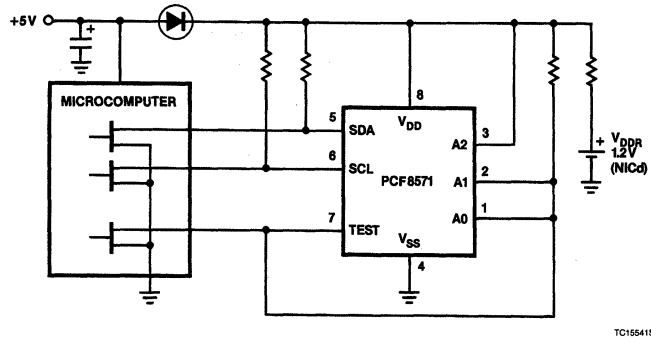
POWER SAVING MODE

With the condition TEST = A2 = A1 = A0 = V_{DDR}, the PCF8571 goes into the power saving mode.



Where:
$t_{SU} \geq 4\mu s$
$t_{HD} \geq 4\mu s$

Figure 12. Timing for Power Saving Mode



NOTES:
1. In the operating mode, TEST = 0 (A0, A1, = 0; A2 = 1).
2. In the power saving mode, TEST = A0 = A1 = A2 = V_{DDR}.

Figure 13. Application Example for Power Saving Mode

PCF8573
Clock/Calendar With Serial I/O

Product Specification

Linear Products

DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real-time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two-lin bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2V nickel cadmium battery. The time base is generated from a 32.768kHz crystal-controlled oscillator.

FEATURES

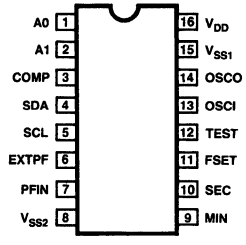
- **Serial input/output bus (I^2C) interface for minutes, hours, days and months**
- **Additional pulse outputs for seconds and minutes**
- **Alarm register for presetting a time for alarm or remote switching functions**
- **Battery back-up for clock function during supply interruption**
- **Crystal oscillator control (32.768kHz)**

APPLICATIONS

- **Automotive**
- **Telephony**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD10281S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address input
2	A1	Address input
3	COMP	Comparator output
4	SDA	Serial data line } I^2C bus
5	SCL	Serial clock line } I^2C bus
6	EXTPF	Enable power fail flag input
7	PFIN	Power fail flag input
8	V_{SS2}	Negative supply 2 (I^2C interface)
9	MIN	One pulse per minute output
10	SEC	One pulse per second output
11	FSET	Oscillator tuning output
12	TEST	Test input; must be connected to V_{SS2} when not in use
13	OSCI	Oscillator input
14	OSCO	Oscillator input/output
15	V_{SS1}	Negative supply 1 (clock)
16	V_{DD}	Common positive supply

ORDERING INFORMATION

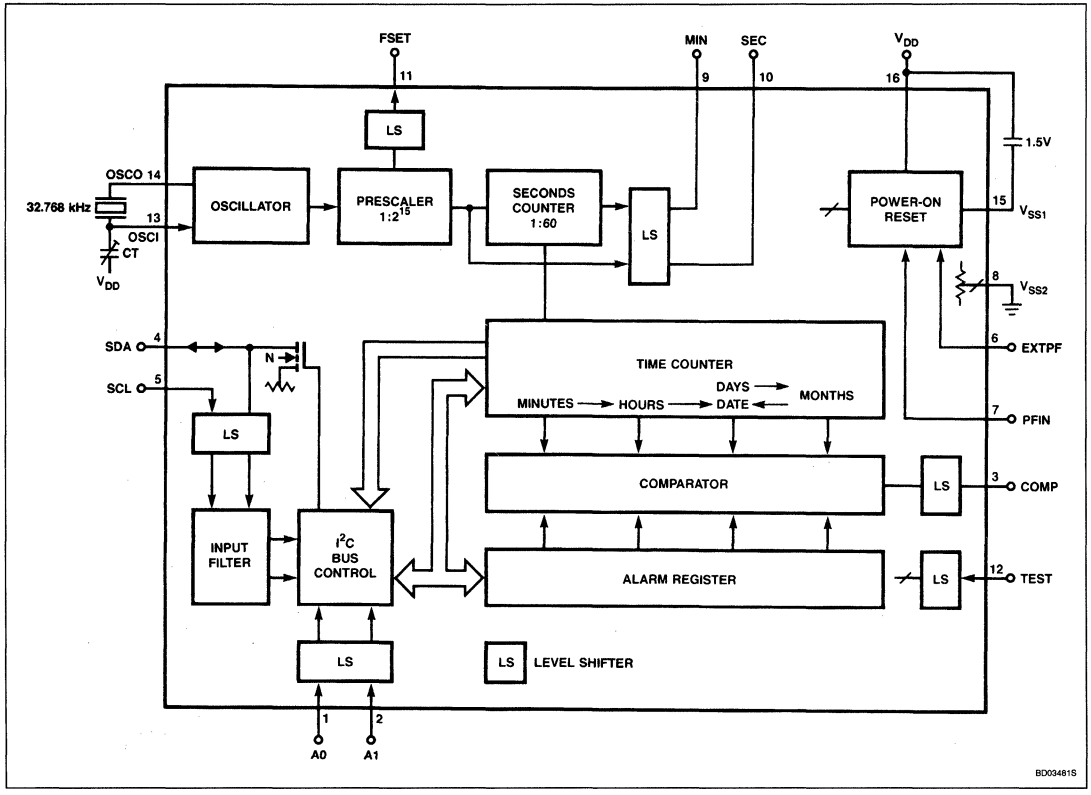
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to +85°C	PCF8573PN
16-Pin Plastic SOL (SOT-162A)	−40°C to +85°C	PCF8573T

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (clock)	−0.3 to 8	V
V_{SS2}	Supply voltage range (I^2C interface)	−0.3 to 8	V
I_{IN}	Input current	10	mA
I_{OUT}	Output current	10	mA
P_D	Maximum power dissipation per package	200	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

Clock/Calendar With Serial I/O PCF8573

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{SS2} = 0V; T_A = −40 to + 85°C, unless otherwise specified. Typical values at T_A = + 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
$V_{DD} - V_{SS2}$	Supply voltage (I^2C interface)	2.5	5	6.0	V
$V_{DD} - V_{SS1}$	Supply voltage (clock)	1.1	1.5	$(V_{DD} - V_{SS2})$	V
	Supply current V_{SS1}				
$-I_{SS1}$	at $V_{DD} - V_{SS1}$ = 1.5V		3	10	μA
$-I_{SS1}$	at $V_{DD} - V_{SS1}$ = 5V		12	50	μA
	Supply current V_{SS2}				
	at $V_{DD} - V_{SS2}$ = 5V				
$-I_{SS2}$	(I_O = 0mA on all outputs)			50	μA
Inputs SCL, SDA, A0, A1, TEST					
V_{IH}	Input voltage HIGH	0.7 × V_{DD}			V
V_{IL}	Input voltage LOW			0.3 × V_{DD}	V
	Input leakage current				
$\pm I_I$	at $V_I = V_{SS2}$ to V_{DD}			1	μA
Inputs EXTPF, PFIN					
$V_{IH} - V_{SS1}$	Input voltage HIGH	0.7 × $(V_{DD} - V_{SS1})$			V
$V_{IL} - V_{SS1}$	Input voltage LOW	0		0.3 × $(V_{DD} - V_{SS1})$	V
	Input leakage current				
$\pm I_I$	at $V_I = V_{SS1}$ to V_{DD}			1	μA
	at T_A = 25°C;				
$\pm I_I$	$V_I = V_{SS1}$ to V_{DD}			0.1	μA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
	Output voltage HIGH				
	at $V_{DD} - V_{SS2}$ = 2.5V;				
V_{OH}	$-I_O$ = 0.1mA	$V_{DD} - 0.4$			V
	at $V_{DD} - V_{SS2}$ = 4 to 6V;				
V_{OH}	$-I_O$ = 0.5mA	$V_{DD} - 0.4$			V
	Output voltage LOW				
	at $V_{DD} - V_{SS2}$ = 2.5V;				
V_{OL}	I_O = 0.3mA			0.4	V
	at $V_{DD} - V_{SS2}$ = 4 to 6V;				
V_{OL}	I_O = 1.6mA			0.4	V
Output SDA (N-Channel open drain)					
	Output 'ON': I_O = 3mA				
V_{OL}	at $V_{DD} - V_{SS2}$ = 2.5 to 6V			0.4	V
	Output 'OFF' (leakage current)				
I_O	at $V_{DD} - V_{SS2}$ = 6V; V_O = 6V			1	μA
Internal Threshold Voltage					
V_{TH1}	Power failure detection	1	1.2	1.4	V
	Power 'ON' reset				
V_{TH2}	at $V_{SCL} = V_{SDA} = V_{DD}$	1.5	2.0	2.5	V

AC ELECTRICAL CHARACTERISTICS

V_{SS2} = 0V; T_A = −40 to + 85°C, unless otherwise specified. Typical values at T_A = + 25°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Rise and Fall Times of Input Signals					
t_R, t_F	Input EXTPF			1	μs
t_R, t_F	Input PFIN			∞	μs
	Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels				
t_R	rise time			1	μs
t_F	fall time			0.3	μs
Frequency at SCL					
	at $V_{DD} - V_{SS2}$ = 4 to 6V				
t_{LOW}	Pulse width LOW (see Figures 7 and 9	4.7			μs
t_{HIGH}	Pulse width HIGH (see Figures 7 and 9	4			μs
t_I	Noise suppression time constant at SCL and SDA input	0.25	1	2.5	μs
c_{IN}	Input capacitance (SCL, SDA)			7	pF
Oscillator					
C_{OUT}	Integrated oscillator capacitance		40		pF
R_F	Oscillator feedback resistance		3		MΩ
	Oscillator stability for: $\triangle(V_{DD} - V_{SS1})$ = 100mV at $V_{DD} - V_{SS1}$ = 1.55V;				
f/f_{OSC}	T_A = 25°C		2×10^{-6}		
	Quartz crystal parameters				
	Frequency = 32.768 kHz				
R_S	Series resistance			40	kΩ
C_L	Parallel capacitance		9		pF
C_T	Trimmer capacitance	5		25	pF

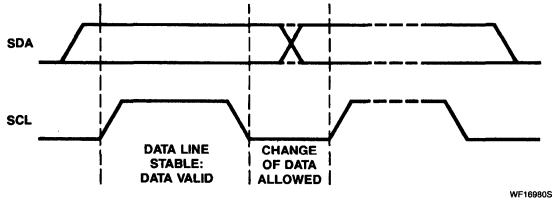


Figure 1. Bit Transfer

Table 1. Cycle Length of the Time Counter

UNIT	NUMBER OF BITS	COUNTING CYCLE	CARRY FOR FOLLOWING UNIT	CONTENT OF MONTH COUNTER
Minutes	7	00 to 59	59 → 00	
Hours	6	00 to 23	23 → 00	
Days	6	01 to 28	28 → 01	} 2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
Months	5	01 to 12	12 → 01	

NOTE: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the time base for the prescaler. The frequency is determined by a single 32.768kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and Time Counter

The prescaler provides a 128Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC and MIN, respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1:1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Alarm Register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Table 2. Power Fail Selection

EXTPF	PFIN	FUNCTION
0	0	Power fail is sensed internally
0	1	Test mode
1	0	Power fail is sensed externally
1	1	No power fail sensed

NOTE:
0: connected to V_{SS1} (LOW)
1: connected to V_{DD} (HIGH)

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal, the flag COMP will be set 4ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set, and then it will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

Power On/Power Fail Detection

If the voltage $V_{DD} - V_{SS1}$ falls below a certain value, the operation of the clock becomes undefined. Thus, a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTIVE ADDRESS has been received. The flag POWF can be set by an internally-generated power fail level-discriminator signal for application with ($V_{DD} - V_{SS1}$) greater than V_{TH1}, or by an externally-generated power fail signal for application with ($V_{DD} - V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally-or externally-controlled POWF can be selected by input EXTPF as shown in Table 2.

The external power fail control operates by absence of the $V_{DD} - V_{SS2}$ supply. Therefore, the input levels applied to PFIN and EXTPF must be within the range of $V_{DD} - V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power-on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD} - V_{SS2}$ is less than V_{TH2}.

Interface Level Shifters

The level shifters adjust the 5V operating voltage ($V_{DD} - V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD} - V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD} - V_{SS2}$ supply voltage. If the voltage $V_{DD} - V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD} - V_{SS2}$ and the $V_{DD} - V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD} - V_{SS2} = 0$.

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer (see Figure 1)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and Stop Conditions (see Figure 2)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System Configuration (see Figure 3)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

Acknowledge (see Figure 4)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse. So that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition (see Figures 11 and 12).

Timing Specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-Speed Mode — Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 5.

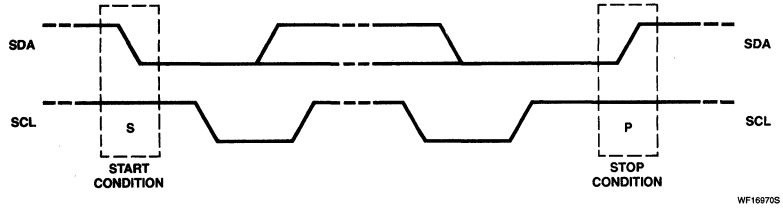


Figure 2. Definition of Start and Stop Conditions

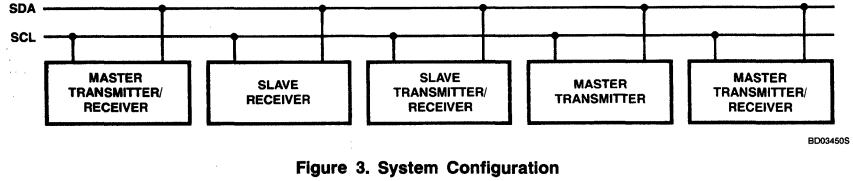


Figure 3. System Configuration

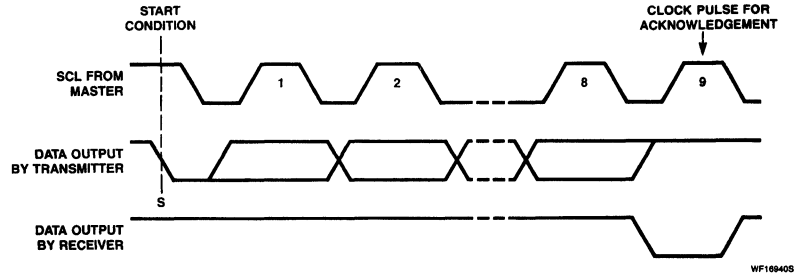
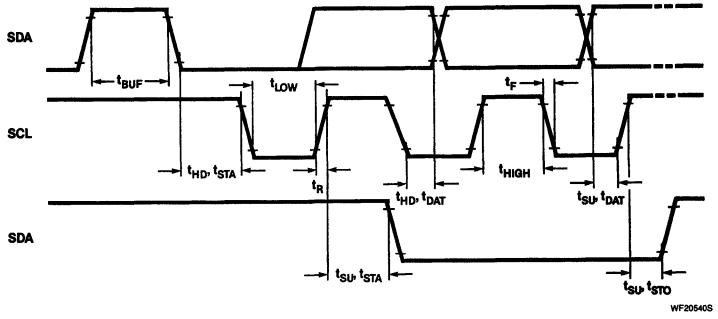


Figure 4. Acknowledgement on the I^2C Bus

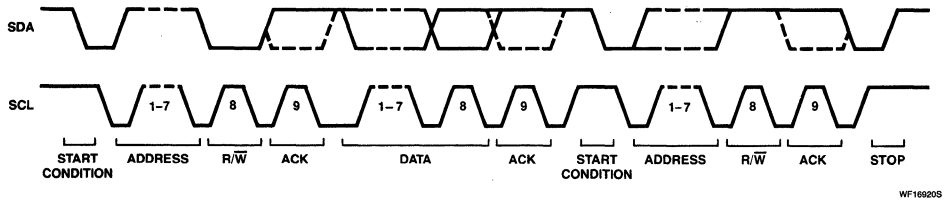


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
t_{HD}, t_{STA}	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
t_{SU}, t_{STA}	$t \geq t_{LOWmin}$	Start condition setup time, only valid for repeated start code
t_{HD}, t_{DAT}	$t \geq 0\mu s$	Data hold time
t_{SU}, t_{DAT}	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
t_{SU}, t_{STO}	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
1. All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

Figure 5. Timing of the High-Speed Mode

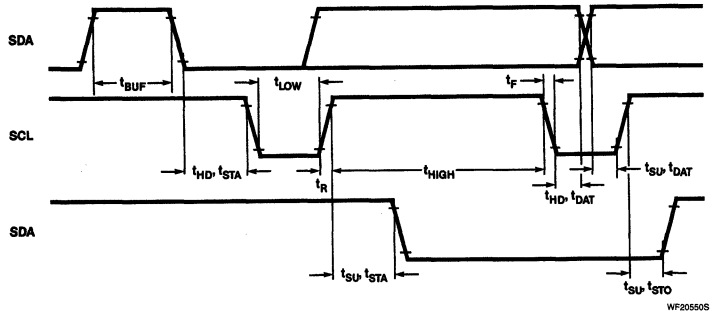


Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Figure 6. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode — Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 7.



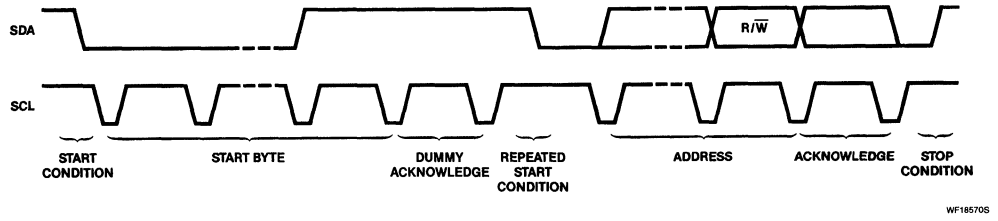
Where:

t_{BUF}	$t \geq 105\mu s$ (t_{LOWmin})
t_{HD}, t_{STA}	$t \geq 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	130μs ± 25μs
t_{HIGH}	390μs ± 25μs
t_{SU}, t_{STA}	130μs ± 25μs*
t_{HD}, t_{DAT}	$t \geq 0\mu s$
t_{SU}, t_{DAT}	$t \geq 250ns$
t_R	$t \leq 1\mu s$
t_F	$t \leq 300ns$
t_{SU}, t_{STO}	130μs ± 25μs

*Only valid for repeated start code.

NOTE:
1. All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}; for definitions see high-speed mode.

Figure 7. Timing of the Low-Speed Mode



Where:

Clock t_{LOWmin}	130μs ± 25μs
$t_{HIGHmin}$	390μs ± 25μs
Mark-to-space ratio	1:3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

NOTE:
1. The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: *ICs for digital systems in radio, audio and video equipment.*

Figure 8. Complete Data Transfer in the Low-Speed Mode

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave Address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Figure 9.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

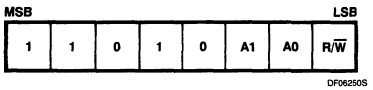


Figure 9. Slave Address

Clock/Calendar READ/WRITE Cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Figures 10 and 11.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

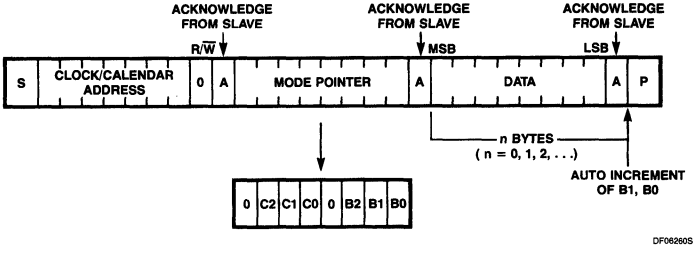


Figure 10. Master Transmitter Transmits to Clock/Calendar Slave Receiver

Table 3. CONTROL-nibble

	C2	C1	C0	FUNCTION
0	0	0	0	Execute address
0	0	0	1	Read control/status flags
0	0	1	0	Reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	Time adjust, with carry for minute counter[1]
0	1	0	0	Reset NODA flag
0	1	0	1	Set NODA flag
0	1	1	0	Reset COMP flag

NOTE:
1. If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 sec. From the count 30 there is a carry which adjusts the time by max. +30 sec.

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register, respectively.

Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

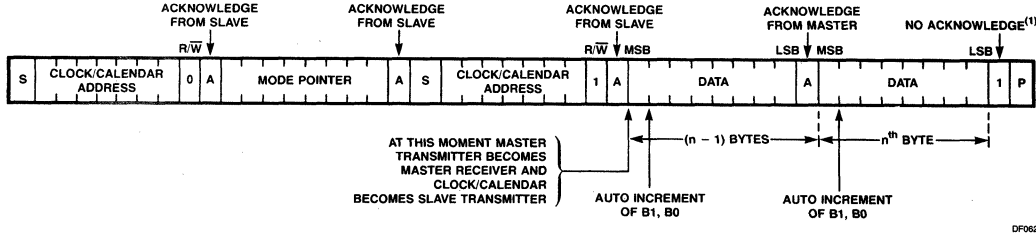
Table 4. ADDRESS-nibble

	B2	B1	B0	ADDRESSED TO:
0	0	0	0	Time counter hours
0	0	0	1	Time counter minutes
0	0	1	0	Time counter days
0	0	1	1	Time counter months
0	1	0	0	Alarm register hours
0	1	0	1	Alarm register minutes
0	1	1	0	Alarm register days
0	1	1	1	Alarm register months

Table 5. Placement of BCD Digits in the DATA Byte

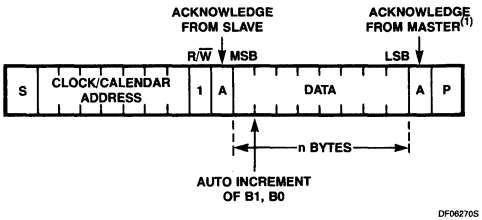
MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
X	X	D	D	D	D	D	D	Hours
X	D	D	D	D	D	D	D	Minutes
X	X	D	D	D	D	D	D	Days
X	X	X	D	D	D	D	D	Months

NOTE:
1. Where "X" is the don't care bit and "D" is the data bit.



NOTE:
The master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Figure 11. Master Transmitter Reads Clock/Calendar After Setting Mode Pointer



NOTE:
The master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave.

Figure 12. Master Reads Clock/Calendar Immediately After First Byte

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.
The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER conditon occurs.

Table 6. Slave Receiver Acknowledgement

MODE POINTER								ACKNOWLEDGE ON BYTE		
								Address	Mode pointer	Data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

NOTE:
1. Where "X" is the don't care bit.

Table 7. Organization of the BCD Digits in the DATA Byte

MSB DATA LSB								ADDRESSED TO:
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	
0	0	D	D	D	D	D	D	Hours
0	D	D	D	D	D	D	D	Minutes
0	0	D	D	D	D	D	D	Days
0	0	0	D	D	D	D	D	Months
0	0	0	*	**	NODA	COMP	POWF	Control/status flags

NOTES:
1. Where: "D" is the data bit, * = minutes, ** = seconds.

APPLICATION INFORMATION

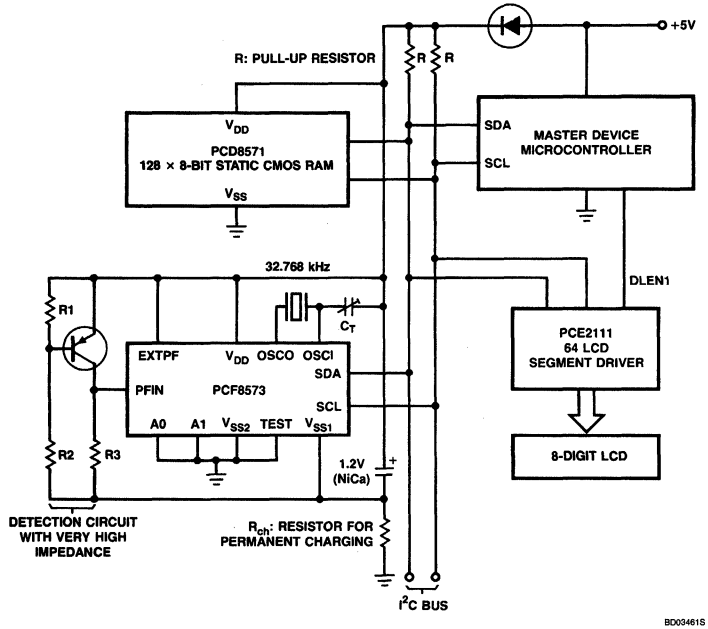


Figure 13. Application Example of the PCF8573 Clock/Calendar

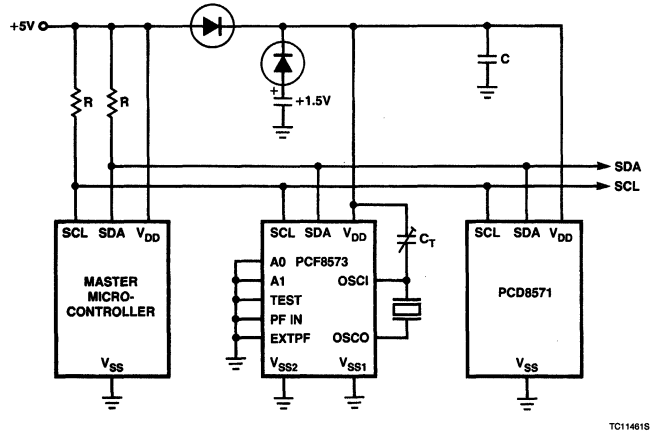


Figure 14. Application Example of the PCF8573 With Common V_{SS1} and V_{SS2} Supply

PCF8574
8-Bit Remote I/O Expander

Product Specification

Linear Products

DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C). It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only). The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.

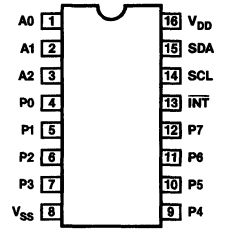
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

FEATURES

- **Operating supply voltage: 2.5V to 6V**
- **Low standby current consumption: max. 10μA**
- **Bidirectional expander**
- **Open-drain interrupt output**
- **8-bit remote I/O port for the I^2C bus**
- **Peripheral for the MAB8400 and PCF8500 microcomputer families**
- **Latched outputs with high current drive capability for directly driving LEDs**
- **Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD07880S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address inputs
2	A1	
3	A2	
4	P0	8-bit quasi-bidirectional I/O ports
5	P1	
6	P2	
7	P3	
8	V_{SS}	
9	P4	8-bit quasi-bidirectional I/O ports
10	P5	
11	P6	
12	P7	
13	$\overline{INT}$	Interrupt output
14	SCL	Serial clock line
15	SDA	Serial data line
16	V_{DD}	Positive supply

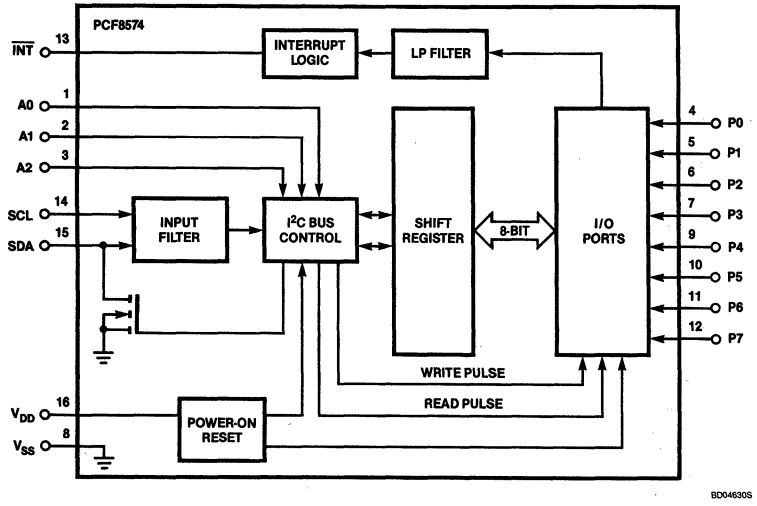
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to +85°C	PCF8574PN
16-Pin Plastic SO package (SO16L; SOT-162A)	−40°C to +85°C	PCF8574TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +7	V
V_I	Input voltage range (any pin)	V_{SS} − 0.5 to V_{DD} + 0.5	V
$\pm I_I$	DC current into any input	20	mA
$\pm I_O$	DC current into any output	25	mA
$\pm I_{DD}$; I_{SS}	V_{DD} or V_{SS} current	100	mA
P_{TOT}	Total power dissipation	400	mW
P_O	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

BLOCK DIAGRAM



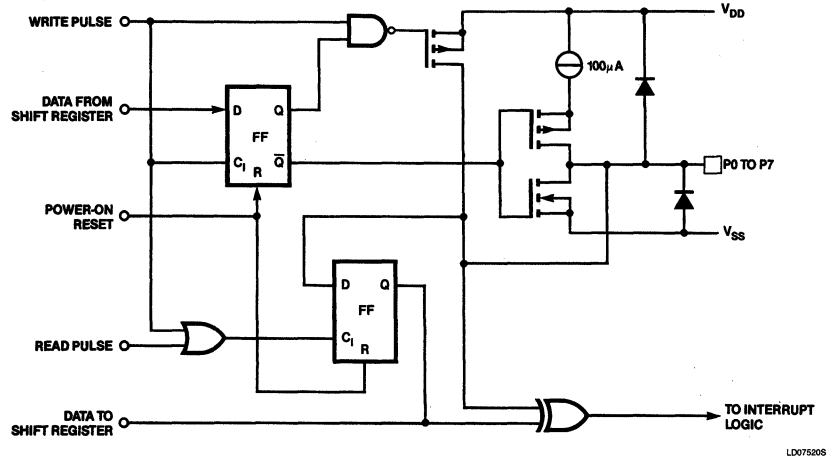


Figure 1. Simplified Schematic Diagram of Each Port

DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 6V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 16)					
V_{DD}	Supply voltage	2.5		6	V
I_{DD} I_{DDO}	Supply current at V_{DD} = 6V; no load, inputs at V_{DD}, V_{SS} operating standby			100 10	μA μA
V_{REF}	Power-on reset voltage level[1]		1.3	2.4	V
Input SCL; input/output SDA (Pins 14; 15)					
V_{IL}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD} + 0.5	V
I_{OL}	Output current LOW at V_{OL} = 0.4V	3			mA
$\|I_{LI}\|$	Input/output leakage current			100	nA
f_{SCL}	Clock frequency (See Figure 6)			100	kHz
t_S	Tolerable spike width at SCL and SDA input			100	ns
C_I	Input capacitance (SCL, SDA) at $V_I = V_{SS}$			7	pF
I/O ports (Pins 4 to 7; 9 to 12)					
V_{IL}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD} + 0.5V	V
$\pm I_{IHL}$	Maximum allowed input current through protection diode at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$			400	μA
I_{OL}	Output current LOW at V_{OL} = 1V; V_{DD} = 2.5V	5			mA
$-I_{OH}$	Output current HIGH at $V_{OH} = V_{SS}$ (current source only)	30	100	300	μA
$-I_{OH}t$	Transient pull-up current HIGH during acknowledge (see Figure 14) at $V_{OH} = V_{SS}$		0.5		mA
$C_{I/O}$	Input/output capacitance			10	pF
Port timing; $C_L \leqslant$ 100pF (see Figures 10 and 11)					
t_{PV}	Output data valid			4	μs
t_{PS}	Input data setup	0			μs
t_{PH}	Input data hold	4			μs
Interrupt $\overline{INT}$ (Pin 13)					
I_{OL}	Output current LOW at V_{OL} = 0.4V	1.6			mA
$\|I_{OH}\|$	Output current HIGH at $V_{OH} = V_{DD}$			100	nA
$\overline{INT}$ timing; $C_L \leqslant$ 100pF (see Figure 11)					
t_{IV} t_{IR}	Input data valid Reset delay			4 4	μs μs
Select inputs A0, A1, A2 (Pins 1 to 3)					
V_{IH}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD} + 0.5V	V
$\|I_L\|$	Input leakage current at $V_I = V_{DD}$ or V_{SS}			100	nA

NOTE:
1. The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

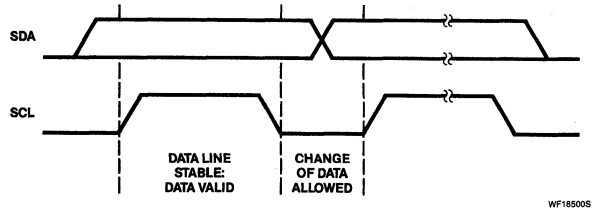


Figure 2. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

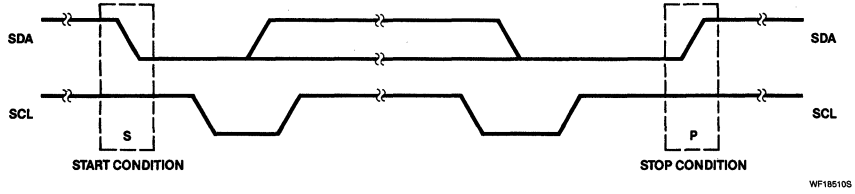


Figure 3. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

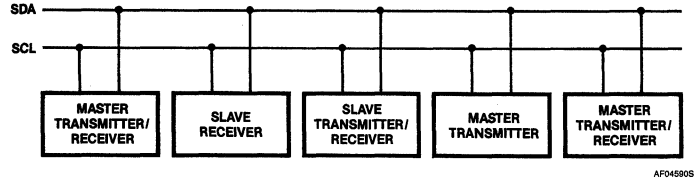


Figure 4. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge. Related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

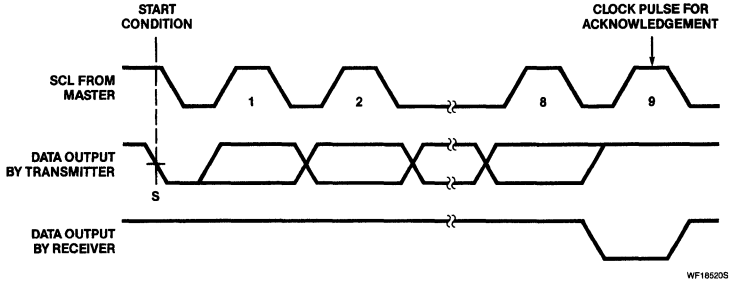


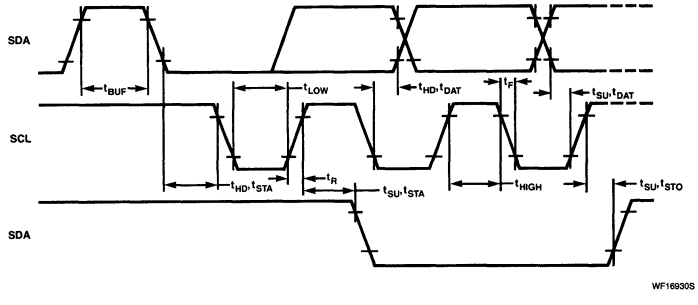
Figure 5. Acknowledgement on the I^2C Bus

Timing Specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-Speed Mode

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 6.

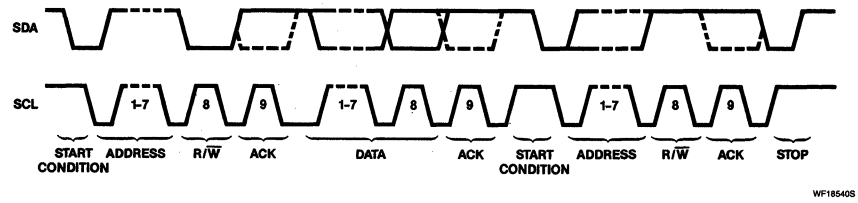


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD};\ t_{STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
$t_{SU};\ t_{STA}$	$t \geq t_{LOWmin}$	Start condition set-up time; only valid for repeated start code
$t_{HD};\ t_{DAT}$	$t \geq 0\mu s$	Data hold time
$t_{SU};\ t_{DAT}$	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
$t_{SU};\ t_{STO}$	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 6. Timing of the High-Speed Mode



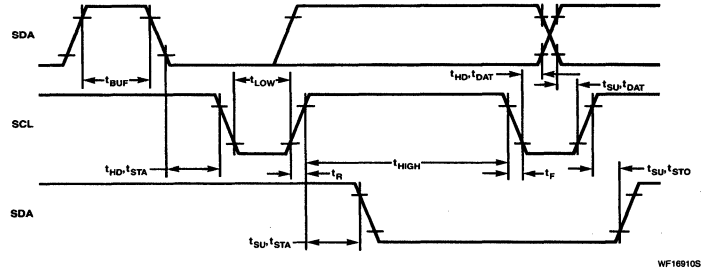
Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 7. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode

Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 8.



Where:

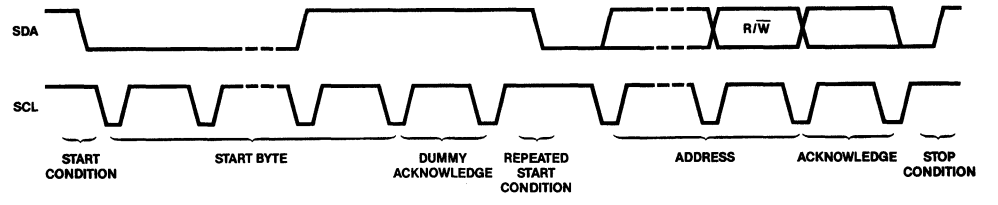
t_{BUF}	$t \geqslant 105\mu s$ (t_{LOWmin})
$t_{HD};\ t_{STA}$	$t \geqslant 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	130μs ± 25μs
t_{HIGH}	390μs ± 25μs
$t_{SU};\ t_{STA}$	130μs ± 25μs*
$t_{HD};\ t_{DAT}$	$t \geqslant 0\mu s$
$t_{SU};\ t_{DAT}$	$t \geqslant 250ns$
t_R	$t \leqslant 1\mu s$
t_F	$t \leqslant 300ns$
$t_{SU};\ t_{STO}$	130μs ± 25μs

NOTES:

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

* Only valid for repeated start code.

Figure 8. Timing of the Low-Speed Mode



Where:

Clock t_{LOWmin}	130μs ± 25μs
$t_{HIGHmin}$	390μs ± 25μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Figure 9. Complete Data Transfer in the Low-Speed Mode

FUNCTIONAL DESCRIPTION

Addressing (See Figures 10 and 11)

Each bit of the PCF8574 I/O port can be independently used as an input or an output.

Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

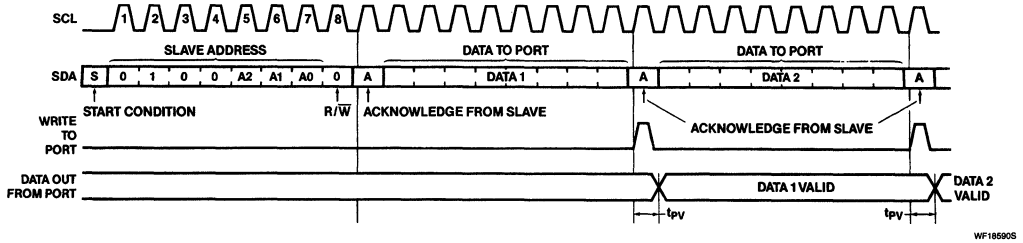
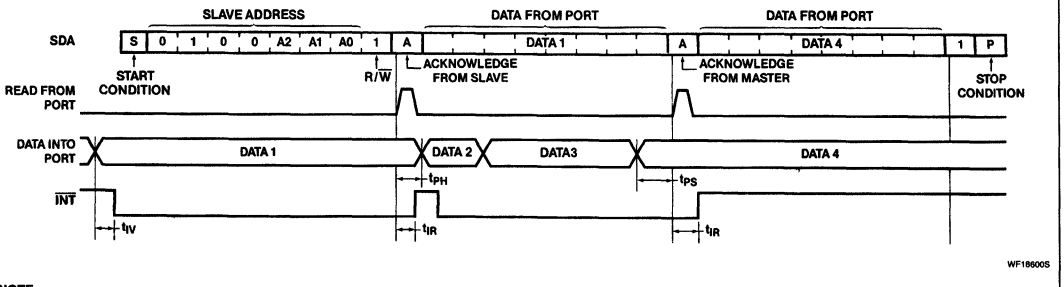


Figure 10. WRITE Mode (Output Port)



NOTE:
A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Figure 11. READ Mode (Input Port)

Interrupt (See Figures 12 and 13)

The PCF8574 provides an open-drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{IV} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt. Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit.

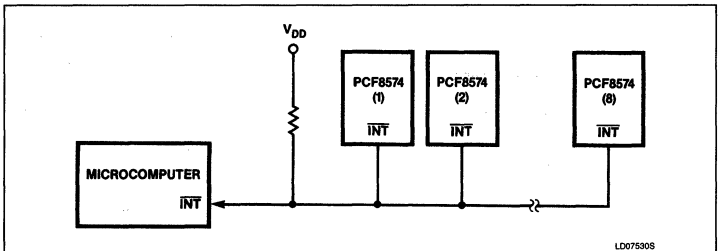


Figure 12. Application of Multiple PCF8574s With Interrupt

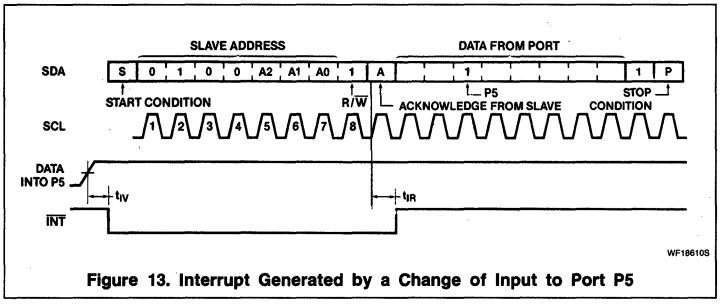


Figure 13. Interrupt Generated by a Change of Input to Port P5

Quasi-Bidirectional I/O Ports (See Figure 14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW-to-HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

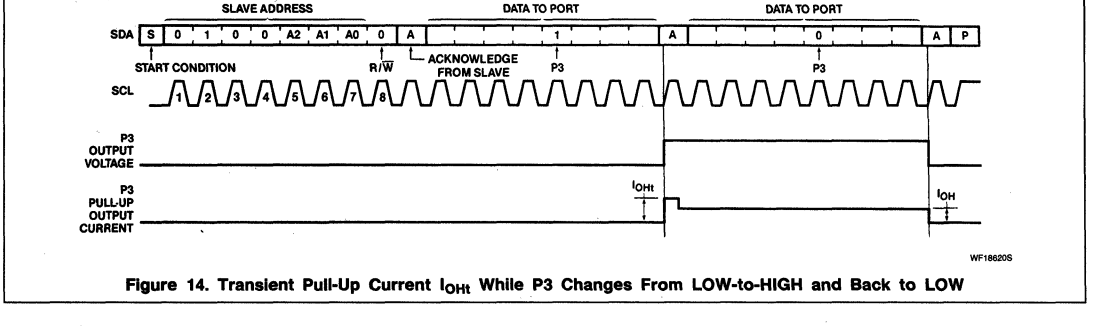


Figure 14. Transient Pull-Up Current I_{OHt} While P3 Changes From LOW-to-HIGH and Back to LOW

PCF8582
Static CMOS EEPROM (256 × 8-bit)

Preliminary Specification

DESCRIPTION

The PCF8582 is 2K-bit 5V electrically erasable programmable read only memory (EEPROM) organized as 256 by 8 bits. It is designed in a floating-gate CMOS technology.

As data bytes are received and transmitted via the serial I^2C bus, an 8-pin DIP package is sufficient. Up to eight PCF8582 devices may be connected to the I^2C bus.

Chip select is accomplished by three address inputs.

FEATURES

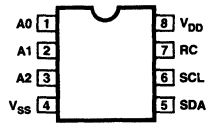
- **Non-volatile storage of 2K-bit organized as 256 × 8**
- **Only one power supply required (5V)**
- **On-chip voltage multiplier for erase/write**
- **Serial input/output bus (I^2C)**
- **Automatic word address incrementing**
- **Low power consumption**
- **One point erase/write timer**
- **Power-on reset**
- **10,000 erase/write cycles per byte**
- **10 years non-volatile data retention**
- **Infinite number of read cycles**
- **Pin-and address-compatible to PCD8571 and PCD8572**

APPLICATIONS

- **Telephone**
- **Radio and television**
- **General purpose**

PIN CONFIGURATION

N Package



TOP VIEW

CD12090S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	
2	A1	Address inputs/test
3	A2	Mode select
4	V_{SS}	Ground
5	SDA	I^2C bus lines
6	SCL	
7	RC	Input for timer constant
8	V_{DD}	Positive supply

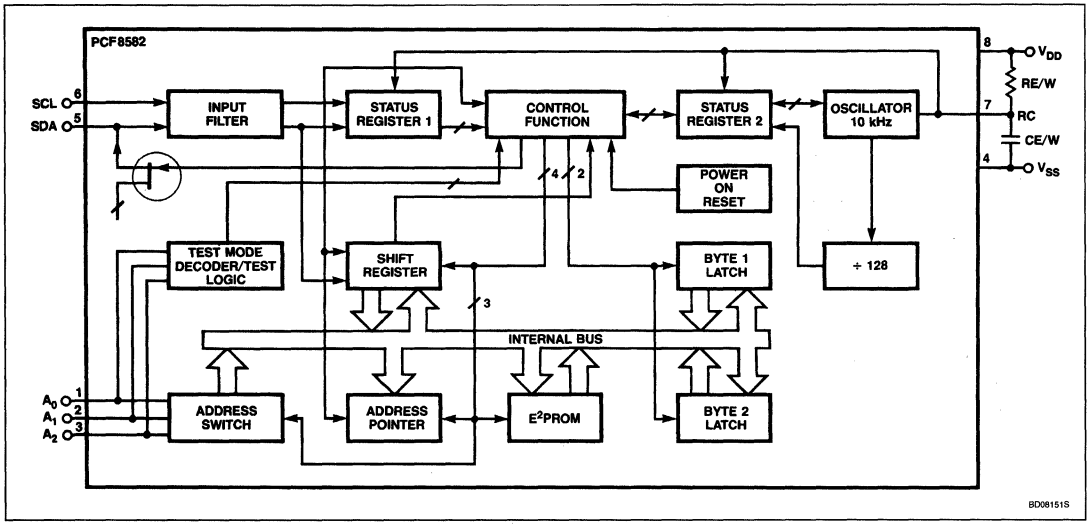
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	0 to +70°C	PCF8582N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	−0.3 to 7	V
V_{IN}	Input voltage, at Pin 4, (input impedance 500Ω)	V_{SS} − 0.8 to V_{DD} + 0.8	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
I_I	Current into any input pin	100	μA
I_O	Output current	10	mA

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{DD} = 5V$; $V_{SS} = 0V$; $T_A = -40°C$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Operating supply voltage	4.5	5	5.5	V
I_{DDR}	Operating supply current, READ (f_{SLC} = 100kHz)		1	TBD	mA
I_{DDW}	Operating supply current, WRITE/ERASE		1	TBD	mA
I_{DDO}	Standby supply current (V_{DD} = 5V)		5	TBD	µA
Input SCL					
V_{IL} V_{IH} V	Input/output SDA: Input voltage LOW Input voltage HIGH Output voltage LOW	 −0.3 3		 1.5 V_{DD} + 0.8	 V V
V_{OL}	(I_{OL} = 3mA, V_{DD} = 4.5V)			0.4	V
I_{OH}	Output leakage current HIGH ($V_{OH} = V_{DD}$) Input leakage current			1	µA
$\pm I_{IN}$	(A0, A1, A2, SCL)[1]			1	µA
f_{SCL}	Clock frequency	0		100	kHz
C_I	Input capacity (SCL, SDA)			7	pF
t_I	Noise suppression time constant at SCL and SDA input	0.25	0.5	1	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
t_{HD}, t_{STA}	Hold time start condition. After this period the first clock pulse is generated	4			µs
t_{LOW}	The LOW period of the clock	4.7			µs
t_{HIGH}	The HIGH period of the clock	4			µs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 5V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{SU}, t_{STA}	Setup time for start condition (only relevent for a repeated start condition)	4.7			μs
	Hold time DATA for:				
t_{HD}, t_{DAT}	CBUS compatible masters	5			μs
t_{HD}, t_{DAT}	I^2C devices[2]	0			μs
t_{SU}, t_{DAT}	Setup time DATA	250			ns
t_R	Rise time for both SDA and SCL lines			1	μs
t_F	Fall time for both SDA and SCL lines			300	ns
t_{SU}, t_{STO}	Setup time for stop condition	4.7			μs
Erase/write timer constant					
$C_{E/W}$	Erase/write timing capacitor for erase/write cycle of 20ms		3.3		nF
$R_{E/W}$	Erase/write cycle timing resistor		39		kΩ

NOTES:
1. Selection of the chip address is done by connecting the A0, A1, and A2 inputs either to V_{SS} or V_{DD}.
2. A transmitter must internally provide at least a hold time to bridge the undefined region (maximum 30ns) of the falling edge of SCL.

FUNCTIONAL DESCRIPTION

Characteristics of the I^2C bus

The I^2C bus is intended for communication between different ICs. The serial bus consists of two bidirectional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy — both data and clock lines remain HIGH.

Start Data Transfer — a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition.

Stop Data Transfer — a change in the state of the data line, from LOW to HIGH, defines the stop condition.

Data Valid — the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I^2C bus specifications a low-speed mode (2kHz clock rate) and a high-speed mode (100kHz clock rate) are defined. The PCF8582 works in both modes. By definition a device that gives out a signal is called a "transmitter," and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge-related clock pulse. A slave receiver which it addresses is obliged to generate an acknowledge after the reception of each byte.

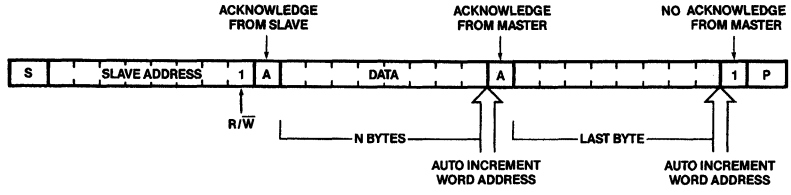
Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse.

Setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

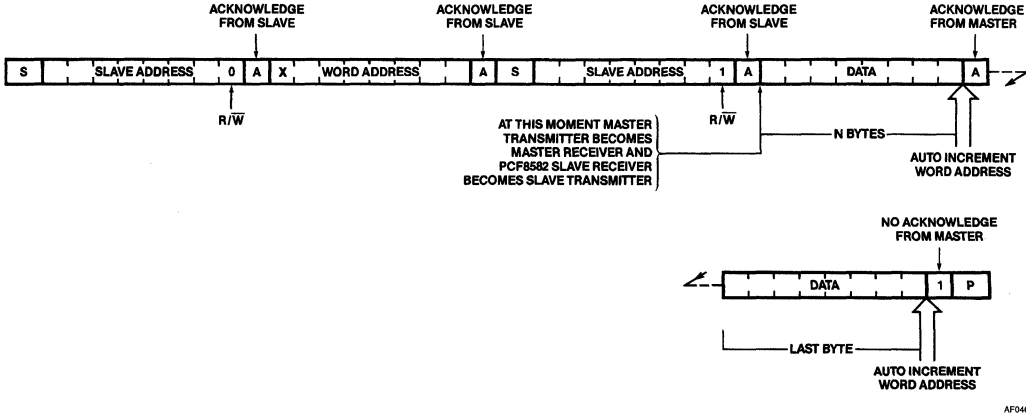
I^2C Bus Protocol

The I^2C bus configuration for different READ and WRITE cycles of the PCF8582 are shown in Figures 1a and 1b.



NOTES:
1. After this stop condition the erase/write cycle starts and the bus is free for another transmission; the duration of the erase/write cycle is approximately 20ms if only one byte is written, and 40ms if two bytes are written. During the erase/written cycle the slave receiver does not send an acknowledge bit if addressed via I^2C bus.
2. The second data byte is voluntary. Trying to erase/write more than two bytes is not allowed.

a. Master Transmitter Transmits to PCF8582 Slave Receiver (ERASE/WRITE Mode)



b. Master Reads PCF8582 Slave After Setting Word Address (WRITE Word Address; READ Data)

Figure 1

I^2C Bus Timing

Figure 2 shows the I^2C bus timing.

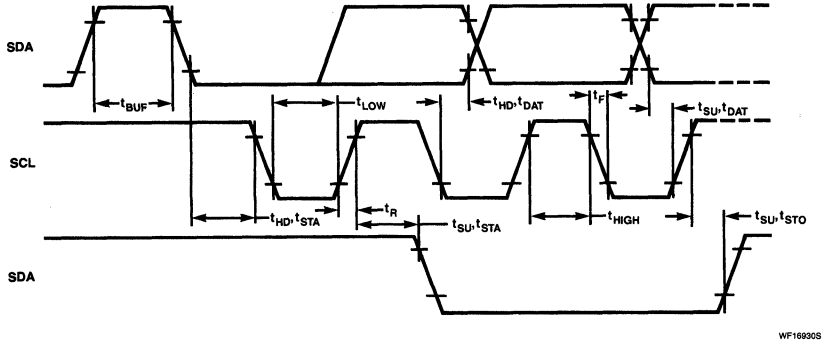


Figure 2. Timing Requirements for the I^2C Bus

SAB3013
Hex 6-Bit DAC

Product Specification

Linear Products

DESCRIPTION

The SAB3013 is a MOS N-channel integrated circuit which provides 6 analog memories controlled by a microcomputer.

FEATURES

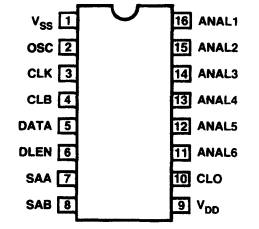
- **Replacement for 6 μP-controlled potentiometers**
- **6-function analog memory; D/A converter with 6-bit resolution**
- **The output of the analog values is pulse-width modulated with adjustable repetition rate (max. 21.8kHz)**
- **Microcomputer-adapted asynchronous serial interface for data input (CBUS)**
- **Parallel operation of up to four SAB3013 circuits is possible**
- **Serial CBUS-controlled**

APPLICATIONS

- **Television receivers**
- **Radio receivers**
- **Computer-controlled TV/radio**
- **Industrial**
- **Instrumentation**

PIN CONFIGURATION

N Package



CD11930S

PIN NO.	SYMBOL	DESCRIPTION	
1	V_{SS}	Ground (0V)	
2	OSC	Oscillator output	
3	CLK	Oscillator input (Schmitt-trigger)	
4	CLB	Asynchronous clock pulse	CBUS
5	DATA	Data input	CBUS
6	DLEN	Data line enable input	CBUS
7	SAA	Address inputs	
8	SAB	Address inputs	
9	V_{DD}	Positive supply	
10	CLO	Buffered oscillator output	
11	ANAL6	Analog outputs	
12	ANAL5	Analog outputs	
13	ANAL4	Analog outputs	
14	ANAL3	Analog outputs	
15	ANAL2	Analog outputs	
16	ANAL1	Analog outputs	

ORDERING INFORMATION

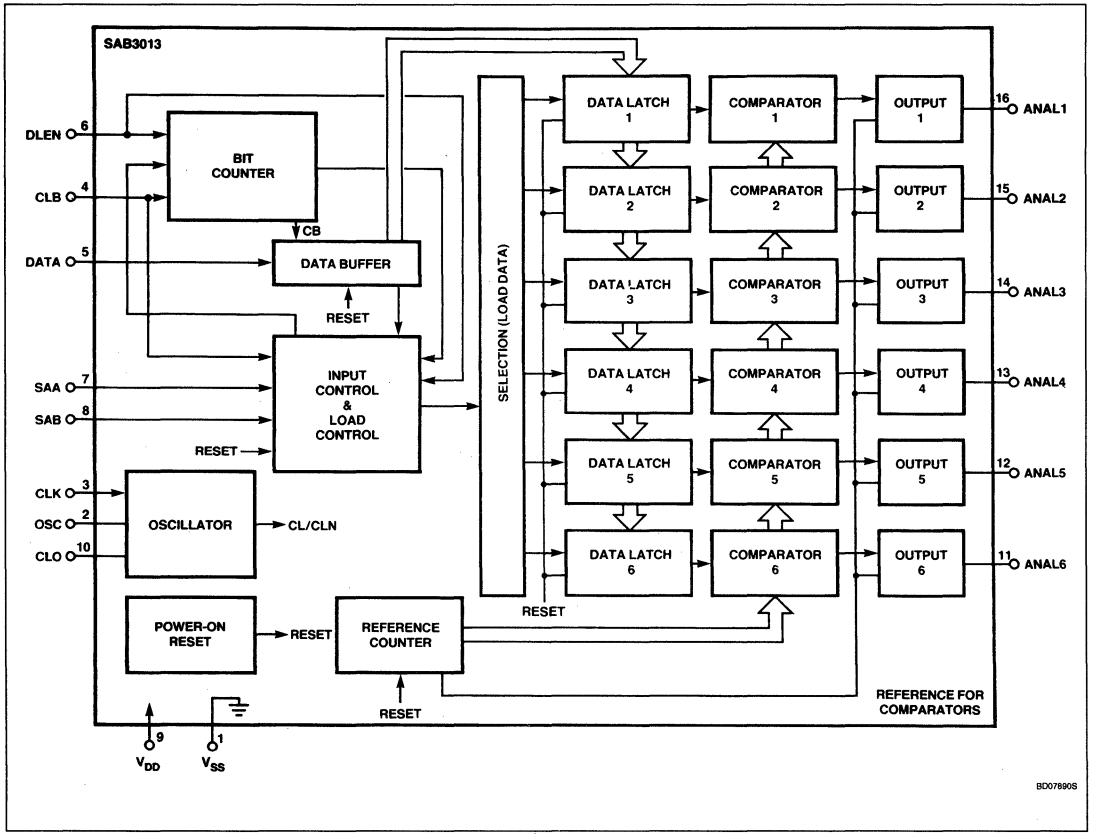
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to 70°C	SAB3013N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.3 to +7.5	V
V_I	Input voltage range	−0.3 to +15	V
$\pm I_I$	Input current	100	μA
V_O	Output voltage (open drain outputs)	V_{SS} to 15	V
$\pm I_O$	Output current (open drain/push-pull outputs)	10	mA
P_O	Power dissipation per output	25	mW
P_{TOT}	Total power dissipation per package	250	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

Hex 6-Bit DAC SAB3013

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS

V_{SS}=0; T_A = 0°C to +70°C; V_{DD} = 4.5 to 5.5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5	5.5	V
I_{DD}	Supply current	V_{DD} = 5.5V			35	mA
Inputs DATA, CLB, DLEN, SAA, SAB						
V_{IL}	Input voltage LOW		−0.3		0.8	V
V_{IH}	Input voltage HIGH		2.0		12	V
I_{IR}	Input leakage current	V_I = −0.3 to +12V			1	μA
Outputs ANAL1 to ANAL6 (open-drain)						
V_{OL}	Output voltage LOW	I_O = 6mA			0.7	V
I_{OR}	Output leakage current	V_{OH} = 15V			20	μA
C_L	Load capacitance				1000	pF
Input CLK						
V_{IL}	Input voltage LOW		−0.3		0.8	V
V_{IH}	Input voltage HIGH		3.5		12	V
I_{IR}	Input leakage current	V_I = −0.3 to 12V			1	μA
t_{WH}	Pulse duration HIGH		355			ns
t_{WL}	Pulse duration LOW		355			ns
Output CLO						
V_{OL}	Output voltage LOW	I_O 500μA			0.8	V
V_{OH}	Output voltage HIGH	$-I_O$ = 100μA	3.5			V
Inputs DATA, CLB						
t_{WH}	Pulse duration HIGH	see Figure 1	450			ns
t_{WL}	Pulse duration LOW	see Figure 1	450			ns
f_{CLB}	Input frequency CLB		0		1	MHz
Internal oscillator CLK/OSC						
R	External resistor		27		1000	kΩ
C	External capacitor		27		1000	pF
f_{CLK}	Clock frequency	R = 27kΩ; C = 27pF	0.7	1.0	1.4	MHz
f_{CLK}	Frequency for external oscillator		0.03		1.4	MHz
Timing (see Figure 1)						
t_{SUDA}	Data setup time DATA → CLB		800			ns
t_{HDDA}	Data hold time DATA → CLB		300			ns
t_{SUEN}	Enable setup time DLEN → CLB	Measured with a voltage swing of minimum $V_{IH} - V_{IL}$	400			ns
t_{SUDI}	Disable setup time CLB → DLEN		400			ns
t_{SULD}	Setup time DLEN → CLB (load pulse)		1000			ns

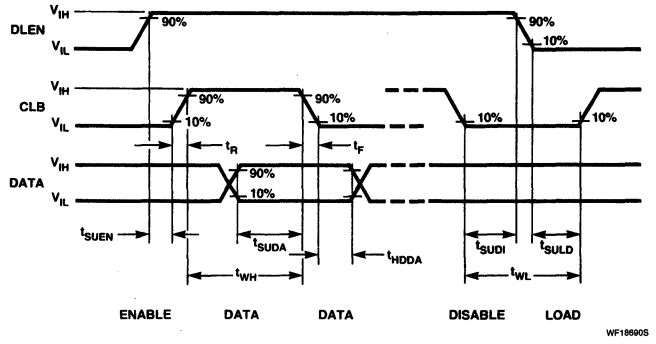


Figure 1. CBUS Timing

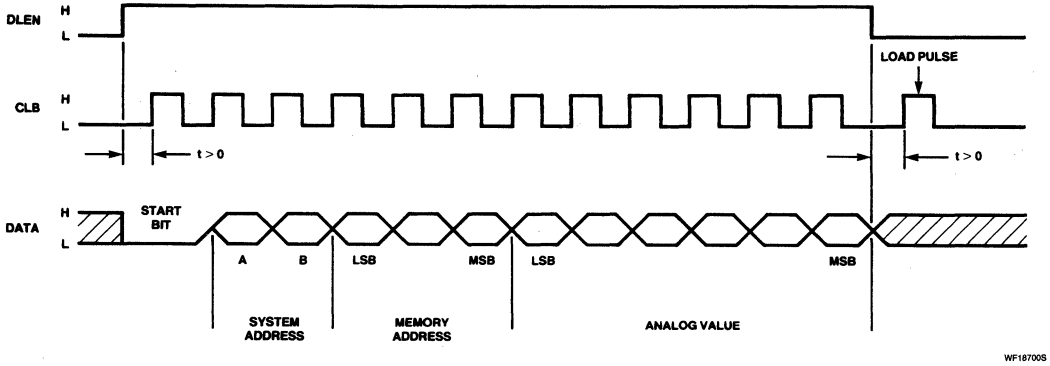


Figure 2. Waveforms Showing a CBUS Transmission

FUNCTIONAL DESCRIPTION

The SAB3013 is designed to deliver analog values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analog memory and D/A converter for six analog functions with a 6-bit resolution for each. The information for the analog memory is transferred by the microcomputer via an asynchronous serial data bus.

The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.

The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2 bits), for addressing the analog memories concerned (3 bits) and processing of the wanted analog value (6 bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.

The built-in oscillator can be used for a frequency between 30kHz and 1.4MHz. The analog values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (maximum 21.8kHz at f_{CLK} = 1.4MHz), and the analog values are determined by the ratio of the HIGH-time and the cycle time. A DC voltage proportional to the analog value is obtained by means of an external integration network (low-pass filter).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. The data from the data buffer is loaded directly into the output latch on receipt of a load pulse at input CLB (DLEN = LOW), provided the following conditions are met:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH)
- The start-bit must be LOW
- The system address bits must be A = SAA and B = SAB
- The analog address must be valid

The data word for the SAB3013 consists of the following bits (see Figure 2):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the required analog memory
6 data bits for processing the analog value

ADDRESS INPUTS (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be defined and not left open-circuit.

Reset

The circuit internally generates a reset cycle with a duration of one clock cycle after switching on the supply. If a spike on the supply is likely to destroy data, a reset signal will be generated. All analog memories are set to 50% (analog value 32/64) after the reset cycle. The supply voltage rise dV_{DD}/dt must be maximum 0.5V/μs and minimum 0.2V/μs.

4

SAB3035
FLL Tuning and Control Circuit

Product Specification

Linear Products

DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It also controls up to 8 analog functions, 4 general purpose I/O ports, and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I^2C bus.

FEATURES

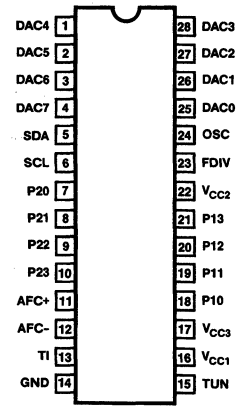
- **Combined analog and digital circuitry minimizes the number of additional interfacing components required**
- **Frequency measurement with resolution of 50kHz**
- **Selectable prescaler divisor of 64 or 256**
- **32V tuning voltage amplifier**
- **4 high-current outputs for direct band selection**
- **8 static digital-to-analog converters (DACs) for control of analog functions**
- **Four general purpose input/output (I/O) ports**
- **Tuning with control of speed and direction**
- **Tuning with or without AFC**
- **Single-pin, 4MHz on-chip oscillator**
- **I^2C bus slave transceiver**

APPLICATIONS

- **Satellite receivers**
- **Television receivers**
- **CATV converters**

PIN CONFIGURATION

N Package



TOP VIEW

CD11950S

PIN NO.	SYMBOL	DESCRIPTION
1	DAC4	Outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	Serial data line (I^2C bus)
6	SCL	Serial clock line (I^2C bus)
7	P20	General purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	AFC inputs
12	AFC−	
13	TI	Tuning voltage amplifier inverting input
14	GND	Ground
15	TUN	Tuning voltage amplifier output
16	V_{CC1}	+12V supply voltage
17	V_{CC3}	+32V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{CC2}	Positive supply for high-current band-selection output circuits
23	FDIV	Input from prescaler
24	OSC	Crystal oscillator input
25	DAC0	Outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

ORDERING INFORMATION

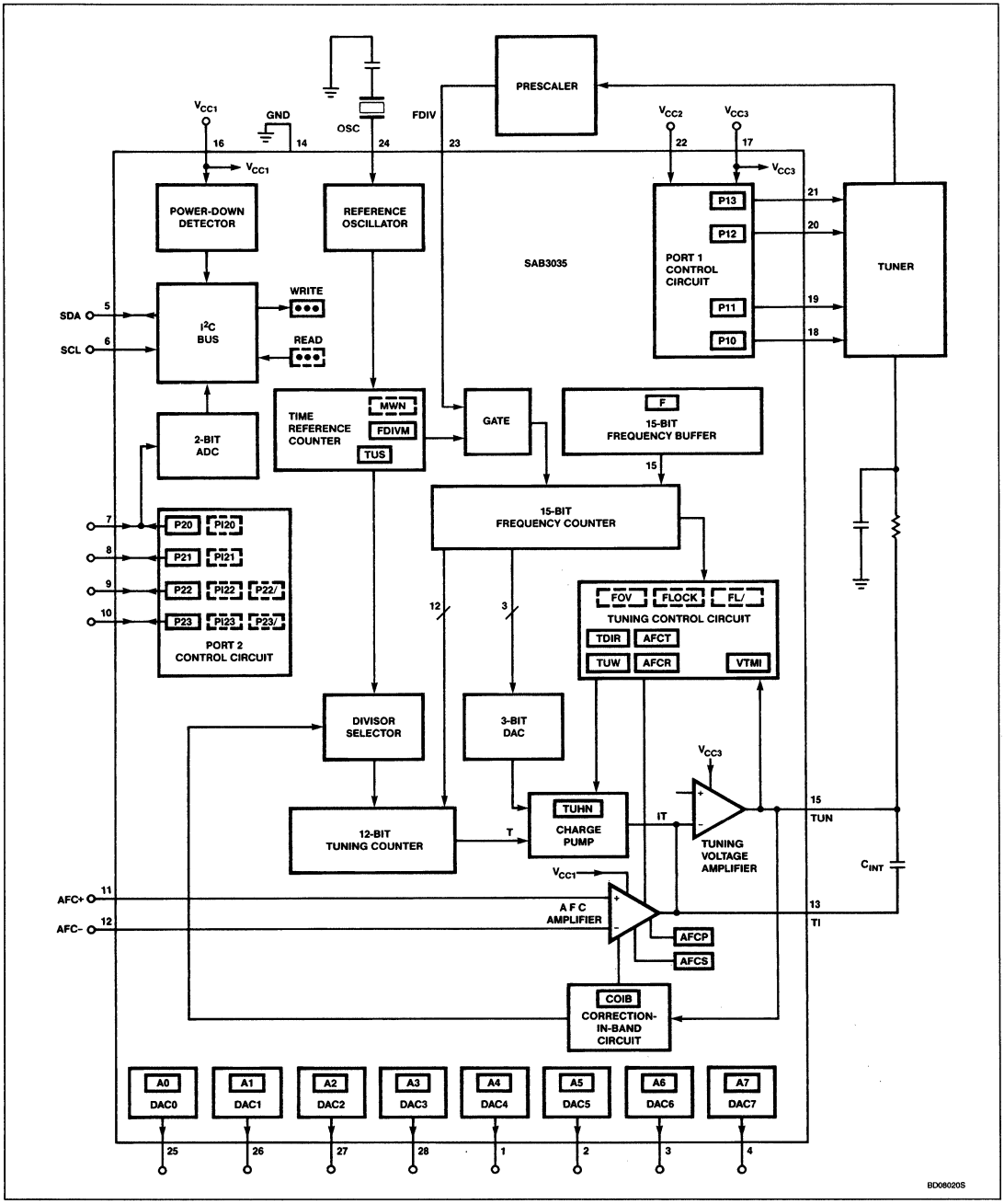
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−20°C to +70°C	SAB3035N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges:		
V_{CC1}	(Pin 16)	−0.3 to +18	V
V_{CC2}	(Pin 22)	−0.3 to +18	V
V_{CC3}	(Pin 17)	−0.3 to +36	V
	Input/output voltage ranges:		
V_{SDA}	(Pin 5)	−0.3 to +18	V
V_{SCL}	(Pin 6)	−0.3 to +18	V
V_{CC2X}	(Pins 7 to 10)	−0.3 to +18	V
$V_{AFC+,\ AFC-}$	(Pins 11 and 12)	−0.3 to V_{CC1} [1]	V
V_{TI}	(Pin 13)	−0.3 to V_{CC1} [2]	V
V_{TUN}	(Pin 15)	−0.3 to V_{CC3} [1]	V
V_{CC1X}	(Pins 18 to 21)	−0.3 to V_{CC2} [2]	V
V_{FDIV}	(Pin 23)	−0.3 to V_{CC1} [1]	V
V_{OSC}	(Pin 24)	−0.3 to +5	V
V_{DACX}	(Pins 1 to 4 and 25 to 28)	−0.3 to V_{CC1} [1]	V
P_{TOT}	Total power dissipation	1000	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

NOTES:
1. Pin voltage may exceed supply voltage if current is limited to 10mA.
2. Pin voltage must not exceed 18V but may exceed V_{CC2} if current is limited to 200mA.

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC1}	Supply voltages	10.5	12	13.5	V
V_{CC2}		4.7	13	16	V
V_{CC3}		30	32	35	V
I_{CC1}	Supply currents (no outputs loaded)	20	32	50	mA
I_{CC2}		0		0.1	mA
I_{CC3}		0.2	0.6	2	mA
I_{CC2A}	Additional supply currents (A)	−2		I_{OHP1X}	mA
I_{CC3A}	See Note 1	0.2		2	mA
P_{TOT}	Total power dissipation		400		mW
T_A	Operating ambient temperature	−20		+70	°C
I²C bus inputs/outputs SDA input (Pin 5) SCL input (Pin 6)					
V_{IH}	Input voltage HIGH[2]	3		$V_{CC1} - 1$	V
V_{IL}	Input voltage LOW	−0.3		1.5	V
I_{IH}	Input current HIGH[2]			10	μA
I_{IL}	Input current LOW[2]			10	μA
	SDA output (Pin 5, open-collector)				
V_{OL}	Output voltage LOW at $I_{OL} = 3mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
Open-collector I/O ports P20, P21, P22, P23 (Pins 7 to 10, open-collector)					
V_{IH}	Input voltage HIGH	2		16	V
V_{IL}	Input voltage LOW	−0.3		0.8	V
I_{IH}	Input current HIGH			25	μA
$-I_{IL}$	Input current LOW			25	μA
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
I_{OL}	Maximum output sink current		4		mA
AFC amplifier Inputs AFC+, AFC− (Pins 11, 12)					
	Transconductance for input voltages up to 1V differential:				
	AFCS1 AFCS2				
g00	0 0	100	250	800	nA/V
g01	0 1	15	25	35	μA/V
g10	1 0	30	50	70	μA/V
g11	1 1	60	100	140	μA/V
ΔM_g	Tolerance of transconductance multiplying factor (2, 4, or 8) when correction-in-band is used	−20		+20	%
V_{IOFF}	Input offset voltage	−75		+75	mV
V_{COM}	Common-mode input voltage	3		$V_{CC1} - 2.5$	V
CMRR	Common-mode rejection ratio		50		dB
PSRR	Power supply (V_{CC1}) rejection ratio		50		dB
I_I	Input current			500	nA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltage, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuning voltage amplifier Input TI, output TUN (Pins 13, 15)					
V_{TUN}	Maximum output voltage at $I_{LOAD} = \pm 2.5mA$	$V_{CC3} - 1.6$		$V_{CC3} - 0.4$	V
	Minimum output voltage at $I_{LOAD} = \pm 2.5mA$:				
	VTMI1 VTMI0				
V_{TM00}	0 0	300		500	mV
V_{TM10}	1 0	450		650	mV
V_{TM11}	1 1	650		900	mV
$-I_{TUNH}$	Maximum output source current	2.5		8	mA
I_{TUNL}	Maximum output sink current		40		mA
I_{TI}	Input bias current	−5		+5	nA
PSRR	Power supply V_{CC3} rejection ratio		60		dB
	Minimum charge IT to tuning voltage amplifier				
	TUHN1 TUHN0				
CH_{00}	0 0	0.4	1	1.7	μA/μs
CH_{01}	0 1	4	8	14	μA/μs
CH_{10}	1 0	15	30	48	μA/μs
CH_{11}	1 1	130	250	370	μA/μs
ΔCH	Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	−20		+20	%
	Maximum current I into tuning amplifier				
	TUHN1 TUHN0				
I_{T00}	0 0	1.7	3.5	5.1	μA
I_{T01}	0 1	15	29	41	μA
I_{T10}	1 0	65	110	160	μA
I_{T11}	1 1	530	875	1220	μA
Correction-in-band					
ΔV_{CIB}	Tolerance of correction-in-band levels 12V, 18V, and 24V	−15		+15	%
Band-select output ports P10, P11, P12, P13 (Pins 18 to 21)					
V_{OH}	Output voltage HIGH at $-I_{OH} = 50mA$[3]	$V_{CC2} - 0.6$			V
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
$-I_{OH}$	Maximum output source current[3]		130	200	mA
I_{OL}	Maximum output sink current		5		mA
FDIV input (Pin 23)					
$V_{FDIV\ (P-P)}$	Input voltage (peak-to-peak value) t_{RISE} and $t_{FALL} \leqslant 40ns$	0.1		2	V
	Duty cycle	40		60	%
f_{MAX}	Maximum input frequency	14.5			MHz
Z_I	Input impedance		8		kΩ
C_I	Input capacitance		5		pF
OSC input (Pin 24)					
R_X	Crystal resistance at resonance (4MHz)			150	Ω

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltage, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
DAC outputs 0 to 7 (Pins 25 to 28 and 1 to 4)					
V_{DH}	Maximum output voltage (no load) at $V_{CC1} = 12V$[4]	10		11.5	V
V_{DL}	Minimum output voltage (no load) at $V_{CC1} = 12V$[4]	0.1		1	V
ΔV_D	Positive value of smallest step (1 least significant bit)	0		350	mV
	Deviation from linearity			0.5	V
Z_O	Output impedance at $I_{LOAD} = \pm 2mA$			70	Ω
$-I_{DH}$	Maximum output source current			6	mA
I_{DL}	Maximum output sink current		8		mA
Power-down reset					
V_{PD}	Maximum supply voltage V_{CC1} at which power-down reset is active	7.5		9.5	V
t_R	V_{CC1} rise time during power-up (up to V_{PD})	5			μs
Voltage level for valid module address					
	Voltage level at P20 (Pin 7) for valid module address as a function of MA1, MA0				
	MA1 MA0				
V_{VA00}	0 0	−0.3		16	V
V_{VA01}	0 1	−0.3		0.8	V
V_{VA10}	1 0	2.5		$V_{CC1} - 2$	V
V_{VA11}	1 1	$V_{CC1} - 0.3$		V_{CC1}	V

NOTES:

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{CC2} and I_{CC3}, respectively.
2. If $V_{CC1} < 1V$, the input current is limited to 10μA at input voltages up to 16V.
3. At continuous operation the output current should not exceed 50mA. When the output is short-circuited to ground for several seconds, the device may be damaged.
4. Values are proportional to V_{CC1}.

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4ms (or 2.56ms), controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC, and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHNO and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50kHz$ equals $250\mu A/\mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf=50kHz equals $2^6 \times 2^3 \times 250\mu A/\mu s$ (typical).

The maximum tuning current I is $875\mu A$ (typical). In the tuning-hold (TUHN) mode (TUHN is Active-LOW), the tuning current I is reduced and, as a consequence, the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable AFC hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, AFC will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The AFC has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and AFC to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner from being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs — P10 to P13 — which are capable of sourcing up to 50mA at a voltage drop of less than 600mV with respect to the separate power supply input V_{CC2}

For additional digital control, four open-collector I/O ports — P20 to P23 — are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analog converters — DACO to DAC7 — are provided for analog control.

Reset

CITAC goes into the power-down reset mode when V_{CC1} is below 8.5V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus. For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte, and a data/control byte, are written into CITAC in the format shown in Figure 1.

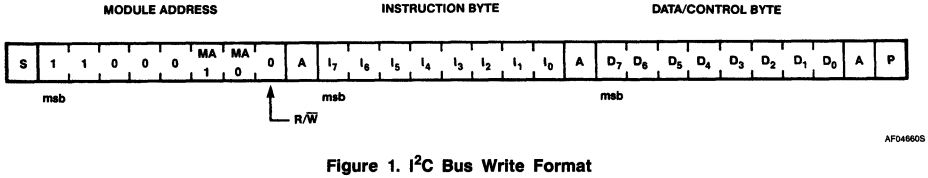


Figure 1. I^2C Bus Write Format

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down reset mode (V_{CC1} > 8.5V (typical)).

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

Frequency

Frequency is set when Bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50kHz. All frequency bits are set to logic 1 at reset.

Tuning Hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50kHz) into the tuning amplifier.

Table 1. Valid Module Addresses

MA1	MA0	P20
0	0	Don't care
0	1	GND
1	0	½ V_{CC1}
1	1	V_{CC1}

Table 2. Tuning Current Control

TUHN1	TUHN0	TYP. I_{MAX} (μA)	TYP. IT_{MIN} (μA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (μV)
0	0	3.5[1]	1[1]	1[1]
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

NOTE:
1. Values after reset.

During tuning but before lock-in, the highest current value should be selected. After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (maximum 5nA). However, it is good practice to program the lowest current value during tuner band switching.

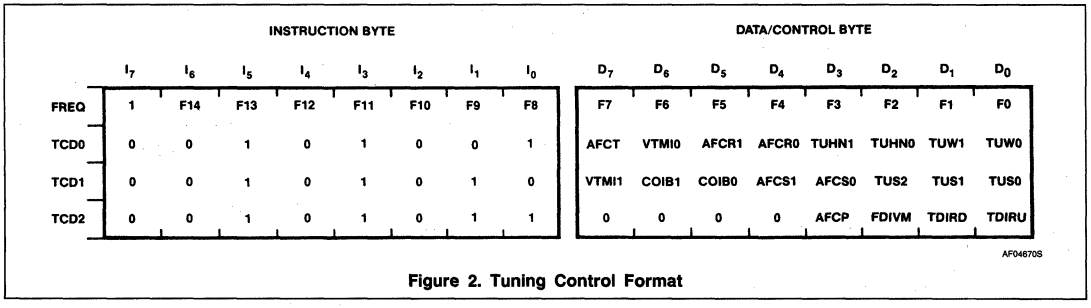


Figure 2. Tuning Control Format

Table 3. Minimum Charge IT as a Function of TUS Δf = 50kHz; TUHN0 = Logic 1; TUHN1 = Logic 1

TUS2	TUS1	TUS0	TYP. IT_{MIN} (mA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (mV)
0	0	0	0.25[1]	0.25[1]
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

NOTE:
1. Values after reset.

Table 4. Programming Correction-In-Band

COIB1	COIB0	CHARGE MULTIPLYING FACTORS AT TYPICAL VALUES OF V_{TUN} AT:			
		< 12V	12 to 18V	18 to 24V	> 24V
0	0	1[1]	1[1]	1[1]	1[1]
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

NOTE:
1. Values after reset.

Table 5. Tuning Window Programming

TUW1	TUW0	|Δf| (kHz)	TUNING WINDOW (kHz)
0	0	0[1]	0[1]
0	1	50	100
1	0	150	300

NOTE:
1. Values after reset.

Table 6. AFC Hold Range Programming

AFCR1	AFCR0	|Δf| (kHz)	AFC HOLD RANGE (kHz)
0	0	0[1]	0[1]
0	1	350	700
1	0	750	1500

NOTE:
1. Values after reset.

Table 7. Transconductance Programming

AFCS1	AFCS0	TYP. TRANSCONDUCTANCE (μA/V)
0	0	0.25[1]
0	1	25
1	0	50
1	1	100

NOTE:
1. Value after reset.

Tuning Sensitivity
To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf=50kHz; TUHN0 and TUHN1 = logic 1.

Correction-In-Band
This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

The transconductance multiplying factor of the AFC amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning Window
Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation |Δf| between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If |Δf| is up to 50kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

AFC
When AFCT is set to logic 1 it will not be cleared and the AFC will remain on as long as |Δf| is less than the value programmed for the AFC hold range AFCR (see Table 6). It is possible for the AFC to remain on for values of up to 50kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Transconductance
The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bits AFCS as shown in Table 7.

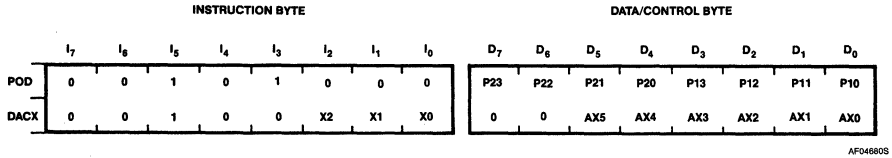


Figure 3. Control Programming

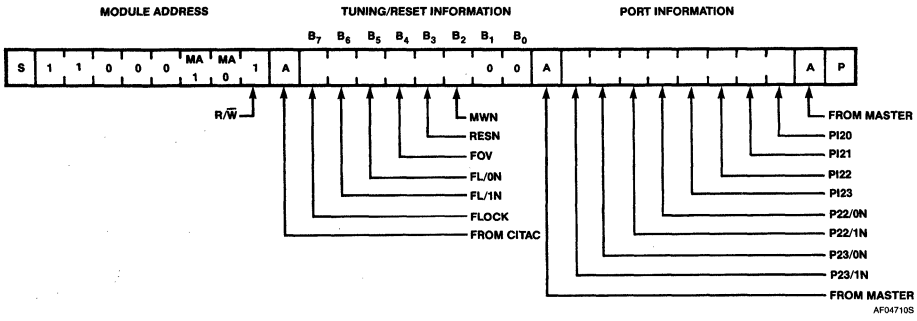


Figure 4. Information Byte Format

AFC Polarity

If a positive differential input voltage is applied to the (switched on) AFC amplifier, the tuning voltage V_{TUN} falls when the AFC polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum Tuning Voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in the DC Electrical Characteristics table.

Frequency Measuring Window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Tuning Direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analog converter control) are shown in Figure 3, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open-collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analog converters. The digital-to-analog converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

Table 8. Frequency Measuring Window Programming

FDIVM	PRESCALER DIVISION FACTOR	CYCLE PERIOD (ms)	MEASURING WINDOW (ms)
0	256	6.4[1]	5.12[1]
1	64	2.56	1.28

NOTE:
1. Values after reset.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master, the slave (CITAC) stops transmitting. The format of the information bytes is shown in Figure 4.

Tuning/Reset Information Bits

FLOCK — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.

FL/1N — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

FL/ON — As for FL/1N, but is set to logic 0 when FLOCK changes from 1 to 0.

FOV — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.

RESN — Set to logic 0 (Active-LOW) by a programmed reset or a power-down reset. It is reset to logic 1 automatically after tuning/reset information has been read.

MWN — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured.

When slightly different frequencies are programmed repeatedly and AFC is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port Information Bits

P23/1N, P22/1N — Set to logic 0 (Active-LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22, respectively. Both are reset to logic 1 after the port information has been read.

P23/0N, P22/0N — As for P23/1N and P22/1N, but are set to logic 0 at a HIGH-to-LOW transition.

PI23, PI21, PI20, PI — Indicate input voltage levels at P23, P22, P21, and P20, respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Figure 5. Reset is activated only at data byte HEX06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

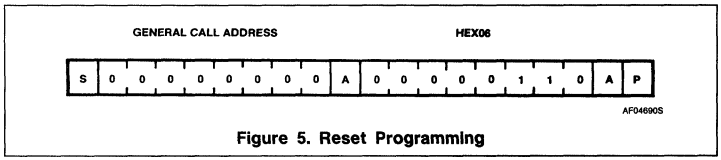


Figure 5. Reset Programming

I^2C BUS TIMING (Figure 6)

I^2C bus load conditions are as follows:

4kΩ pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			μs
t_{SU}, t_{STA}	Start condition setup time	4			μs
t_{HD}, t_{STA}	Start condition hold time	4			μs
t_{LOW}	SCL, SDA LOW period	4			μs
t_{HIGH}	SCL HIGH period	4			μs
t_R	SCL, SDA rise time			1	μs
t_F	SCL, SDA fall time			0.3	μs
t_{SU}, t_{DAT}	Data setup time (write)	1			μs
t_{HD}, t_{DAT}	Data hold time (write)	1			μs
t_{SU}, t_{CAC}	Acknowledge (from CITAC) setup time			2	μs
t_{HD}, t_{CAC}	Acknowledge (from CITAC) hold time	0			μs
t_{SU}, t_{STO}	Stop condition setup time	4			μs
t_{SU}, t_{RDA}	Data setup time (read)			2	μs
t_{HD}, t_{RDA}	Data hold time (read)	0			μs
t_{SU}, t_{MAC}	Acknowledge (from master) setup time	1			μs
t_{HD}, t_{MAC}	Acknowledge (from master) hold time	2			μs

NOTE:
Timings t_{SU}, t_{DAT} and t_{HD}, t_{DAT} deviate from the I^2C bus specification.
After reset has been activated, transmission may only be started after a 50μs delay.

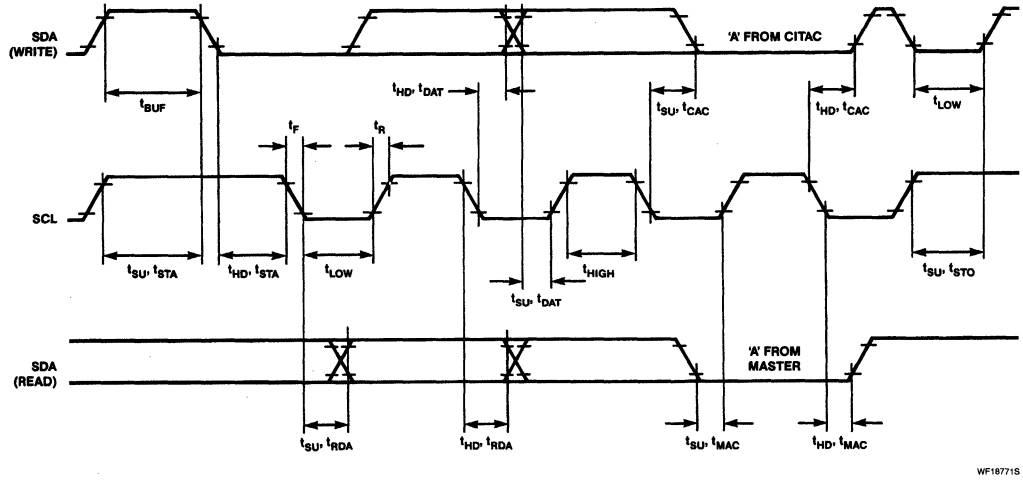


Figure 6. I^2C Bus Timing SAB3035

AN157
Microcomputer Peripheral IC Tunes and Controls a TV Set

Application Note

Linear Products

Author: K.H. Seidler

The necessity for television set manufacturers to reduce costs, provide more features, simplify tuning and incorporate remote control has led to a need for all-electronic digital tuning and control circuits. Naturally enough, component manufacturers would prefer to meet the need with a dedicated integrated system which they can make in large quantities. This, however, is impractical because it would not allow the set manufacturers to satisfy the widely varying requirements of the TV market. The most suitable system is therefore one controlled by a standard microcomputer (e.g., one from the MAB/SCN8400 family), so that the variants can be accommodated by software. The only additional components that then need to be separately integrated are those required for interfacing and for performing functions that cannot be handled by the microcomputer because of speed, voltage or power consumption considerations. To minimize costs and maximize performance, however, the partitioning of the remaining functions and their allocation to various integrated circuits peripheral to the microcomputer must be carefully considered.

Figure 1 illustrates the control and tuning functions in a basic TV set, and shows how the circuitry is positioned within the cabinet. Some of the functions are concentrated around the microcomputer and mounted close to the front panel to reduce the cost of the wiring to the local keyboard and displays. The tuning and analog controls are on the main chassis. The only link between the microcomputer and the main chassis is a 2-wire bidirectional I^2C bus which allows the microcomputer to read tuning status and other information from the main chassis, and to write data regarding required frequency and analog control settings to the main chassis.

The foregoing considerations have led to the design of the SAB3035 integrated Computer Interface for Tuning and Analog Control (CITAC). The SAB3035 is an I^2C bus-compatible microcomputer peripheral IC for digital frequency-locked loop (FLL) tuning and control of analog functions associated with the TV picture and sound. This is shown in block form in Figure 2. The IC incorporates a frequency synthesizer using the charge pump FLL principle and contains the following circuits:

- 15-bit frequency counter with a resolution of 50kHz
- Charge pump and 30V tuning-voltage amplifier
- AFC amplifier
- Logic circuitry for programming the currents for the charge pump and AFC amplifier
- Four high-current band switches
- Four general-purpose I/O ports for additional control functions
- A single-pin crystal-controlled 4MHz reference oscillator
- Receiving/transmitting logic for the 2-wire I^2C bus
- Eight static DACs for control of analog functions associated with the picture and sound.

FUNCTIONAL DESCRIPTION

I^2C Bus

The SAB3035 is microcomputer-controlled via an asynchronous, Inter-IC (I^2C) bus. The bus is a two-wire, bidirectional serial interconnect which allows integrated circuits to communicate with each other and pass control and data from one IC to another. The communication commences after a start code incorporating an IC address and ceases on receipt of a stop code. Every byte of transmitted data must be acknowledged by the IC that receives it. Data to be read must be clocked out of the IC by the microcomputer. The address byte includes a control bit which defines the read/write mode.

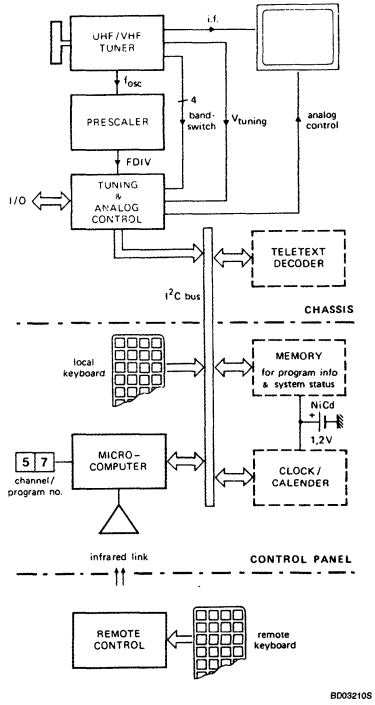


Figure 1. Basic TV Control System

Microcomputer Peripheral IC Tunes and Controls a TV Set

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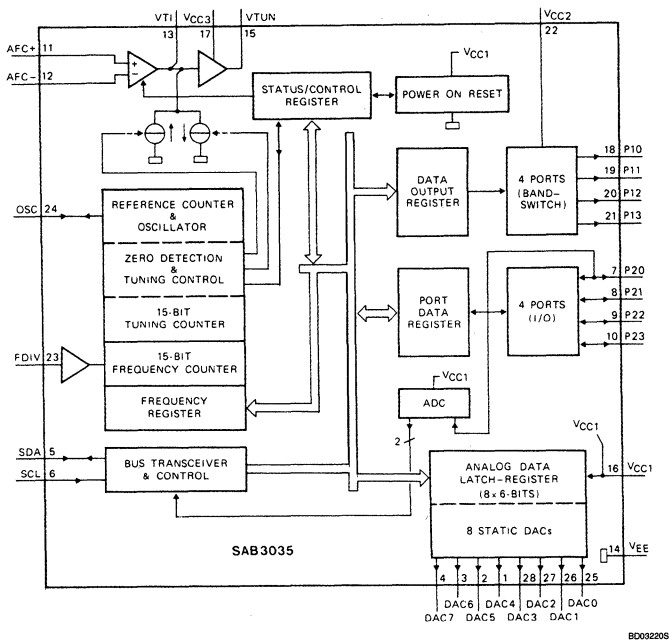

Figure 2. Block Diagram of the SAB3035

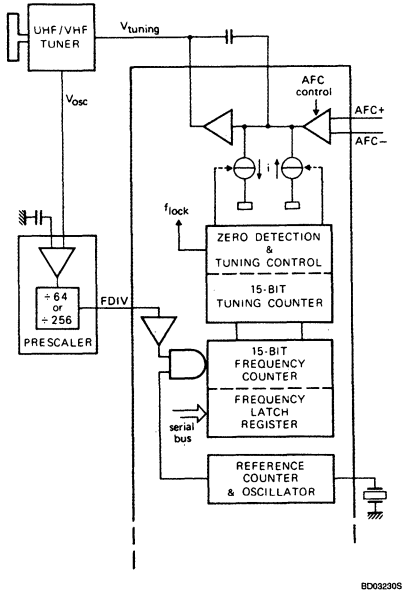

Figure 3. Block Diagram of the SAB3035

Frequency Synthesis Tuning System

Figure 3 is the block diagram of the frequency synthesizing system comprising a frequency-locked loop (FLL) and an external prescaler which divides the frequency of the voltage-controlled local oscillator in the TV tuner by 64 or 256. The tuning section comprises a 15-bit programmable frequency counter, a 15-bit tuning counter, tuning control and zero detection logic, a reference counter and a charge pump followed by a low-pass filter amplifier.

FDIV Input accepts frequency-divided local oscillator signals with a level of more than 100mV and a frequency of up to 16MHz. The frequency measurement period is defined by passing the internally-amplified signal from FDIV through a gate which is controlled by the reference counter. The reference counter is driven by a crystal-controlled oscillator, the low level output of which is almost free from high-order harmonics. This oscillator also generates the internal clock for the IC. Before starting the frequency measurement cycle, the 15 bits of data in the latch register, which represent the required local oscillator frequency, are loaded into the frequency counter. Pulses from the prescaler then decrement the frequency counter for the duration of the measurement period.

Microcomputer Peripheral IC Tunes and Controls a TV Set

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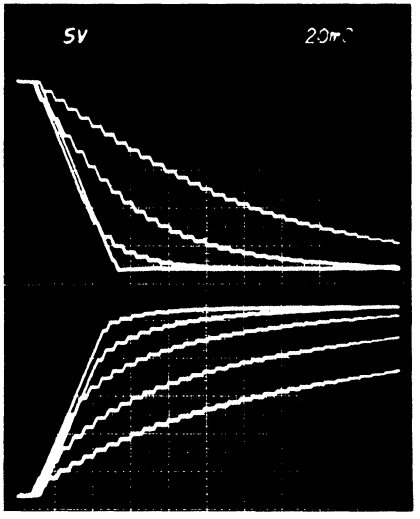
The contents of the frequency counter at the end of the measurement period indicate whether or not the frequency of the local oscillator in the tuner is the same as the desired frequency, which was preloaded into the frequency counter. If the frequency counter contents is zero after the measurement period, a flag (FLOCK), which can be read by the microcomputer serial bus, is set to indicate that the local-oscillator is correctly tuned.

A frequency counter contents of other than zero at the end of the measurement period indicates that the tuner local oscillator frequency is either too high (contents below zero) or too low (contents above zero). If it is too high, an overflow flag which initiates the "tuning down" function is set. To generate the tuning voltage correction, the tuning counter is loaded with the remaining contents of the frequency counter at the end of the measurement period, and then decremented to zero by an internal clock. The duration of the pulse applied to the charge pump is proportional to the time taken to decrement the tuning counter to zero, and therefore also proportional to the tuning error. The frequency correction has a resolution of 50kHz.

The frequency measurement method of tuning used in the SAB3035 can also be easily combined with analog AFC to allow tracking of a drifting transmitter frequency within a limited range. The required tuning mode (with or without AFC) is selected and controlled by software. By not testing some of the LSBs of the contents of the frequency counter, tune-in "windows" of ± 100kHz or ± 200kHz can be defined. The corresponding AFC "windows" are ± 400kHz or ± 800kHz. The SAB3035 also contains the AFC control logic and amplifier. To allow matching to a wide variety of tuners, the tuning loop gain and tuning speed can be adjusted over a wide range. To minimize sound on picture, a "tuning hold" mode is selectable in which the charge pump and AFC currents can be reduced when correct tuning has been achieved.

Bandswitching

The IC also incorporates four 50 mA current sources with outputs at ports P10 to P13 for executing band switching instructions from the microcomputer. Bandswitching data is stored in the data output register. The supply voltage for the current sources is derived from a separate input (V_{CC2}) and is therefore independent of the logic supply voltage (V_{CC1}).



WF16220S

NOTES:
Decreasing frequency (top)
Increasing frequency (bottom)

Figure 4. Using Some of the Selectable Charge Pump Currents for Making 50kHz Tuning Steps in the UHF Band

I/O Ports

There are four bidirectional ports P20 to P23 for additional control signals to or from the TV receiver. Typical examples of these additional controls are stereo/dual sound, search tuning and switching for external video sources. The output data for ports P20 to P23 is stored in the port data register.

Input data must be present during the read cycle. Two of the inputs are edge-triggered. Each input signal transition is stored and can be read by the microcomputer via the serial data bus. The stored data is cleared after each read cycle.

Analog Controls

The SAB3035 includes eight static DACs for controlling analog functions associated with the TV picture and sound (volume, tone, brightness, contrast, color saturation, etc.). External RC networks are not necessary to complete the D/A conversion. The control data for the DACs is derived from the serial data bus and stored in eight 6-bit latch registers. The output voltage range at DAC0 to DAC7 is 0.5V to 10.5V and can be adjusted in 64 increments.

ACKNOWLEDGEMENTS

Special thanks are due to F.A.v.d.Kerkhof and B.Strassenburg for their contributions, and to M.F.Geurts for the electrical design of the SAB3035.

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Microcomputer Peripheral IC Tunes and Controls a TV Set

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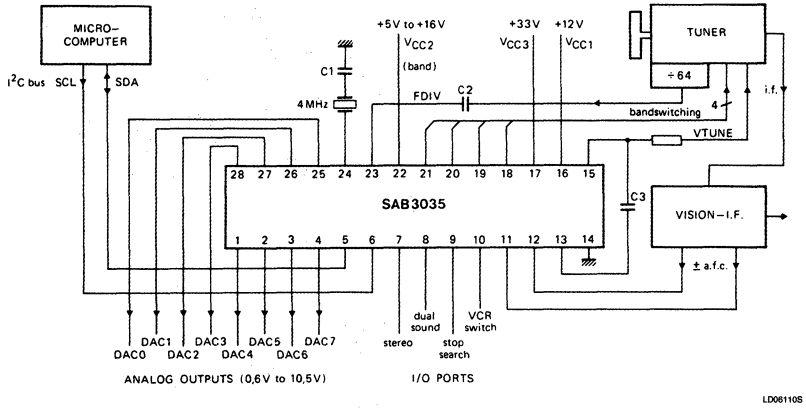


Figure 5. This Typical Example of the SAB3035 in a TV Tuning and Control System Shows how the Peripheral Components Have Been Reduced to Three Capacitors, a Resistor and a 4MHz Crystal

NOTE:
Originally published as Technical Publication 097, Electronic Components and Applications, Vol. 5 No. 2, February, 1983, the Netherlands.

SAB3036
FLL Tuning and Control Circuit

Product Specification

Linear Products

DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I^2C bus.

FEATURES

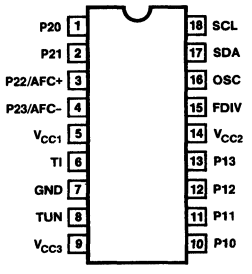
- **Combined analog and digital circuitry minimizes the number of additional interfacing components required**
- **Frequency measurement with resolution of 50kHz**
- **Selectable prescaler divisor of 64 or 256**
- **32V tuning voltage amplifier**
- **4 high-current outputs for direct band selection**
- **Four general purpose input/output (I/O) ports**
- **Tuning with control of speed and direction**
- **Tuning with or without AFC**
- **Single-pin, 4MHz on-chip oscillator**
- **I^2C bus slave transceiver**

APPLICATIONS

- **TV receivers**
- **Satellite receivers**
- **CATV converters**

PIN CONFIGURATION

N Package



TOP VIEW

CD11960S

PIN NO.	SYMBOL	DESCRIPTION
1	P20	General purpose
2	P21	Input/output ports
3	P22/AFC+	General purpose input/output
4	P23/AFC−	ports and AFC inputs
5	V_{CC1}	+12V supply voltage
6	TI	Tuning voltage amplifier inverting input
7	GND	Ground
8	TUN	Tuning voltage amplifier output
9	V_{CC3}	+32V supply for tuning voltage amplifier
10	P10	High-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{CC2}	Positive supply for high-current band-selection output circuits
15	FDIV	Input from prescaler
16	OSC	Crystal oscillator input
17	SDA	Serial data line (I^2C bus)
18	SCL	Serial clock line (I^2C bus)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−20°C to +70°C	SAB3036N

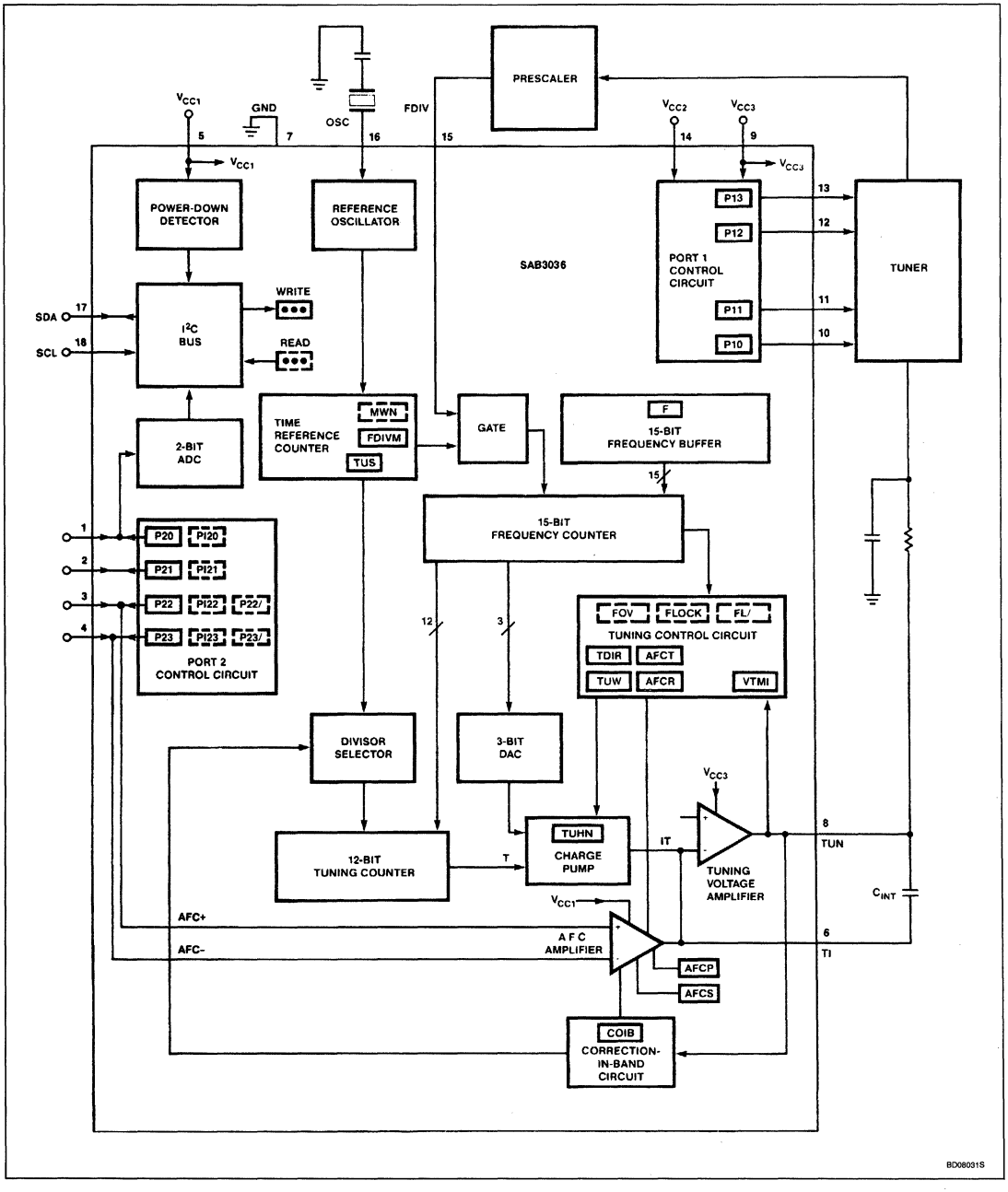
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges:		
V_{CC1}	(Pin 5)	−0.3 to +18	V
V_{CC2}	(Pin 14)	−0.3 to +18	V
V_{CC3}	(Pin 9)	−0.3 to +36	V
	Input/output voltage ranges:		
V_{SDA}	(Pin 17)	−0.3 to +18	V
V_{SCL}	(Pin 18)	−0.3 to +18	V
$V_{P20, P21}$	(Pins 1 and 2)	−0.3 to +18	V
$V_{P22, P23, AFC}$	(Pins 3 and 4)	−0.3 to V_{CC1} [1]	V
V_{TI}	(Pin 6)	−0.3 to V_{CC1} [1]	V
V_{TUN}	(Pin 8)	−0.3 to V_{CC3}	V
V_{P1X}	(Pins 10 to 13)	−0.3 to V_{CC2} [2]	V
V_{FDIV}	(Pin 15)	−0.3 to V_{CC1} [1]	V
V_{OSC}	(Pin 16)	−0.3 to +5	V
P_{TOT}	Total power dissipation	1000	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

NOTES:

1. Pin voltage may exceed supply voltage if current is limited to 10mA.
2. Pin voltage must not exceed 18V but may exceed V_{CC2} if current is limited to 200mA.

BLOCK DIAGRAM



4

DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC1}	Supply voltages	10.5	12	13.5	V
V_{CC2}		4.7	13	16	V
V_{CC3}		30	32	35	V
I_{CC1}	Supply currents (no outputs loaded)	14	23	40	mA
I_{CC2}		0		0.1	mA
I_{CC3}		0.2	0.6	2	mA
I_{CC2A}	Additional supply currents (A)[1]	−2		I_{OHP1X}	mA
I_{CC3A}		0.2		2	mA
P_{TOT}	Total power dissipation		300		mW
T_A	Operating ambient temperature	−20		+70	°C
I²C bus inputs/outputs SDA input (Pin 17); SCL input (Pin 18)					
V_{IH}	Input voltage HIGH[2]	3		$V_{CC1} - 1$	V
V_{IL}	Input voltage LOW	−0.3		1.5	V
I_{IH}	Input current HIGH[2]			10	μA
I_{IL}	Input current LOW[2]			10	μA
	SDA output (Pin 17, open-collector)				
V_{OL}	Output voltage LOW at $I_{OL} = 3mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
Open-collector I/O ports P20, P21, P22, P23 (Pins 1 to 4, open-collector)					
V_{IH}	Input voltage HIGH (P20, P21)	2		16	V
V_{IH}	Input voltage HIGH (P22, P23) AFC switched off	2		$V_{CC1} - 2$	V
V_{IL}	Input voltage LOW	−0.3		0.8	V
I_{IH}	Input current HIGH			25	μA
$-I_{IL}$	Input current LOW			25	μA
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
I_{OL}	Maximum output sink current		4		mA
AFC amplifier Inputs AFC+, AFC− (Pins 3, 4)					
	Transconductance for input voltage up to 1V differential: AFCS1 AFCS2				
g_{00}	0 0	100	250	800	nA/V
g_{01}	0 1	15	25	35	μA/V
g_{10}	1 0	30	50	70	μA/V
g_{11}	1 1	60	100	140	μA/V
ΔM_g	Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	−20		+20	%
V_{IOFF}	Input offset voltage	−75		+75	mV
V_{COM}	Common-mode input voltage	3		$V_{CC1} - 2.5$	V
CMRR	Common-mode rejection ratio		50		dB
PSRR	Power supply (V_{CC1}) rejection ratio		50		dB
I_I	Input current (P22 and P23 programmed HIGH)			500	nA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuning voltage amplifier Input TI, output TUN (Pins 6, 8)					
V_{TUN}	Maximum output voltage at $I_{LOAD} = \pm 2.5mA$	$V_{CC3} - 1.6$		$V_{CC3} - 0.4$	V
	Minimum output voltage at $I_{LOAD} = \pm 2.5mA$: VTMI1 VTMI0				
V_{TM00}	0 0	300		500	mV
V_{TM10}	1 0	450		650	mV
V_{TM11}	1 1	650		900	mV
$-I_{TUNH}$	Maximum output source current	2.5		8	mA
I_{TUNL}	Maximum output sink current		40		mA
I_{TI}	Input bias current	−5		+5	nA
PSRR	Power supply (V_{CC3}) rejection ratio		60		dB
	Minimum charge IT to tuning voltage amplifier TUHN1 TUHN0				
CH_{00}	0 0	0.4	1	1.7	µA/µs
CH_{01}	0 1	4	8	14	µA/µs
CH_{10}	1 0	15	30	48	µA/µs
CH_{11}	1 1	130	250	370	µA/µs
ΔCH	Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	−20		+20	%
	Maximum current I into tuning amplifier TUHN1 TUHN0				
I_{T00}	0 0	1.7	3.5	5.1	µA
I_{T01}	0 1	15	29	41	µA
I_{T10}	1 0	65	110	160	µA
I_{T11}	1 1	530	875	1220	µA
Correction-in-band					
ΔV_{CIB}	Tolerance of correction-in-band levels 12V, 18V and 24V	−15		+15	%
Band-select output ports P10, P11, P12, P13 (Pins 10 to 13)					
V_{OH}	Output voltage HIGH at $-I_{OH} = 50mA$[3]	$V_{CC2} - 0.6$			V
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
$-I_{OH}$	Maximum output source current[3]		130	200	mA
I_{OL}	Maximum output sink current		5		mA
FDIV input (Pin 15)					
$V_{FDIV\ (P-P)}$	Input voltage (peak-to-peak value) (t_{RISE} and $t_{FALL} \leqslant 40ns$)	0.1		2	V
	Duty cycle	40		60	%
f_{MAX}	Maximum input frequency	16			MHz
Z_I	Input impedance		8		kΩ
C_I	Input capacitance		5		pF

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
OSC Input (Pin 24)					
R_X	Crystal resistance at resonance (4MHz)			150	Ω
Power-down reset					
V_{PD}	Maximum supply voltage V_{CC1} at which power-down reset is active	7.5		9.5	V
t_R	V_{CC1} rise time during power-up (up to V_{PD})	5			μs
Voltage level for valid module address					
	Voltage level at P20 (Pin 1) for valid module address as a function of MA1, MA0				
	MA1 MA0				
V_{VA00}	0 0	−0.3		16	V
V_{VA01}	0 1	−0.3		0.8	V
V_{VA10}	1 0	2.5		$V_{CC1} - 2$	V
V_{VA11}	1 1	$V_{CC1} - 0.3$		V_{CC1}	V

NOTES:
1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{CC2} and I_{CC3}, respectively.
2. If $V_{CC1} < 1V$, the input current is limited to 10μA at input voltages up to 16V.
3. At continuous operation the output current should not exceed 50mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{CC1}.

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4ms (or 2.56ms), controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50kHz$ equals 250μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50kHz$ equals $2^6 \times 2^3 \times 250\mu A\mu s$ (typical).

The maximum tuning current I is 875μA (typical). In the tuning-hold (TUHN) mode (TUHN is Active-LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable AFC hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, AFC will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The AFC has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and AFC to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs — P10 to P13 — which are capable of sourcing up to 50mA at a voltage drop of less than 600mV with respect to the separate power supply input V_{CC2}.

For additional digital control, four open-collector I/O ports — P20 to P23 — are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC– inputs, respectively. The AFC amplifier must be switched off when P22 and/or P23 are used. When AFC is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down reset mode when V_{CC1} is below 8.5V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus. For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Figure 1.

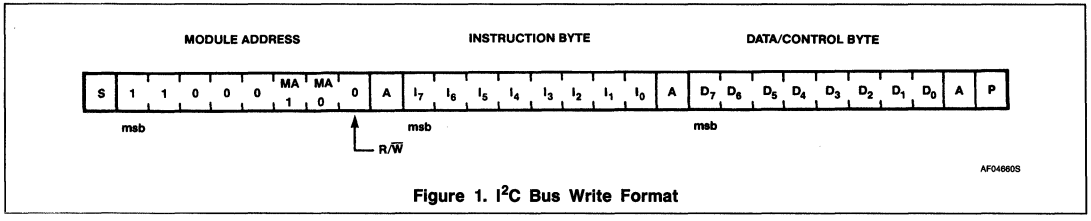


Figure 1. I^2C Bus Write Format

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down reset mode (V_{CC1} > 8.5V (typical)).

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

Frequency

Frequency is set when Bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50kHz. All frequency bits are set to logic 1 at reset.

Tuning Hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50kHz) into the tuning amplifier.

During tuning but before lock-in, the highest current value should be selected. After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (maximum 5nA). However, it is good practice to program the lowest current value during tuner band switching.

Tuning Sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50kHz; TUHN0 and TUHN1 = logic 1.

Table 1. Valid Module Addresses

MA1	MA0	P20
0	0	Don't care
0	1	GND
1	0	½ V_{CC1}
1	1	V_{CC1}

Table 2. Tuning Current Control

TUHN1	TUHN0	TYP. I_{MAX} (μA)	TYP. IT_{MIN} (μA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (μV)
0	0	3.5[1]	1[1]	1[1]
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

NOTE:
1. Values after reset.

Table 3. Minimum Charge IT as a Function of TUS Δf = 50kHz; TUHN0 = Logic 1; TUHN1 = Logic 1

TUS2	TUS1	TUS0	TYP. IT_{MIN} (mA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (mV)
0	0	0	0.25[1]	0.25[1]
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

NOTE:
1. Values after reset.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
FREQ	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

AF04670S

Figure 2. Tuning Control Format

Correction-In-Band
This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

The transconductance multiplying factor of the AFC amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning Window
Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

AFC
When AFCT is set to logic 1 it will not be cleared and the AFC will remain on as long as $|\Delta f|$ is less than the value programmed for the AFC hold range AFCR (see Table 6). It is possible for the AFC to remain on for values of up to 50kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Transconductance
The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bits AFCS as shown in Table 7.

AFC Polarity
If a positive differential input voltage is applied to the (switched on) AFC amplifier, the tuning voltage V_{TUN} falls when the AFC polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum Tuning Voltage
Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency Measuring Window
The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Tuning Direction
Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Table 4. Programming Correction-In-Band

COIB1	COIB0	CHARGE MULTIPLYING FACTORS AT TYPICAL VALUES OF V_{TUN} AT:			
		< 12V	12 to 18V	18 to 24V	> 24V
0	0	1[1]	1[1]	1[1]	1[1]
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

NOTE:
1. Values after reset.

Table 5. Tuning Window Programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	TUNING WINDOW (kHz)
0	0	0[1]	0[1]
0	1	50	100
1	0	150	300

NOTE:
1. Values after reset.

Table 6. AFC Hold Range Programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	AFC HOLD RANGE (kHz)
0	0	0[1]	0[1]
0	1	350	700
1	0	750	1500

NOTE:
1. Values after reset.

Table 7. Transconductance Programming

AFCS1	AFCS0	TYP. TRANSCONDUCTANCE (μA/V)
0	0	0.25[1]
0	1	25
1	0	50
1	1	100

NOTE:
1. Value after reset.

Table 8. Frequency Measuring Window Programming

FDIVM	PRESCALER DIVISION FACTOR	CYCLE PERIOD (ms)	MEASURING WINDOW (ms)
0	256	6.4[1]	5.12[1]
1	64	2.56	1.28

NOTE:
1. Values after reset.

Control

The instruction byte POD (port output data) is shown in Figure 3, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open-collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Figure 4.

Tuning/Reset Information Bits

FLOCK — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.

FL/1N — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

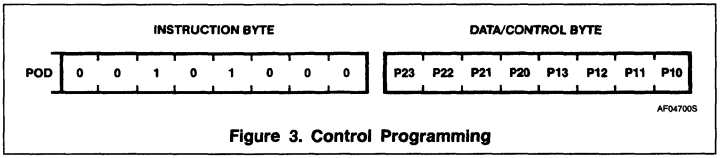


Figure 3. Control Programming

FL/ON — As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.

FOV — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.

RESN — Set to logic 0 (Active-LOW) by a programmed reset or a power-down reset. It is reset to logic 1 automatically after tuning/reset information has been read.

MWN — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured.

When slightly different frequencies are programmed repeatedly and AFC is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port Information Bits

P23/1N, P22/1N — Set to logic 0 (Active-LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22, respectively. Both are reset to logic 1 after the port information has been read.

P23/0N, P22/0N — As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.

P123, P122, P121, P120 — Indicate input voltage levels at P23, P22, P21 and P20, respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Figure 5. Reset is activated only at data byte HEX06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

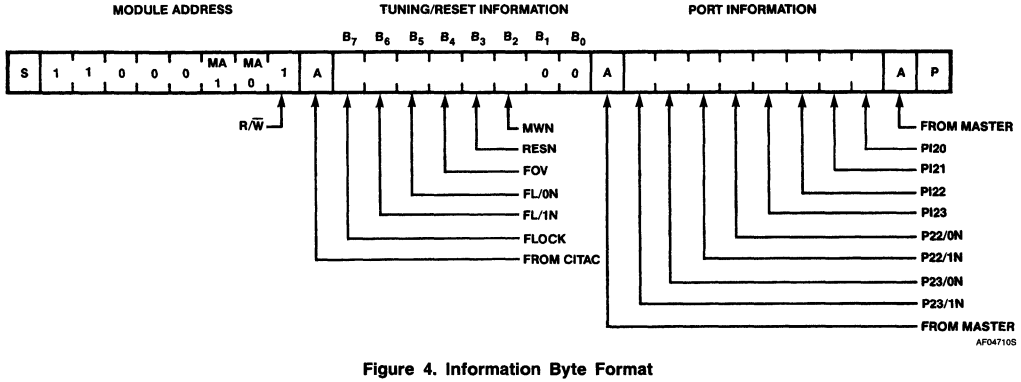


Figure 4. Information Byte Format

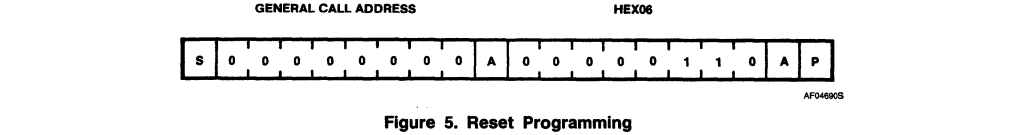


Figure 5. Reset Programming

I²C Bus Timing

I²C bus load conditions are as follows:

4kΩ pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			µs
t_{SU}, t_{STA}	Start condition setup time	4			µs
t_{HD}, t_{STA}	Start condition hold time	4			µs
t_{LOW}	SCL, SDA LOW period	4			µs
t_{HIGH}	SCL HIGH period	4			µs
t_R	SCL, SDA rise time			1	µs
t_F	SCL, SDA fall time			0.3	µs
t_{SU}, t_{DAT}	Data setup time (write)	1			µs
t_{HD}, t_{DAT}	Data hold time (write)	1			µs
t_{SU}, t_{CAC}	Acknowledge (from CITAC) setup time			2	µs
t_{HD}, t_{CAC}	Acknowledge (from CITAC) hold time	0			µs
t_{SU}, t_{STO}	Stop condition setup time	4			µs
t_{SU}, t_{RDA}	Data setup time (read)			2	µs
t_{HD}, t_{RDA}	Data hold time (read)	0			µs
t_{SU}, t_{MAC}	Acknowledge (from master) setup time	1			µs
t_{HD}, t_{MAC}	Acknowledge (from master) hold time	2			µs

NOTE:

1. Timings t_{SU}, t_{DAT} and t_{HD}, t_{DAT} deviate from the I²C bus specification.
   After reset has been activated, transmission may only be started after a 50µs delay.

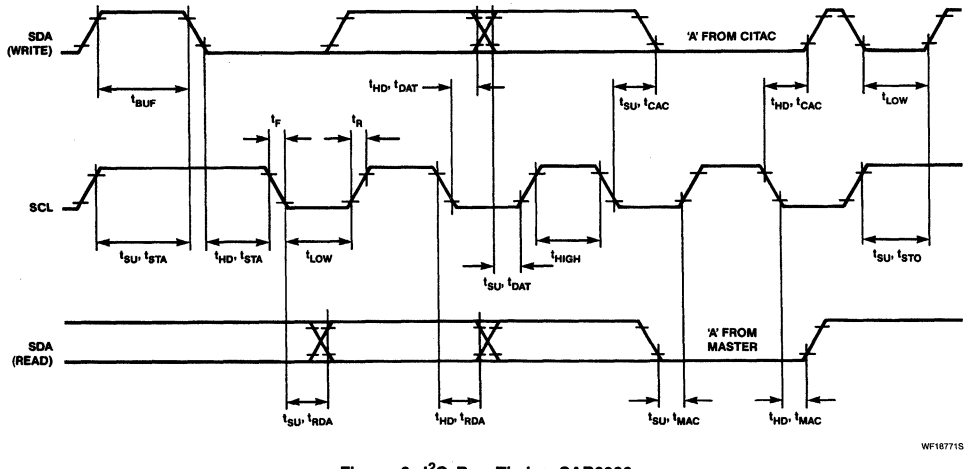


Figure 6. I²C Bus Timing SAB3036

SAB3037
FLL Tuning and Control Circuit

Product Specification

Linear Products

DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It also controls up to 4 analog functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I^2C bus.

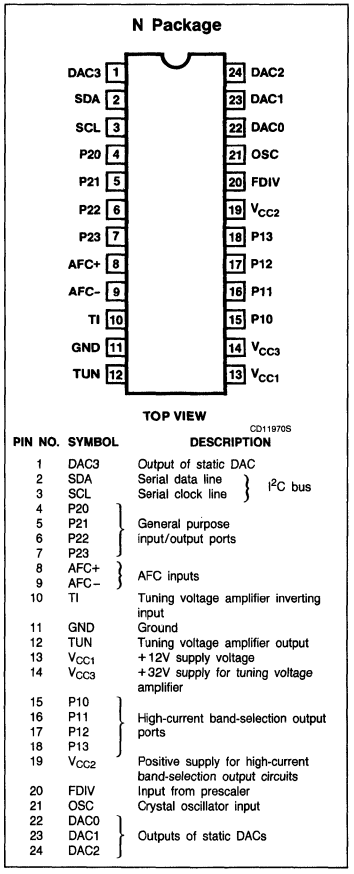
FEATURES

- **Combined analog and digital circuitry minimizes the number of additional interfacing components required**
- **Frequency measurement with resolution of 50kHz**
- **Selectable prescaler divisor of 64 or 256**
- **32V tuning voltage amplifier**
- **4 high-current outputs for direct band selection**
- **4 static digital to analog convertors (DACs) for control of analog functions**
- **Four general purpose input/output (I/O) ports**
- **Tuning with control of speed and direction**
- **Tuning with or without AFC**
- **Single-pin, 4MHz on-chip oscillator**
- **I^2C bus slave transceiver**

APPLICATIONS

- **TV receivers**
- **Satellite receivers**
- **CATV converters**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	DAC3	Output of static DAC
2	SDA	Serial data line } I^2C bus
3	SCL	Serial clock line } I^2C bus
4	P20	General purpose input/output ports
5	P21	
6	P22	
7	P23	
8	AFC+	AFC inputs
9	AFC−	
10	TI	Tuning voltage amplifier inverting input
11	GND	Ground
12	TUN	Tuning voltage amplifier output
13	V_{CC1}	+12V supply voltage
14	V_{CC3}	+32V supply for tuning voltage amplifier
15	P10	High-current band-selection output ports
16	P11	
17	P12	
18	P13	
19	V_{CC2}	Positive supply for high-current band-selection output circuits
20	FDIV	Input from prescaler
21	OSC	Crystal oscillator input
22	DAC0	Outputs of static DACs
23	DAC1	
24	DAC2	

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−20°C to +70°C	SAB3037N

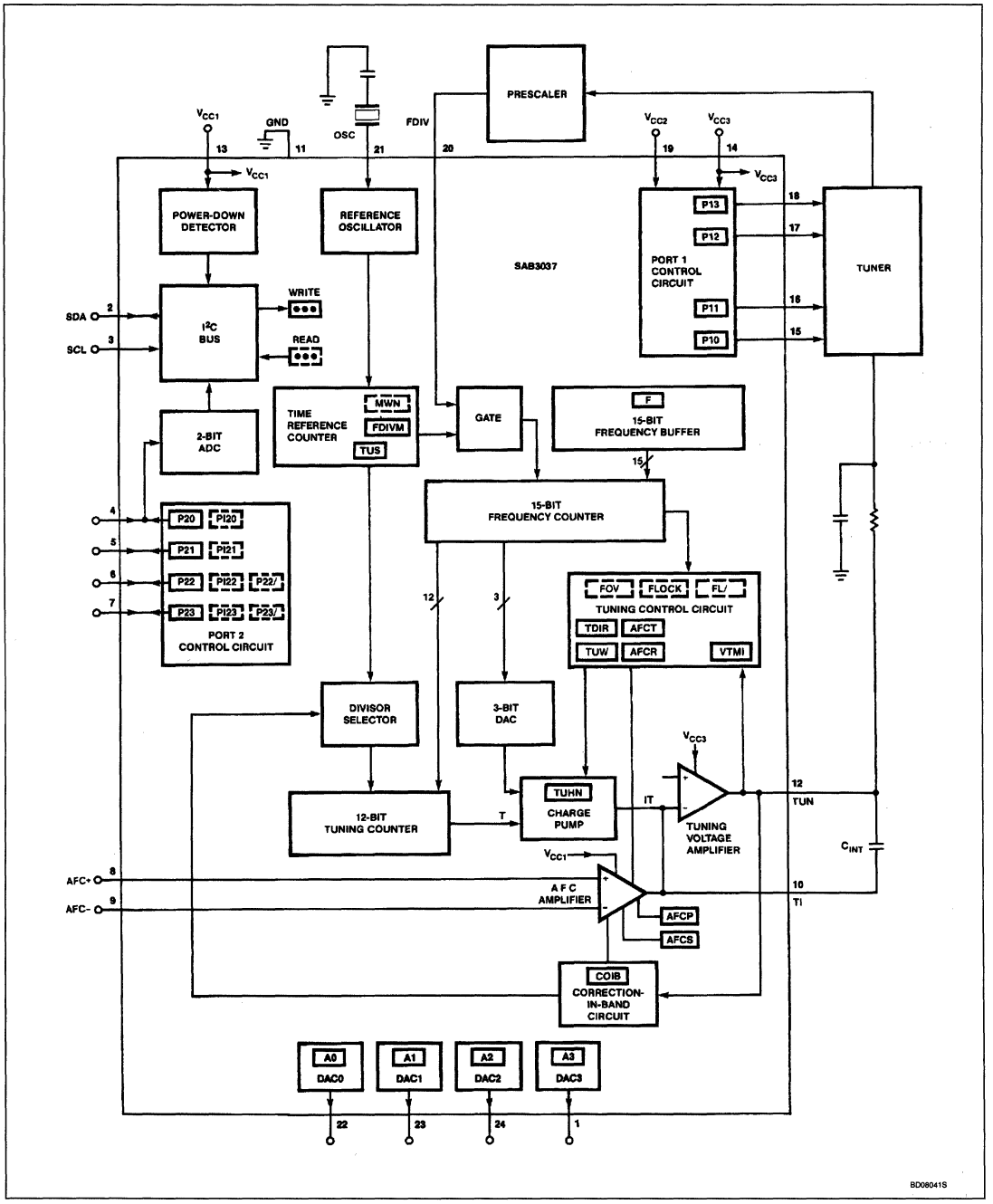
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges:		
V_{CC1}	(Pin 13)	−0.3 to +18	V
V_{CC2}	(Pin 19)	−0.3 to +18	V
V_{CC3}	(Pin 14)	−0.3 to +36	V
	Input/output voltage ranges:		
V_{SDA}	(Pin 2)	−0.3 to +18	V
V_{SCL}	(Pin 3)	−0.3 to +18	V
V_{P2X}	(Pins 4 to 7)	−0.3 to +18	V
$V_{AFC+, AFC-}$	(Pins 8 and 9)	−0.3 to V_{CC1} [1]	V
V_{TI}	(Pin 10)	−0.3 to V_{CC1} [1]	V
V_{TUN}	(Pin 12)	−0.3 to V_{CC3} [3]	V
V_{P1X}	(Pins 15 to 18)	−0.3 to V_{CC2} [3]	V
V_{FDIV}	(Pin 20)	−0.3 to V_{CC1} [1]	V
V_{OSC}	(Pin 21)	−0.3 to +5	V
V_{DACX}	(Pins 1 and 22 to 24)	−0.3 to V_{CC} [1]	V
P_{TOT}	Total power dissipation	1000	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

NOTES:

1. Pin voltage may exceed supply voltage if current is limited to 10mA.
2. Pin voltage must not exceed 18V but may exceed V_{CC2} if current is limited to 200mA.

BLOCK DIAGRAM



4

DC AND AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC1}	Supply voltages	10.5	12	13.5	V
V_{CC2}		4.7	13	16	V
V_{CC3}		30	32	35	V
I_{CC1}	Supply currents (no outputs loaded)	18	30	45	mA
I_{CC2}		0		0.1	mA
I_{CC3}		0.2	0.6	2	mA
I_{CC2A}	Additional supply currents (A)[1]	−2		I_{OHP1X}	mA
I_{CC3A}		0.2		2	mA
P_{TOT}	Total power dissipation		380		mW
T_A	Operating ambient temperature	−20		+70	°C
I²C bus inputs/outputs SDA input (Pin 2); SCL input (Pin 3)					
V_{IH}	Input voltage HIGH[2]	3		$V_{CC}-1$	V
V_{IL}	Input voltage LOW	−0.3		1.5	V
I_{IH}	Input current HIGH[2]			10	μA
I_{IL}	Input current LOW[2]			10	μA
	SDA output (Pin 2, open-collector)				
V_{OL}	Output voltage LOW at $I_{OL} = 3mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
Open-collector I/O ports P20, P21, P22, P23 (Pins 4 to 7, open-collector)					
V_{IH}	Input voltage HIGH	2		16	V
V_{IL}	Input voltage LOW	−0.3		0.8	V
I_{IH}	Input current HIGH			25	μA
$-I_{IL}$	Input current LOW			25	μA
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
I_{OL}	Maximum output sink current		4		mA
AFC amplifier Inputs AFC+, AFC− (Pins 8, 9)					
	Transconductance for input voltages up to 1V differential: AFCS1 AFCS2				
g00	0 0	100	250	800	nA/V
g01	0 1	15	25	35	μA/V
g10	1 0	30	50	70	μA/V
g11	1 1	60	100	140	μA/V
ΔM_g	Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	−20		+20	%
V_{IOFF}	Input offset voltage	−75		+75	mV
V_{COM}	Common-mode input voltage	3		$V_{CC1}-2.5$	V
CMRR	Common-mode rejection ratio		50		dB
PSRR	Power supply (V_{CC1}) rejection ratio		50		dB
I_I	Input current			500	nA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuning voltage amplifier Input TI, output TUN (Pins 10, 12)					
V_{TUN}	Maximum output voltage at $I_{LOAD} = \pm 2.5mA$	$V_{CC3} - 1.6$		$V_{CC3} - 0.4$	V
	Minimum output voltage at $I_{LOAD} = \pm 2.5mA$: VTMI1 VTMI0				
V_{TM00}	0 0	300		500	mV
V_{TM10}	1 0	450		650	mV
V_{TM11}	1 1	650		900	mV
$-I_{TUNH}$	Maximum output source current	2.5		8	mA
I_{TUNL}	Maximum output sink current		40		mA
I_{TI}	Input bias current	−5		+5	nA
PSRR	Power supply V_{CC3} rejection ratio		60		dB
	Minimum charge IT to tuning voltage amplifier TUHN1 TUHN0				
CH_{00}	0 0	0.4	1	1.7	µA/µs
CH_{01}	0 1	4	8	14	µA/µs
CH_{10}	1 0	15	30	48	µA/µs
CH_{11}	1 1	130	250	370	µA/µs
ΔCH	Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	−20		+20	%
	Maximum current I into tuning amplifier TUHN1 TUHN0				
I_{T00}	0 0	1.7	3.5	5.1	µA
I_{T01}	0 1	15	29	41	µA
I_{T10}	1 0	65	110	160	µA
I_{T11}	1 1	530	875	1220	µA
Correction-in-band					
ΔV_{CIB}	Tolerance of correction-in-band levels 12V, 18V, and 24V	−15		+15	%
Band-select output ports P10, P11, P12, P13 (Pins 15 to 18)					
V_{OH}	Output voltage HIGH at $-I_{OH} = 50mA$[3]	$V_{CC2} - 0.6$			V
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
$-I_{OH}$	Maximum output source current[3]		130	200	mA
I_{OL}	Maximum output sink current		5		mA
FDIV input (Pin 20)					
$V_{FDIV\ (P-P)}$	Input voltage (peak-to-peak value) (t_{RISE} and $t_{FALL} \leqslant 40ns$)	0.1		2	V
	Duty cycle	40		60	%
f_{MAX}	Maximum input frequency	14.5			MHz
Z_I	Input impedance		8		kΩ
C_I	Input capacitance		5		pF
OSC input (Pin 21)					
R_X	Crystal resistance at resonance (4MHz)			150	Ω

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
DAC outputs 0 to 3 (Pins 22 to 24 and Pin 1)					
V_{DH}	Maximum output voltage (no load) at $V_{CC1} = 12V$[4]	10		11.5	V
V_{DL}	Minimum output voltage (no load) at $V_{CC1} = 12V$[4]	0.1		1	V
ΔV_D	Positive value of smallest step (1 least significant bit)	0		350	mV
	Deviation from linearity			0.5	V
Z_O	Output impedance at $I_{LOAD} = \pm 2mA$			70	Ω
$-I_{DH}$	Maximum output source current			6	mA
I_{DL}	Maximum output sink current		8		mA
Power-down reset					
V_{PD}	Maximum supply voltage V_{CC1} at which power-down reset is active	7.5		9.5	V
t_R	V_{CC1} rise time during power-up (up to V_{PD})	5			μs
Voltage level for valid module address					
	Voltage level at P20 (Pin 4) for valid module address as a function of MA1, MA0				
	MA1 MA0				
V_{VA00}	0 0	−0.3		16	V
V_{VA01}	0 1	−0.3		0.8	V
V_{VA10}	1 0	2.5		$V_{CC1} - 2$	V
V_{VA11}	1 1	$V_{CC1} - 0.3$		V_{CC1}	V

NOTES:
1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{CC2} and I_{CC3}, respectively.
2. If $V_{CC1} < 1V$, the input current is limited to 10μA at input voltages up to 16V.
3. At continuous operation the output current should not exceed 50mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{CC1}.

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4ms (or 2.56ms), controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1 (see OPERATION) the minimum charge IT at $\Delta f = 50kHz$ equals $250\mu A/\mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50kHz$ equals $2^6 \times 2^3 \times 250\mu A/\mu s$ (typical).

The maximum tuning current I is $875\mu A$ (typical). In the tuning-hold (TUHN) mode (TUHN is Active-LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable AFC hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, AFC will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The AFC has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and AFC to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner from being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs — P10 to P13 — which are capable of sourcing up to 50mA at a voltage drop of less than 600mV with respect to the separate power supply input V_{CC2}.

For additional digital control, four open-collector I/O ports — P20 to P23 — are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analog converters — DAC0 to DAC3 — are provided for analog control.

Reset

CITAC goes into the power-down reset mode when V_{CC1} is below 8.5V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus. For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Figure 1.

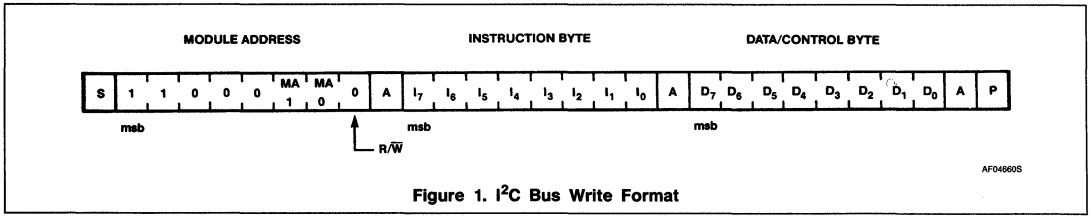


Figure 1. I^2C Bus Write Format

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down reset mode (V_{CC1} > 8.5V (typical)).

Table 1. Valid Module Addresses

MA1	MA0	P20
0	0	Don't care
0	1	GND
1	0	½ V_{CC1}
1	1	V_{CC1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

Frequency

Frequency is set when Bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50kHz. All frequency bits are set to logic 1 at reset.

Tuning Hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50kHz) into the tuning amplifier.

Table 2. Tuning Current Control

TUHN1	TUHN0	TYP. I_{MAX} (μA)	TYP. IT_{MIN} (μA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (μV)
0	0	3.5[1]	1[1]	1[1]
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

NOTE:
1. Values after reset.

During tuning but before lock-in, the highest current value should be selected. After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (maximum 5nA). However, it is good practice to program the lowest current value during tuner band switching.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
FREQ	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

AF04670S

Figure 2. Tuning Control Format

Table 3. Minimum Charge IT as a Function of TUS Δf = 50kHz; TUHN0 = Logic 1; TUHN1 = Logic 1

TUS2	TUS1	TUS0	TYP. IT_{MIN} (mA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (mV)
0	0	0	0.25[1]	0.25[1]
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

NOTE:
1. Values after reset.

Table 4. Programming Correction-In-Band

COIB1	COIB0	CHARGE MULTIPLYING FACTORS AT TYPICAL VALUES OF V_{TUN} AT:			
		< 12V	12 to 18V	18 to 24V	> 24V
0	0	1[1]	1[1]	1[1]	1[1]
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

NOTE:
1. Values after reset.

Table 5. Tuning Window Programming

TUW1	TUW0	|Δf| (kHz)	TUNING WINDOW (kHz)
0	0	0[1]	0[1]
0	1	50	100
1	0	150	300

NOTE:
1. Values after reset.

Table 6. AFC Hold Range Programming

AFCR1	AFCR0	|Δf| (kHz)	AFC HOLD RANGE (kHz)
0	0	0[1]	0[1]
0	1	350	700
1	0	750	1500

NOTE:
1. Values after reset.

Table 7. Transconductance Programming

AFCS1	AFCS0	TYP. TRANSCONDUCTANCE (μA/V)
0	0	0.25[1]
0	1	25
1	0	50
1	1	100

NOTE:
1. Values after reset.

Tuning Sensitivity
To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50kHz; TUHN0 and TUHN1 = logic 1.

Correction-In-Band
This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

The transconductance multiplying factor of the AFC amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning Window
Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation |Δf| between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If |Δf| is up to 50kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

AFC
When AFCT is set to logic 1 it will not be cleared and the AFC will remain on as long as |Δf| is less than the value programmed for the AFC hold range AFCR (see Table 6). It is possible for the AFC to remain on for values of up to 50kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Transconductance
The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bits AFCS as shown in Table 7.

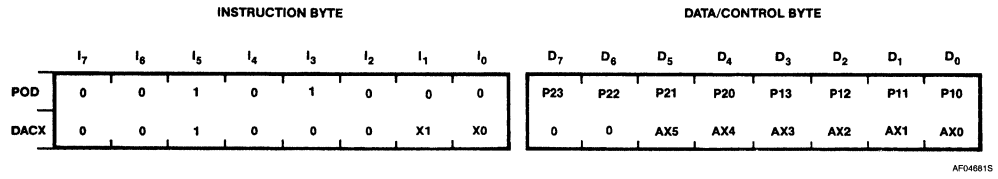


Figure 3. Control Programming

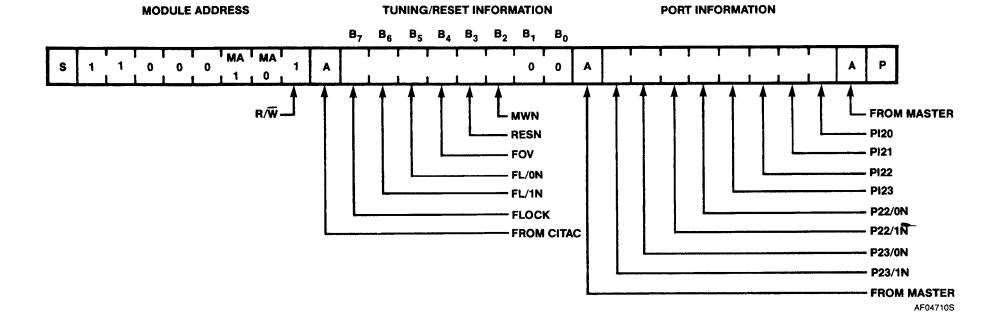


Figure 4. Information Byte Format

AFC Polarity
If a positive differential input voltage is applied to the (switched-on) AFC amplifier, the tuning voltage V_{TUN} falls when the AFC polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum Tuning Voltage
Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in the DC Electrical Characteristics table.

Frequency Measuring Window
The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Tuning Direction
Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analog converter control) are shown in Figure 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes High. All outputs are Low after reset.

P23, P22, P21, P20 — Open-collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analog converters. The digital-to-analog converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

Table 8. Frequency Measuring Window Programming

FDIVM	PRESCALER DIVISION FACTOR	CYCLE PERIOD (ms)	MEASURING WINDOW (ms)
0	256	6.4[1]	5.12[1]
1	64	2.56	1.28

NOTE:
1. Values after reset.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master, the slave (CITAC) stops transmitting. The format of the information bytes is shown in Figure 4.

Tuning/Reset Information Bits

FLOCK — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.

FL/1N — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

FL/0N — As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.

FOV — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.

RESN — Set to logic 0 (Active-LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.

MWN — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured.

When slightly different frequencies are programmed repeatedly and AFC is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port Information Bits

P23/1N, P22/1N — Set to logic 0 (Active-LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22, respectively. Both are reset to logic 1 after the port information has been read.

P23/0N, P22/0N — As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.

PI23, PI22, PI21, PI20 — Indicate input voltage levels at P23, P22, P21 and P20, respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Figure 5. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

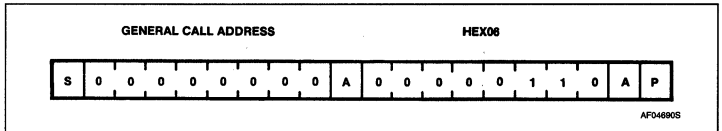


Figure 5. Reset Programming

I^2C BUS TIMING (Figure 6)

I^2C bus load conditions are as follows:

4kΩ pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			μs
t_{SU}, t_{STA}	Start condition setup time	4			μs
t_{HD}, t_{STA}	Start condition hold time	4			μs
t_{LOW}	SCL, SDA LOW period	4			μs
t_{HIGH}	SCL HIGH period	4			μs
t_R	SCL, SDA rise time			1	μs
t_F	SCL, SDA fall time			0.3	μs
t_{SU}, t_{DAT}	Data setup time (write)	1			μs
t_{HD}, t_{DAT}	Data hold time (write)	1			μs
t_{SU}, t_{CAC}	Acknowledge (from CITAC) setup time			2	μs
t_{HD}, t_{CAC}	Acknowledge (from CITAC) hold time	0			μs
t_{SU}, t_{STO}	Stop condition setup time	4			μs
t_{SU}, t_{RDA}	Data setup time (read)			2	μs
t_{HD}, t_{RDA}	Data hold time (read)	0			μs
t_{SU}, t_{MAC}	Acknowledge (from master) setup time	1			μs
t_{HD}, t_{MAC}	Acknowledge (from master) hold time	2			μs

NOTE:

1. Timings t_{SU}, t_{DAT} and t_{HD}, t_{DAT} deviate from the I^2C bus specification. After reset has been activated, transmission may only be started after a 50μs delay.

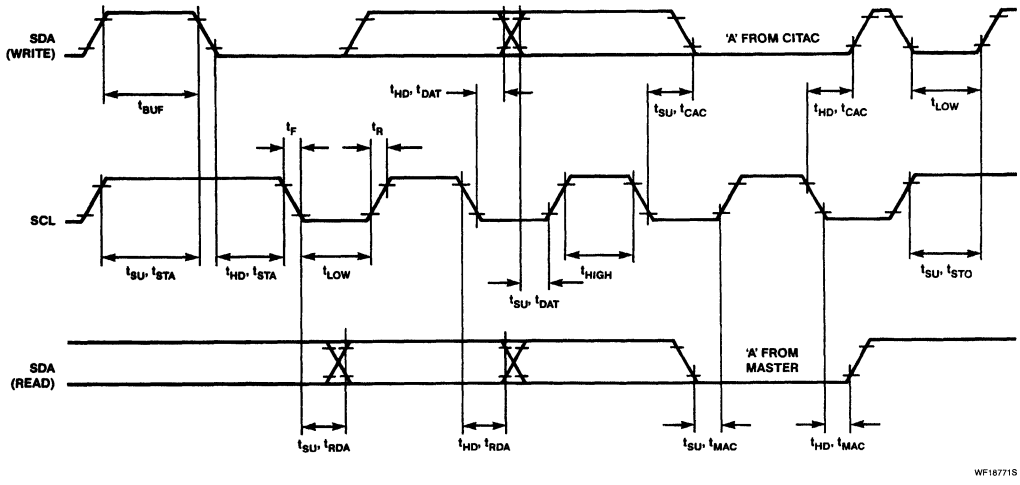


Figure 6. I²C Bus Timing SAB3037

Signetics

Linear Products

TDA8400

FLL Tuning Circuit With Prescaler

Product Specification

DESCRIPTION

The TDA8400 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It comprises a 1.1GHz prescaler, with the divide-by-64 ratio, which drives a tuning interface providing a tuning voltage of 33V (maximum) via an external output transistor. The TDA8400 can also drive external PNP transistors to provide 4 high-current outputs for tuner band selection.

The IC can be used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I^2C bus.

FEATURES

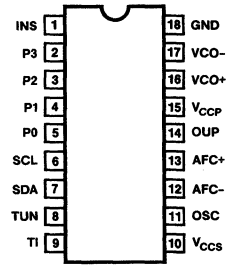
- **Combined analog and digital circuitry minimizes the number of additional interfacing components required**
- **Frequency measurement with resolution of 50kHz**
- **On-chip prescaler**
- **Tuning voltage amplifier**
- **4 high-current outputs for direct band selection**
- **Tuning with control of speed**
- **Tuning with or without AFC**
- **Single-pin, 4MHz, on-chip oscillator**
- **I^2C bus slave transceiver**

APPLICATIONS

- **TV receivers**
- **Satellite receivers**
- **CATV converters**

PIN CONFIGURATION

N Package



TOP VIEW

CD11980S

PIN NO.	SYMBOL	DESCRIPTION
1	INS	Input synthesizer (test)[1]
2	P3	High-current band-selection output ports
3	P2	
4	P1	
5	P0	
6	SCL	Serial clock line (I^2C bus)
7	SDA	Serial data line (I^2C bus)
8	TUN	Tuning voltage amplifier output
9	TI	Tuning voltage amplifier inverting input
10	V_{CCS}	+5V supply voltage (synthesizer)
11	OSC	Crystal oscillator input
12	AFC–	AFC amplifier inputs
13	AFC+	
14	OUP	Output from prescaler (test)
15	V_{CCP}	+5V supply voltage (prescaler)[2]
16	VCO+	Inputs to prescaler
17	VCO–	
18	GND	Ground

NOTES:
1. Connected to ground for application.
2. Left open-circuit for application.

ORDERING INFORMATION

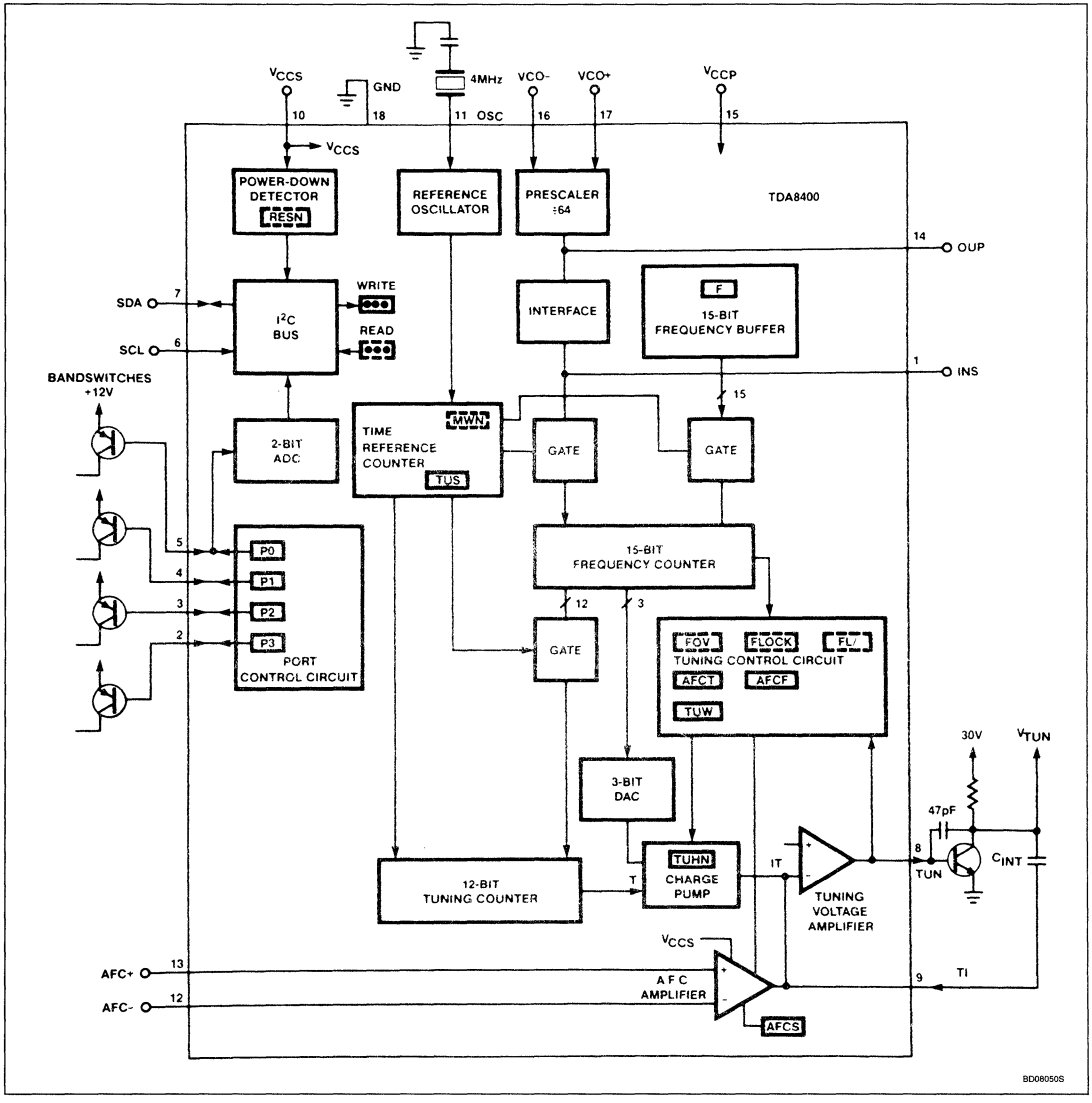
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin DIP (SOT – 102 HE, KE)	0 to 70°C	TDA8400N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage:		
V_{CCS}	(Pin 10)	6	V
V_{CCP}	(Pin 15)	6	V
V_N	Input/output voltage (each pin)	6	V
P_{TOT}	Total power dissipation	350	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−10 to +80	°C

4

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; V_{CCS}, V_{CCP} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Supply voltage				
V_{CCS}	Synthesizer (Pin 10)	4.5	5	5.5	V
V_{CCP}	Prescaler (Pin 15)	4.5	5	5.5	V
	Supply current				
I_{CCS}	Synthesizer (Pin 10)		12		mA
I_{CCP}	Prescaler (Pin 15)		43		mA
P_{TOT}	Total power dissipation		275		mW
T_A	Operating ambient temperature range	0		+70	°C
T_{STG}	Operating storage temperature range	−10		+85	°C
I^2C bus inputs/outputs Inputs: SDA (Pin 7); SCL (Pin 6)					
V_{IH}	Input voltage HIGH	3.1		5.5	V
V_{IL}	Input voltage LOW	−0.3		1.6	V
I_{IH}	Input current HIGH			10	μA
I_{IL}	Input current LOW			10	μA
	SDA output (Pin 7, open-collector)				
V_{OL}	Output voltage LOW at I_{OL} = 3mA			0.4	V
I_{OL}	Output sink current			5	mA
Tuning voltage amplifier Input TI, output TUN (Pins 9, 8)					
I_{TI}	Input bias current	−5		+5	nA
$-I_{TUNL}$	Output current LOW at V_{TUN} = 0.4V	20			μA
	Minimum charge IT to tuning amplifier				
CH_0	TUHN = 0		5		μA•μs
CH_1	TUHN = 1		125		μA•μs
	Maximum current I into tuning amplifier				
I_{T0}	TUHN = 0		18		μA
I_{T1}	TUHN = 1		440		μA
AFC amplifier (Inputs AFC+, AFC− Pins 13, 12)					
V_{DIF}	Differential input voltage			1	V
g_1	Transconductance at AFCS = 1	5	10	15	μA/V
g_0	Transconductance at AFCS = 0	30	50	70	μA/V
V_{CM}	Common mode input voltage	2.5		$V_{CC1} - 1$	V
CMRR	Common mode rejection ratio		50		dB
PSRR	Power supply (V_{CC1}) rejection ratio		50		dB
I_I	Input current			1	μA
Main band-selection output ports P0, P1, P2, P3 (Pins 5 to 2, open-collector)					
	Output sink current				
I_{BSL1}	LOW impedance	0.8	1	1.2	mA
I_{BSH1}	HIGH impedance			10	μA

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CCS}, V_{CCP} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Prescaler inputs (VCO+ Pin 16; VCO– Pin 17)					
	Input differential voltage (RMS value)				
$V_{I(RMS)}$	at f = 70MHz	17.5		200	mV
$V_{I(RMS)}$	at f = 150MHz	10		200	mV
$V_{I(RMS)}$	at f = 300MHz	10		200	mV
$V_{I(RMS)}$	at f = 500MHz	10		200	mV
$V_{I(RMS)}$	at f = 900MHz	10		200	mV
$V_{I(RMS)}$	at f = 1.1GHz	25		200	mV
f_I	Input frequency	0.07		1.1	GHz
OSC input (Pin 11)					
R_{XTAL}	Crystal resistance at resonance (4MHz)			150	Ω
Power-down reset					
V_{PD}	Maximum supply voltage V_{CC1} at which power-down reset is active	3		4	V
Voltage level for valid module address					
	Voltage level P0 (Pin 5) for valid module address as a function of MA1, MA0				
	MA1 MA0				
	0 0	pin used as an output			
V_{VA01}	0 1	−0.3		0.8	V
V_{VA10}	1 0	2.4		$V_{CCS} - 1.6$	V
V_{VA11}	1 1	$V_{CCS} - 0.3$		V_{CCS}	V

FUNCTIONAL DESCRIPTION

Prescaler

The integrated prescaler has a divide-by-64 ratio with a maximum input frequency of 1.1GHz. It will oscillate in the absence of an input signal within the frequency range of 800MHz to 1.1GHz.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in the 15-bit frequency buffer. The actual tuner frequency (1.1GHz maximum) is applied to the circuit on the two complementary inputs VCO+ and VCO– which drive the integrated prescaler. The resulting frequency (FDIV) is measured over a period controlled by a time reference counter and fed via a gate to a 15-bit frequency counter where it is compared to the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 2.56ms, controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier (external capacitance $C_{INT} = 0.5\mu F$) is controlled by the tuning counter, 3-bit DAC, and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (control bit TUHN = logic 1; see Table 2) the minimum charge IT at Δf = 50kHz equals $125\mu A \cdot \mu s$ (typ.).

By programming the tuning sensitivity bits (TUS; see Table 3) the charge IT can be doubled up to 6 times. From this, the maximum charge IT at Δf = 50kHz equals $2^6 \times 125\mu A \cdot \mu s$ (typ.). The maximum tuning current I is 440μA, while T is limited to the duration of the tuning cycle (2.56ms).

In the tuning-hold mode (TUHN = logic 0) the tuning current I is reduced, and, as a consequence, the charge into the tuning amplifier is also reduced. An in-lock situation can be detected by reading FLOCK. The TDA8400 can be programmed to tune in the digital mode or the AFC mode by setting AFCF. In the digital mode (AFCF = logic 0), the tuning window is programmable through the TUW flag. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1.

In the AFC mode, FLOCK will remain at logic 1 provided the tuner frequency is within a ±800kHz hold range. Switching from digital mode to AFC mode is determined by the microcontroller (AFCF flag). Switching from AFC mode to digital mode can be determined by the microcontroller, but if the frequency of the tuning oscillator does not remain within the hold range, the system automatically reverts to digital tuning. Switching back to the AFC mode will then have to be effected externally again. The tuning mode can be checked by reading the AFCT flag.

The occurence of positive and negative transitions in the FLOCK signal can be read by FL/1N and FL/0N. The AFC amplifier has programmable transconductance to 2 predefined values.

Control

For tuner band selection there are four output ports, P0 to P3, which are capable of driving external PNP transistors (open collector) as current sources. Output port P0 can also be used as valid address input with an active level determined by module address bits MA0 and MA1.

Reset

The TDA8400 goes into the power-down reset mode when V_{CC1} is below 3V (typ.). In this mode all registers are set to a defined state.

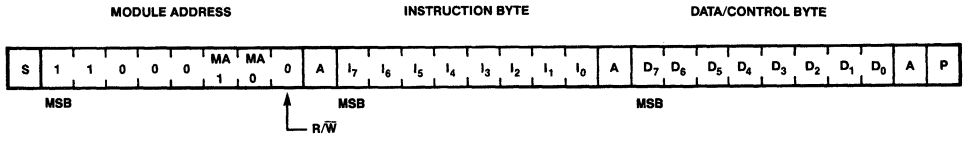


Figure 1. I²C Bus Write Format

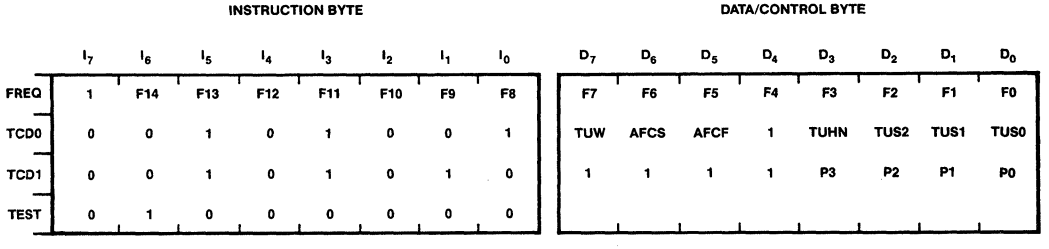


Figure 2. Tuning Control Format

OPERATION

Write

The TDA8400 is controlled via a bidirectional two-wire I²C bus; additional information on the I²C bus is available on request.

For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte, and a data/control byte are written into the device in the format shown in Figure 1.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port input P0 as shown in Table 1.

Table 1. Valid Module Addresses

P0	MA1	MA0
Don't care	0	0
GND	0	1
½ V_{CCS}	1	0
V_{CCS}	1	1

Acknowledge (A) is generated by the TDA8400 only when a valid address is received and the device is not in the power-down reset mode.

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

Frequency

Frequency is set when Bit I_7 of the instruction byte is set to logic 1; the remaining bits of this byte are processed as being data. Instruction bytes are fully decoded. All frequency bits are set to logic 1 and control bits to logic 0 at reset. The test instruction byte cannot be used for any other purpose.

Table 2. Tuning Current Control

TUHN	TYP. I_{MAX} (μA)	TYP. IT_{MIN} (μA/μs)
0	18[1]	5[1]
1	440	125

NOTE:
1. Values after reset.

Tuning Hold

The TUHN bit is used to decrease the maximum tuning current (I) and, as a consequence, the minimum charge IT (at Δf = 50kHz) into the tuning amplifier.

Tuning Sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50kHz; TUHN = logic 1.

Table 3. Minimum Charge IT as a Function of TUS

TUS2	TUS1	TUS0	TYP. IT_{MIN} (mA·μs)
0	0	0	0.125
0	0	1	0.25
0	1	0	0.5
0	1	1	1
1	0	0	2
1	0	1	4
1	1	0	8

NOTE:
The minimum tuning pulse is 2μs.

Tuning Mode

AFCF determines whether the TDA8400 has to tune in the digital mode or the AFC mode as shown in Table 4.

Table 4. Selection of Tuning Mode as a Function of AFCF

AFCF	TUNING MODE
0	Digital
1	AFC

If the tuner oscillator frequency comes out of the hold range when in the AFC mode, the device will automatically switch to digital tuning and AFCF is reset to logic 0.

Tuning Window

In the digital tuning mode TUW determines the tuning window (see Table 5) and the device is said to be in the "in-lock" situation.

Table 5. Tuning Window Programming

TUW	TUNING WINDOW (kHz)
0	0
1	±200

Transconductance

The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bit AFCS as shown in Table 6.

Table 6. Transconductance Programming

AFCS	TYP. TRANSCONDUCTANCE (μA/V)
1	10
0	50

Band Selection Control Ports (PX)

For band selection control, there are four output ports, P0 to P3, which are capable of driving external PNP transistors (open collector) as current sources. If a logic 1 is programmed on any of the PX bits P0 to P3, the PNP transistor will conduct and the relevant output goes LOW. All outputs are HIGH after reset.

Read

Information is read from the TDA8400 when the R/$\overline{W}$ bit is set to logic 1. Only one information byte is sent from the device. No acknowledge is required from the master after transmitting. The format of the information byte is shown in Figure 3.

Tuning/Reset Information Bits

FLOCK — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window (TUW) in the digital tuning mode, or within the ± 800kHz AFC hold range in the AFC mode.

FL/1N — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

FL/0N — Same as for FL/1N but it is set to logic 0 when FLOCK changes from 1 to 0.

FOV — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and, when too low, FOV is at logic 0.

RESN — Set to logic 0 (active Low) by a power-down reset. It is reset to logic 1 automatically after tuning/reset information has been read.

MWN — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. During the remaining time, MWN is at logic 0 and the received frequency is measured.

AFCT — AFCT (tuning mode flag) is set to logic 1 when the TDA8400 is in AFC mode and reset to logic 0 when in the digital mode.

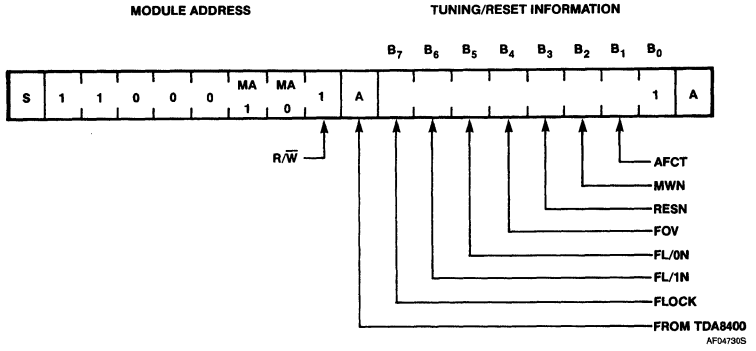


Figure 3. Information Byte Format

Signetics

SAB1164/65
1GHz Divide-by-64 Prescaler

Product Specification

Linear Products

DESCRIPTION

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V ±10% and an ambient temperature of 0 to 70°C. It features a high sensitivity and low harmonic contents of the output signal.

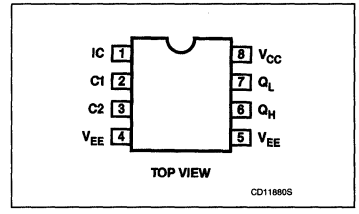
FEATURES

- **3mV (typ) sensitivity**
- **Differential inputs**
- **AC input coupling; internally based**
- **Outputs edge-controlled for low RFI**
- **Power consumption: 210mW (typ)**
- **Mini-DIP package**
- **Low output impedance (SAB1165)**

APPLICATIONS

- **PLL or FLL tuning systems, FM/communications/TV**
- **Frequency counters**

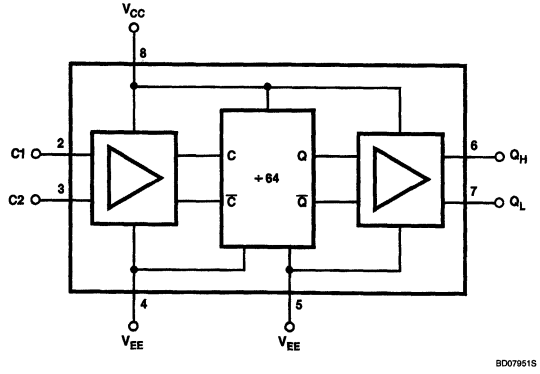
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	0 to +70°C	SAB1164N
8-Pin Plastic DIP (SOT-97A)	0 to +70°C	SAB1165N

BLOCK DIAGRAM



NOTE:
Divide-by-64 = 6 binary dividers

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (DC)	7	V
V_I	Input voltage	0 to V_{CC}	V
T_{STG}	Storage temperature range	−65 to +125	°C
T_J	Junction temperature	125	°C
θ_{CA}	Thermal resistance from crystal to ambient	120	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{EE} = 0V (ground); V_{CC} = 5V; T_A = 25°C, unless otherwise specified.

The circuit has been designed to meet the DC specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Output voltage				
V_{OH}	HIGH level			V_{CC}	V
V_{OL}	LOW level			V_{CC} − 0.8	V
I_{CC}	Supply current		42	50	mA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = 0V (ground); V_{CC} = 5V± 10%; T_A = 0 to +70°C

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_{I(RMS)}$	Input voltage RMS value (see Figure 2)				
	input frequency 70MHz		9	17.5	mV
	150MHz		4	10	mV
	300MHz		3	10	mV
	500MHz		3	10	mV
	900MHz		2	10	mV
	1GHz		3	17.5	mV
$V_{I(RMS)}$	Input overload voltage RMS value input frequency range 70MHz up to 1GHz			200	mV
$V_{O(P-P)}$	Output voltage swing	0.8	1		V
	Output resistance				
R_O	SAB1164		1		kΩ
R_O	SAB1165		0.5		kΩ
ΔV_O	Output unbalance			0.1	V
	Output rise time[1]				
t_{TLH}	f_I = 1GHz		25		ns
	Output fall time[1]				
t_{THL}	f_I = 1GHz		25		ns

NOTE:
1. Between 10% and 90% of observed waveform.

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V ± 10% and an ambient temperature of 0 to +70°C.

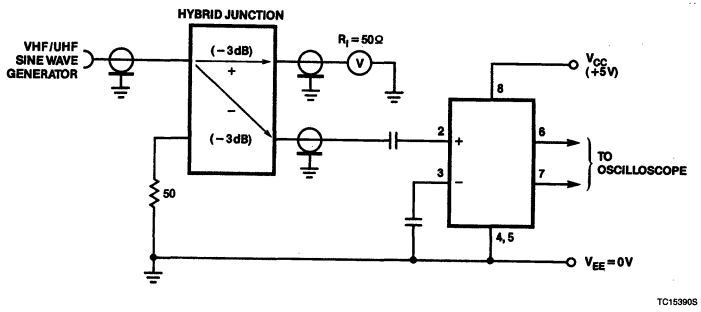
The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

1GHz Divide-by-64 Prescaler | SAB1164/65



NOTES:
Cables must be 50Ω coaxial.
The capacitors are leadless ceramic (multilayer capacitors) of 10nF.
All connections to the device and to the meter must be kept short and of approximately equal lengths.
Hybrid junction is ANZAC H-183-4 or similar.

Figure 1. Test Circuit for Defining Input Voltage

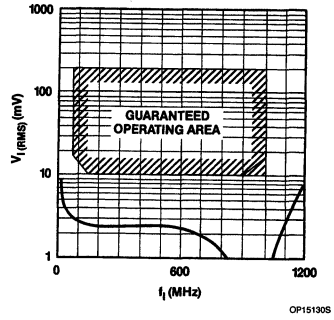
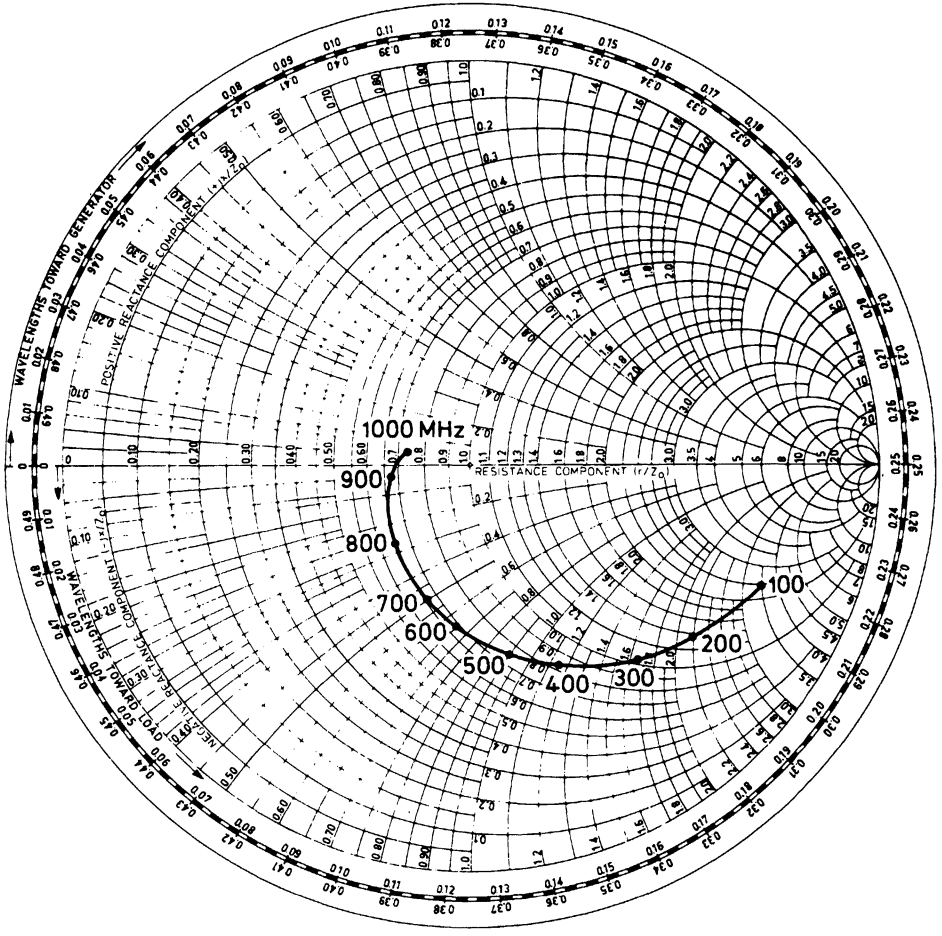


Figure 2. Typical Sensitivity Curve Under Nominal Conditions

4



NOTE:
$V_{I(RMS)}$ = 25mV; V_{CC} = 5V; reference value = 50Ω.

Figure 3. Smith Chart of Typical Input Impedance

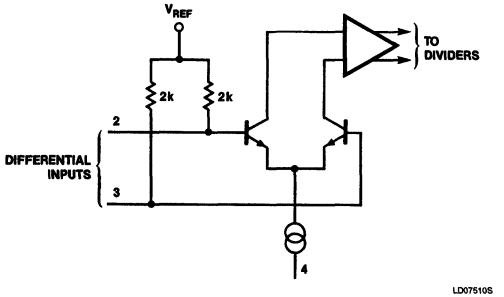
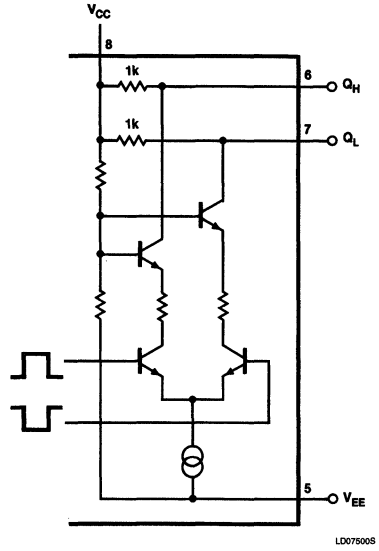
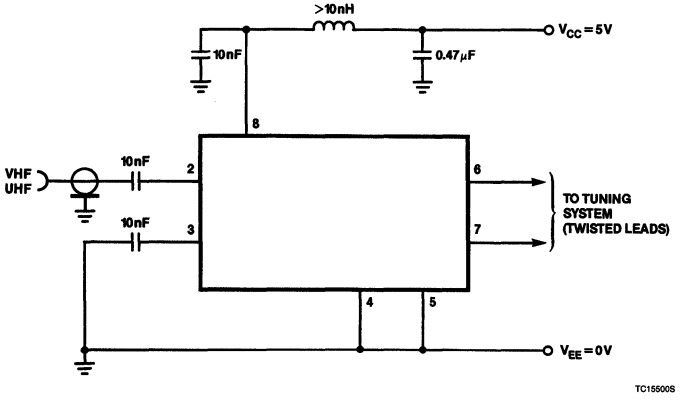


Figure 4. Input Stage



NOTES:
1. SAB1164: R1 = R2 = 1kΩ; I = 1mA
2. SAB1165: R1 = R2 = 0.5kΩ; I = 2mA
3. V_{CC} = 5V

Figure 5. Output Stage



NOTE:
TV tuning system. The output peak-to-peak voltage is about 1V.

Figure 6. Circuit Diagram

SAB1256
1GHz Divide-by-256 Prescaler

Product Specification

Linear Products

DESCRIPTION

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V± 10% and an ambient temperature of 0 to 70°C. It features a high sensitivity and low harmonic contents of the output signal.

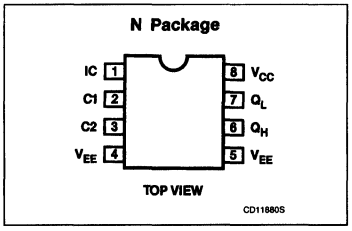
FEATURES

- **3mV (typ.) sensitivity**
- **AC input coupling, internally biased**
- **Outputs edge-controlled for low RFI**
- **235mV typical power dissipation**
- **Low output impedance ≈ 1kΩ**

APPLICATIONS

- **PLL or FLL tuning systems, FM/communications/TV**
- **Frequency counters**

PIN CONFIGURATION



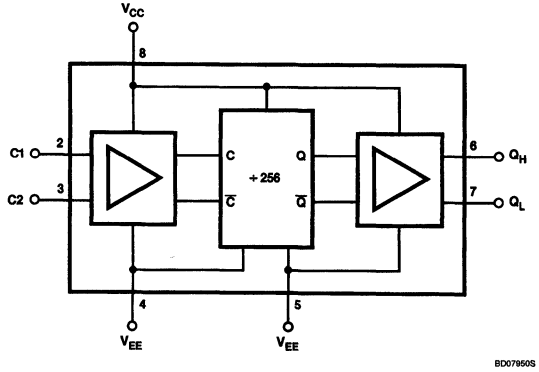
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97)	0 to 70°C	SAB1256N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (DC)	7	V
V_I	Input voltage	0 to V_{CC}	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	125	°C
θ_{CA}	Thermal resistance from crystal to ambient	120	°C/W

BLOCK DIAGRAM



NOTE:
Divide-by-256 = 8 binary dividers.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = 0V (ground); V_{CC} = 5V; T_A = 25°C, unless otherwise specified. The circuit has been designed to meet the DC specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{OH}	Output voltage HIGH level			V_{CC}	V
V_{OL}	LOW level			V_{CC} - 0.8	V
I_{CC}	Supply current		47	55	mA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = 0V (ground); V_{CC} = 5V ± 10%; T_A = 0°C to +70°C.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_{I(RMS)}$	Input voltage RMS value (see Figure 2)				
	Input frequency 70MHz		9	17.5	mV
	150MHz		4	10	mV
	300MHz		3	10	mV
	500MHz		3	10	mV
	900MHz		2	10	mV
	1GHz		3	17.5	mV
$V_{I(RMS)}$	Input overload voltage RMS value input frequency range 70MHz to 1GHz			200	mV
$V_{O(P-P)}$	Output voltage swing	0.8	1		V
R_O	Output resistance		1		kΩ
ΔV_O	Output unbalance			0.1	V
t_{TLH}	Output rise time[1] f_I = 1GHz		40		ns
t_{THL}	Output fall time f_I = 1GHz		40		ns

NOTE:
1. Between 10% and 90% of observed waveform.

FUNCTIONAL DESCRIPTION

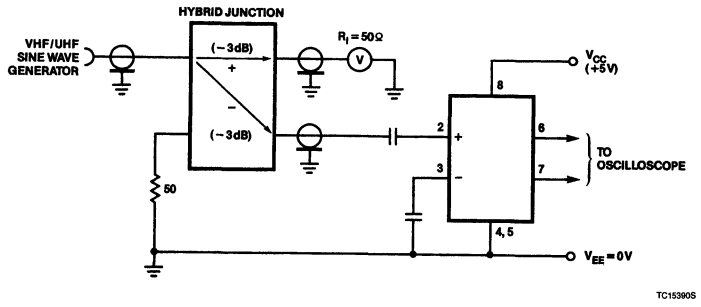
The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70MHz up to 1GHz, for a supply voltage of 5V ± 10% and an ambient temperature of 0 to 70°C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.



NOTES:
Cables must be 50Ω coaxial.
The capacitors are leadless ceramic (multi-layer capacitors) of 10nF.
All connections to the device and to the meter must be kept short and of approximately equal lengths.
Hybrid junction is ANZAC H-183-4 or similar.

Figure 1. Test Circuit for Defining Input Voltage

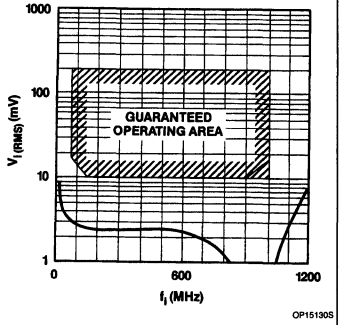
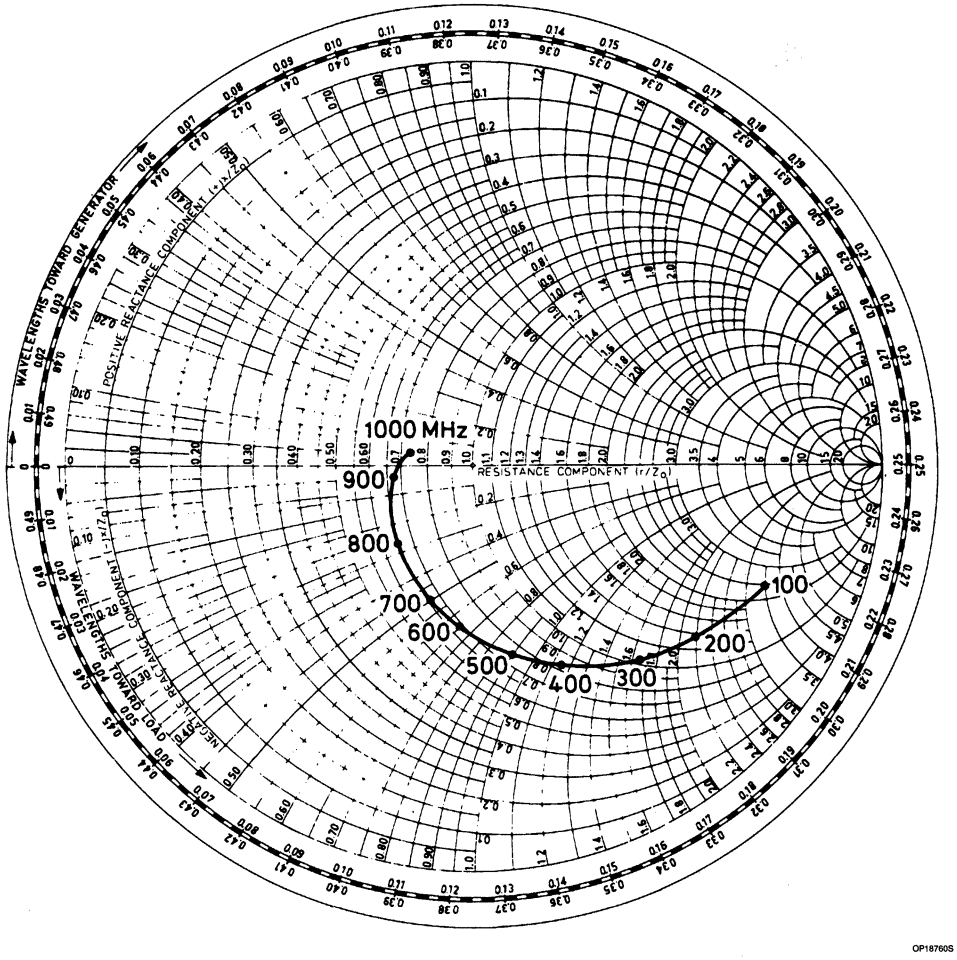


Figure 2. Typical Sensitivity Curve Under Nominal Conditions



NOTE:
$V_{I(RMS)}$ = 25mV; V_{CC} = 5V; reference value = 50Ω

Figure 3. Smith Chart of Typical Input Impedance

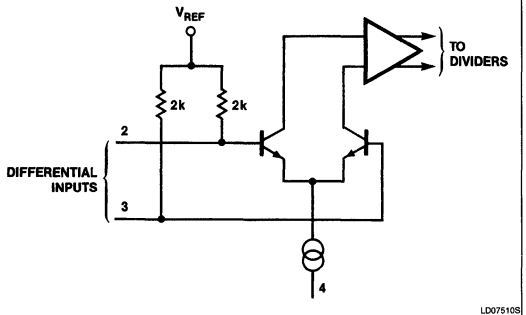
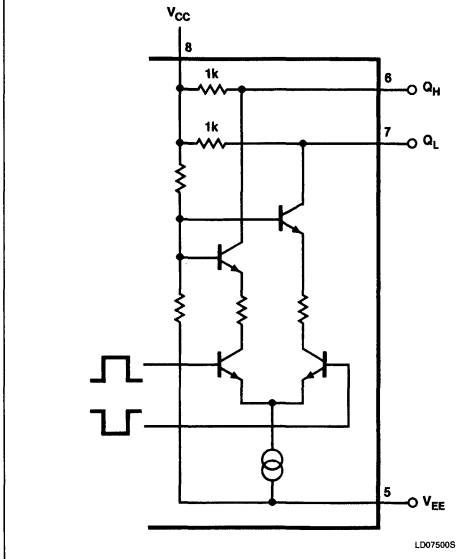
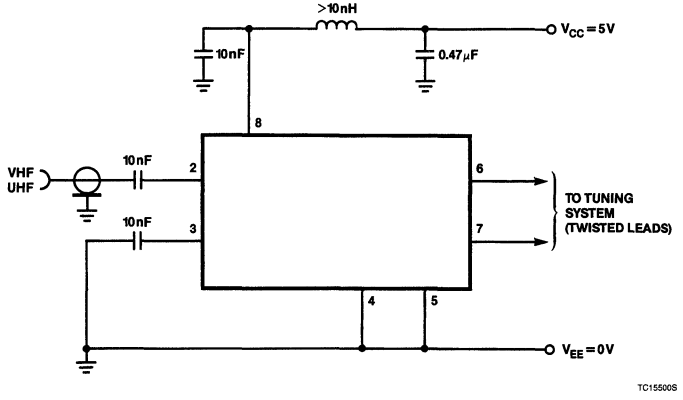


Figure 4. Input Stage



NOTE:
V_{CC} = 5V; I = 1mA.

Figure 5. Output Stage



NOTE:
Application in a television tuning system. The output peak-to-peak voltage is about 1V.

Figure 6. Circuit Diagram

Signetics

TDA5030A
VHF Mixer/Oscillator Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA5030A performs the VHF mixer, VHF oscillator, SAW filter IF amplifier, and UHF IF amplifier functions in television tuners.

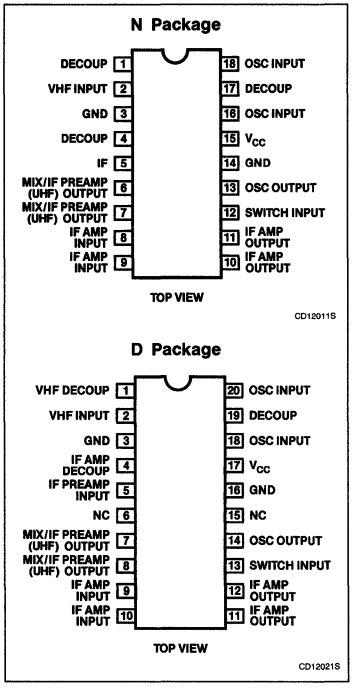
FEATURES

- **A balanced VHF mixer**
- **An amplitude-controlled VHF local oscillator**
- **A surface acoustic wave filter IF amplifier**
- **A UHF IF preamplifier**
- **A buffer stage for driving an external prescaler with the local oscillator signal**
- **A voltage stabilizer**
- **A UHF/VHF switching circuit**

APPLICATIONS

- **Mixer/oscillator**
- **TV tuners**
- **CATV**
- **LAN**
- **Demodulator**

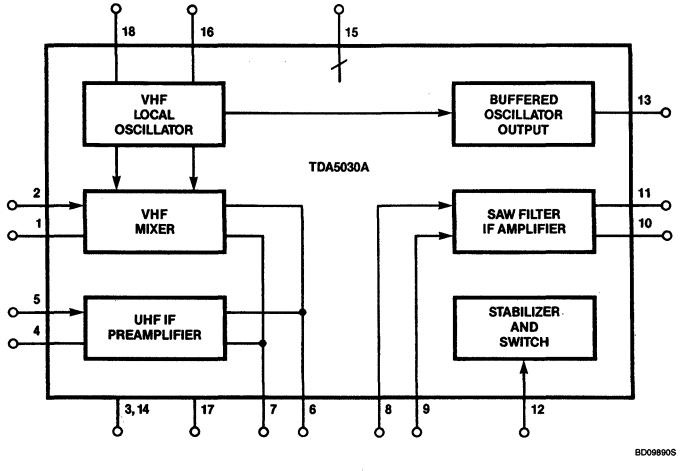
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102A)	−25°C to +85°C	TDA5030AN
20-Pin Plastic SO DIP (SOT-163A)	−25°C to +85°C	TDA5030ATD

BLOCK DIAGRAM



NOTE:
Pinout is for 18-pin N package.

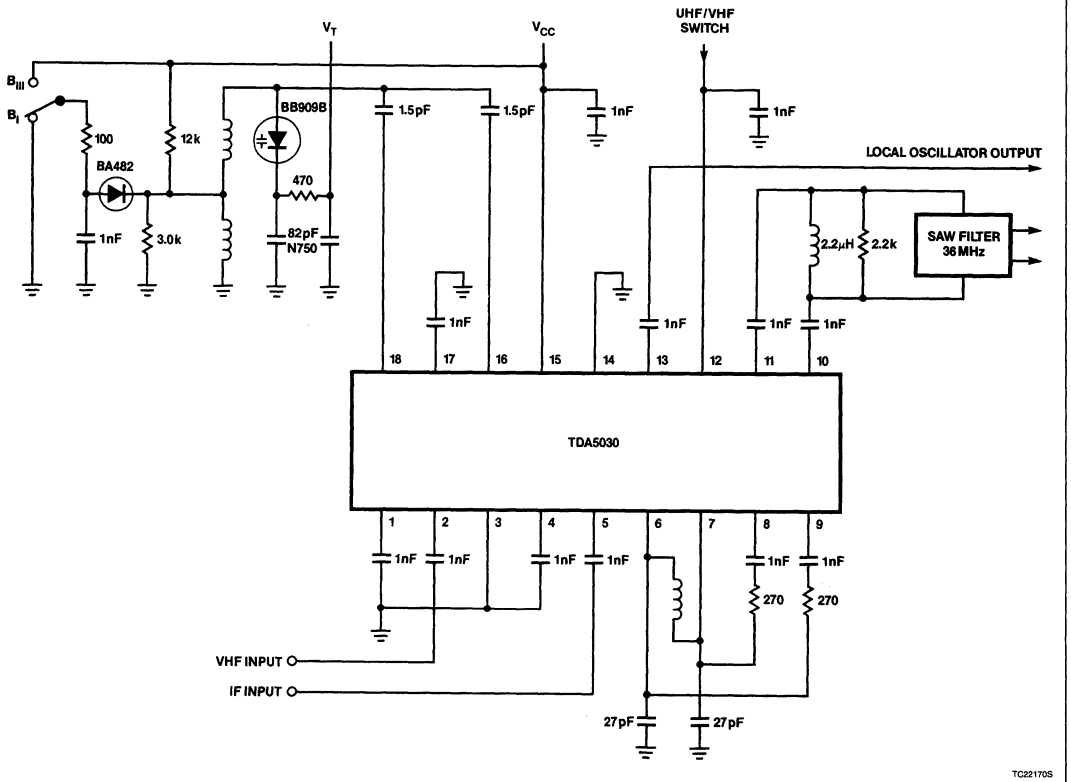


Figure 1. Test Circuit

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 15)	14	V
V_I	Input voltage (Pin 1, 2, 4, and 5)	0 to 5	V
V_{12}	Switching voltage (Pin 12)	0 to V_{CC}+0.3	V
$-I_{10, 11, 13}$	Output currents	10	mA
t_{SS}	Storage-circuit time on outputs (Pin 10 and 11)	10	s
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +85	°C
T_J	Junction temperature	+125	°C
θ_{JA}	Thermal resistance from junction to ambient	+55	°C/W

DC AND AC ELECTRICAL CHARACTERISTICS Measured in circuit of Figure 1; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{CC}	Supply voltage	10		13.2	V
I_{CC}	Supply current		42	55	mA
V_{12}	Switching voltage VHF	0		2.5	V
V_{12}	Switching voltage UHF	9.5		V_{CC}+0.3	V
I_{12}	Switching current UHF			0.7	mA
VHF mixer (including IF amplifier)					
f_R	Frequency range	50		470	MHz
NF	Noise figure (Pin 2) 50MHz 225MHz 300MHz		 7.5 9 10	 9 10 12	 dB dB dB
G	Optimum source admittance (Pin 2) 50MHz 225MHz 300MHz		 0.5 1.1 1.2		 ms ms ms
G_I	Input conductance (Pin 2) 50MHz 225MHz 300MHz		 0.23 0.5 0.67		 ms ms ms
C_I	Input capacitance (Pin 2) 50MHz		 2.5		 pF
$V_{2\text{-}3}$	Input voltage for 1% cross-modulation (in channel); R_P > 1kΩ; tuned circuit with C_P = 22pF; f_{RES} = 36MHz	97	99		dBμV
$V_{2\text{-}14}$	Input voltage for 10kHz pulling (in channel) at < 300MHz	100			dBμV
A_V	Voltage gain	22.5	24.5	26.5	dB
UHF preamplifier (including IF amplifier)					
G_I	Input conductance (Pin 5)		0.3		ms
C_I	Input capacitance (Pin 5)		3.0		pF
NF	Noise figure		5	6	dB
$V_{5\text{-}14}$	Input voltage for 1% cross-modulation (in channel)	88	90		dBμV
A_V	Voltage gain	31.5	33.5	35.5	dB
G_5	Optimum source admittance		3.3		ms

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Measured in circuit of Figure 1; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
VHF mixer					
$Yc_{2-6,\ 7}$	Conversion transadmittance		5.7		ms
Z_O	Output impedance		1.6		kΩ
VHF oscillator					
f_R	Frequency range	70		520	MHz
Δf	Frequency shift ΔV_{CC} = 10%; 70 to 330MHz			200	kHz
Δf	Frequency drift ΔT = 15k; 70 to 330MHz			250	kHz
Δf	Frequency drift from 5sec to 15min after switching on			200	kHz
SAW filter IF amplifier					
$Z_{8,\ 9}$	Input impedance $Z_{10,\ 11}$ = 2kΩ, f = 36MHz		340+j100		Ω
$Z_{8,\ 9-10,\ 11}$	Transimpedance		2.2		kΩ
$Z_{10,\ 11}$	Output impedance $Z_{8,\ 9}$ = 1.6kΩ; f = 36MHz		50+j40		Ω
VHF local oscillator buffer stage					
V_{13} V_{13}	Output voltage R_L = 75Ω; f < 100MHz R_L = 75Ω; f > 100MHz	14 10	20 20		mV mV
Z_{13}	Output impedance f = 100MHz		90		Ω
$\frac{RF}{(RF+LO)}$	RF signal on LO output; R_L = 50Ω; V_I = 1V; f ≤ 225MHz			10	dB

Signetics

TDA5230

VHF, Hyperband, and UHF Mixer/Oscillator With IF Amp

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5230 consists of three (VHF, Hyperband, UHF) mixer/oscillators, and an IF Amplifier Circuit for TV tuner or communication front end designs. The integration of these functions within one IC facilitates the construction of a complex tuner design with higher performance and fewer components than circuitry using discrete transistors.

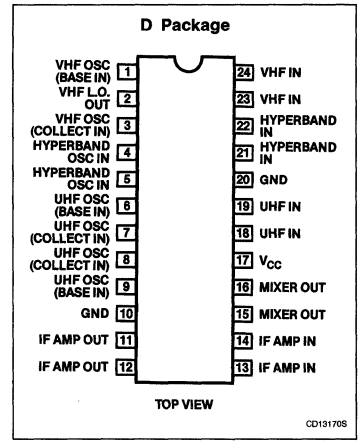
FEATURES

- **Balanced mixer for VHF having a common emitter input**
- **Amplitude-controlled oscillator for VHF**
- **Balanced mixer for hyperband & UHF with common base input**
- **Balanced hyperband & UHF oscillator**
- **Balanced mixer for UHF with common base input**
- **SAW filter preamplifier with a 75Ω output impedance**
- **Buffer stage for drive of a prescaler with the oscillator signal (VHF only)**
- **Voltage stabilizer for oscillator stability**
- **Band switch circuit**

APPLICATIONS

- **CATV**
- **Communication receiver**
- **TV tuners**
- **Data communication**

PIN CONFIGURATION

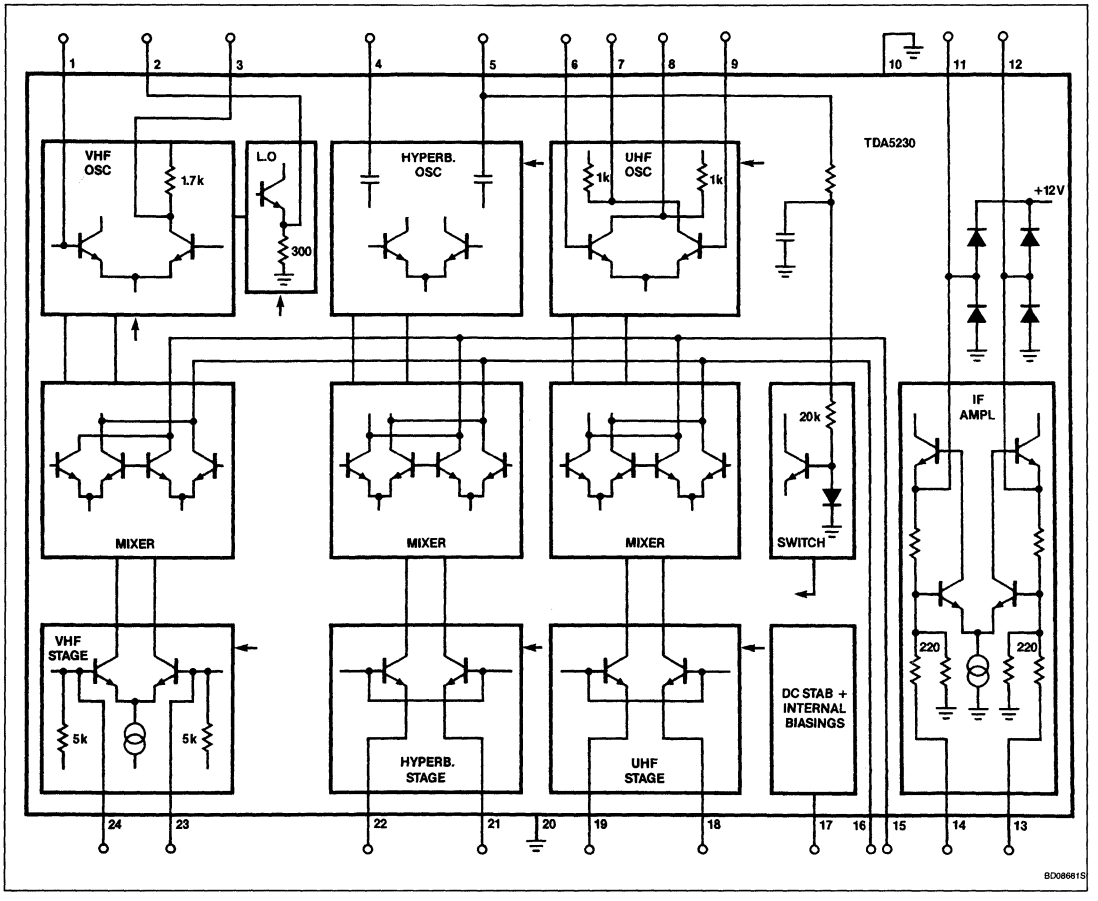


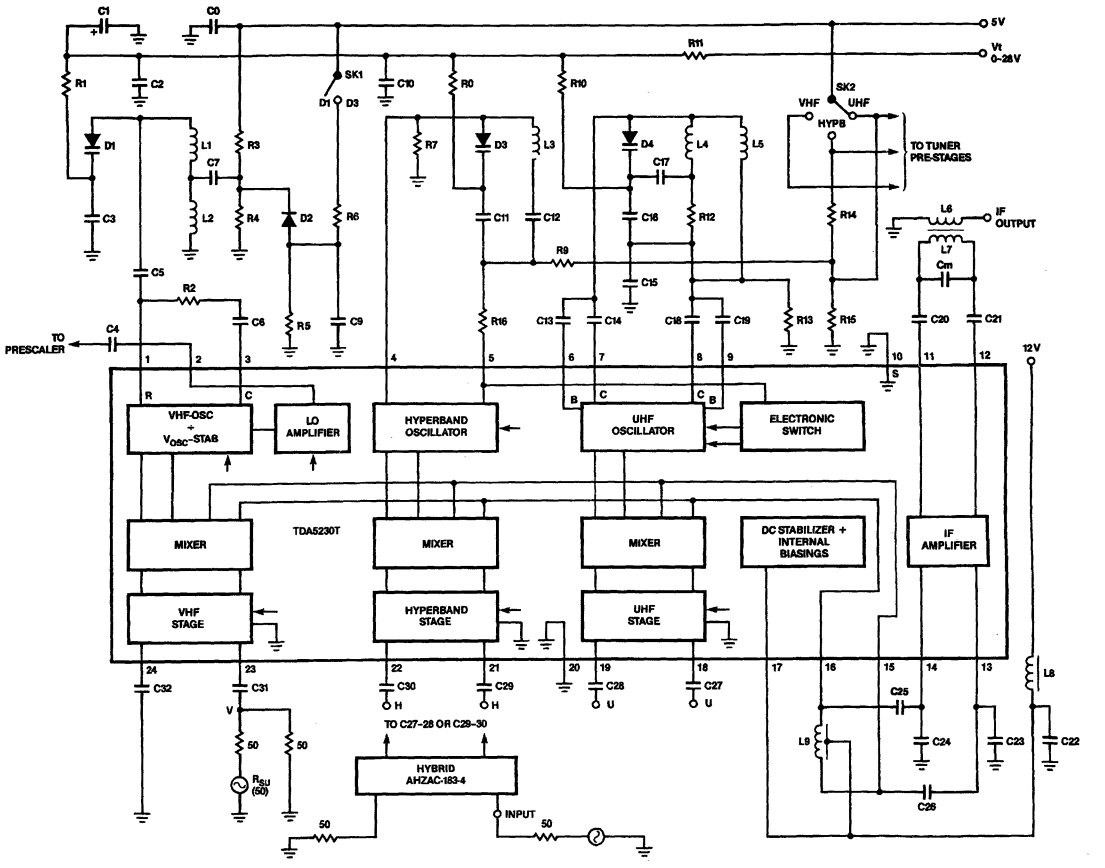
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-137)	−25°C to +80°C	TDA5230D

VHF, Hyperband, and UHF Mixer/Oscillator With IF Amp TDA5230

BLOCK DIAGRAM





BD08691S

NOTES:
1. L6 – L7 is a matching transformer (n = L7/L6 = 6). Terminated with 50Ω, it simulates the impedance of a saw-filter on Pins 11 – 12.
2. Cm is the simulated maximum allowable input capacitance of the saw-filter, which is 18pF if the capacitance between the leads to Pins 11 – 12 is < 4pF.
3. In the application Cm, L6 and L7 must be replaced by a saw-filter and an inductance across its input which tunes out the total capacitance between the pins if no IC has been connected.
4. This circuit is mounted on the V-H-U p.b.c. number: 3373.

Figure 1. Test Circuit for All Band VHF-UHF Mixer Oscillation IC TDA5230

Component Values of Circuit in Figure 1

Resistors

R1 = 47kΩ	R6 = 100Ω R11 = 1kΩ	
R2 = 18Ω	R7 = 22kΩ R12 = 2.2kΩ	
R3 = 4.7kΩ	R8 = 22kΩ R13 = 22kΩ	
R4 = 1.2kΩ	R9 = 2.2kΩR14 = 2.2kΩ	
R5 = 47kΩ	R10 = 22kΩR15 = 2.2kΩ	
		R16 = 10Ω (SMD)

Capacitors

C1 = 1μF – 40V	C11 = 12pF (N750)	C21 = 1nF	C31 = 1nF
C2 = 1nF	C12 = 1nF	C22 = 1nF	C32 = 1nF
C3 = 82pF (N750)	C13 = 1.5pF (SMD)	C23 = 15pF (N750)	C_M = 18pF (N750)
C4 = 1nF	C14 = 1.5pF (SMD)	C24 = 15pF (N750)	
C5 = 1.8pF (N750)	C15 = 1nF	C25 = 1nF	
C6 = 1.8pF (N750)	C16 = 5.6pF (SMD)	C26 = 1nF	
C7 = 1nF	C17 = 100pF (SMD)	C27 = 1nF	
C8 = 1nF	C18 = 1.5pF (SMD)	C28 = 1nF	
C9 = 1nF	C19 = 1.5pF (SMD)	C29 = 1nF	
C10 = 1nF	C20 = 1nF	C30 = 1nF	

Diodes and IC

D1 = BB909B D2 = BA482 D3 = BB909B D4 = BB405B IC = TDA5230

Coils

L1 = 2.5t ϕ3	L6 = 2t	T0K0 7kN
L2 = 6.5t ϕ4	L7 = 10t	Mat : 113kN
L3 = 2.5t ϕ2.5	L8 = 5μH	
L4 = 1.5t ϕ2.5	L9 = 2 × 6 t	T0K0 7kN
L5 = 1.5t ϕ3		Mat : 113kN

wire used: 0.4 for $L_1 - L_5$ and 0.1 for L_6, L_7, and L_9

Section 5
Remote Control Systems

INDEX

SAF1032P/1039P
R/C Receiver; R/C Transmitter

Product Specification

Linear Products

DESCRIPTION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (PCM: pulse code modulation) for infrared operation.

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

FEATURES

SAF1032P Receiver/Decoder:

- **16 program selection codes**
- **Automatic preset to standby at power 'ON', including automatic analog base settings to 50% and automatic preset of program selection '1' code**
- **3 analog function controls, each with 63 steps**
- **Single supply voltage**
- **Protection against corrupt codes**

SAF1039P Transmitter:

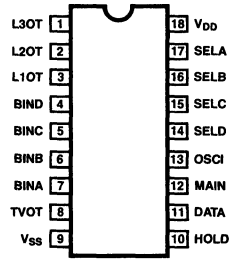
- **32 different control commands**
- **Static keyboard matrix**
- **Current drains from battery only during key closure time**
- **Two transmission modes selectable**

APPLICATIONS

- **TV**
- **Audio**
- **Industrial equipment**

PIN CONFIGURATIONS

SAF1032P N Package

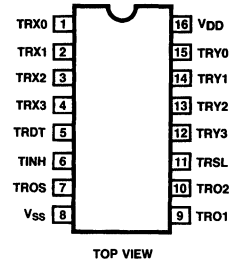


TOP VIEW

CD11270S

PIN NO.	SYMBOL	DESCRIPTION
1	L3OT	Linear ouput
2	L2OT	Linear output
3	L1OT	Linear output
4	BIND	Binary 8 output
5	BINC	Binary 4 output
6	BINB	Binary 2 output
7	BINA	Binary 1 output
8	TVOT	On/off input/output
9	V_{SS}	
10	HOLD	Control input
11	DATA	Data input
12	MAIN	Reset input
13	OSCI	Clock input
14	SELD	Binary 8 output
15	SELC	Binary 4 output
16	SELB	Binary 2 output
17	SELA	Binary 1 output
18	V_{DD}	

SAF1039P N Package



TOP VIEW

CD11260S

PIN NO.	SYMBOL	DESCRIPTION
1	TRX0	Keyboard input
2	TRX1	Keyboard input
3	TRX2	Keyboard input
4	TRX3	Keyboard input
5	TRDT	Data input
6	TINH	Inhibit output/mode select input
7	TROS	Oscillator output
8	V_{SS}	
9	TRO1	Oscillator control input
10	TRO2	Oscillator control input
11	TRSL	Keyboard select line
12	TRY3	Keyboard input
13	TRY2	Keyboard input
14	TRY1	Keyboard input
15	TRY0	Keyboard input
16	V_{DD}	

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102A)	−40°C to +85°C	SAF1032PN
16-Pin Plastic DIP (SOT-38Z)	−40°C to +85°C	SAF1039PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{DD} - V_{SS}$	Supply voltage range	−0.5 to 11	V
V_I	Input voltage	11	V
$\pm I_I$	Current into any terminal	10	mA
P_O	Power dissipation (per output)	50	mW
P_{TOT}	Power dissipation (per package)	200	mW
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 0$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	T_A (°C)	SAF1039			UNIT
				Min	Typ	Max	
V_{DD}	Recommended supply voltage			7		10	V
Supply current							
I_{DD}	Quiescent	10 7	25 65		1	10 50	μA μA
I_{DD}	Operating; TRO1 at V_{SS}: outputs unloaded; One keyboard switch closed	10 10	All 25		0.8	1.7	mA mA
Inputs[1]							
	TRO2; TINH[2]						
V_{IH}	Input voltage HIGH	7 to 10	All	$0.8V_{DD}$		V_{DD}	V
V_{IL}	Input voltage LOW	7 to 10	All	0		$0.2V_{DD}$	V
I_I	Input current	10	25		10^{-5}	1	μA
Outputs							
$-I_{OH}$	TRDT; TROS; TRO1 Output current HIGH at $V_{OH} = V_{DD} - 0.5V$	7	All	0.4			mA
I_{OL}	Output current LOW at $V_{OL} = 0.4V$	7	All	0.4			mA
I_{OL}	TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	10	25			1	μA
I_{OL}	TINH Output current LOW $V_{OL} = 0.4V$	7	All	0.4			mA
Oscillator							
f_{OSC}	Maximum oscillator frequency			120			kHz
Δf	Frequency variation with supply voltage, Temperature and spread of IC properties at $f_{NOM} = 36kHz$[3]	7 to 10	All			$0.15f_{NOM}$	kHz
I_{OSC}	Oscillator current drain at $f_{NOM} = 36kHz$	10	25		1.3	2.5	mA

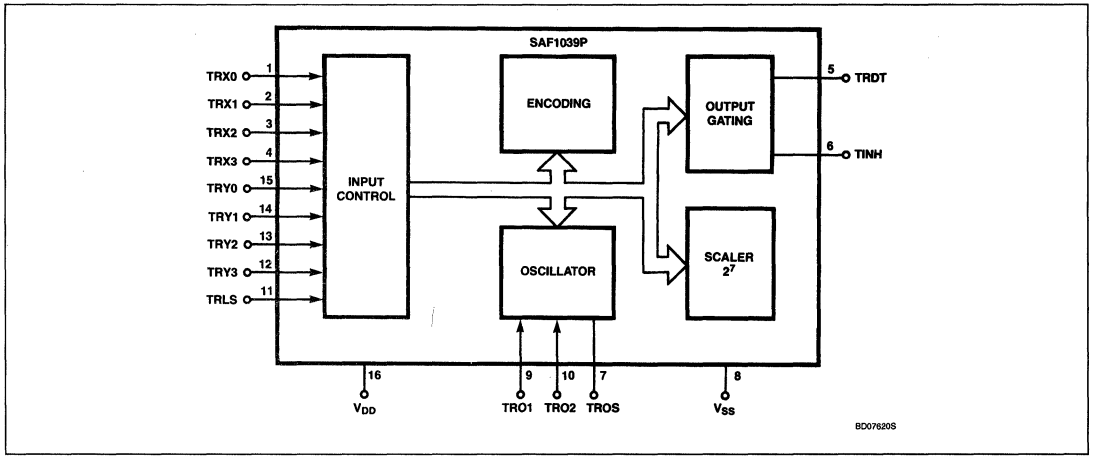
DC ELECTRICAL CHARACTERISTICS $T_A = 0$ to $+85°C$, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	T_A (°C)	SAF1032			UNIT
				Min	Typ	Max	
V_{DD}	Recommended supply voltage			8		10	V
Supply current							
I_{DD}	Quiescent	10 10	25 85		1	50 300	μA μA
I_{DD}	Operating; $I_O = 0$; at OSCI frequency of 100kHz	10	All			1	mA
Inputs							
	DATA; OSCI, HOLD; TVOT[4]						
V_{IH}	Input voltage HIGH	8 to 10	All	$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage LOW	8 to 10	All	0		$0.2V_{DD}$	V
	MAIN; tripping levels						
V_{TI}	Input voltage increasing	5 to 10	All	$0.4V_{DD}$		$0.9V_{DD}$	
V_{TD}	Input voltage decreasing	5 to 10	All	$0.1V_{DD}$		$0.6V_{DD}$	V
I_I	Input current; all inputs except TVOT	10	25		10^{-5}	1	μA
t_R, t_F	Input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	8 to 10	All			5	μs
Outputs							
	Program selection: BINA/B/C/D Auxiliary: SELA/B/C/D Analog: L3OT; L2OT; L1OT TVOT[4] All open-drain n-channel						
I_{OL}	output current LOW at $V_{OL} = 0.4V$	8	All	1.6			mA
I_{OL}	output leakage current at $V_O = V_{SS}$ to V_{DD}	10	All			10	μA

NOTES:

1. The keyboard inputs (TRX, TRY, TRSL) are not voltage driven (see Application Information Diagram, Figure 5).
   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage V_{DD} and the leakage current (between device and printed circuit board) externally applied to the keyboard inputs. If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7V$. At a leakage due to a 1MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} = 7V$. The highest permissible values of the contact series resistance of the keyboard switches is 500Ω.
2. Inhibit output transistor disabled.
3. Δf is the width of the distribution curve at 2σ points (σ = standard deviation).
4. Terminal TVOT is input for manual ON. When applying a LOW level TVOT becomes an output carrying a LOW level.

BLOCK DIAGRAM OF SAF1039P TRANSMITTER

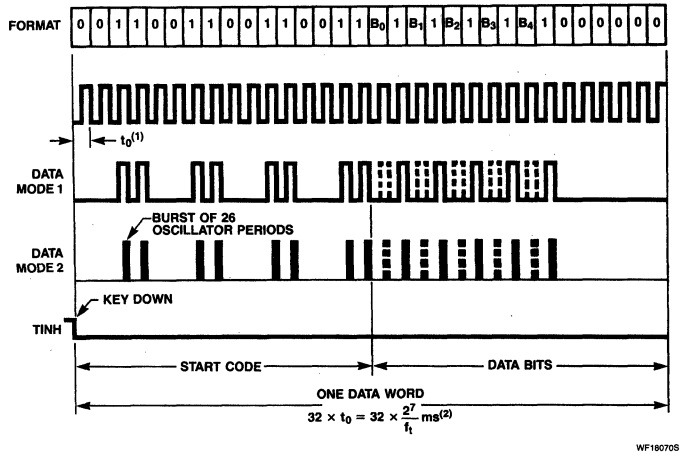


OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Figure 1), in which the data bit locations B_0 to B_4 represent the generated key command code. To cope with IR (infrared) interferences of other sources, a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place (See operating code table).

The contents of the 3 analog function registers are available on the three outputs in a pulse code versus time modulation format after D-to-A (digital-to-analog) conversion. The proper analog levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Figure 4).



NOTES:
1. T_O = 1 clock period = 128 oscillator periods.
2. f_T in kHz.

Figure 1. Pattern for Data to be Transmitted

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_T) of the transmitter, the receiver oscillator frequency ($f_R = 3 \times f_T$) must be kept constant with a tolerance of ±20%.

On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown above, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency-controlled with the external components R1 and C1 (see circuit Figure 3); the addition of resistor R2 means that the oscillator frequency is virtually independent of supply voltage variations. A complete data word is arranged as shown in Figure 1, and has a length of $32 \times T_0$ms, where $T_0 = 2^7/f_T$.

OPERATION MODE

MODE	DATA	FUNCTION OF TINH
1	Unmodulated: LOCAL operation	Output, external pull-up resistor to V_{DD}
2	Modulated: REMOTE control	Input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the Block Diagram.

Part I

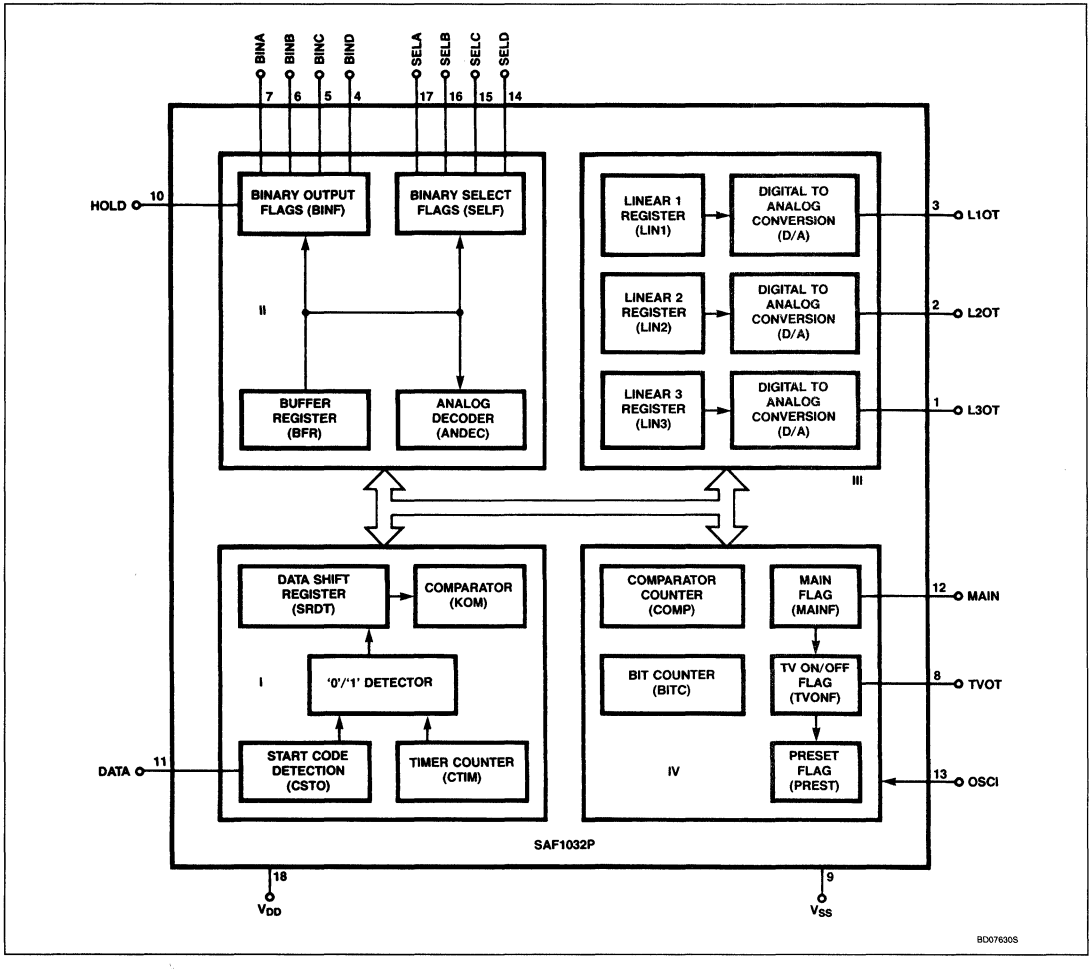
This part decodes the applied DATA information into logic '1' and '0'. It also recognizes the start code and compares the stored data bits with the new data bits accepted.

Part II

This part stores the program selection code in the output group (BINF) and memorizes it for condition HOLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally-used analog commands (ANDEC).

BLOCK DIAGRAM OF SAF1032P RECEIVER/DECODER



Part III

This part controls the analog function registers (each 6 bits long), and connects the contents of the three registers to the analog outputs by means of D/A conversion. During sound mute, output L1OT will be forced to HIGH level.

Part IV

This part keeps track of correct power 'ON' operation, and puts chip in 'standby' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (OSCI), while the required control timing signals are derived from the bit counter (BITC).

Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTO) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word, a comparison (KOM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (COMP).

As shown in the operating code table on the next page, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bits wide, will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analog function registers (each 6 bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Figure 2).

First power ON will always put the chip in the standby position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analog registers (analog base value). The program selection '1' code will also be prepared and all the outputs will be nonactive (see operating output code table).

From standby, the chip can be made operational via a program selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVOT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER-ON RESET, a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized and pulse width LOW $\geqslant 100\mu s$.

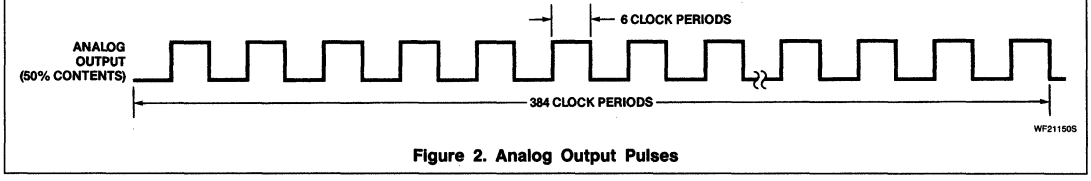


Figure 2. Analog Output Pulses

OPERATING CODE TABLE

KEY-MATRIX POSITION			BUFFER BFR					BINF (BIN.)				SELF (SEL.)				FUNCTION
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	Program
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	Select + ON
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	Program
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	Select + ON
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	Analog base
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	Reg. (LIN3) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	Reg. (LIN2) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	Reg. (LIN1) + 1
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	OFF
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	Reg. (LIN3) – 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	Reg. (LIN2) – 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	Reg. (LIN1) – 1
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	Mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	Spare functions
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

NOTE:
Reset mute also on program select codes, (LIN1) ±1, and analog base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(L.OT)			TVOT
	A	B	C	D	A	B	C	D	1	2	3	
Standby OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON — 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON — 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

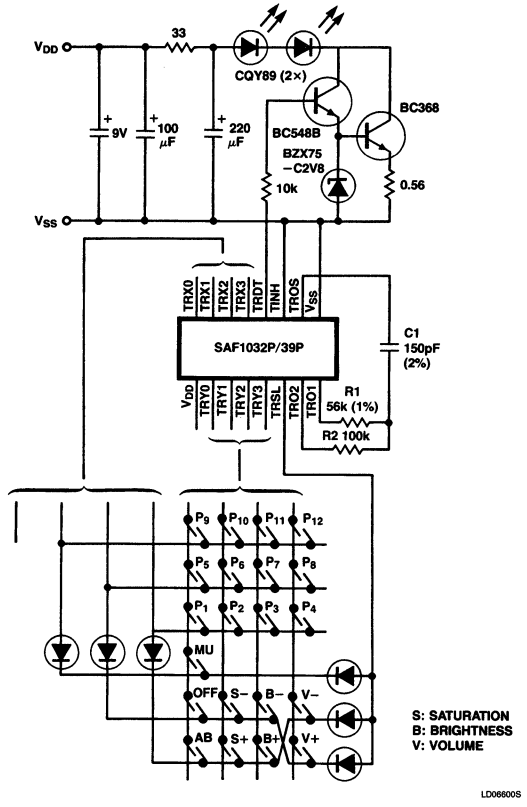


Figure 3. Interconnection Diagram of Transmitter Circuit SAF1039P in a Remote Control System for a Television Receiver With 12 Programs

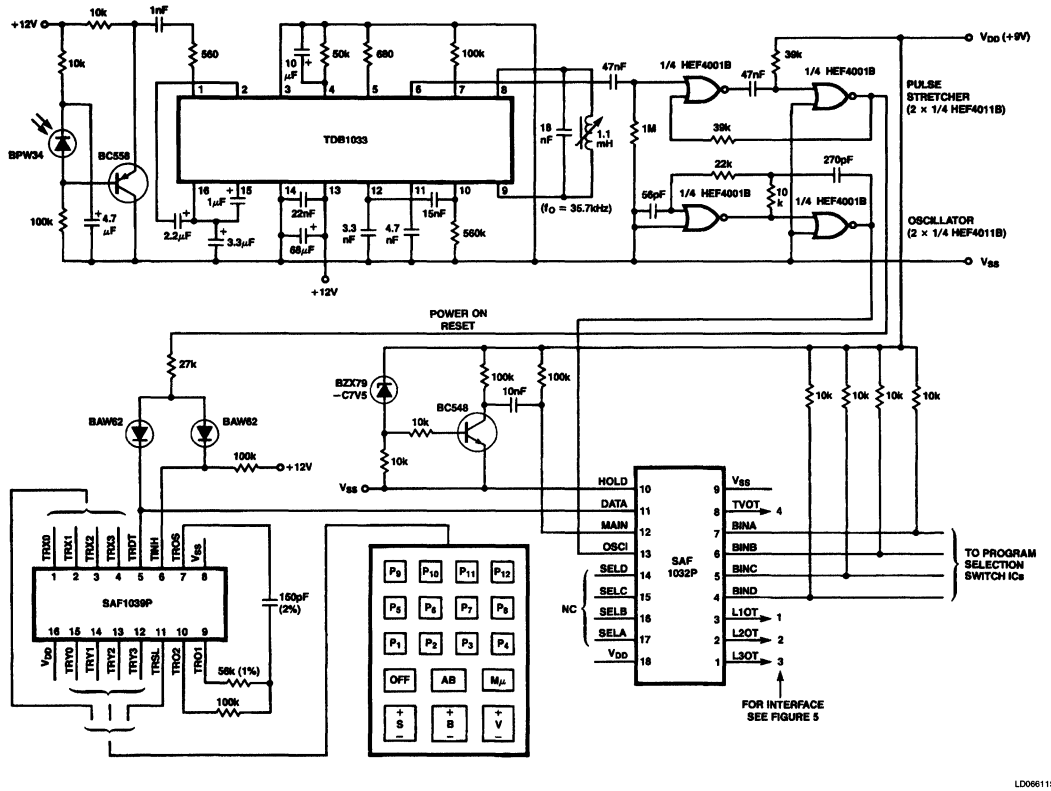


Figure 4. Interconnection Diagram Showing the SAF1032P and SAF1039P Used in a TV Control System

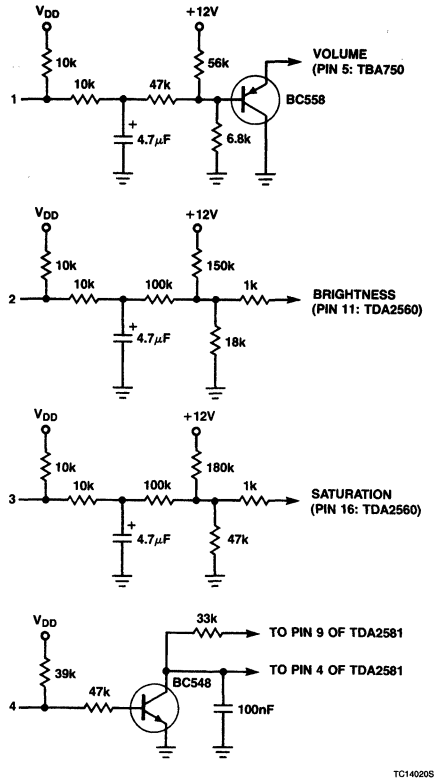


Figure 5. Additional Circuits from Outputs L1OT(1), L2OT(2), L3OT(3) and TVOT(4) of the SAF1032P in Circuit of Figure 4

SAA3004
Infrared Transmitter

Product Specification

Linear Products

DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 subsystem groups with 64 commands each. The subsystem code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the subsystem address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

FEATURES

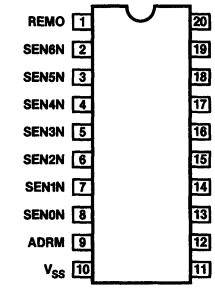
- **Flashed or modulated transmission**
- **7 subsystem addresses**
- **Up to 64 commands per subsystem address**
- **High-current remote output at V_{DD} = 6V ($-I_{OH}$ = 40mA)**
- **Low number of additional components**
- **Key release detection by toggle bits**
- **Very low standby current ($< 2\mu A$)**
- **Operational current < 2mA at 6V supply**
- **Wide supply voltage range (4 to 11V)**
- **Ceramic resonator controlled frequency (typ. 450kHz)**
- **Encapsulation: 20-lead plastic DIP or 20-lead plastic mini-pack (SO-20)**

APPLICATIONS

- **TV**
- **Audio**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD12000S

PIN NO.	SYMBOL	DESCRIPTION
1	REMO	Remote data output
2	SEN6N	Key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	Address mode control input
10	V_{SS}	Ground
11	OSCI	Oscillator input
12	OSCO	Oscillator output
13	DRV0N	Key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	Positive supply

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP (SOT-146C1)	−20°C to +70°C	SAA3004PN
20-Pin Plastic SOL (SOT-163AC3)	−20°C to +70°C	SAA3004TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +15	V
V_I	Input voltage range	−0.5 to V_{DD} + 0.5	V
V_O	Output voltage range	−0.5 to V_{DD} + 0.5	V
±I	DC current into any input or output	10	mA
$-I_{(REMO)M}$	Peak REMO output current during 10μs; duty factor = 1%	300	mA
P_{TOT}	Power dissipation per package for T_A = −20 to +70°C	200	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage T_A = 0 to +70°C		4		11	V
I_{DD} I_{DD}	Supply current; active f_{OSC} = 455kHz; REMO output unloaded	 6 9		 1 3		 mA mA
I_{DD} I_{DD}	Supply current; inactive (stand-by mode) T_A = 25°C	 6 9			 2 2	 µA µA
f_{OSC}	Oscillator frequency (ceramic resonator)	4 to 11	400		500	kHz
Keyboard matrix						
	Inputs SEN0N to SEN6N					
V_{IL}	Input voltage LOW	4 to 11			0.2 × V_{DD}	V
V_{IH}	Input voltage HIGH	4 to 11	0.8 × V_{DD}			V
$-I_I$ $-I_I$	Input current V_I = 0V	 4 11	 10 30		 100 300	 µA µA
I_I	Input leakage current V_I = V_{DD}	 11			 1	 µA
	Outputs DRV0N to DRV6N					
V_{OL} V_{OL}	Output voltage "ON" I_O = 0.1mA I_O = 1.0mA	 4 11			 0.3 0.5	 V V
I_O	Output current "OFF" V_O = 11V	 11			 10	 µA
Control input ADRM						
V_{IL}	Input voltage LOW				0.8 × V_{DD}	V
V_{IH}	Input voltage HIGH		0.2 × V_{DD}			V
	Input current (switched P-and N-channel pull-up/pull-down)					
I_{IL} I_{IL}	Pull-up active standby voltage: 0V	4 11	10 30		100 300	µA µA
I_{IH} I_{IH}	Pull-down active standby voltage: V_{DD}	4 11	10 30		100 300	µA µA
Data output REMO						
V_{OH} V_{OH}	Output voltage HIGH $-I_{OH}$ = 40mA	6 9	3 6		 	V V
V_{OL} V_{OL}	Output voltage LOW I_{OL} = 0.3mA	6 9			0.2 0.1	V V
Oscillator						
I_I	Input current OSCI at V_{DD}	6	0.8		2.7	µA
V_{OH}	Output voltage HIGH $-I_{OL}$ = 0.1mA	6			V_{DD} – 0.6	V
V_{OL}	Output voltage LOW I_{OH} = 0.1mA	6			0.6	V

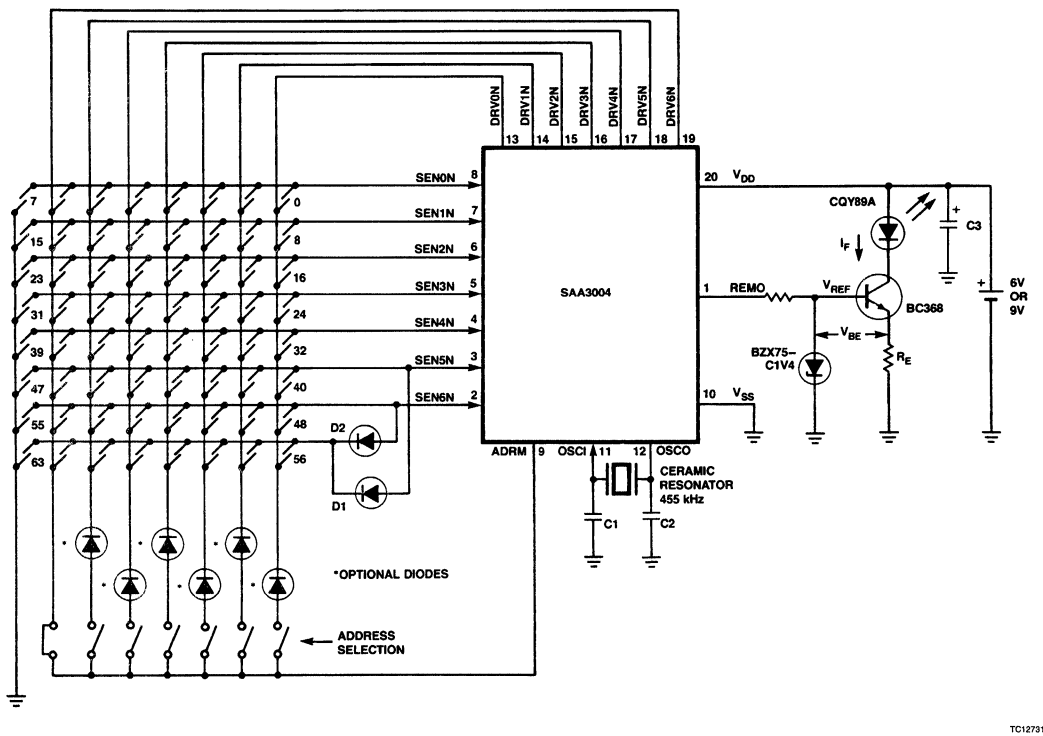


Figure 1. Transmitter With SAA3004

INPUTS AND OUTPUTS

Key Matrix Inputs and Outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Figure 1. The driver outputs DRV0N to DRV6N are open-drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address Mode Input (ADRM)

The subsystem address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven subsystem addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (subsystem address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the subsystem address and the mode of transmission.

The arrangement of the subsystem address coding is such that only the driver DRVnN with the highest number (n) defines the subsystem address, e.g., if driver DRV2N and DRV4N are connected to ADRM, only DRVN4N will define the subsystem address. This option can be used in transmitters for more than one subsystem address. The transmitter may be hard-wired for subsystem address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted subsystem address changes to 4.

A change of the subsystem address will not start a transmission.

Remote Control Signal Output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Figure 3).

The format of the output data is given in Figures 2 and 3. In the flashed transmission mode, the data word starts with two toggle bits, T1 and T0, followed by three bits for defining the subsystem address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit, T1, is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the subsystem address and the selected key are given in Tables 3 and 4.

Oscillator Input/Output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400kHz and 500kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard Operation

In the standby mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Figure 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied subsystem address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the subsystem address is sensed only within the first scan cycle. If the applied subsystem address is changed while the command key is pressed, the transmitted subsystem address is not altered.

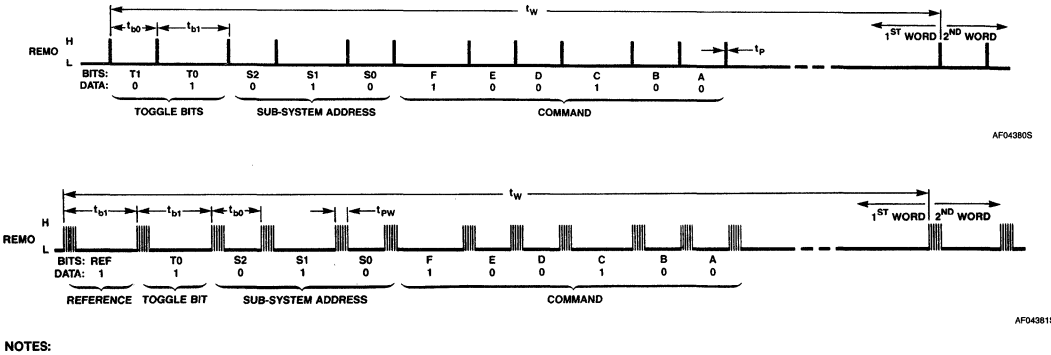
In a multiple keystroke sequence (see Figure 5), the command code is always altered in accordance with the sensed key.

Multiple Keystroke Protection

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Figure 5). In case of a multiple keystroke the scan repetition rate is increased to detect the release of a key as soon as possible.

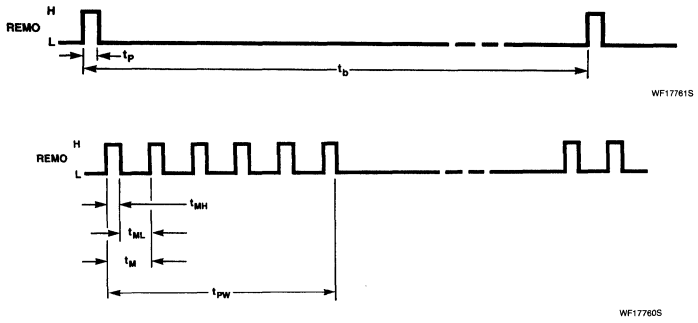
There are two restrictions caused by the special structure of the keyboard matrix:

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).



NOTES:
a. Flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
b. Modulated mode: transmission with reference time, toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

Figure 2. Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle Bits; S0, S1 and S2 = System Address; A, B, C, D, E, and F = Command Bits



NOTES:
1. Flashed pulse.
2. Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Figure 3. REMO Output Waveform

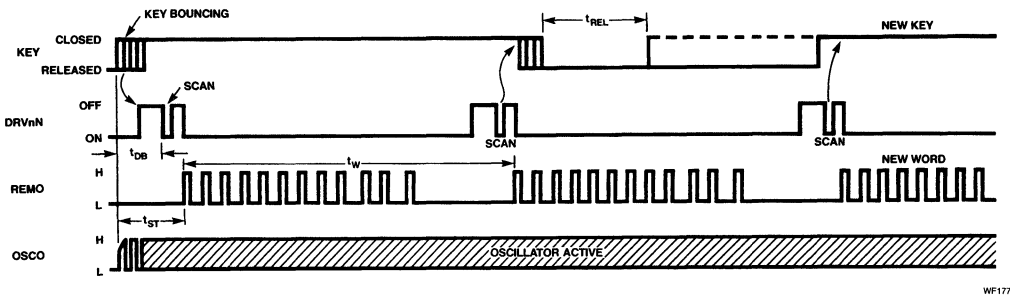
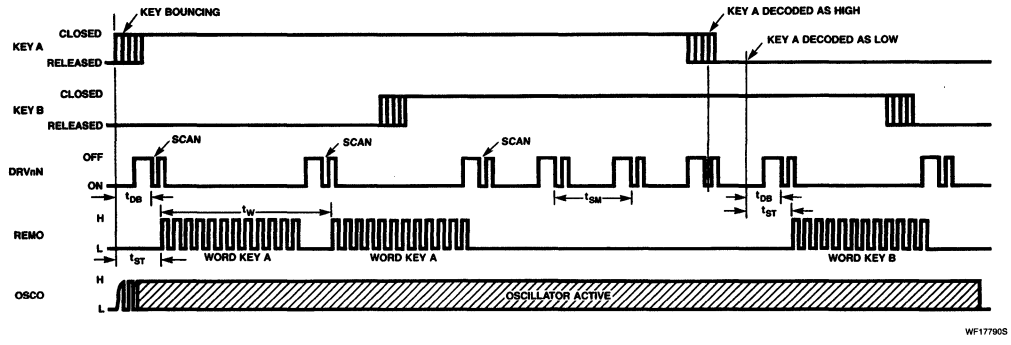


Figure 4. Single Key-Stroke Sequence

Output Sequence (Data Format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figures 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Figure 4). The toggle bits remain unchanged within a multiple keystroke sequence.



NOTES:
1. Scan rate multiple key-stroke: $t_{SM} = 6$ to $10 \times t_O$.
2. For t_{DB}, t_{ST} and t_W see Figure 4.

Figure 5. Multiple Key-Stroke Sequence

Table 1. Pulse Train Timing

MODE	t_O (ms)	t_P (μs)	t_M (μs)	t_{ML} (μs)	t_{MH} (μs)	t_W (ms)
Flashed	2.53	8.8				121
Modulated	2.53		26.4	17.6	8.8	121

NOTES:

f_{OSC}	455kHz	$t_{OSC} = 2.2\mu s$
t_P	$4 \times t_{OSC}$	Flashed pulse width
t_M	$12 \times t_{OSC}$	Modulation period
t_{ML}	$8 \times t_{OSC}$	Modulation period LOW
t_{MH}	$4 \times t_{OSC}$	Modulation period HIGH
t_O	$1152 \times t_{OSC}$	Basic unit of pulse distance
t_W	$55\ 296 \times t_{OSC}$	Word distance

Table 2. Pulse Train Separation (t_B)

CODE	t_B
Logic "0"	$2 \times t_O$
Logic "1"	$3 \times t_O$
Reference time	$3 \times t_O$
Toggle bit time	$2 \times t_O$ or $3 \times t_O$

Table 3. Transmission Mode and Subsystem Address Election

MODE	SUBSYSTEM ADDRESS				DRIVER DRVnN FOR n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

NOTES:

o	= Connected to ADRM
Blank	= Not connected to ADRM
X	= Don't care

Table 4. Key Codes

MATRIX DRIVE	MATRIX SENSE	CODE						MATRIX POSITION
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
1	SEN1N	0	0	1		2		8 to 15
1	SEN2N	0	1	0		2		16 to 23
1	SEN3N	0	1	1		2		24 to 31
1	SEN4N	1	0	0		2		32 to 39
1	SEN5N	1	0	1		2		40 to 47
1	SEN6N	1	1	0		2		48 to 55
1	SEN5N and SEN6N	1	1	1		2		56 to 63

NOTES:
1. The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.
2. The C, B and A codes are identical to SEN0N as given above.

The subsystem address and the transmission modes are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

5

AN1731
Low-Power Remote Control IR Transmitter and Receiver

Application Note

Linear Products

LOW-POWER IR TRANSMITTER SAA3004

The SAA3004 is a new MOS transmitter IC for infrared remote control systems in which the received commands are decoded by a microcomputer. It can transmit up to 448 commands, divided into 7 subsystem groups of 64 commands each and is therefore suitable for single or multi-system use. To allow remote control systems with a variety of ranges, noise immunities, and costs to be built, two operating modes are available: unmodulated (single pulse per bit) or modulated (burst of 6 pulses per bit). The subsystem address and mode of operation may be selected by keyboard contacts for multi-system use, or may be hard-wired for single system use. The output from the SAA3004 is Pulse Distance Modulated (PDM) for maximum power economy and the high level of output current available (40mA with a 6V supply) allows the IC to drive an IR LED via a very simple amplifier using a single external transistor.

Compared with earlier IR transmitter ICs, the SAA3004 operates over a much wider supply voltage range (4V to 11V), consumes less current during operation (1mA typical with a 6V supply), has a lower standby current ($< 2\mu A$), and requires a minimum number of external components. The low current consumption is largely due to the fairly low oscillator frequency (455kHz).

Transmission Formats

The formats of the two transmission modes are shown in Figure 1.

At least one complete 11-bit word is generated for each legal detected keystroke. The logic state of a bit is defined by the interval between consecutive output pulses or bursts, measured from leading edge to leading edge. The word is repeated as long as a key remains pressed. When a key is released, the transmission ceases as soon as the current word has been transmitted.

In the unmodulated mode, only one pulse per bit is generated and passed to output pin REMO. For this mode, the IR preamplifier in the receiver can be a broadband type and therefore inexpensive. However, the interference immunity and range of the remote control will not be as high as that for a transmitter in the modulated mode in conjunction with a narrow-band IR receiver.

In the modulated mode, each bit is transmitted as a burst of 6 pulses at a repetition rate of about 38kHz. Since this frequency lies between the first and second harmonics of the TV line frequency, a narrow-band IR receiver tuned to 38kHz should be used in the equipment being controlled. Although such a receiver is more expensive than a broadband one, the remote control will be less sensitive to interference and will have a longer range. However, if these requirements are not stringent, a broadband receiver could also be used to receive transmissions in the modulated mode.

Remote control systems normally detect a command continuously from the moment it is received. To distinguish between multiple keystrokes and new commands, it is then necessary to detect the length of the transmitted data words. The disadvantage of this method is that a repeated command can be seen as a new one if the data stream is interrupted by an external influence. In the SAA3004, this problem is eliminated by incorporating toggle bits in the data stream. The toggle bits change state after each key release according to the truth table given in Table 1. The toggle bits therefore inform the remote control receiver that new data is arriving so that the microcomputer can easily distinguish between new data words and repeated ones. It can also count the number of identical commands if they are issued more than once in sequence. This is an important facility for selection of Teletext pages with repeated digits, resetting clock/calendars and programming VCRs.

Figure 1a is a pulse diagram of the output signal from the SAA3004 in the unmodulated mode. The data word consists of 2 toggle bits (T1 and T0), 3 address bits (S2, S1, and S0) and 6 command bits (F, E, D, C, B, and A). Toggle Bit T1 provides additional protection against interference. If the second keystroke in a sequence of three is disturbed, the decoding part of the receiver will recognize the same data twice; the fact that T1 has changed state will indicate that a new command is being transmitted.

Figure 2 shows the timing of a single bit for each transmission mode.

A complete message always consists of 12 pulses, the timing of which is directly related to the oscillator period t_{OSC}. The pulse timing data for $f_{OSC} = 455kHz$ is as follows.

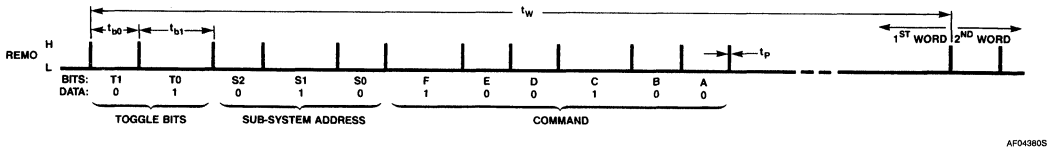
Oscillator period	$t_{OSC} = 2.2\mu s$
Pulse width	$V_{CC} = t_{MH} = 4t_{OSC} = 8.8\mu s$
Low period of modulation pulses	$t_{ML} = 8t_{OSC} = 17.6\mu s$
Modulated pulse burst period	$t_M = 12t_{OSC} = 26.4\mu s$
Duration of modulated pulse burst	$t_{PW} = 64t_{OSC} = 141\mu s$
Interval between pulses	$t_0 = 1152t_{OSC} = 2.53ms$
Data word repetition period	$t_W = 48T_0 = 121ms$
Logic '0' pulse or burst spacing	$t_{B0} = 2T_0 = 5.06ms$
Logic '1' pulse or burst spacing	$t_{B1} = 3T_0 = 7.6ms$

The data word format and timing shown in Figure 1b for the modulated mode of transmission is the same as that previously described for the unmodulated mode. In this case, however, each bit consists of a $141\mu s$ burst of 6 pulses, and toggle bit T1 is replaced by a reference pulse with a permanent logic 1, the timing of which is ($t_{REF} = t_{B1} = 7.6ms$). This allows a lower stability oscillator to be used in the transmitter because t_{REF} can be used as a reference for decoding in the equipment being controlled.

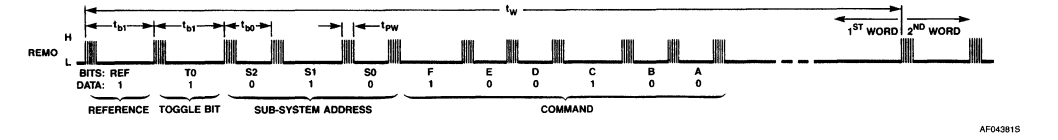
Functional Description of the SAA3004

A detailed functional block diagram of the SAA3004 is given in Figure 3 and the key sequencing diagram is given in Figure 4, which shows that, during standby, all the drive outputs are LOW. When a keystroke is detected (one or more sense inputs LOW) by the sense detector, the sequence control block enables the oscillator which starts to generate clock pulses. The oscillator increments the scan counter which, after debouncing time ($t_{DB} > 4T_0$) has elapsed, sequentially activates the drive outputs at intervals of $t_{OSC}/72$ ($158\mu s$ for $f_{OSC} = 455kHz$). See Figure 5.

The activated key position is stored in the data memory together with the subsystem address (determined by which of the drive outputs 1 – 5 is connected to ADRM) and the output mode (whether or not drive output 6 is connected to ADRM). However, unlike the command code, the subsystem address is only sensed during the first scan cycle and does not cause any output when it is changed. The stored data, together with the toggle bits, are applied to the data multiplexer, the serial output from which is converted into the correct pulse distances by the modulation counter. The pulses are then fed to

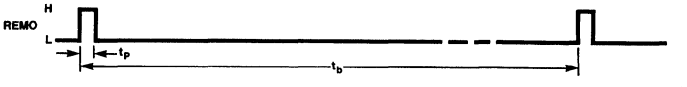


a. Unmodulated Transmission Mode

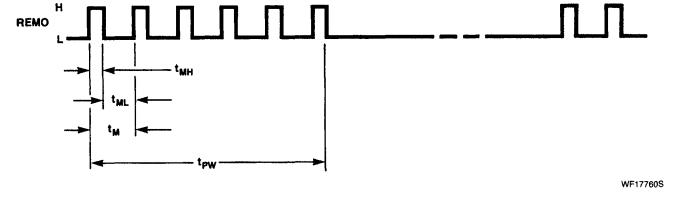


b. Modulated Transmission Mode

Figure 1. Transmission Format at Output REMO



a. Unmodulated Transmission Mode



b. Modulated Transmission Mode

Figure 2. Timing of a Single Bit at Output REMO

output REMO via the output modulator. After a key is released, the oscillator stops and the circuits return to the standby state to conserve battery power as soon as the output sequence is completed.

The SAA3004 has built-in protection against multiple keystrokes (two or more keys pressed at a time). In this event, the IC reacts as shown in Figure 6. At the end of any current output sequence, output REMO becomes inactive, and the keyboard scanning interval t_W = 121ms is reduced to t_{SM} (about 20ms). This ensures that a key release is detected as soon as possible. Also, the toggle bits remain unchanged during multiple keystrokes.

Table 1. Sequence of Toggle Bits

KEY SEQUENCE	T0	T1
n	0	1
n+1	1	1
n+2	0	0
n+3	1	0
n+4	0	1
n+5	1	1
.	.	.
.	.	.
.	.	.

A Practical IR Transmitter

An example of a complete IR remote control transmitter is given in Figure 7.

Forty-nine of the keys (7 × 7 matrix) are connected directly between driver lines DRV0N to DRV6N and sense lines SEN0N to SEN6N. Expanding the keyboard for 64 commands is done in three steps. First, seven keys are added to switch each of the sense lines to ground. Next, seven keys are added to switch each of the drive lines to SEN5N and SEN6N via diodes D_1 and D_2. The final key is added to switch sense lines SEN5N and SEN6N to ground via diodes D_1 and D_2.

In standby, the drive lines are LOW and the sense lines are HIGH. A scan cycle starts as soon as one of the sense inputs is forced LOW by a keystroke. If the keystroke is detected as being legal (only one key pressed), the appropriate command is decoded according to the scheme in Table 2, and the correct data word is fed to output REMO. Bits ABC in Table 2 indicate which of the seven driver outputs is activated and bits DEF indicate which of the seven sense inputs has detected a LOW level.

Address mode input ADRM selects the subsystem address and determines the transmission mode (modulated or unmodulated). The subsystem address and mode of operation depend on which of the seven drive lines is connected to ADRM as shown in Tab
The address is selected either by c
address switch to connect a d
input ADRM before pressin
or by installing a perm
of the drive outpu
address sele
bits S2, S1, a
ly generated.

Mode selection is
drive line DRV6N

Low-Power Remote Control IR Transmitter and Receiver AN1731

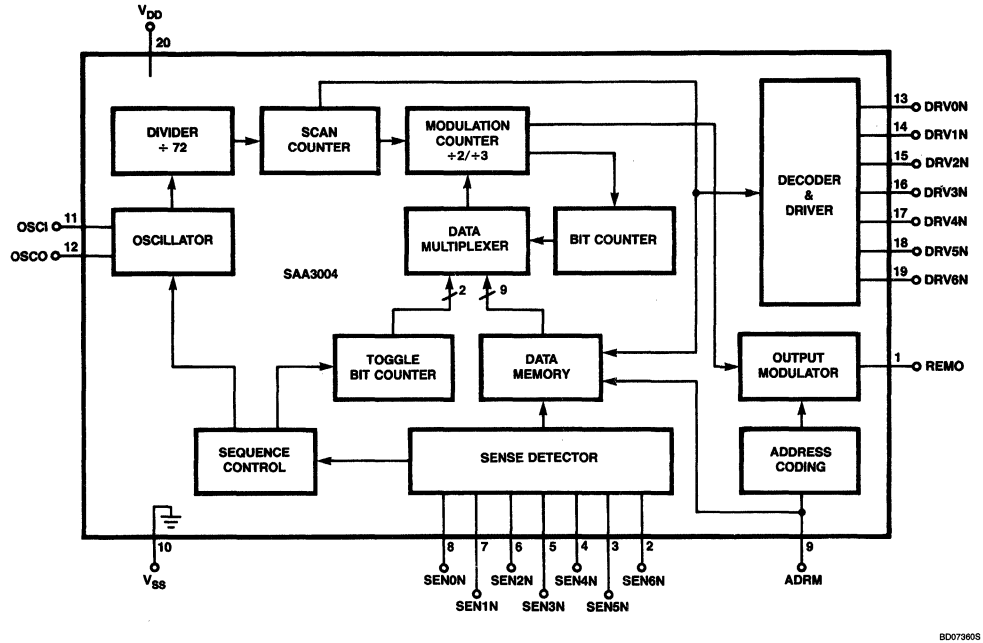
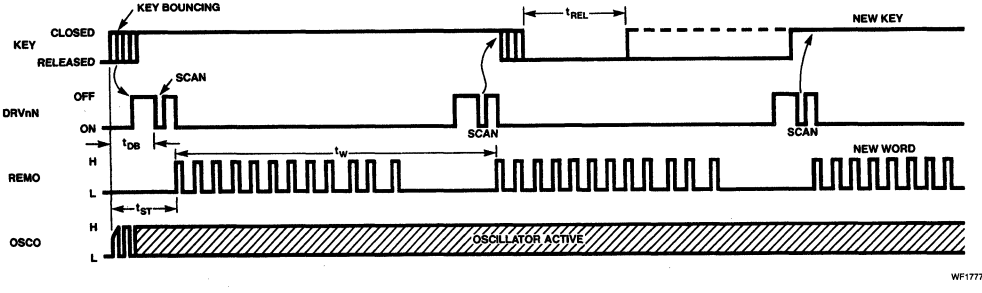


Figure 3. Block Diagram of Remote Control Transmitter SAA3004



NOTE:
$T_0 = 1152t_{OSC}$, debounce time $t_{DB} = 4$ to $9 \times t_0$, start time $t_{ST} = 5$ to $10 \times t_0$, minimum release time $t_{REL} = t_0$.

Figure 4. Single Keystroke Sequence

transmission is modulated with the link fitted or unmodulated without it.

Capacitors C_1 and C_2 associated with the oscillator must be chosen with regard to low current consumption and quick starting over whole supply voltage range.

The output stage of the SAA3004 shown in Figure 8 provides a current output of up to 40mA with a 6V supply, sufficient to drive a very simple single transistor amplifier to provide current for an infrared LED. When the output stage is driven by a HIGH level, the NPN transistor conducts and pulls output pin REMO HIGH (3V min. with a 6V supply). When the output stage is driven by a LOW level, the NPN transistor is turned off and the n-channel output FET conducts and pulls output pin REMO LOW (200mV maximum with a 6V supply). In this state, the output stage can sink a typical current of 300μA.

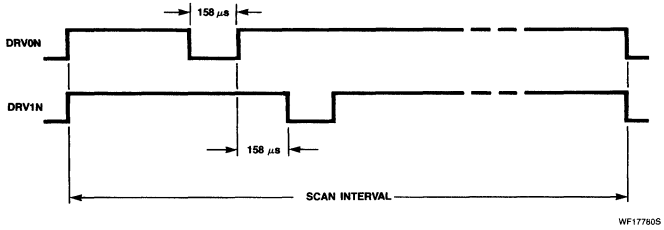
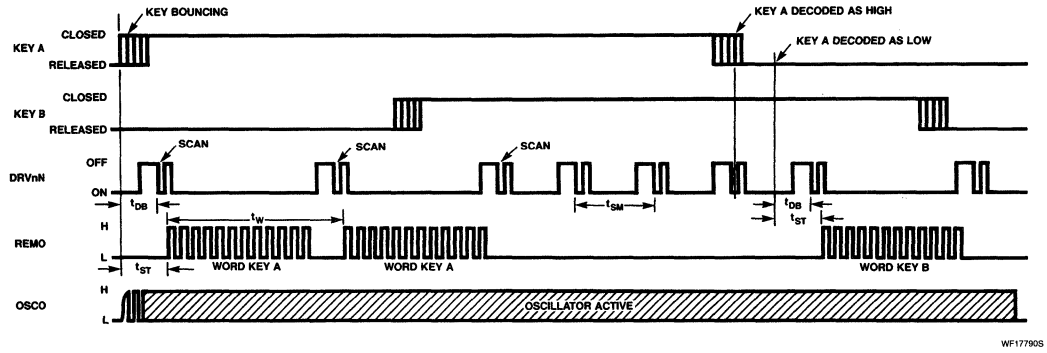


Figure 5. Timing at Outputs DRV0N to DRV6N

Table 2. Key Codes

MATRIX POS.	CODE F	E	D	C	B	A	MATRIX POS.	CODE F	E	D	C	B	A
0	0	0	0	0	0	0	32	1	0	0	0	0	0
1	0	0	0	0	0	1	33	1	0	0	0	0	1
2	0	0	0	0	1	0	34	1	0	0	0	1	0
3	0	0	0	0	1	1	35	1	0	0	0	1	1
4	0	0	0	1	0	0	36	1	0	0	1	0	0
5	0	0	0	1	0	1	37	1	0	0	1	0	1
6	0	0	0	1	1	0	38	1	0	0	1	1	0
7	0	0	0	1	1	1	39	1	0	0	1	1	1
8	0	0	1	0	0	0	40	1	0	1	0	0	0
9	0	0	1	0	0	1	41	1	0	1	0	0	1
10	0	0	1	0	1	0	42	1	0	1	0	1	0
11	0	0	1	0	1	1	43	1	0	1	0	1	1
12	0	0	1	1	0	0	44	1	0	1	1	0	0
13	0	0	1	1	0	1	45	1	0	1	1	0	1
14	0	0	1	1	1	0	46	1	0	1	1	1	0
15	0	0	1	1	1	1	47	1	0	1	1	1	1
16	0	1	0	0	0	0	48	1	1	0	0	0	0
17	0	1	0	0	0	1	49	1	1	0	0	0	1
18	0	1	0	0	1	0	50	1	1	0	0	1	0
19	0	1	0	0	1	1	51	1	1	0	0	1	1
20	0	1	0	1	0	0	52	1	1	0	1	0	0
21	0	1	0	1	0	1	53	1	1	0	1	0	1
22	0	1	0	1	1	0	54	1	1	0	1	1	0
23	0	1	0	1	1	1	55	1	1	0	1	1	1
24	0	1	1	0	0	0	56	1	1	1	0	0	0
25	0	1	1	0	0	1	57	1	1	1	0	0	1
26	0	1	1	0	1	0	58	1	1	1	0	1	0
27	0	1	1	0	1	1	59	1	1	1	0	1	1
28	0	1	1	1	0	0	60	1	1	1	1	0	0
29	0	1	1	1	0	1	61	1	1	1	1	0	1
30	0	1	1	1	1	0	62	1	1	1	1	1	0
31	0	1	1	1	1	1	63	1	1	1	1	1	1



NOTE:
$t_0 = 1152t_{OSC}$, debounce time $t_{DB} = 4$ to $9 \times t_0$, scan rate $t_{SM} = 6$ to $10 \times t_0$.

Figure 6. Multiple Keystroke Sequence

Table 3. Transmission Mode and Subsystem Address Selection

OUTPUT FORMAT	SUBSYSTEM ADDRESS				DRIVE OUTPUT DRVnN n =						
	No.	S2	S1	S0	0	1	2	3	4	5	6
unmodulated	1	1	1	1							
	2	0	0	0	X						
	3	0	0	1	–	X					
	4	0	1	0	–	–	X				
	5	0	1	1	–	–	–	X			
	6	1	0	0	–	–	–	–	X		
	7	1	0	1	–	–	–	–	–	X	
modulated	1	1	1	1							X
	2	0	0	0	X						X
	3	0	0	1	–	X					X
	4	0	1	0	–	–	X				X
	5	0	1	1	–	–	–	X			X
	6	1	0	0	–	–	–	–	X		X
	7	1	0	1	–	–	–	–	–	X	X

NOTES:
X Connected to ADRM.
– Allowed connection to ADRM without any influence on the subsystem address.

Power Consumption Considerations

The intensity of IR radiation I_E, and therefore the transmitter range, is proportional to the LED forward current I_F. The peak value of I_F in the circuit of Figure 7 is determined by the value of emitter resistor R_E and is given by:

$$I_F = (V_{REF} - V_{BE})/R_E.$$

'owever, since the output is pulsed, the 'tery life is mainly determined by the aver- value of the forward current. This aver- age LED current is the peak current multiplied by the duty factor of the output signal. The duty factor is the ratio of the total HIGH time of a data word (12 pulses each of width $T_P = 8.8\mu s$) to the data word repetition period ($t_W = 121ms$).

In the unmodulated mode, the average LED current is:

$$I_{Fav} = I_F(12t_P/t_W) = 8.7I_F \times 10^{-4}.$$

In the modulated mode, each pulse is a burst of six 8.8μs pulses. The total HIGH time of a data word is therefore six times that for the unmodulated mode so that the duty factor is multiplied by six.

In the modulated mode, the average LED current is therefore:

$$I_{Fav} = 52I_F \times 10^{-4}.$$

At first glance, the higher required average current for the modulated mode makes it appear unattractive because of increased battery drain. However, if a narrow-band receiver is used with a modulated transmitter,

Low-Power Remote Control IR Transmitter and Receiver AN1731

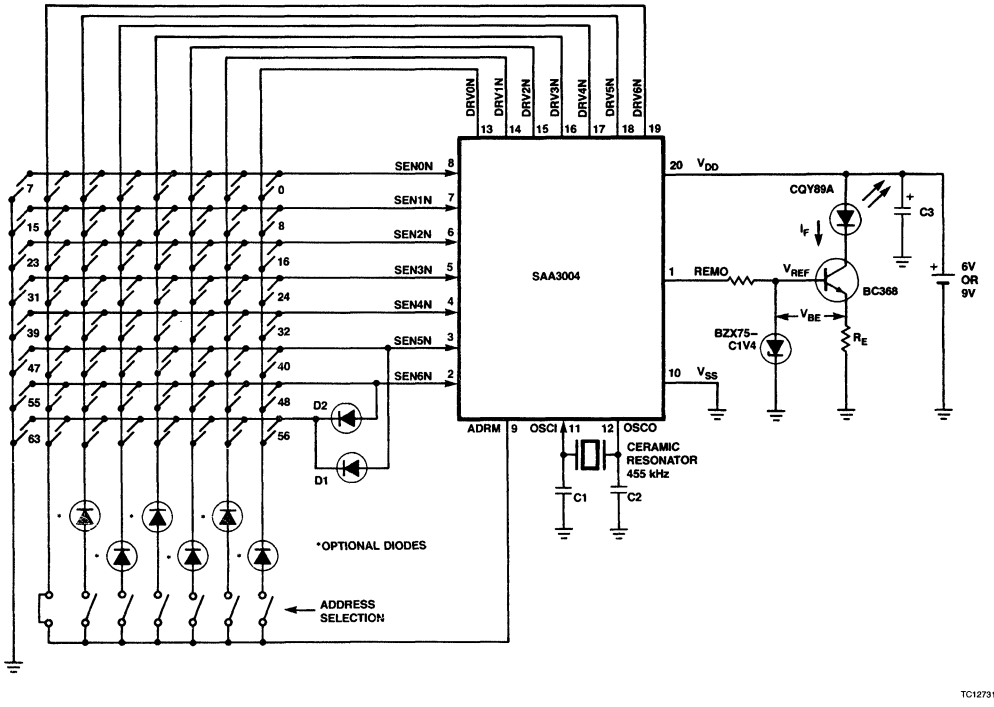


Figure 7. A Complete Remote Control Infrared Transmitter Using SAA3004

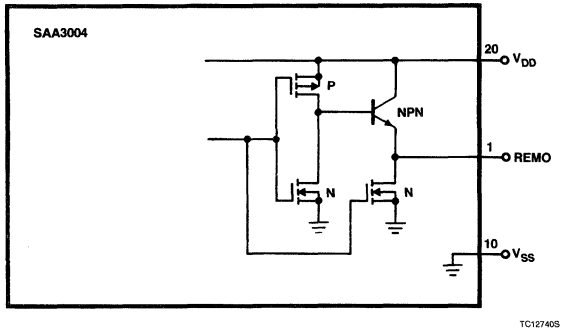


Figure 8. Output Stage of the SAA3004

this will not be the case because the resonance peak of the tuned circuit at the input makes a narrow-band receiver more sensitive to infrared radiation and less sensitive to interference than a broadband receiver. For a given remote control range, then, the required forward current for the transmitter LED is less than that required for an LED in an unmodulated transmitter used with a broadband receiver. This is confirmed by the range measurement results given at the end of this publication.

The total current drain from the battery when the transmitter is in use is the sum of I_{Fav}, the very small leakage current of the battery buffer electrolytic capacitor C_3, and the current drain of the SAA3004 (typically 1mA with a 6V supply or 3mA with a 9V supply). During standby, the maximum current drain of the SAA3004 is 2μA, regardless of the supply voltage.

INFRARED RECEIVER PREAMPLIFIERS TDA3047 AND TDA3048

The TDA3047 and TDA3048 are bipolar preamplifier ICs for infrared remote control receivers. The ICs differ only in the polarity of the output signal; the TDA3047 is activ HIGH and the TDA3048 is active LOW choice of polarity allows the preampl be selected to suit the micropro system being controlled. Fo 8048 microprocessor i level (active-LOW in the correct choice. Po ICs is only 10mW from

considerably less than that of earlier preamplifier ICs. Operation from a 5V supply means that the preamplifiers can use the same supply as the microprocessor in the equipment being controlled.

Both ICs are excellent for use in narrow-band IR receivers which are necessary to achieve high noise immunity and long range for the reception of a modulated data stream. The ICs can also be used in inexpensive broadband IR receivers for the reception of unmodulated data or modulated data if noise immunity and long range are not of major importance.

The 66dB AGC range of the ICs ensures stable amplification of a wide range of signal levels, thus allowing remote-control systems to operate over a wide range of transmitter-to-receiver distances.

The ICs in a Narrow-Band IR Receiver

The functional block diagram of the TDA3047/48 in a narrow-band IR receiver is shown in Figure 9. Figure 10 shows some of the internal circuitry connected to the IC pins.

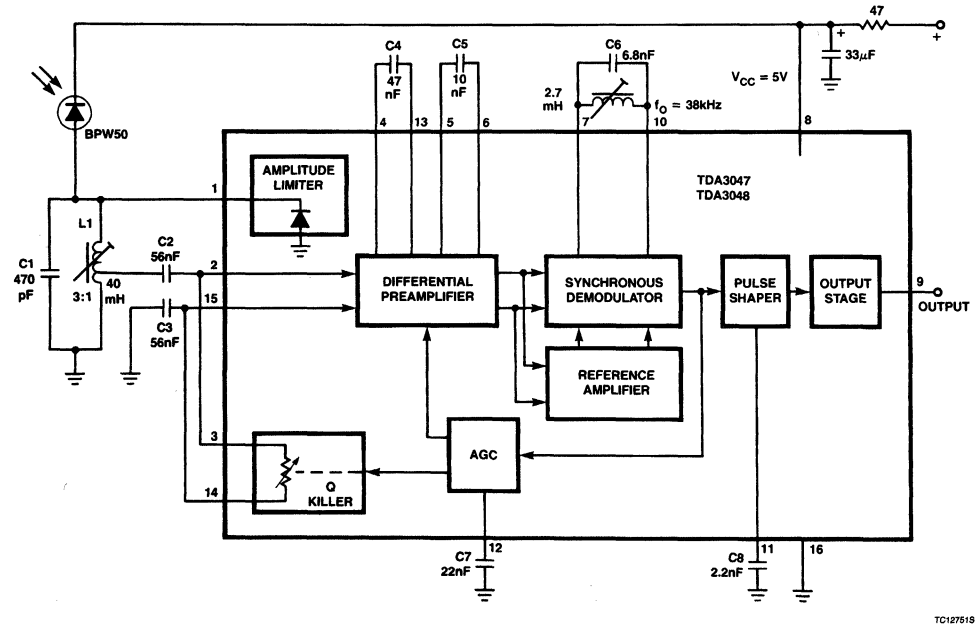
The input signal from the photodiode is coupled to input Pins 2 and 15 via a 38kHz parallel tuned circuit with a Q of about 10 giving a bandwidth of about 3kHz. This considerably improves selectivity and attenuates continuous IR interference caused, for example, by sunlight. The low resistance of L_1 (125Ω) ensures that the photodiode never saturates. The tapping point for the coil (3:1) is chosen to match the input resistance of the IC (16kΩ) and is optimum for low-level signals (Q-killer inactive) so that the operating range of the remote-control system remains almost independent of component value spreads or frequency tolerance in either the transmitter or the receiver.

Alternatively, L_1 could be capacitively tapped as shown in Figure 11. The total capacitance of C_{1a} and C_{1b} must be that required to tune the circuit to 38kHz (470pF with a 40mH coil). The ratio C_{1a}/C_{1b} must be 3:1. Values of 2.2nF for C_{1a} and 560pF for C_{1b} meet these requirements and give about the same Q as the input tuned circuit given in Figure 9.

The signal from the tuned circuit is capacitively-coupled to Pins 2 and 15 of the IC and is then amplified by an internal two-stage gain-controlled differential amplifier. The first stage of the differential amplifier has a maximum gain of 56dB, and the second stage has a maximum gain of 26dB, giving overall gain of more than 80dB. Feedback capacitors C_4 and C_5 stabilize the first and second stage, respectively. Together, they set the lower frequency limit of the circuit, C_4 having the most effect because the first stage has the higher gain. The values of both capacitors should be chosen such that IR interference is suppressed, bearing in mind that incandescent lamps radiate IR at multiples of 100Hz. The upper frequency limit of the amplifier is set by internal capacitance and is above 1MHz.

The amplified signal is fed to a synchronous demodulator and a reference amplifier that limits high amplitude input signals. The 2.7mH coil in the 38kHz demodulator tuned circuit has a Q of about 7 in conjunction with the resistance between Pins 7 and 10 (6kΩ).

After multiplication of the input and reference signals, the demodulated signal is fed to a pulse shaper and an AGC circuit. A Q-killer in the AGC loop damps the Q of the input tuned circuit for high level inputs so that the circuit can handle large variations of signal amplitude. An absolute maximum input level of about 600mV is set by the limiter at Pin 1. The AGC acquisition time and the time constant of the pulse shaper are determined by C_7 at Pin



NOTE:
Capacitor C_5 should be kept well clear of the input pins.

Figure 9. TDA3047/3048 in a Narrow-Band IR Receiver

12 and C_8 at Pin 11, respectively. The time constant at Pin 12 is equal to the duration of one data bit. The time constant at Pin 11 sets the delay between the pulse shaper and the output stage. The value of C_8 must be low enough to ensure that, with a charging time of one pulse width (8.8μs from the SAA3004 transmitter), the threshold of the pulse shaper (about 4V) can be exceeded. If the value of C_8 is too low, however, short duration interference pulses can easily trigger the pulse shaper. The value of C_8 is therefore a compromise between the receiver sensitivity and immunity to interference.

The ICs in a Broadband IR Receiver

The TDA3047 and TDA3048 are shown in a broadband IR receiver circuit in Figure 12. This circuit is similar to the previously described narrow-band receiver except that the Q-Killer and amplitude limiter are not necessary. (Pins 1, 3, 14 are not used.) Also, the IR photodiode is simply connected between two 12kΩ load resistors and connected to the IC inputs via 10nF capacitors instead of via a tuned circuit.

CONTROL SYSTEM RANGE MEASUREMENTS

Measurements have been made with both IR receivers in conjunction with an IR transmitter based on the SAA3004 to determine the operating range.

As previously explained, when the SAA3004 transmitter in the unmodulated mode drives a single infrared LED with a constant peak forward current I_F of 2A, the average current, which is proportional to the infrared radiation, is:

$$I_{Fav} = 8.7I_F \times 10^{-4} = 1.7\text{mA}.$$

Under these conditions, the range of the remote-control was 11m with a narrow-band receiver and 12m with a broadband receiver.

Under the same conditions in the modulated mode, the average current is:

$$I_{Fav} = 52I_F \times 10^{-4} = 10.4\text{mA}.$$

Under these conditions, the range of the remote-control was 25m with a narrow-band receiver and 16m with a broadband receiver.

To allow direct comparison between the two transmission modes, the average LED current for the modulated mode was reduced to 1.7mA. Under these conditions, the range of the remote-control was 11m with a narrow-band receiver and 8m with a broadband receiver.

Originally published as Technical Publication 167, March 22, 1985, The Netherlands.

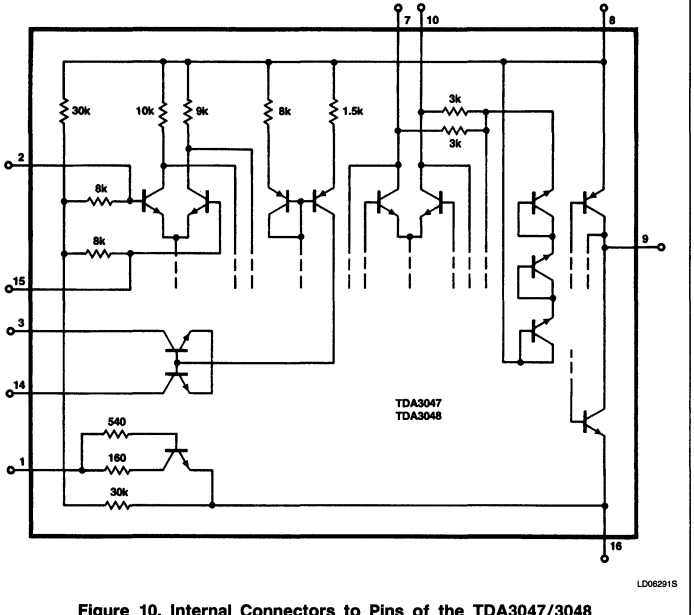


Figure 10. Internal Connectors to Pins of the TDA3047/3048

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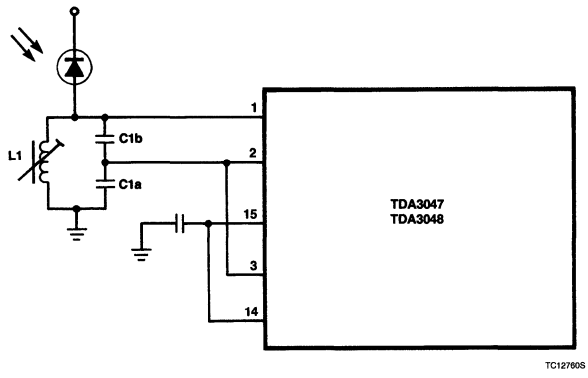


Figure 11. Alternative Input Coupling for a Narrow-Band IR Receiver

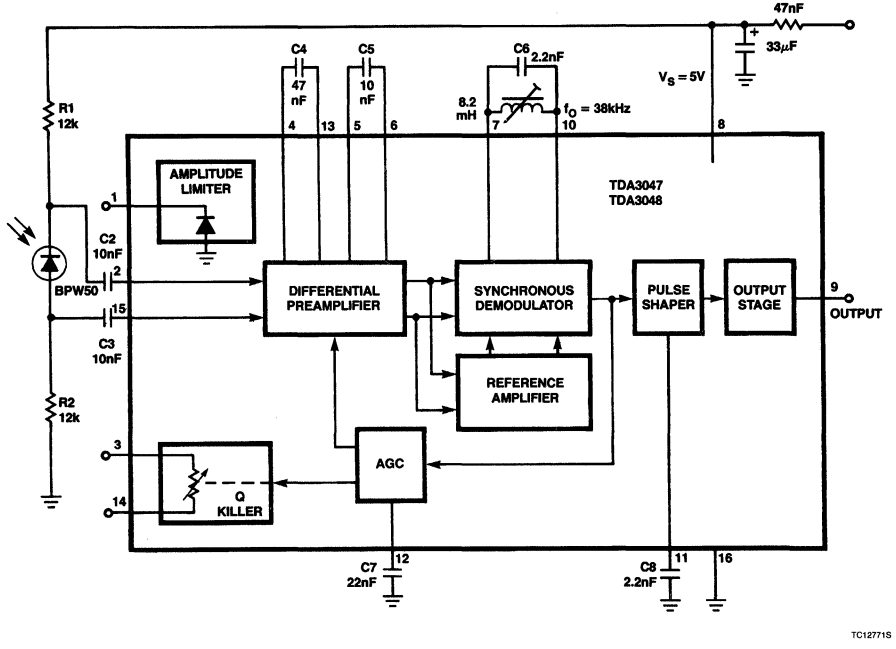


Figure 12. TDA3047/3048 in a Broadband IR Receiver

SAA3006
Infrared Transmitter

Product Specification

Linear Products

DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

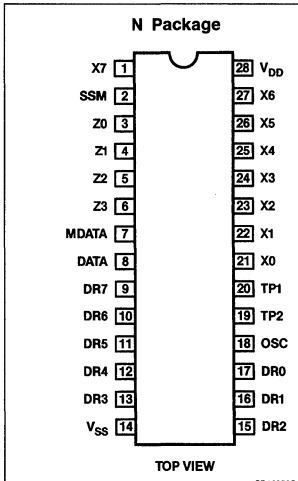
FEATURES

- **Low supply voltage requirements**
- **Very low current consumption**
- **For infrared transmission link**
- **Transmitter for 32 × 64 commands**
- **One transmitter controls 32 systems**
- **Transmission biphase technique**
- **Short transmission times; speed-up of system reaction time**
- **Single-pin oscillator input**
- **Input protection**
- **Test mode facility**

APPLICATIONS

- **Audio**
- **TV**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	X7	Keyboard command inputs with P-channel pull-up transistors
21	X0	
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
2	SSM	System mode selection input
3	Z0	Keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
7	MDATA	Remote signal outputs (3-state outputs)
8	DATA	
9	DR7	Scan driver outputs with open-drain N-channel transistors
10	DR6	
11	DR5	
12	DR4	
13	DR3	
15	DR2	
16	DR1	
17	DR0	
14	V_{SS}	Negative supply (ground)
18	OSC	Oscillator input
19	TP2	Test input/output
20	TP1	Test input
28	V_{DD}	Positive supply

ORDERING INFORMATION

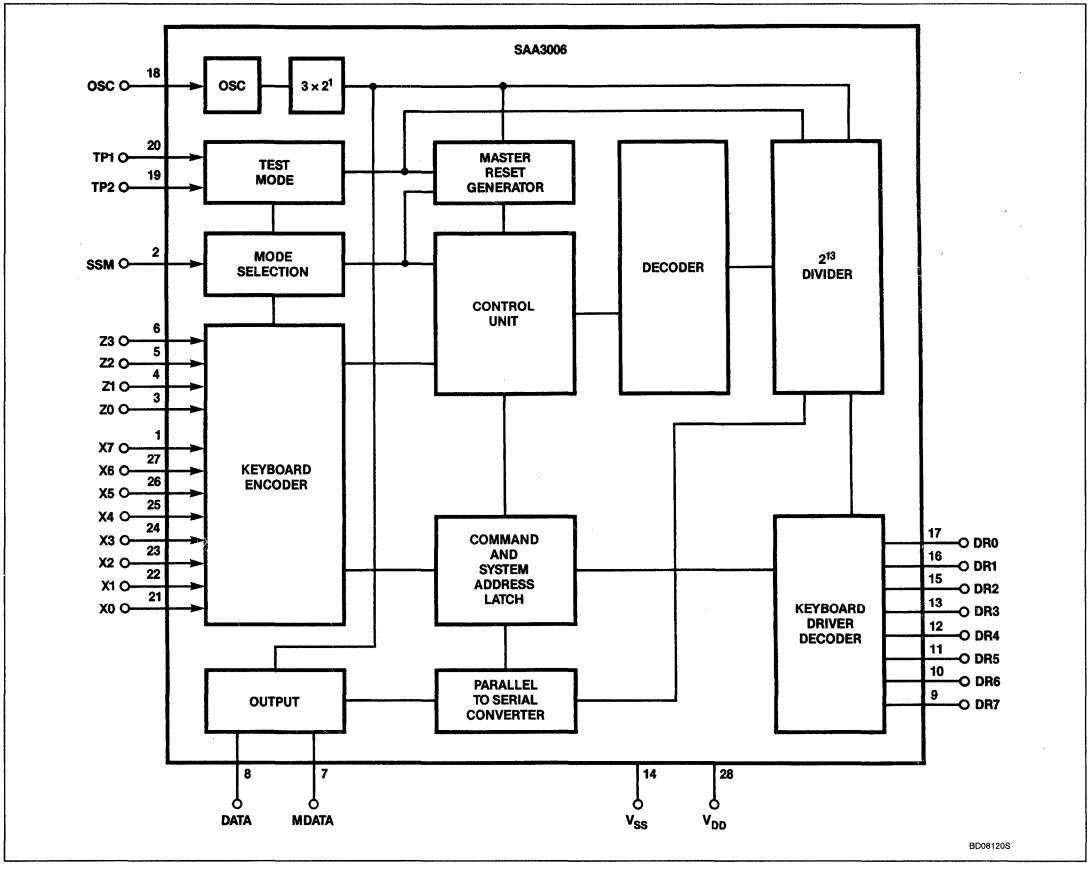
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +85°C	SAA3006PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range with respect to V_{SS}	−0.5 to +8.5	V
V_I	Input voltage range	−0.5 to (V_{DD} + 0.5)	V[1]
$+I_I$	Input current	10	mA
V_O	Output voltage range	−0.5 to (V_{DD} + 0.5)	V[1]
$+I_O$	Output current	10	mA
P_O	Power dissipation output OSC	50	mW
P_O	Power dissipation per output (all other outputs)	100	mW
P_{TOT}	Total power dissipation per package	200	mW
T_A	Operating ambient temperature range	−25 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. V_{DD}+0.5V not to exceed 9V.

BLOCK DIAGRAM

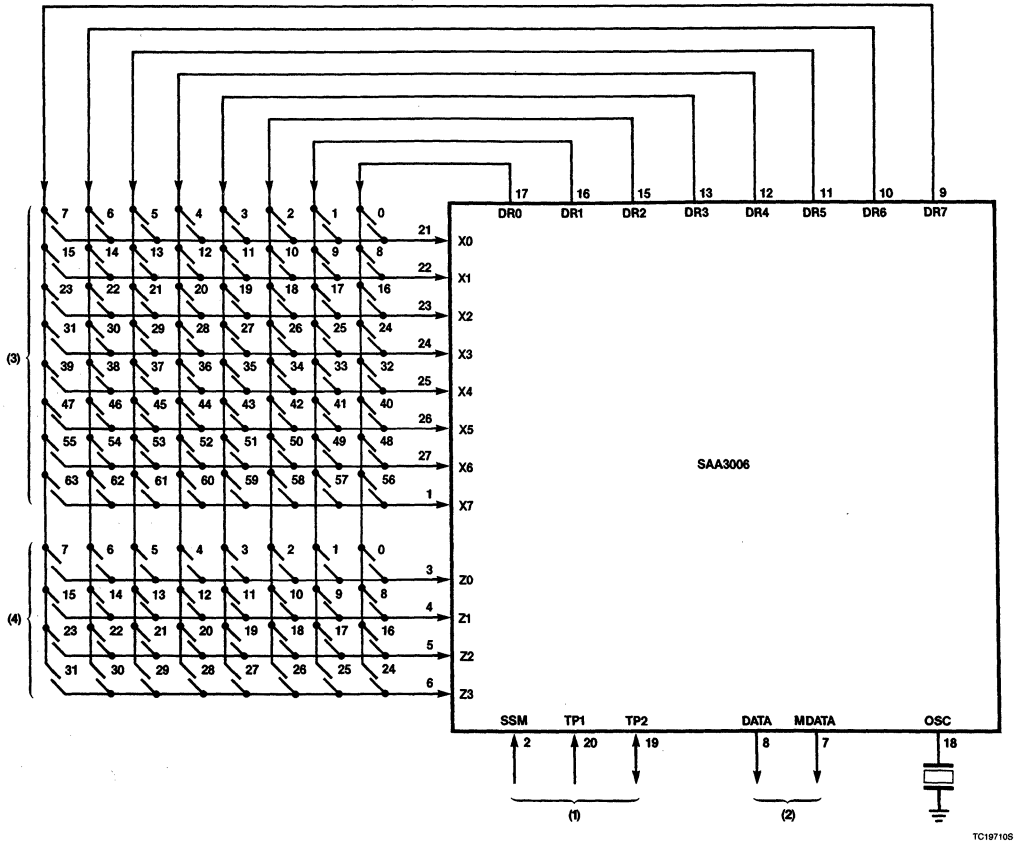


DC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$; $T = -25$ to $85°C$, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		2		7	V
	Supply current at $I_O = 0mA$ for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open-drain N-channel outputs					
I_{DD}	$T_A = 25°C$	7			10	μA
Inputs Keyboard inputs X and Z with P-channel pull-up transistors						
$-I_I$	Input current (each input) at $V_I = 0V$; TP = SSM = LOW	2 to 7	10		600	μA
V_{IH}	Input voltage HIGH	2 to 7	$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Input voltage LOW	2 to 7	0		$0.3 \times V_{DD}$	V
	Input leakage current at $T_A = 25°C$; TP = HIGH;					
I_{IR}	$V_I = 7V$				1	μA
$-I_{IR}$	$V_I = 0V$				1	μA
SSM, TP1 and TP2						
V_{IH}	Input voltage HIGH	2 to 7	$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Input voltage LOW	2 to 7	0		$0.3 \times V_{DD}$	V
	Input leakage current at $T_A = 25°C$;					
I_{IR}	$V_I = 7V$				1	μA
$-I_{IR}$	$V_I = 0V$				1	μA
OSC						
$-I_I$	Input leakage current at $T_A = 25°C$; $V_I = 0V$; TP1 = HIGH; Z2 = Z3 = LOW	2 to 7			2	μA
Outputs DATA and MDATA						
V_{OH}	Output voltage HIGH at $-I_{OH} = 0.4mA$	2 to 7	$V_{DD} - 0.3$			V
V_{OL}	Output voltage LOW at $I_{OL} = 0.6mA$	2 to 7			0.3	V
	Output leakage current at:					
I_{OR}	$V_O = 7V$				10	μA
$-I_{OR}$	$V_O = 0V$				20	μA
	$T_A = 25°C$;					
I_{OR}	$V_O = 7V$				1	μA
$-I_{OR}$	$V_O = 0V$				2	μA
DR0 to DR7, TP2						
V_{OL}	Output voltage LOW at $I_{OL} = 0.3mA$	2 to 7			0.3	V
	Output leakage current					
I_{OR}	at $V_O = 7V$	7			10	μA
	at $V_O = 7V$;					
I_{OR}	$T_A = 25°C$				1	μA

DC ELECTRICAL CHARACTERISTICS (Continued) V_{SS} = 0V; T = −25 to 85°C, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
OSC						
I_{OSC}	Oscillator current at OSC = V_{DD}	7	4.5		30	μA
Oscillator						
f_{OSC}	Maximum oscillator frequency at C_L = 40pF (Figures 4 and 5)	2			450	kHz
f_{OSC}	Free-running oscillator frequency at T_A = 25°C	2	10		120	kHz



NOTES:
1. Control inputs for operating modes, test modes and reset.
2. Remote signal outputs.
3. Keyboard command code matrix 8 × 8.
4. Keyboard system code matrix 4 × 8.

Figure 1. Keyboard Interconnection

FUNCTIONAL DESCRIPTION

Combined System Mode (SSM = LOW)

The X and Z lines are active-HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X input senses a LOW level, a latch enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z or X input matrix. After latching a system address number, the device will generate the last command (i.e., all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single System Mode (SSM = HIGH)

The X lines are active-HIGH in the quiescent state; the pull-up transistors of the Z lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X lines are switched off. Those in the Z lines are switched on during the first scan cycle. The wired connection in the Z matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z lines are switched off and the inputs are disabled again, while the transistors in the X lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

The oscillator is formed by a ceramic resonator (cataloq number 2422 540 98021 or equivalent) feeding the single-pin input OSC. Direct connection is made for supply voltages in the range 2 to 5.25V but it is necessary to fit a 10kΩ resistor in series with the resonator when using supply voltages in the range 2.6 to 7V.

Key Release Detection

An extra control bit is added which will be complemented after key release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g., by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'takeover' of key operation during the code transmission, the correct system and command numbers are generated.

Outputs

The output DATA carries the generated information according to the format given in Figure 2 and Tables 2 and 3. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Figure 3.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1')
- Control part formed by 1 bit
- System part formed by 5 bits
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of $1/12$ the oscillator frequency, so that each bit is presented as a burst of 32 pulses. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open-drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation all the driver outputs go into the high ohmic state; a scanning procedure is then started so that the outputs are switched into the conducting state one after the other.

Reset Action

The circuit will be reset immediately when a key release occurs during:

- Debounce time
- Between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- The key is released while one of the driver outputs is in the low-ohmic '0' state
- The key is released before detection of that key
- There is no wired connection in the Z-DR matrix while SSM is HIGH.

Test Pin

The test pins TP1 and TP2 are used for testing in conjunction with inputs Z2 and Z3 as shown in Table 1.

Table 1. Test Functions

TP1	TP2	Z2	Z3	FUNCTION
LOW	LOW	Matrix input	Matrix input	Normal
LOW	HIGH	Matrix input	Matrix input	Scan + output frequency 6 times faster than normal
HIGH	Output $f_{OSC}{}^6$	LOW	LOW	Reset
HIGH	Output $f_{OSC}{}^6$	HIGH	HIGH	Output frequency 3×2^7 faster than normal

KEY ACTIVITIES

Every connection of one X input and one DR output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z input and one DR output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z inputs, or Z inputs and X inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z input and a DR output. If no connection is made, the code is not generated.

When one X or Z input is connected to more than one DR output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 7kΩ.

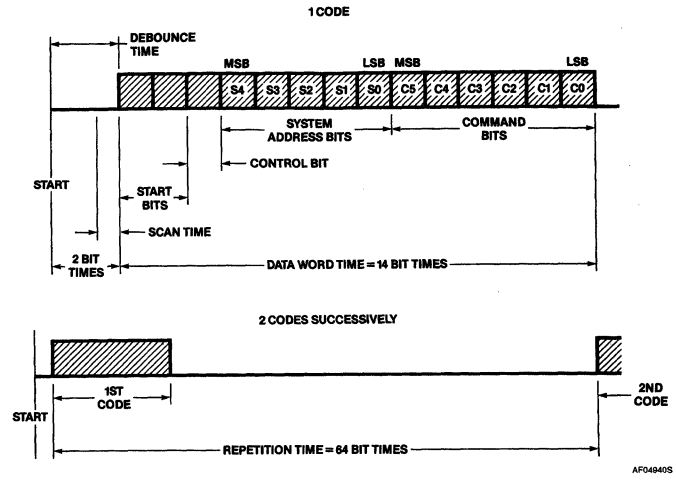
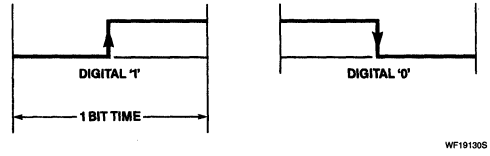


Figure 2. DATA Output Format (RC-5)



NOTE:
1. Bit time = $3 \times 2^8 \times t_{OSC}$ (typically 1.778ms) where t_{OSC} is the oscillator period time.

Figure 3. Biphase Transmission Code

Table 2. Command Matrix X-DR

CODE NO	X-LINES X								DR-LINES DR								COMMAND BITS C					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

5

Table 2. Command Matrix X-DR (Continued)

CODE NO	X-LINES X								DR-LINES DR								COMMAND BITS C					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 3. System Matrix Z-DR

SYSTEM NO	Z-LINES Z				DR-LINES DR								SYSTEM BITS S				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

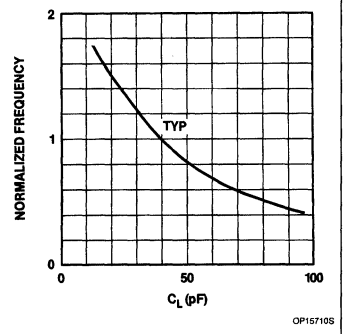


Figure 4. Typical Normalized Input Frequency as a Function of the Load (Keyboard) Capacitance

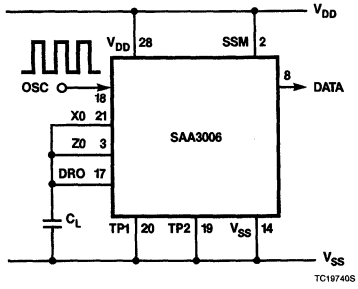


Figure 5. Test Circuit for Measurement of Maximum Oscillator Frequency

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

SAA3027
Infrared Remote Control Transmitter (RC-5)

Product Specification

DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

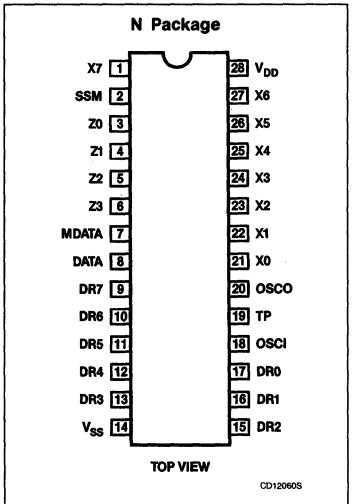
FEATURES

- **Transmitter for 32 × 64 commands**
- **One transmitter controls 32 systems**
- **Very low current consumption**
- **For infrared transmission link**
- **Transmission by biphase technique**
- **Short transmission times; speed-up of system reaction time**
- **LC oscillator; no crystal required**
- **Input protection**
- **Test mode facility**

APPLICATION

- **Remote control systems**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	X7	Keyboard command inputs with P-channel pull-up transistors
21	X0	
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
2	SSM	System mode selection input
3	Z0	Keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
7	MDATA	Remote signal outputs (3-state outputs)
8	DATA	
9	DR7	Scan driver outputs with open-drain N-channel transistors
10	DR6	
11	DR5	
12	DR4	
13	DR3	
15	DR2	
16	DR1	
17	DR0	
14	V_{SS}	Negative supply (ground)
18	OSCI	Oscillator input
19	TP	Test pin
20	OSC0	Oscillator output
28	V_{DD}	Positive supply

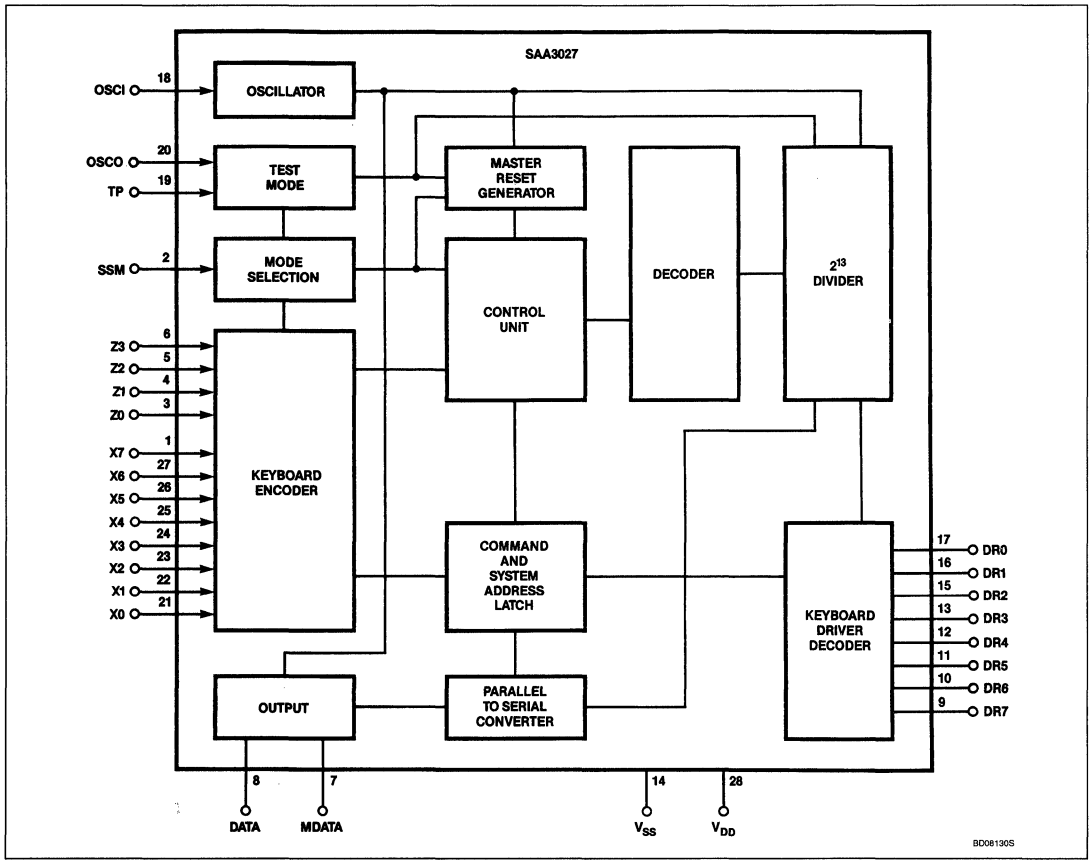
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +85°C	SAA3027PN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range with respect to V_{SS}	−0.5 to +15	V
V_I	Input voltage range	−0.5 to (V_{DD} + 0.5)	V
$\pm I_I$	Input current	10	mA
V_O	Output voltage range	−0.5 to (V_{DD} + 0.5)	V
$\pm I_O$	Output current	10	mA
P_O	Power dissipation output OSCO	50	mW
P_O	Power dissipation per output (all other outputs)	100	mW
P_{TOT}	Total power dissipation per package	200	mW
T_A	Operating ambient temperature range	−25 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



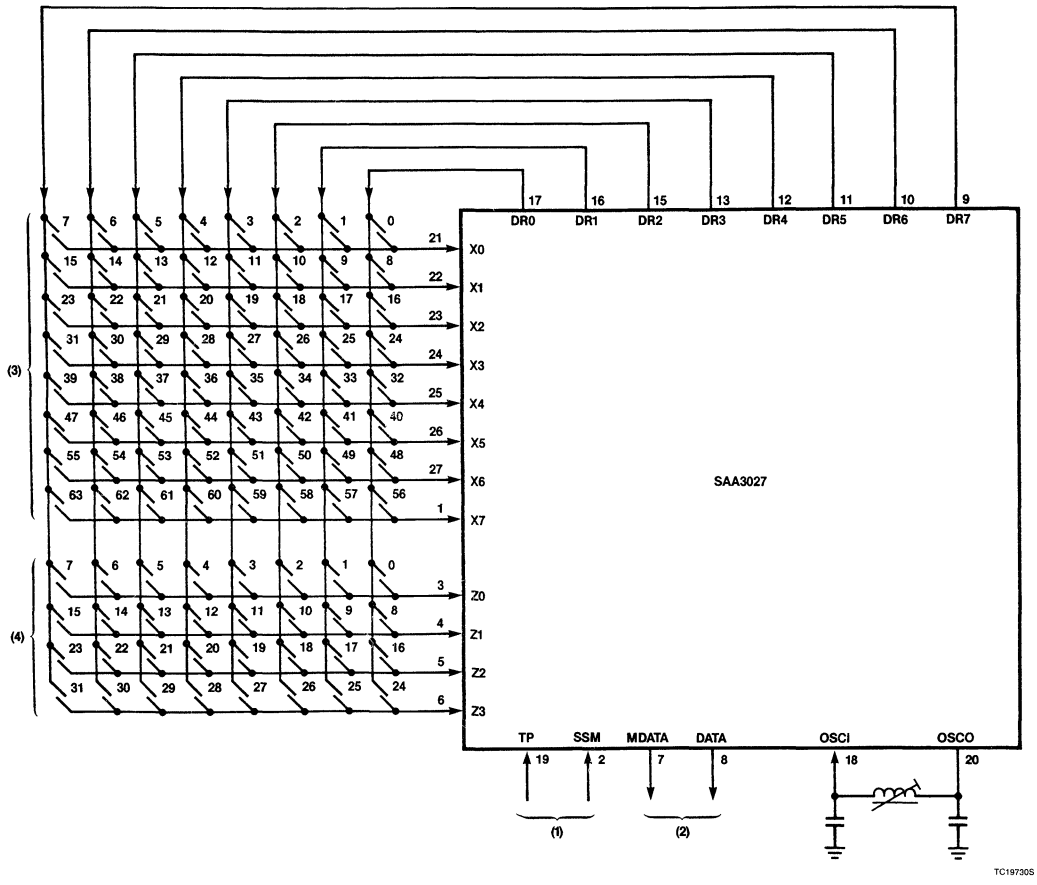
DC AND AC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_A = −25°C to 85°C, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.75		12.6	V
	Supply current at I_O = 0mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs;					
I_{DD}	T_A = 25°C	12.6			10	μA
Inputs Keyboard inputs X and Z with P-channel pull-up transistors						
$-I_I$	Input current (each input) at V_I = 0V; TP = SSM = LOW	4.75 to 12.6	10		300	μA
V_{IH}	Input voltage HIGH	4.75 to 12.6	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage LOW	4.75 to 12.6	0		0.3 × V_{DD}	V
	Input leakage current at T_A = 25°C; TP = HIGH;					
I_{IR}	V_I = 12.6V	12.6			1	μA
$-I_{IR}$	V_I = 0V	12.6			1	μA
SSM, TP and OSCI inputs						
V_{IH}	Input voltage HIGH	4.75 to 12.6	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage LOW	4.75 to 12.6	0		0.3 × V_{DD}	V
	Input leakage current at T_A = 25°C;					
I_{IR}	V_I = 12.6V	12.6			1	μA
$-I_{IR}$	V_I = 0V	12.6			1	μA
Outputs **DATA, MDATA**						
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 0.8mA	4.75 to 12.6	V_{DD} −0.6			V
V_{OL}	Output voltage LOW at I_{OL} = 0.8mA	4.75 to 12.6			0.4	V
	Output leakage current at:					
I_{OR}	V_O = 12.6V	12.6			10	μA
$-I_{OR}$	V_O = 0V	12.6			20	μA
	T_A = 25°C;					
I_{OR}	V_O = 12.6V	12.6			1	μA
$-I_{OR}$	V_O = 0V	12.6			2	μA
DR0 to DR7 outputs						
V_{OL}	Output voltage LOW at I_{OL} = 0.35mA	4.75 to 12.6			0.4	V
	Output leakage current					
I_{OR}	at V_O = 12.6V	12.6			10	μA
	at V_O = 12.6V;					
I_{OR}	T_A = 25°C	12.6			1	μA
OSCO output						
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 0.2mA; OSCI = V_{SS}	4.75 to 12.6	V_{DD} − 0.6			V
V_{OL}	Output voltage LOW at $-I_{OL}$ = 0.45mA; OSCI = V_{DD}	4.75 to 12.6			0.5	V
Oscillator						
	Maximum oscillator frequency					
f_{OSCI}	at C_L = 40pF (Figures 4 and 5)	4.75	75	72		kHz
f_{OSCI}		6	120	72		kHz
f_{OSCI}		12.6	300	72		kHz

5

Handling

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.



NOTES:
(1) Programming inputs for operating modes, test mode and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 × 8.
(4) Keyboard system code matrix 4 × 8.

Figure 1. Keyboard Interconnection

FUNCTIONAL DESCRIPTION

Combined System Mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches; depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the device will generate the last command (i.e., all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single System Mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off; those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input/output, respectively, of a two-pin oscillator. The oscillator is formed externally by one inductor and two capacitors and operates at 72kHz (typical).

Key-Release Detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

Outputs

The output DATA carries the generated information according to the format given in Figure 2 and Tables 1 and 2. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Figure 3.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1')
- Control part formed by 1 bit
- System part formed by 5 bits
- Command part formed by 6 bits

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of half the oscillator frequency, so that each bit is presented as a burst of 32 oscillator periods. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation, a scanning procedure is started so that they are switched into the conducting state one after the other.

Reset Action

The circuit will be reset immediately when a key release occurs during:

- Debounce time
- Between two codes

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- The key is released while one of the driver outputs is in the low-ohmic '0' state;
- The key is released before detection of that key;
- There is no wired connection in the Z-DR matrix while SSM is HIGH.

Test Pin

The test pin TP is an input which can be used for testing purposes.

When LOW, the circuit operates normally.

When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.

When Z2 = Z3 = LOW, the counter will be reset to zero.

Key Activities

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 10kΩ

Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current.

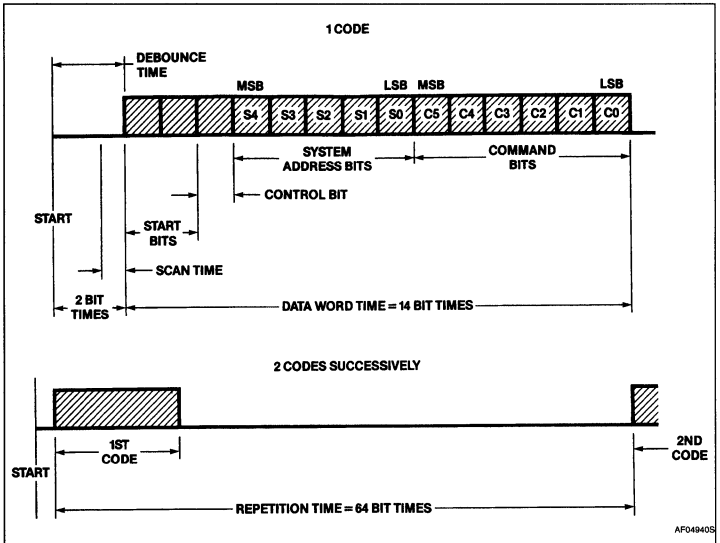
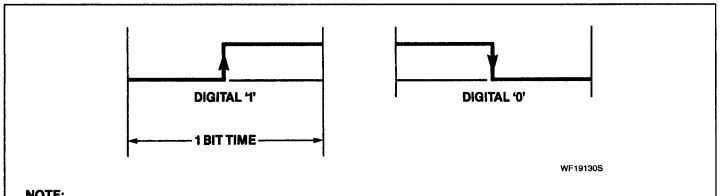


Figure 2. DATA Output Format (RC-5)



NOTE:
1. Bit Time = $2^7 \times T_{OSC}$ = 1.778ms (Typical), where T_{OSC} is the oscillator period time.

Figure 3. Biphase Transmission Code

Table 1. Command Matrix X-DR

CODE NO	X-LINES X								DR-LINES DR								COMMAND BITS C					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

Table 1. Command Matrix X-DR (Continued)

CODE NO	X-LINES X								DR-LINES DR								COMMAND BITS C					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

5

Table 2. System Matrix Z-DR

SYSTEM NO	Z-LINES Z				DR-LINES DR								SYSTEM BITS S				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

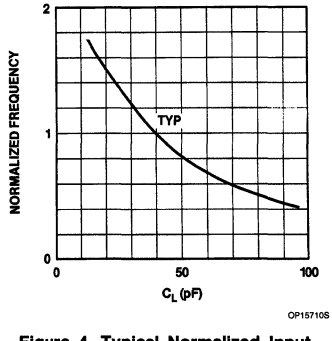


Figure 4. Typical Normalized Input Frequency as a Function of the Load (Keyboard) Capacitance

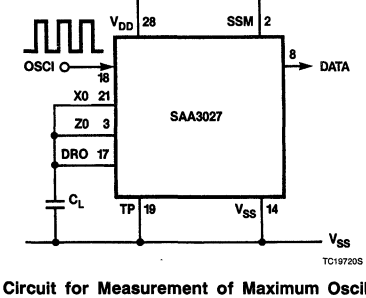


Figure 5. Test Circuit for Measurement of Maximum Oscillator Frequency

SAA3028
Infrared Receiver

Product Specification

Linear Products

DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other selectable to accept RC-5 coded signals only, or RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

FEATURES

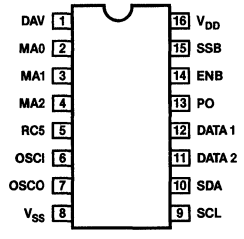
- **Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents**
- **Two data inputs: one fixed (RC-5); one selectable (RC-5/RC-5(ext))**
- **Rejects all codes not in RC-5/ RC-5(ext) format**
- **I^2C output interface capability**
- **Power-off facility**
- **Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode**
- **Power-on reset for defined start-up**

APPLICATION

- **Remote control systems**

PIN CONFIGURATION

N Package



TOP VIEW

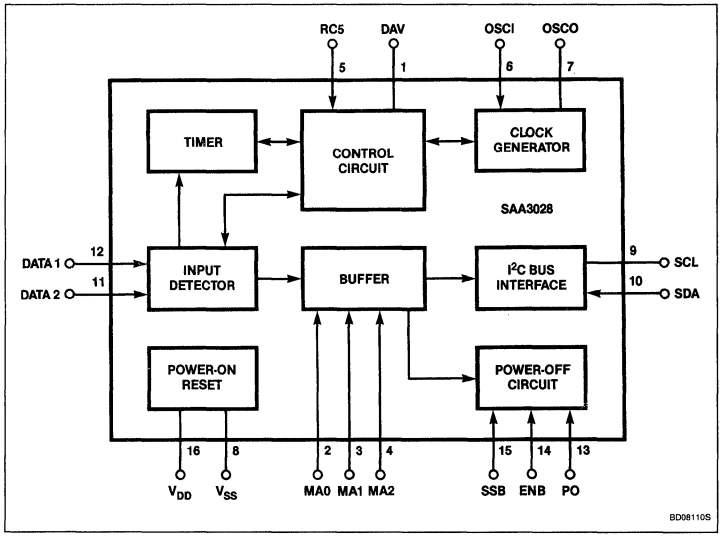
CD12040S

PIN NO.	SYMBOL	DESCRIPTION
1	DAV	Data valid output with open drain N-channel transistor
2	MA0	Master address inputs
3	MA1	Master address inputs
4	MA2	Master address inputs
5	RC5	Data 2 input select
6	OSCI	Oscillator input
7	OSCO	Oscillator output
8	V_{SS}	Negative supply (ground)
9	SCL	Serial clock line (I^2C bus)
10	SDA	Serial data line (I^2C bus)
11	DATA 2	Data 2 input
12	DATA 1	Data 1 input
13	PO	Power-off signal output with open drain N-channel transistor
14	ENB	Enable input
15	SSB	Set standby input
16	V_{DD}	Positive supply (+5V)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38Z)	−25°C to 85°C	SAA3028N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range with respect to V_{SS}	−0.5 to +15	V
V_I	Input voltage range	−0.5 to (V_{DD} + 0.5)	V[1]
$\pm I_I$	Input current	10	mA
V_O	Output voltage range	−0.5 to (V_{DD} + 0.5)	V[1]
$\pm I_O$	Output current	10	mA
P_O	Power dissipation output OSCO	50	mW
P_O	Power dissipation per output (all other outputs)	100	mW
P_{TOT}	Total power dissipation per package	200	mW
T_A	Operating ambient temperature range	−25 to +85	°C
T_{STG}	Storage temperature range	−55 to +150	°C

NOTE:
1. V_{DD}+0.5 not to exceed 15V.

DC ELECTRICAL CHARACTERISTICS V_{SS}=0V; T_A = −25°C to 85°C, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5		5.5	V
I_{DD}	Supply current; quiescent at T_A = 25°C	5.5			200	μA
Inputs MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
V_{IH}	Input voltage HIGH	4.5 to 5.5	0.7 × V_{DD}		V_{DD}	V
V_{IL}	Input voltage LOW	4.5 to 5.5	0		0.3 × V_{DD}	V
I_I	Input leakage current at V_I = 5.5V; T_A = 25°C	5.5			1	μA
$-I_I$	Input leakage current at V_I = 0V; T_A = 25°C	5.5			1	μA
Outputs DAV, PO						
V_{OL}	Output voltage LOW at I_{OL} = 1.6mA	4.5 to 5.5			0.4	V
I_{OR}	Output leakage current at V_O = 5.5V; T_A = 25°C	5.5			1	μA
OSCO						
V_{OH}	Output voltage HIGH at $-I_{OH}$ = 0.2mA	4.5 to 5.5	V_{DD} − 0.5			V
V_{OL}	Output voltage LOW at I_{OL} = 0.3mA	4.5 to 5.5			0.4	V
	Output leakage current at T_A = 25°C;					
I_{OR}	V_O = 5.5V	5.5			1	μA
I_{OR}	V_O = 0V	5.5			1	μA
SDO						
V_{OL}	Output voltage LOW at I_{OL} = 2mA	4.5 to 5.5			0.4	V
I_{OR}	Output leakage current at V_O = 5.5V; T_A = 25°C	5.5			1	μA
Oscillator						
f_{OSCI}	Maximum oscillator frequency (Figure 6)	4.75	500			kHz

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

FUNCTIONAL DESCRIPTION

Input Function

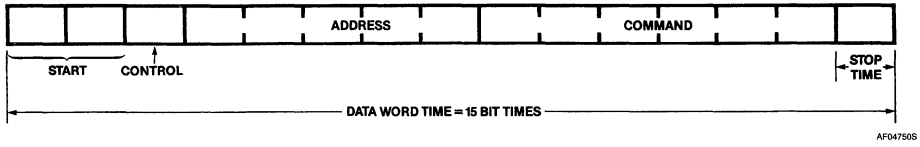
The two data inputs are accepted into the buffer as follows:

DATA 1: Only biphase coded signals which conform to the RC-5 format are accepted at this input.

DATA 2: This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

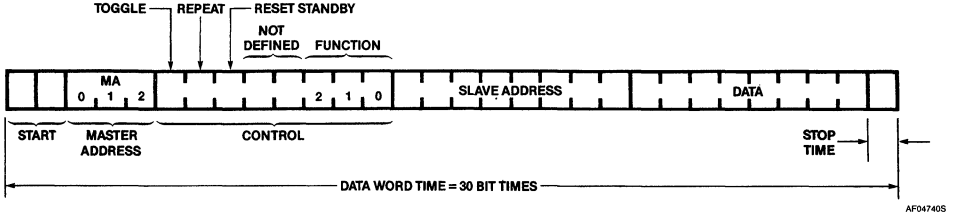
The input detector selects the input, DATA 1 or DATA 2, in which a HIGH-to-LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figures 1 and 2, respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Figure 3.



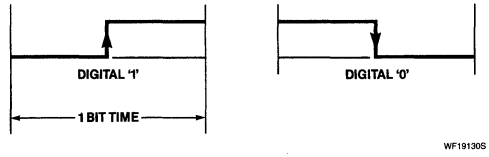
NOTE:
Stop time = 1.5 bit-times (nominal).

Figure 1. RC-5 Code Format: the First Start Bit is Used Only for Detection and Input Gain-Setting



NOTE:
Stop time = 1.5 bit-times (nominal).

Figure 2. RC-5 (extended) Code Format: the First Start Bit is Used Only for Detection and Input Gain-Setting



NOTE:
RC-5 bit-time = $2^7 \times t_{OSC}$ = 1.778ms (typical), RC-5(ext) bit-time = $2^6 \times t_{OSC}$ = 0.89ms (typical), where t_{OSC} = the oscillator period time.

Figure 3. Biphase Code Definition

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as shown in the table.

RC-5 BUFFER CONTENTS		RC-5(EXT) BUFFER CONTENTS	
• Data valid indicator	1 Bit	• Data valid indicator	1 Bit
• Format indicator	1 Bit	• Format indicator	1 Bit
• Input indicator	1 Bit	• Input indicator	1 Bit
• Control	1 Bit	• Master address	3 Bits
• Address data	5 Bits	• Control	8 Bits
• Command data	6 Bits	• Slave address	8 Bits
		• Data	8 Bits

The information assembled in the buffer is subjected to the following controls before being made available at the I_2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:
RC-5: When the binary equivalent value is transferred to the buffer.
RC-5(ext): When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.
At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output Function

The data is assembled in the buffer in the format shown in Figure 4 for RC-5 binary equivalent values, or in the format shown in Figure 5 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figures 4 and 5.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

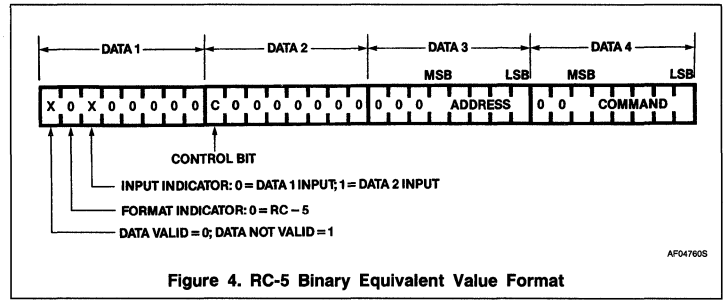


Figure 4. RC-5 Binary Equivalent Value Format

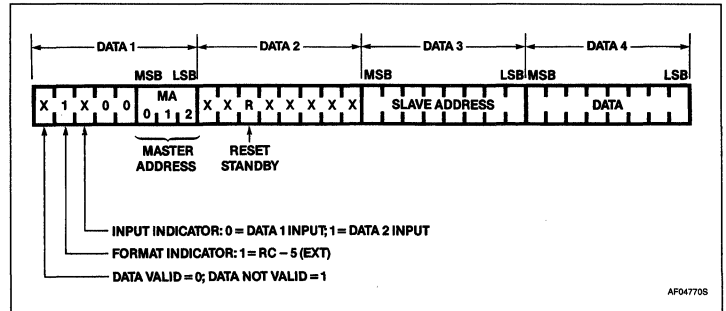
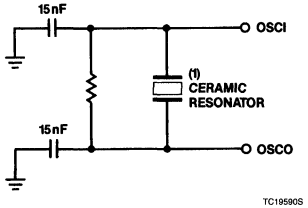


Figure 5. RC-5(ext) Binary Equivalent Value Format

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Figure 6. The typical frequency of oscillation is 455kHz.



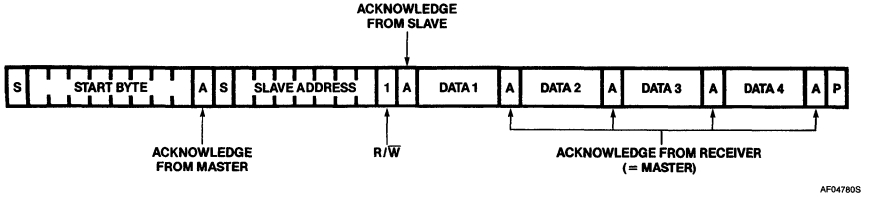
NOTE:
(1) Catalog number of ceramic resonator: 2422 540 98008.

Figure 6. Oscillator Circuit

FUNCTIONAL DESCRIPTION

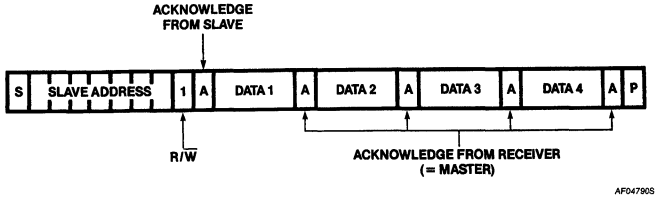
I²C Bus Transmission

Formats for I²C transmission in low-and high-speed modes are shown respectively in Figures 7 and 8.



NOTES:
When R/$\overline{W}$ bit = 0, the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.
When the receiver generates a NACK, the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).
When all data has been transmitted, the data line remains HIGH and the slave waits for P.

Figure 7. Format for Transmission in I²C Low-Speed Mode



NOTES:
When R/$\overline{W}$ bit = 0, the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.
When the receiver generates a NACK, the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).
When all data has been transmitted, the data line remains HIGH and the slave waits for P.

Figure 8. Format for Transmission in I²C High-Speed Mode

Signetics

TDA3047
IR Preamplifier

Product Specification

Linear Products

DESCRIPTION

The TDA3047 is for infrared reception with low power consumption.

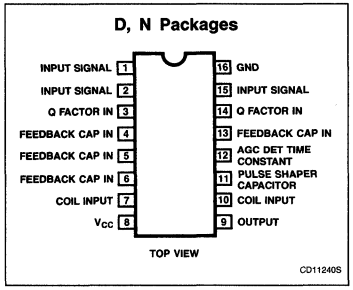
FEATURES

- **HF amplifier with a control range of 66dB**
- **Synchronous demodulator and reference amplifier**
- **AGC detector**
- **Pulse shaper**
- **Q-factor killing of the input selectivity, which is controlled by the AGC circuit**
- **Input voltage limiter**

APPLICATION

- **IR remote control systems**

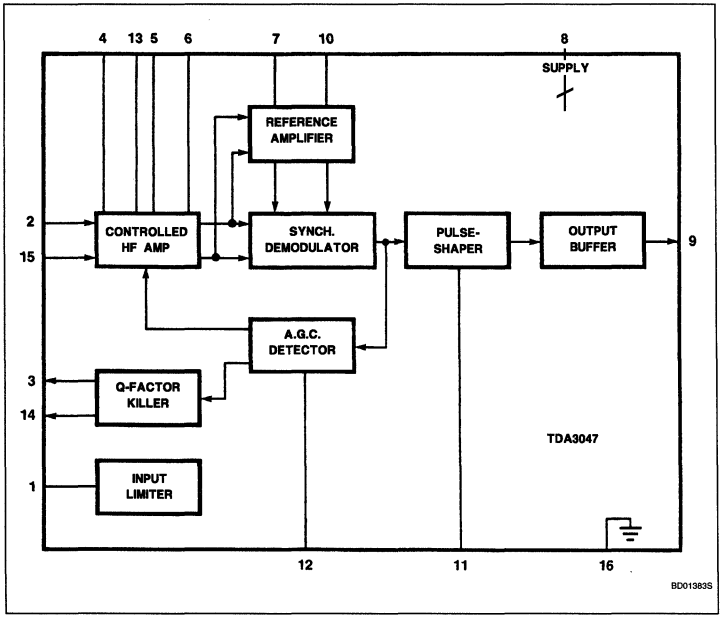
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−25°C to +125°C	TDA3047N
16-Pin Plastic SO (SOT-109A)	0 to +70°C	TDA3047TD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 8)	13.2	V
I_{11}	Output current pulse shaper (Pin 11)	10	mA
	Voltages between pins[1]		
V_{2-15}	Pins 2 and 15	4.5	V
V_{4-13}	Pins 4 and 13	4.5	V
V_{5-6}	Pins 5 and 6	4.5	V
V_{7-10}	Pins 7 and 10	4.5	V
V_{9-11}	Pins 9 and 11	4.5	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +125	°C

NOTE:
1. All pins except Pin 11 are short-circuit protected.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = V_8 = 5V$; $T_A = 25°C$, measured in Figure 3, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 8)					
V_{CC}	Supply voltage	4.65	5.0	5.35	V
$I_{CC} = I_8$	Supply current	1.2	2.1	3.0	mA
Controlled HF amplifier (Pins 2 and 15)					
	Minimum input signal (peak-to-peak value)				
$V_{2-15(P-P)}$	at f = 36kHz[1]		15	25	μV
$V_{2-15(P-P)}$	at f = 36kHz[2]			5	μV
	AGC control range (without Q-killing)	60	66		dB
$V_{2-15(P-P)}$	Input signal for correct operation (peak-to-peak value)[3]	0.02		200	mV
$V_{2-15(P-P)}$	Q-killing inactive ($I_3 = I_{14} < 0.5\mu A$) peak-to-peak value)			140	μV
$V_{2-15(P-P)}$	Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	28			mV
	Q-killing range		Figure 1		
Inputs					
V_2	Input voltage (Pin 2)	2.25	2.45	2.65	V
V_{15}	Input voltage (Pin 15)	2.25	2.45	2.65	V
R_{2-15}	Input resistance (Pin 2)	10	15	20	kΩ
C_{2-15}	Input capacitance (Pin 2)		3		pF
V_{1-16}	Input limiting (Pin 1) at I_1 = 3mA		0.8	0.9	V
Outputs					
$-V_{9-8}$	Output voltage HIGH (Pin 9) at $-I_9 = 75\mu A$		0.1	0.5	V
V_9	Output voltage LOW (Pin 9) at $I_9 = 75\mu A$		0.1	0.5	V
	Output current; output voltage HIGH				
$-I_9$	at V_9 = 4.5V	75	120		μA
$-I_9$	at V_9 = 3.0V	75	130		μA
$-I_9$	at V_9 = 1.0V	75	140		μA
I_9	Output current; output voltage LOW at V_9 = 0.5V	75	120		μA
R_{7-10}	Output resistance between Pins 7 and 10	3.1	4.7	6.2	kΩ

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_8 = 5V$; $T_A = 25°C$, measured in Figure 3, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Pulse shaper (Pin 11)					
V_{11}	Trigger level in positive direction (voltage Pin 9 changes from HIGH to LOW)	3.75	3.9	4.05	V
V_{11}	Trigger level in negative direction (voltage Pin 9 changes from LOW to HIGH)	3.4	3.55	3.7	V
ΔV_{11}	Hysteresis of trigger levels	0.25	0.35	0.45	V
AGC detector (Pin 12)					
$-I_{12}$	AGC capacitor charge current	3.3	4.7	6.1	μA
I_{12}	AGC capacitor discharge current	67	100	133	μA
Q-factor killer (Pins 3 and 14)					
$-I_3$	Output current (Pin 3) at $V_{12-16} = 2V$	2.5	7.5	15	μA
$-I_{14}$	Output current (Pin 14) at $V_{12-16} = 2V$	2.5	7.5	15	μA

NOTES:
1. Voltage Pin 9 is HIGH; $-I_9 = 75\mu A$.
2. Voltage Pin 9 remains LOW.
3. Undistorted output pulse with 100% AM input.

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5V supply and has a current consumption of 2mA. The output is a current source which can drive or suppress current of $> 75\mu A$ with a voltage swing of 4.5V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600mV by an input limiter. The typical input is an AM signal at a frequency of 36kHz. Figures 2 and 3 show the circuit diagrams for the application of narrow-band and wide-band receivers, respectively. Circuit description of the eight sections shown in the Block Diagram are given below.

Controlled HF Amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three DC amplifier stages connected in cascade. The overall gain of the circuit is approximately 83dB and the gain control range is in the order of 66dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the DC coupled amplifier are minimized by two negative feedback loops. These also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference Amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous Demodulator

In the synchronous demodulator, the input signal and reference signal are multiplied. The demodulator output current is $25\mu A$ peak-to-peak. The output signal of the demodulator is fed to the input of the AGC detector and to the input of the pulse-shaper circuit.

AGC Detector

The AGC detector comprises two NPN transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the AGC circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-Shaper

The pulse-shaper comprises two NPN transistors operating as a differential pair connected in parallel with the AGC differential pair. The slicing level of the pulse shaper is lower than the slicing level of the AGC detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to Pin 11 which is applied directly to the output buffer.

Output Buffer

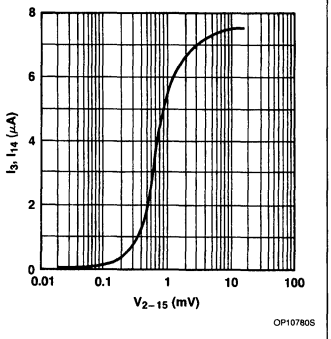
The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at Pin 9 is active HIGH.

Q-factor Killer

Figure 2 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at Pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; Pin 3 to Pin 2, and Pin 14 to Pin 15.

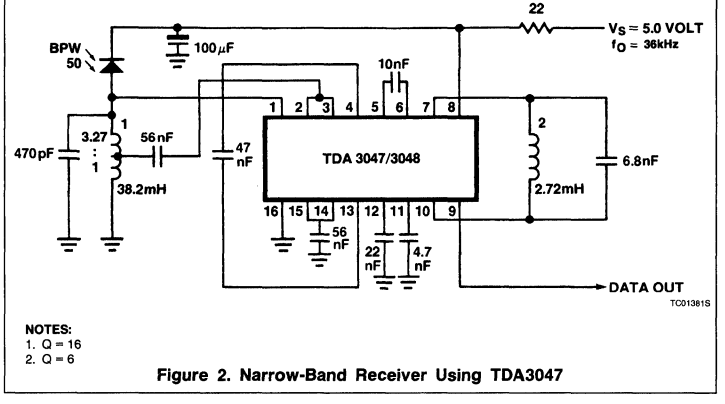
Input Limiter

In the narrow-band application, high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0.7V. Limiting is 0.9V maximum at $I_1 = 3mA$.



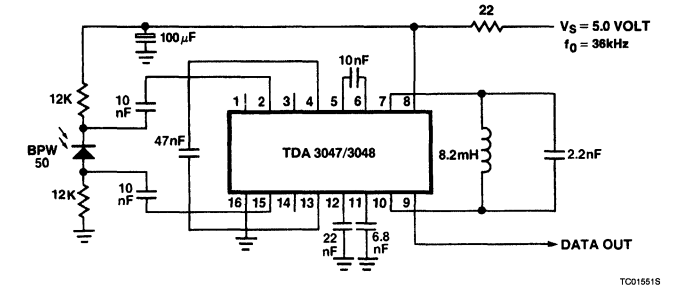
NOTE:
$I_{3,\ 14}$ is measured to ground, $V_{2\text{-}15(P\text{-}P)}$ is a symmetrical square wave. Measured in Figure 3; V_{CC} = 5V.

Figure 1. Typical Q-Factor Killer Current (Pins 3 and 14) as a Function of the Peak-to-Peak Input Voltage (V_2-15)



NOTES:
1. Q = 16
2. Q = 6

Figure 2. Narrow-Band Receiver Using TDA3047



NOTE:
For better sensitivity, both 12kΩ resistors may have a higher value.

Figure 3. Wide-Band Receiver With TDA3047

Signetics

TDA3048
IR Preamplifier

Product Specification

Linear Products

DESCRIPTION

The TDA3048 is for infrared reception with low power consumption.

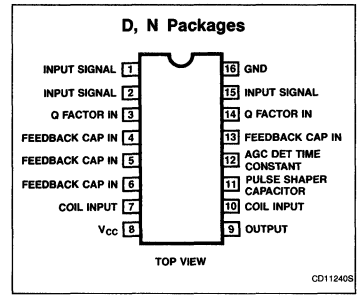
FEATURES

- **HF amplifier with a control range of 66dB**
- **Synchronous demodulator and reference amplifier**
- **AGC detector**
- **Pulse shaper**
- **Q-factor killing of the input selectivity, which is controlled by the AGC circuit**
- **Input voltage limiter**

APPLICATION

- **IR Remote control systems**

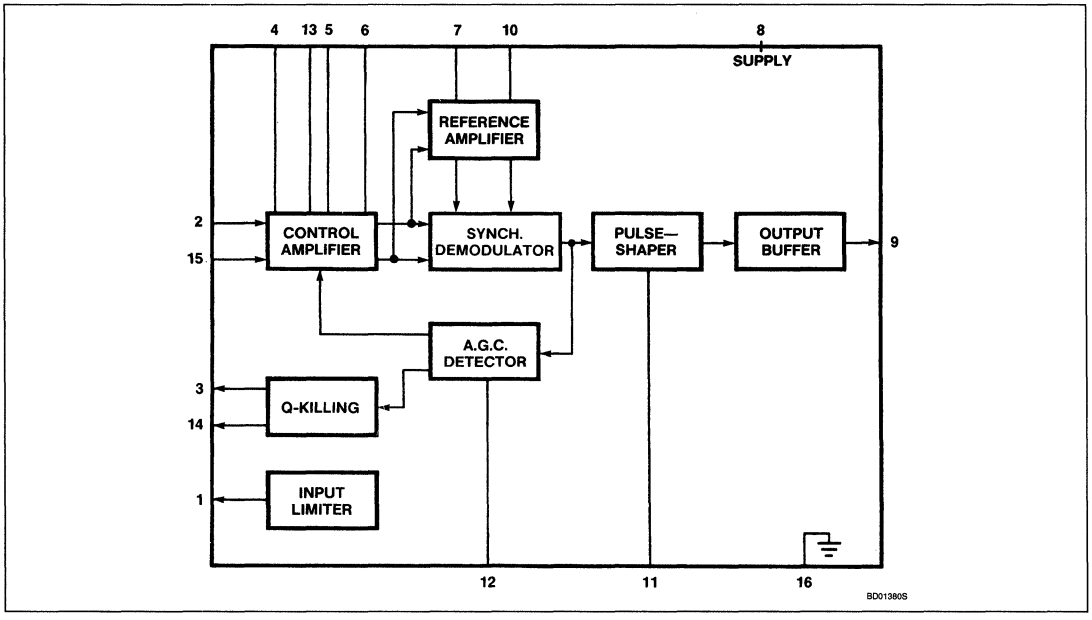
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−25°C to +125°C	TDA3048N
16-Pin Plastic SO (SOT-109A)	0 to +70°C	TDA3048TD

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5V supply and has a current consumption of 2mA. The output is a current source which can drive or suppress a current of $> 75\mu A$ with a voltage swing of 4.5V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of $> 600mV$ by an input limiter. The typical input is an AM signal at a frequency of 36kHz. Figures 2 and 3 show the circuit diagrams for the application of narrow-band and wide-band receivers, respectively. Circuit description of the eight sections shown in the Block Diagram are given below.

Controlled HF Amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three DC amplifier stages connected in cascade. The overall gain of the circuit is approximately 83dB and the gain control range is in the order of 66dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the DC coupled amplifier are minimized by two negative feedback loops. These also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference Amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous Demodulator

In the synchronous demodulator, the input signal and reference signal are multiplied. The demodulator output current is $25\mu A$ peak-to-peak. The output signal of the demodulator is fed to the input of the AGC detector and to the input of the pulse-shaper circuit.

AGC Detector

The AGC detector comprises two NPN transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the AGC circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-Shaper

The pulse-shaper comprises two NPN transistors operating as a differential pair connected in parallel with the AGC differential pair. The slicing level of the pulse shaper is lower than the slicing level of the AGC detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to Pin 11, which is applied directly to the output buffer.

Output Buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at Pin 9 is active LOW.

Q-Factor Killer

Figure 2 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at Pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; Pin 3 to Pin 2 and Pin 14 to Pin 15.

Input Limiter

In the narrow-band application, high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0.7V. Limiting is 0.9V max. at $I_1 = 3mA$.

ABSOLUTE MAXIMUM RATINGS

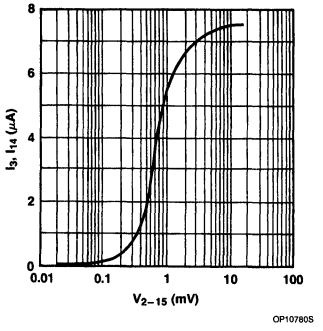
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 8)	13.2	V
I_{11}	Output current pulse shaper (Pin 11)	10	mA
	Voltages between pins[1]		
V_{2-15}	Pins 2 and 15	4.5	V
V_{4-13}	Pins 4 and 13	4.5	V
V_{5-6}	Pins 5 and 6	4.5	V
V_{7-10}	Pins 7 and 10	4.5	V
V_{9-11}	Pins 9 and 11	4.5	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +125	°C

NOTE:
1. All pins except Pin 11 are short-circuit protected.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = V_8 = 5V$; $T_A = 25°C$; measured in Figure 3, unless otherwise specified.

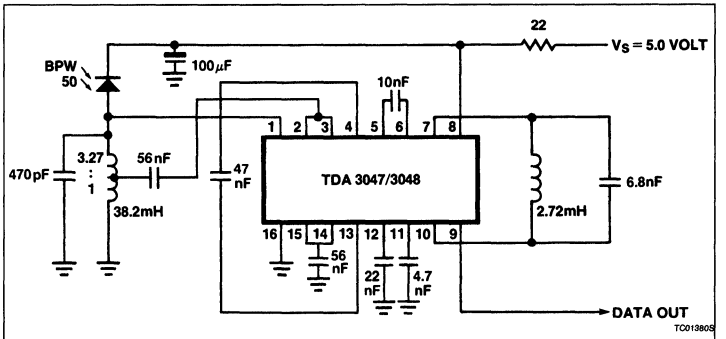
SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 8)					
V_{CC}	Supply voltage	4.65	5.0	5.35	V
I_{CC}	Supply current	1.2	2.1	3.0	mA
Controlled HF amplifier (Pins 2 and 15)					
V_{2-15} V_{2-15}	Minimum input signal (peak-to-peak value) at f = 36kHz[1] at f = 36kHz[2]		15	25 5	μV μV
	AGC control range (without Q-killing)	60	66		dB
V_{2-15}	Input signal for correct operation (peak-to-peak value)[3]	0.02		200	mV
V_{2-15}	Q-killing inactive ($I_3 = I_{14} < 0.5\mu A$) (peak-to-peak value)			140	μV
V_{2-15}	Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak) value	28			mV
	Q-killing range	See Figure 1			
Inputs					
V_2	Input voltage (Pin 2)	2.25	2.45	2.65	V
V_{15}	Input voltage (Pin 15)	2.25	2.45	2.65	V
R_{2-15}	Input resistance (Pin 2)	10	15	20	kΩ
C_{2-15}	Input capacitance (Pin 2)		3		pF
V_{1-16}	Input limiting (Pin 1) at $I_1 = 3mA$		0.8	0.9	V
Outputs					
$-V_{9-8}$	Output voltage HIGH (Pin 9) at $-I_9 = 75\mu A$		0.1	0.5	V
V_9	Output voltage LOW (Pin 9) at $I_9 = 75\mu A$		0.1	0.5	V
I_9 I_9 I_9	Output current; output voltage LOW $-V_{9-8} = 4.5V$ $-V_{9-8} = 3.0V$ $-V_{9-8} = 1.0V$	 75 75 75	 120 130 140		 μA μA μA
$-I_9$	Output current; output voltage HIGH $-V_{9-8} = 0.5V$	 75	 120		 μA
R_{7-10}	Output resistance between Pins 7 and 10	3.1	4.7	6.2	kΩ
Pulse shaper (Pin 11)					
V_{11}	Trigger level in positive direction (voltage Pin 9 changes from HIGH to LOW)	3.75	3.9	4.05	V
V_{11}	Trigger level in negative direction (voltage Pin 9 changes from LOW to HIGH)	3.4	3.55	3.7	V
ΔV_{11}	Hysteresis of trigger levels	0.25	0.35	0.45	V
AGC detector (Pin 12)					
$-I_{12}$	AGC capacitor charge current	3.3	4.7	6.1	μA
I_{12}	AGC capacitor discharge current	67	100	133	μA
Q-factor killer (Pins 3 and 14)					
$-I_3$	Output current (Pin 3) at $V_{12} = 2V$	2.5	7.5	15	μA
$-I_{14}$	Output current (Pin 14) at $V_{12} = 2V$	2.5	7.5	15	μA

NOTES:
1. Voltage Pin 9 is LOW; $I_9 = 75\mu A$.
2. Voltage Pin 9 remains HIGH.
3. Undistorted output pulse with 100% AM input.



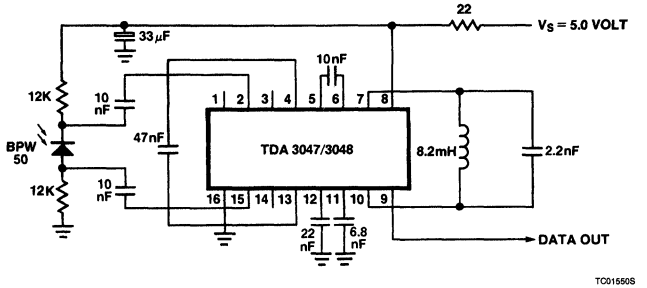
NOTE:
$I_{3,\ 14}$ is measured to ground, $V_{2-15(P-P)}$ is a symmetrical square wave measured in Figure 3; V_{CC} = 5V.

Figure 1. Typical Q-Factor Killer Current (Pins 3 and 14) as a Function of the Peak-to-Peak Input Voltage



NOTE:
N1 = 3.21
N2 = 1
Q = 16

Figure 2. Narrow-Band Receiver Using TDA3048



NOTE:
For better sensitivity both 12kΩ resistors may have a higher value.

Figure 3. Wide-Band Receiver With TDA3048

Signetics

AN172
Circuit Description of the Infrared Receiver TDA3047/ TDA3048

Linear Products

Application Note

Author: A.J.E. Bretveld

INTRODUCTION

As a successor of the current integrated circuits TCA440 and NE555 for receiving infrared remote-controlled signals, a new integrated circuit has been developed.

In comparison with the TCA440-NE555 combination, this IC is aimed to have a higher replacement value and improved performance. The TDA3048 is equal to the TDA3047 except for the polarity of the output signal.

GENERAL DESIGN CONSIDERATIONS

The target of this development is to make a receiver integrated circuit for infrared remote-controlled signals which functions optimally in a narrow-band application.

This integrated circuit shall have the following advantages in comparison with the present TCA440-NE555 combination:

- A higher replacement value
- A considerable saving of the current consumption
- An improvement of the specification (less spread)
- Less periphery and no adjustment points
- Total spread on pulse widening $< 10\%$ by a standard RC-5 signal.

Besides, the IC is also suitable to be used in a RC-5 extended receiver and in a wide band receiver.

A standard bipolar process with single layer interconnect and without collector wall has been used.

Due to the low currents, a collector wall is not necessary.

FUNCTIONAL DESCRIPTION OF THE BLOCK PARTS

Figure 1 shows the block diagram of the TDA3047 and TDA3048.

Amplifier

The input signal is amplified by the gain-controlled amplifier. The output signal of the amplifier is fed to the synchronous demodulator inputs and to the reference amplifier.

Reference Amplifier

The reference amplifier amplifies and limits the input signal. The output signal of this amplifier is fed to the synchronous demodulator.

Synchronous Demodulator

In the synchronous demodulator, the input signal and reference signal are multiplied. The output signal of the demodulator is fed to the input of a pulse-shaper circuit and to the input of the AGC circuit.

AGC Circuit

The output signal of the synchronous demodulator is fed to the AGC circuit. The top level of the signal is detected by the AGC detector. Noise pulses are integrated by an internal capacitor. The output signal from the AGC detector is amplified and supplied to the first and second stage of the amplifier and to the Q-killing circuit.

Pulse-shaper Circuit

The output of the synchronous demodulator is also fed to the pulse-shaper circuit. The slicing level of the pulse-shaper is lower than the slicing level of the AGC detector.

The output of the pulse-shaper is fed to the output buffer.

Output Buffer

The output buffer gives for the TDA3047 an active-high level and for the TDA3048 an active-low level on the output pin. To obtain a correct RC-5 code a hysteresis circuit protects the output against spikes.

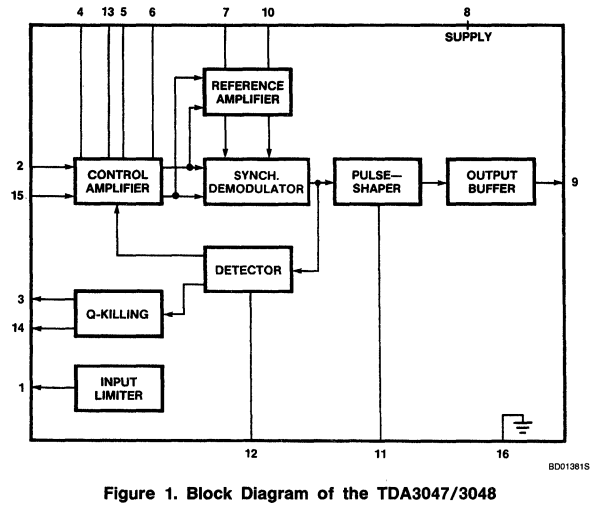


Figure 1. Block Diagram of the TDA3047/3048

Circuit Description of the Infrared Receiver TDA3047/TDA3048 AN172

Q-Killing Circuit

In the narrow-band application it is necessary to degenerate the Q of the input selectivity particularly when large signals occur at the input.

The output of the Q-killing circuit can be directly coupled to the input.

Input Voltage Limiter

In the narrow-band application high voltage peaks can occur on the input selectivity. The input limiter limits these voltage peaks to about 0.7V.

APPLICATION

The narrow-band application diagram has been given in Figure 2 and a lower performance wide-band application diagram in Figure 3.

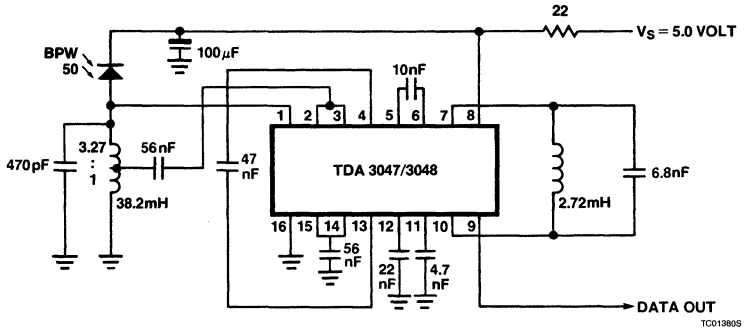


Figure 2. Narrow-Band Application Diagram of the TDA3047/3048

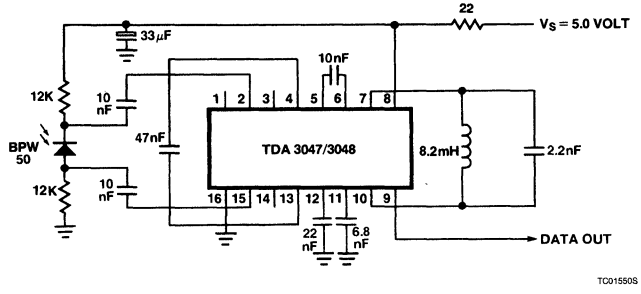


Figure 3. Wide-Band Application Diagram of the TDA 3047/3048

Signetics

AN173
Low Power Preamplifiers for IR Remote Control Systems

Application Note

Linear Products

INTRODUCTION

The monolithic integrated bipolar circuits TDA3047 and TDA3048 are amplifiers intended for use in infrared remote control systems. Both circuits are excellent and applicable as narrow-band amplifiers, especially for those types of remote control concepts which use the modulated transmission technique. Under certain conditions both ICs are also applicable as broadband amplifiers. The only difference between the ICs is polarity of the output signal. This type of IR amplifier offers the following advantages:

- Low power consumption, typically 10.5mV
- Gain-controlled amplification, control range 66dB
- High amplification factor, > 80dB, ensures a long range
- Great stability in signal handling
- Demodulation via a synchronous demodulator
- Automatic limitation of large input signals, 600mV
- Independent of large input amplitude variations with a Q-killer
- Applicable as narrow-or broadband amplifier

This circuit proves to be a reliable device with regard to interference from other IR sources such as light bulbs, etc.

The automatic gain control (AGC) ensures very good stability in amplification of large or low input signals, which correspond to short or long distances from transmitter to receiver.

FUNCTIONAL DESCRIPTION

The functional block diagram is shown in Figure 1. The input signal is applied to the gain-controlled multi-stage differential preamplifier, capacitively-coupled via C_2 and C_3. The capacitors C_4 and C_5 stabilize the differential preamplifier. Hereafter the signal is fed to a synchronous demodulator and the reference amplifier, which limits the input signal. After multiplication of the input and reference signal by the demodulator, the signal is applied to a pulse-shaper, whose time constant is controlled by C_8. The same signal is also used for the feedback loop, resulting in an automatic gain control defined by the amplitude of the input signal. The AGC acquisition time is set by C_7. The Q-killer limits the amplification of the tuned input circuit in conjunction with input amplitude. In this way the behavior of this device on large amplitude variations ensures a great stability in the signal handling. A maximum input limitation is achieved via the amplitude limiter, typically activated by a 600mV input signal.

The differential preamplifier has, in principle, two stages, as shown in Figure 2. Each stage is stabilized via an external feedback capacitor. Both define the lower boundary of the frequency, with the greatest influence from C_4 because stage 1 has the highest gain. Both capacitors should be specified so that interference from low frequencies is suppressed. For instance, bulbs radiate infrared frequencies at (n)(100Hz).

The highest boundary in frequency of this amplifier is greater than 1MHz and is given by the internal capacitance of this device.

IR AMPLIFIER

For remote control systems two different types of amplifiers are available. Both are described in the following sections.

Narrow-Band Amplifier

The diagram of Figure 3 shows the TDA3047/48 in such an application. Pin 15, one of the differential inputs, is grounded for AC, while the second input, Pin 2, is connect-

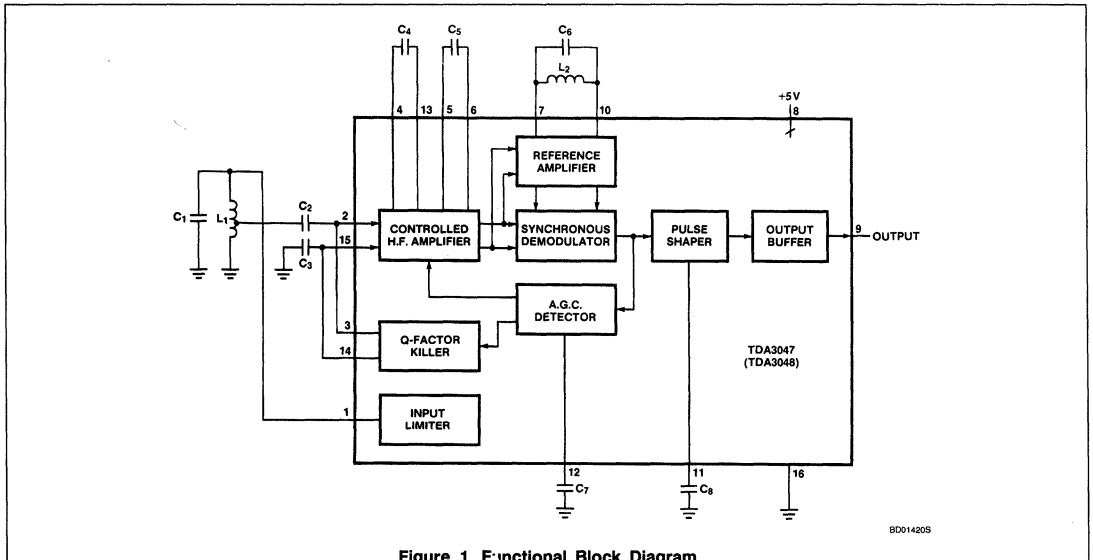


Figure 1. Functional Block Diagram

Low Power Preamplifiers for IR Remote Control Systems AN173

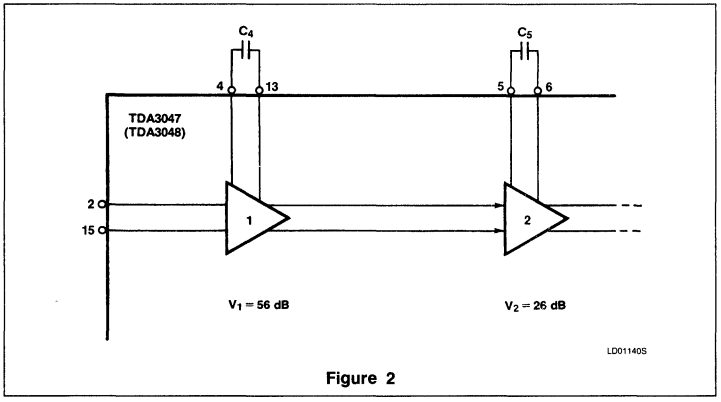


Figure 2

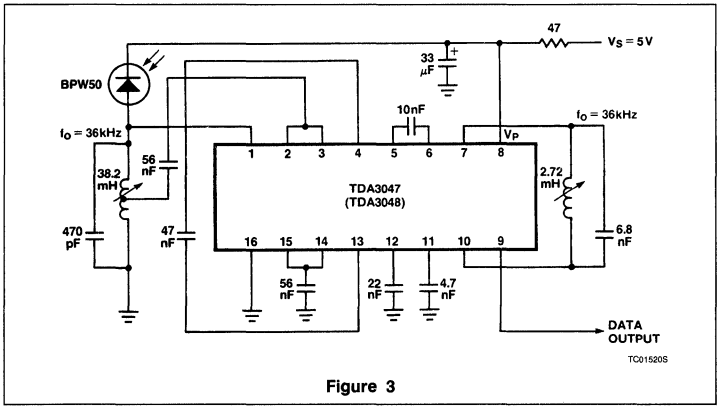


Figure 3

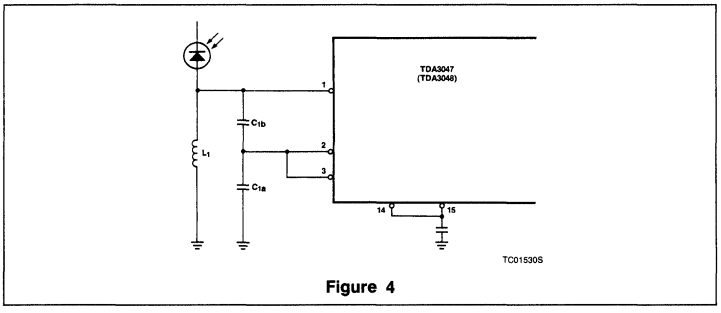


Figure 4

ed to the tuned input circuit via a capacitor of 0.056µF. The input voltage is taken with a transformer ratio N = 1:3. Direct coupling to the top will only lower the quality Q factor of the tuned input circuit, due to the relatively low input resistor, R_{IN}, of the IC.

The selectivity is obtained with the tuned input circuit and strongly reduces IR interferences. The effect of direct IR radiation is also avoided. Due to the low ohmic resistance of the coil, the IR receiving diode will never become saturated. The center frequency of the input tank must be equal to the modulation frequency of the transmitter used.

For this frequency (f_O) the input tank has a high impedance. Small variations of the current of the IR receiving diode at f_O result directly in large input signals.

This frequency (f_O) is equal to 37.5kHz for the SAA3004 transmitting chip. The RC combination of 47Ω and 0.33µF suppresses the unwanted current variations caused by the supply line.

The Q of the tuned input circuit is practically defined by the transformer ratio and the input resistor R_{IN} of the IC. The effect of R_{IN} to the quality Q_1 of the coil is negligible, because R_{IN} is relatively low (typically 16kΩ).

The transformer ratio must be adjusted for small signals, so that the range is hardly influenced by component spread and/or tolerances in frequency at both sides in the system. The Q can be calculated from:

$$Q = \frac{1}{R_{L1}\sqrt{\frac{C_1}{L_1}} + \frac{1}{R_P}\sqrt{\frac{L_1}{C_1}}}$$

where R_{L1} is the ohmic resistance of the coil and the parallel resistor $R_P = n^2 R_{IN1}$.

With the component values shown in Figure 3 and a given $R_{L1} = 125\Omega$, $R_{IN} = 16k\Omega$, the factor Q is calculated as Q = 13. The bandwidth is now known from

$$\Delta f = \frac{f_O}{Q} = 2.9kHz$$

The transformer ratio can also be realized with two capacitors in series, as shown in Figure 4, where the total capacity is equal to the required one.

$$\text{The ratio is } n = \frac{C_{1a} + C_{1b}}{C_{1b}}$$

With values of C_{1a} = 2.2nF, C_{1b} = 560pF and L_1 = 40mH, about the same input quality will be obtained.

The AGC acquisition time and the time constant of the pulse-shaper are defined by the capacitors C_7 and C_8, respectively. The time constant at Pin 12 equals the length of a received data bit and C_8 delays the pulse-shaper output to the output stage.

The Q_S of the tuned circuit of the synchronous demodulator is practically given by the internal resistance, R_{IN2}, between Pins 7 and 10 and is calculated from

$$Q_s = \frac{1}{R_{L2}\sqrt{\frac{C_6}{L_2}} + \frac{1}{R_{In2}}\sqrt{\frac{L_2}{C_6}}}$$

with 12Ω for R_{L2} and 5kΩ for R_{IN}, $Q_S \simeq 7$. The quality Q_S is continuously limited. With a relatively high value for Q_S, the acquisition time will be increased and this will delay the pulse edges. By amplification of "biphase" modulated signals, disturbances could occur in the decoding. For correct decoding of

Low Power Preamplifiers for IR Remote Control Systems AN173

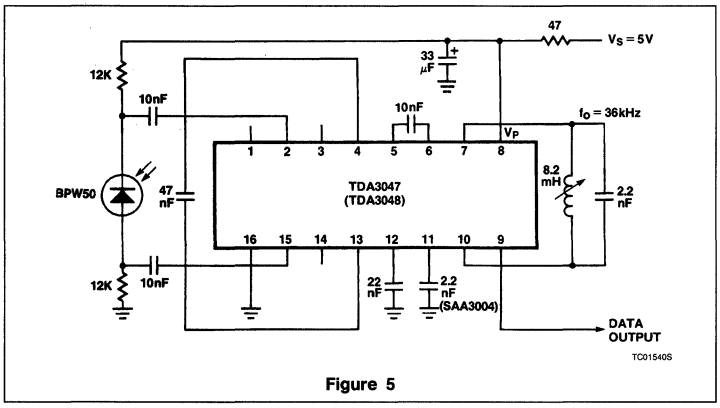


Figure 5

"biphase" coded data, a nearly exact position of the pulse edges is required.

Broadband Amplifier

The application as broadband amplifier is shown in Figure 5. The IR receiving diode is now positioned between both differential inputs, while the series resistors of 12kΩ are the work resistors. The Q killer and Amplitude Limiter do not have any function here and are not used. Also the resonance frequency, f_O, of the tuned demodulator circuit equals the modulation frequency of the remote transmitter.

The charge current to capacitor C_8 is equal to

$$I_{C8} = (C_8)\frac{\Delta V_{C8}}{\Delta t}$$

where Δt is the charge time and ΔV_{C8} is the voltage increment. IC_8 is generated by an internal current source.

The voltage increment at C_8 is proportional to Δt, with IC_8 constant and expressed as

$$\Delta V_{C8} = \frac{(I_{C8})(\Delta t)}{C_8}$$

The pulse width, Δt, of the demodulated signal must be large enough that VC_8 exceeds the threshold voltage of the pulse-shaper.

Given the format of the received data, C_8 will have different values

	Pulse Width	C_8
SAA3004	8.8µs	2.2nF

A 2.2nF capacitor in the SAA3004 remote control system is an optimum one.

The SAA3004, used in unmodulated mode, has a pulse width of 8.8µs. C_8 must have a low value so that the threshold voltage of the pulse-shaper is exceeded. On the other hand, if C_8 becomes too small, interference pulses will easily trigger the pulse-shaper. The selection of C_8 is a compromise between the sensitivity of the amplifier and the immunity against interference. Such a compromise is a 2.2nF capacitor for the unmodulated mode of the SAA3004, including the tolerances of the internal current sources. Given the technology, small tolerances are not possible.

Correct operation can not be guaranteed for the combination of a small pulse width (8.8µs) and a low source current. However, practical tests did show that correct operation of the SAA3004, in the unmodulated mode in combination with this type of preamplifier, can be realized.

CONSIDERATIONS FOR AMPLIFIER SELECTION

The narrow- or broadband application is defined by the following points:

- Modulation mode of the transmitter
- Requirements for the reach in distance
- Reliability (insensitivity to interference)
- Price-attractive total remote control system

Either modulated or unmodulated data transmission is possible with the SAA3004.

In the unmodulated mode, the logic representation of the data word is defined by the time intervals between the generated output pulses, each of 8.8µs width. In the modulated output mode, each active output stage has a burst of 6 clock periods.

The ground wave of this output, with a frequency of 38kHz, contains the IR power generated.

The greatest sensitivity is realized with a narrow-band amplifier, whose tuned input circuit is selected for this ground wave frequency.

In the unmodulated transmission mode, the single output pulse represents a continuous frequency spectrum, in which the generated IR power is divided. A broadband amplifier is then required.

The greatest range, with constant-current through the IR transmission diode(s), will be obtained with a narrow-band amplifier, because the signal-to-noise ratio is the largest value.

When IR interference is absent, the combination of modulated transmission mode and the narrow-band amplifier is the most preferable. With lower requirements for the reliability, less range, etc., the broadband amplifier is the most effective solution for both types of modulation modes.

RANGE

To give some idea what range can be expected, a number of measurements are made with the remote transmitters SAA3004.

With Various IR Output Powers

Transmitter SAA3004 drives 1 IR-transmitting diode with a peak current IC≅2A. In the modulated mode, the power product per bit equals

(m) (I_F) (n) (t_P)

where m = number of diodes, n = number of pulses per bit, and t_P = pulse width.

The power product for each bit is:

- Modulated mode (m) (I_F) (n) (t_P) = (1) (2) (6) (8.8) = 106µA/sec
- Unmodulated mode (m) (I_F) (n) (t_P) = (1) (2) (1) (8.8) = 18µA/sec

This power product is proportional to the generated IR power. Table 1 indicates the results of the measurements. Optic lenses will increase the distances about 10%.

With Equal Output Power

These measurements are done with one transmitting diode for each transmitter type

Low Power Preamplifiers for IR Remote Control Systems AN173

Table 1. Distance Reach With Various Power Products

	SAA3004	
	Modulated	**Unmodulated**
Power product	106μA/sec	18μA/sec
Narrow-band C_8 = 4.7nF	25mt	11mt
Broadband C_8 = 2.2nF	16mt	12mt

Table 2. Distance Reach With Constant Power Product of 18μA/sec

	SAA3004	
	Modulated	**Unmodulated**
Narrow-band C_8 = 4.7nF	11mt	11mt
Broadband C_8 = 2.2nF	8mt	12mt

Table 3. Application Possibilities

	SAA3004	
	Unmodulated	**Modulated**
Narrow-band	No sense; no selectivity	Great distance reach, high selectivity, reliable
Broadband	Function only possible with small width output pulse; less reliable	Low reach, low selectivity; interference.

and the power product/bit constant at 18μA/sec. Table 2 is comprised of the results from these measurements.

Results of the Measurements

The results of the measurements can be summarized as follows:

a. Only the combinations "modulated and narrow-band amplifier" are reasonable.

b. With the peak current I_F through one IR-transmitting diode, the range with one IR diode is limited.

c. A maximum range is obtained using the modulated mode of data transmitting, but the loss of power in the transmitter is of subordinate importance.

POWER DISSIPATION

In comparison with older types of preamplifiers, the power consumption is enormously reduced. For instance, the TDB2033 consumed 204mW at 12V supply, while the TDA3047/48 only takes 10mW at 5V supply, which is very useful for "standby" mode. A second advantage is the 5V supply which can also be used by the decoding microcomputer.

POSSIBLE APPLICATION COMBINATIONS

In Table 3, the different combinations are given for remote control systems operating in the modulated or unmodulated mode.

OUTPUT SIGNAL

As indicated in the introduction, the TDA3047 has an active-high output signal, while an active-low output is generated by the TDA3048. This choice in polarity is made available for maximum cooperation with the decoding part. If, for example, an 8048 microcomputer is used on interrupt level, with active-low at input $\overline{INT}$, the TDA3048 is then the correct amplifier. If the $\overline{INT}$ input is active-High, the TDA3047 outputs the proper high level.

PC BOARD DESIGN

Special attention must be given to the placement of C_5. The greatest distance must be realized between the position of this capacitor and the inputs 2 and/or 15. Ground connections and screening must also be done with great accuracy.

Signetics

Linear Products

Section 6
Television Subsystems

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Signetics

TDA4501

Small-Signal Subsystem IC for Color TV

Product Specification

Linear Products

DESCRIPTION

The integration into a single package of all small-signal functions (except the tuner) required for color TV reception is achieved in the TDA4501. The only additional circuits needed to complete the receiver are a tuner, the deflection output stages, and a color decoder. The TDA3563 or 67, NTSC color decoder, and TDA3653, vertical output, are ideal complements for the TDA4501.

The IC includes a vision IF amplifier with synchronous demodulator and AFC circuit, an AGC detector with tuner output, an integral three-level sandcastle pulse generator, and fully synchronized vertical and horizontal drive outputs. A triggered vertical divider automatically adapts to a 50 or 60Hz vertical signal and eliminates the need for an external vertical frequency control.

Signal strength-dependent, time constant switches in the horizontal phase detector make external VCR switching unnecessary.

Sound signals are demodulated and amplified within the IC in a circuit which includes volume control and muting.

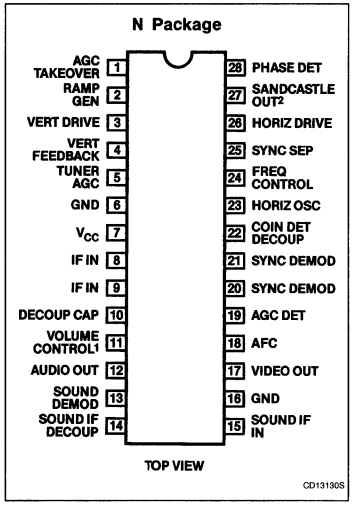
FEATURES

- **Vision IF amplifier with synchronous demodulator**
- **AGC detector for negative modulation**
- **AGC output to tuner**
- **AFC circuit**
- **Video and audio preamplifiers**
- **Sound IF amplifier and demodulator**
- **Choice of sound volume control or horizontal oscillator starting function**
- **Horizontal synchronization circuit with two control loops**
- **Triggered divider system for vertical synchronization and sawtooth generation giving automatic amplitude adjustment for 50 or 60Hz vertical signal**
- **Transmitter identification circuit with mute output**
- **Sandcastle pulse generator**

APPLICATION

- **Color TV**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4501N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{7-6}$	Supply voltage (Pin 7)	13.2	V
P_{TOT}	Total power dissipation	1.7	W
T_A	Operating ambient temperature range	−25 to +65	°C
T_{STG}	Storage temperature range	−65 to +150	°C

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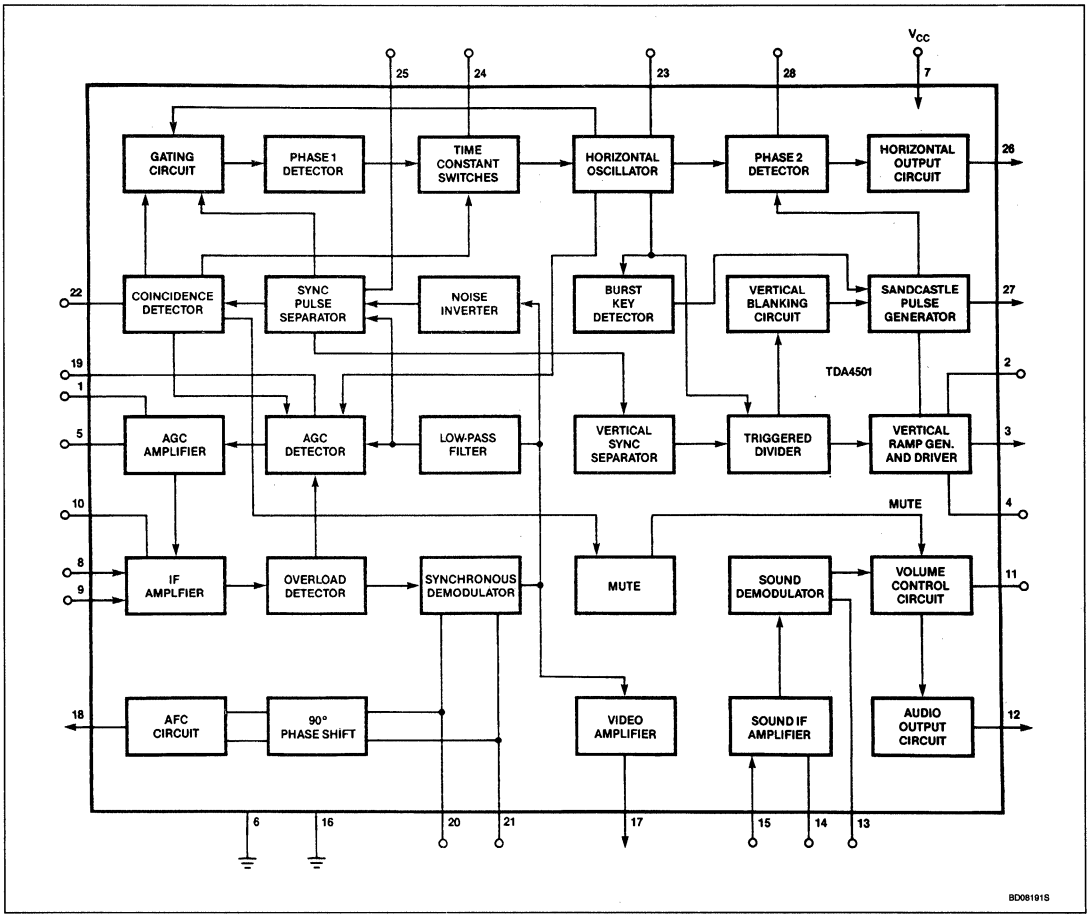
BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{7-6} = 10.5V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
V_{CC}	Supply voltage (Pin 7)	9.5	10.5	13.2	V
I_{CC}	Supply current (Pin 7)		120		mA
V_{11-6}	Supply voltage (Pin 11)		10.5		V
I_{11}	Supply current (Pin 11) for horizontal oscillator start		6		mA
Vision IF amplifier (Pins 8 and 9)					
V_{8-9}	Input sensitivity at 38.9MHz[1]	40	70	120	μV
V_{8-9}	Input sensitivity at 45.75MHz[1]		90		μV
R_{8-9}	Differential input resistance (Pin 8 to 9)		1.3		kΩ
C_{8-9}	Differential input capacitance (Pin 8 to 9)		5		pF
	AGC range		60		dB
V_{8-9}	Maximum input signal	50	70		mV
ΔV_{17-6}	Expansion of output signal for 50dB variation of input signal with V_{8-9} at 150μV (0dB)		1		dB
Video amplifier					
V_{17-6}	Output level for zero signal input (zero point of switched demodulator)		4.5		V
V_{17-6}	Output signal top sync level[2]		1.4		V
$V_{17-6(P-P)}$	Amplitude of video output signal (peak-to-peak value)		2.8		V
$I_{17(INT)}$	Internal bias current of output transistor (NPN emitter-follower)	1.4	2.0		mA
BW	Bandwidth of demodulated output signal		6		MHz
dG_{17}	Differential gain (Figure 3)		6		%
$d\rho$	Differential phase (Figure 3)		4		%
	Video non-linearity complete video signal amplitude			10	%
	Intermodulation (Figure 4) at gain control = 45dB				
	f = 1.1MHz; blue;	55	60		dB
	f = 1.1MHz; yellow;	50	54		dB
	f = 3.3MHz; blue;	60	66		dB
	f = 3.3MHz; yellow	55	59		dB
	Signal-to-noise ratio[3] $Z_S = 75Ω$				
S/N	$V_I = 10mV$	50	54		dB
S/N	End of gain control range	50	56		dB
	Residual carrier signal		7	30	mV
	Residual 2nd harmonic of carrier signal		3	30	mV

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 10.5V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuner AGC[4]					
V_{1-6}	Take-over voltage (Pin 1) for positive-going tuner AGC (NPN tuner)		3.5		V
$V_{1-6(RMS)}$	Starting point takeover; V = 5V		0.4	2	mV
$V_{1-6(RMS)}$	Starting point takeover; V = 1.2V	50	70		mV
V_{1-6}	Take-over voltage (Pin 1) for negative-going tuner AGC (PNP tuner)		8		V
$V_{1-6(RMS)}$	Starting point takeover; V = 9.5V		0.3	2	mV
$V_{1-6(RMS)}$	Starting point takeover; V = 5.6V	50	70		mV
$I_{5\ MAX}$	Maximum output swing	2	3		mA
$V_{5-6(SAT)}$	Output saturation voltage I = 2mA			300	mV
I_5	Leakage current			1	μA
ΔV_I	Input signal variation complete tuner control	0.5	2	4	dB
AFC circuit (Pin 18)[5]					
$V_{18-6(P-P)}$	AFC output voltage swing	9		10	V
$\pm I_{18}$	Available output current		1		mA
	Control steepness 100% picture carrier 10% picture carrier	20	 40 15	80	 mV/kHz mV/kHz
V_{18-6}	Output voltage at nominal tuning of the reference-tuned circuit		5.25		V
V_{18-6}	Output voltage without input signal	2.7	5.25	8.5	V
Sound circuit					
V_{15LIM}	Input limiting voltage $V_O = V_O$ maximum −3dB; $Q_L = 16$ f_{AF} = 1kHz; f_C = 5.5MHz		400		μV
R_{15-6}	Input resistance $V_{I(RMS)}$ = 1mV		2.6		kΩ
C_{15-6}	Input capacitance $V_{I(RMS)}$ = 1mV		6		pF
 AMR AMR	AM rejection (Figures 7 and 8) V_I = 10mV V_I = 50mV		 35 43		 dB dB
$V_{12-6(RMS)}$	AF output signal Δf = 7.5kHz; minimum distortion	220	320		mV
Z_{12-6}	AF output impedance		150		Ω
THD	Total harmonic distortion Δf = 27.5kHz		1		%
 RR RR	Ripple rejection f_K = 100Hz, volume control 20dB when muted		 22 26		 dB dB
V_{12-6}	Output voltage Mute condition		2.6		V
S/N	Signal-to-noise ratio weighted noise (CCIR 468)		47		dB

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 10.5V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Volume control					
V_{11-6}	Voltage (Pin 11 disconnected)		4.8		V
I_{11}	Current (Pin 11 short-circuited)		1		mA
R_{11-6}	External control resistor		10		kΩ
	Suppression output signal during Mute condition		66		dB
Horizontal synchronization					
	Slicing level sync separator		30		%
	Holding range PLL	800	1100	1500	Hz
	Catching range PLL	600	1000		Hz
	Control sensitivity video-to-oscillator; at weak signal at strong signal during scan during vertical retrace and during catching		 2 3 6		 kHz/μs kHz/μs kHz/μs
Second control loop (positive edge)					
$\Delta t_D/\Delta t_O$	Control sensitivity		300		μs
t_D	Control range		25		μs
	Phase adjustment via second control loop; control sensitivity maximum allowed phase shift		 25 ±2		 μA/μs μs
Horizontal oscillator (Pin 23)					
f_{FR}	Free-running frequency R = 35kΩ; C = 2.7nF		15,625		Hz
	Spread with fixed external components			4	%
Δf_{FR}	Frequency variation due to change of supply voltage from 8 to 12V		0	0.5	%
Δf_{FR}	Frequency variation with temperature			1×10^{-4}	K^{-1}
Δf_{FR}	Maximum frequency shift			10	%
Δf_{FR}	Maximum frequency deviation ($V_{7-6} = 8V$)			10	%
Horizontal output (Pin 26)					
V_{26-6}	Output voltage HIGH			13.2	V
V_{26-6}	Output voltage at which protection commences			15.8	V
V_{26-6}	Output voltage LOW at $I_{26} = 10mA$		0.3	0.5	V
δ_0	Duty cycle of horizontal output signal		45		%
t_R, t_F	Rise and fall times of output pulse		150		ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 10.5V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Flyback input and sandcastle output					
I_{27}	Input current required during flyback pulse	0.1		2	mA
V_{27-6}	Output voltage during burst key pulse	7.5			V
V_{27-6}	Output voltage during horizontal blanking	3.5	4.0	4.5	V
V_{27-6}	Output voltage during vertical blanking	1.8	2.2	2.6	V
	Width of burst key pulse	3.1	3.5	3.9	μs
	Width of horizontal blanking pulse	flyback pulse width			
	Width of vertical blanking pulse 50Hz working 60Hz working		 21 17		 lines lines
	Delay between start of sync pulse at video output and rising edge of burst key pulse		5.2		μs
Coincidence detector mute output (Pin 22)					
V_{22-6}	Voltage for in-sync condition		9.5		V
V_{22-6}	Voltage for no-sync condition no signal		1.0	1.5	V
V_{22-6}	Switching level to switch phase detector from slow to fast	4.9	5.3	5.8	V
	Fast-to-slow hysteresis		1		V
V_{22-6}	Switching level to activate mute function (transmitter identification)	2.25	2.5	2.75	V
$I_{22(P-P)}$	Output current for in-sync condition (peak-to-peak value)	0.7	1.0		mA
Vertical ramp generator (Pin 2)					
I_2	Input current during scan		12		mA
I_2	Discharge current during retrace		0.5		mA
V_{2-6}	Minimum voltage		1.5		V
Vertical output (Pin 3)					
I_3	Output current			10	mA
R_{3-6}	Output impedance		400		Ω
Feedback input (Pin 4)					
 V_{4-6} $V_{4-6(P-P)}$	Input voltage DC component AC component (peak-to-peak value)		 3 1.2		 V V
I_4	Input current			12	μA
	Internal precorrection to sawtooth		6		%
	Deviation amplitude 50/60Hz			5	%

NOTES:

1. Typical value taken at starting level of AGC.
2. Signal with negative-going sync, maximum white level 10% of the maximum sync amplitude (see Figure 2).
3. Signal-to-noise ratio equals $20\log \frac{V_O(\text{black-to-white})}{V_{N(RMS)}}$ at B = 5MHz
4. Starting point tuner takeover NPN current 1.8mA;
5. $V_{I(RMS)} = 10mV$; see Figure 1; Q-factor = 36.

FUNCTIONAL DESCRIPTION

IF Amplifier, Demodulator, and AFC

The IF amplifier has a symmetrical input (Pins 8 and 9), the input impedance of which is suitable for SAW filtering to be used. The synchronous demodulator and the AFC circuit share an external reference tuned circuit (Pins 20 and 21). An internal RC network provides the necessary phase-shifting for AFC operation. The AFC circuit provides a control voltage output with a swing greater than 9V from Pin 18.

AGC Circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC circuit connected to Pin 19. Tuner AGC voltage is supplied from Pin 5 and is suitable for tuners with PNP or NPN RF stages. The sense of the AGC (to increase in a positive or negative direction) and the point of tuner take-over are preset by the voltage level at Pin 1.

Video Amplifier

The signal through the video amplifier comprises video and sound information; therefore, no gating of the video amplifier is performed during flyback periods.

Sound Circuit and Horizontal Oscillator Starting Function

The input to the sound IF amplifier is obtained by a bandpass filter coupling from the video output (Pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (10kΩ) between Pin 11 and ground, or by supplying Pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no input signal is present.

The horizontal oscillator starting function is obtained by supplying Pin 11 with a current of 6mA during the switching-on period. The IC then uses this current to generate drive pulses for the horizontal deflection. For this application, the main supply voltage for the IC can be obtained from the horizontal deflection circuit.

Vertical Divider System

A triggered divider system is used to synchronize the vertical drive waveforms, adjusting automatically to 50 or 60Hz working. A large window (search window) is opened between counts of 488 and 722; when a separated vertical sync pulse occurs before count 576, the system works in the 60Hz mode; otherwise, 50Hz working is chosen.

A narrow window is opened when 15 approved sync pulses have been detected. Divider ratio between 522 and 528 switches to 60Hz mode; between 622 and 628 switches to 50Hz mode.

The vertical blanking pulse is also generated via the divider system by adding the anti-topflutter pulse and the blanking pulse.

Line Phase Detector

The circuit has three operating conditions:

a. Strong input signal and synchronized.

b. Weak signal and synchronized.

c. Non-synchronized (weak and strong) signal.

The input signal condition is obtained from the AGC circuit.

DC Volume Control/Horizontal Oscillator Start

The operation depends on the application. When during switch-on no current is supplied, Pin 11 will act as volume control. When a current of 6mA is applied, the volume control is set to maximum and the circuit will generate drive pulses for the horizontal deflection.

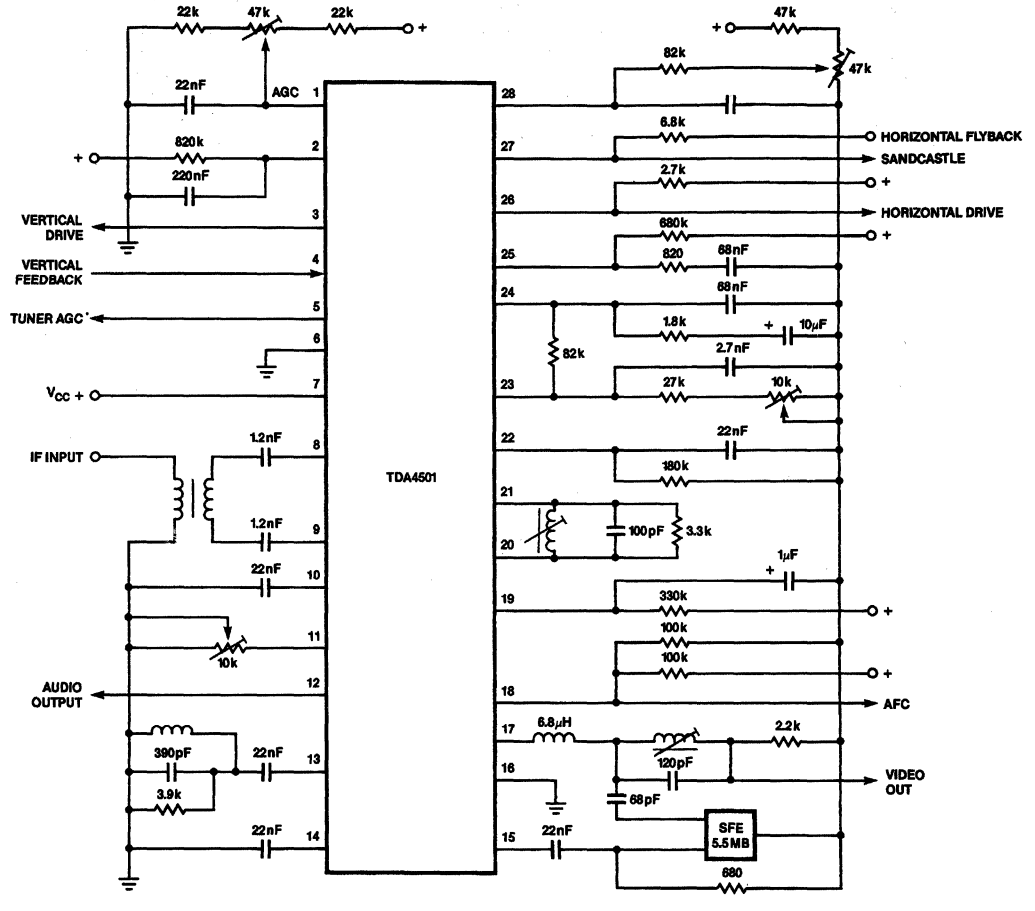


Figure 1. Application Diagram

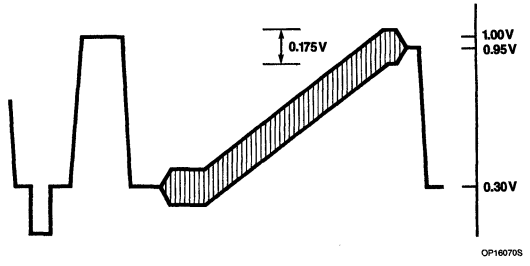


Figure 2. Video Output Signal

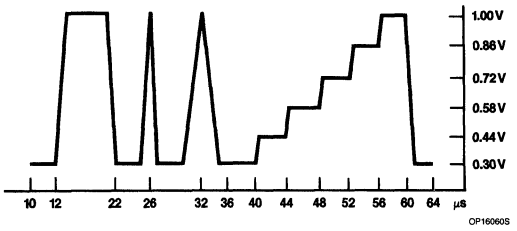


Figure 3. EBU Test Signal Waveform (Line 330)

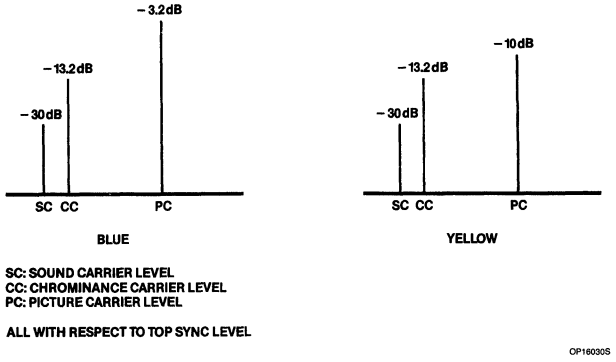


Figure 4. Input Signal Conditions

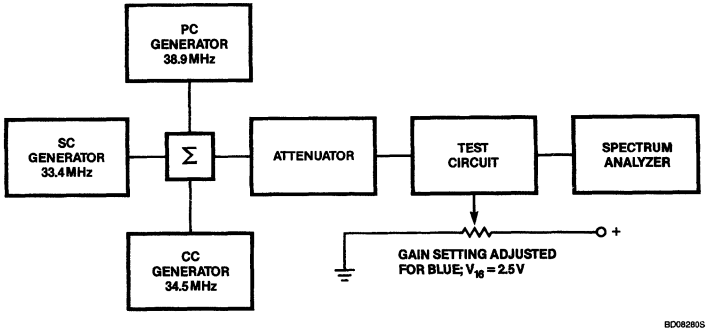


Figure 5. Test Setup Intermodulation

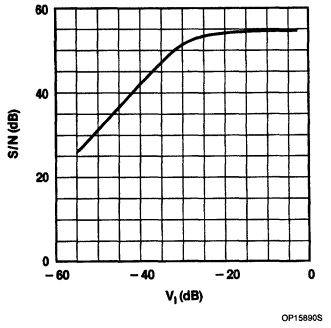


Figure 6. S/N Ratio as a Function of the Input Voltage

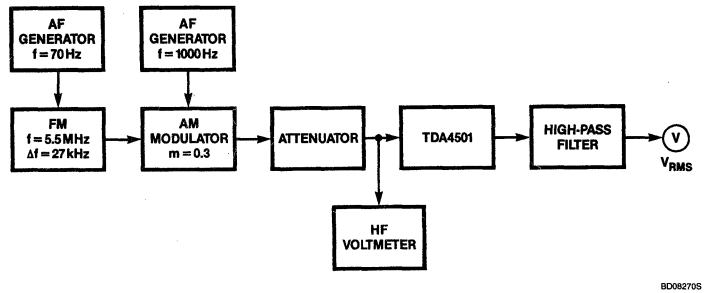


Figure 7. Test Setup AM Suppression

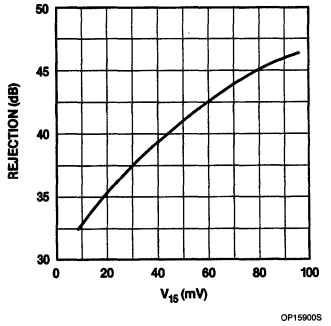


Figure 8. AM Rejection

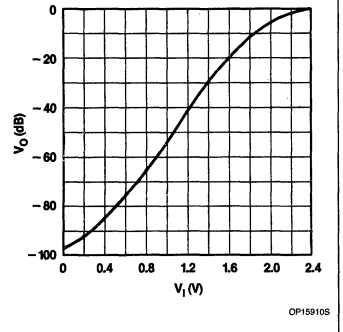


Figure 9. Volume Control Characteristics

Signetics

TDA4502

Small-Signal Subsystem IC for Color TV With Video Switch

Objective Specification

Linear Products

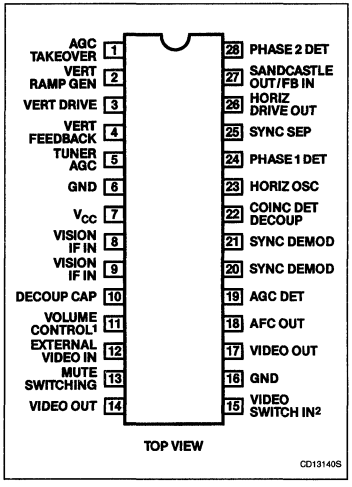
DESCRIPTION

The TDA4502 is a TV subsystem circuit intended to be used in color TV receivers. It is similar to the TDA4505, with the exception that it has no sound IF circuit or audio preamplifiers. Instead, it has a video switching input circuit for switching an external video signal.

FEATURES

- **Vision IF amplifier with synchronous demodulator**
- **AGC detector suited for negative modulation**
- **Tuner AGC**
- **AFC circuit with on/off switch**
- **Video preamplifier**
- **Video switch for an external video signal**
- **Horizontal synchronization circuit with two control loops**
- **Vertical synchronization (divider system) and sawtooth generation**
- **Sandcastle pulse generation**

PIN CONFIGURATION



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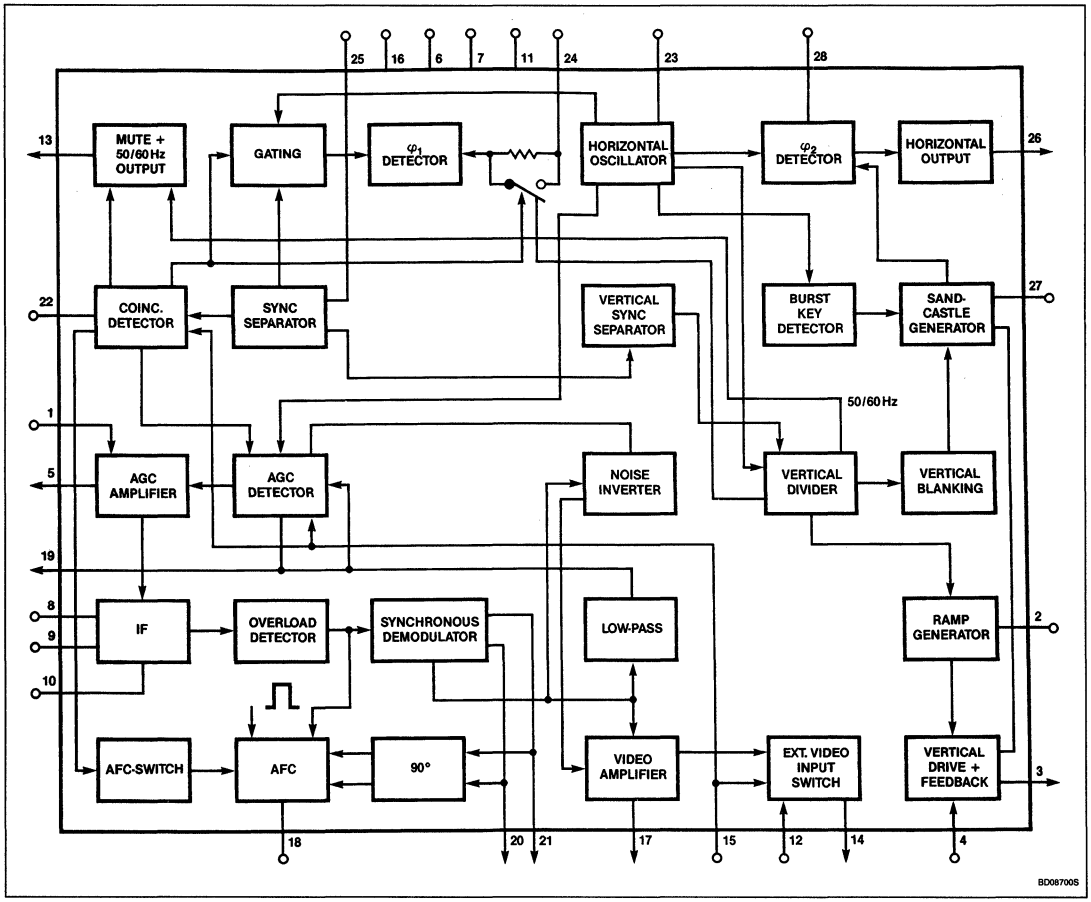
Small-Signal Subsystem IC for Color TV With Video Switch TDA4502

BLOCK DIAGRAM



Signetics

TDA4503

Small-Signal Subsystem for Monochrome TV

Product Specification

Linear Products

DESCRIPTION

The TDA4503 combines all small-signal functions (except the tuner) which are required for monochrome TV receivers. For a complete monochrome TV receiver only power output stages are required to be added for horizontal and vertical deflection, video and sound. This part is designed to work with the TDA3561, Vertical Output IC.

The TDA4503 can also be used in low cost color television receivers.

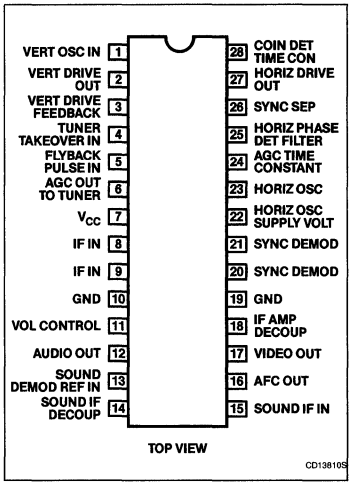
FEATURES

- **Vertical sync separator and oscillator**
- **Video preamplifier**
- **AGC detector**
- **Sync separator**
- **Horizontal synchronization**
- **Vision IF amplifier and synchronous demodulator**
- **Tuner AGC**
- **AFC circuit**
- **Sound IF amplifier and demodulator**
- **Audio preamplifier with DC volume control**
- **Gate pulse generator**

APPLICATIONS

- **Television receiver**
- **CATV converter**

PIN CONFIGURATION

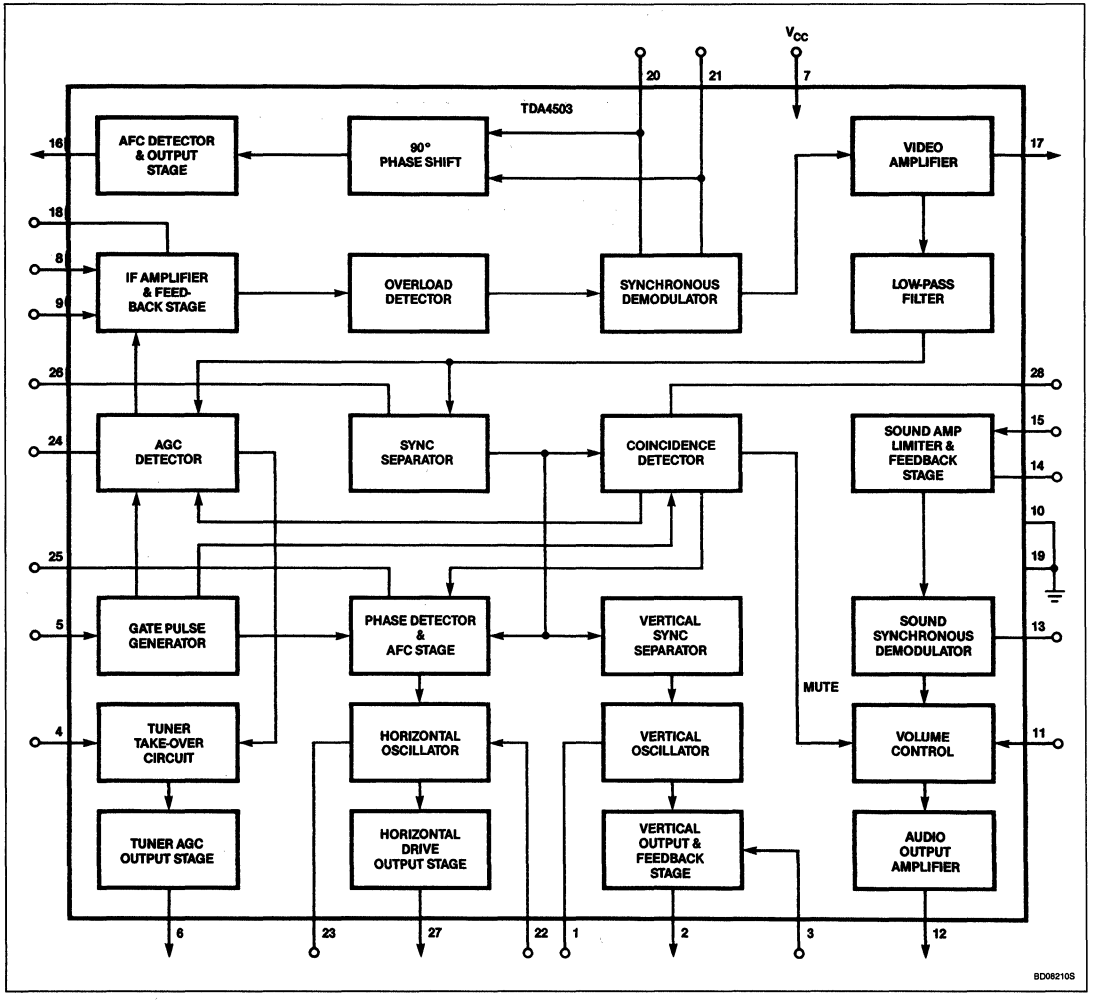


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4503N

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{7-10}$	Supply voltage (Pin 7)	13.2	V
P_{TOT}	Total power dissipation	1.7	W
T_A	Operating ambient temperature range	−25 to +65	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC AND AC ELECTRICAL CHARACTERISTICS $V_{7-10} = 10.5V$; $V_{22-10} = 10.5V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
V_{7-10}	Supply voltage (Pin 7)	9.5	10.5	13.2	V
I_7	Supply current (Pin 7)		82	100	mA
V_{22-10}	Supply voltage (Pin 22)	9.5	10.5	13.2	V
I_{22}	Supply current (Pin 22)[1]		5	6.5	mA
P_{TOT}	Total power dissipation		920	1150	mW
Vision IF amplifier (Pins 8 and 9)					
V_{8-9}	Input sensitivity at 38.9 MHz[2]	40	80	120	μV
V_{8-9}	Input sensitivity at 45.75 MHz[2]		90		μV
R_{8-9}	Differential input resistance (Pin 8 to 9)		1.3		kΩ
C_{8-9}	Differential input capacitance (Pin 8 to 9)		5		pF
	AGC range		59		dB
V_{8-9}	Maximum input signal	50	70		mV
ΔV_{17-10}	Expansion of output signal (Pin 17) for 50dB variation of input signal (Pins 8 and 9)[3]		0.5	1.0	dB
Video amplifier[4]					
V_{17-10}	Output level for zero signal input (zero point of switched demodulator)	4.2	4.5	4.8	V
V_{17-10}	Output signal top sync level[5]	1.25	1.45	1.65	V
$V_{17-10(P-P)}$	Amplitude of video output signal (peak-to-peak value)	2.4	2.7	3.0	V
$I_{17(INT)}$	Internal bias current of output transistor (NPN emitter-follower)	1.4	2.0		mA
BW	Bandwidth of demodulated output signal		5		MHz
G_{17}	Differential gain[6] (Figure 5)		6		%
	Differential phase[6] (Figure 5)		4		%
	Video non-linearity over total video amplitude (peak white to black)			10	%
	Intermodulation (Figures 6 and 7) at gain control = 45dB				
	f = 1.1MHz; blue	55	60		dB
	f = 1.1MHz; yellow	50	54		dB
	f = 3.3MHz; blue	60	66		dB
	f = 3.3MHz; yellow	55	59		dB
	Signal-to-noise ratio[7]				
S/N	at $V_I = 10mV$	50	54		dB
S/N	at end of AGC range	50	56		dB
S/N	as a function of input signal	see Figure 8			
	Residual AM of intercarrier output signal[8]		5	10	%
	Residual carrier signal		7	30	mV
	Residual 2nd harmonic of carrier signal		3	30	mV

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{7-10} = 10.5V; V_{22-10} = 10.5V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuner AGC[9]					
V_{4-10}	Takeover voltage (Pin 4) for positive-going tuner AGC (NPN tuner)		3.5		V
$V_{8-9(RMS)}$	Starting point takeover at V_{4-10} = 5V (RMS value)		0.4	2.0	mV
$V_{8-9(RMS)}$	Starting point takeover at V_{4-10} = 1.2V (RMS value)	50	70		mV
V_{4-10}	Takeover voltage (Pin 1) for negative-going tuner AGC (PNP tuner)		8		V
$V_{8-9(RMS)}$	Starting point takeover at V_{4-10} = 9.5V (RMS value)		0.3	2.0	mV
$V_{8-9(RMS)}$	Starting point takeover at V_{4-10} = 5.6V (RMS value)	50	70		mV
I_{6MAX}	Maximum tuner AGC output swing	2	3		mA
$V_{6-10(SAT)}$	Output saturation voltage at I_6 = 2mA			300	mV
I_6	Leakage current at Pin 6			1	μA
ΔV_{8-9}	Input signal variation required for complete tuner control	0.5	2	4	dB
AFC circuit (Pin 16)[10]					
$V_{16-10(P-P)}$	AFC output voltage swing (peak-to-peak value)	9		10	V
$\pm I_{16}$	Available output current		1		mA
	Control steepness at 100% picture carrier 10% picture carrier	20	 40 15	80	 mV/kHz mV/kHz
V_{16-10}	Output voltage at nominal tuning of the reference-tuned circuit		5.25		V
V_{16-10}	Output voltage without input signal	2.7	6.0	8.5	V
Sound circuit					
V_{15LIM}	Input limiting voltage[11] (RMS value) at $V_O = V_{O\ MAX}$–3dB		2		mV
R_{15-10}	Input resistance at $V_{I(RMS)}$ = 1mV		2.6		kΩ
C_{15-10}	Input capacitance at $V_{I(RMS)}$ = 1mV		6		pF
	AM rejection (Figures 7 and 8) at				
AMR	V_I = 10mV		35		dB
AMR	V_I = 50mV		43		dB
$V_{12-6(RMS)}$	AF output signal[12] (RMS value)	220	320		mV
Z_{12-10}	AF output impedance		150		Ω
THD	Total harmonic distortion[12]		1		%
	Ripple rejection at				
RR	f_K = 100Hz, volume control 20dB		22		dB
RR	when muted		26		dB
V_{12-10}	Output voltage in mute condition		2.6		V
S/N	Signal-to-noise-ratio; weighted noise (CCIR 468)		47		dB
Volume control					
V_{11-10}	Voltage (Pin 11 disconnected)		6.9		V
I_{11}	Current (Pin 11 connected to ground)		1		mA
R_{11-10}	External control resistor[13]		5		kΩ
	Suppression of output signal during mute condition		66		dB

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{7-10} = 10.5V$; $V_{22-10} = 10.5V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal synchronization					
	Slicing level sync separator[14]		30		%
	Phase-locked loop holding range	±800	±1100	±1500	Hz
	Phase-locked loop catching range	±600	1000		Hz
	Control sensitivity video to flyback[15]		2.3		kHz/μs
	Delay between leading edge of sync pulse and zero cross-over of sawtooth (Pin 5)		3		μs
Horizontal oscillator (Pin 23)					
f_{FR}	Free-running frequency; R = 35kΩ; C = 2.7nF		15,626		Hz
	Spread with fixed external components			4	%
Δf_{FR}	Frequency variation due to change of supply voltage from 8 to 12V		0	0.5	%
TC	Temperature coefficient			1×10^{-4}	$°C^{-1}$
Δf_{FR}	Maximum frequency shift			10	%
Δf_{FR}	Maximum frequency deviation ($V_{7-10} = 8V$)			10	%
Horizontal output (Pin 27)					
I_{27}	Output current	5			mA
R_{27}	Output impedance		200		Ω
V_{27-10} V_{27-22}	Output voltage at $I_{27} = 5mA$		1.4 2.5		V V
α	Duty factor of horizontal output signal[16]	0.35	0.40	0.45	%
t_R, t_F	Rise and fall times of output pulse		400		ns
Flyback input (Pin 5)					
V_5	Amplitude of input pulse	2	4	6	V
V_5	Voltage at which gate pulse generator changes state[17]		0		V
Coincidence detector mute output (Pin 28)[18]					
V_{28-10}	Voltage for in-sync condition		9.5		V
V_{28-10}	Voltage for no-sync condition (no input signal)		1.0	1.5	V
V_{28-10}	Voltage level for phase detector to switch from slow to fast	3.7	4.1	4.5	V
	Fast-to-slow hysteresis		1		V
V_{28-10}	Voltage level to activate mute function (transmitter identification)	2.25	2.5	2.75	V
$I_{22(P-P)}$	Output current for in-sync condition (peak-to-peak value)	0.7	1.0		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{7-10} = 10.5V; V_{22-10} = 10.5V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Vertical oscillator (Pin 1)					
f_{FR}	Free-running frequency at C = 220nF; R = 560kΩ		47.5		Hz
	Spread with fixed external components			4	%
	Holding range at nominal frequency	52.5			Hz
TC	Temperature coefficient			2×10^{-4}	$°C^{-1}$
Δf_{FR}	Frequency variation due to change of supply voltage from 9.5 to 12V		3	5	%
I_1	Leakage current at Pin 1			1.6	μA
Vertical output (Pin 2)					
I_2	Output current	1	1.3		mA
R_2	Output resistance		2		kΩ
Feedback input (Pin 3)					
V_{3-10} $V_{3-10(P-P)}$	Input voltage DC component AC component (peak-to-peak value)	4.0	5.0 1.2	5.5	V V
I_3	Input current			12	μA
ΔI_3	Non-linearity of deflector current at V_{7-10} = 10.5V			2.5	%
	Delay between leading edge of vertical sync and start of vertical oscillator flyback	6		10	μs

NOTES:

1. The horizontal oscillator can be started by supplying a current of 6mA to Pin 22. Taking this current from the mains rectifier allows the positive supply voltage to Pin 7 to be derived from the horizontal output stage (the load current of Pin 27 is additional to the 6mA quoted).
2. At start of AGC.
3. Measured with 0dB = 200μV.
4. Measured at 10mV (RMS) top sync output signal.
5. Signal with negative-going sync; top white = 10% of the top sync amplitude.
6. Measured with test line as shown in Figure 3. The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest values relative to the subcarrier amplitude at blanking level. The differential phase is defined as the difference in degrees between the largest and smallest phase angles.
7. Measured with a source impedance of 75Ω.

   $$\text{Signal-to-noise ratio} = 20\log \frac{V_O \text{ black-to-white}}{V_{I(RMS)} \text{ at B = 5MHz}}$$

8. Measured with a sawtooth-modulated input signal: m = 90%; $V_{I(RMS)}$ = 10mV;

   $$\text{Amplitude modulation} = \frac{V_O \text{ SC at top sync} - V_O \text{ SC at white}}{V_O \text{ SC at top sync} + V_O \text{ SC at white}} \times 100\%.$$

   (SC = sound carrier)
9. Starting point of tuner take-over for an NPN tuner is when I_6 = 1.8mA, and for a PNP tuner is when I_6 = 0.2mA.
10. Measured at $V_{8-9(RMS)}$ = 10mV and Pin 16 loaded with 2 × 100kΩ between V_7 and ground. Reference tuned circuit Q-factor = 36.
11. Reference tuned circuit Q-factor = 16; audio frequency = 1kHz; carrier frequency = 5.5 MHz.
12. The demodulator tuned circuit must be tuned for minimum distortion; output signal is measured at Δf = 7.5kHz; other measurements are at Δf = 27.5kHz.
13. Volume control can be realized by a variable resistor (5kΩ) connected between Pin 11 and ground, or by a variable voltage direct to Pin 11 (the low value of input impedance to Pin 11 must be taken into account).
14. The sync separator is noise-gated; the slicing level is referred to the top sync level and is independent of the video signal. The value stated is a percentage of the sync pulse amplitude, the level being dependent on external resistors connected to Pin 26.
15. The phase detector current is increased by a factor of seven during catching and when the phase detector is switched to 'fast' via Pin 28, thus ensuring a wide catching range and a high dynamic loop gain.
16. The negative going edge initiates switching-off of the line output transistor (simultaneous driver).
17. The circuit requires an integrated flyback pulse. Gate pulses for AGC and coincidence detectors are obtained from the sawtooth waveform.
18. The functions of in-sync, out-of-sync, and transmitter identification are combined on Pin 28. For the reception of VCR signals, V_{28} must be fixed between 3V and 4.5V so that the time constant is fast and sound information is preserved.

FUNCTIONAL DESCRIPTION

IF Amplifier, Demodulator, and AFC

The IF amplifier operates with symmetrical inputs at Pins 8 and 9 and has an input impedance suitable for SAW filter application. The amplifier sensitivity gives a peak-to-peak output voltage of 3V for an RMS input of 70μV. The demodulator and the AFC circuit share an external reference tuned circuit (Pins 20 and 21) and an internal RC network provides the phase-shifting necessary for AFC operation. The AFC circuit provides a control voltage output with a (typical) swing of 9V from Pin 16 (V_{CC} = 10.5V).

AGC Circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC network connected to Pin 24. The typical gain control range of the IF amplifier is 60dB. Tuner AGC voltage is supplied from Pin 6 and is suitable for tuners with PNP or NPN RF stages. The sense of the AGC (to increase in a positive or negative direction) and the point of tuner takeover are preset by the voltage level at Pin 4 (V_4 = 3.5V (typ.) for positive AGC; V_4 = 8V (typ.) for negative AGC).

Video Amplifier

The video signal output from Pin 17 has a peak-to-peak value of 3V (top sync level = 1.5V) and carries negative-going sync. In order to retain sound information at Pin 17, the video signal is not blanked during flyback periods.

Sound Circuit

The sound IF signal present at the video output (Pin 17) is coupled to the sound circuit by a bandpass filter to Pin 15. The sound circuit has an amplifier-limiter stage, a synchronous demodulator with reference tuned circuit at Pin 13, a volume control stage, and an output amplifier. The volume control has a range of approximately 80dB and the audio output signal at maximum volume and with Δf = 7.5kHz is 320mV (RMS value). The sound output signal is suppressed when no input signal is detected.

Synchronization Circuits

The sync separator slicing level is determined by an external resistor network at Pin 26. The slicing level is referred to the top sync level and the recommended value for slicing is 30%. Internal protection from electrical noise is included.

A gated phase detector compares the phase of the separated sync pulses with a sawtooth waveform obtained from the flyback pulse at Pin 5. In sync and out-of-sync conditions are detected by the coincidence detector at Pin 28 (this circuit also gives transmitter identification). During the out-of-sync condition, gating of the phase detector is switched off and the output current from the phase detector increases to give the detector a short time-constant and thus a fast response. This condition can be imposed by clamping the voltage at Pin 28 to 3.5V for the reception of VCR signals.

The horizontal oscillator frequency is controlled by the output voltage of the phase detector circuit. The horizontal drive output from Pin 27 has a duty factor of 40%.

Vertical sync pulses are separated by an internal integrating network and are used to trigger the vertical oscillator. A comparator circuit compares the vertical sawtooth waveform, generated by the vertical oscillator, with feedback from the deflection coils, and supplies the drive voltage for the output stage at Pin 2.

Power Supplies

The main supply is to Pin 7 (positive supply) and Pin 10 (ground). The horizontal oscillator is supplied from Pin 22 to facilitate starting of the oscillator from a high-voltage rail. A special ground connection at Pin 19 is used by critical voltage dividers in the feedback loops of the vision and sound IF circuits.

Small-Signal Subsystem for Monochrome TV TDA4503

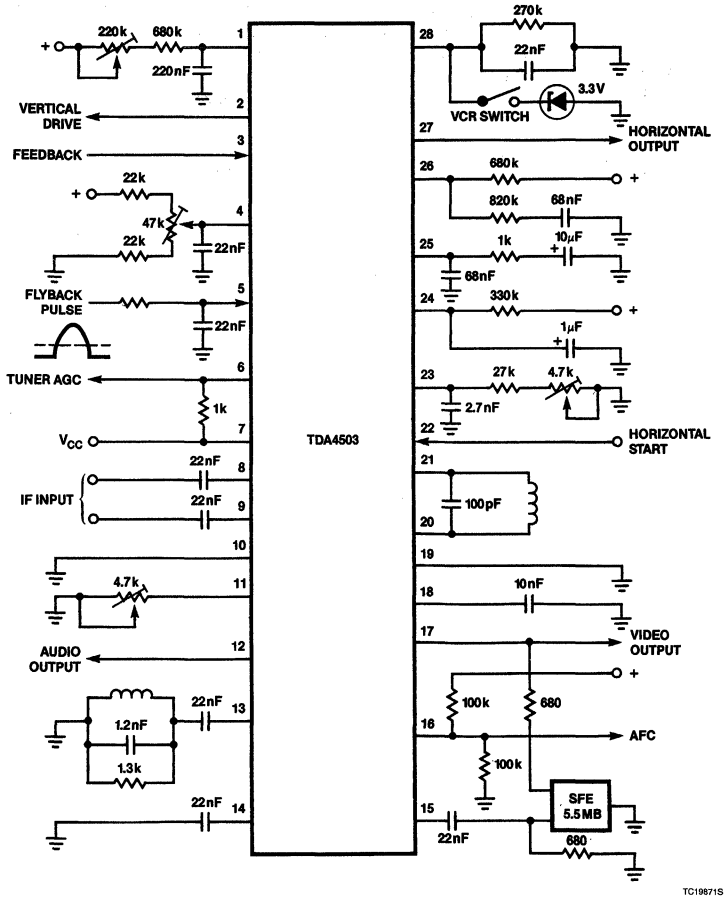


Figure 1. Application Circuit Diagram

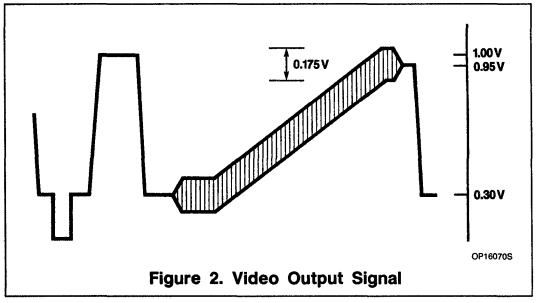


Figure 2. Video Output Signal

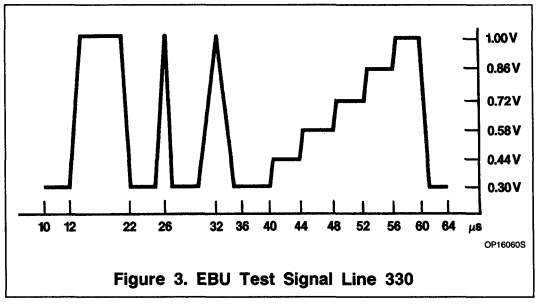


Figure 3. EBU Test Signal Line 330

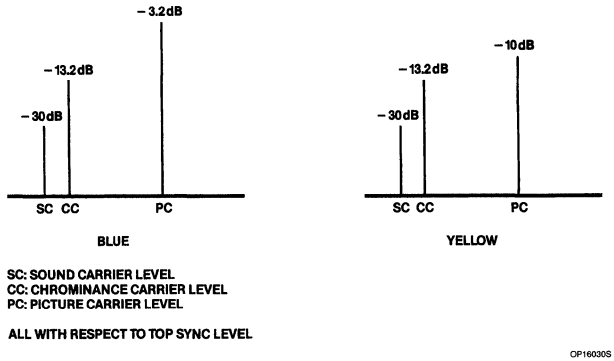
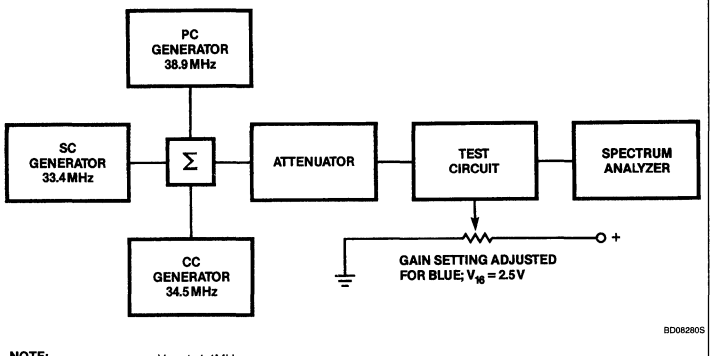


Figure 4. Input Signal Conditions for Intermodulation Test



NOTE:

Value at 1.1MHz = $20\log\frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 1.1MHz} + 3.6dB$;

Value at 3.3MHz = $20\log\frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 3.3MHz}$

Figure 5. Circuit for Intermodulation Test

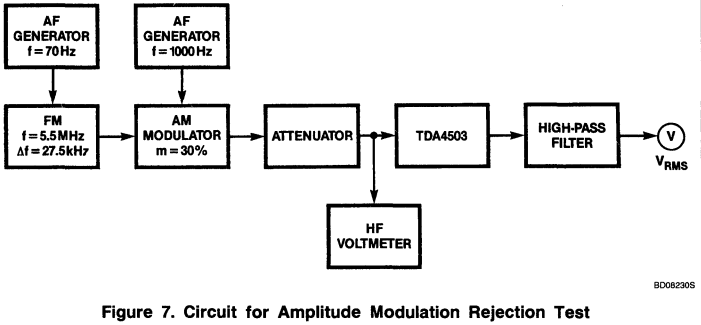


Figure 7. Circuit for Amplitude Modulation Rejection Test

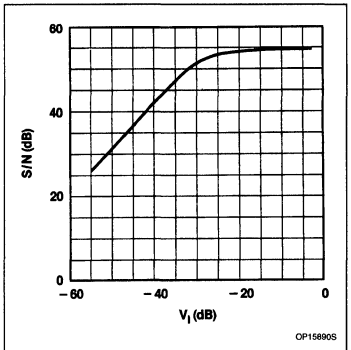


Figure 6. Signal-to-Noise Ratio as a Function of Input Voltage

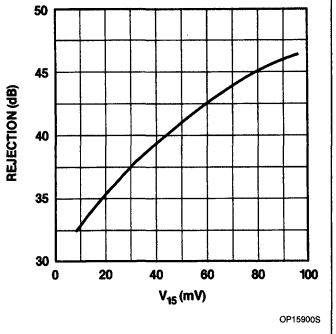


Figure 8. Typical Amplitude Modulation Rejection Curve

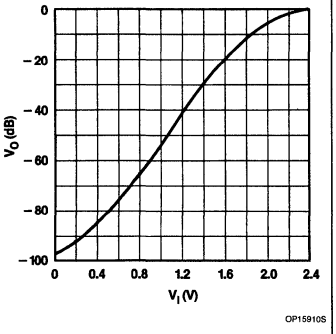


Figure 9. Volume Control Characteristic

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Signetics

TDA4505

Small-Signal Subsystem IC for Color TV

Preliminary Specification

Linear Products

DESCRIPTION

The TDA4505 is a TV subsystem circuit intended to be used for base-band demodulation applications. This circuit consists of all small-signal functions (except the tuner) required for a quality color television receiver. The only additional circuits needed to complete a receiver are a tuner, the deflection output stages, and a color decoder. The TDA3563 or 67, NTSC color decoder, and the TDA3654 vertical output, are ideal complements for the TDA4505.

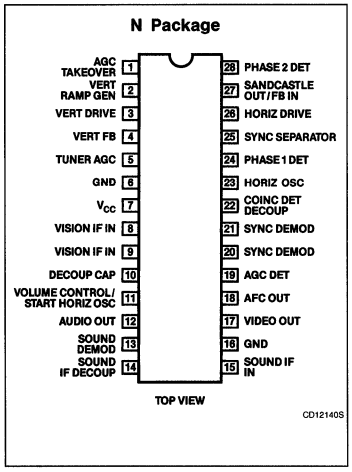
FEATURES

- **Vision IF amplifier with synchronous demodulator**
- **Tuner AGC (negative-going control voltage with increasing signal)**
- **AGC detector for negative modulation**
- **AFC circuit**
- **Video preamplifier**
- **Sound IF amplifier, demodulator and preamplifier**
- **DC volume control**
- **Horizontal synchronization circuit with two control loops**
- **Extra time constant switches in the horizontal phase detector**
- **Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 or 60Hz**
- **Three-level sandcastle pulse generation**

APPLICATIONS

- **Color television receiver**
- **CATV converters**
- **Base-band processing**

PIN CONFIGURATION



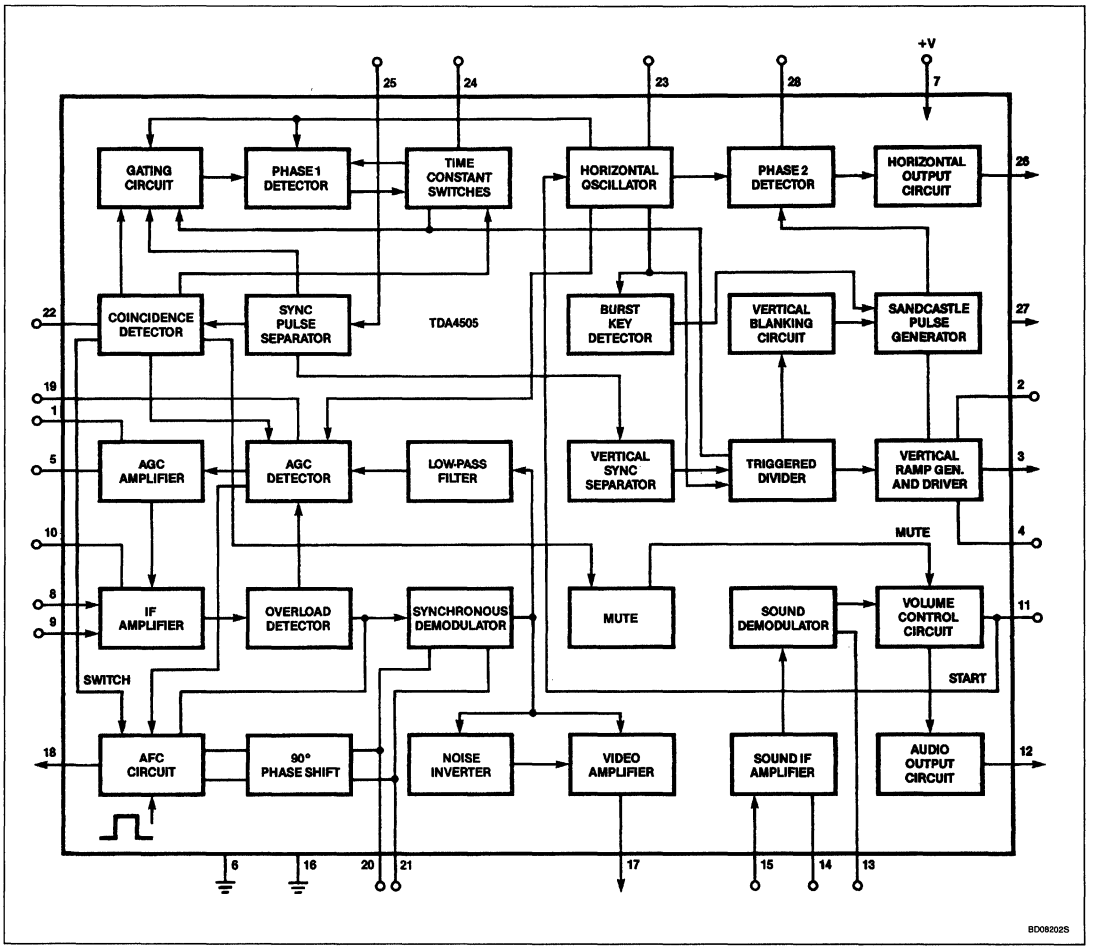
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4505N
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4505AN
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA4505BN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 7)	13.2	V
P_{TOT}	Total power dissipation	2.3	W
T_A	Operating ambient temperature range	−25 to +65	°C
T_{STG}	Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
V_{7-6}	Supply voltage (Pin 7)	9.5	12	13.2	V
I_7	Supply current (Pin 7)		135		mA
V_{11-6}	Supply voltage (Pin 11)[1]		8.6		V
I_{11}	Supply current (Pin 11) for horizontal oscillator start		6	8	mA
Vision IF amplifier (Pins 8 and 9)					
V_{8-9}	Input sensitivity 38.9MHz on set AGC	60	100	140	μV
V_{8-9}	45.75MHz on set AGC		120		μV
R_{8-9}	Differential input resistance (Pin 8 to 9)	800	1300	1800	Ω
C_{8-9}	Differential input capacitance (Pin 8 to 9)		5		pF
G_{8-9}	Gain control range	56	60		dB
V_{8-9}	Maximum input signal	50	100		mV
ΔV_{17-6}	Expansion of output signal for 50dB variation of input signal with V_{8-9} at 150μV (0dB)		1		dB
Video amplifier measured at top sync input signal voltage (RMS value) of 10mV					
V_{17-6}	Output level for zero signal input (zero point of switched demodulator)		5.8		V
V_{17-6}	Output signal top sync level[2]	2.7	2.9	3.1	V
$V_{17-6(P-P)}$	Amplitude of video output signal (peak-to-peak value)		2.6		V
$I_{17(INT)}$	Internal bias current of output transistor (NPN emitter-follower)	1.4	2.0		mA
BW	Bandwidth of demodulated output signal	5			MHz
G_{17}	Differential gain (Figure 3)[3]		4	10	%
φ	Differential phase (Figure 3)[3]		3	10	deg.
	Video non-linearity[4] complete video signal amplitude			10	%
	Intermodulation (Figure 4) at gain control = 45dB				
	f = 1.1MHz; blue	55	60		dB
	f = 1.1MHz; yellow	50	54		dB
	f = 3.3MHz; blue	60	66		dB
	f = 3.3MHz; yellow	55	59		dB
	Signal-to-noise ratio[5]				
S/N	$Z_S = 75\Omega$; $V_I = 10mV$	50	54		dB
S/N	end of gain control range	50	56		dB
	Residual carrier signal		7	30	mV
	Residual 2nd harmonic of carrier signal		24	30	mV

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuner AGC[13]					
$V_{1-6(RMS)}$	Minimum starting point take-over			0.5	mV
$V_{1-6(RMS)}$	Maximum starting point take-over	50	100		mV
I_{5MAX}	Maximum output swing	6	8		mA
$V_{5-6(SAT)}$	Output saturation voltage I = 2mA			300	mV
I_5	Leakage current			1	µA
ΔV_I	Input signal variation complete tuner control (ΔI_5 = 2mA)	0.5	2	5	dB
AFC circuit (Pin 18)[6]					
$V_{18-6(P-P)}$	AFC output voltage swing	9.5	10.35	11	V
$\pm I_{18}$	Available output current		2.6		mA
	Control steepness		70		mV/kHz
V_{18-6}	Output voltage at nom. tuning of the reference-tuned circuit		6		V
I_{18}	Offset current AFC output (Pins 20 and 21 short-circuited)		TBD		µA
Sound circuit					
V_{15LIM}	Input limiting voltage $V_O = V_{O\ MAX} - 3dB$; $Q_L = 16$; f_{AF} = 1kHz; f_C = 5.5MHz		400	800	µV
R_{15-6}	Input resistance $V_{I(RMS)}$ = 1mV		2.6		kΩ
C_{15-6}	Input capacitance $V_{I(RMS)}$ = 1mV		6		pF
AMR AMR	AM rejection (Figures 7 and 8) V_I = 10mV V_I = 50mV		46 50		dB dB
$V_{12-6(RMS)}$	AF output signal Δf = 7.5kHz; minimum distortion	400	600	800	mV
$V_{12-6(RMS)}$	AF output signal; Δf = 50kHz Pin 11 used as starting pin	300	700	1200	mV
Z_{12-6}	AF output impedance		25	100	Ω
THD	Total harmonic distortion volume control 20dB, Δf = 27.5kHz; weighted acc. CCIR 468		1	3	%
RR RR	Ripple rejection f_k = 100Hz, volume control 20dB when muted		35 30		dB dB
V_{12-6}	Output voltage in Mute condition		3.0		V
S/N	Signal-to-noise ratio; Δf = 27.5kHz weighted noise (CCIR 468)		45		dB
Volume control (Figure 8)					
V_{11-6}	Voltage (Pin 11 disconnected)		5.0		V
I_{11}	Circuit (Pin 11 short circuited)		0.9		mA
R_{11-6}	External control resistor		5		kΩ
OSS	Suppression output signal during mute condition		66		dB

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sync separator and first control loop					
$V_{25-6(P-P)}$	Required sync pulse amplitude; $R_{17-25} = 2k\Omega$[7]	200	800		mV
	Input current				
I_{25}	$V_{25-6} > 5V$		10		μA
I_{25}	$V_{25-6} = 0V$		TBD		mA
$\pm \Delta f$	Holding range PLL		1100	1500	Hz
$\pm \Delta f$	Catching range PLL	600	1000		Hz
	Control sensitivity[8]				
	video to oscillator; at weak signal		2.5		kHz/μs
	at strong signal during scan		3.75		kHz/μs
	during vertical retrace and catching		7.5		kHz/μs
Second control loop (positive edge)					
$\Delta t_D / \Delta t_O$	Control sensitivity R_{28-6} = see Figure 1		50		
t_D	Control range		25		μs
Phase adjustment (via second control loop)					
	Control sensitivity		25		μA/μs
α	Maximum allowed phase shift		±2		μs
Horizontal oscillator (Pin 23)					
f_{FR}	Free-running frequency R = 34kΩ; C = 2.7nF		15,625		Hz
Δf	Spread with fixed external components		0.4	4	%
Δf_{FR}	Frequency variation due to change of supply voltage from 9.5 to 13.2V		0	0.5	%
TC	Frequency variation with temperature			1×10^{-4}	$°C^{-1}$
Δf_{FR}	Maximum frequency shift			10	%
Δf_{FR}	Maximum frequency deviation at start H-out		8	10	%
Horizontal output (Pin 26)					
V_{26-6}	Output voltage high level			13.2	V
V_{26-6}	Output voltage at which protection commences			15.8	V
V_{26-6}	Output voltage low at I_{26} = 10mA		0.15	0.5	V
d	Duty cycle of horizontal output signal at $t_P = 10\mu s$		0.45		
t_R	Rise time of output pulse		260		ns
t_F	Fall time of output pulse		100		ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{7-6} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Flyback input and sandcastle output[9]					
I_{27}	Input current required during flyback pulse	0.1		2	mA
V_{27-6}	Output voltage during burst key pulse	8	9.0		V
V_{27-6}	Output voltage during horizontal blanking	4	4.35	5	V
V_{27-6}	Output voltage during vertical blanking	2.1	2.5	2.9	V
t_W	Width of burst key pulse (60Hz)	3.1	3.5	3.9	µs
t_W	Width of burst key pulse (50Hz)	3.6	4.0	4.4	µs
	Width of horizontal blanking pulse	flyback pulse width			
	Width of vertical blanking pulse 50Hz divider in search window 60Hz divider in search window 50Hz divider in narrow window 60Hz divider in narrow window		 21 17 25 21		 lines lines lines lines
	Delay between start of sync pulse at video output and rising edge of burst key pulse		5.2		µs
Coincidence detector mute output[10]					
V_{22-6}	Voltage for in-sync condition		10.3		V
V_{22-6}	Voltage for no-sync condition no signal		1.5		V
V_{22-6}	Switching level to switch off the AFC		6.4		V
V_{22-6}	Hysteresis AFC switch		0.4		V
V_{22-6}	Switching level to activate mute function (transmitter identification)		2.4		V
V_{22-6}	Hysteresis Mute function		0.5		V
$I_{22(P-P)}$	Charge current in sync condition 4.7µs	0.7	1.0		mA
$I_{22(P-P)}$	Discharge current in sync condition 1.3µs		0.5		mA
Vertical ramp generator[11]					
I_2	Input current during scan		0.5	2	µA
I_2	Discharge current during retrace		0.4		mA
$V_{2-6(P-P)}$	Sawtooth amplitude		0.8	1.1	V
Vertical output (Pin 3)					
I_3	Output current			7	mA
V_{3-6}	Maximum output voltage		5.7		V
Feedback input (Pin 4)					
 V_{4-6} $V_{4-6(P-P)}$	Input voltage DC component AC component (peak-to-peak value)		 3.3 1.2		 V V
I_4	Input current			12	µA
Δt_P	Internal precorrection to sawtooth		5		%
	Deviation amplitude 50/60Hz		0	2	%
Vertical guard[12]					
 ΔV_{4-6} ΔV_{4-6}	Active at a deviation with respect to the DC feedback level; $V_{27-6} = 2.5V$; at switching level low at switching level high		 1.3 1.9		 V V

NOTES:

1. Pin 11 has a double function. When during switch-on a current of 6mA is supplied to this pin, this current is used to start the horizontal oscillator. The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as volume control. The indicated maximum value is the current at which all ICs will start. Higher currents are allowed: the excess current is bypassed to ground.
2. Signal with negative-going sync top white 10% of the top sync amplitude (Figure 2).
3. Measured according to the test line given in Figure 3.
   — The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   — The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
4. This figure is valid for the complete video signal amplitude (peak white to black).
5. The $S/N = 20 \log \frac{V_{OUT\ BLACK\text{-}TO\text{-}WHITE}}{V_{N(RMS)}}$ at B = 5MHz
6. The AFC control voltage is obtained by multiplying the IF-output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90° phase shift network. The IF-output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal, the AFC circuit is gated by means of an internally generated gating pulse. As a result the detector is operative only during black level at a constant carrier amplitude which contains no additional side bands. As a result the AFC output voltage contains no video information.
   At very weak input signals, the driver signal for the AFC circuit will contain a lot of noise. This noise signal has again an asymmetrical frequency spectrum and this will cause an offset of the AFC output voltage. To avoid problems due to this effect, the AFC is switched off when the AGC is controlled to maximum gain.
   The measured figures are obtained at an input sign RMS voltage of 10mV and the AFC output loaded with 2 times 220kΩ between $+V_S$ and ground. The unloaded Q-factor of the reference tuned circuit is 70. The AFC is switched off when no signal is detected by the coincidence detector or when the voltage at Pin 22 is between 1.2V and 6.4V. This can be realized by a resistor of 68kΩ connected between Pin 22 and ground.
7. The slicing level can be varied by changing the value of R_{17-25}. A higher resistor value results in a larger value of the minimum sync pulse amplitude. The slicing level is independent of the video information.
8. Frequency control is obtained by supplying a correction current to the oscillator RC-network via a resistor, connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the right frequency in one of the two following ways:
   a) Interrupt R_{23-24}.
   b) Short circuit the sync separator bias network (Pin 25) to $+V_{CC}$.
   To avoid the need of a VCR switch, the time constant of phase detector at strong input signal is sufficient short to get a stable picture during VCR playback. During the vertical retrace period, the time constant is even shorter so that the head errors of the VCR are compensated at the beginning of the scan. Only at weak signal conditions (information derived from the AGC circuit) is the time constant increased to obtain a good noise immunity.
9. The flyback input and sandcastle output have been combined on one pin.
   The flyback pulse is clamped to a level of 4.5V. The minimum current to drive the second control loop is 0.1mA.
10. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
11. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60Hz and corrects the vertical amplitude.
12. To avoid screenburn due to a collapse of the vertical deflection, a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
13. Starting point tuner takeover at 1 = 0.2mA. Takeover to be adjusted with a potentiometer of 47kΩ.

FUNCTIONAL DESCRIPTION

IF Amplifier, Demodulator, and AFC

The IF amplifier has a symmetrical input (Pins 8 and 9). The synchronous demodulator and the AFC circuit share an external reference tuned circuit (Pins 20 and 21). An internal RC-network provides the necessary phase-shifting for AFC operation. The AFC circuit is gated by means of an internally generated gating pulse. As a result, the AFC output voltage contains no video information. The AFC circuit provides a control voltage output with a swing greater than 10V from Pin 18.

AGC Circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC circuit connected to Pin 19. The point of tuner take-over is preset by the voltage level at Pin 1.

Video Amplifier

The signal through the video amplifier comprises video and sound information.

Sound Circuit and Horizontal Oscillator Starting Function

The input to the sound IF amplifier is obtained by a band-pass filter coupling from the video output (Pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (5kΩ) between Pin 11 and ground, or by supplying Pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

DC Volume Control/Horizontal Oscillator Start

The circuit can be used with a DC volume control or with a starting possibility of the horizontal oscillator. The operation depends on the application. When during switch-on no current is supplied to Pin 11, this pin will act as volume control. When a current of 6mA is supplied to Pin 11, the volume control is set to a fixed output signal and the IC will generate drive pulses for the horizontal deflection. The main supply of the IC can then be derived from the horizontal deflection.

Horizontal Synchronization

The video input signal (positive video) is connected to Pin 25.

The horizontal synchronization has two control loops. This has been introduced because a sandcastle pulse had to be generated. An accurate timing of the burstkey pulse can be made in an easy way when the oscillator sawtooth is used. Therefore, the phase of this sawtooth must have a fixed relation with respect to the sync pulse. That can only be realized when a second loop is used.

Horizontal Phase Detector

The circuit has the following operating conditions:

a. Strong input signal, synchronized or not synchronized. (The input signal condition is obtained from the AGC-circuit, the in-sync/out-of-sync from the coincidence detector). In this condition the time constant is optimal for VCR playback; i.e., fast time constant during the vertical retrace (to be able to correct head-errors of the VCR) and such a time constant during scan that fluctuations of the sync are corrected. In this condition the phase detector is not gated.

b. Weak signal. In this condition the time constant is doubled compared with the previous condition. Furthermore, the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by the noise in the video signal.

c. Not synchronized (weak signal). In this condition the time constant during scan and vertical retrace are the same as during scan in condition a.

Vertical Sync Pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of only 10μs with a separation of 22μs. This type of vertical sync pulses are generated by certain video tapes with anti-copy guard.

Vertical Ramp Generator

To avoid problems during VCR-playback in the so-called feature modes (fast or slow), the vertical ramp generator is not coupled to the horizontal oscillator when such signals are received. For normal signals the coupling between vertical ramp generator and horizontal oscillator is maintained. This ensures a reliable interface.

Vertical Divider System

The IC embodies a synchronized divider system for generating the vertical sawtooth at Pin 2. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency; one line period equals 2 clock pulses.

Due to the divider system no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60Hz to 50Hz system. When the trigger pulse comes before line 576 the system works in the 60Hz mode, otherwise 50Hz mode is chosen. The divider system operates with 2 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter.

The counter increases its counter value with 1 for each time the separated vertical sync. pulse is within the search window. When it is not, the counter value is lowered with 1.

The different working modes of the divider system are specified below.

a. Large (search) window: divider ratio between 488 and 722.

This mode is valid for the following conditions:

1. Divider is locking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Non-standard TV signal condition detected while a double or enlarged vertical sync pulse is still found after the internally-generated anti-topflutter pulse has ended. This means a vertical sync pulse width larger than 10 clock pulses (50Hz) viz. 12 clock pulses (60Hz).

   In general this mode is activated for video tape recorders operating in the feature trick mode. When the wide vertical sync. pulses are detected, the vertical ramp generator is decoupled from the horizontal oscillator. As a consequence, the retrace time of this ramp generator is now determined by the external capacitor and the discharge current. This decoupling prevents instability of the picture due to irregular incoming signals (variable number of lines per field).

4. Up/down counter value of the divider system operating in the narrow window mode drops below count 6.

b. Narrow window: divider ratio between 522 – 528 (60Hz) or 622 – 628 (50Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is lowered with 1. At a counter value below 6, the divider system switches over the large window mode. The divider system also generates the so-called anti-topflutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The width of this pulse depends on the divider mode. For the divider mode a the start is generated at the reset of the divider. In mode b the anti-topflutter pulse starts at the beginning of the first equalizing pulse.

The anti-topflutter pulse ends at count 10 for 50Hz and count 12 for 60Hz. The vertical

blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse width is 34 (17 lines) for 60Hz and at count 42 (21 lines) for 50Hz systems.

The vertical blanking pulse generated at the sandcastle output Pin 27 is made by adding the anti-topflutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b mode. The total length of the vertical blanking in this condition is 21 lines in the 60Hz mode and 25 lines in the 50Hz mode.

Application When External Video Signals Have to Be Synchronized

The input of the sync separator is externally available. For the normal application, the video output signal (Pin 17) is AC-coupled to this input (see Figure 2). It is possible to interrupt this connection and to drive the sync separator from another source; e.g., a teletext decoder in serial mode or a signal coming from the PT-plug. When a teletext decoder is applied, the IF-amplifier and synchronization circuit are running in the same phase so that the various connections between the two parts (like AGC gating) can remain active. When external signals are applied to the sync separator, the connections between the two parts must be interrupted. This can be obtained by connecting Pin 22 to ground.

This results in the following condition:

- AGC detector is not gated.
- AFC circuit is active.
- Mute circuit not active so that the sound channel remains switched-on.
- The first phase detector has an optimal time constant for external video sources.

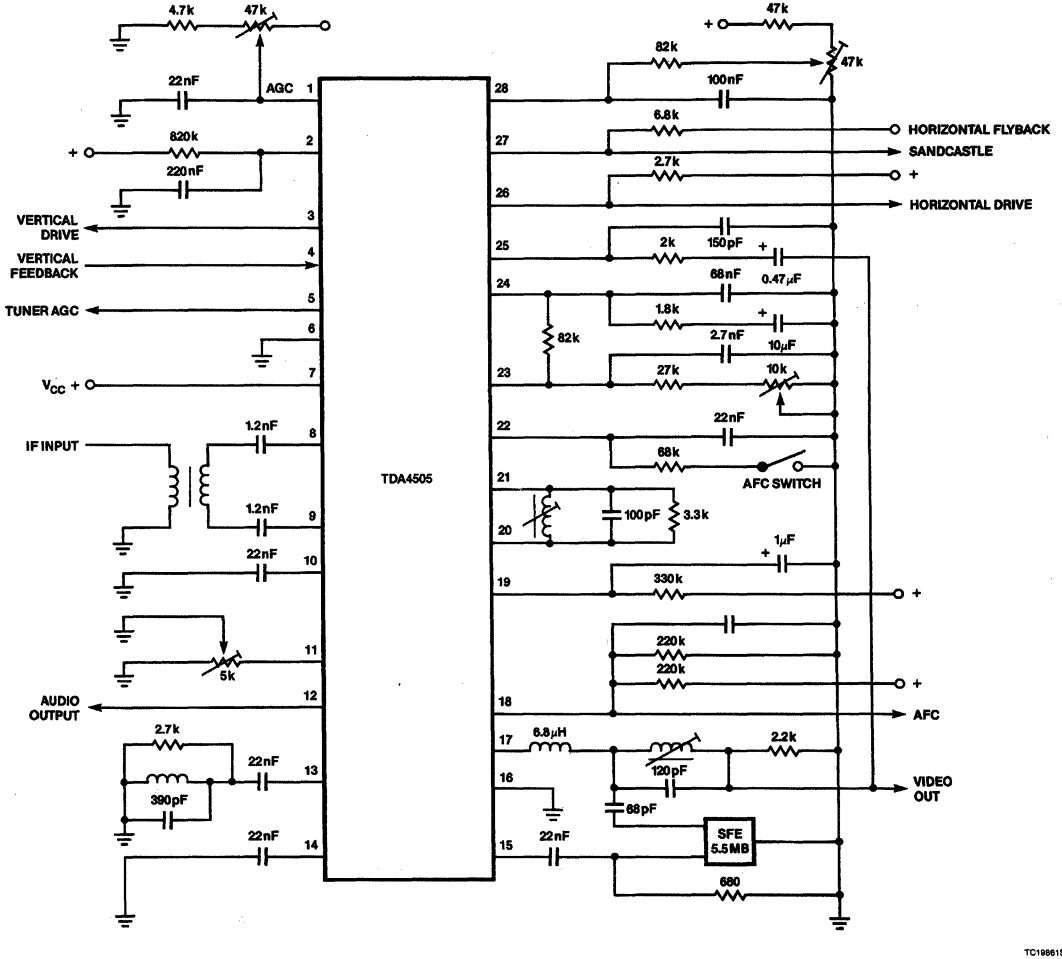


Figure 1. Application Diagram

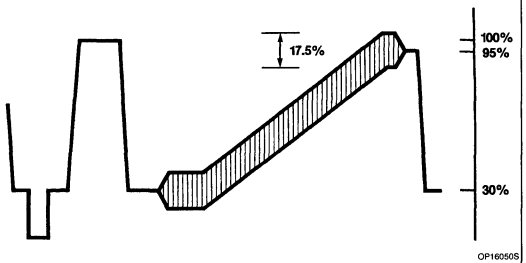


Figure 2. Video Output Signal

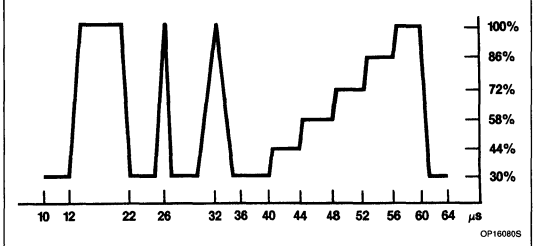
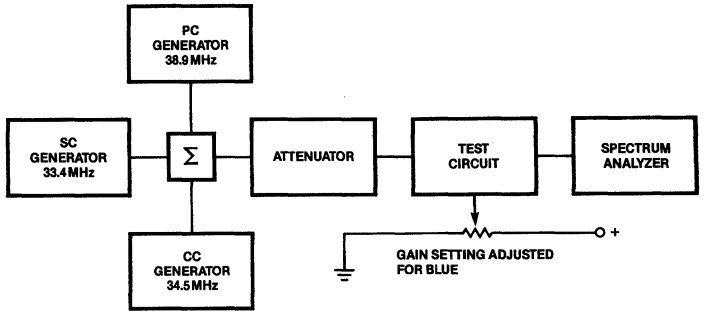


Figure 3. E.B.U. Test Signal Waveform (Line 330)



NOTES:
Value at 1.1MHz; $20\log\frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 1.1MHz} + 3.6dB$.
Value at 3.3MHz; $20\log\frac{V_O \text{ at } 4.4 \text{ MHz}}{V_O \text{ at } 3.3MHz}$.

Figure 4. Test Setup Intermodulation

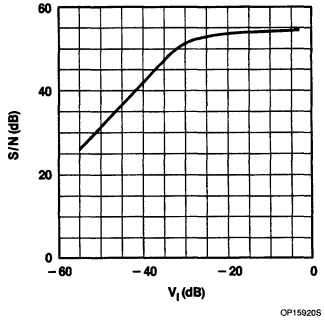


Figure 5. S/N Ratio as a Function of the Input Voltage

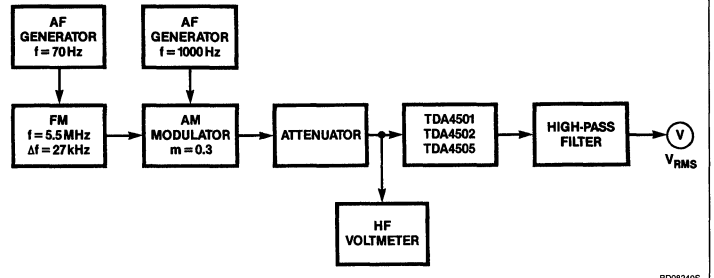


Figure 6. Test Setup AM Suppression

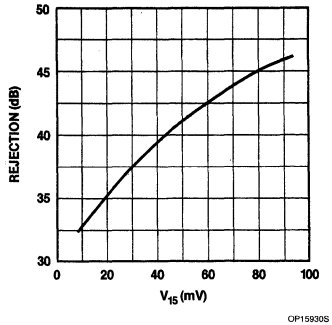


Figure 7. AM Rejection

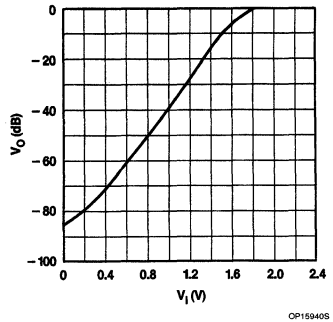


Figure 8. Volume Control Characteristics

Signetics

Linear Products

Section 7
Video/IF

INDEX

Signetics

TDA2540
Video IF/AFT

Product Specification

Linear Products

DESCRIPTION

The TDA2540 is an IF amplifier and demodulator circuit for color and black-and-white television receivers using NPN tuners.

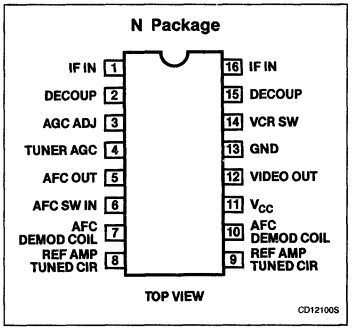
FEATURES

- **Gain-controlled, wide-band amplifier, providing complete IF gain**
- **Synchronous demodulator**
- **White spot inverter**
- **Video preamplifier with noise protection**
- **AFC circuit which can be switched on/off by a DC level, e.g., during tuning**
- **AGC circuit with noise gating**
- **Tuner AGC output (NPN tuners)**
- **VCR switch, which switches off the video output; e.g., for insertion of a VCR playback signal**

APPLICATIONS

- **Black/white and color TV receivers/monitors**
- **Video cassette recorders (VCRs)**
- **CATV converters**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−25°C to +60°C	TDA2540N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{11-13}	Supply voltage	13.2	V
V_{4-13}	Tuner AGC voltage	12	V
P_{TOT}	Total power dissipation	900	mW
T_{STG}	Storage temperature range	−65 to +125	°C
T_A	Operating ambient temperature range	−25 to +60	°C

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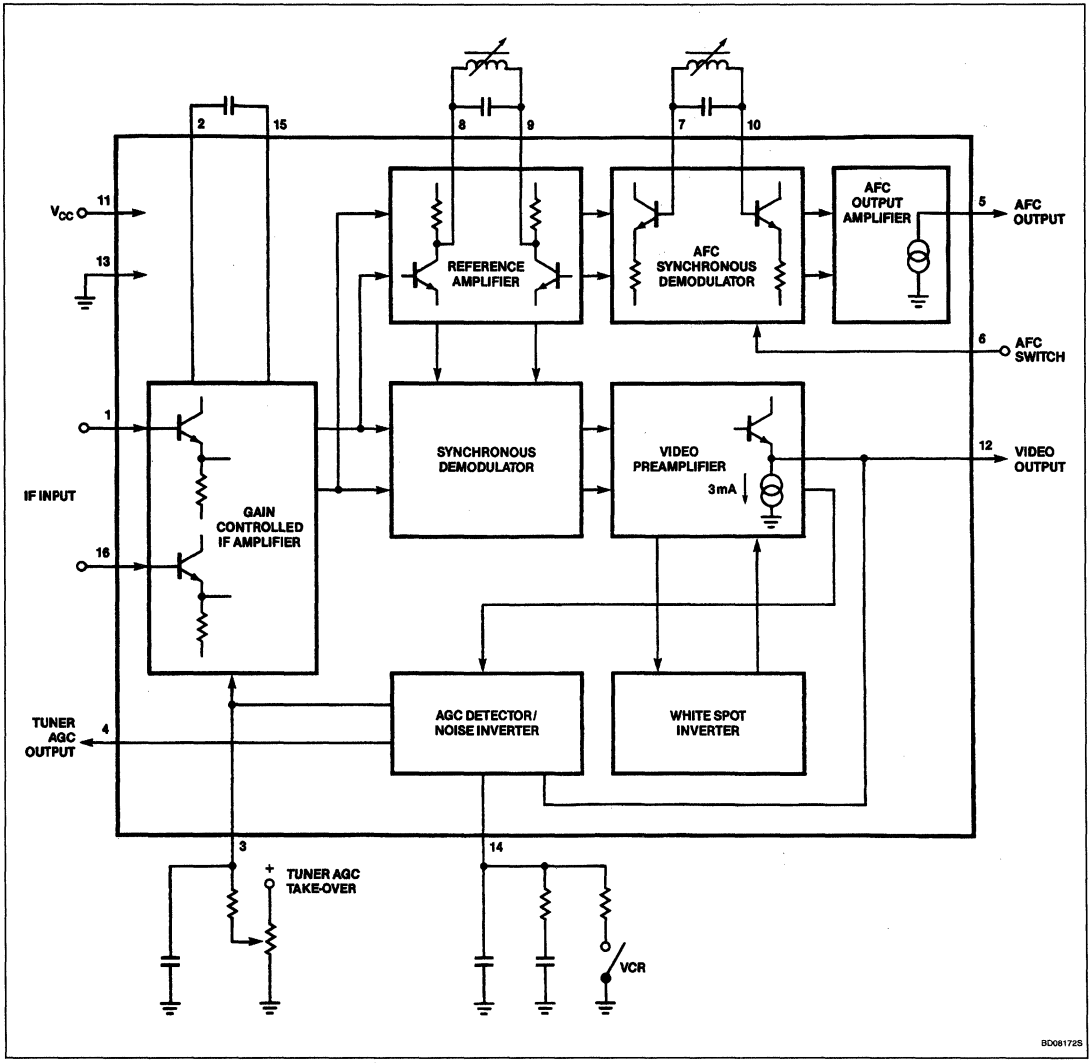
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Measured in Figure 4) The following characteristics are measured at $T_A = 25°C$; $V_{11-13} = 12V$; $f = 38.9MHz$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{11-13}	Supply voltage range	10.2	12	13.2	V
$V_{1-16(RMS)}$	IF input voltage for onset of AGC (RMS value)		100	150	μV
$\lvert Z_{1-16}\rvert$	Differential input impedance $C_L = 2pF$		2		kΩ
V_{12-13}	Zero-signal output level		6± 0.3		V[1]
V_{12-13}	Top sync output level	2.9	3.07	3.2	V
G_V	IF voltage gain control range		64		dB
BW	Bandwidth of video amplifier (3dB)		6		MHz
S/N	Signal-to-noise ratio at $V_I = 10mV$		58		dB[2]
dG	Differential gain		4	10	%
dφ	Differential phase[1]		2	10	degrees
	Intermodulation at 1.1MHz: blue[3] yellow[3] at 3.3MHz[4]	46 46 46	60 50 54		dB dB dB
	Carrier signal at video output		4	30	mV
	2nd harmonic of carrier at video output		20	30	mV
	White spot inverter threshold level (Figure 3)		6.6		V
	White spot insertion level (Figure 3)		4.7		V
	Noise inverter threshold level (Figure 3)		1.8		V
	Noise insertion level (Figure 3)		3.8		V
V_{14-13}	External video switch (VCR) switches off the output			1.1	V
I_4	Tuner AGC output current range	10		0	mA
V_{4-13}	Tuner AGC output voltage at $I_4 = 10mA$			0.3	V
I_4	Tuner AGC output leakage current $V_{14-13} = 5V$; $V_{4-13} = 12V$			15	μA
ΔV_{5-13}	Maximum AFC output voltage swing	10	11		V
Δf	Detuning for AFC output voltage swing of 10V		 100	100 200	kHz kHz
V_{5-13}	AFC zero-signal output voltage (minimum gain)	4	6	8	V
V_{6-13}	AFC switches on at:	3.2		3	V
V_{6-13}	AFC switches off at:			1.5	V

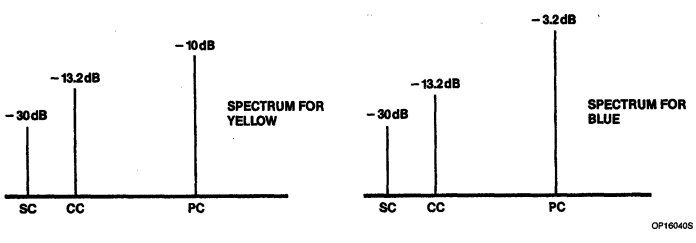
NOTES:

1. So-called 'projected zero point', e.g., with switched demodulator.

2. $S/N = \frac{V_O \text{ black-to-white}}{V_{N(RMS)} \text{at } B = 5MHz}$

3. $20\log \frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 1.1MHz} + 3.6dB.$

4. $20\log \frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 3.3MHz}.$



NOTES:
SC: Sound carrier level
CC: Chrominance carrier
PC: Picture carrier level

} With respect to top sync level

Figure 1. Input Conditions for Intermodulation Measurements; Standard Color Bar With 75% Contrast

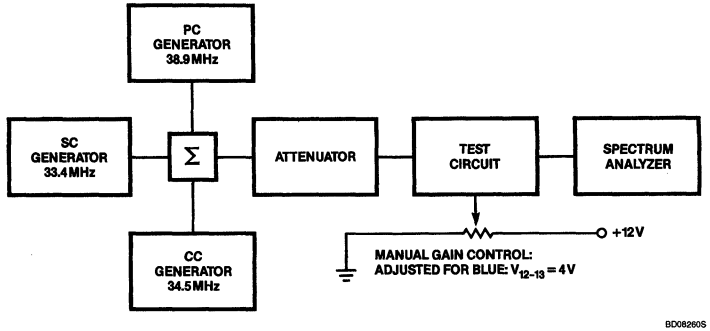


Figure 2. Test Setup for Intermodulation

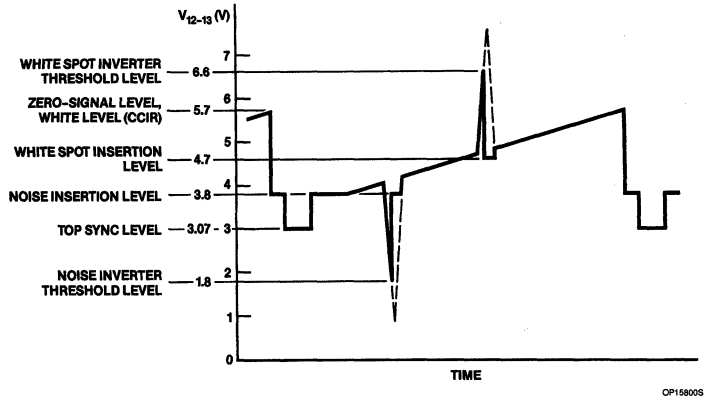
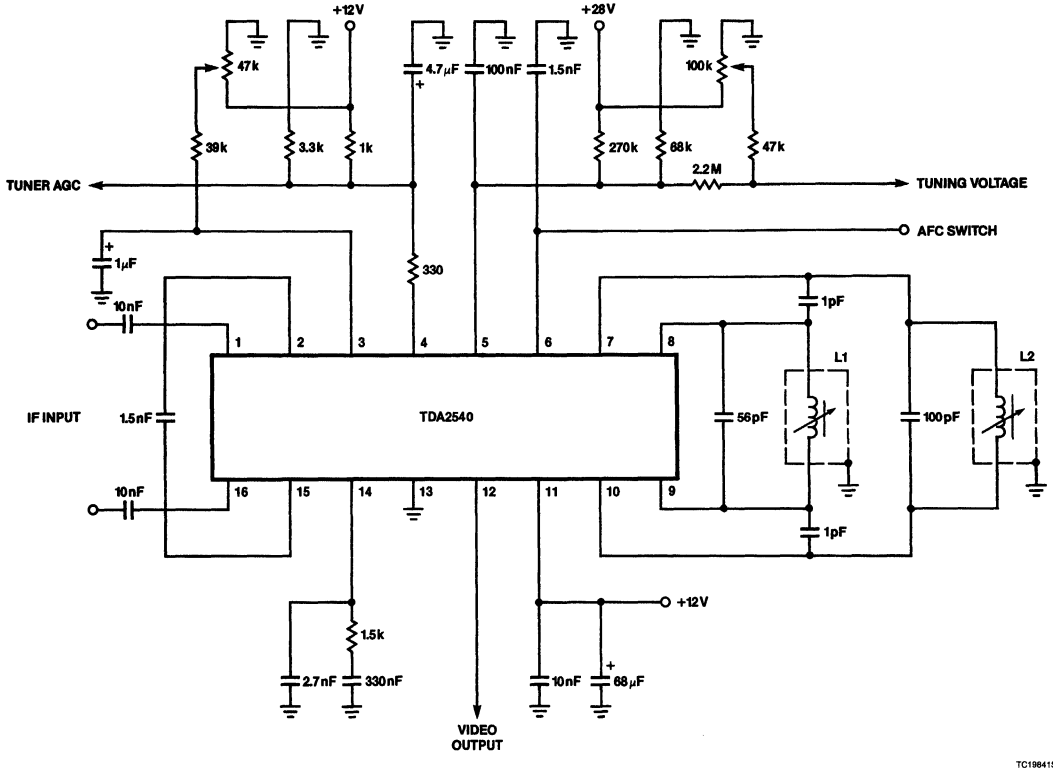


Figure 3. Video Output Waveform Showing White Spot and Noise Inverter Threshold Levels



NOTES:
Q of L1 and L2 ≈ 80; f = 38.9MHz

Figure 4. Typical Application Circuit Diagram

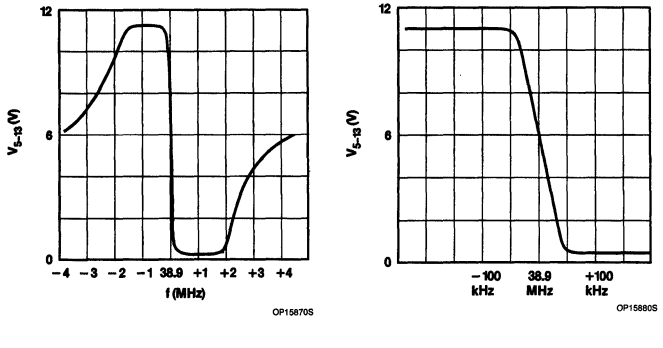


Figure 5. AFC Output Voltage (V_{5-13}) as a Function of the Frequency

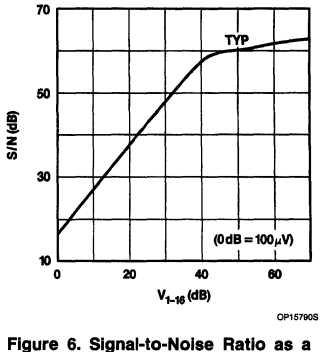


Figure 6. Signal-to-Noise Ratio as a Function of the Input Voltage (V_{1-16})

Signetics

TDA2541
Video IF/AFT

Product Specification

Linear Products

DESCRIPTION

The TDA2541 is an IF amplifier and demodulator circuit for color and black-and-white television receivers using PNP tuners.

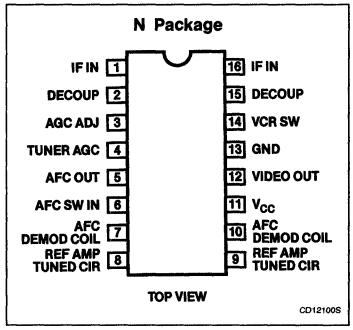
FEATURES

- **Gain-controlled wide-band amplifier, providing complete IF gain**
- **Synchronous demodulator**
- **White spot inverter**
- **Video preamplifier with noise protection**
- **AFC circuit which can be switched on/off by a DC level, e.g., during tuning**
- **AGC circuit with noise gating**
- **Tuner AGC output (PNP tuners)**
- **VCR switch, which switches off the video output; e.g., for insertion of a VCR playback signal**

APPLICATIONS

- **Black/white and color TV receivers**
- **Video cassette recorders (VCRs)**
- **CATV converters**

PIN CONFIGURATION



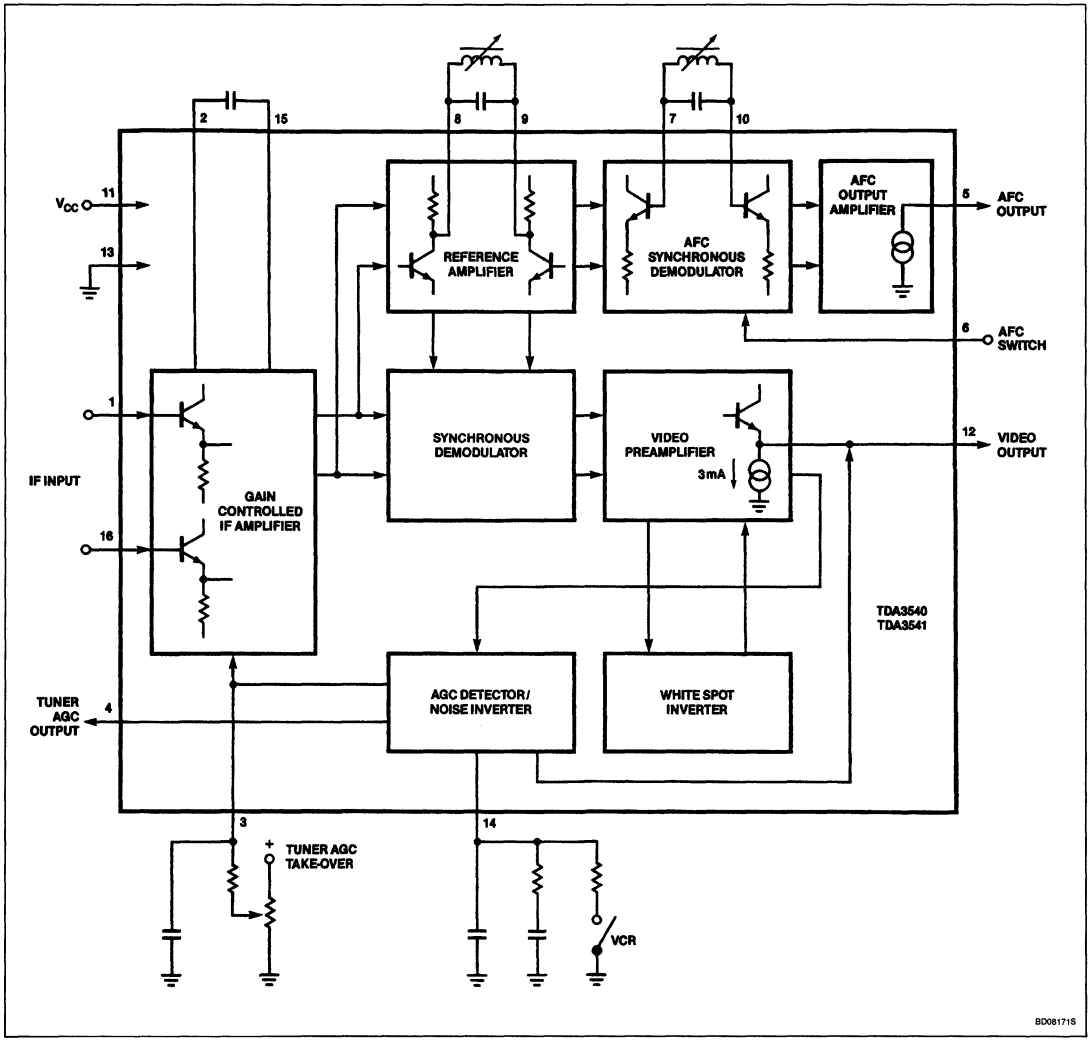
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−25°C to +60°C	TDA2541N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	13.2	V
V_{4-13}	Tuner AGC voltage	12	V
P_{TOT}	Total power dissipation	900	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +60	°C

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS (Measured in Figure 4) $T_A = 25°C$; $V_{11-13} = 12V$; f = 38.9MHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	10.2	12.0	13.2	V
$V_{1-16(RMS)}$	IF input voltage for onset of AGC (RMS value)		100	150	μV
$\|Z_{1-16}\|$	Differential input impedance $C_{L\ 2PF}$		2		kΩ
V_{12-13}	Zero-signal output level		6 ± 0.3		V[1]
V_{12-13}	Top sync output level	2.9	3.07	3.2	V
A_V	IF voltage gain control range		64		dB
BW	Bandwidth of video amplifier (3dB)		6		MHz
S/N	Signal-to-noise ratio at $V_I = 10mV$		58		dB[2]
dG	Differential gain		4 10		% %
dφ	Differential phase		2 10		
	Intermodulation at 1.1MHz: blue[1] yellow[1] at 3.3MHz[2]	46 46 46	60 50 54		dB dB dB
	Carrier signal at video output		4	30	mV
	2nd harmonic of carrier at video output		20	30	mV
	White spot inverter threshold level (Figure 3)		6.6		V
	White spot insertion level (Figure 3)		4.7		V
	Noise inverter threshold level (Figure 3)		1.8		V
	Noise insertion level (Figure 3)		3.8		V
V_{14-13}	External video switch (VCR) switches off the output at:			1.1	V
I_4	Tuner AGC output current range	0		10	mA
V_{4-13}	Tuner AGC output voltage at $I_4 = 10mA$			0.3	V
I_4	Tuner AGC output leakage current $V_{14-13} = 11V$; $V_{4-13} = 12V$			15	μA
ΔV_{5-13}	Maximum AFC output voltage swing	10	11		V
Δf	Detuning for AFC output voltage swing of 10V		100	200	kHz
V_{5-13}	AFC zero-signal output voltage (minimum gain)	4	6	8	V
V_{6-13}	AFC switches on at:	3.2			
V_{6-13}	AFC switches off at:			1.5	V

NOTES:

1. So-called 'projected zero point', e.g., with switched demodulator.
2. $S/N = \frac{V_O \text{ black-to-white}}{V_{N(RMS)} \text{ at } B = 5MHz}$.

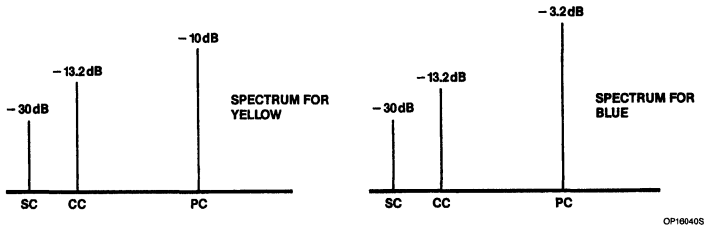
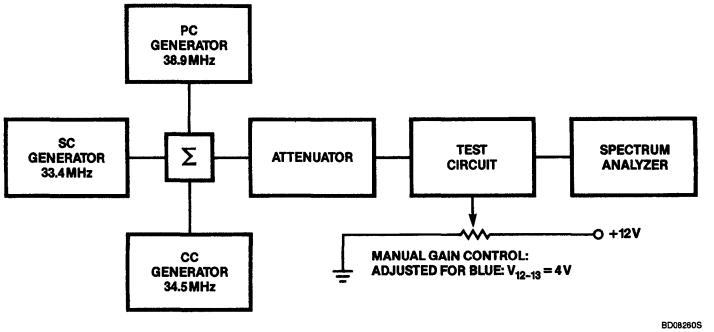


Figure 1. Input Conditions for Intermodulation Measurements; Standard Color Bar With 75% Contrast



NOTES:

1. $20 \log \frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 1.1MHz} + 3.6dB$

2. $20 \log \frac{V_O \text{ at } 4.4MHz}{V_O \text{ at } 3.3MHz}$

Figure 2. Test Setup for Intermodulation

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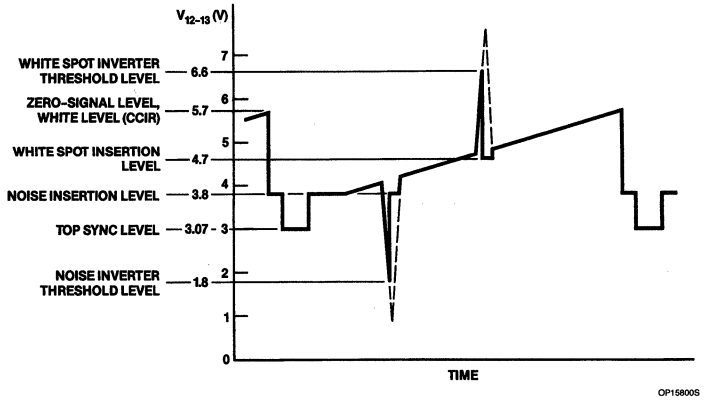

Figure 3. Video Output Waveform Showing White Spot and Noise Inverter Threshold Levels

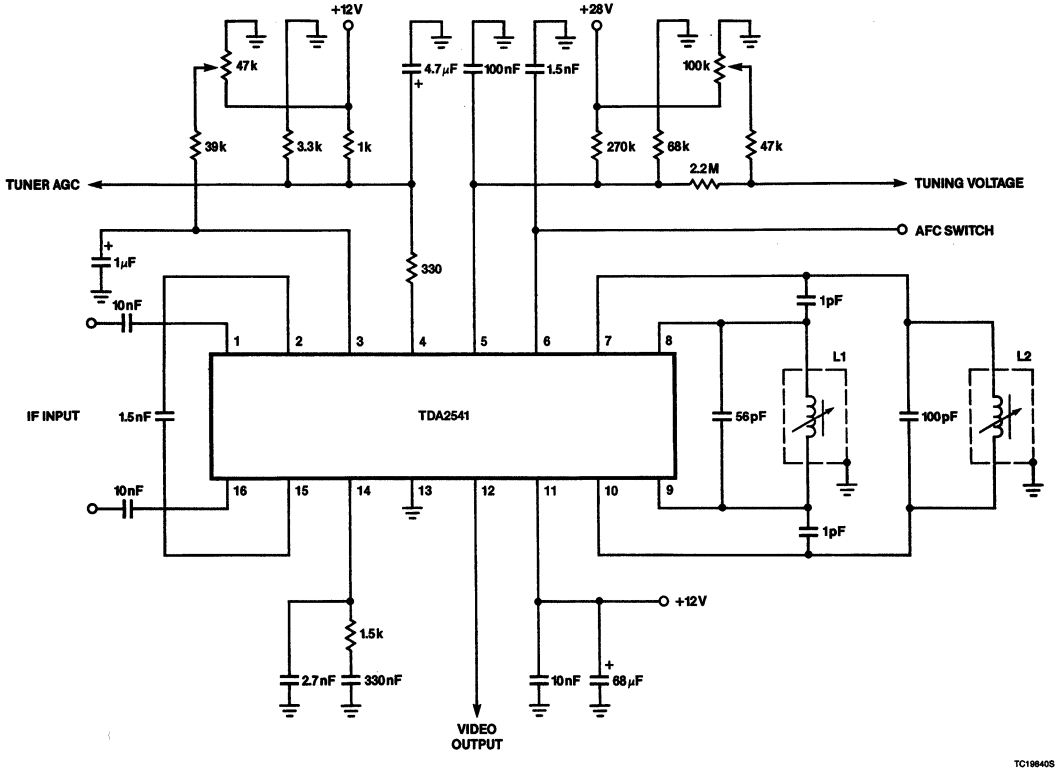

Figure 4. Typical Application Circuit Diagram; Q of L1 and L2 ≈ 80; f_O = 38.9MHz

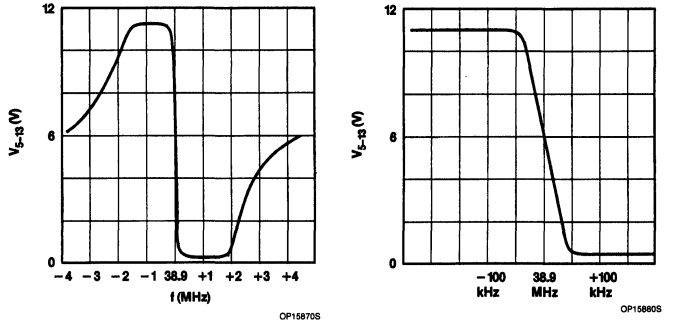

Figure 5. AFC Output Voltage (V_{5-13}) as a Function of the Frequency

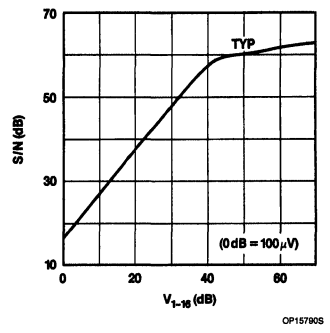

Figure 6. Signal-to-Noise Ratio as a Function of the Input Voltage (V_{1-16})

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Signetics

TDA2549
Multistandard Video IF/Demodulator

Product Specification

Linear Products

DESCRIPTION

The TDA2549 is a complete IF circuit with AFC, AGC, demodulation, and video preamplification facilities for multistandard television receivers. It is capable of handling positively and negatively modulated video signals in both color and black/white receivers.

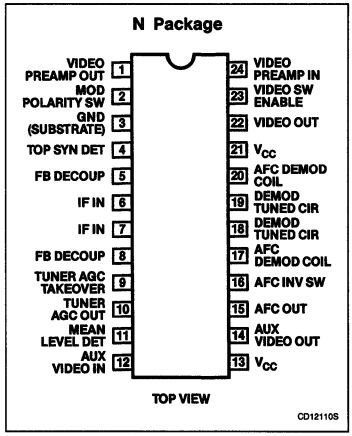
FEATURES

- **Gain-controlled wide-band amplifier providing complete IF gain**
- **Synchronous demodulator for positive and negative modulation**
- **Video preamplifier with noise protection for negative modulation**
- **Auxiliary video input and output (75Ω)**
- **Video switch to select between auxiliary video input signal and demodulated video signal**
- **AFC circuit with on/off switch and inverter switch**
- **AGC circuit for positive modulation (mean level) and negative modulation (noise gate)**
- **AGC output for controlling MOSFET tuners**

APPLICATIONS

- **NTSC/PAL/SECAM TV receiver/monitors**
- **Multistandard VCR**
- **CATV converters**

PIN CONFIGURATION



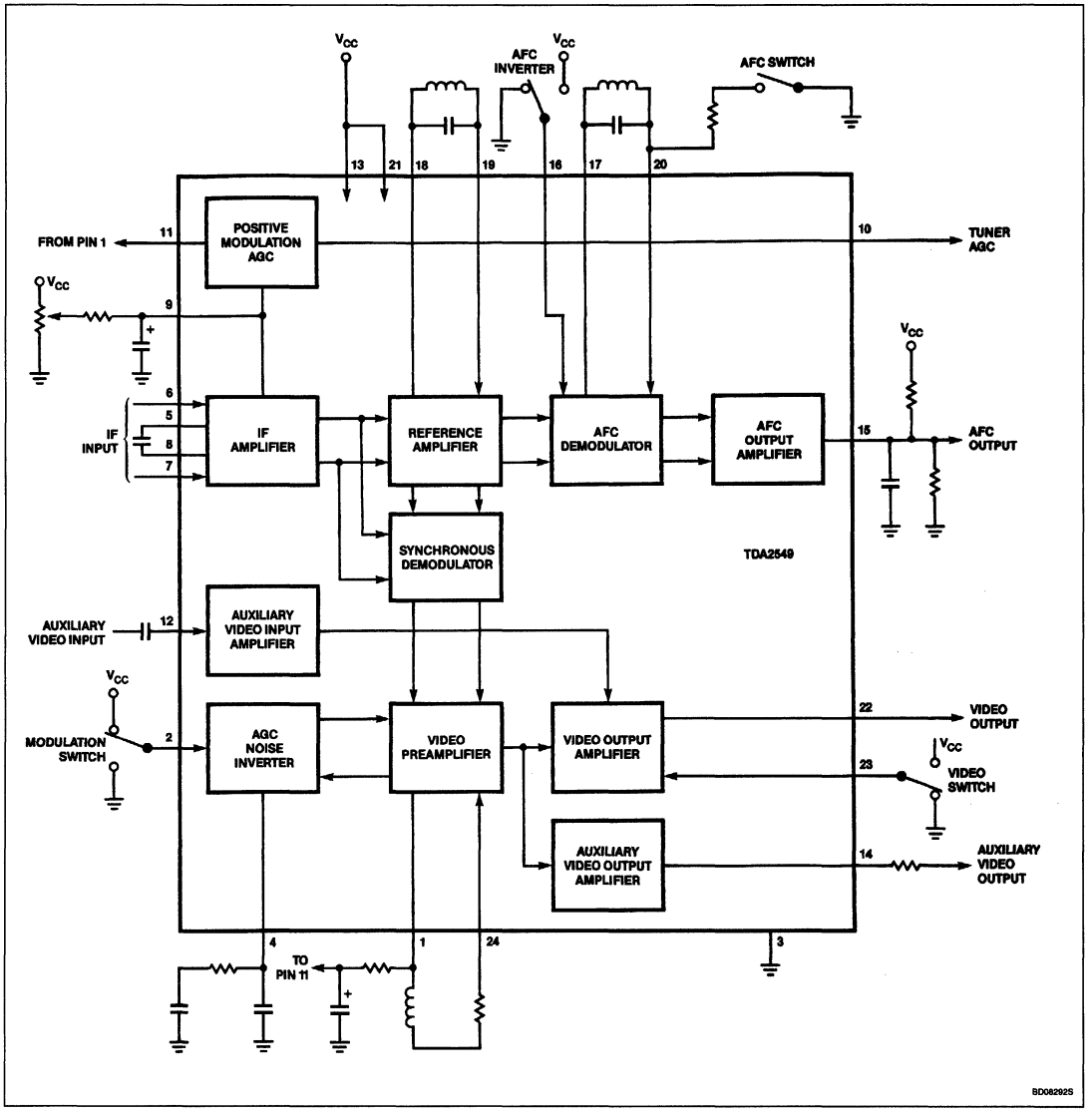
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−25°C to +70°C	TDA2549N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage (Pins 13 and 21)	13.8	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (Measured in Figure 4) V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	10.8	12	13.2	V
I_{CC}	Supply current (Pins 13 and 21)		82		mA
$V_I = V_{6-7}$	IF input signal for V_O = 2V (between Pins 6 and 7)		50	150	μV
$\|Z_{6-7}\|$	Input impedance (differential)		2		kΩ
C_{6-7}	Input capacitance (differential)		2		pF
	Zero signal output level				
V_{22-3}	Positive modulation	1.6	2	2.3	V
V_{22-3}	Negative modulation	3.7	4	4.3	V
V_{22-3}	Top sync output level	1.7	2	2.3	V
A_V	Gain control range	50	74		dB
S/N	Signal-to-noise ratio at V_I = 10mV[1]	50	57		dB
$V_{23-3(P-P)}$	Maximum video output amplitude for positive modulation (peak-to-peak value)	4.5			V
BW	Bandwidth of video amplifier (3dB)		5.5		MHz
dG	Differential gain at V_O = 2V		4	10	%
dφ	Differential phase at V_O = 2V		2	10	%
$V_{24-3(RMS)}$	Residual carrier signal (RMS value)		10	20	mV
$V_{24-3(RMS)}$	Residual second harmonic of carrier signal (RMS value)		20	60	mV
V_{15-3}	AFC output voltage swing	10			V
Δf	Change of frequency required for AFC output voltage swing of 10V		70	200	kHz
V_{17-3}	AFC switch off for a voltage lower than:			1.5	V
	AFC inverter switch				
V_{16-3}	positive AFC (Figure 1)	0		1.5	V
V_{16-3}	negative AFC (Figure 2)	4		12	V
Tuner AGC					
I_{10}	Leakage current			15	μA
	Saturation voltage				
V_{10-3}	I_{10} = 0.3mA		0.1	0.3	V
V_I	take-over point Low			3	mV
V_I	take-over point High	10			mV
ΔV_{22-3}	Signal expansion at A_V = 50dB			0.5	dB
	Negative modulation (Figure 3)				
V_{22-3}	white spot inverter threshold level		4.6		V
V_{22-3}	white spot insertion level		3.2		V
V_{22-3}	noise inverter threshold level		0.9		V
V_{22-3}	noise insertion level		2.5		V
V_{11-3}	Positive modulation AGC detector reference level	3.0	3.2	3.4	V
V_{12-3}	Auxiliary video input signal for $V_{O(P-P)}$ = 2V	0.7	1	1.4	V
	Auxiliary video output				
V_{14-3}	output signal[2]		1		V
V_{14-3}	top sync level	1	2	3	V
$\|Z_{14-3}\|$	output impedance		7		Ω

DC ELECTRICAL CHARACTERISTICS (Continued)

(Measured in Figure 4) V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Levels for video switches				
V_{2-3}	positive video			1	V
V_{2-3}	negative video	3			V
V_{23-3}	internally demodulated signal			1	V
V_{23-3}	auxiliary video signal	3			V

NOTES:

1. Signal-to-noise ratio $S/N = \frac{V_O \text{ black-to-white}}{V_{N(RMS)} \text{ at } B = 5MHz}$.
2. Measured in application of Figure 4.

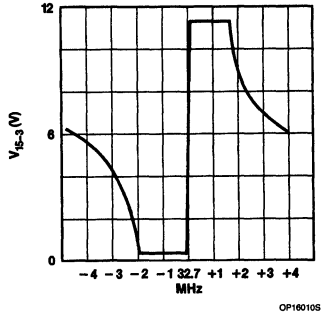


Figure 1. AFC Output Voltage V_{15-3} for Positive AFC

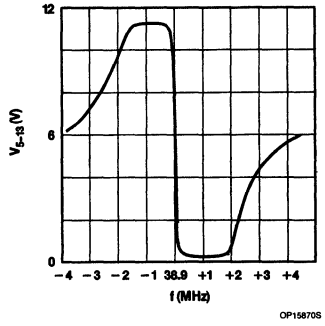


Figure 2. AFC Output Voltage V_{15-3} for Negative AFC

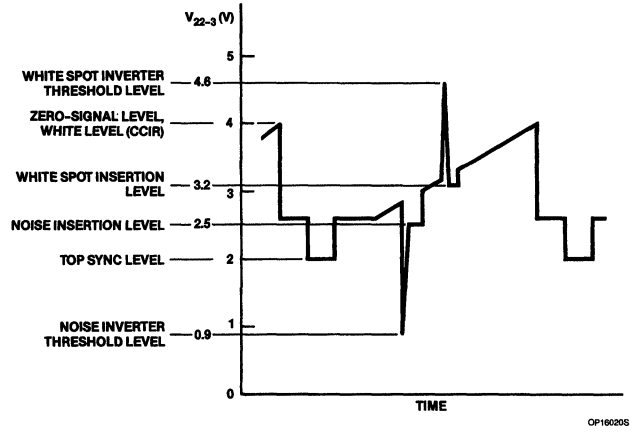


Figure 3. Video Output Waveform Showing White Spot and Noise Inverter Threshold Levels

APPLICATION INFORMATION

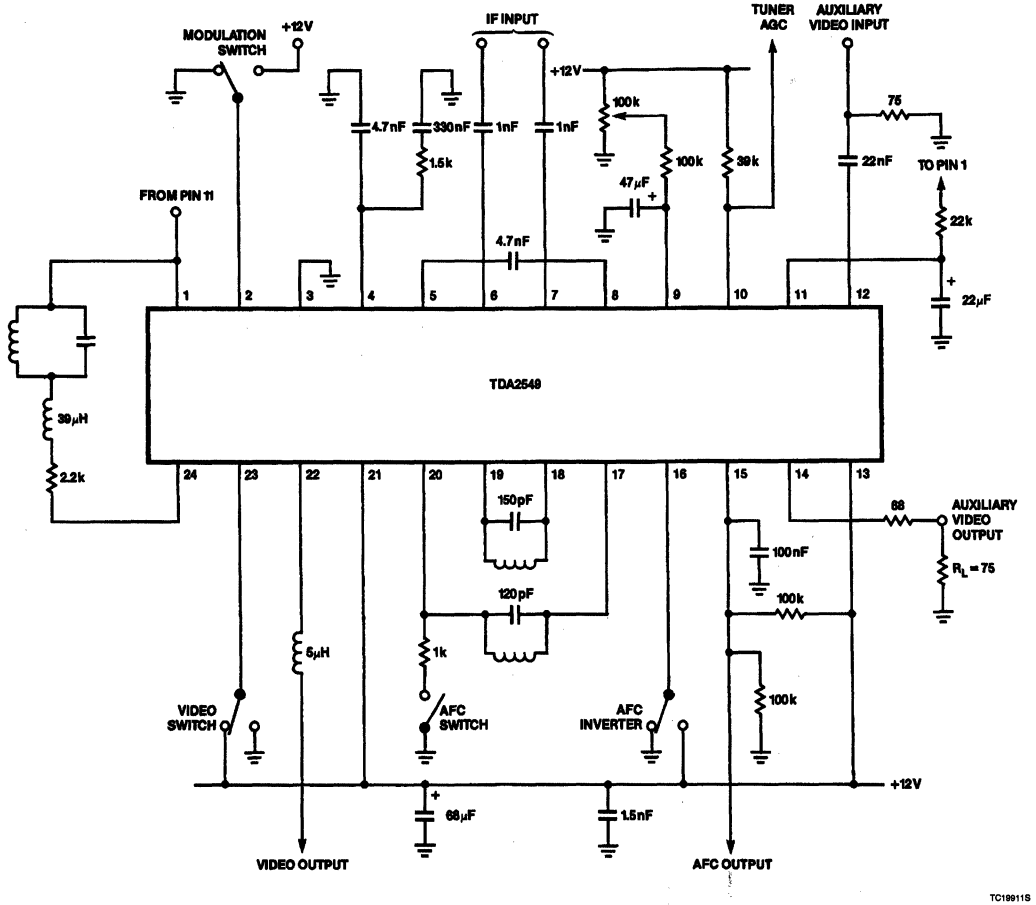


Figure 4. Application Diagram

Signetics

Linear Products

Section 8
Sound IF and Special Audio Decoding

INDEX

TBA120U
Sound IF Amplifier/ Demodulator for TV

Product Specification

DESCRIPTION

The TBA120U is an IF amplifier with a symmetrical FM demodulator and an AF amplifier with adjustable output voltage. The AF amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC circuits, but the input can also be used with a ceramic filter.

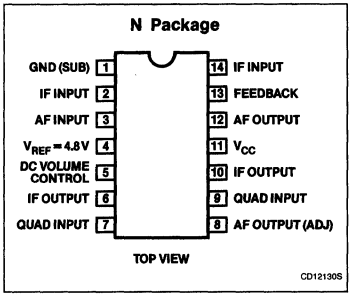
FEATURES

- **Outstanding limiting**
- **AF Input**
- **Few external components**
- **DC volume control**

APPLICATIONS

- **Black/white and color TV receivers**
- **Video cassette recorders (VCRs)**
- **CATV converters**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP (SOT-27K)	0 to +70°C	TBA120UN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{11-1}$	Power voltage (Pin 11)	18	V[1]
V_{5-1}	Adjustment voltage (Pin 5)	6	V
P_{TOT}	Total power dissipation	400	mW
R_{13-14}	Bypass resistance	1	kΩ
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−15 to +70	°C

NOTE:
1. Supply voltage operating range is 10 to 18V.

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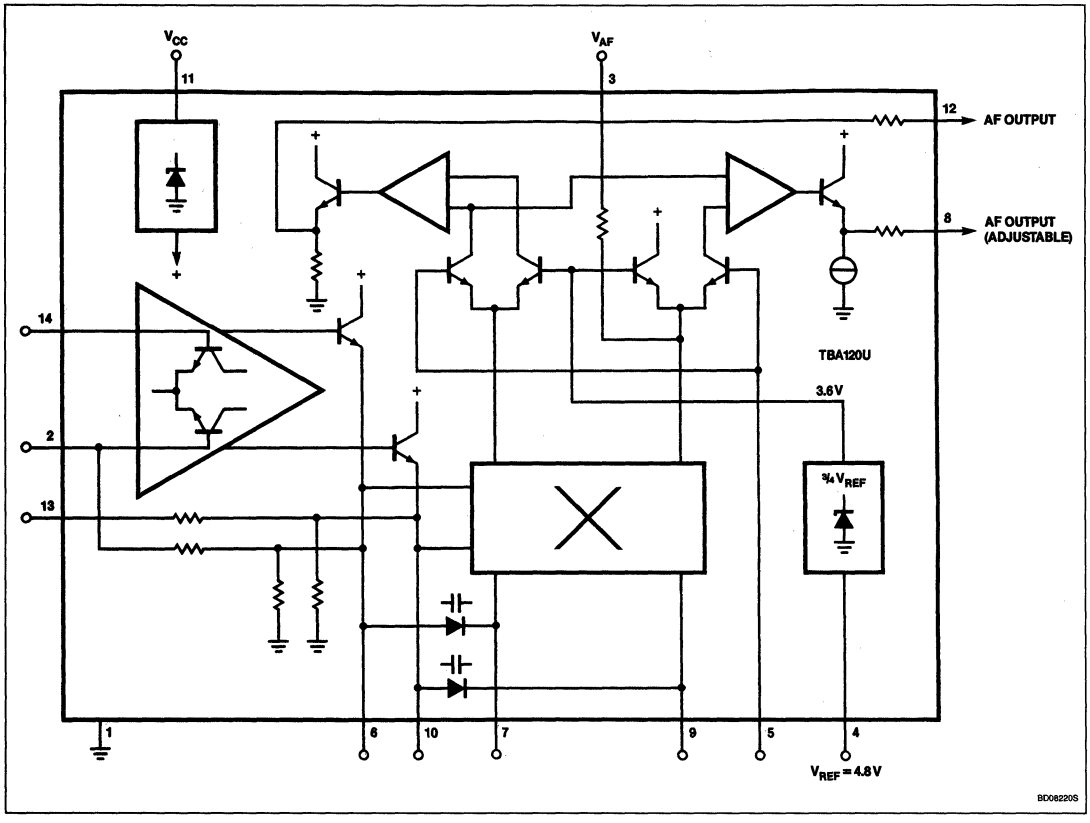
Sound IF Amplifier/Demodulator for TV TBA120U

BLOCK DIAGRAM

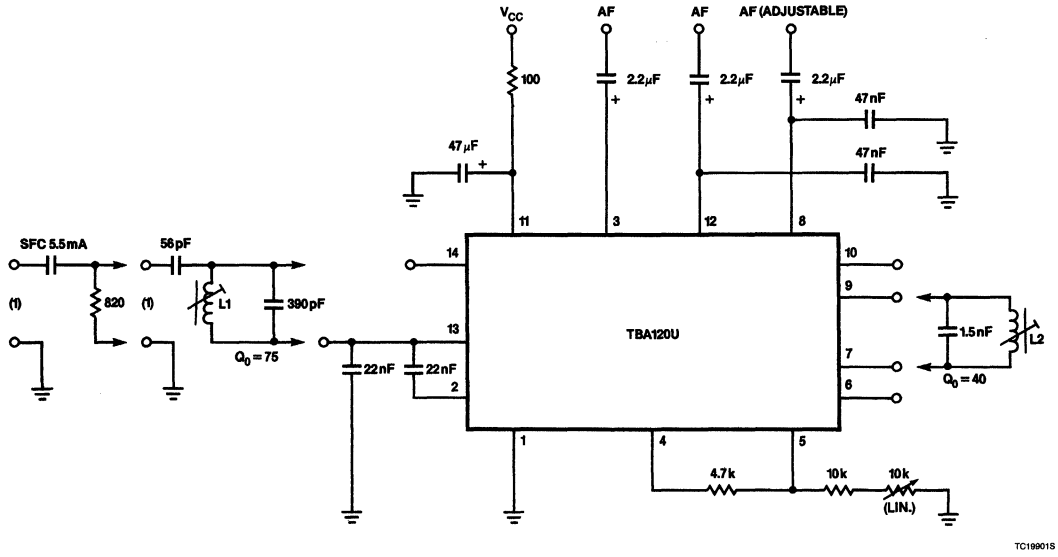


DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; T_A = 25°C; f = 5.5MHz, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$A_{V\ IF\ 6-14}$	IF voltage gain		68		dB
V_I	Input voltage starting limiting at $\Delta f = \pm$ 50kHz; f_M = 1kHz		30	60	μV
$V_{O\ IF\ (P-P)}$	IF output voltage at limiting (peak-to-peak value)		250		mV
α	AM suppression at $\Delta f = \pm$ 50kHz; V_I = 500μV; f_M = 1kHz; m = 30%	50	60		dB
	IF residual voltage without de-emphasis				
V_{IF12}	at Pin 12		30		mV
V_{IF8}	at Pin 8		20		mV
$A_{V\ AF8-3}$	AF voltage gain		7.5		
$\Delta V_{O\ AF}$	AF adjustment at R_{4-5} = 5kΩ; R_{5-1} = 13kΩ	20	28	36	dB
$\Delta V_{O\ AF}$	AF output voltage control range	70	85		dB
R_{4-5}	Adjustment resistor[1]		1 to 10		kΩ
	DC voltage portion at the AF outputs				
V_{12-1}	Pin 12		5.6		V
V_{8-1}	Pin 8		4.0		V
	Output resistance of the AF outputs				
$R_{O\ 12-1}$	Pin 12		1.1		kΩ
$R_{O\ 8-1}$	Pin 8		1.1		kΩ
$R_{I\ 3-1}$	Input resistance of the AF input		2		kΩ
$V_{4-1} = V_{REF}$	Stabilized reference voltage	4.2	4.8	5.3	V
R_{4-1}	Source resistance of reference voltage source		12		Ω
	Ripple rejection				
V_{12}/V_{11}	at Pin 12		30		dB
V_8/V_{11}	at Pin 8		35		dB
$I_{CC} = I_{11}$	Supply current (Pin 11)	9.5	13.5	17.5	mA
$\lvert Z_I \rvert$	IF input impedance				
	C_L 4.5pF		40		kΩ
	C_L 6.0pF	15			kΩ
	AF output voltage at $\Delta f = \pm$ 50kHz; f_M = 1kHz; V_I = 10mV; Q_O = 45; RMS value				
$V_{O\ AF\ (RMS)}$	at Pin 12		1.0		V
$V_{O\ AF\ (RMS)}$	at Pin 8		1.2		V
d_{TOT}	Distortion at $\Delta f = \pm$ 50kHz; f_M = 1kHz; V_I = 10mV; Q_O = 20		1		%

NOTE:
1. Pin 5 must be connected to Pin 4, when volume control adjustment is not applicable.

Sound IF Amplifier/Demodulator for TV TBA120U



NOTE:
1. Either one of these circuits may be used.

Figure 1. Application Example Using TBA120U

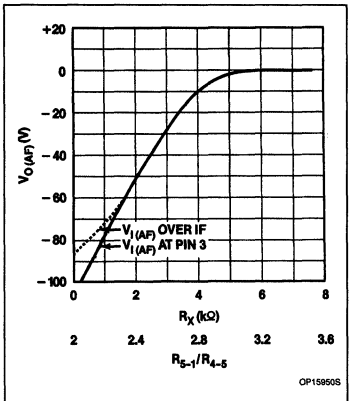


Figure 2. The AF Output Voltage at Pin 8 as a Function of the Resistance Values as Shown in Figure 3

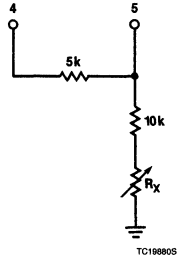
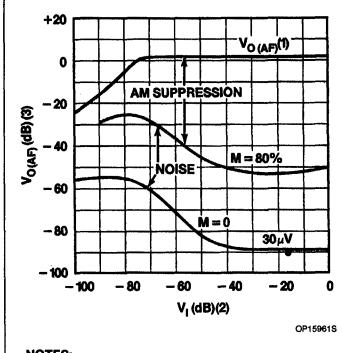
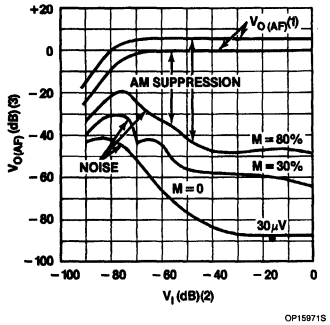


Figure 3. Resistor Conditions for Curves in Figure 2



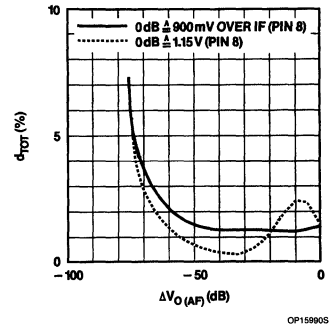
NOTES:
1. $V_{O\ AF}$ with de-emphasis at $\Delta f = \pm 50$kHz; f_M = 1kHz; d_{TOT} = 1.5%; 0dB ≈ 770mV.
2. V_I: 0dB ≈ 200mV at 60Ω

Figure 4. The AF Output Voltage at Pin 8 as a Function of the Input Voltage With SFC 5.5mA at the Input (see Figure 1)



NOTES:
1. $V_{O\ AF}$ with de-emphasis at f_m = 1kHz; 0dB ≈ 770mV;
   curve a: Δf = ± 50kHz; d_{TOT} = 3%;
   curve b: Δf = ± 25kHz; d_{TOT} = 1%.
2. V_I: 0dB ≈ 200mV at Pin 14.

Figure 5. The AF Output Voltage at Pin 8 as a Function of the Input Voltage With Broadband Input (60Ω)



NOTES:
——— 0dB ≈ 900mV over IF (Pin 8)
- - - - 0dB ≈ 1.15V (Pin 8)

Figure 7. Total Distortion as a Function of the AF Output Voltage Change

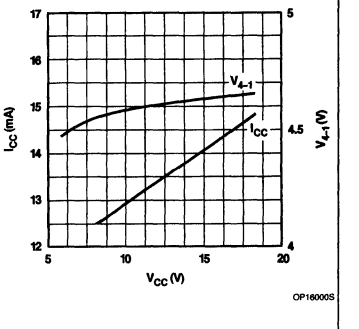


Figure 8. Supply Current and the Reference Voltage at Pin 4 as a Function of Supply Voltage

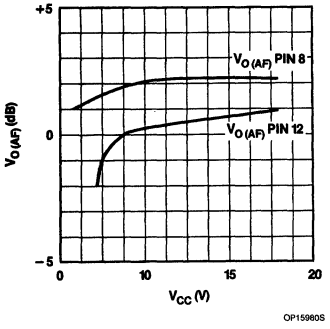


Figure 6. The AF Output Voltage at Pins 8 and 12 as a Function of the Supply Voltage; 0dB ≈ 770mV

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Signetics

TDA2545A
Quasi-Split-Sound Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

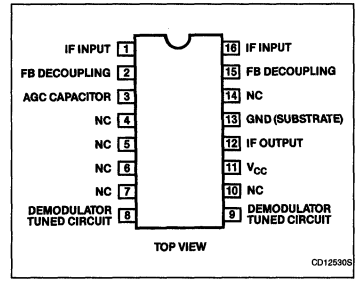
FEATURES

- **3-stage gain-controlled IF amplifier**
- **AGC circuit**
- **Reference amplifier and limiter amplifier for vision carrier processing**
- **Linear multiplier for quadrature demodulation**

APPLICATIONS

- **Stereo MTS television receiver**
- **Video cassette recorder with MTS**
- **CATV converters**

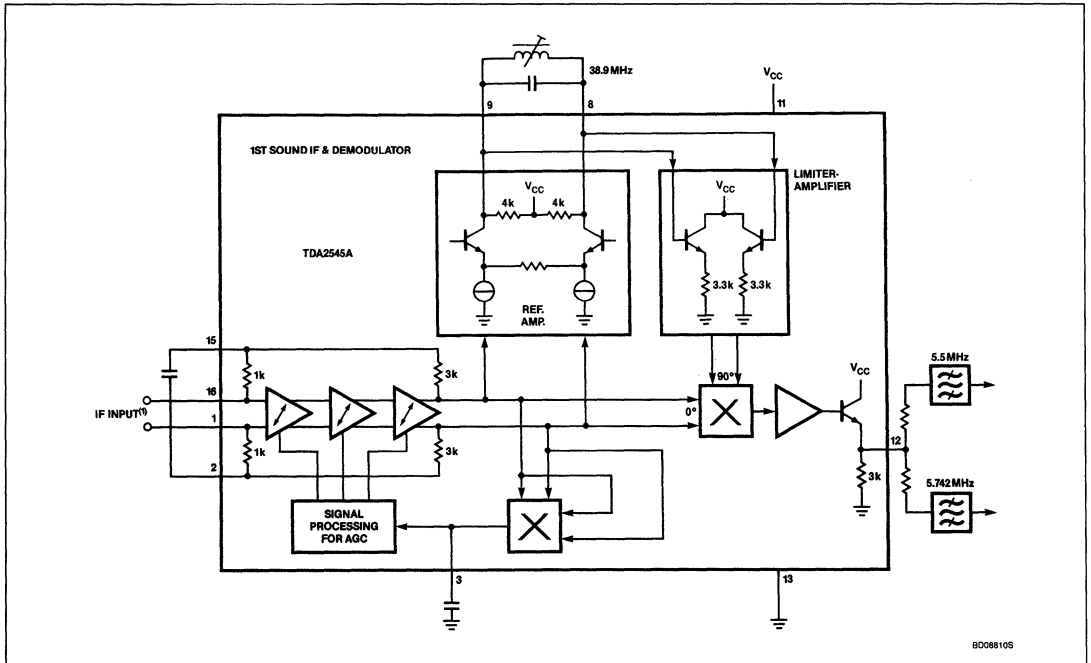
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to +70°C	TDA2545AN

BLOCK DIAGRAM



NOTE:
1. IF signal: vision carrier (VC) and sound carrier (SC).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 11)	13.2	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

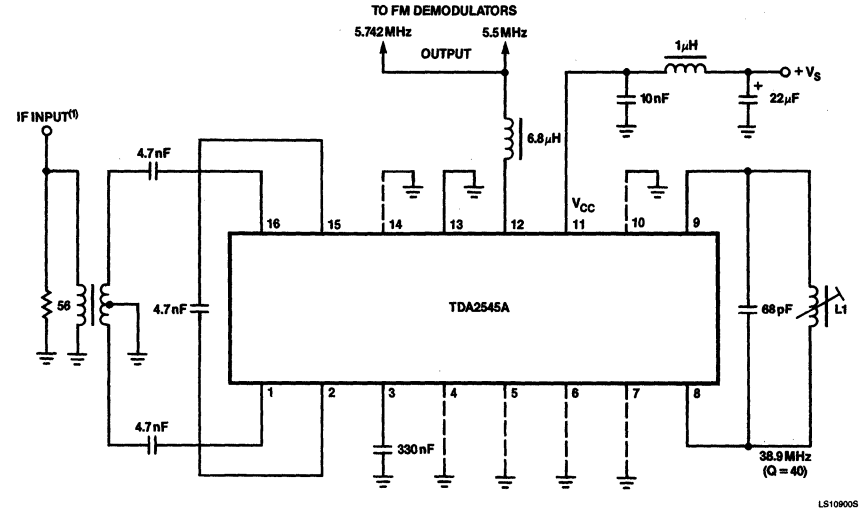
DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V; T_A = 25°C; measured at f_{VC} = 38.9MHz, f_{SC1} = 33.4MHz, f_{SC2} = 33.158MHz:
Vision carrier (VC) modulated with 2T/20T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% residual carrier).
Sound carriers (SC1, SC2) modulated with f = 1kHz and Δf = ±30kHz.
Vision-to-sound carrier ratios are VCSC1 = 13dB and VCSC2 = 20dB.
Vision carrier amplitude (RMS value) is V_{VC} = 10mV.
For measuring circuit see Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 11)					
V_{CC}	Supply voltage	10.8	12	13.2	V
$I_{CC} = I_{11}$	Supply current		42		mA
IF amplifier					
$V_{VC1-16(RMS)}$	Minimum input voltage (RMS value) (intercarrier signals −3dB)		50		μV
$V_{VC1-16(RMS)}$	Maximum input voltage (RMS value) (intercarrier signals +1dB		100		mV
ΔG_V	IF control range	66			dB
V_{3-13}	Control voltage range	4		9	V
R_{1-16}	Input resistance		2		kΩ
C_{1-16}	Input capacitance		2		pF
Intercarrier generation					
$V_{12-13(RMS)}$	Output voltage; 5.5MHz (RMS value)		100		mV
$V_{12-13(RMS)}$	Output voltage; 5.742MHz (RMS value)		45		mV
V_{12-13}	DC output voltage		5.9		V
R_{12-13}	Allowable load resistance at the output	7			kΩ
$-I_{12}$	Allowable output current			1	mA
Intercarrier signal-to-noise (measured behind the FM demodulators)					
	Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak				
S + W/W	at 5.5MHz	53			dB
S + W/W	at 5.742MHz	51			dB
	with black level (vision carrier modulated with sync pulses only)				
S + W/W	at 5.5MHz	60			dB
S + W/W	at 5.742MHz	58			dB

8

Quasi-Split-Sound Circuit TDA2545A



NOTES:
Pins 4, 5, 6, 7, 10 and 14 not connected.
1. IF signal: vision carrier (VC) and sound carrier (SC)

Figure 1. Measuring Circuit for TDA2545A

TDA2546A
Quasi-Split-Sound IF With Sound Demodulator

Product Specification

Linear Products

DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5.5MHz demodulation, in television receivers.

FEATURES

First IF (VC: vision carrier plus SC: sound carrier)

- **3-stage, gain-controlled IF amplifier**
- **AGC circuit**
- **Reference amplifier and limiter amplifier for vision carrier (VC) processing**
- **Linear multiplier for quadrature demodulation**

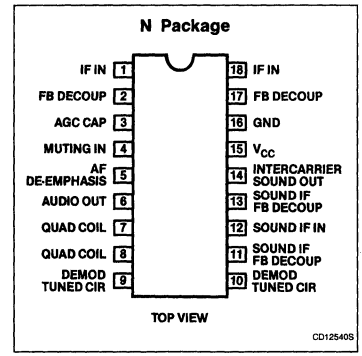
Second IF (5.5MHz signal)

- **8-stage limiter amplifier**
- **Quadrature demodulator**
- **AF amplifier with de-emphasis**
- **AV switch**

APPLICATIONS

- **Television stereo MTS receiver**
- **Video cassette recorder with MTS stereo**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102CS)	0 to +70°C	TDA2546AN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 15)	13.2	V
I_{IN}	Input current (Pin 4)	5	mA
T_{STG}	Storage temperature range	−25 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

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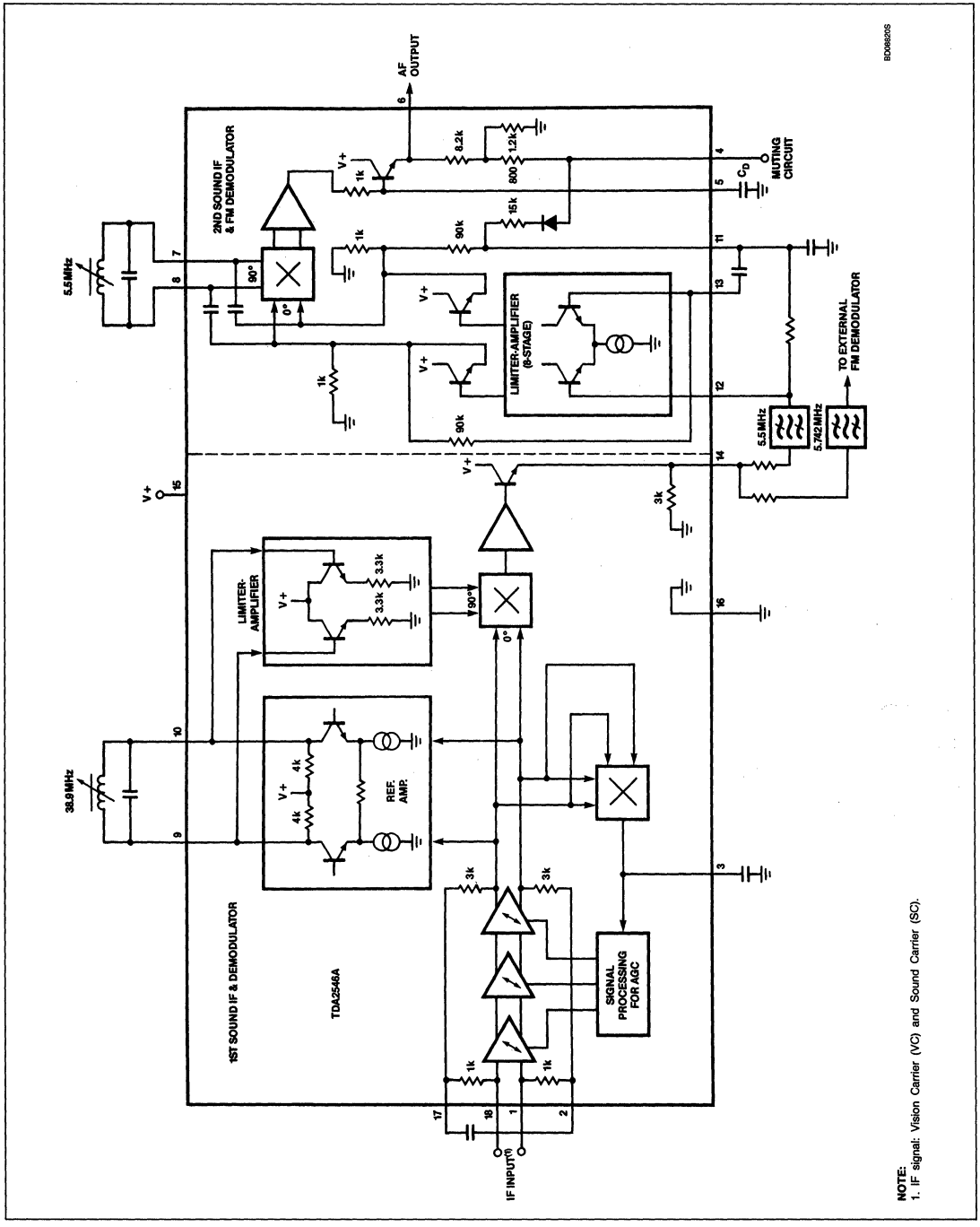
Quasi-Split-Sound IF With Sound Demodulator TDA2546A

BLOCK DIAGRAM



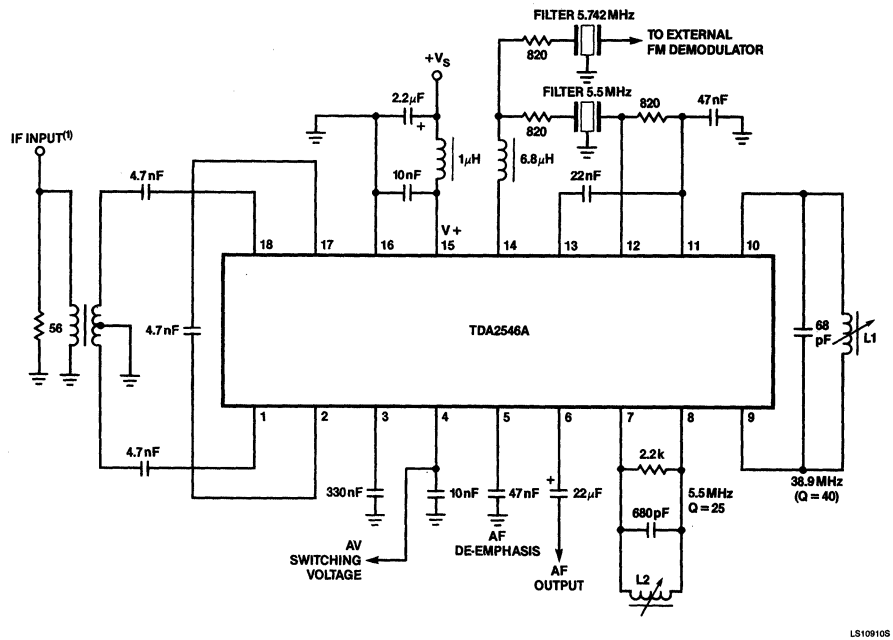
DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{15-16} = 12V$; $T_A = 25°C$; measured at $f_{VC} = 38.9MHz$, $f_{SC1} = 33.4MHz$, $f_{SC2} = 33.158MHz$:
Vision carrier (VC) modulated with 2T/20T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% residual carrier).
Sound carriers (SC1, SC2) modulated with f = 1kHz and $\Delta f = \pm 30kHz$.
Vision-to-sound carrier ratios are VC/SC1 = 13dB and VC/SC2 = 20dB.
Vision carrier amplitude (RMS value) is $V_{VC} = 10mV$.
For measuring circuit see Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 15)					
$V_{CC} = V_{15-16}$	Supply voltage	10.8	12	13.2	V
$I_{CC} = I_{15}$	Supply current		54		mA
IF amplifier					
$V_{VC1-18(RMS)}$	Minimum input voltage (RMS value) (intercarrier signals −3dB)		50		μV
$V_{VC1-18(RMS)}$	Maximum input voltage (RMS value) (intercarrier signals +1dB)		100		mV
ΔG_V	IF control range	66			dB
V_{3-16}	Control voltage range	4		9	V
R_{1-18}	Input resistance		2		kΩ
C_{1-18}	Input capacitance		2		pF
Intercarrier generation					
$V_{14-16(RMS)}$	Output voltage; 5.5MHz (RMS value)		100		mV
$V_{14-16(RMS)}$	Output voltage; 5.742MHz (RMS value)		45		mV
V_{14-16}	DC output voltage		5.9		V
R_{14-16}	Allowable load resistance at the output	7			kΩ
$-I_{14}$	Allowable output current			1	mA
Frequency demodulator (measured at f = 5.5MHz)					
$V_{12-16(RMS)}$	Input voltage for start of limiting (RMS value)			100	μV
$V_{12-16(RMS)}$	Maximum input voltage (RMS value)		200		mV
$V_{11, 12, 13-16}$	DC output voltage		2.2		V
$V_{6-16(RMS)}$	AF output voltage (RMS value)		600		mV
V_{6-16}	DC output voltage		4		V
R_{6-16}	Allowable load resistance at the output	27			kΩ
THD	Total harmonic distortion			1	%
R_{15-16}	Internal de-emphasis resistance		1		kΩ
	Switching voltage (Pin 4)				
V_{4-16}	for mute	9			V
V_{4-16}	for AF on			2.5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
	Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak				
S + W/W	at 5.5MHz	53			dB
S + W/W	at 5.742MHz	51			dB
	with black level (vision carrier modulated with sync pulses only)				
S + W/W	at 5.5MHz	60			dB
S + W/W	at 5.742MHz	58			dB

8

Quasi-Split-Sound IF With Sound Demodulator TDA2546A



NOTE:
1. IF signal: Vision Carrier (VC) and Sound Carrier (SC).

Figure 1. Measuring Circuit for TDA2546A

Signetics

TDA2555
Dual TV Sound Demodulator Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA2555 incorporates two FM demodulator systems to perform the demodulator functions required in a dual sound carrier TV system for demodulating the sound carriers.

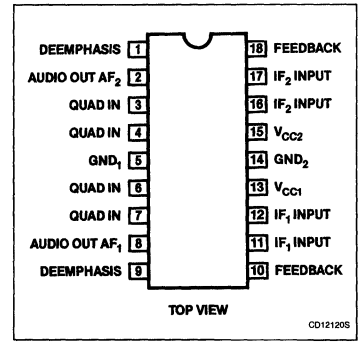
FEATURES

- **Eight-stage limiting amplifier**
- **Quadrature demodulator for FM detection**
- **De-emphasis stage**
- **Output amplifier**

APPLICATIONS

- **Black-and-white/color receivers**
- **Video cassette recorders (VCR)**
- **Satellite receivers**
- **CATV converters**

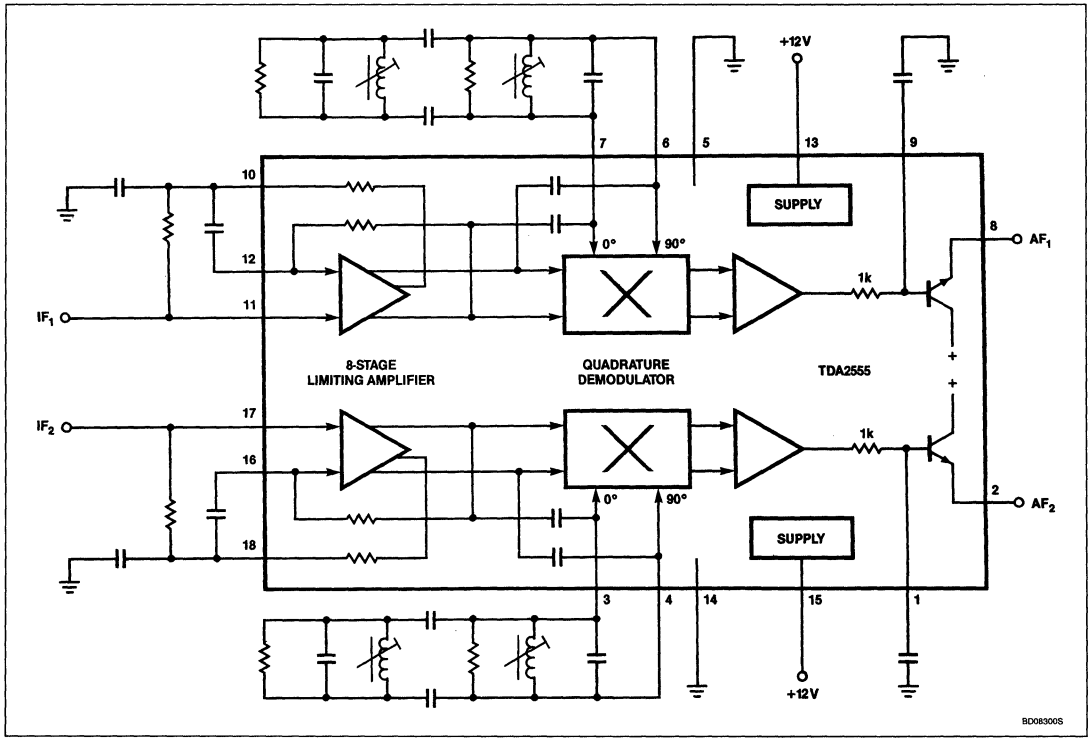
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	0 to +70°C	TDA2555N

BLOCK DIAGRAM



8

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pins 13 and 15)	13.2	V
P_{TOT}	Total power dissipation	400	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{13,\ 15-14} = 12V$; $T_A = 25°C$; $f = 5.5MHz$; $f_{M1} = 1kHz$; $\Delta f = \pm 30kHz$; $V_{I\ (RMS)} = 5mV$, see Test Circuit Figure 1, voltages with respect to ground (Pin 14), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage (Pins 13 and 15)	10.8	12.0	13.2	V
$I_{13,\ 15}$	Supply current		24.5		mA
$V_{12,\ 17(RMS)}$	Input voltage (RMS value) for start of limiting			100	μV
$V_{12,\ 17-14}$	Maximum input voltage		200		mV
V_I	DC voltage at inputs-Pins 10, 11, 12, 16, 17, and 18 to 14		2.0		V
AMS	AM suppression $f_{M(FM)} = 70Hz$; $\Delta f = \pm 30kHz$ $f_{M(AM)} = 1kHz$; $m = 30\%$	50			dB
$V_{2,\ 8-14}$	AF output voltage RMS value	350			mV
$V_{2,\ 8-14}$	DC voltage at outputs Pins 2 and 8		3.7		V
R_L	Output lead resistance Pins 2 and 8	10			kΩ
THD	Total harmonic distortion			0.1	%
R_I	Internal de-emphasis resistance Pins 1 and 9		1.0		kΩ
α	Channel separation	60			dB

Dual TV Sound Demodulator Circuit TDA2555

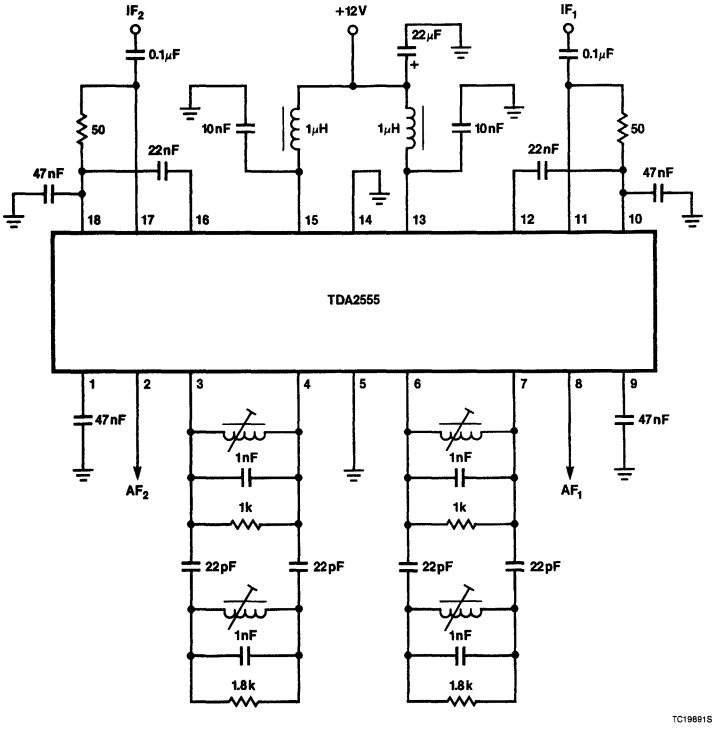


Figure 1. Test Circuit

8

Signetics

Linear Products

Section 9
SYNC Processing and Generation

INDEX

Signetics

TDA2577A

Sync Circuit With Vertical Oscillator and Driver

Product Specification

Linear Products

DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

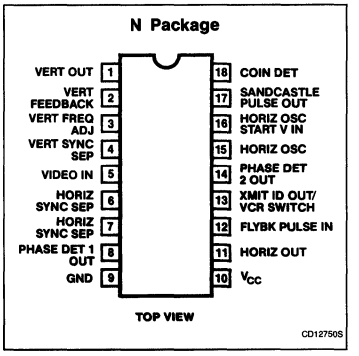
FEATURES

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise-only conditions
- Time constant externally switchable (e.g., fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3 levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the supply voltage
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6.5V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic precorrection of the oscillator/sawtooth generator. Comparator supplied with precorrected sawtooth and external feedback input
- Vertical comparator with internal 3% precorrection circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

APPLICATIONS

- Video monitors
- TV receivers
- Video processing

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−25°C to +65°C	TDA2577AN

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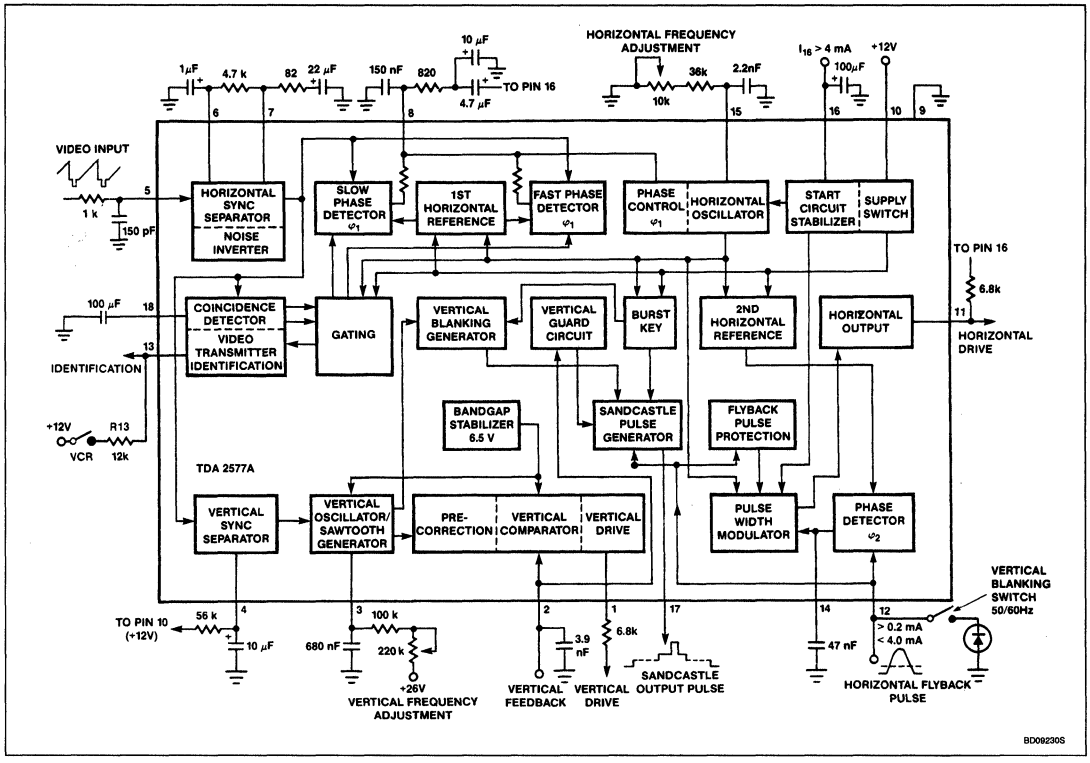
Sync Circuit With Vertical Oscillator and Driver | TDA2577A

BLOCK DIAGRAM



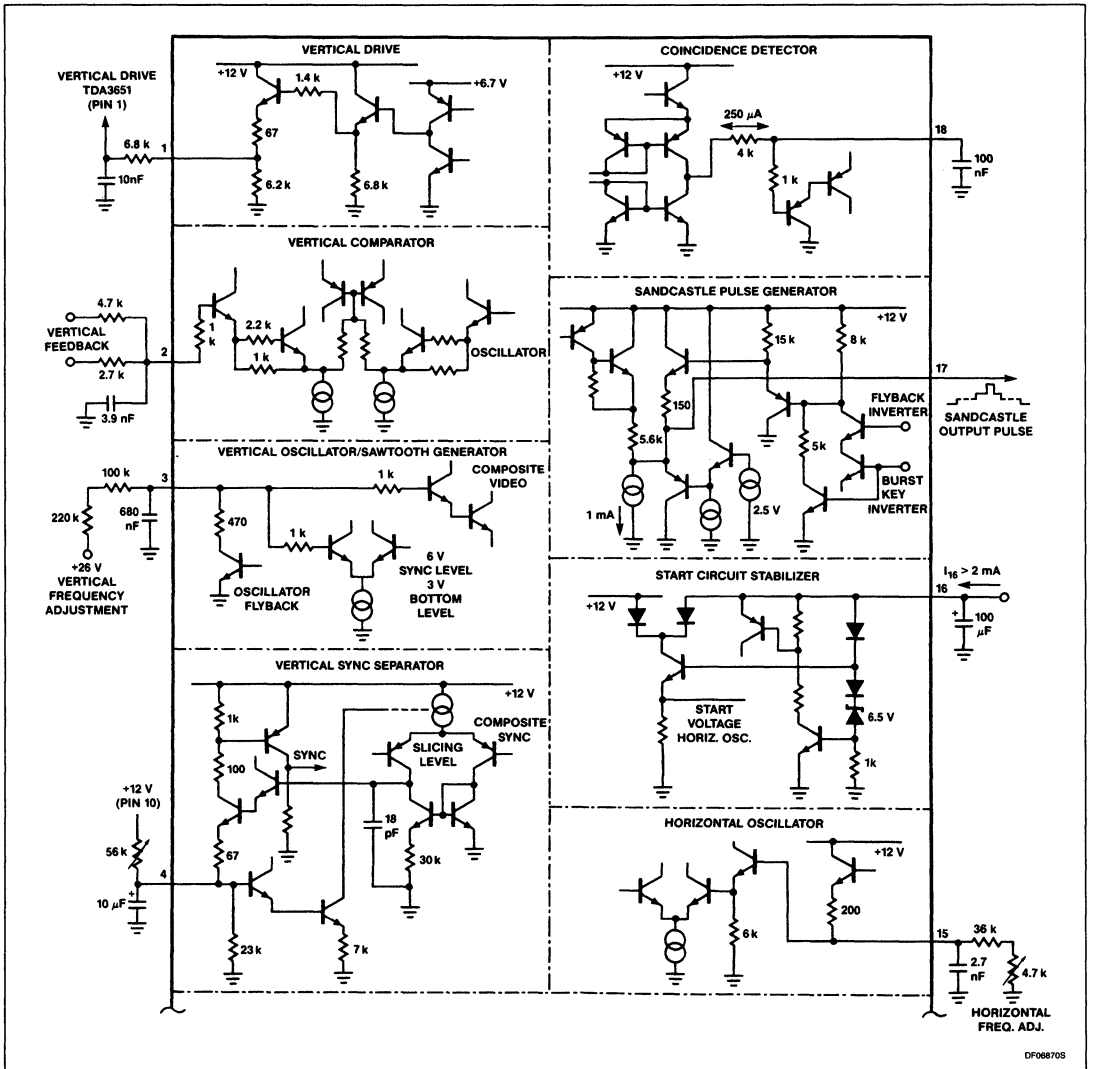


Figure 1. TDA2577A Circuit Diagram

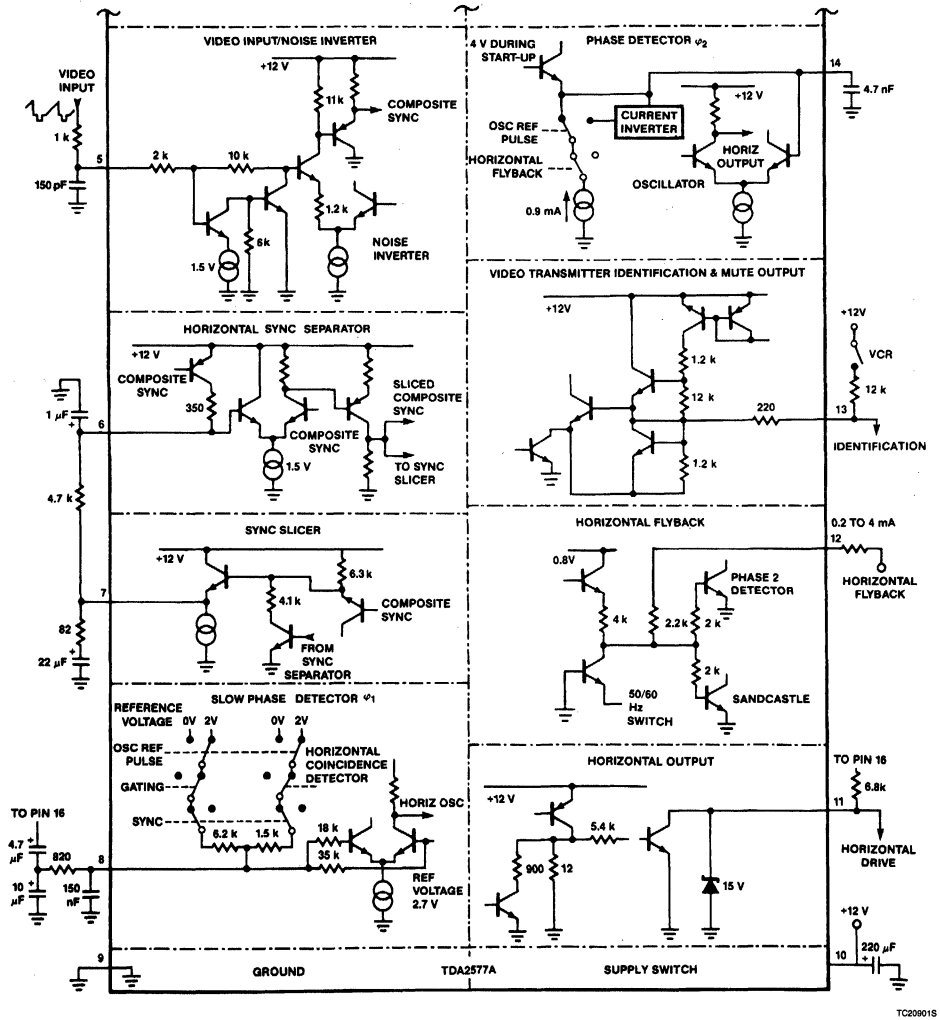


Figure 1. TDA2577A Circuit Diagram (Continued)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
I_{16}	Start current (Pin 16)	8	mA
$V_{CC} = V_{10-9}$	Supply voltage (Pin 10)	13.2	V
P_{TOT}	Total power dissipation	1.1	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient in free air	50	°C/W

DC ELECTRICAL CHARACTERISTICS I_{16} = 5mA; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
I_{16}	Supply current at Pin 16	4		8	mA
V_{16-9}	Stabilized supply voltage (Pin 16)	8.0	8.7	9.5	V
I_{10}	Supply current (Pin 10)		55	70	mA
$V_{CC} = V_{10-9}$	Supply voltage (Pin 10)	10	12	13.2	V
Video input (Pin 5)					
V_{5-9}	Top-sync level	1.5	3.1	3.75	V
$V_{5-9(P-P)}$	Sync pulse amplitude (peak-to-peak value)[1]	0.15	0.6	1	V
	Slicing level	35	50	65	%
t_1	Delay between video input and detector output		0.35		µs
Noise gate (Pin 5)					
V_{5-9}	Switching level		0.7	1	V
First control loop (sync to oscillator; Pin 8)					
Δf	Holding range		±800		Hz
Δf	Catching range	±600	800	1100	Hz
	Control sensitivity video with respect to oscillator, burst key, and flyback pulse for slow time constant for fast time constant		 1 275		 kHz/µs kHz/µs
Second control loop (horizontal output to flyback; Pin 14)					
$\Delta t_D/\Delta t_O$	Control sensitivity; static[2]		400		µs/µs
t_D	Control range	1		50	µs
	Controlled edge		negative		
Phase adjustment (via 2nd control loop; Pin 14)					
	Control sensitivity		25		µA/µs
$\pm I_{14}$	Maximum permissible control current		0	50	µA
Horizontal oscillator (Pin 15)					
f_{OSC}	Frequency (no sync)		15625		Hz
Δf_{OSC}	Frequency spread (C_{OSC} = 2.2nF; R_{OSC} = 40kΩ)			4	%
Δf_{OSC}	Frequency deviation between starting point of output signal and stabilized condition		6	8	%
T_C	Temperature coefficient		1×10^{-4}		°C

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DC ELECTRICAL CHARACTERISTICS (Continued) I_{16} = 5mA; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal output (Pin 11)					
V_{11-9}	Output voltage; high level			13.2	V
V_{11-9}	Voltage at which protection starts	13		15.8	V
V_{11-9}	Output voltage; low level start condition at I_{11} = 10mA		0.3	0.5	V
V_{11-9}	normal condition at I_{11} = 40mA		0.3	0.5	V
δ	Duty factor of output signal during starting (no phase shift; voltage at Pin 11 Low)		65		%
δ	Duty factor of output signal without flyback pulse	45	50	55	%
	Controlled edge	negative			
	Duration of output pulse (see Figure 2)	$t_D + t_O + 2.5$			µs
Sandcastle output pulse (Pin 17)					
	Output voltage during:				
V_{17-9}	burst key	10			V
V_{17-9}	horizontal blanking	4.2	4.6	5	V
V_{17-9}	vertical blanking	2	2.5	3	V
t_P	Pulse duration				
	burst key	3.6	4	4.4	µs
	horizontal blanking	flyback pulse[3]			
	vertical blanking				
	for 50Hz application ($-I_{12}$: 0 to 0.1mA)			21	lines
	for 60Hz application ($-I_{12}$: typ. 0.2mA)			17	lines
t_2	Delay between the start of the sync at the video input and the rising edge of the burst key pulse	4.8	5.2	5.6	µs
Coincidence detector; video transmitter identification circuit; time constant switches (Pin 18); see also Figure 1					
$\pm I_{18}$	Detector output current		300		µA
V_{18-9}	Voltage during noise[4]		0.3		V
V_{18-9}	Voltage level for in-sync condition		7.5		V
V_{18-9}	Switching level slow-to-fast	3.2	3.5	3.8	V
	Switching level				
V_{18-9}	mute function active; φ_1 fast-to-slow	1.0	1.2	1.4	V
	vertical period counter				
V_{18-9}	3 periods fast	0.08	0.12	0.16	V
V_{18-9}	Switching level slow-to-fast (locking) mute function inactive	1.5	1.7	1.9	V
V_{18-9}	Switching level fast-to-slow (locking)	4.7	5.0	5.3	V
V_{18-9}	Switching level for VCR (fast time constant) without mute function	8.2	8.6	9	V

DC ELECTRICAL CHARACTERISTICS (Continued) I_{16} = 5mA; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Video transmitter identification output (Pin 13)					
V_{13-9}	Output voltage active (no sync) at I_{13} = 1mA	10	11		V
V_{13-9}	Output voltage active (no sync) at I_{13} = 5mA	7	10		V
V_{13-9}	Output voltage inactive		0.1	0.5	V
VCR switching (Pin 13)					
I_{13}	Input current for fast time constant phase detector φ_1, with mute function active	0.4	0.6	0.8	mA
Flyback input pulse (Pin 12)					
V_{12-9}	Switching level		1		V
I_{12}	Input current	0.2		4	mA
$V_{12-9(P-P)}$	Input pulse amplitude (peak-to-peak value)			12	V
R_{12-9}	Input resistance		2.7		kΩ
t_O	Delay time of sync pulse (measured in φ_1) to flyback at switching level; $t_{FL} = 12\mu s$[2] (see also Figure 3)		1.3		μs
Duration of vertical blanking pulse (Pin 12)					
	Required input current (negative)				mA
$-I_{12}$	for 50Hz application; 21 lines blanking	0.15	0.2	0.3	mA
$-I_{12}$	for 60Hz application; 17 lines blanking			0.1	mA
$-I_{12}$	Maximum allowed input current			0.4	mA
Vertical sawtooth generator (Pin 3)					
f_S	Vertical frequency (no sync)		46		Hz
Δf_S	Frequency spread (C_{OSC} = 680nF; R_{OSC} = 180kΩ; at +26V)			4	%
	Synchronization range		22		%
I_3	Input current at V_{3-9} = 6V			2	μA
Δf_S	Frequency shift for V_{CC} = 10 to 13V			0.2	%
T_C	Temperature coefficient		1×10^{-4}		$°C^{-1}$
Comparator (Pin 2)					
V_{2-9}	Input voltage	4.0	4.4	4.8	V
$V_{2-9(P-P)}$	DC level AC level (peak-to-peak value)		1.6		V
I_2	Input current at V_{2-9} = 6V			2	μA
	Sawtooth internal precorrection (parabolic convex)		3		%
Vertical output stage; emitter-follower (Pin 1)					
V_{1-9}	Output voltage at I_1 = 10mA	3.2	3.6	5	V
I_1	Output current			20	mA
Vertical guard circuit					
	Activating voltage levels (vertical blanking level is 2.5V)				
V_{2-9}	switching level Low	2.7	3	3.3	V
V_{2-9}	switching level High	5.4	5.8	6.3	V

NOTES:
1. Up to $1V_{P-P}$ the slicing level is constant; at amplitudes exceeding $1V_{P-P}$, the slicing level will increase.
2. t_D = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_O = delay between the rising edge of the flyback pulse and the start of the current in $\varphi 1$ (Pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about $1V(t_{FL})$.
4. Depends on DC level at Pin 5; value given applicable for $V_{5-9} \approx 5V$.

Sync Circuit With Vertical Oscillator and Driver — TDA2577A

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geq 4mA$), which can be taken directly from the supply line. Therefore, it is possible to derive the main supply (Pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting up, the second phase detector ($\varphi 2$) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6.5V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between Pins 6 and 7 determines its value. A 4.7kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3.1V. The amplitude selective noise inverter is activated at a level of 0.7V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared to a waveform with its rising edge refering to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared to another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore, the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

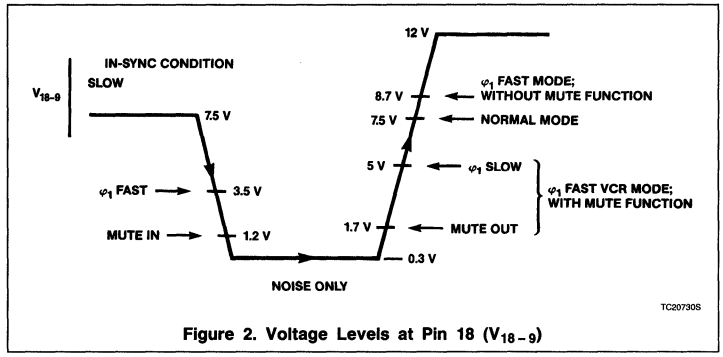


Figure 2. Voltage Levels at Pin 18 (V_{18-9})

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync, or no-video condition is detected by the video transmitter identification/coincidence detector circuit (Pin 18). The voltage on Pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Figure 2. The complete survey of the switching actions is given in Table 1.

Table 1. Switching Levels at Pin 18

VOLTAGE AT PIN 18	FIRST PHASE DETECTOR φ_1				MUTE OUTPUT AT PIN 13		RECEIVING CONDITIONS
	Time Constant		Gating		On	Off	
	Slow	Fast	On	Off			
7.5V	X		X			X	Video signal detected
7.5 to 3.5V	X		X			X	Video signal detected
3.5 to 1.2V		X		X		X	Video signal detected
1.2 to 0.1V	X		X		X		Noise only
0.1 to 1.7V	X	*	X	*	X		New video signal detected
1.7 to 5.0V		X		X		X	Horizontal oscillator locked VCR playback with mute function
5.0 to 7.5V	X		X			X	Horizontal oscillator locked
8.7V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g., channel number) during noise-only conditions is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on Pin 5 during noise-only conditions should not exceed 5.5V. Otherwise, the time constant switch may be set to fast due to the average voltage level on Pin 18 dropping below 0.1V. When the voltage on Pin 18 drops below 100mV, a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at Pin 5. When the horizontal oscillator is locked, the voltage on Pin 18 increases. Nominally, a level of 5V is reached within 15ms (1 vertical period). The mute switching level of 1.2V is reached within 5ms (C_{18} = 47nF). If the video transmitter identification circuit is required to operate under VCR playback conditions, the first phase detector can be set to fast by connecting a resistor of 180kΩ between Pin 18 and ground. Also, a current of 0.6mA into Pin 13 sets the first phase detector to fast without affecting the mute output function (active High with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1kΩ to the supply (Pin 10).

The supply for the horizontal oscillator (Pin 15) and horizontal output stage (Pin 11) is derived from the voltage at Pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into Pin 16

of 3.5mA, which will result in a supply voltage of about 5.5V (for guaranteed operation of all devices $I_{16} > 4mA$). It is possible that the main supply voltage at Pin 10 is 0V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at Pin 10. At 5.5V, all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at Pin 14 is clamped by means of an internally-loaded NPN emitter-follower. This ensures that the duty factor of the horizontal output signal (Pin 11) remains at about 65%. The second phase detector will close if the supply voltage at Pin 10 reaches 8.8V. At this value, the supply current for the horizontal oscillator and output stage is delivered by Pin 10, which also causes the voltage at Pin 16 to change to a stabilized 8.7V. This change switches off the NPN emitter-follower at Pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at Pin 16, and the duty factor of the output signal at Pin 12 is at the value required by the delay at the horizontal deflection stage. Thus, switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected, the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47nF capacitor connected to Pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to Pin 2) via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at Pin 1. For a linear sawtooth in the oscillator, the load resistor at Pin 3 should be connected to a voltage source of 26V or higher. The sawtooth amplitude is not influenced by the main supply at Pin 10. The feedback signal is applied to Pin 2 and compared to the sawtooth signal at Pin 3. For an economical feedback circuit with less picture bounce, the sawtooth signal is internally precorrected by 3% (convex) referred to Pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at Pin 3 and the feedback signal at Pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at Pin 13.

To minimize the influence of the horizontal part on the vertical part, a 6.5V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at Pin 17, has three different voltage levels. The highest level (11V) can be used for burst gating and black level clamping. The second level (4.6V) is obtained from the horizontal flyback pulse at Pin 12 and used for horizontal blanking. The third level (2.5V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50Hz, the blanking pulse duration is 21 lines and for 60Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at Pin 12.

The IC also incorporates a vertical guard circuit which monitors the vertical feedback signal at Pin 2. If this level is below 3V or higher than 5.8V, the guard circuit will insert a continuous level of 2.5V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

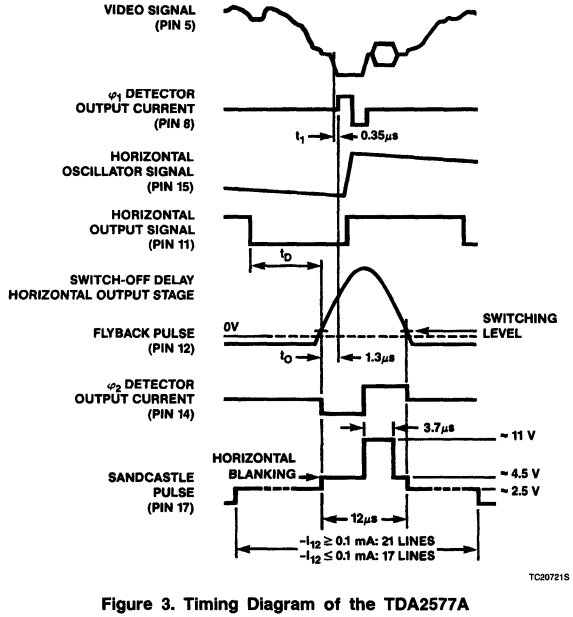


Figure 3. Timing Diagram of the TDA2577A

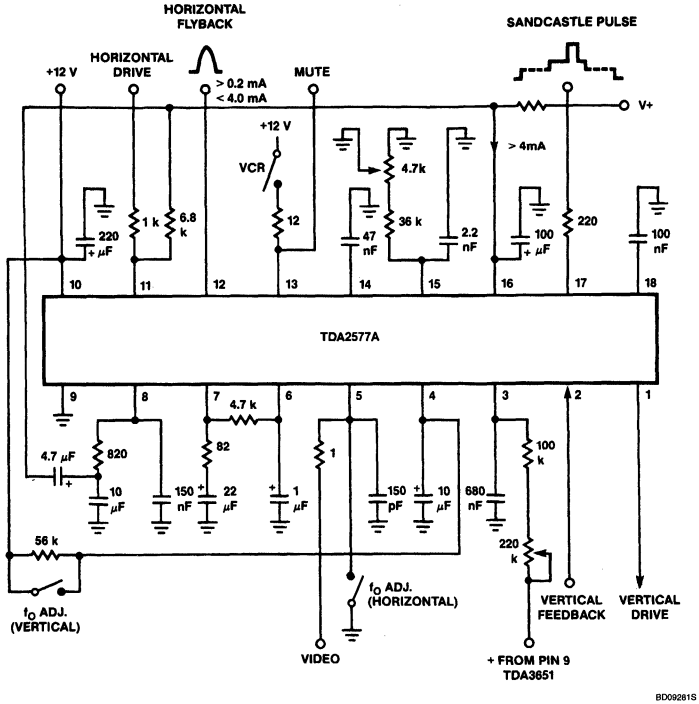


Figure 4. Typical Application Circuit Diagram; for Combination of the TDA2577A with the TDA3651 (see Figure 6)

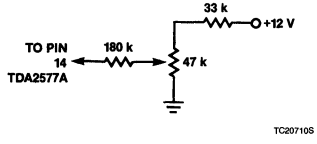


Figure 5. Circuit Configuration at Pin 14 for Phase Adjustment

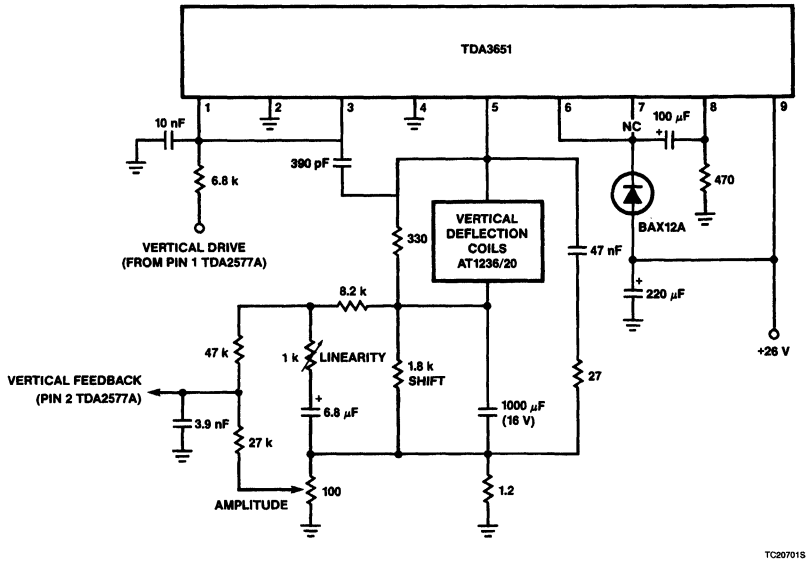


Figure 6. Typical Application Circuit Diagram of the TDA3651 (Vertical Output) When Used in Combination With the TDA2577A (90°C Application)

9

Signetics

TDA2578A

Sync Circuit With Vertical Oscillator and Driver

Product Specification

Linear Products

DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

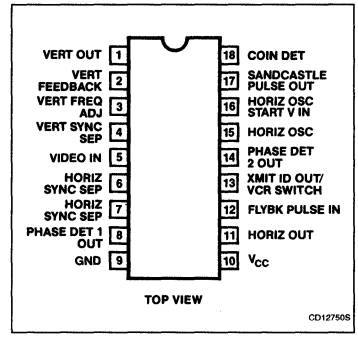
FEATURES

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync-to-oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise-only conditions
- Time constant externally switchable (e.g., fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3 levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the power line rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6.5V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60Hz detector
- 50/60Hz identification output
- Automatic amplitude adjustment for 60Hz
- Automatic adjustment of blanking pulse duration (50Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

APPLICATIONS

- Video terminals
- Television

PIN CONFIGURATION

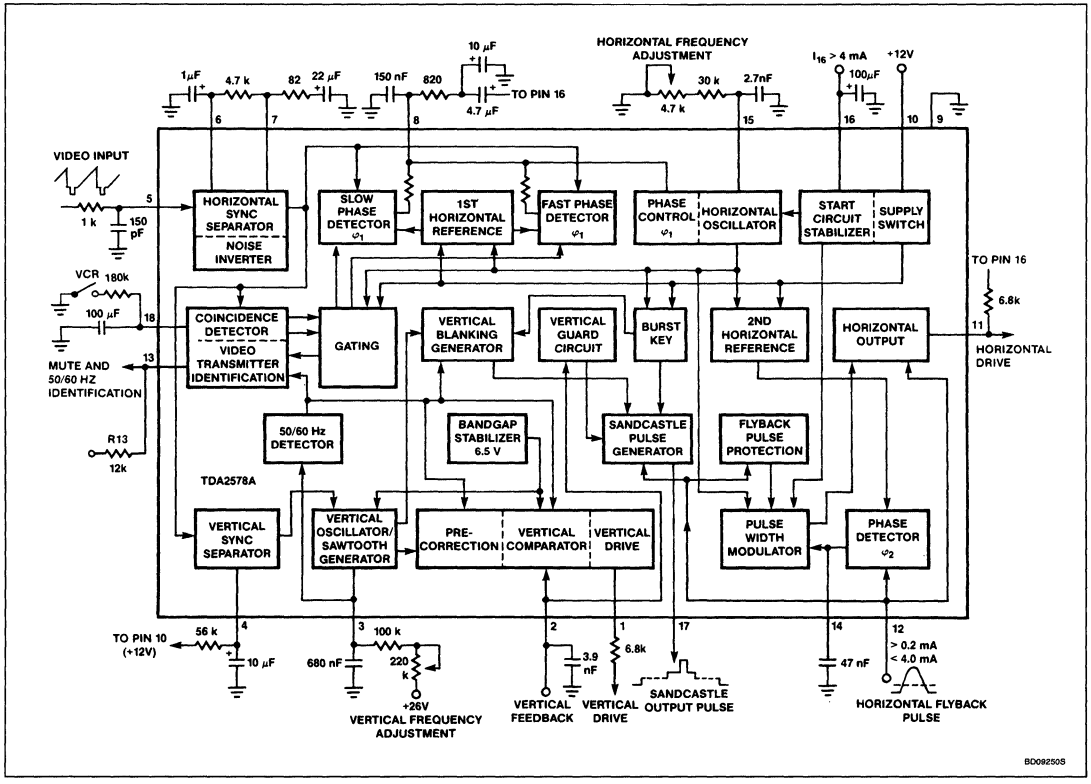


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−25°C to +65°C	TDA2578A

Sync Circuit With Vertical Oscillator and Driver | TDA2578A

BLOCK DIAGRAM



Sync Circuit With Vertical Oscillator and Driver TDA2578A

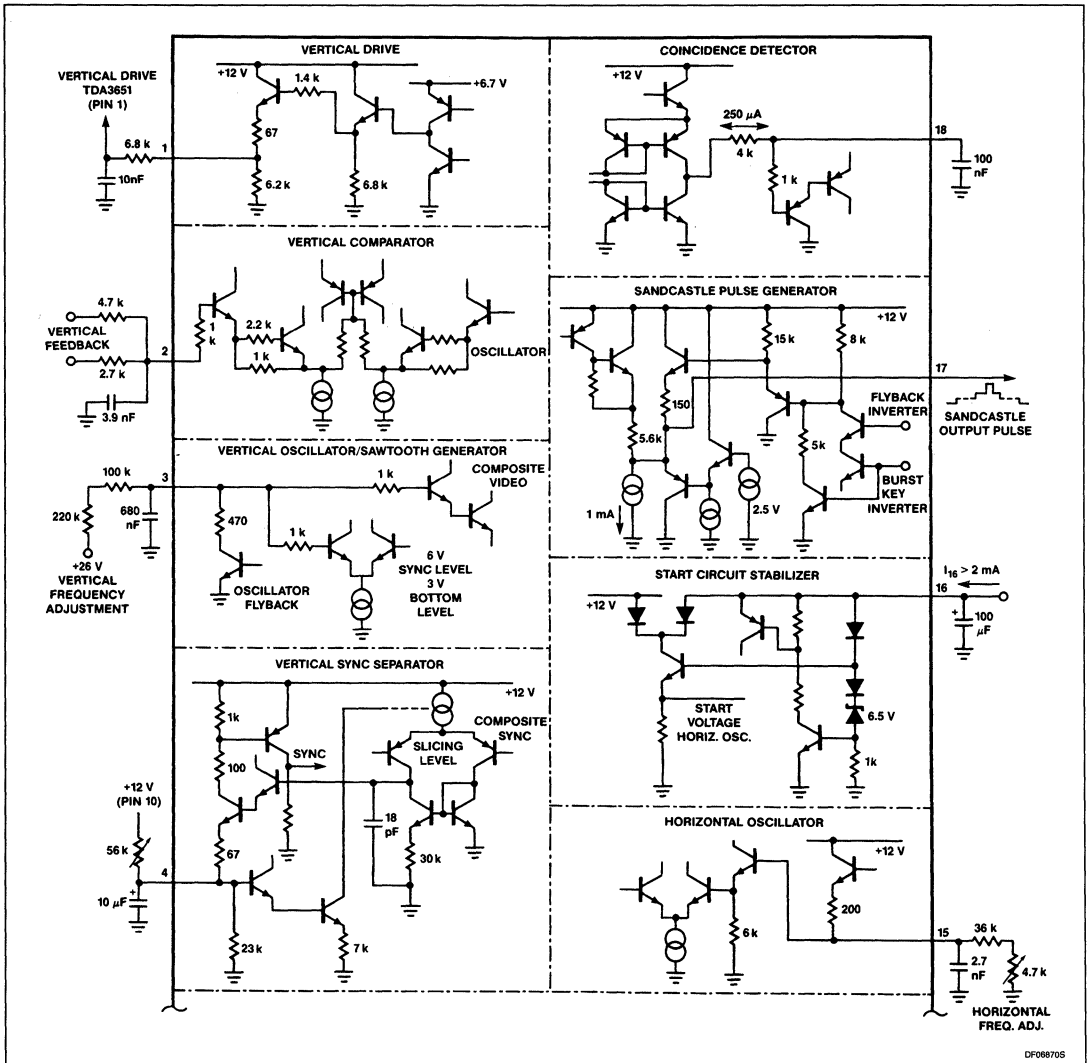


Figure 1a. TDA2578A Circuit Diagram

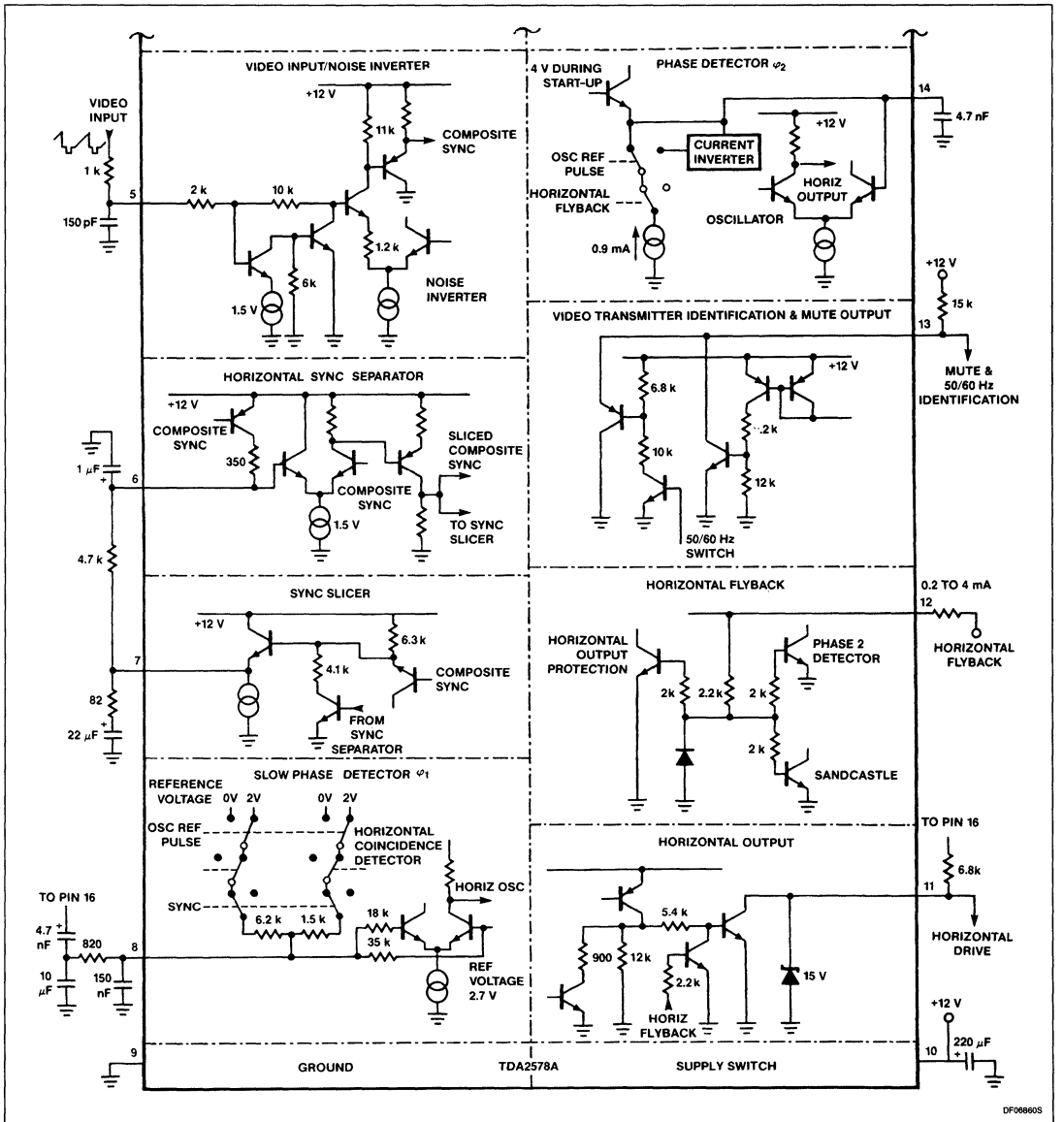


Figure 1b. TDA2578A Circuit Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
I_{16}	Start current (Pin 16)	8	mA
$V_{CC} = V_{10-9}$	Supply voltage (Pin 10)	13.2	V
P_{TOT}	Total power dissipation	1.1	W
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient in free air	50	°C

DC AND AC ELECTRICAL CHARACTERISTICS I_{16} = 5mA; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
I_{16}	Supply current at Pin 16	4		8	mA
V_{16-9}	Stabilized supply voltage (Pin 16)	8	8.7	9.5	V
I_{10}	Supply current (Pin 10)		55	70	mA
$V_{CC} = V_{10-9}$	Supply voltage (Pin 10)	10	12	13.2	V
Video input (Pin 5)					
V_{5-9}	Top-sync level	1.5	3.1	3.75	V
$V_{5-9(P-P)}$	Sync pulse amplitude (peak-to-peak value)[1]	0.15	0.6	1	V
	Slicing level	35	50	65	%
t_1	Delay between video input and detector output		0.35		μs
Noise gate (Pin 5)					
V_{5-9}	Switching level		0.7	1	V
First control loop (sync to oscillator; Pin 8)					
Δf	Holding range		±800		
Δf	Catching range	600	800	1100	Hz
	Control sensitivity video with respect to oscillator, burst key, and flyback pulse for slow time constant for fast time constant		 1 2.75		 kHz/μs kHz/μs
Second control loop (horizontal output to flyback; Pin 14)					
$\Delta t_D/\Delta t_O$	Control sensitivity; static[2]		400		μs/μs
t_D	Control range	1		45	μs
	Controlled edge (positive)				
Phase adjustment (via 2nd control loop; Pin 14)					
	Control sensitivity		25		μA
$\pm I_{14}$	Maximum permissible control current			50	μA
Horizontal oscillator (Pin 15)					
f_{OSC}	Frequency (no sync)		15625		Hz
Δf_{OSC}	Frequency spread (C_{OSC} = 2.7nF; R_{OSC} = 33kΩ; no sync)			4	%
Δf_{OSC}	Frequency deviation between starting point of output signal and stabilized condition	6		8	%
TC	Temperature coefficient		10^{-4}		°C

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) I_{16} = 5mA; V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal output (Pin 11)					
V_{11-9}	Output voltage; high level			13.2	V
V_{11-9}	Voltage at which protection starts	13		15.8	V
	Output voltage; low level				
V_{11-9}	start condition at I_{11} = 10mA		0.3	0.5	V
V_{11-9}	normal condition at I_{11} = 40mA		0.3	0.5	V
δ	Duty factor of output signal during starting (no phase shift) I_{16} = 4mA (voltage at Pin 11 low)		65		%
δ	Duty factor of output signal without flyback pulse	45	50	55	%
	Controlled edge (positive)				
	Duration of output pulse (see Figure 3)	t_D+ horizontal flyback pulse			
Sandcastle output pulse (Pin 17)					
	Output voltage during:				
V_{17-9}	burst key			10	V
V_{17-9}	horizontal blanking	4.2	4.6	5	V
V_{17-9}	vertical blanking	2	2.5	3	V
t_P	Pulse duration burst key	3.6	4	4.4	µs
	horizontal blanking (flyback pulse)[3]				
	vertical blanking				
	at 50Hz	21 lines			
	at 60Hz	17 lines			
t_2	Delay between the start of the sync at the video input and the rising edge of the burst key pulse	4.5			
Coincidence detector; video transmitter identification circuit; time constant switches (Pin 18) (see also Figure 2)					
$\pm I_{18}$	Detector output current		300		µA
V_{18-9}	Voltage during noise[4]		0.3		V
V_{18-9}	Voltage level for in-sync condition		7.5		V
V_{18-9}	Switching level slow to fast	3.2	3.5	3.8	V
	Switching level				
V_{18-9}	mute function active; φ_1 fast to slow	1	1.2	1.4	V
V_{18-9}	vertical period counter; 3 periods fast	0.08	0.12	0.16	V
	Switching level slow-to-fast (locking)				
V_{18-9}	mute function inactive	1.5	1.7	1.9	V
V_{18-9}	Switching level fast-to-slow (locking)	4.7	5	5.3	V
	Switching level for VCR (fast time constant)				
V_{18-9}	without mute function	8.2	8.6	9	V
Video transmitter identification output (Pin 13)					
V_{13-9}	Output voltage active (no sync) at I_{13} = 1mA		0.3	0.5	V
I_{13}	Sink current active (no sync)		5		mA
I_{13}	Output current inactive (sync: 50Hz)			1	µA
50/60Hz identification (Pin 13)					
	R13 = 15kΩ to +12V[5]				
V_{13-9}	at f = 50Hz (in sync condition)		V_{10-9}		V
V_{13-9}	at f = 60Hz (in sync condition)	7.2	7.6	8	V

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $I_{16} = 5mA$; $V_{CC} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Flyback input pulse (Pin 12)					
V_{12-9}	Switching level		1		V
I_{12}	Input current	0.2		4	mA
$V_{12-9(P-P)}$	Input pulse amplitude (peak-to-peak value)			12	V
R_{12-9}	Input resistance		2.7		kΩ
t_O	Delay time of sync pulse (measured in φ_1) to flyback at switching level; $t_{FL} = 12\mu s$[2] (see also Figure 3)		1.3		μs
Vertical sawtooth generator (Pin 3)					
f_S	Vertical frequency (no sync)		46		Hz
Δf_S	Frequency spread ($C_{OSC} = 680nF$; $R_{OSC} = 180k\Omega$; at +26V)			4	%
	Synchronization range[6]		33		%
I_3	Input current at $V_{3-9} = 6V$			3	μA
Δf_S	Frequency shift for $V_{CC} = 10$ to 13V			0.2	%
TC	Temperature coefficient		10^{-4}		°C
Comparator (Pin 2)					
V_{2-9} $V_{2-9(P-P)}$	Input voltage; DC level AC level (peak-to-peak value)	4	4.4 0.8	4.8	V V
I_2	Input current at $V_{2-9} = 6V$			2	μA
	Sawtooth internal precorrection (parabolic convex)		6		%
Vertical output stage; emitter-follower (Pin 1)					
V_{1-9}	Output voltage at $I_1 = 10mA$	3.2		5	V
I_1	Output current			20	mA
Vertical guard circuit					
	Activating voltage levels (vertical blanking level is 2.5V)				
V_{2-9}	switching level LOW	3	3.35	3.7	V
V_{2-9}	switching level HIGH	4.75	5.15	5.55	V

NOTES:
1. Up to $1V_{P-P}$ the slicing level is constant; at amplitudes exceeding $1V_{P-P}$ the slicing level will increase.
2. t_D = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_O = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (Pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about $1V(t_{FL})$.
4. Depends on DC level at Pin 5; value given applicable for $V_{5-9} \approx 5V$.
5. For 60Hz, a PNP emitter clamp is activated.
6. When $f_O = 46Hz$, the 50/60Hz detector switches over to 60Hz; video input signal at Pin $5 \approx 55Hz$.

Table 1. Switching Levels at Pin 18

VOLTAGE AT PIN 18	FIRST PHASE DETECTOR φ_1				MUTE OUTPUT AT PIN 13		RECEIVING CONDITIONS
	Time Constant		Gating		On	Off	
	Slow	Fast	On	Off			
7.5V	X		X			X	Video signal detected
7.5 to 3.5V	X		X			X	Video signal detected
3.5 to 1.2V		X		X		X	Video signal detected
1.2 to 0.1V	X		X		X		Noise only
0.1 to 1.7V	X	*	X	*	X		New video signal detected
1.7 to 5.0V		X		X		X	Horizontal oscillator locked VCR playback with mute function
5.0 to 7.5V	X		X			X	Horizontal oscillator locked
8.7V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4mA$), which can be taken directly from the power line rectifier. Therefore, it is possible to derive the main supply (Pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting up, the second phase detector ($\varphi 2$) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6.5V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between Pins 6 and 7 determines its value. A 4.7kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3.1V. The amplitude selective noise inverter is activated at a level of 0.7V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared to a waveform with its rising edge refering to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared to another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

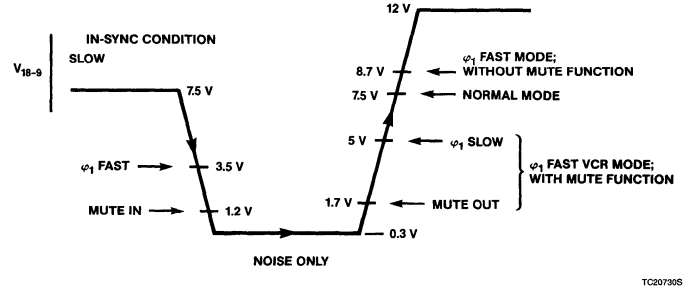

Figure 2. Voltage Levels at Pin 18 (V_{18-9})

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync, or no-video condition is detected by the video transmitter identification/coincidence detector circuit (Pin 18). The voltage on Pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Figure 2. The complete survey of the switching actions is given in Table 1.
The stability of displayed video information (e.g., channel number) during noise-only conditions is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on Pin 5 during noise-only conditions should not exceed 5.5V. Otherwise, the time constant switch may be set to fast due to the average voltage level on Pin 18 dropping below 0.1V. When the voltage on Pin 18 drops below 100mV, a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at Pin 5. When the horizontal oscillator is locked, the voltage on Pin 18 increases. Nominally a level of 5V is reached within 15ms (1 vertical period). The mute switching level of 1.2V is reached within 5ms (C_{18} = 47nF). If the video transmitter identification circuit is required to operate under VCR playback conditions, the first phase detector can be set to fast by connecting a resistor of 180kΩ between Pin 18 and ground (see Figure 6).

The supply for the horizontal oscillator (Pin 15) and horizontal output stage (Pin 11) is derived from the voltage at Pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into Pin 16 of 3.6mA, which will result in a supply voltage of about 5.5V (for guaranteed operation of all devices $I_{16} > 4mA$). It is possible that the main supply voltage at Pin 10 is 0V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at Pin 10. At 5.5V, all IC functions

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start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at Pin 14 is clamped by means of an internally-loaded NPN emitter-follower. This ensures that the duty factor of the horizontal output signal (Pin 11) remains at about 65%. The second phase detector will close if the supply voltage at Pin 10 reaches 8.8V. At this value, the supply current for the horizontal oscillator and output stage is delivered by Pin 10, which also causes the voltage at Pin 16 to change to a stabilized 8.7V. This change switches off the NPN emitter-follower at Pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at Pin 16, and the duty factor of the output signal at Pin 12 is at the value required by the delay at the horizontal deflection stage. Thus, switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected, the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47nF capacitor connected to Pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to Pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at Pin 1. For a linear sawtooth in the oscillator, the load resistor at Pin 3 should be connected to a voltage source of 26V or higher. The sawtooth amplitude is not influenced by the main supply at Pin 10. The feedback signal is applied to Pin 2 and compared to the sawtooth signal at Pin 3. For an economical feedback circuit with less picture bounce, the sawtooth signal is internally pre-corrected by 6% (convex) referred to Pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at Pin 3 and the feedback signal at Pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at Pin 13.

To minimize the influence of the horizontal part on the vertical part, a 6.7V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at Pin 17, has three different voltage levels. The highest level (11V) can be used for burst gating and black level clamping. The second level (4.6V) is obtained from the horizontal flyback pulse at Pin 12 and used for horizontal blanking. The third level (2.5V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50Hz the blanking pulse duration is 21 lines, and for 60Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60Hz detector.

The IC also incorporates a vertical guard circuit which monitors the vertical feedback signal at Pin 2. If this level is below 3.35V or higher than 5.15V, the guard circuit will insert a continuous level of 2.5V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

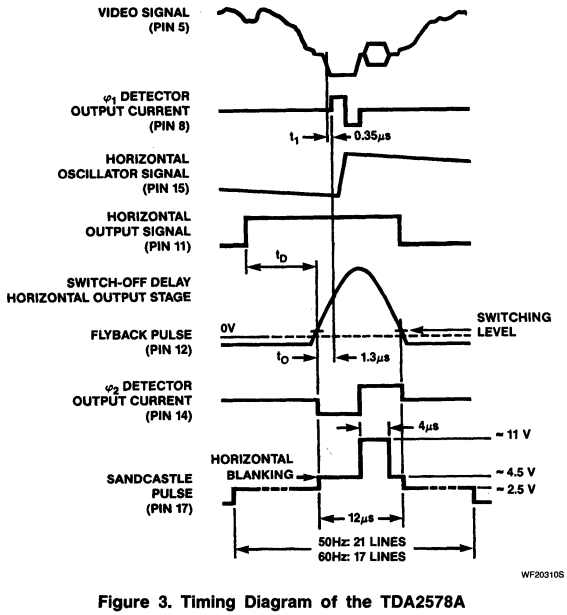
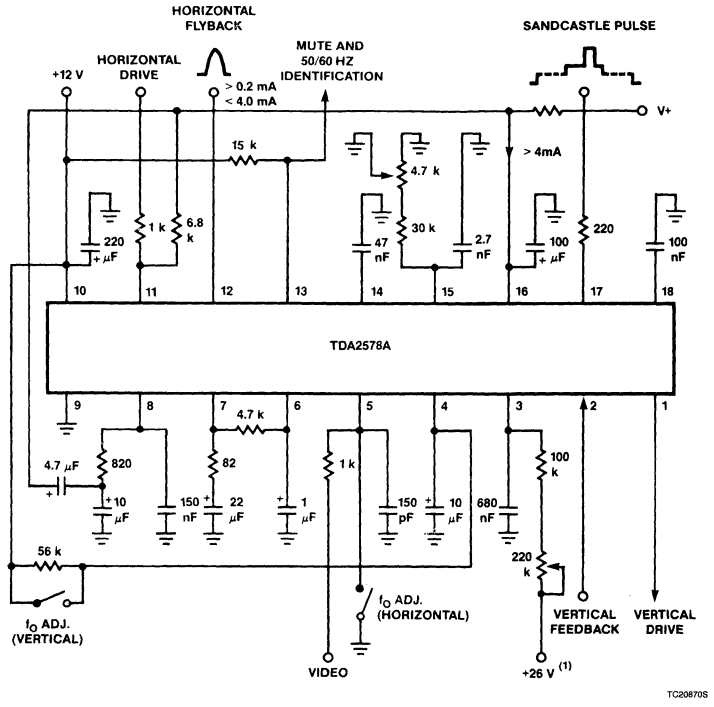


Figure 3. Timing Diagram of the TDA2578A

APPLICATION INFORMATION (Continued)



NOTE:
1. ⩾26V for linear scan.

Figure 4. Typical Application Circuit Diagram; for Application of the TDA2578A With the TDA3651 — See Figure 7

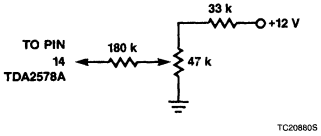
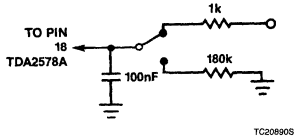


Figure 5. Circuit Configuration at Pin 14 for Phase Adjustment



NOTES:
1kΩ resistor between Pin 18 and + 12V: without mute function.
180kΩ between Pin 18 and ground: with mute function.

Figure 6. Circuit Configuration at Pin 18 for VCR Mode

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APPLICATION INFORMATION (Continued)

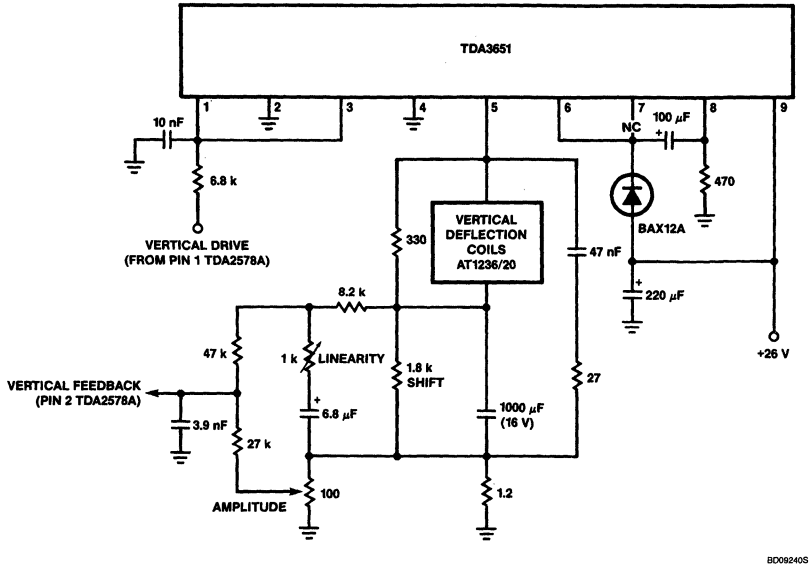

Figure 7. Typical Application Circuit Diagram of the TDA3651 (Vertical Output) When Used in Combination With the TDA2578A, (90° Application)

AN162
A Versatile High-Resolution Monochrome Data and Graphics Display Unit

Application Note

INTRODUCTION

The Data and Graphics Display (DGD) unit, (also referred to as a Video Display Unit), is built for wide ranging applications. It consists of a very high resolution CRT paired with precision deflection coils and all the associated display circuitry, as shown in Figure 1. Using the same printed circuit board and components, it can easily be adapted to operate over a wide range of line and field frequencies with different flyback times in either horizontal (landscape) or vertical (portrait) format.

The possible applications of this unit range from video games to high-resolution displays. However, it is as a computer terminal display device that the DGD will be most useful. Normally, it is the logic design that determines all the parameters to be specified in a computer system, and it is only when the logic circuitry has been finalized that a suitable display is sought. Consequently, the display must be tailormade for the application. There are no signs of any standardization in the future. For this reason the DGD has been designed to allow different dedicated display units to be built up very simply from one basic design.

The DGD is a straightforward and efficient design which will operate with line frequencies of between 15 and 70kHz and field frequencies of 50 to 100Hz, interlaced or non-interlaced. All the design features combine to provide the resolution required for very high density displays (up to 1.5 million picture elements per page). They also ensure a sharp picture right to the screen corners, and allow operation at high horizontal line frequencies without undue temperature rise. A diode-split transformer provides combined line scan and EHT and it is this component which allows changes in line frequency and flyback time to be accomplished very easily.

NOTE:
EHT stands for *extreme haute-tension*, or extreme high voltage.

GENERAL DESCRIPTION

Figure 2 shows a block diagram of the DGD unit and its auxiliary circuits. (The unit is to the right of the broken line, with the auxiliary circuits to the left.) The circuit diagram is shown in Figure 3.

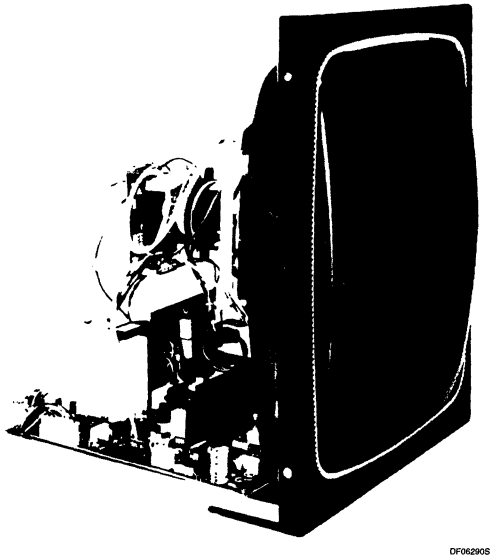

Figure 1. DGD Unit

The normal DGD requirements of good raster geometry and minimal loss of display quality between the screen center and corners are even more important in high-definition systems. To ensure a display offering the best possible resolution over the whole line frequency range, the unit uses high-quality purpose-designed deflection coils type AT1039. These are paired with either the 12 in (M31-326) or 15 in (M38-328) picture tubes. These coils have been designed using recently developed techniques to give good deflection performance and raster geometry suitable for correction by built-in magnets. For the 12 in tube, type AT1039/03 deflection coils are used. Two types of coil are available for the 15 in tube, the AT1039/00 which has been optimized for portrait (vertical) formats and the AT1039/01 for landscape (horizontal) displays. Terminations to each coil are brought out separately to allow for both series and parallel connections.

Both line scanning and EHT are provided by a purpose-built diode-split transformer. It is the flexibility of this device which produces the extreme versatility of the DGD unit as a whole and allows operation of the wide range of line frequencies and flyback times. In addition, all auxiliary power supply requirements are obtained from the same transformer. The primary is provided with several taps, each of which corresponds to a different peak voltage and hence flyback time. By careful positioning of these transformer primary taps, and by utilizing both parallel and series connection of the line deflection coils, a wide variety of flyback times can be accomodated in steps. Each step allows sensible values of flyback ratio for the different line frequencies. Apart from the selection of the correct transformer tap, the only other components that may need to be changed in order to use a different line frequency are the oscillator timing capacitor C6, S-correction capacitor C22, base drive resistor R52, linearity control L1, and heater resistor R84 (see Figure 3).

Although deflection defocusing has been minimized by careful design of the line deflection coils, there is still some focusing action in the deflection process. Also, there is a difference between the electron beam path lengths for axial beams and those deflected to the tube corners. These effects combine to produce a change in focus requirements from the center to the edges of the picture tube. To overcome this, dynamic focus is employed. The active dynamic focus circuit applies parabolic cor-

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

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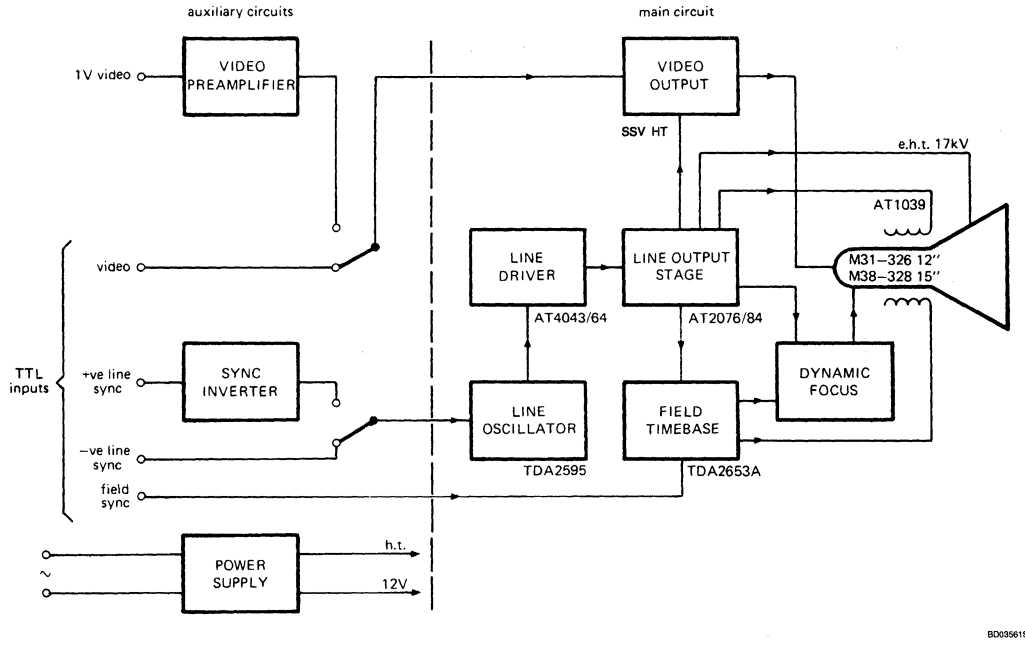

Figure 2. DGD Unit Block Diagram

rection in both the line and field directions to give precise focus over the whole raster. Because the electron gun is a unipotential type, the tube has a fairly flat focus characteristic. The amplitude of the dynamic focus can therefore be preset and adjustment is unnecessary.

Width control is accomplished with a series-parallel inductance arrangement which does not affect the flyback time or EHT. Adjustable picture shift is supplied in both the line and field directions by passing DC through the appropriate deflection coils.

The TDA2595 line oscillator combination IC provides the correct waveforms to drive the line output transistor via a transformer-coupled driver stage. This IC includes both the line oscillator and coincidence detector, a line flyback pulse, obtained from the collector of the line output transistor TR2, is required for phase detection. A protection circuit which turns off the output drive if the voltage at Pin 8 is either below 4 or above 8V is used to provide overvoltage protection for the line output stage.

All the field timebase functions are converted by the TDA2653A IC. It takes a positive-going field sync input at TTL level and drives the impedance-matched AT-1039 deflection coils in series connection. A field blanking pulse, which may be used for screen burn protection, is available from Pin 2. The IC is contained in a 13-lead DIP plastic power encapsulation type SOT-141, which offers straightforward heatsinking.

An emitter-driven video output stage is used with output transistor TR6 and driver TR7. The collector load resistors R87 and R88 with peaking coil L5 and some compensation in the emitter circuit ensure a bandwidth of 60MHz at 35V, measured at the cathode. In order to minimize stray capacitance, the video amplifier is placed on the tube-base printed circuit board close to the cathode pin of the tube. The 55V HT (High Tension) line is provided from the line output stage.

The unit will accept video input at TTL level with positive-going field sync and negative-going line sync. However, inputs at other levels and polarities may be accepted by using the auxiliary circuits, as shown in Figure 2.

The main HT line input will depend upon the line frequency and varies from about 30 to 150V. If lower values of HT are preferred, a floating tap will accommodate a series boosted circuit arrangement.

A 12V supply is required at all frequencies. The total power consumption of the unit is about 40W.

Standard measures are taken to protect the circuitry in the event of a picture tube flashover. Spark gaps for all picture tube pins are provided and all are returned to a single point which is, in turn, connected to the outside aquadag layer of the tube and the common earth point.

To achieve a satisfactory stable display with good linearity and one that is free from undesirable modulation, well recognized procedures should be adopted with regard to printed circuit board layout. It is essential that each individual circuit block has its own grounding system connected to a central point on the main printed circuit board which is, in turn, connected to the chassis. Circuit layout within the individual blocks may also be critical.

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

Table 1. DGD Unit Specifications

Picture tube	12 in M31-326 series 15 in M38-328 series
Deflection coils	AT1039 series
Line output transformer	AT2076/84
Character display	Up to 1.5×10^6 pixels
Line frequency landscape format portrait format	 15 to 50kHz 15 to 70kHz
Field frequency non-interlaced or interlaced	 50 to 100Hz
EHT	17kV
Line linearity	Better than 3%
Field linearity	Better than 3%
Raster breathing (0 to 100μA)	 Better than 2%
Line flyback time	3 to 9μs
Field flyback time	0.6ms
Video bandwidth (at 35V output measured at the cathode)	 60MHz
Input signals	Positive field sync at TTL level, negative line sync at TTL level, video input at TTL level
Power input	40W total 30 to 150V 36W 12V 4W

Originally published as "Technical Publication 115," ELCOMA, The Netherlands, 1983.

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

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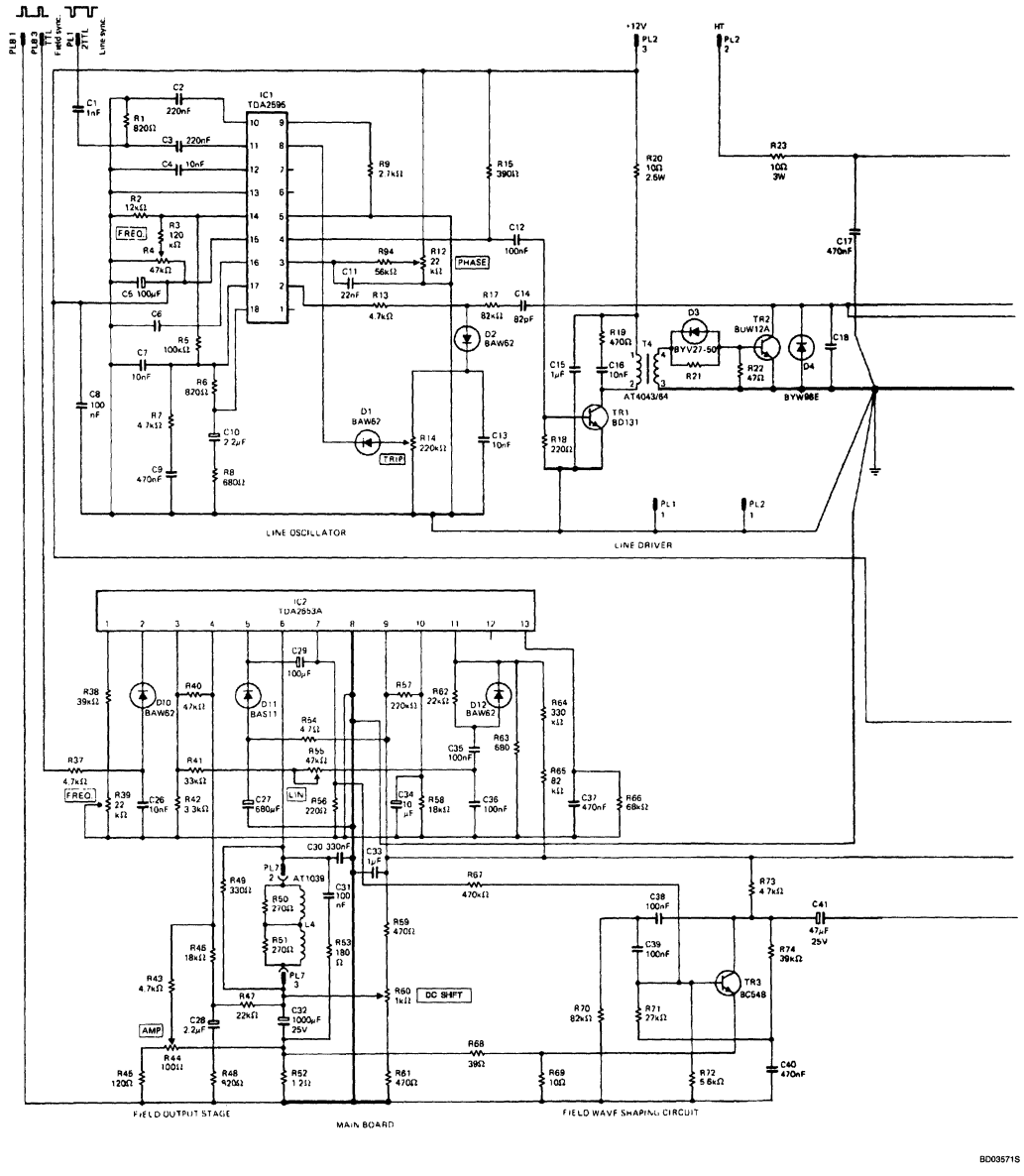

Figure 3. Data and Graphics Display Unit Circuit Diagram

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

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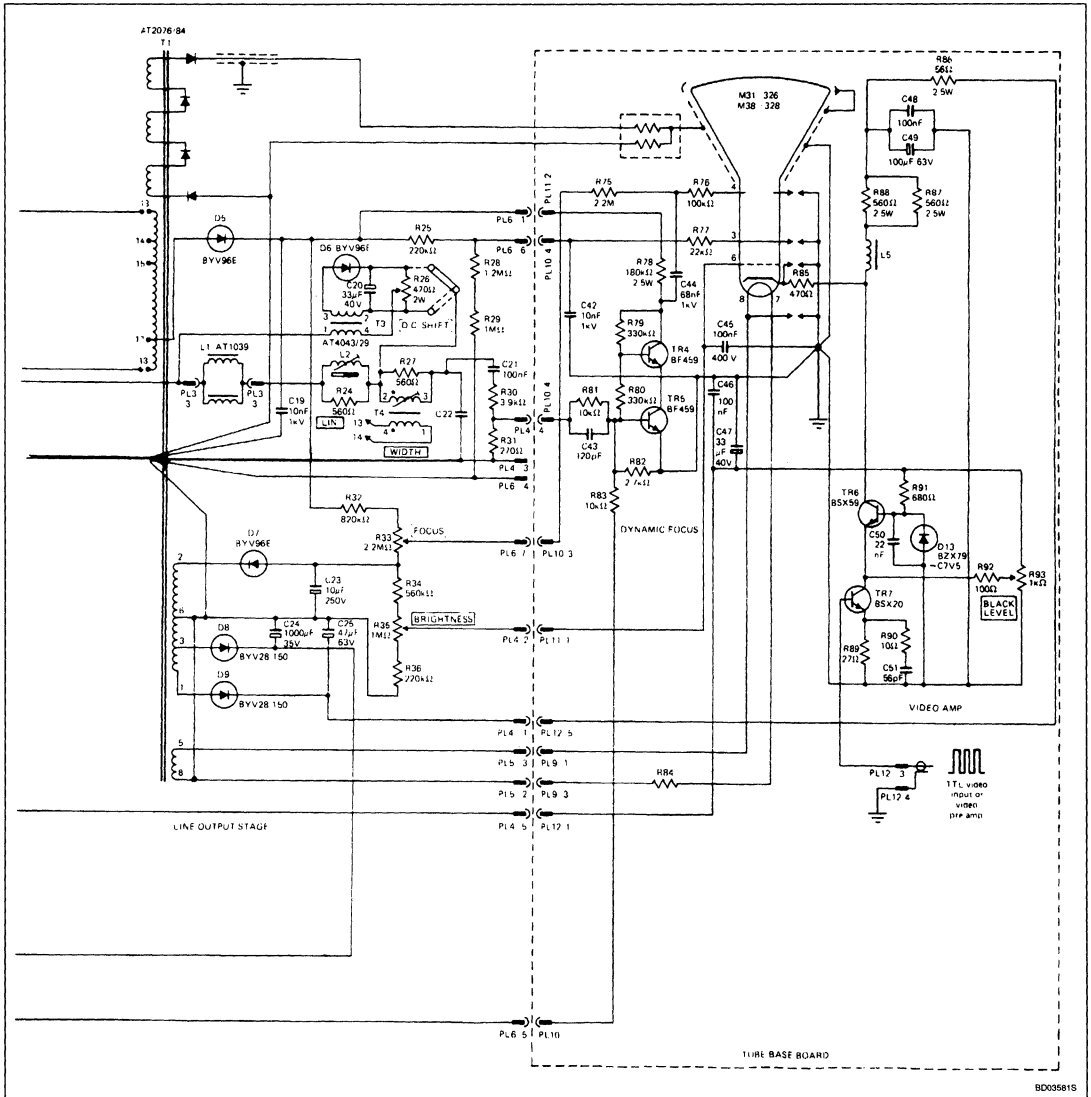

Figure 3. Data and Graphics Display Unit Circuit Diagram (Continued)

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AN1621
TDA2578A/TDA3651 PCB Layout Directives

Application Note

The TDA2578A is a sync separator and horizontal/vertical synchronization circuit while the TDA3651 is a vertical deflection output driver.

This application note covers general directives for the circuit and PCB layout to achieve stable horizontal time stability and correct vertical interface.

The TDA2578A combines both a horizontal oscillator/PLL and a vertical oscillator/PLL. When used in conjunction with a TDA3651 vertical driver, high system loop gains are involved. This requires careful attention to ground points and consideration to magnetic fields within the receiver/monitor design.

GENERAL PCB LAYOUT DIRECTIVES

- Each IC and discrete component should be surrounded by a good ground plane (See Figure 1).
- The ground plane should not be a complete closed-loop. This is to avoid ground plane-induced currents created by magnetic fields.
- All circuit peripheral components should be connected to the ground plane.
- All high current points should be grounded on another ground plane (double-sided PCB).
- Each IC circuit should have its own common "solid" ground point and should be connected to the other circuitry so that no "strange" ground plane currents are injected.
- Input leads should be short and direct to avoid cross-coupling by both electrostatic and electromagnetic fields.
- A small value resistor in series with input leads can decrease flashover IC failure problems
- Position components with respect to leakage fields of the horizontal line output transformer.

TDA2578A PCB CONSIDERATION

- Grounding point of vertical oscillator timing capacitor (Pin 3 & ground) should be connected to the Pin 9 ground pin, *not* via a PCB trace which carries either large horizontal line currents or video information.
- The vertical feedback voltage input (Pin 2) decoupling capacitor should be connected to the same PCB trace as the vertical oscillator timing capacitor.
- The vertical feedback input (Pin 2) has a very high input impedance; therefore, the scaling resistors should be situated close to Pin 2 to prevent parasitic capacitive horizontal line cross-coupling.
- The vertical integrator capacitor (Pin 4) can carry high peak currents up to 30mA during vertical interval. Therefore it should be firmly grounded to Pin 9, *not*, however, by the same ground PCB trace as used by the vertical oscillator timing capacitor.
- The TDA2578A horizontal output (Pin 11) to drive the base of the horizontal output transistor should be restricted to 30mA peak. This prevents disturbing voltage drops on the TDA2578A ground lead which can result in an offset voltage to the vertical comparator.
- Special attention is required when capacitive coupling is used to drive the horizontal output transistor.
- Vertical interlace is strongly influenced by parasitic signals when coincidence occurs between the vertical oscillator flyback and the horizontal blanking interval. Coincidence is determined by slicing in the vertical integrator and the pre-adjustment of the vertical oscillator.
- Decoupling of the supply voltages (Pins 10 and 16) should be kept as short and direct to the ground pin (Pin 9) as possible. Ripple on the supplies should be less than 1%.

TDA3651 PCB LAYOUT CONSIDERATIONS

- The vertical deflection current loop should be short and be of low impedance, i.e., ample PCB traces on Pin 5 deflection coil, coupling capacitor, and connection to the feedback resistor on Pin 4.
- Damping components and horizontal line suppression across the yoke deflection coil should be located as close as possible to the deflection coil connector.
- Horizontal line information modulated on the vertical waveform at Pin 5 should not exceed $1V_{P-P}$. This is usually caused by:
  1. Inductive & capacitive coupling across the yoke coils.
  2. Capacitive coupling within vertical control loop.
  3. Inductive magnetic coupling.
  4. Supply voltage variations.
- Vertical input (Pin 1) requires a bypass capacitor of 10pF to ground (Pin 2) to suppress the IC current noise.
- Feedback capacitance of 220pF from Pin 1 (input) and Pin 5 (output) improves loop stability.
- Supply voltage decoupling (Pin 9) should be connected directly to ground (Pin 4).
- The supply to both the TDA2578A and the TDA3651 should be decoupled at the source to remove any extraneous noise.

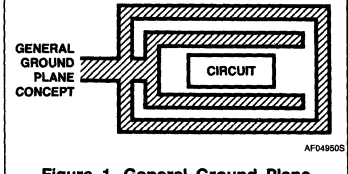


Figure 1. General Ground Plane Concept

Signetics

TDA2579
Synchronization Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA2579 generates and synchronizes horizontal and vertical signals. The device has a 3-level sandcastle output, a transmitter identification signal and also 50/60Hz identification.

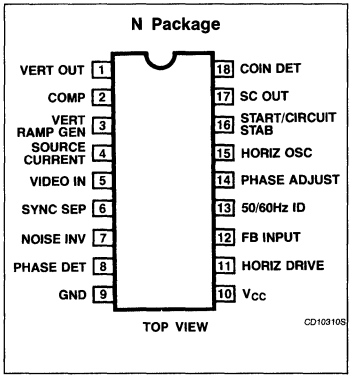
FEATURES

- **Horizontal phase detector, (sync to osc), sync separator and noise inverter**
- **Triple current source in the phase detector with automatic selection**
- **Inhibit of horizontal phase detector and video transmitter identification**
- **Second phase detector for storage compensation of the horizontal output stage**
- **Stabilized direct starting of the horizontal oscillator and output stage**
- **Horizontal output pulse with constant duty cycle value of 29μs**
- **Duty factor of the horizontal output pulse is 50% when horizontal flyback pulse is absent**
- **Internal vertical sync separator and two integration selection times**
- **Divider system with three different reset enable windows**
- **Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified**
- **Vertical comparator with a low DC feedback signal**
- **50/60Hz identification output combined with mute function**
- **Automatic amplitude adjustment for 50 and 60Hz and blanking pulse duration**

APPLICATIONS

- **Video terminals**
- **Television**
- **Video tape recorder**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-102HE)	0 to +70°C	TDA2579N

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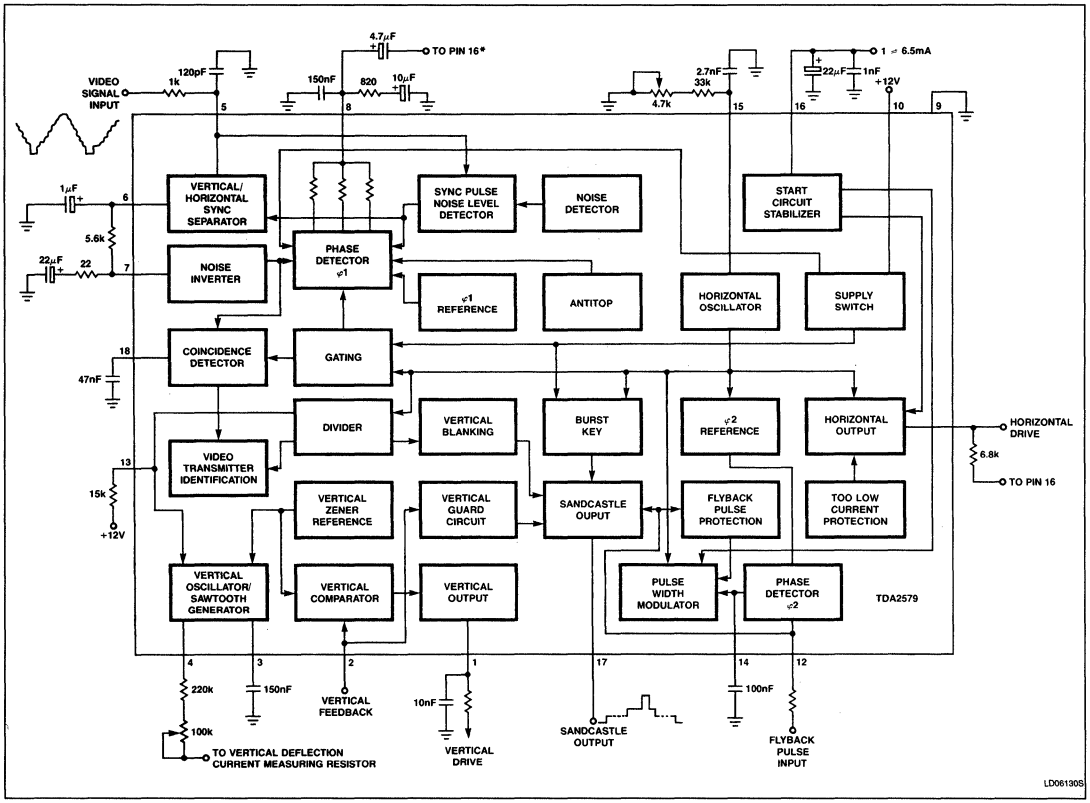
Synchronization Circuit TDA2579

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
I_{16}	Start current	10	mA
V_{10}	Supply voltage	13.2	V
P_{TOT}	Power dissipation	1.2	W
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient in free air	50	°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
I_{16}	Supply current, Pin 16 $V_{10} = 0V$	6.5		10	mA
I_{16}	Supply current, Pin 16 $V_{10} = 9.5V$	2.5		10	mA
V_{16}	Stabilized voltage, Pin 16	8.1	8.7	9.3	V
I_{10}	Current consumption, Pin 10		68	85	mA
V_{CC}	Supply voltage range, Pin 10	9.5	12	13.2	V
Video input (Pin 5)					
V_5	Top sync. level	1.5	3.1	3.75	V
V_5	Sync. pulse amplitude[1]	0.1	0.6	1	V_{CC}
	Slicing level[2]	35	50	65	%
	Delay between video input and det. output (see also Figure 2)	0.2	0.3	0.5	μs
	Sync. pulse noise level detector circuit active		600		mV_{TT}
Sync. Pulse					
	Noise level detector circuit hysteresis		3		dB
Noise gate (Pin 5)					
V_5	Switching level		+0.7	+1	V
First control loop (Pin 8) (Horizontal osc. to sync.)					
Δf	Holding range		±800		Hz
Δf	Catching range	±600	±800	±1100	Hz
	Control sensitivity video with respect to burstkey and flyback pulse				
	Slow time constant		2.5		$kHz/\mu s$
	Normal time constant		10		$kHz/\mu s$
	Fast time constant		5		$kHz/\mu s$
	Phase modulation due to hum on the supply line Pin 10[3]		0.2		$\mu s/V_{TT}$
	Phase modulation due to hum on input current Pin 16[3]		0.08		$\mu s/mA_{TT}$
Second control loop (Pin 14) (Horizontal flyback to horizontal oscillator)					
$\Delta t_d/\Delta t_o$	Control sensitivity $t_D = 10\mu s$	200	300	600	μs
t_D	Control range	1		> 45	μs
t_D	Control range for constant duty cycle horizontal output	1	29 (–t flyback pulse)		
	Controlled edge of horizontal output signal Pin 11		positive		
Phase adjustment (Pin 14) (via second control loop)					
	Control sensitivity $t_D = 10\mu s$		25		$\mu A/\mu s$
I_{14}	Maximum allowed control current			±60	μA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal oscillator (Pin 15) ($C = 2.7nF$; $R_{OSC} = 33k\Omega$					
f	Frequency (no sync.)		15625		Hz
Δf	Spread (fixed external component, no sync.)			±4	%
Δf	Frequency deviation between starting point output signal and stabilized condition		+5	+8	%
TC	Temperature coefficient		10		°C
Horizontal output (Pin 11) (Open-collector)					
V_{11}	Output voltage high			13.2	V
V_{11}	Start voltage protection (internal zener diode)	13		15.8	V
I_{16}	Low input current Pin 16 protection output enabled		5.5	6.5	mA
V_{11}	Output voltage low start condition ($I_{11} = 10mA$)		0.1	0.5	V
	Duty cycle output current during starting $I_{16} = 6.5mA$	55	65	75	%
V_{11}	Output voltage low normal condition ($I_{11} = 25mA$)		0.3	0.5	V
	Duty cycle output current without flyback pulse Pin 12	45	50	55	%
	Duration of the output pulse high $t_D = 8\mu s$	27	29	31	μs
	Controlled edge		positive		
	Temperature coefficient horizontal output pulse		−0.05		$\mu s/°C$
Sandcastle output signal (Pin 17) ($I_{LOAD} = 1mA$)					
	Output voltage during:				
V_{17}	burstkey	9.75	10.6		V
V_{17}	horizontal blanking	4.1	4.5	4.9	V
V_{17}	vertical blanking	2	2.5	3	V
V_{17}	Zero level output voltage $I_{SINK} = 0.5mA$			0.7	V
	Pulse width:				
t_P	burstkey	3.45	3.75	4.1	μs
V_{12}	horizontal blanking		1		V
	Phase position burstkey Time between middle synchronization pulse at Pin 5 and start burst at Pin 17	2.3	2.7	3.1	μs
	Time between start sync. pulse and end of burst pulse, Pin 17			9.2	μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Coincidence detector, video transmitter identification circuit and time constant switching levels (see also Figure 1)					
I_{18}	Detector output current		0.25		mA
V_{18}	Voltage level for in sync. condition (φ1 normal)		6.5		V
V_{18}	Voltage for noisy sync. pulse (φ1 slow and gated)	9	10		V
V_{18}	Voltage level for noise only[5]		0.3		V
V_{18}	Switching level normal-to-fast	3.2	3.5	3.8	V
V_{18}	Switching level Mute output active and fast-to-slow	1.0	1.2	1.4	V
V_{18}	Switching level frame period counter (3 periods fast)	0.08	0.12	0.16	V
V_{18}	Switching level Slow-to-fast (locking) Mute output inactive	1.5	1.7	1.9	V
V_{18}	Switching level fast-to-normal (locking)	4.7	5.0	5.3	V
V_{18}	Switching level normal-to-slow (gated sync. pulse)	7.4	7.8	8.2	V
Video transmitter identification output (Pin 13)					
V_{13}	Output voltage active (no sync., $I_{13} = 2mA$)		0.15	0.32	V
I_{13}	Sink current active (no sync.), $V_{13} < 1V$			5	mA
I_{13}	Output current inactive (sync. 50Hz)			1	μA
50/60Hz identification (Pin 13) (R_{13} positive supply 15kΩ)					
V_{13}	Emitter-follower, PNP 60Hz: $\frac{2 \times fH}{fV}$ < 576 voltage	7.2	7.65	8.1	V
V_{13}	50Hz: $\frac{2 \times fH}{fV}$ > 576 voltage		V_{10}		V
Flyback input pulse (Pin 12)					
V_{12}	Switching level		+1		V
I_{12}	Input current	+0.2		+4	mA
V_{12}	Input pulse			12	V_{CC}
R_{IN}	Input resistance		3		kΩ
	Phase position without shift				
t_D	Time between the middle of the sync. pulse at Pin 5 and the middle of the horizontal blanking pulse of Pin 17		2.5		μs
Vertical ramp generator (Pin 3)					
	Pulse width charge current		26		clock pulses
I_3	Charge current		3		mA
	Top level ramp signal voltage				
V_3	Divider in 50Hz mode[6]	5.1	5.5	5.9	V
V_3	Divider in 60Hz mode[6]	4.35	4.7	5.05	V
	Ramp amplitude $C_3 = 150nF$, $R_4 = 330k\Omega$, 50Hz[6] $R_4 = 330k\Omega$, 60Hz[6]		3.1 2.5		V_{CC} V_{CC}

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $I_{16} = 6.5mA$; $V_{10} = 12V$, unless otherwise specified. Voltage measurements are taken with respect to Pin 9 (ground).

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Current source (Pin 4)					
$V_{4.9}$	Output voltage $I_4 = 20\mu A$	6.6	7.1	7.6	V
I_4	Allowed current range	10		55	μA
	Temperature coefficient output voltage				
TC	$I_4 = 20\mu A$		+50		$10^{-6}/°C$
TC	$I_4 = 40\mu A$		+20		$10^{-6}/°C$
TC	$I_4 = 50\mu A$		−40		$10^{6}/°C$
Comparator (Pin 2) $C_3 = 150nF$; $R_4 = 330k\Omega$					
	Input voltage				
V_{2-9}	DC level[6]	0.9	1	1.1	V
V_{2-9}	AC level		0.8		V_{CC}
	Deviation amplitude 50/60Hz			2.5	%
	Vertical output stage, Pin 1 (NPN) emitter follower				
V_{1-9}	Output voltage I_O Pin 1 = +1.5mA	4.8	5.2	5.6	V
R_S	Sync. separator resistor		160		Ω
	Continuous sink current		0.25		mA
Vertical guard circuit (Pin 2) Active ($V_{17} = 2.5V$)					
V_2	Switching level low[6]	> 1.7	1.9	2.1	V
V_2	Switching level high[6]	< 0.3	0.4	0.5	V

NOTES:

1. Up to $1V_{P-P}$ the slicing level is constant, at amplitudes exceeding $1V_{P-P}$ the slicing level will increase.
2. The slicing level is fixed by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100\% \quad (R_S \text{ value in } k\Omega)$$

3. Measured between Pin 5 and sandcastle output Pin 17.
4. Divider in search (large) mode:
   start: reset divider = start vertical sync. plus 1 clock pulse
   stop:

$$n = \frac{2 \times fH}{fV} > 576 \text{ clock pulse } 42$$

$$n = \frac{2 \times fH}{fV} < 576 \text{ clock pulse } 34$$

   Divider in small window mode:
   start: clock pulse 517 (60Hz) clock pulse 619 (50Hz)
   stop: clock pulse 34 (60Hz) clock pulse 42 (50Hz)
5. Depends on DC level of Pin 5, given value is valid for $V_5 \approx 5V$.
6. Value related to internal zener diode reference voltage source spread includes the complete spread of reference voltage.

FUNCTIONAL DESCRIPTION

Vertical Part (Pins 1, 2, 3, 4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at Pin 3. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency and one line period equals 2 clock pulses. Due to the divider system, no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60Hz to 50Hz system. The divider system operates with 3 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its counter value by 1 for each time the separated vertical sync. pulse is within the searched window. The count is reduced by 1 when the vertical sync. pulse is not present.

Large (Search) Window: Divider Ratio Between 488 and 722

This mode is valid for the following conditions:

1. Divider is looking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Non-standard TV-signal condition detected while a double or enlarged vertical sync. pulse is still found after the internally-generated antitop flutter pulse has ended. This means a vertical sync. pulse width larger than 8 clock pulses (50Hz), that is, 10 clock pulses (60Hz). In general this mode is activated for video tape recorders operating in the feature/trick mode.
4. Up/down counter value of the divider system operating in the narrow window mode drops below count 1.
5. Externally setting. This can be reached by loading Pin 18 with a resistor of 180kΩ to earth or connecting a 3.6V diode stabistor between Pin 18 and ground.

Narrow Window: Divider Ratio Between 522 – 528 (60Hz) or 622 – 628 (50Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync. pulses. When the divider operates in this mode and a vertical sync. pulse is missing within the window, the divider is reset at the end of the window and the counter value is lowered by 1. At a counter value below count 1 the divider system switches over to the large window mode.

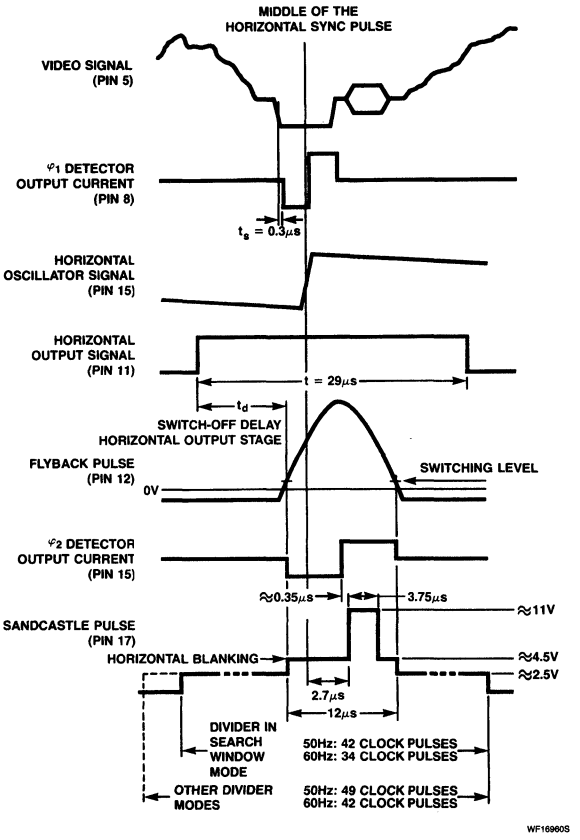


Figure 1. Timing Diagram of the TDA2579

Standard TV Norm

When the up/down counter has reached its maximum value of 12 in the narrow window mode, the information applied to the up/down counter is changed such that the standard divider ratio value is tested. When the counter has reached a value of 14, the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync. pulse is missing. A missed vertical sync. pulse lowers the counter value by 1. When the counter reaches the value of 10, the divider system is switched over to the large window mode. The standard TV norm condition gives maximum protection for video recorders playing tapes with anti-copy guards.

No TV Transmitter Found: (Pin 18 < 1.2V)

In this condition, only noise is present, the divider is reset to count 628. In this way a stable picture display at normal height is achieved.

Video Tape Recorders in Feature Mode

It should be noted that some VTRs operating in the feature modes, such as picture search, generate such distorted pictures that the no TV transmitter detection circuit can be activated as Pin V_{18} drops below 1.2V. This would imply a rollowing picture (condition d). In general, VTR machines use a reinserted vertical sync. pulse in the feature mode. Therefore, the divider system has been made such that the automatic reset of the divider at count 628 when V_{18} is below 1.2V is inhibited when a vertical sync. pulse is detected.

The divider system also generates the anti-top flutter pulse which inhibits the phase 1 detector during the vertical sync. pulse. The width of this pulse depends on the divider mode. For the divider mode a, the start is

generated at the reset of the divider. In modes b and c, the anti-top flutter pulse starts at the beginning of the first equalizing pulse. The anti-top flutter pulse ends at count 8 for 50Hz and count 10 for 60Hz. The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34 (17 lines for 60Hz, and at count 42 (21 lines) for 50Hz systems. The vertical blanking pulse generated at the sandcastle output Pin 17 is made by adding the anti-top flutter pulse and the blank pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b or c mode. For generating a vertical linear sawtooth voltage a capacitor should be connected to Pin 3. The recommended value is 150nF to 330nF (see Block Diagram).

The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is activated also at reset. When the capacitor has reached a voltage value of 5.5V for the 50Hz system or 4.7V for the 60Hz system the voltage is kept constant until the charging period ends. The charge period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an NPN transistor current source, the value of which can be set by an external resistor between Pin 4 and ground (Pin 9). Pin 4 is connected to a PNP transistor current source which determines the current of the NPN current source. The PNP current source on Pin 4 is connected to an internal zener diode reference voltage which has a typical voltage of ≈ 7.1V. The recommended operating current range is 10 to 50μA. The resistance at pin R_4 should be 140 to 700kΩ. By using a double current mirror concept the vertical sawtooth pre-correction can be set on the desired value by means of external components between Pin 4 and Pin 3, or by connecting the Pin 4 resistor to the vertical current measuring resistor of the vertical output stage. The vertical amplitude is set by the current of Pin 4. The vertical feedback voltage of the output stage has to be applied to Pin 2. For the normal amplitude adjustment the values are DC = 1V and AC = 0.8V. Due to the automatic system adaption both values are valid for 50Hz and 60Hz.

The low DC-voltage value improves the picture bounce behaviour as less parabola compensation is necessary. Even a fully DC-coupled feedback circuit is possible.

Vertical Guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on Pin 2. When the level on Pin 2 is below 0.4V or higher than 1.9V, the guard circuit inserts a continuous level of 2.5V in the sandcastle output signal of Pin 17. This results in the blanking of the picture displayed, thus preventing a burnt-in horizontal line. The guard levels specified refer to the zener diode reference voltage source level.

Driver Output

The driver output is at Pin 1, it can deliver a drive current of 1.5mA at 5V output. The internal impedance is about 150Ω. The output pin is also connected to an internal current source with a sinking current of 0.25mA.

Sync. Separator, Phase Detector and TV Station Identification, (Pins 5, 6, 7, 8, and 18)

The video input signal is connected to Pin 5. The sync. separator is designed such that the slicing level is independent of the amplitude of the sync. pulse. The black level is measured and stored in the capacitor at Pin 7. The slicing level value is stored in the capacitor at Pin 6. The slicing level value can be chosen by the value of the external resistor between Pins 6 and 7. The value is given by the formula:

$$P = \frac{R_S \times 100}{5.3 + R_S} \quad (R_S \text{ value in } k\Omega)$$

Where R_S is the resistor between Pins 6 and 7 and top sync. level equals 100%. The recommended resistor value is 5.6kΩ.

Black Level Detector

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty cycle of 50% and the flyback pulse at Pin 12. In this way the TV transmitter identification operates also for all DC conditions at input Pin 5 (no video modulation, plain carrier only).

During the frame interval the slicing level detector is inhibited by a signal which starts with the anti-top flutter pulse and ends with the reset vertical divider circuit. In this way shift of the slicing level due to the vertical sync. signal is reduced and separation of the vertical sync. pulse is improved.

Noise Inverter

An internal noise inverter is activated when the video level at Pin 5 drops below 0.7V. The IC embodies also a built-in sync. pulse noise level detection circuit. This circuit is directly connected to Pin 5 and measures the noise level at the middle of the horizontal sync. pulse. When a noise level of 600mV_{P-P} is detected, a counter circuit is activated. A video input signal is processed as "acceptable noise-free" when 12 out of 16 sync. pulses have a noise level below 600mV for two succeeding frame periods. The sync. pulses are processed during a 16 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of about 150mV (≈ 3dB).

When the "acceptable noise-free" condition is found, the phase detector of Pin 8 is switched to not-gated and normal time constant. When a higher sync. pulse noise level is found, the phase detector is switched over to slow time constant and gated sync. pulse phase detection. At the same time the integration time of the vertical sync. pulse separator is adapted.

Phase Detector

The phase detector circuit is connected to Pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of Pin 18 and the state of the sync. pulse noise detection circuit.

All three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top flutter pulse period, and the separated vertical sync. pulse time.

As a result, phase jumps in the video signal related to video head takeover of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period, the phase detector time constant is lowered by 2.5 times. In this way no need for external VTR time constant switching exists, so all station numbers are suitable for signals from VTR, video games or home computers.

For quick locking of a new TV station starting from a noise-only signal condition (normal time constant), a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage drop below 0.1V at Pin 18. This will activate a frame period counter which switches the phase detector to fast for 3 frame periods.

Horizontal Oscillator

The horizontal oscillator will now lock to the new TV station and as a result, the voltage on Pin 18 will increase to about 6.5V. When Pin 18 reaches a level of 1.8V the mute output transistor of Pin 13 is switched off and the divider is set to the large window. In general the mute signal is switched off within 5ms (pin C_{18} = 47nF) after reception of a new TV signal. When the voltage on Pin 18 reaches a level of 5V, usually within 15ms, the frame counter is switched off and the time constant is switched from fast to normal.

If the new TV station is weak, the sync. noise detector is activated. This will result in a changeover of Pin 18 voltage from 7V to ≈ 10V. When Pin 18 exceeds the level of 7.8V the phase detector is switched to slow time constant and gated sync. pulse condition.

When desired, most conditions of the phase detector can also be set by external means in the following way:

a. Fast time constant TV transmitter identification circuit not active, connect Pin 18 to earth (Pin 9).

b. Fast time constant TV transmitter identification circuit active, connect a resistor of 180kΩ between Pin 18 and ground. This condition can also be set by using a 3.6V stabistor diode instead of a resistor.

c. Slow time constant, (with exception of frame blanking period), connect Pin 18 via a resistor of 10kΩ to +12V, Pin 10. In this condition the transmitter identification circuit is not active.

d. No switching to slow time constant desired (transmitter identification circuit active), connect a 6.8V zener diode between Pin 18 and ground.

Figure 2 illustrates the operation of the 3 phase detector circuits.

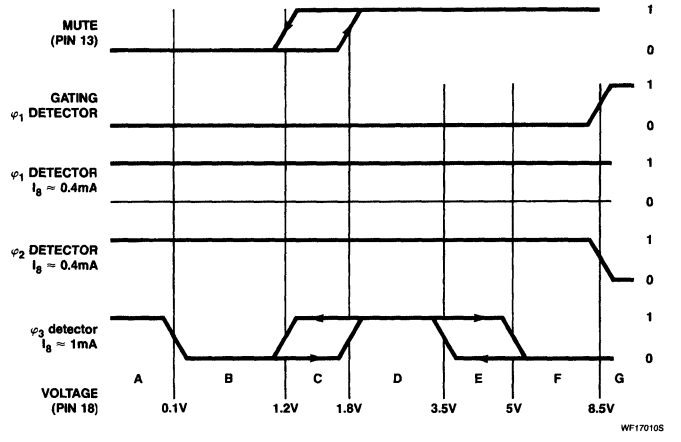


Figure 2. Timing Diagram, Phase Detectors.

Supply (Pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage can start operating by application of a very low supply current into Pin 16.

The horizontal oscillator starts at a supply current of about 4.5mA. The horizontal output stage is forced into the non-conducting stage until the supply current has a typical value of 5.5mA. The circuit has been designed so that after starting the horizontal output function a current drop of ≈ 1mA is allowed. The starting circuit gives the possibility to derive the main supply (Pin 10), from the horizontal output stage. The horizontal output signal can also be used as the oscillator signal for synchronized switch-mode power supplies. The maximum allowed starting current is 10mA. The main supply should be connected to Pin 10, and Pin 9 should be used as ground. When the voltage on Pin 10 increases from zero to its final value (typically 12V) a part of the supply current of the starting circuit is taken from Pin 10 via internal diodes, and the voltage on Pin 16 will stabilize to a typical value of 8.7V.

In stabilized condition (Pin $V_{10} > 9.5V$) the minimum required supply current to Pin 16 is ≈ 2.5mA. All other IC functions are switched on via the main supply voltage on Pin 10. When the voltage on Pin 10 reaches a value of ≈ 7V the horizontal phase detector circuit is activated and the vertical ramp on Pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on Pin 10 reaches the stabilized voltage value of Pin 16 which is typically 8.7V.

For closing the second phase detector loop, a flyback pulse must be applied to Pin 12. When no flyback is detected, the duty cycle of the horizontal output stage is 50%.

For remote switch-off Pin 16 can be connected to ground (via an NPN transistor with a series resistor of ≈ 500Ω) which switches off the horizontal output.

Horizontal Oscillator, Horizontal Output Transistor, and Second Phase Detector (Pins 11, 12, 14 and 15)

The horizontal oscillator is connected to Pin 15. The frequency is set by an external RC combination between Pin 15 and ground, Pin 9. The open collector horizontal output stage is connected to Pin 11. An internal zener diode configuration limits the open voltage of Pin 11 to ≈ 14.5V.

The horizontal output transistor at Pin 11 is blocked until the current into Pin 16 reaches a value of ≈ 5.5mA.

A higher current results in a horizontal output signal at Pin 11, which starts with a duty cycle of ≈ 35% HIGH.

The duty cycle is set by an internal current source-loaded NPN emitter-follower stage connected to Pin 14 during starting. When Pin 16 changes over to voltage stabilization, the NPN emitter-follower and current source load at Pin 14 are switched off and the second phase detector circuit is activated, provided a horizontal flyback pulse is present at Pin 12. When no flyback pulse is detected at Pin 12 the duty cycle of the horizontal output stage is set to 50%.

The phase detector circuit at Pin 14 compensates for storage time in the horizontal deflection output stage. The horizontal output pulse duration in 29μs HIGH for storage times between 1μs and 17μs (29μs flyback pulse of 12μs). A higher storage time increases the HIGH time. Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor of Pin 14.

Mute Output and 50/60Hz Identification (Pin 13)

The collector of an NPN transistor is connected to Pin 13. When the voltage on Pin 18 drops below 1.2V (no TV transmitter) the NPN transistor is switched ON.

When the voltage on Pin 18 increases to a level of ≈ 1.8V (new TV transmitter found) the NPN transistor is switched OFF.

Pin 13 has also the possibility for 50/60Hz identification. This function is available when Pin 13 is connected to Pin 10 (+12V) via an external pull-up resistor of 10 – 20kΩ. When no TV transmitter is identified, the voltage on Pin 13 will be LOW (< 0.5V). When a TV transmitter with a divider ratio > 576 (50Hz) is detected the output voltage of Pin 13 is HIGH (+12).

When a TV transmitter with a divider ratio < 576 (60Hz) is found an internal PNP transistor with its emitter connected to Pin 13 will force this pin output voltage down to ≈ 7.5V.

Sandcastle Output (Pin 17)

The sandcastle output pulse generated at Pin 17, has three different voltage levels. The highest level, (11V), can be used for burst gating and black level clamping. The second level, (4.5V), is obtained from the horizontal flyback pulse at Pin 12, and is used for horizontal blanking. The third level, (2.5V), is used for vertical blanking and is derived via

the vertical divider system. For 50Hz the blanking pulse duration is 42 clock pulses and for 60Hz it is 34 clock pulses started from the vertical divider reset. For TV signals which have a divider ratio between 622 and 628 or 522 and 528 the blanking pulse is started at the first equalizing pulse.

TYPICAL APPLICATION

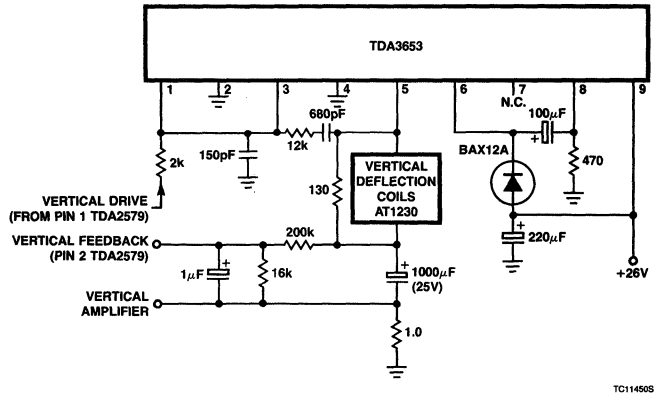


Figure 3

TDA2593
Horizontal Combination

Product Specification

Linear Products

DESCRIPTION

The TDA2593 is a monolithic integrated circuit intended for use in color television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3505, TDA3510, and TDA3520.

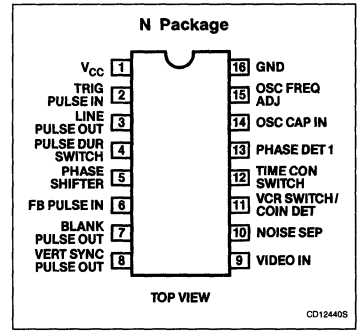
FEATURES

- **Horizontal oscillator based on the threshold switching principle**
- **Phase comparison between sync pulse and oscillator voltage (φ_1)**
- **Internal key pulse for phase detector (φ_1) (additional noise limiting)**
- **Phase comparison between line flyback pulse and oscillator voltage (φ_2)**
- **Larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)**
- **Switch for changing the filter characteristic and the gate circuit (VCR operation)**
- **Sync separator**
- **Noise separator**
- **Vertical sync separator and output stage**
- **Color burst keying and line flyback blanking pulse generator**
- **Phase shifter for the output pulse**
- **Output pulse duration switching**
- **Output stage with separate supply voltage for direct drive of thyristor deflection circuits**
- **Low supply voltage protection**

APPLICATIONS

- **Video monitors**
- **TV receivers**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−20°C to +70°C	TDA2593N

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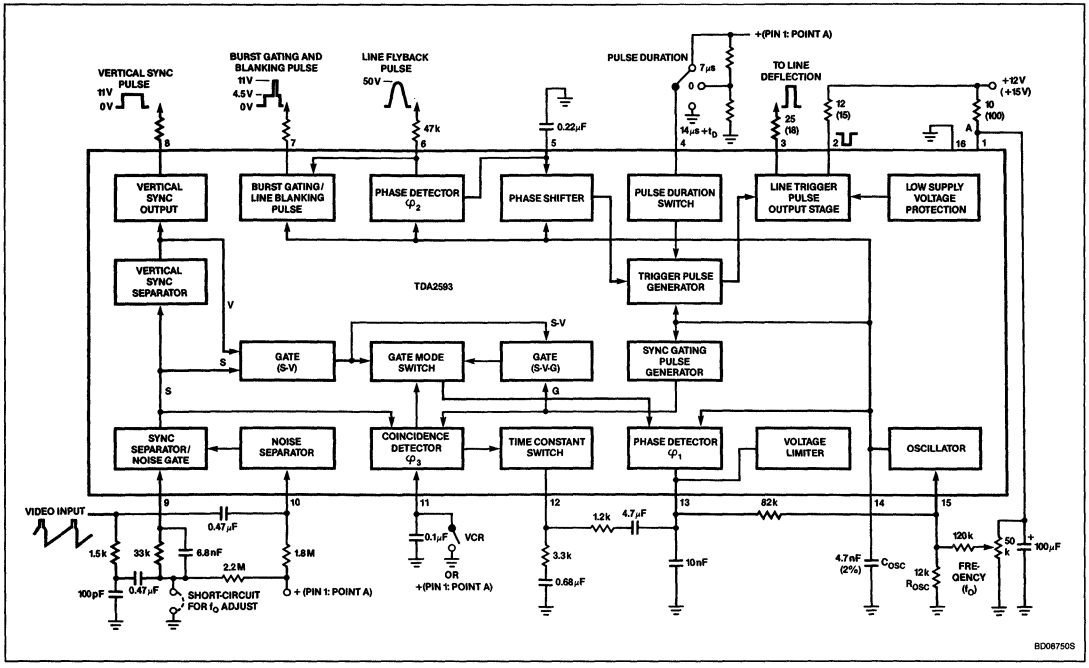
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V_{1-16}	at Pin 1 (voltage source)	13.2	V
V_{2-16}	at Pin 2	18	V
	Voltages		
V_{4-16}	Pin 4	13.2	V
$\pm V_{9-16}$	Pin 9	6	V
$\pm V_{10-16}$	Pin 10	6	V
V_{11-16}	Pin 11	13.2	V
	Currents		
I_{2M}, $-I_{3M}$	Pins 2 and 3 (thyristor driving) (peak value)	650	mA
I_{2M}, $-I_{3M}$	Pins 2 and 3 (transistor driving) (peak value)	400	mA
I_4	Pin 4	1	mA
$\pm I_6$	Pin 6	10	mA
$-I_7$	Pin 7	10	mA
I_{11}	Pin 11	2	mA
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−25 to +125	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS at $V_{CC} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sync separator					
V_{9-16}	Input switching voltage		0.8		V
I_9	Input keying current	5		100	μA
I_9	Input leakage current at $V_{9-16} = -5V$			1	μA
I_9	Input switching current			5	μA
I_9	Switch off current	100	150		μA
$V_{9-16(P-P)}$	Input signal (peak-to-peak value)	3		4	V[1]
Noise separator					
V_{10-16}	Input switching voltage		1.4		V
I_{10}	Input keying current	5		100	μA
I_{10}	Input switching current	100	150		μA
I_{10}	Input leakage current at $V_{10-16} = -5V$			1	μA
$V_{10-16(P-P)}$	Input signal (peak-to-peak value)	3		4	V[1]
$V_{10-16(P-P)}$	Permissible superimposed noise signal (peak-to-peak value)			7	V
Line flyback pulse					
I_6	Input current	0.02	1	2	mA
V_{6-16}	Input switching voltage		1.4		V
V_{6-16}	Input limiting voltage	−0.7		+1.4	V
Switching on VCR					
V_{11-16} V_{11-16}	Input voltage	0 to 2.5 9 to V_{1-16}			V V
$-I_{11}$ I_{11}	Input current			200 2	μA mA
Pulse duration switch for $t = 7\mu s$ (thyristor driving)					
V_{4-16}	Input voltage		9.4 to V_{1-16}		V
I_4	Input current	200			μA
Pulse duration switch for $t = 14\mu s + t_D$ (transistor driving)					
V_{4-16}	Input voltage	0		3.5	V
$-I_4$	Input current	200			μA
Pulse duration switch for $t = 0$; $V_{3-16} = 0$ or input Pin 4 open					
V_{4-16}	Input voltage	5.4		6.6	V
I_4	Input current		0	0	μA
Vertical sync pulse (positive-going)					
$V_{8-16(P-P)}$	Output voltage (peak-to-peak value)	10	11		V
R_8	Output resistance		2		kΩ
t_{ON}	Delay between leading edge of input and output signal		15		μs
t_{OFF}	Delay between trailing edge of input and output signal		t_{on}		μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at V_{CC} = 12V; T_A = 25°C; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Burst gating pulse (positive-going)					
$V_{7-16(P-P)}$	Output voltage (peak-to-peak value)	10	11		V
R_7	Output resistance		70		Ω
t_P	Pulse duration; V_{7-16} = 7V	 3.7	4 4.3		µs µs
t	Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; V_{7-16} = 7V	2.15	2.65	3.15	µs
I_7	Output trailing edge current		2		mA
Line flyback-blanking pulse (positive-going)					
$V_{7-16(P-P)}$	Output voltage (peak-to-peak value)	4	5		V
R_7	Output resistance		70		Ω
I_7	Output trailing edge current		2		mA
Line drive pulse (positive-going)					
$V_{3-16(P-P)}$	Output voltage (peak-to-peak value)		10.5		V
 R_3 R_3	Output resistance for leading edge of line pulse for trailing edge of line pulse		 2.5 20		 Ω Ω
t_P	Pulse duration (thyristor driving) V_{4-16} = 9.4 to V_{1-16} V	5.5	7	8.5	µs
t_P	Pulse duration (transistor driving) V_{4-16} = 0 to 4V; t_{FP} = 12µs		14 + t_D		μs^2
V_{1-16}	Supply voltage for switching off the output pulse		4		V
Overall phase relation					
t	Phase relation between middle of sync pulse and the middle of the flyback pulse		2.6		μs^3
$\lvert\Delta t\rvert$	Tolerance of phase relation			0.7	µs
$\Delta I_5/\Delta t$	The adjustment of the overall phase relation and consequently the leading edge of the line drive occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at Pin 5		30		µA/µs
Oscillator					
V_{14-16}	Threshold voltage low level		4.4		V
V_{14-16}	Threshold voltage high level		7.6		V
$\pm I_{14}$	Discharge current		0.47		mA
f_O	Frequency; free running (C_{OSC} = 4.7nF; R_{OSC} = 12kΩ)		15.625		kHz
$\Delta f_O/f_O$	Spread of frequency		< ± 5		$\%^4$
$\Delta f_O/\Delta I_{15}$	Frequency control sensitivity		31		Hz/µA
$\Delta f_O/f_O$	Adjustment range of network in circuit (see Block Diagram)		± 10		%
$\frac{\Delta f_O/f_O}{\Delta V/V_{NOM}}$	Influence of supply voltage on frequency		< ± 0.05		$\%^4$
Δf_O	Change of frequency when V_{1-16} drops to 5V		< ± 10		$\%^4$
	Temperature coefficient of oscillator frequency		< ± 10^{-4}		Hz/°C[4]

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at V_{CC} = 12V; T_A = 25°C; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Phase comparison φ_1					
V_{13-16}	Control voltage range	3.8	8.2		V
$\pm I_{13M}$	Control current (peak value)	1.9	2.3		mA
I_{13}	Output leakage current at V_{13-16} = 4 to 8V			1	μA
R_{13} R_{13}	Output resistance at V_{13-16} = 4 to 8V[5] at V_{13-16} < 3.8V or > 8.2V[6]		high ohmic low ohmic		
	Control sensitivity		2		kHz/μs
Δf	Catching and holding range (82kΩ between Pins 13 and 15)		±780		Hz
$\Delta(\Delta f)$	Spread of catching and holding range		±10		%[4]
Phase comparison φ_2 and phase shifter					
V_{5-16}	Control voltage range	5.4		7.6	V
$\pm I_{5M}$	Control current (peak value)		1		mA
R_5	Output resistance at V_{5-16} = 5.4 to 7.6V[7] at V_{5-16} < 5.4 or > 7.6V		high ohmic 8		kΩ
I_5	Input leakage current V_{5-16} = 5.4 to 7.6V			5	μA
t_D	Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{FP} = 12μs)			15	μs
$\Delta t/\Delta t_D$	Static control error			0.2	%
Coincidence detector φ_3					
V_{11-16}	Output voltage	0.5		6	V
I_{11M} $-I_{11M}$	Output current (peak value) without coincidence with coincidence		0.1 0.5		mA mA
Time constant switch					
V_{12-16}	Output voltage		6		V
$\pm I_{12}$	Output current (limited)			1	mA
R_{12} R_{12}	Output resistance at V_{11-16} = 2.5 to 7V at V_{11-16} < 1.5V or > 9V		0.1 60		kΩ kΩ
Internal gating pulse					
t_P	Pulse duration		7.5		μs

NOTES:
1. Permissible range 1 to 7V.
2. t_D = switch-off delay of line output stage.
3. Line flyback pulse duration t_{FP} = 12μs.
4. Excluding external component tolerances.
5. Current source.
6. Emitter-follower.
7. Current source.

Signetics

TDA2594
Horizontal Combination

Product Specification

Linear Products

DESCRIPTION

The TDA2594 is a monolithic integrated circuit intended for use in color television receivers.

FEATURES

- **Horizontal oscillator based on the threshold switching principle**
- **Phase comparison between sync pulse and oscillator voltage (φ_1)**
- **Internal key pulse for phase detector (φ1) (additional noise limiting)**
- **Phase comparison between line flyback pulse and oscillator voltage (φ_2)**
- **Larger catching range obtained by coincidence detector (φ_3 between sync and key pulse)**
- **Switch for changing the filter characteristic and the gate circuit (VCR operation)**
- **Sync separator**
- **Noise separator**
- **Vertical sync separator and output stage**
- **Color burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking**
- **Phase shifter for the output pulse**
- **Output pulse duration for transistor reflection systems**
- **External switching off of the line trigger pulse**
- **Output stage with separate supply voltage**
- **Low supply voltage protection**
- **Transmitter identification and muting circuit, and vertical sync switch-off**

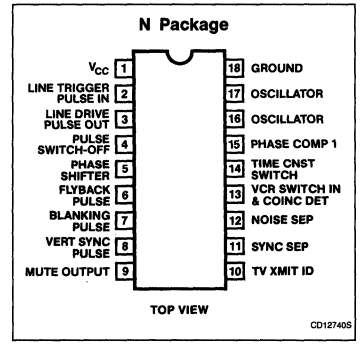
APPLICATIONS

- **Video processing**
- **Television receivers**
- **Video monitors**
- **Sync separator**

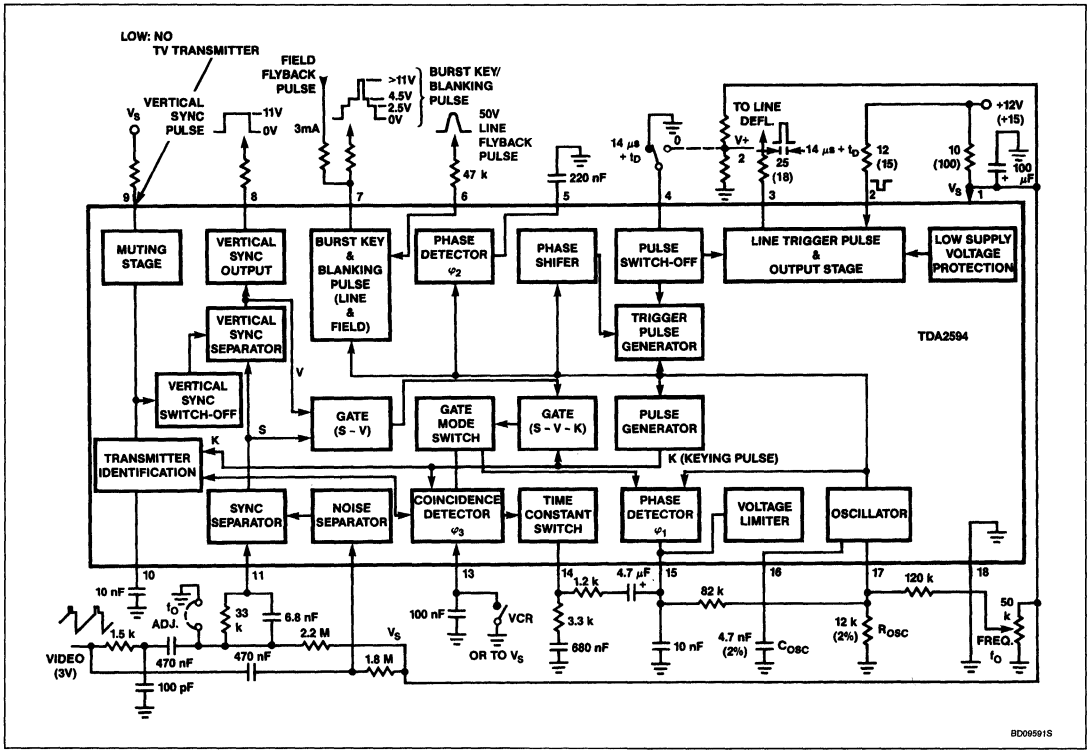
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102DS)	−20°C to +70°C	TDA2594N

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
$V_{1-18} = V_S$	at Pin 1 (voltage source)	13.2	V
V_{2-18}	at Pin 2	18	V
	Voltages		
V_{4-18}	Pin 4	13.2	V
V_{9-18}	Pin 9	18	V
$-V_{9-18}$		0.5	V
$\pm V_{11-18}$	Pin 11	6	V
$\pm V_{12-18}$	Pin 12	6	V
V_{13-18}	Pin 13	13.2	V
	Currents		
I_{2M}, $-I_{3M}$	Pins 2 and 3 (transistor driving) (peak value)	400	mA
I_4	Pin 4	1	mA
$\pm I_6$	Pin 6	10	mA
$-I_7$	Pin 7	5	mA
I_9	Pin 9	10	mA
I_{13}	Pin 13	2	mA
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−25 to +125	°C
T_A	Operating ambient temperature range	−20 to +70	°C

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DC AND AC ELECTRICAL CHARACTERISTICS at $V_{1-18} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sync separator (Pin 11)					
V_{11-18}	Input switching voltage		0.8		V
I_{11}	Input keying current	5		100	μA
I_{11}	Input leakage current at $V_{11-18} = -5V$			1	μA
I_{11}	Input switching current			5	μA
I_{11}	Switch off current	100	150		μA
$V_{11-18(P-P)}$	Input signal (peak-to-peak value)	3		4	V[1]
Noise separator (Pin 12)					
V_{12-18}	Input switching voltage		1.4		V
I_{12}	Input keying current	5		100	μA
I_{12}	Input switching current	100	150		μA
I_{12}	Input leakage current at $V_{12-18} = -5V$			1	μA
$V_{12-18(P-P)}$	Input signal (peak-to-peak value)	3		4	V[1]
$V_{12-18(P-P)}$	Permissible superimposed noise signal (peak-to-peak value)			7	V
Line flyback pulse (Pin 6)					
I_6	Input current	0.02	1		mA
V_{6-18}	Input switching voltage		1.4		V
V_{6-18}	Input limiting voltage	−0.7		+1.4	V
Switching on VCR (Pin 13)					
V_{13-18}	Input voltage	0		2.5 9 to V_S	V V
$-I_{13}$ or: I_{13}	Input current			200 2	μA mA
Pulse switching off (Pin 4) For t = 0; input Pin 4 open or $V_{3-18} = 0$					
V_{4-18}	Input voltage	5.4		6.6	V
I_4	Input current		0		μA
Vertical sync pulse (Pin 8) (positive-going)					
$V_{8-18(P-P)}$	Output voltage (peak-to-peak value)	10	11		V
R_8	Output resistance		2		kΩ
t_{ON}	Delay between leading edge of input and output signal		15		μs
t_{OFF}	Delay between trailing edge of input and output signal	t_{ON}			μs
V_{10-18}	Switching off the vertical sync pulse			3	V
Burst key pulse (Pin 7) (positive-going)					
V_{7-18}	Output voltage	10	11		V
R_7	Output resistance		70		Ω
t_P	Pulse duration; $V_{7-18} = 7V$	3.7	4	4.3	μs
t	Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7V$	2.15	2.65	3.15	μs
I_7	Output trailing edge current		2	2	mA
V_{7-18}	Saturation voltage during line scan			1	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at $V_{1-18} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Line flyback-blanking pulse (Pin 7) (positive-going)					
V_{7-18}	Output voltage	4.1		4.9	V
R_7	Output resistance		70		Ω
I_7	Output trailing edge current		2		mA
Field flyback/blanking pulse (Pin 7)					
V_{7-18}	Output voltage with externally forced in current $I_7 = 2.4$ to 3.6mA	2		3	V
R_7	Output resistance at $I_7 = 3mA$		70		Ω
TV transmitter identification output (Pin 9) (open-collector)					
V_{9-18}	Output voltage at $I_9 = 3mA$; no TV transmitter			0.5	V
R_9	Output resistance at $I_9 = 3mA$; no TV transmitter			100	Ω
I_9	Output current at $V_{10-18} \geqslant 3V$; TV transmitter identified			5	μA
TV transmitter identification (Pin 10)					
	When receiving a TV signal, the voltage V_{10-18} will change from $\leqslant 1V$ to $\geqslant 7V$				
Line drive pulse (positive-going)					
$V_{3-18(P-P)}$	Output voltage (peak-to-peak value)		10		V
R_3	Output resistance for leading edge of line pulse for trailing edge of line pulse		 2.5 20		 Ω Ω
t_P	Pulse duration (transistor driving) $V_{4-18} = 0$ to 3.5V; $-I_4 \geqslant 200\mu A$; $t_{FP} = 12\mu s$			$14 + t_D$	μs^2
V_{1-18}	Supply voltage for switching off the output pulse		4		V
Overall phase relation					
Δt	Phase relation between middle of sync pulse and the middle of the flyback pulse		2.6		μs^3
	The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.				
$\Delta I/\Delta t$	If additional adjustment is applied, it can be arranged by current supply at Pin 5, such that: supplying current		 30		 $\mu A/\mu s$

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) at $V_{1-18} = 12V$; $T_A = 25°C$; measured in Block Diagram.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Oscillator (Pins 16 and 17)					
V_{16-18}	Threshold voltage low level		4.4		V
V_{16-18}	Threshold voltage high level		7.6		V
$\pm I_{16}$	Charging current		0.47		mA
f_O	Frequency; free running ($C_{OSC} = 4.7nF$; $R_{OSC} = 12k\Omega$)		15.625		kHz
Δf_O	Spread of frequency			±5	%[6]
$\Delta f_O/\Delta_{17}$	Frequency control sensitivity		31		Hz/μA
Δf_O	Adjustment range of network in circuit (Block Diagram)		±10		%
$\frac{\Delta f_O/f_O}{\Delta V/V_{NOM}}$	Influence of supply voltage on frequency; reference at $V_S = 12V$			±0.05	%[6]
Δf_O	Change of frequency when V_S drops to 5V; reference at $V_S = 12V$			±10	%[6]
TC	Temperature coefficient of oscillator frequency			$\pm 10^{-4}$	K^{-1} [6]
Phase comparison φ_1 (Pin 15)					
V_{15-18}	Control voltage range	4.1		7.9	V
$\pm I_{15M}$	Control current (peak value)	1.8		2.2	mA
I_{15}	Output leakage current at $V_{15-18} = 4.3$ to 7.7V			1	μA
R_{13} R_{13}	Output resistance at $V_{15-18} = 4.3$ to 7.7V[4] at $V_{15-18} \leqslant 4.1V$ or $\geqslant 7.9V$[5]		high ohmic low ohmic		
	Control sensitivity		2		kHz/μs
Δf	Catching and holding range (82kΩ between Pins 15 and 17)		±680		Hz
$\Delta(\Delta f)$	Spread of catching and holding range		±12		%[6]
Phase comparison φ_2 and phase shifter (Pin 5)					
V_{5-18}	Control voltage range	5.4		7.6	V
$\pm I_{5M}$	Control current (peak value)		1		mA
R_5	Output resistance at $V_{5-18} = 5.4$ to 7.6V[4]		high ohmic		
I_5	Input leakage current at $V_{5-18} = 5.4$ to 7.6V			5	μA
t_D	Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{FP} = 12\mu s$)			15.5	μs
$\Delta t/\Delta t_D$	Static control error			0.2	%
Coincidence detector φ_3 (Pin 13)					
V_{13-18}	Output voltage	0.5		6	V
I_{13M} $-I_{13M}$	Output current (peak value) without coincidence with coincidence		0.1 0.5		mA mA

NOTES:
1. Permissible range 1 to 7V.
2. t_D = switch-off delay of line output stage.
3. Line flyback pulse duration $t_{FP} = 12\mu s$.
4. Current source.
5. Emitter-follower.
6. Excluding external component tolerances.

Signetics

TDA2595
Horizontal Combination

Product Specification

Linear Products

DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in color television receivers.

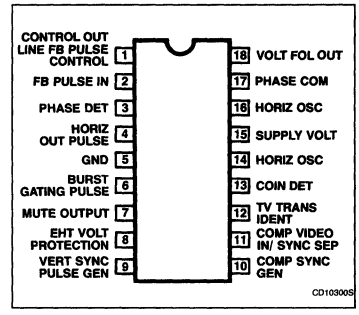
FEATURES

- **Positive video input; capacitively coupled (source impedance $< 200\Omega$)**
- **Adaptive sync separator; slicing level at 50% of sync amplitude**
- **Internal vertical pulse separator with double slope integrator**
- **Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting**
- **φ_1 phase control between horizontal sync and oscillator**
- **Coincidence detector φ_3 for automatic time constant switching; overruled by the VCR switch**
- **Time constant switch between two external time constants for loop gain; both controlled by the coincidence detector φ_3**
- **φ_1 gating pulse controlled by coincidence detector φ_3**
- **Mute circuit depending on TV transmitter identification**
- **φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately**
- **Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)**
- **Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor**
- **Detector for too low supply voltage**
- **Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4V or higher than 8V**
- **Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse**
- **Spot suppressor controlled by the line flyback control**

APPLICATIONS

- **Television receivers**
- **Video receivers**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102CS)	−20°C to +70°C	TDA2595N

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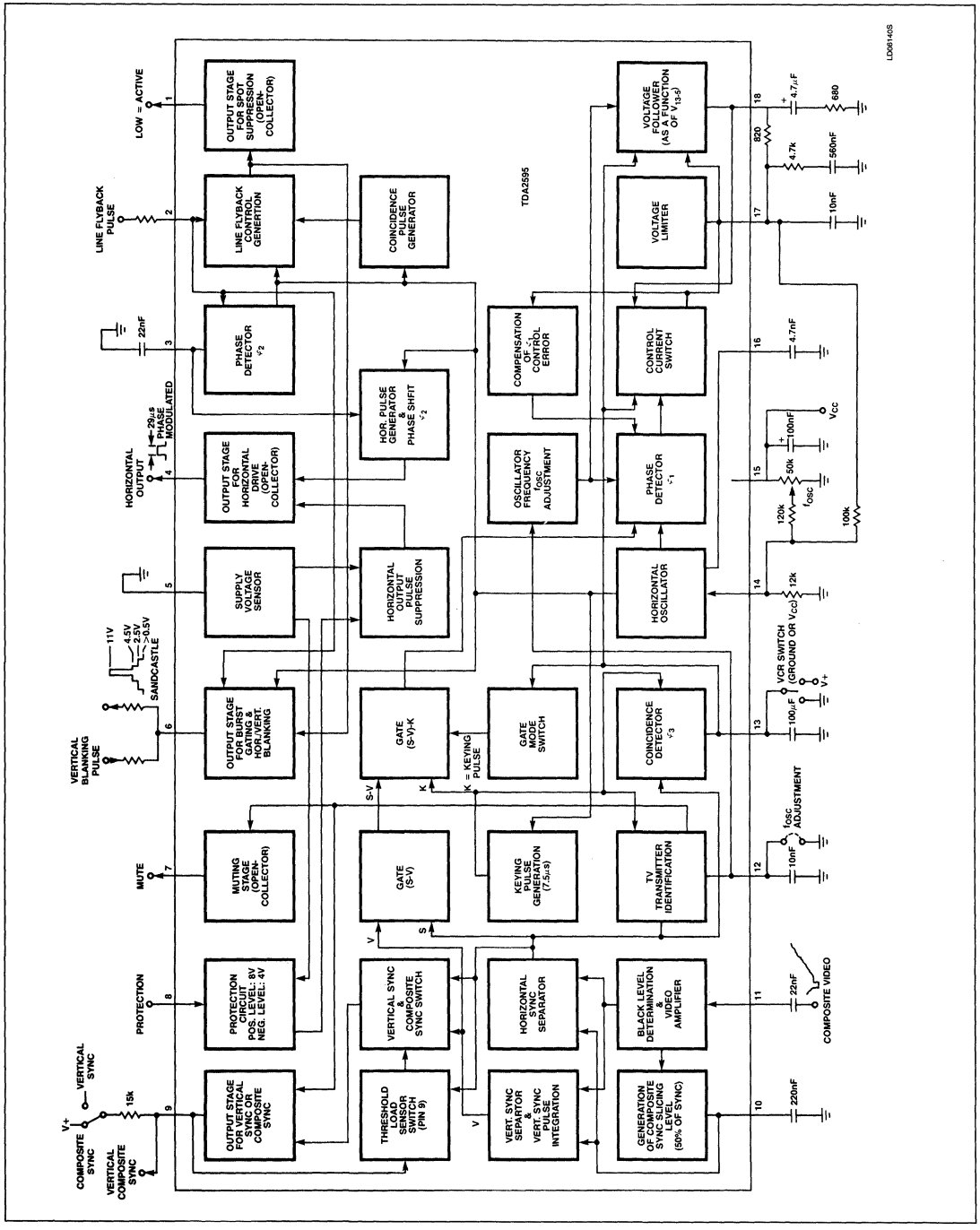
Horizontal Combination

TDA2595

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	DESCRIPTION	RATING	UNIT
$V_{15-5} = V_{CC}$	Supply voltage (Pin 15)	13.2	V
	Voltages at:		
$V_{1;4;7-5}$	Pins 1, 4 and 7	18	V
$V_{8;13;18-5}$	Pins 8, 13 and 18	V_{CC}	V
V_{11-5}	Pin 11 (range)	−0.5 to +6	V
	Currents at:		
I_1	Pin 1	10	mA
$\pm I_{2M}$	Pin 2 (peak value)	10	mA
I_4	Pin 4	100	mA
$\pm I_{6M}$	Pin 6 (peak value)	6	mA
I_7	Pin 7	10	mA
I_8	Pin 8 (range)	−5 to +1	mA
I_9	Pin 9 (range)	−10 to +3	mA
$\pm I_{18}$	Pin 18	10	mA
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Composite video input and sync separator (Pin 11) (internal black level determination)					
$V_{11-5(P-P)}$	Input signal (positive video; standard signal; peak-to-peak value)	0.2	1	3	V
$V_{11-5(P-P)}$	Sync pulse amplitude (independent of video content)	50			mV
R_G	Generator resistance			200	Ω
	Input current during				
I_{11}	Video		5		μA
$-I_{11}$	Sync pulse		40		μA
$-I_{11}$	Black level		30		μA
Composite sync generation (Pin 10) horizontal slicing level at 50% of the sync pulse amplitude					
	Capacitor current during				
I_{10}	Video		12		μA
$-I_{10}$	Sync pulse		170		μA
Vertical sync pulse generation (Pin 9) slicing level at 25% (50% between black level and horizontal slicing level)					
V_{9-5}	Output voltage	10			V
t_P	Pulse duration		190		μs
t_D	Delay with respect to the vertical sync pulse (leading edge)		45		μs
	Pulse-mode control				
	Output current for vertical sync pulse (dual integrated)	No current applied at Pin 9			
	Output current for horizontal and vertical sync pulse (non-integrated separated signal)	Current applied via a resistor of 15kΩ from V_{CC} to Pin 9			

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal oscillator (Pins 14 and 16)					
f_{OSC}	Frequency; free-running		15.625		kHz
V_{14-5}	Reference voltage for f_{OSC}		6		V
$\Delta f_{OSC}/\Delta I_{14}$	Frequency control sensitivity		31		Hz/μA
Δf_{OSC}	Adjustment range of circuit Figure 1		±10		%
Δf_{OSC}	Spread of frequency			5	%
$\frac{\Delta f_{OSC}/f_{OSC}}{\Delta V_{15-5}/V_{15-5}}$	Frequency dependency (excluding tolerance of external components) with supply voltage (V_{CC} = 12V)		±0.05		%
Δf_{OSC}	with supply voltage drop of 5V			10	%
TC	with temperature			$\pm 10^{-4}$	$°C^{-1}$
	Capacitor current during:				
$-I_{16}$	Charging		1024		μA
I_{16}	Discharging		313		μA
	Sawtooth voltage timing (Pin 14)				
t_R	Rise time		49		μs
t_F	Fall time		15		μs
Horizontal output pulse (Pin 4)					
V_{4-5}	Output voltage Low at I_4 = 30mA			0.5	V
t_P	Pulse duration (High)		29 ±1.5		μs
V_{CC}	Supply voltage for switching off the output pulse (Pin 15)		4		V
Phase comparison φ_1 (Pin 17)					
V_{17-5}	Control voltage range	3.55		8.3	V
I_{17}	Leakage current at V_{17-5} = 3.55 to 8.3V			1	μA
$\pm I_{17}$	Control current for external time constant switch	1.8	2	2.2	mA
$\pm I_{17}$	Control current at $V_{18-5} = V_{15-5}$ and $V_{13-5} < 2V$ or $V_{13-5} > 9.5V$		8		mA
$\pm I_{17}$	Control current at $V_{18-5} = V_{15-5}$ and V_{13-5} = 2 to 9.5V	1.8	2	2.2	mA
	Horizontal oscillator control				
S_φ	Control sensitivity	6			kHz/μs
Δf_{OSC}	Catching and holding range		±680		Hz
Δf_{OSC}	Spread of catching and holding range		±10		%
t_P	Internal keying pulse at V_{13-5} = 2.9 to 9.5V		7.5		μs
	Time constant switch				
V_{13-5}	Slow time constant	9.5		2	V
V_{13-5}	Fast time constant	2		9.5	V
$\pm V_{17-18}$	Impedance converter offset voltage (slow time constant)			3	mV
	Output resistance				
R_{18-5}	Slow time constant			10	Ω
R_{18-5}	Fast time constant	high impedance			
I_{18}	Leakage current			1	μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Coincidence detector φ_3 (Pin 13)					
	Output voltage				
V_{13-5}	without coincidence with composite video signal			1	V
V_{13-5}	without coincidence without composite video signal (noise)			2	V
V_{13-5}	With coincidence with composite video signal		6		V
	Output current				
I_{13}	without coincidence with composite video signal		50		μA
$-I_{13}$	with coincidence with composite video signal		300		μA
	Switching current				
I_{13}	at $V_{13-5} = V_{CC} - 0.5V$			100	μA
$I_{13(av)}$	at $V_{13-5} = 0.5V$ (average value)			100	μA
Phase comparison φ_2 (Pins 2 and 3)[1]					
Δt	Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at $t_{FP} = 12\mu s$[2]		2.6 ± 0.7		μs
ΔI/Δt	If additional adjustment is required, it can be arranged by applying a current at Pin 3, such that for applied current:		30		μA/μs
Input for line flyback pulse (Pin 2)					
V_{2-5}	Switching level for φ_2 comparison		3		V
V_{2-5}	Switching level for horizontal blanking and flyback control		3		V
V_{2-5}	Input voltage limiting		−0.7 +4.5		V V
	Switching current				
I_2	at horizontal flyback	0.01	1		mA
I_2	at horizontal scan			2	μA
Phase detector output (Pin 3)					
$\pm I_3$	Control current for φ_2		1		mA
$\Delta t_{\varphi 2}$	Control range		19		μs
$\Delta t/\Delta t_d$	Static control error			0.2	%
I_3	Leakage current			5	μA
Burst gating pulse (Pin 6)[3]					
V_{6-5}	Output voltage	10	11		V
t_P	Pulse duration	3.7	4	4.3	μs
$t_{\varphi 6}$	Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at $V_{6-5} = 7V$	2.15	2.65	3.15	μs
I_6	Output trailing edge current		2		mA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Horizontal blanking pulse (Pin 6)[3]					
V_{6-5}	Output voltage	4.2	4.5	4.9	V
I_6	Output trailing edge current		2		mA
V_{6-5sat}	Saturation voltage at horizontal scan			0.5	V
Clamping circuit for vertical blanking pulse (Pin 6)[3]					
V_{6-5}	Output voltage at I_6 = 2.8mA	2.15	2.5	3	V
I_{6min}	Minimum output current at V_{6-5} > 2.15V		2.3		mA
I_{6max}	Maximum output current at V_{6-5} < 3V		3.3		mA
TV transmitter identification (Pin 12)					
V_{12-5} V_{12-5}	Output voltage no TV transmitter TV transmitter identified	 7		1	 V V
Mute output (Pin 7)					
V_{7-5}	Output voltage at I_7 = 3mA; no TV transmitter			0.5	V
R_{7-5}	Output resistance at I_7 = 3mA; no TV transmitter			100	Ω
I_7	Output leakage current at V_{12-5} > 3V; TV transmitter identified			5	μA
Protection circuit (beam current/EHT voltage protection) (Pin 8)					
V_{8-5}	No-load voltage for I_8 = 0 (operative condition)		6		V
V_{8-5}	Threshold at positive-going voltage		8 ±0.8		V
V_{8-5}	Threshold at negative-going voltage		4 ±0.4		V
$\pm I_8$	Current limiting for V_{8-5} = 1 to 8.5V		60		μA
R_{8-5}	Input resistance for V_{8-5} > 8.5V		3		kΩ
t_d	Response delay of threshold switch		10		μs
Control output of line flyback pulse control (Pin 1)					
V_{1-5sat}	Saturation voltage at standard operation; I_1 = 3mA			0.5	V
I_1	Output leakage current in case of break in transmission			5	μA

NOTES:
1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase-modulated (φ_2) horizontal output pulse with constant duration.
2. t_{FP} is the line flyback pulse duration.
3. Three-level sandcastle pulse.

Signetics

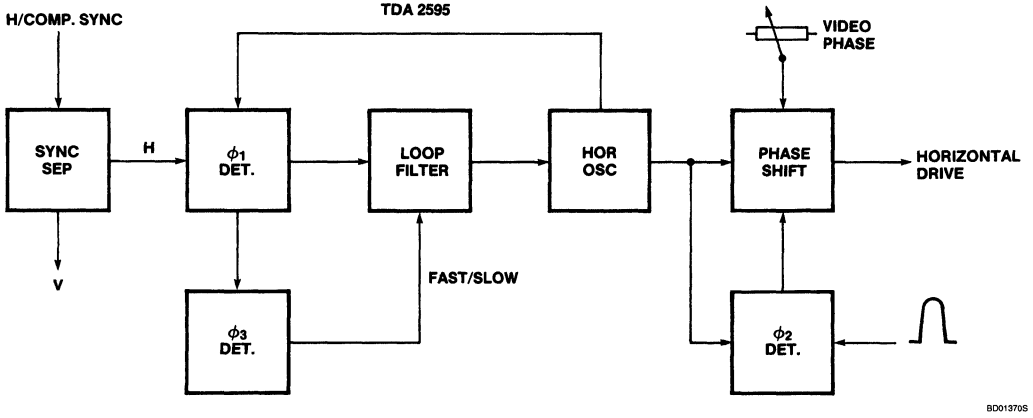
AN158
Features of the TDA2595 Synchronization Processor

Application Note

Linear Products

FEATURES

- Positive video input, capacitive coupled (source impedance $< 200\Omega$)
- Adaptive sync slicer at 50% of sync pulse amplitude
- Internal vertical pulse separator with double-slope integrator
- Outputstage for vertical sync pulse or composite sync depending on the load. Both are switched off by mute
- ϕ_1 phase control between H-sync and oscillator
- Coincidence detector ϕ_3 for automatic time-constant switching, overruled by the VCR-switch
- Time-constant switch between two external time-constants or loop-gain switch both controlled by coincidence detector ϕ_3
- ϕ_1 gating pulse controlled by coincidence detector ϕ_3
- Mute circuit depending on TV transmitter identification
- ϕ_2 phase control between line flyback and oscillator. The slicing levels for ϕ_2 control and line blanking can be set separately
- Burst keying and line blanking pulse generation, combined with clamping of field blanking pulse (triple-level sandcastle)
- H-drive output with constant duty cycle inhibited by the protection circuit or the supply voltage detector
- Detector for too low supply voltage
- Protection circuit switching off H-drive output continuously if input voltage is below 4V or higher than 8V
- Line flyback control causing line-blanking level at sandcastle output continuously in case of missing flyback pulse
- Spot-suppressor controlled by the line flyback control



ϕ_1 OSCILLATOR vs SYNC loss of sync

ϕ_2 FLYBACK vs OSCILLATOR storage time variations: video shift

ϕ_3 COINCIDENCE DETECTOR fast/slow ϕ_1 loop switch

Figure 1

9

Features of the TDA2595 Synchronization Processor AN158

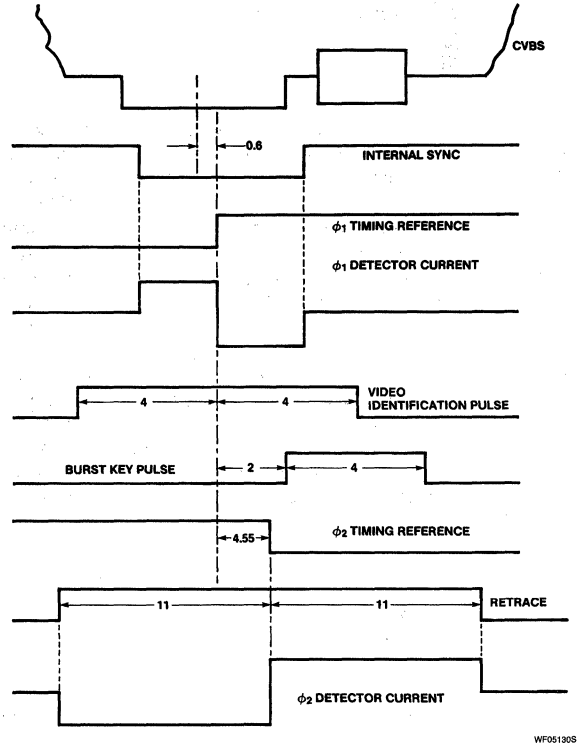


Figure 2. Timing Diagram

Features of the TDA2595 Synchronization Processor AN158

SYNC SEPARATOR

Adaptive sync separator to slice H-sync at 50% and V-sync at 25% independent on sync-amplitude. This is to insure immunity against deteriorated sync impulses. The black level is stored on a capacitor which is fed to the positive video-signal (source impedance 200Ω) into Pin 11. The slicing level is detected internally and stored in a capacitor at Pin 12.

The internal vertical integrator has a delay of 45μs and is of the double-slope type to avoid jitter and to improve noise immunity.

VERTICAL/COMPOSITE SYNC

The output stage at Pin 9 delivers a positive vertical pulse or a positive composite sync signal if the current drain is higher than 3mA.

If no TV transmitter is detected, the output is switched to ground. The source impedance is low-ohmic.

15kHz VCO

The VCO is a current controlled ramp oscillator with 49μs rise time and 15μs fall time. The timing capacitor is connected to Pin 16; the control current has to be fed into Pin 14.

While adjusting f_0, Pin 12 should be connected to ground.

The oscillator generates the following signals (see timing diagram Figure 2):

- timing reference for ϕ_1
- gating pulse for ϕ_1
- reference pulse for video identification circuit and coincidence detector ϕ_3
- burst keying pulse
- time reference for ϕ_2

ϕ_1 PHASE CONTROL

The phase control ϕ_1 compares the ϕ_1 timing reference of the VCO with the center of the H-sync signal and converts the time difference into a proportional current at Pin 17.

The external low-pass filter at Pin 17 determines the time constant and the catching and tracking range of the VCO.

If Pin 18 is connected to the V+, the loop gain is increased 4 times as long as the oscillator is not locked in or Pin 13 is connected to ground or V+ (VCR switch).

If Pin 18 is connected as shown in the circuit diagram, Pin 18 has the same voltage as Pin 17 as long as the oscillator is not locked in or Pin 13 is connected to ground. Due to this the "long" time constant connected from Pin 18 to ground, ground is electrically disconnected from Pin 17.

If the oscillator is locked in and Pin 13 not connected to ground, Pin 18 switches to high impedance and thus the loop filter to the "long" time-constant.

By switching loop gain or loop time-constant, the lock in condition of the oscillator is not disturbed. This enables a fast search tuning using the TV transmitter identification ($\overline{\text{mute}}$) as a search stop.

To increase noise immunity the phase detector is inhibited during horizontal retrace and vertical retrace if the oscillator is locked in and Pin 13 not connected to ground or V+.

COINCIDENCE DETECTOR ϕ_3

The coincidence circuit detects whether there is coincidence between the H-sync pulse and a 8μs impulse generated by the VCO. The capacitor at Pin 13 is discharged continuously by 8μs current pulses of 50μA. If there is coincidence, the capacitor is additionally charged by H-sync pulses of 350μA.

If the voltage at Pin 13 exceeds 3V, the loop gain is reduced and the loop time constant is switched to the "long" value.

If the voltage exceeds 4.5V, the phase detector ϕ_1 is gated to improve noise immunity.

MUTE CIRCUIT

The mute circuit detects whether there is coincidence between the H-sync impulse and a 8μs impulse generated by the VCO. The capacitor at Pin 12 is discharged during sync-pulses of 50μA and by 8μs current pulses of 50μA. If there is coincidence, the capacitor is additionally charged by H-sync pulses of 450μA.

If the voltage at Pin 12 exceeds 4V, mute is released and the mute output at Pin 7 is switched to high impedance. Although the coincidence detector ϕ_3 and the mute circuit act similarly, separate circuits have been chosen. This is to gain in design flexibility as far as the time constants are related and to keep the mute function alive independently on the VCR switch.

ϕ_2 PHASE CONTROL

The phase control ϕ_2 compares the center of the positive flyback pulse at Pin 2 at a threshold of 3V with the ϕ_2 timing reference. The time difference is converted into a proportional current at Pin 3. Loop gain and time-constant are influenced by the external components at Pin 3. The voltage at Pin 3 in turn controls the phase shift.

To achieve a small phase adjustment a small current may be injected into Pin 3.

The aim of having two different thresholds at the flyback input is to determine the performance of the ϕ_2 loop, e.g., a straight vertical center line, by the amplitude of the applied flyback pulse without affecting the blanking time.

SUPER SANDCASTLE

For burst keying and vertical and horizontal blanking there is a 3 level pulse at Pin 6.

The burst keying part is driven from the VCO and is 4μs wide. Due to its small tolerances in widths and phase it keys the burst very exactly and is suitable as black level clamping pulse.

The blanking part is derived from the line flyback pulse at Pin 2 at a threshold of 0.2V. If no flyback is applied to Pin 2, there will be continuous blanking level superimposed by the burst keying pulse.

The frame blanking part has to be fed in externally as a 2mA current.

HORIZONTAL DRIVE

The H-drive output is an open-collector output at Pin 4. The output pulse has a constant aspect ratio of 45.3% off and 54.7% on dependent upon the line frequency. An internal guard logic insures that there will be high level during flyback. The output is inhibited by the protection circuit also if the supply voltage is below 4V. In both cases the line flyback vanishes and by this the spot suppressor is activated.

SPOT SUPPRESSOR

The spot suppressor is an open collector output at Pin 1. If no flyback impulses are detected at Pin 2, the output switches to high impedance and remains there as long as the flyback pulses are missing even if the supply voltage vanishes during that time.

PROTECTION CIRCUIT

The protection circuit is activated if the voltage at Pin 8 exceeds 8V or decreases below 4V. One of both thresholds may be used (as indicated in Figures 4a and b) to have X-ray protection or overcurrent protection.

If activated, the H-drive is inhibited by this and the line flyback vanishes and in turn the spot suppressor is activated.

The protection circuit is reset if the supply voltage decreases below 4V, e.g., the set is switched off.

Features of the TDA2595 Synchronization Processor AN158

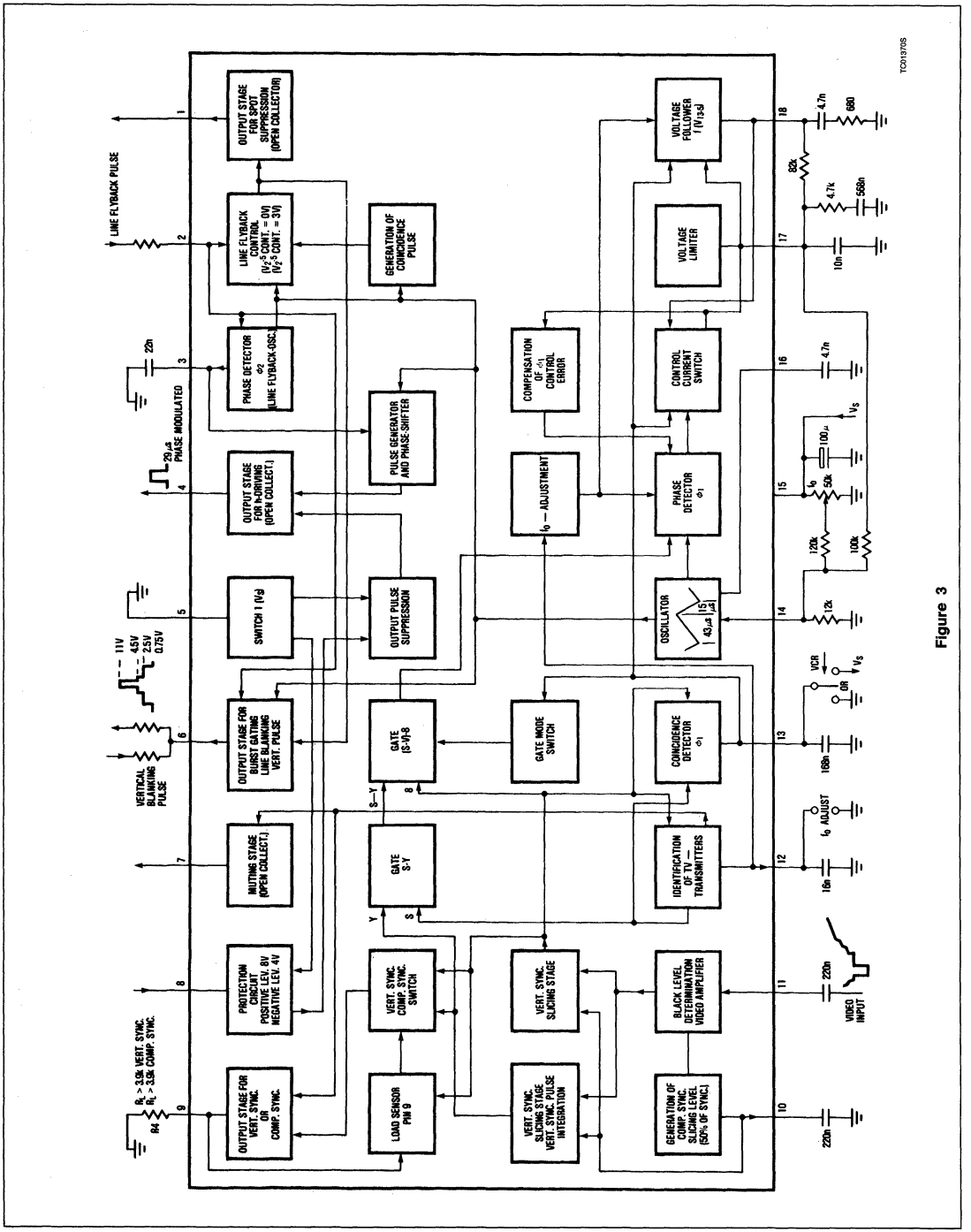
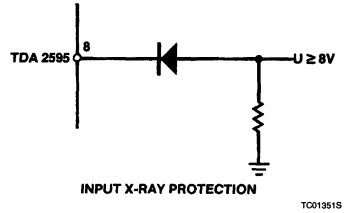
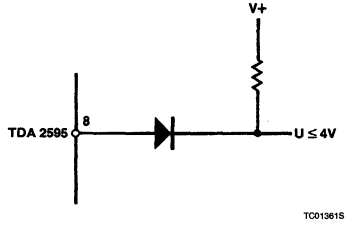


Figure 3



a. Input X-ray Protection



b. Input Over Current Protection

Figure 4

Signetics

TDA8432

Computer-Controlled Deflection Processor for Video Displays

Objective Specification

Linear Products

DESCRIPTION

The TDA8432 is an I^2C bus-controlled deflection processor (analog picture geometry processor) which contains the control and drive functions of the deflection circuits in a computer-controlled TV (CCTV) or monitor. This IC replaces all picture geometry settings which are performed manually during manufacturing. The alignment of 10 picture geometry parameters for the vertical and horizontal deflection is accomplished by means of a microcontroller via the I^2C bus. Furthermore, it eliminates the external components needed for adjusting the horizontal frequency and phase position, vertical linearity, picture height, east-west parabola, and picture width. The east-west shaping circuit is also eliminated. Provisions have been incorporated to make several sync processor (TDA2579 and TDA2595) functions I^2C bus-controllable.

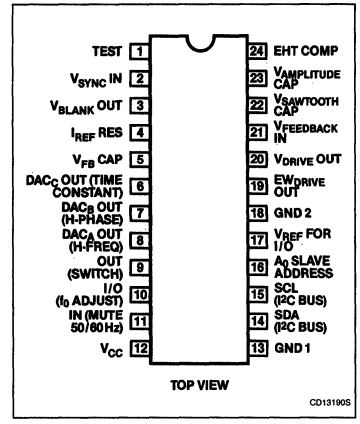
FEATURES

- **I^2C bus interface for all functions**
- **Input for vertical sync from sync processor**
- **Vertical sawtooth generator with frequency-independent amplitude**
- **Vertical output stage with feedback input for driving a vertical deflection amplifier**
- **East-west raster correction drive output**
- **EHT modulation input, providing optimum picture geometry compensation for static and dynamic EHT load variations**
- **I^2C bus-controlled alignment of 10 deflection parameters**
- **Provisions for controlling a sync processing IC which does not have an I^2C bus interface, including:**
  - **Two digital-to-analog converters for alignment of the free-running horizontal frequency and horizontal phase position**
  - **An I/O pin enabling computer alignment of the free-running horizontal frequency**
  - **A special purpose 4-level output for time constant switching of the horizontal phase-locked loop**
  - **A special purpose 3-level input for detection of the mute function and the 50Hz/60Hz state of the sync processor**
- **A switchable output (e.g., for controlling a video source selector)**

APPLICATIONS

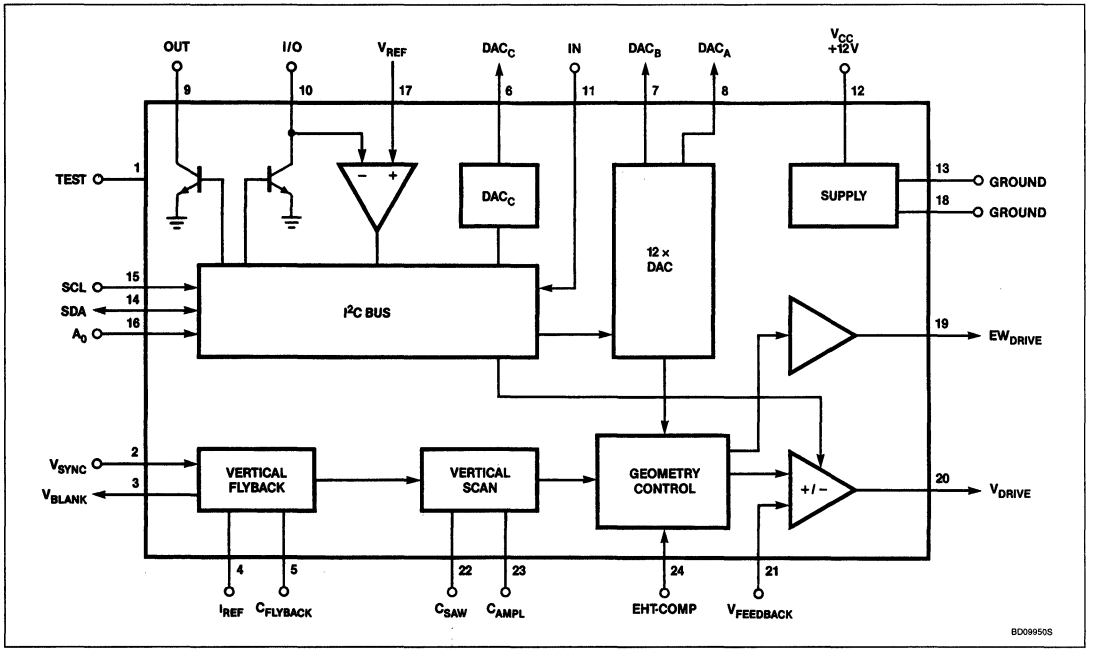
- **Video monitors**
- **Color TV receivers**

PIN CONFIGURATION



Computer-Controlled Deflection Processor for Video Displays TDA8432

BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 17)	14	V
	Switching voltage (Pin 5)	8	V
	Output currents of each pin to ground (Pins 11 and 12)	−10	mA
	Maximum short-circuit time outputs	10	sec
T_{STG}	Storage temperature	−55 to +150	°C
T_A	Operating temperature	−25 to 80	°C
T_J	Junction temperature	+150	°C
θ_{JA}	Thermal resistance	75	°C/W

RECOMMENDED OPERATING CONDITIONS

In application circuit Figure 1 at $T_A = 25°C$ and $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage (Pins 17 – 20, 10)	10		13.2	V
I_{CC}	Supply current (Pin 17)		42	55	mA
	Switching voltage VHF (Pin 5)	0		1.5	V
	Switching voltage hyperband	2		3.5	V
	Switching voltage UHF (Pin 5)	4		5	V
	Switching current UHF (Pin 15)			0.2	mA

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
VHF mixer including IF, measurement in circuit of Figure 1					
f_R	Frequency range: printed circuit board	50		300	MHz
	Noise Figure 1 (Pin 23) 50MHz 225MHz 300MHz		7.5 9 10	9 10 12	dB dB dB
	Optimum source admittance (Pin 23) 50MHz 225MHz 300MHz		0.5 1.1 1.2		mmho mmho mmho
	Input conductance (Pin 23) 50MHz 225MHz 300MHz		0.23 0.5 0.67		mmho mmho mmho
C_{IN}	Input capacitance (Pin 23) 50MHz – 300MHz		2		pF
V_{IN}	Input voltage for 1% × mod in channel (Pin 23)	97	100		dBμV
V_{IN}	Input voltage for 10kHz pulling (in channel) (Pin 23)	100	108		dBμV
A_V	Voltage gain = 20log (V_{11-12}/V_{23}) (Pins 11 – 12, 23)	22	24.5	27	dB
VHF mixer					
	Conversion transadmittance mixer = SC = I15/V23 = −I16/V23 (Pins 15, 16 – 23)		3.8		mmho
	Output admittance mixer (Pins 15 – 16)		0.1		mmho
	Output capacitance mixer (Pins 15 – 16)		2		pF

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
VHF oscillator					
f_R	Frequency range	70		330	MHz
	Shift V_B = 10%; 70 to 330MHz			200	kHz
	Drift T = 15°; 70 to 330MHz			250	kHz
	Drift from 5 seconds to 15 minutes after switching on			200	kHz
Hyperband mixer including IF (measured in circuit of Figure 1[2]) (measurements with hybrid)					
f_R	Frequency range	300		470	MHz
	Noise figure (Pins 21, 22) 300MHz 470MHz		8 8	10 10	dB dB
	Input reflection coefficient (Pins 21, 22) 300MHz |S11|[5] phase 470MHz |S11| phase		−4.4 +162 −4.7 +151		dB deg dB deg
	Input available power Pav for 1% X-mod 300MHz in-channel (Pins 21, 22) 470MHz		−19 −19		dBm dBm
	10kHz pulling (in-channel) (Pins 21, 22) 470MHz N + 5 − 1MHz pulling[3] (Pins 21, 22) 470MHz		−11 −29		dBm dBm
	Gain = [4] 300MHz 470MHz	34 34	37 37	40 40	dB dB
Hyperband oscillator					
	Frequency range (MHz)	330		520	MHz
	Shift ΔV_B = 5%			400	kHz
	Drift ΔT = 15°			500	kHz
	Drift from 5 seconds to 15 minutes after switching on			600	kHz
	Input reflection coefficient (Pins 4 − 5) |S11| at f = 330MHz phase		TBD TBD		dB deg
UHF mixer including IF (Pins 18 and 19) (measured in circuit of Figure 1[2]) (measurements with hybrid)					
	Frequency range	470		860	MHz
	Noise figure 470MHz 860MHz		8 9	10 11	dB dB
	Input reflection coefficient 470MHz |S11| phase 860MHz phase		−4 +157 −4.2 +138		 deg deg
	Input available power P_{AV} for 470MHz 1% X-mod in-channel 860MHz		−19 −19		dBm dBm
	10kHz pulling (in-channel) 860MHz N + 5 − 1MHz pulling[3] 820MHz	 −42	−10 −35		dBm dBm
	Gain = [4] 470MHz 860MHz	34 34	37 37	40 40	dB dB

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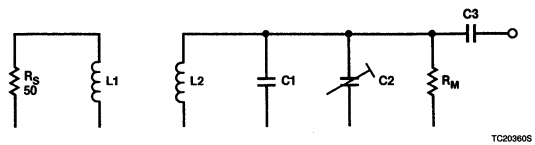
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
UHF oscillator					
f_R	Frequency range (MHz)	500		900	MHz
	Shift $\Delta V_B = 5\%$			400	kHz
	Drift $\Delta T = 25°C$ to $40°C$			500	kHz
	Drift from 5 seconds to 15 minutes after switching on			300	kHz
IF amplifier					
			Mod	**Phase**	
	S11 S21 measured at 36MHz, differentially S12 S22		−0.5 12 −41 −7.9	−1 160 −5.2 13.7	dB/deg dB/deg dB/deg dB/deg
LO output (Pin 2)					
	Output voltage into 75Ω f ⩽ 330MHz	14	37	100	mV
	Output reflection coefficient (VHF position) S22 (Hyperband and UHF) at 500MHz		TBD TBD		dB/deg dB/deg
	Spurious signal on LO output wrt LO output signal, measured in 75Ω with RF signal level at Pin 24 1V ⩽ 225MHz 0.3V 225MHz – 300MHz			−10	dB
	Harmonics of LO signal wrt LO signal, measured in 75Ω			−10	dB

NOTES:
1. The Pins 2, 5, 11, 12, 13, 14 withstand the ESD test.
2. Measured with an input circuit for optimum noise figure.
3. The values have been corrected for hybrid and cable losses. The symmetrical output impendance of the hybrid is 100Ω.
4. The input level of an N + 5 – 1MHz signal which is just visible (Amtsblatt 69).
5. The gain is defined as the transducer gain measured in Figure 1 + the voltage transformation ratio of L6-L7. The ratio is 6:1 (16dB).
6. All S parameters are referred to a 50Ω system.



NOTES:
Component values: F = 50MHz F = 225MHz F = 300MHz
L1 = L2 =
C1 =
C2 =
C3 =
R_M =

Electrical parameters of the circuit are (for appropriate impedance and selectivity)
Insertion loss
VSWR without IC
VSWR with IC
Impedance of tuned circuit without
IC at VSWR = 1
Image suppression
Output impedance (source for IC)

Figure 1

Signetics

Linear Products

Section 10
Color Decoding and Encoding

INDEX

AN155A
Multi-Standard Color Decoder With Picture Improvement

Application Note

Linear Products

The decoder concept presented here comprises a multi-standard color decoder and a video combination. The concept can also be extended by means of a picture improvement circuit.

A brief overview will first be given to clarify this arrangement. Figure 1 shows the block diagram of a complete color decoder from the CVBS interface up to the picture tube. There are switchable filters for separation of the luminance and chrominance signals from one another. Only one IC is necessary for the demodulation of four color standards.

The output signals are the standard-independent color difference signals (B-Y) and (R-Y), i.e., U and V. The baseband signals (i.e., color difference signals and luminance signal Y) can either be directly supplied to the video combination or they can be supplied via a signal processor IC as shown here.

The video combination comprises all functions for advanced video signal processing. The RGB output signals of the IC can be fed to the video final stages directly.

The interface selected in this decoder concept, with the baseband signals as input signals of the video combination, also permits new circuit concepts to be introduced; e.g., the delay line which is required for PAL and SECAM can be realized with CCD lines. Picture improvement circuits with picture memories can also be added.

The Color Transient Improvement (CTI) IC which is incorporated in Figure 1 was also developed for this interface. Two functions are integrated in this circuit: a transient improvement for a better picture, and a Y delay line in gyrator technique to replace the previously-required wound line.

In the past, multi-standard color decoders (MSD) have been built up with a number of integrated circuits. Parallel working concepts are known, and also transcoder concepts specially for PAL and SECAM. The decoders of the various standards require circuit blocks of the same type; this applies in particular to the quadrature amplitude modulation standards (QAM standards) PAL and NTSC, but also to a large extent to the FM standard SECAM. Therefore, an obvious approach for the integration of a multi-standard decoder on one chip is to make use of as many circuit blocks as possible in common for the different standards in order to minimize the components and, also, the crystal area required. Under the condition of automatic standard identification, as is already the state of the art for present MSD concepts, multiple utilization of the circuit blocks can only be realized if automatic standard identification is effected by *sequential standard scanning*. A system of this kind gives the great advantage that the entire decoder, including the filters, can be designed in the optimum way for the individual standards.

The single-chip multi-standard decoder TDA4555/TDA4556 is examined fully in AN1551. Please refer to AN1551 for application information.

The Video Combination IC — TDA3505

The video combination IC incorporates all setting functions for color picture reproduction. A black current stabilizing circuit is provided. This saves three tuning operations and also automatically regulates operating-point changes due to warming up after switch-on and to aging.

RGB signal inputs are provided for signal supply from RGB sources via the audio/video plug, e.g., from cameras or from internal teletext decoders.

Figure 2 shows the block diagram of the input part of this IC. The two color difference signals −(R-Y) and −(B-Y) are fed in via capacitors and clamped in the input stages to reference values. After the saturation control stages, the −(G-Y) signal is generated with the (G-Y) matrix. These color difference signals, together with the Y-signal which is also clamped in the input stage, are converted to the R, G, and B signals in the R, G, and B matrix.

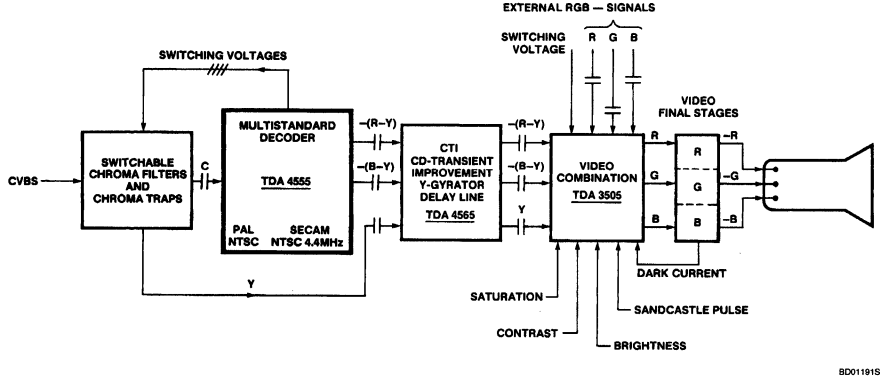


Figure 1. Block Diagram of the Multi-Standard Color Decoder

Multi-Standard Color Decoder With Picture Improvement AN155A

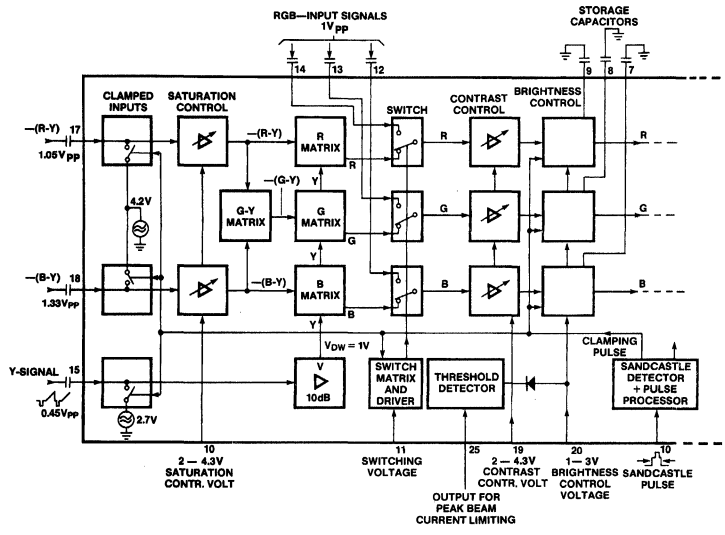


Figure 2. Front Part of the Video Combination TDA3505

Switching stages, together with a switching matrix and a driver stage for the switching, permit the choice between the picture signals from the color difference and Y inputs, or from the R, G, B inputs. When the R, G, B signals from the R, G, B inputs are selected, they are added to the black levels, which are simultaneously inserted. The switching times between blanking, insertion, and changeover are about 50ns and are so small that there are no visible errors in the picture. If the RGB inputs are constantly connected, synchronization with the other signals is not necessary. The signals also pass through the contrast- and brightness-control stages. A peak beam current limitation can be effected via an input to a threshold level switching circuit. The threshold level circuit then reduces the contrast-control voltage. Average beam current limitation is effected directly via the contrast-control voltage, whereby under certain circumstances the brightness control is also reduced via an internal diode.

All the pulses required in the IC, and especially for the black current stabilization which will be explained later, are derived from the sandcastle pulse.

Signal processing is effected in parallel in three R, G, B channels and, therefore, the description and explanation will continue to be limited to the R channel.

Figure 3 shows the functional block diagram of the black current stabilizer. The R signal is blanked out and a measuring pulse is inserted for the black current measurement. A subsequent limiter stage prevents overdriving of the video final stages. A control stage is provided for white-point adjustment, which can be effected by means of a DC setting voltage. There is an adding stage in which the voltage from the black current stabilization circuit is added to the R signal. The output stage of the IC can feed the video final stage directly. Its output voltage is supplied via a PNP measuring transistor to the cathode of the CRT. The collector circuit includes a measuring resistor at which voltage drops occur at the respective sequential measuring times; these are due on the one hand to any leakage currents which occur and on the other hand to dark current with leakage currents. These voltages are given to the IC. Following a buffer stage, the measurement voltage for the leakage currents is stored on the capacitor C_L. Switch S_L is only closed at the time when the signal is blanked and no signal current can flow. During the black level measurement time, a reference voltage of 0.5V is subtracted from the voltage to be measured and then compared in a comparator circuit with the stored voltage for the leakage currents. Switch S_d is only closed during the black measurement time and closes the control loop. Capacitor C_d stores the control voltage.

A dark current of 10μA is not too small for reliable evaluation and not too big, so that if it is in the right time position no disturbing effects are visible on the screen.

Insertion of the measurement pulses and their evaluation is sequential; this means that from the measuring resistor through the measurement input and leakage current storage up to and including the comparator circuit, these circuits only have to be realized once and are used for all three channels.

Figure 4 shows the time positions of the various measurement pulse insertions and evaluations. The measurement pulses are after the vertical flyback pulse and are thus above the upper picture edge in the overscan.

The R, G, B signals are blanked up to the inserted measurement pulses. The leakage current of all channels is measured in the line before the first measurement pulse. This is followed by the measurement pulses and their evaluation in the sequence red, green, blue.

A comprehensive application diagram with the video combination TDA3505 and the video final stages is shown in Figure 5.

For two sets of external RGB inputs and larger video input bandwidth, the TDA4580 can be used in place of the TDA3505 (see Figure 6).

The Color Transient Improvement IC — TDA4565

A complete multi-standard decoder can be built with the two ICs described above. A third IC, which can be interconnected in the color difference interface, can be used for color

Multi-Standard Color Decoder With Picture Improvement AN155A

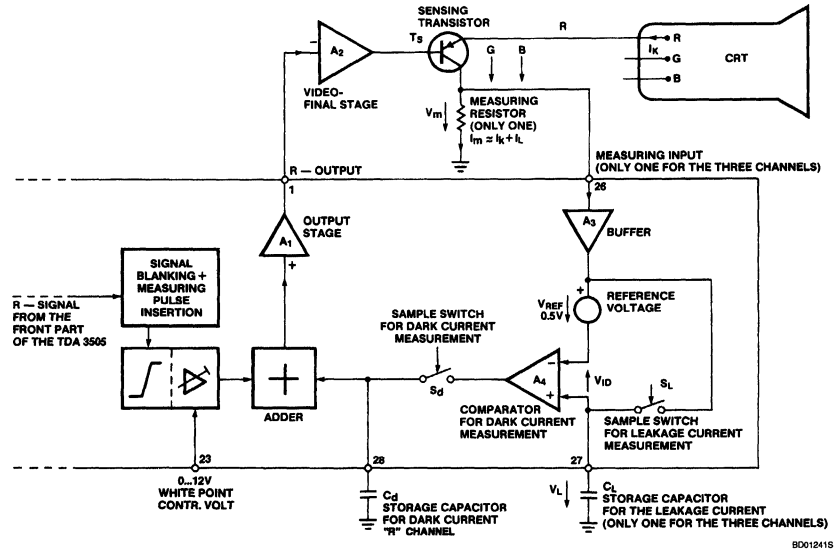


Figure 3. Functional Block Diagram for the Dark Current Stabilization With the Video Combination TDA3505 (R-channel)

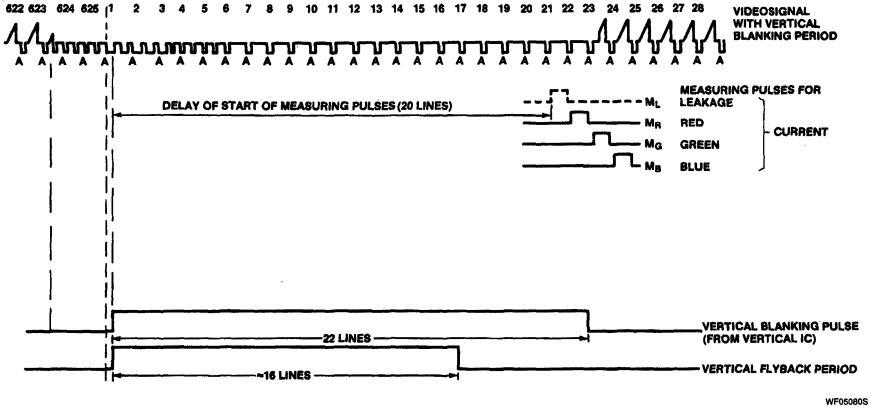


Figure 4. Position of the Measuring Lines of the Video Combination TDA3505

The Color Transient Improvement IC — TDA4565

A complete multi-standard decoder can be built with the two ICs described above. A third IC, which can be interconnected in the color difference interface, can be used for color picture improvements by means of transient improvement of the color difference signals.

In Figure 7, the signal characteristics a) and b) show a transient in the Y and color difference signal. The rise time of the color difference signal is longer, corresponding to the smaller bandwidth. A delay line in the Y channel coordinates the centers of the transients as shown in Figure 7c.

In deviation from the previous signal processing, with the Color Transient Improvement IC, the color difference transient does not occur until the input signal transient is finished, but then occurs with a steepness corresponding to that of the Y signal. The characteristic of this color difference signal is shown in Figure 7d. It is now clear that – as shown in Figure 7e – a correspondingly longer delay is necessary for the Y signal in order to achieve coincidence of the transients.

Color signal transmissions, especially of test pictures coming via this CTI circuit, appear on the screen with the same color definition as RGB transmissions.

Figure 8 gives an explanation of the CTI function: the simplified circuits are shown on the left and the signals occurring at these are

Multi-Standard Color Decoder With Picture Improvement AN155A

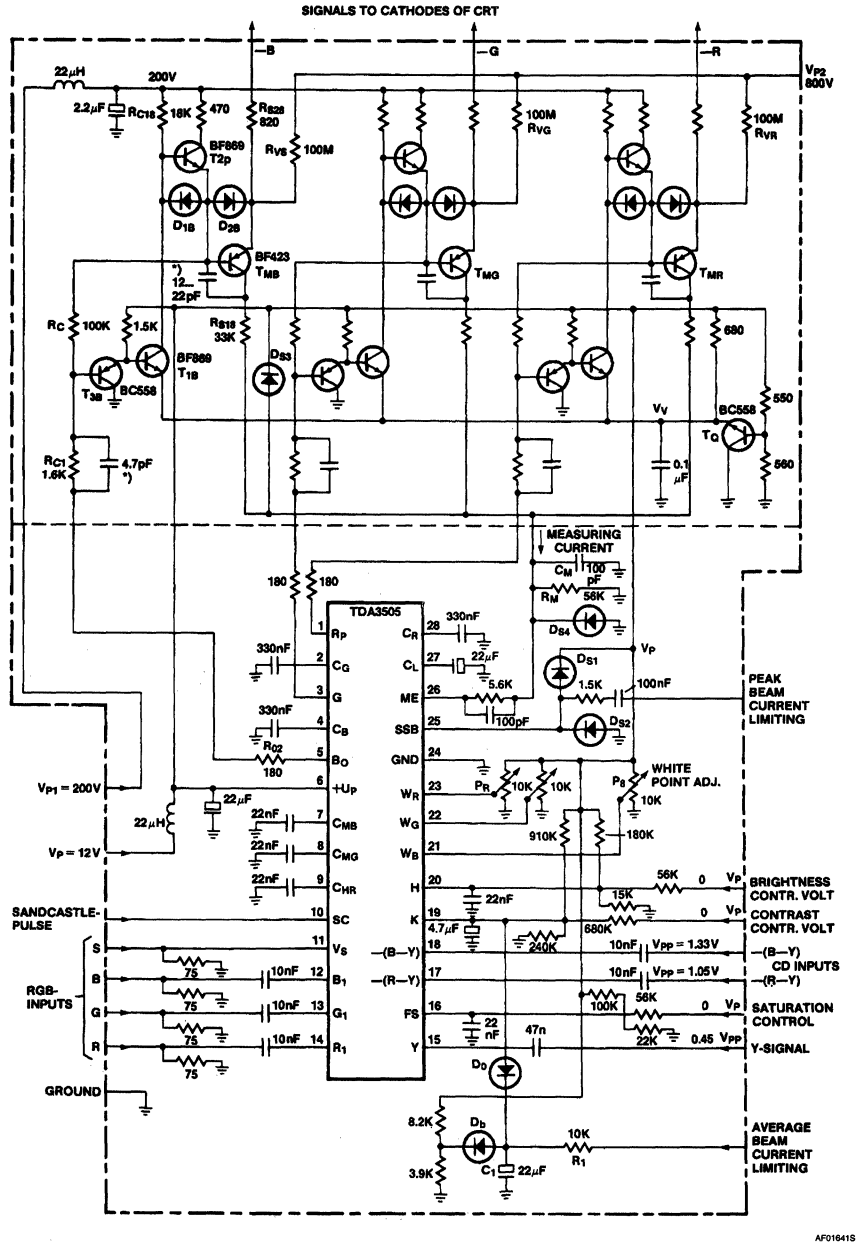


Figure 5. Application Diagram for the Video Combination TDA3505 and the Video Final Stages

Multi-Standard Color Decoder With Picture Improvement AN155A

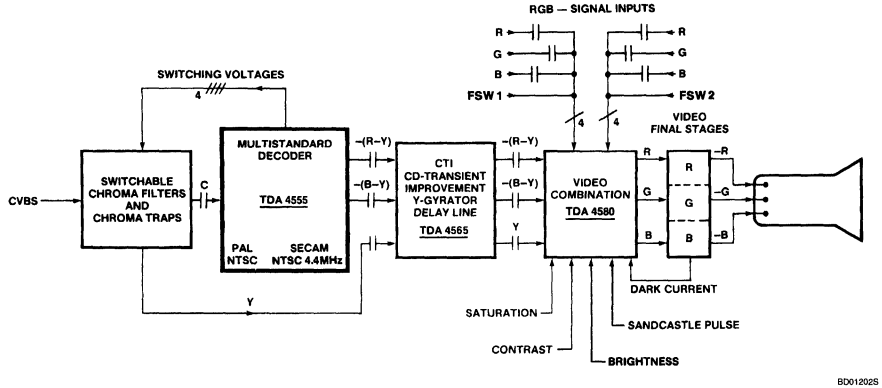


Figure 6. Multi-Standard Decoder Using the TDA4580

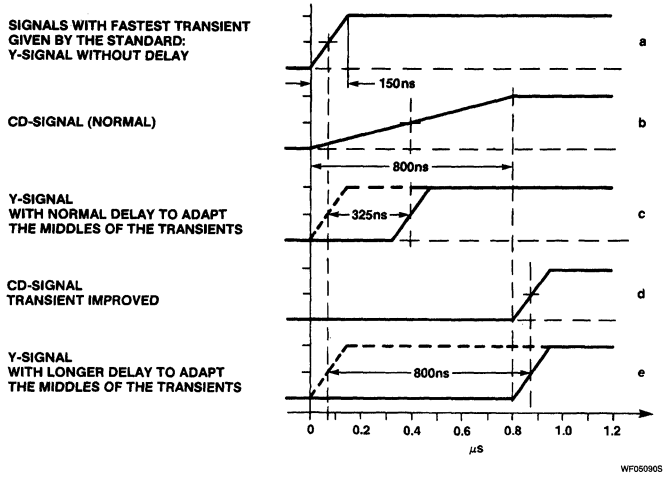


Figure 7. Y-delay Time for CD Signals With and Without Transient Improvement

shown on the right. Part "A" shows a color difference input signal with a fast positive transient corresponding to the maximum bandwidth of the color difference signal.

The subsequent negative signal characteristics are slower. In this circuit, the input signal is supplied after an impedance transformer via a switch and a further impedance transformer to the output. A storage capacitor is connected between the switch and the output impedance transformer, and is charged by the input impedance transformer in accordance with the signal characteristic.

Processing of the switching signal is affected by differentiation of the color difference signal, followed by full-wave rectification. Figure 8b shows the signals obtained in this way, which are supplied to a comparator via a high-pass filter. A diode at the high-pass filter reduces the charge reversal time and, thus, the dead time for generation of a switching signal for transients following in rapid succession. A comparator with threshold voltage generates a switching voltage as shown in Figure 8d from the signal of 8c when the threshold voltage is exceeded, and this triggers the switch. The switch is thus opened at the beginning of a transient and the voltage is maintained by the storage capacitor at the time before the transient. After completion of a fast transient, the switch is closed and the capacitor's charge is changed in approximately 150ns to the voltage after the transient. The effect of a slower transient characteristic is shown in the second part of the signal in Figure 8c. Only a small part is affected. For even slower characteristics, the differential quotient is so small that the threshold voltage is no longer exceeded and there is no effect on the signal. Thus, for the most part, only transients having a steepness approaching the system limit are improved, whereas slower signal characteristics remain unchanged.

Figure 10 shows the entire block diagram with external circuitry of the CTI IC.

The lower CTI section affects signal processing for the two color difference signals in parallel circuits, as already described. Only

one switching signal forming stage is incorporated, and this is triggered by the differentiating stage of the two channels. Thus, the signal switches will always work in parallel, so that transient improvement is also parallel in the two channels.

The transient-improved color difference signals require a longer Y signal delay line with a delay time of up to 1000ns, which is additionally realized in this IC in gyrator technique.

A selection capability has been incorporated for the delay time, by means of a switching voltage, since the total required delay time is dependent on the overall television receiver concept. The delay line comprises a total of 11 gyrator all-pass elements with a delay time of 90ns each, making a total of 990ns. The group delay and frequency behavior of the gyrator delay line is very good up to 5MHz.

A switching stage permits optional by-pass of one, two, or three of these elements, so that a minimum of 8 × 90ns = 720ns is effective. The transient improvement of the color difference signal makes coincidence errors with respect to the Y signal especially visible. A slight increase in delay time by 45ns has therefore been provided for fine tuning, working via an IC pin to be connected to ground.

A signal tapping is available before the last delay element for a further picture improvement capability by means of deflection modulation.

Figure 11 depicts the circuit diagram of the TDA4565.

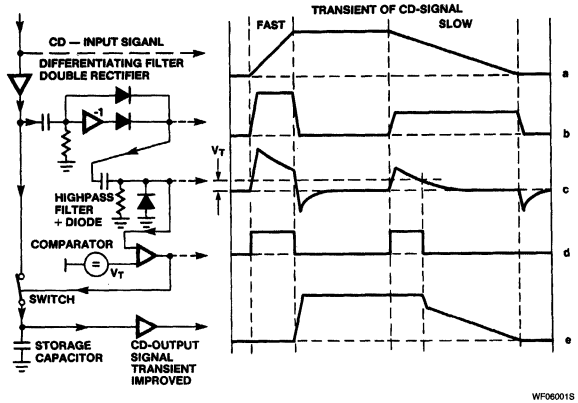
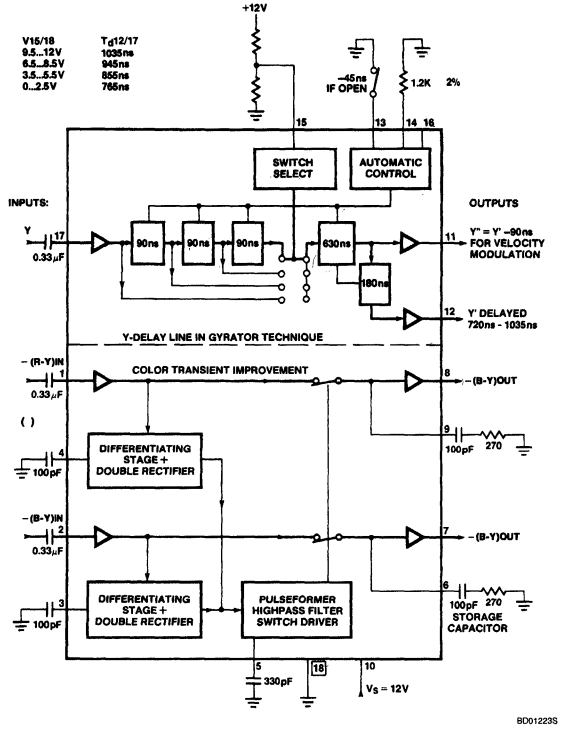


Figure 8. Function of CTI



NOTE:
* The TDA4565 is a high-performance TDA4560.

Figure 9. Block Diagram of Picture-Improvement IC TDA4565*

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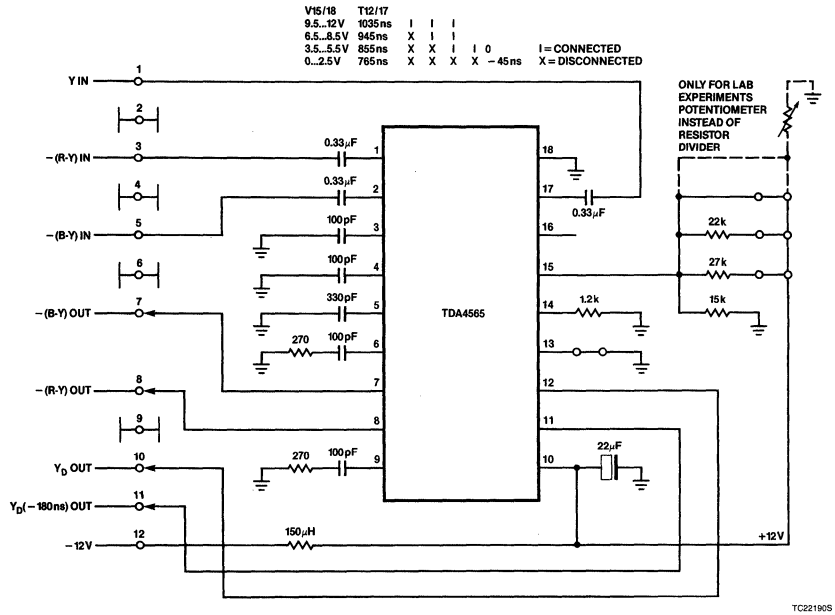
Multi-Standard Color Decoder With Picture Improvement AN155A



NOTE:
* If "Picture Signal Improvement" chip is *not* used, a 330ns delay line in Y channel, as shown in dotted lines, is required.

Figure 10. Various Combinations Used to Implement the Multi-Standard Color Decoder

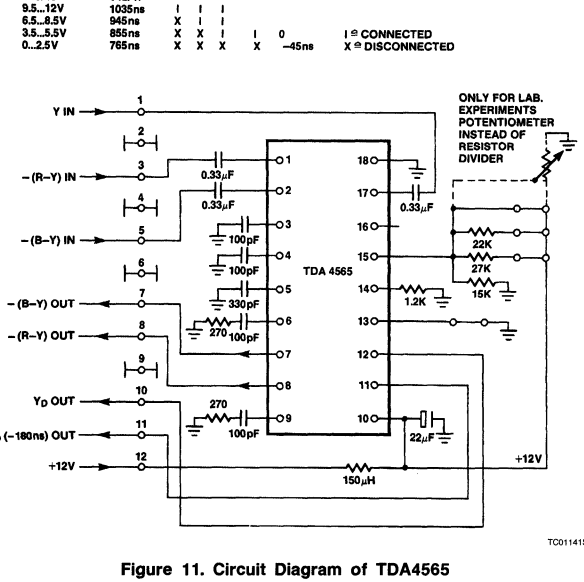


Figure 11. Circuit Diagram of TDA4565

Signetics

TDA3505
Chroma Control Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA3505 performs the control functions in a PAL/SECAM decoder, which also comprises the TDA3510 (PAL decoder) and/or TDA3530 (SECAM decoder).

The required input signals are: luminance and color difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from external sources. RGB output signals are delivered for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

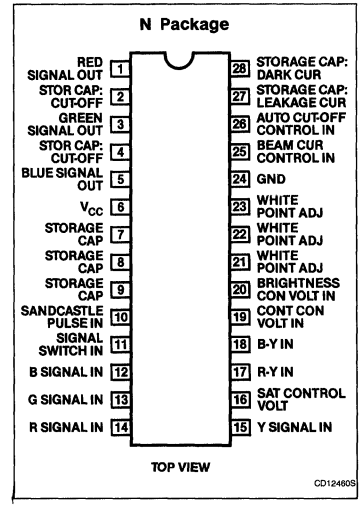
FEATURES

- **Capacitive coupling of the color difference and luminance input signals with black level clamping in the input stages**
- **Linear saturation control in the color difference stages**
- **(G-Y) and RGB matrix**
- **Linear transmission of inserted signals**
- **Equal black levels for inserted and matrixed signals**
- **3 identical channels for the RGB signals**
- **Linear contrast and brightness control, operating on both the inserted and matrixed RGB signals**
- **Peak beam current limiting input**
- **Horizontal and vertical blanking and clamping of the three input signals obtained via a 3-level sandcastle pulse**
- **DC gain controls for each of the RGB output signals (white point adjustment)**
- **Emitter-follower outputs for driving the RGB output stages**
- **Input for automatic cut-off control of the picture tube**
- **Compensation for leakage current of the picture tube**

APPLICATIONS

- **Video processing**
- **TV receivers**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−20°C to +80°C	TDA3505N

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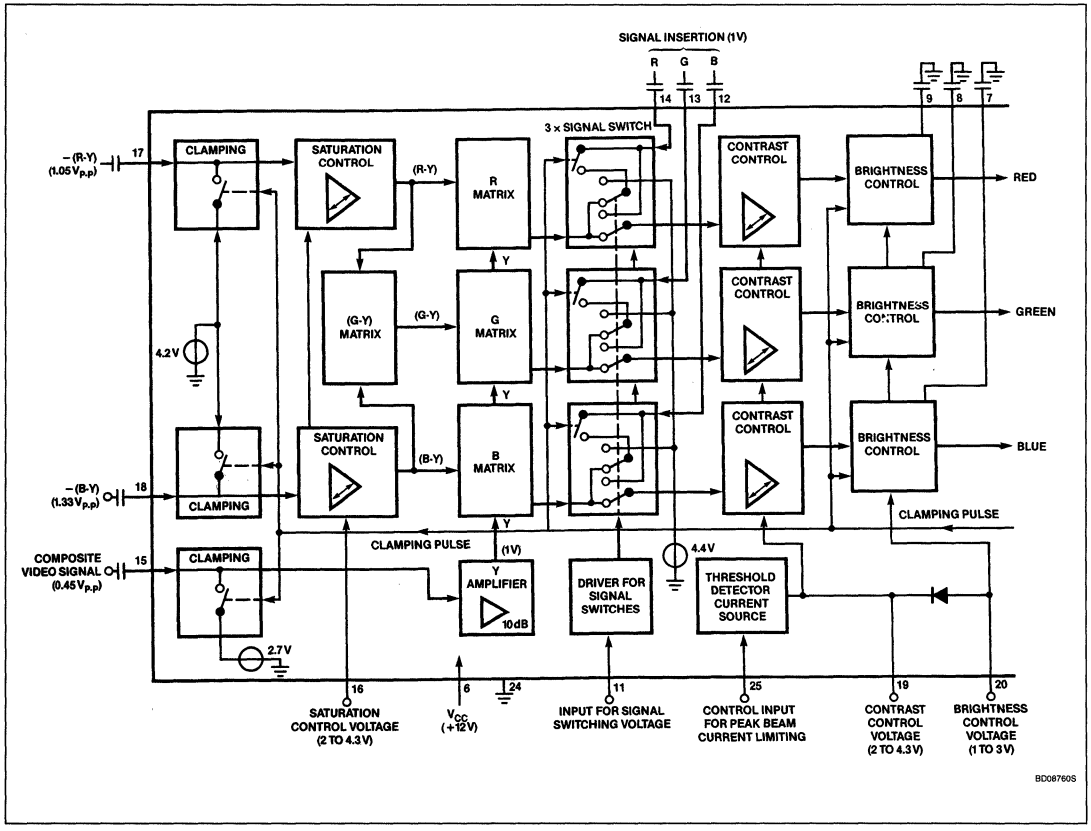
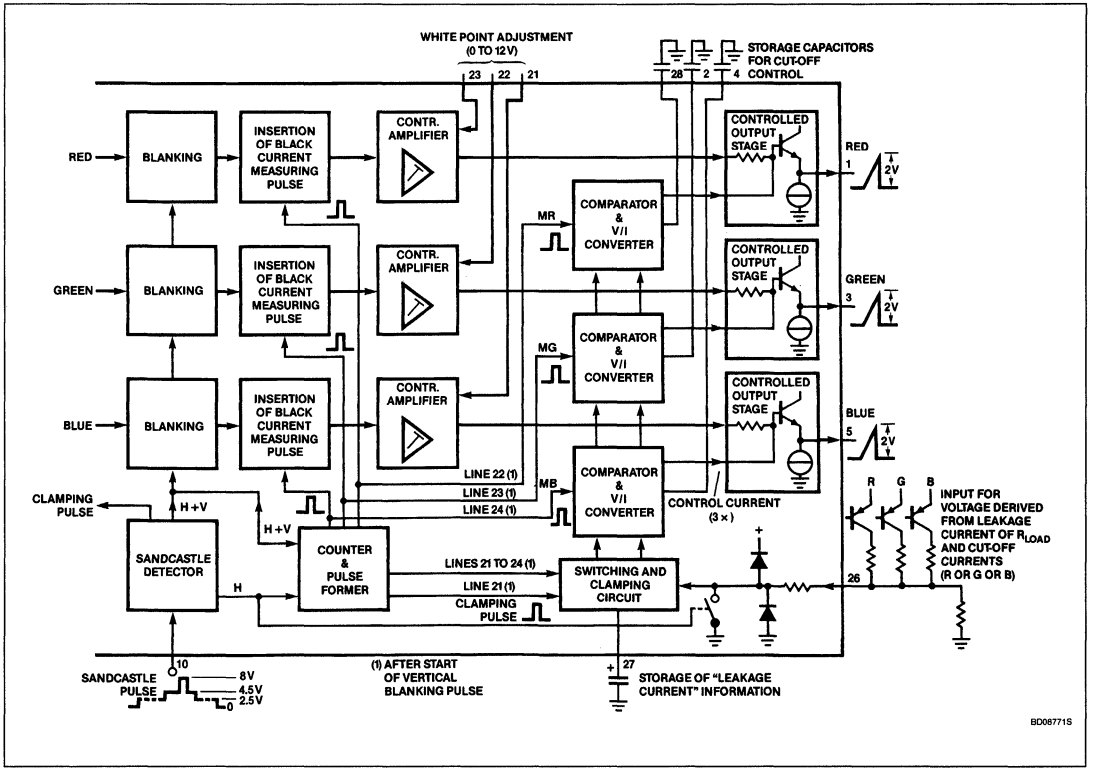
Chroma Control Circuit | TDA3505

BLOCK DIAGRAM (PART A)



BLOCK DIAGRAM (PART B)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{6-24}$	Supply voltage	13.2	V
	Voltages with respect to Pin 24		
V_{26-24}	Pin 26	V_{CC}	V
V_{25-24}	Pin 25	V_{CC}	V
V_{10-24}	Pin 10	V_{CC}	V
V_{11-24}	Pin 11	−0.5 to 3	V
$V_{16, 19, 20-24}$	Pins 16, 19, 20	0.5 V_{CC}	V
$V_{21, 22, 23-24}$	Pins 21, 22, 23	V_{CC}	V
No external DC voltage	Pins 1, 3, 5; 2, 4, 28; 7, 8, 9; 12, 13, 14; 15, 17, 18; 27		
	Currents		
$-I_{1, 3, 5}$	Pins 1, 3, 5	3	mA
I_{19}	Pin 19	10	mA
I_{20}	Pin 20	5	mA
$-I_{25}$	Pin 25	5	mA
P_{TOT}	Total power dissipation	1.7	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC ELECTRICAL CHARACTERISTICS The following characteristics are measured in a circuit similar to Figure 1; $V_{CC} = 12V$; $T_A = 25°C$; $V_{18-24(P-P)} = 1.33V$; $V_{17-24(P-P)} = 1.05V$; $V_{15-24(P-P)} = 0.45V$; $V_{12,13,14-24(P-P)} = 1V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_{CC} = V_{6-24}$	Supply voltage range	10.8		13.2	V
$I_6 = I_{CC}$	Supply current		85		mA
Color difference inputs					
$V_{18-24(P-P)}$	−(B-Y) input signal at Pin 18 (peak-to-peak value)		1.33		V
$V_{17-24(P-P)}$	−(R-Y) input signal at Pin 17 (peak-to-peak value)		1.05		V
$I_{17, 18}$	Input current during scanning			1	μA
$R_{17, 18-24}$	Input resistance	100			kΩ
$V_{17, 18-24}$	Internal DC voltage due to clamping		4.2		V
	Saturation control at Pin 16				
V_{16-24}	control voltage range for a change of saturation from −20dB to +6dB	2.1		4.3	V
V_{16-24}	control voltage for attenuation > 40dB			1.8	V
V_{16-24}	nominal saturation (6dB below maximum)		3.1		V
I_{16}	input current			20	μA
(G-Y) matrix					
$V_{(G-Y)} = -0.51\ V_{(R-Y)} - 0.19\ V_{(B-Y)}$	Matrixed according to the equation				
Luminance amplifier (Pin 15)					
$V_{15-24(P-P)}$	Composite video input signal (peak-to-peak value)		0.45		V
R_{15-24}	Input resistance	100			kΩ
V_{15-24}	Internal DC voltage		2.7		V
I_{15}	Input current during scanning			1	μA
RGB channels					
	Signal switching input voltage for insertion (Pin 11)				
V_{11-24}	on level	0.9		3	V
V_{11-24}	off level			0.4	V
I_{11}	Input current	−100		+200	μA
	Signal insertion (Pin 12: blue; Pin 13: green; Pin 14: red)				
$V_{12, 13, 14-24(P-P)}$	external RGB input signal (black-to-white values)			1	V
$V_{12, 13, 14-24}$	internal DC voltage due to clamping[2]		4.4		V
$I_{12, 13, 14}$	input current during scanning			1	μA
	Contrast control (Pin 19)				
V_{19-24}	control voltage range for a change of contrast from −18dB to +3dB	2		4.3	V
V_{19-24}	nominal contrast (3dB below maximum)		3.6		V
V_{19-24}	control voltage for −6dB		2.8		V
I_{19}	input current at $V_{25-24} \geqslant 6V$			2	μA

DC ELECTRICAL CHARACTERISTICS (Continued) The following characteristics are measured in a circuit similar to Figure 1; V_{CC} = 12V; T_A = 25°C; $V_{18-24(P-P)}$ = 1.33V; $V_{17-24(P-P)}$ = 1.05V; $V_{15-24(P-P)}$ = 0.45V; $V_{12,13,14-24(P-P)}$ = 1V, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Peak beam current limiting (Pin 25)				
V_{25-24}	internal DC bias voltage		5.5		V
R_{25-24}	input resistance		10		kΩ
	input current at contrast control input				
I_{19}	at V_{25-24} = 5.1V		17		mA
V_{20-24}	Brightness control (Pin 20)	1		3	V
	control voltage range				
$-I_{20}$	input current			10	μA
V_{20-24}	control voltage for nominal black level which equals the inserted artificial black level		2		V
ΔV_{20-24}	change of black level in the control range related to the nominal luminance signal (black-white)		50		%
	Internal signal limiting				
	signal limiting for nominal luminance (black to white = 100%)				
	black		−25		%
	white		120		%
White point adjustment (Pin 21: blue; Pin 22: green; Pin 23: red)					
	AC voltage gain[3]				
	at $V_{21, 22, 23-24}$ = 5.5V		100		%
	at $V_{21, 22, 23-24}$ = 0V		60		%
	at $V_{21, 22, 23-24}$ = 12V		140		%
$R_{21, 22, 23-24}$	Input resistance		20		kΩ
Emitter-follower outputs (Pin 1: red; Pin 3: green; Pin 5: blue)					
At nominal contrast, saturation, and white point adjustment					
$V_{1, 3, 5-24(P-P)}$	Output voltage (black-to-white signal, positive)		2		V
$V_{1, 3, 5-24}$	Black level without automatic cut-off control ($V_{28, 2, 4-24}$ = 10V)		6.7		V
I_{SOURCE}	Internal current source		3		mA
$-\Delta V_{1, 3, 5-24}$	Cut-off current control range		4.6		V
Automatic cut-off control (Pin 26)					
The measurement occurs in the following lines after start of the vertical blanking pulse: line 21: measurement of leakage current line 22: measurement of red cut-off current line 23: measurement of green cut-off current line 24: measurement of blue cut-off current					
V_{26-24}	Input voltage range	0		+6.5	V
ΔV_{26-24}	Voltage difference between cut-off current measurement and leakage current measurement[5] Input 26 switches to ground during horizontal flyback		0.7		V

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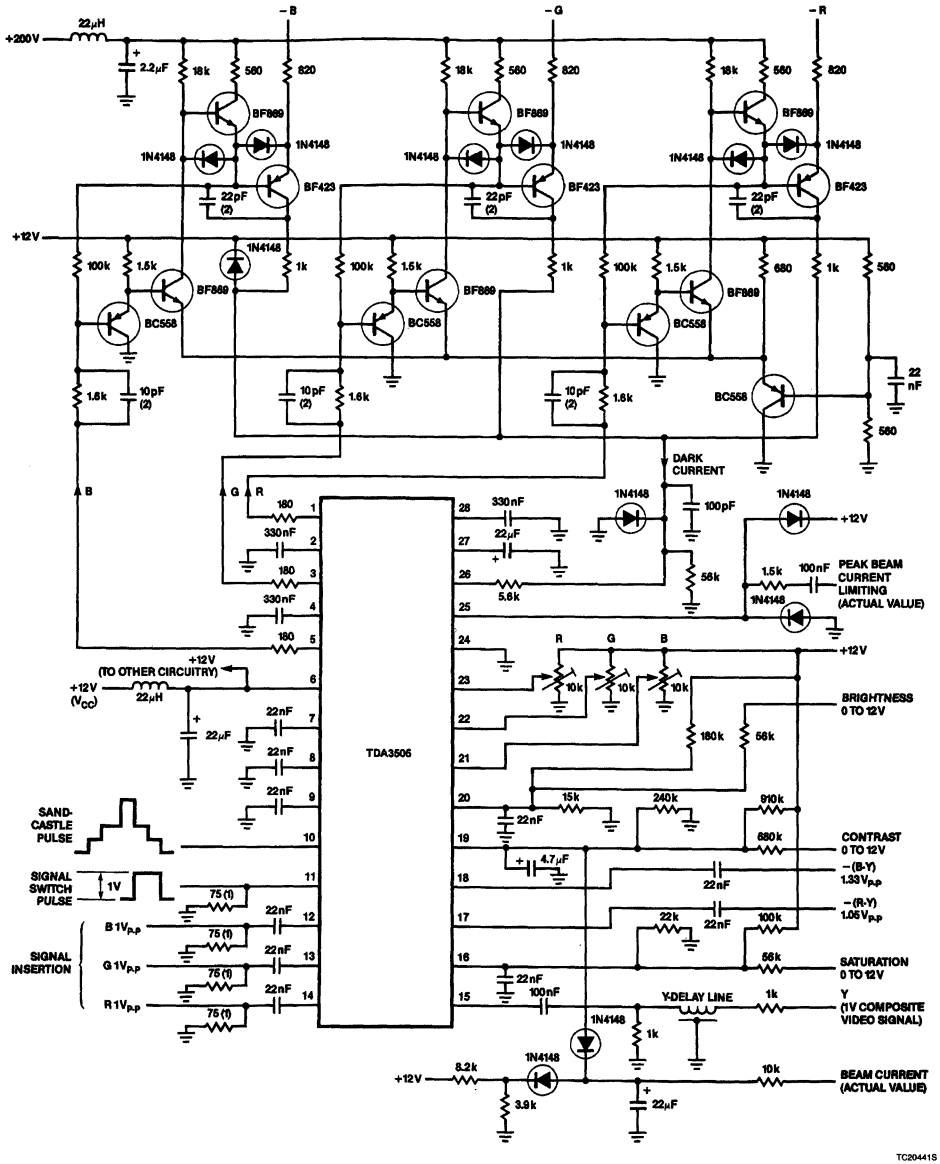
DC ELECTRICAL CHARACTERISTICS (Continued) The following characteristics are measured in a circuit similar to Figure 1; V_{CC} = 12V; T_A = 25°C; $V_{18-24(P-P)}$ = 1.33V; $V_{17-24(P-P)}$ = 1.05V; $V_{15-24(P-P)}$ = 0.45V; $V_{12,13,14-24(P-P)}$ = 1V, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Gain data					
At nominal contrast, saturation, and white point adjustment					
$G_{1, 3, 5-15}$	Voltage gain with respect to Y-input (Pin 15)		16		dB
$d_{1, 3, 5-15}$	Frequency response (0 to 5MHz)			3	dB
$G_{5-18} = G_{1-17}$	Voltage gain with respect to color difference inputs (Pins 17 and 18)		6		dB
$d_{5-18} = d_{1-17}$	Frequency response (0 to 2MHz)			3	dB
$G_{1-14} = G_{3-13} = G_{5-12}$	Voltage gain of inserted signals		6		dB
$d_{1-14} = d_{3-13} = d_{5-12}$	Frequency response (0 to 6MHz)			3	dB
Sandcastle detector (Pin 10)					
	There are 3 internal thresholds (proportional to V_{CC})[6]. The following amplitudes are required for separating the various pulses:				
V_{10-24}	horizontal and vertical blanking pulses[7]	2		3	V
V_{10-24}	horizontal pulse	4		5	V
V_{10-24}	clamping pulse[8]	7.5			V
V_{10-24}	DC voltage for artificial black level (scan and flyback)	7.5			V
V_{10-24}	no keying			1	V
$-I_{10}$	input current			110	μA

NOTES:

1. For saturated color bar with 75% of maximum amplitude.
2. $V_{11-24} < 0.4V$ during clamping time: the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
   $V_{11-24} > 0.9V$ during clamping time: the black levels of the inserted signals are clamped on an internal DC voltage.
   Correct clamping of the external RGB signals is only possible when they are synchronous with the sandcastle pulse.
3. With input Pins 21, 22, and 23 not connected, an internal bias voltage of 5.5V is supplied.
4. Black level of measured channel is nominal; the other two channels are blanked to ultra-black.
5. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal signal blanking continues until the end of the last measurement line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses; otherwise, another control cycle begins.
6. The thresholds are for
   horizontal and vertical blanking: V_{10-24} = 1.5V
   horizontal pulse: V_{10-24} = 3.5V
   clamping pulse: V_{10-24} = 7.0V
7. Blanking to ultra-black (−25%).
8. Pulse duration ⩾ 3.5μs.



NOTES:
1. When supplied via a 75Ω line.
2. Capacitor value depends on circuit layout.

Figure 1. Typical Application Circuit Diagram Using the TDA3505

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TDA3563
NTSC Decoder With RGB Inputs

Product Specification

Linear Products

DESCRIPTION

The TDA3563 is a monolithic, integrated color decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore, it contains a luminance amplifier, and an RGB matrix and amplifier. These amplifiers supply signals up to 5.3V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains inputs for data insertion, analog as well as digital, which can be used for Teletext information, channel number display, etc.

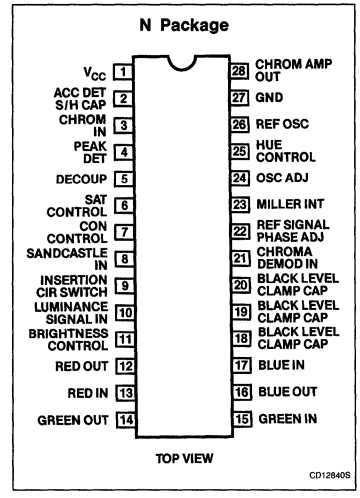
FEATURES

- **Single-chip chroma & luminance processor**
- **ACC with peak detector**
- **DC control settings**
- **External linear RGB inputs**
- **High level RGB outputs**
- **No black level disturbance when nonsync external RGB signals are available on the inputs**
- **Luminance signal with clamp**
- **Black current stabilizer**
- **On-chip hue control**

APPLICATIONS

- **Video monitors and displays**
- **Text display systems**
- **Television receivers**
- **Graphic systems**
- **Video processing**

PIN CONFIGURATION



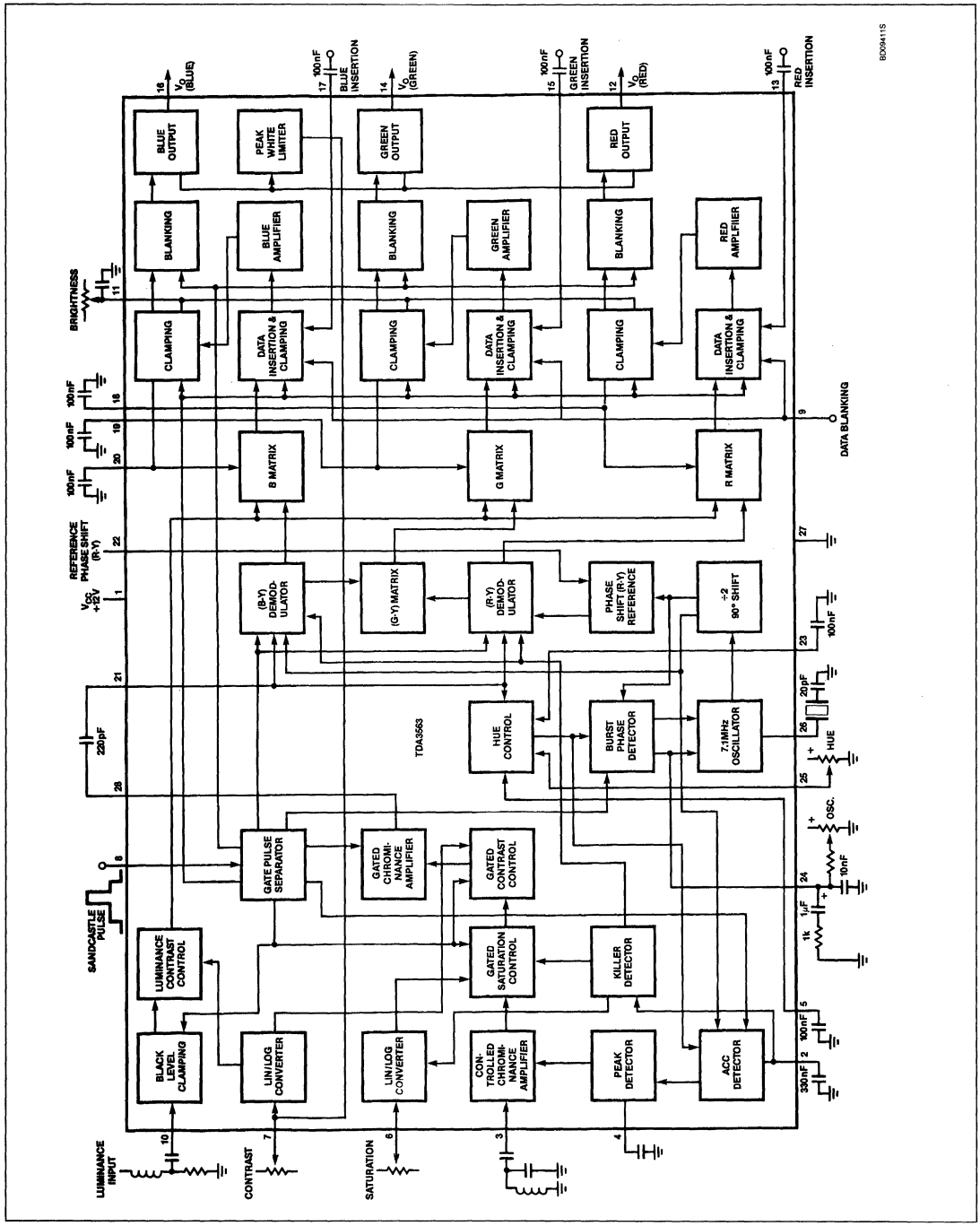
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +65°C	TDA3563N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{1-27}$	Supply voltage (Pin 1)	13.2	V
P_{TOT}	Total power dissipation	1.7	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient (in free-air)	50	°C/W

BLOCK DIAGRAM



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DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 1)					
$V_{CC} = V_{1-27}$	Supply voltage	10	12	13.2	V
$I_{CC} = I_1$	Supply current		85	115	mA
P_{TOT}	Total power dissipation		1	1.4	W
Luminance amplifier					
$V_{10-27(P-P)}$	Input voltage[1] (peak-to-peak value)		0.45		V
	Contrast control range (see Figure 1)	−17		+3	dB
	Control voltage for an attenuation of 40dB		1.2		V
I_7	Contrast control input current			15	μA
Chrominance amplifier					
$V_{3-27(P-P)}$	Input voltage[2] (peak-to-peak value)	55	550	1100	mV
	ACC control range	30			dB
	Change of the burst signal at the output over the whole control range			1	dB
V_{28-27}	Output voltage[3] (peak-to-peak value) at a burst signal of 0.3V peak-to-peak		0.15		V
V_{28-27}	Maximum output voltage range (peak-to-peak value); $R_L = 2k\Omega$		4		V
α_{28-3}	Frequency response between 0 and 5MHz			−2	dB
	Saturation control range (see Figure 2)	50			dB
I_6	Saturation control input current			20	μA
$\lvert Z_{28-27} \rvert$	Output impedance of chrominance amplifier		25		Ω
I_{28}	Output current			10	mA
Reference part					
	Phase-locked loop				
Δf	catching range[4]	500	700		Hz
$\Delta\varphi$	phase shift[4, 5]			5	deg
	Oscillator				
TC_{OSC}	temperature coefficient of oscillator frequency[4]		−1.5		Hz/°C
Δf_{OSC}	frequency variation when supply voltage increases from 10V to 13.2V[4]		40		Hz
R_{26-27}	input resistance (Pin 26)		400		Ω
C_{26-27}	input capacitance (Pin 26)			10	pF
	ACC generation (Pin 2)				
V_{2-27}	control voltage at nominal input signal		5.0		V
V_{2-27}	control voltage without chrominance input		2.7		V
V_{2-27}	color-off voltage		3.0		V
V_{2-27}	color-on voltage		3.3		V
	HUE control				
	control range	±50			deg

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Demodulator part					
$V_{21-27(P-P)}$	Input burst signal amplitude (peak-to-peak value)		300		mV
	Ratio for demodulated signals for equal input signal amplitudes				
$\frac{V_{16-27}}{V_{12-27}}$	(B-Y)/(R-Y)		1.06± 10%		
$\frac{V_{14-27}}{V_{12-27}}$	(G-Y)/(R-Y); no (B-Y) signal		−0.27± 20%		
$\frac{V_{14-27}}{V_{16-27}}$	(G-Y)/(B-Y); no (R-Y) signal		−0.2± 20%		
	Frequency response between 0 and 1MHz			−3	dB
RGB matrix and amplifiers					
$V_{12, 14, 16-27}$	Output voltage[3] (peak-to-peak value) at nominal luminance/contrast (black-to-white)	4.5	5.3	6.3	V
$V_{12, 14, 16-27}$	Maximum peak-white level[6]	9.0	9.3	9.6	V
$I_{12, 14, 16}$	Maximum output current			10	mA
	Output black level voltage for brightness control of 2V		2.7		V
	Brightness control voltage range		see Figure 3		
I_{11}	Brightness control input current			50	μA
	Relative spread between the R, G, and B output signals			10	%
	Blanking level at the RGB outputs	1.9	2.1	2.3	V
$\frac{\Delta V_{BL}}{V_{BL}} \times \frac{V_{CC}}{\Delta V_{CC}}$	Tracking of output black level with supply voltage		1.1		
$\lvert Z_{12, 14, 16-27} \rvert$	Output impedance of RGB outputs		50		Ω
	Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5MHz			−3	dB
Data insertion					
$V_{13, 15, 17-27(P-P)}$	Input signals (peak-to-peak value) for an RGB output voltage of 5V (peak-to-peak)	0.9	1	1.1	V
Data blanking (Pin 9)					
V_{9-27}	Input voltage for no data insertion			0.3	V
V_{9-27}	Input voltage for data insertion	0.9			V
$V_{9-27(m)}$	Maximum input voltage			2	V
t_D	Delay of data blanking			20	ns
I_9	Input current			35	μA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sandcastle input (Pin 8)					
V_{8-27}	Level at which the RGB blanking is activated	1	1.5	2	V
V_{8-27}	Level at which burst gating and clamping pulse are separated	6.5	7.0	7.5	V
t_D	Delay between black level clamping and burst gating pulse		0.4		µs
	Input current				
$-I_8$	at $V_{8-27} = 0$ to 1V			1	mA
I_8	at $V_{8-27} = 1$ to 8.5V		20		µA
I_8	at $V_{8-27} = 8.5$ to 12V			2	mA

NOTES:
1. Signal with negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a color bar with 75% saturation; chrominance to burst ratio is 2.2:1.
3. At nominal contrast and saturation. Nominal contrast is specified as the maximum contrast −3dB and nominal saturation as the maximum saturation −6dB.
4. All frequency variations are referred to 3.58MHz carrier frequency.
5. For ±400Hz deviation of the oscillator frequency.
6. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at Pin 7 (contrast control); discharge current is 1.5mA.

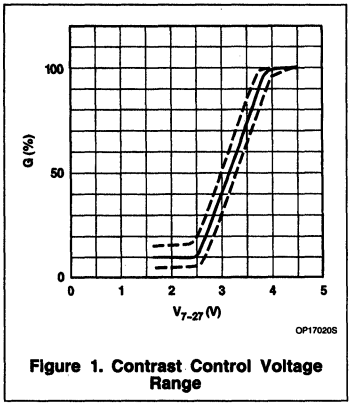


Figure 1. Contrast Control Voltage Range

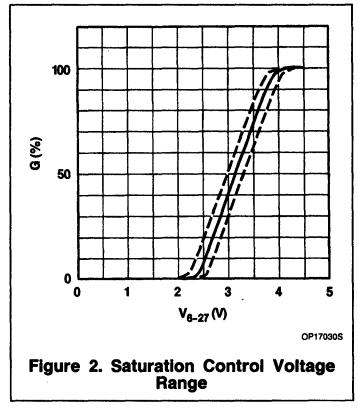


Figure 2. Saturation Control Voltage Range

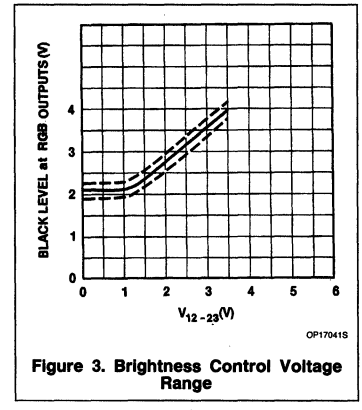


Figure 3. Brightness Control Voltage Range

APPLICATION INFORMATION

The function is described beside the corresponding pin number.

1 +12V power supply — The circuit gives good operation in a supply voltage range between 8 and 13.2V provided that the supply voltage for the controls is equal to the supply voltage of the TDA3563. All signal and control levels have a linear dependency on the supply voltage. The current consumed by the IC at +12V is typically 85mA. It is linearly dependent on the supply voltage.

2 Control voltage for identification — The output pulses of the ACC detector are detected with a sample-and-hold circuit to obtain information for the color-killer. The output is available at Pin 2.

3 Chrominance input — The chrominance signal must be AC-coupled to the input. Its amplitude must be between 55 and 1100mV$_{P-P}$ (25 to 500mV$_{P-P}$ burst signal). All figures for the chrominance signals are based on a color bar signal with 75% saturation, if the burst-to-chrominance ratio of the input is 1:2.2.

4 Control voltage ACC detector — The shifted burst signal is synchronously demodulated in a separate ACC detector to generate the ACC voltage. The output pulses of this detector are peak detected to control the gain of the chrominance amplifier, thus preventing blooming-up of the color during weak signal reception.

5 Decoupling of the 90° phase shift circuit — A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. The control circuit is decoupled by a capacitor at this pin.

6 Saturation control — The saturation control range is in in excess of 50dB. The control voltage range is 2 to 4V. Saturation control is a linear function of the control voltage.

When the color-killer is active, the saturation control voltage is reduced to a low level if the resistance of the external control network is sufficiently high. Then the chrominance amplifier supplies no signal to the demodulator. Color switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply, the color-killer circuit is overruled so that the color signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also Pins 24 and 26).

7 Contrast control — The contrast control range is 20dB for a control voltage change from +2V to +4V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1V or less. If one or more output signals surpasses the level of 9V, the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging a 10μF capacitor via an internal current sink.

8 Sandcastle and vertical blanking input — The output signals are blanked if the amplitude of the pulse is between 2V and 6.5V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7.5V. The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of the video signal on the sync pulse. The duration should be about 4μs for proper ACC operation.

9 Video-data switching — The insertion circuit is activated by means of this input by an input pulse between 1 and 2V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted, this pin should be connected to ground (Pin 27).

The switching times are very short (< 20ns) to avoid colored edges of the inserted signals on the screen.

10 Luminance signal input — The input signal should have a peak-to-peak amplitude of 0.45V (peak white to sync) to obtain a black-white output signal of 5.3V at nominal contrast. It must be AC-coupled to the input by a capacitor of about 22nF. The signal is clamped at the input to an internal reference voltage. The 1kΩ luminance delay line can be applied because the luminance impedance is very high. Consequently, the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally, the coupling capacitor value may be small.

11 Brightness control — The black level of the RGB outputs can be set by the voltage on this pin (see Figure 3). The minimum black level is identical to the blanking level. The black level can be set higher than 4V; however, the available output signal amplitude is reduced (see also Pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16 RGB outputs — The output circuits for red, green, and blue are identical. Output signals are 5.3V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2.1V. The peak white level is limited to 9V. When this level is exceeded, the output signal amplitude is reduced via the contrast control (see also Pin 7).

13, 15, 17 Inputs for external RGB signals — The external signals must be AC-coupled to the inputs via a coupling capacitor of about 100nF. Source impedance should not exceed 150Ω. The input signal required for a 5V$_{P-P}$ output signal is 1V$_{P-P}$. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used, the coupling capacitors have to be connected to ground (Pin 27).

18, 19, 20 Black level clamp capacitors — The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100nF.

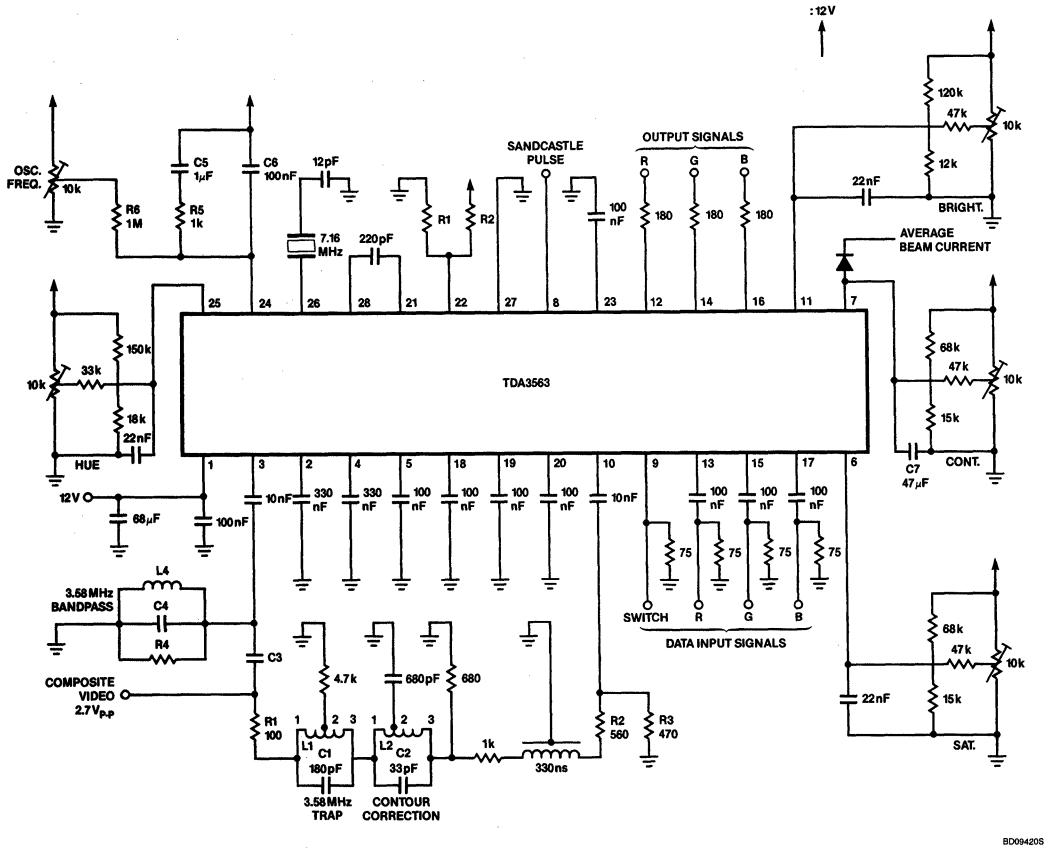
21, 22 Demodulator input and reference signal phase adjustment — The (R-Y) and (B-Y) demodulator inputs are internally connected (Pin 21). The phase angle between the two reference carriers is 115°. At the nominal hue adjustment, the (B-Y) signal is demodulated with a difference of 0°. The phase shift of 115° can be changing the voltage at Pin 22. The gain at the two demodulators is identical. The (G-Y) is composed of −0.27(R-Y) −0.22(B-Y).

23, 25 Hue control — The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the demodulator input signal. This phase shift is obtained by generating a 90° shifted sine wave via a Miller integrator (biased via Pin 23) which is mixed with the original burst signal.

24, 26 Reference oscillator — As the burst phase detector has an asymmetrical output, the oscillator can be adjusted by changing the voltage of the output (Pin 24) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When Pin 6 (saturation control) is connected to the positive supply line, the burst phase detector is based in its nominal position and the color-killer is overruled. This position can, therefore, be used for the adjustment of the oscillator.

27 Ground

28 Output of the chrominance amplifier — The (R-Y) and (B-Y) demodulator input (Pin 21) is AC-coupled to this output.



NOTES:
Coils: TOKO 7P material
L1: 24 turns chroma bandpass
L2: 2 × 12 chroma trap
L3: 16 + 39 delay equalization

Figure 4. The Application Circuit of the TDA3563

Signetics

AN156
Application of the NTSC Decoder: TDA3563

Application Note

Linear Products

Author: H.J.S. Aben

INTRODUCTION

The 28-pin single-chip decoder TDA3563 combines all the functions required for the identification and demodulation of NTSC signals.

Furthermore it contains a luminance amplifier, and an RGB matrix and RGB amplifiers which provide nominal output signals of $5.3V_{P-P}$.

It also contains analog inputs for external RGB data signals. Switching over from video handling to data insertion occurs via fast video-data switching, which allows inlay of data into the running picture, without causing colored edges at the transients. So these inputs can be used for teletext, channel numbering, TV games, etc. The output signals are controlled by a peak white limiter, by means of an internal current sink on the contrast control voltage, which reduces the outputs when they tend to become too large. A description of the IC and its external circuitry is given in this report.

CIRCUIT DESCRIPTION

The block diagram of the TDA3563 is given in Figure 1. The internal circuitry connected directly to the pins will be discussed at the concerning subjects.

The Luminance Signal (see Figure 2)

The luminance channel is designed for luminance signals with negative-going sync pulses which should have a typical amplitude of $0.45V_{P-P}$ (peak white to sync). So the decoder can also be easily designed to accept external video signals with an amplitude of $1V_{P-P}$ (e.g., video recorder signals). The luminance signal is AC-coupled to the luminance input (Pin 10) where it is clamped to an internal reference voltage of about $2.5V_{DC}$.

The input impedance is very high (input current typ. 0.15μA) and the charging and discharging currents of the coupling capacitor are very small. Therefore a 1k delay line circuit can be placed in front of it, without influencing the black level of the input signal noticeably (also see Figure 3). Additionally, the coupling capacitor can be small: 10nF. During clamping the input is very low-ohmic, which reduces noise and residual signals.

The clamping pulse is obtained from the upper part of the sandcastle pulse (Pin 8) and it operates only during the back porch of the video signal. In the luminance contrast control stage, the luminance is gain-controlled by a DC voltage from the lin-log converter of the contrast control voltage at Pin 7. For a control range of 2.0 to 4.0V, there exists a linear relationship between a voltage change at Pin 7 and the gain of the luminance contrast control stage (see Figure 4a).

The input impedance at this Pin 7 is very high (maximum input current 15μA), so remote control circuitry can directly drive the contrast control without need for an impedance converter. (This also holds for the saturation and the brightness control inputs, respectively, Pins 6 and 11.)

The total contrast range is in excess of 20dB. At nominal contrast control voltage ($3.4V_{DC}$) and nominal input signal of $0.45V_{P-P}$ (including sync pulse) the output signals at the RGB output pins (Pins 12, 14 and 16, respectively) are $5.3V_{P-P}$ (black-to-white). At maximum contrast control voltage ($4V_{DC}$), the output signals have an amplitude of +3dB, with respect to their nominal value. At minimum contrast control voltage ($2.0V_{DC}$), the output signals still have an amplitude of minus 17dB with regard to their nominal value (about 15% rest signal). This is to avoid having the picture completely disappear when the front controls are not tuned correctly.

If the voltage at Pin 7 is below $1.2V_{DC}$ (this is outside of the normal contrast control range) the output signals are completely suppressed (minus 40dB); also see Figure 4a. After contrast control, the luminance signal is fed to the three matrix circuits.

The External Luminance Input Circuit (see Figure 3)

A composite video signal of $2.7V_{P-P}$ is assumed with a low-ohmic source impedance: The video signal is fed to a 3.58MHz trap (L1C1) and a delay equalization circuit (L2C2). Because of the latter, the attenuation of the 3.58MHz chroma signal can be very high without causing group delay distortion into the luminance signal. It also has the additional advantage of contour correction, which generates very sharp transients. As shown in Figure 6:

- the upper signal shows a 250kHz bar with a contour correction of about 10%
- the lower signal is the corresponding sweep signal up to 10MHz.

The extension of contour correction depends on the source impedance of the video signal (the original source impedance plus the value of resistor R1) and on the adjustment of L2. (If a cheaper 3.58MHz trap or a comb filter is preferred, the filters L1C1 and L2C2 can be replaced by it.)

After trapping, the luminance signal is fed via a luminance delay line and a resistor network to a coupling capacitor of 10nF.

***NOTE:**
If a video input signal of $1V_{P-P}$ is used R2 can be omitted and R3 should then have a value of 1kΩ without changing the rest of the input circuit.

The Chrominance Signal (see Figures 3 and 7)

The composite video signal is fed to the 3.58MHz bandpass filter, consisting of L4, C4 and R4 via C3. The chrominance information is then fed via a coupling capacitor of 10nF to the chroma input (Pin 3). The chrominance channel has an asymmetrical input and must be AC-coupled; its amplitude should be between 55 and $1100mV_{P-P}$ (which corresponds to 25 and $500mV_{P-P}$ burst information of a 75% saturated color bar). It may not exceed $1.1V_{P-P}$, otherwise clipping of the input signal will occur. The chrominance signal is first fed to the gain control stage, which has a control range in excess of 30dB, controlled by the ACC (Automatic Color Control) detector. After this the signal is fed to the gated saturation and contrast control stages. The contrast stage is directly coupled to the luminance contrast control, so that there is good tracking between the luminance and the chrominance contrast control. Typical tracking is within 1dB over a control range of 10dB, starting at maximum contrast.

The saturation control stage is driven by a DC voltage of the lin-log converter of the saturation control voltage at Pin 6. The control range is in excess of 50dB, which corresponds to a saturation control voltage of 2.0 to $4.0V_{DC}$; also see Figure 4b.

To cancel the settings of saturation and contrast control during the burst information, the two control stages are set at maximum gain during flyback. The chrominance signal is fed to the chrominance output (Pin 28) via an emitter-follower.

***NOTE:**
If a video signal of $1V_{P-P}$ is used, C4 should have a value of xxpF and R4 can be omitted.

Via a capacitor of 220pF, the chrominance output signal at Pin 28 is fed to the demodula-

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tor input, Pin 21, where the chrominance signal is split up into two ways, the first going to the color demodulators and the second going to the chrominance reference circuit.

The Chrominance Reference Circuit (see Figure 8)

The chrominance signal at Pin 21 is fed to a Miller integrator, which is biased via Pin 23, where it is shifted over 90 degrees. Both the original incoming signal and the shifted signal are fed to a mixer circuit, which is controlled by the DC voltage of the hue control voltage at Pin 25.

The voltage range of the hue control at Pin 25 corresponds to a phase control (see Figure 5a). In this way the chrominance signal of the reference circuit is phase-controlled. A gain control circuit is required in the 90° phase-shift circuitry to make the chrominance voltage independent of the hue setting. Its control voltage is decoupled by the capacitor connected at Pin 5.

The Burst Phase Detector

The burst phase detector consists of a synchronous detector, in which the phase-controlled chrominance signal is demodulated by the (R-Y) reference signal, obtained from the divide-by-2 circuit of the reference oscillator. Via the low-pass filter R5, C5 and C6 at Pin 24 the demodulated burst information is fed to the reference oscillator. In this way the reference oscillator is locked to the hue-controlled chrominance signal.

The Reference Oscillator

The 7.16MHz reference oscillator operates at twice the subcarrier frequency and is controlled by the burst phase detector, which is gated with the narrow part of the sandcastle pulse. As the burst phase detector has an asymmetrical output, the oscillator can be adjusted by changing the voltage of the output (Pin 24) via a high-ohmic resistor (R6). The capacitor in series with the X-tal (Pin 26) should then have a fixed value.

When Pin 6 (saturation control) is connected to the positive supply line, the burst phase detector is biased in its nominal position and the color-killer is overruled. In this position the reference oscillator can be adjusted.

By dividing the oscillator signals by a factor 2, two reference signals, with a mutual phase difference of 90 degrees, are obtained.

ACC and Color Killing

For the generation of the ACC control voltage, the phase-controlled burst information is synchronously demodulated in a separate ACC detector. Because the burst information as well as the reference signals are phase-controlled, there will be no mutual phase difference. In this way the demodulated burst amplitude information will be independent of hue settings.

The output pulses of this detector are peak detected at Pin 4 to control the gain of the chrominance amplifier, thus preventing blooming up of the color during weak signal reception, and fed to the ACC gain control stage of the chrominance channel (see Figure 7). To obtain information for the color-killer, the output pulses of the ACC detector are also detected by a sample-and-hold circuit; this output voltage is available at Pin 2. For a decreasing burst information, the control voltage also decreases until it reaches an internal fixed reference voltage of xxV_{DC}; then the killer becomes active. At that moment the demodulators are switched off and an internal current sink reduces the saturation control voltage to a low level (provided the source impedance of the external saturation control network is sufficiently high). Color switch-on can be delayed by proper choice of the time constant of the saturation setting circuit. Manual killing can be achieved by connecting Pin 6 to ground.

Reference Signals for the Demodulators (see Figure 9)

The reference signal for the (B-Y) color demodulator is directly achieved from the divide-by-two circuit.

To obtain a flesh-tone correction, the reference signal for the (R-Y) color demodulator is achieved by mixing the (R-Y) and (B-Y) reference signals to a new (R-Y)* reference signal. When Pin 22 is left open there is a mutual phase relation of about 115 degrees between the (B-Y) and the (R-Y)* reference signal. If a DC voltage is connected to Pin 22, this phase angle can be adjusted between 90° and 140° (see Figure 10).

The Color Demodulators

The incoming chrominance signal at Pin 21 is also fed to the two demodulators. The reference signals for the demodulators are hue-controlled, so the chrominance output signals of the demodulators will also be hue-controlled.

Also, for flesh-tone correction, the gain of the two demodulators is made identical. This means that the amount of (R-Y) information is increased by a factor of 1.78.

The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix, where the (G-Y) signal is composed by:

$$(G\text{-}Y) = -0.27(R\text{-}Y) - 0.22(B\text{-}Y).$$

This means that only the red information is increased.

The Video Control Circuits (see Figure 11)

The RGB Matrices

Because the three matrix and output circuits are identical, only the R-channel will be described.

The luminance signal from the luminance contrast control stage and the color-difference signal from the (R-Y) matrix are added in the matrix circuit. After this the signal is fed to the Video-Data switch.

The Video-Data Switch

This single-chip NTSC decoder also has the facility for inserting external analog RGB signals at Pins 13, 15 and 17, respectively. The black level of the inserted signals are equalized to the black level of the internal video signals. In this way there will be no mutual black level difference between the video and the inserted RGB signals. For this purpose, the external signals are AC-coupled to the input pins and clamped during the upper part of the sandcastle pulse. The source impedance of the external signals should not exceed a value of 150Ω to avoid any disturbance of black level during clamping.

Switching-over from video handling to external data insertion is activated by means of the input signal at Pin 9. If the voltage level at this switch input Pin 9 exceeds a DC level of $0.9V_{DC}$, the internal RGB signals, coming from the matrix circuits, are switched off and the external RGB signals are inserted. Because switching times are very short (within 20ns) inlay of data into the running picture, e.g., teletext information, channel numbering is possible without causing colored edges at the transients of the inserted signals. For an output signal amplitude of nominal $5.3V_{P\text{-}P}$, the external input signal should have an amplitude of $1V_{P\text{-}P}$.

Because the inserted signals are clamped by means of the sandcastle pulse, the external RGB signals must be synchronous with the video input signal and the sandcastle pulse.

Even if they are not inserted by means of the video-data switching signal at Pin 9, the external signals at the input Pins 13, 15 and 17 must be synchronized. This is to avoid a disturbance of the control voltages at the storage capacitors at Pins 18, 19 and 20, by large current surges, introduced by voltage steps in the external signals during clamping time. This effect would disturb the black level of the output signals considerably and would be visible on the screen. If only video handling is wanted, the components at the switch and data inputs can be omitted.

The Brightness Control
After the Video-Data Switch, the signal is amplified and fed to a black level clamp. The black level of the output signal is compared with an external reference voltage level (Pin 11) which is used for brightness setting, and the control voltage is stored in a capacitor that is connected to Pin 20 (Pins 19 and 18 for G and B, respectively). The clamping pulse is derived from the small upper part of the sandcastle pulse at Pin 8.

The Peak White Limiter
The maximum white level of the output signals is $9.3V_{DC}$. If one (or more) of the output signals tends to surpass this level, the output signal will be clipped to this maximum voltage level and at the same time the peak white limiter will become active. It reduces the output signals via the contrast control by discharging the smoothing capacitor C7 at Pin 7 via an internal current sink of about 5mA. As long as the output signal is too high, the current sink will be active. The time constant of decreasing the contrast setting voltage is determined by the internal discharging current of 5mA and by the value of the smoothing capacitor C7. The recovery time is determined by the source impedance of the resistor network at Pin 7. The complete time constant of loading and unloading should be chosen so that the peak white limiting action will not become visible on the screen within one field period. When this time constant is too small, the contrast setting voltage will decrease too rapidly (e.g., within some line periods) and will also recover too fast after the limiting action stops (depending on the picture contents). When this happens, the complete action becomes visible on the screen; if there is a white object on the screen (with too high amplitude), the complete video signal amplitude will be reduced rapidly, and when the object ends, the video signal amplitude will also increase very fast. This would result in a display of horizontal bars of different brightness on the screen; the length and the number of bars depends on the video contents.

NOTE:
The peak white limiter will also be activated if the inserted RGB signals become too large. However, these signals are not contrast-controlled and cannot be reduced by the limiter. If the inserted signals are inlaid into a running picture, and the peak white limiter is activated by them, the RGB signals will be clipped at $9.3V_{DC}$, but the normal video signal will disappear because the limiter will reduce the contrast-setting voltage completely.

The Sandcastle Pulse Processor (see Figure 9)

In the sandcastle pulse processor, the sandcastle pulse at Pin 8 is separated into two timing pulses. The first pulse is separated at a voltage level of $1.5V_{DC}$ and will be used for gating in the chrominance channel (for the gated saturation and contrast amplifiers) and for blanking the RGB output signals. During blanking, a level of $2V_{DC}$ is available at the outputs.

The second timing pulse is separated at a voltage level of $7V_{DC}$; this pulse is used for black level clamping and burst-keying. Therefore, the upper part of the sandcastle pulse should start just after the horizontal synchronization pulse to prevent black level clamping during the sync. pulse.

The Control-Setting Circuits

Figure 3 also shows the resistor networks that are used to make the control voltage ranges, for the several controls, out of a control range of 0 to V_{SUPPLY}. This means that all the front controls of the color receiver are standard from zero up to the supply voltage. Using such networks it is also possible to transform control voltage ranges from remote-control systems to the required voltage ranges in an easy way. See Appendix I.

The contrast control voltage should also be controlled by the average beam current-limiter, which should become active if the average beam current exceeds a certain value. At that moment the capacitor at Pin 7 should be discharged via diode D1.

The contrast and saturation control voltages can be overruled by service switches used for adjustment procedures.

ALIGNMENT PROCEDURES

Only four adjustments are required by the whole decoder:

- the reference oscillator
- the 3.58MHz trap in the luminance channel
- the contour correction in the luminance channel
- the 3.58MHz bandpass in the chrominance channel.

The Reference Oscillator[1]

For adjusting the frequency of the reference oscillator, the color information on the screen can be used without using any extra measuring instruments:

1. Apply a color bar signal.
2. Connect Pin 6 (sat.) to the supply voltage; the oscillator is free-running and the killer is set at unkilling.
3. Adjust R9 for minimum rolling of the colors on the screen.
4. Remove connection of Pin 6 to supply voltage.

The 3.58MHz Trap in the Luminance Channel

1. Apply a color bar signal.
2. Observe one of the output signals (Pin 12, 14 or 16) and adjust L1 for minimum subcarrier information.

or

1. Apply a plain color picture, e.g., red.
2. Put the saturation control to minimum so that the screen becomes grey.
3. Put contrast to maximum.
4. Put brightness to normal position.
5. Adjust L1 for minimum 3.58MHz interference on the screen.

Contour Correction

1. Apply a 250kHz bar luminance signal, with rise and fall times of about 90ns.
2. Observe one of the output signals (Pin 12, 14 or 16) and adjust L2 for equal pre- and overshoots (see Figure 5).

The 3.58MHz Bandpass in the Chrominance Channel

1. Apply a color bar signal.
2. Observe one of the output signals (Pin 12, 14 or 16) and adjust L4 for optimum step response.

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NOTE:
1. For alternative adjustment procedure, see Appendix II.

Application of the NTSC Decoder: TDA3563

AN156

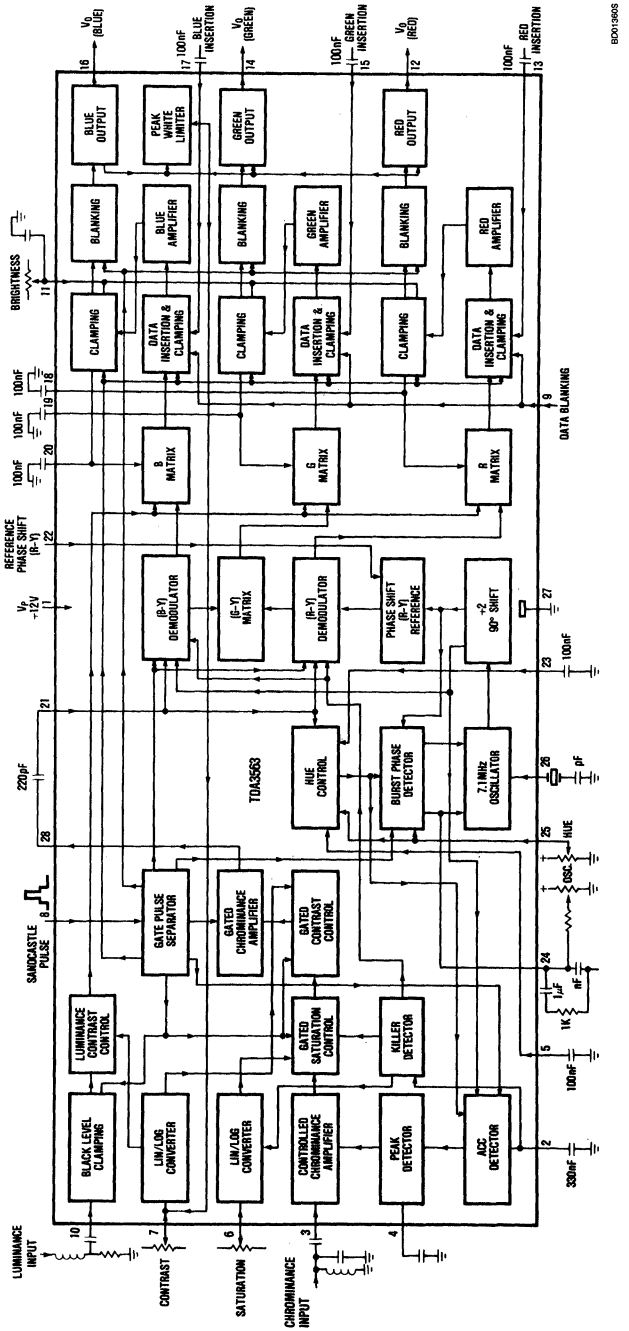

Figure 1. Block Diagram of the NTSC Decoder, TDA3563

Application of the NTSC Decoder: TDA3563 AN156

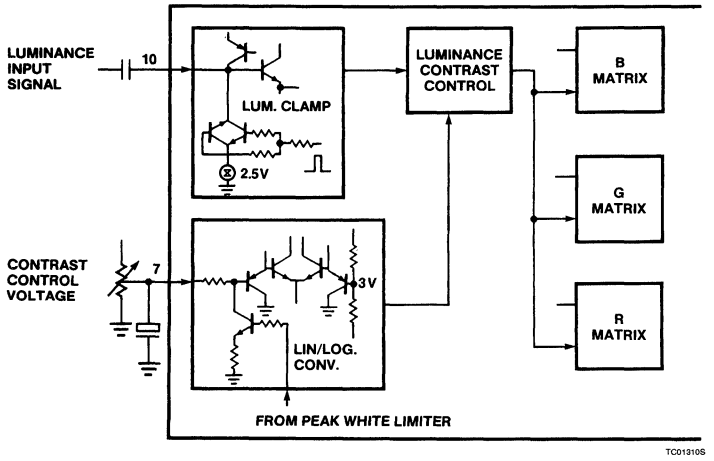

Figure 2. Luminance Channel

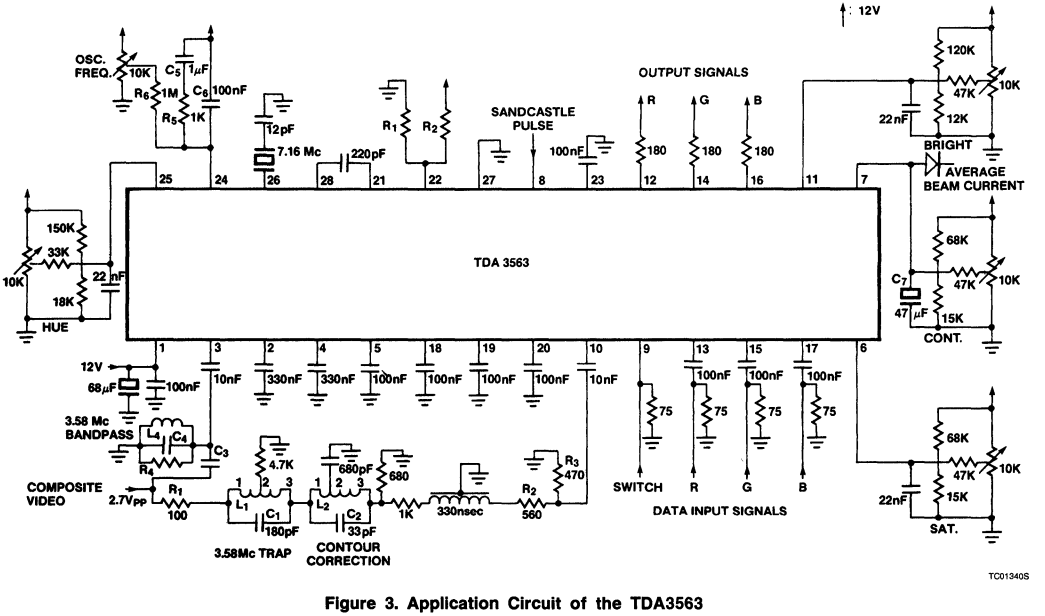

Figure 3. Application Circuit of the TDA3563

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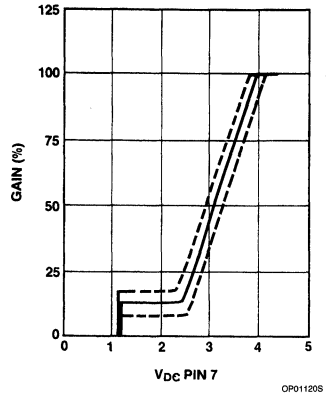
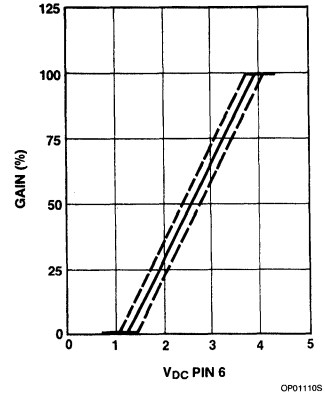
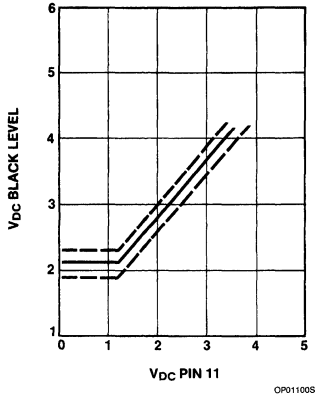


a. Control Characteristic of the Contrast Control

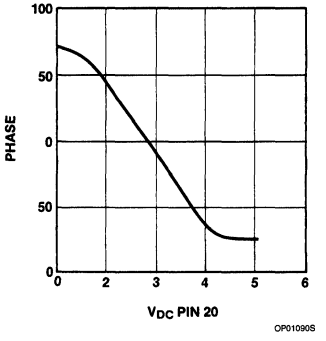


b. Control Characteristic of the Saturation Control

Figure 4



a. Control Characteristic of the Brightness Control



b. Control Characteristic of the Hue Control

Figure 5

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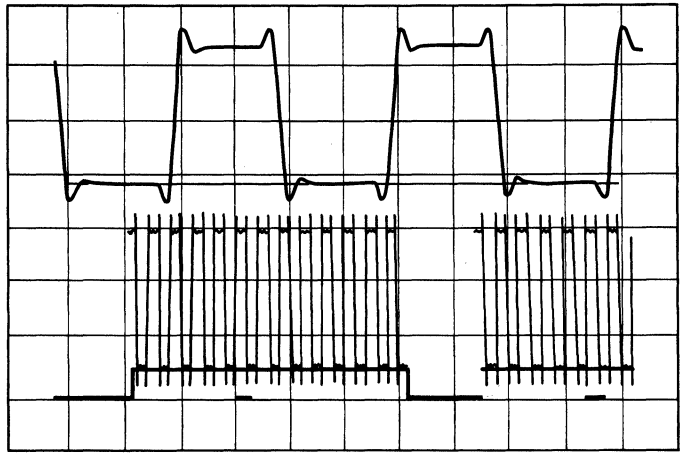
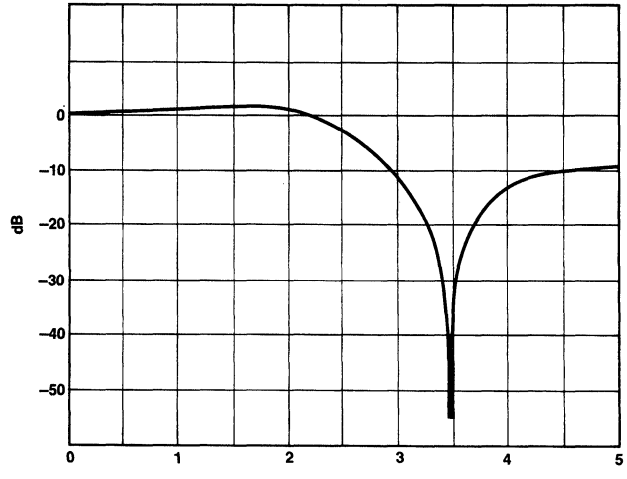


200kHz BAR SIGNAL

OP01080S

a



SWEEP SIGNAL 0 to 5MHz

OP01070S

b

Figure 6. Contour Correction

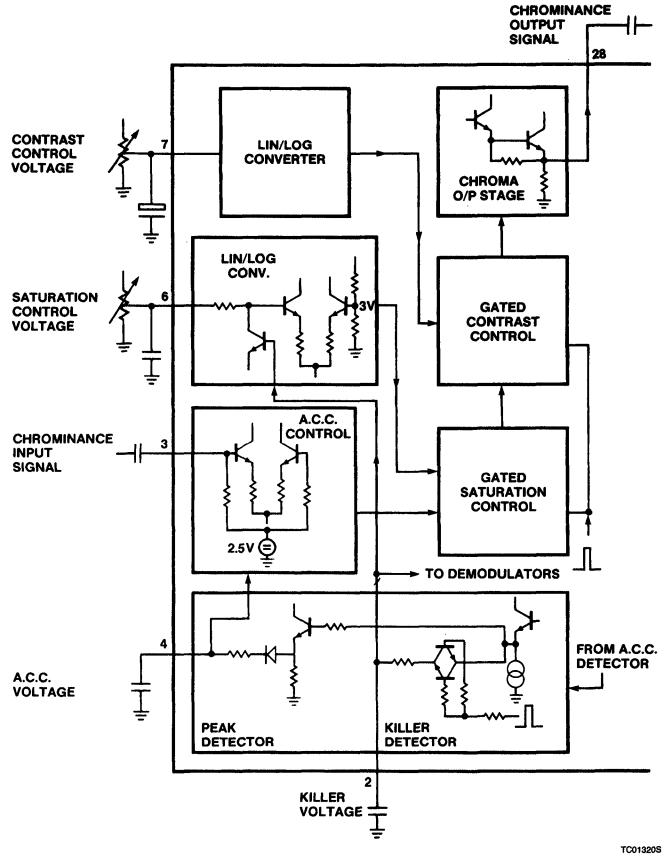


Figure 7. Chrominance Channel

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Application of the NTSC Decoder: TDA3563 AN156

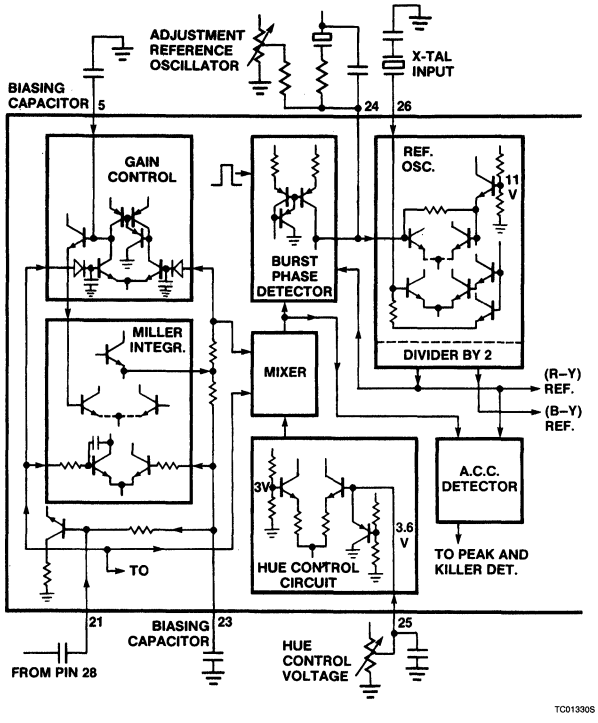


Figure 8. Chrominance Reference Circuits

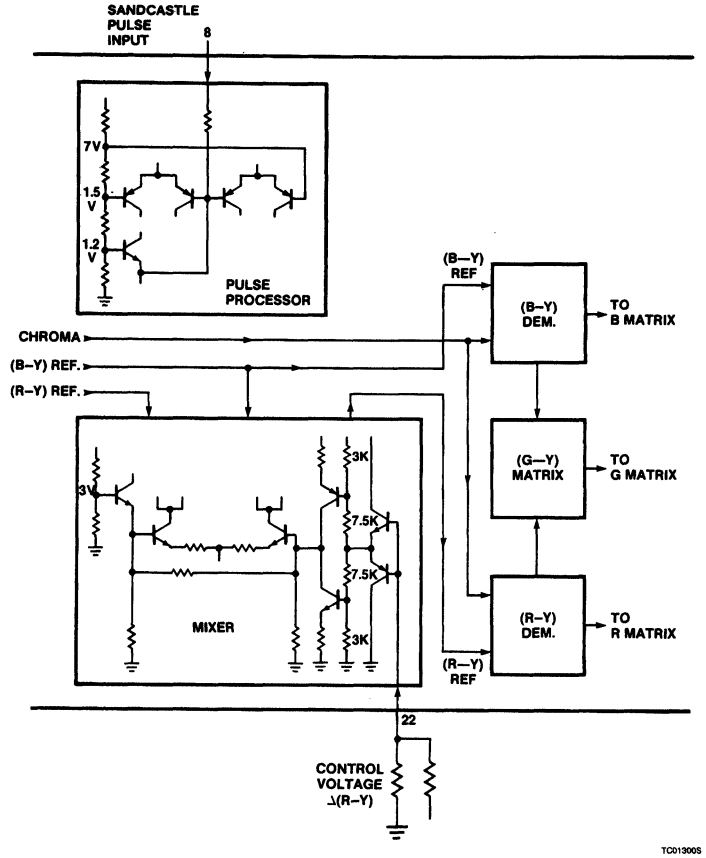


Figure 9. Chrominance Reference Circuits (Continued)

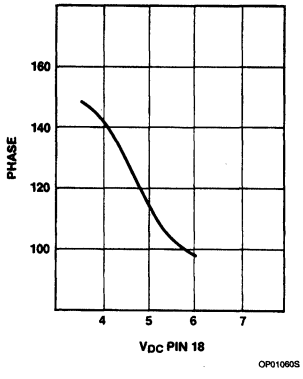


Figure 10. Control Characteristic of the Phase of the (R-Y) Reference Signal, (B-Y) Phase is Equal to Zero

Application of the NTSC Decoder: TDA3563 AN156

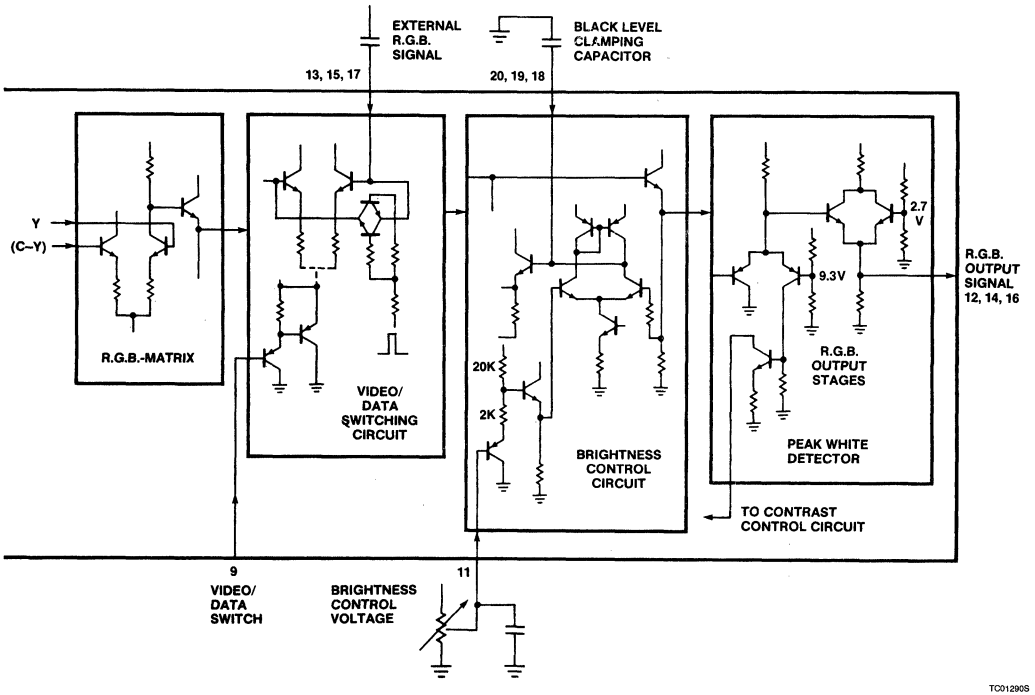
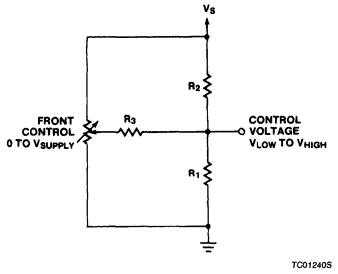


Figure 11. Video Control Circuits

Application of the NTSC Decoder: TDA3563 AN156

APPENDIX I

Conversion of a full-swing control voltage range (from zero up to V_{SUPPLY}) into a restricted control voltage range of V_{LOW} to V_{HIGH}:



The resistors R_1, R_2 and R_3, as a function of the source impedance R_s of the network, are defined by the following formula:

* first define a source impedance R_S

$$* \; R_1 = \frac{V_S}{V_S - V_H} \times R_S$$

$$* \; R_2 = \frac{V_S}{V_L} \times R_S$$

$$* \; R_3 = \frac{V_S}{V_H - V_L} \times R_S$$

APPENDIX II

Temporary Information, Concerning TDA3563 Versions Up to N6

Alternative Adjustment Procedure for the Reference Oscillator of the TDA3563

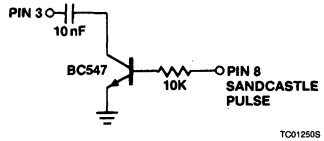
Using the normal frequency adjustment procedure for the reference oscillator of the TDA3563, i.e., setting the saturation control voltage (Pin 6) to 12V (unkilling and unlocking of the reference oscillator), and adjusting the trimmer capacitor for minimum rolling of color bars on the TV screen, the adjustment is disturbed by an internal defect of the burst phase detector.

If the reference frequency is adjusted in this way, it results into a frequency deviation of about 1kHz when removing the 12V connection at the saturation control input. So this frequency adjustment of the oscillator of the TDA3563, N6 cannot be used.

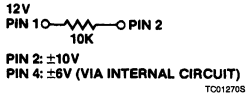
Therefore an alternative adjustment procedure is developed:
The X-tal has now a fixed capacitor of 12pF in series to ground, instead of the trimmer capacitor. The frequency adjustment is done via current injection into the burst phase detector (Pin 24).

The reference oscillator is made free-running by removing the burst information out of the chrominance signal.

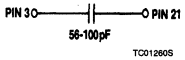
ADJUSTMENT PROCEDURE FOR THE REFERENCE OSCILLATOR OF THE TDA3565, N5



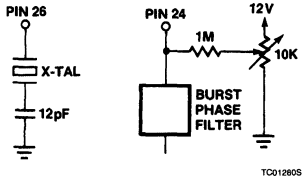
1. Connect an Electronic Switch to Pin 3. (Removing the burst information)



2. Connect a Resistor of 10kΩ Between Pin 2 and 12V Supply Line. (Color killer off and ACC control to minimum)



3. Connect a Capacitor of 56 to 100pF Between Pins 3 and 21. (Input signal at the demodulator input will be without any burst information)



4. Frequency Adjustment of the Oscillator. (Adjust the potentiometer for minimum rolling of color bars at the TV screen)

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Signetics

TDA3564
NTSC Decoder

Product Specification

Linear Products

DESCRIPTION

The TDA3564 is a monolithic integrated decoder for the NTSC color television standards. It combines all functions required for the demodulation of NTSC signals. Furthermore, it contains a luminance amplifier and an RGB matrix and amplifier. These amplifiers supply output signals up to $5V_{P-P}$ (picture information) enabling direct drive of the discrete output stages.

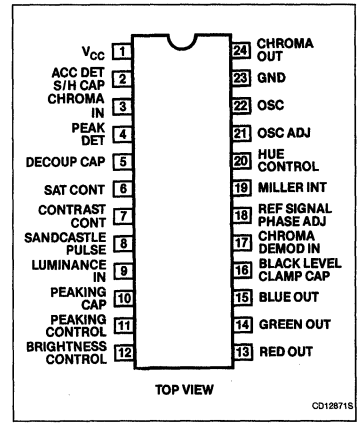
FEATURES

- **Single-chip chroma and luminance processor**
- **ACC with peak detector**
- **DC control settings**
- **High-level RGB outputs**
- **Luminance signal with clamp**
- **Black current stabilizer**
- **On-chip hue control**

APPLICATIONS

- **Video monitors and displays**
- **Television receivers**
- **Video processing**

PIN CONFIGURATION



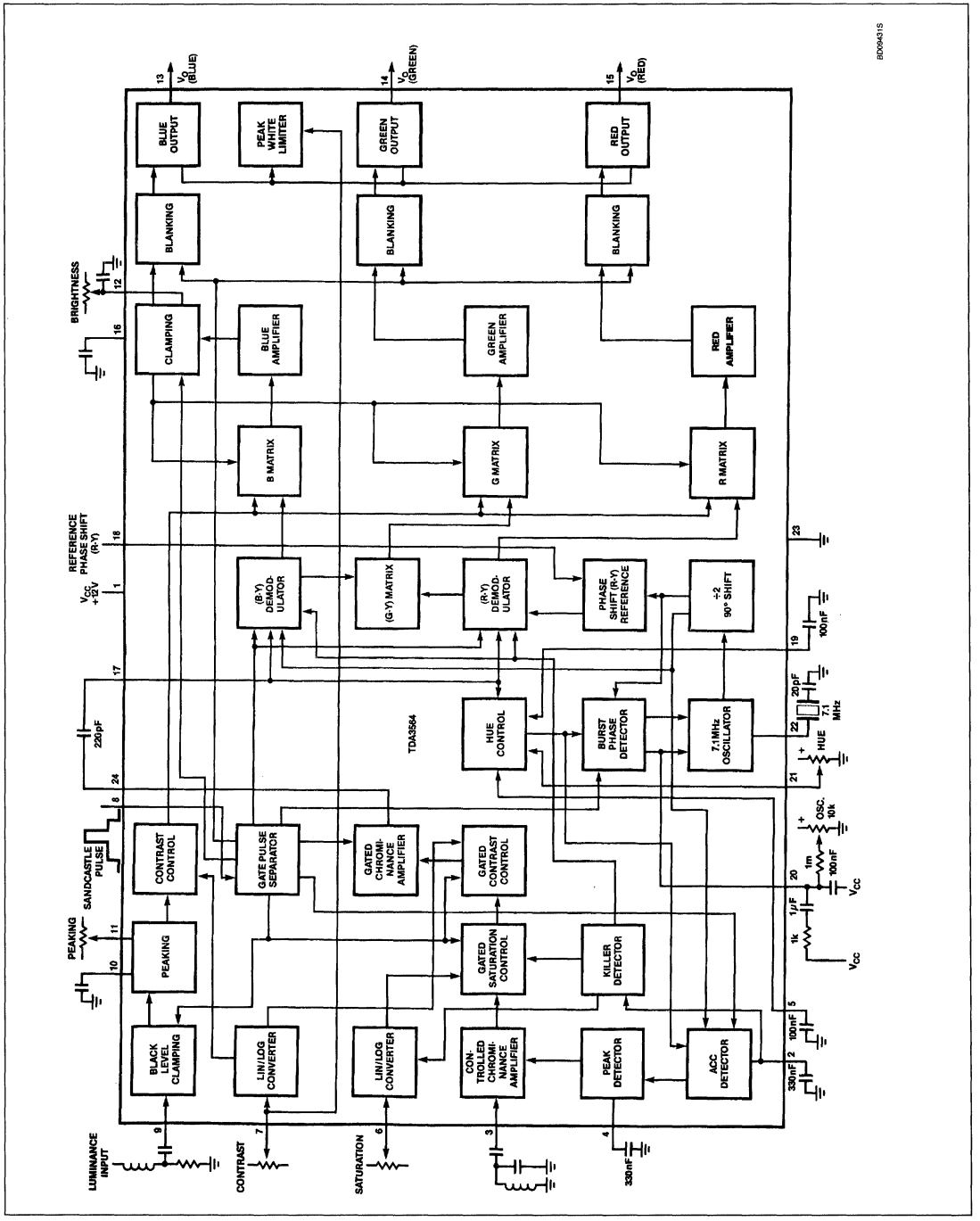
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−25°C to +65°C	TDA3564N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{1-23}$	Supply voltage (Pin 1)	13.2	V
P_{TOT}	Total power dissipation	1.7	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient (in free air)	50	°C/W

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{1-23} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 1)					
$V_{CC} = V_{1-23}$	Supply voltage	8	12	13.2	V
$I_{CC} = I_1$	Supply current		85		mA
P_{TOT}	Total power dissipation		1		W
Luminance amplifier (Pin 9)					
$V_{9-23(P-P)}$	Input voltage[1] (peak-to-peak value)		450		mV
V_{9-23}	Input level before clipping			2	V
I_9	Input current		0.15	1	μA
	Contrast control range (see Figure 1)	−17		+3	dB
	Control voltage for an attenuation of 40dB		1.2		V
I_7	Input current contrast control			15	μA
Peaking of luminance signal					
$\lvert Z_{10-23} \rvert$	Output impedance (Pin 10)		200		Ω
	Ratio of internal/external current when Pin 10 is short-circuited		3		
V_{11-23}	Control voltage for peaking adjustment (Pin 11)		2 − 4		V
$\lvert Z_{11-23} \rvert$	Input impedance (Pin 11)		10		kΩ
Chrominance amplifier (Pin 3)					
$V_{3-23(P-P)}$	Input voltage[2] (peak-to-peak value)	55	550	1100	mV
$\lvert Z_{3-23} \rvert$	Input impedance		8		kΩ
C_{3-23}	Input capacitance		4	6	pF
	ACC control range	30			dB
	Change of the burst signal at the output over the whole control range			1	dB
	Gain at nominal contrast/saturation Pin 3 to Pin 24[3]	13			dB
$V_{24-23(P-P)}$	Output voltage[3] (peak-to-peak value) at a burst signal of $300mV_{P-P}$		240		mV
$V_{24-23(P-P)}$	Maximum output voltage range (Pin 24) (peak-to-peak value)		1 − 7		V
d	Distortion of chrominance amplifier at $V_{24-23(P-P)} = 0.5V$ (output) up to $V_{3-23(P-P)} = 1V$ (input)		3	5	%
α_{24-3}	Frequency response between 0 and 5MHz			−2	dB
	Saturation control range (see Figure 2)	50			dB
I_6	Input current saturation control (Pin 6)			20	μA
	Tracking between luminance and chrominance contrast control			2	dB
	Cross-coupling between luminance and chrominance amplifier[4]			−46	dB
S/N	Signal-to-noise ratio at nominal input signal[5]	56			dB
$\Delta\phi$	Phase shift between burst and chrominance at nominal contrast/ saturation			±5	deg
$\lvert Z_{24-23} \rvert$	Output impedance of chrominance amplifier		25		Ω
I_{24}	Output current			10	mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-23} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reference part					
	Phase-locked loop				
Δf	Catching range[6]	500	700		Hz
$\Delta\phi$	Phase shift for ±400Hz deviation of f_{OSC}[6]			5	deg
	Oscillator				
TC_{OSC}	Temperature coefficient of oscillator frequency[6]		−1.5		Hz/°C
Δf_{OSC}	Frequency variation when supply voltage increases from 10 to 13.2V[6]		40		Hz
R_{22-23}	Input resistance (Pin 22)		300		Ω
C_{22-23}	Input capacitance (Pin 22)			10	pF
	ACC generation (Pin 2)				
V_{2-23}	Control voltage at nominal input signal		5.3		V
V_{2-23}	Control voltage without chrominance input		2.8		V
V_{2-23}	Color-off voltage		3.4		V
V_{2-23}	Color-on voltage		3.6		V
	Change in burst amplitude with supply voltage	independent			
V_{4-23}	Voltage at Pin 4 at nominal input signal		5.2		V
	Hue control				
	Control range	±50			deg
	Control voltage range	see Figure 4			V
Demodulator part					
$V_{17-23(P-P)}$	Input burst signal amplitude (Pin 17) (peak-to-peak value)		320		mV
$\lvert Z_{17-23} \rvert$	Input impedance (Pin 17)[7]		2		kΩ
$\frac{V_{15-23}}{V_{13-23}}$	Ratio of demodulated signals (B-Y)/(R-Y)		1.1		
$\frac{V_{14-23}}{V_{13-23}}$	(G-Y)/(R-Y); no (B-Y) signal		0.26		
$\frac{V_{14-23}}{V_{15-23}}$	(G-Y)/(B-Y); no (R-Y) signal		0.22		
	Frequency response between 0 and 1MHz			−3	dB
	Cross-talk between color difference signals	40			dB
ϕ	Control range reference signal (R-Y) demodulator (Pin 18)[8]	see Figure 5			deg
RGB matrix and amplifiers					
$V_{13, 14, 15-23(P-P)}$	Output voltage (peak-to-peak value) at nominal input signal (black-to-white)[3]		5		V
$V_{13-23(P-P)}$	Output voltage at Pin 13 (peak-to-peak value) at nominal contrast/ saturation and no luminance signal to (R-Y)		5.25		V
$V_{13, 14, 15-23}$	Maximum peak-white level[9]	9	9.3	9.6	V
$I_{13, 14, 15}$	Maximum output current (Pins 13, 14, 15)			10	mA
$V_{13, 14, 15-23}$	Output black level voltage for a brightness control voltage at Pin 12 of 2V		2.7		V
	Black level shift with vision contents			40	mV
	Brightness control voltage range	see Figure 3			V

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-23} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_{12}	Brightness control input current			5	μA
$\Delta V/\Delta T$ ΔV	Variation of black level with temperature with contrast		0.35 10	1 100	mV/°C mV
	Relative spread between the R, G, and B output signals			10	%
	Relative black level variation between the three channels during variation of contrast, brightness, and supply voltage		0	20	mV
	Differential black level drift over a temperature range of 40°C		0	20	mV
	Blanking level at the RGB outputs	1.9	2.1	2.3	V
	Difference in blanking level of the three channels		0		mV
	Differential drift of the blanking levels over a temperature range of 40°C		0		mA
$\frac{\Delta V_{B1}}{V_{B1}} \times \frac{V_{CC}}{\Delta V_{CC}}$	Tracking of output black level with supply voltage		1.1		
S/N	Signal-to-noise ratio of output signals[5]	62			dB
	Residual 7.1MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		75	150	mV
$\lvert Z_{13,\ 14,\ 15-23} \rvert$	Output impedance of RGB outputs		50		Ω
	Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5MHz			−3	dB
Sandcastle input (Pin 8)					
V_{8-23}	Level at which the RGB blanking is activated	1	1.5	2	V
V_{8-23}	Level at which burst gating and clamping pulse are separated	6.5	7	7.5	V
t_D	Delay between black level clamping and burst gating pulse		0.4		μs
$-I_8$ I_8 I_8	Input current at V_{8-23} = 0 to 1V at V_{8-23} = 1 to 8.5V at V_{8-23} = 8.5 to 12V		 20	1 2	mA μA mA

NOTES:
1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a color bar with 75% saturation; chrominance-to-burst ratio is 2.2:1.
3. Nominal contrast is specified as the maximum contrast −3dB and nominal saturation as the maximum saturation −6dB.
4. Cross coupling is measured under the following conditions:
   - Input signals nominal
   - Contrast and saturation such that nominal output signals are obtained
   - The signals at the output at which no signal should be available must be compared to the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to RMS noise.
6. All frequency variations are referred to 3.58MHz carrier frequency.
7. These signal amplitudes are determined by the ACC circuit of the reference part.
8. When Pin 18 is open circuit, the phase shift between the (R-Y) and (B-Y) reference carrier is 115°. This phase shift can be varied by changing the voltage applied to Pin 18.
9. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at Pin 7 (contrast control); discharge current is 1.5mA.

FUNCTIONAL DESCRIPTION

Luminance Amplifier

The luminance amplifier is voltage driven and requires an input signal of $450mV_{P-P}$ (positive video). The luminance delay line must be connected between the IF amplifier and the decoder. The input signal is AC-coupled to the input (Pin 9).

The black level at the output of the preamplifier is clamped to a fixed DC level by the black level clamping circuit. The high input impedance of the luminance amplifier minimizes disturbance of the input signal black level by the source impedance (delay line matching resistors).

During clamping, the low-input impedance reduces noise and residual signals. After clamping, the signal is fed to a peaking stage. The overshoot is defined by the capacitor connected to Pin 10 and the peaking is adjusted by the control voltage at Pin 11.

The peaking stage is followed by a contrast control stage. The contrast control voltage range (Pin 7) is nominally −17 to +3dB. The linear relationship between the contrast-control voltage and the gain is shown in Figure 1.

Chrominance Amplifier

The chrominance amplifier has an asymmetrical input. The input signal must be AC-coupled (Pin 3) and have a minimum amplitude of $55mV_{P-P}$. The gain control stage has a control range in excess of 30dB, the maximum input signal must not exceed $1.1V_{P-P}$, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance contrast control stages are directly coupled to obtain good tracking. Saturation is linearly controlled via Pin 6 (see Figure 2). The control voltage range is 2V to 4V, the input impedance is High, and the saturation control range is in excess of 50dB. The burst signal is not affected by saturation control. The output signal at Pin 24 is AC coupled to the demodulators via Pin 17.

Oscillator and ACC Detector

The 7.16MHz reference oscillator operates at twice the subcarrier frequency. The reference signals for the (R-Y) and (B-Y) demodulators, burst-phase detector, and ACC detector are obtained via the divide-by-2 circuit, which provides a 90° phase shift. The oscillator is controlled by the burst phase detector, which is gated with the narrow part of the sandcastle pulse (Pin 8). As the burst phase detector has an asymmetrical output, the oscillator can be adjusted by changing the voltage of the output (Pin 21) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When Pin 6 (saturation control) is connected to the positive supply line, the burst signal is suppressed and the color killer is overruled. This position can therefore be used for adjustment of the oscillator. The adjustment is visible on the screen.

The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the chrominance signal applied to the demodulators. This phase shift is obtained by generating a 90° shifted sine wave via a Miller integrator (biased via Pin 19) which is mixed with the original burst signal. A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. The control circuit is decoupled by a capacitor connected to Pin 5.

As the shifted burst signal is synchronously demodulated in a separate ACC detector to generate the ACC voltage, it is not affected by the hue control. The output pulses of this detector are peak detected (Pin 4) to control the gain of the chrominance amplifier, thus preventing blooming-up of the color during weak signal reception. This ensures reliable operation of the color killer. During color killing, the color channel is blocked by switching off saturation control and the demodulators.

Demodulators

The (R-Y) and (B-Y) demodulators are driven by the chrominance signal (Pin 24) and the reference signals from the 7.16MHz divider circuit. The phase angle between the two reference carriers is 115°. This is achieved by the (R-Y) demodulator receiving an additional phase shift by mixing the two signals from the divider circuit. The phase shift of 115° can be varied between 90° and 140° by changing the bias voltage at Pin 18. The demodulator output signals are fed to R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G matrix. The demodulator circuits are killed and blanked by bypassing the input signals.

RGB Matrix and Amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described. The luminance and the color difference signals are added in the matrix circuit to obtain the color signal. Output signals are $5V_{P-P}$ (black-white) for the following nominal input signals and control settings.

- Luminance $450mV_{P-P}$
- Chrominance $550mV_{P-P}$ (burst-to-chrominance ratio of the input 1:2, 2)
- Contrast −3dB maximum
- Saturation −6dB maximum

The maximum output voltage is approximately $7V_{P-P}$.

The black level of the blue channel is compared to a variable external reference level (Pin 12) which provides brightness control. The brightness control range is 1V to 3.2V (see Figure 3). The control voltage is stored in a capacitor (connected to Pin 16) and controls the black level at the output (Pin 15) between 2V and 4V, via a change of the level of the luminance signal before matrixing.

NOTE:
Black levels of up to approximately 6V are possible, but amplitude of the output signal is reduced to $3V_{P-P}$.

If the output signal surpasses the level of 9V, the peak white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB Signals

The RGB signals can be blanked via the sandcastle input (Pin 8). A slicing level of 1.5V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking, a level of +2V is available at the output.

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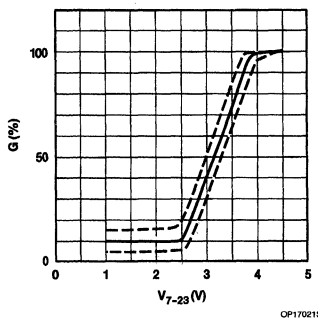


Figure 1. Contrast Control Voltage Range

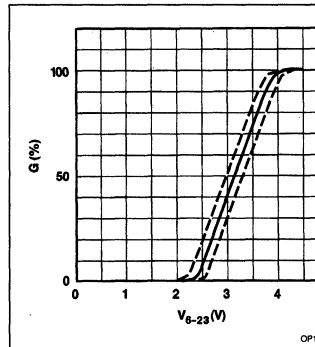


Figure 2. Saturation Control Voltage Range

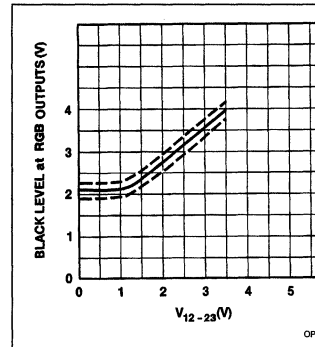


Figure 3. Brightness Control Voltage Range

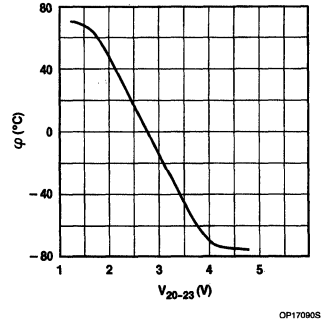


Figure 4. Hue Control Voltage Range

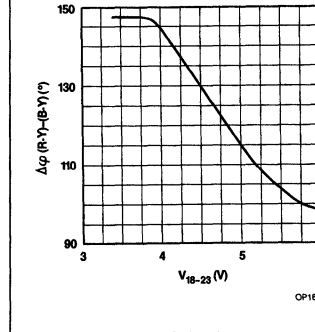
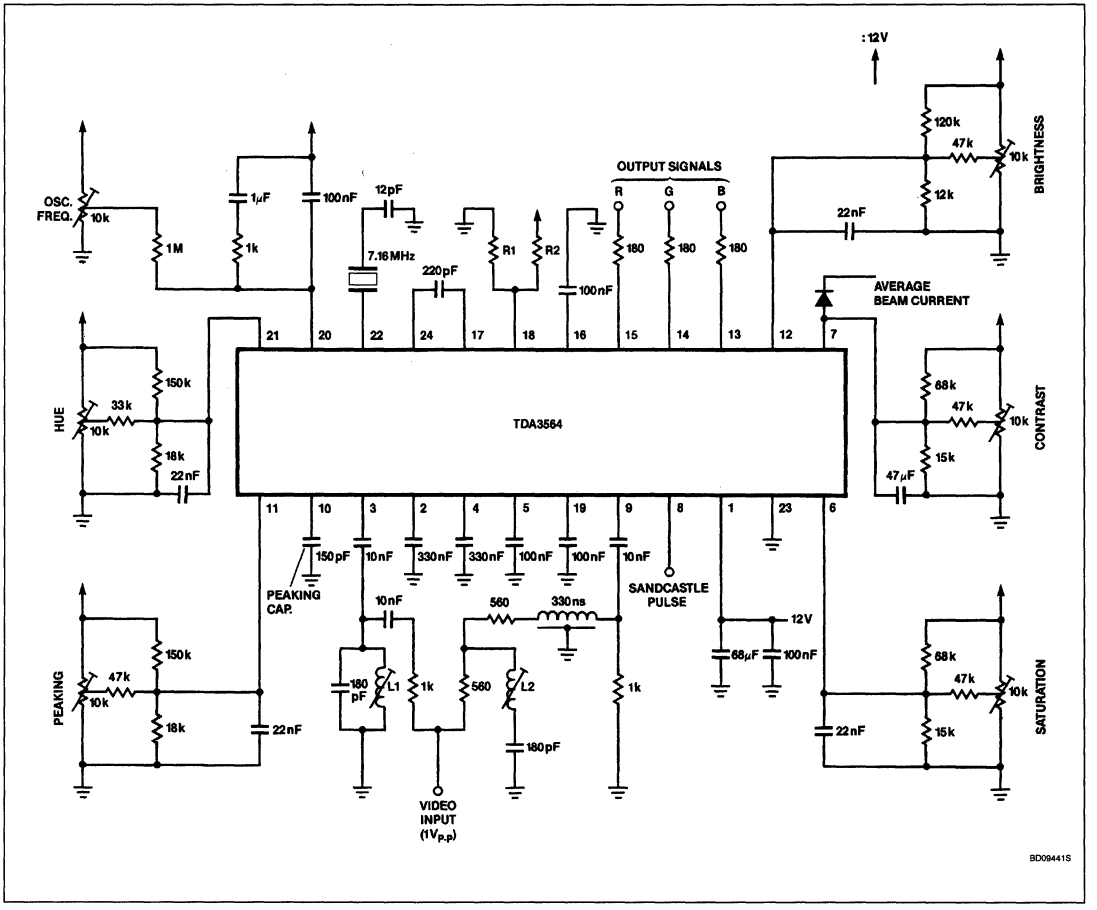
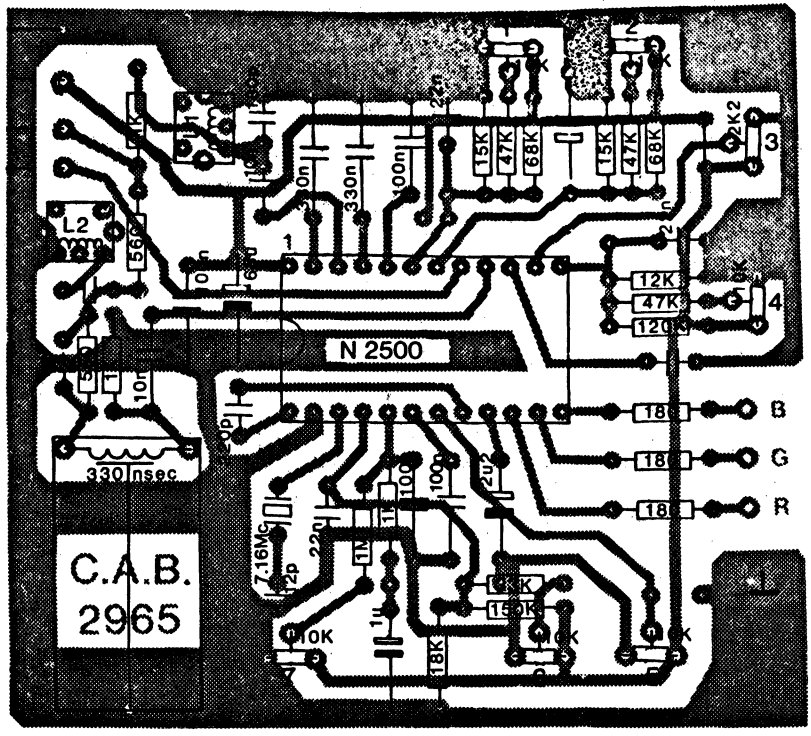


Figure 5. Phase Shift Between (R-Y) and (B-Y) as a Function of V_{18-23}

APPLICATION CIRCUIT FOR TDA3564 NTSC COLOR DECODER



NTSC DECODER N 2500



NOTES:
L1 = L2 μH TOKO 7P mat.

Controls:
1. Saturation
2. Contrast
3. Peaking
4. Brightness
5. ΔQ (R-Y)
6. Hue
7. Osc. freq.

Signetics

TDA3566
PAL/NTSC Decoder With RGB Inputs

Product Specification

Linear Products

DESCRIPTION

The TDA3566 is a monolithic, integrated decoder for the PAL® and/or NTSC color television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore, it contains a luminance amplifier, and an RGB matrix and amplifier. These amplifiers supply output signals up to $4V_{P-P}$ (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analog as well as digital, which can be used for text display systems (e.g., Teletext/broadcast antiope), channel number display, etc.

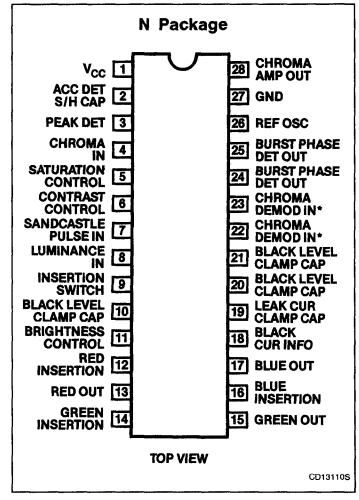
FEATURES

- **A black current stabilizer which controls the black currents of the three electron guns to a level low enough to omit the black level adjustment**
- **Contrast control of inserted RGB signals**
- **No black level disturbance when nonsynchronized external RGB signals are available on the inputs**
- **NTSC capability with hue control**
- **Single-chip chroma and luminance processor**
- **ACC with peak detector**
- **DC control settings**
- **External linear or digital RGB inputs**
- **High-level RGB outputs**
- **Luminance signal with clamp**
- **On-chip hue control for NTSC**

APPLICATIONS

- **Video monitors and displays**
- **Text display systems**
- **TV receivers**
- **Graphic systems**
- **Video processing**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +70°C	TDA3566N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{1-27}$	Supply voltage (Pin 1)	13.2	V
P_{TOT}	Total power dissipation	1.7	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C
θ_{JA}	Thermal resistance from junction to ambient (in free air)	40	°C/W

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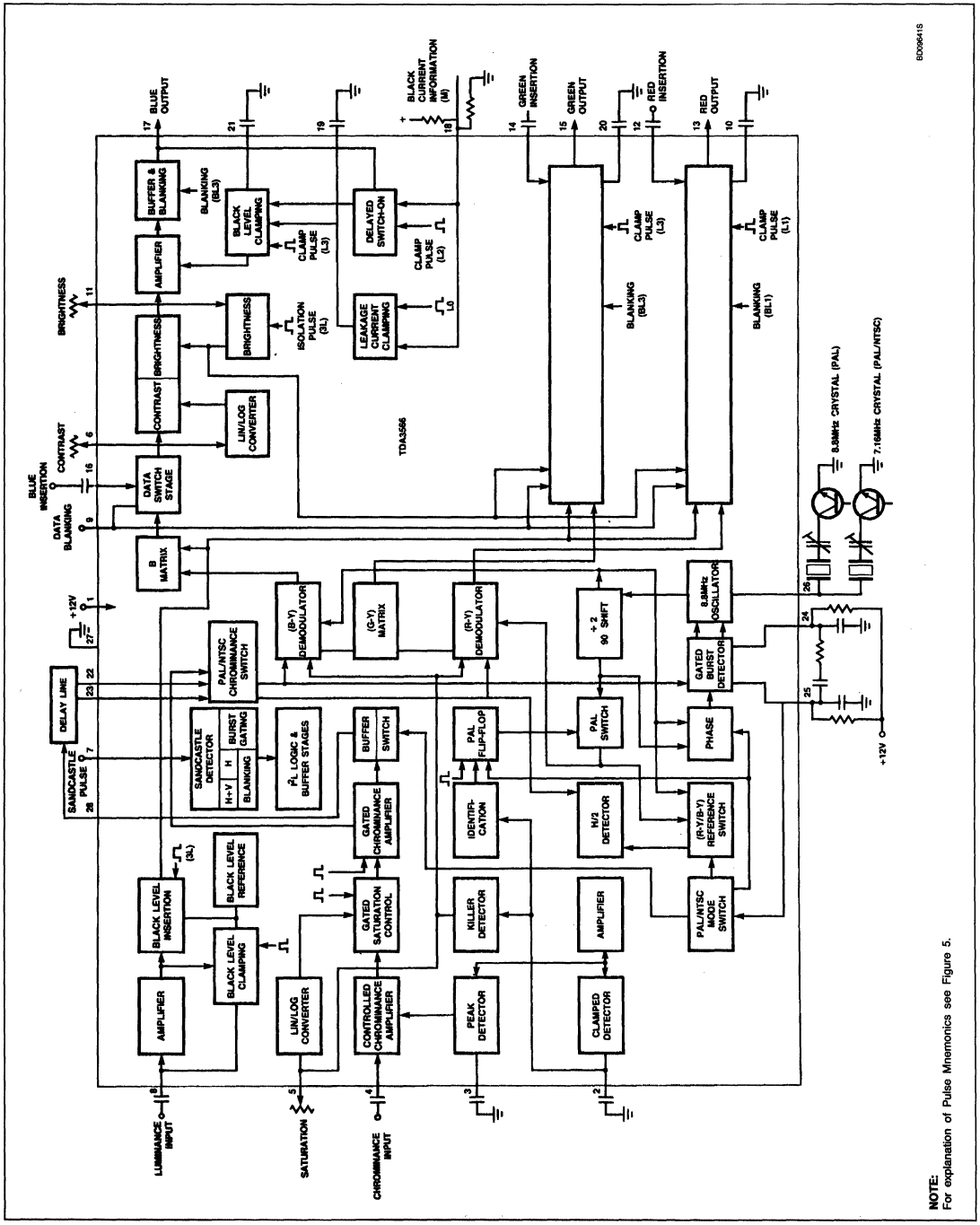
BLOCK DIAGRAM



NOTE:
For explanation of Pulse Mnemonics see Figure 5.

DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 1)					
$V_{CC} = V_{1-27}$	Supply voltage	10.8	12	13.2	V
$I_{CC} = I_1$	Supply current		80	110	mA
P_{TOT}	Total power dissipation		0.95	1.3	W
Luminance amplifier (Pin 8)					
$V_{8-27(P-P)}$	Input voltage[1] (peak-to-peak value)		0.45	0.63	V
V_{8-27}	Input level before clipping			1	V
I_8	Input current		0.1	1	μA
	Contrast control range (see Figure 1)	−15		+5	dB
I_7	Input current contrast control			15	μA
Chrominance amplifier (Pin 4)					
$V_{4-27(P-P)}$	Input voltage[2] (peak-to-peak value)	40	390	1100	mV
$\lvert Z_{4-27} \rvert$	Input impedance (Pin 4)		10		kΩ
C_{4-27}	Input capacitance			6.5	pF
	ACC control range	30			dB
ΔV	Change of the burst signal at the output over the whole control range			1	dB
A_V	Gain at nominal contrast/saturation Pin 4 to Pin 28[3]	34			dB
	Chrominance to burst ratio at nominal saturation at Pin 28[2, 3]		12		dB
$V_{28-27(P-P)}$	Maximum output voltage range (peak-to-peak value); $R_L = 2k\Omega$	4	5		V
d	Distortion of chrominance amplifier at $V_{28-27(P-P)} = 2V$ (output) up to $V_{4-27(P-P)} = 1V$ (input)			5	%
α_{28-4}	Frequency response between 0 and 5MHz			−2	dB
	Saturation control range (see Figure 2)	50			dB
I_5	Input current saturation control (Pin 5)			20	μA
	Cross-coupling between luminance and chrominance amplifier[4]			−46	dB
S/N	Signal-to-noise ratio at nominal input signal[5]	56			dB
$\Delta\varphi$	Phase shift between burst and chrominance at nominal contrast/ saturation			±5	deg
$\lvert Z_{28-27} \rvert$	Output impedance of chrominance amplifier		10		Ω
I_{28}	Output current			15	mA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reference part					
	Phase-locked loop				
Δf	catching range[6]	500	700		Hz
$\Delta\varphi$	phase shift for ±400Hz deviation of f_{OSC}[6]			5	deg
	Oscillator				
TC_{OSC}	temperature coefficient of oscillator frequency[6]		−2	−3	Hz/°C
Δf_{OSC}	frequency variation when supply voltage increases from 10 to 13.2V[6]		40	100	Hz
R_{26-27}	input resistance (Pin 26)	280	400	520	Ω
C_{26-27}	input capacitance (Pin 26)			10	pF
	ACC generation (Pin 2)				
V_{2-27}	control voltage at nominal input signal		4.6		V
V_{2-27}	control voltage without chrominance input		2.6		V
V_{2-27}	color-off voltage		3.4		V
V_{2-27}	color-on voltage		3.6		V
V_{2-27}	identification-on voltage		2.0		V
	change in burst amplitude with temperature		0.1	0.25	%/°C
V_{3-27}	voltage at Pin 3 at nominal input signal		5.1		V
Demodulator part					
$V_{23-27(P-P)}$	Input burst signal amplitude[7] (peak-to-peak value) between Pins 23 and 27	68	80	95	mV
$\lvert Z_{22-27/23-27} \rvert$	Input impedance between Pins 22 or 23 and 27	0.7	1	1.3	kΩ
	Ratio of demodulated signals[8]				
$\frac{V_{17-27}}{V_{13-27}}$	(B-Y)/(R-Y)		1.78± 10%		
$\frac{V_{15-27}}{V_{13-27}}$	(G-Y)/(R-Y); no (B-Y) signal		−0.51± 10%		
$\frac{V_{15-27}}{V_{17-27}}$	(G-Y)/(B-Y); no (R-Y) signal		−0.19± 10%		
α_{17}	Frequency response between 0 and 1MHz			−3	dB
	Cross-talk between color difference signals	40			dB
$\Delta\varphi$	Phase difference between (R-Y) signal and (R-Y) reference signals			5	deg
$\Delta\varphi$	Phase difference between (R-Y) signal and (B-Y) reference signals	85	90	95	deg

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
RGB matrix and amplifiers					
$V_{13, 15, 17-27(P-P)}$	Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white)[9]	3.5	4	4.5	V
$V_{13-27(P-P)}$	Output voltage at Pin 13 (peak-to-peak value) at nominal contrast/ saturation and no luminance signal to (R-Y)		4.2		V
$V_{13, 15, 17(m)}$	Maximum peak-white level	9.7	10	10.3	V
$I_{13, 15, 17}$	Available output current (Pins 13, 15, 17)	10			mA
$\Delta V_{13, 15, 17-27}$	Difference between black level and measuring level at the output for a brightness control voltage at Pin 11 of 2V[9]		0		V
ΔV	Difference in black level between the three channels without black current stabilization[10]			100	mV
	Control range of black-current stabilization $V_{CC1} = 3V$; $V_{11-17} = 2V$			±2	V
ΔV	Black level shift with vision contents			40	mV
	Brightness control voltage range	see Figure 2			
I_{11}	Brightness control input current			5	μA
$\Delta V/\Delta T$	Variation of black level with temperature		0		mV/°C
ΔV	Variation of black level with contrast*			100	mV
	Relative spread between the R, G, and B output signals			10	%
ΔV	Relative black-level variation between the three channels during variation of contrast, brightness, and supply voltage (±10%)*		0	20	mV
ΔV	Differential black-level drift over a temperature range of 40°C		0	20	mV
V_{BL}	Blanking level at the RGB outputs		0.95	1.1	V
V_{BL}	Difference in blanking level of the three channels		0		mV
V_{BL}	Differential drift of the blanking levels over a temperature range of 40°C		0	10	mV
$\frac{\Delta V_{BL}}{V_{BL}} \times \frac{V_{CC}}{\Delta V_{CC}}$	Tracking of output black level with supply voltage	0.9	1	1.1	
	Tracking of contrast control between the three channels over a control range at 10dB			0.5	dB
V_O	Output signal during the clamp pulse (3L) after switch-on	7.5			V
S/N	Signal-to-noise ratio of output signals[5]	62			dB
$V_{R(P-P)}$	Residual 4.4MHz signal at RGB outputs (peak-to-peak value)			50	mV
$V_{R(P-P)}$	Residual 8.8MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)			150	mV
$\lvert Z_{13, 15, 17-27} \rvert$	Output impedance of RGB outputs		50		Ω
α	Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5MHz		−1	−3	dB
I_O	Current source of output stage	2	3		mA
ΔV	Difference of black level at the three outputs at nominal brightness*			10	mV
	Tracking of brightness control			2	%

NOTE:
*With respect to the measuring pulses.

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Signal insertion (Pins 12, 14, and 16)					
$V_{12, 14, 16-27(P-P)}$	Input signals (peak-to-peak value) for RGB output voltage of 4V (peak-to-peak) at nominal contrast	0.9	1	1.1	V
ΔV	Difference between the black levels of the RGB signals and the inserted signals at the output[11]			100	mV
t_R	Output rise time		50	80	ns
t_D	Differential delay time for the three channels		0	40	ns
$I_{12, 14, 16}$	Input current			10	μA
Data blanking (Pin 9)					
V_{9-27}	Input voltage for no data insertion			0.4	V
V_{9-27}	Input voltage for data insertion	0.9			V
$V_{9-27(m)}$	Maximum input voltage			3	V
t_D	Delay of data blanking			20	ns
R_{9-27}	Input resistance	7	10	13	kΩ
	Suppression of the internal RGB signals when $V_{9-27} > 0.9V$	46			dB
Sandcastle input (Pin 7)					
V_{7-27}	Level at which the RGB blanking is activated	1	1.5	2	V
V_{7-27}	Level at which the horizontal pulses are separated	3	3.5	4	V
V_{7-27}	Level at which burst gating and clamping pulse are separated	6.5	7.0	7.5	V
t_D	Delay between black level clamping and burst gating pulse		0.6		μs
$-I_7$ I_7 I_7	Input current at $V_{7-27} = 0$ to 1V at $V_{7-27} = 1$ to 8.5V at $V_{7-27} = 8.5$ to 12V			1 50 2	mA μA mA
Black current stabilization (Pin 18)					
V_{18-27}	Bias voltage (DC)	3.5	5	7.0	V
ΔV	Difference between input voltage for 'black' current and leakage current	0.35	0.5	0.65	V
I_{18}	Input current during 'black' current			1	μA
I_{18}	Input current during scan			10	mA
V_{18-27}	Internal limiting at Pin 10	8.5	9	9.5	V
V_{18-27}	Switching threshold for 'black' current control ON	7.6	8	8.4	V
R_{18-27}	Input resistance during scan	1	1.5	2	kΩ
$I_{10, 20, 21}$	Input current during scan at Pins 10, 20, and 21 (DC)			TBD	nA
	Maximum charge/discharge current during measuring time		1		nA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-27} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
NTSC					
V_{24-25}	Level at which the PAL/NTSC switch is activated (Pins 24 and 25)		8.8	9.2	V
$I_{24+25(AV)}$	Average output current[12]	75	90	105	μA
	Hue control	see Figure 4			

NOTES:

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a color bar with 75% saturation; chrominance to burst ratio is 2.2:1.
3. Nominal contrast is specified as the maximum contrast — 5dB and nominal saturation as the maximum saturation — 6dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to RMS noise.
6. All frequency variations are referred to 4.4MHz carrier frequency.
7. These signal amplitudes are determined by the ACC circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5V), but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discoloration during adjustment of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150Ω and the black level clamp pulse width is 4μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at Pins 24 and 25 can be changed by connecting the load resistors (10kΩ in this application) to the slider bar of the hue control potentiometer (see Figure 7). When the transistor is switched on, the voltage at Pins 24 and 25 is reduced below 9V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4μs typical.

FUNCTIONAL DESCRIPTION

The TDA3566 is a further development of the TDA3562A. It has the same pinning and almost the same application. The differences between the TDA3562A and the TDA3566 are as follows:

- The NTSC application has largely been simplified. In the case of NTSC, the chroma signal is now internally coupled to the demodulators, ACC, and phase detectors. The chroma output signal (Pin 28) is suppressed in this case. It follows that the external switches and filters which are needed for the TDA3562A are not needed for the TDA3566. Furthermore, there is no difference between the amplitude of the color output signals in the PAL or NTSC mode. The PAL/NTSC switch and the hue control of the TDA3566 and the TDA3562A are identical.
- The switch-on and the switch-off behavior of the TDA3566 has been improved. This has been obtained by suppressing the output signals during the switch-on and switch-off periods.
- The clamp capacitors connected to the Pins 10, 20, and 21 can be reduced to 100nF for the TDA3566. The clamp capacitors also receive a pre-bias voltage to avoid colored background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. This has the consequence that optimal tuning capacitance must be reduced to 10pF.

Luminance Amplifier

The luminance amplifier is voltage driven and requires an input signal of 450mV peak-to-peak (positive video). The luminance delay line must be connected between the IF amplifier and the decoder. The input signal is AC coupled to the input (Pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed DC level by the black clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via Pin 11 (brightness). At the same time, the RGB signals are clamped. Noise and residual signals have no influence during clamping; thus, simple internal clamping circuitry is used.

Chrominance Amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be AC coupled (Pin 4) and have a minimum amplitude of $40mV_{p-p}$. The gain control stage has a control range in excess of 30dB; the maximum input signal must not exceed $1.1V_{p-p}$ or clipping of the input signal will occur. From the gain-control stage, the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via Pin 5. The control voltage range is 2 to 4V, the input impedance is high, and the saturation control range is in excess of 50dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12dB higher gain during the chrominance signal. As a result, the signal at the output (Pin 28) has a burst-to-chrominance ratio which is 6dB lower than that of the input signal when the saturation control is set at −6dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (Pins 22 and 23). These signals are fed to the burst phase detector. In the case of NTSC, the chroma signal is internally coupled to the demodulators, ACC, and phase detector.

Oscillator and Identification Circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (Pin 7). In the detector, the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared to the oscillator signal divided-by-2 ((R-Y) reference signal). The control voltage is available at Pins 24 and 25, and is also applied to the 8.8MHz oscillator. The 4.4MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the ACC. To avoid 'blooming-up' of the picture under weak input signal conditions, the ACC voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (Pin 5) provides a delayed switch-on after killing.

Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between Pins 24 and 25 (see Figure 6). With this application, the trimmer capacitor in series with the 8.8MHz crystal (Pin 26) can be replaced by a fixed value capacitor to compensate for imbalance of the phase detector.

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the color difference signals from the delay-line matrix circuit and the reference signals from the 8.8MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G matrix. The demodulation circuits are killed and blanked by bypassing the input signals.

NTSC Mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (Pins 24 and 25) is adjusted below 9V. To ensure reliable application, the phase detector load resistors are external. When the TDA3566 is used only for PAL, these two 33kΩ resistors must be connected to +12V (see Figure 6). For PAL/NTSC application, the value of each resistor must be reduced to 10kΩ and connected to the slider of a potentiometer (see Figure 7). The switching transistor brings the voltage at Pins 24 and 25 below 9V, which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. (In the PAL mode it is driven by the (R-Y) reference signal.)

Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at Pins 24 and 25 between 7.5V and 8.5V, nominal position 8.0V. The hue control characteristic is shown in Figure 4.

RGB Matrix and Amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described. The luminance and the color difference signals are added in the matrix circuit to obtain the color signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to Pin 6 (high-input impedance). The control range is +3dB to −17dB nominal. The relationship between the control voltage and the gain is linear (see Figure 1).

During the 3-line period after blanking, a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at Pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1V to 3V.

While this offset level is present, the 'black-current' input impedance (Pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at Pin 19 with the voltage developed across the external resistor network R_A and R_B (Pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from Pins 10, 20, and 21 to ground, which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to Pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10V. When the signal tends to exceed this level, the output signal is clipped. The black level at the outputs (Pins 13, 15, and 17) will be about 3V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used, it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (Pin 18) via a resistor network.

Data Insertion

Each color amplifier has a separate input for data insertion. A $1V_{P-P}$ input signal provides a $4V_{P-P}$ output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore, AC coupling is required for the data inputs.

To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150Ω.

The data insertion circuit is activated by the data blanking input (Pin 9). When the voltage at this pin exceeds a level of 0.9V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid colored edges, the data blanking switching time is short.

The amplitude of the data output signals is controlled by the contrast control at Pin 6. The black level is equal to the video black level and can be varied between 2 and 4V (nominal condition) by the brightness control voltage at Pin 11. Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and Data Signals

Both the RGB and data signals can be blanked via the sandcastle input (Pin 7). A slicing level of 1.5V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking, a level of +1V is available at the output. To prevent parasitic oscillations on the third overtone of the crystal, the optimal tuning capacitance should be 10pF.

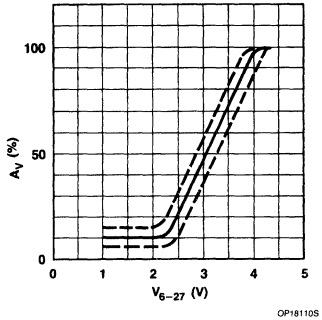


Figure 1. Contrast Control Voltage Range

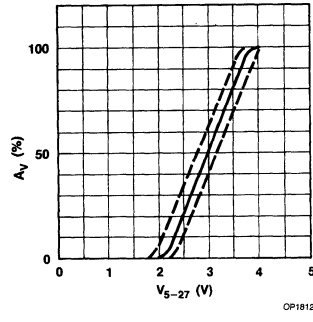


Figure 2. Saturation Control Voltage Range

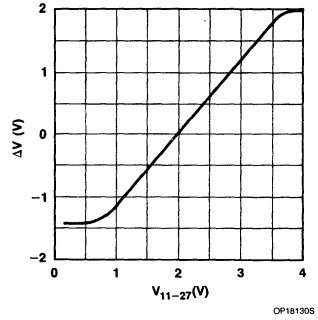


Figure 3. Difference Between Black Level and Measuring Level at the RGB Outputs (ΔV) as a Function of the Brightness Control Input Voltage (V_{11-27})

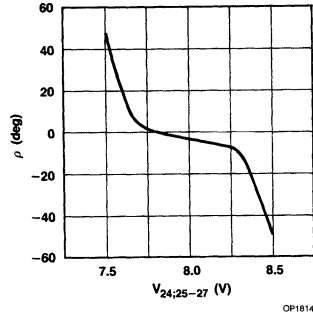


Figure 4. Hue Control Voltage Range

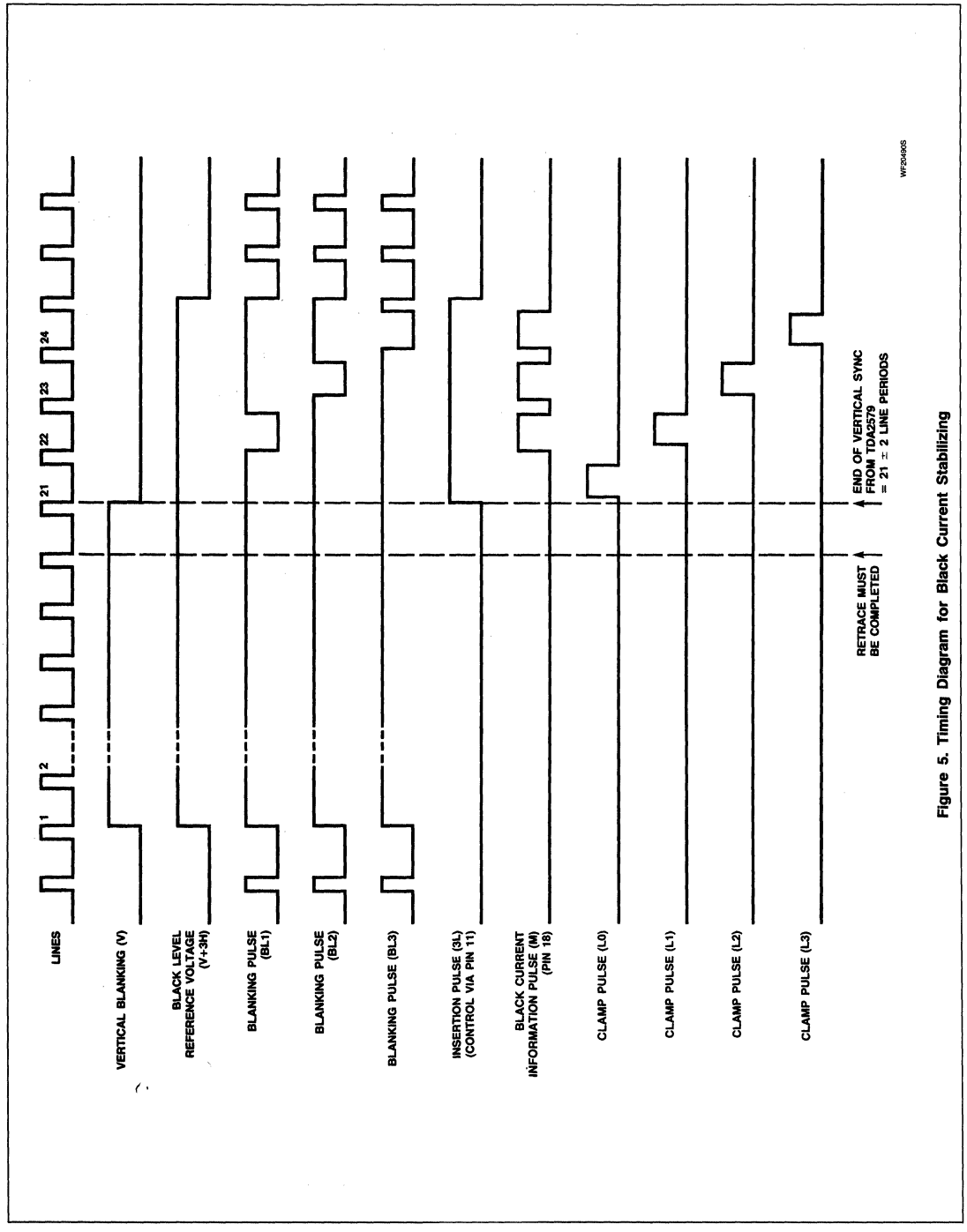
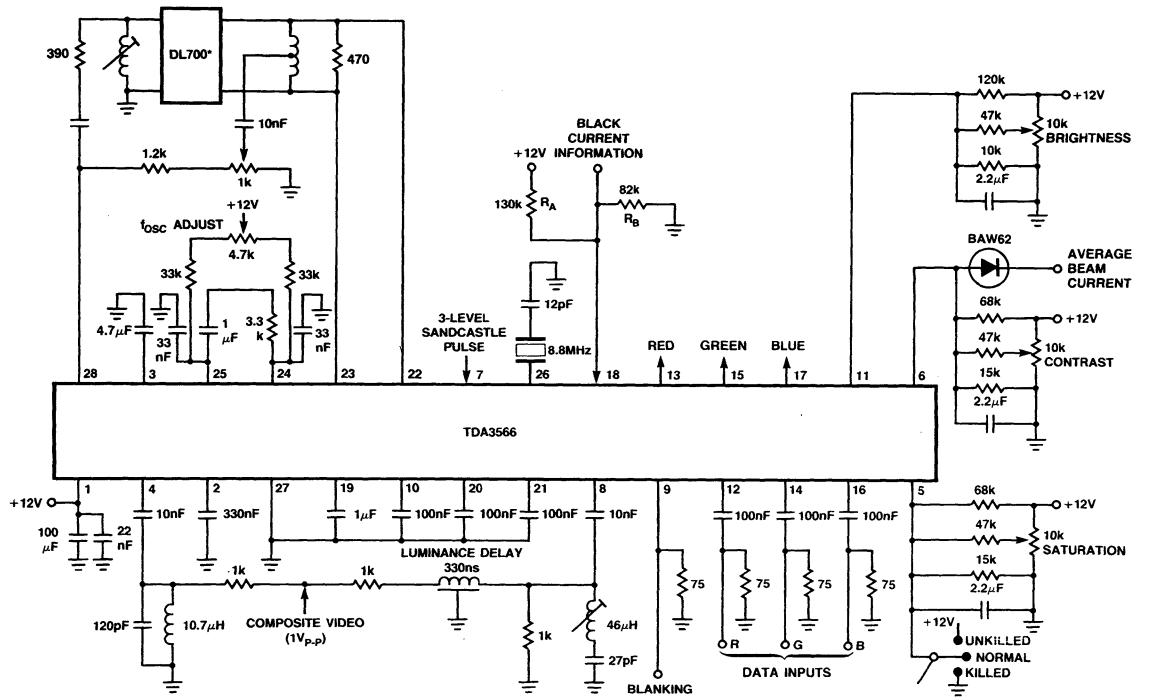


Figure 5. Timing Diagram for Black Current Stabilizing



NOTE:
*D1700 AMPEREX CORP

Figure 6. Application Diagram Showing the TDA3566 for a PAL Decoder

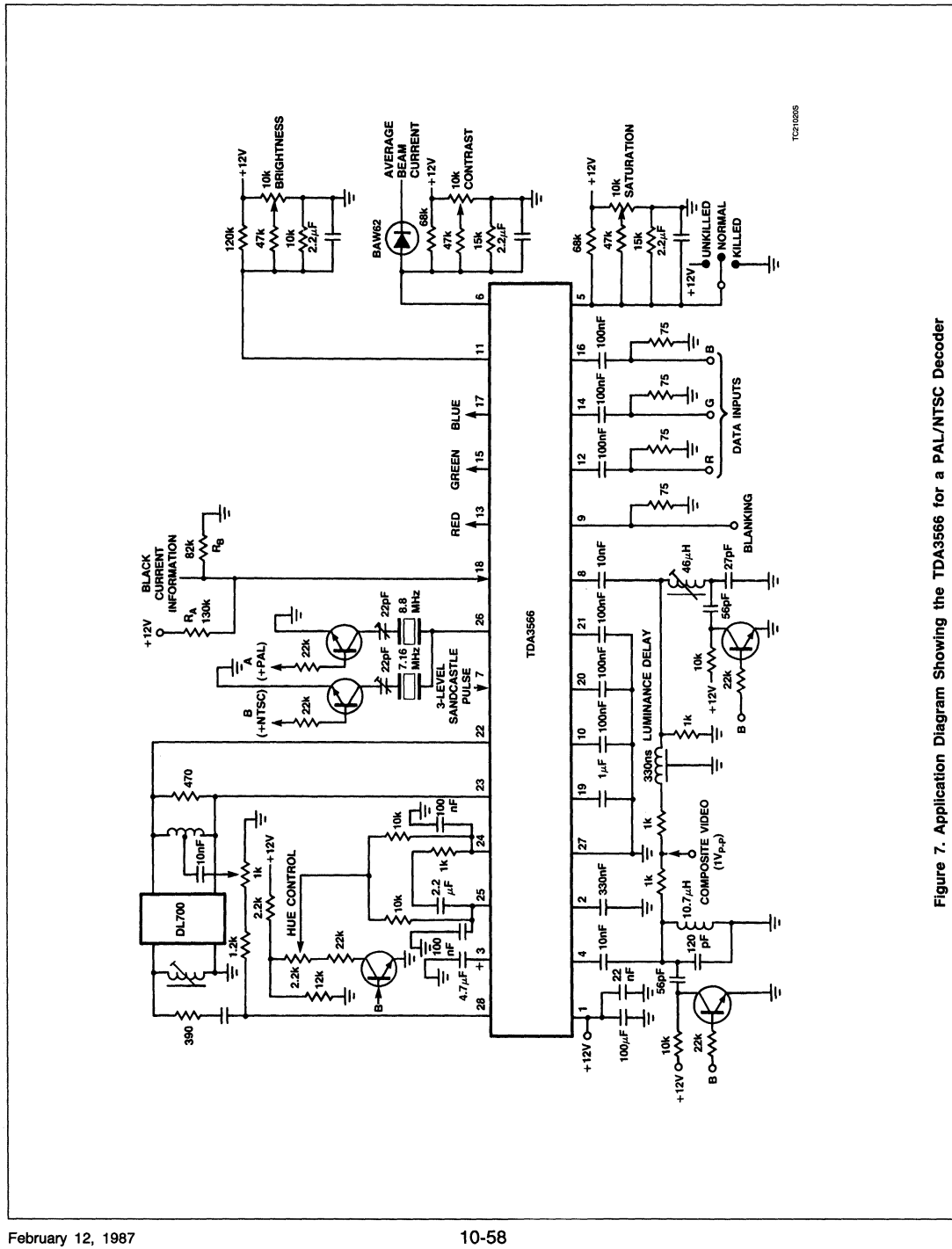
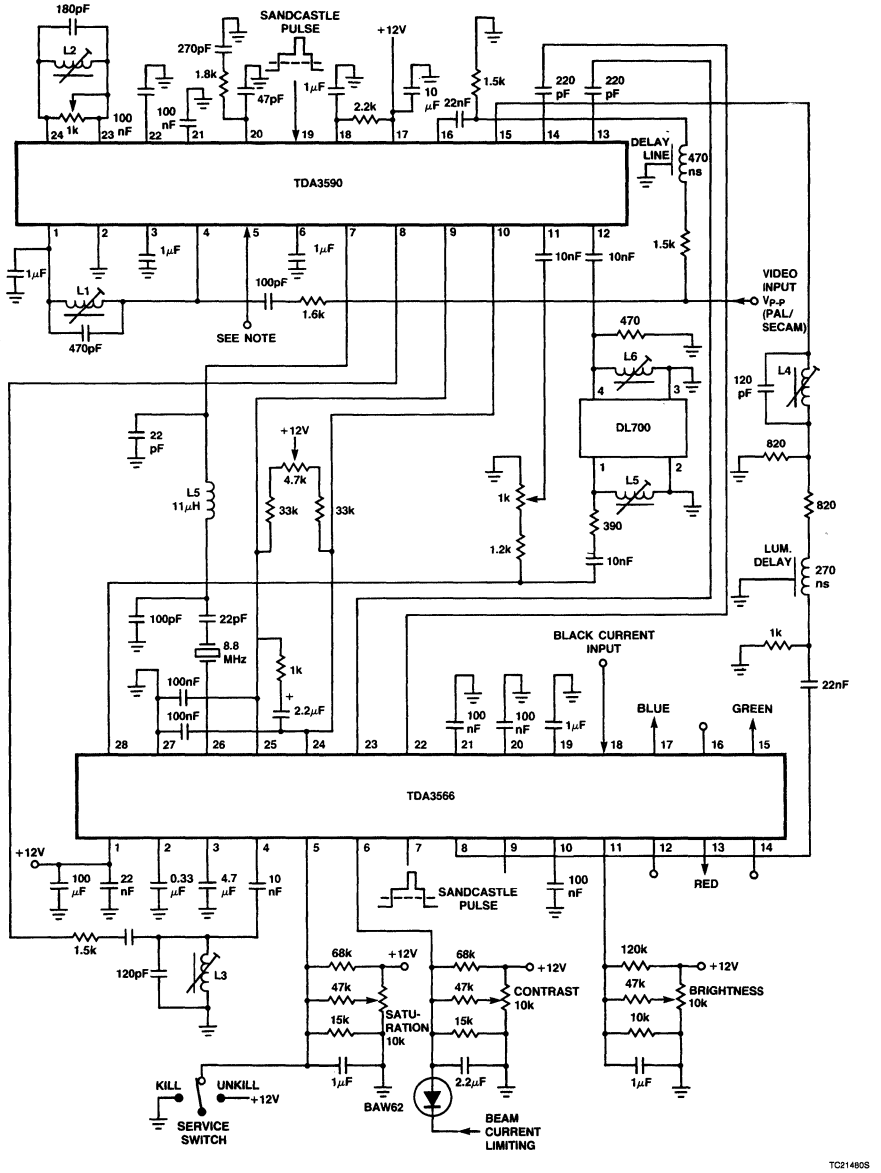


Figure 7. Application Diagram Showing the TDA3566 for a PAL/NTSC Decoder



NOTES:
Note to Pin 5 TDA3590:
$V_{5-2} < 1V$; horizontal identification and black level clamping.
$V_{5-2} > 11V$; vertical identification and artificial black level.
$V_{5-2} = 5$ to 7V; horizontal identification and artificial black level.

Figure 8. PAL/SECAM Application Circuit Diagram Using the TDA3590 and TDA3566

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Signetics

TDA3567
NTSC Color Decoder

Product Specification

Linear Products

DESCRIPTION

The TDA3567 is a monolithic integrated decoder for the NTSC color television standards. It combines all functions required for the demodulation of NTSC signals. Furthermore, it contains a luminance amplifier, and an RGB-matrix and amplifier. These amplifiers supply output signals up to $5V_{P-P}$ (picture information) enabling direct drive of the discrete output stages.

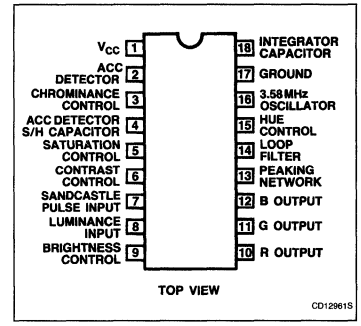
FEATURES

- **Single-chip chroma and luminance processor**
- **ACC with peak detector**
- **DC control settings**
- **High-level RGB outputs**
- **Luminance signal with clamp**
- **Requires few external components**
- **On-chip hue control circuit**

APPLICATIONS

- **Video monitors and displays**
- **TV receivers**
- **Video processing**

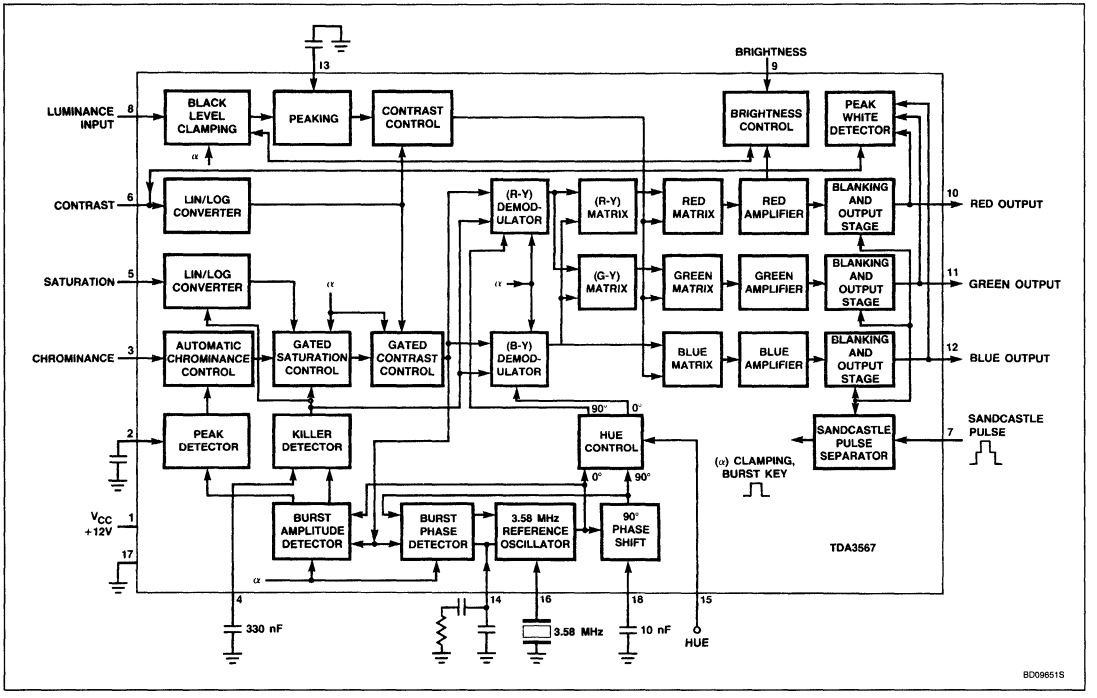
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102HE)	−25°C to +65°C	TDA3567N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{1-17}$	Supply voltage	13.2	V
P_{TOT}	Total power dissipation	1.7	W
T_{STG}	Storage temperature range	−25 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	°C
θ_{JA}	Thermal resistance from junction to ambient (in free-air)	50	°C/W

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DC AND AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{1-17} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
$V_{CC} = V_{1-17}$	Supply voltage		9	12	13.2	V
$I_{CC} = I_1$	Supply current			65		mA
P_{TOT}	Total power dissipation			0.78		W
Luminance input signal						
$V_{8-17(P-P)}$	Input voltage[1] (peak-to-peak value)	Pin 8		450		mV
V_{8-17}	Input voltage level before clipping occurs in the input stage				1	V
I_8	Input current			0.15	1	μA
	Contrast control range	See Figure 1	−17		+3	dB
I_7	Input current contrast control	For $V_{6-17} < 6V$		0.5	15	μA
I_7	Input current when the peak white limiter is active	$V_{6-17} = 2.5V$		5.5		mA
R_{7-17}	Input resistance	$V_{6-17} > 6V$	1.4	2	2.6	kΩ
Peaking of luminance signal						
$\lvert Z_{13-17} \rvert$	Output impedance	Pin 13		200		Ω
	Ratio of internal/external current when Pin 13 is short-circuited			3		
Chrominance amplifier						
$V_{3-17(P-P)}$	Input signal amplitude[2] (peak-to-peak value)	Pin 3		550		mV
$V_{3-17(P-P)}$	Input signal amplitude before clipping occurs in the input stage (peak-to-peak value)				1.1	V
	Minimum burst signal amplitude within the ACC control range (peak-to-peak)		35			mV
	ACC control range		30			dB
ΔV	Change of the burst signal at the output for the complete control range				+1	dB
$\lvert Z_{3-17} \rvert$	Input impedance	Pin 3	6	8	10	kΩ
C_{3-17}	Input capacitance	Pin 3		4	6	pF
	Saturation control range	See Figure 3	50			dB
I_5	Input current saturation control	For $V_{5-17} > 6V$		1	20	μA
$\lvert Z_{5-17} \rvert$	Input impedance	$V_{5-17} = 6V$ to 10V	1.4	2	2.6	kΩ
$\lvert Z_{5-17} \rvert$	Input impedance when the color killer is active		1.4	2	2.6	kΩ
$\lvert Z_{5-17} \rvert$	Input impedance	For $V_{5-17} > 10V$	0.7	1	1.3	kΩ
	Tracking between luminance and chrominance contrast	For 10dB of control		1	2	dB
	Cross-coupling between luminance and chrominance amplifier[4]			−50	−46	dB
Reference part phase-locked loop						
Δf	Catching range		±400	±500		Hz
Δ	Phase shift for 400Hz deviation of the carrier frequency				5	deg

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-17} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Oscillator						
TC_{OSC}	Temperature coefficient of oscillator frequency			1.5	2.5	Hz/°C
Δf_{OSC9}	Frequency deviation	$\Delta V_{CC} = \pm 10\%$		150	250	Hz
R_{16-17}	Input resistance	Pin 16	260	360	460	Ω
C_{22-17}	Input capacitance	Pin 16			10	pF
ACC generation						
V_{4-17}	Voltage at Pin 4 nominal input signal			4		V
V_{4-17}	Voltage at Pin 4 without burst input			1.9		V
V_{4-17}	Color-off voltage			2.5		V
V_{4-17}	Color-on voltage			2.8		V
	Change in burst amplitude with temperature			0.1		%/°C
	Change in burst amplitude with 10% supply voltage change			0		%/V
V_{2-17}	Voltage at Pin 2 at nominal input signal			5		V
Hue control						
	Control voltage range		see Figure 4			
I_{14}	Input current	for $V_{15-17} < 5V$		0.5	20	μA
$\lvert Z_{14-17} \rvert$	Input impedance	for $V_{15-17} > 5V$	1.5	2.5	3.5	kΩ
Demodulation part						
	Ratio of demodulation signals (measured at the various outputs)[7]					
$\frac{V_{10-17}}{V_{12-17}}$	(R-Y)/(B-Y); no (R-Y) signal			-0.42		
$\frac{V_{10-17}}{V_{12-17}}$	(R-Y)/(B-Y); color bar signal			1.4		
$\frac{V_{11-17}}{V_{12-17}}$	(G-Y)/(R-Y); no (B-Y) signal			-0.25		
$\frac{V_{11-17}}{V_{12-17}}$	(G-Y)/(B-Y); no (R-Y) signal			-0.11		
	Frequency response	0 to 0.7MHz			-3	dB
RGB matrix and amplifier						
$V_{10, 11, 12-17(P-P)}$	Output signal amplitude[3]	at nominal luminance input signal and nominal contrast (peak-to-peak value) black-white	4	5	6	V
$V_{12-17(P-P)}$	Output signal amplitude of the "blue" channel	at nominal contrast and saturation control setting and no luminance signal to the input (B-Y) signal (peak-to-peak value)		3.8		V
$V_{10, 11, 12-7}$	Maximum peak-white level[6]		9	9.3	9.6	V

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{1-17} = 12V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$I_{10, 11, 12-17}$	Maximum output current				10	mA
	Difference in the black level between the three channels				600	mV
	Black level shift with vision content			10	40	mV
	Brightness control voltage range		see Figure 3			
I_9	Brightness control input current				−50	μA
V/T	Black level variation with temperature			0.15	1	mV/°C
ΔV	Black level variation with contrast control			75	200	mV
	Relative spread between the three output signals				10	%
ΔV	Relative variation in black level between the three channels	during variations of contrast (10dB), brightness (± 1V), and supply voltage (± 10%)		0	20	mV
ΔV	Differential drift of black level over a temperature range of 40°C			0	20	mV
V_{B1}	Blanking level at the RGB outputs		1.95	2.15	2.35	V
$\frac{\Delta V_{B1}}{V_{B1}} \times \frac{V_{CC}}{\Delta V_{CC}}$	Tracking of output black levels with supply voltage		1	1.05	1.1	
S/N	Signal-to-noise ratio of output signals[5]		62			dB
$V_{R(P-P)}$	Residual 3.58MHz in RGB outputs (peak-to-peak value)			50	75	mV
$V_{R(P-P)}$	Residual 7.1MHz and higher harmonics in the RGB outputs (peak-to-peak value)			50	75	mV
$\lvert Z_{10, 11, 12-17} \rvert$	RGB output impedance				50	Ω
	Frequency response of total luminance and RGB amplifier circuits	0 to 5MHz			−3	dB
Sandcastle input						
V_{7-17}	Level at which the RGB blanking is activated		1	1.5	2	V
V_{7-17}	Level at which burst gate clamping pulses are separated		6.5	7	7.5	V
t_D	Delay between black level clamping and burst gating pulse		300	375	450	ns
I_7 I_7 I_7	Input currents	$V_{7-17} = 0$ to 1V $V_{7-17} = 1$ to 8.5V $V_{7-17} = 8.5$ to 12V		−20	−1 −40 2	mA μA mA

NOTES:

1. Signal with negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for color bar with 75% saturation, so the chrominance-to-burst ratio is 2.2:1.
3. Nominal contrast is specified as maximum contrast −3dB and nominal saturation as maximum saturation −10dB.
4. Cross-coupling is measured under the following conditions:
   - input signals nominal
   - contrast and saturation such that nominal output signals are obtained
   - the signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is specified as peak-to-peak signal with respect to RMS noise.
6. When this level is exceeded, the amplifier of the output signal is reduced via a discharge of the capacitor on Pin 7 (contrast control). Discharge current is 5.5mA.
7. These matrixed values are found by measuring the ratio of the various output signals. The values are derived from the matrix equations given in the section 'FUNCTIONAL DESCRIPTION'.

FUNCTIONAL DESCRIPTION

Luminance Amplifier

The luminance amplifier is voltage driven and requires an input signal of $450mV_{P-P}$ [1]. The luminance delay line must be connected between the IF amplifier and the decoder. The input signal must be AC coupled to the input Pin 8.

The black level clamp circuit of the RGB amplifiers uses the coupling capacitor as a storage capacitor. After clamping, the signal is fed to a peaking stage. The RC network connected to Pin 13 is used to define the amount of overshoot.

The peaking stage is followed by a contrast control stage. The control voltage has to be supplied to Pin 6. The control voltage range is nominally −17 to +3dB. The linear curve of the contrast control voltage is shown in Figure 1.

Chrominance Amplifier

The chrominance amplifier has an asymmetrical input. The input signal at Pin 3 must be AC coupled, and must have an amplitude of $550mV_{P-P}$. The gain control stage has a control range in excess of 30dB, the maximum input signal should not exceed $1.1V_{P-P}$, otherwise clipping of the input signal will occur. From the gain control stage, the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance control stages are directly coupled to obtain good tracking. The saturation is linearly controlled via Pin 5. The control voltage range is 2V to 4V. The impedance is high and the saturation control range is in excess of 50dB. The burst signal is not affected by contrast or saturation control. After the amplification and control stages, the chrominance signal is internally fed to the (R-Y) and (B-Y) demodulators, burst phase, and ACC detectors.

Oscillator and ACC Circuit

The 3.58MHz reference oscillator operates at the subcarrier frequency. The crystal must be connected between Pin 16 and ground. The oscillator does not require adjustment due to the small spreads of the IC. The free-running frequency of the oscillator can be checked by connecting the saturation control (Pin 5) to the positive supply line. Then the loop is opened so that the frequency can be measured. The oscillator has an internal gain-limiting stage which controls the gain to unity, so that internal signals are sinusoidal. This prevents the generation of higher harmonics of the subcarrier signals. The burst signal is compared to a 0° reference signal by the burst amplitude detector, and is then amplified and fed to a peak detector for ACC and to a sample-and-hold circuit which drives the color-killer circuit. The reference signal for the burst phase detector is provided by the 90° phase-shifted signal. An RC network is used to obtain the required catching range and noise immunity for the output voltage of the burst phase detector.

The hue control is obtained by mixing oscillator signals with a phase of 0° and 90° before they are fed to the (R-Y) and (B-Y) demodulators. The 90° phase-shifted signal is provided by a Miller integrator (biased by Pin 18). As the hue control is independent of the PLL, the control will react without time delay on the control voltage changes.

Demodulator Circuits

The demodulators are driven by the amplified and controlled chrominance signals; the reference signals are obtained from the hue control circuit. In nominal hue control position, the phase angle of (R-Y) reference signal is 0°; the phase angle of the (B-Y) reference signal is 90°.

For flesh-tone corrections, the demodulated (R-Y) signal is matrixed with the demodulated (B-Y) signal according to the following equations:

$$(R\text{-}Y)\text{matrixed} = 1.61\ (R\text{-}Y)_{IN} - 0.42\ (B\text{-}Y)_{IN}$$

$$(G\text{-}Y)\text{matrixed} = 0.43\ (R\text{-}Y)_{IN} - 0.11\ (B\text{-}Y)_{IN}$$

$$(B\text{-}Y)\text{matrixed} = (B\text{-}Y)_{IN}$$

In these equations $(R\text{-}Y)_{IN}$ and $(B\text{-}Y)_{IN}$ indicate the color difference signal amplitudes when the chrominance signal is demodulated with a phase difference between the R-Y and B-Y demodulator of 90° and a gain ratio B-Y/R-Y = 1.78.

RGB Matrix Circuit and Amplifiers

The three matrix and amplifier circuits are identical. The luminance signal and the color difference signals are added in the matrix circuit to obtain the color signal.

Output signals are $5V_{P-P}$ (black-white) for the following nominal input signals and control settings:

- Luminance $450mV_{P-P}$
- Chrominance $550mV_{P-P}$ (burst-to-chrominance ratio of the input 1:2.2)
- Contrast −3dB (maximum)
- Saturation −10dB (maximum)

The maximum available output voltage is approximately $7V_{P-P}$. The black level of the red channel is compared to a variable external reference level (Pin 9), which provides the brightness control. The control loop is closed via the luminance input.

The luminance input is varied to control the black level control; therefore, the green and blue outputs will follow any variation of the red output. The output of the black control can be varied between 2V to 4V. The corresponding brightness control voltage is shown in Figure 3.

If the output signal surpasses the level of 9V, the peak white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB Signals

A slicing level of about 1.5V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the rest of the pulse. During blanking, a level of +2V is available at the output.

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NOTE:
1. Signal with negative-going sync; amplitude includes sync pulse amplitude.

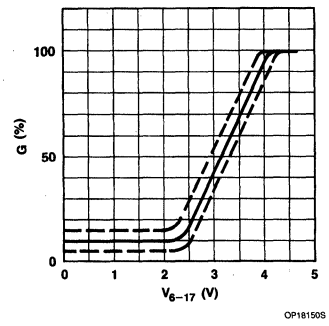


Figure. 1. Contrast Control Voltage Range

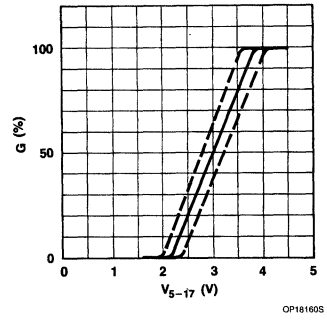


Figure 2. Saturation Control Voltage Range

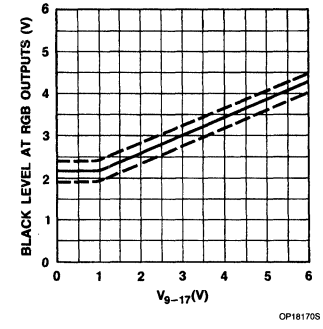


Figure 3. Brightness Control Voltage Range

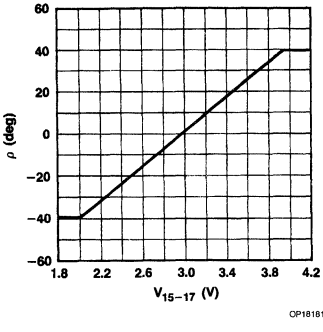


Figure 4. Hue Control Voltage Range

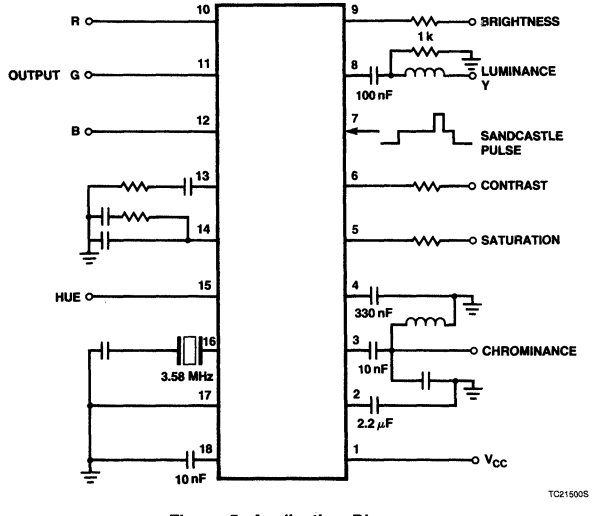


Figure 5. Application Diagram

TDA4555/56
Multistandard Color Decoder

Product Specification

Linear Products

DESCRIPTION

The TDA4555 and TDA4556 are monolithic, integrated, multistandard color decoders for the PAL®, SECAM, NTSC 3.58MHz and NTSC 4.43MHz standards. The difference between the TDA4555 and the TDA4556 is the polarity of the color difference output signals (B-Y) and (R-Y).

FEATURES

Chrominance Part

- Gain-controlled chrominance amplifier for PAL, SECAM, and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64μs glass delay line
- Chrominance output stage for driving the 64μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator Part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference-tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) color difference output stages (blanking)

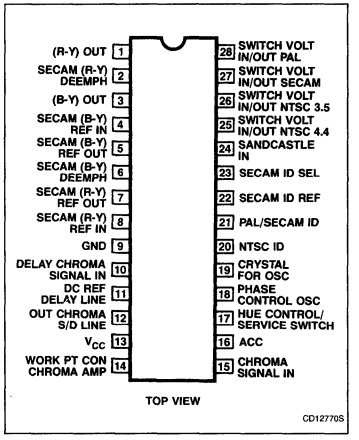
Identification Part

- Automatic standard recognition by sequential inquiry
- Delay for color-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps, and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical, or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double color subcarrier frequency
- HUE control (NTSC)
- Service switch

APPLICATIONS

- Video monitors
- Video processing
- TV receivers

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	0 to +70°C	TDA4555N

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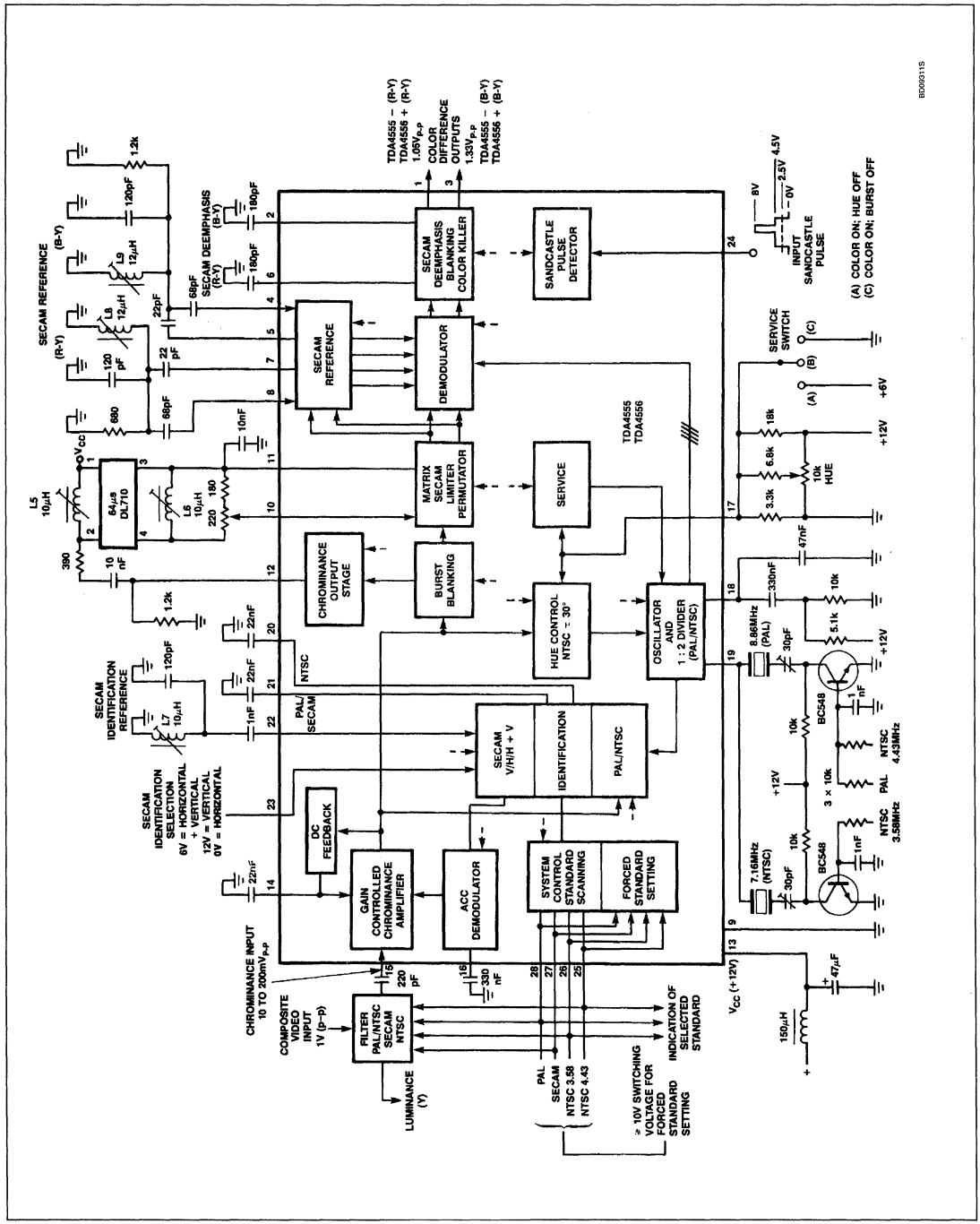
Multistandard Color Decoder | TDA4555/56

BLOCK DIAGRAM AND PERIPHERAL CIRCUITS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{13-9}$	Supply voltage (Pin 13)	13.2	V
V_{n-9}	Voltage range at Pins 10, 11, 17, 23, 24, 25, 26, 27, 28, to Pin 9 (ground)	0 to V_{CC}	V
I_{12}	Current at Pin 12	8	mA
I_{12M}	Peak value	15	mA
P_{TOT}	Total power dissipation	1.4	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{13-9} = 12V$; $T_A = 25°C$; measured in Block Diagram, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 13)					
$V_{CC} = V_{13-9}$	Supply voltage range	10.8		13.2	V
$I_{CC} = I_{13}$	Supply current		65		mA
Chrominance part					
	Chrominance input signal (Pin 15)				
$V_{15-9(P-P)}$	input voltage with 75% color bar signal (peak-to-peak value)	20	100	200	mV
$\lvert Z_{15-9} \rvert$	input impedance	2.3	3.3		kΩ
	Chrominance output signal (Pin 12)				
$V_{12-9(P-P)}$	output voltage (peak-to-peak value)		1.6		V
$\lvert Z_{12-9} \rvert$	output impedance (NPN emitter-follower)			20	Ω
V_{12-9}	DC output voltage		8.2		V
	Input for delayed signal (Pin 10)				
I_{10}	DC input current			10	μA
R_{10-9}	input resistance	10			kΩ
Demodulator part (PAL/NTSC)					
	Color difference output signals output voltage (proportional to V_{13-9}) (peak-to-peak value) TDA4555				
$V_{1-9(P-P)}$	−(R-Y) signal (Pin 1)		1.05V ± 2dB		V
$V_{3-9(P-P)}$	−(B-Y) signal (Pin 3)		1.33V ± 2dB		V
	TDA4556				
$V_{1-9(P-P)}$	+(R-Y) signal (Pin 1)		1.05V ± 2dB		V
$V_{3-9(P-P)}$	+(B-Y) signal (Pin 3)		1.33V ± 2dB		V
$V_{1/3-9}$	Ratio of color difference output signals (R-Y)/(B-Y)		0.79 ± 10%		
$V_{1,\ 3-9(P-P)}$	Residual carrier (subcarrier frequency) (peak-to-peak value)			30	mV
$V_{1,\ 3-9(P-P)}$	Residual carrier (PAL only) (peak-to-peak value)		10		mV
$V_{1-9(P-P)}$	H/2 ripple at (R-Y) output (Pin 1) (peak-to-peak value) without input signal			10	mV
	DC output voltage NPN emitter-follower with				
$V_{1,\ 3-9}$	internal current source of 0.3mA		7.7		V
$\lvert Z_{1,\ 3-9} \rvert$	output impedance			150	Ω

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{13-9} = 12V$; $T_A = 25°C$; measured in Block Diagram, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Demodulator part (SECAM)					
	Color difference signals[1] output voltage (proportional to V_{13-9}) (peak-to-peak value)				
	TDA4555				
$V_{1-9(P-P)}$	−(R-Y) signal (Pin 1)		1.05		V
$V_{3-9(P-P)}$	−(B-Y) signal (Pin 3)		1.33		V
	TDA4556				
$V_{1-9(P-P)}$	+(R-Y) signal (Pin 1)		1.05		V
$V_{3-9(P-P)}$	+(B-Y) signal (Pin 3)		1.33		V
$V_{1/3-9}$	Ratio of color difference output signals (R-Y)/(B-Y)		0.79[2] ±10%		
$V_{1,\ 3-9(P-P)}$	Residual carrier (4 to 5MHz) (peak-to-peak value)		20	30	mV
$V_{1,\ 3-9(P-P)}$	Residual carrier (8 to 10MHz) (peak-to-peak value)		20	30	mV
$V_{1,\ 3-9(P-P)}$	H/2 ripple at (R-Y) (B-Y) outputs (Pins 1 and 3) (peak-to-peak value) with f_O signals			20	mV
$V_{1,\ 3-9}$	DC output voltage		7.7		V
$\Delta V/\Delta T(R-Y)$	Shift of inserted levels relative to levels of demodulated		−0.55		mV/°C
$\Delta V/\Delta T(B-Y)$	f_O frequencies (IC only)		+0.25		mV/°C
HUE control (NTSC)/service switch					
	Phase shift of reference carrier				
$-\phi$	at $V_{17-9} = 2V$		30[3]		deg
ϕ	at $V_{17-9} = 3V$		0		deg
$+\phi$	at $V_{17-9} = 4V$		30[3]		deg
R_{17-9}	Input resistance		5		kΩ
Service position					
	Switching voltage (Pin 17)				
V_{17-9}	burst OFF; color ON (for oscillator adjustment)			0.5	V
V_{17-9}	Hue control OFF; color ON (for forced color ON)	6			V
Crystal oscillator (Pin 19)					
	For double color subcarrier frequency				
R_{19-9}	input resistance		350		Ω
Δf	lock-in-range referred to subcarrier frequency	±400			Hz

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = V_{13-9} = 12V$; $T_A = 25°C$; measured in Block Diagram, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Identification part					
	Switching voltages for chrominance filters and crystals at Pin 28 (PAL) at Pin 27 (SECAM) at Pin 26 (NTSC 3.58MHz) at Pin 25 (NTSC 4.43MHz)				
$V_{25, 26, 27, 28-9}$	Control voltage OFF state			0.5	V
	Control voltage ON state				
$V_{25, 26, 27, 28-9}$	during scanning; color OFF		2.45		V
$V_{25, 26, 27, 28-9}$	color ON		5.8		V
$-I_{25, 26, 27, 28-9}$	Output current			3	mA
	Voltage for forced switching ON				
V_{28-9}	PAL	9			V
V_{27-9}	SECAM	9			V
V_{26-9}	NTSC 3.58MHz	9			V
V_{25-9}	NTSC 4.43MHz	9			V
	Delay time for				
t_{DS}	restart of scanning	2 to 3 vertical periods			
t_{DC1}	color ON	2 to 3 vertical periods			
t_{DC2}	color OFF	0 to 1 vertical periods			
	SECAM identification (Pin 23)				
	Input voltage for				
V_{23-9}	horizontal identification (H)			2	V
V_{23-9}	vertical identification (V)	10			V
V_{23-9}	combined (H) and (V) identification		6[2]		V
	Sequence of standard inquiry PAL-SECAM-NTSC 3.58MHz NTSC 4.43MHz Reliable SECAM identification by PAL priority circuit				
t_S	Scanning time for each standard	4 vertical periods			
Sandcastle pulse detector[4]					
	Input voltage pulse levels (Pin 24)				
V_{24-9}	to separate vertical and horizontal blanking pulses	1.2		2.0	V
$V_{24-9(P-P)}$	required pulse amplitude	2.0		3.0	V
V_{24-9}	to separate horizontal blanking pulse	3.2		4.0	V
$V_{24-9(P-P)}$	required pulse amplitude	4.0		5.0	V
V_{24-9}	to separate burst gating pulse	6.5		7.7	V
$V_{24-9(P-P)}$	required pulse amplitude	7.7		V_{CC}	V
V_{24-9}	Input voltage during horizontal scanning			1.0	V
$-I_{24}$	Input current			100	μA

NOTES:

1. The signal amplitude of the color difference signals (R-Y) and (B-Y) is dependent on the characteristics of the external tuned circuits at Pins 7, 8 and 4, 5, respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_O) provides the same output level as the internally inserted reference voltage (achromatic value).
2. Value measured without influence of external circuitry.
3. Relative to phase at $V_{17-9} = 3V$.
4. The sandcastle pulse is compared to three internal threshold levels, which are proportional to the supply voltage.

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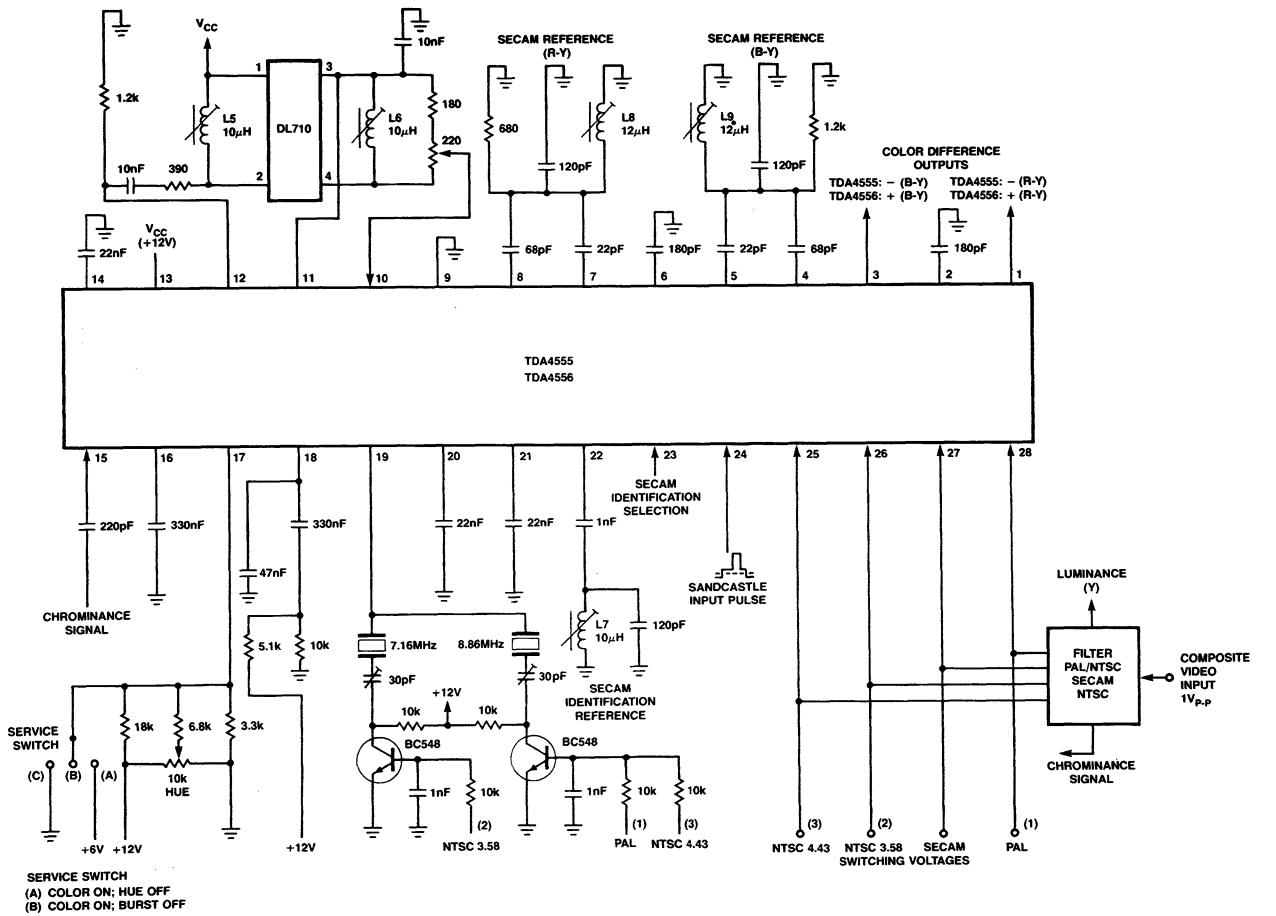

Figure 1. Application Diagram

AN1551
Single-Chip Multistandard Color Decoder TDA4555/ TDA4556

Application Note

In areas where TV transmissions to more than one color standard can be received, color receivers are required which can handle multistandard transmissions without additional manual switching. This requirement will greatly increase with the introduction of satellite TV.

Such receivers have, in the past, incorporated a multistandard color decoder (MSD) using several integrated circuits to automatically select the standard of the received signal. However, the growing need for these MSDs makes it economically and technically desirable to incorporate all the active parts in one IC and to reduce, as far as possible, the external circuitry.

This publication describes two new single-chip MSDs using bipolar technology, the TDA4555 and TDA4556. The ICs are similar except for the polarity of the color difference signals at the output. The TDA4555 provides −(R-Y) and −(B-Y) signals; the TDA4556 provides +(R-Y) and +(B-Y) signals. Only the TDA4555 will be described.

Since all the active parts of the MSD are in a single IC, the design and layout of the printed circuit board is considerably simplified and assembly cost is reduced. The greater reliability of "wiring on silicon" increases the overall reliability of the decoder and reduction of external circuitry simplifies assembly.

The ICs are universally applicable and allow the design of a range of TV receivers having a common chassis. Automatic selection of the required standard has been made more reliable and the maximum time required for identification and switching is a little over half a second.

When reception is difficult because signals are weak, noisy, or badly distorted, the automatic standard recognition (ASR) can be switched off and the standard chosen manually.

Although the ICs are capable of processing multistandard signals, their performance is as high as that for single-standard decoders.

Figure 1 is a block diagram of a typical multistandard color decoder incorporating the TDA4555.

The composite video input signal (CVBS) is fed via switchable filters to the input of the MSD. The filters separate the chrominance and luminance signals according to the standard selected and are controlled by the ASR circuit within the TDA4555.

Chrominance signals from the filters are AC coupled to the input of the TDA4555, which produces the color difference outputs that are, in turn, AC coupled to the Color Transient Improvement (CTI) TDA4565. This IC also contains an adjustable luminance delay-line (Y) formed by gyrators, so a conventional wirewound delay line is not needed.

The signals are then fed to the Video Combination IC, TDA3505, which converts the color difference signals −(R-Y) and −(B-Y) and the luminance signal (Y) into the RGB signals. The TDA3505 also incorporates the saturation, contrast, and brightness control circuits and allows for the insertion of external RGB signals. Finally, the processed video signals are applied, via the RGB output stage, to the picture tube.

The new MSD can decode color TV signals transmitted according to the following standards:

1. NTSC standards with any color subcarrier frequency, for example:
   - NTSC-M (f_O = 3.579545MHz), referred to as NTSC-3.5.
   - Non-standard NTSC systems, for example with $f_O = f_{OPAL}$ = 4.43361MHz. This is a de facto standard used for VCR signals in some European communities and the Middle East, and is referred to as NTSC 4.43. As the color subcarrier frequency is the same as that of the normal PAL system, the same crystal can be used without switching in the reference oscillator for both systems.
2. PAL standard, characterized by phase reversal of the (R-Y) signal on alternate scan lines. The color subcarrier frequency for normal PAL is 4.43361875MHz.
3. SECAM, characterized by transmission of the color difference signals (R-Y) and (B-Y) on alternate scan lines and frequency mod-

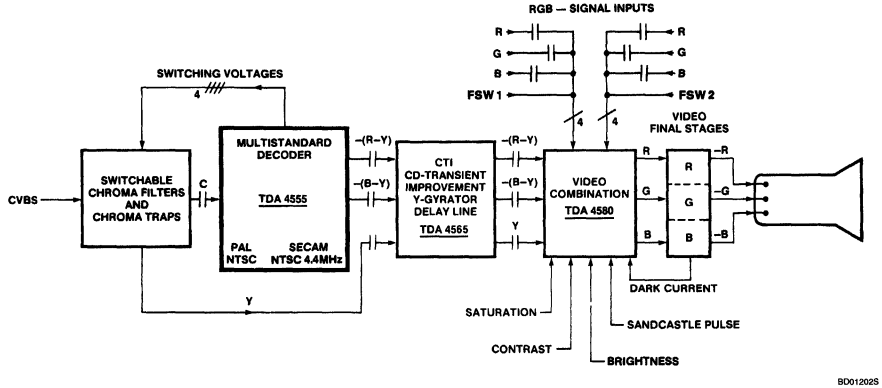

Figure 1. Block Diagram of a Color Decoder

Single-Chip Multistandard Color Decoder TDA4555/TDA4556

AN1551

ulation of the color subcarriers. The frequency of the color signals may vary between 3.900MHz and 4.756MHz. The frequencies of the color subcarriers are:
f_{OB} = 4.250MHz for a "blue line"
f_{OR} = 4.40625MHz for a "red line".

With these capabilities, the new decoders can handle most of the color TV transmissions used in the world.

DESIGN CONSIDERATIONS

To minimize the number of integrated components and reduce the required crystal area and power dissipation of the MSD, the same sections of the IC are used, where possible, for several standards. For example:

- the gain-controlled input stages
- the common switching pulse generators
- the PAL and NTSC quadrature demodulators and oscillators
- the PAL and SECAM delay line
- the common driver stage preceding the delay lines
- part of the stage following the delay line and the demodulator

The number of connections are kept to a minimum compatible with the required functions. With the new ICs, the reference oscillator, its filter, and the SECAM identification circuit, each require only a single pin. The sandcastle pulse is the only external pulse signal. These, and other measures, allow the TDA4555 chip to be housed in a 28-lead SO-117 encapsulation, despite the many functions it performs.

There are three alternative approaches to multi-standard color decoder design.

1. Separate parallel-connected decoders for each standard with the appropriate output selected by switching. This is the principle used in the three-standard decoder comprised of the TDA3510 for PAL, TDA3520 for SECAM, and TDA3570 for NTSC. The color ON/OFF switch voltages generated in each decoder are used for automatic switching of the standards, and each decoder has to be kept at least partially activated.
2. A single PAL decoder can be switched to handle NTSC signals. SECAM signals are converted into quasi-PAL signals by a SECAM-PAL transcoder. The PAL decoder derives the color-difference signals from this quasi-PAL signal. An example of this approach is the circuit using the single-chip PAL decoder TDA3562A with NTSC option and one of the SECAM circuits, TDA3590, TDA3590A, or TDA3591.
3. The methods described in 1 and 2 are not suited to a single-chip MSD because the multiple use of circuit blocks is limited. A much better usage can be obtained if the standards are scanned sequentially. In this approach, the decoder circuit, including the filters at the input, is switched to decode each standard in turn. The switching continues until the standard recognition circuit (SRC) indicates that the standard of the received signal corresponds to the standard of decoding selected at that moment. The scanning procedure is restarted if the standard of the input signal changes because of tuning to another transmitter or switching to an external signal source. The same thing applies if the signal temporarily becomes too weak or disappears. A major advantage of sequential standard switching is that it allows the complete decoder, including the external filters at its input, to be optimized for each standard. This is why the TDA4555 and TDA4556 are designed in this manner.

TDA4555 CIRCUIT DESCRIPTION

Figure 2 is the circuit of a multistandard color decoder using TDA4555/TDA4556.

Pulse Generation

The IC only requires a single sandcastle pulse at Pin 24 for the generation of all internal pulses (e.g., burst key, horizontal, and vertical blanking pulses). The sandcastle pulse levels are > 8V for the burst key, 4.5V for horizontal blanking, and 2.5V for vertical blanking.

Level detectors in the sandcastle pulse detector separate the three levels which are used to generate the required key pulse and clamp pulses.

Standard Control Circuit

A special System Control and Standard Scanning circuit (SCSS) provides the 4 switching voltages to set the MSD to the desired standard.

As long as no color standard is recognized, the SCSS circuit switches the decoder sequentially to the PAL, SECAM, NTSC-3.58 and NTSC-4.43 standards. If the standard of the received signal is not recognized after four field periods (80ms), the next decoding system is activated. This time interval, also called the standard scanning period, is a good compromise between fast switch-on of the color, and effective interference suppression with noisy signals. The maximum time between the start of scanning and switching on the color is 360ms, including the color switch-on delay of two field periods. However, in the TDA4555, a PAL priority circuit is incorporated to improve the reliability for SECAM, so the scanning can last for another two scanning periods (520ms maximum).

After recognition of a SECAM signal, the information is stored and the decoding is switched to PAL. A second SECAM recognition is only provided if no PAL recognition occurs. This gives reliable SECAM recognition when the SECAM-PAL transcoding at the source (e.g., in cable systems) is not perfect, or when PAL signals are distorted by reflections so that they simulate SECAM signals.

With b/w signals, the scanning is continuous and the color is kept switched off because there is no standard recognition.

The switching voltage corresponding to the recognized standard ramps from 2.5V to 6V during scanning while the remaining switching voltages are held at 0.5V maximum.

These 4 voltages are used to switch the filters at the inputs, the crystals of the reference oscillators, and the color subcarrier traps, and also to indicate the recognized standard (e.g., by LEDs).

To prevent unnecessary restarting of scanning because of momentary disturbances (e.g., short-term interruptions of the color signal), the TDA4555 incorporates a delay of two field periods (40ms) before scanning can start.

Finally, the IC allows the automatic standard recognition (ASR) to be switched off by forcing one of the decoding modes by applying at least 9V to Pin 28 for PAL; Pin 27 for SECAM; Pin 26 for NTSC-3.58; and Pin 25 for NTSC-4.43. These pins also serve as outputs for the internally-generated switch voltages which indicate the selected standard.

Color Signal Control

The MSD must provide color-difference output signals with an amplitude referred to a given test signal, despite amplitude variations (within limits) of the color input signal. This is required to maintain a fixed amplitude relationship between the luminance signal (Y) and the color-difference signals, independent of different IF filters or receiver detuning. The TDA4555/56 incorporates an Automatic Color Control circuit (ACC) for this purpose.

In the case of PAL and NTSC, the reference for the control is the burst amplitude. For SECAM, the complete color signal is used. The color signal is AC-coupled, via Pin 15, to a gain-controlled amplifier and the control voltage is obtained by in-phase synchronous demodulation of the burst or the color signal.

This approach has the advantage that the same demodulator, having only one external capacitor at Pin 16, can be used for all standards and also results in noise reduction with noisy signals. Unwanted increase of saturation with noisy signals (color bright-up

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effect) is prevented without an extra peak detector being required.

In-phase synchronous demodulation has the advantage that it is independent of synchronization and the state of the decoder, so the color gain can settle quickly and the color standard scanning period is therefore short. Special low-distortion symmetrical circuits were chosen for the gain-control stage and the following amplifier stage so that H/2 components in the color-difference channel are reduced as far as possible during SECAM reception. Biasing of the color gain-control stage is stabilized by a DC feedback loop decoupled by an external capacitor at Pin 14.

The nominal amplitude of the color input signal at Pin 15 is $100mV_{P-P}$ for a 75% colorbar signal. It may vary between $10mV_{P-P}$ and $200mV_{P-P}$. This range is chosen so that, for a normal $1V_{P-P}$ composite video signal at the input to the filters, transformation is not required.

For PAL and NTSC decoding, the amplitude-controlled color signal, including its burst, is then fed to the SRC, reference generation, and burst blanking stages. The output of the latter stage is applied to the color signal demodulators and the delay-line driver stage.

Standard Recognition Circuit

The SRC tells the SCSS whether the activated decoding mode is the same as that of the incoming signal. This task is performed using the signals occurring during the back porch of horizontal blanking.

For SECAM, it is necessary to distinguish between line (H) identification signals of carrier frequency at the back porch and field (V) identification (special lines carrying identification signals during the field blanking period).

The standard recognition comprises the following parts: a phase discriminator which compares the burst phase of PAL and NTSC signals with the internal reference signal, a frequency discriminator for generating an H/2 signal during SECAM reception, an H/2 demodulator for PAL and SECAM signals, and the logic circuits for the final recognition.

The two phase discriminators for PAL and NTSC signals are supplied with the color signal, and the amplitude-controlled burst. The phase detector for the PAL signals uses the (R-Y) reference signal for the phase comparison; the NTSC phase detector uses the (B-Y) reference signal. Both reference signals are generated by dividing the reference oscillator output. When the correct signals are received, the phase discriminators output the demodulated burst signal for standard recognition.

The discriminator for generating the H/2 signal comprises an internal phase discriminator and an external phase-shift circuit, known as the SECAM identification reference, connected to Pin 22.

The polarity of the PAL and SECAM phase discriminator output signals is reversed line-sequentially. With PAL, this is caused by a change of phase of the burst at line-frequency. With SECAM, it is the result of the color subcarrier frequency changing at line frequency.

Since the signal is changing polarity, it is of no use for the following circuitry. Therefore, the discriminator output signals are fed to the H/2 demodulator which line-sequentially reverses the signal polarity. The pulses are then integrated by external capacitors connected to Pin 21 (PAL and SECAM discriminator output) and to Pin 20 (NTSC phase discriminator output). The voltages on these capacitors are the identification signals which are used by the comparator and logic circuits to derive the control signals. They are dependent on the standard of the incoming signal and on the activated decoding standard and are composed of an internal biasing at half the supply voltage (6V) and a contribution from the identification signal. In the following explanation, only the latter part ΔV_{20} and ΔV_{21} is considered.

a. When the decoder is set to PAL, the frequency of the reference signal is about 4.43MHz. The NTSC discriminator is switched off and the voltage at C_{20} is only the bias voltage. The H/2 demodulator is therefore driven by the output of the PAL discriminator. The output of the SECAM discriminator is not used. With a PAL signal at the input, the H/2 demodulator delivers pulses with equal polarity so that capacitor C_{21} is charged to ΔV_{21} if the reference oscillator is correctly locked.

   With an NTSC-4.43 input signal, the H/2 modulator provides no pulses or, in case of phase faults, small pulses with a line-sequentially changing polarity. The latter is caused by the constant burst phase of NTSC signals which is line-sequentially reversed by the H/2 demodulator. The average charge current of C_{21} is, therefore, zero, and the capacitor voltage equals the biasing voltage.

   When a SECAM or NTSC-3.58 signal is received, the difference between the burst and f_O frequency is so large that the phase changes very rapidly and, as a result, the H/2 pulses are irregular. This causes the average charge current of C_{21} to be zero.

b. When the decoder is set to NTSC-4.43, the PAL and NTSC-4.4 phase discriminator is activated and the SECAM frequency discriminator is switched off. The PAL phase discriminator and the H/2 demodulator operate as previously described.

   With an NTSC-4.43 signal at the input, the output of the NTSC phase discriminator consists of pulses with the same polarity because the burst of the NTSC signal and the reference signal (B-Y) have the same phase.

   With a PAL input signal, the NTSC phase discriminator also outputs pulses with the same polarity, because the PAL burst comprises a component which is stable in the negative (B-Y) direction for each line. Capacitor C_{20} at the output of the NTSC phase discriminator is therefore charged by an NTSC-4.43, as well as a PAL, input signal, although the decoder is set to the NTSC-4.43 mode.

   With NTSC-3.58 and SECAM signals, the average output current of the NTSC phase discriminator is zero ($\Delta V_{20} = 0$) because the frequency of the burst of the carrier frequency does not match that of the reference.

c. When the decoder is set to NTSC-3.58, the oscillator circuit (including dividers) generates reference signals of about 3.58MHz and the SECAM frequency discriminator is switched off. The NTSC-3.58 phase discriminator provides demodulated burst pulses with constant polarity. At the H/2 demodulator output, no pulses, or, in case of phase faults, small pulses with alternating polarity, appear as in the NTSC-4.43 mode.

   For all other color input signals (PAL, SECAM, NTSC-4.43), the large difference between burst or carrier frequency and reference signal frequency prevents defined discriminator output pulses. As a result, the average charge currents of capacitor C_{20} and C_{21} are zero.

d. When decoding SECAM, the H/2 demodulator obtains its signals from the SECAM discriminator. The output of the PAL phase discriminator is not used and the NTSC phase discriminator is switched off so no output signal is available ($\Delta V_{20} = 0$).

   For SECAM decoding, a frequency discriminator in the recognition block is active. H/2 pulses with line-alternating polarity occur when the frequency of the applied signal is alternately higher and lower than the resonant frequency f_{RES} of the SECAM identification circuit.

   $$f_{RES} = (f_{OB} + f_{OR})/2 \cong 4.43MHz$$

   Therefore, the output of the H/2 demodulator is a train of equal polarity pulses charging the capacitor C_{21}. For PAL, NTSC-3.58 and NTSC-4.43 signals, the burst frequency is constant so the output of the frequen-

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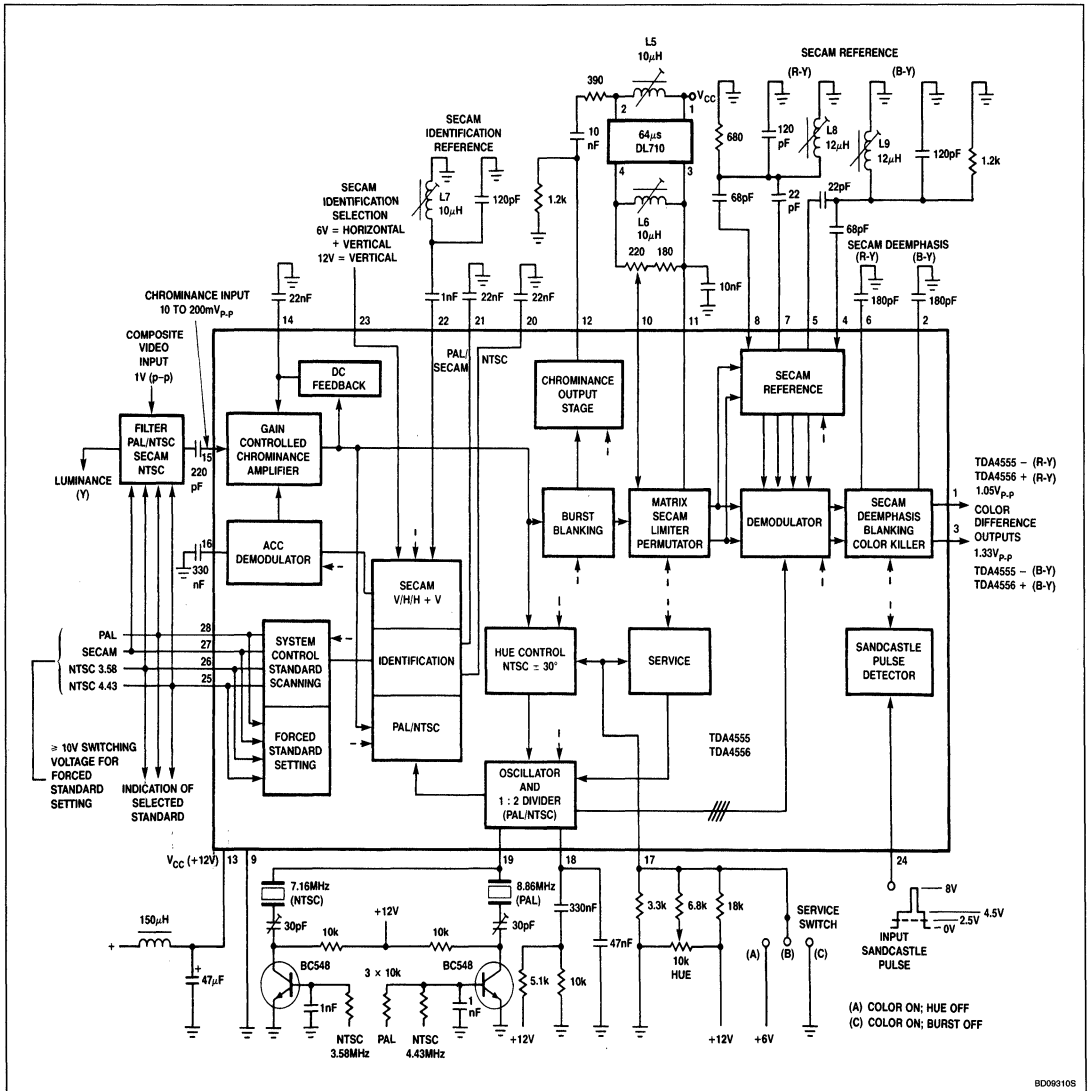

Figure 2. Block Diagram and Peripheral Circuitry

cy discriminator consists of unipolar pulses and the H/2 demodulator outputs alternating polarity pulses. The average charge current of capacitor C_{21} is therefore zero ($\Delta V_{21} = 0$).

The TDA4555 is designed so that identification of SECAM signals can be performed as required by using the special signals in each field blanking period (V-identification) or the burst signal at the back porch (H-identification), or both signals at the same time (H + V-ident). The required standard is selected by applying the appropriate voltage to Pin 23 as follows:

$V_{23} < 2V$ (e.g., ground), H-identification

$V_{23} > 10V$ (e.g., V_{SUPPLY}), V-identification

$V_{23} = 6V$ or floating, H + V-identification.

V-identification is more reliable than the H-identification because the identification signals are longer and have a greater frequency deviation ($\Delta f_{I,B} = 3.9MHz$; $\Delta f_{I,R} = 4.756MHz$). With H-identification, only the normal carrier signal at the end of the back porch is available for identification. When it is required to transmit other information during the field-blanking period, several transmitters (e.g.,in France) stop transmitting the V-identification

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signals. However, the TDA4555 can easily be adapted to such system changes.

Table 1 summarizes the foregoing. For b/w signals, the average charge current is zero, so no standard is recognized and the scanning is continuous.

Generation of PAL and NTSC Reference Signals

For demodulation and identification of the quadrature amplitude-modulated PAL and NTSC color signals, the reference signals Ref(R-Y) and Ref(B-Y) are needed. These signals are derived from the transmitted burst by a PLL which comprises a voltage-controlled oscillator (VCO), a 2:1 frequency divider, and a phase discriminator. The oscillator frequency is twice the subcarrier frequency ($2f_O$) and the circuit has the advantage that the two quadrature reference signals are available at the output of the divider.

With PAL and NTSC, the phase discriminator compares the (R-Y) reference signal and the burst. The burst and the color signal obtained from the ACC stage are applied to the discriminator directly for PAL and via the hue control for NTSC. In the hue control block, the phase of the burst signal can be shifted ±30° by an external voltage of between 2V and 4V at Pin 17. This voltage is derived from the supply by a simple resistor network. Pin 17 also receives the voltage from the "service" switch. If V_{17} is less than 1V (e.g., ground), the color is forced ON and the oscillator free runs because the burst is switched OFF. The oscillator frequency can be adjusted with the trimmers in series with the crystals. If V_{17} is greater than 6V (e.g., the supply voltage), the color is forced ON and the hue control is switched OFF.

The phase discriminator, which provides a VCO control voltage which depends on the phase difference between burst and reference signal, is activated by a burst key pulse. The control voltage is filtered by an external second-order, low-pass filter connected to Pin 18.

The two crystals for the reference oscillator are both connected between Pin 19 and ground via a switch circuit comprising two transistors driven by the external standard switch voltages. To prevent interference, the oscillator is switched off during SECAM decoding.

Color Signal Demodulators

Demodulation of the color signals is performed in the same way as in single standard predecessors.

In the PAL decoding mode, the burst signal is removed from the color signal derived from the gain-controlled chroma amplifier to prevent disturbances caused by reflections in the glass delay-line delayed by other than a single line period. The color signal is applied to an 18dB amplifier and driver stage (emitter-follower) which compensate for the "worst-case" loss in the external delay-line circuit. Color subcarrier signals CSC_{R-Y} and CSC_{B-Y} are separated by the delay line connected to Pin 12 and terminated at both input and output. Direct and delayed signals are matched by a potentiometer in the output termination. Phase matching can be obtained with coils L_5 and L_6, which compensate the delay-line capacitances.

The delayed signal is taken from the potentiometer slider and fed to the internal matrix via Pin 10, where the direct and delayed signal are added and subtracted to obtain the separated color subcarriers CSC_{R-Y} and CSC_{B-Y}. The matrixing is very simple because the demodulators have symmetrical differential inputs and the direct color signal is available in both polarities. Signals of one polarity are applied to one of the (B-Y) demodulator inputs, and signals of the other polarity to one of the (R-Y) demodulator inputs. The remaining input of both demodulators is supplied with the delayed signal. Unlike previous PAL decoders, the PAL switch is located just in front of the (R-Y) demodulator, i.e., in the CSC_{R-Y} signal path.

The actual color signal demodulators are conventional synchronous types comprising an analog multiplying differential stage with a current source in the emitter circuit and balanced, cross-coupled switching stages in the collector circuit. The latter are driven by reference signals Ref(R-Y) or Ref(B-Y) and one or both analog inputs receive the color signal $CSC_{(R-Y)}$ or $CSC_{(B-Y)}$. The color-difference signals CD, obtained after demodulation, are blanked during the line blanking interval to provide signals with clean levels.

For NTSC decoding, the color signal is demodulated in a similar manner except that only the direct (undelayed) signal is used. The PAL switch in the $CSC_{(R-Y)}$ path is not used.

For reception of the line sequential SECAM color signals, a parallel-crossover switch ("permutator") is required before the demodulators. This permutator alternately feeds both demodulators with a direct and (via the external delay line) a delayed color signal of the same subcarrier frequency.

After the permutator, both color channels incorporate a limiter stage to eliminate amplitude modulation. The color signals are demodulated by quadrature demodulators, each comprising an internal multiplier and an external single-tuned phase-shift circuit, known as the SECAM reference circuit. These reference circuits, connected to Pins 5.6 and 7.8, cause a phase shift of about 90° for the unmodulated subcarrier frequency. Thus, for unmodulated subcarrier signals, there is no output apart from the biasing voltage. The SECAM reference circuits are adjusted by L_8 and L_9 so that the reference levels appear at the CD outputs when the subcarrier is unmodulated or when the color is switched off.

In each color-difference channel, the demodulators are followed by internal low-pass de-emphasis networks which remove the unwanted high-frequency components (harmonics of reference and color signals).

The color-difference signals pass, via the output emitter-followers with current sources

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Table 1. Charge on Storage Capacitors C_{20} and C_{21} for Combinations of Input Signals and Decoding Mode

DECODING MODE	STANDARD OF THE COLOR INPUT SIGNAL									
	PAL		NTSC-4.433		NTSC-3.588		SECAM		B/W	
	C_{20}	C_{21}	C_{20}	C_{21}	C_{20}	C_{21}	C_{20}	C_{21}	C_{20}	C_{21}
PAL	0*	+	0*	0	0*	0	0*	0	0	0
NTSC-4.43	+	+	+	0	0	0	0	0	0	0
NTSC-3.58	0	0	0	0	+	0	0	0	0	0
SECAM	0*	0	0*	0	0*	0	0*	+	0	0

NOTES:
0 average charge current $I_{AV} = 0$, $\Delta V_C = 0$, $V_C = ½$ supply
+ average charge current $I_{AV} > 0$, $\Delta V_C > 0$ (assuming correct locking of the reference oscillator and proper switching of the H/2 demodulators)
* NTSC phase discriminators switched off

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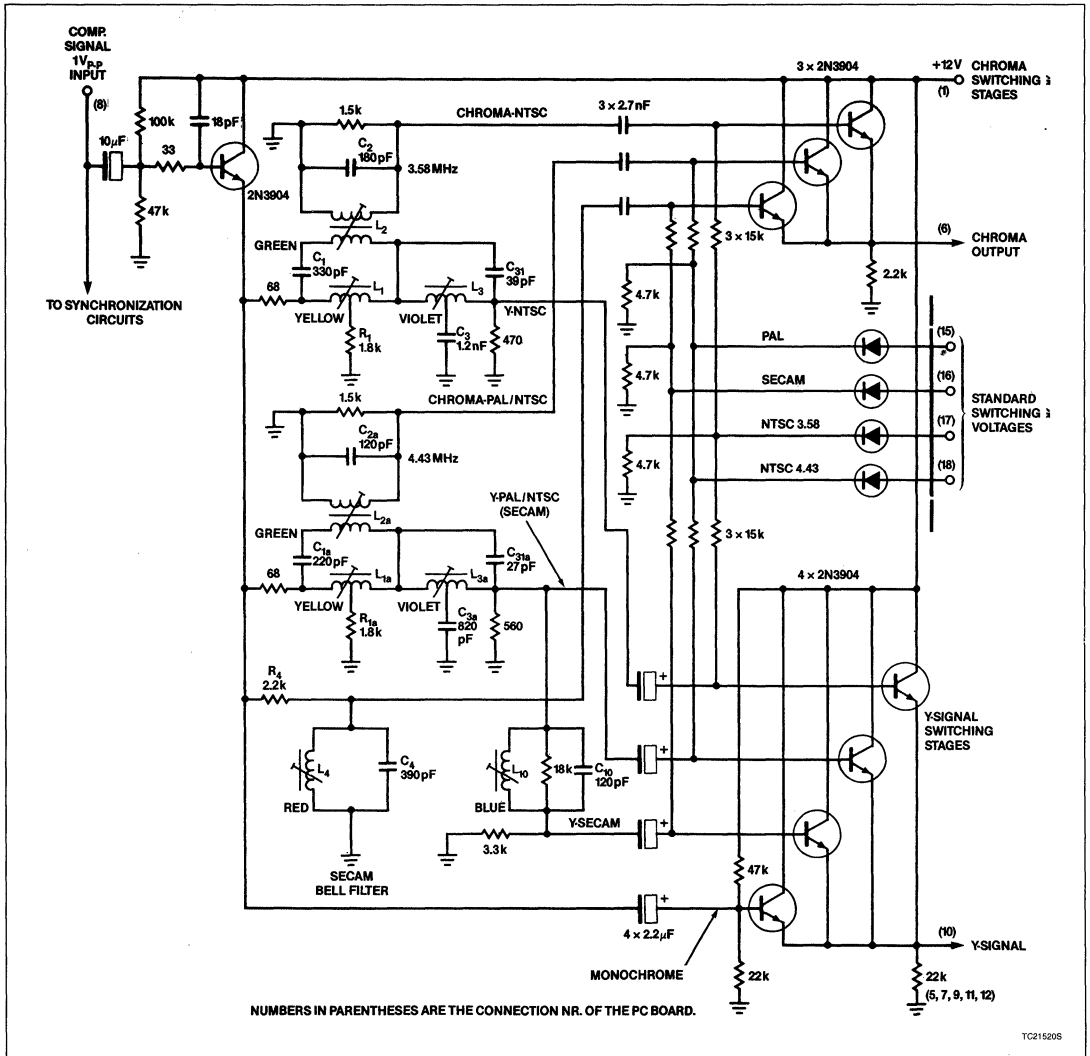

Figure 3. Input Filters and Standard Switching

in their emitter circuits, to Pins 1 and 3, no matter what decoding mode is selected. They have the following nominal amplitudes referred to a 75% saturated color bar:

$V_{(R-Y)} = 1.05V_{P-P}$; $V_{(B-Y)} = 1.33V_{P-P}$.

For the TDA4555, the polarity of the signals is negative and therefore suitable for input to the video combination family TDA3500 (except TDA3506).

The TDA4556 is similar to the TDA4555 except for the positive polarity of the TDA4556 color difference output signals. Therefore, this TDA4556 can be used with the Video Combination TDA3506.

APPLICATION CONSIDERATIONS

Circuit Example

Figure 2 is a tested circuit of a multistandard decoder. A more detailed circuit of the input filters is shown in Figure 3. These filters separate the luminance signal (Y) from the color signals for the four decoding modes.

The same filters can be used for PAL and NTSC-4.43 signals since they have a similar frequency spectrum. For SECAM signals, it is possible to use the 4.43MHz subcarrier trap of the PAL/NTSC-4.43 filter, but it is then necessary to add a trap tuned to about 4.05MHz in the Y channel. This filter suppresses the color signal components below about 4.2MHz, which mainly occur during the "blue SECAM line".

The filter circuits for PAL and NTSC signals are based on a separation filter which also equalizes phase delay. This means that, be-

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Table 2. Coil Data for the Multistandard Decoder of Figure 2 and Figure 3

COIL NO	INDUCTANCE (μH)	Q	TOKO TYPE NO.[1]	NO. OF TURNS	COLOR	USE	FIGURE
L_1/L_{1a}	5.5	> 90 (4.43MHz)	119 LNS-A 4449 AH	8 + 8	Yellow	Separation filter	3
L_2/L_K L_{2a}/L_{Ka}	12.5	> 90 (4.43MHz)	119 LNS-A 4451 DY	24/1	Green	Color bandpass filter	3
L_3 L_{3a}	66	60 (2.52MHz)	KANS-K 4087 HU	19 + 46	Violet	Phase delay correction	3
L_4	3.8	60 (4.43MHz)	113 CNS-2 K 843 EG	17 (= 14 + 3)	Red	Bell filter	3
L_5, L_6, L_7	10	> 80 (4.43MHz)	119 LN-A 3753 GO	11 + 11	Blue	Decoder board and SECAM trap for f_{OB}	2
L_{10}	10	> 80 (4.43MHz)	119 LN-A 3753 GO	11 + 11	Blue	PAL/NTSC trap	3
L_8, L_9	12	> 80	119 LN-A 3753 GO	12 + 12	Blue	Decoder board	2

NOTE:
1. Toko America, Mt. Prospect, IL 312/297-0070

sides separating the luminance and color signals, the impulse response of the luminance channel is improved and has symmetrical overshoots, giving the impression of better resolution on the screen. This type of filter is only given as an example. Simpler filters can also be used. The SECAM circuit contains the obligatory "bell" filter. Coil data for the circuit shown in Figure 3 is given in Table 2.

Figure 4 shows oscillograms of the luminance and color filtering in the three signal paths. It can be seen that the color passband in the PAL and NTSC decoding mode has its minimum just below the color subcarrier frequency. This means that the lower sideband of the color signal is mainly used and, as a result, the filter may have a narrower bandwidth. Generally, the upper sideband of the color signal is already attenuated by the IF filter. The passband of the filter in the SECAM color signal path has the required "bell" shape as shown in Figure 4c.

From the low-pass characteristics of the luminance channels, it follows that the subcarriers (4.43MHz for PAL/NTSC-4.43 and 3.58MHz for NTSC-3.58) and the unmodulated carrier frequency ($f_{OB} \cong 4.41$MHz for SECAM) are strongly attenuated. Additionally, low-pass filter ($L_{10}C_{20}$) of the SECAM luminance channel resonates at about 4.05MHz which provides the required attenuation of frequencies below 4.2MHz for modulated carriers.

All three separation filters are fed with the CVBS input signal via an emitter-follower (transistor BC548B). Therefore, the complete decoder has a high input resistance and the filters are driven for a low impedance signal source.

Depending on the decoding mode, the luminance signal is fed from the appropriate filter, via the luminance delay line, to the video combination IC, and the color signal is fed via a small coupling capacitor (220pF) to input Pin 15 of the decoder IC.

Emitter-followers in the color signal path provide the required switching. There is one for each mode, PAL/NTSC-4.43, NTSC-3.58, and SECAM, feeding a common emitter-resistor. Three more emitter-followers in the luminance signal path are combined with a fourth which supplies the unfiltered video signal to the video combination IC during b/w reception, or while the standards are being scanned. The video signals are applied to the bases of the transistor switches via coupling capacitors, the switch voltages being supplied via resistor-diode networks. The fourth transistor switch in the luminance channel has fixed-base biasing of about 4.4V.

The resistors in parallel with the SECAM tuned circuits determine their Q and therefore the conversion efficiency (dV/df) of the demodulators in the SECAM mode and can be used to set the nominal output values of the CD signals (with a color bar signal). The switch transistors for the oscillator crystals at Pin 19 have their collectors connected, via 10kΩ resistors, to the supply line. Because they are either fully conducting or completely cutoff and the voltages are low (12V max.), the type of transistor is not critical.

The standard control voltage outputs (Pins 25 to 28) can deliver a current of 3mA which is insufficient to drive a LED to indicate the standard to which the circuit is set. An additional transistor amplifier such as that shown in Figure 5 is therefore required. Resistor R_{CS} determines the current through the LED, and R_{BS} limits the maximum base current.

If an indication is provided for each of the standard switch voltages, then it is easy to establish which standard, if any, is recognized. When all the diodes light up in sequence, the circuit is still scanning and no standard has been recognized.

Alignment of the Input Filter

The alignment of both the PAL/NTSC-4.43 and NTSC-3.58 separation filters consists of three procedures for each separation filter.

1. **Alignment of the Color Bandpass**
   Apply a sweep signal [f = 3.5MHz (4MHz); $\Delta f \cong \pm 3$MHz (± 3MHz) to the filter input (PCB Pin 8). Connect an oscilloscope to PCB Pin 6 and make the filter output available at IC Pin 6 by applying an external switch voltage to the appropriate switch transistor. Adjust $L_2(L_{2a})$ for maximum output at 3.45MHz (4.2MHz).
2. **Alignment of the Compensation Circuit**
   Apply a 3.58MHz (4.43MHz) subcarrier to the filter input (PCB Pin 8) and adjust $L_1(L_{1a})$ so that the voltage at the Y output of the filter is minimum. This Y output can be measured at the 470Ω (560Ω) terminating resistor, or at PCB Pin 10, if the proper switch transistor is activated by an external switch voltage.
3. **Alignment of the Phase Delay Equalizer**
   Apply a 16 100kHz square wave to the filter input (PCB Pin 8) and connect an oscilloscope to the output of the luminance filter (470Ω or 560Ω terminating resistor).

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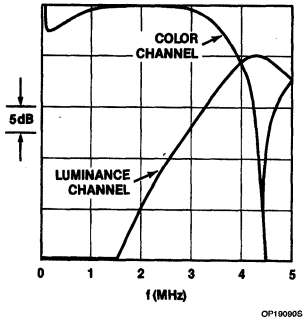
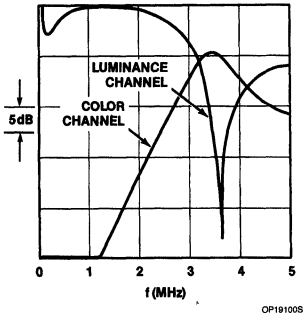
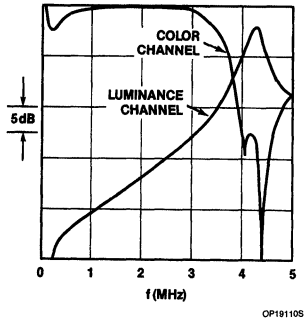


a. PAL/NTSC-4.43 (f_O = 4.433MHz)



b. NTSC-3.58 (f_O = 3.579MHz)



c. SECAM (f_{OB} = 4.250MHz, f_{OR} = 4.406MHz), "Bell" Filter (f_{RES} = 4.286MHz)

Figure 4. Amplitude-frequency Characteristics of Input Filter

Alternatively, the oscilloscope can be connected to PCB Pin 10, if an external switch voltage is applied to the appropriate input. Adjust coil $L_3(L_{3a})$ to obtain a symmetrical overshoot at the leading and trailing edges of the pulse.

Because the impulse response of a receiver also depends on the IF filter, it is recommended that the filter be included in the test signal path when aligning L_3/L_{3a}. In practice, a square wave-modulated IF signal should be applied to the input of the IF circuit for this adjustment.

Filter $L_{10}C_{10}$ attenuates the SECAM color signal in the luminance channel below 4.2MHz. L_{10} is adjusted so that an applied 4.05MHz signal has minimum amplitude at the output of the SECAM Y-filter (terminating resistor 3.3kΩ, or PCB Pin 10, if an external switch voltage is applied to the appropriate input).

To align the SECAM "bell" filter, a SECAM color bar is applied to the filter input (PCB Pin 8) and an external switch voltage (e.g., the supply voltage) to PCB Pin 16 to force the SECAM decoding mode. L_4 is then adjusted for minimum amplitude-modulation of the filtered color signal (PCB Pin 6).

To locate the coils to be adjusted, it is useful to color code them as shown in Table 2 and Figure 3.

Decoder Alignment

PAL and NTSC-4.43 Signals

Force the PAL decoding mode by an external voltage exceeding 9V (e.g., the supply voltage) applied to Pin 28 of the IC (or PCB Pin 15) and apply a PAL color signal (e.g., color bar) to the filter input, PCB Pin 8. Connect IC Pin 17 to ground with the service switch. The color is forced ON and the oscillator is free-running because the PLL oscillator circuit does not receive the burst.

Adjust the trimmer in series with the 8.8MHz crystal for minimum color rolling. Alternatively, observe the color-difference signals at IC output Pins 1 and 3 and minimize the beat frequency with the trimmer. This 8.8MHz oscillator adjustment is also valid for the decoder in NTSC-4.43 mode.

To adjust the phase of the delay-line decoder, apply a PAL color bar signal to the input of the circuit (PCB Pin 8) with the service switch in its normal (middle) position. Adjust L_5 and L_6 to minimize amplitude differences of each color bar in the (B-Y) output signal (IC Pin 3 or PCB Pin 13).

Alternatively, minimize the PAL structure (pairing of the lines) observed on the screen. If the adjustment range of L_5 is too small, adjust L_6.

To adjust the amplitude of the delay-line decoder, apply an NTSC-4.43 color bar signal to the input of the circuit (PCB Pin 8) and connect IC Pin 17 to the supply line with the service switch. The color is forced ON and the hue control is switched off. Adjust the 220Ω potentiometer connected to Pin 4 of the DL711 delay line for minimum amplitude differences of each color bar in the (R-Y) output signal (IC Pin 1 or PCB Pin 14) using an oscilloscope, or, observing the picture-tube screen, minimize the PAL structure (pairing of the lines).

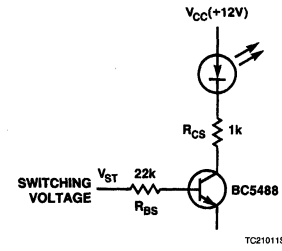


Figure 5. Example of Standard Indicator Circuit

Special test patterns can also be used for delay line adjustment.

Finally, remove the external switching voltage applied to Pin 28 and put the service switch in the mid (normal) position.

NTSC-3.58 Signals

In this case, only the 7.16MHz oscillator has to be adjusted. Force the circuit to the NTSC-3.58 decoding mode by connecting IC Pin 26 or PCB Pin 17 to the supply voltage. Apply an NTSC 3.58 color signal to the filter input (PCB Pin 8). Connect IC Pin 17 to ground with the service switch. The color is forced ON and the oscillator is free-running because the PLL oscillator does not receive burst signals.

Adjust the trimmer in series with the 7.16MHz crystal for minimum color rolling. Alternatively, observe the CD signals at the IC output Pins 1 and 3 and minimize the beat frequency.

Finally, remove the connection between PCB Pin 17 and the supply voltage and put the service switch back to its mid position.

Alignment for SECAM Signals

Force the circuit in the SECAM decoding mode by connecting the supply voltage to IC Pin 27 (or PCB Pin 16). Apply a SECAM color bar to the filter input (PCB Pin 8).

Connect IC Pin 23 (or PCB Pin 20) to the supply line to activate the H-identification. Connect a high-impedance (> 10MΩ) voltmeter between IC Pin 21 and ground. Adjust coil L_7 for the maximum voltage at IC Pin 21.

Observe the −(R-Y) output signal at IC Pin 1 (PCB Pin 14) with an oscilloscope. Adjust L_8 so that the levels of the black and white bars are in accordance with the level inserted during blanking.

Observe the −(B-Y) output signal at IC Pin 3 (PCB Pin 13) with an oscilloscope. Adjust L_9

Single-Chip Multistandard Color Decoder TDA4555/TDA4556

AN1551

so that the levels of the black and white bars are in accordance with the levels inserted during blanking.

Use of the PC Board for a PAL-Only Decoder With the TDA4510

To efficiently manufacture a family of receivers, based on the same main PC board, the TDA4555/TDA4556 can be used as a single standard decoder (e.g., a NTSC-only decoder), but the "pin-aligned" TDA4570 is a cheaper alternative. The connections of the TDA4570 and those of the TDA4555 are shown in Figure 6. Apart from the omission of many peripheral components, only small changes in the external circuitry are needed.

NOTE:
This application note, written by Klaus Juhnke and published as Technical Publication 169 by ELCOMA in 1985, has been revised and edited.

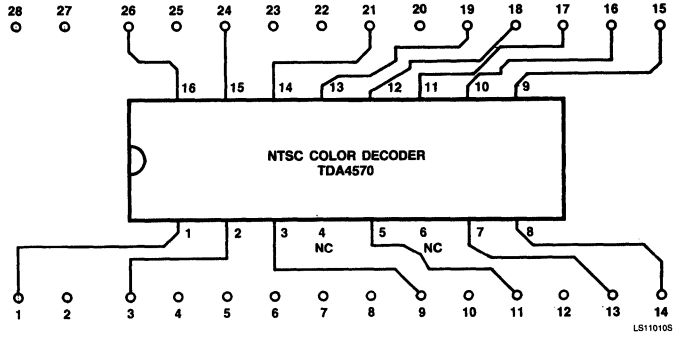


Figure 6

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Signetics

TDA4565
Color Transient Improvement Circuit

Product Specification

Linear Products

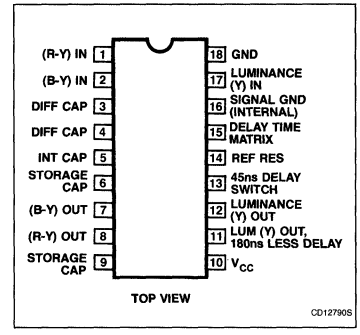
DESCRIPTION

The TDA4565 is a monolithic integrated circuit for color transient improvement (CTI) and luminance delay line in gyrator technique in color television receivers.

FEATURES

- **Color transient improvement for color difference signals (R-Y) and (B-Y) with transient detecting, storage, and switching stages resulting in high transients of color difference output signals**
- **A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line**
- **Switchable delay time from 690ns to 1005ns in steps of 45ns**
- **Two Y output signals; one of 180ns less delay**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102CS)	0 to +70°C	TDA4565N

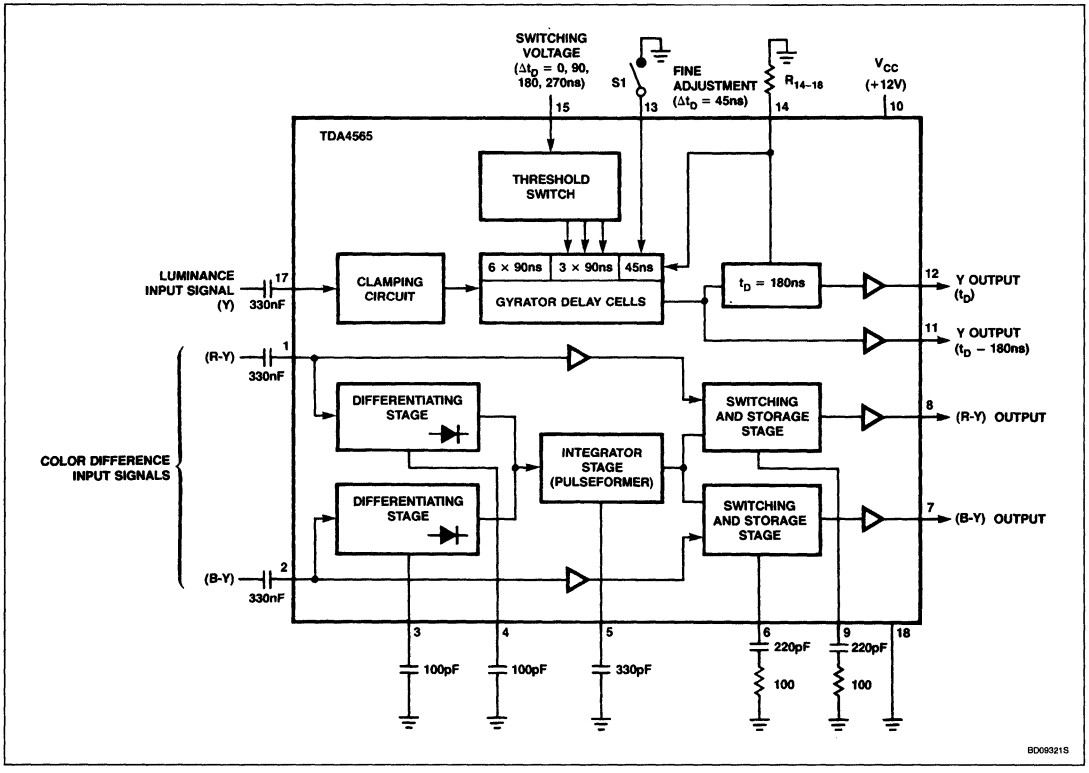
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{10-18}$	Supply voltage (Pin 10)	13.2	V
	Voltage ranges to Pin 18 (ground)		
V_{n-18}	at Pins 1, 2, 12, and 15	0 to V_{CC}	V
V_{11-18}	at Pin 11	0 to (V_{CC}–3V)	V
V_{17-18}	at Pin 17	0 to 7	V
	Voltage ranges		
V_{7-6}	at Pin 7 to Pin 6	0 to 5	V
V_{8-9}	at Pin 8 to Pin 9	0 to 5	V
	Currents		
$\pm I_{6, 9}$	at Pins 6, 9	15	mA
$I_{7, 8, 11, 12}$	at Pins 7, 8, 11, and 12		
P_{TOT}	Total power dissipation	1.1	W
T_{STG}	Storage temperature range	–25 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

NOTE:
DC potential not published for Pins 3, 4, 5, 6, 9, 13, and 14.

Color Transient Improvement Circuit TDA4565

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS $V_{CC} = V_{10-18} = 12V$; $T_A = 25°C$; measured in application circuit Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 10)					
$V_{CC} = V_{10-18}$	Supply voltage	10.8	12	13.2	V
$I_{CC} = I_{10}$	Supply current		35	50	mA
Color difference channels (Pins 1 and 2)					
V_{1-18}	(R-Y) input voltage (peak-to-peak value) 75% color bar signal		1.05		V
V_{2-18}	(B-Y) input voltage (peak-to-peak value) 75% color bar signal		1.33		V
$R_{1,\ 2-18}$	Input resistance		12		kΩ
$V_{1,\ 2-18}$	Internal bias (input)		4.3		V
α_{CD}	(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$		0		dB
$V_{7,\ 8-18}$	Output voltage (DC)		4.3		V
$-I_{7,\ 8}$	Output current (emitter-follower with constant-current source 0.6mA)		1.2		mA
t_{TR}	(R-Y) and (B-Y) output signal transient time		150		ns
Y-signal path (Pin 17)					
$V_{17-18(P-P)}$	Y-input voltage (composite signal) (peak-to-peak value)		1		V
V_{17-18}	Internal bias voltage (during clamping)		1.5		V
I_{17} $-I_{17}$	Input current during picture content during synchronizing pulse		 8 100		 μA μA
α_Y	Y-signal attenuation $\frac{V_{11}}{V_{17}}$		6.5		dB
α_Y	Y-signal attenuation $\frac{V_{12}}{V_{17}}$		6.5		dB
V_{11-18}	Output voltage (DC)		2.3		V
V_{12-18}	Output voltage (DC)		10.3		V
$-I_{11,\ 12}$	Output current (emitter-follower with constant-current source 0.6mA)		1.2		mA
$f_{11,\ 12-17}$	Cut-off frequency[1, 3] $R_{14-18} = 1.2k\Omega$; $V_{15-18} = 12V$; S1 open		5		MHz
	Adjustable delay[2, 3] (S1 open)				
t_D	at $V_{15-18} = 0$ to 2.5V; $R_{14-18} = 1.2k\Omega$	630	690	750	ns
t_D	at $V_{15-18} = 3.5$ to 5.5V; $R_{14-18} = 1.2k\Omega$	720	780	840	ns
t_D	at $V_{15-18} = 6.5$ to 8.5V; $R_{14-18} = 1.2k\Omega$	810	870	930	ns
t_D	at $V_{15-18} = 9.5$ to 12V; $R_{14-18} = 1.2k\Omega$	900	960	1020	ns
Δt_D	Fine adjustment delay (S1 closed) at $V_{13-18} = 0V$		45		ns
t	Signal delay for velocity modulation (Pin 11)		$t_D - 180ns$		
θ_{JA}	Thermal resistance from junction to ambient (in free air)			70	°C/W

NOTES:
1. R_{14-18} influences the bandwidth.
2. Delay time is proportional to resistor R_{14-18}.
3. Devices with suffix "α" require the value of resistor R_{14-18} to be 1.1kΩ, but the cut-off frequency and delay times remain as stated in these characteristics.

FUNCTIONAL DESCRIPTION

The IC consists of two color difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in the Block Diagram.

Color Difference Channels

The (B-Y) and (R-Y) color difference channels consist of a buffer amplifier at the input, a switching stage, and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the color difference detecting signal (Pins 1 and 2). Two parallel storage stages are incorporated in which the color difference signals are stored during the transient time of the signal. At the end of this transient time, they are switched immediately (transient time of 150 ns) to the outputs. The color difference channels are not attenuated.

Y-signal Path

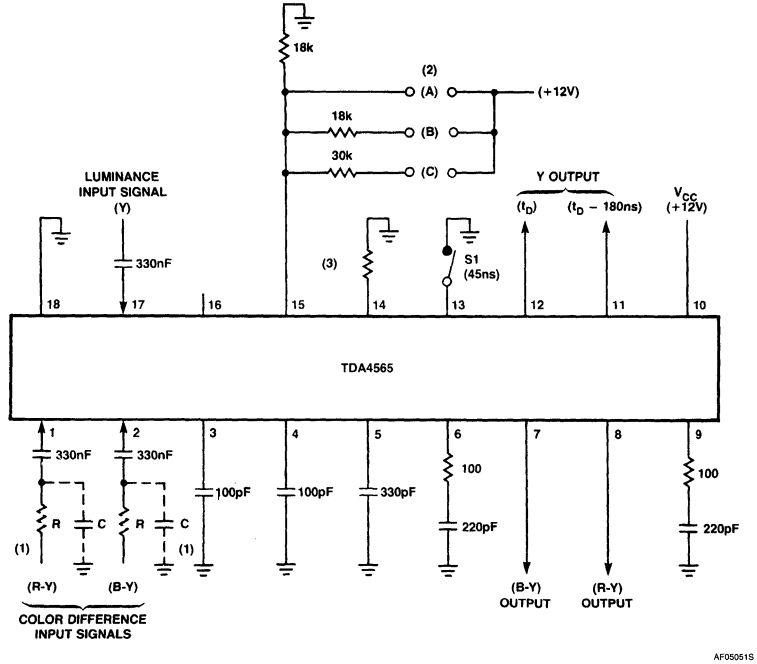
The Y-signal input (Pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1005ns, including an additional delay of 45ns via the fine adjustment switch (S1) at Pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at Pin 15. Thus, three switchable delay times of 90ns, 180ns, or 270ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 6.5dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to Pin 12 via a buffer amplifier. An additional output stage provides a signal of 180ns less delay at Pin 11.

Table 1. Switching Sequence for Delay Times

CONNECTION			VOLTAGE AT PIN 15	DELAY TIME (ns)*
(A)	(B)	(C)		
O	O	O	0 to 2.5V	690
O	O	X	3.5 to 5.5V	780
O	X	X	6.5 to 8.5V	870
X	X	X	9.5 to 12V	960

Where:
X = connection closed; O = connection open.
*When switch (S1) is closed, the delay time is increased by 45ns.

APPLICATION INFORMATION



NOTES:
1. Residual carrier reduced to $20mV_{P-P}$ (R = 1kΩ, C = 100pF).
2. Switching sequence for delay times shown in Table 1.
3. R_{14-18} = 1.2kΩ for TDA4565.

Figure 1. Application Diagram and Test Circuit

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Signetics

TDA4570
NTSC Color Difference Decoder

Product Specification

Linear Products

DESCRIPTION

The TDA4570 is a monolithic, integrated NTSC decoder for NTSC television receivers, which is decoder for NTSC television receivers, which is pin-sequence compatible with multistandard decoder TDA4555.

It can be used in applications with 3.58MHz subcarrier frequency as well as in applications with 4.43MHz subcarrier frequency.

FEATURES

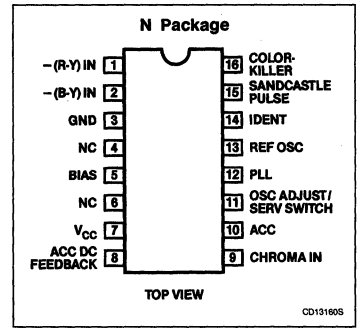
Chrominance part:

- **Gain-controlled amplifier with operating point control stage**
- **ACC (automatic chrominance control) with sampled rectifier during burst-key**
- **Blanking circuit for the color burst signal**
- **Voltage-controlled reference oscillator for double subcarrier frequency**
- **Divider stages which provide −(R-Y) and −(B-Y) reference signals with the correct 90° phase relation for the demodulators**
- **Phase comparator, which compares the −(R-Y) reference signal with the burst pulse and controls the frequency and phase of the reference oscillator**
- **Hue-control stage for phase-shifting via the combined service and hue-control input Pin 11**
- **Identification demodulator, which delivers a positive-going identification signal for NTSC signals at Pin 14; also used for the automatic color-killer**
- **Service switch with two functions. The first position ($V_{14-3} < 1V$) allows the adjustment of the reference oscillator; therefore, the color is switched on, the hue-control and the burst for the oscillator PLL is switched off. The second position ($V_{14-3} > 5V$) switches the color on, the hue-control is switched off, and the output signals can be observed**
- **Sandcastle pulse detector for burst gate, −line and +line vertical blanking pulse detection; the vertical part of the sandcastle pulse is needed for the internal color-on and color-off delay**
- **Pulse processing part which shall prevent a premature switching on of the color; the color-on delay, two or three field periods after identification of the NTSC signal, is achieved by a counter. The color is switched off immediately, or, at the latest, one field period after disappearance of the identification voltage**

Demodulator part:

- **Two synchronous demodulators for the (B-Y) and (R-Y) signals, which incorporate stages for blanking during line- and field-flyback**
- **Internal filtering of the residual carrier in the demodulated color difference signals**
- **Color switching stages controlled by the pulse processing part in front of the output stages**

PIN CONFIGURATION



- **−(B-Y) and −(R-Y) signal output stages; the output stages are low-resistance NPN emitter-followers**
- **Separate color switching output**

APPLICATIONS

- **Video processing**
- **TV receivers**
- **Graphic systems**

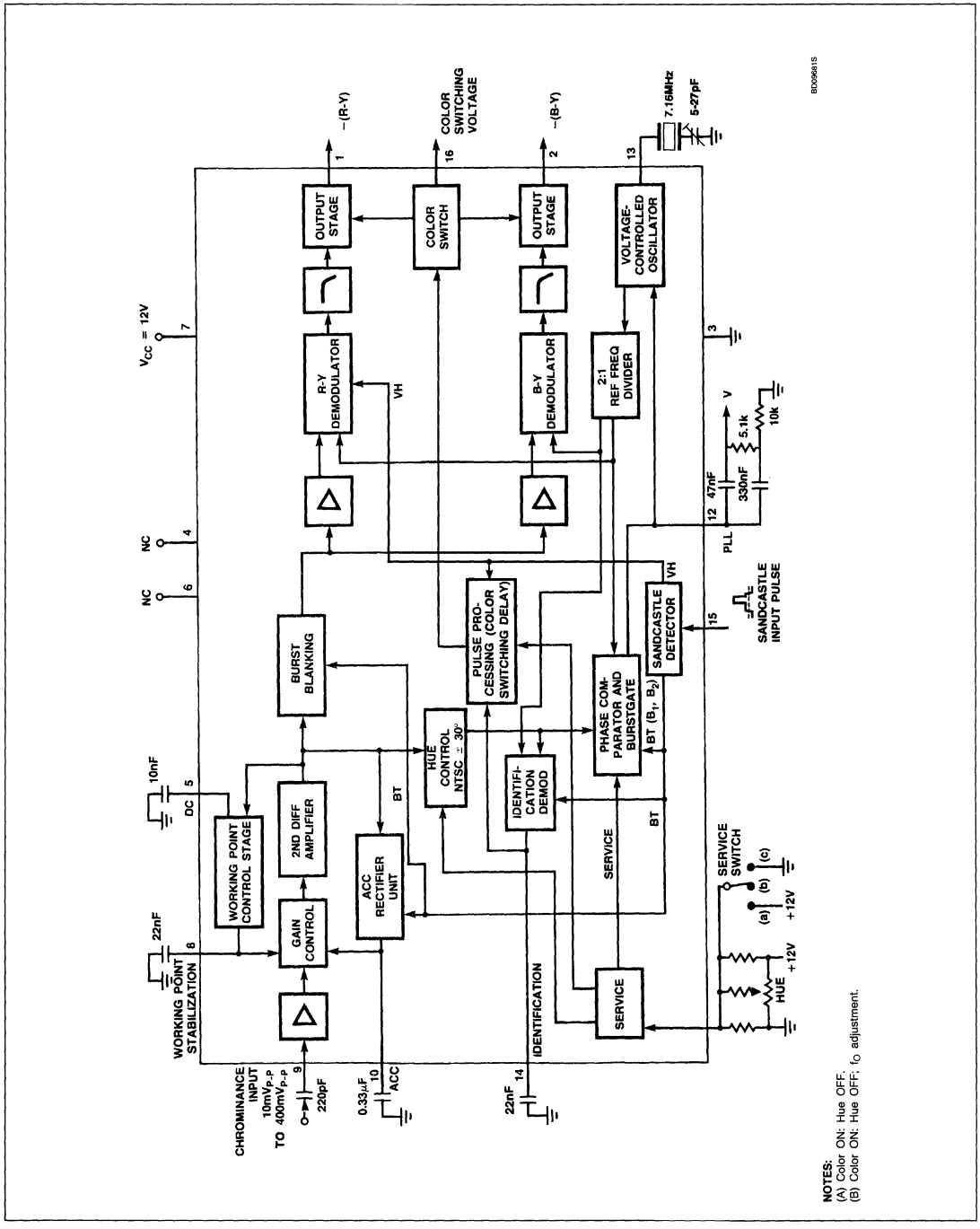
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to +70°C	TDA4570N

NTSC Color Difference Decoder

TDA4570

BLOCK DIAGRAM



NOTES:
(A) Color ON: Hue OFF.
(B) Color ON: Hue OFF; f_O adjustment.

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{7-3}$	Supply voltage range	10.8 to 13.2	V
	Currents		
$-I_{1,2}$	at Pins 1 and 2	5	mA
$-I_{16}$	at Pin 16	5	mA
θ_{JA}	Thermal resistance	80	°C/W
P_{TOT}	Total power dissipation	800	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 12V$; $T_A = 25°C$; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_7	Supply current		50		mA
Chrominance part					
$V_{9-3(P-P)}$	Input voltage range (peak-to-peak value)	10		400	mV
$V_{9-3(P-P)}$	Nominal input voltage (peak-to-peak values) with 75% color bar signal		100		mV
Z_{9-3}	Input impedance		3.3		kΩ
C_{9-3}	Input capacitance		4		pF
Oscillator and control voltage part					
f_O	Oscillator frequency for subcarrier frequency of 3.58MHz		7.16		MHz
R_{13-3}	Input resistance		350		Ω
Δf	Catching range (depending on RC network between Pins 12 and 3)	±300			Hz
	Control voltage				
V_{14-3}	without burst signal		6		V
V_{14-3}	color switching threshold		6.6		V
V_{14-3}	hysteresis of color switching		150		mV
t_D ON	Color-on delay			3	Field period
t_D OFF	Color-off delay			1	Field period
	Color-switching output (open NPN emitter)				
$-I_{16}$	output current			5	mA
V_{16-3}	color-on voltage		6		V
V_{16-3}	color-off voltage		0		V
Hue control and service switches					
ϕ	Phase shift of reference carrier relative to the input signal $V_{11-3} = 3V$	−5	0	5	Degree
	Phase shift of reference carrier relative to phase				
$-\phi$	at $V_{11-3} = 3V$ $V_{11-3} = 2V$	30			Degree
ϕ	$V_{11-3} = 4V$	30			Degree
	Internal source (open pin)		3		V
V_{11-3}	First service position (PLL is inactive for oscillator adjustment, color ON, hue OFF)	0		1	V
V_{11-3}	Second service position (color ON; hue OFF)	5		V_{CC}	V

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C; measured in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Demodulator part					
	Color difference output signals (peak-to-peak value)				
$V_{1-3(P-P)}$	– (R-Y) signal	0.84	1.05	1.32	V
$V_{2-3(P-P)}$	– (B-Y) signal	1.06	1.33	1.67	V
$\frac{V_{1-3}}{V_{2-3}}$	Ratio of color difference output signals (R-Y)/(B-Y)	0.71	0.79	0.87	
$V_{1,\,2-3}$	DC voltage at color difference outputs		7.7		V
	Residual carrier at color difference outputs				
$V_{1,\,2-3(P-P)}$	(1 × subcarrier frequency)			20	mV
$V_{1,\,2-3(P-P)}$	(2 × subcarrier frequency)			30	mV
Sandcastle pulse detector					
The sandcastle pulse is compared to three internal threshold levels, which are proportional to the supply voltage.					
	Thresholds:				
V_{15-3}	Field- and line-pulse separation; pulse on	1.3	1.6	1.9	V
$V_{15-3(P-P)}$	Required pulse amplitude	2	2.5	3	V
V_{15-3}	Line-pulse separation; pulse on	3.3	3.6	3.9	V
$V_{15-3(P-P)}$	Required pulse amplitude	4.1	4.5	4.9	V
V_{15-3}	Burst-pulse separation; pulse on	6.6	7.1	7.6	V
$V_{15-3(P-P)}$	Required pulse amplitude	7.7			V
V_{15-3}	Input voltage during horizontal scanning			1.1	V
$-I_{15}$	Input current			100	μA

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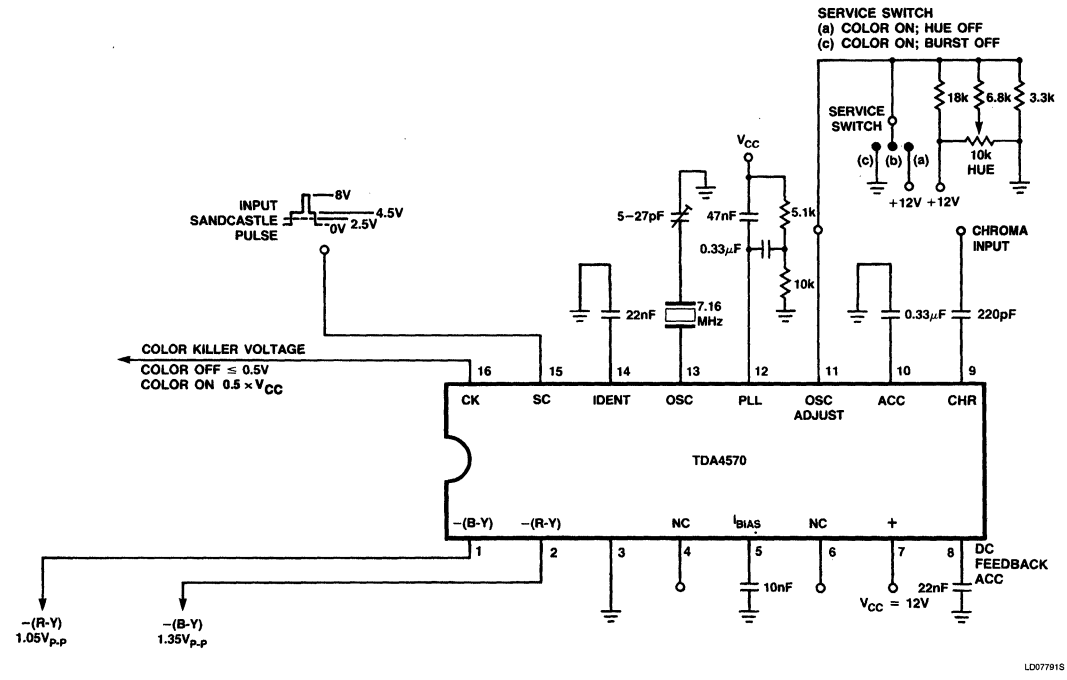
NTSC Color Difference Decoder TDA4570



NOTE:
Crystal frequency = 7.16MHz; resonance resistance 60Ω; load capacitance 20pF, dynamic capacitance 22pF and static capacitance 5.5pF.

Figure 1

Signetics

TDA4580

Video Control Combination Circuit With Automatic Cut-Off Control

Linear Products

Product Specification

DESCRIPTION

The TDA4580 is a monolithic integrated circuit which performs video control functions in television receivers with a color difference interface. For example, it operates in conjunction with the multi-standard color decoder TDA4555. The required input signals are: luminance and negative color difference -(R-Y) and -(B-Y), and a 3-level sandcastle pulse for control purposes. Analog RGB signals can be inserted from two sources, one of which has full performance adjustment possibilities. RGB output signals are available for driving the video output stages. This circuit provides automatic cut-off control of the picture tube.

FEATURES

- **Capacitive coupling of the color difference, luminance, and RGB input signals with black level clamping**
- **Two sets of analog RGB inputs via fast switch 1 and fast switch 2**
- **First RGB inputs and fast switch 1 in accordance with peritelevision connector specification**
- **Saturation, contrast, and brightness control acting on first RGB inputs**
- **Brightness control acting on second RGB inputs**
- **Equal black levels for television and inserted signals**
- **Clamping, horizontal and vertical blanking, and timing of automatic cut-off, controlled by a 3-level sandcastle pulse**
- **Automatic cut-off control with compensation for leakage current of the picture tube**
- **Measuring pulses of cut-off control start immediately after end of vertical part of sandcastle pulse**
- **Three selectable blanking intervals for PAL, SECAM, and NTSC/PAL-M**
- **Two switch-on delays for run-in without discoloration**
- **Adjustable peak drive limiter**
- **Average beam current limiter**
- **G-Y and RGB matrix coefficients selectable for PAL/SECAM and NTSC (correction for FCC primaries)**
- **Bandwidth 10MHz (typ.)**
- **Emitter-follower outputs for driving the RGB output stages**

APPLICATIONS

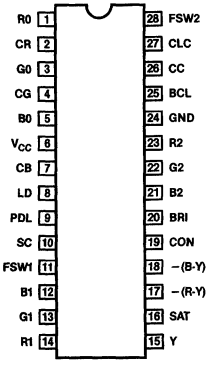
- **Video processing**
- **TV receivers**
- **Projection TV**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP, (SOT-117)	0 to 70°C	TDA4580N

PIN CONFIGURATION

N Package



TOP VIEW

CD12030S

PIN NO.	SYMBOL	DESCRIPTION
1	R0	Red output
2	CR	Red storage capacitor for cut-off control
3	G0	Green output
4	CG	Green storage capacitor for cut-off control
5	B0	Blue output
6	V_{CC}	Positive supply voltage (+12V)
7	CB	Blue storage capacitor for cut-off control
8	LD	PAL/NTSC matrix and blanking time level detector input
9	PDL	Peak drive limiting input
10	SC	Sandcastle pulse input
11	FSW1	Fast switch 1 for Y, CD, and RGB inputs
12	B1	Blue input (external signal)
13	G1	Green input (external signal)
14	R1	Red input (external signal)
15	Y	Luminance input
16	SAT	Saturation control input
17	-(R-Y)	Color difference input -(R-Y)
18	-(B-Y)	Color difference input -(B-Y)
19	CON	Contrast control input
20	BRI	Brightness control input
21	B2	Teletext blue input
22	G2	Teletext green input
23	R2	Teletext red input
24	GND	Ground
25	BCL	Average beam current limiting input
26	CC	Automatic cut-off control input
27	CLC	Storage capacitor for leakage current
28	FSW2	Fast switch 2 for teletext inputs

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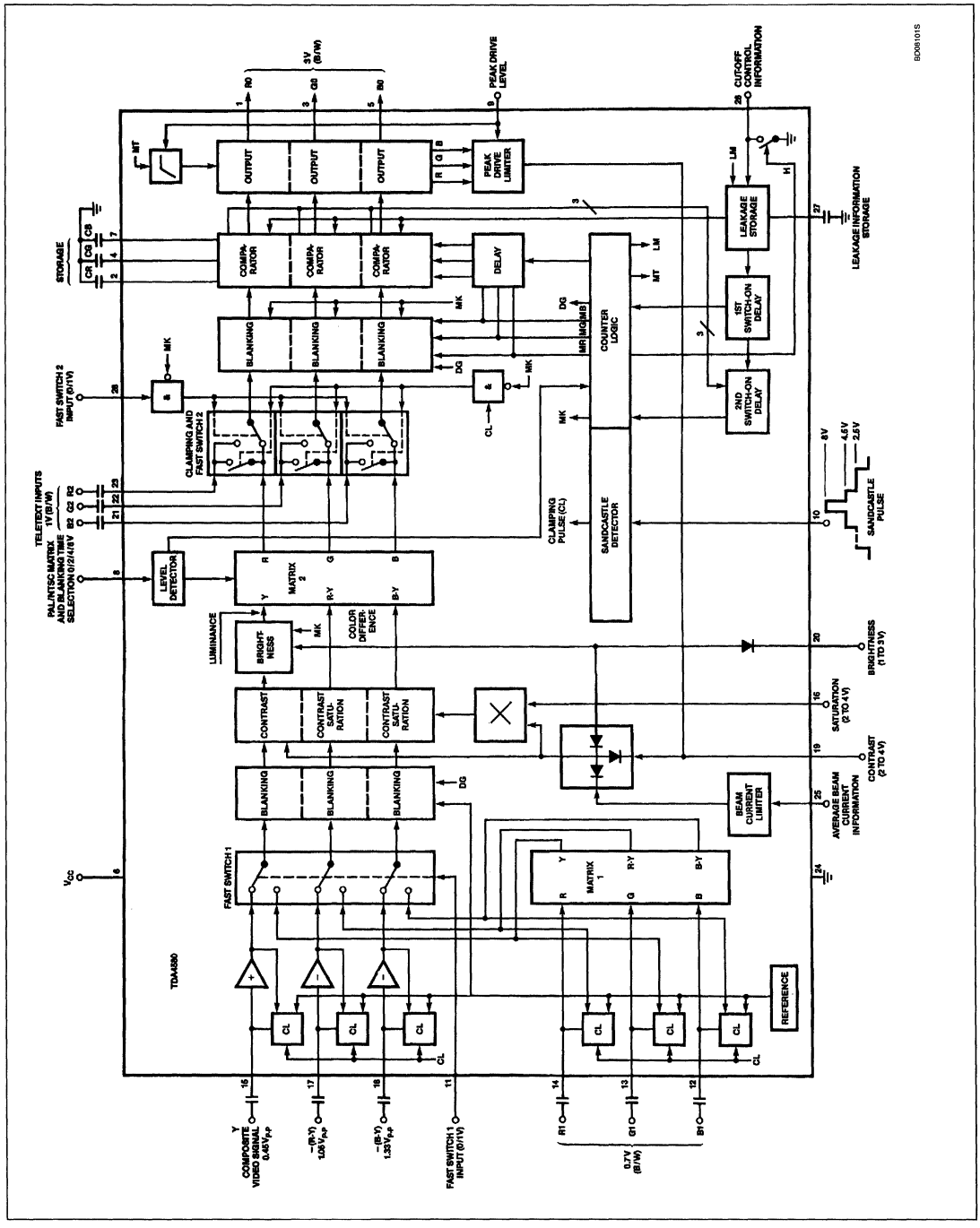
Video Control Combination Circuit With Automatic Cut-Off Control

TDA4580

BLOCK DIAGRAM



Video Control Combination Circuit With Automatic Cut-Off Control

TDA4580

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC} = V_{6-24}$	Supply voltage range (Pin 6)	0 to 13.2	V
V_{n-24}	Voltage range at Pins 2, 4, 7, 9, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 25, 27 to Pin 24 (ground)	0 to V_{CC}	V
	Voltage ranges		
$V_{8, 11, 28-24}$	at Pins 8, 11, 28	−0.5 to V_{CC}	V
V_{10-24}	at Pin 10	0 to V_{CC}+0.7	V
V_{26-24}	at Pin 26	−0.7 to V_{CC}+0.7	V
	Currents		
$-I_{1, 3, 5(AV)}$	at Pins 1, 3, 5 (average)	3	mA
$-I_{1, 3, 5(M)}$	at Pins 1, 3, 5 (peak)	10	mA
$I_{19(AV)}$	at Pin 19 (average)	5	mA
I_{26}	at Pin 26	1	mA
P_{TOT}	Total power dissipation	2	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C
θ_{JA}	Thermal resistance from junction to ambient	37	°C /W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V; T_A = 25°C; measured in a circuit similar to Figure 2 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to Pin 24 (ground), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 6)					
$V_{CC} = V_{6-24}$	Supply voltage range	10.8		13.2	V
$I_{CC} = I_6$	Supply current		110		mA
Color difference inputs (Pins 17 and 18)					
$V_{17-24(P-P)}$	−(R − Y) input signal at Pin 17 (peak-to-peak value)[1, 2]		1.05		V
$V_{18-24(P-P)}$	−(B − Y) input signal at Pin 18 (peak-to-peak value)[1, 2]		1.33		V
$\|I_{17, 18}\|$	Input current during scanning			0.3	μA
$R_{17, 18}$	Input resistance	5			MΩ
$V_{17, 18-24}$	Internal DC bias voltage during clamping time		7.5		V
Luminance input (Pin 15)[2]					
$V_{15-24(P-P)}$	Composite video input signal (VBS) (peak-to-peak value)		0.45		V
$\|I_{15}\|$	Input current during scanning			0.3	μA
R_{15}	Input resistance	5			MΩ
V_{15-24}	Internal DC bias voltage during clamping time		7.4		V
Signal switch 1 input (Pin 11)					
V_{11-24}	Input voltage level for insertion of Y and CD signals			0.4	V
V_{11-24}	RGB1 signals	0.9		3.0	V
R_{11}	Internal resistor to ground		10		kΩ

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DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C; measured in a circuit similar to Figure 2 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to Pin 24 (ground), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
RGB1 inputs (R1 Pin 14, G1 Pin 13, B1 Pin 12) (signals controlled by saturation, contrast, and brightness)[2]					
$V_{12, 13, 14-24}$	Input signal (black to white value)		0.7		V
$\|I_{12, 13, 14}\|$	Input current during scanning			0.3	μA
$R_{12, 13, 14}$	Input resistance	5			MΩ
$V_{12, 13, 14-24}$	Internal DC bias voltage during clamping time		8.2		V
RGB/Y, (R – Y), (B – Y) — Matrix					
Matrixed according to the equations $V_{(R-Y)} = 0.7\ V_R - 0.59\ V_G - 0.11\ V_B$ $V_{(B-Y)} = -0.3\ V_R - 0.59\ V_G + 0.89\ V_B$ $V_{(Y)} = 0.3\ V_R + 0.59\ V_G + 0.11\ V_B$					
Contrast control input (Pin 19) (contrast control acts on Y and CD signals or RGB1 signals, respectively)[3]					
V_{19-24}	Maximum contrast		4		V
V_{19-24}	Nominal contrast (6dB below maximum)		3		V
	Attenuation of contrast at V_{19-24} = 2V (related to maximum)		22		dB
$-I_{19}$	Input current at V_{19-24} = 2 to 4V			3	μA
Peak drive limiting input (Pin 9)[4]					
V_{9-24}	Internal DC bias voltage		9		V
R_9	Input resistance at $V_{9-24} > 9V$		10		kΩ
I_{19}	Control current into contrast input (Pin 19) during peak drive $V_{1, 2, \text{ or } 3-24} > V_{9-24}$		20		mA
Average beam current limiting input (Pin 25)[5]					
V_{25-24}	Start of contrast reduction at maximum contrast setting		8.5		V
ΔV_{25-24}	Input range for full contrast reduction		1.0		V
R_{25}	Input resistance at $V_{25-24} < 6V$		2.2		kΩ
Saturation control input (Pin 16) (saturation control acts on CD signals or RGB1 signals, respectively)					
V_{16-24}	Maximum saturation		4		V
V_{16-24}	Nominal saturation (6dB below maximum)		3		V
	Attenuation of saturation at V_{16-24} = 1.8V (related to maximum at 100kHz)	50			dB
I_{16}	Input current at V_{16-24} = 1.8 to 4V			10	μA
Brightness control input (Pin 20)[6, 7]					
V_{20-24}	Control voltage range	1		3	V
$-I_{20}$	Input current at V_{20-24} = 1 to 3V			10	μA
V_{20-24}	Control voltage for nominal brightness		2.2		V
	Change of black level in the control range related to the nominal output signal (black/white) for ΔV_{20-24} = 1V		33		%
V_{20-24}	Signal switched off and black level equal to cut-off level	11.5			V

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C; measured in a circuit similar to Figure 2 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to Pin 24 (ground), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Y, (R-Y), (B-Y)/RGB-Matrix[8]					
	PAL matrix (V_{8-24} = ⩽4.5V)				
	Matrixed according to the equation $V_{(G-Y)} = -0.51V_{(R-Y)} - 0.19V_{(B-Y)}$				
	NTSC matrix (V_{8-24} = ⩾5.5V)				
	(Adaption for NTSC-FCC primaries, nominal hue control set on −5°C)				
	Matrixed according to the equation $V_{(G-Y)}{}^{8} = -0.43V_{(R-Y)} - 0.11V_{(B-Y)}$ $V_{(R-Y)}{}^{8} = 1.57V_{(R-Y)} - 0.41V_{(B-Y)}$ $VI_{(B-Y)}{}^{8} = V_{(B-Y)}$				
RGB2 inputs (Teletext) (R2 Pin 23, G2 Pin 22, B2 Pin 21)[2]					
	(RGB signals controlled by brightness control)				
$V_{21, 22, 23-24}$	Input signal for 100% output signals (black to white value)		1		V
$I_{21, 22, 23}$	Input current during scanning			0.3	μA
$I_{21, 22, 23}$	Input resistance	5			MΩ
Signal switch 2 input (Pin 28)					
	Input voltage level for insertion of Y, CD signals or RGB1 signals, respectively				
V_{28-24} V_{28-24}	RGB signals from matrix[9] RGB2 signals[9]	 0.9		0.4 3.0	V V
R_{28-24}	Internal resistor to ground		10		kΩ
Automatic cut-off control input (Pin 26) (Leakage current measuring time and insertion of RGB cut-off measuring lines — see Figure 3; types of ultra-black level — see Figure 1.)[10]					
V_{26-24}	Allowed maximum external DC bias voltage	5.5			V
ΔV_{26-24}	Voltage difference between cut-off current measurement and leakage current measurement		0.5		V
$V_{1, 3, 5-24}$	Warm-up test pulse		$V_{9-24}{}^{8}$		V
V_{26-24}	Threshold for warm-up detector		8		V
Storage input for leakage current (Pin 27)					
R_{27}	Internal resistance during leakage current measuring time (current limiting at I_{27} = 0.2mA)		400		Ω
$\lvert I_{27} \rvert$	Input current except during cut-off control cycle			0.5	μA
Storage inputs for automatic cut-off control (Pins 2, 4, 7)					
$\lvert I_{2, 4, 7} \rvert$	Charge and discharge currents		0.3		mA
$\lvert I_{2, 4, 7} \rvert$	Input currents of storage inputs out of control time			0.1	μA

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DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; T_A = 25°C; measured in a circuit similar to Figure 2 at nominal settings (saturation, contrast, brightness), no beam current or peak drive limiting; all voltages with respect to Pin 24 (ground), unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Switch input for PAL/NTSC matrix and vertical blanking time (Pin 8)[11]					
	Switching voltage input for PAL matrix and vertical blanking period of				
V_{8-24}	25 lines		0	0.5	V
V_{8-24}	22 lines	1.5	2	2.5	V
V_{8-24}	18 lines	3.5	4	4.5	V
V_{8-24}	NTSC matrix and vertical blanking period of 18 lines	5.5	6	12	V
I_8	Input current			50	μA
Sandcastle pulse detector (Pin 10)[12]					
	The following amplitudes are required for separating the various pulses:				
V_{10-24}	horizontal and vertical blanking pulses	2.0	2.5	3.0	V
V_{10-24}	horizontal pulses for counter logic	4.0	4.5	5.0	V
V_{10-24}	clamping pulses	7.5			V
t_D	delay of leading edge of clamping pulse		1		μs
$-I_{10}$	Input current at V_{10-24} = 0V			100	μA
Outputs for positive RGB signals (R0 Pin 1, G0 Pin 3, B0 Pin 5)[13]					
$V_{1, 3, 5-24}$	Nominal signal amplitude (black/white)		3		V
	Spreads between channels			10	%
$V_{1, 3, 5-24}$	Maximum signal amplitude (black/white)	4			V
$I_{1, 3, 5}$	Internal current source		3		mA
$R_{1, 3, 5}$	Output resistance		160	220	Ω
$V_{1, 3, 5-24}$	Minimum output voltage		1		V
$V_{1, 3, 5-24}$	Maximum output voltage		10		V
	Horizontal and vertical blanking to ultra-black level 2, related to nominal signal black level in percentage of nominal signal amplitude	45	55		%
	Vertical blanking to ultra-black level 1, related to cut-off measuring level in percentage of nominal signal amplitude	25	35		%
	Recommendation: Range for cut-off measuring level 1.5 to 5.0V; nominal value at 3V[14]				
Gain data[15]					
d	Frequency response of Y path (0 to 8MHz) Pins 1, 3, and 5 to Pin 15			3	dB
d	Frequency response of CD path (0 to 8MHz) Pin 1 to Pin 17 = Pin 5 to Pin 18			3	dB
d	Frequency response of RGB1 path (0 to 8MHz) Pin 1 to Pin 14 = Pin 3 to Pin 13 = Pin 5 to Pin 12			3	dB
d	Frequency response of RGB2 path (0 to 10MHz) Pin 1 to Pin 23 = Pin 3 to Pin 22 = Pin 5 to Pin 21			3	dB

Video Control Combination Circuit With Automatic Cut-Off Control

TDA4580

NOTES:

1. The value of the color difference input signals, $-(B-Y)$ and $-(R-Y)$, is given for saturated color bar with 75% of maximum amplitude.
2. Capacitive coupled to a low ohmic source; recommended value 600Ω (maximum).
3. At Pin 19 for $V_{19-24} \leqslant 2.0V$, no further decrease of contrast is possible.
4. The peak drive limiting of output signals is achieved by contrast reduction. The limiting level of the output signals is equal to the voltage V_{9-24}, adjustable in the range 5 to 11V. After exceeding the adjusted limiting level at peak drive, limiter will not be active during the first line.
5. The average beam current limiting acts on contrast and at minimum contrast on brightness (the external contrast voltage at Pin 19 is not affected).
6. At nominal brightness the black level at the output is 0.3V (≈ −10% of nominal signal amplitude) below the measuring level.
7. The internal control voltage can never be more positive than 0.7V above the internal contrast voltage.
8. Matrix equation

$V_{(R-Y)}$, $V_{(B-Y)}$	: output of NTSC decoder of PAL type demodulating axis and amplitudes
$V_{(G-Y)}{}^*$, $V_{(R-Y)}{}^*$, $V_{(B-Y)}{}^*$	: for NTSC modified CD signals; equivalent to demodulation with the following axes and amplification factors:
$(B-Y)^*$ demodulator axis	0°
$(R-Y)^*$ demodulator axis	115° (PAL 90°)
$(R-Y)^*$ amplification factor	1.97 (PAL 1.14)
$(B-Y)^*$ amplification factor	2.03 (PAL 2.03)

$V_{(G-Y)}{}^* = -0.27V_{(R-Y)}{}^* - 0.22V_{(B-Y)}{}^*$.

9. During clamping time, in each channel the black level of the inserted signal is clamped on the black level of the internal signal behind the matrix (dependent on brightness control).
10. During warm-up time of the picture tube, the RGB outputs (Pins 1, 3, and 5) are blanked to minimum output voltage. An inserted white pulse during the vertical flyback is used for beam current detection. If the beam current exceeds the threshold of the warm-up detector at Pin 26, the cut-off current control starts operating, but the video signal is still blanked. After run-in of the cut-off current control loop, the video signal will be released. The first measuring pulse occurs in the first complete line after the end of the vertical part of the sandcastle pulse. The absolute minimum vertical part must contain 9 line-pulses. The cycle time of the counter is 63 lines. When the vertical pulse is longer than 61 lines, the IC is reset to the switch-on condition. In this event the video signal is blanked and the RGB outputs are blanked to minimum output voltage as during warm-up time. During leakage current measurement, all three channels are blanked to ultra-black level 1. With the measuring level only in the controlled channel, the other two channels are blanked to ultra-black level 1. The brightness control shifts both the signal black level and the ultra-black level 2. The brightness control is disabled from line 4 to the end of the last measuring line (see Figure 1).
    With the most adverse conditions (maximum brightness and minimum black level 2) the blanking level is located 30% of nominal signal amplitude below the cut-off measuring level.
11. The given blanking times are valid for the vertical part of the sandcastle pulse of 9 to 15 lines. If the vertical part is longer and the cut-off lines are outside the vertical blanking period of 18, 22, or 25 lines, respectively, the blanking of the signal ends with the end of the last of the three cut-off measuring pulses as shown in Figure 3.
12. The sandcastle pulse is compared with three internal thresholds (proportional to V_{CC}) to separate the various pulses. The internal pulses are generated when the input pulse at Pin 10 exceeds the thresholds. The thresholds are for:
    - Horizontal and vertical blanking $V_{10-24} = 1.5V$
    - Horizontal pulse $V_{10-24} = 3.5V$
    - Clamping pulse $V_{10-24} = 7.0V$
13. The outputs at Pins 1, 3, and 5 are emitter-followers with current sources and emitter protection resistors.
14. The value of the cut-off control range for the positive RGB output signals is given for a nominal output signal. If the signal amplitude is reduced, the cut-off range can be increased.
15. The gain data is given for a nominal setting of the contrast and saturation controls, measured without load at the RGB outputs (Pins 1, 3, and 5).

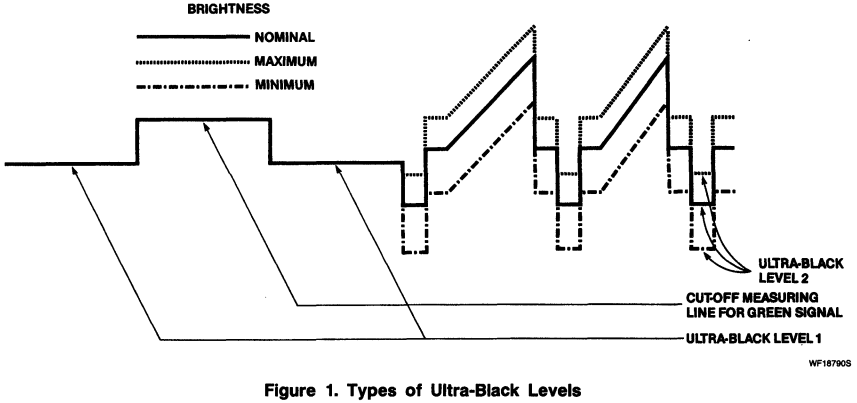

Figure 1. Types of Ultra-Black Levels

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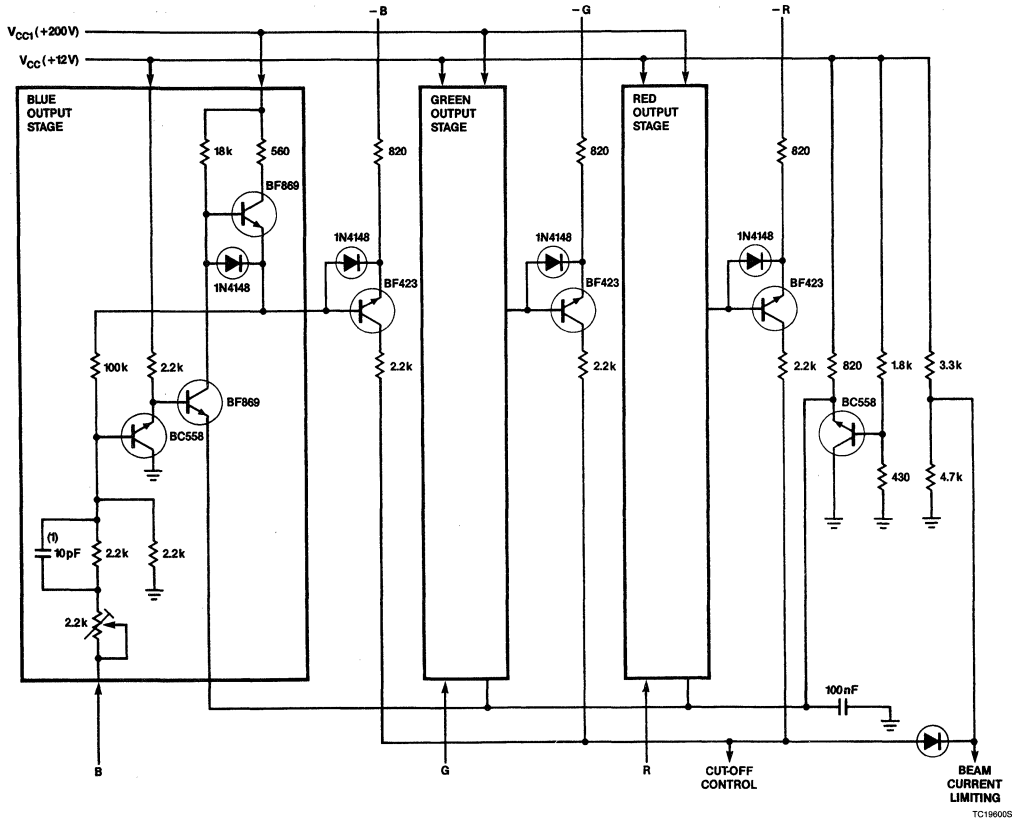
Video Control Combination Circuit With Automatic Cut-Off Control

TDA4580



NOTE:
1. Capacitor value depends on circuit layout.

Figure 2a. Part of Typical Application Circuit Diagram Using the TDA4580; Continued in Figure 2b

Video Control Combination Circuit With Automatic Cut-Off Control

TDA4580

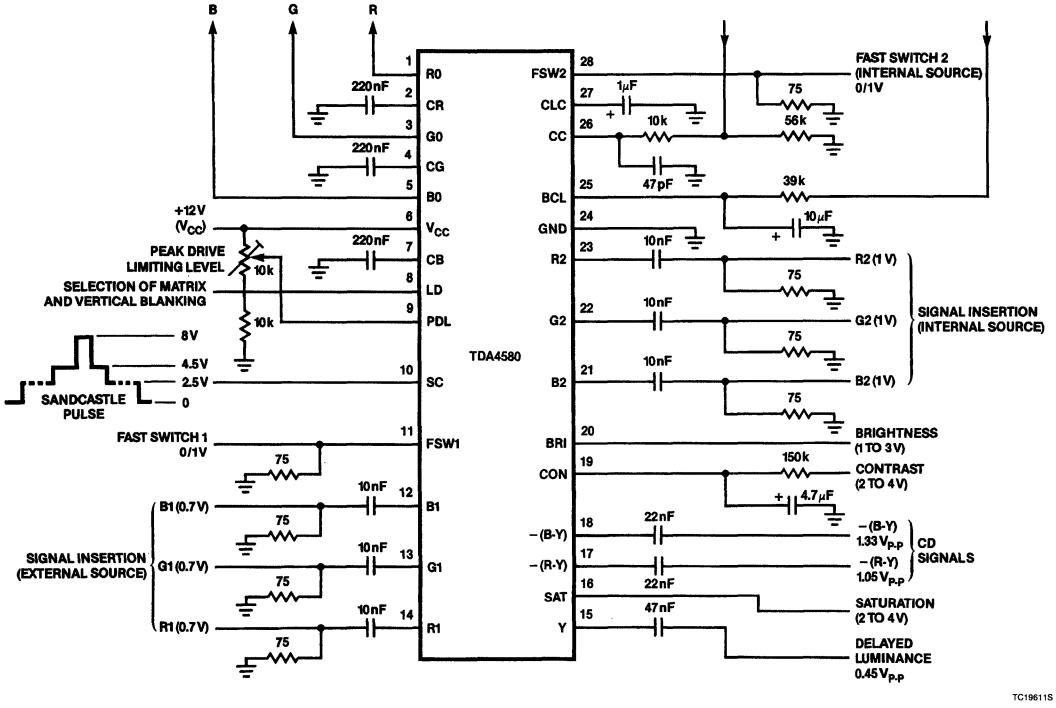


Figure 2b. Part of Typical Application Circuit Diagram Using the TDA4580; Continued from Figure 2a

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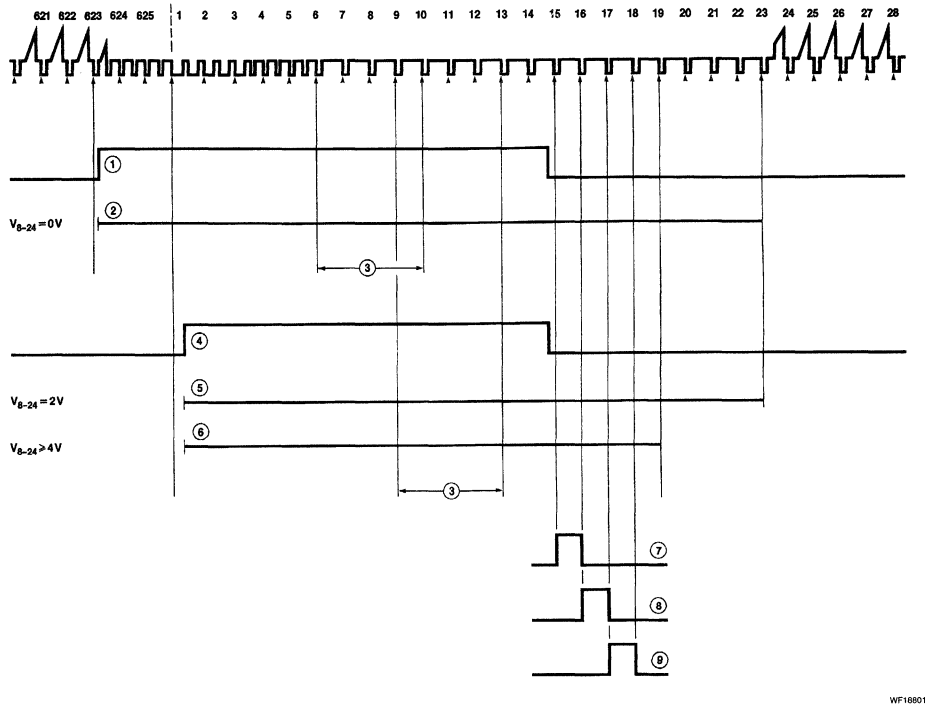


NOTES:
1. Vertical part of sandcastle pulse starts with equalizing pulses and ends with flyback.
2. Blanking period of 25 complete lines.
3. Leakage measuring period (LM).
4. Vertical part of sandcastle pulse starts and ends with flyback.
5. Blanking period of 22 complete lines.
6. Blanking period of 18 complete lines.
7. Cut-off measuring line for red signal (MR).
8. Cut-off measuring line for green signal (MG).
9. Cut-off measuring line for blue signal (MB).

Figure 3. Blanking and Measuring Lines

Signetics

TDA8442
Quad DAC With I²C Interface

Product Specification

Linear Products

DESCRIPTION

The TDA8442 consists of four 6-bit D/A converters and 3 output ports. This IC was designed to provide I²C control, by replacing the potentiometers, for the TDA3560-series single-chip color decoders. Control of the IC is performed via the two-line, bidirectional I²C bus.

FEATURES

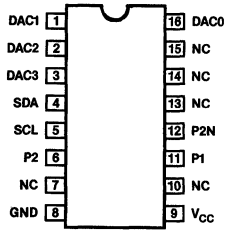
- **6-bit resolution**
- **3 output ports**
- **I²C control**

APPLICATIONS

- **I²C interface control**
- **System control**
- **Switching**

PIN CONFIGURATION

N Package



TOP VIEW

CD12850S

PIN NO.	SYMBOL	DESCRIPTION
1	DAC1	Analog output 1
2	DAC2	Analog output 2
3	DAC3	Analog output 3
4	SDA	Serial data line } I²C bus
5	SCL	Serial clock line } I²C bus
6	P2	Port 2 NPN collector output with internal pull-up resistor
7	NC	Not connected
8	GND	Supply return (ground)
9	V_{CC}	Positive supply voltage
10	NC	Not connected
11	P1	Port 1 open NPN emitter output
12	P2N	Inverted P2 output
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	DAC0	Analog output 0

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−20°C to +70°C	TDA8442N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range (Pin 9)	−0.3 to +13.2	V
	Input/output voltage ranges		
V_{SDA}	(Pin 4)	−0.3 to +13.2	V
V_{SCL}	(Pin 5)	−0.3 to +13.2	V
V_{CC2}	(Pin 6)	−0.3 to V_{CC}[1]	V
V_{CC2N}	(Pin 12)	−0.3 to V_{CC}[1]	V
V_{CC1}	(Pin 11)	−0.3 to V_{CC}[1]	V
V_{DAX}	(Pins 1 to 3 and Pin 16)	−0.3 to V_{CC}[1]	V
P_{TOT}	Total power dissipation	1	W
T_A	Operating ambient temperature range	−20 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Pin voltage may exceed V_{CC} if the current in that pin is limited to 10mA.

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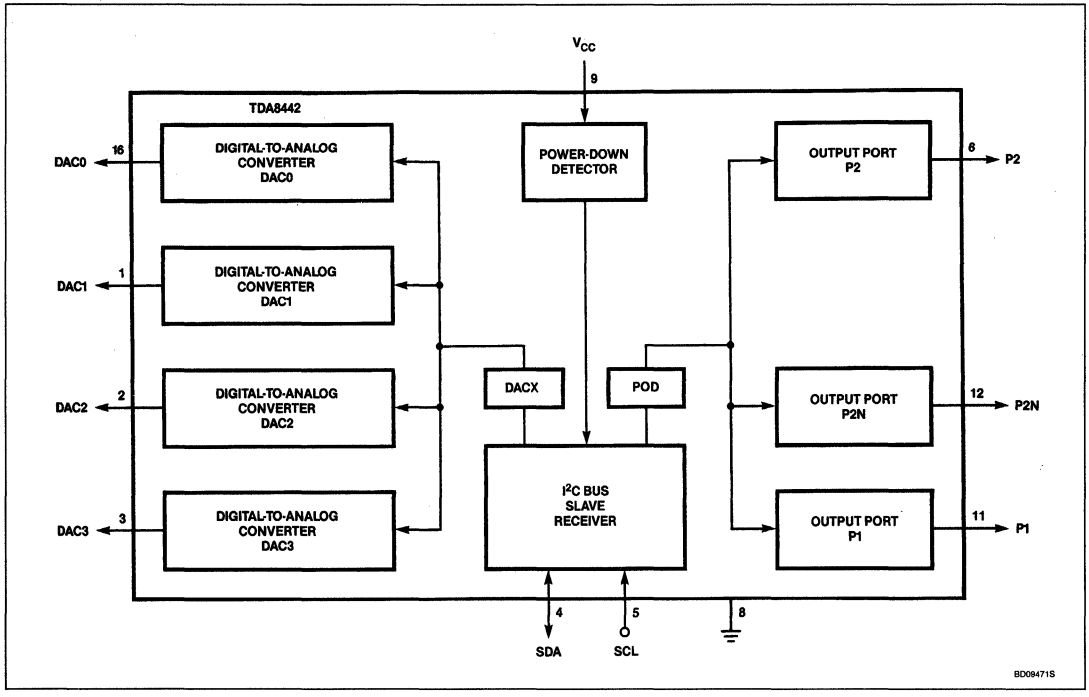
BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supplies					
V_{CC}	Supply voltage (Pin 9)	10.8	12	13.2	V
I_{CC}	Supply currents (no outputs loaded) (Pin 9)		12		mA
I²C bus inputs SDA (Pin 4) and SCL (Pin 5)					
V_{IH}	Input voltage High[1]	3		$V_{CC}-1$	V
V_{IL}	Input voltage Low	−0.3		1.5	V
I_{IH}	Input current High[1]			10	μA
I_{IL}	Input current Low[1]			10	μA
I²C bus output SDA (Pin 4) (open-collector)					
V_{OL}	Output voltage Low at $I_{OL} = 3.0mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
Ports P2 and P2N (Pins 6 and 12) (NPN collector output with pull-up resistor to V_{CC})					
R_O	Internal pull-up resistor to V_{CC}	5	10	15	kΩ
V_{OL}	Output voltage Low at $I_{OL} = 2mA$			0.4	V
I_{OL}	Maximum output sink current	2	5		mA
Port P1 (Pin 11) (open NPN emitter output)					
I_{OH}	Output current High at $0 < V_O < V_{CC} - 1.5V$	14			mA
I_{OL}	Output leakage current at $0 < V_O < V_{CC}V$			100	μA
Digital-to-analog outputs Output DAC0 (Pin 16)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	3			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		100	mV
	Deviation from linearity			150	mV
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA
Output DAC1 (Pin 1)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	4			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1.7	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		120	mV
	Deviation from linearity			170	mV
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Output DAC2 (Pin 2)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	4			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1.7	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		120	mV
	Deviation from linearity			170	mV
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA
Output DAC3 (Pin 3)					
V_{OMAX}	Maximum output voltage (unloaded)[2]	10			V
V_{OMIN}	Minimum output voltage (unloaded)[2]			1	V
V_{OLSB}	Positive value of smallest step[2] (1 LSB)	0		350	mV
	Deviation from linearity			0.50	V
Z_O	Output impedance at $-2 < I_O < +2mA$			70	Ω
$-I_{OH}$	Maximum output source current	2		6	mA
I_{OL}	Maximum output sink current	2	8		mA
Power-down reset					
V_{CCD}	Maximum value of V_{CC} at which power-down reset is active	6		10	V
t_R	Rise time of V_{CC} during power-on (V_{CC} rising from 0V to V_{CCD})	5			μs

NOTES:
1. If $V_{CC} < 1V$, the input current is limited to 10μA at input voltages up to 13.2V.
2. Values are proportional to V_{CC}.

FUNCTIONAL DESCRIPTION

Control

Analog control is facilitated by four 6-bit digital-to-analog converters (DAC0 to DAC3). The values of the output voltages from the DACs are set via the I²C bus.

The high-current output port (P1) is suitable for switching between internal and external RGB signals. It is an open NPN emitter output capable of sourcing 14mA (minimum).

The two output ports (P2 and P2N) can be used for NTSC/PAL switching. These are NPN collector outputs with internal pull-up resistors of 10kΩ (typical). Both outputs are capable of sinking up to 2mA with a voltage drop of less than 400mV. If one output is programmed to be Low, the other output will be High, and vice versa.

Reset

The power-down reset mode occurs whenever the positive supply voltage falls below 8.5V (typical) and resets all registers to a defined state.

OPERATION

Write

The TDA8442 is controlled via the I²C bus. Programming of the TDA8442 is performed using the format shown in Figure 1.

Acknowledge (A) is generated by the TDA8442 only when a valid address is received and the device is not in the power-down reset mode (V_{CC} > 8.5V (typ)).

Control

Control is implemented by the instruction bytes POD (port output data) and DACX (digital-to-analog converter control), and the corresponding data/control bytes (see Figure 2).

POD Bit P1 — If a '1' is programmed, the P1 output is forced High. If a '0' is programmed, or after a power-down reset, the P1 output is Low (high-impedance state).

POD Bit P2/P2N — If a '1' is programmed, the P2 output goes High and the P2N output goes Low. If a '0' is programmed, and after a power-down reset, the P2 output is Low and the P2N output is High.

DAX Bits AX5 to AX0 — The digital-to-analog converter selected corresponds to the decimal equivalent of the two bits X1 and X0. The output voltage of the selected DAC is programmed using Bits AX5 to AX0, the lowest value being all AX5 to AX0 data at '0', or when power-down reset has been activated.

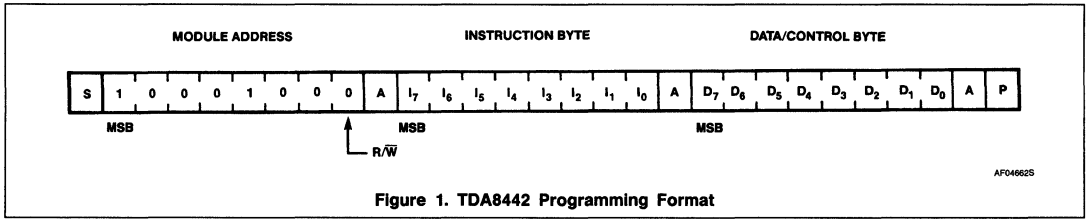

Figure 1. TDA8442 Programming Format

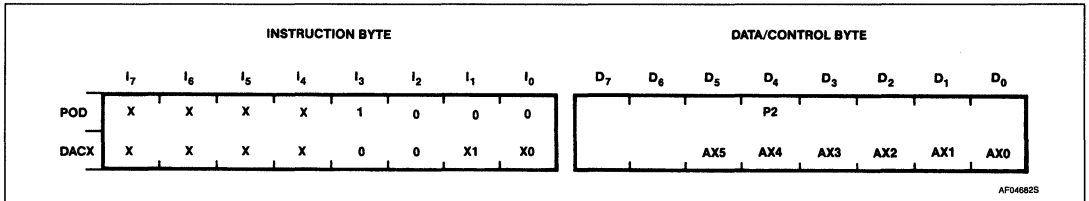

Figure 2. Control Programming

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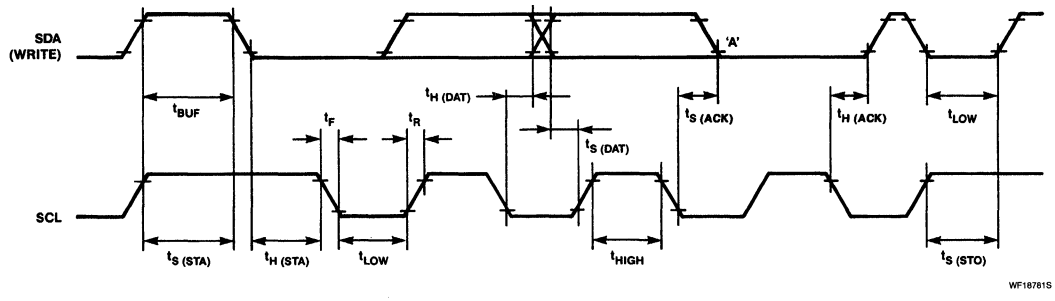
I²C BUS TIMING

Bus loading conditions: 4kΩ pull-up resistor to +5V; 200pF capacitor to GND.
All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			µs
t_{SU}, t_{STA}	Start condition setup time	4			µs
t_{HD}, t_{STA}	Start condition hold time	4			µs
t_{LOW}	Low period SCL, SDA	4			µs
t_{HIGH}	High period SCL	4			µs
t_R	Rise time SCL, SDA			1	µs
t_F	Fall time SCL, SDA			0.30	µs
t_{SU}, t_{DAT}	Data setup time (write)	0.25			µs
t_{HD}, t_{DAT}	Data hold time (write)	0			µs
t_{SU}, t_{ACK}	Acknowledge (from TDA8442) setup time			2	µs
t_{HD}, t_{ACK}	Acknowledge (from TDA8442) hold time	0			µs
t_{SU}, t_{STO}	Stop condition setup time	4			µs



NOTE:
Reference levels are 10 and 90%.

Figure 3. I²C Bus Timing, TDA8442

Signetics

TDA8443, TDA8443A
RGB/YUV Switch

Preliminary Specification

Linear Products

DESCRIPTION

The TDA8443/8443A is intended to be used in color TV sets which have more than one base-band video source. The IC has two sets of inputs. The first (Inputs 1) is intended for the internal video signals (R-Y), Y, (B-Y), and the associated synchronization pulse coming from the color decoder; the second (Inputs 2) is intended for external video signals R, G, B, and the associated synchronization pulse coming from the accessory inputs. The latter ones (Inputs 2) can also consist of the video signals (R-Y), Y, (B-Y), and the associated synchronization pulse. The RGB signals at Inputs 2 can also be matrixed internally into the luminance signal Y and the color-difference signals (R-Y) and (B-Y) before they become available at the outputs. By means of I^2C bus mode or manual control (control by DC voltages), one of these inputs can be selected and will be available at the outputs. The IC contains three pins for programming the sub-address; this means that within one TV set the system can be expanded up to seven ICs. The TDA8443 is designed to be used with the CCTV levels, while the TDA8443A is designed to be used for the standard decoder signal levels.

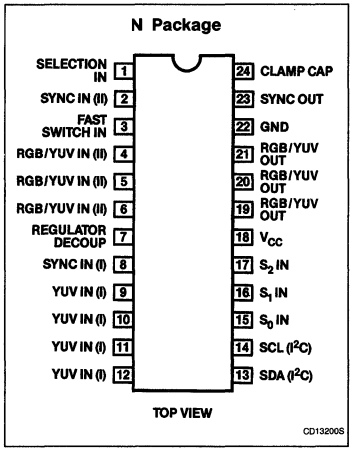
FEATURES

- **Two RGB/YUV selectable clamped inputs with associated sync**
- **An RGB/YUV matrix**
- **3-State switching with an OFF state**
- **Four amplifiers with selectable gain**
- **Fast switching to allow for mixed mode**
- **I^2C or non-I^2C mode (control by DC voltages)**
- **Slave receiver in the I^2C mode**
- **External OFF command**
- **System expansion possible up to 7 devices**

APPLICATIONS

- **TV receivers**
- **Video switching**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101)	0 to +70°C	TDA8443N
24-Pin Plastic DIP (SOT-101)	0 to +70°C	TDA8443AN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNIT
T_{STG}	Storage temperature range		−65 to +150	°C
T_A	Operating ambient temperature range		0 to +70	°C
V_{18-7}	Supply voltage		14	V
P_D	Total power dissipation			W
T_{JMAX}	Maximum junction temperature		125	°C
V_{SDA}	Input voltage range	Pin 13	−0.3 to 14	V
V_{SCL}		14	−0.3 to 14	V
		other pins	−0.3 to V_{CC}+0.3	V
I_{OMAX}	Maximum output current		TBD	mA

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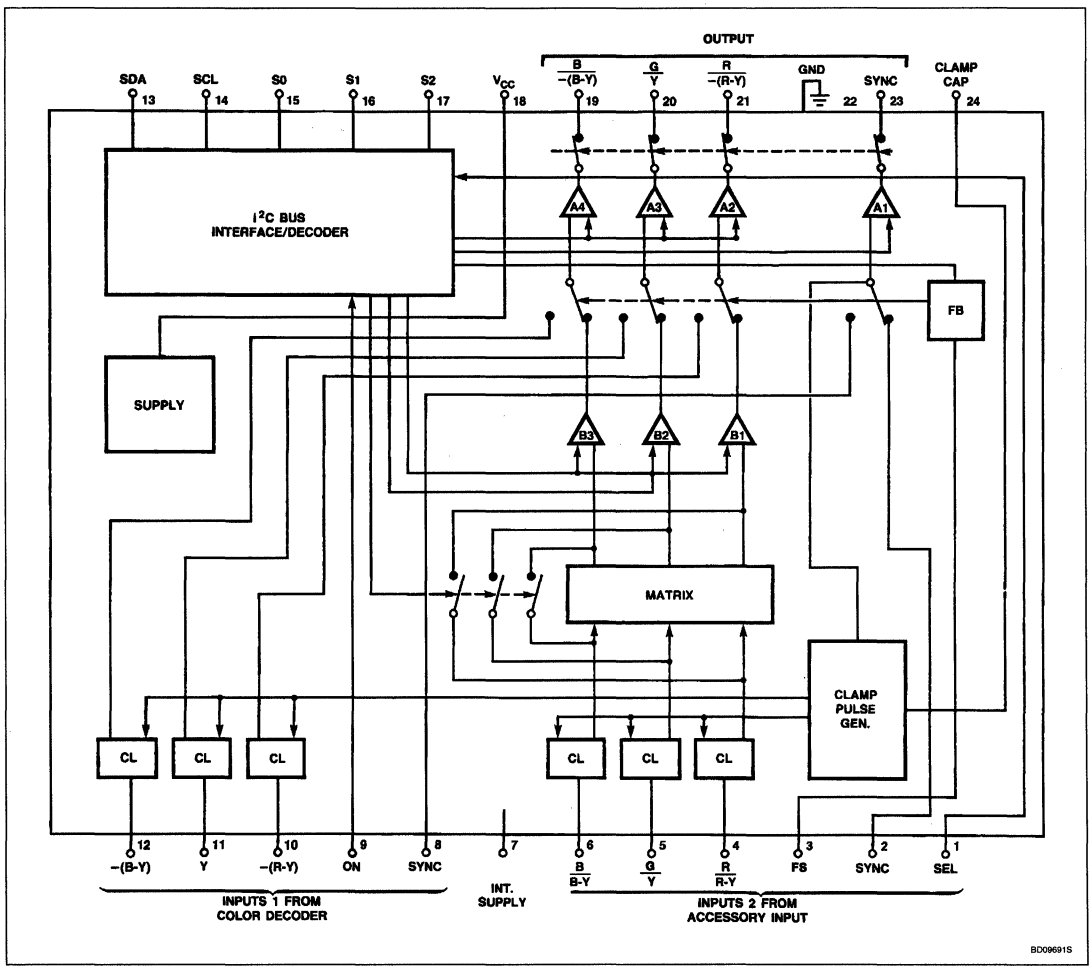
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{18-7}	Supply voltage	10		13.2	V
I_{18}	Supply current		TBF	TBF	mA
RGB/YUV channels					
	Absolute gain difference with respect to programmed value		0	10	%
	Relative gain difference between any 2 channels of one input		0	5	%
I_{IN}	Input current		TBF	0.3	μA
Z_{OUT}	Output impedance		TBF	30	Ω
	3dB bandwidth (mode 0 or 2)		10		MHz
	3dB bandwidth mode 1		10		MHz
	Mutual time difference at output if all inputs of one source are connected together		TBF	25	ns
	Maximum output amplitude of YUV signals	2.8			V_{P-P}
	Crosstalk between inputs of same source, at 5MHz[1]			−30	dB
	Crosstalk between different sources			−50	dB
	Isolation (OFF state) at 10MHz	50			dB
	Differential gain at nominal output signals: R-Y = $1.05V_{P-P}$ B-Y = $1.33V_{P-P}$ Y = $0.34V_{P-P}$			10	%
S/N	Signal-to-noise ratio at nominal input	50			dB
BW	Bandwidth = 5MHz[2]				
	Supply voltage rejection[3]	50			dB
	DC level of outputs during clamp		5.3		V
Sync channels					
	Gain difference with respect to programmed value			10	%
BW	3dB bandwidth		TBF		MHz
	Input amplitude of sync pulse for proper operation of clamp pulse generator	0.2		2.5	V_{P-P}
Z_{OUT}	Output impedance		TBF	30	Ω
	Maximum output amplitude (undistorted)	2.5			V_{P-P}
	DC level on top of sync pulse at output	TBF	1.8	TBF	V
I^2C bus inputs/outputs					
	SDA input (Pin 13)				
	SCL input (Pin 14)				
V_{IH}	Input voltage High	3		V_{CC}	V
V_{IL}	Input voltage Low	−0.3		1.5	V
I_{IH}	Input current High			10	μA
I_{IL}	Input current Low			10	μA
	SDA output (open-collector)				
V_{OL}	Output voltage Low at IO-L = 3mA			0.4	V
I_{OL}	Maximum output sink current		5		mA

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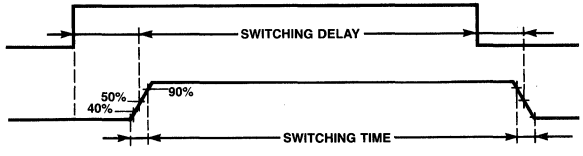
DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ and $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sub-address inputs S0 (Pin 15), S1 (Pin 16), S2 (Pin 17)					
V_{IH}	Input voltage High	3		V_{CC}	V
V_{IL}	Input voltage Low	−0.3		0.4	V
I_{IH}	Input current High			TBF	μA
I_{IL}	Input current Low			TBF	μA
Fast switching pin					
V_{3-7}	Input voltage High	1		3	V
V_{3-7}	Input voltage Low	−0.3		0.4	V
I_3	Input current High			TBF	μA
I_3	Input current Low			TBF	μA
	Switching delay[4]			TBF	
	Switching time[4]			TBF	
SEL pin					
V_{1-7}	Input voltage High	3		V_{CC}	V
V_{1-7}	Input voltage Low	−0.3		0.4	V
I_1	Input current High			TBF	μA
I_1	Input current Low			TBF	μA
ON pin					
V_{9-7}	Input voltage High	3		V_{CC}	V
V_{9-7}	Input voltage Low	−0.3		1.5	V
I_9	Input current High			TBF	μA
I_9	Input current Low			TBF	μA

NOTES:

1. Crosstalk is defined as the ratio between the output signal originating from another input and the nominal output signal on the same output.
2. $S/N = 20\log \frac{V_{OP-P}}{V_O \text{ noise RMS } B = 5MHz}$.
3. Supply voltage rejection $= 20\log \frac{V_R \text{ supply}}{V_R \text{ on output}}$.
4. Fast switching input signal
   Output signal: YUV
   Input : 0V input 1, mode 2
   0.75V RGB input 2, mode 1



FUNCTIONAL DESCRIPTION

The circuit contains two sets of inputs: input 1 from the color decoder (color difference signals), and input 2 from the accessory input, RGB, or possibly YUV, both with associated synchronization inputs.

In the RGB mode, the signals are matrixed internally to color difference signals for further processing in a control circuit (e.g., TDA8461).

The inputs are clamped, thus the clamp pulse is internally derived from the sync signals. The outputs can be made high-ohmic (OFF) in order to be able to put several circuits in parallel.

Control

The circuit can be controlled by an I²C bus or directly by DC voltages. The fast switching input can be operated by Pin 16 of the accessory input.

I²C BUS MODE

The protocol for the TDA8443 for I²C bus mode is:

STA	A6	A5	A4	A3	A2	A1	A0	R/W	AC	D7	D6	D5	D4	D3	D2	D1	D0	AC	STO

STA : Start condition
A6 : 1 } fixed address bits
A5 : 1 } fixed address bits
A4 : 0 } fixed address bits
A3 : 1 } fixed address bits
A2 : Sub-address bit set by S2
A1 : Sub-address bit set by S1
A0 : Sub-address bit set by S0
R/W : Read/Write bit (= 0 only write mode allowed)

AC : Acknowledge, generated by the TDA8443
D7 : MOD1 } mode control bits, see Table 2
D6 : MOD0 } mode control bits, see Table 2
D5 : G2 } gain control bits, see Table 4
D4 : G1 } gain control bits, see Table 4
D3 : G0 } gain control bits, see Table 4
D2 : PRIOR, priority bit
D1 : ON/OFF bit
D0 : ON/OFF active bit

Table 1. Sub-Addressing

SLAVE ADDRESS BITS			ADDRESS SELECT PINS		
A2	A1	A0	S2	S1	S0
0	0	0	GND	GND	GND
0	0	1	GND	GND	V_{CC}
0	1	0	GND	V_{CC}	GND
0	1	1	GND	V_{CC}	V_{CC}
1	0	0	V_{CC}	GND	GND
1	0	1	V_{CC}	GND	V_{CC}
1	1	0	V_{CC}	V_{CC}	GND
1	1	1	V_{CC}	V_{CC}	V_{CC}

NOTE:
Non-I²C bus operation, see Table 5.

Table 2. Mode Control

MOD1	MOD0	MODE	FUNCTION
0	0	0	Inputs 2 are selected directly
0	1	1	Inputs 2 are selected via RGB/YUV matrix
1	0	2	Inputs 1 are selected directly
1	1	3	Reserved; not to be used

Table 3. Priority Fast Switching Action

PRIOR	FS	MODE SELECTED
0	X	As set by mode control (Table 2)
1	0.4V	Mode 2
1	1 – 3V	Mode 1 if mode 1 is selected Mode 0 if mode 0 or 2 is selected

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Table 4. Gain Settings (see Block Diagram)

G2	G1	G0	TDA8443/C3			TDA8443A/C3	
			A1	A2, A3, A4	B1, B3	B1, B3	B2
0	0	0	1	1	−0.6	−1	0.45
0	0	1	1	1	1	1	1
0	1	0	Reserved; not to be used				
0	1	1	1	1	−0.6	−1	0.45
1	0	0	2	2	−0.6	−1	0.45
1	0	1	2	1	1	1	1
1	1	0	2	2	1	1	1
1	1	1	2	1	−0.6	−1	0.45

NOTES:

Matrix equations: relations between output and input signals of the matrix

$Y = 0.3R + 0.59V + 0.11B$

$R\text{-}Y = 0.7R - 0.59V - 0.11B$

$B\text{-}Y = -0.3R - 0.59V + 0.89B$

ON BIT

ON	FUNCTION
0	OFF, no output signal, outputs high-ohmic
1	ON, normal functioning

OFFACT-ON (Pin 9) Function

OFFACT	ON	FUNCTIONING
0	L	OFF
0	H	In accordance with last defined D7 – D1 (may be entered while OFF = L)
1	X	In accordance with last defined D7 – D1

POWER-ON RESET

When the circuit is switched on in the I^2C mode, bits D0 – D7 are set to zero.

Table 5. Non-I^2C Bus Mode (S2 = S1 = S0 = 0)

CONTROL			MODE SWITCHED BY FS	GAIN SETTINGS				
				TDA8443			TDA8443A	
SDA	SCL	SEL		A1	A4, A3, A2	B1, B3	B1, B3	B2
L	L	L	2/0	1	1	1	1	1
L	L	H	2/0	1	2	1	1	1
L	H	L	2/1	1	1	−0.6	−1	0.45
L	H	H	2/0	1	1	−0.6	−1	0.45
H	L	L	2/0	2	1	1	1	1
H	L	H	2/0	2	2	1	1	1
H	H	L	2/1	2	1	−0.6	−1	0.45
H	H	H	2/0	2	1	−0.6	−1	0.45

Fast Switching Input

F S	MODE SELECTED
⩽0.4V	Mode 2
1 – 3V	Mode 0 or 1 as set by control

ON Input

ON	FUNCTION
L	OFF, no output signal, outputs high-ohmic
H	Functioning as determined in Table 5

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I²C BUS LOAD CONDITIONS

4kΩ pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	RATING			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			µs
t_{SU}, t_{STA}	Start condition setup time	4			µs
t_{HD}, t_{STA}	Start condition hold time	4			µs
t_{LOW}	SCL, SDA Low period	4			µs
t_{HIGH}	SCL High period	4			µs
t_R	SCL, SDA rise time			1	µs
t_F	SCL, SDA fall time			0.3	µs
t_{SU}, t_{DAT}	Data setup time (write)	1			µs
t_{HD}, t_{DAT}	Data hold time (write)	1			µs
t_{SU}, t_{CAC}	Acknowledge (from TDA8443) setup time			2	µs
t_{HD}, t_{CAC}	Acknowledge (from TDA8443) hold time	0			µs

NOTE:
Timings t_{SU}, t_{DAT} and t_{HD}, t_{DAT} deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after 50µs delay.

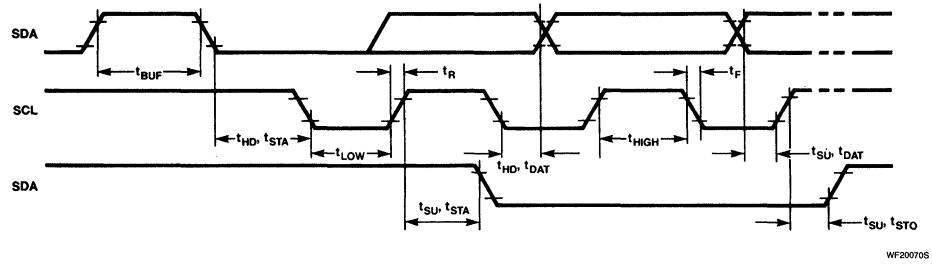

Figure 1. I²C Timing Diagram

Table 6. Application Information

INPUT 1	INPUT 2	OUTPUT	MODE	G2	G1	G0
YUV/S 0.34/−1.33/−1.05/0.3		YUV/S 0.34/−1.33/−1.05/0.6	2	1	1	1
	RGB/S 0.75/0.75/0.75/0.3		1	1	1	1
YUV/S 0.34/−1.33/−1.05/0.3			2	1	0	0
	RGB/S 0.75/0.75/0.75/0.3	YUV/S 0.68/−2.66/−2.1/0.6	1	1	0	0
YUV/S 0.34/−1.33/−1.05/0.3		YUV/S 0.34/−1.33/−1.05/0.6	2	1	0	1
	YUV/S 0.34/−1.43/−1.05/0.3		0	1	0	1
YUV/S 0.34/−1.33/−1.05/0.3		YUV/S 0.68/−2.66/−2.1/0.6	2	1	1	0
	YUV/S 0.34/−1.33/−1.05/0.3		0	1	1	0

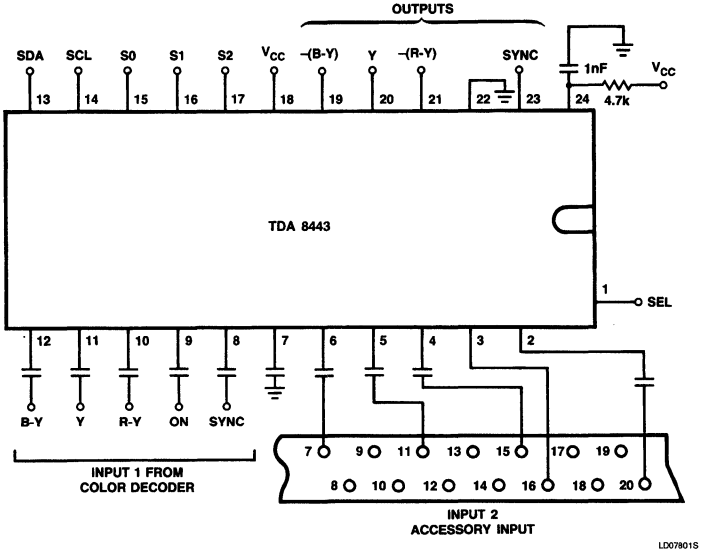

Figure 2. Application of the TDA8443

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Signetics

TEA2000
PAL/NTSC Color Encoder

Objective Specification

Linear Products

DESCRIPTION

The TEA2000 is a monolithic integrated circuit, which encodes color information and provides composite video output for driving a VHF or UHF modulator.

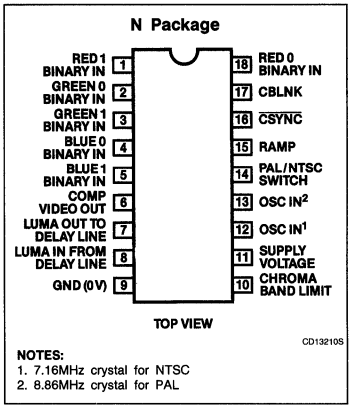
FEATURES

- **European PAL® and American NTSC/M standard selectable**
- **Internal generation of burst timing and PAL switch function**
- **6-bit binary TTL-compatible input provides 64 different colors**
- **TTL-compatible color blanking input**
- **TTL-compatible sync input**

APPLICATIONS

- **Video processing**
- **Graphics**
- **Computers**

PIN CONFIGURATION



NOTES:
1. 7.16MHz crystal for NTSC
2. 8.86MHz crystal for PAL

ORDERING INFORMATION

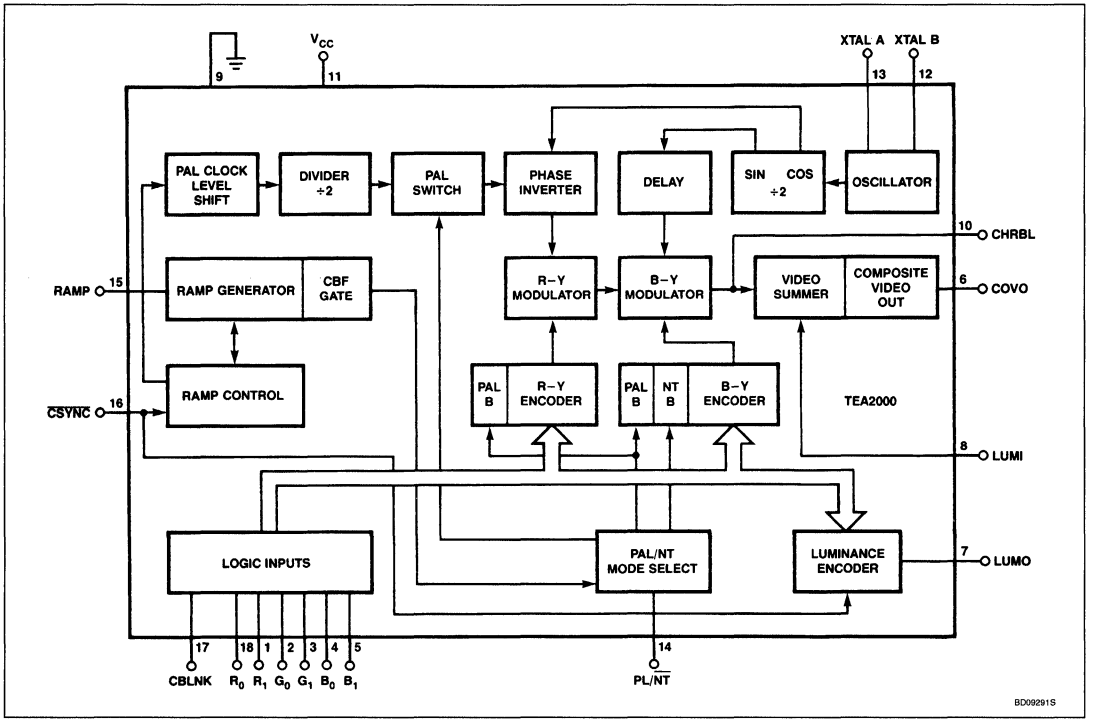
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102)	−20°C to +70°C	TEA2000N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{11-9}	Supply voltage	13.2	V
	Voltages, Pins 1, 2, 3, 4, 5, 14, 16, 17, 18	V_{CC}	V
T_{STG}	Storage temperature range	−65 to +125	°C
T_A	Operating ambient temperature range	−20 to +70	°C

®PAL is a registered trademark of Monolithic Memories, Inc.

BLOCK DIAGRAM



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DC AND AC ELECTRICAL CHARACTERISTICS V_{11-9} = 12V; T_A = 25°C; measured in Figure 2, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{11-9}	Supply voltage	10.8	12	13.2	V
I_{11}	Supply current V_{11-9} = 12V		55		mA
Oscillator stability (Pins 12 and 13)					
	Crystal type 4322 143 04051 V_{CC} = 10.8 to 12V V_{CC} = 12 to 13.2V		 +50 −50		 Hz Hz
Digital inputs					
 V_{IL} V_{IH}	$\overline{CSYNC}$, CBLNK, PL/$\overline{NT}$ Pins 16, 17, 14 R0, R1, G0, G1, B0, B1, Pins 18, 1, 2, 3, 4, 5 V_{IN} (LOW) V_{IN} (HIGH)	 −0.5 2		 0.8 V_{11-9}	 V V
C_I	Input capacitance			10	pF
t_R, t_F	Input rise and fall times			200	ns
	$\overline{CSYNC}$, CBLNK, R0, R1, G0, G1, B0, B1, Pins 16, 17, 18, 1, 2, 3, 4, 5				
I_{IL}	Input current DC for V_{IN} = 0V			−100	µA
I_{IH}	Input current DC for V_{IN} = 2V			20	µA
	PL/$\overline{NT}$, Pin 14				
I_{IL}	Input current DC for V_{IN} = 0V			−500	µA
I_{IH}	Input current DC for V_{IN} = 2V			−200	µA
Composite video output (Pin 6)					
$V_{6-9\ (P-P)}$	Output amplitude (sync tip-white)		2		V
V_{6-9}	Sync tip level		5		V
R_{6-9}	Output load resistor	0.47	1		kΩ
V_{P-P}	Variation of output amplitude; T_A = 0 to +70°C			TBD	%
ΔV	Over supply range; V_{11-9} = 10.8 to 13.2V			TBD	%
R_L	Output impedance (with 1kΩ load)		15		Ω
ΔV_{RMS}	Residual chrominance on white		30		mV
ΔV	Tolerance on luminance amplitude		10		%
ΔV	Tolerance on chrominance amplitude		10		%
ΔΩ	Tolerance on chrominance phase		TBD		%
Chrominance band limiting (Pin 10)					
R_{10-11}	Internal resistance		1.5		kΩ
Luminance delay (Pins 7 and 8)					
R_S	Nominal series resistor (±5%)		1.2		kΩ
R_L	Nominal load resistor at luminance input (±5%)		1		kΩ
Ramp timing (Pin 15) (see Figure 2)					
	With external RC circuit; R = 36kΩ; C = 330pF[1]				
t_B	Start of burst from line sync		5.7		µs
t_W	Burst width		2.5		µs
t	Threshold for separation of equalizing pulses and sync pulses	36	44	56	µs

NOTE:
1. A figure of 5pF is assumed for external capacitance. This figure includes temperature dependence of the components.

PAL/NTSC Color Encoder | TEA2000

FUNCTIONAL DESCRIPTION

The TEA2000 PAL/NTSC color encoder and video summer integrated circuit has an internal oscillator from which the (R-Y) and (B-Y) waveforms are generated. The TEA2000 accepts timing signals (composite sync, composite blanking) and a 6-bit binary-coded input giving color information. The inputs are organized as 2 bits per primary color, and gamma correction is applied to the resultant luminance and chrominance levels. Each of the equally-spaced intensity levels (for each primary color) is combined with those of the other primary colors. This produces 64 output colors comprising a wide range of saturated and desaturated colors, black, white, and two levels of grey. The resultant output is a composite video signal compatible with the PAL and NTSC/M standards.

PIN DESCRIPTION

R0, R1, G0, G1, B0, B1, Pins 18, 1, 2, 3, 4, and 5. These are the red, green, and blue logic inputs, 2 bits per primary color. These inputs are TTL compatible. The functions of the remaining pins are described beside the corresponding pin number.

16 $\overline{\text{CSYNC}}$ — Composite sync input requiring a negative logic signal, TTL compatible. For PAL operation, the field sync must include line sync information.

12, 13 XTALA, XTALB — Oscillator inputs. A crystal in series with a trimmer capacitor is connected between Pins 12 and 13. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder. The crystal frequencies are:

PAL mode 8.867238MHz
NTSC mode 7.15909MHz

7, 8 LUMO, LUMI — Luminance output and input. The combined luminance and sync signal appearing at Pin 7 must be DC coupled to Pin 8 via an appropriate luminance delay line or resistor network. Resistors must have a tolerance of ±5%, or better, as they affect the DC level at COVO, Pin 6.

10 CHRBL — Chrominance filtering can be accomplished by connecting a chrominance frequency tuned filter (4.43MHz or 3.57MHz), via a blocking capacitor to Pin 10. This point is the chrominance summing junction and has a nominal internal impedance of 1.5kΩ. If a filter is used at this point, then the delay caused to the chrominance signal should be compensated by an appropriate luminance delay line.

6 COVO — Composite video output is internally buffered, giving a nominal output voltage swing of 2V sync-white and a nominal sync 5V level.

14 PL/$\overline{\text{NT}}$ — PAL/NTSC select input selects PAL mode when HIGH and NTSC mode when LOW. This input is TTL compatible. An internal pull-up resistor selects PAL if the pin is not connected.

15 RAMP — Ramp timing component connection. A capacitor and resistor connected to Pin 15 provide timing information for the color burst and for PAL phase switching. Alternative components may be used to optimize for NTSC operation.

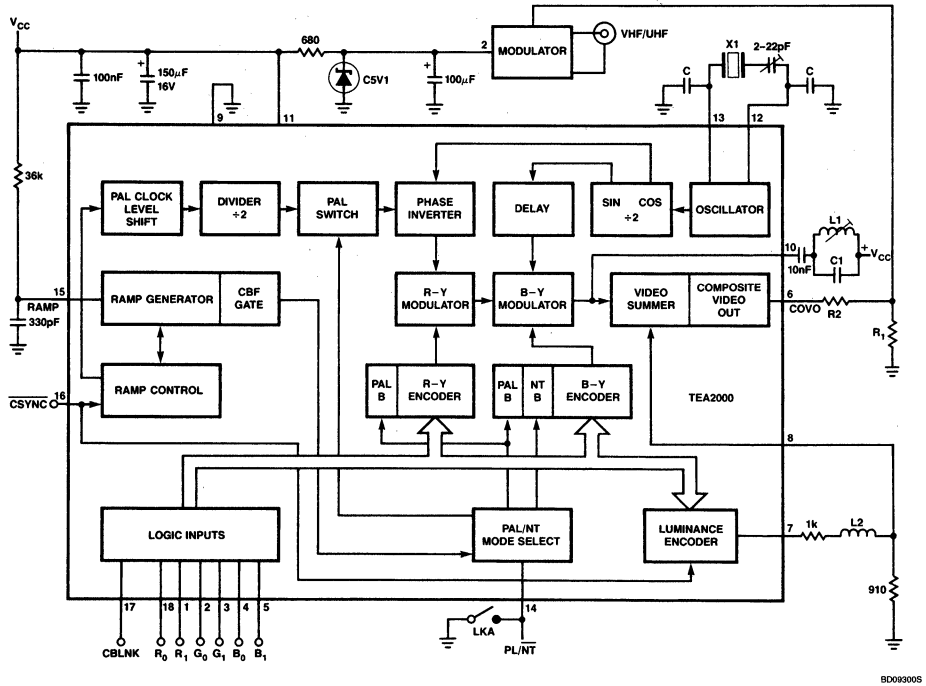
11 V_{CC} — 12V supply.

9 GND — Ground connection, zero volts.

17 CBLNK — Blanking input, when HIGH, switches off color inputs. CBLNK must be HIGH during sync and color burst unless color inputs are all LOW at this time. This input is TTL-compatible.

10

PAL/NTSC Color Encoder — TEA2000



NOTES:
X1 (PAL) = 8.867238MHz
X1 (NTSC) = 7.159100MHz
C = 5.6pF only for mask version 1

Component List for Figure 1

COMPONENT	PAL	NTSC
L1	15µH	18µH
C1	82pF	100pF
L2	DL270	DL330
R1	430Ω	510Ω
R2	510Ω	750Ω
M1	UM1233	UM1622
LKA	O/C	made

Figure 1. Internal Circuit Details and Typical External Connections

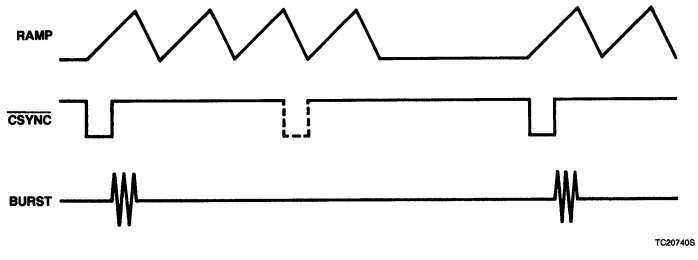


Figure 2. Ramp Timing

Signetics

AN1561
Applications of the Digital RGB Color Encoder TEA2000

Application Note

Linear Products

Figure 1 shows the basic block diagram of the TEA2000. Functionally, it encodes digital RGB signals into a standard $1V_{P-P}$ composite video signal to either NTSC or PAL® standards.

Each of the RGB inputs consists of two bits, which produce 64 color combinations (including "black level"). Each of the RGB 2-bit input color words is used to drive D/A modules in the luminance and chroma encoders. This produces four equally-spaced levels on each of the primary colors as follows: 0, 0.333, 0.666, 1.00 (full intensity).

The composite blanking input, CBLNK, can be used to force the colors to black during horizontal or vertical blanking. If the color inputs are already blanked, the CBLNK input may be used to selectively blank areas of the TV screen. If the CBLNK input is not required, it should be grounded.

The reference for the chroma signal is supplied by a crystal and an internal oscillator operating at twice the color sub-carrier frequency (NTSC = 7.16MHz, PAL = 8.87MHz). This frequency is divided by two to produce the quadrature chroma sub-carriers.

In the PAL mode, the phase of the R-Y subcarrier is switched by 180°C at the start of each horizontal line by the internally-generated PAL switch.

An internal ramp generator and comparator circuits are used to generate the color burst timing and the PAL switch from the composite sync input signal. Ramp timing is by an RC time constant.

Outputs of the R-Y and B-Y encoders, together with color burst information, are fed to a pair of double-balanced modulators whose outputs are summed to produce the modulated chroma signal. This signal is available at Pin 10 to allow external bandpass filtering of the chroma signal if desired.

The output from the luminance encoder, which includes composite sync, is connected to Pin 7 to allow the inclusion of a delay line in the luma path. This is to compensate for the delay introduced by the chroma filter if used. Delayed luminance is fed back into the IC at Pin 8; it is then amplified to compensate for amplitude losses in the delay line, and then summed with the modulated chroma signal in order to produce a composite video signal. This signal is fed to the output stage, which produces a 2V signal from the bottom of sync tip to full white signal at a low output impedance.

The output is adequate to drive standard VHF/UHF modulators via a simple resistor network or allows a standard 1V composite video 75Ω output implementation with just one buffer transistor.

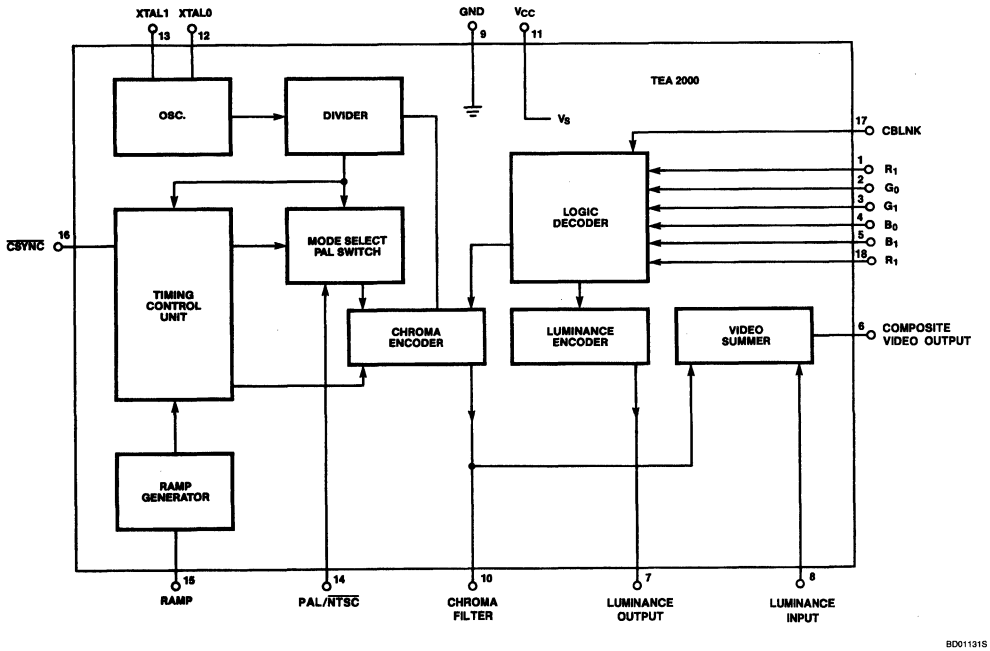


Figure 1. TEA2000 Block Diagram

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Applications of the Digital RGB Color Encoder TEA2000 AN1561

REFERENCE DATA

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{11-9}	Supply voltage		12		V
I_{11}	Supply current at $V_{11-9} = 12V$		55		mA
V_{IL} V_{IH}	Input voltage (Pins 1, 2, 3, 4, 5, 14, 16, 17, 18)	 2.0		0.8	V V
V_6	Composite video output (peak-to-peak)		2		V

TEA2000 EVALUATION CIRCUIT

Figure 2 shows a circuit diagram of a simple evaluation system including all external components that are required to demonstrate the TEA2000 color encoder, either with an RF modulator or with a standard 1V, 75Ω composite video output.

All the inputs to the TEA2000 are TTL compatible; however, all can interface with other signal voltages up to the TEA2000 supply V_{CC} voltage.

The six RGB inputs (two per primary color) in a simple computer or digital video system could be grouped as R, G, B to give the usual six full-saturated colors or black and white.

Alternatively, some form of Color Look-Up Table (CLUT) could be used to allow a choice of any eight (or more if more color bits are available) from the full palette of 64 colors. In circuit terms, this could be a small RAM which could be loaded from time to time to select different colors, or a ROM with a fixed selection of colors.

The blanking input, CBLNK, can be used to force the colors to black during line and field blanking intervals. If the color inputs are already blanked and CBLNK is not required for any other purpose, it should be connected to ground. CBLNK may also be used to blank areas of the screen.

Composite sync is used by the TEA2000 as a reference for the timing of color burst and, in PAL mode, to generate PAL SWITCH, which is used to alternate the phase of the R-Y chroma component on successive lines. The latter function means that in PAL mode the field sync region must either contain full line sync information, or an even number of line sync pulses may be missing.

The internal oscillator requires the connection of an appropriate twice sub-carrier crystal and trimmer (8.867238MHz for PAL and 7.159100MHz for NTSC). Capacitors C_9 and C_{10} are needed to ensure oscillator stability; these capacitors and the crystal and trimmer must be placed close to the oscillator pins.

The chroma band limiting filter consists of a second-order bandpass resonant LC circuit (L_1 on Figure 2) connected to the chroma band limiting, Pin 10 via a DC-blocking capacitor. The inductor should have an unloaded Q factor of about 100 at f_{SC}. The bandwidth of the filter is controlled by the internal circuit resistance at Pin 10, which has a value of $\simeq 1.5k\Omega$. The bandwidth of this filter determines the response to color change and the degree of patterning that occurs on a picture.

It is important that the inductor Q is reasonably high, as its equivalent parallel resistance shunts the internal resistance of the CHRBL input, thus affecting the chroma amplitude.

Useful equations for chroma filter calculations are:

1. $Q = \omega_{SC} \cdot C \cdot R_D$
2. $\text{Delay} = 2 \cdot R_D \cdot C$
3. $L = 1/(\omega_{SC}{}^2 \cdot C)$

Where:

$\omega_{SC} = 2 \cdot \pi \cdot f_{SC}$

$R_D \approx 1.5k\Omega$

The delay line DL_1 delays the luminance signal to match the delay in the chrominance path caused by the chroma filter.

If a chroma filter is not used, the luminance delay line should be replaced by a resistor of value equal to the delay line DC resistance (110Ω for the Philips DL270 (270ns) and DL330 (330ns)).

The position of color burst is defined by an internal ramp generator circuit which uses external timing components at Pin 15.

With the components shown, the timing of the burst will fall typically within ±5% of the nominal data sheet specification for PAL. This should prove satisfactory, but, if desired, the values could be changed slightly to give a closer match to the NTSC specifications.

A value of 5pF is allowed for in stray PCB capacitances in the values shown for the external ramp components connected to Pin 15.

The simple resistive divider couples the encoder output to the modulator and defines both the signal amplitude and the DC level at the input to the modulator. The 12V supply should be stable, as changes in the supply affect the DC level and signal swing at encoder output.

A simple signal transistor buffer circuit is used to produce the standard 1V sync-tip-to-white composite video working into a 75Ω load.

Color Look-Up Table System

When used in a computer system, the TEA2000 provides the possibility of displaying 64 screen colors that could be used in a number of configurations. All six bits could come from the display generator, or a color mapping system could be included.

When displaying color graphics, a reduction in memory size or complexity can be achieved if only three of four bits are used to define the color of each pixel. These bits would select eight or sixteen of the possible 64 colors from a palette.

The palette could contain a fixed selection of colors, or, by using a small, dedicated RAM, a different set of colors could be selected for each new display.

The schematic diagram, Figure 3, shows a system that allows a palette of sixteen colors to be selected. Before using the display, the RAM is loaded with sixteen 6-bit color codes. The multiplexer (74LS157) is then switched so that data from the display generator is used to address the RAM and so select colors from the palette.

The six output data lines from the RAM (two off 74S189) are connected to the color inputs of the TEA2000. The timing signals CBLNK and $\overline{\text{CSYNC}}$ from the display generator must also be taken to the color encoder.

Phase Locking To Line Rate

If the TEA2000 color encoder is used with a computer-based system to display text or graphics, the line rate ($\overline{\text{CSYNC}}$) is determined by the computer display generator crystal oscillator, and the color sub-carrier frequency is determined by the TEA2000 crystal oscillator. If these oscillators are not locked, the result is that the on-screen dot-crawl 'fades' in and out of visibility as one oscillator drifts with respect to the other. This effect can be

overcome by locking the sub-carrier frequency to a multiple of line frequency.

When used with a Teletext Broadcast Information System, the frequency locking can be indirectly achieved by locking sub-carrier frequency to the broadcast color burst. This solution, however, does not apply in the case of a computer system not linked to broadcast Teletext.

The exact relationship between sub-carrier frequency (f_{SC}) and line frequency (f_H) is (according to the relevant CCIR document):

for PAL,

$$f_{SC} = (284 - 1/4)\ f_H + 25Hz$$

rearranging,

$$(f_H)/2 = (2 \cdot f_{SC} - 50Hz)/1135$$

for NTSC,

$$f_{SC} = (455 \cdot f_H)/2$$

rearranging,

$$(f_H)/2 = (2 \cdot f_{SC})/910$$

In the block diagram, Figure 4, this relationship is used directly to derive $(f_H)/2$ from a $2 \cdot f_{SC}$ oscillator. A second $(f_H)/2$ is simply derived from line sync, and the two signals are applied to a phase comparator and low-pass filter to control the $2 \cdot f_{SC}$ oscillator. When this PLL is locked, the exact relationship between sub-carrier frequency and line frequency is assured.

In the case of PAL, field sync is used to subtract one cycle of $2 \cdot f_{SC}$ every field (50Hz). In the case of NTSC, this function is not required. For displays that are non-standard (i.e., different number of lines, non-interlaced) the subtraction of one cycle per field may or may not be required.

Phase Locking To Broadcast Color Burst

To mix locally-generated, colored text with a broadcast picture, it is necessary to phase-lock the local and broadcast color burst and horizontal and vertical sync, since they have to share a common color burst reference.

Comparing the phase of color burst generated within the TEA2000 with the broadcast color burst, and using the error signal to correct the $2 \cdot f_{SC}$ crystal presents certain problems.

The Effect of PAL Switch

In the case of PAL-encoded video, the phase of the color burst signal is switched by ± 45°C about the Y axis for each new line. If the PAL switch within the TEA2000 is not synchronized with that of the broadcast signal, then there will be a 90°C phase error in the TEA2000 color burst.

If an error which reverses on successive lines is detected, this indicates that the TEA2000 PAL switch is out of phase. The resulting error could be corrected by inhibiting one H line sync pulse per field into the TEA2000.

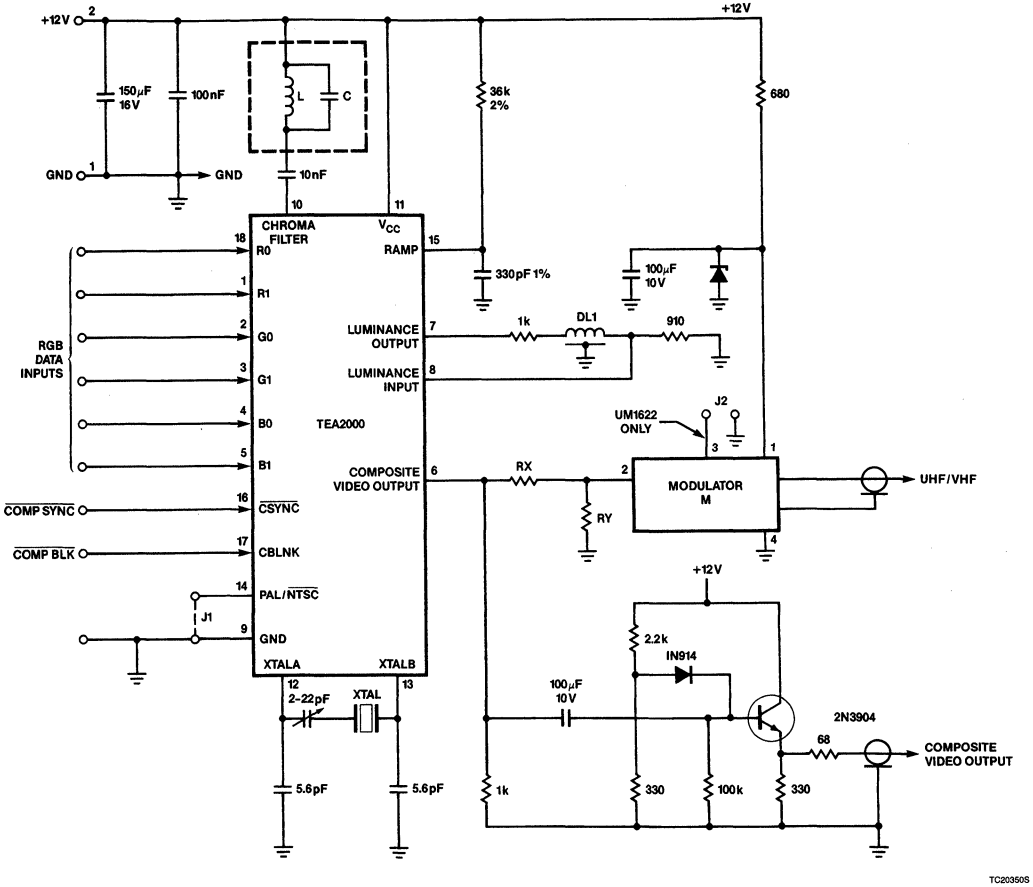
This effect does not occur in NTSC mode.

Phase Difference When In Lock

In some PLL designs, when in the lock condition, there is a 90° phase difference between the VCO and the reference signal. As zero phase difference is required in this application, some means of removing this 90° difference is needed, e.g., phase shifting of the reference before locking.

The internal divide-by-two, which produces f_{SC} from the twice sub-carrier oscillator, might be thought to introduce an ambiguity into the phase-locked loop; however, this is not so, because the phases of the actual sub-carrier frequency signals are locked together.

Applications of the Digital RGB Color Encoder TEA2000 AN1561



SYMBOL	COMPONENT	SOURCE	TYPE	NTSC	PAL
L	Inductor	TOKO		18µH Q = 100	15µH Q = 100
C	Capacitor			100pF	82pF
DL_1	Delay line	PHILIPS	DL330	330µs	
DL_1	Delay line	PHILIPS	DL270		270µs
XTAL	Crystal			7,159,090Hz	8,867,238Hz
M	Modulator	ASTEC	UM1632	UM1632	UM1233
J1	Jumper			Jumpered	Open
J2	Jumper			Jumper	Open
Rx	Resistor			750	510
Rx	Resistor			510	430

Figure 2. TEA2000 Evaluation System

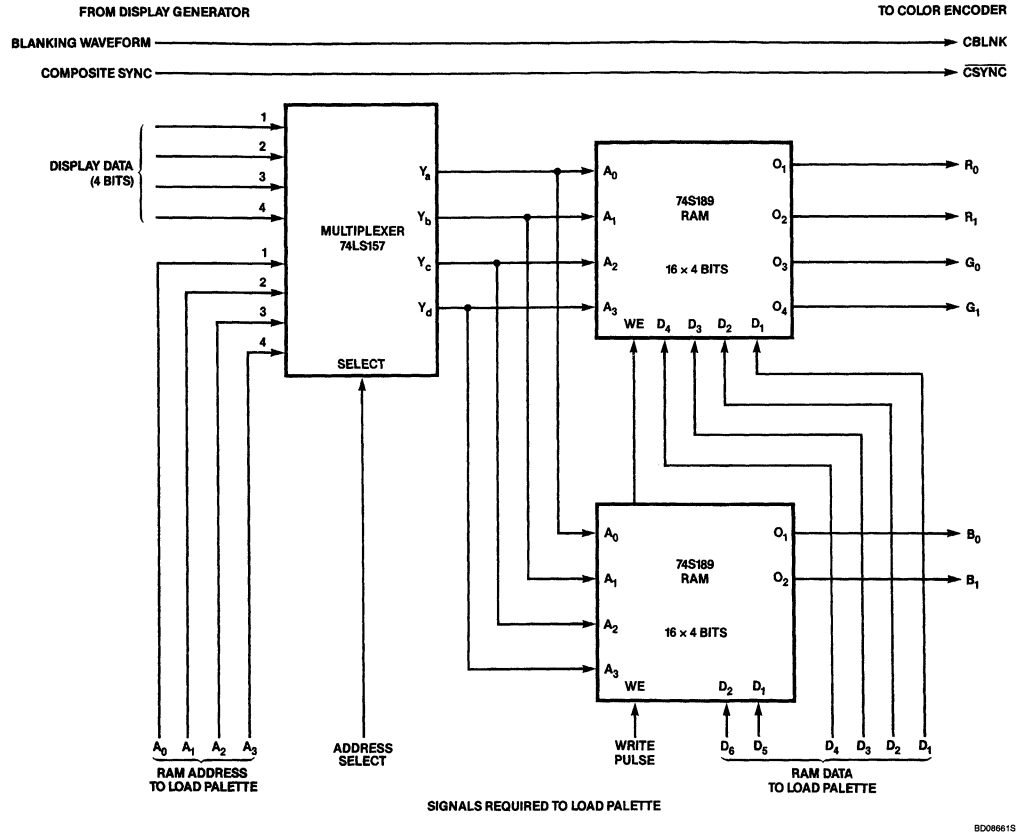


Figure 3. Diagram of Color Palette, 16 Colors Out of 64, System

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Applications of the Digital RGB Color Encoder TEA2000 AN1561

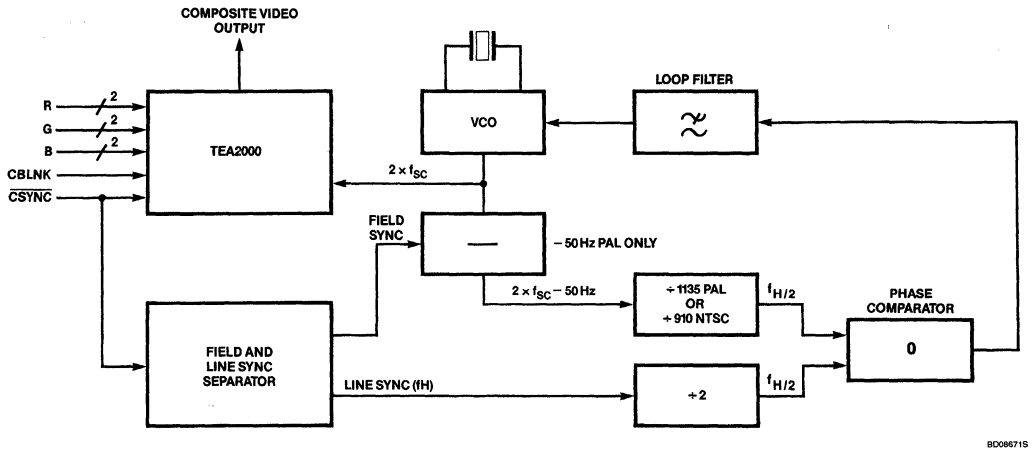


Figure 4. Basic Block Diagram for Phase Locking to Horizontal Line Rate

This application note was edited from Mullard MTH8502.
Application of the TEA2000 Color Encoder by
R.C. Eason and J.A. Tijou. June 10, 1985.

Signetics

Linear Products

Section 11
Special-Purpose Video Processing

INDEX

Signetics

TDA6800
Video Modulator Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA6800 is a modulator circuit for modulation of video signals on a VHF/UHF carrier. The circuit requires a 5V power supply and few external components for the negative modulation mode. For positive modulation an external clamp circuit is required. This circuit can be used as a general-purpose modulator without additional external components.

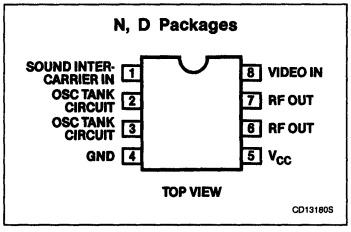
FEATURES

- **Balanced modulator**
- **Symmetrical oscillator**
- **Video clamp circuit for negative modulation**
- **Frequency range 50 to 800MHz**

APPLICATIONS

- **Video modulators**
- **General-purpose modulators**
- **Computers**

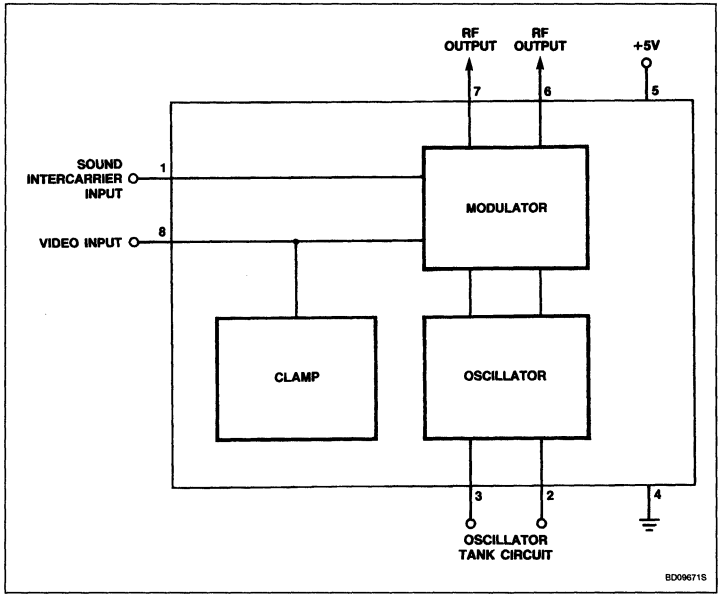
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP (SOT-97A)	−25°C to 85°C	TDA6800N
8-Pin Plastic SO (SOT-96A)	−25°C to +85°C	TDA6800TD

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7	V
V_{8-4}	Input voltage	4	V
$V_{6,\,7-4}$	Output voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	125	°C
T_A	Operating ambient temperature range	−65 to +85	°C
θ_{JA}	Thermal resistance from junction to ambient in free air TDA6800T TDA6800	 260 120	 °C/W °C/W

DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V; T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage range	4.5		5.5	V
I_{CC}	Supply current consumption		9	13	mA
$V_{8(P-P)}$	Video input voltage		1		V
R_8	Input impedance	30			kΩ
V_8	Voltage (DC) at video input (clamp voltage)		1.4		V
V_1	Voltage (DC) at sound input		2.5		V
V_{6-7}	Output voltage f = 50MHz; R_L = 75Ω		13		mV
V_{6-7}	Output voltage f = 600MHz; R_L = 75Ω		10		mV
Δ_G	Differential gain			10	%
Δ_ϕ	Differential phase			10	deg.
	Intermodulation[1] (1.1MHz)		−80	−60	dB
Δ_F	Frequency shift V_B = 5%, f = 600MHz			100	kHz
Δ_F	Frequency shift V_B = 5%, f = 800MHz		TBD		kHz
Δ_F	Frequency drift 25 to 40°C			100	kHz
Δ_F	Frequency drift 15 to 55°C			300	kHz
Positive modulation (see Figure 2)					
V_R	Residual carrier voltage			2.5	%
α	Cross modulation[2]		0.1	0.25	%

NOTES:

1. Input signal: DC 0.45V (V_{8-4} = 1.85V)
   4.4MHz; input voltage (P-P) = 0.6V
   5.5MHz; input voltage (P-P) = 1.26V
   measured with respect to picture carrier, at f = 600MHz.
2. Input signal: DC 1V (V_{8-4} = 3.5V)
   5.5MHz AM modulated, f_M = 100kHz
   m = 0.8; input voltage (P-P) = 2.27V (including modulation)
   measured with respect to the picture carrier, at f = 600MHz.

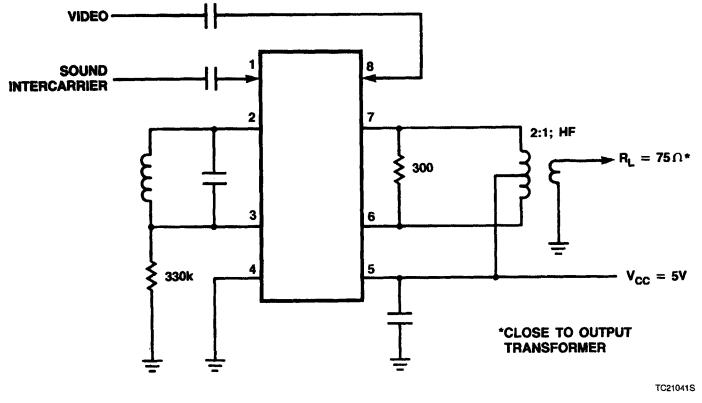

Figure 1. Application for Negative Modulation

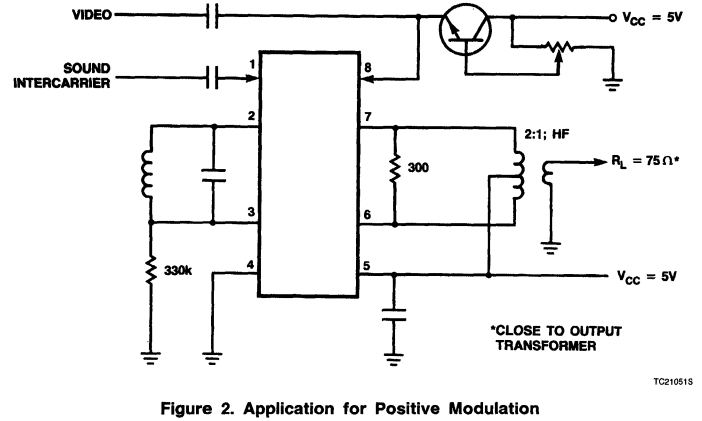

Figure 2. Application for Positive Modulation

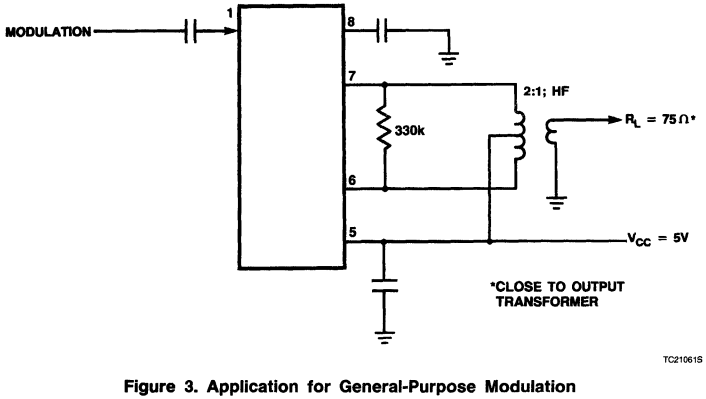

Figure 3. Application for General-Purpose Modulation

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Signetics

NE568
150MHz Phase-Locked Loop

Preliminary Specification

Linear Products

DESCRIPTION

The NE568 is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate ±10% deviations with less than 4.0% non-linearity (1.5% typical). In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20-pin dual in-line and 20-pin SO (surface-mounted) plastic packages.

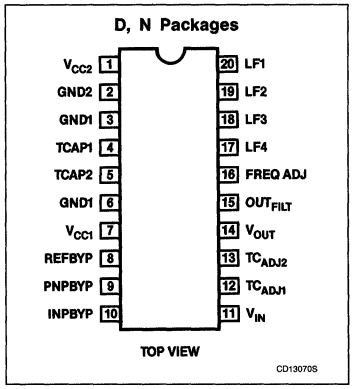
FEATURES

- **Operation to 150MHz**
- **High linearity buffered output**
- **Series or shunt loop filter component capability**
- **Temperature compensated**

APPLICATIONS

- **Satellite receivers**
- **Fiber-optic video links**
- **VHF FSK demodulators**
- **Clock recovery**

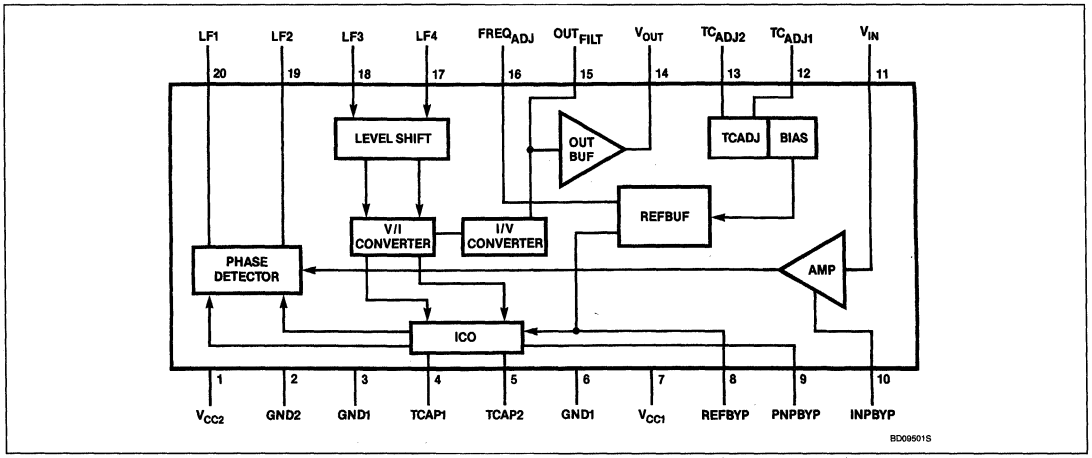
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL Package	0 to +70°C	NE568D
20-Pin Plastic DIP	0 to +70°C	NE568N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation	500	mW

ELECTRICAL CHARACTERISTICS

The electrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test setup is not necessarily optimum. The NE568 is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1 – 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 5V$, $f_O = 70MHz$, Test Circuit Figure 1, $f_{IN} = -20dBm$, $R_4 = 0\Omega$ (ground), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current			60	75	mA

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±10%, Input = −20dBm Dev = ±20%, Input = −20dBm Dev = ±20%, Input = +10dBm		1.5	4.0 5.5 5.5	%
	Lock range[2]	Input = −20dBm	±25	±35		% of f_O
	Capture range[2]	Input = −20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 4	0.45	0.52		V_{P-P}
	AM rejection	V_{IN} = −20dBm (30% AM) 0dBm (30% AM) referred to ±20% deviation		30 50		dB
f_O	Distribution[6]	Centered at 70MHz, R_2 = 1.2kΩ, C_2 = 17pF, R_4 = 0Ω (C_2 + C_{STRAY} = 20pF)	−15	0	+15	%
f_O	Drift with supply	4.75V to 5.25V		1		%/V

NOTES:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitance. See Figures 4 and 5.
5. Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Nonlinearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

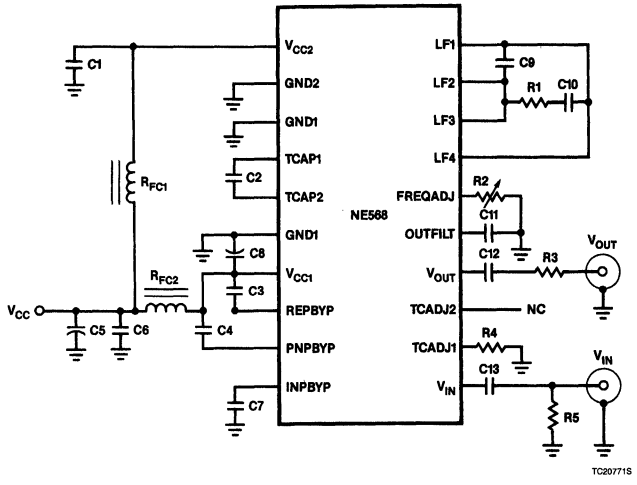

Figure 1. Test and Application Circuit

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FUNCTIONAL DESCRIPTION

The NE568 is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \text{ F}$$

where

$$C^* = C_2 + C_{STRAY}.$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See Figure 6 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568 was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constants are:

$K_D = 0.127$V/Radian (Phase Detector Constant)

$$K_O = 4.2 \times 10^9 \frac{\text{Radians}}{\text{V-sec}} \text{ (ICO Constant)}$$

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)(f_O)} \text{ F}$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 56pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10$MHz, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1 f_{BW}} \text{ F}$$

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568D

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	34pF	±2%	Ceramic OR chip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	56pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip	⅛W
R_2	2kΩ		Trim pot	⅛W
R_3[3]	43Ω	±10%	Chip	⅛W
R_4[4]	4.5kΩ	±10%	Chip	⅛W
R_5[3]	50Ω	±10%	Chip	⅛W
RFC_1[5]	10μH	±10%	Surface mount	
RFC_2[5]	10μH	±10%	Surface mount	

NOTES:
1. $C_2 + C_{STRAY} = 20pF$.
2. $C_2 + C_{STRAY} = 36pF$ for temperature-compensated configuration with $R_4 = 4.5k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

For the test circuit, R_1 was chosen to be 27Ω. The calculated value of C_{10} is 590pF; 560pF was chosen as a production value. (In actual satellite receiver applications, improved video with low carrier/noise has been observed with a wider loop-filter bandwidth.)

A typical application of the NE568 is demodulation of FM signals. In this mode of operation, a second single-pole filter is available at Pin 15 to minimize high frequency feedthrough to the output. The roll-off frequency is set by an internal resistor of 350Ω ±20%, and an external capacitor from Pin 15 to ground. The value of the capacitor is:

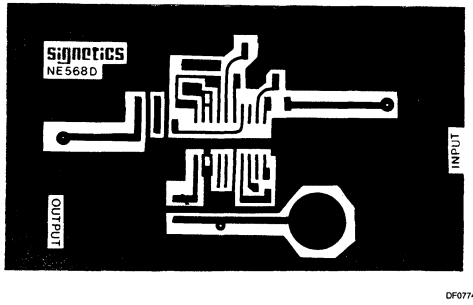
$$C = \frac{1}{2\pi\ (350) f_{BW}}\ F$$

Two final components complete the active part of the circuitry. A resistor from Pin 12 to ground sets the temperature stability of the circuit, and a potentiometer from Pin 16 to ground permits fine tuning of the free-running oscillator frequency. The Pin 16 potentiometer is normally 1.2kΩ. Adjusting this resistance controls current sources which affect the charge and discharge rates of the timing capacitor and, thus, the frequency. The value of the temperature stability resistor is chosen from the graph in Figure 6.

The final consideration is bypass capacitors for the supply lines. The capacitors should be ceramic chips, preferably surface-mount types. They must be kept very close to the device. The capacitors from Pins 8 and 9 return to V_{CC1} before being bypassed with a separate capacitor to ground. This assures that no differential loops are created which might cause instability. The layouts for the test circuits are recommended.

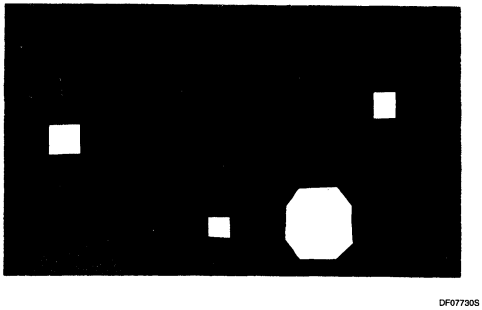
11

(Shown at 82% of original size.)



DF07740S

a. Component Side Top of Board



DF07730S

b. Back of Board

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent. Mount on bottom (back) of board. Add stand-off in each corner.
2. Back and top side ground must be connected at 8 point minimum.

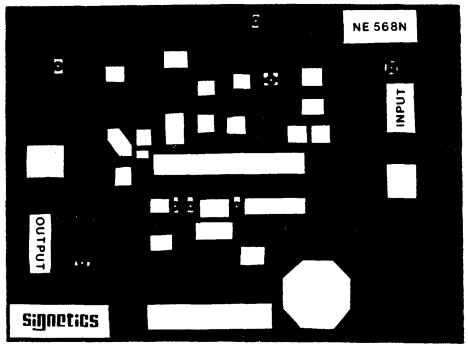
Figure 2

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568N

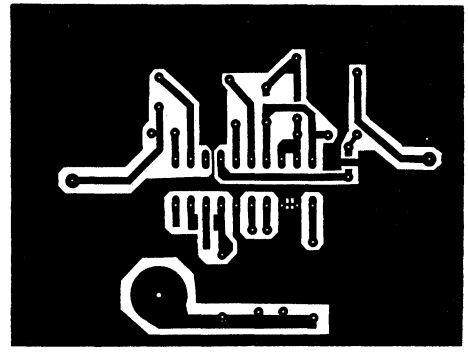
C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	17pF	±2%	Ceramic OR chip	50V
C_2[2]	34pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic OR chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	56pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic OR chip	50V
C_{12}	100nF	±10%	Ceramic OR chip	50V
C_{13}	100nF	±10%	Ceramic OR chip	50V
R_1	27Ω	±10%	Carbon	¼W
R_2	2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Carbon	¼W
R_4[4]	4.5kΩ	±10%	Carbon	¼W
R_5[3]	50Ω	±10%	Carbon	¼W
RFC_1	10μH	±10%		
RFC_2	10μH	±10%		

NOTES:
1. $C_2 + C_{STRAY} = 20pF$ for test configuration with $R_4 = 0\Omega$.
2. $C_2 = 34pF$ for temperature-compensated configuration with $R_4 = 4.5k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$; $R_3 = 75\Omega$ for 75Ω applications.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 17pF$.

(Shown at 82% of original size.)



DF07750S



DF07760S

a. Component Side for Leaded Components **b. Solder Side of Board and Chip Capacitors**

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent mounted on the component side of the board.
2. Component side and solder side ground planes must be connected at 8 points minimum.

Figure 3

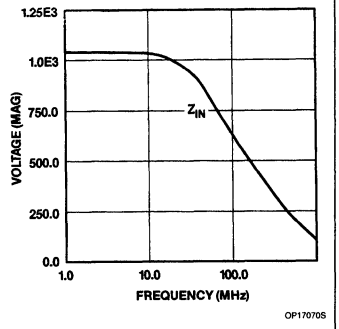


Figure 4. NE568 Input Impedance With CP = 0.5pF 20-Pin SO Package

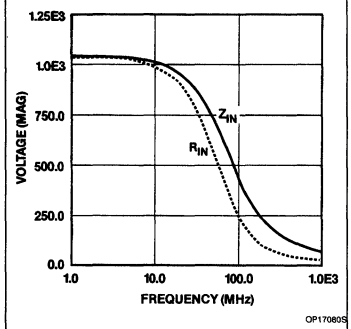


Figure 5. NE568 Input Impedance With CP = 1.49pF 20-Pin Dual In-Line Plastic Package

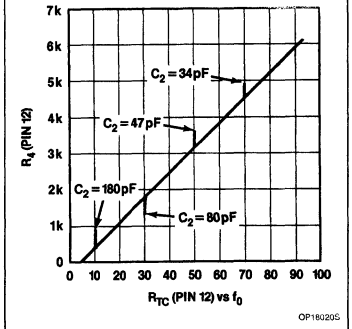


Figure 6

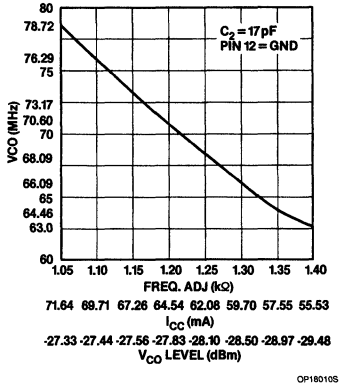


Figure 7. Typical V_{CO} Frequency vs R_2 Adjustment

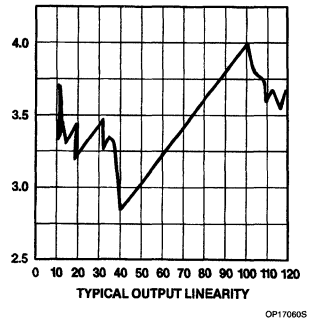


Figure 8. Typical Output Linearity

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Signetics

PNA7509
7-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analog-to-digital converter designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22MHz.

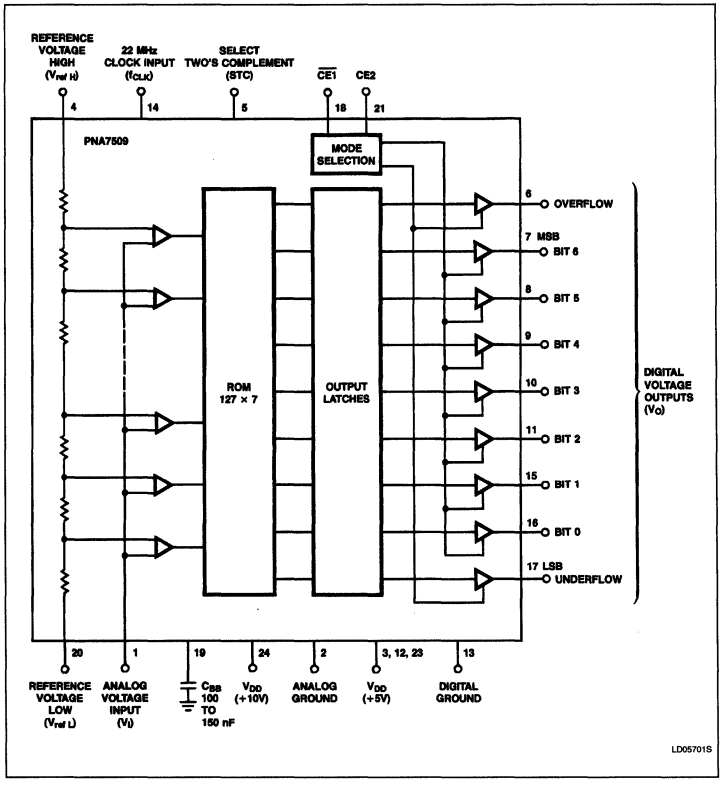
The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge-triggered and can be switched into 3-State mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

FEATURES

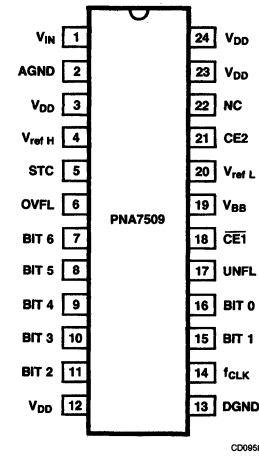
- **7-bit resolution**
- **22MHz clock frequency**
- **No external sample and hold required**
- **High input impedance**
- **Binary or two's complement 3-State TTL outputs**
- **Overflow and underflow 3-State TTL outputs**
- **Low reference current (250μA typ.)**
- **Positive supply voltages (+5V, +10V)**
- **Low power consumption (400mW typ.)**
- **Available in SO Package**

BLOCK DIAGRAM



PIN CONFIGURATION

D, N Packages



CD09580S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{IN}	Analog voltage input
2	AGND	Analog ground
3	V_{DD}	Positive supply voltage (+5V)
4	V_{REFH}	Reference voltage HIGH
5	STC	Select two's complement
6	OVFL	overflow
7	bit 6	Most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD}	Positive supply voltage (+5V)
13	DGND	Digital ground
14	f_{CLK}	22MHz clock input
15	bit 1	
16	bit 0	Least-significant bit (LSB)
17	UNFL	Underflow
18	$\overline{CE1}$	Chip enable input 1
19	V_{BB}	Back bias output
20	V_{REFL}	Reference voltage LOW
21	CE2	Chip enable input 2
22	NC	Not connected
23	V_{DD}	Positive supply voltage (+5V)
24	V_{DD}	Positive supply voltage (+10V)

APPLICATIONS

- **High-speed A/D conversion**
- **Video signal digitizing**
- **Radar pulse analysis**
- **High energy physics research**
- **Transient signal analysis**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	PNA7509N
24-Pin Plastic SO (SOT-101)	0 to +70°C	PNA7509D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pins 3, 12, 23)	7	V
V_{DD}	Supply voltage range (Pin 24)	12	V
V_{IN}	Input voltage range	7	V
V_{OUT}	Output current	5	mA
P_D	Power dissipation	400	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

7-Bit Analog-to-Digital Converter | PNA7509

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{3, 12, 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $C_{BB} = 100nF$; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pins 3, 12, 23)	4.5		5.5	V
V_{DD}	Supply voltage (Pin 24)	9.5		10.5	V
I_{DD}	Supply current (Pins 3, 12, 23)		60	TBD	mA
I_{DD}	Supply current (Pin 24)		10	TBD	mA
Reference voltages					
V_{REFL}	Reference voltage LOW (Pin 20)	2.4	2.5	2.6	V
V_{REFH}	Reference voltage HIGH (Pin 4)	5.0	5.1	5.2	V
I_{REF}	Reference current	175	250	375	mA
Inputs					
	Clock input (Pin 14)				
V_{IL}	Input voltage LOW	−0.3		0.8	V
V_{IH}	Input voltage HIGH	3.0		5.5	V
	Digital input levels (Pins 5, 18, 21)*				
V_{IL}	Input voltage LOW	0		0.8	V
V_{IH}	Input voltage HIGH	2.0		5.5	V
	Input current				
$-I_{5, 21}$	at $V_{5, 21-13} = 0V$	TBD		100	μA
I_{18}	at $V_{18-13} = 5V$	TBD		100	μA
	Input leakage current				
I_{LI}	(except Pins 5, 18, 21)			10	μA
	Analog Input levels (Pin 1)				
	at $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$				
$V_{IN\ P-P}$	Input voltage amplitude (peak-to-peak value)		2.6		V
V_{IN}	Input voltage (underflow)		2.5		V
V_{IN}	Input voltage (overflow)		5.1		V
$V_I - V_{REFL}$	Offset input voltage (underflow)		10		mV
$V_I - V_{REFH}$	Offset input voltage (overflow)		−10		mV
$C_{1, 2}$	Input capacitance	TBD		60	pF
Outputs					
	Digital voltage outputs (Pins 6 to 11 and 15 to 17)				
	Output voltage LOW				
V_{OL}	at $I_O = 2mA$	0		−0.4	V
	Output voltage HIGH				
V_{OH}	at $-I_O = 0.5mA$	2.4		V_{DD}	V

*When Pin 5 is LOW, binary coding is selected.
When Pin 5 is HIGH, two's complement is selected.
If Pins 5, 18 and 21 are open-circuit, Pins 5, 21 are HIGH and Pin 18 is LOW.
For output coding see Table 1; for mode selection see Table 2.

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{3, 12, 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$; $f_{CLK} = 22MHz$; $C_{BB} = 100nF$; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing (see also Figure 1)					
	Clock input (Pin 14)				
f_{CLK}	clock frequency	1		22	MHz
t_{LOW}	clock cycle time LOW	20			ns
t_{HIGH}	clock cycle time HIGH	20			ns
	Input rise and fall times[1]				
t_R	rise time			3	ns
t_F	fall time			3	ns
	Analog input[1]				
BW	Bandwidth (−3 dB)				
	at $V_{1-2(P-P)} = 2.2V$	10			MHz
dG	Differential gain				
	at $f_I = \leqslant 4.5MHz$[2]			5	%
dp	Differential phase				
	at $f_I = \leqslant 4.5MHz$[2]			5	deg
P_E	Phase error				
	at $f_I = \leqslant 4.5MHz$[3]			±10	deg
S/N	Signal-to-noise ratio				
	at $V_{1-2(P-P)} = 2.2V$;				
	$f_I = \leqslant 4.5MHz$; B = ±1 MHz	36			dB
	Harmonics				
	at $V_{1-2(P-P)} = 2.2V$;				
	$f_I = 3.6MHz$				
f_0	Fundamental		0	0	dB
f_{2nd}	2nd harmonic			tbd	dB
f_{3rd}	3rd harmonic			tbd	dB
f_{4th}	4th harmonic			tbd	dB
f_{5th}	5th harmonic			tbd	dB
f_{6th}	6th harmonic			tbd	dB
f_{7th}	7th harmonic			tbd	dB
	Harmonics				
	at $V_{1-2(P-P)} = 2.2V$;				
	$f_I = 4.5MHz$				
f_0	Fundamental		0	0	dB
f_{2nd}	2nd harmonic			tbd	dB
f_{3rd}	3rd harmonic			tbd	dB
f_{4th}	4th harmonic			tbd	dB
f_{5th}	5th harmonic			tbd	dB
f_{6th}	6th harmonic			tbd	dB
f_{7th}	7th harmonic			tbd	dB
	Digital outputs[2, 4]				
t_{HOLD}	Output hold time	6	15		ns
t_D	Output delay time		20	28	ns
t_{CY}	Internal delay		3		clocks
	Propagation delay time				
t_{PD}	at $f_{CLK} = 20.25MHz$	154		176	ns
t_{DT}	3-State delay time (see Figure 2)	t_{BF}	10	20	ns
C_{OL}	Capacitive output load[2]	0		15	pF
	Transfer function				
	Non-linearity				
INL	integral			±1	LSB
DNL	differential			±1/2 = 0.4%	LSB

NOTES:

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sine wave (peak-to-peak value of the analog input voltage at $V_{IN} = 1.8V$) amplitude modulated with a sine wave voltage ($V_{IN} = 0.7V$) at $f_I \leqslant 4.5MHz$.
3. Sine wave voltage with increasing amplitude at $f_I \leqslant 4.5MHz$ (minimum amplitude $V_{IN} = 0.25V$; maximum amplitude $V_{IN} = 2.5V$).
4. The timing values of the digital output Pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5V.

7-Bit Analog-to-Digital Converter | PNA7509

Table 1. Output Coding (V_{REFL} = 2.5V; V_{REFH} = 5.1V)

STEP	$V_{1, 2}$ (Typ)	UNFL	OVFL	BINARY Bit 6 – Bit 0	TWO's COMPLEMENT Bit 6 – Bit 0
Underflow	< 2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
Overflow	⩾ 5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

Table 2. Mode Selection

CE1	CE2	BIT 0 to BIT 6	UNFL, OVFL
X	0	High impedance	High impedance
0	1	Active	Active
1	1	High impedance	Active

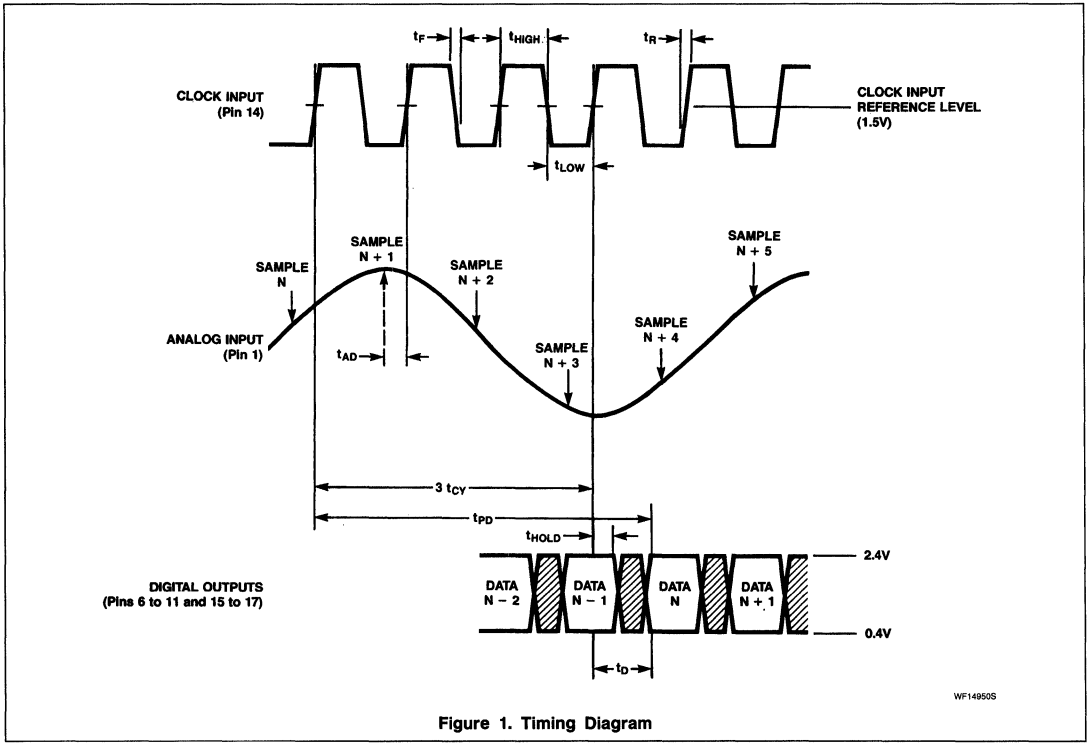


Figure 1. Timing Diagram

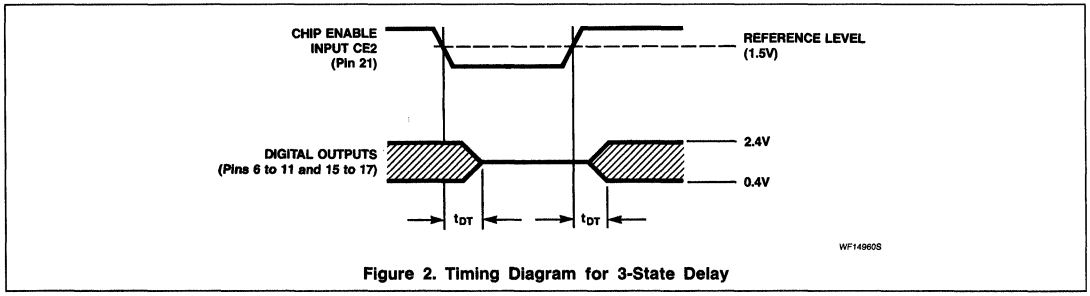


Figure 2. Timing Diagram for 3-State Delay

7-Bit Analog-to-Digital Converter PNA7509

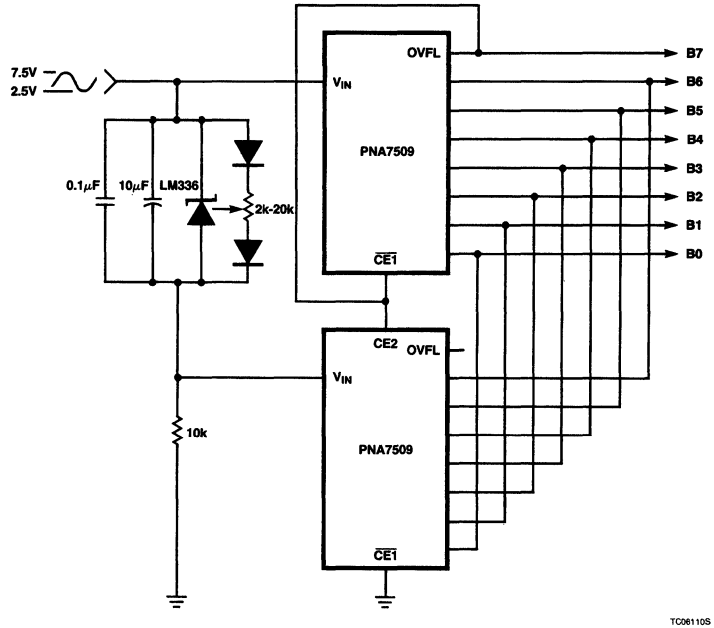


Figure 3

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Signetics

AN108

An Amplifying, Level-Shifting Interface for the PNA7509 Video A/D Converter

Linear Products

Application Note

Author: Nick Gray

The NE5539 is well-suited for use as a level-shifting amplifier at the input of the PNA7509 video speed analog-to-digital converter. Designing this circuit is straightforward and relatively simple.

The first step is to determine the gain that is required. Since the PNA7509 requires a maximum input of 5.0 V_{DC} and a minimum input of 2.5V_{DC} the required amplifier gain is

$$A_V = \frac{5.0 - 2.5}{V_{MAX} - V_{MIN}} = \frac{2.5}{V_{MAX} - V_{MIN}}.$$

where V_{MAX} is the maximum level of the amplifier input signal, and V_{MIN} is the minimum level of the amplifier input signal.

This gain must be greater than unity as the gain of a non-inverting amplifier such as this is

$$A_V = 1 + (R_F/R_I).$$

The ratio of R_F to R_I is then

$$R_F/R_I = A_V - 1.$$

The task is now to select R_F and R_I. These resistors should be low enough to swamp out the effects of any stray capacitance. If R_I is arbitrarily chosen, R_F is found to be

$$R_F = \frac{2.5\ R_I}{V_{MAX} - V_{MIN}}.$$

The required offset voltage, V_O, is then found to be

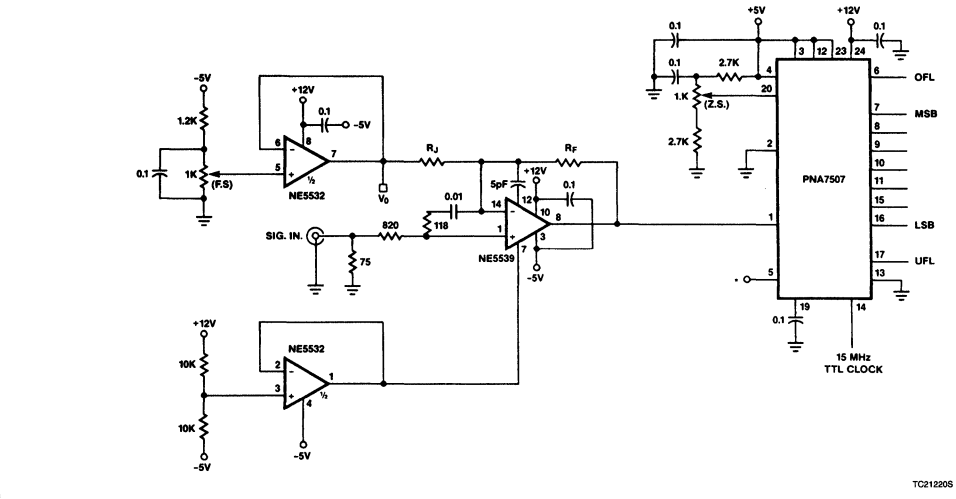
$$V_O = V_{MAX} - [(5 - V_{MAX})\ (R_I/R_F)].$$

Because the NE5539 input cannot be driven closer to its negative supply than about 4.7V, that negative supply must be −4.7V or more negative in order to accommodate an input signal whose minimum potential is 0V. The NE5539 output must never come any closer to the supply rail than about 5.5V, and the maximum output required to drive the PNA7509 is 5V, so the positive supply must be at least 5 + 5.5V, or 10.5V. If we use standard power supply potentials of +12V and −5V, this would satisfy these requirements, except we must insure that the negative supply is at least as negative as −4.7V. Tests have been conducted that indicate satisfactory operation with the positive supply between 10.5V and 13.5V, and the negative supply between −4.7V and −5.7V. Furthermore, because the NE5539 is sensitive to unbalance in the supplies, it is necessary to insure that its Pin 7 potential is close to halfway between the positive and the negative supply. Two resistors and an op amp driving Pin 7 nicely provide this balance. Another op amp is used to set the offset voltage.

The three diodes are used to drop the 12V supply to 10V for the PNA7509. If available and desired, a separate 10V supply could be used without the diodes.

Other components are shown for the convenience of the user. The potentiometer at Pin 5 of the NE5514 is used to adjust V_O. The potentiometer at Pin 12 of the NE5514 sets the voltage at the low end of the PNA7509 reference ladder, so is a zero-scale adjustment. The potentiometer at Pin 3 of the NE5514 sets the high end voltage on the PNA7509 reference ladder and is, effectively, a full-scale adjustment. It is also possible to use a signal divider at the NE5539 input for full-scale adjustment. R_F can also be made variable to provide full-scale adjustment. Care should be exercised, however, when introducing potentiometers into feedback loops or into high-frequency signal paths.

The NE5514 was chosen for its low input offset voltage temperature coefficient.



NOTE:
*Pin 5 should be grounded for binary output, or tied to a logic high for two's complement output.

TDA5703
Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5703 is an 8-bit analog-to-digital converter (ADC) designed for video and professional applications. The TDA5703 converts the analog input signal into 8-bit binary-coded digital words at a sampling rate of up to 25MHz.

FEATURES

- **8-bit binary coded resolution**
- **Digitizing rates up to 25MHz**
- **Internal reference**
- **Only 3 external capacitors required**
- **Two voltage supply connections:**
  - **analog +5V**
  - **digital +5V**
- **1V full-scale analog input (75Ω external resistor tied to V_{CC1})**
- **Full-scale bandwidth; 10.5MHz at 3dB**
- **Low power consumption; typically 250mW**
- **24-lead plastic DIP**

APPLICATION

- **Video data conversion**

ORDERING INFORMATION

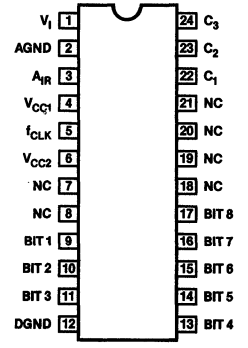
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101 BE17)	0 to +70°C	TDA5703N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltages at Pin 4 at Pin 6	 8 8	 V V
V_{IN}	Input voltage at Pins 1 and 5	8	V
I_{OUT} I_O	Output current at Pins 9, 10, 11, 13, 14, 15, 16 and 17	10	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	+125	°C
T_A	Operating ambient temperature range	0 to +70	°C

PIN CONFIGURATION

N Package



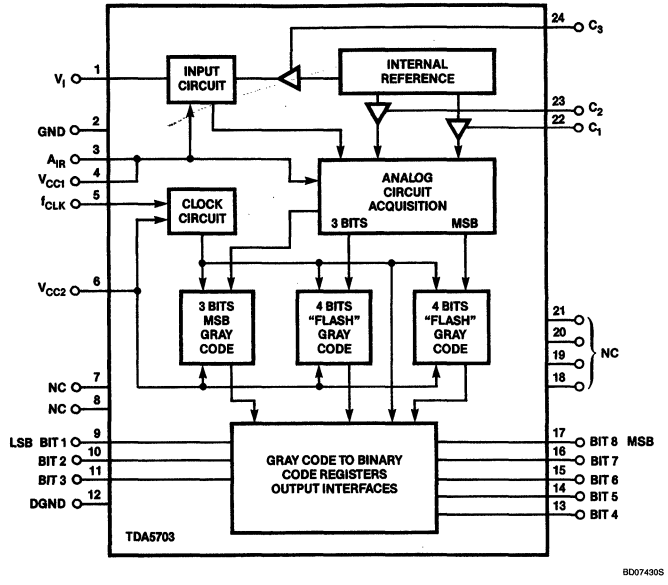
TOP VIEW

CD10850S

PIN NO.	SYMBOL	DESCRIPTION
1	V_I	Analog voltage input
2	AGND	Analog ground
3	A_{IR}	Analog input reference
4	V_{CC1}	Analog supply voltage
5	f_{CLK}	Clock input
6	V_{CC2}	Digital supply voltage
7	NC	Not connected
8	NC	Not connected
9	Bit 1	Least significant bit (LSB)
10	Bit 2	
11	Bit 3	
12	DGND	Digital ground
13	Bit 4	
14	Bit 5	
15	Bit 6	
16	Bit 7	
17	Bit 8	Most significant bit (MSB)
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	NC	Not connected
22	C_1	Decoupling for internal reference
23	C_2	
24	C_3	

Analog-to-Digital Converter TDA5703

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{CC1}	Analog supply voltage	Pin 4	4.75	5.0	5.25	V
V_{CC2}	Digital supply voltage	Pin 6	4.75	5.0	5.25	V
I_{CC1}	Analog supply current	Pin 4		60		mA
I_{CC2}	Digital supply current	Pin 6		110		mA
Res	Resolution			8		bits
Digital input levels[1]						
V_{IH}	Input voltage HIGH		2.2			V
V_{IL}	Input voltage LOW				0.8	V
I_{IH}	Input current HIGH				70	μA
I_{IL}	Input current LOW		−7	−.35		A
	Analog input levels					
	Absolute linearity	V_1	−1.0		+1.0	LSB
	Differential linearity	V_1	−0.5		+0.5	LSB
BW	Bandwidth	1dB 3dB	 6.0	6.0 10		mHz mHz
	Differential phase Differential gain	F_0 = 25MHz, measured with TDA5702		1 2.5		°C %
	Offset error			17		mV
R_{IN}	Input resistance			80		kΩ
C_{IN}	Input capacitance			5.5		pF
Digital output levels (I_O = 10mA)						
V_{OH}	Output voltage HIGH		2.4			V
V_{OL}	Output voltage LOW				0.45 0.40	V
C_O	External capacitance	C_1, C_2, C_3		100		nF
Temperature						
T_A	Operating ambient temperature range		0		+70	°C

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Timing						
f_C	Maximum conversion rate		25			MHz
t_{DELAY}	Aperture delay[1]			19		ns
t_D	Digital output delay[1]			24		ns
t_{PWH}	Pulse width conversion HIGH[1]		20			ns
t_{PWL}	Pulse width conversion LOW[1]		20			ns

NOTE:
1. See Timing Diagram, Figure 1

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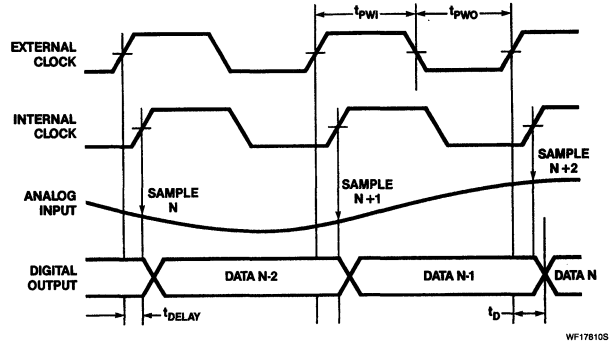


Figure 1. Timing Diagram

Signetics

NE5150/5151/5152
Triple 4-Bit RGB D/A Converter With and Without Memory

Preliminary Specification

Linear Products

DESCRIPTION

The NE5150/5151/5152 are triple 4-bit DACs intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150/5152 are single integrated circuit chips containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DACs. The input buffers are user-selectable as either ECL or TTL compatible for the NE5150. The NE5152 is similar to the NE5150, but is TTL compatible only, and operates off of a single +5V supply. The RAM is organized as 16 × 12, so that 16 "color words" can be down-loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the horizontal retrace time. The latches resynchronize the digital data to the DACs to prevent glitches. The DACs include all the composite video functions to make the output waveforms meet RS-170 and RS-343 standards, and produce $1V_{P-P}$ into 75Ω. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DACs." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on-chip, by building in high-frequency PSRR (eliminating separate V_{EE}s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency for the NE5150/5152 is 110MHz over the commercial termperature range. The devices are housed in a standard 24-pin package and consume less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

FEATURES

- **Single-chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **110MHz update rate (NE5150, 5152)**
- **150MHz update rate (NE5151)**
- **Low power and cost**
- **Drives 75Ω cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

APPLICATIONS

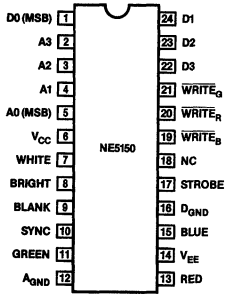
- **Bit-mapped graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-scan displays**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Ceramic DIP	0°C to +70°C	NE5150F
24-Pin Ceramic DIP	0°C to +70°C	NE5151F
24-Pin Ceramic DIP	0°C to +70°C	NE5152F

PIN CONFIGURATIONS

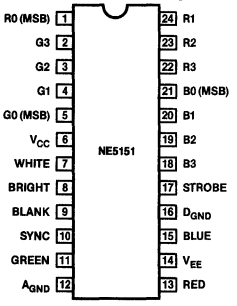
NE5150 F Package



TOP VIEW

CD09550S

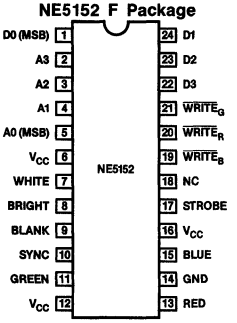
NE5151 F Package



TOP VIEW

CD10431S

NE5152 F Package



TOP VIEW

CD09570S

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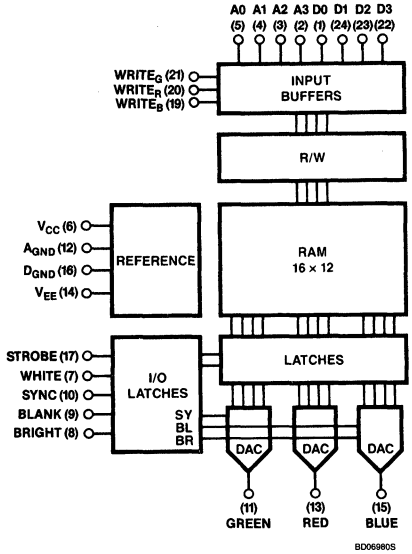
Triple 4-Bit RGB D/A Converter With and Without Memory

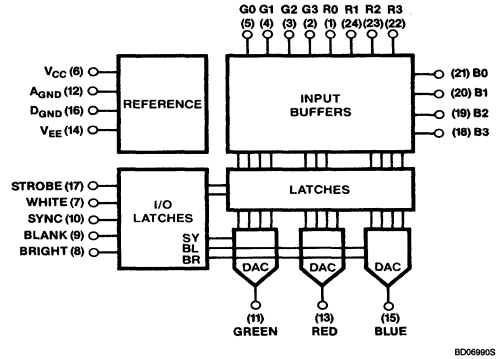
NE5150/5151/5152

BLOCK DIAGRAMS

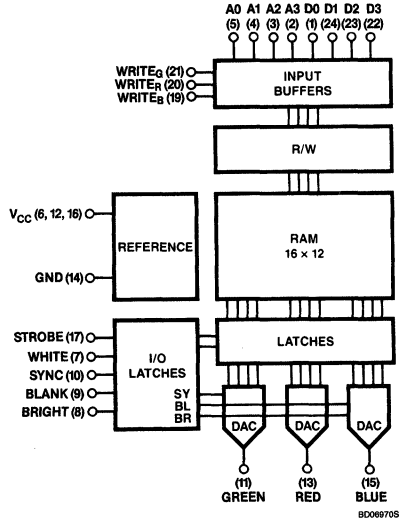
NE5150



NE5151



NE5152



Triple 4-Bit RGB D/A Converter With and Without Memory

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Temperature range		
T_A	Operating	0 to +70	°C
T_{STG}	Storage	−65 to +150	°C
V_{CC}	Power supply	7.0	V
V_{EE}		−7.0	V
	Logic levels		
	TTL-high	5.5	V
	TTL-low	−0.5	V
	ECL-high	0.0	V
	ECL-low	0 to V_{EE}	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Resolution	4			bits
	Monotonicity	4			bits
NL	Non-linearity		± 1/16	± 1/2	LSB
DNL	Differential non-linearity		± 1/8	± 1	LSB
	Offset error (25°C) [1111] (BRT = 1)		− 1/5	± 1	LSB
	Gain error (25°C) [0000] (BRT = 1)		± 1/2	± 1	LSB
V_{CC}	Positive power supply (TTL mode) (NE5150)	4.5	5.0	5.5	V
	(TTL mode) (NE5151)	4.75	5.0	5.5	V
	(ECL mode)	−0.1	0.0	0.1	V
V_{EE}	Negative power supply (TTL or ECL mode) (NE5150/5151)	−4.75	−5.0	−5.5	V
I_{CC}	Positive supply current (NE5150/5151)		15	25	mA
	(NE5152)		175	210	mA
I_{EE}	Negative supply current (NE5150)		175	210	mA
	(NE5151)		145	175	mA
	Analog voltage range (ZS to FS)		603		mV
	Gain tracking (any two channels)			± 1/4	LSB
LSB	Least significant bit		40.2		mV
EWH	Enhanced white level (25°C)[2]		0		mV
BS	Bright shift (25°C)(0 to 1)		71.4		mV
EBL	Enhanced blanking level (25°C)[2]		−674		mV
ESY	Enhanced sync level (25°C)[2]		−960		mV
R_O	Output resistance (25°C)	67.5	75.0	82.5	Ω
V_{IH}	TTL logic input high	2.0			V
V_{IL}	TTL logic input low			0.8	V
I_{IH}	TTL logic high input current (V_{IN} = 2.4V)			20	μA
I_{IL}	TTL logic low input current (V_{IN} = 0.4V)			−1.6	mA
V_{IH}	ECL logic input high	−1.045			V
V_{IL}	ECL logic input low			−1.48	V
I_{IH}	ECL logic high input current (V_{IN} = −0.8V)			−1.0	mA
I_{IL}	ECL logic low input current (V_{IN} = −1.8V)			−1.0	mA

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TEMPERATURE CHARACTERISTICS

V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Offset TC[1]		±50	±100	ppm/°C
	Gain TC[1]		±70	±200	ppm/°C
	Gain Tracking TC (any two channels)		±20	±50	ppm/°C
	Enhanced white level TC[1]		±50	±100	ppm/°C
	Bright shift TC		±70	±200	ppm/°C
	Enhanced blanking level TC		±100	±300	ppm/°C
	Enhanced sync level TC		±100	±300	ppm/°C
	Output resistance TC		+1000	+2000	ppm/°C

NOTES:
1. Normalized to full-scale (603mV).
2. With respect to [1111] (BRT = 1).

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < +70°C, for NE5150/5151; V_{CC} = +5V (TTL), GND = 0V for NE5152, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{MAX}	Maximum operating frequency (NE5150/5152)	110			MHz
t_{WAS}	Write address setup (NE5150/5152)	0			ns
t_{WAH}	Write address hold (NE5150/5152)	0			ns
t_{WDS}	Write data setup (NE5150/5152)	4			ns
t_{WDH}	Write data hold (NE5150/5152)	2			ns
t_{WEW}	Write enable pulse width (NE5150/5152)	3			ns
t_{RCS}	Read composite[1] setup (NE5150/5152)	3			ns
t_{RCH}	Read composite[1] hold (NE5150/5152)	2			ns
t_{RAS}	Read address setup (NE5150/5152)	3			ns
t_{RAH}	Read address hold (NE5150/5152)	2			ns
t_{RSW}	Read strobe pulse width (NE5150/5152)	3			ns
t_{RDD}	Read DAC delay (NE5150/5152)		8		ns
f_{MAX}	Maximum operating frequency (NE5151)	150			MHz
t_{CS}	Composite[1] setup (NE5151)	3			ns
t_{CH}	Composite[1] hold (NE5151)	2			ns
t_{DS}	Data-bits setup (NE5151)	1			ns
t_{DH}	Data-bits hold (NE5151)	5			ns
t_{SW}	Strobe pulse width (NE5151)	3			ns
t_{DD}	DAC delay (NE5151)		8		ns
t_R	DAC rise time (10 – 90%)		3		ns
t_S	DAC full-scale settling time[2]		10		ns
C_{OUT}	Output capacitance (each DAC)		10		pF
SR	Slew rate		200		V/μs

Triple 4-Bit RGB D/A Converter With and Without Memory

NE5150/5151/5152

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
GE	Glitch energy			30	pV-s
PSRR[3]	Power supply rejection ratio (to red, green or blue outputs)				
	V_{EE} at 1kHz		43		dB
	V_{EE} at 10MHz		28		dB
	V_{EE} at 50MHz		14		dB
	V_{CC} at 1kHz		80		dB
	V_{CC} at 10MHz		50		dB
	V_{CC} at 50MHz		36		dB

NOTES:
1. Composite implies any of the WHITE, BRIGHT, BLANK or SYNC signals.
2. Setting to ± ½ LSB, measured from STROBE 50% point (rising edge). This time includes the delay throught the strobe input buffer and latch.
3. Listed PSRR is for the NE5150/51. The NE5152 PSRR specs are identical to the V_{EE} numbers in the table.

NE5150 PIN DESCRIPTION

Write enable inputs use negative-true logic while all other inputs are positive-true. All inputs operate synchronously with the positive edge-triggered strobe input. When V_{CC} is taken high (5V), all inputs are TTL compatible. When V_{CC} is grounded, all inputs are ECL compatible. All DACs are complementary, so that all ones is the highest absolute voltage and all zeroes is the lowest. All ones is called zero-scale (ZS) and all zeroes is called full-scale (FS). The analog output voltage is approximately 0V (ZS) to −1V (SYNC).

Pins 1, 24, 23, 22: **DATA** bits D0 (MSB) through D3, used to input digital information to the memory during the write phase. During this phase, the data bits are presented to the internal latches (noninverted) and the DACs will output the analog equivalent of the stored word, unless overridden by WHITE, BLANK or SYNC.

Pins 5, 4, 3, 2: **ADDRESS** lines A0 (MSB) through A3, used for selecting a memory address to write to or read from.

Pin 7: **WHITE** command. Presets the latches to all ones [1111] and outputs 0V absolute on all DACs. Can be modified to −71mV absolute when BRIGHT is taken low. Will be overridden by either a BLANK or SYNC command.

Pin 8: **BRIGHT** command. A low input here turns on an additional −71mV (10 IRE unit) switch, shifting all other levels downward. Not overridden by any other input.

Pin 9: **BLANK** command. Presets the latches to all zeroes [0000] and turns on an additional −71mV (10 IRE unit) switch. Absolute output is −671mV. Can be modified another −71mV to −742mV absolute when BRIGHT is taken low. Will override WHITE, and will be overridden by SYNC.

Pin 10: **SYNC** command. Presets the latches to all zeroes [0000] and turns on the BLANK switch. Additionally turns on a −286mV (40 IRE unit) switch in the green channel only. Absolute output is −671mV for the red and blue channels, and −957mV for the green channel. All levels can be shifted −71mV by taking BRIGHT low. Overrides WHITE and BLANK.

Pins 11, 13, 15: **GREEN, RED, BLUE.** Analog outputs with 75Ω internal termination resistors. Can directly drive 75Ω cable and should be terminated at the display end of the line with 75Ω. Output voltage range is approximately 0V to −1V, independent of whether the digital inputs are ECL or TTL compatible. All outputs are simultaneously affected by the WHITE, BLANK or BRIGHT commands. Only the GREEN channel carries SYNC information.

NOTE:
There are 100 IRE units from WHITE to BLANK. One IRE unit is approximately 7.1mV. Full-scale is 90 IRE units and 10 IRE units is 1/9 of full-scale (e.g., BRIGHT function).

Pins 19, 20, 21: $\overline{\text{WRITE}}_B$, $\overline{\text{WRITE}}_R$, $\overline{\text{WRITE}}_G$. Write enable commands for each of the three 16 × 4 memories. When all write commands are high, then the READ operation is selected. This is the normal display mode. To write data into memory, the write enable pin is taken low. Data D0 − D3 will be written into address A0 − A3 of each memory when its corresponding write enable pin goes low.

Pin 17: **STROBE.** The strobe signal is the main system clock and is used for resynchronizing digital signals to the DACs. Preventing data skew eliminates glitches which would otherwise become visible color distortions on a CRT display. The strobe command has no special drive requirements and is TTL or ECL compatible.

Pins 12, 16: A_{GND}, D_{GND}. Both Analog and Digital ground carry a maximum of approximately 100mA of DC current. For proper operation, the difference voltage between A_{GND} and D_{GND} should be no greater than 50mV, preferably less.

Pin 14: V_{EE}. The negative power supply is the main chip power source. V_{CC} is only used for TTL input buffers. As is usual, good bypassing techniques should be used. The chip itself has a good deal of power supply rejection — well up into the VHF frequency range — so no elaborate power supply filtering is necessary.

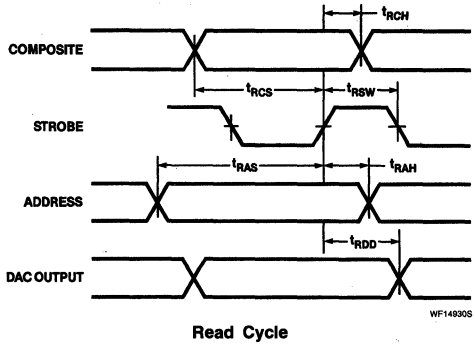
Pin 18: **NC.** This unused pin should be tied high or low.

11

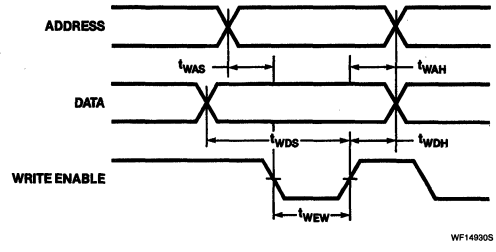
Triple 4-Bit RGB D/A Converter With and Without Memory

NE5150/5151/5152

NE5150/5152 TIMING DIAGRAMS



Read Cycle



Write Cycle

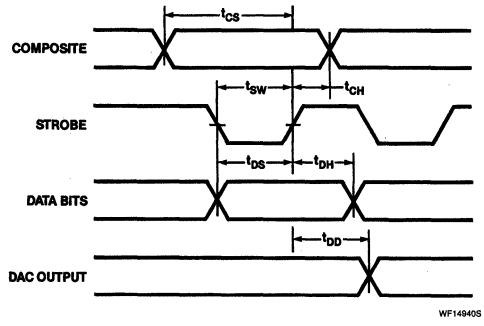
NE5151 PIN DESCRIPTION AND TIMING DIAGRAM

The eleven digital inputs D0 – D3, A0 – A3, $\overline{\text{WRITE}}_{G/R/B}$, and the unused Pin 18 of the NE5150 are replaced in the NE5151 with the three 4-bit DAC digital inputs G0 – G3, R0 – R3, and B0 – B3. All other pin functions (e.g., composite functions, power supplies, strobe, etc.) are identical to the NE5150.

NE5152 PIN DESCRIPTION

The NE5152 is a TTL-compatible-only version of the NE5150, operating off of a single +5V supply. V_{CC} Pins 6, 12 and 16 should be connected to +5V and Pin 14 to 0V. DAC output is referenced to V_{CC}.

NE5151 TIMING DIAGRAM



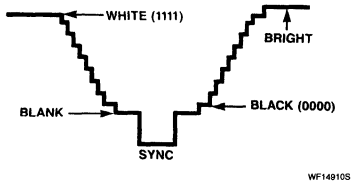
NE5150/NE5151/NE5152 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT[3]	CONDITION
1	X	X	0	X	X	-1031mV	SYNC[1]
1	X	X	1	X	X	-960mV	Enhanced SYNC[1]
0	1	X	0	X	X	-746mV	BLANK
0	1	X	1	X	X	-674mV	Enhanced BLANK
0	0	1	0	X	X	-71mV	WHITE
0	0	1	1	X	X	0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	-674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	-603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	-71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	0mV	Enhanced WHITE (EZS)

NOTES:

1. Green channel output only. RED and BLUE will output BLANK or Enhanced BLANK under these conditions.
2. For the NE5150/5152 the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.
3. Note output voltages in Logic Table are referenced to V_{CC} for the NE5152 only.

COMPOSITE VIDEO WAVEFORM



11

Signetics

AN1081
NE5150/51/52 Family of Video Digital-to-Analog Converters

Application Note

Linear Products

Author: Michael J. Sedayao

INTRODUCTION

Raster-scan systems and bit-mapped graphics are here to stay. For a computer to be of use, it needs an interactive means of communicating with the user. So for every computer, whether it is a 10MFLOP (millions of floating-point operations per second) supercomputer or a home computer for playing video games, some type of terminal or graphics display device is needed. Not long ago, inputs to the computer were made using stacks of Hollerith cards pushed into a hopper and then read into the computer. Results would then come from a printer. The hardcopy results were exactly what they looked like: final judgment from the computer. In order to respond, it was back to the punch-card machine. Needless to say, debugging programs became quite laborious. This problem led to the interactive display, allowing the user to enter information and see the results immediately. A new age in computing had arrived.

The areas of word processing, on-screen circuit simulation, and computer graphics developed with great rapidity. As technology improved, so did the ability to make larger displays having more colors and better resolution. As software developed, so did techniques such as windowing, the use of icons, and the ability to use graphic input devices such as mouses, light pens, and joysticks. Three-dimensional images and photographic quality reproduction soon followed.

Of the different technologies, how did raster scanning predominate over other forms? What differentiates bit-mapped graphics systems from character or vector-map systems? In the following sections it will become clear how technology and economics drove the market and, consequently, product development.

Displays: Raster, Vector Refresh, Storage Tube

A *raster* is technically a display of horizontal lines. How the display is created is what makes it unique. An electron beam generated by a CRT (Cathode Ray Tube) and containing video information, starts at the top left of the screen and traces a path to the right part of the screen (see Figure 1). It makes a slight angle as it travels across. The gun is then turned off as the beam rapidly returns to the left. It then repeats this zig-zag path until it reaches the bottom of the screen. The gun is again turned off as the beam travels back to the top of the screen. This entire process is repeated from 30 to 60 times per second so flicker is decreased (motion pictures or film typically display 24 images per second). What the electron beam has done is *scanned* its information onto the screen. This process is called *raster scanning.*

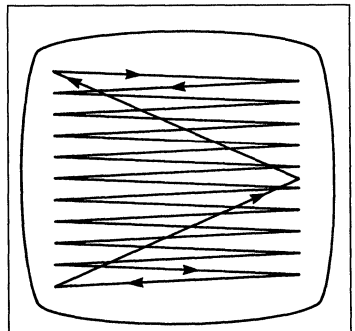


Figure 1. Raster-Scanned Display

All television sets display information in this manner. For television sets in the United States, the screen is redrawn 30 times per second. Additionally, the screen is *interlaced*, meaning that every other line is scanned and then the lines in between are scanned. This gives the illusion that the image is continuous. Since the television sets have 525 lines, 262.5 lines are scanned first (the odd field) and then the other 262.5 (the even field) are scanned. To visualize this, consider a 21-line system (see Figure 2). Scanning occurs at the above-mentioned 30Hz rate which is also known as the *frame rate*. Two fields (odd and even) equal one frame. Scanning 525 lines 30 times a second equals 15,750 horizontal lines scanned in a second. This is called the *horizontal scan frequency*. These are standard in the U.S., coming under the standard known as NTSC (National Television Standards Committee). In Europe, television has 625 lines and has a frame rate of 25Hz, or half the power line frequency, 50Hz.

Vector refresh displays, or stroke-writers, work on the principle that one line is the base unit of information. Each line then corresponds to a vector. Instead of scanning continuously, information is drawn line-by-line, hence the name stroke-writer. These systems off-load the refreshing tasks to special hardware, making the system slightly more cost-effective. Still, during the 1960's making them proved too expensive for everyday applications.

In 1971, Tektronix introduced the Direct View Storage Tube (DVST) for displaying and interfacing graphic data. It was based on oscilloscope techniques, storing information in a special, long-persistence phosphor which coats the inside of the screen. The display resolution is limited only by the phosphor grain size and the quality of the deflection circuitry. Although inexpensive, these devices were fine for oscilloscopes in the lab, but too cumbersome for fully interactive work. When the screen would redraw itself after the entry of new information, the sudden disappearance and reappearance was almost like looking at the light of a camera flashbulb. Another problem with the storage refresh screen was that when new information entered, it would write directly over the existing information. Only upon refreshing the screen would the new information be clear and readable. In many cases, the annoyance did not justify the low cost.

Bit-Mapped Graphics

In a bit-mapped graphics system, the screen is divided into individual elements called pixels, short for picture elements. When they say "bit-mapped", each pixel corresponds to a bit, or, in most cases, an address or memory location. This is what differentiates television from bit-mapped computer displays. Although both systems use raster scanning techniques, the information transmitted on television is continuous — a stream of analog information between horizontal sync pulses (the pulses used to denote the beginning and end of a horizontal line) — whereas in bit-mapped systems, each line is divided into discrete elements (the aforementioned pixels). The approximation of analog images would then be determined by the pixel density or screen resolution. As an example, Figure 3 shows a line approximated by a finite number of pixels.

The lines seem to staircase rather than flow because of the enlargement of the pixels. The effect is known in some computer graphics circles as "jaggies", short for jagged edges.

So, with more pixels, better resolution is possible. This is not without a price, though. Since each pixel corresponds to a memory location, memory cost rises dramatically as pixel resolution increases. Drawing speed

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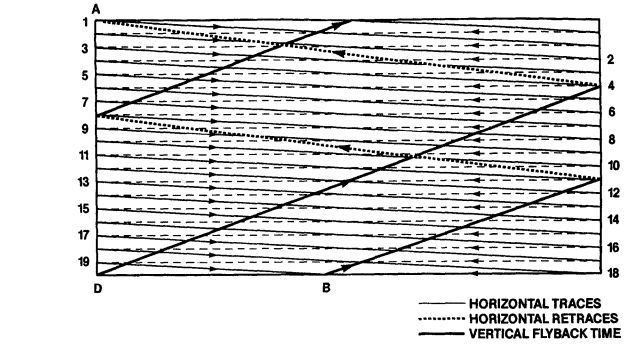

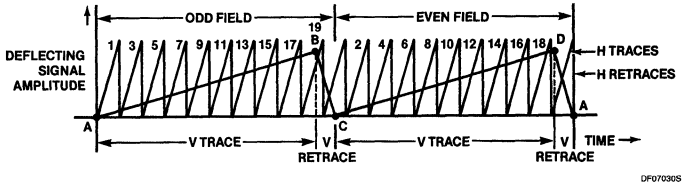

NOTES:
A sample scanning pattern for 21 interlaced lines per frame and 10½ lines per field. The corresponding H and V sawtooth deflection waveforms are shown below pattern. Starting at point A, the scanning motion continues through B, C, and D, and back to A again.

Figure 2. Interlaced Raster for 21-Line System

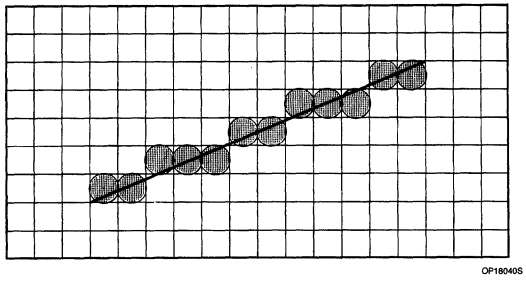

Figure 3. Ideal Line and Its Discrete Pixel Representation

must also increase since more pixels have to be drawn to maintain the ⩾30Hz frame rate needed to avoid flicker. Clearly then, the increase in bit-mapped graphics systems can be tied to the continuing price reductions in memory, specifically, the Dynamic Random Access Memory (DRAM). Fortunately, as the price has dropped, the memory size has not stood still. The last 14 years have seen size increases from 4k to 16k, 16k to 64k, 64k to 256k, and now, 256k to 1M bits of memory. One might expect to see DRAMs on the order of 4Mb within 2 to 3 years. Additionally, the continuing development of video RAMs cannot be ignored.

A bit-mapped system might be described in one of three ways. First, assume the display is monochrome and that each pixel can be represented by a certain number, for instance, 4 bits of information. This means that there are $2^4 = 16$ possible values of shading. Each bit of information can be represented by a "plane" of information. The plane would correspond to the area that was mapped by the pixels, namely the drawing area or display. Imagine an 8×8 pixel display. This means that there are 4 bit-planes and each pixel would have to pierce all four planes to give the proper information (see Figure 4). This is a fairly quick way to draw the screen since the data goes directly from the bit-map to the DAC (Digital/Analog Converter; DAC is singular here since the display is monochrome).

A direct conversion system for color is the second step. This is just an upgrade of the first case. Instead of 4 bit-planes, there are 12: three sets of the 4 planes for the three primary colors red, green, and blue. The advantage here is that there are now $2^{12} = 4096$ different colors, but the corresponding disadvantage is that the memory requirement has tripled. For more bit resolution per pixel, the associated memory demands increase by 3 times the pixel size times n, where n is the additional bit of resolution per pixel.

The third type of bit-map system uses a color look-up table (CLUT) as the driver for the display. The operation is straightforward. As the controller scans the bit-map each time it comes upon a pixel, it retrieves the bits which are then decoded into an address. This address is a pointer to the look-up table where sixteen 12-bit words (colors) are stored (see Figure 5). Once selected, that word is then sent to the color DACs and, from there, to the screen. The idea is similar to that of having cache memory in a computer, a fast memory used when the information in the memory is frequently accessed. Note that the bit-planes grow as n for 2^n additional colors while memory grows for 3n in the direct conversion case, a definite savings in memory.

The limitation in this case is that only 16 colors can be displayed at a time. In some systems, however, the CLUT is fast enough to be reloaded during the horizontal retrace time (CLUT size is sometimes referred to as the maximum number of colors that can be displayed on one horizontal line). This is especially important if the image is to simulate a smooth motion such as the rotation of a merry-go-round or the movement of an object with mirrored surfaces. In most cases, 16 colors is sufficient for any single display. 64 colors (6 bit-planes) is extremely good. 256 colors (8 bit-planes) is definitely a luxury.

It's clear that the memory speed and memory density, which are direct functions of the color and screen resolution, play a large part in the feasibility of a bit-mapped system. For that reason, the enormous gains and technological advancements in the field of memory design have made bit-mapped raster-scan graphic systems the best choice for both cost and performance.

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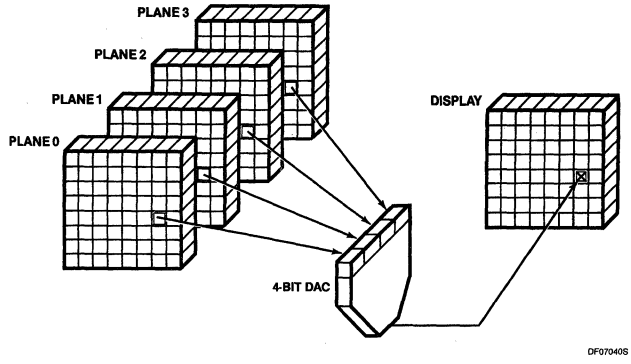


Figure 4. Monochrome Bit-Map With Direct Conversion to Display

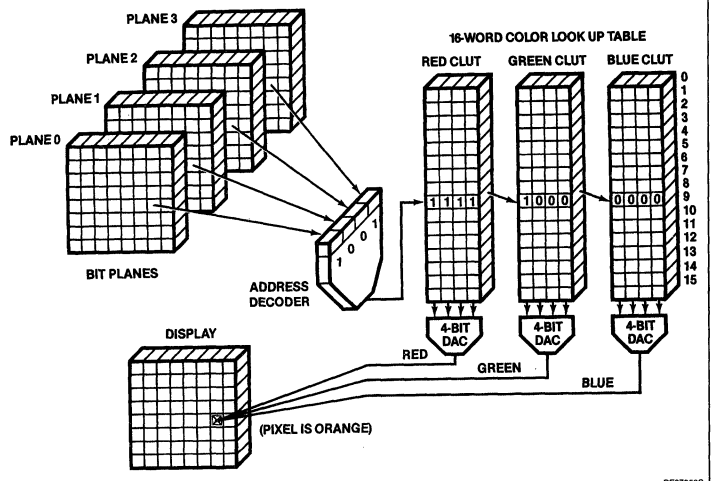


Figure 5. Color Bit-Map With 16-Word Color Look-Up Table

ISSUES FOR GRAPHIC DISPLAY SYSTEMS

Making the DAC Fit the Application

When designing graphic display systems, there are many decisions to be made in specifying the hardware and software needed for a system. What kind of speed is necessary in a given application? What kind of resolution will the users of the system require? Is color needed or will monochrome be adequate? If color, how many colors? Will images be viewed in two or three dimensions? How much memory is needed? How should the microprocessor/CRT controller/video DAC/frame buffer be matched with the rest of the system? What's the best type of software for a particular application? and on and on...

These questions could form the subject of an entire book and so will not be discussed in detail. This section will, however, discuss the few issues needed in the selection of the proper video DAC for a system.

Display Resolution vs Bit Resolution

When the quality of a display terminal is being evaluated, one primary consideration is the kind of resolution it has. There are two different types of resolution: display resolution, which is determined by the monitor and cannot be changed by the design; and bit resolution, which is dependent on the design of the video DAC used.

Display resolution determines how many pixels can be projected onto the monitor at any one time. (Actually, only one pixel is displayed on the screen at a time, in rapid succession). Table 1 shows commonly-used screen resolutions corresponding to various applications.

However, since each pixel must correspond to a memory element, the more pixels per screen the faster the DAC and video RAM must be in order to write the information to the screen fast enough to avoid flicker. This imposes speed requirements that have to be satisfied.

The other type of resolution, bit resolution, depends on the type of DAC used. The number of bits converted also determines the size of the color palette which is the number of possible colors that can be displayed. This should not be confused with the number of colors displayed at once (see Section on Color Look-Up Tables). Assuming that the monitor is an RGB-type, the bit resolution, n, must be multiplied by 3 to get the total bit resolution, 3n. Taking this number as 2^{3n} gives the size of our color palette. Table 2 shows common bit sizes for video DACs with their corresponding palettes.

It should be clear that, if imaging is the goal, a higher bit resolution gives access to the assorted tones and mixtures of colors that make color graphics as realistic as possible. The major problems associated with higher-resolution DACs are that they are larger and more complex than lower-resolution DACs and tend to take longer for their signals to settle. This has a direct effect on selection of the proper DAC for a particular system because of the DAC's bandwidth and because of the need to weigh advantages and disadvantages of higher and lower bit resolutions.

For a low-end personal computer graphics screen on which the pixels can actually be seen at arm's length, it makes little sense to have a bit resolution that shows flesh tones because the benefit of the large palette is defeated by a screen that shows jagged edges. On the other hand, having a high screen resolution with a limited amount of colors does not defeat the purpose in the same way — if many colors aren't needed.

Integrated circuit layout, for instance, may not require thousands of colors — only enough to distinguish 12 – 15 masks; but sharply defined edges and zooming ability are needed to examine the circuit. The need for this user could be a bit resolution of 2 (64 colors) and a display resolution of 1024 × 1280.

For all this talk of colors and bit resolution, monochrome should not be totally ignored. After all, people got along fine with black and white TV for years before color came along. For applications such as word processing or

Table 1. Display Resolutions With Applications

DISPLAY RESOLUTION	APPLICATION
250 × 500	Low-end personal computers (home computers)
640 × 480	High-end personal computers
600 × 800	Next-generation personal computers
768 × 576	Next-generation personal computers
1024 × 800	Workstations
1024 × 1024	High-end workstations
1024 × 1280	High-end graphics terminals (CAE/CAD)
1024 × 1500	High-end graphics terminals (3-D Imaging)
1500 × 1500	High-end graphics terminals
2048 × 2048	High-end graphics terminals (photo quality)

Table 2. Bit Resolution With Palette Size

BITS/DAC	RGB	PALETTE SIZE	APPLICATION
1	3	8	Digital RGB, "rainbow colors"
2	6	64	Some home and personal computers
4	12	4096	Color workstations, CAD/CAE
6	18	262,144	High-end CAD/CAE, medical imaging
8	24	16,777,216	Photographic quality reproduction

Table 3. Display Resolution With Minimum DAC Speed

DISPLAY RESOLUTION	# PIXELS	MINIMUM DAC SPEED
250 × 500	125,000	10MHz
640 × 480	308,000	25MHz
600 × 800	480,000	38MHz
768 × 576	443,000	35MHz
1024 × 800	820,000	65MHz
1024 × 1024	1,049,000	85MHz
1024 × 1280	1,311,000	105MHz
1024 × 1500	1,536,000	125MHz
1500 × 1500	2,250,000	180MHz
2048 × 2048	4,195,000	330MHz

circuit design, monochrome is fine. To achieve different shades of black and white, no chrominance operation is necessary. All of the bit resolution can be done with one DAC to operate on the luminance, or brightness signal. In this case, the brightness resolution can be said to be 2^n. Remember, the decision to go with color or monochrome does not rest upon the designers of the graphics board. A monitor is either color or monochrome to begin with. Adding a color video DAC won't change that.

DAC Speed

The DAC's update rate or bandwidth is a crucial consideration in choosing a DAC if the type of monitor has already been specified. For raster-scan systems, a few calculations can be made to determine the minimum speed required for the DAC.

First of all, assume that the screen needs to be refreshed at 60Hz to avoid flicker. To account for the electron beam going back to the top to start the next frame, assume that the retrace time is 30% of the drawing time. Multiply the frame rate by 1.3 to account for the retrace. Thus, the minimum bandwidth for the DAC would be determined by the following formula:

Speed (Hz) = 1.3 (retrace factor)
× # pixels × 60Hz (frame rate)

For the screen resolutions noted earlier, a new table can be generated for the minimum DAC speed required (see Figure 8).

For the 60Hz frame rate, the screen is probably not interlaced. Interlacing the screen at 30Hz would give the same effect because interlacing gives the *illusion* that the screen is being refreshed at a faster rate. The DAC would only have to operate at a quarter of the speed of the 60Hz non-interlaced rate because only half of the lines are being drawn at a speed that's half the 60Hz frame rate. This is how scanning operates under the NTSC television standard. The FCC says that televisions can't refresh the screen faster than 30Hz, so interlacing was developed to get around it. There are no such restrictions in graphics monitors. In fact, there are monitors that have horizontal scan rates as much as 4 times faster (65kHz) than that for television (15.75kHz).

Color Look-Up Tables: Yes or No?

As mentioned in the Bit-Mapped Graphics section, graphic systems may have direct conversion from a bit-map or they can use color look-up tables (CLUTs). It should be pointed out that one is not necessarily faster than the other. Speed depends primarily on the system. A fast CLUT is of no use if the external frame buffer can't load a new set of colors into the CLUT during the retrace time (horizontal or vertical). A video DAC without the CLUT may be faster since it can bypass the memory accesses needed for the CLUT, but, as seen in the Bit-Mapped Graphics section, the extra cost of the bit-planes (1 million additional bits for a 1024 × 1024 display) may be excessive, and accessing the additional planes may produce some design problems.

If a CLUT is needed, the size of the CLUT should also be a major consideration. Each bit-plane added requires 2^n more memory cells. Constraints on die-size and power requirements become apparent. Also, one must ask whether one needs 16, 32, 64, 128, or 256 colors on every line. This depends on the color resolution desired *for the entire screen*. An easy way to determine the system needs is to picture the most common scene that would be displayed. The general rule is that the more complex and three-dimensional the images that are required, the more variations and shading are needed to truly represent them. Conversely, if the image is simple and two-dimensional, fewer colors would be needed. An example of the former would be geological formations. For the latter, consider the colors of flags of the world's nations. Almost all of them can be displayed with a CLUT of 16 colors. Remember, this refers to the number of colors needed at any one time.

No flag has more than 16 colors. The range of colors available for display after CLUT refresh depends on the color resolution or the number of data bits for each pixel.

Gamma Correction

A problem encountered in both television systems and in display monitors in general is the gamma effect. This is due to the nonlinear relationship between light output and the signal voltage applied to a cathode-ray tube. Although it would be desirable to have the luminous output of the phosphors on the display to vary directly with the changes in the signal applied to it, they usually do not. Each monitor has its own characteristic, but the international convention is to assume that the fractional value of the luminous output can be approximated by raising the percentage of display signal input to the 2.2 power. For example, a 60% of full-scale input signal will result in 33% of the full-scale luminous output ($0.6^{2.2} = 0.33$).

In Figure 6, the monitor does not respond linearly for a linear input signal. Adding a gamma correction circuit can take care of this problem.

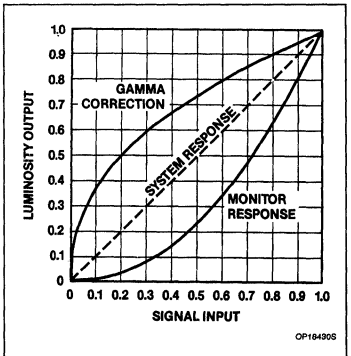


Figure 6. Monitor and System Response With Gamma Correction

In the television industry, correction for this non-linearity takes place at the camera as the image is recorded. The camera takes the 2.2 root of its full-scale fractional value. This cancels the gamma effect and produces a linear system response.

In graphics systems for which the image is generated from digital information, DACs convert the digital information into a voltage that drives the guns of the CRT. Basically, the systems designer has three choices:

1. Correct for gamma in the software. This can be done by using the 2.2 power/root compensation to pixel values before they are stored into the frame buffer. This could be an expensive addition to the software and might slow the overall system because of the added computation time.
2. Apply analog gamma correction in the hardware. The correction factor could be done with additional circuitry to the output of the DAC before it drives the monitor. As mentioned before, this presents an additional hardware overhead. This is not done, however, without some risks. Since every monitor has individual characteristics, the resulting correction would not look the same on every monitor.
3. Ignore the whole subject and accept the non-linearity of the luminous output as a characteristic of the system. Since most graphics applications are for the generation of images for specific problems and not for the lifelike reproduction of scenes (although it would be desirable), a gamma correction mechanism is unnecessary.

This last approach seems to be the most prevalent solution since few, if any, DACs contain gamma correction circuitry. When graphics software designers select their colors, they do so for the best visual performance. This fine-tuning for colors and shading is really software gamma correction because they can select the digital information needed for colors and intensity and see the results from the other side of the monitor.

CIRCUIT FEATURES AND OPERATION

This section covers the basic features and operation of the NE5150/51/52. The first two sections briefly discuss RS-170 and RS-343A, the standards for color and monochrome video systems. The next section covers the composite video signal (CVS) that is specified in the two previous standards.

RS-343A and RS-170

RS-170, the Electrical Performance Standards for Monochrome Television Studio Facilities, and RS-343A, the Electrical Performance Standards for High Resolution Monochrome Closed Circuit Television Cameras, were issued in November 1957 and September 1969, respectively, by the EIA (Electronic Industries Association). The specifications outlined in RS-343A determine the voltage levels required for the part.

Composite Video Signal

Shown in Figure 7 is a section of a composite video signal. With the exception of the BRIGHT function, the levels and tolerances are specified by RS-343A.

Sync, Blank, and Setup

The sync signal is situated 286mV (40 IRE) below the blanking level which lies 714mV (100 IRE) below the reference white level (next section). The sync signal synchronizes the monitor horizontal and vertical scanning. This, and the rest of the composite video signal, is not to be confused with the composite sync signal which is often used for a combined horizontal *and* vertical sync signal.

The blank level lies just below the reference black level, separated by an amount known as the setup. The difference between reference white and the blanking level is defined as 100 IRE. Applying the blanking level voltage to the monitor input will reduce the CRT electron beam current so that there will be no visible trace of the electron gun on the phosphor.

For television, the setup is defined as the *ratio* between the reference white and the reference black level measured from the blanking level. It is usually expressed as a percentage. Basically, it's the difference between the reference black level and the composite blanking level. RS-343A has set the limits of the setup as 7.5 ±5 IRE. Any value between 2.5 to 12.5% of the blanked picture signal can be designated as the setup (2.5 – 12.5 IRE or 17.85 – 89.25mV). Since the full-scale range of the video signal represents 100 IRE, a percentage of the signal is synonymous with its IRE value. For the NE5150, the setup is 71mV or 10 IRE.

Reference Black and White

Reference black and white correspond to the signal levels for a maximum limit of black and white peaks. White corresponds to having all color guns on and black to having all guns off. The gray scale, which refers to the rest of the color values and contains a majority of the signal information, is defined by the amplitude between reference white and reference black. Since the reference white to blanking level is fixed at 100 IRE, the reference black level is determined by the setup. Since the setup can be between 2.5 and 12.5 IRE, the gray scale range must reflect those tolerances and so has a range of 92.5 ±5 IRE (660.5mV ±35.7mV).

To allow for a BRIGHT function, the NE5150/51/52 family of video DACs were designed for a full-scale range (blank to reference white) of 675mV (about 94 IRE) and a gray-scale range of 643mV (about 90 IRE). Using the BRIGHT function adds 71mV (10 IRE) to the reference white value.

For instance, in a 12-bit system like the NE5150/51/52, using 4 bits/DAC would enable us to resolve the gray scale range into 16 parts. For the NE5150, that would be about 40.1mV (5.6 IRE) = 1 LSB. For 6 bits, 64 parts could be resolved, and for 8 bits, 256 parts.

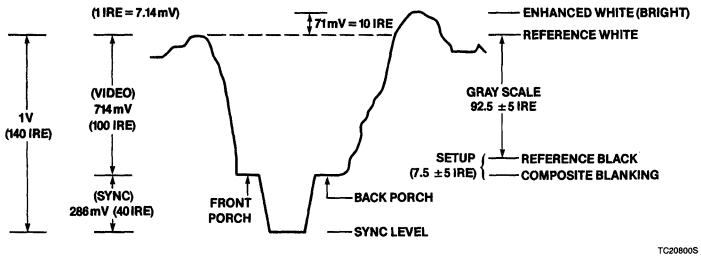


Figure 7. RS-343A Video and Sync Levels

NE5150/NE5151/NE5152 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT[3]	CONDITION
1	X	X	0	X	X	-1031mV	SYNC[1]
1	X	X	1	X	X	-960mV	Enhanced SYNC[1]
0	1	X	0	X	X	-746mV	BLANK
0	1	X	1	X	X	-674mV	Enhanced BLANK
0	0	1	0	X	X	-71mV	WHITE
0	0	1	1	X	X	0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	-674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	-603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	-71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	0mV	Enhanced WHITE (EZS)

NOTES:
1. Green channel output only. RED and BLUE will output BLANK or ENHANCED BLANK (BRIGHT ON) under these conditions.
2. For the NE5150/5152, the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.
3. Note output voltages in Logic Table are referenced to V_{CC} for the NE5152 only.

Device Description and Operation

Corresponding to the RS-343A requirements outlined in the previous section, the logic table indicates the output voltages given the digital inputs shown. Although the output voltages for the DACs are shown, the user should also know what is happening to the circuit and how the priority given to each function influences the output. [All ones (1111) is called zero-scale (ZS) and all zeroes (0000) is called full-scale (FS).]

The BLANK command presets all the latches to all zeroes (0000) and sends the output to its blanking level of 100 ± 5 IRE below reference white (-71mV) or about -746mV. When BRIGHT is on (a '1'), the output is raised 10 IRE (71mV or 1/9th of full-scale) to -674mV. BLANK overrides WHITE and is overridden by SYNC.

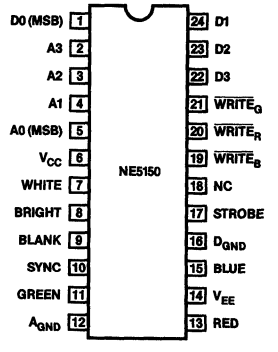
The WHITE command presets the latches to all ones (1111) and outputs -71mV to all DACs. When the BRIGHT command is on, this value is raised to 0V. WHITE will be overridden by both SYNC and BLANK.

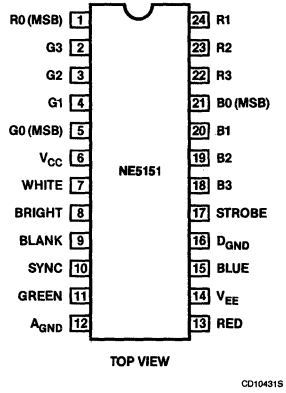
The SYNC command presets all of the latches to zeroes and turns on the BLANK switch. In addition, it turns on a 40 IRE switch (drops voltage 286mV) in the GREEN channel only. So the GREEN channel sits at 140 IRE down and the RED and BLUE channels will be 100 IRE below ground.

The BRIGHT command turns off one current switch within the circuit and adds 10 IRE (71mV) to the output levels of all three guns. This comes in handy if using a cursor (optional blinking) to brighten other parts of the screen. This switch cannot be overridden by any other switch.

Referring to the pinouts of both the NE5150/52 and the NE5151 (see Figure 9), there are additional considerations.

The $\overline{WRITE}_G$, $\overline{WRITE}_R$, and $\overline{WRITE}_B$ pins are the write enable pins for each of the 16 × 4 memories in the CLUT. When these pins are pulled High, the memory is then in the READ mode. This is the normal mode of operation. To write to the memory, **one** of the pins must be pulled Low. The data on D0 - D3 will then be written to the memory location A0 - A3 of the corresponding WRITE pin.





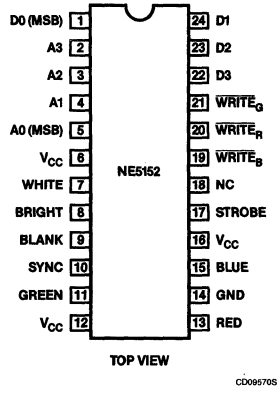


Figure 8. Pinouts of NE5150/52 and NE5151

STROBE is the main system clock and synchronizes all digital operations on the DAC.

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NE5150/51/52 Family of Video Digital-to-Analog Converters AN1081

The strobe is ECL and TTL compatible and demands no special drive requirements. The positive edge of STROBE clocks the latches.

The GREEN, RED, and BLUE pins are the analog outputs of the DACs. The DACs are voltage output and need no external components (75Ω resistors are on-chip). The output voltage range is approximately 0 to −1V and is independent of the input logic (either TTL or ECL).

The DATA and ADDRESS bits are designated so that D0 and A0 represent the most significant data and address bits (MSB), respectively. Similarly, D3 and A3 correspond to the least significant data and address bits (LSB). Since the NE5151 has no CLUT, there is no need for the address pins (4) or the write enable pins (3). Adding the NC (no connection) pin (1) gives the eight additional input pins for two 4-bit DACs. The original data bus now carries the logic for the RED gun.

Analog and digital ground (A_{GND} and D_{GND}) should always be connected together in any configuration and should not have more than 50mV of potential between them to insure proper operation of the device. The next section will cover connection of V_{CC} and V_{EE}, in addition to A_{GND} and D_{GND}, on different system configurations.

Using Different Logic and Supply Voltages

Different users have different needs. Some have access to dual supplies, other only to single-ended supplies. Signal logic may be TTL or ECL. In any case or configuration, the NE5150/51/52 family can be used. The following configurations cover most cases.

Explanation of the configurations are as follows:

A. Case A shows a basic ECL configuration for the NE5150 and NE5151. The signal voltage is basic ECL with a −1.3V threshold and is powered from ground and −5V (or −5.2V). Since the TTL buffers are no longer needed, V_{CC} is tied to analog and digital ground (A_{GND} and D_{GND}), excluding the buffers from the circuit.

B. In some cases, people use ECL logic but run it off a single supply, +5V and ground. In this case, operation is the same except that the supplies are shifted up 5V. In this new ECL mode, the threshold −1.3V is moved up by 5V to +3.7V. ECL operation is not available for the NE5152.

C. For TTL operation in the NE5150 and NE5151, dual supplies are normally needed. If available, standard TTL-level signals with a +1.4V threshold (between a logic '1' Low of 2.0V and a logic '0' High of 0.8V) can be connected directly.

D. In some situations, a dual supply is not available. Single-supply TTL operation is made possible by making similar connections and by pulling up the inputs of each pin with a 10kΩ resistor connected to V_{CC} = +5V. This is necessary because the threshold is now 3.7V.

E. Case (D) necessitated the construction of the NE5152, which has only one mode using a single 5V supply and accepts TTL inputs. A_{GND} and D_{GND} become V_{CCA} and V_{CCD} and are tied to V_{CC}.

In some cases, a single supply is used and the internal ECL mode has been shifted up to the positive supply; the output voltage will be swinging from 0V to −1V, but, referenced from V_{CC} = +5V, it will swing from 5V to 4V. If the monitor accepts only positive sync pulses or video information, DC-offsetting the outputs or AC-coupling them with 1μF capacitors would make the signal acceptable to the monitor.

Since the outputs have internal 75Ω resistors, the monitor should have a 75Ω resistor to ground in order to doubly-terminate the cable and to prevent reflections.

Unused Inputs

For ECL mode (NE5150), any unused inputs, regardless of desired permanent stage, should be tied to a fixed-level output of an unused gate.

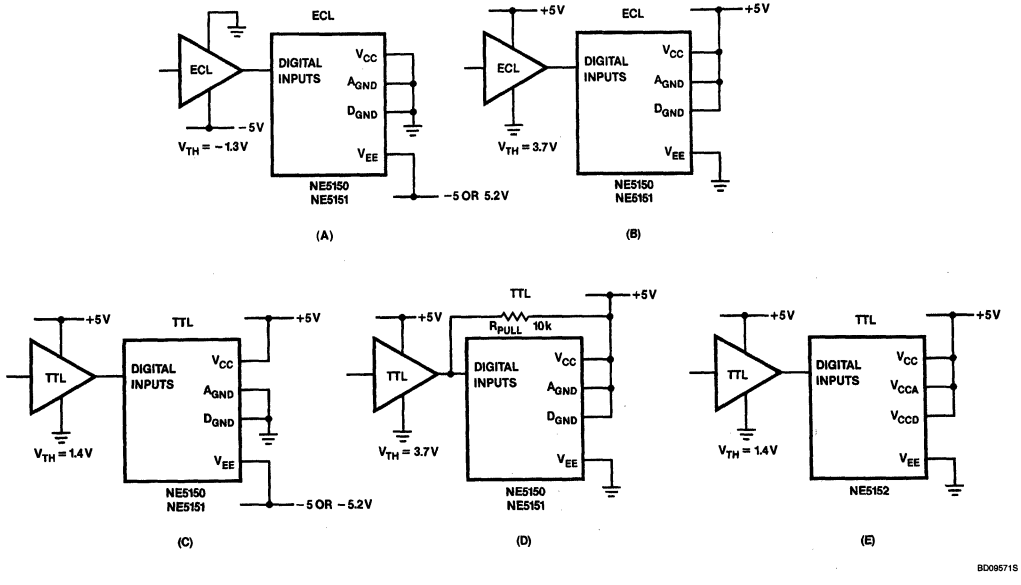

Figure 9. Video DAC Modes of Operation

BLOCK DIAGRAMS

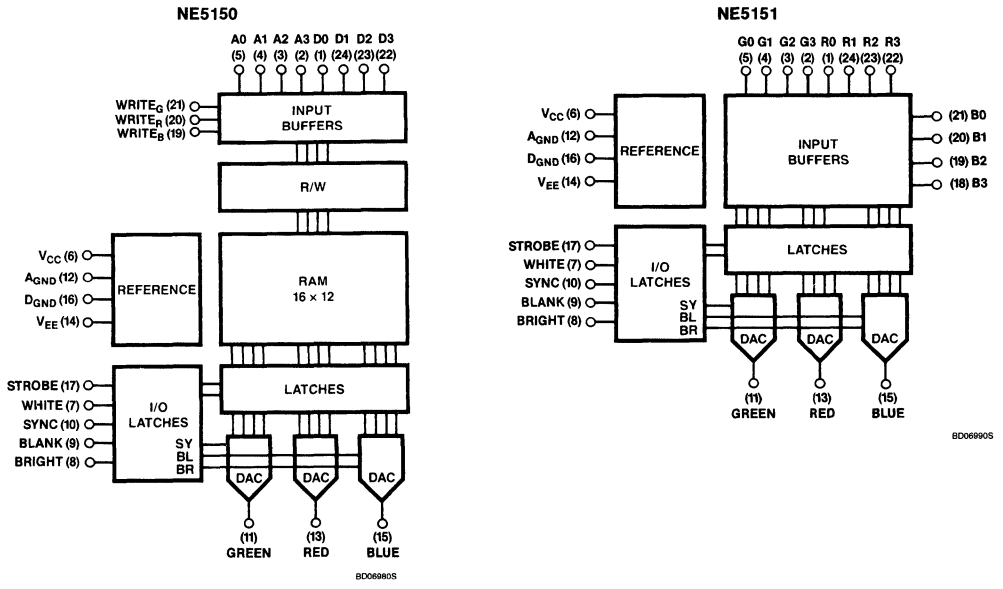

Figure 10. NE5150/51/52 Block Diagrams

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Circuit Description

As can be seen from the block diagrams in Figure 13, the only difference between the NE5150/52 and the NE5151 is the lack of a color look-up table on the NE5151. Bypassing the CLUT with its assorted address decoding, sense amplifiers, and read/write logic enables it to not only use 200mW less power, but also to increase its update rate to 150MHz.

The NE5151 is basically the same die as the NE5150/52, with the exception of a metal mask option that permits it to bypass all of the circuitry associated with the CLUT. It is also bonded differently to enable all 12 bits to be loaded into the DAC at any one time instead of being multiplexed 4 bits at a time to the NE5150/52 CLUT.

DAC Reference

The need for separate references for the DACs resulted from the problems associated with glitching and crosstalk between the DACs. When one DAC maintains a constant value through pixel updates, while another undergoes major transitions such as the 1111 to 0000 on/off switching of currents through the DAC, feedthrough can be expected if all 3 DACs derive their reference voltage from the same source. Having separate references solves this problem. It also isolates the DACs from each other and the other parts of the circuit.

The reasons for choosing the DAC shown in Figure 12 are its simplicity, the bandgap's insensitivity to temperature variations, and its excellent supply rejection (PSRR) through high frequencies. It consists of a PTAT current source supplying a bandgap reference. The output of the bandgap is approximately −1.2V.

To provide the bias for the different current sources on each of the DAC stages, the circuit uses a control amplifier that provides negative feedback to maintain its stability. BIT and its complement drive the differential pair that (along with QS2) makes up one part of the DAC. The bandgap drives the current sources through the control amplifier. If the bias line voltage should rise or fall, the negative feedback in the QS1 and QS3 current path would correct for it.

The control amplifier consists of a transconductance stage driving an emitter-follower. The output of the emitter-follower provides a low-output impedance line that drives QS4. The inclusion of QS4 prevents switching transients from degrading settling time. The control amplifier has a 60MHz unity-gain bandwidth, providing power supply rejection up into the VHF range.

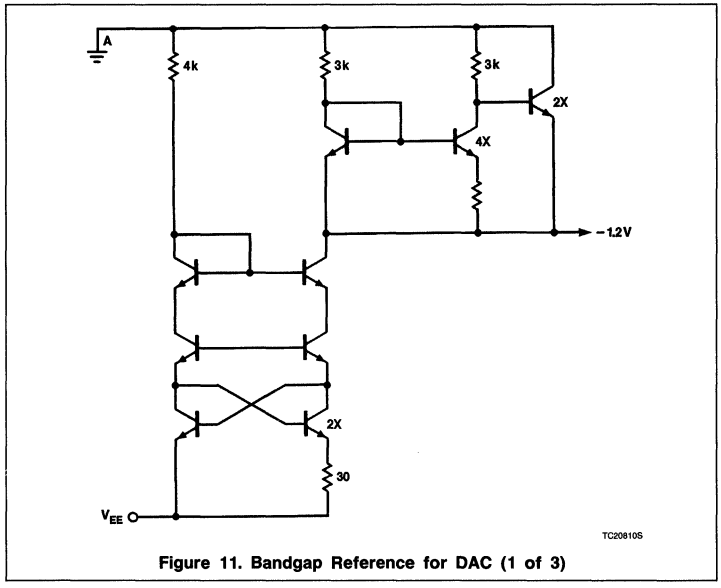


Figure 11. Bandgap Reference for DAC (1 of 3)

Digital-to-Analog Converters

The three DACs consist of differential pairs that are switched on or off depending on the value of the bits. Each of the transistors switches a different amount of current depending on the significance of each bit (see Figure 13). Although only one transistor is shown for each bit, the circuit actually has several transistors in parallel to get the required current. In this case, B3 is the least significant bit since it switches the least amount of current and would produce the smallest voltage drop across the 75Ω load resistor. The reverse is true for B0, the most significant bit, since it draws the most current.

So for all bits low, 0000, all of the current would go through the load resistor, bringing the output voltage to its lowest point. If all three DACs are low, this would correspond to reference BLACK. All bits high, or 1111, shunt current away from the load and leave the output voltage at reference WHITE. Different combinations of bits give 16 values between WHITE and BLACK. One additional 2mA switch is turned on by the input value of BRIGHT, which level-shifts the output by 1/9th the full-scale value, or about 10%. The BLANK and SYNC pins work in a similar manner. Refer to the Logic Table beside Figure 8 for the output voltages for each of these functions.

Some of the problems associated with DACs can be attributed to switching glitches, usually measured in terms of glitch energy. Glitching occurs when digital switching of the transistors causes spikes onto the collectors of the current sources to each of the differential pairs. These current spikes charge the collector-base capacitance, C_{JC}, of the collector transistor, and result in a slower settling time. The asymmetrical turn-on/off behavior of bipolar transistors and mismatched load bit-wiring capacitances also contribute to glitches. This can also be seen as an overshoot of the waveform, a "glitch" on the rising or falling edge of what should look like a square wave. Signals that overshoot the desired analog output level consequently take longer to settle to their final value. The measure of this overshoot is the glitch energy, usually given in pV-sec. The units do not actually work out as units of energy or Joules, which is C-V (Coulomb-Volts), but result from measuring the area of the glitch [Area = Height (V) × Width (psec)].

The NE5150/51/52 resolves this problem by putting the current sources in series with another set of transistors (see Figure 14). The stage below the differential pair is then biased by a low-impedance line which reduces the effect of the current spiking. The biasing for the lower transistor comes from the control amplifier mentioned in the DAC Reference Section.

Video DAC Timing

For the NE5150 and NE5152, the presence of the memory dictates both a READ and a WRITE cycle, whereas the NE5151 needs only one diagram. The explanation of each of the waveforms can be found in the timing glossary. For the guaranteed specifications, the user is referred to the data sheet.

NE5150/52 (With CLUT)
In the NE5150/52 READ cycle, the COMPOSITE signal refers to either the WHITE, BRIGHT, BLANK, or SYNC signals. The read composite hold time, t_{RCH}, is defined from the rising edge of the strobe to the end of the composite pulse. This is the required time the composite signal must remain on the bus for latching. The time between the end of the composite pulse to the next rising edge of the strobe defines the read composite setup time, t_{RCS}. This is the same as the read address setup time, t_{RAS}. The read DAC delay time, t_{RDD}, is the propagation time of the signal through the device clocked from the strobe to the 50% change of the DAC output.

In the WRITE cycle, t_{WAS}, the write address setup time is defined by the start of address to the falling edge of the write enable strobe. At the end of this time, data can be written to the CLUT. Both ADDRESS and DATA must remain latched until they reach the rising edge of the WRITE ENABLE. This defines the WRITE ENABLE pulse width, t_{WEW}. The data should also be latched at the same time as the address. The start of the data (and address) to the end of the write enable pulse is defined as t_{WDS}, or the write data setup time. After the write pulse finishes, an address and data hold time is also specified.

NE5151 (No CLUT)
Since the NE5151 has no memory for the signal to propagate through, it typically has a faster conversion time. As can be seen from the pinouts, the three 4-bit words enter the DAC simultaneously as opposed to the sequential 4-bit loading scheme used in the NE5150/52. With no memory, there's no need for READ or WRITE cycles and so there is only one standard timing diagram. (See Figure 16).

This timing diagram is similar to the READ cycle of the NE5150/52 with the exception that addresses are not clocked to the CLUT; instead, data bits are sent directly to the DACs. In this case, t_{DH} is analogous to the address hold time in the NE5150/52. All other definitions are analogous to the earlier READ case.

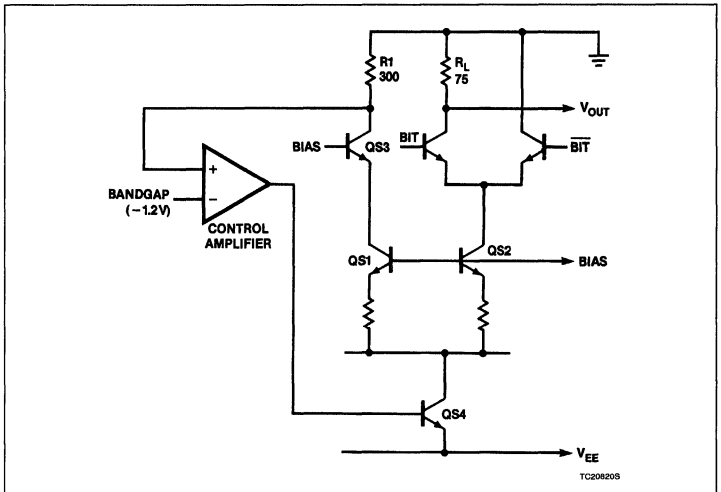


Figure 12. Negative Feedback Referenced to Bandgap

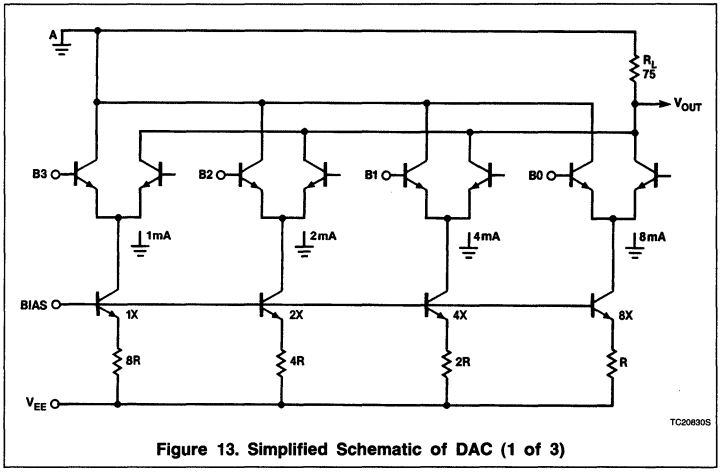


Figure 13. Simplified Schematic of DAC (1 of 3)

WORKSTATION APPLICATION

Introduction

This section describes the design of a color graphics interface for the Modula, Inc. Lilith Workstation. The workstation initially loads 16 colors (it only requires 16) into the NE5150's color look-up table. After the colors are loaded, the workstation then generates addresses to the look-up table. The entire color range (4096) is not required in this application.

The LILITH Workstation
The Lilith Workstation is a 16-bit workstation manufactured by Modula, Inc. It was originally designed by Niklaus Wirth and his students at the Swiss Federal Institute of Technology (ETH). The Lilith is a Modula-2 computing engine. In its original package, the Lilith includes 256kB of memory, a 15MB Winchester disk drive, a floppy disk, a mouse, and an 832 × 640 monochrome graphics tube.

The Signetics Logic Design Group in Orem, Utah, has modified the Lilith by adding 2MB of memory and a high-resolution 1024 × 1024 color monitor. The changes made to the Lilith graphics section comprise the bulk of this application description. Benchmarks of the modified workstation have shown that its performance on applications ranging from matrix multiplications to complete circuit analysis is approximately half as fast as a VAX 11/780 minicomputer. In addition to the circuit simulator used, the Signetics-modified Lilith also supports a layout editor, SLED, that uses about 10,000 lines of Modula-2 source code. More detailed information on the Lilith can be obtained from the manufacturer and from the articles listed in the reference section.

For the purposes of this application, it is sufficient to know that the Lilith contains a 16-bit data bus for interaction with the SCC63484 Advanced CRT Controller and a

14-bit bus that is used to initialize the color look-up table in the NE5150 video DAC. Read/write, I/O lines, CLOCK, data acknowledge, and chip select signals are also sent to the SCC63484 for data and control purposes.

Software Aspects (Pascal and Modula-2)
Modula-2 is a superset of Pascal. Anyone with a working knowledge of Pascal should have no trouble programming a Lilith workstation or in understanding the initialization program outlined in this section. Some noteworthy features about Modula-2 and its influence on the architecture of the Lilith (the M-machine) is the fact that the Lilith instruction set (M-code) has only 256 carefully chosen instructions. This limits any instruction to a 1B length and increases the speed of operation. The Modula-2 language constructs map neatly to M-code. There are no excess instructions to add extra baggage. For additional details, the reader is referred to the August 1984 issue of BYTE magazine that contains several good articles on Modula-2.

Considering each '1' as ON and each '0' as OFF, the binary values for each color can be specified for each of the respective guns. Starting from the top, all guns OFF = BLACK. Similarly, all guns ON corresponds to word 7, WHITE. In the software definition module used to load the values, two constants were declared: black = 0 and white = 15. These correspond to the addresses shown in the table and were predefined because of their frequent use. Single guns completely ON give 1, 2, and 4 — the primary colors RED, GREEN, and BLUE, respectively.

System Hardware

The basic system configuration for the color graphics interface is shown below. The Lilith workstation sends data to the SCC63484 and the NE5150. The information sent to the NE5150 is the data for the CLUT initialization. Control signals are sent to the ACRTC. The ACRTC in turn controls the video DAC. The frame buffer sends and receives data (via an address/data buffer stage) to and from the ACRTC for video DAC addressing. The ACRTC also provides horizontal and vertical sync to the CRT while the video DAC supplies the video information. One stage not shown is the address and data buffering for the frame buffer and the pixel stage. This stage, in addition to assorted logic and timing chips, merely facilitates functionality between the major blocks shown in Figure 22.

The host microprocessor, system memory, and DMA control are local to the workstation and will not be described. The horizontal and vertical deflection sections are local to the CRT and will also be omitted. The rest of this section supplies an overall parts list and then describes each of the graphics blocks in somewhat greater detail. Although the actual pin numbers have been omitted, the functionality of each pin is shown for understanding. For actual pinouts and more detailed information, refer to the appropriate data sheet.

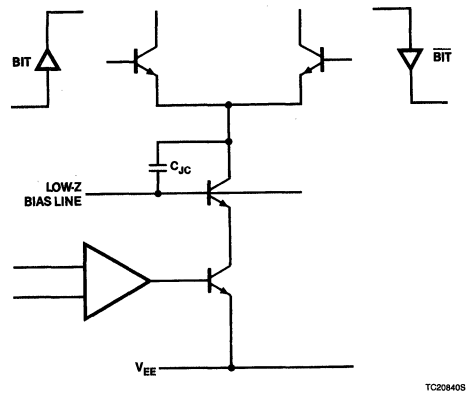


Figure 14. Low-Z Bias Line to Improve Settling Time of DAC

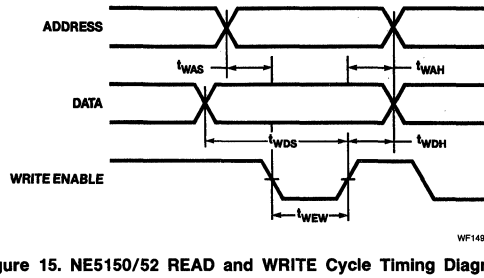


Figure 15. NE5150/52 READ and WRITE Cycle Timing Diagrams

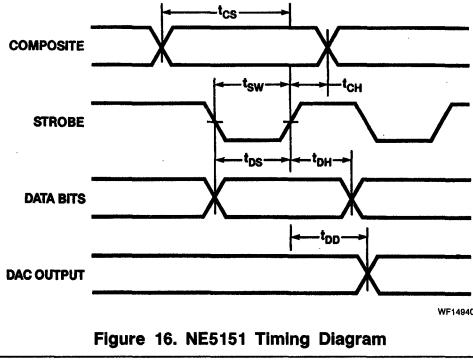


Figure 16. NE5151 Timing Diagram

Parts List

The following parts were used in the design of the color graphics interface (the actual quantity of each part is not listed). The "F" designation stands for Signetics FAST-type logic.

- NE5150 Video DAC
- SCC63484 Advanced CRT Controller
- MB85103-10 64k × 8 Dynamic RAM modules (Fujitsu)
- 7404 Hex Inverter
- 7432 2-Input NAND Gate

- 7474 Dual D-Type Flip-Flop
- 74123 Dual Retriggerable Monostable Multivibrator
- 74138 1-of-8 Decoder/Demultiplexer
- 74F139 Dual 1-of-4 Decoder/Multiplexer
- 74F157 Quad 2-Input Data Selector/ Multiplexer (Non-Inverted)
- 74F161 4-Bit Binary Counter
- 74F164 8-Bit Serial-In/Parallel-Out Shift Register
- 74F166 8-Bit Serial/Parallel-In, Serial-Out Shift Register
- 74F245 Octal Transceiver (3-State)
- 74F373 Octal Transparent Latch
- 7905 5V Voltage Regulator
- M1001 40MHz Crystal (MF Electronics)

PC Board Layout Considerations

Whenever dealing with high-frequency systems, analog or digital, care must be taken with PC board layout in order to insure good, reliable operation. Video DACs are hybrid devices in the sense that they are both analog and digital. They are also run at frequencies well into the RF range. This makes them especially susceptible to RF interference and different types of radiation. Signal traces should be kept as short as possible and 90° turns should be avoided. Power supplies should have adequate decoupling.

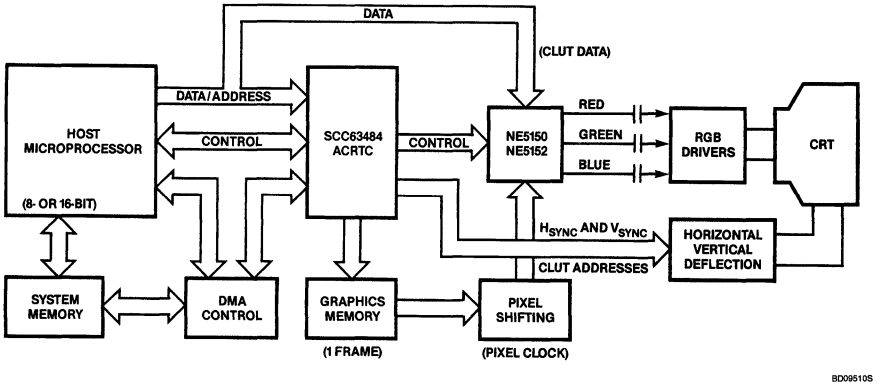


Figure 17. Block Diagram of Color Graphics Interface

More details are provided in the reference section under Reference Number 4, "Getting the Best Performance From Your Video Digital-to-Analog Converter".

Functional Description

The interface is designed to drive a Mitsubishi C-6919 or 6920 19-inch monitor. The monitor has 1024 × 1024 display resolution. Of these, 1024 × 768 pixels are actually drawn, giving us about 790,000 pixels, and, according to our earlier formulas, requiring a DAC with a conversion frequency of about 62MHz. That, however, assumes a non-interlaced display with a frame rate of 60Hz. This application uses a 30Hz interlaced display and so it needs only one-fourth that speed since it is drawing half as many lines at half of the frame rate. The pixel clock is derived from a 40MHz crystal. Other timing signals are also derived from the same crystal.

Table 4. Colors with Corresponding Bit Values

WORD #	COLOR	BLUE	GREEN	RED
0	BLACK	0000	0000	0000
1	RED	0000	0000	1111
2	GREEN	0000	1111	0000
3	YELLOW	0000	1111	1111
4	BLUE	1111	0000	0000
5	VIOLET	1111	0000	1111
6	TURQUOISE	1111	1111	0000
7	WHITE	1111	1111	1111
8	GREY	1010	1010	1010
9	ORANGE	0000	1000	1111
10	AVOCADO	0000	1010	1000
11	LIME	0101	1111	1111
12	NAVY	1111	1000	1000
13	ROUGE	1000	0000	1111
14	LAVENDER	1111	1111	1000
15	PEA	1000	1111	1000

NOTE:
The colors listed are for an application example only. The colors were randomly ordered and their gun and bit values in no way represent the de facto standard values or colors.

11

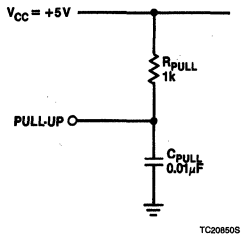


Figure 18. Circuit for Pull-Up to V_{CC}

The interface uses a 512kByte frame buffer that is organized as 64k by 64-bit words. Within each 16-bit block of memory (1 of 4 per word), there are 4 pixels of 4 bits each. Each bit supplies an address to the Color Look-Up Table in the Video DAC. The interface shifts out 64-bits or 16 pixels of information during each display cycle.

In each of the following schematics certain pins have been pulled up to V_{CC}, indicated by an arrow. For each arrow pointing to PULL-UP, the connection goes into the pull-up circuit shown below.

C_{PULL} is used for decoupling any power line ripple. Each point has a similar circuit.

ADVANCED CRT CONTROLLER

The Signetics SCC63484 is a state-of-the-art device ideal for controlling raster-scan-type CRTs. It is a CMOS VLSI system that can control both text and graphics. One of the advantages of this part is its ability to do on-board graphic processing in its Drawing and Display Processor, relieving some of the computational overhead from the Lilith.

Another attractive feature of the part is its flexibility. It has three different operating modes: character only, graphic only, and multiplexed character/graphic mode. In addition, it offers three scanning modes: non-interlace, interlace sync (this application), and interlace sync and video modes. With 2MB of graphic memory and a maximum drawing speed of 2 million pixels/second, it can supply the information to almost any type of high-resolution display (4096 × 4096 pixels maximum).

For additional information on the command set and a full listing of features, please refer to the data sheet and user's manual. This application note will concentrate on only the interconnections relevant to this application.

In this configuration (Figure 19), the SCC63484 Graphics Controller provides the horizontal and vertical sync pulses to the CRT and important timing pulses to the address and data buffers. It supplies timing to the frame buffer, the pixel-shifting stage, and to the frame buffer through direct and logical modifications made to the following system outputs:

1. MRD — Memory Read or the Bus Direction Control Line. This determines the bus direction for the Frame Buffer Data Bus.
2. $\overline{DRAW}$ — the Drawing/Refresh Cycle pin. This differentiates between drawing cycles and CRT display refresh cycles.
3. $\overline{AS}$ — Address Strobe. This provides the address strobe for demultiplexing the frame buffer/data bus (MAD0/MAD15).
4. MCYC — Memory Clock. Provides the frame buffer memory access timing. Equal to one-half the frequency of 2CLK signal.
5. $\overline{DISP1}$ — Display Enable Timing. This is a programmable display enable timing signal used to selectively enable, disable, and blank logical screens.
6. MAD0 – MAD15 — Address and Data Bus. Multiplexed frame buffer address/data bus.
7. MA16, MA17 — Address Bits/Raster Address Outputs. Gives the higher-order address bits for graphic screens and the raster address outputs for character screens. (lower 2 bits of MA16 – MA19).

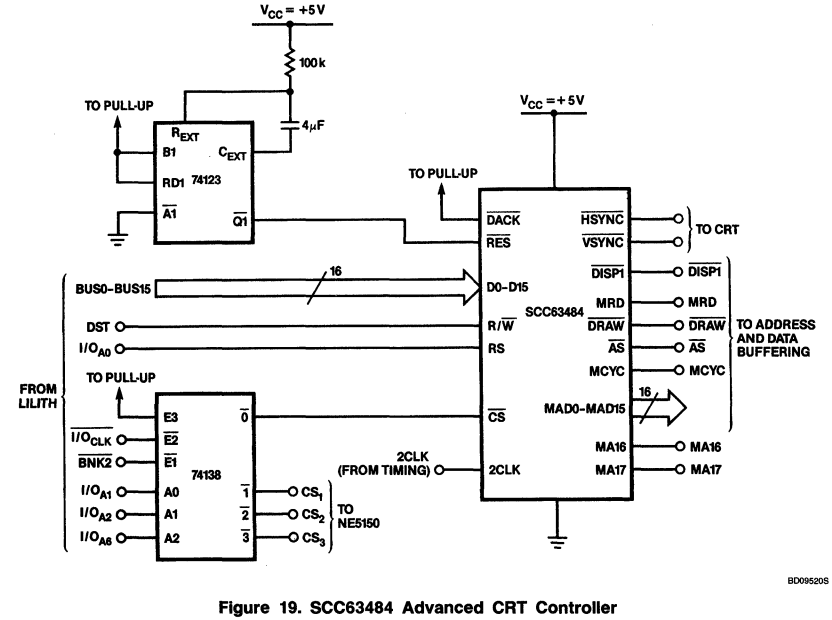


Figure 19. SCC63484 Advanced CRT Controller

The 2CLK signal provides the main clock input to the SCC63484 and is derived from the pixel clock (see System Timing).

The ACRTC also provides horizontal and vertical sync pulses directly to the CRT via the $\overline{HSYNC}$ and $\overline{VSYNC}$ outputs.

In Figure 19, the 16-bit bus of the Lilith is connected directly to the data inputs. The Lilith also provides a write signal (DST) to the R/$\overline{W}$ input. The first I/O line (I/OA0) is connected to the RS (Register Select) input. In addition, there is a high-order I/O bank select, three lower-order address lines, and a negative true I/O clock that, used with the 74138 Decoder, selects one of 4 devices: the ACRTC or 3 areas in the NE5150's color look-up table.

On the ACRTC, a 74123 one-shot produces a reset pulse ($\overline{RES}$) on power-up. The Data Acknowledge pin is not used and is pulled up to V_{CC}.

ADDRESS AND DATA BUFFERING

The address and data buffer stage provides an interface between the SCC63484 and the rest of the circuit. This stage takes the address/data lines MAD0 – MAD15 and separates them into two blocks. The 74F373 latches the upper bank for the addresses; this is the first bank. The second bank consists of 74F245 transceivers in the lower bank for the data.

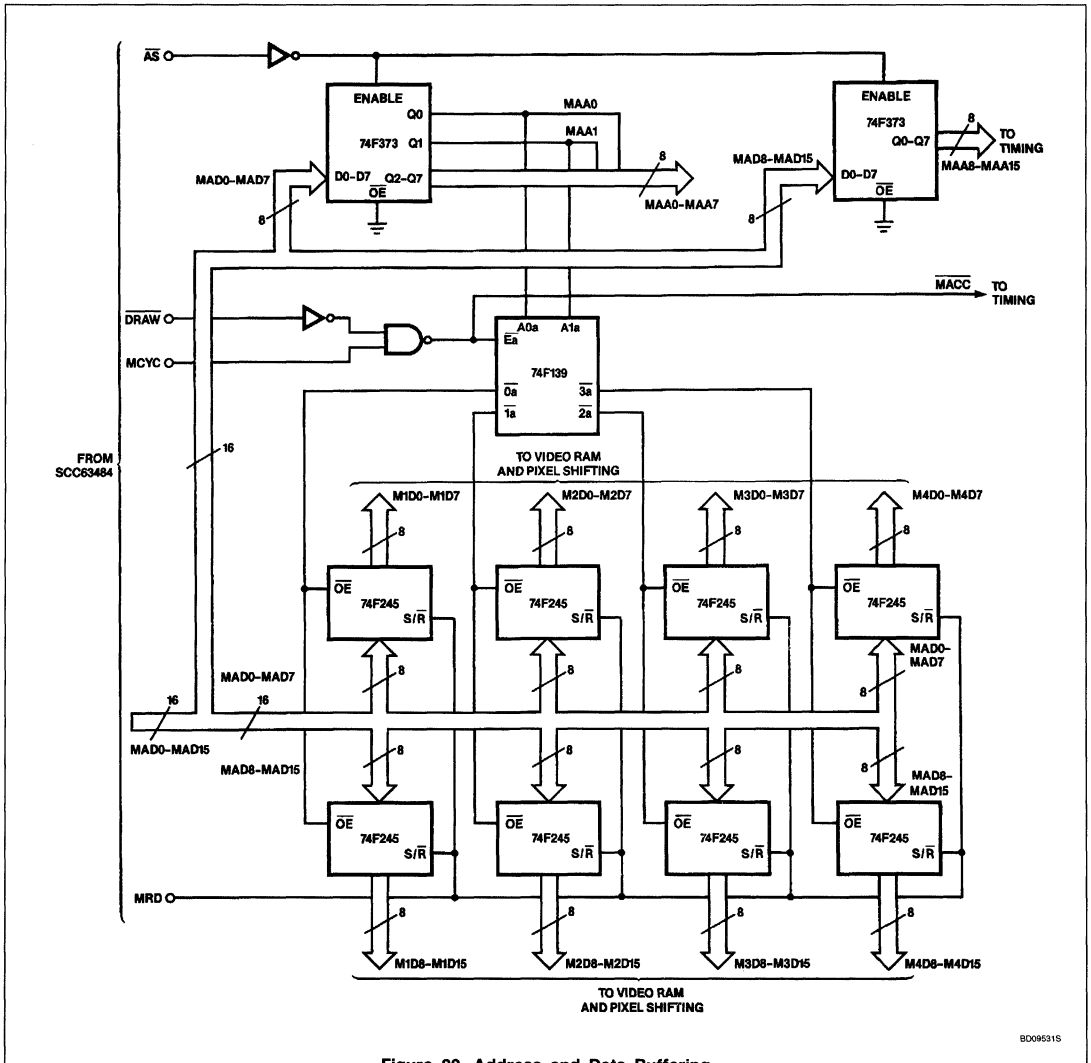


Figure 20. Address and Data Buffering

The 74F373s are used to latch the addresses at the beginning of every memory cycle. The latches are enabled by the $\overline{AS}$ signal coming from the ACRTC. Since the ACRTC is configured to increment its display addresses by four between display cycles, 4 words or 64 bits are shifted out every cycle. For modifying memory cycles, the two lower address lines are used to enable one of four sets of 74F245 transceivers (2 per set). Enabling is performed by the 74F139 Decoder. The signal that clocks the decoder is a combination of MCYC (Memory Cycle) and $\overline{DRAW}$, that results in a new signal, $\overline{MACC}$. This signal is also used in the timing block.

The transceiver outputs are now written into the frame buffer. From there, they will be sent to the pixel-shifting stage and then to the DAC. Each set of four 4-bit pixels in a serial string of displayed pixels is contained in a different block of memory. This is the reason the two lower-order address signals are used to select one of the four banks in the Video RAM (frame buffer).

SYSTEM TIMING

In a system as complicated as a graphics display board, the timing of the various elements grows exceedingly complicated as the number of components grows. It becomes even more apparent when the components are individual systems with their own set of timing considerations. In our case, this means the Lilith, the ACRTC, and the frame buffer.

Figure 21 shows the many elements it takes to generate the timing signals for the system. In the middle of the diagram, there are two 74F164 8-bit serial-in/parallel-out shift registers that count the timing states for the rest of the interface. The Address Strobe ($\overline{AS}$) signal, coming from the ACRTC, starts and ends this timing train. Because of the pulse width of $\overline{AS}$, many states at the end of the train are unusable. The video RAM $\overline{RAS}$ signal (Row Address Strobe) starts at the beginning of State 1, and terminates as $\overline{AS}$ goes Low, activating the register's MR (Master Reset). The precharge requirement of $\overline{RAS}$ is met by the $\overline{AS}$ pulse width.

The 74F157 Multiplexers are connected in such a way that the lower-order addresses are used for the video RAM row addresses (the 157 on top). At the beginning of State 3, the higher-order addresses are presented at the Video RAM address inputs as the column address. At State 5 the $\overline{CAS}$ signal becomes valid. Because of changes in the data hold (WRITE cycle) and data setup (READ cycle) of the ACRTC, the timing edge of $\overline{CAS}$ might have to be changed to insure proper operation.

MRD (Memory Read) along with a combination of MCYC and $\overline{DRAW}$ from the Address and Data Buffer called $\overline{MACC}$, are used with the two lowest-order address lines from the 74F373s (MAA0 and MAA1) to write-select one of the four memory planes (this memory plane runs orthogonal to the bit-planes discussed earlier). Because this signal comes well before the $\overline{CAS}$ signal, this qualifies as an early WRITE cycle, allowing the use of DRAMs with Data-In and Data Out signals connected together.

Using two flip-flops, the output of the lower shift register generates the PE (Parallel Enable) signal for the pixel-shifting stage. Because it is clocked from the fifth point in the shifter, this pulse occurs between States 10 and 11.

The upper left-hand corner of Figure 21 shows the creation of the 2CLK signal derived from the 40MHz pixel clock by using a 74F161 Counter that performs a divide-by-eight operation.

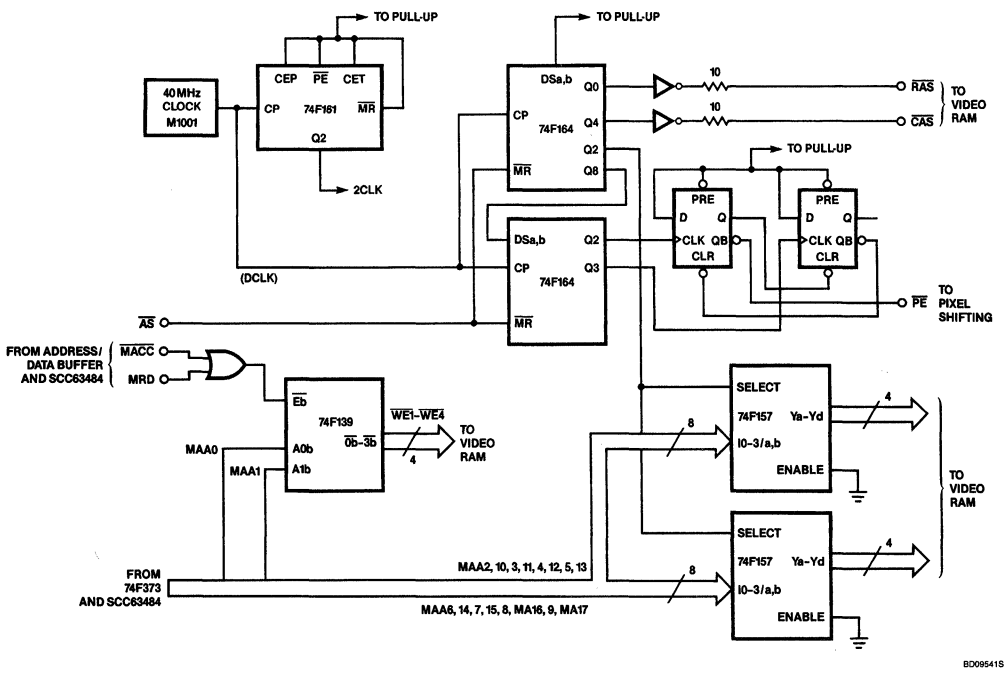


Figure 21. Components for System Timing

PIXEL SHIFTING

The pixel-shifting stage consists of 8 very fast 74F166 Shift Registers divided into 4 banks, one for each address bit. These shift registers have maximum operating frequencies of 120MHz.

The data comes from the address and data buffering and the video RAM. The $\overline{PE}$ (Parallel Enable Input) signal from the system timing block activates the register, while the pixel clock, DCLK, strobes each of the registers. All chips are permanently enabled by grounding their chip enable ($\overline{CE}$) pins. The master reset ($\overline{MR}$) is permanently disabled by tying it to a pull-up.

The connection between the registers and the memory is such that all the bits of each pixel are shifted out simultaneously before going to the 74F157 multiplexer. From there, they address the colors of the CLUT on the Video DAC.

VIDEO RAM

The phrase "Video RAM" refers to a set of dynamic RAMs used as the memory section in this application. It is not meant to be confused with the Video RAM which is a dedicated device for video applications.

The Video RAM or frame buffer section consists of 8 Fujitsu MB85103-10 modules. The 10 suffix signals a 100ns row access time. The cycle time is about 200ns, or about 5MHz. This is fine because only the pixel clock has to travel at the high screen draw speeds. These modules are SIPs (single in-line packages) and were used because of space considerations. Each module consists of eight 64k × 1-bit DRAMs, giving eight modules of 64k × 8 or a 64k × 64 buffer. This buffer is divided into four sections (64k × 16) that represent the four bits of address that are shifted out to the NE5150's CLUT.

One can see how the frame buffer is set up to shift out data to the pixel shifter. The memory is divided into 4 banks that are write-selected by the $\overline{WE1}$ – $\overline{WE4}$ pulses. Two modules (64k × 16 bits) make up one bank. This makes up the four 16-bit words that are shifted out. But where is the information for each pixel? Taking the 1st bank as an example, it can be divided into 4 quadrants:

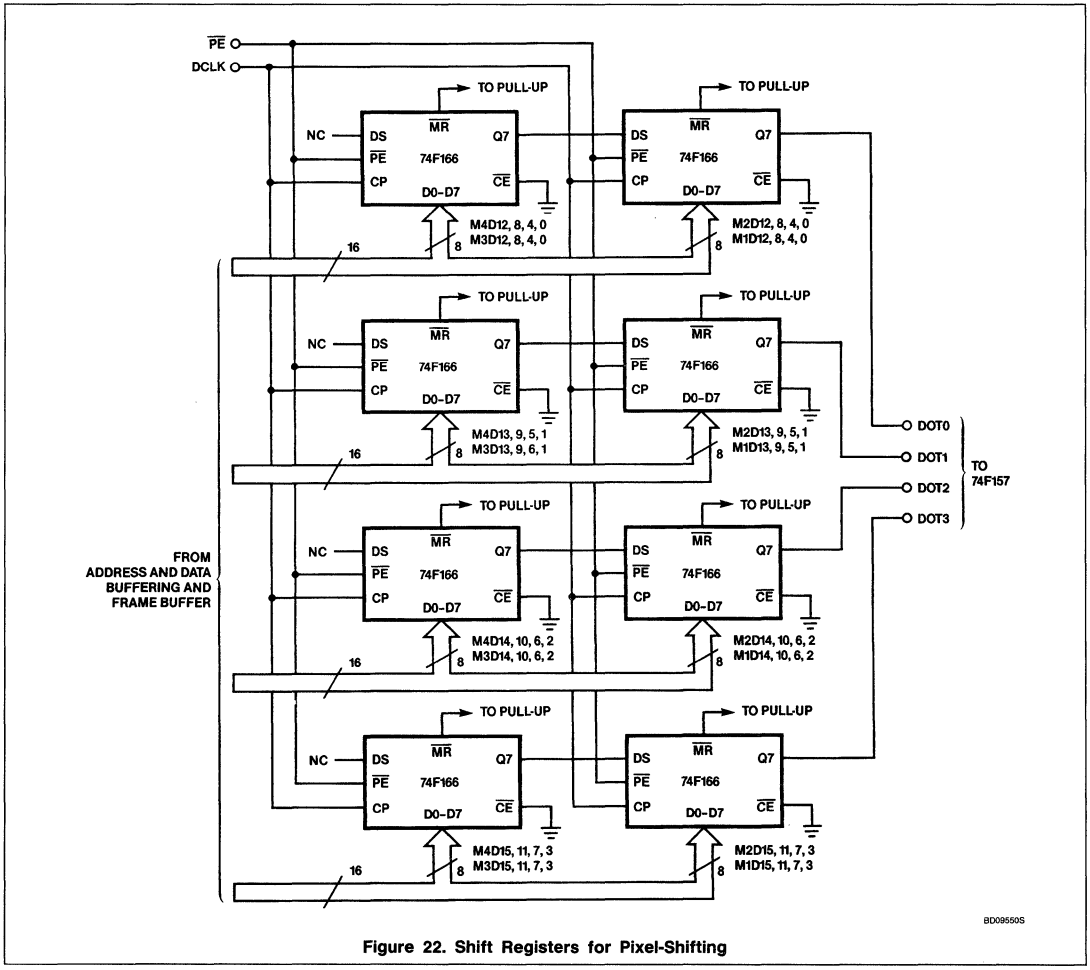


Figure 22. Shift Registers for Pixel-Shifting

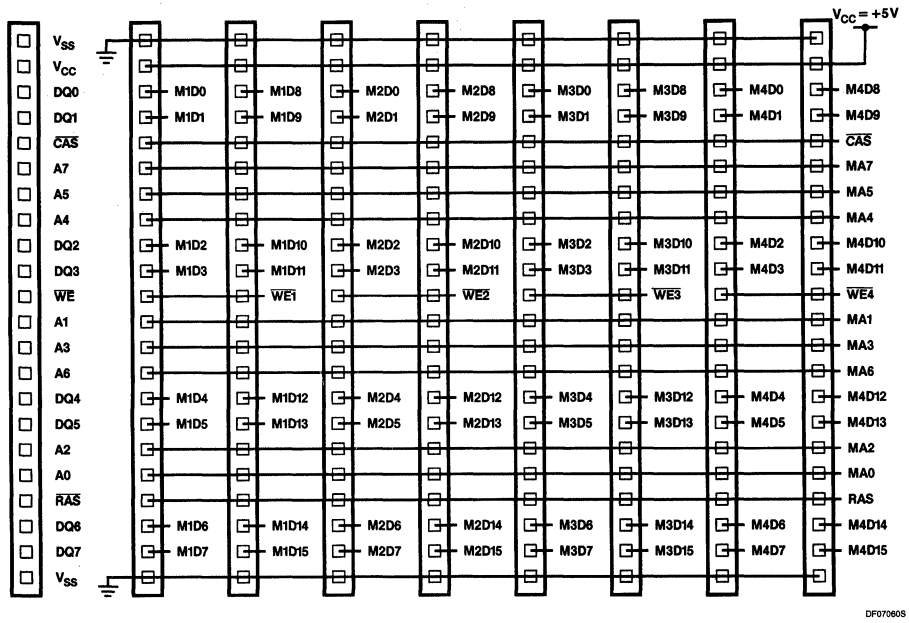


Figure 23. Memory Configuration to Store Pixels

M1D0 – M1D3, M1D4 – M1D7, M1D8 – M1D11, and M1D12 – M1D15. Each of these quadrants represents a dot. By tracking each dot in parallel back to the shift register in the pixel-shifting stage, they turn out to be each of the four quadrants in parallel. Comparing diagrams reveals the same to be true for each of the quadrants in each of the four banks of memory. Each quadrant, then, corresponds to one pixel, and all of the pixels for one bank are written out to the shift register during a write cycle.

VIDEO DAC INTERFACE

The interface to the NE5150 is shown in Figure 24. The 8-bit data bus comes from the lower 8 bits of the Lilith. The low 4 bits are connected directly to the Video DAC data inputs. Bits 4 – 7 are tied to the 74F157 Multiplexer. This provides the address to the CLUT when it is initialized.

The other set of inputs to the multiplexer comes from the pixel-shifting stage. After the first CLUT initialization, all of the addresses come from the pixel-shifter. The inverters, NAND gates, and OR gates are used to delay the write pulses $\overline{WRR}$, $\overline{WRG}$, and $\overline{WRB}$ so that they fit into the address setup window. The chip select pulses come from the 74F138 which are selected by the Lilith. $\overline{I/OCLK}$ clocks the 74138 and the OR gates for the chip select.

DCLK drives the STROBE of the DAC and clocks the two D-type flip-flops which provide the BLANKing signal. Both of these signals come from the ACRTC and the system timing section. The WHITE, BRIGHT, and SYNC inputs are not utilized and are connected to ground. V_{EE} is run off a 7905 voltage regulator powered by a –12V power supply.

The capacitors to the monitor and voltage regulator are polarized with the positive end to the monitor for the RGB outputs and to ground for the regulator. The regulator uses Tantalum capacitors.

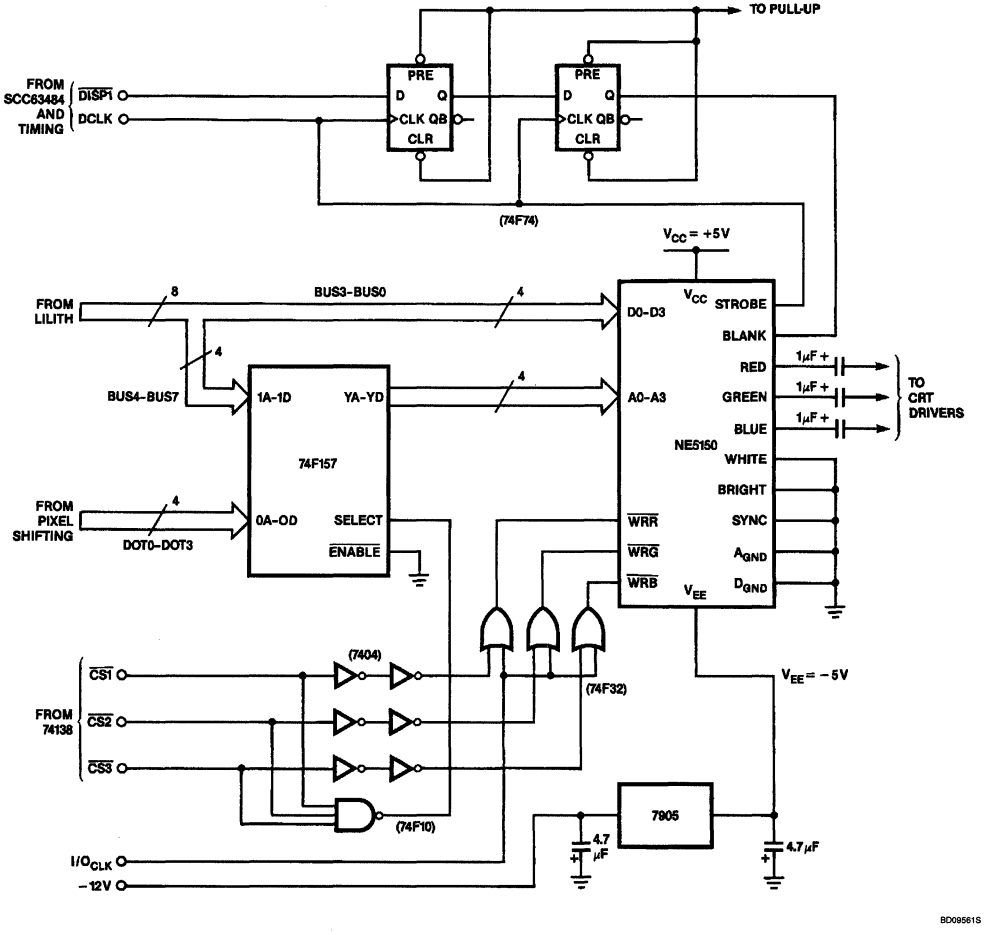


Figure 24. NE5150 Video DAC Interface

NE5150/51/52 Family of Video Digital-to-Analog Converters AN1081

GLOSSARY

This glossary consists of three parts: a section for graphics terminology, one for the timing of the NE5150 used in the Lilith workstation application, and a list of references. For the glossary section, many analogies are made with television to clarify some terminology.

GRAPHICS TERMINOLOGY

ACRTC — Short for Advanced CRT Controller. A device that helps to interface a microprocessor or microcomputer with a monitor. Advanced refers to the Signetics ACRTC, the SCC63484, called advanced because of its ability to do most of its graphics computations on-board, thus relieving some of the workload from the microprocessor and increasing its overall efficiency.

Bit-Map, Bit-Plane — A memory representation in which one or more bits correspond to a pixel. For each bit used in the representation of a pixel, there is a plane on which it can be mapped. To represent each pixel by 4 bits, 4 bit planes are needed. This is the case whether the bits store the actual data for the pixel or hold the address of the memory location containing the data.

Blanking — The process of turning off an electron gun so that it leaves no trace on the screen as it returns to the left or top of the screen in a raster-scan system. Applies to both television sets and monitors. The period for the blanking is defined as the horizontal blanking and the vertical blanking interval for their respective cases.

CRT — Short for Cathode Ray Tube, a type of electron tube that produces an electron beam that strikes the phosphor-coated screen, causing that screen to emit light.

Chrominance — The color information supplied in a signal. While this information has to be extracted by color decoders in television (via phase differencing with a fixed-frequency subcarrier), in computer monitors and bit-mapped systems it is supplied digitally and then converted to analog to directly drive color guns.

Color Look-up Table — Sometimes referred to as the CLUT, it is associated with a Video DAC and speeds system access of often-used colors. The time savings results because a color can be generated by sending a CLUT address to the DAC instead of loading a word from external memory. Current CLUTs range in size from 16 to 256 words. Word length depends on the bit resolution of the DAC.

DAC — Short for Digital-to-Analog Converter. Most DACs have a single output. Some have as many as eight. RGB Video DACs have three — one for each of the primary colors. Video DACs typically operate at very high speeds since they have to supply a new piece of information for each pixel on the screen at rates of 30 to 80 times per second.

ECL — Short for Emitter-Coupled-Logic. A fast, non-saturating form of bipolar logic that usually operates from 0 to −5.2V. It has a threshold of −1.3V.

Frame Buffer — Sometimes used interchangeably with video RAM. A frame buffer is a large, fast-access store of memory that contains the digital information necessary to display part or all of a display. It is used in conjunction with bit-mapped graphic systems. It actually "stores" the bit-plane.

Glitch Energy — The area displaced by an analog signal as it overshoots or undershoots its ideal value. This is a problem usually found in DACs. Units are usually given in pV-s. When glitch energy is high, settling times tend to be longer and may result in visual color aberrations on the screen.

Hue — The actual color(s) on a monitor. The hue depends on the frequency of the light striking the human eye. For television transmission, it is determined by the video signal's phase difference with a color subcarrier reference frequency. For computer graphics systems, it is determined by the combination of binary values applied to the DAC. The resolution of hue/colors is determined by the bit length of each word of information.

Lilith — The brand name of the workstation manufactured by Modulo, Inc. of Provo, UT.

Luminance — The brightness information in a video signal. A black and white (monochrome) monitor displays only variations in brightness. Only a luminance signal is being manipulated. The same holds true for television. Although chrominance information is also present in a television signal, B/W TV sets do not have the necessary decoders.

Modula-2 — A language that is the superset of Pascal. This was also invented by Niklaus Wirth of the Swiss Technological Institute.

NTSC — Short for the National Television Standards Committee, the ruling body for television standards in the United States. Other countries also use this standard as is, or with a different frequency for the color subcarrier.

Orthogonal — Defined as being mutually perpendicular. The product of two orthogonal vectors is zero. In bit-mapped systems, the bit length of a word lies orthogonal to the plane itself. Hence, each plane supplies only one bit of information for each pixel.

Pixel — Short for "picture element". The smallest resolvable element on a graphics display. Each pixel usually corresponds to at least one bit. The entire display is made up of a map of pixels. The term bit-map comes from the bit association. There is no equivalent in television. What is seen is the true analog representation of what is being recorded by a camera and then retraced on horizontal lines.

Raster-Scan — The form of visual display transmission used in all television sets and in most monitors. It consists of an electron beam tracing a path from left-to-right while going top-to-bottom.

Saturation — The "deepness" of a color. Usually depends on the amplitude of the color signal in television systems. Red and pink are the same hue, but red is actually more saturated than pink. In graphics systems, there is no true equivalent. Changing bit-values changes the color itself. The closest analogy would be to raise or lower the voltages on all three color guns simultaneously (the BRIGHT function on the NE5150/51/52). This would, however, depending on the amplitude change, give the impression of brightening or dimming the color (changing luminance) rather than saturating it.

Sync — The voltage level specified in RS-343A as being 140 IRE (1V) below the enhanced white level (ground). It is also 40 IRE (286mV) below the blanking level. Generically it is also used to refer to vertical and horizontal sync pulses that synchronize the timing and movement of the electron beam on a CRT. It should not be confused with "composite sync".

Teletext — A form of data transmission via television signals. In many cases, digital information is sent during the vertical blanking interval (VBI). In some cases, it is sent during every retrace. This is known as full-field teletext.

TTL — Short for Transistor-Transistor Logic. It has a threshold voltage of approximately 1.4V and is the most widely-used form of logic in the world today.

DEFINITIONS FOR NE5150/51/52 TIMING DIAGRAMS

This section contains explanations for the NE5150/51/52 Video DAC's timing diagram specifications. For the typical, minimum, and maximum values, please refer to Signetics' data sheet.

t_{WAS} — Write Address Setup (NE5150/52)

t_{WAH} — Write Address Hold (NE5150/52)

t_{WDS} — Write Data Setup (NE5150/52)

t_{WDH} — Write Data Hold (NE5150/52)

t_{WEW} — Write Enable Pulse Width (NE5150/52)

t_{RCS} — Read Composite Setup (NE5150/52)

t_{RCH} — Read Composite Hold (NE5150/52)

t_{RAS} — Read Address Setup (NE5150/52)

t_{RAH} — Read Address Hold (NE5150/52)

t_{RSW} — Read Strobe Pulse Width (NE5150/52)

t_{RDD} — Read DAC Delay (NE5150/52)

t_{CS} — Composite Setup (NE5151)

t_{CH} — Composite Hold (NE5151)

t_{DS} — Data bits Setup (NE5151)

t_{DH} — Data bits Hold (NE5151)

t_{SW} — Strobe Pulse Width (NE5151)

t_{DD} — DAC Delay (NE5151)

t_R — DAC Rise Time (NE5151)

t_S — DAC Full-Scale Settling Time (NE5151)

REFERENCES

The following books, articles, notes, and correspondences were used in the preparation of this application note.

1. *Raster Graphics Handbook*, 2nd edition, by the Conrac Corporation
2. "Trends in Graphics Hardware", paper by Randall R. Bird, Genisco Computers Corporation; presented at WESCON '85
3. *Basic Television and Video Systems*, 5th edition, by Bernard Grob, McGraw-Hill
4. *Getting the Best Performance from Video Digital-to-Analog Converters*, (AN-1) by Dennis Packard, Brooktree Corporation, San Diego
5. "A Cost-Effective Custom CAD System", paper by R.C. Burton, D.G. Brewer, R.E. Penman, and R. Schilimoeller, Computer Science Department, Brigham Young University and Signetics Corporation
6. "Lilith and Modula-2", by Richard Ohran, *Byte Magazine*, pgs. 181 – 192; August 1984
7. "Monolithic Color Palette Fills in the Picture for High-Speed Graphics", by Steven Sidman and John C. Kuklewicz, *Electronic Design*; November 29, 1984
8. *EIA Standard RS-343A: Electrical Performance Standards for High-Resolution Monochrome Closed-Circuit Television Camera*, by the Video Engineering Department of the Electronic Industries Association; September, 1969
9. "A Single-Chip RGB Digital-to-Analog Converter with High-Speed Color-Map Memory", by W. Mack and M. Horowitz, *Digest of the International Conference on Consumer Electronics*, p. 90; 1985

Signetics

PNA7518
8-Bit Multiplying DAC

Product Specification

Linear Products

DESCRIPTION

The PNA7518 is an NMOS 8-bit multiplying digital-to-analog converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analog output at a sampling rate of 30MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analog signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive edge-triggered. The output impedance is approximately 0.5kΩ, depending upon the applied digital code. An additional operational amplifier is required for the full bandwidth. Two's complement is selected when STC (Pin 11) is HIGH or is not connected.

FEATURES

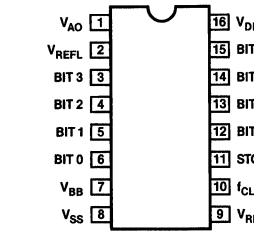
- **TTL input levels**
- **Positive edge-triggered**
- **Analog voltage output at 30MHz sampling rate**
- **Binary or two's complement input**
- **Output voltage accuracy to within ± ½ of the input LSB**

APPLICATIONS

- **Video data conversion**
- **CRT displays**
- **Waveform/test signal generation**
- **Color/black-and-white graphics**

PIN CONFIGURATION

N Package



TOP VIEW

CD10200S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{AO}	Analog output voltage
2	V_{refL}	Reference voltage LOW
3	bit 3	Digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	Least-significant bit (LSB)
7	V_{BB}	Back bias
8	V_{SS}	Ground
9	V_{refH}	Reference voltage HIGH
10	f_{CLK}	Clock input
11	STC	Select two's complement
12	bit 7	Most-significant bit (MSB)
13	bit 6	Digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	Positive supply voltage

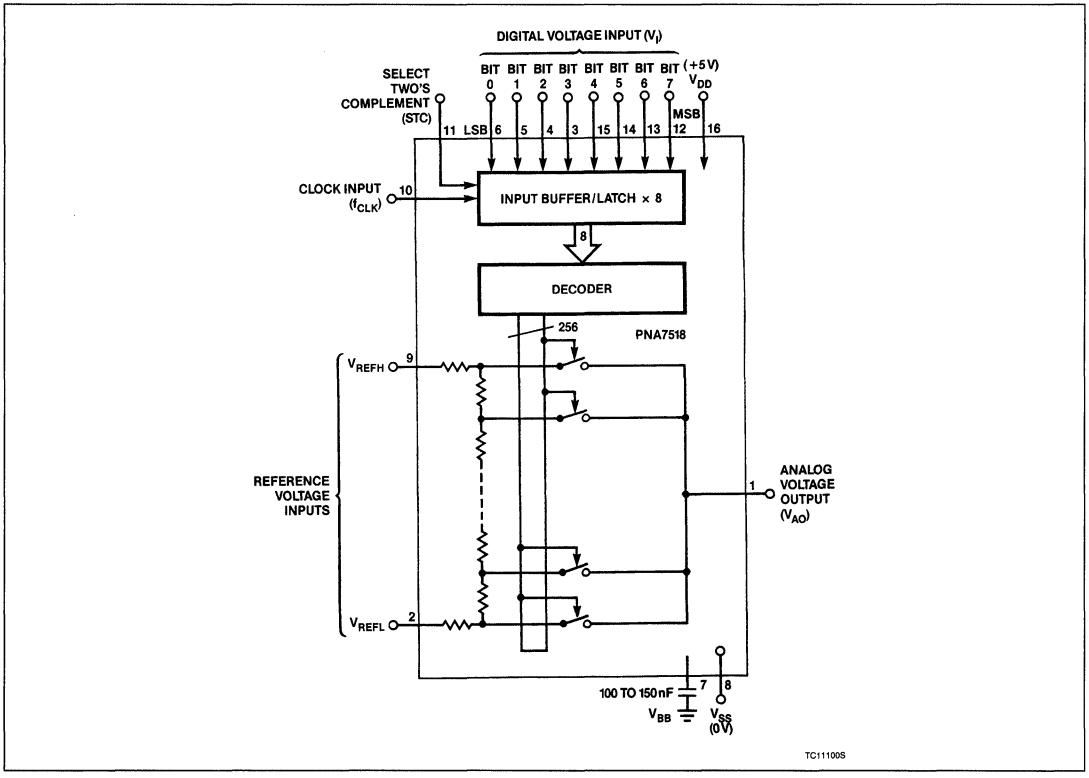
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38WE-1)	0 to +70°C	PNA7518N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 16)	−0.5 to +7	V
V_I	Input voltage range (Pins 3, 4, 5, 6, 11, 12, 13, 14 and 15)	−0.5 to +7	V
V_{AO}	Output voltage range (Pin 1)	−0.5 to +7	V
P_{TOT}	Total power dissipation	400	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

BLOCK DIAGRAM



HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

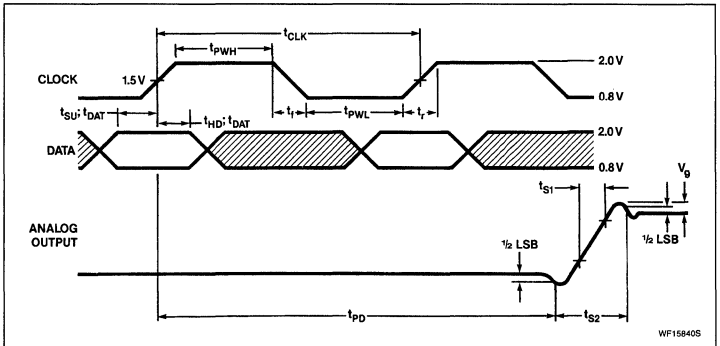


Figure 1. Switching Characteristics

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DC ELECTRICAL CHARACTERISTICS V_{DD} = 4.5 to 5.5; V_{SS} = 0V; C_{BB} = 100nF; T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 16)					
V_{DD}	Supply voltage	4.5	5	5.5	V
I_{DD}	Supply current		50	80	mA
Reference voltages					
V_{REFL}	Reference voltage LOW (Pin 2)	−0.1		+2.1	V
V_{REFH}	Reference voltage HIGH (Pin 9)	−0.1		+2.1	V
R_{REF}	Reference ladder	150	230	300	Ω
Inputs					
	Digital input levels (TTL)[1]				
V_{IL}	input voltage LOW	0		0.8	V
V_{IH}	input voltage HIGH	2.0		5.25	V
I_{LI}	input leakage current			10	μA
	Clock input (Pin 10)				
V_{IL}	input voltage LOW	0		0.8	V
V_{IH}	input voltage HIGH	2.0		5.25	V
I_{LI}	input leakage current			10	μA
Output					
	Analog voltage output (Pin 1)				
V_{AO}	at R_L = 200 kΩ)	0		2	V
BW	Bandwidth (−3 dB) at C_L = 6 pF		12		MHz
Output transients (glitches)[2]					
V_G	Glitch occurring at step 7F-80 (HEX):		3		LSB
	maximum amplitude for 1 LSB change area		23		LSB ns
V_G	Glitch occurring at step 00-AA (HEX):		5		LSB
	maximum amplitude for 1 LSB change area		41		LSB ns
P_{TOT}	Total power dissipation		300		mW

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 to 5.5; V_{SS} = 0V; C_{BB} = 100nF; T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Clock input (Pin 10)				
f_{CLK}	frequency	1		30	MHz
t_{PWH}	pulse width HIGH	10			ns
t_{PWL}	pulse width LOW	10			ns
t_R	input rise time at f_{CLK} = 30MHz			3	ns
t_F	input fall time at f_{CLK} = 30MHz			3	ns
Switching characteristics (Figure 1)					
t_{SU}, t_{DAT}	Data setup time	3			ns
t_{HD}, t_{DAT}	Data hold time	4			ns
t_{PD}	Propagation delay time, input to output	t_{CLK} + 15	t_{CLK} + 22	t_{CLK} + 30	ns
t_{S1}	Settling time; 10 to 90% full-scale change; C_L = 6pF; R_L = 200kΩ		13	20	ns
t_{S2}	Settling time to ±1 LSB; C_L = 6pF; R_L = 200kΩ		40		ns
	Linearity at R_L = 200kΩ; $V_O = 2V_{P-P}$			± ½	LSB
Influence of clock frequency[2]					
	Cross-talk at 2 × f_{CLK}				
	amplitude		2		LSB
	area		8		LSB ns

NOTES:

1. Inputs Bit 0 to Bit 7 are positive edge-triggered and STC.
2. Measured at $V_{REFH} - V_{REFL}$ = 2.0 V; 1 × LSB = 7.8mV. The energy equivalent of output transients is given as the area contained by the graph of output amplitude (LSB) against time (ns). The glitch area is independent of the value of V_{REF}. Glitch amplitudes and clock cross-talk can be reduced by using a shielded printed circuit board (see Pin Configuration).

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TDA5702
8-Bit Digital-to-Analog Converter

Preliminary Specification

Linear Products

DESCRIPTION

The TDA5702 is an 8-bit digital to analog converter (DAC) designed for video and professional applications. The TDA5702 converts the 8-bit binary-coded digital words into an analog output signal at a sampling rate of 25MHz. The design of the TDA5702 has eliminated the need for an operational amplifier, buffer and deglitching circuit at the analog output.

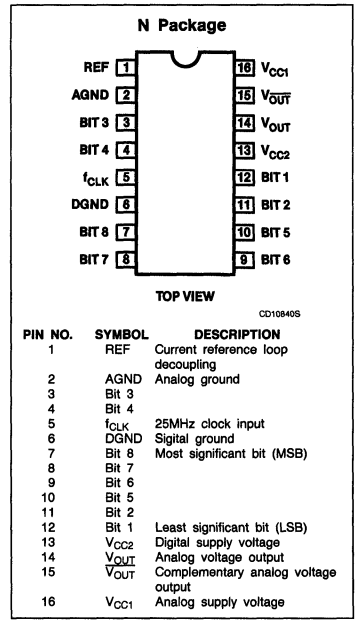
FEATURES

- **8-bit accuracy**
- **Internal input register**
- **TTL compatible digital signals**
- **Two voltage supply connections:**
  - **analog +5V**
  - **digital +5V**
- **Two complementary outputs (V_{OUT}, $\overline{V_{OUT}}$)**
- **No deglitching circuit required**
- **Low power consumption; typically 300mW**
- **16-lead plastic DIP**

APPLICATIONS

- **Video data conversion**
- **Color/black-and-white graphics**
- **CRT displays**
- **Waveform/test signal generation**

PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	REF	Current reference loop decoupling
2	AGND	Analog ground
3	Bit 3	
4	Bit 4	
5	f_{CLK}	25MHz clock input
6	DGND	Sigital ground
7	Bit 8	Most significant bit (MSB)
8	Bit 7	
9	Bit 6	
10	Bit 5	
11	Bit 2	
12	Bit 1	Least significant bit (LSB)
13	V_{CC2}	Digital supply voltage
14	V_{OUT}	Analog voltage output
15	$\overline{V_{OUT}}$	Complementary analog voltage output
16	V_{CC1}	Analog supply voltage

ORDERING INFORMATION

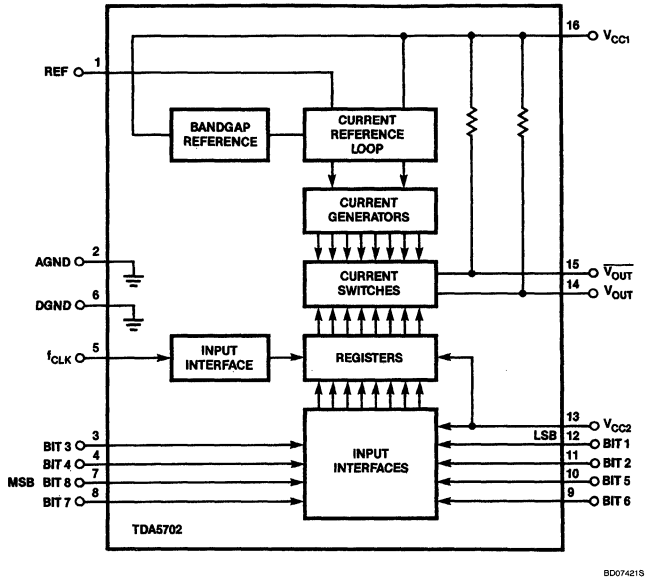
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	0 to +70°C	TDA5702N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V_{CC2}	at Pin 13	8	V
V_{CC1}	at Pin 16	8	V
	Input voltage		
V_{IN}	at Pins 3, 4, 5, 7, 8, 9, 10, 11 and 12	8	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Junction temperature	+125	°C
T_A	Operating ambient temperature range	0 to +70	°C

8-Bit Digital-to-Analog Converter TDA5702

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V, $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{CC2}	Digital supply voltage	Pin 13	4.75	5.0	5.25	V
V_{CC1}	Analog supply voltage	Pin 16	4.75	5.0	5.25	V
I_{CC2}	Digital supply current	Pin 13	25	34	43	mA
I_{CC1}	Analog supply current	Pin 16	20	27	34	mA
Res	Resolution			8		bits
Digital input levels						
V_{IH}	Input voltage HIGH		2.2			V
V_{IL}	Input voltage LOW				0.8	V
I_{IH}	Input current HIGH				10	μA
I_{IL}	Input current LOW		−1.5			mA
I_{IL}	Clock input current LOW		−1.0			mA
Outputs[2]						
V_{FS}	Full-scale voltage	with respect to V_{CC}	1.43	1.6	1.75	V
V_{ZS}	Zero offset voltage	with respect to V_{CC}		10	25	mV
	Absolute linearity	V_{14}, V_{15}	−0.5		+0.5	LSB
	Differential linearity	V_{14}, V_{15}	−0.5		+0.5	LSB
R_{16-14}	Output resistance			75		Ω
C_1	External capacitance			100		nF

NOTES:
1. See Figure 3.
2. See Figure 2.
3. See Figure 1.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 4.75$ to 5.25V, $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Timing						
f_C	Maximum conversion rate		25			MHz
t_{DS}	Data turn-on delay[1]			10		ns
t_{SET1}	Transient settling time	½ LSB		30		ns
t_{SET2}	Transient settling time	1 LSB		20		ns
t_O	Transient output (glitch) energy				+50	LSB ns
t_{PW}	Pulse width[3]		10			ns
t_{SU}	Data setup time		4			ns
t_H	Data hold time		6			ns

NOTE:
1. See Figure 1.

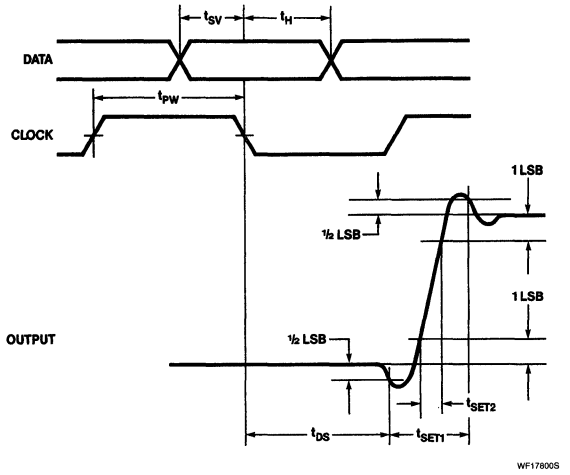

Figure 1. Timing Diagram

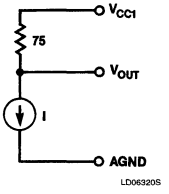

Figure 2. Equivalent Analog Output Circuit

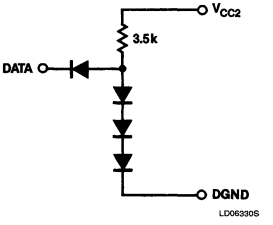

Figure 3. Equivalent Digital Input Circuit

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Signetics

TDA8440
Video and Audio Switch IC

Product Specification

Linear Products

DESCRIPTION

The TDA8440 is a versatile video/audio switch, intended to be used in applications equipped with video/audio inputs.

It provides two 3-State switches for audio channels and one 3-State switch for the video channel and a video amplifier with selectable gain (times 1 or times 2).

The integrated circuit can be controlled via a bidirectional I^2C bus or it can be controlled directly by DC switching signals. Sufficient sub-addressing is provided for the I^2C bus mode.

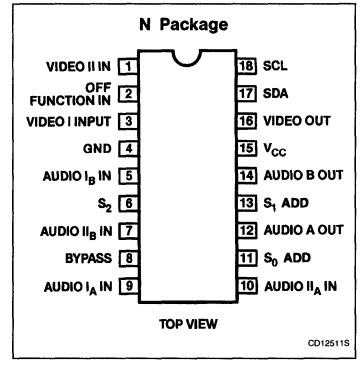
FEATURES

- **Combined analog and digital circuitry gives maximum flexibility in channel switching**
- **3-State switches for all channels**
- **Selectable gain for the video channels**
- **Sub-addressing facility**
- **I^2C bus or non-I^2C bus mode (controlled by DC voltages)**
- **Slave receiver in the I^2C bus mode**
- **External OFF command**
- **System expansion possible up to 7 devices (14 sources)**
- **Static short-circuit proof outputs**

APPLICATIONS

- **TVRO**
- **Video and audio switching**
- **Television**
- **CATV**

PIN CONFIGURATION



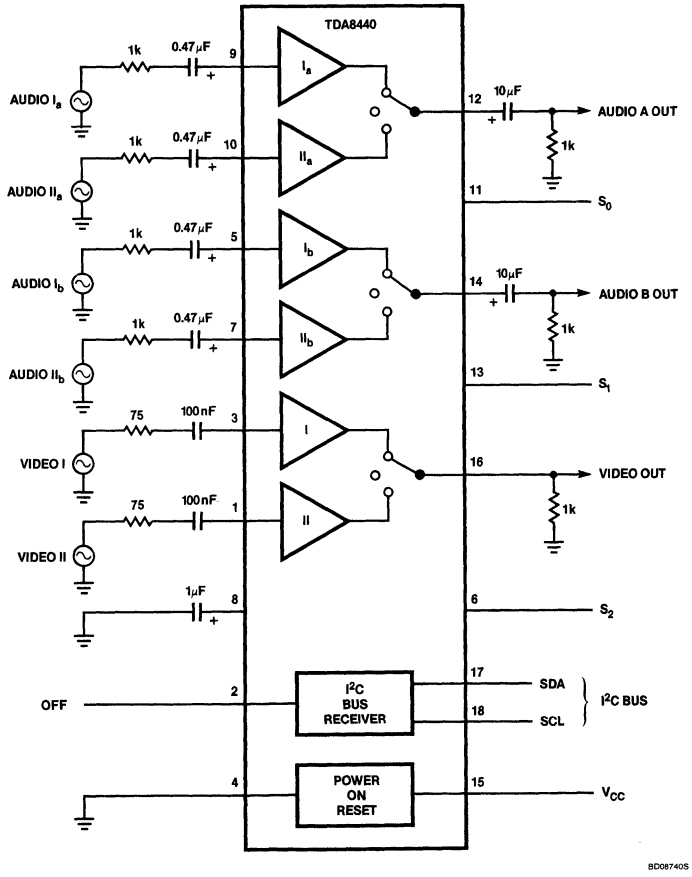
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP (SOT-102)	0 to 70°C	TDA8440N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage Pin 15	14	V
	Input voltage		
V_{SDA}	Pin 17	−0.3 to V_{CC} +0.3	V
V_{SCL}	Pin 18	−0.3 to V_{CC} +0.3	V
V_{OFF}	Pin 2	−0.3 to V_{CC} +0.3	V
V_{S0}	Pin 11	−0.3 to V_{CC} +0.3	V
V_{S1}	Pin 13	−0.3 to V_{CC} +0.3	V
V_{S2}	Pin 6	−0.3 to V_{CC} +0.3	V
$-I_{16}$	Video output current Pin 16	50	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
θ_{JA}	Thermal resistance from junction to ambient in free-air	50	°C/W

BLOCK DIAGRAM AND TEST CIRCUIT



NOTE:
S0, S1, S2, and OFF (Pins 11, 13, 6, and 2) connected to V_{CC} or GND. If more than 1 device is used, the outputs and Pin 8 (bias decoupling of the audio inputs) may be connected in parallel.

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DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{15-4}	Supply voltage	10		13.2	V
I_{15}	Supply current (without load)		37	50	mA
Video switch					
C_1C_3	Input coupling capacitor	100			nF
A_{3-16} A_{3-16}	Voltage gain (times 1; SCL = L) (times 2; SCL = H)	−1 +5	0 +6	+1 +7	dB dB
A_{1-16} A_{1-16}	Voltage gain (times 1; SCL = L) (times 2; SCL = H)	−1 +5	0 +6	+1 +7	dB dB
V_{3-4}	Input video signal amplitude (gain times 1)			4.5	V
V_{1-4}	Input video signal amplitude (gain times 1)			4.5	V
Z_{16-4}	Output impedance		7		Ω
Z_{16-4}	Output impedance in 'OFF' state	100			kΩ
	Isolation (off-state) (f_O = 5MHz)	60			dB
S/S + N	Signal-to-noise ratio[2]	60			dB
V_{16-4}	Output top-sync level	2.4	2.8	3.2	V
G	Differential gain			3	%
V_{16-4}	Minimum crosstalk attenuation[1]	60			dB
RR	Supply voltage rejection[3]	36			dB
BW	Bandwidth (1dB)	10			MHz
∝	Crosstalk attenuation for interference caused by bus signals (source impedance 75Ω)	60			db
Audio switch "A" and "B"					
V_{9-4} (RMS) V_{10-4} (RMS) V_{5-4} (RMS) V_{7-4} (RMS)	Input signal level			2 2 2 2	V V V V
Z_{9-4} Z_{10-4} Z_{5-4} Z_{7-4}	Input impedance	50 50 50 50	100 100 100 100		kΩ kΩ kΩ kΩ
Z_{12-4} Z_{14-4}	Output impedance			10 10	Ω Ω
Z_{14-4}	Output impedance (off-state)	100			kΩ
V_{9-12} V_{10-12} V_{5-14} V_{7-14}	Voltage gain	−1 −1 −1 −1	0 0 0 0	+1 +1 +1 +1	dB dB dB dB
	Isolation (off-state) (f = 20kHz)	90			dB
S/S + N	Signal-to-noise ratio[4]	90			dB
THD	Total harmonic distortion[6]			0.1	%

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $V_{CC} = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Crosstalk attenuation for interferences caused by video signals[5]				
α	Weighted	80			dB
α	Unweighted	80			dB
α	Crosstalk attenuation for interferences caused by sinusoidal sound signals[5]	80			dB
	Crosstalk attenuation for interferences caused by the bus signal (weighted) (source impedance = 1kΩ)	80			dB
RR	Supply voltage rejection	50			dB
BW	Bandwidth (−1dB)	50			kHz
I^2C bus inputs/outputs SDA (Pin 17) and SCL (Pin 18)					
V_{IH}	Input voltage HIGH	3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+1.5	V
I_{IH}	Input current HIGH[7]			10	μA
I_{IL}	Input current LOW[7]			10	μA
V_{OL}	Output voltage LOW at I_{OL} = 3mA			0.4	V
I_{OL}	Maximum output sink current		5		mA
C_I	Capacitance of SDA and SCL inputs, Pins 17 and 18			10	pF
Sub-address inputs S_0 (Pin 11), S_1 (Pin 13), S_2 (Pin 6)					
V_{IH}	Input voltage HIGH	3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+0.4	V
I_{IH}	Input current HIGH			10	μA
I_{IL}	Input current LOW	−50		0	μA
OFF input (Pin 2)					
V_{IH}	Input voltage HIGH	+3		V_{CC}	V
V_{IL}	Input voltage LOW	−0.3		+0.4	V
I_{IH}	Input current HIGH			20	μA
I_{IL}	Input current LOW	−10		2	μA

NOTES:

1. Caused by drive on any other input at maximum level, measured in B = 5MHz, source impedance for the used input 75Ω,
   crosstalk = $20\log \frac{V_{OUT}}{V_{IN}\ max}$.
2. S/N = $20\log \frac{V_O\ \text{video noise}\ (P-P)\ (2V)}{V_O\ \text{noise}\ _{RMS}\ B = 5MHz}$.
3. Supply voltage ripple rejection = $20\log \frac{V_R\ \text{supply}}{V_R\ \text{on output}}$ at f = max. 100kHz.
4. S/N = $20\log \frac{V_O\ \text{nominal (0.5V)}}{V_O\ \text{noise}\ B = 20kHz}$.
5. Caused by drive of any other input at maximum level, measured in B = 20kHz, source impedance of the used input = 1kΩ,
   crosstalk = $20\log \frac{V_{OUT}}{V_{IN}\ max}$ according to DIN 45405 (CCIR 468).
6. f = 20Hz to 20kHz.
7. Also if the supply is switched off.

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AC ELECTRICAL CHARACTERISTICS I^2C bus load conditions are as follows: 4kΩ pull-up resistor to +5V; 200pF to GND. All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			μs
$t_{S\ (STA)}$	Start condition setup time	4			μs
$t_{H\ (STA)}$	Start condition hold time	4			μs
t_{LOW}	SCL, SDA LOW period	4			μs
t_{HIGH}	SCL, HIGH period	4			μs
t_R	SCL, SDA rise time			1	μs
t_F	SCL, SDA fall time			0.3	μs
$t_{S\ (DAT)}$	Data setup time (write)	1			μs
$t_{H\ (DAT)}$	Data hold time (write)	1			μs
$t_{S\ (CAC)}$	Acknowledge (from TDA8440) setup time			2	μs
$t_{H\ (CAC)}$	Acknowledge (from TDA8440) hold time	0			μs
$t_{S\ (STO)}$	Stop condition setup time	4			μs

Table 1. Sub-Addressing

S_2	S_1	S_0	SUB-ADDRESS		
			A_2	A_1	A_0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I^2C addressable		

FUNCTIONAL DESCRIPTION

The TDA8440 is a monolithic system of switches and can be used in CTV receivers equipped with an auxiliary video/audio plug. The IC incorporates 3-State switches which comprise:

a) An electronic video switch with selectable gain (times 1 or times 2) for switching between an internal video signal (from the IF amplifier) with an auxiliary input signal.

b) Two electronic audio switches, for two sound channels (stereo or dual language), for switching between internal audio sources and signals from the auxiliary video/audio plug.

A selection can be made between two input signals and an OFF-state. The OFF-state is necessary if more than one TDA8440 device is used.

The SDA and SCL pins can be connected to the I^2C bus or to DC switching voltages. Inputs S_0 (Pin 11), S_1 (Pin 13), and S_2 (Pin 6) are used for selection of sub-addresses or switching to the non-I^2C mode. Inputs S_0, S_1, and S_2 can be connected to the supply voltage (H) or to ground (L). In this way, no peripheral components are required for selection.

NON-I^2C BUS CONTROL

If the TDA8440 switching device has to be operated via the auxiliary video/audio plug, inputs S_2, S_1, and S_0 must be connected to the supply line (12V).

The sources (internal and external) and the gain of the video amplifier can be selected via the SDA and SCL pins with the switching voltage from the auxiliary video/audio plug:

- Sources I are selected if SDA = 12V (external source)
- Sources II are selected if SDA = 0V (TV mode)
- Video amplifier gain is 2 × if SCL = 12V (external source)
- Video amplifier gain is 1 × if SCL = 0V (TV mode)

If more than one TDA8440 device is used in the non-I^2C bus system, the OFF pin can be used to switch off the desired devices. This can be done via the 12V switching voltage on the plug.

- All switches are in the OFF position if OFF = H (12V)
- All switches are in the selected position via SDA and SCL pins if OFF = L (0V)

I^2C BUS CONTROL

Detailed information on the I^2C bus is available on request.

Table 2. TDA8440 I²C Bus Protocol

STA	A_6	A_5	A_4	A_3	A_2	A_1	A_0	R/W	AC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	AC	STO

STA = start condition
A_6 = 1
A_5 = 0
A_4 = 0
A_3 = 1
Fixed address bits
A_2 = sub-address bit, fixed via S_2 input
A_1 = sub-address bit, fixed via S_1 input
A_0 = sub-address bit, fixed via S_0 input
R/W = read/write bit (has to be 0, only write mode allowed)
AC = acknowledge bit (= 0) generated by the TDA8440
D_7 = 1 audio I_a is selected to audio output a
D_7 = 0 audio I_a is not selected
D_6 = 1 audio II_a is selected to audio output a
D_6 = 0 audio II_a is not selected
D_5 = 1 audio I_b is selected to audio output b
D_5 = 0 audio I_b output is not selected
D_4 = 1 audio II_b is selected to audio output b
D_4 = 0 audio II_b is not selected
D_3 = 1 video I is selected to video output
D_3 = 0 video I is not selected
D_2 = 1 video II is selected to video output
D_2 = 0 video II is not selected
D_1 = 1 video amplifier gain is times 2
D_1 = 0 video amplifier gain is times 1
D_0 = 1 OFF-input inactive
D_0 = 0 OFF-input active
STO = stop condition

D_0/OFF Gating

D_0	OFF input	Outputs
0 (off input active)	H	OFF
0	L	In accordance with last defined $D_7 - D_1$ (may be entered while OFF = HIGH)
1 (off input inactive)	H	In accordance with $D_7 - D_1$
1	L	In accordance with $D_7 - D_1$

OFF FUNCTION

With the OFF input all outputs can be switched off (high ohmic mode), depending on the value of D_0.

Power-on Reset

The circuit is provided with a power-on reset function.

When the power supply is switched on, an internal pulse will be generated that will reset the internal memory S_0. In the initial state all the switches will be in the off position and the OFF input is active ($D_7 - D_0 = 0$), (I^2C mode). In the non-I^2C mode, positions are defined via SDA and SCL input voltages.

When the power supply decreases below 5V, a pulse will be generated and the internal memory will be reset. The behavior of the switches will be the same as described above.

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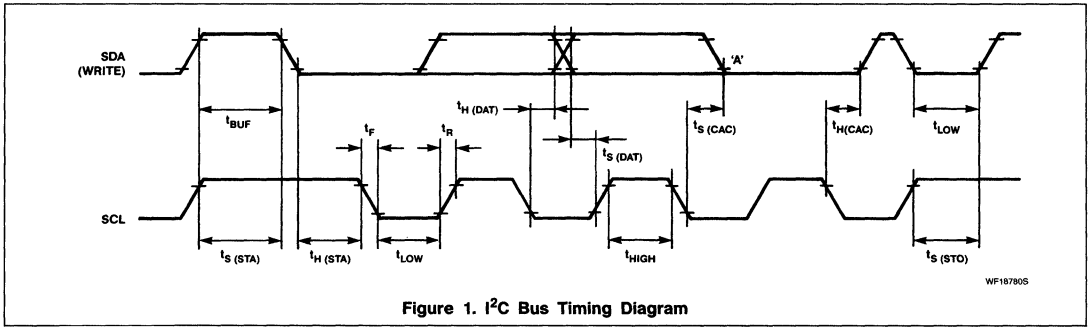


Figure 1. I²C Bus Timing Diagram

Signetics

NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

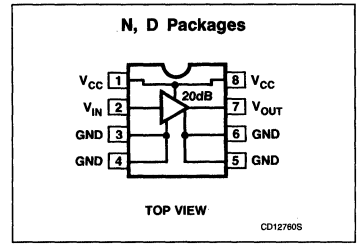
No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **200MHz (min.), ± 0.5dB bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION



APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

ORDERING INFORMATION

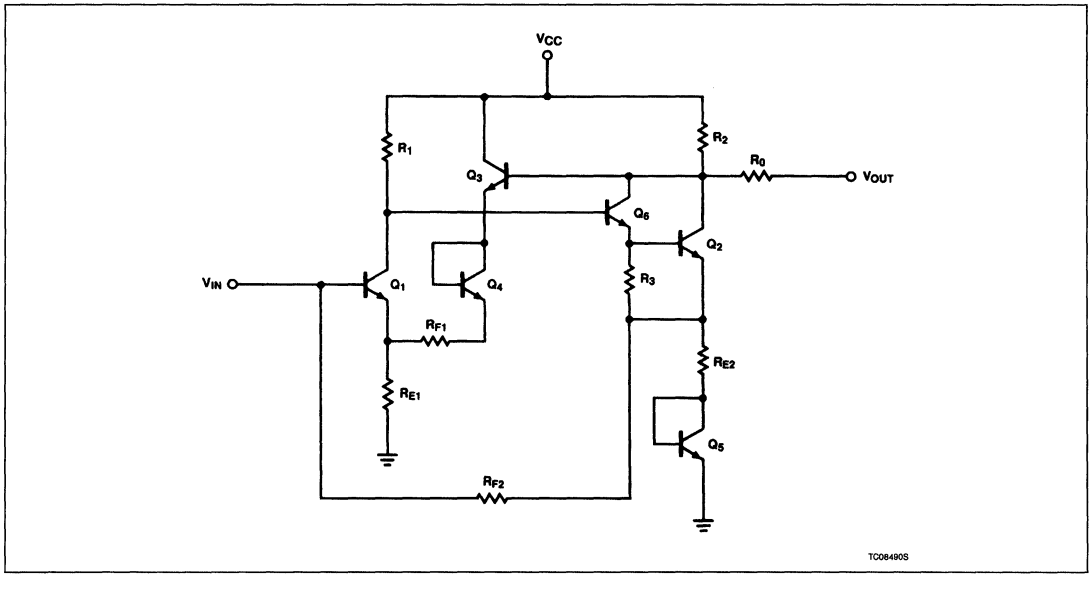
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade	 0 to +70 −40 to +85	 °C °C
P_D	Maximum power dissipation[1, 2] T_A = 25°C (still-air) N package D package	 1160 780	 mW mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



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DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz, over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f = 100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm

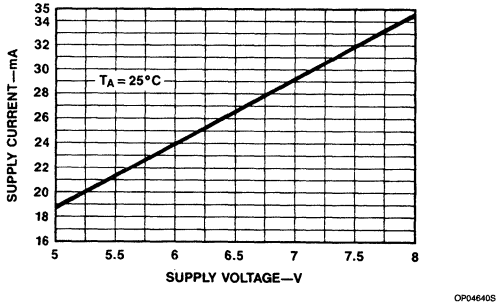

Figure 1. Supply Current vs Supply Voltage

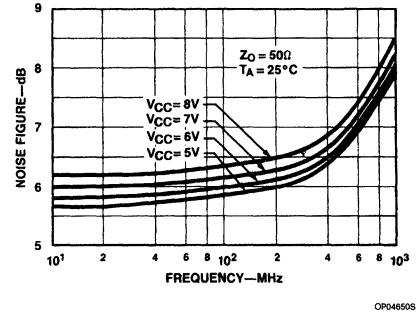

Figure 2. Noise Figure vs Frequency

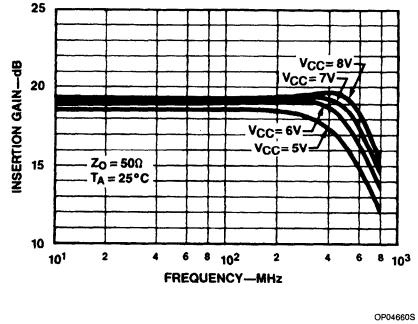

Figure 3. Insertion Gain vs Frequency (S_{21})

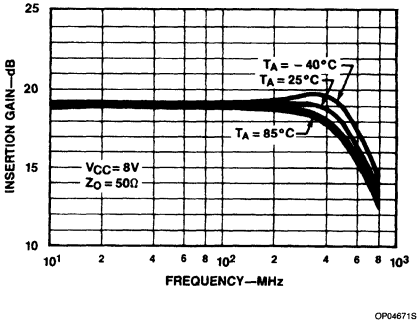

Figure 4. Insertion Gain vs Frequency (S_{21})

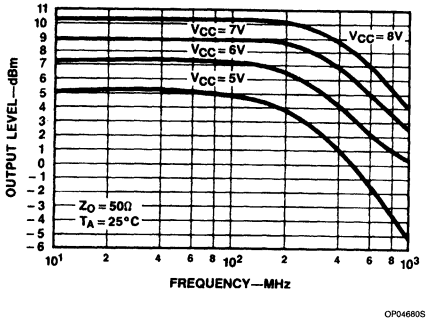

Figure 5. Saturated Output Power vs Frequency

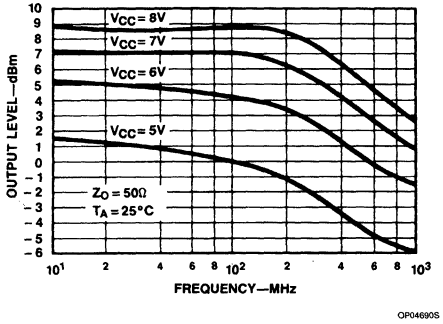

Figure 6. 1dB Gain Compression vs Frequency

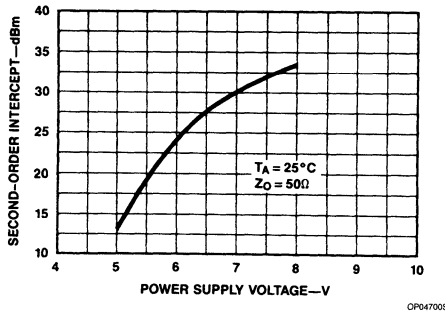

Figure 7. Second-Order Output Intercept vs Supply Voltage

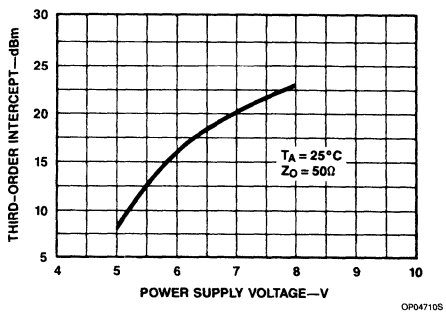

Figure 8. Third-Order Intercept vs Supply Voltage

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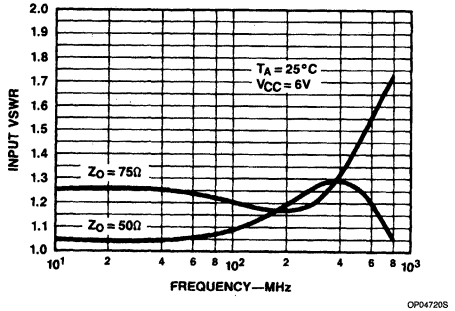


Figure 9. Input VSWR vs Frequency

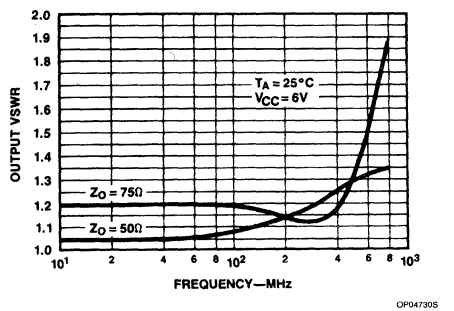


Figure 10. Output VSWR vs Frequency

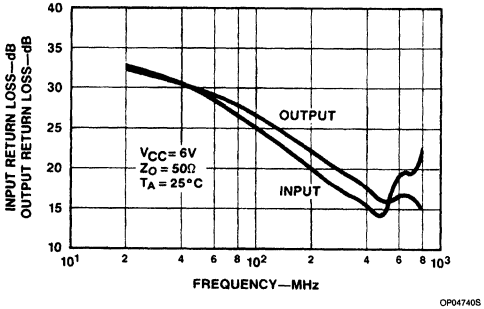


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

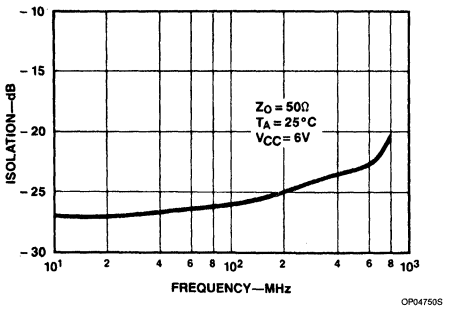


Figure 12. Isolation vs Frequency (S_{12})

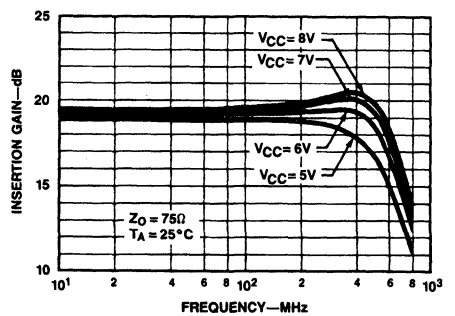


Figure 13. Insertion Gain vs Frequency (S_{21})

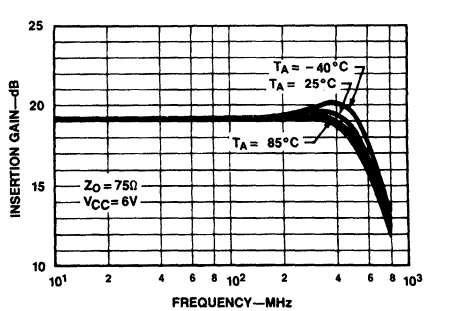


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10Log\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} dB \quad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\,R_{E1} \quad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

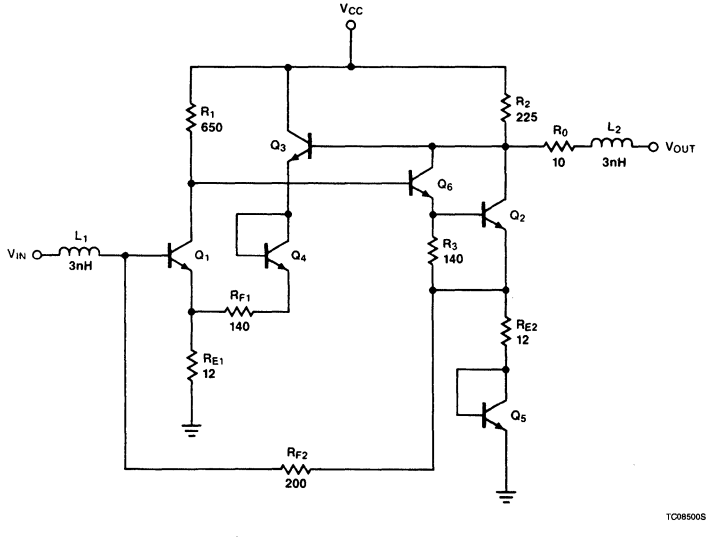


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

Both of the evaluation boards that will be discussed next do not have input and output capacitors because it is assumed the user will use AC-coupled test systems. Chip or foil capacitors can easily be inserted between the part and connector if the board trace is removed.

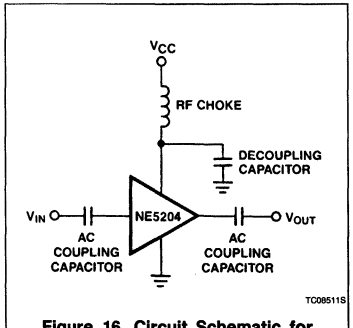


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

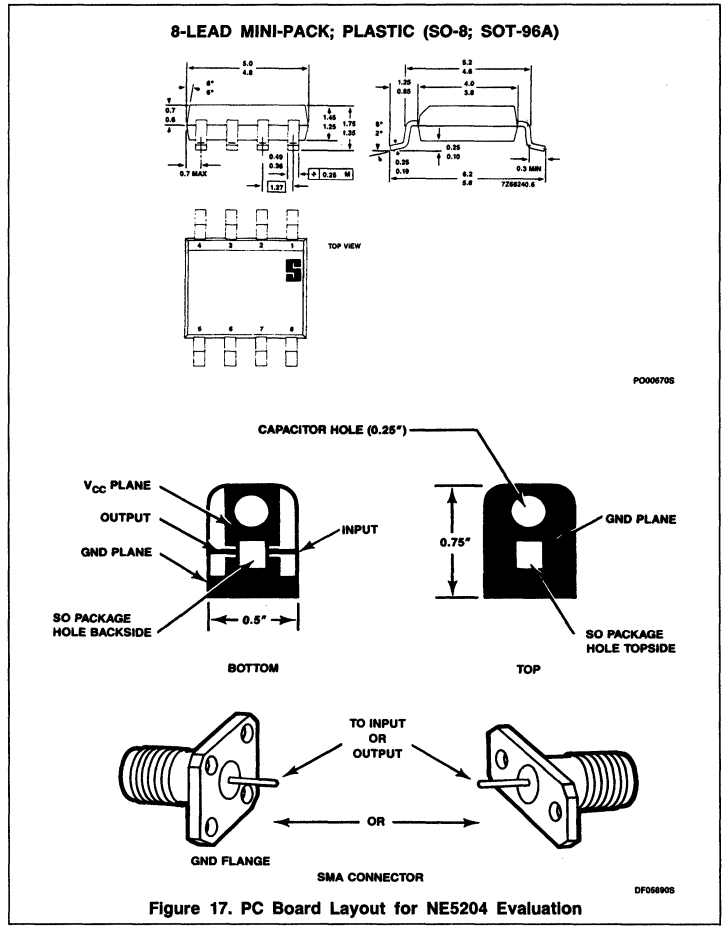


Figure 17. PC Board Layout for NE5204 Evaluation

50Ω EVALUATION BOARD

The evaluation board layout shown in Figure 17 produces excellent results. The board is to scale and is for the SO package. Both top and bottom are copper clad and the ground planes are bonded together through 50Ω SMA cable connectors. These are solder mounted on the sides of the board so that the signal traces line up straight to the connector signal pins.

Solid copper tubing is soldered through the flange holes between the two connectors for increased strength and grounding characteristics. Two- or four-hole flanges can be used. A flat, round decoupling capacitor is placed in the board's round hole and soldered between the bottom V_{CC} plane and the top side ground. The capacitor is as thin or thinner than the PC board thickness and has insulation around its side to isolate V_{CC} and ground. The square hole is for the SO package which is put in upside-down through the bottom of the board so that the leads are kept in position for soldering. Both holes are just slightly larger than the capacitor and IC to provide for a tight fit.

This board should be tested in a system with 50Ω input and output impedance for correct operation.

75Ω EVALUATION BOARD

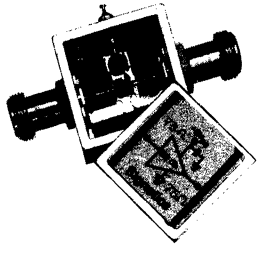
Another evaluation board is shown in Figure 18. This system uses the same PC board as presented in Figure 17, but makes use of 75Ω female N-type connectors. The board is mounted in a nickel plated box* that is used to support the N-type connectors. This is an excellent way to test the part for cable TV applications. Again, the board should be tested in a system with 75Ω input- and output-impedance for correct operation.

NOTE:

*The box and connectors are available as a "MOD-PACK SYSTEM" from the ANZAC division of ADAMS-RUSSELL CO., INC., 80 Cambridge Street, Burlington, MA 01803.

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.



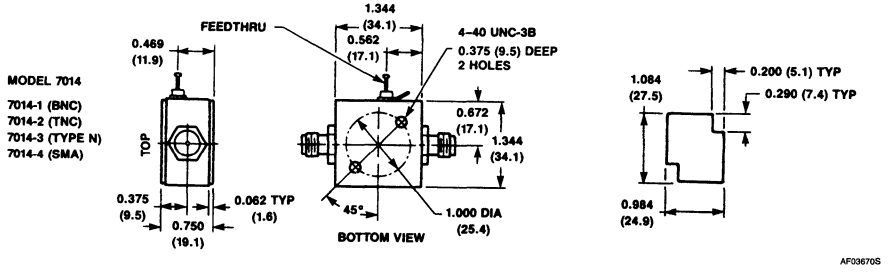
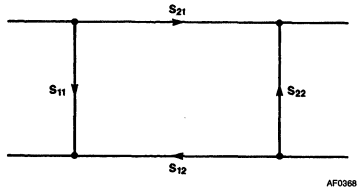


Figure 18. 75Ω N-Type Connector System



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

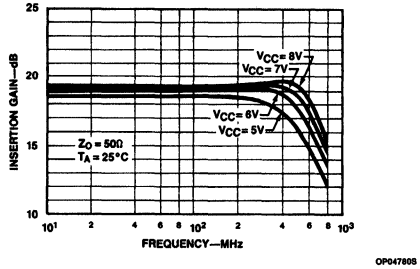
$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

b.

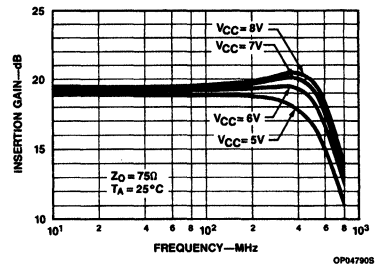
Figure 19

50Ω System

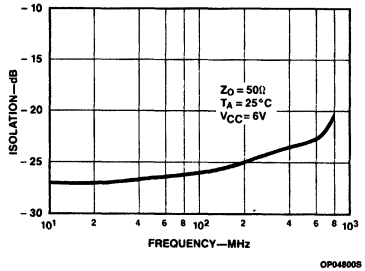


a. Insertion Gain vs Frequency (S_{21})

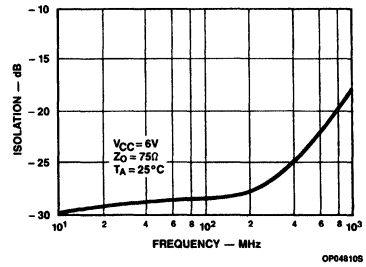
75Ω System



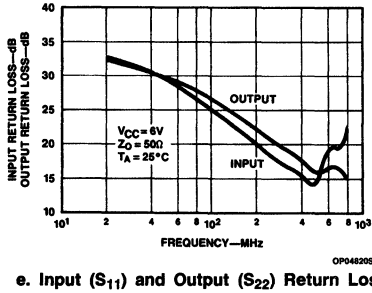
b. Insertion Gain vs Frequency (S_{21})



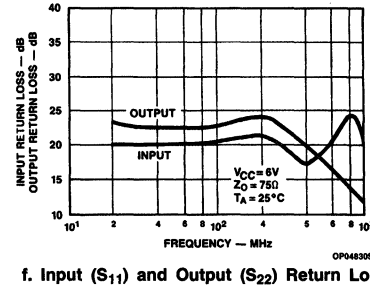
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20

Actual S-parameter measurements, using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B), are shown in Figure 20. These were obtained with the device mounted in a PC board as described in Figures 17 and 18.

For 50Ω system measurements, SMA connectors were used. The 75Ω data was obtained using N-connectors.

Values for Figure 20 are measured and specified in the data sheet to ease adaptation and comparison of the NE5204 to other high-frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5204

$P_{IN} = \frac{V_{IN}^2}{Z_D}$ — NE5204 (Z_D) — $P_{OUT} = \frac{V_{OUT}^2}{Z_D}$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I = V_I^2$

P_I = Insertion Power Gain
V_I = Insertion Voltage Gain

Measured value for the NE5204 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

and $V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$

In decibels:

$P_{I(dB)} = 10\text{Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20\text{Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing-wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB

$S_{11}\text{dB} = 20\text{Log } |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB

$S_{22}\text{dB} = 20\text{Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to non-linearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

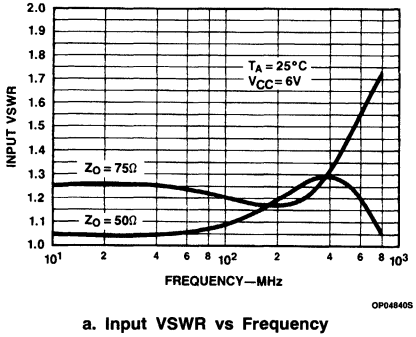
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second-order IMR is equal to the difference between the second-order intercept and the fundamental output level. The third-order IMR is equal to twice the difference between the third-order intercept and the fundamental output level. These are expressed as:

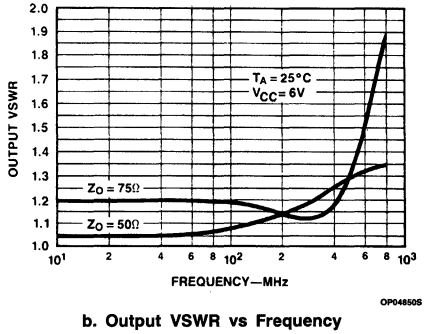
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second- and third-order output intercepts in dBm, and IMR_2 and IMR_3 are the second- and third- order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small-signal operat-



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 21. Input/Output VSWR vs Frequency

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ing range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point, the intermodulation products no longer follow the straight-line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select levels which are too low, because the test equipment may not be able to recover the signal from the noise. For the NE5204, an output level of −10.5dBm was chosen with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers*; by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985, published by John Wiley & Sons, Inc.

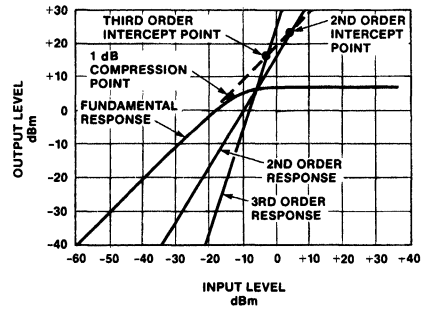


Figure 22

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

Signetics

NE/SA/SE5205
Wide-band High-Frequency Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA/SE5205 is a High Frequency Amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 650MHz. The metal can and Cerdip package are hermetically sealed, and can operate over the full −55°C to +125°C range.

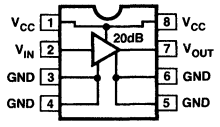
No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

PIN CONFIGURATIONS

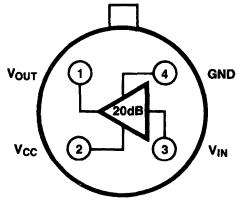
N, FE, D Packages



TOP VIEW

CD12760S

EC Package



CD09850S

NOTE:
Tab denotes Pin 1.

FEATURES

- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **Excellent performance in cable TV 75Ω systems**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

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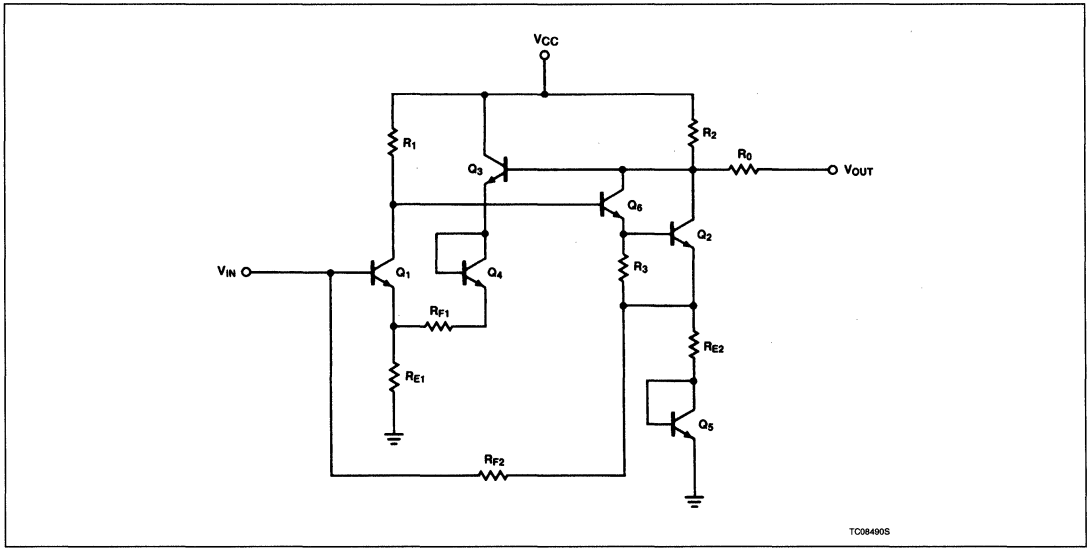
Wide-band High-Frequency Amplifier NE/SA/SE5205

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
8-Pin Metal can	0 to +70°C	NE5205EC
4-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	−40°C to +85°C	SA5205D
8-Pin Plastic DIP	−40°C to +85°C	SA5205N
8-Pin Cerdip	−40°C to +85°C	SA5205FE
8-Pin Cerdip	−55°C to +125°C	SE5205FE

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	−40 to +85	°C
	SE grade	−55 to +125	°C
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1, 2]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW
	EC package	1250	mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA/SE5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC − f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC − f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC − f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC − F_{MAX}				10			dB
S12	Isolation	f = 100MHz		−25			−25		dB
		DC − f_{MAX}	−18			−18			dB

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DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA/SE5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
f_{MAX}	Bandwidth	±0.5dB EC		300			500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	-3dB EC				600			MHz
f_{MAX}	Bandwidth	-3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+7.0			+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24			+24		dBm

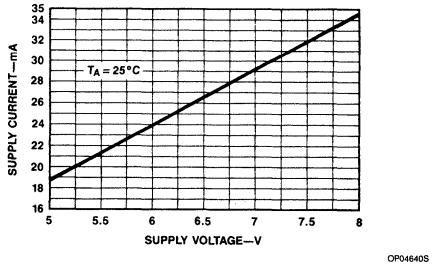

Figure 1. Supply Current vs Supply Voltage

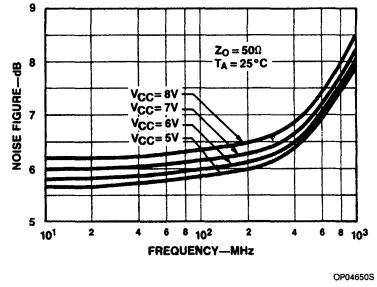

Figure 2. Noise Figure vs Frequency

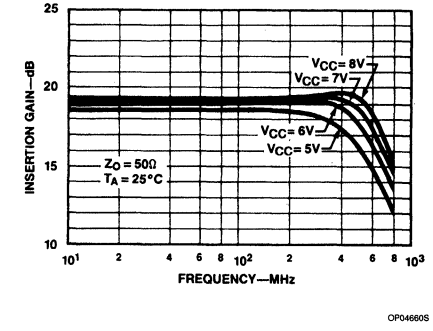

Figure 3. Insertion Gain vs Frequency (S_{21})

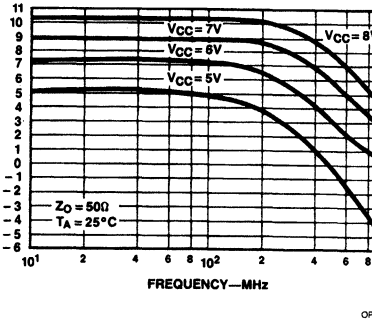

Figure 4. Insertion Gain vs Frequency (S_{21})

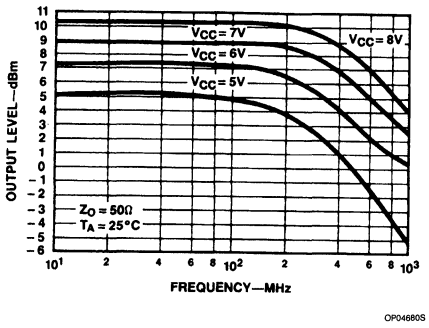

Figure 5. Saturated Output Power vs Frequency

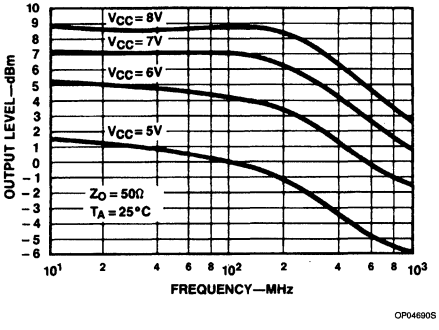

Figure 6. 1dB Gain Compression vs Frequency

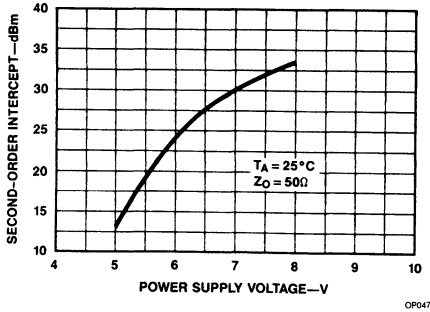

Figure 7. Second-Order Output Intercept vs Supply Voltage

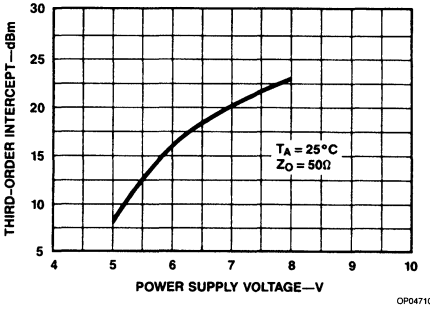

Figure 8. Third-Order Intercept vs Supply Voltage

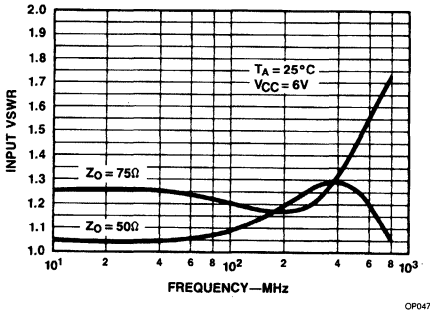

Figure 9. Input VSWR vs Frequency

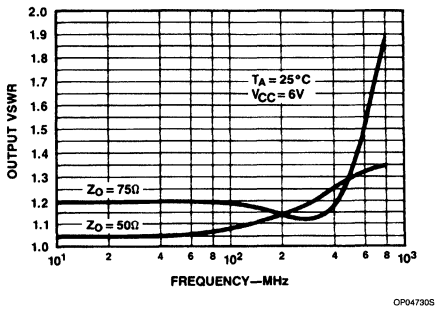

Figure 10. Output VSWR vs Frequency

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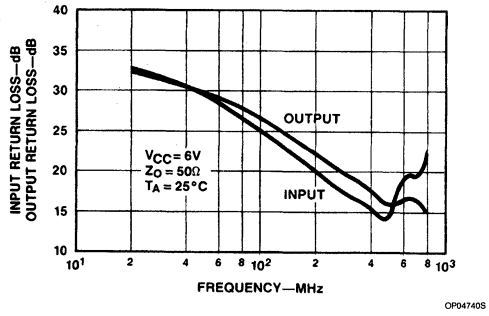


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

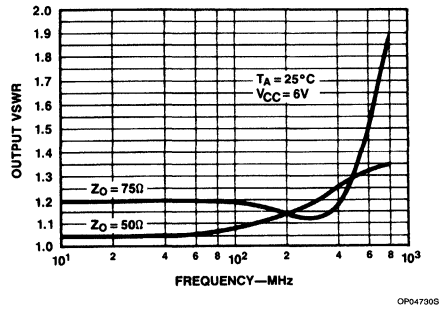


Figure 12. Isolation vs Frequency (S_{12})

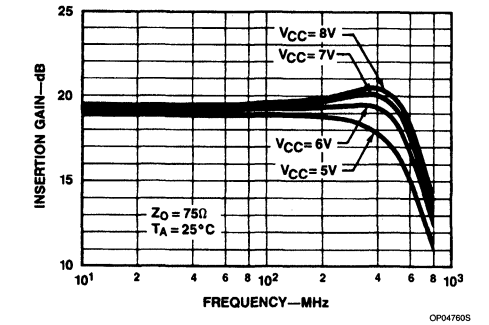


Figure 13. Insertion Gain vs Frequency (S_{21})

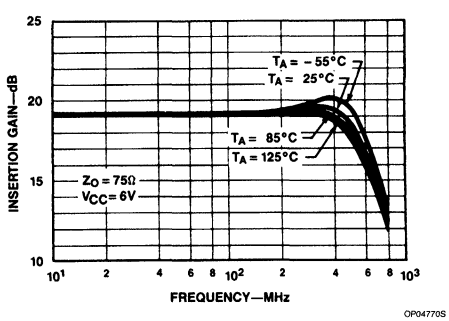


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log } \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0} \right\} \text{ dB} \quad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all

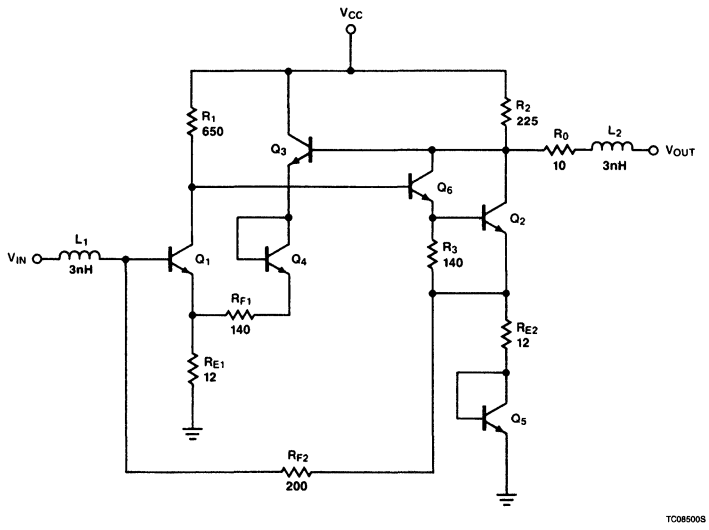


Figure 15. Schematic Diagram

11

GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

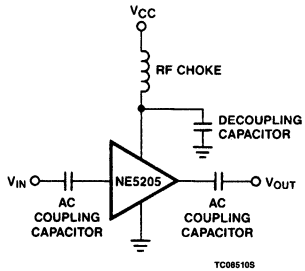
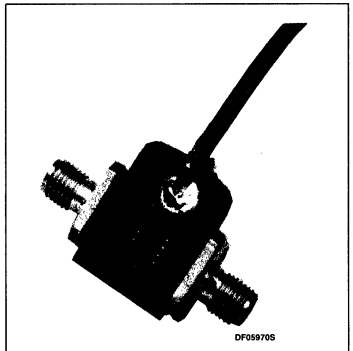


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



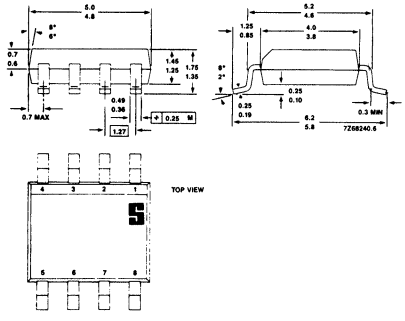
Both of the evaluation boards that will be discussed next do not have input and output capacitors because it is assumed the user will use AC coupled test systems. Chip or foil capacitors can easily be inserted between the part and connector if the board trace is removed.

50Ω EVALUATION BOARD

The evaluation board layout shown in Figure 17 produces excellent results. The board is to scale and is for the SO package but can be used for the EC package as well. Both top and bottom are copper clad and the ground planes are bonded together through 50Ω SMA cable connectors. These are solder mounted on the sides of the board so that the signal traces line up straight to the connector signal pins.

Solid copper tubing is soldered through the flange holes between the two connectors for increased strength and grounding characteristics. Two or four hole flanges can be used. A flat round decoupling capacitor is placed in the board's round hole and soldered between the bottom V_{CC} plane and the top side ground. The capacitor is as thin or thinner than the PC board thickness and has insulation around its side to isolate V_{CC} and ground. The square hole is for the SO package which is put in upside down through the bottom of the board so that the leads are kept in

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)



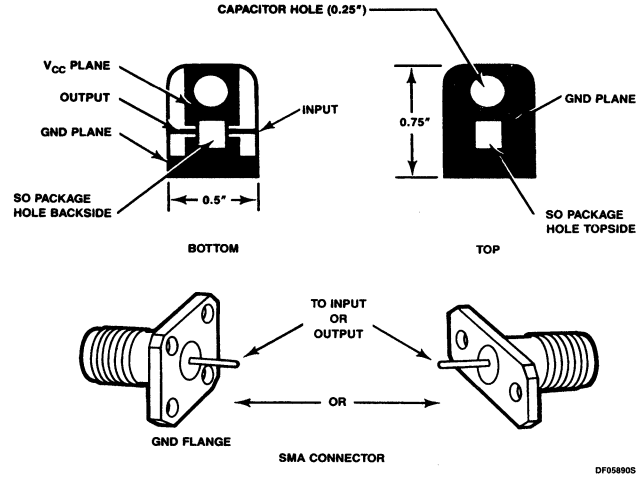


Figure 17. BC Board Layout for NE/SA/SE5205 Evaluation

position for soldering. Both holes are just slightly larger than the capacitor and IC to provide for a tight fit.

This board should be tested in a system with 50Ω input and output impedance for correct operation.

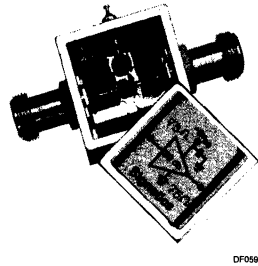
75Ω EVALUATION BOARD

Another evaluation board is shown in Figure 18. This system uses the same PC board as presented in Figure 17, but makes use of 75Ω female N-type connectors. The board is mounted in a nickel plated box* that is used to support the N-type connectors. This is an excellent way to test the part for cable TV applications. Again, the board should be tested in a system with 75Ω input and output impedance for correct operation.

*The box and connectors are available as a "MOD-PACK SYSTEM" from the ANZAC division of ADAMS-RUSSELL CO., INC., 80 Cambridge Street, Burlington, MA 01803.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.



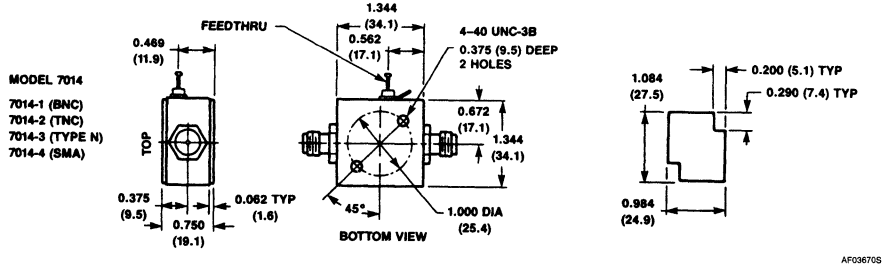


Figure 18. 75Ω N-Type Connector System

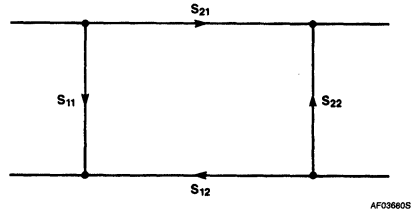


Figure 19a. Two-Port Network Defined

11

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

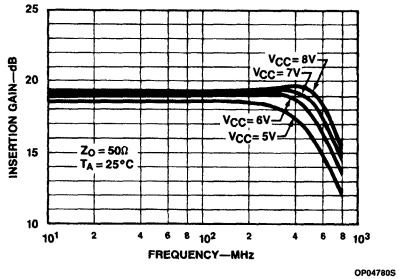
Figure 19b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 20. These were obtained with the device mounted in a PC board as described in Figures 17 and 18.

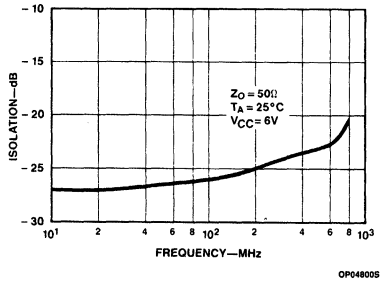
For 50Ω system measurements, SMA connectors were used. The 75Ω data was obtained using N-connectors.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high frequency amplifiers.

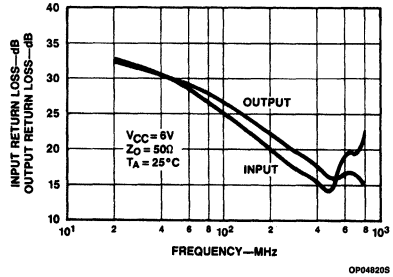
50Ω System



a. Insertion Gain vs Frequency (S_{21})

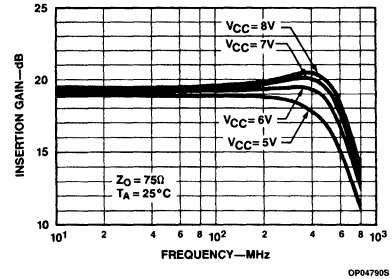


c. Isolation vs Frequency (S_{12})

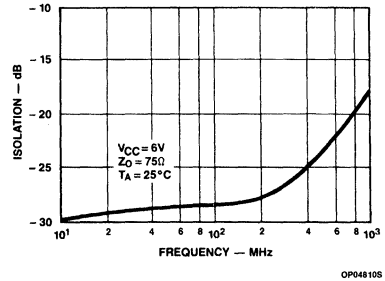


e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

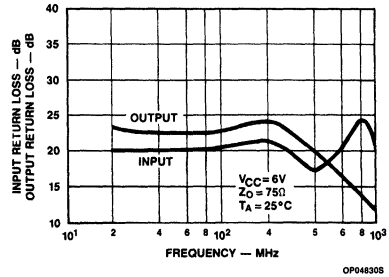
75Ω System



b. Insertion Gain vs Frequency (S_{21})



d. S_{12} Isolation vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \text{NE/SA/SE5205 } Z_D \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$

$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

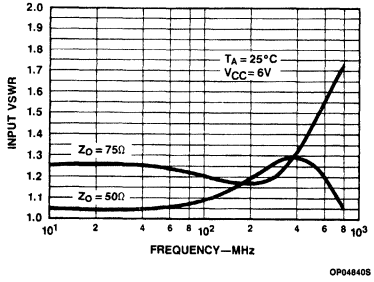
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

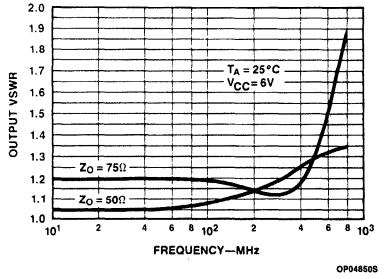
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 21. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

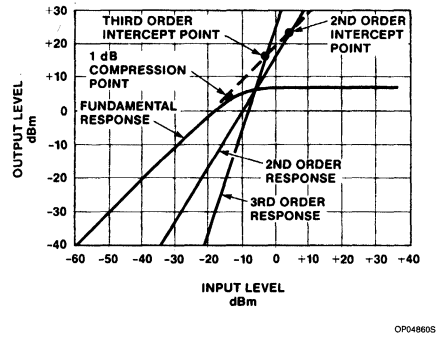


Figure 22

Signetics

Linear Products

NE/SE5539
Ultra-High Frequency Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

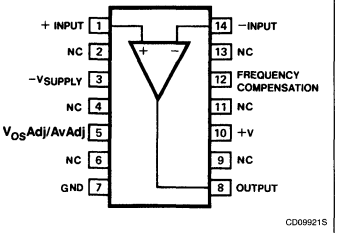
- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600/Vμs**
- **Full power response: 48MHz**
- **A_{VOL}: 52dB typical**
- **350MHz unity gain**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION

D, F, N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range NE SE	 0 to 70 −55 to +125	 °C °C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTE:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.

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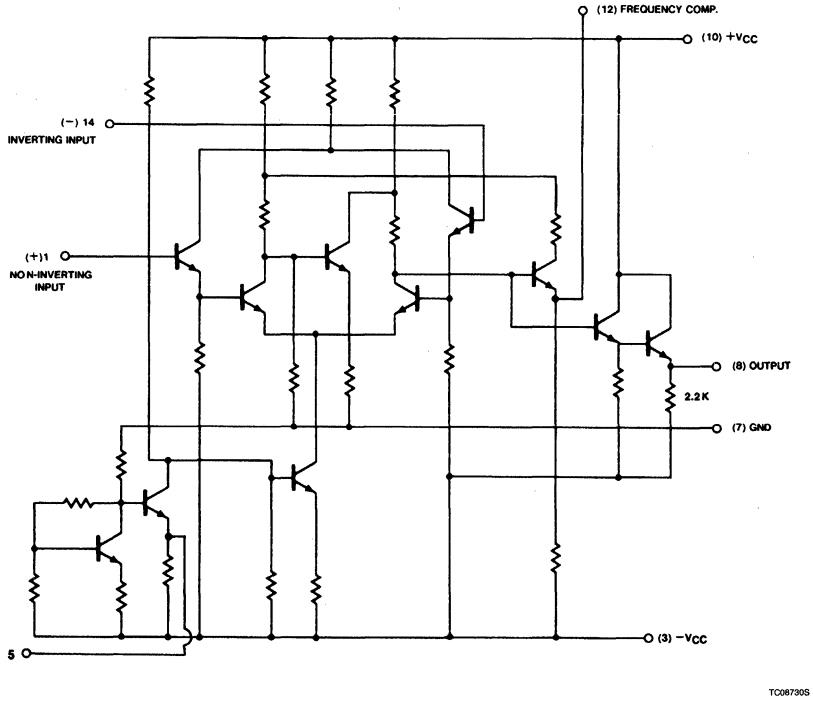
Ultra-High Frequency Operational Amplifier — NE/SE5539

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				−Swing	−1.5	−2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_0 = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_0 = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_0 = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_0 = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				−Swing	−1.1	−1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				−Swing	−1.4	−1.8		

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AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_O = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$		4			4		$nV/\sqrt{Hz}$

NOTE:
1. External compensation.

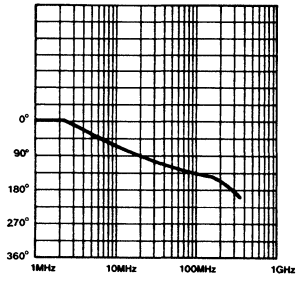
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2$[1]		120		MHz
t_S	Settling time	$A_{CL} = 2$[1]		23		ns
SR	Slew rate	$A_{CL} = 2$[1]		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$[1]		4.5		ns
	Full power response	$A_{CL} = 2$[1]		20		MHz

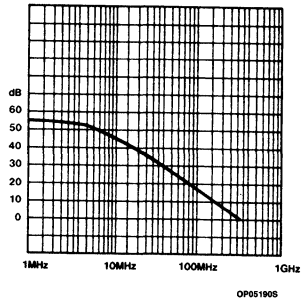
NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

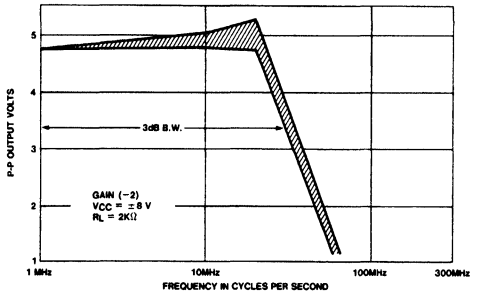


NE5539 Open-Loop Gain



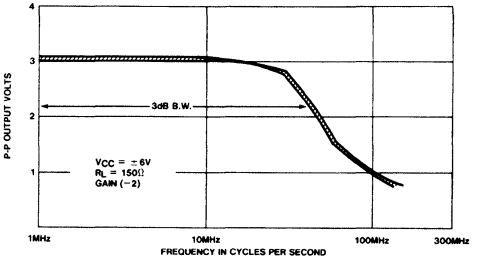
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



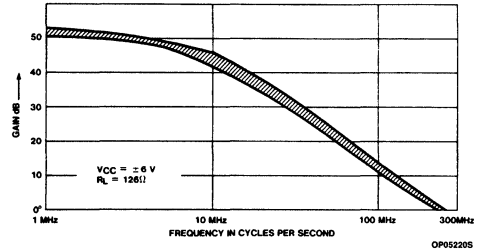
OP05200S

Power Bandwidth (NE)



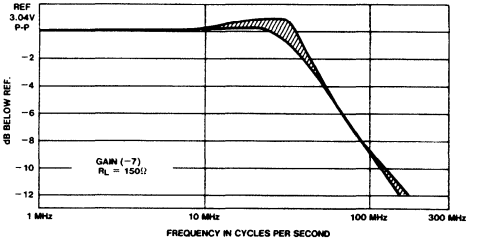
OP05210S

SE5539 Open-Loop Gain vs Frequency



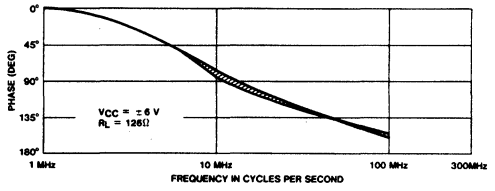
OP05220S

Power Bandwidth

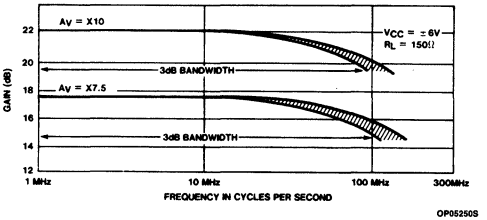


OP05230S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05250S

NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05240S

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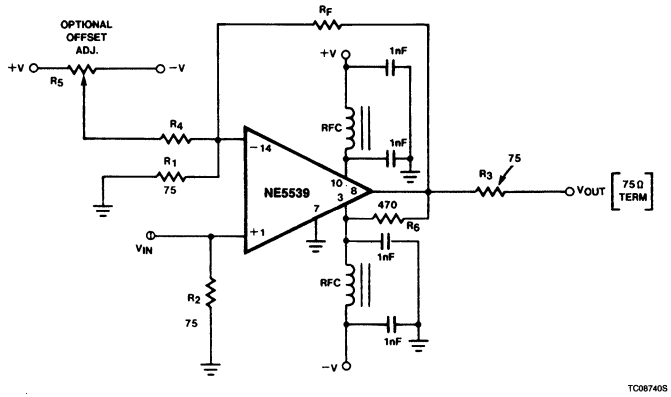
CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

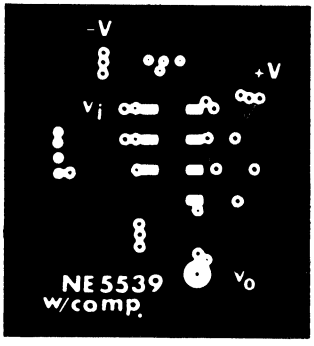


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

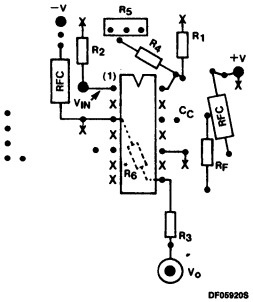
RFC 3T # 26 BUSSWIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



DF05910S

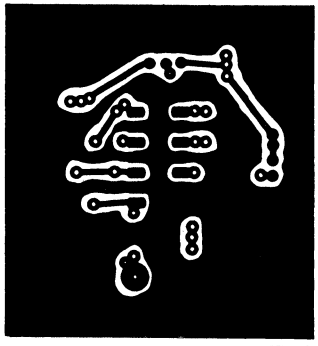
Component Side (Component Layout)



DF05920S

NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

Bottom Plane Copper[1]



DF05930S

NOTE:
Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

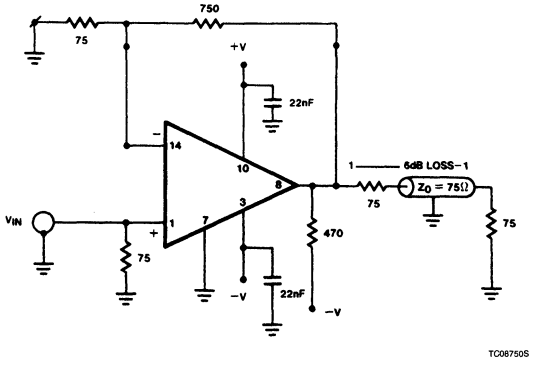


Figure 2. NE5539 Video Amplifier

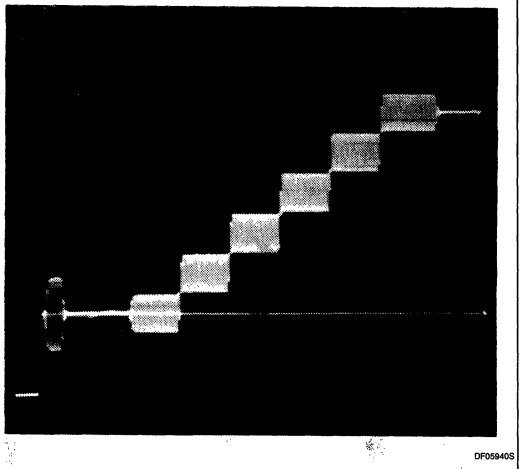


Figure 3. Input Signal

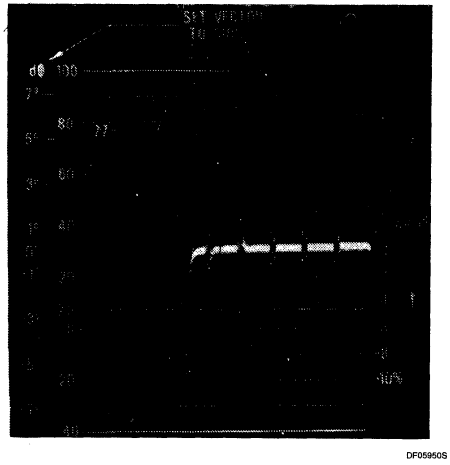


Figure 4. Differential Gain < 0.5%

NOTE:

1. Instruments used for these measurements were Tektronix, 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

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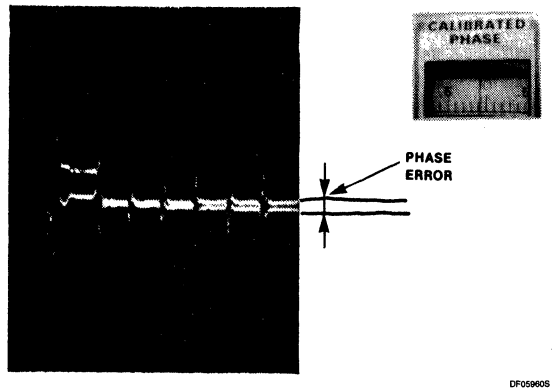


Figure 5. Differential Phase +0.1°

APPLICATIONS

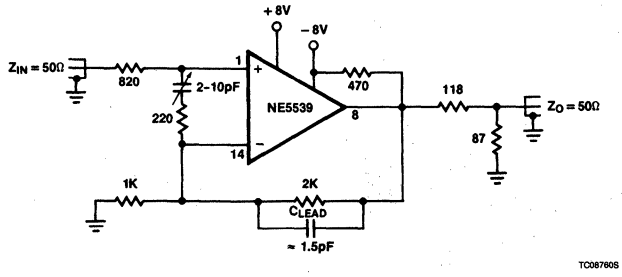


Figure 6. Non-Inverting Follower

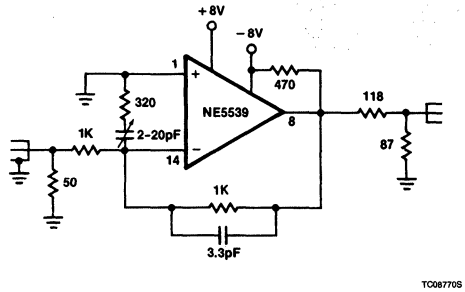


Figure 7. Inverting Follower

AN140
Compensation Techniques for Use With the NE/SE5539

Application Note

NE5539 DESCRIPTION

The Signetics NE/SE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today. With a unity gain bandwidth of 350MHz and a slew rate of 600V/μs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the NE/SE5539.

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1. The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude. This zero improves the phase margin.

To determine components, it can be shown that the optimal conditions for amplifier stability occur when:

$$(R1)(C_{DIST}) = (R_F)(C_{LEAD}) \quad (1)$$

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{LEAD} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{LEAD} = C_{DIST}\frac{R1}{R_F} \quad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary (Reference Figure 1). For practical applications, the following equations can be used to determine proper lag-lead components:

$$\frac{R_F}{R1/R_{LAG}} \geqslant 7 \quad (4)$$

Therefore,

$$R_{LAG} \leqslant \frac{R_F}{7 - R_F/R1} \quad (5)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{LAG} may now be approximated using:

$$W_{LAG} \cong \frac{2\pi(GBW)}{10}\ \text{Rad/Sec} \quad (6)$$

$$W_{LAG} = \frac{\pi(GBW)}{5}\ \text{Rad/Sec} \quad (7)$$

where

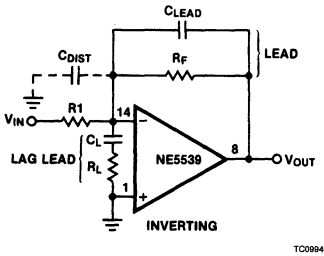
$$W_{LAG} = \frac{1}{(R_{LAG})(C_{LAG})} \quad (8)$$

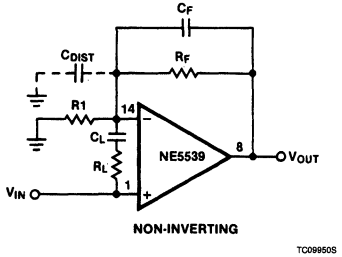
therefore,

$$\frac{\pi(GBW)}{5} = \frac{1}{(R_{LAG})(C_{LAG})} \quad (9)$$

and

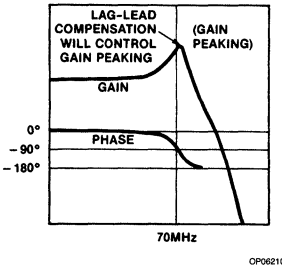
$$C_{LAG} = \frac{5}{\pi R_{LAG}(GBW)} \quad (10)$$



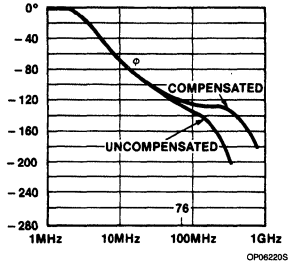


NOTES:
$C_L = C_{LAG}$
$R_L = R_{LAG}$

Figure 1. Standard Lag-Lead Compensation



a. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)



b. Open-Loop Phase

Figure 2

Compensation Techniques for Use With the NE/SE5539 AN140

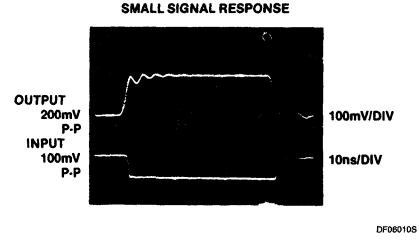


Figure 3. Compensated Pulse Response

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz, see Figures 2a and 2b.) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains. The result of using this technique is shown for a pulse amplifier in Figure 3.

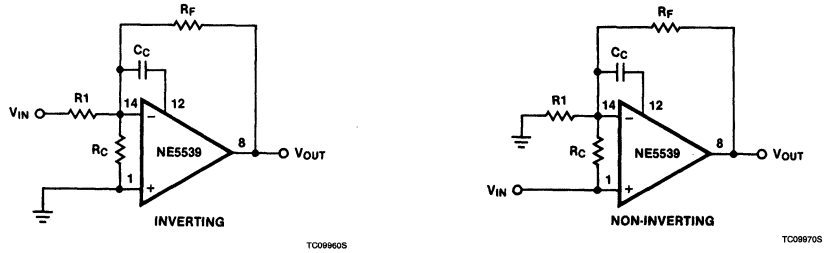


Figure 4. Pin 12 Compensation

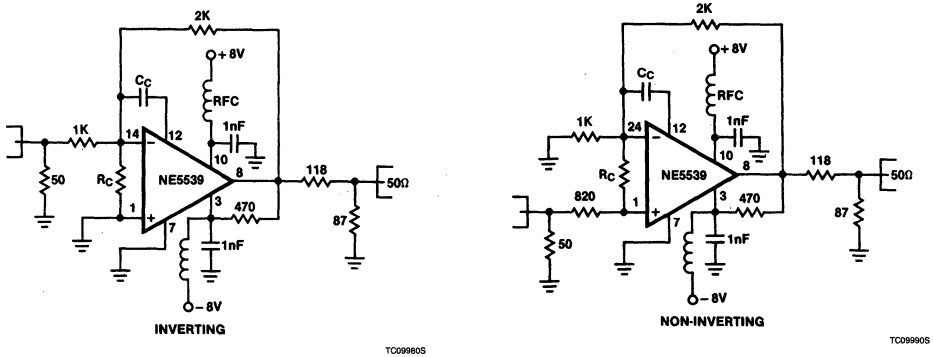


Figure 5. Pulse Response Test Circuits

Compensation Techniques for Use With the NE/SE5539 AN140

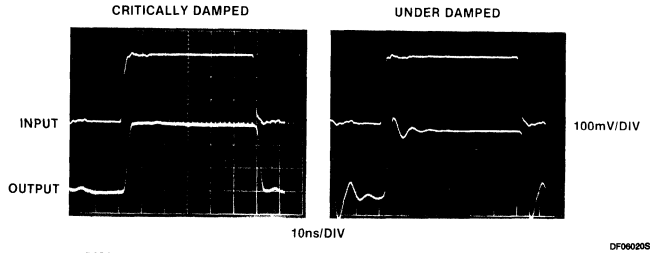


Figure 6. Small Signal Response — Non-Inverting

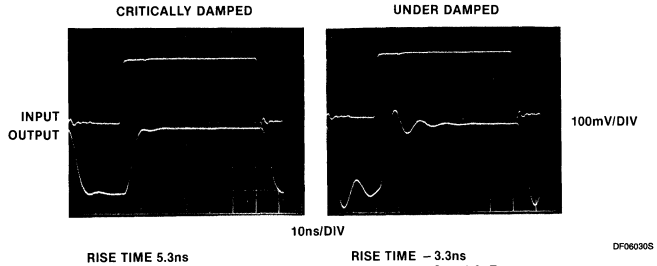


Figure 7. Small Signal Response — Inverting

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the NE/SE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most importantly, both methods are equally effective; i.e., a good wide-band amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using Pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

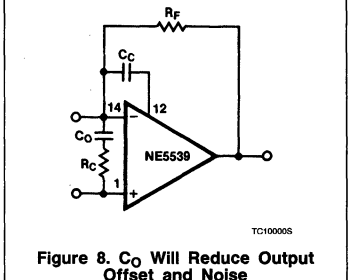


Figure 8. C_O Will Reduce Output Offset and Noise

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01μF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE NE/SE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1 A_2}{1 - (B_F A_2)} + A_3 (1 + B_F A_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11a. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12a and 12b. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to Pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13a through 13f. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

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Compensation Techniques for Use With the NE/SE5539 AN140

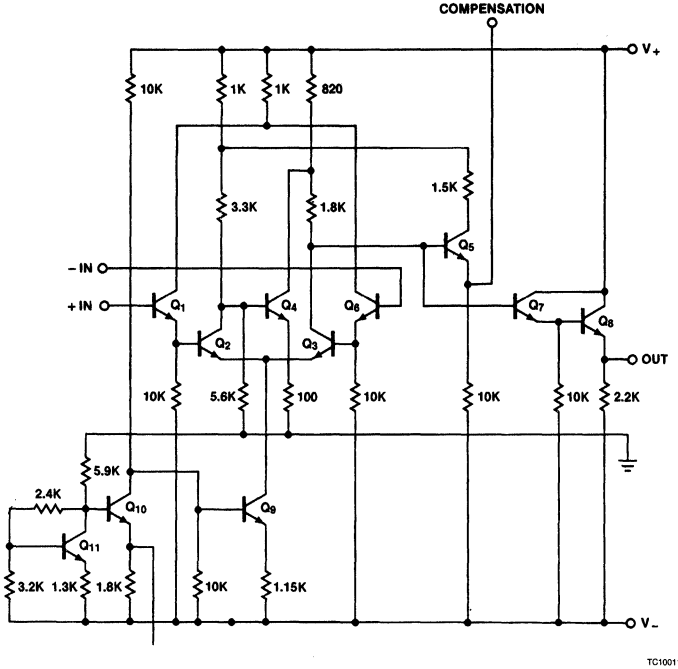


Figure 9. Complete Schematic of NE/SE5539

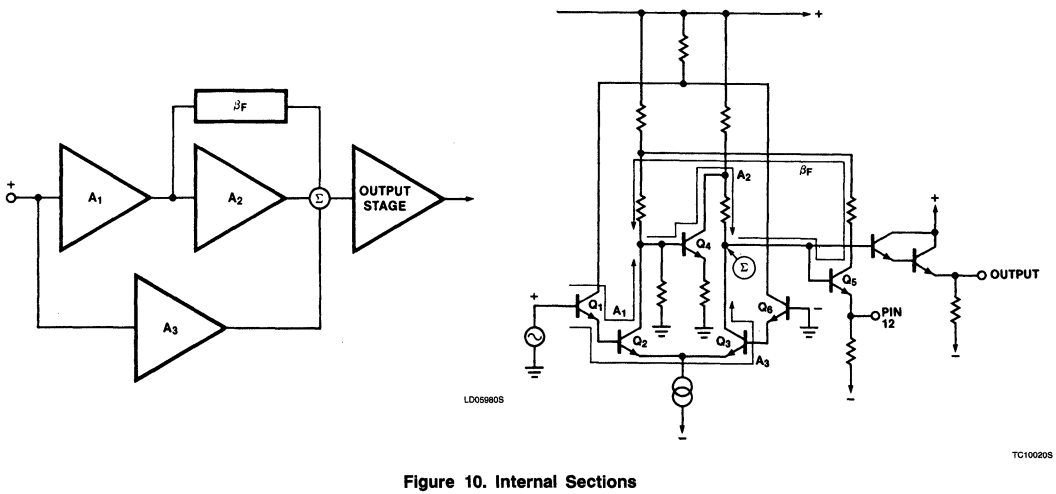
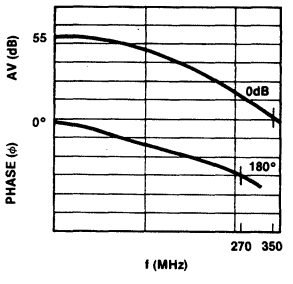


Figure 10. Internal Sections

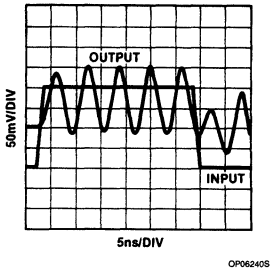
Compensation Techniques for Use With the NE/SE5539 AN140

COMPUTER ANALYSIS

The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. These models are then combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.



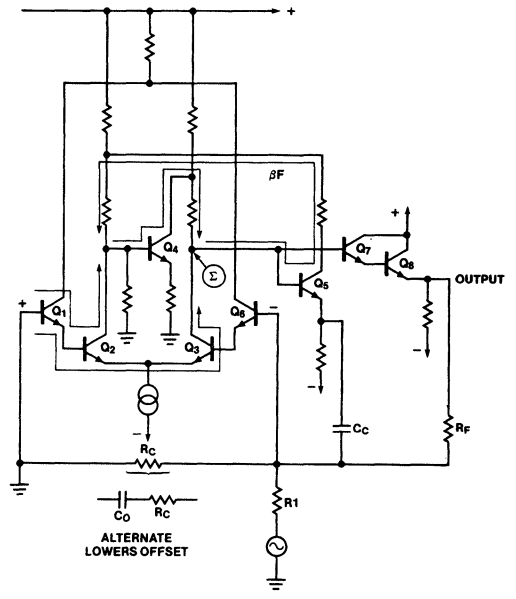
a. Open-Loop Gain — No Compensation (Computer Simulation)



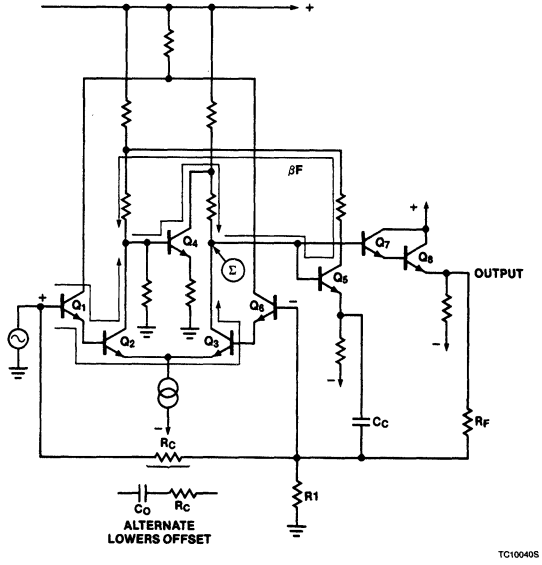
b. Closed-Loop Non-Inverting Response — No Compensation (Computer Simulation — Oscillation is Evident)

Figure 11

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.



a. Pin 12 Compensation Showing Internal Connections — Inverting

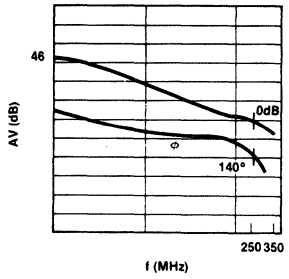


b. Pin 12 Compensation Showing Internal Connections — Non-Inverting

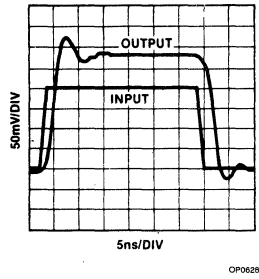
Figure 12

11

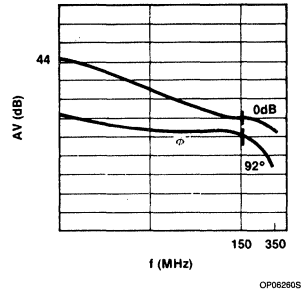
Compensation Techniques for Use With the NE/SE5539 AN140



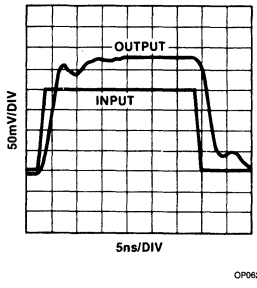
a. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 1pF$, (Computer Simulation)



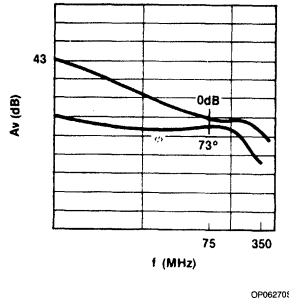
b. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 1pF$, $A_V = 3$ (Computer Simulation — Underdamped)



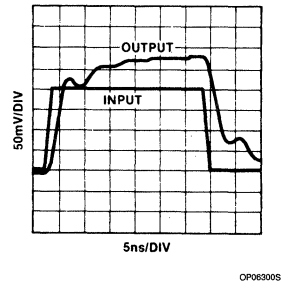
c. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 2pF$ (Computer Simulation)



d. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 2pF$, $Av = 3$ (Computer Simulation — Critically-Damped)



e. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 3pF$, (Computer Simulation)



f. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 3pF$, $A_V = 3$ (Computer Simulation — Overdamped)

Figure 13

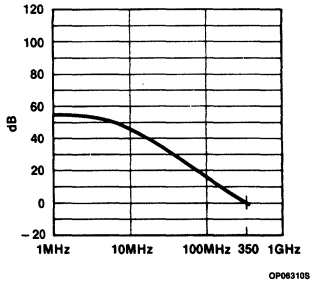


Figure 14. Actual Open-Loop Gain Measured in Lab

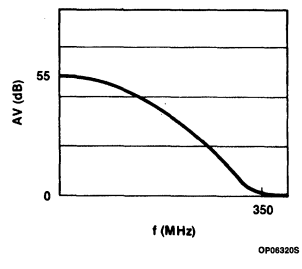


Figure 15. Computer-Generated Open-Loop Gain

1. J. Millman and C. C. Halkias: *Integrated Electronics: Analog and Digital Circuits and Systems,* McGraw-Hill Book Company, New York, 1972.

2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sanquiovanni-Vincentelli: "Spice Version 2G," University of California, Berkeley, California, August 10, 1981.

3. Signetics: *Analog Data Manual 1983,* Signetics Corporation, Sunnyvale, California 1983.

Signetics

NE5592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

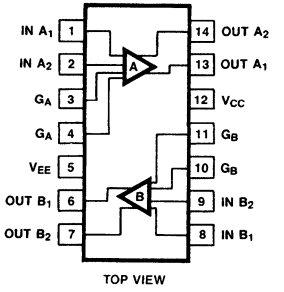
- **120MHz bandwidth**
- **Adjustable gain from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATION

D, N Packages



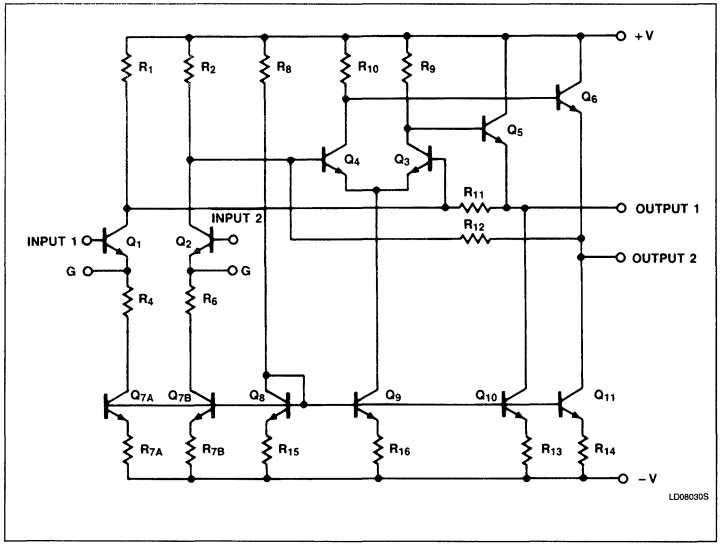
TOP VIEW

CD13050S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



LD08030S

11

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = ±6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage is $V_S = ±6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	μA
I_{BIAS}	Input bias current			5	20	μA
	Input noise voltage	BW 1kHz to 10MHz		4		$nV/\sqrt{Hz}$
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f < 100kHz V_{CM} ± 1V, f = 5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S = ± 0.5V	50	85		dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; f = 100kHz (output referenced) $R_L = 1k\Omega$	65	75		dB
V_{OS}	Output offset voltage gain select pins open	$R_L = \infty$ $R_L = \infty$		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$		35	44	mA

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $R_S = \phi$	55			dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		75		dB
V_{OS}	Output offset voltage gain select pins connected together	$R_L = \infty$			1.5	V
	gain select pins open	$R_L = \infty$			1.0	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$			47	mA

AC ELECTRICAL CHARACTERISTICS

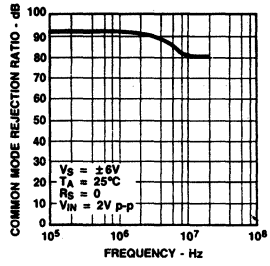
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	$V_{OUT} = 1V_{P-P}$		25	20	MHz
t_R	Rise time			15		ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$		7.5	12	ns

11

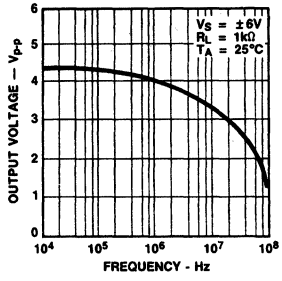
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



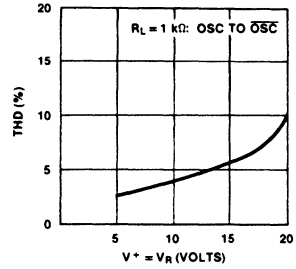
OP18580S

Output Voltage Swing as a Function of Frequency



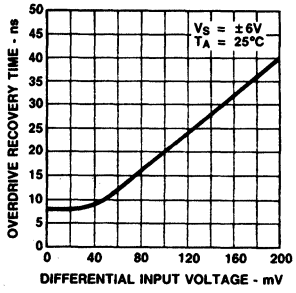
OP18590S

Channel Separation as a Function of Frequency



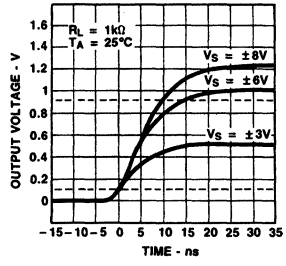
OP18500S

Differential Overdrive Recovery Time



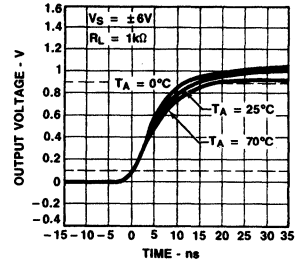
OP18610S

Pulse Response as a Function of Supply Voltage



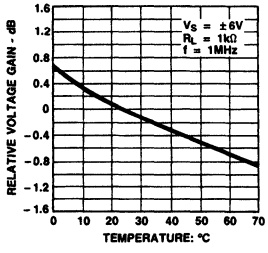
OP18620S

Pulse Response as a Function of Temperature



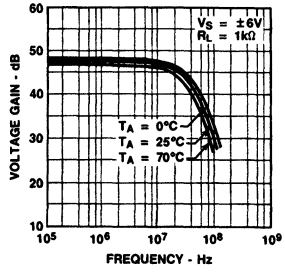
OP18630S

Voltage Gain as a Function of Temperature



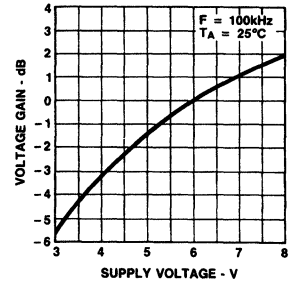
OP18640S

Gain vs Frequency as a Function of Temperature



OP18650S

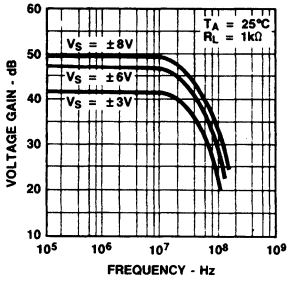
Voltage Gain as a Function of Supply Voltage



OP18660S

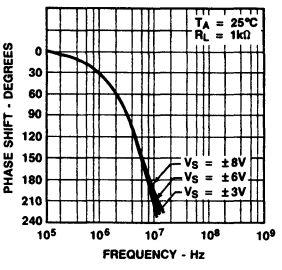
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



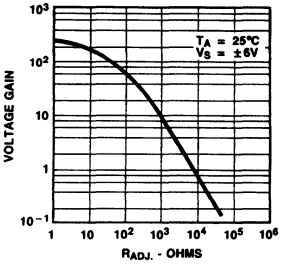
OP18670S

Phase vs Frequency as a Function of Supply Voltage



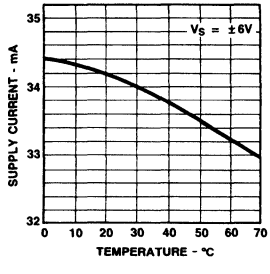
OP18680S

Voltage Gain as a Function of R_{ADJ}



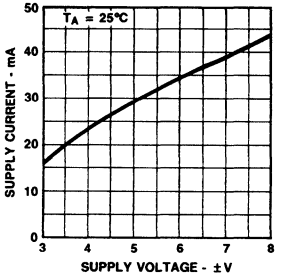
OP18690S

Supply Current as a Function of Temperature



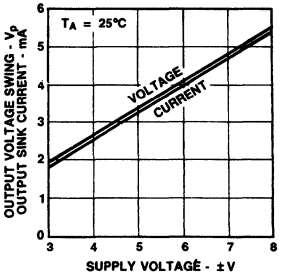
OP18700S

Supply Current as a Function of Supply Voltage



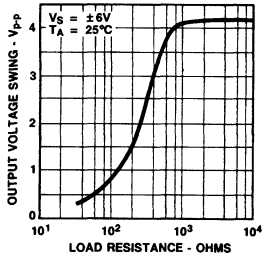
OP18710S

Output Voltage Swing and Sink Current as a Function of Supply Voltage



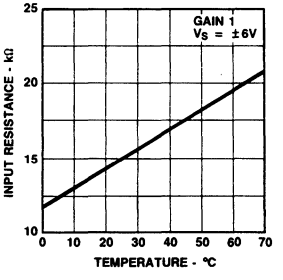
OP18720S

Output Voltage Swing as a Function of Load Resistance



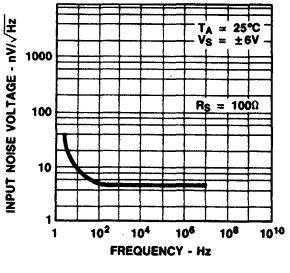
OP18730S

Input Resistance as a Function of Temperature



OP18740S

Input Noise Voltage as a Function of Frequency

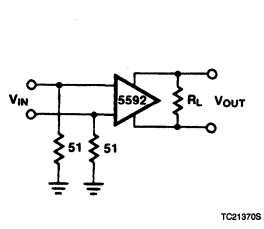


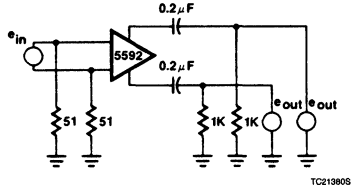
OP18750S

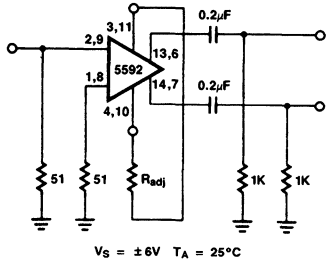
11

Video Amplifier | NE5592

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.







Signetics

NE/SE592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

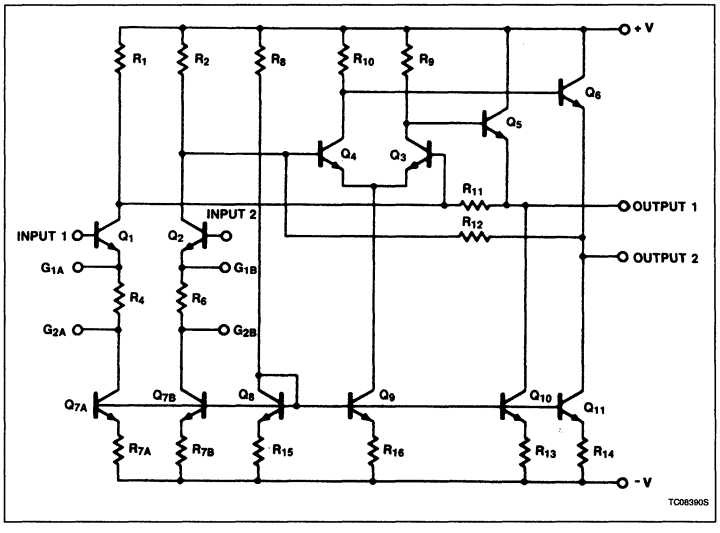
FEATURES

- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

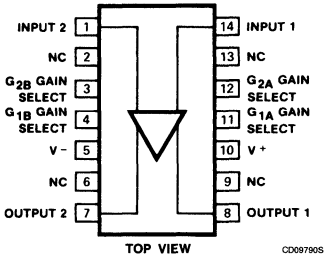
- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

EQUIVALENT CIRCUIT

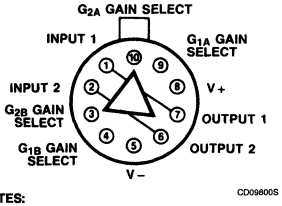


PIN CONFIGURATIONS

D, F, N Packages

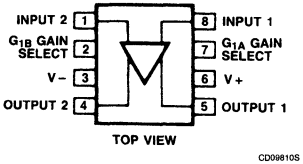


H Package*



NOTES:
Pin 5 connected to case.
*Metal cans (H) not recommended for new designs.

D, F, N, Packages



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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	−55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic Dip	0 to +70°C	NE592N8
8-Pin Cerdip	−55°C to +125°C	SE592F8
8-Pin SO	0 to +70°C	NE592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	−55°C to +125°C	SE592H

NOTE:
Also N8, N14, D8 and D14 package parts available in "High" gain version by adding "H" before package designation, as: NE592HD8.

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range SE592 NE592	 −55 to +125 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2, 4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	V_{CM} ± 1V, f < 100kHz	60	86		60	86		dB
	Gain 2[4]	V_{CM} ± 1V, f = 5MHz		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

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DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$ for NE592; $-55°C \leq T_A \leq 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part Gain 1[1] Gain 2[2, 4]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80		 600 120	 200 80		 600 120	 V/V V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance Gain 2[2, 4]		 8.0			 8.0			 kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	 50			 50			 dB
PSRR	Supply voltage rejection ratio Gain 2[4]	$\Delta V_S = \pm 0.5V$	 50			 50			 dB
V_{OS}	Output offset voltage Gain 1 Gain 2[4] Gain 3[3]	 $R_L = \infty$ $R_L = \infty$ $R_L = \infty$			 1.5 1.5 1.0			 1.5 1.2 1.0	 V V V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

AC ELECTRICAL CHARACTERISTICS

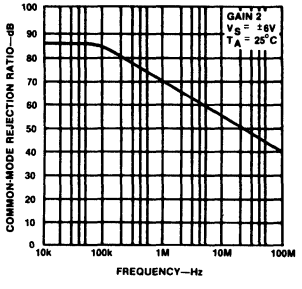
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth Gain 1[1] Gain 2[2, 4]			 40 90			 40 90		 MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2, 4]	$V_{OUT} = 1V_{P-P}$		 10.5 4.5	 12		 10.5 4.5	 10	 ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2, 4]	$V_{OUT} = 1V_{P-P}$		 7.5 6.0	 10		 7.5 6.0	 10	 ns ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

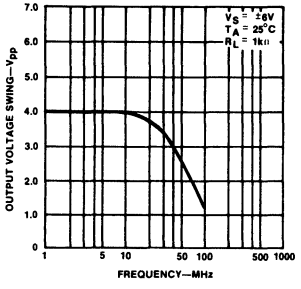
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



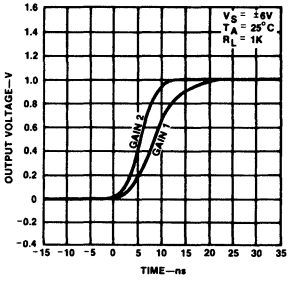
OP04421S

Output Voltage Swing As a Function of Frequency



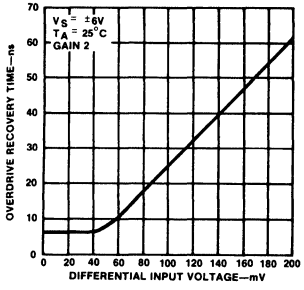
OP04430S

Pulse Response



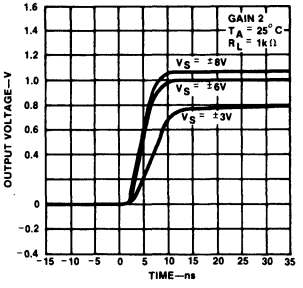
OP04440S

Differential Overdrive Recovery Time



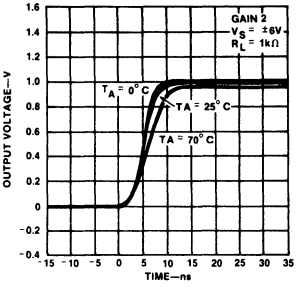
OP04450S

Pulse Response as a Function of Supply Voltage



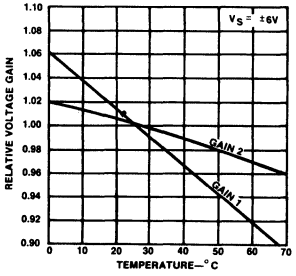
OP04460S

Pulse Response as a Function of Temperature



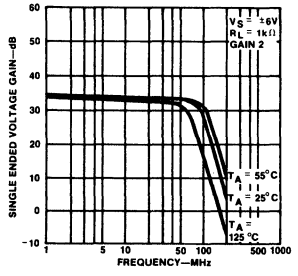
OP04470S

Voltage Gain as a Function of Temperature



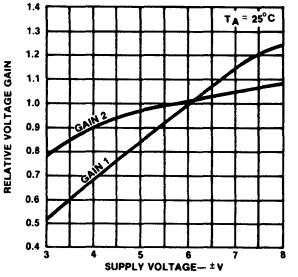
OP04480S

Gain vs Frequency as a Function of Temperature



OP04490S

Voltage Gain as a Function of Supply Voltage



OP04500S

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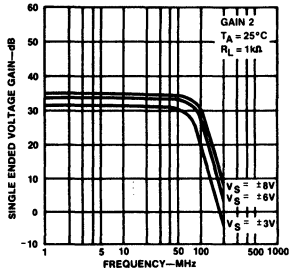
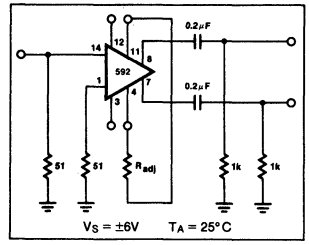
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



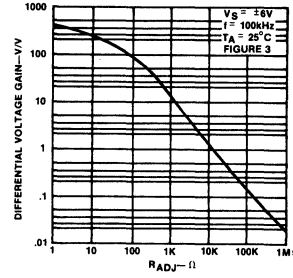
OP04510S

Voltage Gain Adjust Circuit



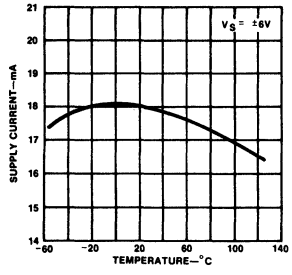
OP04521S

Voltage Gain as a Function of RADJ (Figure 3)



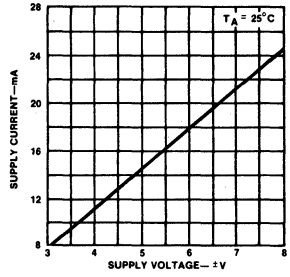
OP04530S

Supply Current as a Function of Temperature



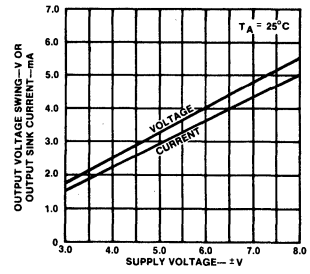
OP04540S

Supply Current as a Function of Supply Voltage



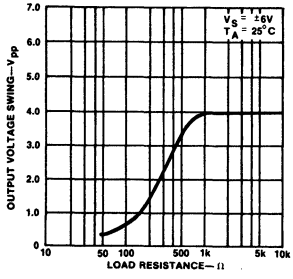
OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage



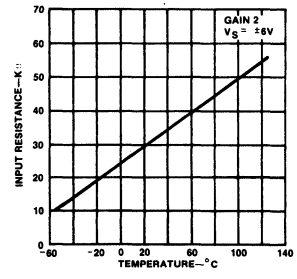
OP04560S

Output Voltage Swing as a Function of Load Resistance



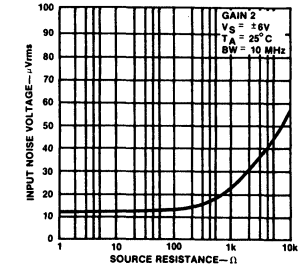
OP04570S

Input Resistance as a Function of Temperature



OP04580S

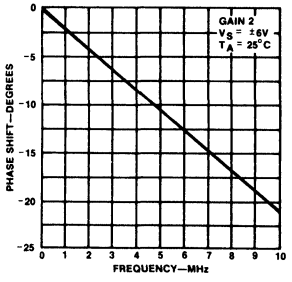
Input Noise Voltage as a Function of Source Resistance



OP04590S

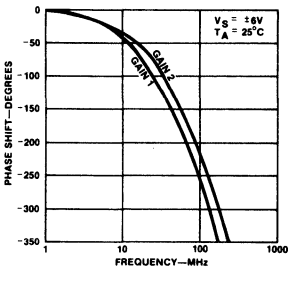
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency



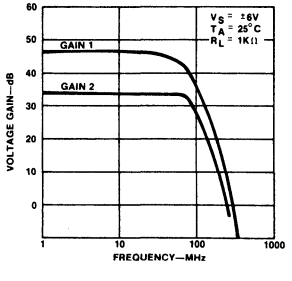
OP04600S

Phase Shift as a Function of Frequency



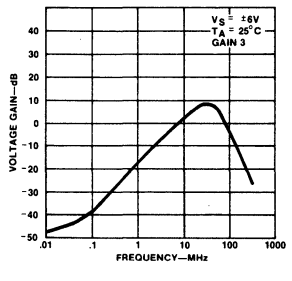
OP04610S

Voltage Gain as a Function of Frequency



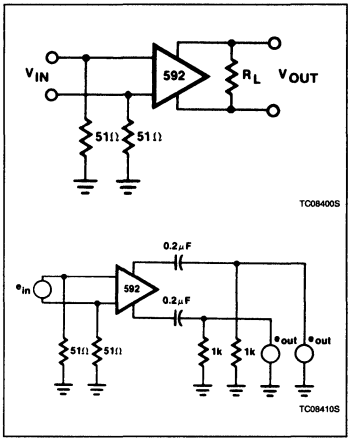
OP04620S

Voltage Gain as a Function of Frequency (All Gain Select Pins Open)



OP04630S

TEST CIRCUITS T_A = 25°C, unless otherwise specified.



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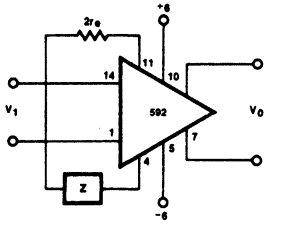
Video Amplifier | NE/SE592

TYPICAL APPLICATIONS

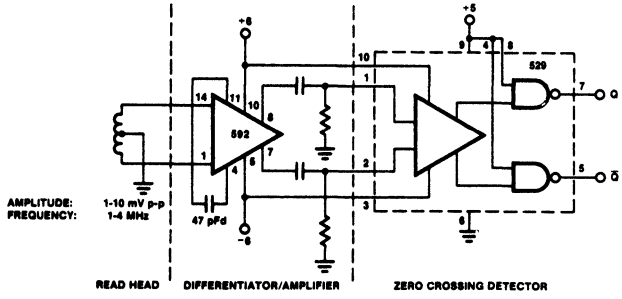


TC08420S

NOTE:

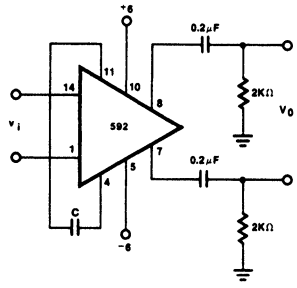
$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration



TC08430S

Disc/Tape Phase-Modulated Readback Systems



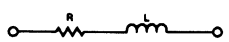
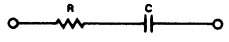
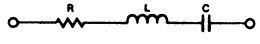
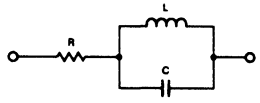
TC08440S

NOTE:
For frequency $F_1 << \frac{1}{2\pi(32)C}$

$$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation With High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

TC06422S

NOTE:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

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Signetics

Linear Products

AN141
Using the NE/SE592 Video Amplifier

Application Note

VIDEO AMPLIFIER PRODUCTS

NE/SE592 Video Amplifier

The 592 is a two-stage differential output, wide-band video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins $G_{1A} - G_{1B}$ and $G_{2A} - G_{2B}$, respectively. As shown by Figure 1, the emitter circuits of the differential pair return through independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus, the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400V/V. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single-ended gains are one-half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer, the input bias current required by the 592 may be passed directly through the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a DC path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output DC offset, they should be small — ideally 0Ω. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).

Table 1. Video Amplifier Comparison File

PARAMETER	NE/SE592	733
Bandwidth (MHz)	120	120
Gain	0,100,400	10,100,400
R_{IN} (k)	4 – 30	4 – 250
V_{P-P} (Vs)	4.0	4.0

2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V – 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \quad (1)$$

$$= \frac{0.005V}{5\mu A}$$

$$= 1.00k\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of PNP transistors and standard level-shifting techniques used in lower frequency devices. Thus, without the aid of level shifting, the output common-mode voltage present on the NE592 is typically 2.9V. Most applications, therefore, require capacitive coupling to the load. An exception to the rule is a differential amplifier with an input common-mode range greater than +2.9V as shown in Figure 2. In this circuit, the NE592 drives a NE511B transistor array connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of $48V_{P-P}$ with a 3dB bandwidth of approximately 10MHz (depending on the capacitive load). For optimum operation, R1 is set for a no-signal level of +18V. The emitter resistors, R_E, were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain selected point of the NE592.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources.

Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 3, the overall gain at low frequencies is a negative 48dB.

Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB, or unity.

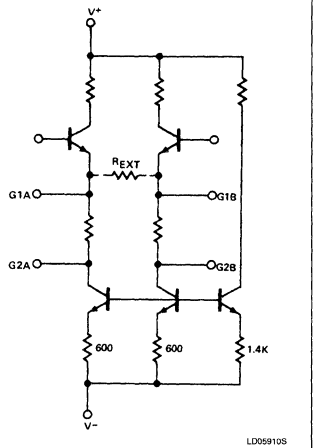
Referring to Figure 4, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA, causing the quantity of 2 r_e to be approximately 32Ω. Overall device gain is thus given by

$$\frac{V_O(s)}{V_{IN}(s)} = \frac{1.4 \times 10^4}{Z_{(S)} + 32} \quad (2)$$

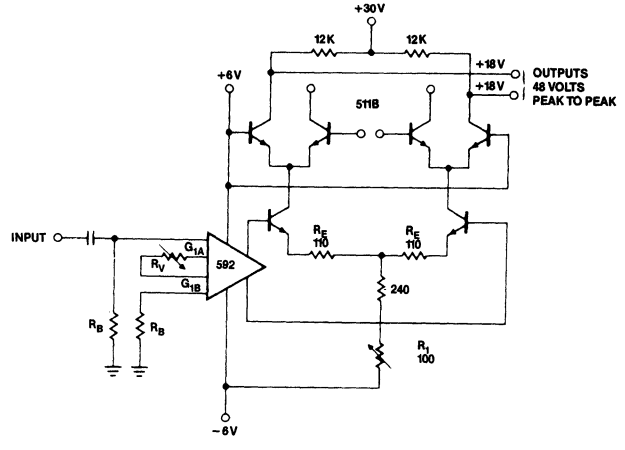
where $Z_{(S)}$ can be resistance or a reactive impedance. Table 2 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 2 is the gain calculation to determine the voltage gain as a function of frequency.

Using the NE/SE592 Video Amplifier AN141



NOTE:
All resistor values are in ohms.

Figure 1. 592 Input Structure



NOTE:
All resistor values are in ohms.

Figure 2. Video Amplifier With High Level Differential Output

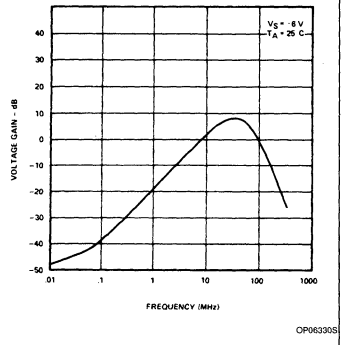
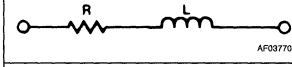
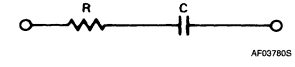
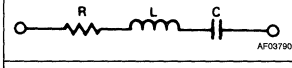
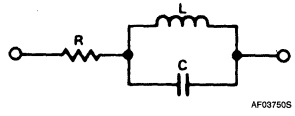


Figure 3. Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

Table 2. Filter Networks

Z NETWORK	FILTER TYPE	$V_0(s)/V_1(s)$ TRANSFER FUNCTION
 AF03770S	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
 AF03780S	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
 AF03790S	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
 AF03750S	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: In the networks above, the R value used is assumed to include 2 r_e, or approximately 32Ω.

Differentiation

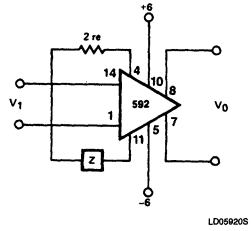
With the addition of a capacitor across the gain select terminals, the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common-mode rejection for proper operation. Figure 5 shows a differential amplifier configuration with transfer function.

Disc File Decoding

In recovering data from disc or drum files, several steps must be taken to precondition the linear data. The NE592 video amplifier, coupled with the 8T20 bidirectional one-shot, provides all the signal conditioning necessary for phase-encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV_{P-P} to 3mV_{P-P} for oxide coated disc files and 1 to 20mV_{P-P} for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

Using the NE/SE592 Video Amplifier AN141

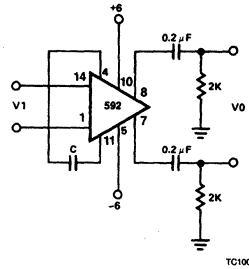


NOTE:

$$\frac{V_0(s)}{V_1(s)} = \frac{1.4 \times 10^4}{Z(s) + 2re}$$

$$= \frac{1.4 \times 10^4}{Z(s) + 32}$$

Figure 4. Basic Gain Configuration for NE592, N14



NOTES:
For frequency $F_1 < < 1/2\pi(32)C$

$V_0 \cong 1.4 \times 10^4 C \frac{d_{vi}}{dT}$

All resistor values are in ohms.

Figure 5. Differential With High Common-Mode Noise Rejection

The classical approach to peak time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 6. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wide-band AC-coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common-mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at DC due to the capacitance across the gain select terminals.

The output of the first stage amplifier is routed to a linear phase shift low-pass filter. The filter is a single-stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$$L = {}^{2R}/_{\omega_C}$$

where
R = characteristic impedance (Ω)

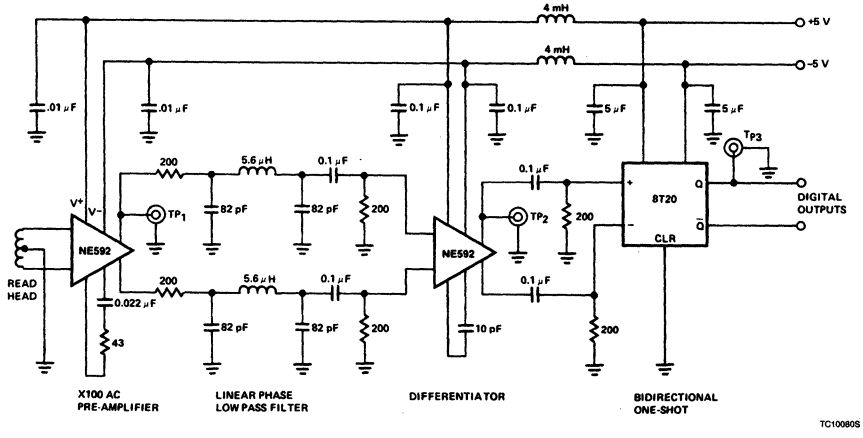
$$C = {}^{1}/_{\omega_C}$$

where
ω_C = cut-off frequency (radians/sec)

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common-mode noise rejection.

The output of the differentiator/amplifier is connected to the 8T20 bidirectional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

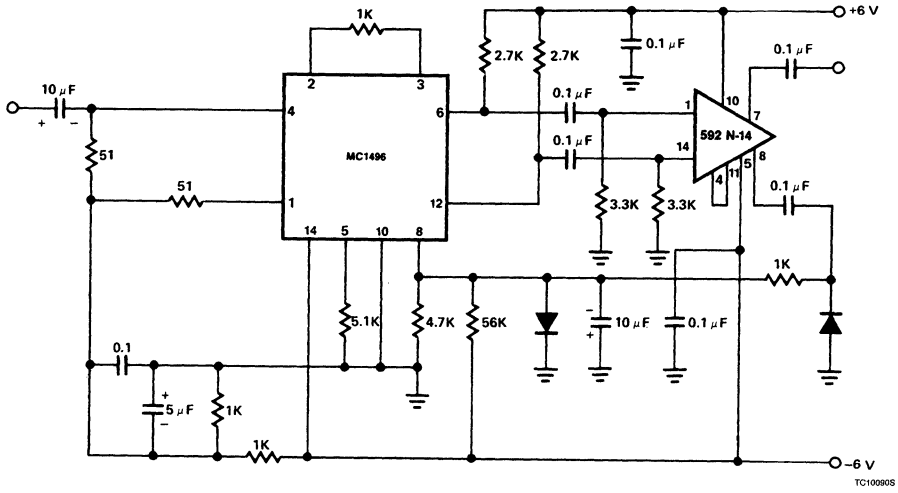
The circuit in Figure 6 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 8.



NOTE:
All resistor values are in ohms

Figure 6. 5MHz Phase-Encoded Data Read Circuitry

Using the NE/SE592 Video Amplifier AN141



NOTE:
All resistor values are in ohms

Figure 7. Wide-band AGC Amplifier

Automatic Gain Control

The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system.

The signal is fed to the signal input of the MC1496 and RC-coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass through unattenuated. Rectifying and filtering one of the NE592 outputs produces a DC signal which is proportional to the AC signal amplitude. After filtering; this control signal is applied to the MC1496 causing its gain to change.

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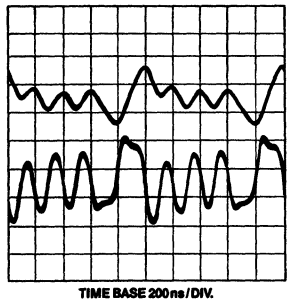


Figure 8. Test Results of Disc File Decoder Circuit

Signetics

μA733/733C
Differential Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

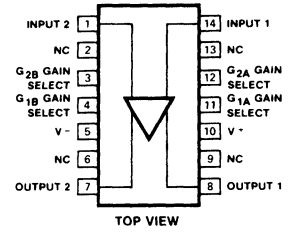
- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10, 100, and 400**
- **No frequency compensation required**
- **MIL-STD-883A, B, C available**

APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

PIN CONFIGURATION

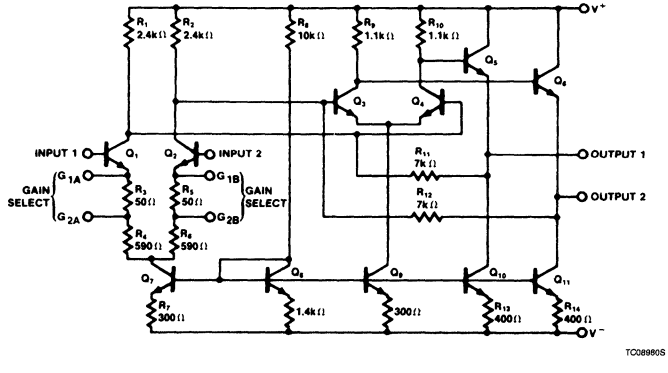
F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Ceramic DIP	−55°C to +125°C	μA733F
14-Pin Plastic DIP	−55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN
14-Pin Ceramic DIP	0 to +70°C	μA733CF

CIRCUIT SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range μA733C μA733	 0 to +70 −55 to +125	 °C °C
P_{MAX}	Maximum power dissipation[1] 25°C ambient temperature (still-air) F package N package	 1190 1420	 mW mW

NOTE:

1. The following derating factors should be applied above 25°C:
   F package at 9.5mW/°C
   N package at 11.4mW/°C.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±6V, V_{CM} = 0, unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain Gain 1[2] Gain 2[2] Gain 3[3]	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$	 250 80 8	 400 100 10	 600 120 12	 300 90 9	 400 100 10	 500 110 11	 V/V V/V V/V
BW	Bandwidth Gain 1[1] Gain 2[2] Gain 3[3]			 40 90 120			 40 90 120		 MHz MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = $1V_{P-P}$		 10.5 4.5 2.5	 12 		 10.5 4.5 2.5	 10 	 ns ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2] Gain 3[3]	V_{OUT} = $1V_{P-P}$		 7.5 6.0 3.6	 10 		 7.5 6.0 3.6	 10 	 ns ns ns
R_{IN}	Input resistance Gain 1[2] Gain 2[2] Gain 3[3]		 10	 4.0 30 250	 	 20	 4.0 30 250	 	 kΩ kΩ kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW = 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2 Gain 2	 V_{CM} = ±1V, f ≤ 100kHz V_{CM} = ±1V, f = 5MHz	 60	 86 60	 	 60	 86 60	 	 dB dB
SVRR	Supply voltage rejection ratio Gain 2	ΔV_S = ±0.5V	50	70		50	70		dB

DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = +25°C$, $V_S = \pm 6V$, $V_{CM} = 0$, unless otherwise specified.
Recommended operating supply voltages $V_S = \pm 6.0V$.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$		 0.6 0.35	 1.5 1.5		 0.6 0.35	 1.5 1.0	 V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			$0°C \leq T_A \leq 70°C$			$-55°C \leq T_A \leq 125°C$			
	Differential voltage gain Gain 1[1] Gain 2[2] Gain[3]	$R_l = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	 250 80 8		 600 120 12	 200 80 8		 600 120 12	 V/V V/V V/V
R_{IN}	Input resistance Gain 2[2]		 8			 8			 kΩ
I_{OS}	Input offset current				6			5	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio Gain 2	$V_{CM} = \pm V$, $F \leq 100kHz$	 50			 50			 dB
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	 50			 50			 dB
V_{OS}	Output offset voltage Gain 1[1] Gain 2 and 3[2, 3]	$R_L = \infty$			 1.5 1.5			 1.5 1.2	 V V
V_{DIFF}	Output voltage swing, differential	$R_L = 2k\Omega$	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

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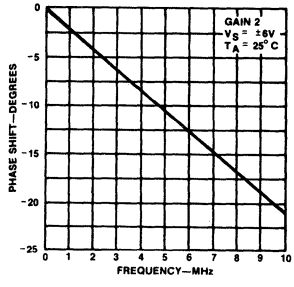
TYPICAL PERFORMANCE CHARACTERISTICS

Phase Shift as a Function of Frequency



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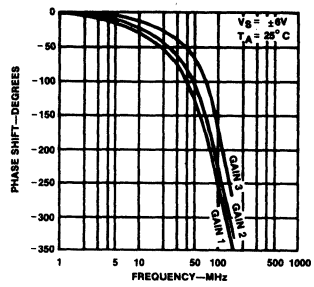
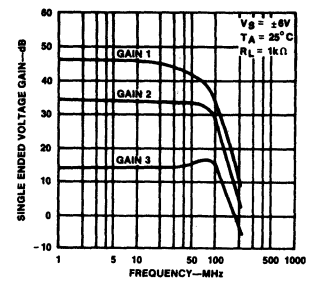
Phase Shift as a Function of Frequency



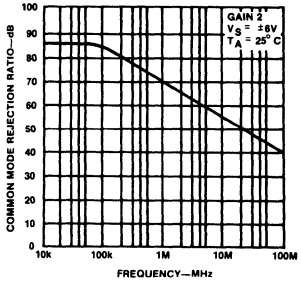
OP05630S

Voltage Gain as a Function of Frequency



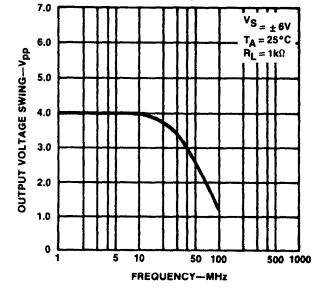
OP05640S

Common Mode Rejection Ratio as a Function of Frequency



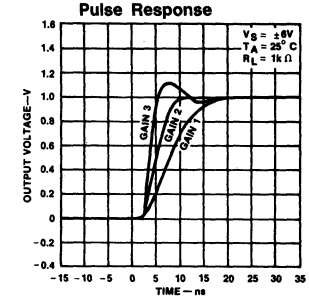
OP05650S

Output Voltage Swing as a Function of Frequency



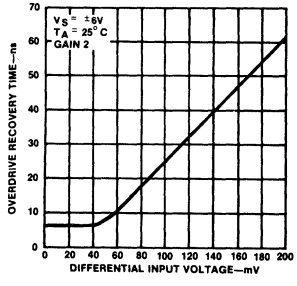
OP05660S

Pulse Response



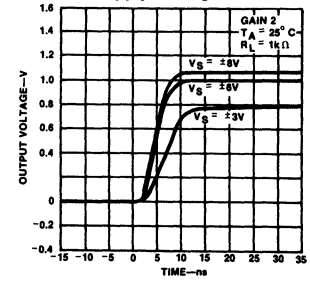
OP05670S

Differential Overdrive Recovery Time



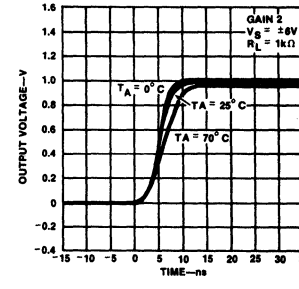
OP05680S

Pulse Response as a Function of Supply Voltage



OP05690S

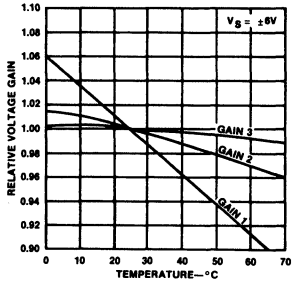
Pulse Response as a Function Of Temperature



OP05700S

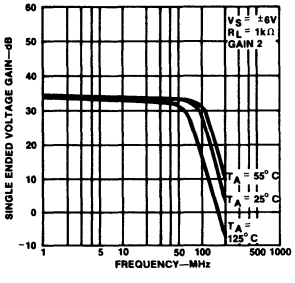
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Voltage Gain as a Function of Temperature



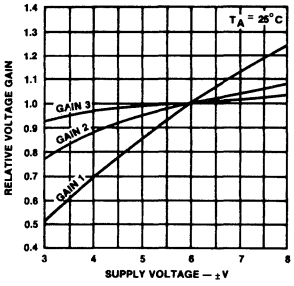
OP05710S

Gain vs Frequency of Temperature



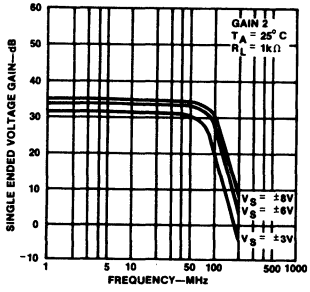
OP05720S

Gain vs Frequency as a Function of Temperature



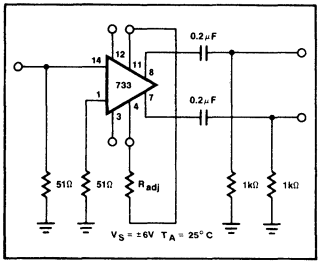
OP05730S

Gain vs Frequency as a Function of Supply Voltage



OP05740S

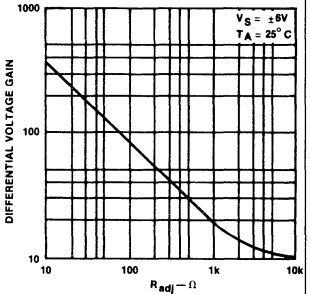
Voltage Gain Adjust Circuit



(Pin numbers apply to K Package)

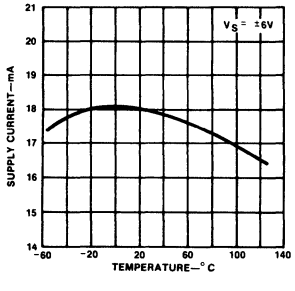
OP05750S

Voltage Gain as a Function of RADJ (Figure 3)



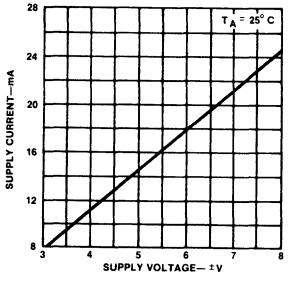
OP05760S

Supply Current as a Function of Temperature



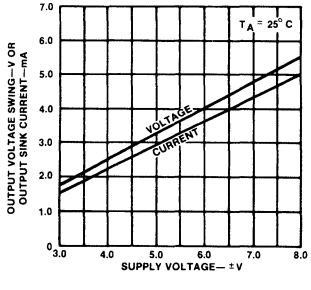
OP05770S

Supply Current as a Function of Supply Voltage



OP05780S

Output Voltage and Current Swing as a Function of Supply Voltage



OP05790S

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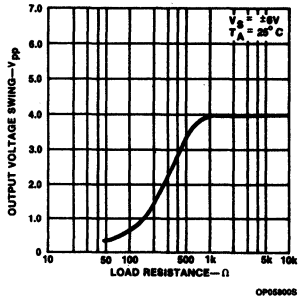
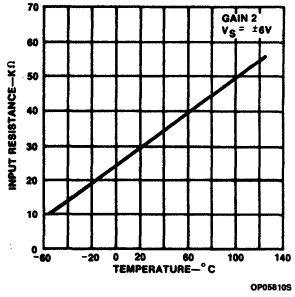
Differential Video Amplifier | μA733/733C

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

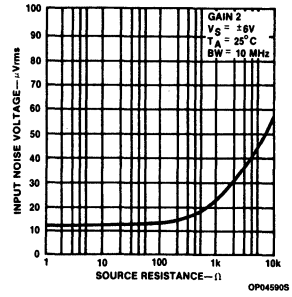
Output Voltage Swing as a Function of Load Resistance



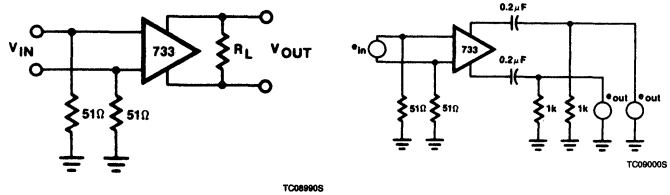
Input Resistance as a Function of Temperature



Input Noise Voltage as a Function of Source Resistance



TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.



SAA9001
317k Bit CCD Memory

Product Specification

Linear Products

DESCRIPTION

The SAA9001 is a 1-bit wide, 317,520-bit long, charge-coupled shift register, organized in 294 blocks of 1080 bits each. It is intended for use in a TV field memory at a maximum frequency of 21.3MHz.

Control is performed by two external signals, memory clock (MC), and memory gating (MG). The circuit has two data inputs (MI_1 and MI_2) and the data may be internally recirculated. An adjustable delay of 0 to 7 bits is incorporated at the output to increment the total delay on a bit-by-bit basis, as programmed by the inputs A0, A1, and A2. All inputs, outputs, and controls are TTL-compatible.

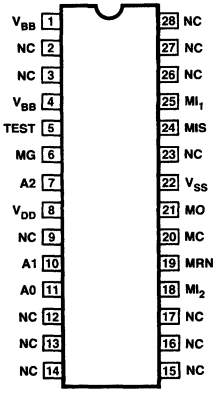
FEATURES

- **317k bits (294 × 1080)**
- **21.3MHz toggle frequency**
- **TTL-compatible**
- **28-pin DIP package**

APPLICATIONS

- **TV field memory**
- **Digitizing images**

PIN CONFIGURATION



TOP VIEW

CD12780S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{BB}	Back-bias supply voltage (to be connected to Pin 4)
4	V_{BB}	Back-bias supply voltage (to be connected to Pin 1)
5	TEST	Control input for testing purposes only. It is internally connected to V_{SS} via a 1kΩ (approx.) resistor and needs no external connection
6	MG	Memory gating input
7	A2	Control input for additional internal delay
8	V_{DD}	Positive supply voltage
10	A1	Control input for additional internal delay
11	A0	Control input for additional internal delay
18	MI_2	Memory input 2
19	MRN	Memory recirculate control. Recirculation is activated when MRN is Low
20	MC	Memory clock input
21	MO	Memory output
22	V_{SS}	Negative supply voltage (ground)
24	MIS	Memory input select; selects MI_1 or MI_2
25	MI_1	Memory input 1

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	0 to +60°C	SAA9001N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage on any pin, except V_{BB} (Pin 4) and MO (Pin 21), with respect to V_{SS}	7	V
V_{BB}	Back-bias voltage	min. −7	V
I_O	DC output current (sink or source)	10	mA
T_A	Operating ambient temperature range (under DC operating conditions)	0 to 60	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{TOT}	Total power dissipation per package	1	W

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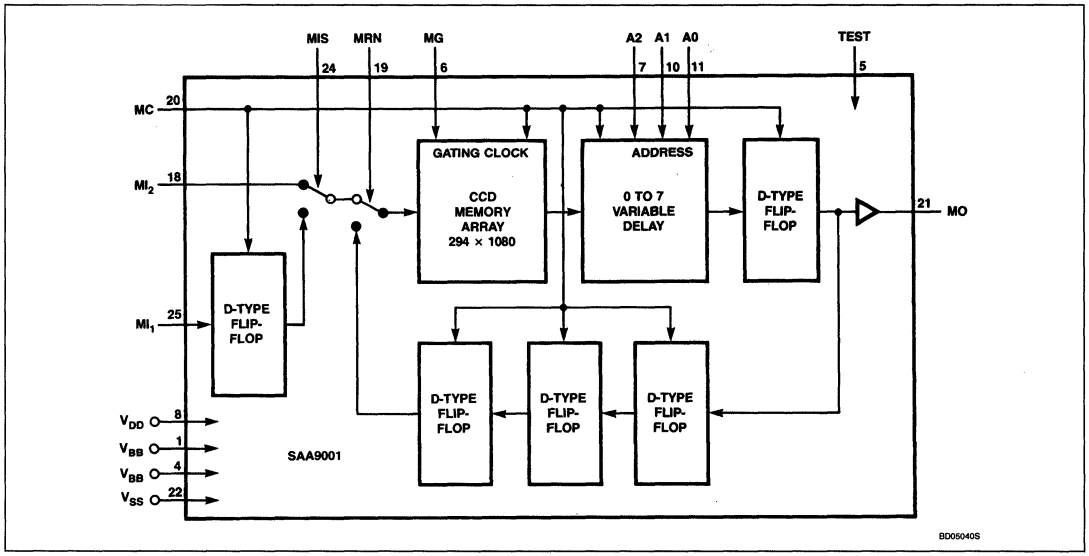
BLOCK DIAGRAM



CAPACITANCE

SYMBOL	PARAMETER	MAX	UNIT
C_I	Data inputs MI_1, MI_2 (Pins 25 and 18)	9	pF
C_C	Clock input MC (Pin 20)	9	pF
C_G	Gating input MG (Pin 6)	9	pF
C_O	Data output MO (Pin 21)	9	pF
C_{RN}	Recirculation control MRN (Pin 19)	9	pF
C_{IS}	Input select control MIS (Pin 24)	9	pF
C_A	Delay program inputs A0, A1, A2 (Pins 11, 10, and 7)	9	pF

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Supply voltage range	4.75		5.25	V
V_{BB}	Back-bias supply range	−3.65		−3.35	V
V_{IL}	Input voltage Low	−1.0		+0.8	V
V_{IH}	Input voltage High	2.0		6.0	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0$ to $+60°C$; $V_{DD} = 4.75$ to $5.25V$; $V_{BB} = -3.5 \pm 0.15V$; output not loaded, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
I_{LI}	Input leakage current at V_I = GND to V_{DD}: MI_1; MI_2; MC; MG; A0; A1; A2; MRN; MIS			10	μA
I_{DD}	Power supply current from V_{DD} at f = 21.3MHz			70	mA
V_{OL}	Output voltage Low at $I_{OL} = 4mA$			0.4	V
V_{OH}	Output voltage High at $I_{OH} = -1mA$	2.4			V

AC TEST CONDITIONS

PARAMETER	LIMIT	UNIT
Input pulse levels	0.6 and 2.4	V
Rise and fall times between 0.8 and 2.0V (t_R, t_F) clock input MC data inputs MI_1, MI_2; gating input MG; control inputs A0, A1, A2, MIS, MRN	 ⩽3 ⩾3	 ns ns
Timing reference levels clock input MC data inputs MI_1, MI_2; gating input MG data output MO	 1.5 0.8 or 2.0 0.8 or 2.0	 V V V
Output load	see Figure 4	

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AC ELECTRICAL CHARACTERISTICS $T_A = 0$ to $+60°C$; $V_{DD} = 4.75$ to $5.25V$; $V_{BB} = -3.5 \pm 0.15V$.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{CL}	Clock frequency[1]			21.3	MHz
t_{CL}	Clock Low time	18			ns
t_{CH}	Clock High time	18			ns
t_R	Recirculation time[1]			27	ms
t_{GW}	Waiting time (gating Low/High time)[2]			1100	µs
t_{GC}	Gating setup time	7.5			ns
t_{CG}	Gating hold time	0.5			ns
t_{IC}	Data setup time	7.5			ns
t_{CI}	Data hold time	0.5			ns
t_{OH}	Output hold time	5.0			ns
t_{OD}	Output delay time			23.5	ns
t_{AH}	Output invalid after address change	0			µs
t_{AD}	Address valid after address change[3]			7 clock pulses + 1	µs
t_{MRNSU}	Recirculation setup time[4]	0		1	µs
t_{MISSU}	Input select setup time[5]	0		1 clock pulse + 1	µs

NOTES:

1. The maximum recirculation time must never be exceeded by any combination of low frequency gating and/or waiting time.
2. Every 1300µs, at least three blocks of 1080 bits must be transferred to the output. This means that immediately after a wait of 1100µs, three blocks must be shifted out.
3. A change in delay will cause invalid data at the output for the time t_{AD}.
4. After a change of MRN, the signal recirculation path is not switched before t_{MRNSU}.
5. After a change of MIS, data at the input is invalid for t_{MISSU}.

FUNCTIONAL DESCRIPTION

Operation

The memory array is organized to handle data in blocks of 1080 bits and has a capacity of 294 data blocks. The structure of the memory array provides fast, serial data input and output, with parallel transfer of data blocks through the memory. Memory input and output are controlled by the memory gating (MG); the serial output is initiated by the rising edge of MG, and the storage of the data present in the memory's input register is performed on the falling edge of MG. In normal operation, one cycle of MG is an uninterrupted High level of at least 1080 clock periods (−4 or +3 clock periods) followed by a Low level of at least 32 clock periods. Input, output, and gating signals are all referred to the rising edge of the memory clock (MC).

The internal recirculation facility is activated when the control input MRN is Low.

Memory output

Output is enabled when MG is High and data is clocked serially from the memory. Referring to Figure 1, the first rising clock edge after the positive transition of MG is defined as clock pulse "0". If the delay control address is A2 = A1 = A0 = 0, then the first bit of the output is valid at clock pulse "17" (the delay of 17 clock periods is due to internal multiplexing of the data in the memory).

The output delay can be increased by the values shown in Table 1 using the internal delay line controlled by A0, A1, and A2.

Table 1. Additional Delay Control

DELAY ADDRESS			ADDITIONAL DELAY (CLOCK PERIODS)
A2	A1	A0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Data input

Data to be stored is directed to the memory from either MI_1 or MI_2 as selected by the control input MIS (see Table 2). The MI_1 input is delayed by one clock period.

Table 2. Input Selection

CONTROL INPUT	MEMORY INPUT
MIS = 0	MI_1
MIS = 1	MI_2

Input data is clocked serially into the input register of the CCD memory. When the negative transition of MG occurs, the 1080 bits of data present in the input register are entered into the memory array. If the interval of MG = High is not an exact multiple of eight clock periods, the timing of the negative transition of MG is internally rounded to be an exact multiple of eight clock periods. Note that the data path from input MI_1 has a delay of one clock period and the path from MI_2 is direct.

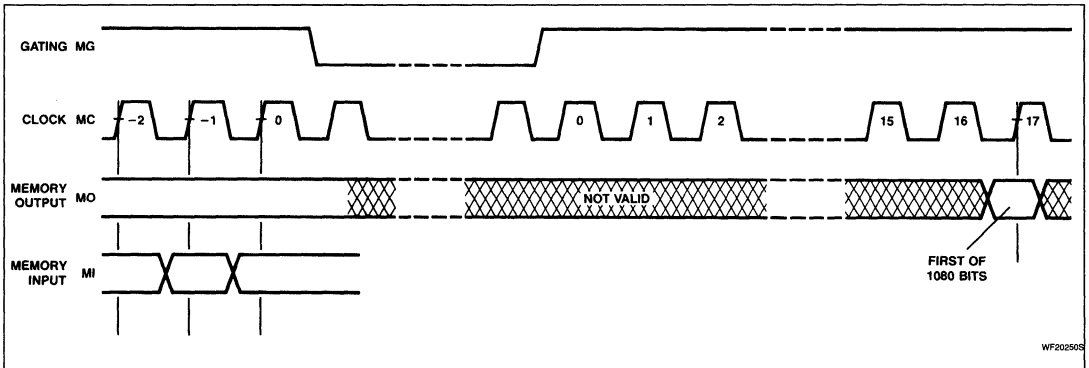

Figure 1. Memory Input and Output Data Timings With Respect to the Memory Clock (MC) for a Memory Gating (MG) High Period that is a Multiple of 8 Clock Periods (no Internal Rounding of Gating Period)

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The length of the MG = High interval required for internal and external recirculation of data is determined as shown in Figure 2. The positive transition of MG (waveform 1) initiates the serial transfer of data from the output register. Due to multiplexing in the memory, valid data is available after 16 clock periods (waveform 2). After a delay of "A" clock periods, determined by A0, A1, and A2 (waveform 3), and a one-clock period delay via a D-type flip-flop, the valid data is available at the output pin MO (waveform 4).

Incoming data can be delayed by two amounts: RP (waveform 5), a phase shift introduced when the data is recirculated through an external processing circuit, and ID (waveform 6), a one-clock period delay when input MI_1 is selected. The negative transition of MG, internally rounded to a multiple of eight clock periods (waveform 7), initiates storage of the last 1080 bits presented at the memory input (waveform 6). Therefore, the MG = High interval is 16 + A + 1 + RP + ID + 1080 clock periods, and this figure is rounded to a multiple of eight. From this, (A + 1 + RP + ID) modulo 8 = 0.

During internal recirculation of the data (MRN = Low), the three D-type flip-flops in the recirculation path give RP a value of three clock periods and ID will be zero. Consequently, the variable delay should be programmed for a delay of A = 4 for proper data retention, i.e., (4 + 1 + 3 + 0) modulo 8 = 0.

In conclusion, to store 1080 bits of valid data and to retrieve at the output 1080 valid data bits, the MG = High interval must be at least 1076 clock periods followed by an MG = Low interval of at least 32 clock periods. The MG = Low interval can be reduced to a minimum of 24 clock periods when MG = High is a multiple of eight clock periods.

Fast Gating

Fast gating is a method of accelerating the internal transfer of data through the memory at the expense of valid data, and is therefore useful for skipping unwanted data blocks. The MG = High interval for fast gating is less than 1076 clock periods to a minimum of 360 clock periods. If the MG = High interval is a multiple of eight clock periods during fast gating, the MG = Low interval can be reduced to 24 clock periods (min.); otherwise, the MG = Low interval must be at least 32 clock periods. The output data is not valid during fast gating and during the first two data blocks at the output after fast gating has ceased. No valid data is clocked into the input register of the CCD memory during fast gating.

Slow Gating

The transfer of data can be decelerated by using slow gating. For this, the MG = High or MG = Low interval is extended to the maximum waiting time (t_{GW}).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

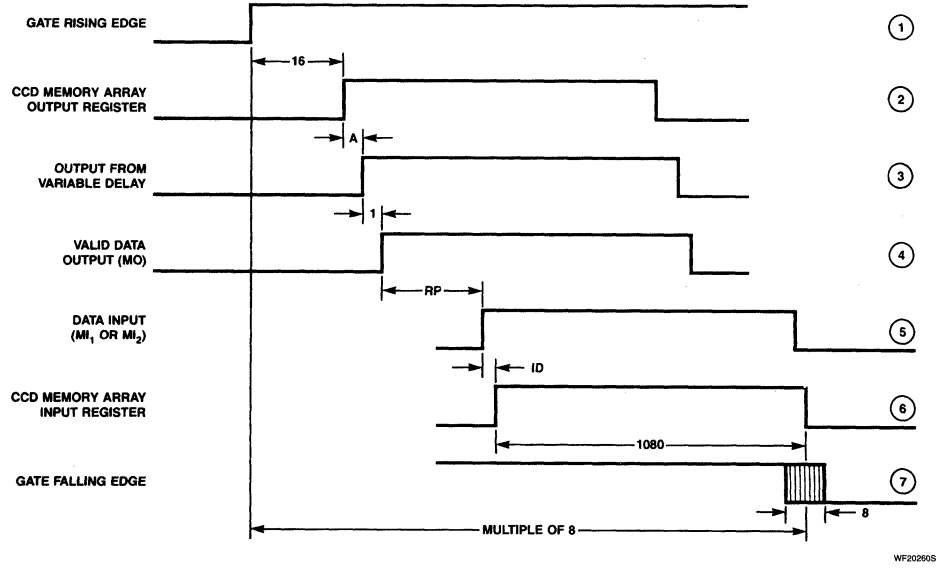

Figure 2. Determination of Memory Gating High Period

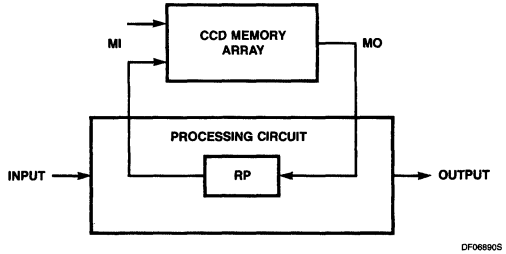

Figure 3. Recirculation via an External Circuit

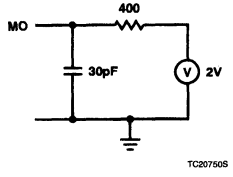

Figure 4. Output Load

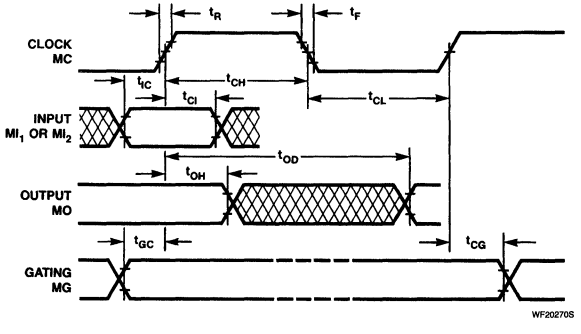

Figure 5. Timing Waveforms for Gating and I/O

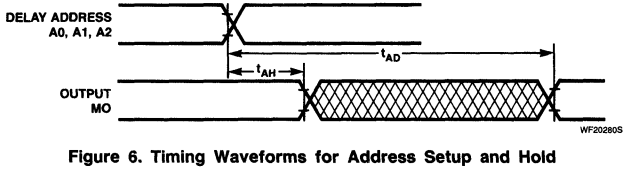

Figure 6. Timing Waveforms for Address Setup and Hold

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Signetics

Linear Products

Section 12
Vertical Deflection

INDEX

Signetics

TDA2653A
Vertical Deflection

Product Specification

Linear Products

DESCRIPTION

The TDA2653A is a monolithic integrated circuit for vertical deflection in video monitors and large screen color television receivers, e.g. 30AX and PIL-S4 systems.

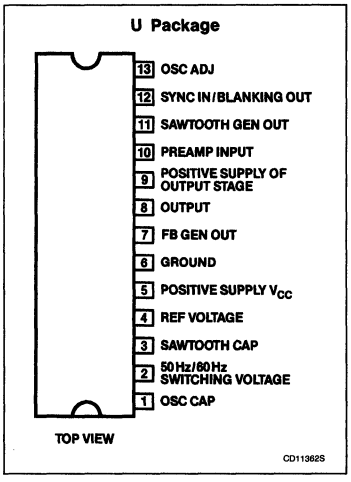
FEATURES

- **Oscillator; switch capability for 50Hz/60Hz operation**
- **Synchronization circuit**
- **Blanking pulse generator with guard circuit**
- **Sawtooth generator with buffer stage**
- **Preamplifier with fed-out inputs**
- **Output stage with thermal and short-circuit protection**
- **Flyback generator**
- **Voltage stabilizer**

APPLICATIONS

- **Video monitor**
- **Television receiver**

PIN CONFIGURATION

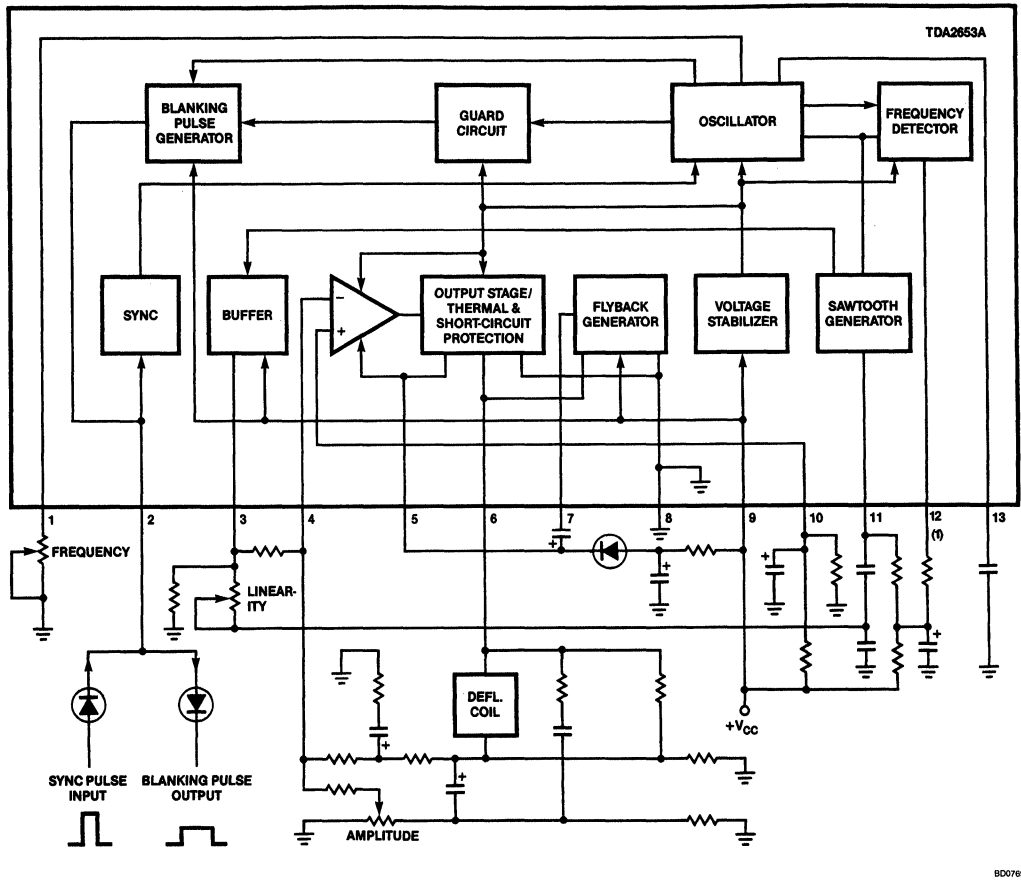


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
13-Pin Plastic SIP power package (SOT-141B)	−20°C to +85°C	TDA2653AU

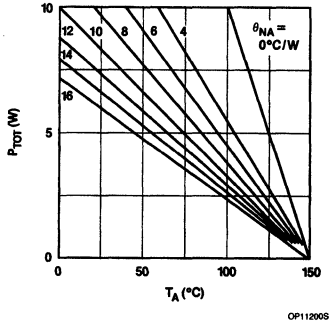
12

BLOCK DIAGRAM



NOTE:
1. Condition for Pin 12: LOW voltage level = 50Hz; HIGH voltage level = 60Hz.

PIN NO.	DESCRIPTION
1, 13	Oscillator The oscillator frequency is determined by a potentiometer at Pin 1 and a capacitor at Pin 13.
2	Sync input/blanking output Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1V and 12V. The integrated frequency detector delivers a switching level at Pin 12. The blanking pulse amplitude is 20V with a load of 1mA.
3	Sawtooth generator output The sawtooth signal is fed via a buffer stage to Pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to Pin 11 (linearity) and via a resistor to Pin 4 (preamplifier).
4	Preamplifier input The DC voltage is proportional to the output voltage (DC feedback). The AC voltage is proportional to the sum of the buffered sawtooth voltage at Pin 3 and the voltage, with opposite polarity, at the feedback resistor (AC feedback).
5	Positive supply of output stage This supply is obtained from the flyback generator. An electrolytic capacitor between Pins 7 and 5, and a diode between Pins 5 and 9 have to be connected for proper operation of the flyback generator.
6	Output of class-B power stage The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.
7	Flyback generator output An electrolytic capacitor has to be connected between Pins 7 and 5 to complete the flyback generator.
8	Negative supply (ground) Negative supply of output stage and small signal part.
9	Positive supply The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.
10	Reference voltage of preamplifier External adjustment and decoupling of reference voltage of the preamplifier.
11	Sawtooth capacitor This sawtooth capacitor has been split to realize linearity control.
12	50Hz/60Hz switching level This pin delivers a LOW voltage level for 50Hz and a HIGH voltage level for 60Hz. The amplitudes of the sawtooth signals can be made equal for 50Hz and 60Hz with these levels.



NOTE:
θ_{HA} includes θ_{MBH} which is expected when heatsink compound is used. $\theta_{JMB} \leq 5°C/W$.

Figure 1. Total Power Dissipation

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_9 = V_{CC}$	Supply voltage (Pin 9)	40	V
V_5	Supply voltage output stage (Pin 5)	58	V
Voltages			
V_3	Pin 3	7	V
V_{13}	Pin 13	7	V
$V_{4;\ 10}$	Pins 4 and 10	24	V
V_6	Pin 6	58	V
$-V_6$		0	V
$V_{7;\ 11}$	Pins 7 and 11	40	V
Currents			
I_1	Pin 1	0	mA
$-I_1$		1	mA
$\pm I_2$	Pin 2	10	mA
IP_3	Pin 3	0	mA
$-I_3$		5	mA
I_7	Pin 7	1.2	A
$-I_7$		1.5	A
I_{11}	Pin 11	50	mA
$-I_{11}$		1	mA
I_{12}	Pin 12	3	mA
$-I_{12}$		0	mA
T_{STG}	Storage temperature range	−25 to +150	°C
T_A	Operating ambient temperature range	−20 to limiting value	°C

NOTES:
1. Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.
2. Total power dissipation: internally limited by the thermal protection circuit.

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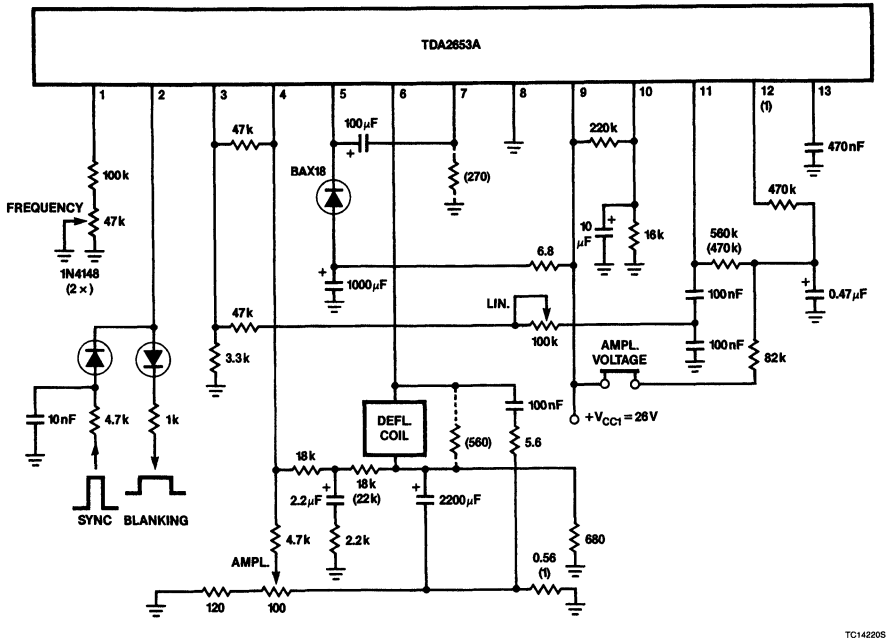
DC ELECTRICAL CHARACTERISTICS T^A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$V_9 = V_{CC}$	Supply voltage	9		30	
	Output voltage				
V_6	at $-I_6 = 1.1A$	$V_5-2.2$	$V_5-1.9$		V
V_6	at $I_6 = 1.1A$		1.3	1.6	V
V_7	Flyback generator output voltage at $-I_6 = 1.1A$		$V_{CC}-2.2$		V
$\pm I_6$	Peak output current			1.2	A
$\pm I_7$	Flyback generator peak current			1.2	A
Feedback					
$-I_{4, 10}$	Input quiescent current		0.1		μA
Synchronization					
V_2	Sync input pulse	1		12	V
	Tracking range		28		%
Oscillator/sawtooth generator					
V_1	Oscillator frequency control input voltage	6		9	V
V_3	Sawtooth generator output voltage	0		V_{CC-1}	V
V_{11}		0		V_{CC-2}	V
$-I_3$		0		4	mA
	Sawtooth generator output current	−2			μA
I_{11}				+30	mA
$(\Delta f/f)/\Delta T_{CASE}$	Oscillator temperature dependency T_{CASE} = 20 to 100°C		10^4		°C
$(\Delta f/f)/\Delta V_S$	Oscillator voltage dependency V_S = 10 to 30V		4×10^4		V^{-1}
Blanking pulse generator					
V_2	Output voltage at $V_S = 24V$; $I_2 = 1mA$		18.5		V
$-I_2$	Output current			3	mA
R_2	Output resistance		410		Ω
t_B	Blanking pulse duration at 50Hz sync		1.4 ± 0.07		ms
50Hz/60Hz switch capability					
V_{12}	Saturation voltage; LOW voltage level		1		V
I_{12}	Output leakage current		1		μA



NOTES:
1. Condition for Pin 12: LOW voltage level = 50Hz; HIGH voltage level = 60Hz.
2. The values given in parentheses and the dotted components are valid for the PIL-S4 system.

Figure 2. Typical Vertical Deflection Circuit for 30AX System (26V)

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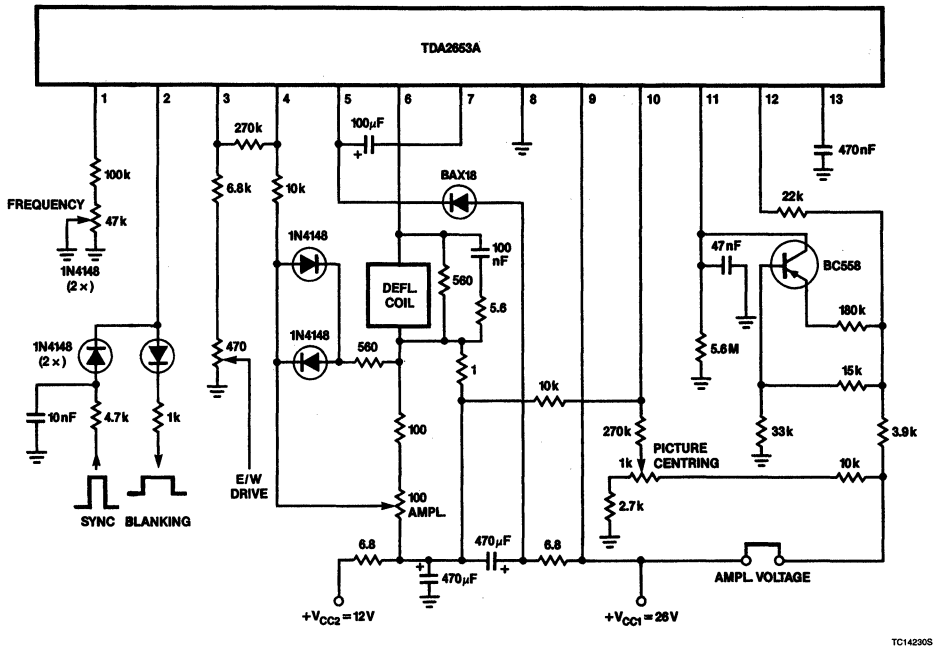


NOTES:
1. Condition for Pin 12: LOW voltage level = 50Hz; HIGH voltage level = 60Hz.
2. V_{CC1} = 26V, V_{CC2} = 12V in Quasi-bridge Connection.

Figure 3. Typical Vertical Deflection Circuit for 30AX System

Data Measured in Figures 2 and 3

SYMBOL	PARAMETER		30AX SYSTEM (26V) (Figure 2)	30AX SYSTEM (26 V/12V) (Figure 3)	PIL-S4 SYSTEM (Figure 2)
V_{S1} V_{S2}	System supply voltages	typ typ	26	26 12	26V −V
I_{S1} I_{S2}	System supply currents	typ typ	315	330 −35	195mA −mA
V_{6-8}	Output voltage	typ	14	14.6	13.5V
V_{6-8}	Output voltage (peak value)	typ	42	42	49V
$I_{6(P-P)}$	Deflection current (peak-to-peak value)	typ	2.2	2.2	1.32A
t_{FL}	Flyback time	typ	1	0.9	1.1ms
P_{TOT}	Total power dissipation per package	typ max	4.1 4.8	4 4.8	3W 3.4W[1]
f	Oscillator frequency unsynchronized	typ	46.5	46.5	46.5Hz

NOTE:
1. Calculated with $\Delta V_S = +5\%$ and $\Delta R_{YOKE} = -7\%$.

TDA3651A/3653
Vertical Deflection

Product Specification

Linear Products

DESCRIPTION

The TDA3651A is a vertical deflection output circuit for drive of various deflection systems with deflector currents up to 2A peak-to-peak.

FEATURES

- **Driver**
- **Output stage**
- **Thermal protection and output stage protection**
- **Flyback generator**
- **Voltage stabilizer**

APPLICATIONS

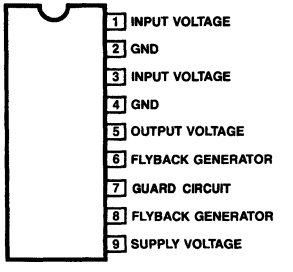
- **Video terminals**
- **Television**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131B)	0 to +70°C	TDA3651A
9-Pin Plastic SIP (SOT-157B)	0 to +70°C	TDA3651AQ
9-Pin Plastic SIP (SOT-110B)	0 to +70°C	TDA3653A

PIN CONFIGURATIONS

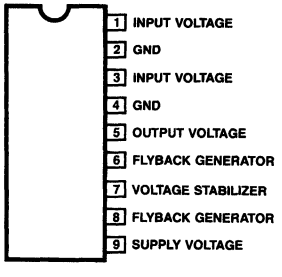
TDA3653
A Package



TOP VIEW

CD10341S

TDA3651
A Package

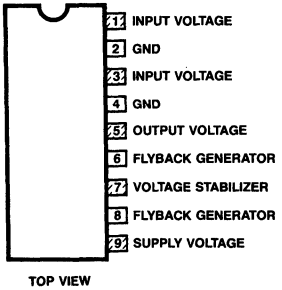


TOP VIEW

CD10350S

TDA3651
AQ Package

(SIL BENT)



TOP VIEW

▨ = BENT LEADS

CD10290S

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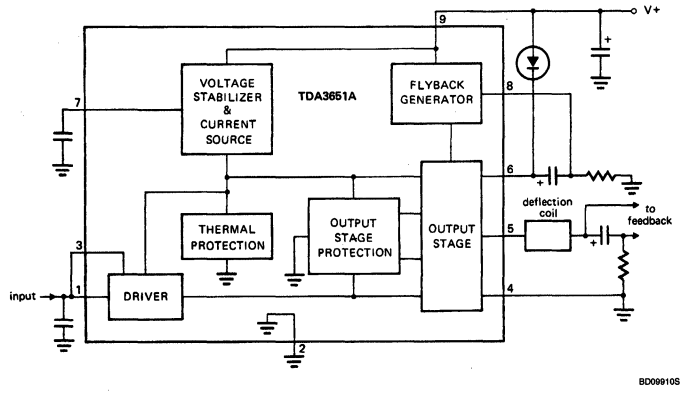
BLOCK DIAGRAM TDA3651A/AQ



FUNCTIONAL DESCRIPTION

Output Stage and Protection Circuit

Pin 5 is the output pin. The supply for the output stage is fed to Pin 6 and the output stage ground is connected to Pin 4. The output transistors of the Class-B output stage can each deliver 1A maximum. The 'upper' power transistor is protected against short-circuit currents to ground, whereas during flyback, the 'lower' power transistor is protected against too high voltages which may occur during adjustments.

Moreover, the output transistors have been given extra solidity by means of special measures in the internal circuit layout.

A thermal protection circuit is incorporated to protect the IC against too high dissipation. This circuit is 'active' at 175°C and then reduces the deflection current to such a value that the dissipation cannot increase.

Driver and Switching Circuit

Pin 1 is the input for the driver of the output stage. The signal at Pin 1 is also applied to Pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator. Pin 3 is connected externally to Pin 1, in order to allow for different applications in which Pin 3 is driven separate from Pin 1.

Flyback Generator

The capacitor at Pin 6 is charged to a maximum voltage, which is equal to the supply voltage V_{CC} (Pin 9), during scan.

When the flyback starts and the voltage at the output pin (Pin 5) exceeds the supply voltage (Pin 9), the flyback generator is activated. The V_{CC} is connected in series (via Pin 8) with the voltage across the capacitor.

The voltage at the supply pin (Pin 6) of the output stage will then be maximum twice V_{CC}. Lower voltages can be chosen by changing the value of the external resistor at Pin 8.

Voltage Stabilizer

The internal voltage stabilizer provides a stabilized supply of 6V for drive of the output stage, so the drive current of the output stage is not affected by supply voltage variations. The stabilized voltage is available at Pin 7.

A decoupling capacitor of 2.2μF can be connected to this pin.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		3651	3653	
Voltage (Pins 4 and 2 externally connected to ground)				
V_{5-4}	Output voltage (Pin 5)	55	60	V
$V_{9-4} = V_{CC}$	Supply voltage (Pin 9)	50	40	V
V_{6-4}	Supply voltage output stage (Pin 6)	55	60	V
V_{1-2}; V_{3-2}	Input voltage (Pins 1 and 3)	V_{CC}	V_{CC}	
V_{7-2}	External voltage (Pin 7)		5.6	V
Currents				
$\pm I_{5RM}$	Repetitive peak output current (Pin 5)	0.75	0.75	A
$\pm I_{5SM}$	Non-repetitive peak output current (Pin 5)	1.5	1.5	A[1]
I_{8SM}	Repetitive peak flyback generator output current (Pin 8)	−0.75 +0.85	−0.75 ±0.85	A A
I_{8SM}	Non-repetitive peak flyback generator output current (Pin 8)	−1.5 +1.6	−1.5 +1.6	A A[1]
Temperatures				
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	−25 to +65	°C
T_J	Operating junction temperature range	−25 to +150	−25 to +150	°C

NOTE:
1. Non-repetitive duty factor maximum 3.3%.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = 26V$; Pins 4 and 2 externally connected to ground, unless otherwise specified.

SYMBOL	PARAMETER	3651			3653			UNIT
		Min	Typ	Max	Min	Typ	Max	
$I_{5(P-P)}$	Output current (peak-to-peak value)		1.2	1.5		1.2	1.5	A
$-I_8$	Flyback generator output current		0.7	0.85		0.7	0.85	A
I_8	Flyback generator output current		0.6	0.75		0.6	0.75	A
Output voltages								
V_{5-4M}	Peak voltage during flyback			55			60	V
$-V_{5-6sat}$	Saturation voltage to supply at $-I_5$ = 1A (3651); 0.6A (3653)		2.5	3.0		2.3	2.8	V
V_{5-4sat}	Saturation voltage to ground at $-I_5$ = 1A (3651); 0.6A (3653)		2.5	3.0		1.7	2.2	V
$-V_{5-6sat}$	Saturation voltage to supply at $-I_5 = 0.75A$		2.2	2.7		2.5	3.0	V
V_{5-4sat}	Saturation voltage to ground at $I_5 = 0.75A$		2.2	2.7		2.0	2.5	V
Supply								
V_{9-2}	Supply voltage	10		50	10		40	V
V_{6-4}	Supply voltage output stage			55			60	V
I_9	Supply current (no load and no quiescent current)		9			10		mA
				12			20	
I_4	Quiescent Current (see Figure 1)		38			25		mA
		25		52	6		40	
	Variation of quiescent current with temperature		−0.04			−0.04		mA

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DC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; $V_{CC} = 26V$; Pins 4 and 2 externally connected to ground, unless otherwise specified.

SYMBOL	PARAMETER	3651			3653			UNIT
		Min	Typ	Max	Min	Typ	Max	
Flyback generator								
V_{9-8sat}	Saturation voltage at $-I_8 = 1.1A$ (3651); 0.85A (3653)		1.6	2.1		1.6	2.1	V
V_{8-9sat}	Saturation voltage at $I_8 = 1A$ (3651); 0.75A (3653)		2.5	3.0		2.3	2.8	V
V_{9-8sat}	Saturation voltage at $I_8 = 0.85A$ (3651); 0.7A (3653)		1.4	1.9		1.4	1.9	V
V_{8-9sat}	Saturation voltage at $I_8 = 0.75A$ (3651); 0.6A (3653)		2.3	2.8		2.2	2.7	V
V_{5-9}	Flyback generator active if	4			4			V
$-I_8$	Leakage current		250	100		5	100	μA
I_1	Input current for $\pm I_5 = 1A$ (3651); 1.5A (3653)	175	2.30	380			1300	μA
V_{1-2}	Input voltage during scan	0.9	1.9	2.7			3.2	V
I_3	Input current during scan	0.01		2.5	.01		.52	mA
V_{3-2}	Input voltage during scan	0.9		V_{CC}	0.9		V_{CC}	V
V_{3-2}	Input voltage during flyback	0		200			250	mV
V_{7-2}	Voltage at Pin 7	5.5	6.1	6.6	4.4	5.0	5.6	V
I_7	Load current of Pin 7			15				V
V_{7-2}	Unloaded voltage at Pin 7 during flyback		15					V
T_J	Junction temperature of switching on the thermal protection	158	175	192				°C
θ_{JMB}	Thermal resistance from junction to mounting base		3	4		10	12	°C/W
P_D	Power dissipation		see Figure 3					
G_O	Open-loop gain at 1kHz; $R_L = 1k\Omega$		36			42		dB
f_R	Frequency response (−3dB); $R = 1k\Omega$		60			40		kHz

NOTE:
1. The maximum supply voltage should be chosen such that during flyback the voltage at Pin 5 does not exceed 55V.

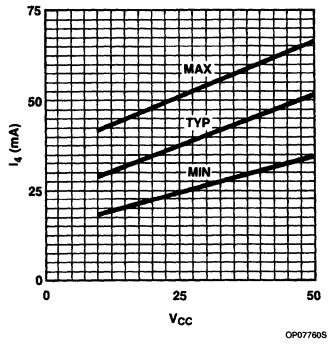

Figure 1. Quiescent Current I_4 as a Function of Supply Voltage V_{CC}

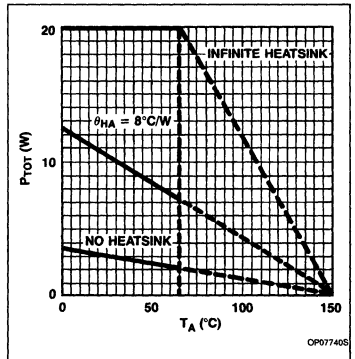

Figure 2. Power Derating Curves

APPLICATION INFORMATION The following application data are measured in a typical application as shown in Figures 3 and 4.

Deflection current (including 6% overscan) peak-to-peak value	$I_{5(P-P)}$ typ. 0.87A
Supply voltage	V_{9-4} typ. 26V
Total supply current	I_{TOT} typ. 148mA
Peak output voltage during flyback	$V_{5-4M} < 50V$
Saturation voltage to supply	typ. 2.0V $V_{5-6sat} < 2.5V$
Saturation voltage to ground	typ. 2.0V $V_{5-4sat} < 2.5V$
Flyback time	typ. 0.95ms $t_{fl} < 1.2ms$
Total power dissipation in IC	P_{TOT} typ. 2.5W
Operating ambient temperature	$T_A < 65°C$

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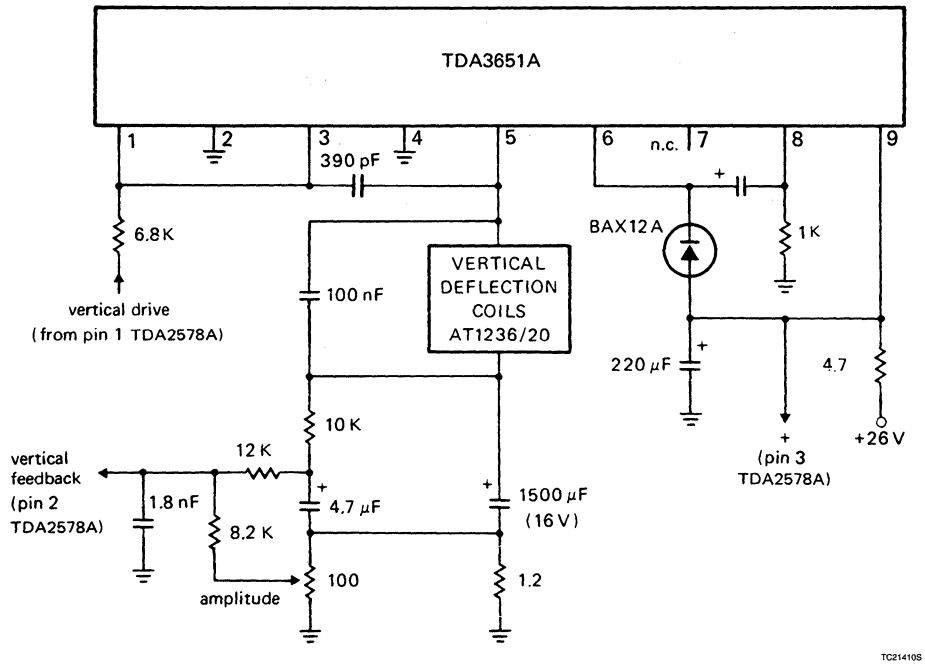
Vertical Deflection TDA3651A/3653



NOTE:
Deflection coils AT1236/20: L = 29mH, R = 13.6Ω; deflection current without overscan is 0.82 A_{P-P} and EHT voltage is 25kV.

Figure 3. Typical Application Circuit Diagram of the TDA3651A (Vertical Output), When Used in Combination With the TDA2578A (See Figure 5)

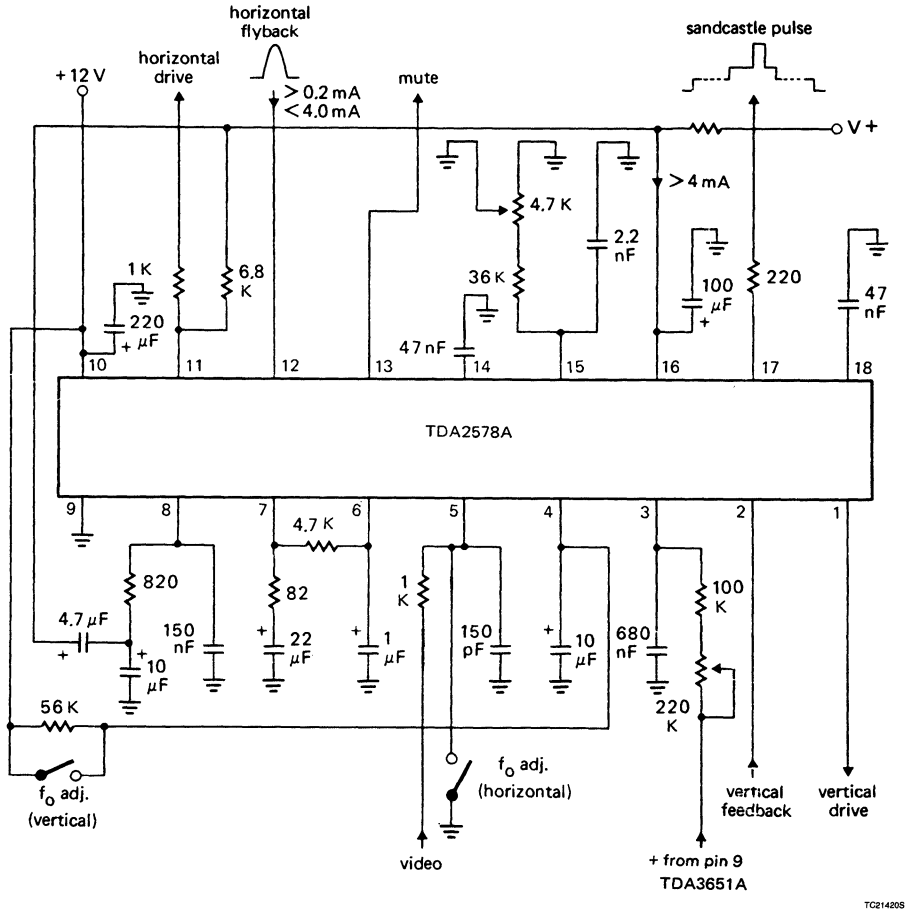


Figure 4. Typical Application Circuit Diagram; for Combination of the TDA2578A With the TDA3651A (See Figure 3)

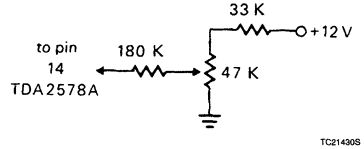
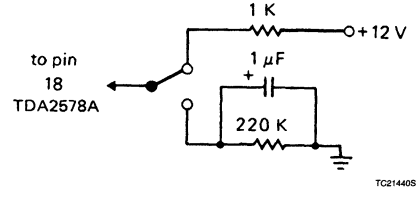


Figure 5. Circuit Configuration at Pin 14 for Phase Adjustment



NOTES:
1kΩ resistor between Pin 18 and +12V: without mute function.
220kΩ between Pin 18 and ground: with mute function.

Figure 6. Circuit Configuration at Pin 18 for VCR Mode

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Signetics

TDA3652
Vertical Deflection

Product Specification

Linear Products

DESCRIPTION

The TDA3652 is an integrated power output circuit for vertical deflection in systems with deflection currents up to $3A_{p-p}$.

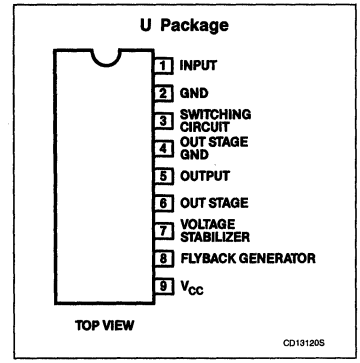
FEATURES

- **Driver**
- **Output stage and protection circuits**
- **Flyback generator**
- **Voltage stabilizer**

APPLICATIONS

- **Video monitors**
- **TV receivers**

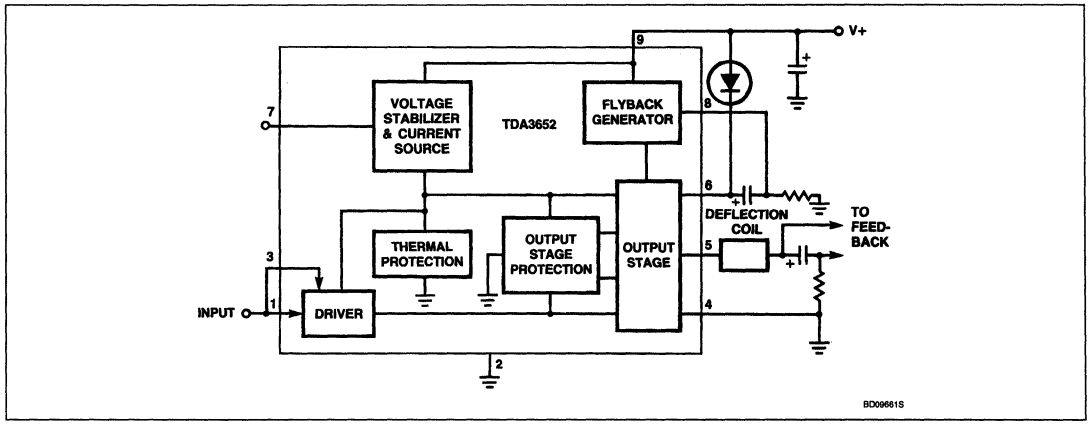
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131B)	−25°C to +65°C	TDA3652U
9-Pin Plastic SIP Bent to DIP (SOT-157B)	−25°C to +65°C	TDA3652QU

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
Voltages (Pins 4 and 2 externally connected to ground)			
V_{5-4}	Output voltage (Pin 5)	55	V
$V_{9-4} = V_{CC}$	Supply voltage (Pin 9)	40	V
V_{6-4}	Supply voltage output stage (Pin 6)	55	V
V_{1-2}	Driver input voltage (Pin 1)	V_{CC}	V[1]
V_{3-2}	Switching circuit input voltage (Pin 3)	5.6	V
Currents			
$\pm I_{5RM}$	Repetitive peak output current (Pin 5)	1.5	A
$\pm I_{5SM}$	Non-repetitive peak output current (Pin 5)	3	A[2]
I_{8RM}	Repetitive peak flyback generator output current (Pin 8)	−1.5 +1.6	A A
$\pm I_{8SM}$	Non-repetitive peak flyback generator output current (Pin 8)	3	A[2]
Temperatures			
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +65	°C
T_J	Operating junction temperature range	−25 to +150	°C

NOTES:
1. The maximum input voltage should not exceed the supply voltage (V_{CC} at Pin 9). In most applications Pin 1 is connected to Pin 3; the maximum input voltage should then not exceed 5.6V.
2. Non-repetitive duty factor maximum 3.3%.

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DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 26V; T_A = 25°C; Pins 4 and 2 externally connected to ground, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{CC}	Supply voltage (Pin 9)	10		40	V[1]
V_{6-4}	Supply voltage output stage (Pin 6)			55	V[1]
I_{CC}	Supply current (no load and no quiescent current) (Pin 9)		9	12	mA
I_4	Quiescent current (see Figure 1)	25	40	65	mA
ΔI_4	Variation of quiescent current with temperature		−0.04		mA/°C
Output current					
$I_{5(P-P)}$	Output current (Pin 5) (peak-to-peak value)		2.5	3.0	A
$-I_8$	Output current flyback generator (Pin 8)		1.35	1.6	A
I_8	Output current flyback generator (Pin 8)		1.25	1.5	A
Output voltage					
V_{5-4M}	Peak voltage during flyback			55	V
$-V_{5-6SAT}$	Saturation voltage to supply at $-I_5$ = 1.5A		2.5	3.0	V
V_{5-4SAT}	Saturation voltage to ground at I_5 = 1.5A		2.5	3.0	V
$-V_{5-6SAT}$	Saturation voltage to supply at $-I_5$ = 1A		2.2	2.7	V
V_{5-4SAT}	Saturation voltage to ground at I_5 = 1A		2.2	2.7	V
Flyback generator					
V_{9-8SAT}	Saturation voltage at $-I_8$ = 1.6A		1.6	2.1	V
V_{8-9SAT}	Saturation voltage at I_8 = 1.5A		2.5	3.0	V
V_{9-8SAT}	Saturation voltage at $-I_8$ = 1.1A		1.4	1.9	V
V_{8-9SAT}	Saturation voltage at I_8 = 1A		2.3	2.8	V
V_{5-9}	Flyback generator active	4			V
$-I_8$	Leakage current at Pin 8		5	100	μA
$I_{1(P-P)}$	Input current for I_5 = 4A at Pin 1 (peak-to-peak value)	190	240	400	μA
V_{1-2}	Input voltage during scan (Pin 1)	1.3	2.0	3.5	V
I_3	Input current during scan (Pin 3)	0.01		2.5	mA
V_{3-2}	Input voltage during scan (Pin 3)	0.9		5.6	V
V_{3-2}	Input voltage during flyback (Pin 3)	0		0.2	V
General data					
T_J	Junction temperature of switching on the thermal protection	158	175	192	°C
θ_{JMB}	Thermal resistance from junction to mounting base			4	°C/W
P_{TOT}	Total power dissipation	see Figure 2			
G_O	Open-loop gain at 1kHz		36		dB
f_R	Frequency response (−3dB) at R_L = 1kΩ		50		kHz

NOTE:
1. The maximum supply voltage should be chosen such that during flyback the voltage at Pin 5 does not exceed 55V.

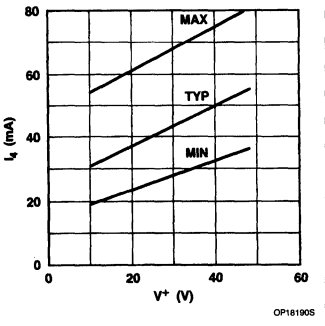

Figure 1. Quiescent Current (I_4 as a Function of Supply Voltage (V_{CC})

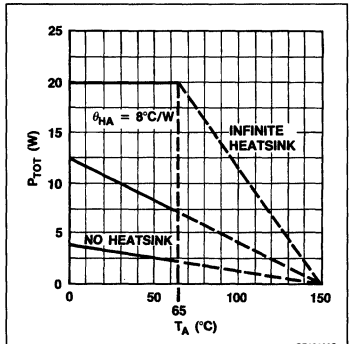

Figure 2. Power Derating Curve

APPLICATION INFORMATION

The function is described beside the corresponding pin number.

1 Driver — This is the input for the driver of the output stage.

2 Negative Supply (Ground)

3 Switching Circuit — This pin is normally connected externally to Pin 1. It is also possible to use this pin to drive the switching circuit for different applications. This switching circuit rapidly turns off the lower output stage at the end of scan and also allows for a quick start of the flyback generator.

4 Output Stage Ground

5, 6 Output Stage and Protection Circuits — Pin 5 is the output pin and Pin 6 is the output stage supply pin. The output stage is a class-B type with each transistor capable of delivering 1.5A maximum. The "upper" output transistor is protected against short-circuit currents to ground. The base of the "lower" power transistor is connected to ground during flyback and so it is protected against too high flyback pulses which may occur during adjustments. In addition, the output transistors are protected by a special layout of the internal circuit. The circuit is protected thermally against excessive dissipation by a circuit which operates at temperatures of 175°C and upwards, causing the output current to drop to a value such that the dissipation cannot increase.

7 Voltage Stabilizer — The internal voltage stabilizer provides a stabilized supply voltage of 6V for drive of the output stage, so the drive current is not influenced by the various voltages of different applications.

8, 9 Flyback Generator — Pin 8 is the output pin of the flyback generator. Depending on the value of the external resistor at Pin 8, the capacitor at Pin 6 will be charged to a fixed level during the scan period. The maximum height of the level is equal to the supply voltage at Pin 9 (V_{CC}). When the flyback starts and the flyback pulse at Pin 5 exceeds the supply voltage, the flyback generator is activated and then the supply voltage is connected in series (via Pin 8) with the voltage across the capacitor. The voltage at the supply pin (Pin 6) of the output stage will then be not more than twice the supply voltage.

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TDA3654
Vertical Deflection Output Circuit

Product Specification

Linear Products

DESCRIPTION

The TDA3654 is a full-performance vertical deflection output circuit in a 9-lead, single in-line encapsulation. The circuit is intended for direct drive of the deflection coils and it can be used for a wide range of 90° and 110° deflection systems.

The TDA3654 is provided with a guard circuit which blanks the picture tube screen in case of absence of the deflection current.

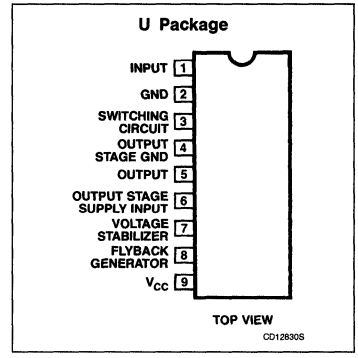
FEATURES

- **Direct drive to the deflection coils**
- **90° and 110° deflection system**
- **Internal blanking guard circuit**
- **Internal voltage stabilizer**

APPLICATIONS

- **Video monitors**
- **TV receivers**

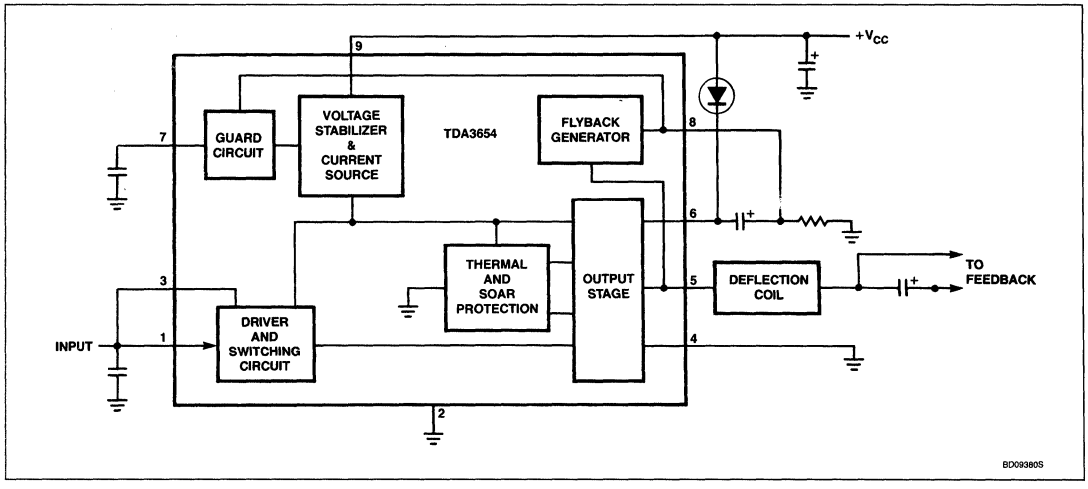
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP (SOT-131B)	−25°C to +60°C	TDA3654U
9-Pin Plastic SIP (SOT-157)	−25°C to +60°C	TDA3654AU

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
Voltages			
V_{5-4}	Output voltage	60	V
V_{9-4}	Supply voltage	40	V
V_{6-4}	Supply voltage output stage	60	V
V_{1-2}	Input voltage	V_{9-4}	V
V_{3-2}	Input voltage switching circuit	V_{9-4}	V
V_{7-2}	External voltage at Pin 7	5.6	V
Currents			
$\pm I_{5RM}$	Repetitive peak output current	1.5	A
$\pm I_{5SM}$	Non-repetitive peak output current[1]	3	A
I_{8RM}	Repetitive peak output current of flyback generator	+1.5 −1.6	A A
$\pm I_{8SM}$	Non-repetitive peak output current of flyback generator[1]	3	A
Temperatures			
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range (see Figure 2)	−25 to +60	°C
T_J	Operating junction temperature range	−25 to +150	°C
θ_{JMB}	Thermal resistance	4	°C/W

NOTE:
1. Pins 2 and 4 are externally connected to ground.

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DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, supply voltage (V_{9-4}) = 26V, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{9-4}	Supply voltage, Pin 9[2]	10		40	V
V_{6-4}	Supply voltage output stage			60	V
$I_6 + I_9$	Supply current, Pins 6 and 9[3]	35	55	85	mA
I_4	Quiescent current[4]	25	40	65	mA
TC	Variation of quiescent current with temperature		−0.04		mA/°C
Output current					
$I_{5(P-P)}$	Output current, Pin 5 (peak-to-peak)		2.5	3	A
$+I_{8(P-P)}$ $-I_{8(P-P)}$	Output current flyback generator, Pin 8		1.25 1.35	1.5 1.6	A A
Output voltage					
V_{5-4}	Peak voltage during flyback			60	V
	Saturation voltage to supply				
$V_{6-5(SAT)}$	at $I_5 = -1.5A$		2.5	3.2	V
$V_{5-6(SAT)}$	at $I_5 = 1.5A$[5]		2.5	3.2	V
$V_{6-5(SAT)}$	at $I_5 = -1.2A$		2.2	2.7	V
$V_{5-6(SAT)}$	at $I_5 = 1.2A$[5]		2.3	2.8	V
	Saturation voltage to ground				
$V_{5-4(SAT)}$	at $I_5 = 1.2A$		2.2	2.7	V
$V_{5-4(SAT)}$	at $I_5 = 1.5A$		2.5	3.2	V
Flyback generator					
	Saturation voltage				
$V_{9-8(SAT)}$	at $I_8 = -1.6A$		1.6	2.1	V
$V_{8-9(SAT)}$	at $I_8 = 1.5A$[5]		2.3	3	V
$V_{9-8(SAT)}$	at $I_8 = -1.3A$		1.4	1.9	V
$V_{8-9(SAT)}$	at $I_8 = 1.2A$[5]		2.2	2.7	V
$-I_8$	Leakage current at Pin 8		5	100	μA
V_{5-9}	Flyback generator active IF	4			V
Input					
I_1	Input current, Pin 1, for $I_5 = 1.5A$		0.33	0.55	mA
V_{1-2}	Input voltage during scan, Pin 1		2.35	3	V
I_3	Input current, Pin 3, during scan[6]	0.03			mA
V_{3-2}	Input voltage, Pin 3, during scan[6]	0.8		V_{9-4}	V
V_{1-2}	Input voltage, Pin 1, during flyback			250	mV
V_{3-2}	Input voltage, Pin 3, during flyback			250	mV
Guard circuit					
V_{7-2}	Output voltage, Pin 7, $R_L = 100k\Omega$[9]	4.1	4.5	5.5	V
V_{7-2}	Output voltage, Pin 7, at $I_L = 0.5mA$[9]	3.4	3.9	5.1	V
R_{I7}	Internal series resistance of Pin 7	0.95	1.35	1.7	kΩ
V_{8-2}	Guard circuit activates[7]			1.0	V
General data					
T_J	Thermal protection activation range	158	175	192	°C

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$, supply voltage (V_{9-4}) = 26V, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Thermal resistance					
θ_{JMB}	From junction to mounting base		3.5	4	°C/W
P_{TOT}	Power dissipation		see Figure 2		
G_O	Open-loop gain at 1kHz[8]		33		dB
f_R	Frequency response, −3dB[10]		60		kHz

NOTES:
1. Non-repetitive duty factor 3.3%.
2. The maximum supply voltage should be chosen so that during flyback the voltage at Pin 5 does not exceed 60V.
3. When V_{5-4} is 13V and no load at Pin 5.
4. See Figure 3.
5. Duty cycle, d = 5% or d = 0.05.
6. When Pin 3 is driven separately from Pin 1.
7. During normal operation the voltage V_{8-2} may not be lower than 1.5V.
8. $R_L = 8\Omega$; $I_L = 125mA_{RMS}$
9. If guard circuit is active.
10. With a 22pF capacitor between Pins 1 and 5.

FUNCTIONAL DESCRIPTION

Output Stage and Protection Circuits

The output stage consists of two Darlington configurations in class B arrangement. Each output transistor can deliver 1.5A maximum and the V_{CEO} is 60V. Protection of the output stage is such that the operation of the transistors remains well within the SOA area in all circumstances at the output pin (Pin 5). This is obtained by the cooperation of the thermal protection circuit, the current-voltage detector, and the short-circuit protection. Special measures in the internal circuit layout give the output transistors extra solidity; this is illustrated in Figure 4, where typical SOA curves of the lower output transistors are given. The same curves also apply for the upper output device. The supply for the output stage is fed to Pin 6 and the output stage ground is connected to Pin 4.

Driver and Switching Circuit

Pin 1 is the input for the driver of the output stage. The signal at Pin 1 is also applied to Pin 3 which is the input of a switching circuit (Pins 1 and 3 are externally connected). This switching circuit rapidly turns off the lower output stage when the flyback starts, and therefore, allows a quick start of the flyback generator. The maximum required input signal for the maximum output current peak-to-peak value of 3A is only 3V; the sum of the currents in Pins 1 and 3 is then maximum 1mA.

Flyback Generator

During scan, the capacitor between Pins 6 and 8 is charged to a level which is dependent on the value of the resistor at Pin 8 (see Block Diagram). When the flyback starts and the voltage at the output pin (Pin 5) exceeds the supply voltage, the flyback generator is activated.

The supply voltage is then connected in series, via Pin 8, with the voltage across the capacitor during the flyback period. This implies that during scan the supply voltage can be reduced to the required scan voltage plus saturation voltage of the output transistors.

The amplitude of the flyback voltage can be chosen by changing the value of the external resistor at Pin 8. It should be noted that the application is chosen such that the lowest voltage at Pin 8 is > 1.5V during normal operation.

Guard Circuit

When there is no deflection current, for any reason, the voltage at Pin 8 becomes less than 1V and the guard circuit will produce a DC voltage at Pin 7. This voltage can be used to blank the picture tube so that the screen will not burn in.

Voltage Stabilizer

The internal voltage stabilizer provides a stabilized supply of 6V to drive the output stage, so the drive current is not affected by supply voltage variations.

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Vertical Deflection Output Circuit TDA3654

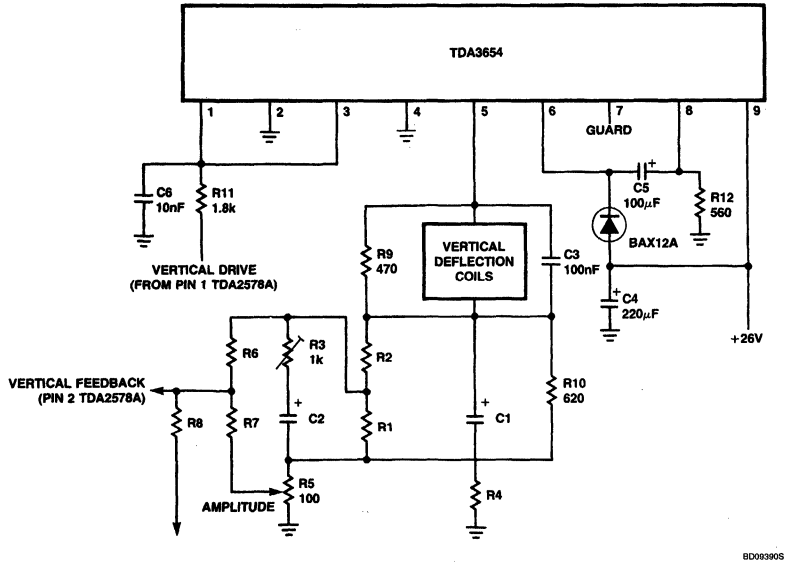


Figure 1. Application Diagram

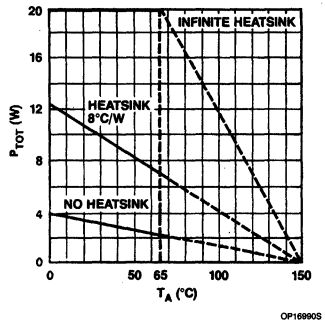


Figure 2. Power Derating Curve

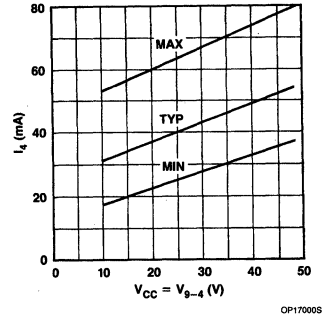
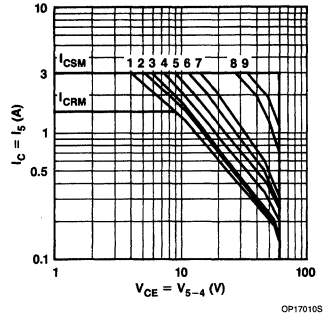


Figure 3. Quiescent Current as a Function of the Supply Voltage

CURVE	t_P	δ	PEAK JUNCTION TEMPERATURE
1	DC		150°C
2	10ms	0.5	150°C
3	10ms	0.25	150°C
4	1ms	0.5	150°C
5	1ms	0.25	150°C
6	1ms	0.05	150°C
7	1ms	0.05	180°C
8	0.2ms	0.1	150°C
9	0.2ms	0.1	180°C



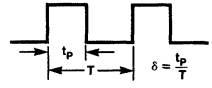


Figure 4. Typical SOA of Lower Output Transistor

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Signetics

Linear Products

Section 13
Videotex/Teletext

INDEX

AN153
The 5-Chip Set Teletext Decoder

Application Note

Author: D. S. Hobbs

SYSTEM REQUIREMENTS

The current 525-line (modified U.K.) Teletext system differs in a few respects from the 625-line system for which the U.K. chip set was designed. These are:

(a) Data Rate 5.727272Mb/s.

(b) Data bytes per data line 32.

(c) Gearing bit system for routing data to RAM.

(d) Approximately 200 display lines available for text with normal raster geometry.

These are catered for in the decoder described below so that the 625-line chip set is presented with signals which it can interpret correctly and provide a suitable display for general use.

Data Rate (a) and (b)

(a) To accomodate the lower data rate the clock coil and tuning capacitor in the SAA5020 video input processor circuit are redesigned.

(b) The write enable (WOK) signal from TAC (SAA5040) to the RAM is limited to 32 data bytes in GALA.

Gearing Bit System (c)

This is accomodated in the Gearing and Address Logic chip (GALA). Since 40 characters per row are displayed, whereas only 32 are transmitted per data line, a routing system is used to position character data in RAM as it is received.

The left hand part of the display is built up by 32 byte rows of data positioned in RAM by transmitted ROW addresses. The right hand side of the display is 'filled-in' by 4 sequential groups of 8 characters sent as one data line but stored in RAM as the last 8 bytes of 4 sequential rows. A gearing bit in the magazine number/row address group (see Table 1) is set to '1' if fill-in information is being transmitted and to '0' if left hand rows are sent. The ROW address of the data line containing the gearing bit set to '1' determines the starting ROW number for the fill-in operation. For ROW zero start, a ROW address for ROW number 1 is employed since ROW zero can only be used for header information. The presence of the gearing bit set = 1 together with ROW address number 1 is detected in GALA.

From Table 1 it will be seen that the gearing bit occupies the position occupied by the most significant bit of the magazine number in the 625 system. In order to allow the Teletext Acquisition Chip (TAC, SAA5040B) to acquire data from such lines the gearing bit is detected by GALA and converted always to zero. This preserves the magazine number as that set by the two least significant bits. The number of magazines available using the present decoder is 4. (Subsequent development of new chip sets will allow expansion of these by using header coding at present designated as time coded page information and detected as such by the 625-line TAC).

Display Compression (d)

In order to allow the display of 40 characters per row and 24 rows on a 525-line raster, a compression technique has been developed which only requires 192 active TV line pairs (interlaced). The character shape is essentially unchanged from the 625-line set but the row timing is now only every 8 TV lines instead of every 10. This is achieved using a special 525-line standard timing chip (SAA5025D), to drive the same TROM (SAA5050) as is used in the 625-line decoder.

DECODER BLOCK SCHEMATIC

Figure 1 shows the basic decoder elements in block form, made up of dedicated chips SAA5025D, SAA5030, SAA5040B, SAA5045 (GALA) and SAA5050 together with RAM. These are divided into functional areas to simplify the decoder description. Only the most important interconnections are shown in order to reduce complexity.

Inputs to the system are the video input to the Video Input Processor (VIP) and remote control signals (see Appendix 'A'), to (TAC) and (TROM).

Outputs consist of R, G and B, blanking, Y and superimpose control. These allow flexible interfacing with the TV set video drive system (see Appendix B).

Video Input Processor (SAA5030)

This chip (VIP) performs mainly analog functions concerned with extracting the data signal from the TV set video and presenting it in a suitable form to the Teletext Acquisition Chip (TAC, SAA5040B).

VIP also provides a phase-locked crystal oscillator at 384MHz horizontal line rate, i.e., 6.041957MHz. This frequency is divided down in the Timing Chip (TIC, SAA5025D) to produce all the line- and field-related timing waveform locked to the input video sync pulses. As ancillary to this function, VIP includes a sync separator to provide field rate sync to TIC.

Data is sliced in VIP by an adaptive slicer referenced to peak detectors. This is followed by Data Clock regeneration in a DC circuit. A data latch driven internally supplies latched data, correctly phased with the Data Clock, to TAC.

Gearing and Address Logic Array (GALA) SAA5045

Due to the system differences between 525- and 625-line Teletext, the data from VIP must be modified before it is presented to the Teletext Acquisition Chip (TAC, SAA5040B). The presence of a gearing bit set to '1' or '0' is detected in GALA and the data is delayed for one byte period in a shift register. This allows the inversion of the gearing bit, if required, to avoid confusion in the decoding of the magazine number (see paragraph on Gearing Bit System).

GALA includes a bistable which is set or not set, according to the state of the gearing bit. This is held for the duration of each data line and reset before the next. Also included in GALA are RAM address and read/write control functions.

Table 1. Data Line Coding for 525-Line Teletext (U.K. Modified) System Characteristics Current for Operating Systems 1982

CLOCK RUN IN	CLOCK RUN IN	FRAMING CODE	MAGAZINE AND ROW ADDRESS																						DATA								DATA	
1 0 1 0 1 0 1 0	1 0 1 0 1 0 1 0	1 1 1 0 0 1 0 0																																
DATA RATE 5.727272Mb/s (364 H = 8/5 COLOR SC) DATA PERIOD = 174.6ns H PERIOD = 63.55μs 32 BYTES DATA/LINE 32/8 SYSTEM 24 ROWS 40 CHARACTERS			P	2^0	P	2^1	P	2^2	P	2^0	P	2^1	P	2^2	P	2^3	P	2^4	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0								
			Hamming	Magazine 1	Hamming	Magazine 2	Hamming	Gearing Bit	Hamming	Row Address 1	Hamming	Row Address 2	Hamming	Row Address 3	Hamming	Row Address 4	Hamming	Row Address 5	Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Data 0	Etc.							
			Invert Bit 1				Invert Bit 2	Invert Bit 3	Invert Bit 4																										
← Start CRI 9.5 Microsec. From Sync 0 (Operation Normal As For 625)			Conversion Coding When Gearing Bit = 1																Operation Normal As For 625 Except Write RAM ENABLE (DATA) Limited To 32 Bytes →																

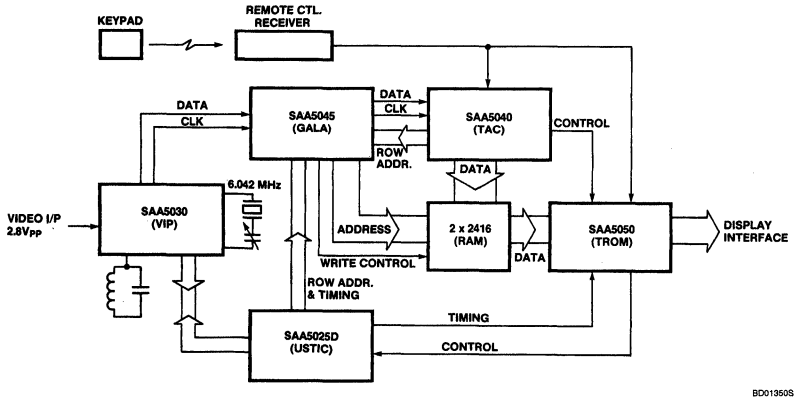

Figure 1. 5-Chip Decoder Block Schematic

Teletext Acquisition and Control (TAC, SAA5040B)

Data from GALA is clocked into TAC, by the data clock (5.727272MHz), where it is decoded byte-by-byte to provide character and control data for the storage in RAM. Row addresses are decoded after Hamming checks and issued to the RAM address system. A column address clock for writing into RAM during data lines (WACK) is also generated at byte (character) rate. Parity checking is carried out to produce write enable pulses ($\overline{WOK}$) for each correctly received character to be written into RAM.

Header (row zero) information is also decoded and Hamming checked in TAC so that only the data relating to the page called up by the remote-control system (Key Pad input of required page number) is written into RAM. Clearing functions are also controlled by Header and Remote Control input data, to clear the RAM.

Selected page number information is written into RAM by TAC during an unused TV line between the end of data entry (DEW) and the start of the text display period. When double-height characters are requested (via remote control), TAC issues commands to the timing chain (TIC) and display device (TROM). Similarly, the system controls for TEXT or TV or MIXED (Text + TV), are issued by TAC as picture ON (PO) and display enable (DE) to VIP and TROM.

Timing Chain (TIC, SAA5025D)

The timing of line and field rate functions together with display dot clock are derived from the VIP crystal oscillator (6.041957MHz) signal fed to TIC. This signal is counted down to line rate (÷384) and field rate, phase-locked to the incoming TV syncs. A composite sync waveform ($\overline{AHS}$) is also generated which free-runs (under crystal control) to allow display of text to continue after the TV signal has ended. This is known as 'after-hours sync'.

Row addresses for the display period are generated in TIC (A_0 through A_4) together with a column count (character rate) clock (RACK). The row addresses are stepped from zero to twenty-three at one-eighth of TV line rate, giving 24 rows at 8 lines/row in each field (60 fields/sec). This address information for reading RAM is multiplexed with the writing address information under control of a field rate signal generated by TIC, called DEW or data entry window. This is timed to occur on TV lines 10 through 19, inclusive, which are the lines in the vertical interval during which data is accepted. The DEW signal controls data entry in TAC, and also the address tri-state switches.

Signals fed back from TIC to VIP are used to reset the data slicer system and to enable rapid phase-locking of the crystal oscillator. A buffered dot rate clock at crystal frequency is issued by TIC to drive the display generators in TROM. The display area on the TV raster is controlled by the LOSE (load output shift register enable) signal from TIC which occurs on all active text lines.

When double-height characters are called up by control signals from TAC, originated at the Key Pad, the row addresses are stepped at half-rate and the top or bottom of the display is selected by the T/B signal. This resets the row address counter in TIC to start at row zero, or twelve of the text display.

Address Logic (GALA)

The address logic in GALA contains column address counters for the character rate address generation, a multiplexer for address combining, and an address latch/step function for the gearing system. Since the teletext address structure for transmission and display contains five row address bits and six column address bits, these must be reduced to a total of ten bits to suit conventional RAM structures. This is achieved in GALA by multiplexing the row and column addresses.

During the input of data lines, containing a gearing bit set to '1', a multiplexer causes the row address to be indexed every 8 bytes. The multiplexer is transparent to addresses during data lines containing a gearing bit set to zero. The row addresses from TAC go to the GALA and are multiplexed with the display row addresses under control of DEW, by tristates in TIC and TAC.

Random Access Memory (RAM)

Character data from TAC is stored in a page display memory with a capacity of 1024 8-bit bytes. Of these, only 960 bytes of 7-bit length are actually used. Data is written in during acquisition from TAC and read out during display to TROM, under control of write enable and chip select signals, generated from the $\overline{WOK}$ and DE signals from TAC via GALA. A common input/output bus structure is used in the devices employed in this decoder. Conflict of signal direction is avoided in the $\overline{WOK}$/DE gating arrangement in GALA.

Display Compression (5025D)

The drive signals from TIC (5025D) to TROM during the display period are organized so that suitably-shaped characters are generated by TROM on an 8 TV line pair per row basis. Since TROM is primarily intended for 10 line pairs per row operation, it is necessary to provide effectively 10 drive pulses per row per field, although output dot data is only required on eight of these in each field. The compression logic in TIC (5025D) inserts additional step pulses during the horizontal sync interval to keep the internal counters in TROM in the correct sequence. A further operation included is the blanking of the display during the same period to avoid spurious 'dots' on the TV tube. Character rounding normally employed in the TROM character generator is also controlled to obtain the best-shaped 'compressed' characters.

Teletext Read Only Memory (TROM, SAA5050)

This device contains the read only memory and character generating system which produces the text display (and graphics) characters. It is controlled by direct input remote-control signals (Key Pad-originated), and by transmitted controls via TAC. Timing of the display system is controlled by signals from TIC, and the actual display data is read in from the page memory RAM.

Output signals for R, G, B, Y, Blanking and superimpose are available by open-collector transistor output buffers. These are interfaced to the regular TV video drive system via 75Ω emitter-followers in this decoder. However, it is simple to obtain outputs at different impedance levels by the emitter-follower input/output components or by substituting TTL buffers with input pull-up resistors. Interfacing will differ for different setmakers, but the 75Ω $1V_{P-P}$ system is flexible in allowing long connections between the decoder and the video circuits of the TV.

FUNCTIONAL LOGIC INTERCONNECTION SCHEMATIC

The complete decoder is built on a double-sided PCB with Molex 0.1″ pitch plug connectors. Supplies required are 150mA at 12V and 250mA at 5V ± 5%. The supply rails are decoupled by distributed discrete 100nF capacitors not shown on the circuit diagram. PCB layout is only critical in the analog area surrounding VIP where connections must be kept short and ground paths sensibly routed. Good video frequency practice is followed in this area to ensure minimum radiation of interference and suppression of local oscillatory effects.

VIP Circuit

IC4, the SAA5030 device, has a number of discrete resistors and capacitors connected to it to define operating levels and frequencies. Tuning capacitors C_{17}, C_{18}, C_{15}, C_{12}, and C_{13} should all be of high-grade RF tuning types. The crystal XT1 is of similar grade to a color sub-carrier crystal in that it needs good setting stability with the possibility of being 'pulled' by about ± 750Hz for phase-locked operation.

The center frequency is 6.041957MHz when series-connected with a load capacitance of 30pF. Capacitor C_{17} and coil L_2 form a

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rejector circuit to avoid oscillation outside the correct frequency range of the crystal.

Inductor L_1 and capacitor C_{15} form the data clock recovery-tuned circuit. A coil Q-factor of greater than 50 is essential for good clock recovery. A component with an unloaded Q of 90 is commonly employed. The clock coil is tuned on test by applying a video signal at Pin 3 of PL3 containing data lines with pseudo-random data at 5.727272MHz preferably throughout the normal display period for ease of observation on an oscilloscope. This should be connected to Pin 18 of VIP.

The coil is adjusted for minimum jitter of the clock falling edge, which should occur approximately at the center of the 'eye' pattern formed by syncing the source data on another trace of the oscilloscope. For best results, it is preferable to trigger the oscilloscope from the data clock of the generator used to form the test data.

Phase-Locking Adjustments For Sync
The series-tuning capacitor, C_{19}, is used to adjust the center frequency of the crystal oscillator which determines horizontal (line) frequency phase-lock, whereas R_{10} is adjusted for field sync lock.

The crystal circuit is adjusted first while observing an input video signal at Pin 3 of PL3, together with a line frequency signal such as that on VIP Pin 5 ('sandcastle waveform'). Connecting Pin 1 of VIP directly to the 12V rail allows the oscillator to free-run, and shunting the filter capacitor C_1 with a 5.6MΩ resistor gives a preferred initial offset. C_{19} is then adjusted to obtain a stationary relationship between the two signals. The test connections on Pin 1 of VIP and C_1 should be removed when the two waveforms are to remain solidly locked in phase.

Field sync adjustment can then be carried out by adjusting R_{10} while observing the output of (FS) at Pin 13 of VIP together with the field sync of the incoming video. When correctly adjusted, the rising edge of (FS) should be half-way along the second broad pulse of the field sync pattern of the input video. This adjustment is important to ensure the correct selection of data lines in the vertical interval by the DEW signal. Field lock in the wrong position may cause the loss of one or more data lines.

The adjustments of the decoder are now complete; all subsequent areas of operation are controlled by digital systems.

Input and Output Requirements of VIP
The video input from the TV should be $2.8V_{P-P}$ at Pin 3 of PL3 and its DC level not $_{P-P}$ greater than 7V. If higher, the electrolytic capacitor C_5 (1μF) may be reverse-biased and cause maloperation of the DC restoration circuit in VIP.

Sync Output Signals
The TV set may be synchronized via VIP if a synchronized display is required from $\overline{AHS}$ when the TV signal disappears. This is obtained from Pin 2 of PL3. The polarity can be set by connecting resistor R_1 (1.5kΩ) via link (LPI) to +12V or 0V for negative- or positive-going syncs, respectively.

TAC (SAA5040B)

Data from GALA is clocked into TAC Pin 2 by the data clock at Pin 3, and also, from GALA. When correct data is received write enable pulses are issued from Pin 15 ($\overline{WOK}$). This is an indication that Hamming codes and parity are correct. Data is output in parallel from Pins 16 through 22 to RAM, while row address A_0 through A_4 are supplied by Pins 23 – 27.

Internal Data Writing to RAM
Selected page numbers, called up by the remote-control Key Pad input, are written into the row zero position in RAM, together with indications such as 'HOLD' and timed-page 'time'. This function occurs during TV line number 37 only. At this time the display enable (DE) output Pin 9 is held low and $\overline{WOK}$ pulses are emitted at Pin 15 in two groups of 8, corresponding to the first and last eight character spaces in row zero. Since this function occurs outside of the DEW period, the column counters are driven by read address pulses (RACK) from TIC.

Character Generator, TROM (SAA5050)

The character generator IC, (SAA5050) receives data from RAM during the display period (TV lines 48 to 239, inclusive) and internally decodes the data to generate characters or control functions. TROM receives direct remote-control information on Pins 3 (DATA) and 11 (DLIM) which control such functions as MIX (TV + text), and conceal/reveal.

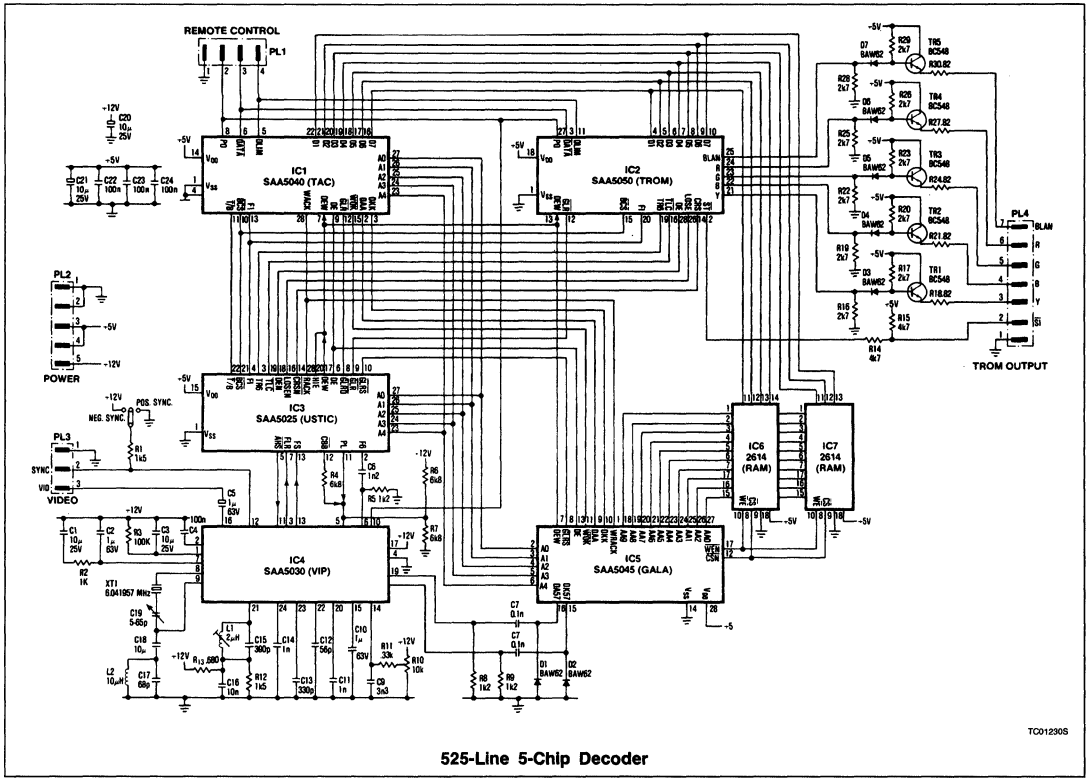
Control of display on/off (DE) and double-height are received from TAC on Pins 28 and 15, together with picture-on (PON), Pin 27. TROM outputs control signals to TIC from Pin 16 when 'Transmitted Large Characters' ($\overline{TLC}$) are called up by transmitted data codes.

The video output of TROM consists of R, G and B signals at Pins 24, 23 and 22 (open-collector) and a Y signal, Pin 21 (open-collector). Blanking is obtained at Pin 25 (open-collector) to switch the TV video on and off under control of signals decoded in TROM.

Superimpose signals from Pin 2 are used to modify the contrast setting of the TV video when MIX mode is called up (by remote-control or News Flash). This output Pin must be connected via a pull-up resistor of 10kΩ to the +5V rail, whether its output is used or not.

The R, G, B, Y and Blanking output buffers will drive interface circuits directly, if required, provided that the open-circuit output voltage does not exceed 13.2V maximum.

The 5-Chip Set Teletext Decoder AN153



525-Line 5-Chip Decoder

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Teletext Decoders: Keeping Up With the Latest Technology Advances

Application Note

Author: Nabil G. Damouny

ABSTRACT

The new generation teletext decoder, unlike its predecessor introduced in 1976, is user programmable under the control of a general purpose microcomputer or microprocessor. The new decoder is programmable to operate in the Vertical Blanking Interval (VBI) or full field teletext mode of operation. It can, simultaneously, acquire multi-pages resulting in a much faster system response time.

The new teletext decoder is I^2C bus controlled; therefore it is easy to integrate into any digitally-controlled I^2C bus system. The modular nature of the I^2C bus architecture allows the system designer to add to or delete from his or her system various function blocks. The teletext decoder can be treated as one of these blocks.

INTRODUCTION

Integrated Circuit (IC) technology has marched a long way since the advent of the first generation teletext decoder in 1976. Some improvements and new features can now be economically incorporated in the second generation decoder while keeping the chip count even lower than its first generation counterpart.

The new generation teletext decoder is microcomputer (or microprocessor) controlled. It is user programmable and therefore more flexible and friendlier to use. Today, virtually every system is microprocessor controlled. The microprocessor controls various special purpose peripheral chips, each controlling one or more functions of the overall system. One of these peripheral chips can control the television tuning function while another chip can control the teletext acquisition and display function. The system can be designed in a modular fashion so that modules performing different functions can be added to or deleted from the system with minimal effort.

The Inter-IC (I^2C) bus has been designed to achieve modularity. Bus interfacing problems are eliminated by integrating all the necessary bus handshake logic in the on-chip silicon. The I^2C bus is a serial bus consisting of two bidirectional lines: the Serial Data (SDA) line and the Serial Clock (SCL) line.

THE NEW GENERATION TELETEXT DECODER

The new generation teletext decoder consists of a super data slicer (the Video Input Processer — VIP), the teletext controller chip, multipage memory, and a general purpose microcomputer (see Figure 1).

The microcomputer communicates with the teletext controller via the I^2C. The microcomputer can be either a master or a slave; the teletext controller chip is a slave-only device.

The new teletext controller is an I^2C peripheral and belongs to the large "CLIPS" family. The new I^2C teletext decoder can be integrated in a system where a single microcomputer is used. The microcomputer is the only master and controls other system functions in addition to the teletext decoder, simultaneously (see Figure 2). On the other hand, since I^2C bus concept allows modularity, a multi-master system can be easily implemented (see Figure 3).

In the single master system, the system designer should allow for possible future software (and, consequently, memory) expansion. This is necessary to allow future system expansion. In the multi-master case, only one microcomputer is shown to receive and decode remote control commands. This microcomputer will then communicate the different commands to other microcomputers via the I^2C bus.

Microcomputers with built-in I^2C bus interface are available today. The instruction set is based on that of the industry standard 8048 microcomputer family.

The New Teletext Decoder Acquisition Circuitry

The teletext decoder accepts as input a composite video baseband signal. This signal is readily available in a TV set (to be discussed later). Digital data is inserted in the Vertical Blanking Interval (VBI) or into, virtually, all available TV lines (full-field). The acquisition circuitry can be programmed to operate in the VBI or in a full-field mode. Full-field teletext is a useful feature contributing to a very fast system response time but, obviously, does not permit any video information to be transmitted.

Since high-speed teletext digital data (data rate is 6.93MHz in Europe and only 5.72MHz in North America due to bandwidth limitation) is transmitted via broadcast information, a high performance data slicer is essential to have at the receiving end.

The video input processor should have good data slicing capability in the presence of echoes, noise, and co-channel interference. The device should provide compensation for high-frequency losses and be able to regenerate the clock from the digital data. The digital data can have different rates, as mentioned above. Other desirable features that the video input processor might have include: providing a mechanism by which it is easy to lock to a VCR; having a minimal number of external components/adjustments required; being able to accept many levels of peak-to-peak amplitudes of the composite video input; and last, but not least, consuming low power.

Digital data and its associated clock (Figure 4) can now be presented by the video input processor in a nice clean form to the teletext controller chip.

The teletext controller is looking for the page addressing information, imbedded in the page header — row number 0 — to find a match with the prespecified page number requested by the user via the remote control keypad. When a page address match is found, this page is captured and stored in page memory. In order to speed up the system response time and to make it friendlier to use, the acquisition circuitry is designed to capture four teletext pages simultaneously. Four independent acquisition circuits co-exist on the teletext controller and are able to capture four pages simultaneously. The four acquired pages can be specified, by the user program, to be the requested page plus the next three sequential pages or the requested page plus the next three linked pages as specified by the linking information received in ghost row number 27.

The teletext controller can then support up to 8k bytes of memory. If ghost rows are to be received and decoded for, 2k bytes of memory will be needed per teletext page.

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Teletext Decoders: Keeping Up With the Latest Technology Advances

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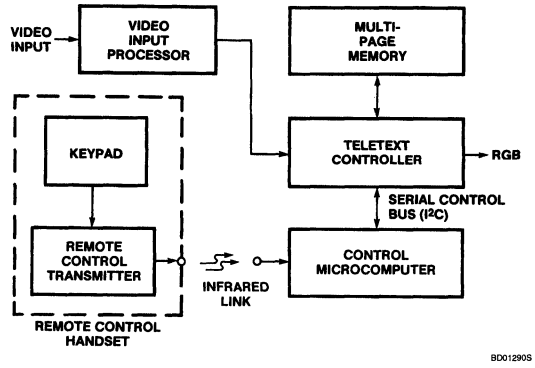

Figure 1. Computer-Controlled Teletext (CCT) Decoder Block Diagram

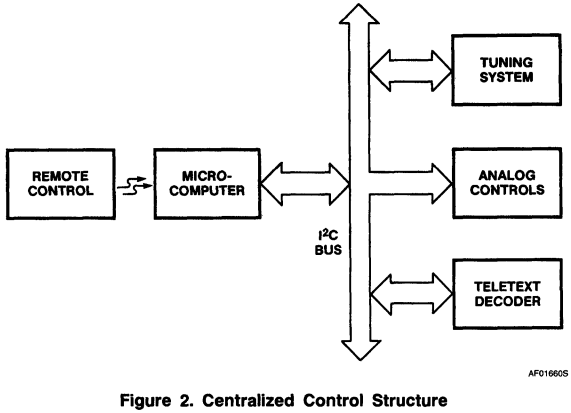

Figure 2. Centralized Control Structure

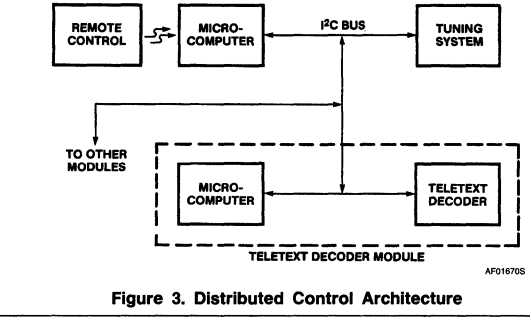

Figure 3. Distributed Control Architecture

The new acquisition circuitry can be programmed to receive the normal 7-bit plus one parity bit or 8-bit byte data. This is useful when a more sophisticated error correction scheme (such as CRC) needs to be implemented. The 8-bit mode is also instrumental in implementing the "telesoftware" concept. Through telesoftware, computer programs can be down-loaded and acquired as teletext information.

It is worth noting that the fixed format, World System Teletext, is virtually error free. This is due to the simple fact that a one-to-one correspondence exists between transmission codes, acquisition memory, display memory, and the actual display position on the screen. Due to the fact that teletext information is being constantly cycled through the system, an error received during one cycle can be automatically corrected during a subsequent cycle.

The New Teletext Decoder Display Circuitry

Since four pages can be acquired and stored in the acquisition memory simultaneously, but only one page can be displayed at a time, a display chapter register, residing on the teletext controller chip, is user programmable to select which acquired page is to be displayed. The display memory is, physically, the same as the acquisition memory. Ghost rows are not displayable and the display consists of 25 rows, (the 25th row contains locally generated status information), 40 characters each. The character cell occupies a 12× 10 dot matrix, giving nicely shaped characters at 12MHz dot rate. The display could be interlaced or non-interlaced.

There are four control functions that can be individually turned on or off under user software control. These are: TV picture, text, background, and contrast reduction. Boxed text information in a TV picture can be displayed by specifying the "Start box", "End box" control characters.

The teletext controller provides RGB outputs as well as a blanking output and a contrast reduction output. These outputs can be used as they are or a video buffer stage can be added (see Figure 4). This stage consists of emitter followers and clamping diodes. The diodes clamp the upper voltage values to a potential suitable for the particular TV receiver's contrast control. The blanking output is a combined box and dot blanking (full screen). The contrast reduction output is used for implementing more readable mixed (text over video) displays or to implement subtitles in reduced contrast boxes.

If a composite video display is desirable, a single chip multi-standard color encoder is available to produce PAL or NTSC compatible displays.

It is important to note that the new teletext decoder provides a secure means to synchronize the incoming video with the resulting text/video display. In addition, the decoder generates a composite sync signal that is suitable for driving the display time base.

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Teletext Decoders: Keeping Up With the Latest Technology Advances

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THE I²C BUS — GENERAL CONCEPT

Many system applications do not require very fast data transfer offered by the traditional parallel schemes.

As shown in Figure 5, a typical microcomputer-controlled television receiver using a parallel bus type architecture implies a large number of interconnects, devices with a large number of pinouts and a bigger layout area. Since many applications do not necessarily need the speed offered by parallel bus type architecture, an economical, easy to implement solution can be used. Figure 6 depicts the television receiver block diagram designed around the 2-wire I²C serial bus.

Many devices have been implemented with on-chip I²C bus interface logic. These devices communicate through the 2-wire serial bus. The system designer will no longer worry about the communication interface between the different blocks in his or her system and can now concentrate on the more important issues: the function/system requirements. Devices with built-in I²C bus interface can be added to or deleted from the system by simply "clipping" them to the common 2-wire bus. The only limitation is the bus capacitance of 400pF. Hence a collection of these devices is known as "CLIPS".

The I²C bus consists of 2 bidirectional lines, the Serial Data (SDA) line and the Serial Clock (SCL) line. Devices with built-in I²C bus interface can be implemented in any technology, i.e., NMOS, CMOS, I²L, TTL, etc. These devices are connected together (wired-AND) to form an I²C bus-based system, provided that they all exhibit an open collector output at each of their respective SDA and SCL lines.

The I²C bus concept allows a flexible master/slave relationship to exist. A device master during the present bus cycle can be a device slave during the following bus cycle.

An I²C bus cycle starts with a START condition (see Figures 7 and 8). A 7-bit device (slave) address is then sent followed by a single bit to determine the direction of the data transfer. A ninth clock pulse is then generated by the master device to allow the addressed receiver to acknowledge reception of this byte. Now any number of 8-bit data transfers can take place with the receiver acknowledging each byte after it has been received. At the end of the data transfer, the device master generates a STOP condition.

The I²C bus uses the wired-AND concept to achieve clock synchronization and proper arbitration between different device masters in the system. If two device masters start bidding for the bus simultaneously by generating the start condition, they will both be driving the SDA and the SCL lines. Clock synchronization is easily achieved through the wired-AND connection. The resulting clock will have a LOW period determined by the device master with the longest clock LOW period. The HIGH period of the resulting clock is determined by the device master with the shortest clock HIGH period.

Arbitration procedure in an I²C bus system is also easy to implement. Keep in mind that all devices are wire-ANDed and that a master device driving the SDA line will sample that line during the same clock period. In Figure 9 master device 1 is driving the data line HIGH but the resulting SDA line is LOW (due to master device 2) and so transmitter 1 loses

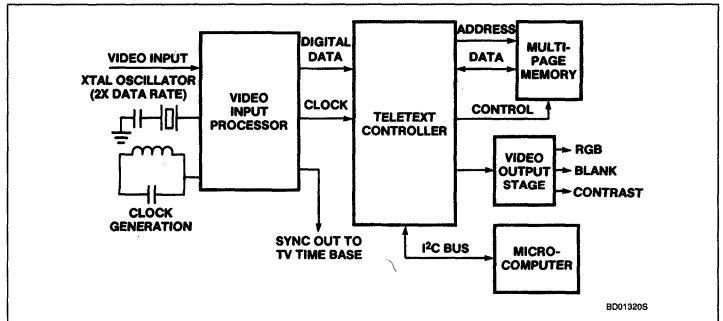

Figure 4. Teletext Decoder — Detailed Block Diagram

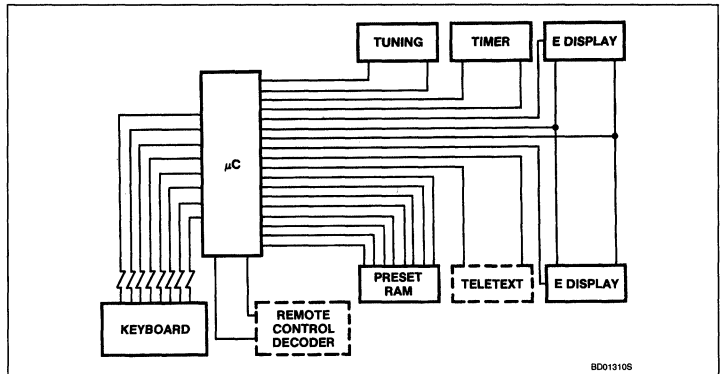

Figure 5. Conventional Microcomputer Controlled TV Receiver Block Diagram

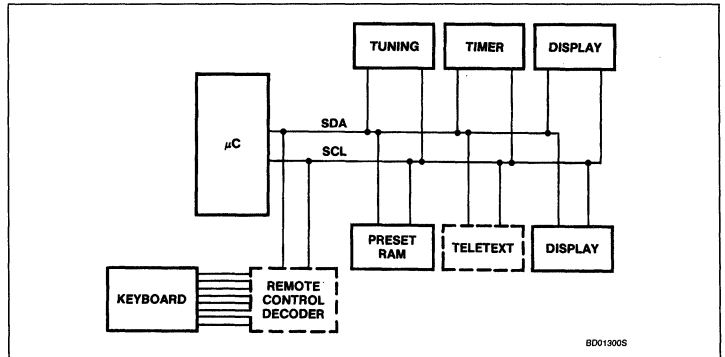

Figure 6. Block Diagram TV Receiver I²C Based

arbitration, after detecting that condition, and prepares itself as a slave that could be addressed during this very same cycle. Note that no time is wasted for the arbitration procedure since both address and data information is used to determine the winning bus master.

It is very comforting to know that all of the functions above have been implemented on all of the "CLIPS" peripherals. This allows system designers to implement modular architectures and build systems around the various available function blocks. Each function block, in its simplest form, can be one of the "CLIPS" peripherals.

TELETEXT DECODER — SYSTEM INTEGRATION

TV Receiver With Built-in Teletext Decoder

Teletext decoders, in general, can be easily integrated into TV receivers. In reality, TV receivers can be considered a natural home to house teletext decoders. The input to the teletext decoder is composite video, baseband signal which is already available at the output of the demodulator stage in a typical TV receiver (see Figure 10). The output of the teletext decoder consists of RGB signals, blanking and contrast reduction/control signals. The signals are of open-collector type and can be easily manipulated. A simple video output circuit might be needed at the output of the teletext decoder, the purpose of which is to provide the buffer/drive capability and the appropriate voltage level control suitable for the TV receiver under consideration. These signals can then be combined with the existing RGB and contrast control signals available at the output of the TV video amplifier stage.

In Figure 10, the digital portion of the TV chassis is depicted to be I^2C controlled. Some of the function blocks can be implemented with a single chip belonging to the "CLIPS" peripheral set. For example, the tuning function, as well as controlling the various analog signals, is implemented using one of the "CLIPS" peripherals. Non-volatile serial memory devices (I^2C bus compatible) as well as LCD display drivers are readily available and can be, as explained earlier, clipped to the I^2C bus.

Teletext Decoder as a Set-Top Adapter

Teletext service can be incorporated in existing TV receivers through the addition of a set-top adapter. The set-top adapter concept is familiar through the use of the CATV cable converter boxes. The set-top adapter concept will offer the average consumer teletext and cable TV service as well as a remote control feature. This is true even though his or her existing TV is, at present, not remotely controlled.

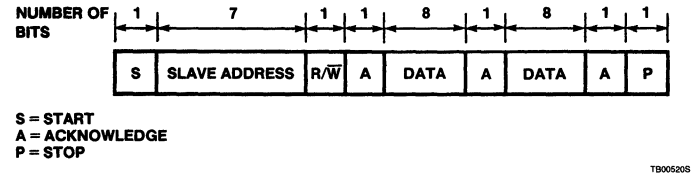

Figure 7. Typical I^2C Data Transfer

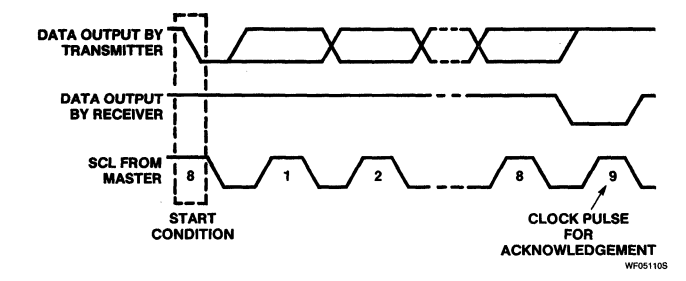

Figure 8. Acknowledgement on the I^2C Bus

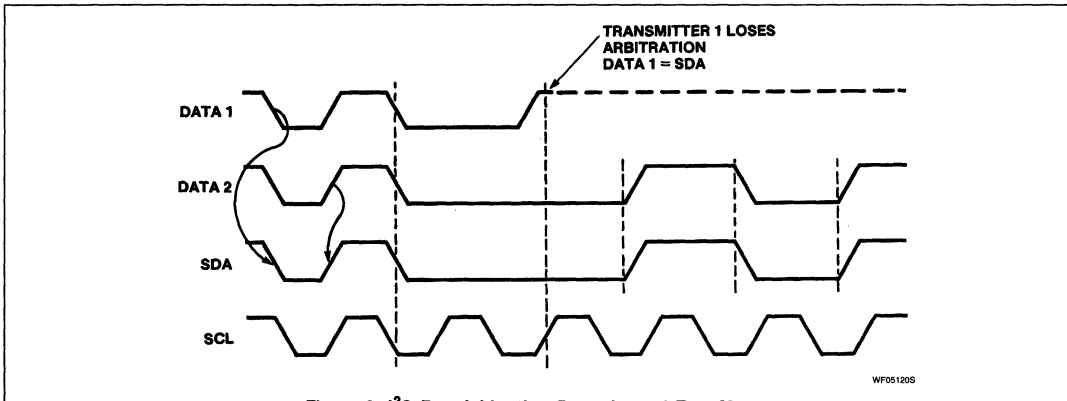

Figure 9. I^2C Bus Arbitration Procedure of Two Masters

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Figure 11 depicts a set-top adapter block diagram. The switch can be used to inhibit the teletext feature, if necessary. On the other hand when switching at high speed, this switch can be used to implement a superimposed text over video feature.

SUMMARY

The newly introduced teletext decoder is discussed. The decoder is microcomputer-controlled so it is user-programmable. The teletext controller chip belongs to the diversified number of I²C bus peripherals, known as "CLIPS", and therefore can be easily integrated in an I²C bus controlled digital system. The new decoder performs well under poor signal conditions, it can work in either VBI or full-field mode, it offers an easy, effective way to implement the "telesoftware" concept, it can acquire multi-teletext pages simultaneously resulting in a fast system response time and is capable of displaying interlaced or non-interlaced type displays. In addition to all of the above, the new teletext decoder is

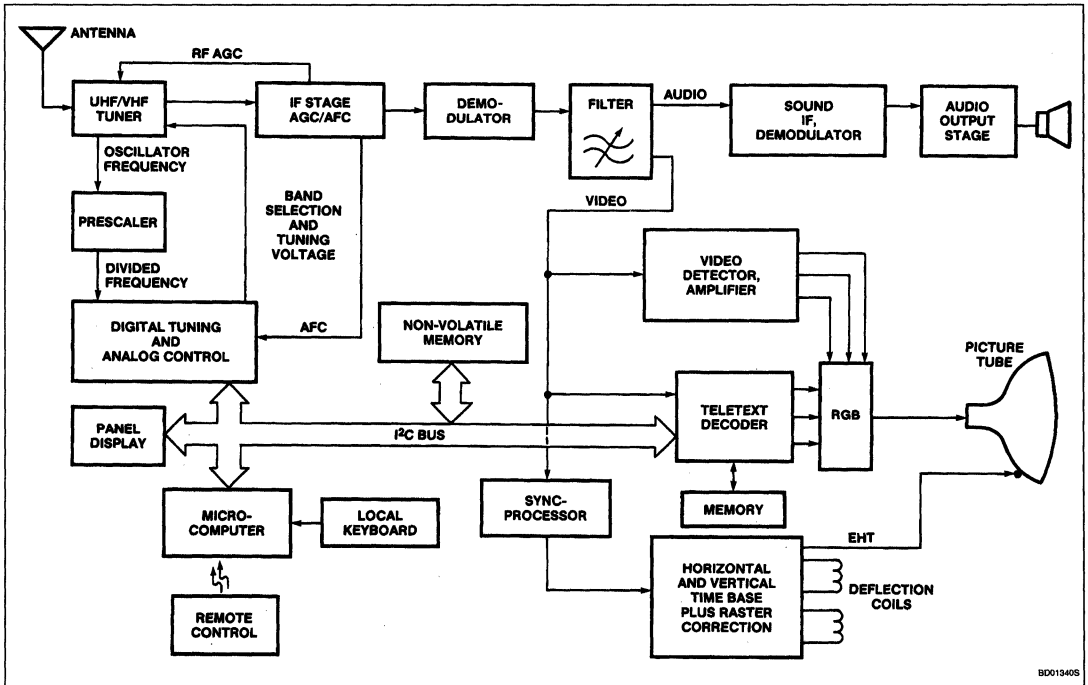


Figure 10. TV Receiver Block Diagram

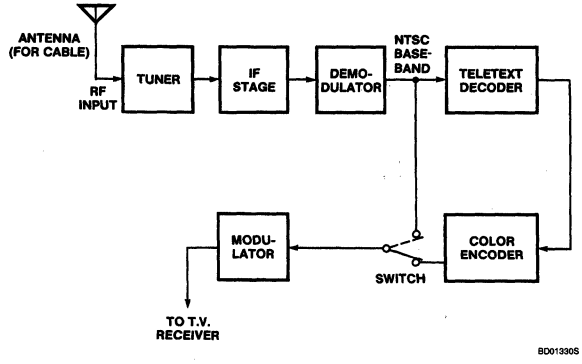


Figure 11. Teletext Set-Top Adapter

easy to integrate into a TV receiver or as a set-top adapter.

REFERENCES

1. LSI Circuits for Teletext and Viewdata, Mullard Technical Publication M81-0001, 1981.
2. "I^2C Bus Specification", Signetics Corporation, 1984.
3. Computer Controlled Teletext, User Manual, N.V. Philips, 1984.
4. Basic Television — Principles and Servicing, Grob, McGraw Hill, 4th Edition.

Signetics

SAA5025

Teletext Timing Chain for USA 525-Line System

Product Specification

Linear Products

DESCRIPTION

The SAA5025 is a MOS N-channel integrated circuit which performs the timing functions for a Teletext system. It provides the necessary timing signals to extract data from a memory and produce a display according to the USA 525-line television standard (system M).

The SAA5025 may be used in conjunction with the SAA5030 (Teletext video processor; VIP) the SAA5050 (Teletext character generator; TROM), the SAA5040B (Teletext acquisition control; TAC) and the SAA5045 (Gearing and Address Logic Array; GALA).

FEATURES

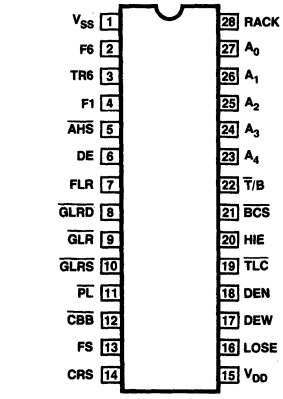
- **Designed to operate with USA 525-line television standard (system M)**
- **For 24 row (8 TV lines per row) × 40 character display**
- **Big character select input for double-height characters**
- **Composite sync signal output for display time-base synchronization**

APPLICATIONS

- **Teletext**
- **Telecaptioning**
- **Videotex**
- **Phase-locking with incoming video (when used with SAA5030)**
- **Composite sync generator**
- **Low cost display systems (when used with SAA5050 series)**

PIN CONFIGURATION

N Package



TOP VIEW

CD12310S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{SS}	Ground
2	F6	6.0419MHz clock input
3	TR6	6.0419MHz clock output
4	F1	1.007MHz clock output
5	$\overline{AHS}$	After hours sync output
6	DE	Display enable input
7	FLR	Fast line reset input
8	$\overline{GLRD}$	General line reset delay output
9	$\overline{GLR}$	General line reset output
10	$\overline{GLRS}$	General line reset starting output
11	$\overline{PL}$	Phase-locked open-drain output
12	$\overline{CBB}$	Color burst blanking output
13	FS	Field (picture) sync input
14	CRS	Character rounding select output
15	V_{DD}	Positive supply (+5V)
16	LOSE	Load output shift register enable output
17	DEW	Data entry window output
18	DEN	Display enable output (negative-going)
19	$\overline{TLC}$	Transmitted large characters input
20	HIE	High impedance enable input
21	$\overline{BCS}$	Big character select input
22	$\overline{T}$/B	Top/bottom select input
23	A_4	Memory row address outputs (3-state)
24	A_3	
25	A_2	
26	A_1	
27	A_0	
28	RACK	Read address clock output

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−20°C to +70°C	SAA5025DN

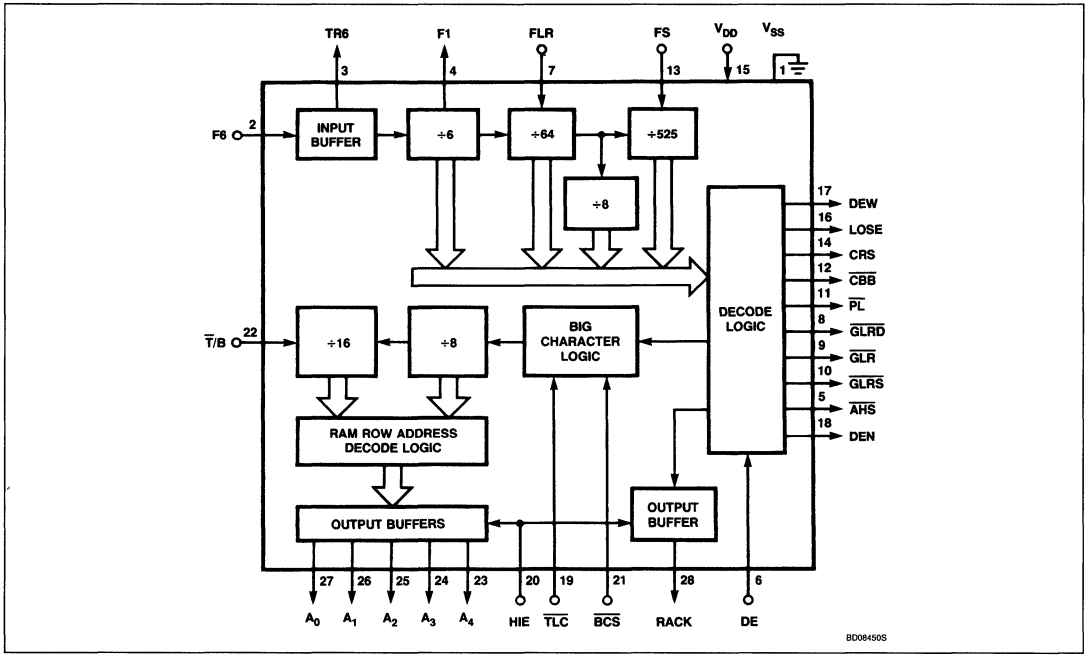
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.3 to +7.5	V
V_I	Input voltage range[1]	−0.3 to +7.5	V
V_{OHZ}	High-impedance state output voltage	−0.3 to +7.5	V
V_{ODD}	Open-drain output voltage	−0.3 to +13.2	V
	Electrostatic charge protection on all inputs and outputs[2, 3]	1000	V
P_{TOT}	Total power dissipation per package	275	mW
T_A	Operating ambient temperature range	−20 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTES:

1. See also characteristics on F6 input and Figure 8.
2. Equivalent to discharging a 250pF capacitor through a 1kΩ series resistor.
3. N.B.: the SAA5025 is not protected against TV tube flash-over.
4. All outputs are TTL compatible.

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	5	5		50	mA
Inputs						
	Input leakage currents					
I_I	F6	5.5	0.2		10	μA
$-I_I$		0			10	μA
$\pm I_I$	FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	0 to 5.5			10	μA
C_I	Input capacitance; all inputs	5			7	pF
	High level input voltages					
V_{IH}	F6 (see Figure 8)	5	2.7		6.5	V
V_{IH}	FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	5	2.0[1]		5.5	V
V_{IL}	Low level input voltage (all inputs); (see Figure 8)	5			0.8[1]	V
t_R, t_F	Input rise and fall time F6 (see Figure 4)	0 and 2.7			30	ns
δ	Input F6 duty factor (see Figure 8)	5	40	50	56	%
Outputs						
C_O	Output node capacitance (all outputs)	5			7	pF
$\pm I_O$	Output leakage current high-impedance state; A_0 to A_4, RACK	0 to 5.5			10	μA
I_O	Output leakage current open-drain; $\overline{PL}$, $\overline{CBB}$	6			10	μA
Output TR6 6.041957MHz clock						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.75		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			15	pF
t_R, t_F	Output rise and fall times (see Figure 5)	5			30	ns
δ	Duty factor at 1.5V level depends on input F6 (see F6 data and Figure 8)	5	40		60	%
Output F1 1.007MHz clock						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.75		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			40	pF
t_R, t_R	Output rise and fall times (see Figure 5)	5			50	ns
t_{PHL}, t_{PLH}	Propagation delays from rising edge of TR6 (see Figure 6) High-to-Low and Low-to-High	5	7		60	ns
δ	Duty factor at 1.5V level	5	45	50	52	%

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Output $\overline{\text{AHS}}$ (see Figure 6)						
V_{OH}	High level output voltage $-I_{OH} = 200\mu A$	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage $I_{OL} = 1.6mA$	5	0		0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times (see Figure 7)	5			100	ns
t_{PLH}	Propagation delay from rising edge of F1 (see Figure 8) Low-to-High	5	0		350	ns
Outputs $\overline{\text{GLR}}$, $\overline{\text{GLRD}}$, $\overline{\text{GLRS}}$ (see Figure 3)						
V_{OH}	High level output voltage $-I_{OH} = 100\mu A$	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage $I_{OL} = 0.8mA$	5	0		0.4	V
C_L	Output load capacitance	5			40	pF
t_R t_F	Output rise and fall times (see Figure 7)	5			70 50	ns ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of F1 (see Figure 8) High-to-Low and Low-to-High	5	0		300	ns
Output $\overline{\text{PL}}$ (see Figure 3)						
V_{OL}	Low level output voltage $I_{OL} = 2mA$	5	0		1.0	V
C_L	Output load capacitance	5			30	pF
t_F	Output fall time (see Figure 7)	5			100	ns
t_{PLH}	Propagation delay from rising edge of F1 (see Figure 8) Low-to-High	5	0		250	ns
Output $\overline{\text{CBB}}$ (see Figure 2)						
V_{OL}	Low level output voltage $I_{OL} = 2mA$	5	0		1.0	V
C_L	Output load capacitance	5			30	pF
t_F	Output fall time (see Figure 5)	5			200	ns
t_{PLH}	Propagation delay from rising edge of F1 (see Figure 6) Low-to-High	5	0		250	ns
Output CRS						
V_{OH}	High level output voltage $-I_{OH} = 100\mu A$	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage $I_{OL} = 100\mu A$	5	0		0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times (see Figure 5)	5			1	μs

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Output LOSE (see Figure 1)						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 100μA	5	0		0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times (see Figure 5)	5			50	ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of F1 (see Figure 6) High-to-Low and Low-to-High	5	0		1	μs
Output DEN						
V_{OH}	High level output voltage $-I_{OH}$ = 200μA	5	2.4			V
V_{OL}	Low level output voltage I_{OL} = 100μA	5			0.4	V
C_L	Output load capacitance	5			30	pF
t_R, t_F	Output rise and fall times	5			50	ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of F1; High-to-Low and Low-to-High	5			250	ns
Output DEW (see Figure 2)						
V_{OH}	High level output voltage $-I_{OH}$ = 200μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 1.6mA	5	0		0.4	V
C_L	Output load capacitance	5			50	pF
t_R, t_F	Output rise and fall times	5			200	ns
t_{PHL}, t_{PLH}	Propagation delay from rising edge of $\overline{CBB}$ (see Figure 6) High-to-Low and Low-to-High	5	6.5	6.96	7.5	μs
Outputs A_0 to A_4 (see Figure 2)						
V_{OH}	High level output voltage $-I_{OH}$ = 100μA	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage I_{OL} = 1.6mA	5	0		0.4	V
C_L	Output load capacitance	5			85	pF
t_R, t_F	Output rise and fall times	5			1	μs
t_{PHL}, t_{PLH}	Propagation delay from falling edge of $\overline{CBB}$ (see Figure 6) High-to-Low and Low-to-High	5	6.5		9.0	μs
t_{PHZ}, t_{PLZ}	Propagation delay from rising edge of HIE to high-impedance state (see Figure 7)	5	0		0.9	μs
t_{PZH}, t_{PZL}	Propagation delay from falling edge of HIE to normal active state (see Figure 7)	5	1		2.9	μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; F6 input frequency = 6.041957MHz, unless otherwise specified.

SYMBOL	PARAMETER	V_{DD} (V)	LIMITS			UNIT
			Min	Typ	Max	
Output RACK (see Figures 1 and 2)						
V_{OH}	High level output voltage $-I_{OH} = 100\mu A$	5	2.4		V_{DD}	V
V_{OL}	Low level output voltage $I_{OL} = 1.6mA$	5	0		0.4	V
C_L	Output load capacitance	5			40	pF
t_R t_F	Output rise and fall times (see Figure 5)	5			60 300	ns ns
t_{PHL}	Propagation delay from falling edge of F1 (see Figure 6) High-to-Low	5	150		280	ns
t_{PHZ}, t_{PLZ}	Propagation delay from rising edge of HIE to high-impedance state (see Figure 7)	5	1		2.9	μs
t_{PZH}, t_{PZL}	Propagation delay from falling edge of HIE to normal active state (see Figure 7)	5	0		0.9	μs

NOTE:
1. These values give no noise immunity.

FUNCTIONAL DESCRIPTION

The basic input to the SAA5025 is a 6.0419MHz clock signal (e.g., from SAA5030). The clock input (F6) is buffered and also available as an output at TR6 to provide a dot rate clock. The signal at F6 is divided by 6 to produce the 1.007MHz character rate clock at output F1, which is in turn divided by 64 to produce the line period of 63.556μs. A divide-by-262 or 263 counter, clocked at line rate, produces a field (picture) period of 16.683ms (average), i.e., 33.366ms for divide-by-525. The display format is 40 characters per row for 24 rows (1 row is 8 TV lines).

A big character select ($\overline{BSC}$) input is provided and it enables double-height characters (16 TV lines per row) to be displayed. The top or bottom select ($\overline{T}/B$) input must be used in conjunction with $\overline{BCS}$ to select either the top half or bottom half of the page to be displayed on the television screen.

A composite sync ($\overline{AHS}$) output is available for synchronizing the display timebase. A high-impedance enable (HIE) input is included to switch the read address clock (RACK) and the memory row address (A_0 to A_4) outputs into their high-impedance states.

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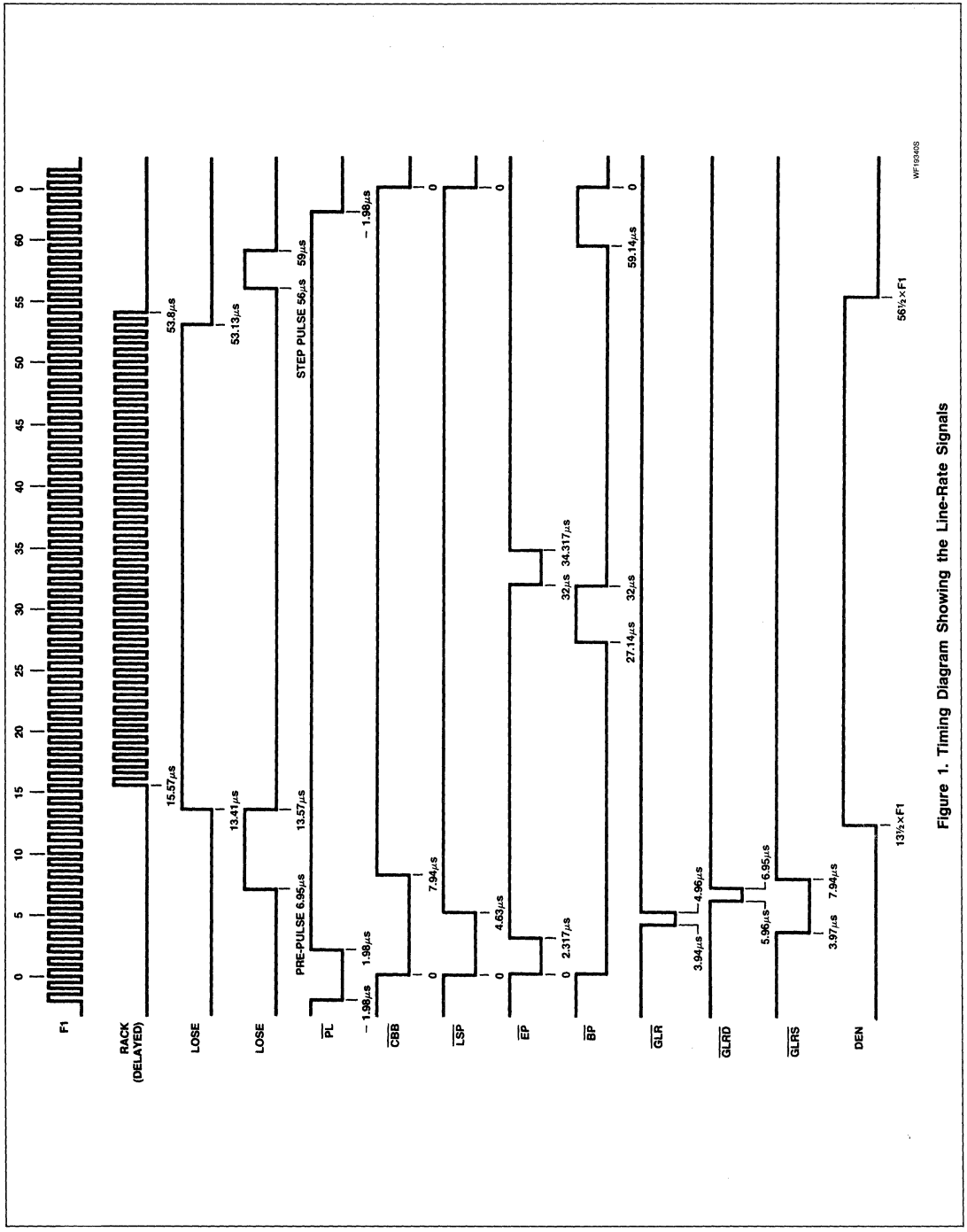

Figure 1. Timing Diagram Showing the Line-Rate Signals

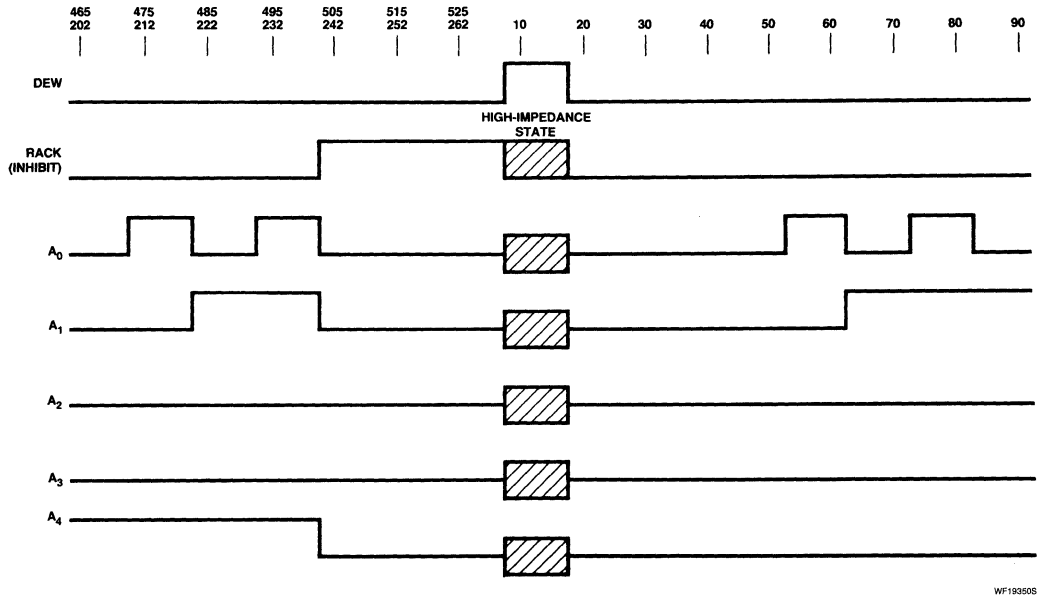

Figure 2. Timing Diagram Showing the Decoded Signals From the Field (Picture) Counters

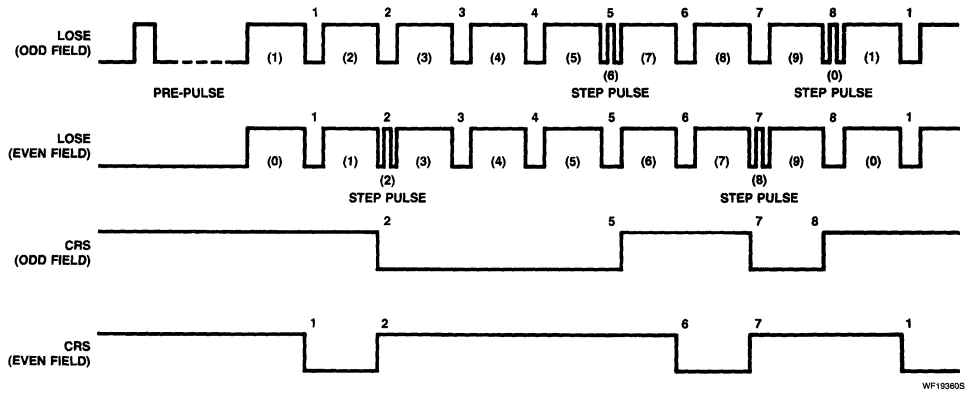

Figure 3. Timing Diagram Showing the Field-Rate Signals

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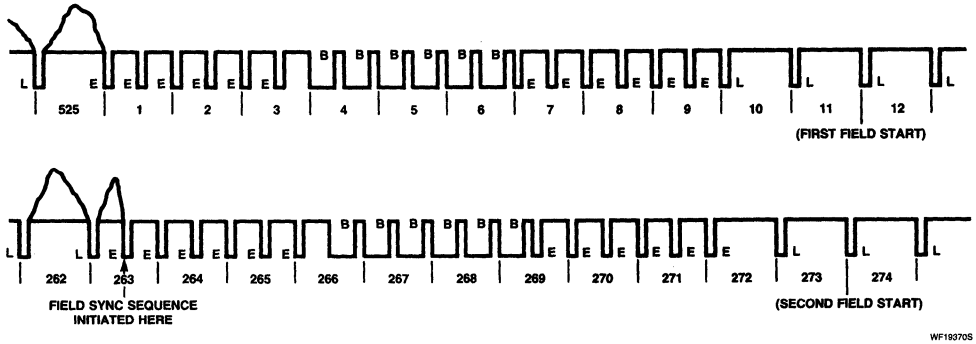
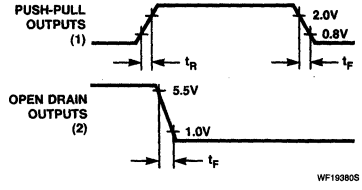


NOTES:
L = line sync pulses (4.2 to 5.1μs)
E = equalizing pulses (2.29μs ± 10%)
B = broad pulses (26.4 to 28μs)

Figure 4. After-Hours Sync Waveforms



NOTES:
1. These outputs will be tested with simulated TTL loads and with the load resistors adjusted such that the correct current conditions are obtained.
2. These outputs will be tested with 3kΩ resistors to the +6V line for outputs $\overline{PL}$ and $\overline{CBB}$.

Figure 5. Definition of the Rise and Fall Times for the Output Stages

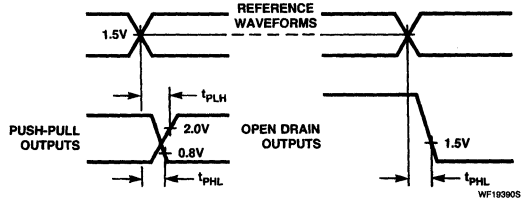


Figure 6. Definition of the Propagation Delays for the Output Stages

APPLICATION INFORMATION

The function is described following the corresponding pin number.

1 V_{SS} — Ground (0V)

2 F6 6.041957MHz Clock Input — Obtained from video processor (SAA5030) or other source. The permissible mark/space ratio is in the range from 56:44 to 40:60 (see also Figure 8).

3 TR6 6.041957MHz Clock Output — Dot-rate clock for Teletext character generator SAA5050 series.

4 F1 1.007MHz Clock Output — Character-rate clock for Teletext character generator SAA5050 series.

5 $\overline{AHS}$ After-Hours Sync Output — A composite sync waveform consisting of a successive sequence of line sync pulses ($\overline{LSP}$) followed by six equalizing pulses ($\overline{EP}$), six broad pulses ($\overline{BP}$), and six equalizing pulses ($\overline{EP}$), and is followed by another sequence of $\overline{LSP}$. This composite sync waveform occurs at the end and beginning of each field/picture (see also Figure 4).

6 DE Display Enable Input — A Low level signal from the Teletext acquisition and control circuit (SAA5040 series) to this input switches output DEN to the Low state.

7 FLR Fast Line Reset Input — This is the input for a positive-going pulse with a duration of 0.5μs to 63μs which resets the line rate counter (÷64). After accepting an FLR pulse, further resets are inhibited for one line period of approximately 63.5μs.

8 $\overline{GLRD}$ General Line Reset Delay Output — A negative-going pulse with a duration of 993ns which commences 5.96μs from the start of each line (see also Figure 1).

9 $\overline{GLR}$ General Line Reset Output — A negative-going pulse with a duration of 993ns which commences 3.97μs from the start of each line (see also Figure 1).

10 $\overline{GLRS}$ General Line Reset Starting Output — A negative-going pulse with starting 3.97μs and ending 7.94μs from the start of each line (see also Figure 1).

11 $\overline{PL}$ Phase-Locked Open-Drain Output — This open-drain output is used to lock the oscillator in the SAA5030 to the line rate. It is a negative-going pulse with a duration of 3.96μs which starts at 61.58μs on one line and ends at 1.98μs after the start of the following line (see also Figure 1).

12 $\overline{CBB}$ Color Burst Blanking Output — This open-drain output blanks the color burst in the SAA5030. It is a 7.94μs negative-going pulse which starts at the beginning of each line (t = 0; see also Figure 1).

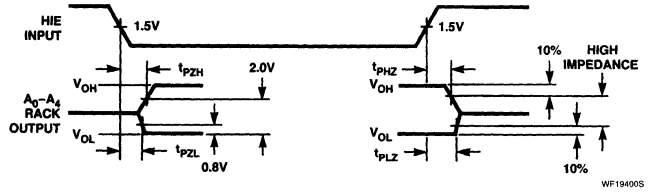
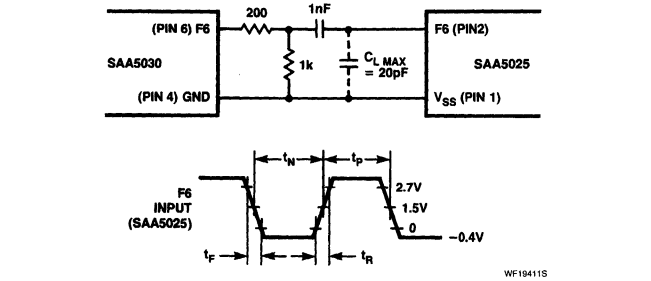


Figure 7. Definitions of the High-Impedance State Propagation Delay Times



NOTES:
1. With this circuitry the F6 input will be set to a level of approximately −0.4V in the low state. This is acceptable as the internal clamping diode in the F6 input of the SAA5025 provides an adequate current clamp.
2. Also shown is the F6 input waveform with the appropriate definitions.
3. The duty factor is defined as: $\frac{t_P}{t_P + t_N} \times 100\%$.

Figure 8. Recommended 6MHz Interface Circuitry Between the SAA5025 and the SAA5030 (Input F6)

13 FS Field (Picture) Sync Input — This input accepts a positive-going pulse of approximately 160μs duration. Its leading edge occurs during the second half of line one on even fields (half picture) and correspondingly in odd fields (other half picture). It is ignored during the odd field.

14 CRS Character Rounding Select Output — The output signal starts High during the even field (lines 1 to 263), goes Low after the first LOSE pulse, again High after the second LOSE pulse, then Low after the sixth LOSE pulse, and finally High at the end of the seventh LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Figure 3). For the odd field (lines 264 to 525) CRS starts High, goes Low after the second LOSE pulse, again High after the fifth LOSE pulse, then Low after the seventh LOSE pulse and finally High at the end of the eighth LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Figure 3).

15 V_{DD} Positive Supply — (+5V)

16 LOSE Load Output Shift Register Enable Output — This is a positive-going output pulse of 39.72μs duration commencing 13.41μs from start of line valid during line 47 to 238 inclusive, for the even field. A step-pulse starting at the count of 3 character rate clock pulses (F1) after the second and seventh LOSE pulses and at the count of 3 character rate clock pulses repeated every row is included. For the odd field, the LOSE pulse is preceded by a pre-pulse of 7μs duration commencing 7.41μs in line 20, and has a step-pulse after the fifth and eighth pulse, repeated every row (see also Figure 3).

17 DEW Data Entry Window Output — This output defines the period during which data may be extracted from the incoming television signal. It is High during lines 7 to 18 inclusive for the even fields and line 270 to 281 inclusive for the odd fields. The positive-going pulse has a duration of 762.67μs and commences at 6.95μs from the start of the line (see also Figure 2).

18 DEN Display Enable Output — The output pulse is positive-going at 13.5μs from the start of a line to 56.5μs and is active during line 47 to 238 inclusive if the DE input is High. If the DE input is Low, the DEN is held in the Low state.

19 $\overline{TLC}$ Transmitted Large Characters Input — When this input is Low, it enables rows of double-height characters to be displayed as required. Large characters descend into the next memory row address location. $\overline{TLC}$ is

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always High (i.e., small) for the first line of a row, even if it contains large characters.

20 HIE High Impedance Enable Input — When this input is in the High state, it will force the RACK and memory row address output into the high-impedance state. For normal Teletext operation, this input should be connected to the DEW output (Pin 17).

21 $\overline{BCS}$ Big Character Select Input — For normal size character display, this input signal must be High while a Low gives double-height characters.

22 $\overline{T}$/B Top/Bottom Select Input — When both $\overline{BCS}$ and $\overline{T}$/B are Low, the top half of a page is displayed with double-height characters. If $\overline{T}$/B is High and $\overline{BCS}$ is Low, the bottom half of the page is also displayed with double-height characters.

23 to 27 A_0 to A_4 Memory Row Address Outputs (3-State) — These binary count outputs sequencing from 00000 (count 0) to address 10111 (count 23) for the 40 × 24 format.

The binary count changes every 8 TV lines per row in the display period of line 47 to 238 inclusive for the 24-row display. The count changes between 6.5μs and 9.0μs during the line period.

28 RACK Read Address Clock Output — This is the read address clock output to the SAA5045 (GALA) column address counter during the display period. It consists of 39 positive pulses at the 1.007MHz rate starting at 13.57μs from the start of the line period with the last negative edge occurring at 51.8μs. This sequence is active on line 45 to 238 inclusive. RACK is delayed by two F1 clock periods for the whole of the field when input DE is Low for the whole of line 39. On lines 19 to 44 inclusive, output RACK is permanently delayed by two F1 clock periods, unaffected by DE.

NOTES:

1. In the big character top mode the memory row address count is 0 to 11, and in the big character bottom mode the count is 12 to 23. Each big character row is equal to 16 television lines.
2. The memory row addresses are held Low for one line period starting 6.5μs to 9μs from the beginning of line 36 which is only valid in the big character bottom mode.

Signetics

SAA5030
Teletext Video Processor

Product Specification

Linear Products

DESCRIPTION

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext TV data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control Circuit SAA5040. A 6MHz crystal-controlled, phase-locked oscillator is incorporated which drives the Timing Chain Circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronize the timing chain.

FEATURES

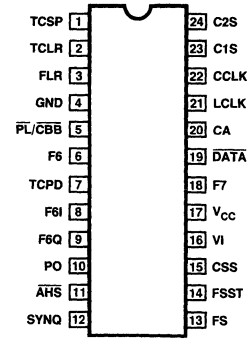
- **Slices digital data embedded in the composite video signal**
- **Generates a synchronized clock for the sliced data**
- **Generates a system display clock, locked with the incoming video signal**
- **On-chip signal quality detector**
- **On-chip adaptive sync separator**

APPLICATIONS

- **Teletext**
- **Data slicer**
- **Phase-locking with incoming video (when used with SAA5025D)**
- **Telecaptioning**

PIN CONFIGURATION

N Package



TOP VIEW

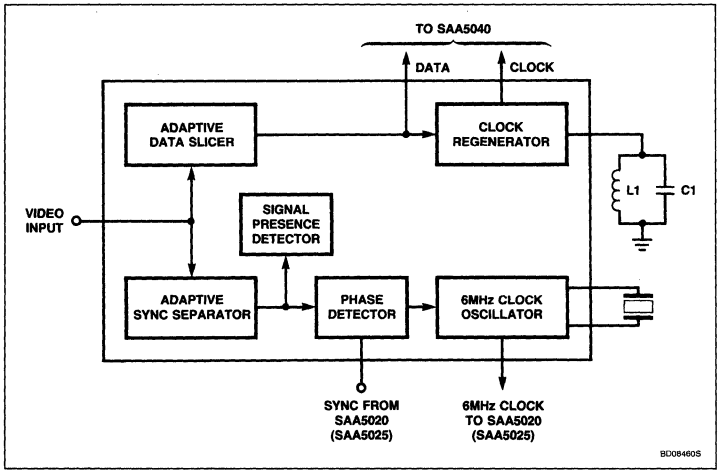
CD12320S

PIN NO.	SYMBOL	DESCRIPTION
1	TCSP	To signal presence time constant components
2	TCLR	Line reset time constant
3	FLR	Fast line reset output
4	GND	Ground (0V)
5	PL/CBB	Sandcastle input
6	F6	6MHz output
7	TCPD	To phase detector time constant components
8	F6I	6MHz crystal oscillator input
9	F6Q	6MHz crystal oscillator output
10	PO	Picture-on input
11	AHS	After-hours sync input
12	SYNQ	Sync output to TV
13	FS	Field sync output
14	FSST	Field sync separator timing
15	CSS	To sync separator capacitor
16	VI	Composite video input
17	V_{CC}	+12V supply
18	F7	Clock output
19	DATA	Data output
20	CA	Clock phase capacitor
21	LCLK	Clock regenerating coil
22	CCLK	To clock pulse timing capacitor
23	C1S	Peak detector capacitor pin
24	C2S	Peak detector capacitor pin

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	−20°C to +70°C	SAA5030N

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V_{17-4}	13.2	V
V_I	Input voltages V_{5-4}	9	V
V_I	V_{10-4}	V_{CC}	V
V_I	V_{11-4}	7.5	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V_{CC} = 12V$, and with external components as shown in Figure 3, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	10.8	12.0	13.2	V
I_{CC}	Supply current ($V_{CC} = 12.0V$)		110		mA
Video input and sync separator					
$V_{16VIDEO(P-P)}$	Video input amplitude (sync to white); see Figure 2	2.0	1.4	3.0	V
$\|Z_S\|$	Source impedance, f = 100kHz			250	Ω
$V_{16SYNC(P-P)}$	Sync amplitude	0.07	0.7	1.0	V
t_D	Delay through sync separator		0.5		µs
t_D	Delay between field sync datum at Pin 12 and the leading edge of separated field sync at Pin 13[1] (see Figure 2)	32	48	62	µs
Field sync output					
V_{OL}	V_O (Low) ($I_{13} = 20\mu A$)			0.5	V
V_{OH}	V_O (High) ($-I_{13} = 100\mu A$)	2.4			V
f_{F6}	Frequency		6.0		MHz
	Holding range	1.5	3.0		kHz
	Catching range	1.5	3.0		kHz
	Control sensitivity of phase detector measured as voltage at Pin 7 with respect to phase difference between separated syncs and phase-locked pulse $\overline{PL}$		0.3		mV/ns
	Control sensitivity of oscillator measured as change in 6MHz phase shift from Pin 8 to Pin 9 with respect to voltage at Pin 7		2		deg/mV
	Gain of sustaining amplifier, V_{9-8} measured with input voltage of $100mV_{P-P}$ and phase detector immobilized	2.5			V/V
	Output voltage of 6MHz signal at Pin 6, measured into 20pF load capacitance; peak-to-peak value		5.5		V
t_R, t_F	Output rise and fall times at Pin 6 into 20pF load			30	ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) At $T_A = 25°C$, $V_{CC} = 12V$, and with external components as shown in Figure 3, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Data slicer and clock regenerator					
	Teletext data input amplitude, Pin 16 (see Figure 2); peak-to-peak value[2]		1.1		V
	Data input amplitude at Pin 16 required to enable amplitude gate flip-flop; peak-to-peak value		0.46		V
	Attack rate, measured at Pins 23 and 24 with a step to Pin 16 (positive) (negative)		 15 9		 V/μs V/μs
	Decay rate, measured at Pins 23 and 24 with a step input to Pin 16	48	100	144	mV/μs
	Width of clock coil drive pulses from Pin 21 when clock amplitude is not being controlled[3]		40		ns
	Clock hangover measured at Pin 18 as the time the clock coil continues ringing after the end of data[4]	20			Clock Periods
	Clock and data output voltages at Pins 18 and 19 measured with 20pF load capacitance; peak-to-peak value		5.5		V
t_R, t_F	Output rise and fall times at Pins 18 and 19 into 20pF loads			30	ns
Sandcastle input					
	Sandcastle detector thresholds, Pin 5 phase-locked pulse (PL) on phase-locked pulse off blanking pulse ($\overline{CBB}$) on blanking pulse off	 2 4.5 	 	 3 5.5	 V V V V
Dual polarity sync buffer					
	After-hours sync ($\overline{AHS}$) pulse input Pin 11 threshold for $\overline{AHS}$ active threshold for $\overline{AHS}$ off	 1.0 	 	 2.0	 V V
	Picture-on (PO) input, Pin 10 threshold for PO active threshold for PO off	 1.0	 	 2.0 	 V V
	Sync output, Pin 12 $\overline{AHS}$ output with Pin 10 < 1V[5]; peak-to-peak value composite sync output with Pin 10 > 2V[5, 6]; peak-to-peak value output current	 	 0.7 0.7 	 1 3	 V V mA

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

At $T_A = 25°C$, $V_{CC} = 12V$, and with external components as shown in Figure 3, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Line reset and signal presence detectors					
	Schmitt trigger threshold on Pin 2 to inhibit line reset output at Pin 3 (syncs coincident)		6.2		V
	Schmitt trigger threshold on Pin 2 to permit line reset output at Pin 3 (syncs non coincident)		7.8		V
	Line reset output V_{OL} ($I_3 = 20\mu A$)			0.5	V
	Line reset output V_{OH} ($-I_3 = 100\mu A$)	2.4			V
	Signal presence Schmitt trigger threshold on Pin 2 below which the circuit accepts the input signal		6.0		V
	Signal presence Schmitt trigger threshold on Pin 2 above which the input signal is rejected		6.3		V
Crystal-controlled, phase-locked oscillator					
	C_1		27.5		pF
	C_0		6.8		pF
	C_L		20		pF
	Trimability (C_L increased to 30pF)	750			Hz
	Fundamental ESR			50	Ω

NOTES:

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at Pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two-level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375Mbit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into Pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centered on +2.3V. With the resistor connected to the supply rail, syncs are negative-going centered on +9.7V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

1 Signal Presence Time Constant — A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2 Line Reset Time Constant — A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see Pin 3).

3 Fast Line Reset Output (FLR) — Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase-locked loop.

4 Ground (0V)

5 Sandcastle Input ($\overline{PL}$ and $\overline{CBB}$) — This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. $\overline{PL}$ is obtained by slicing the waveform at 2.5V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase-locked loop. When the loop has locked up, the edges of $\overline{PL}$ are nominally 2μs before and 2μs after the leading edge of separated line syncs.

CBB is obtained by slicing the waveform at 5V, and is used to prevent the data slicer from being offset by the color burst.

6 6MHz Output (F6) — This is the output of the crystal oscillator (see Pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7 Phase Detector Time Constant — The integrating components for the phase detector of the phase-locked loop are connected between this pin and supply.

8, 9 6MHz Crystal — A 6MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on Pin 7, which forms part of the phase-locked loop.

10 Picture On Input (PO) — The PO signal, from the acquisition and control circuits SAA5040 series, is fed to this input and is used to determine whether the input video (Pin 16) or the AHS waveform (Pin 11) appears at Pin 12.

11 After Hours Sync ($\overline{AHS}$) — A composite sync waveform $\overline{AHS}$ is generated in the timing chain circuit SAA5020 and is used to synchronize the TV (see Pin 10).

12 Sync Output to TV — The input video of $\overline{AHS}$ is available at this output dependent on whether the PO signal is High or Low. In addition, either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13 Field Sync Output (FS) — A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14 Field Sync Separator Timing — A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15 Sync Separator Capacitor — A capacitor connected to this pin forms part of the adaptive sync separator.

16 Composite Video Input (VI) — The composite video is fed to this input via a coupling capacitor.

17 Supply Voltage (+12V)

18 Clock Output — The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 series via a series capacitor.

19 Data Output — The teletext data is sliced off the video waveform, squared up, and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 series via a series capacitor.

20 Clock Decoupling — A 1nF capacitor between Pin 20 and ground is required for clock decoupling.

21 Clock Regenerator Coil — A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see Pin 22).

22 Clock Pulse Timing Capacitor — Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to Pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 series via Pin 18.

23, 24 Peak Detector Capacitors — The teletext data is sliced with an automatic data slicer, having a slicing level at the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

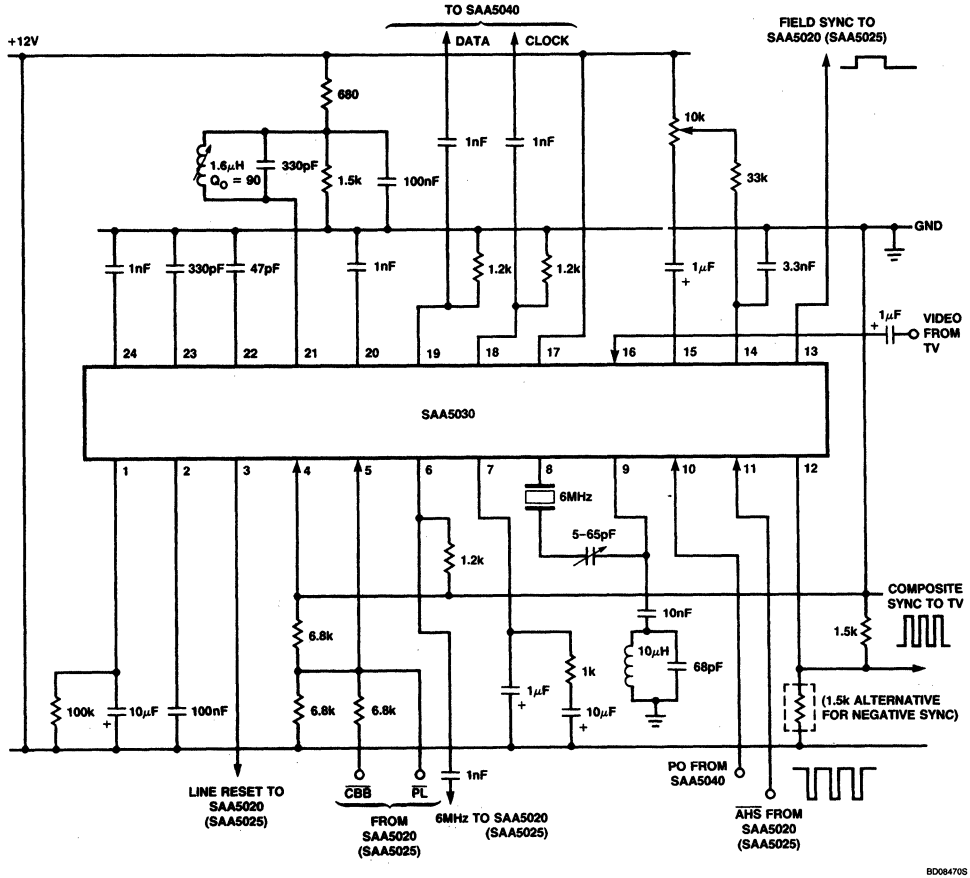

Figure 1. Peripheral Circuit

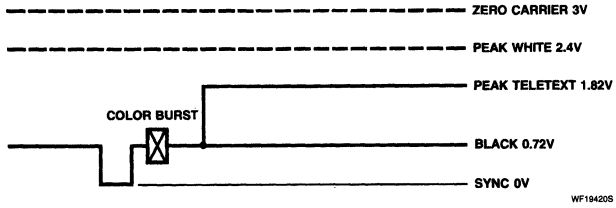

Figure 2. Part of Teletext Line, With Burst Showing Nominal Levels

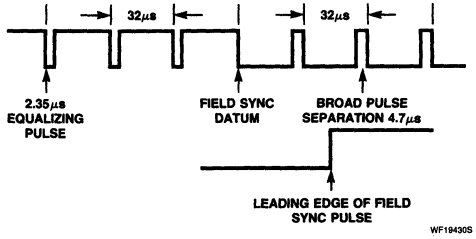

Figure 3. Details of Idealized Composite Sync Waveform

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Signetics

SAA5040
Teletext Acquisition and Control Circuit

Product Specification

Linear Products

DESCRIPTION

The SAA5040A, SAA5040B, SAA5040C, SAA5041, SAA5042 and SAA5043 form the SAA5040 series of MOS N-channel integrated circuits. They perform the control, data acquisition and data routing functions of the teletext system. The circuits differ in the on-screen display that is provided and in the decoding of the remote-control commands. The functions of the circuits are detailed in Tables 1, 2 and 3; throughout the remainder of the data, the SAA5040 is referred to when the complete series of circuits is being described.

The SAA5040 is a 28-lead device which receives serial teletext data and clock signals from the remote-control systems incorporating the SAA5012 or SAB3022, SAB3023 decoder circuits. The SAA5040 selects the required page information and feeds it in parallel form to the teletext page memory.

The SAA5040 works in conjunction with the SAA5020 timing chain and the SAA5050 series of character generators.

The circuit consists of two main sections.

a. Data acquisition section

The basic input to this section is the serial teletext data stream DATA from the SAA5030 video processor circuit. This data stream is clocked at a 6.9375MHz clock rate (F7) from the SAA5030. The incoming data stream is processed and sorted so that the page of data selected by the user is written as 7-bit parallel words into the system memory. Hamming and parity checks are performed on the incoming data to reduce errors. Provision is also made to process the control bits in the page header.

b. Control section

The basic input to this section is the 7-bit serial data ($\overline{DATA}$) from the remote control decoder circuit such as the SAA5012 or SAB3012. This is clocked by the DLIM signal.

The remote-control commands are decoded and the control functions are stored.

Full details of the remote-control commands used in the various SAA5040 series options are given in Tables 1, 2 and 3. The control section also writes data into the page memory independently of the data acquisition section. This gives an on-screen display of certain user-selected functions such as page number and program name.

The 3-State data and address outputs to the system memory are set to high impedance state if certain remote-control commands are received (e.g., view-data mode). This is to allow another circuit to access the memory using the same address and data lines. The address lines are also high impedance while the acquisition and control circuit is not writing into the memory.

Further information on the control of the complete teletext system is available.

The circuit is designed in accordance with the September 1976 Broadcast Teletext specification published by BBC/IBA/BREMA.

A typical circuit diagram of a teletext decoder is shown in Figure 5.

FEATURES

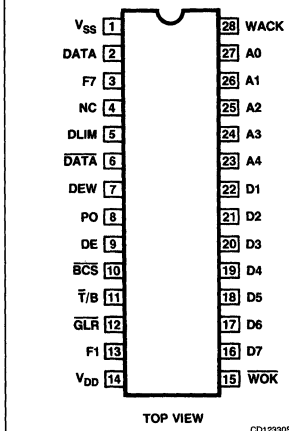
- **Converts serial data into parallel**
- **Performs error detection and correction**
- **Generates memory control signals**
- **Interfaces to the remote-control system**

APPLICATIONS

- **Teletext**
- **Data acquisition**

PIN CONFIGURATION

N Package



TOP VIEW

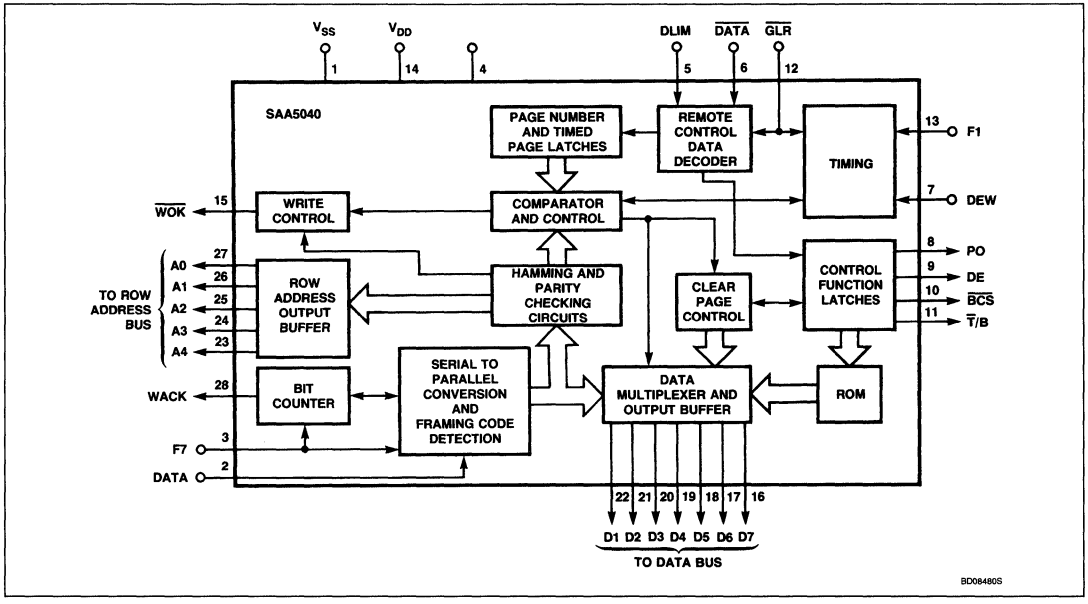
CD12330S

PIN NO.	SYMBOL	DESCRIPTION
1	V_{SS}	Ground
2	DATA	Data input from SAA5030
3	F7	Clock input from SAA5030
4	NC	Not connected
5	DLIM	Remote-control clock input
6	$\overline{DATA}$	Remote-control data input
7	DEW	Data entry window input
8	PO	Picture-on output
9	DE	Display enable output
10	$\overline{BCS}$	Big character select output
11	$\overline{T}$/B	Top/bottom output
12	$\overline{GLR}$	General line reset input
13	F1	1MHz clock input
14	V_{DD}	+5V supply
15	$\overline{WOK}$	Write O.K. output
16	D7	3-State outputs to data bus
17	D6	
18	D5	
19	D4	
20	D3	
21	D2	
22	D1	
23	A4	3-State outputs to row address bus
24	A3	
25	A2	
26	A1	
27	A0	
28	WACK	Write address clock output

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	−20°C to +70°C	SAA5040BN

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage (Pin 14)	−0.3 to 7.5	V
V_I	Input voltage (all inputs)	−0.3 to 7.5	V
V_{O8}	Output voltage (Pin 8)	−0.3 to 13.2	V
V_O	Output voltage (all other outputs)	−0.3 to 7.5	V
T_{STG}	Storage temperature range	−65 to +125	°C
T_A	Operating ambient temperature range	−20 to +70	°C

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DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Supply voltage (Pin 14)	4.5		5.5	V
I_{DD}	Supply current		80	120	mA
F7 DATA (Pin 2), F7 CLOCK (Pin 3)					
V_{IH}	Input voltage; High	3.5		5.5	V
V_{IL}	Input voltage; Low[1]			0.5	V
t_R	Rise time			30	ns
t_F	Fall time			30	ns
R_I	Input resistance (measured at 4V)	2		18	MΩ
C_I	Input capacitance			7	pF
F1 (Pin 13)					
V_{IH}	Input voltage; High	2.4		V_{DD}	V
V_{IL}	Input voltage; Low	0		0.6	V
t_R	Rise time			50	ns
t_F	Fall time			30	ns
C_I	Input capacitance			7	pF
I_{IR}	Input leakage current ($V_I = 0$ to 5.5V)			10	μA
DLIM (Pin 5), $\overline{\text{DATA}}$ (Pin 6), DEW (Pin 7), $\overline{\text{GLR}}$ (Pin 12)					
V_{IH}	Input voltage; High	2.0		V_{DD}	V
V_{IL}	Input voltage; Low	0		0.8	V
C_I	Input capacitance			7	pF
I_{IR}	Input leakage current ($V_I = 0$ to 5.5V)			10	μA
DE (Pin 9), $\overline{\text{BCS}}$ (Pin 10), $\overline{\text{T}}$/B (Pin 11) (with internal pull-up to V_{DD})					
V_{OL}	Output voltage; Low ($I_{OL} = 400\mu A$)	0		0.5	V
V_{OH}	Output voltage; High $-I_{OH} = 50\mu A$ for Pin 9 $-I_{OH} = 30\mu A$ for Pin 10 $-I_{OH} = 20\mu A$ for Pin 11	2.4 2.4 2.4		V_{DD} V_{DD} V_{DD}	V V V
t_R	Output voltage rise time			10	μs
t_F	Output voltage fall time			1	μs
C_O	Output capacitance			7	pF
$-I_O$	Output current with output in High state ($V_O = 0.5V$)	50		500	μA
PO (Pin 8) (with internal pull-up to V_{DD})					
V_{OL}	Output voltage; Low ($I_{OL} = 140\mu A$)	0		0.5	V
V_{OH}	Output voltage; High ($-I_{OH} = 50\mu A$)	2.4		V_{DD}	V
t_R, t_F	Output rise and fall time ($C_L = 40pF$)[3]			10	μs
C_O	Output capacitance			7	pF
$-I_O$	Output current with output in High state ($V_O = 0.5V$)	50		500	μA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
D1 to D7 (Pins 16 to 22) (3-State)					
V_{OL}	Output voltage; Low ($I_{OL} = 100\mu A$)	0		0.5	V
V_{OH}	Output voltage; High ($I_{OH} = -100\mu A$)	2.4		V_{DD}	V
t_R, t_F	Output rise and fall time ($C_L = 40pF$)[3]			100	ns
$\pm I_{OROFF}$	Output leakage current in 'OFF' state ($V_O = 0$ to 5.5V)			10	μA
C_O	Output capacitance			7	pF
$\overline{WOK}$ (Pin 15) (3-State with internal pull-up to V_{DD})					
V_{OL}	Output voltage; Low ($I_{OL} = 400\mu A$)	0		0.5	V
V_{OH}	Output voltage; High ($-I_{OH} = 200\mu A$)	2.4		V_{DD}	V
t_R t_F	Output voltage rise time Output voltage fall time } ($C_L = 80pF$)[3]			50 100	ns ns
$\pm I_{OROFF}$	Output current with 3-State 'OFF' ($V_O = 0.5V$)	80		500	μA
C_O	Output capacitance			7	pF
WACK (Pin 28) (3-State)					
V_{OL}	Output voltage; Low ($I_{OL} = 1.6mA$)	0		0.5	V
V_{OH}	Output voltage; High ($-I_{OH} = -100\mu A$)	2.4		V_{DD}	V
t_R t_F	Output voltage rise time Output voltage fall time } ($C_L = 40pF$)[3]			50 300	ns ns
$\pm I_{OROFF}$	Output leakage current in 'OFF' state ($V_O = 0$ to 5.5V)			10	μA
C_O	Output capacitance			7	pF
A0 to A2 (Pins 25 to 27) (3-State)					
V_{OL}	Output voltage; Low ($I_{OL} = 200\mu A$)	0		0.5	V
V_{OH}	Output voltage; High ($-I_{OH} = 200\mu A$)	2.4		V_{DD}	V
t_R, t_F	Output rise and fall time ($C_L = 90pF$)[3]			300	ns
$\pm I_{OROFF}$	Output leakage current in 'OFF' state ($V_O = 0$ to 5.5V)			10	μA
C_O	Output capacitance			7	pF
A3 and A4 (Pins 23 and 24) (3-State)					
V_{OL}	Output voltage; Low ($I_{OL} = 1.6mA$)	0		0.5	V
V_{OH}	Output voltage; High ($-I_{OH} = 200\mu A$)	2.4		V_{DD}	V
t_R, t_F	Output rise and fall time ($C_L = 40pF$)[3]			300	ns
$+I_{OROFF}$	Output leakage current in 'OFF' state ($V_O = 0$ to 5.5V)			10	μA
C_O	Output capacitance			7	pF
TIMING CHARACTERISTICS					
Teletext data and clock (F7 DATA + F7 CLOCK)[2] (Figure 1)					
TF_7	F7 Clock cycle time	144			ns
	F7 Clock duty cycle (High-to-Low)	30		70	%
t_{SU}	F7 Clock to data setup time		60		ns
t_{HOLD}	F7 Clock to data hold time		40		ns

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Control $\overline{DATA}$ and clock ($\overline{DATA}$ + DLIM)[3]					
t_{CH}	DLIM Clock High time[4]	6.5	8		μs
t_{CL}	DLIM Clock Low time	3.5	8	60	μs
t_{SU}	DLIM to DATA setup time	0	14		μs
t_{HOLD}	DLIM to DATA hold time	8	14		μs
Writing teletext data into memory during DEW (Figure 3)					
t_{WACK}	WACK cycle time	1150			ns
t_{AWW}	WACK rising edge to $\overline{WOK}$ falling edge	250		450	ns
t_{WRW}	WACK rising edge to $\overline{WOK}$ rising edge	150		310	ns
t_{WPD}	$\overline{WOK}$ pulse width	300			ns
t_{DW}	Data output setup time	330			ns
t_{DH}	Data output hold time	0			ns
t_{RAW}	Row address setup time before first $\overline{WOK}$	190			ns
t_{RWR}	Row address valid time after last $\overline{WOK}$	0			ns

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Writing header information into memory during TV line 40 (Figure 4)					
	This arrangement is a combined phasing of the SAA5040 and the SAA5020 and is therefore referred to F1 input. The first $\overline{WOK}$ is related to F1 No 14½ from the SAA5020				
TF_1	F1 clock cycle time	1000			ns
t_{WF}	Time from F1 to $\overline{WOK}$ falling edge	300		500	ns
t_{FW}	Time from F1 to $\overline{WOK}$ rising edge	0		120	ns
t_{DW}	Data output setup time	330			ns
t_{DH}	Data output hold time	0			ns

NOTES:
1. These inputs may be AC-coupled. Minimum rating is −0.3V, but the input may be taken more negative if AC-coupled.
2. Transition times measured between 0.5 and 3.5V levels. Delay times are measured from 1.5V level.
3. Transition times measured between 0.8 and 2.0V levels. Delay times are measured from 1.5V level.
4. There is no maximum DLIM cycle time, provided the DLIM duty cycle is such that $t_{CL\,MAX}$ requirement is not exceeded.

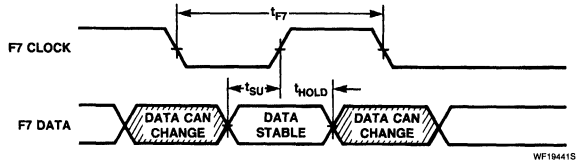


Figure 1. Teletext Data Timing

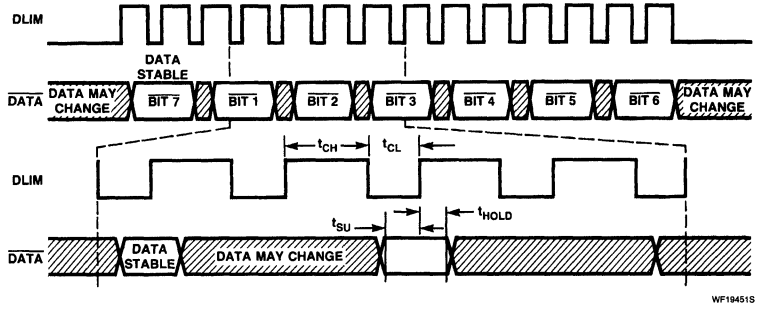


Figure 2. Remote Control Data Input Timing

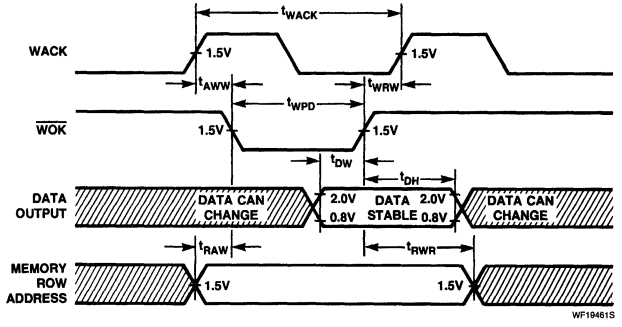
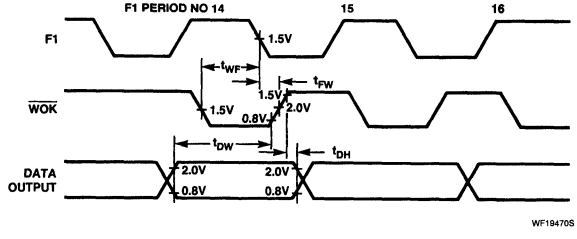


Figure 3. Writing Teletext Data Into Memory During DEW



NOTE:
Memory row address is valid from ≃ F1 period No 14 for complete line.

Figure 4. Writing Data Into Memory During TV Line 40

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APPLICATION DATA

The function is quoted against the corresponding pin number.

1 V_{SS} Ground — 0V.

2 DATA Data Input from SAA5030 — This input is a serial data stream of broadcast teletext data from the SAA5030 video processor, the data being at a rate of 6.9375MHz.

This input from the SAA5030 is AC-coupled with internal DC restoration of the signal levels.

3 F7 Clock Input from SAA5030 — This input is a 6.9375MHz clock from the SAA5030 video processor which is used to clock the teletext data acquisition circuitry. The positive edge of this clock is nominally at the center of each teletext data bit.

This input from the SAA5030 is AC-coupled with internal DC restoration of the signal levels.

5 DLIM Remote-Control Clock Input — This input from the remote-control receiver-decoder is used to clock remote-control data into the SAA5040. The positive-going edge of every second clock pulse is nominally in the center of each remote control data bit.

6 $\overline{\text{DATA}}$ Remote Control Data — This input is a 7-bit serial data stream from the remote-control receiver-decoder.

This data contains the teletext and viewdata remote-control user functions. The nominal data rate is 32μs/bit. The remote-control commands used in the SAA5040 series are shown in Tables 1, 2, and 3.

7 DEW Data Entry Window — This input from the SAA5020 Timing Chain defines the period during which received teletext data may be accepted by the SAA5040. This signal is also used to enable the five memory address outputs (Pins 23 to 27) and the 7-bit parallel data outputs (Pins 16 to 22).

8 PO Picture On — This output to the SAA5012, SAA5030 and SAA5050 circuits is a static level used for the selection of TV picture video 'on' or 'off'. The output is High for TV picture 'ON', Low for TV picture 'OFF'. The output has an internal pull-up to V_{DD}.

9 DE Display Enable — This output to the SAA5050 teletext character generator is used to enable the teletext display.

The output is High for display enabled, Low for display disabled.

The output is also forced to the Low state during the DEW and TV line 40 periods and when a teletext page is cleared.

The output has an internal pull-up to V_{DD}.

10 $\overline{\text{BCS}}$ Big Character Select — This output to the SAA5020 timing chain and to the SAA5050 character generator is used to select double height character format under user control. The output is High for normal height characters, Low for double height characters. It is also forced to the High state on page clear. The output has an internal pull-up to V_{DD}.

11 $\overline{\text{T}}$/B Top/Bottom — This output to the SAA5020 timing chain is used to select whether top or bottom half page is being viewed. The output is High for bottom half page and Low for top half page. It is also forced to the Low state on page clear. The output has an internal pull-up to V_{DD}.

12 $\overline{\text{GLR}}$ General Line Reset — This input from the SAA5020 timing chain is used as a reset signal for internal control and display counter.

13 F1 — This input is a 1MHz clock signal from the SAA5020 timing chain used to clock internal remote-control processing and encoding circuits.

14 V_{DD} +5V Supply — This is the power supply input to the circuit.

15 $\overline{\text{WOK}}$ Write O.K. — This 3-State output signal to the system memory is used to control the writing of valid data into the system memory. The signal is Low to write, and is in the high impedance state when viewdata is selected. The 3-State buffer is enabled at the same time as the data outputs (see below). An internal pull-up device prevents the output from floating into the Low state when the 3-State buffer is OFF.

16, 17, 18, 19, 20, 21, 22 D7 to D1, Data Outputs — These 3-State outputs are the 7-bit parallel data outputs to the system memory. The outputs are enabled at the following times:

a. During the data entry window (DEW) to write teletext data into the memory. The data rate is 867kB per second and is derived from the teletext data clock.

b. During TV line 40 for encoded status information about user commands (e.g., program number), to be written into the memory. This period is known as EDIL (encoded data insertion line). The data rate is 1MB per second and is derived from the 1MHz display clock F1.

c. When the page is cleared. In this case, the data output is forced to the space code (0100000) during the display period for one field. This data is held at the space code from either TV line 40 (if page clear is caused by user command), or the received teletext data line causing the clear function, until the start of the data entry window (DEW) of the next field.

23, 24, 25, 26, 27 A4 to A0 Memory Addresses — These 3-State outputs are the 5-bit row address to the page memory. This address specifies in which of 24 rows the teletext data is to be written. The outputs are enabled during the data entry period (DEW).

28 WACK Write Address Clock — This 3-State output is used to clock the memory address counter during the data entry period (DEW). The output is enabled only during this period. The positive-going edge of WACK is used to clock the address counter.

Table 1. Remote-Control Commands Used in the SAA5040A/SAA5040B/SAA5040C/SAA5043[8]

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$)[7]	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$)[7]
0	0	0	0	0	RESET[1]	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1	TV/ON Gives program display.	
0	0	1	0	0	STATUS Gives program display.	STATUS Program/header display[6]
0	0	1	0	1		HOLD Stops reception of teletext[9]
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display.	DISPLAY CANCEL[3]
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		TAPE Resets to small characters
0	1	1	0	1		
0	1	1	1	0		TIMED PAGE OFF
0	1	1	1	1		TIMED PAGE ON
1	0	0	0	0	PROGRAMS[2]	NUMBERS[4, 6] 1
1	0	0	0	1		2
1	0	0	1	0		3
1	0	0	1	1		4
1	0	1	0	0		5
1	0	1	0	1		6
1	0	1	1	0		7
1	0	1	1	1		8
1	1	0	0	0		9
1	1	0	0	1		0
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS TOP HALF PAGE
1	1	1	0	0		LARGE CHARACTERS BOTTOM HALF PAGE
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE[6]
1	1	1	1	1		TELETEXT/ON[5]

NOTES:

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.
2. Program names are displayed for 5s in a box at the top left of the screen in large characters. Program commands clear the page memory except in timed page mode.

   The following boxed information is displayed:

REMOTE-CONTROL COMMAND b_5	b_4	b_3	b_2	b_1	SAA5040A	SAA5040B	SAA5040C	SAA5043
1	0	0	0	0	BBC1		BBC1	Ch 1
1	0	0	0	1	BBC2		ITV	Ch 2
1	0	0	1	0	ITV		BBC2	Ch 3
1	0	0	1	1	4		BBC1	Ch 4
1	0	1	0	0	5		ITV	Ch 5
1	0	1	0	1	6	Gives no status box	VTR	Ch 6
1	0	1	1	0	7		BBC1	Ch 7
1	0	1	1	1	VCR		ITV	Ch 8
1	1	0	0	0	9		BBC2	Ch 9
1	1	0	0	1	10		BBC1	Ch 0
1	1	0	1	0	11		ITV	Ch 10
1	1	0	1	1	12		VTR	Ch 11

3. Display cancel removes the text and restores the television picture. The device then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives, the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required, using the teletext/on command.
4. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested, the page header turns green and the page numbers roll until the new page is captured.
5. The teletext/on command resets display cancel, hold, and superimpose modes.
6. Status, timed page on, timed page off, numbers, superimpose, and teletext/on commands all reset to top half page and produce a box around the header for 5s. This allows the header to be seen if the television picture is on (e.g. newsflash or display cancel modes).
7. In viewdata mode ($b_7 = b_6 = 1$) the device is disabled and teletext cannot be received. All 3-State outputs are high impedance.

8. Table 1 shows code required for functions specified. The device requires the inverse of these codes i.e., $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.
9. When hold node is selected, 'HOLD' is displayed in green at the top right of the screen.
10. A 'P' is displayed before the page number at the top left of the screen (e.g., P123).

Table 2. Remote-Control Commands Used in the SAA5041[9]

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$)[8]	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$)[8]
0	0	0	0	0		
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0	TIME Gives time display	STATUS Gives header and time display.[6]
0	0	1	0	1		TIMED PAGE On/off toggle function.
0	0	1	1	0		
0	0	1	1	1		
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		
0	1	1	0	1		
0	1	1	1	0		
0	1	1	1	1		TELETEXT RESET[1]
1	0	0	0	0		0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1	PROGRAMS[10]	NUMBERS[2, 7] 5
1	0	1	1	0		6
1	0	1	1	1		7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS Top/bottom toggle function
1	1	1	0	0		HOLD Stops reception of teletext – toggle function[3]
1	1	1	0	1		DISPLAY CANCEL[4]
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		NORMAL DISPLAY[5]

NOTES:

1. The teletext reset command clears the page memory, selects Page 100, goes to small characters, and resets hold, timed page, and display cancel modes.
2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested, the page header turns green and the page numbers roll until the new page is captured.
3. When hold mode is selected, 'HALT' is displayed in green at the top right of the screen.
4. Display cancel removes the text and restores the television picture. The SAA5041 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives, the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required, using the normal display command.
5. The normal display command resets display cancel, hold, and superimpose modes.
6. Status, timed page, numbers, hold, superimpose, and normal display commands all reset to top half page and produce a box around the header for five seconds. This allows the header to be seen even if the television picture is on (e.g., newsflash or display cancel modes).
7. An 'S' is displayed before the page number at the top left of the screen (e.g., S123).
8. In view data mode ($b_7 = b_6 = 1$) the SAA5041 is disabled and teletext cannot be received. All 3-State outputs are high impedance.
9. Table 2 shows code required for functions specified. The SAA5041 requires the inverse of these codes, i.e., b_7 to b_1. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.
10. Clear memory occurs except in timed page mode.

Table 3. Remote-Control Commands Used in the SAA5042[9]

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$)[8]	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$)[8]
0	0	0	0	0	RESET[1]	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0		STATUS Gives header and time display[6]
0	0	1	0	1		HOLD Stops reception of teletext-toggle function[3]
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display	
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		SMALL CHARACTERS
0	1	0	1	1		
0	1	1	0	0		LARGE CHARACTERS TOP HALF PAGE
0	1	1	0	1		LARGE CHARACTERS BOTTOM HALF PAGE
0	1	1	1	0		DISPLAY CANCEL/RECALL[4]
0	1	1	1	1		DISPLAY RECALL
1	0	0	0	0	PROGRAMS[10]	NUMBERS[2, 7] 0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1		5
1	0	1	1	0		6
1	0	1	1	1		7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		TIMED PAGE On/Off toggle function
1	1	0	1	1		CLEAR MEMORY
1	1	1	0	0		LONG TERM STORE/SMALL CHARACTERS
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		TELETEXT/ON[5]

NOTES:

1. Reset clears the page memory, sets page number to 100 and time code to 00.00, and resets timed page and display cancel modes.
2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested, the page header turns green and the page numbers roll until the new page is captured.
3. When hold mode is selected, 'STOP' is displayed in green at the top right of the screen.
4. Display cancel/recall removes the text and restores the television picture. The SAA5042 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives, the page number only is displayed in a box at the top left of the screen. The same command will then cause a normal page to be displayed, but will cancel a newsflash or subtitle page. Alternatively, text can then be recalled by using the teletext/on command.
5. The teletext/on command resets display cancel, hold, and superimpose modes.
6. Status, timed page, numbers, superimpose, and teletext/on commands all reset to top half page and produce a box around the header for five seconds. This allows the header to be seen even if the television picture is on (e.g., newsflash or display cancel modes).
7. A 'P' is displayed before the page number at the top left of the screen (e.g., S123).
8. In view data mode ($b_7 = b_6 = 1$) the SAA5042 is disabled and teletext cannot be received. All 3-State outputs are high impedance.
9. Table 3 shows code required for functions specified. The SAA5042 requires the inverse of these codes, i.e., b_7 to b_1. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.
10. Clear memory occurs except in timed page mode.

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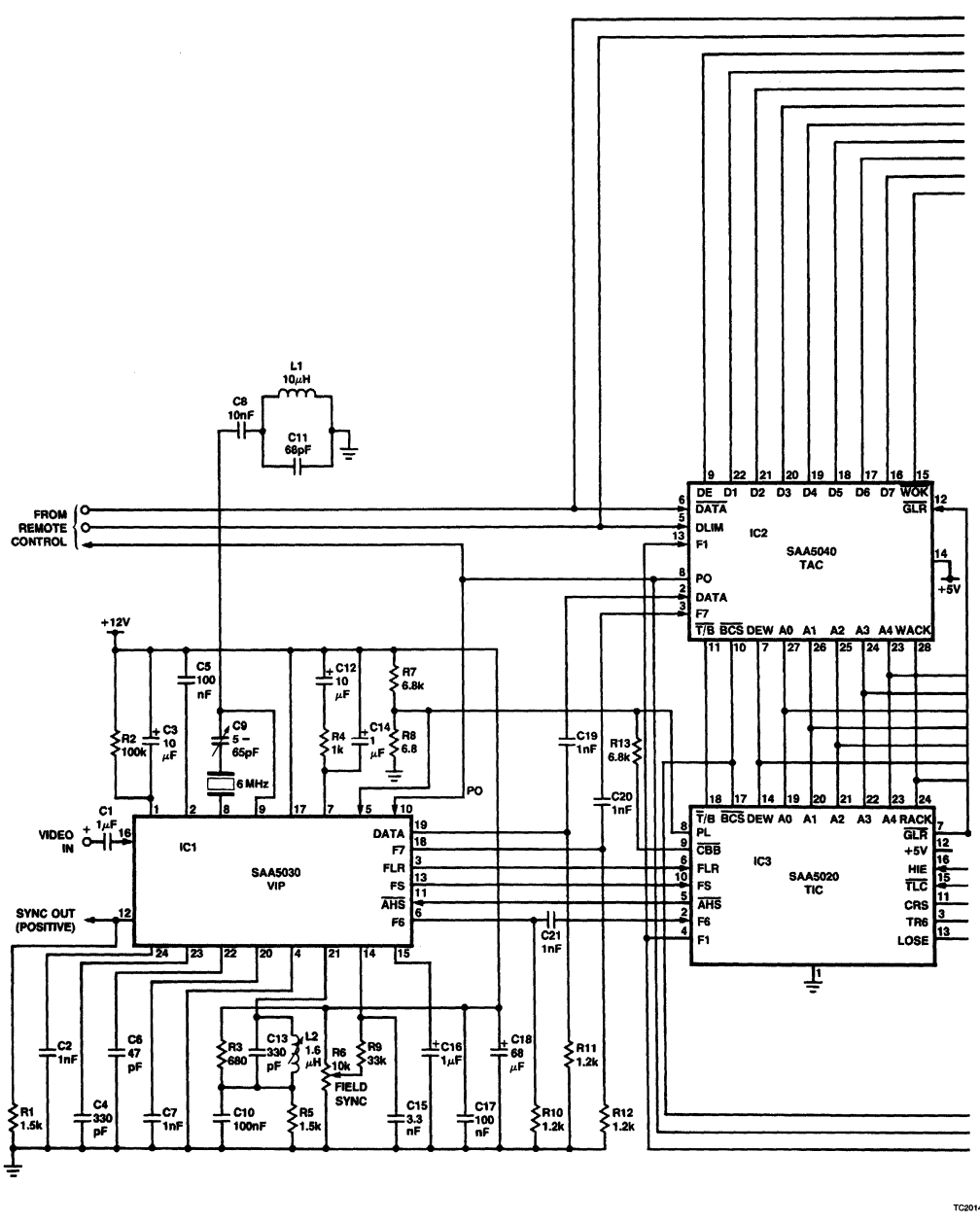


Figure 5. Typical Circuit Diagram of a Teletext Decoder

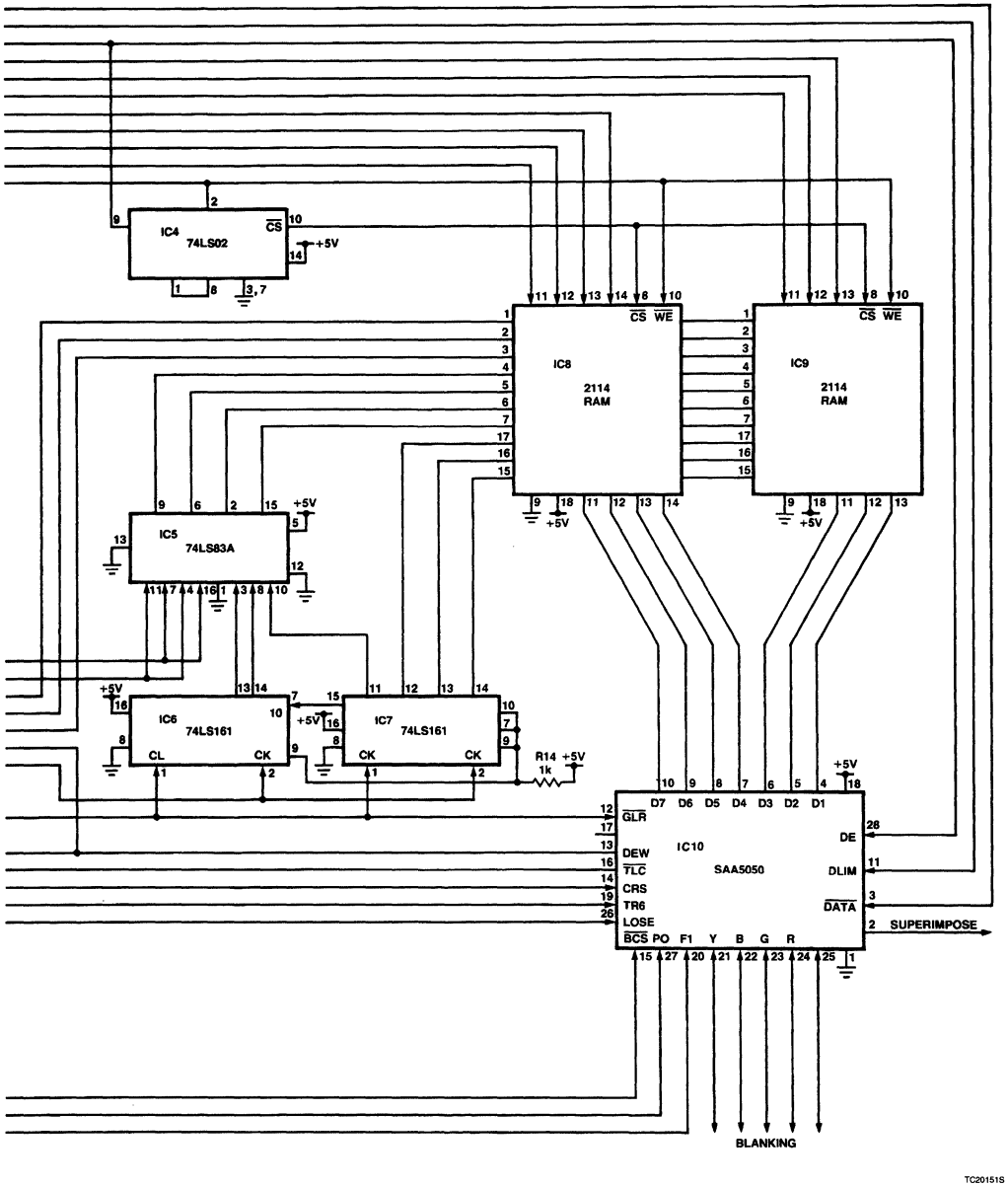


Figure 5. Typical Circuit Diagram of a Teletext Decoder (Continued)

13

Signetics

SAA5045
Gearing and Address Logic Array for USA Teletext

Product Specification

Linear Products

DESCRIPTION

The SAA5045 is a PCF0700 CMOS process gate array designed to interface the SAA5040B Teletext Acquisition Control (TAC) IC to the SAA5030 Video Processor (VIP) data output for modified UK standard 525-line Teletext. It also provides an address interface between SAA5040B, SAA5025D Teletext Timing Chain for USA 525-line system (USTIC) and the page memory RAM. The memory interface includes read/write control compatible with the geared 32 + 8 transmission system at 5.727272MHz data rate employed in the modified UK system.

FEATURES

- **Implements the gearing function, allowing 40 characters/row display**
- **Generates memory control signals**
- **Gate array-based implementation**

APPLICATION

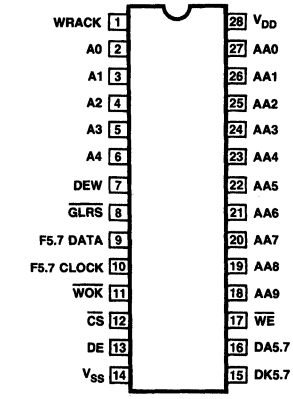
- **Teletext**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117D)	−20°C to +70°C	SAA5045N

PIN CONFIGURATION

N Package



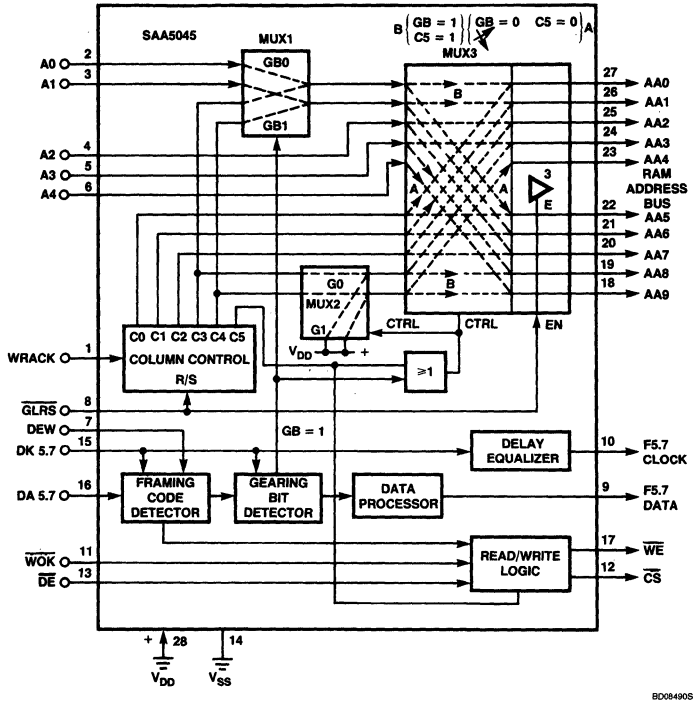
TOP VIEW

CD12340S

PIN NO.	SYMBOL	DESCRIPTION
1	WRACK	Input clock to column counter
2	A0	Row address system inputs
3	A1	
4	A2	
5	A3	
6	A4	
7	DEW	Data entry window input
8	$\overline{GLRS}$	General line reset starting output
9	F5.7 DATA	5.7MHz data output
10	F5.7 CLOCK	5.7MHz clock output
11	$\overline{WOK}$	Write enable input
12	$\overline{CS}$	Chip select output
13	DE	Display enable input
14	V_{SS}	Ground
15	DK5.7	5.7MHz data clock input
16	DA5.7	5.7MHz data input
17	$\overline{WE}$	Write enable output
18	AA9	Memory address outputs
19	AA8	
20	AA7	
21	AA6	
22	AA5	
23	AA4	
24	AA3	
25	AA2	
26	AA1	
27	AA0	
28	V_{DD}	Positive supply (+4.5V to +5.5V)

Gearing and Address Logic Array for USA Teletext SAA5045

BLOCK DIAGRAM



13

Gearing and Address Logic Array for USA Teletext — SAA5045

SYSTEM CONTENT

Functionally the chip contains two main sections which operate during the acquisition and display periods.

Gearing Control Section

The data from the SAA5030 (VIP) and data clock are processed to detect the presence of the gearing bit and convert the data for correct operation of the SAA5040B (TAC). Data and clock outputs to the TAC are internally compensated for processing delays, so that correct clocking-in of data is ensured.

Addressing Section

Column counters are included, which operate from the WACK (TAC) and RACK (USTIC) column clock signals during acquisition and display respectively.

Five row-address input circuits (pins A0 to A4) are provided for (TAC) and (USTIC) address outputs. These are multiplexed with the column address from the internal counters for correct mapping of the RAM via ten output address pins (AA0 to AA9). During acquisition, the multiplexer is controlled by the gearing bit detection to give correct assembly of the 40-character per row page structure.

The address output buffers are 3-State devices controlled by the line reset signal (Pin 8; $\overline{GLRS}$). During the horizontal flyback period, the address pins are 3-State to allow alternative addressing for customized applications.

Read/Write Control to RAM

An internal counter prevents overwriting if more than 32 character WOK pulses are received from TAC due to poor transmission conditions. Two control outputs, one for read/write ($\overline{WE}$) and the other for chip select ($\overline{CS}$), are provided to eliminate conflicts on the input/output RAM bus.

Framing Code Detection

When a valid data line is received and the framing code is detected in the gearing section, then flag pulses (pair of pulses) are available at output $\overline{WE}$, before the $\overline{CS}$ output is driven Low for normal writing into the RAM. If a framing-code-present signal is required, it can be obtained by gating $\overline{WE}$ and $\overline{CS}$ outputs such that an output from the $\overline{WE}$, when output $\overline{CS}$ is High indicates the detection of a framing code; N.B., each framing code produces a pair of pulses.

RAM ADDRESS CONTROL

The Block Diagram shows that the ten RAM address outputs are controlled by a multiplexer (MUX3) which interchanges the two groups of five address lines when a gearing bit equal to logic "1" is received during data input. During display, MUX3 is switched by Bit 6 of the column counter. MUX1, which is switched by the gearing bit, controls stepping of the row address when fill-in rows are received. MUX2 is switched by either the gearing bit or Bit 6 of the column counter to access the part of RAM storing the last eight bytes of each row of data.

The mapping of the 1024-byte RAM is shown in Figure 1. Area "A" stores data corresponding to the left-hand side (32 bytes wide) of the display and area "B" stores the remainder for the right-hand side.

Access to the RAM for custom operations can be made during the time that $\overline{GLRS}$ (Pin 8) is Low, which causes all ten address buffers to be in the open state. It should be noted that $\overline{GLRS}$ Low also resets the column counters and the gearing-bit detection system to logic "0". This normally occurs during the horizontal interval (between 5 and 8μs) after the horizontal sync pulse falling edge.

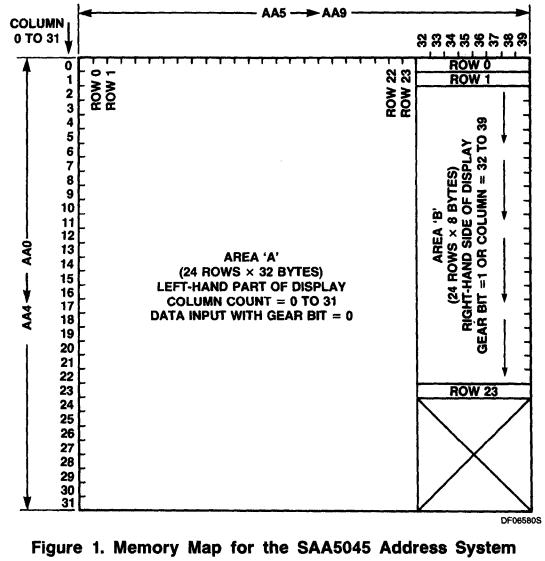


Figure 1. Memory Map for the SAA5045 Address System

Gearing and Address Logic Array for USA Teletext — SAA5045

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1 WRACK Input Clock to Column Counter — Input clock to column counter during data input or display; WACK from SAA5040B (TAC) or RACK from SAA5025D (USTIC).

2 to 6 A0 to A4 Row Address System Inputs — Inputs to row address system during data input or display. Row address numbers greater than 0 to 23 disable writing to the RAM during input.

7 DEW Data Entry Window Input — Data entry window input enables gearing bit detection and data processing part of system.

8 $\overline{\text{GLRS}}$ General Line Reset Starting Output — Input from the SAA5025D is a negative reset pulse at line rate for column counters and gearing system. When this input is Low, it opens 3-State address buffers.

9 F5.7 DATA 5.7MHz Data Output — Data output at 5.7MHz rate to SAA5040B (TAC) during the data acquisition period when DEW is High.

10 F5.7 CLOCK 5.7MHz Clock Output — Data clock output at 5.7MHz rate to SAA5040B (TAC), synchronized to data at Pin 9 (F5.7 DATA).

11 $\overline{\text{WOK}}$ Write Enable Input — Write enable input from SAA5040B (TAC) during data acquisition, when correct data is received, for RAM write/read control (via output $\overline{\text{WE}}$; Pin 17).

12 $\overline{\text{CS}}$ Chip Select Output — Output to drive the RAM chip enable during data input and display periods controlled by the display enable output (DE) and write O.K. ($\overline{\text{WOK}}$) output of the SAA5040B (TAC), avoiding input/output bus conflict.

13 DE Display Enable Input — Display enable input from SAA5040B (TAC) to control $\overline{\text{CS}}$.

14 V_{SS} — Ground.

15 DK5.7 5.7MHz Data Clock Input — Data clock input at 5.7MHz rate from the SAA5030 (VIP); this pin is capacitively-coupled with a DC restoring diode and is externally connected to V_{SS}.

16 DA5.7 5.7MHz Data Input — Data input at 5.7MHz rate from SAA5030 (VIP); this pin is capacitively-coupled with a DC restoring diode and is externally connected to V_{SS}.

17 $\overline{\text{WE}}$ Write Enable Output — Write enable output to control RAM write/read. This output is the gated and delay version of the $\overline{\text{WOK}}$ from the SAA5040B, but limited to 32. A pair of pulses which are possible before the WACK count is equal to 32. A pair of pulses on this output precedes the $\overline{\text{WOK}}$ pulses, while $\overline{\text{CS}}$ is High whenever a framing code is detected.

18 to 27 AA9 to AA0 Memory Address Outputs — Memory address outputs; 3-State buffered outputs, open when $\overline{\text{GLRS}}$ is Low for auxiliary access to the RAM address bus if required.

N.B.: AA9 and AA8 are simultaneously High whenever a gear bit with logic "1" is received during DEW is High. This enables detection of gearing bit reception, following $\overline{\text{GLRS}}$ reset on each line, which always resets AA0 to AA9 to logic "0".

28 V_{DD} Positive Supply (4.5V to 5.5V)

NOTE:

Input pins other than 15 and 16 have internal 15kΩ pull-up resistors for compatibility with SAA5025D and SAA5040B output signal ranges. Pins 15 and 16 are CMOS inputs for DC restored drive from the SAA5030 (VIP) clock and data output signals.

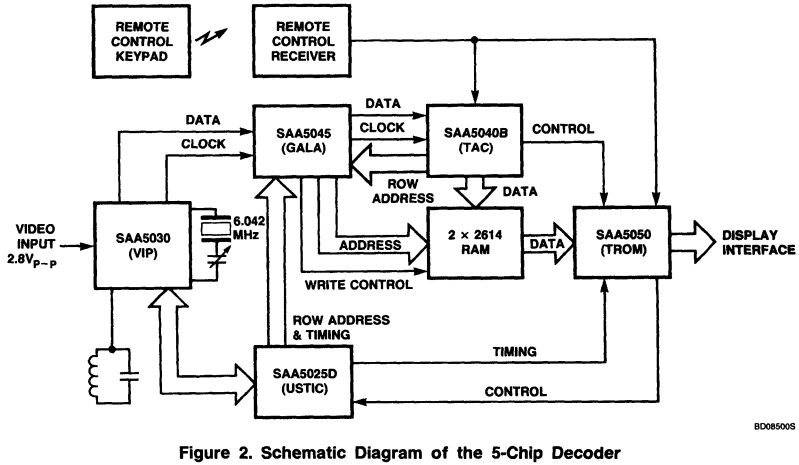


Figure 2. Schematic Diagram of the 5-Chip Decoder

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SAA5050/55
Teletext Character Generator

Product Specification

DESCRIPTION

The SAA5050 series of MOS N-channel integrated circuits provides the video drive signals to the television receiver necessary to produce the teletext/viewdata display.

The SAA5050 is a 28-pin device which incorporates a fast access character generator ROM (4.3kbits), the logic decoding for all the teletext control characters and decoding for some of the remote control functions. The circuit generates 96 alphanumeric and 64 graphic characters. In addition there are 32 control characters which determine the nature of the display.

The SAA5050 is suitable for direct connection to the SAA5010, SAA5012, SAA5020 and SAA5040 Series integrated circuits.

The basic input to the SAA5050 is the character data from the teletext page memory. This is a 7-bit code. Each character code defines a dot matrix pattern. The character period is 1μs and the character dot rate is 6MHz. The timings are derived from the two external input clocks F1 (1MHz) and TR6 (6MHz) which are amplified and re-synchronized internally. Each character rectangle is 6 dots wide by 10 TV lines high. One dot space is left between adjacent characters, and there is one line space left between rows. Alphanumeric characters are generated on a 5 $\times$ 9 matrix, allowing space for descending characters. Each of the 64 graphic characters is decoded to form a 2 $\times$ 3 block arrangement which occupies the complete 6 $\times$ 10 dot matrix (Figure 7). Graphics characters may be either contiguous or separated (Figure 8). The alphanumeric characters are character rounded, i.e, a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix.

The character video output signals comprise a monochrome signal and RGB signals for a color receiver. A blanking output signal is provided to blank out the television video signal under the control of the PO and DE inputs and the box control characters (see Table 3).

The monochrome data signal can be used to inlay characters into the television video. The use of the 32 control characters provides information on the nature of the display, e.g., color. These are also used to provide other facilities such as 'concealed display' and flashing words, etc. The full character set is given in Table 1.

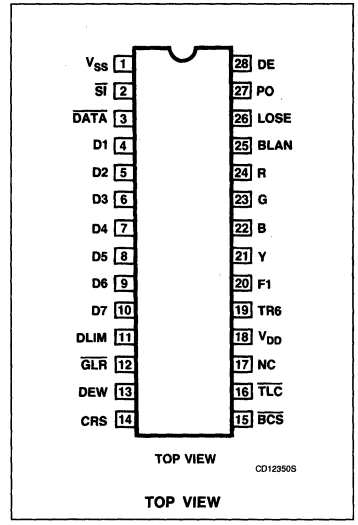
FEATURES

- **On-chip character ROM**
- **Contains 'character rounding' facility**
- **Interprets remote control commands**
- **Video output consists of R, G, B and Y open-collector**
- **Provides a 'Blanking' output**
- **Provides a 'Superimpose' output for use in 'Mix-mode' type displays**

APPLICATIONS

- **Teletext**
- **Videotex**
- **Low cost character generator**
- **Display systems with windowing, boxing, and text overlay capabilities**
- **Telecaptioning**

PIN CONFIGURATION

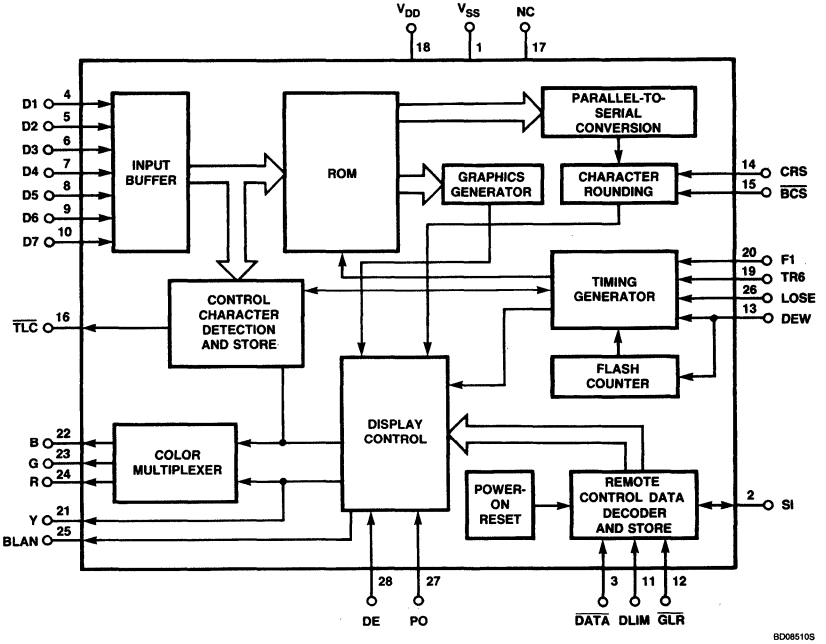


TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	-20°C to +70°C	SAA5050N
28-Pin Plastic DIP (SOT-117)	-20°C to +70°C	SAA5055N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
Voltages (with respect to Pin 1)			
V_{DD}	Supply voltage (Pin 18)	−0.3 to 7.5	V
V_I	Input voltages (all inputs + input/output)	−0.3 to 7.5	V
V_{O16} V_O	Output voltage (Pin 16) (all other output s)	−0.3 to 75 −0.3 to 14.0	V V
Temperature			
T_{STG}	Storage temperature range	−20 to +125	°C
T_A	Operating ambient temperature range	−20 to +70	°C

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DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{DD}	Supply voltage (Pin 18)	4.5		5.5	V
I_{DD}	Supply current		85	160	mA
Inputs					
Character data D1 to D7 (Pins 4 to 10)					
V_{IH}	Input voltage; High	2.65		V_{DD}	V
V_{IL}	Input voltage; Low	0		0.6	V
Clock inputs F1 (Pin 20) TR6 (Pin 19)					
V_{IH}	Input voltage; High	2.65		V_{DD}	V
V_{IL}	Input voltage; Low	0		0.6	V
Logic inputs $\overline{DATA}$ (Pin 3), DLIM (Pin 11), $\overline{GLR}$ (Pin 12) DEW (Pin 13), CRS (Pin 14), $\overline{BCS}$ (Pin 15), LOSE (Pin 26), PO (Pin 27), DE (Pin 28)					
V_{IH}	Input voltage; High	2		V_{DD}	V
V_{IL}	Input voltage; Low	0		0.8	V
All inputs					
I_{IR}	Input leakage current ($V_I = 5.5V$)			10	μA
C_I	Input capacitance			7	pF
Outputs					
Character video outputs + blanking output (open-drain)[3] B– (Pin 22), G– (Pin 23), R– (Pin 24), Y– (Pin 21), blanking (Pin 25)					
V_{OL}	Output voltage; Low ($I_{OL} = 2mA$)			0.5	V
V_{OL}	Output voltage; Low ($I_{OL} = 4mA$)			1.0	V
V_{OL}	Output voltage; Low ($I_{OL} = 6mA$)			2.0	V
V_{OH}	Output voltage; High[5]	V_{DD}		13.2	V
C_L	Output load capacitance			15	pF
t_F	Output fall time[1]			30	ns
Δt_F	Variation of fall time between any outputs[1]	0		20	ns
$\overline{TLC}$ (Pin 16)					
V_{OL}	Output voltage; Low ($I_{OL} = 100\mu A$)	0		0.5	V
V_{OH}	Output voltage; High ($-I_{OH} = 100\mu A$)	2.4		V_{DD}	V
C_L	Output load capacitance			30	pF
t_R	Output rise time Measured between 0.8V and 2.0V levels			1.0	μs
t_F	Output fall time Measured between 0.8V and 2.0V levels			1.0	μs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Input/output					
$\overline{SI}$ (Pin 2) (open-drain)					
V_{IH}	Input voltage; High	2.0		6.5	V
V_{IL}	Input voltage; Low	0		0.8	V
I_{IR}	Input leakage current ($V_I = 5.5V$)			10	μA
C_I	Input capacitance			7	pF
V_{OL}	Output voltage; Low ($I_{OL} = 0.4mA$)	0		0.5	V
V_{OL}	Output voltage; Low ($I_{OL} = 1.3mA$)	0		1.0	V
C_L	Output load capacitance			45	pF
V_{OH}	Output voltage; High state[2]			6.5	V
Character data timing (Figure 2)					
t_D	TR6 rising edge to F1 falling edge	6		60	ns
f_{TR6}	TR6 frequency		6		MHz
	TR6 mark/space ratio	40:60		60:40	
f_{F1}	F1 frequency		1		MHz
	F1 mark/space ratio	40:60		60:40	
t_{CDS}	Data setup time	80			ns
t_{CDH}	Data hold time	100			ns
t_{CDG} t_{CDA}	Delay time — character in/ character data at outputs { Graphics / Alphanumerics		2.6 2.767		μs μs
Display period timing (Figure 3)					
t_{LDH}	F1 falling edge to LOSE rising edge	0		250	ns
t_{LDL}	F1 falling edge to LOSE falling edge	0		250	ns
t_{DON}	LOSE rising edge to 'Display on'		2.6		μs
t_{DOFF}	LOSE falling edge to 'Display off'		2.6		μs
t_{DP}	'Display period'		40		μs
Line rate timing (Figure 4)					
t_{DGL}	F1 rising edge to GLR falling edge	0		200	ns
t_{DGH}	F1 rising edge to GLR rising edge	0		200	ns
t_{GLP}	GLR Low time		1		μs
t_{GLR}	Line start* to GLR falling edge		5		μs
t_{LSL}	Line start* to LOSE rising edge		14.5		μs
t_{LLS}	LOSE falling edge to Line start*		9.5		μs
t_{LNP}	Line period		64		μs
t_{LHP}	LOSE High time		40		μs

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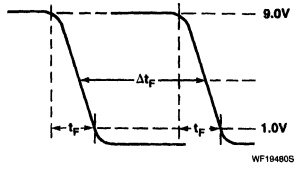
DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Remote data input timing (Figure 6) Assuming F1 period = 1μs and GLR period = 64μs					
t_{CH}	DLIM clock High time[4]	6.5	8		μs
t_{CL}	DLIM clock Low time	3.5	8	60	μs
t_{DS}	DATA to DLIM setup time	0	14		μs
t_{DH}	DLIM to $\overline{DATA}$ hold time	8	14		μs

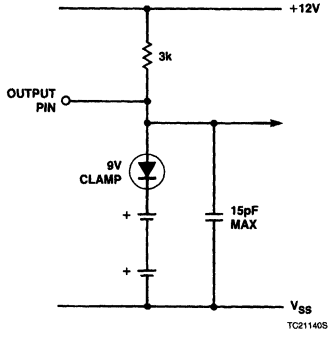
NOTES:

* Taken as falling edge of 'line sync' pulse.

1. Fall time, t_F and Δt_F, are defined as shown and are measured using the circuit shown below:
   t_F is measured between the 9V and 1V levels.
   Δt_F is the maximum time difference between outputs.



2. Recommended pull-up resister for $\overline{SI}$ is 18kΩ.
3. The R, G, B, Y, and blanking outputs are protected against short circuit to supply rails.
4. There is no maximum DLIM cycle time, provided the DLIM duty cycle is such that the t_{CL} max requirement is not exceeded.
5. With maximum pull-up voltage applied to R, G, B, and BLAN outputs the leakage current will not exceed 20μA with the outputs in the off state.



SPECIAL FEATURES

Flash Oscillator

The circuit generates a 0.75Hz signal with a 3:1 on/off ratio to provide the flashing character facility.

Power-On Reset

When the supply voltage is switched on, the character generator will reset to TV, conceal, and not superimpose modes.

Character Rounding

The character rounding function is different for the small and double height characters. In both cases the ROM is accessed twice during the character period of 1μs. The dot information of two rows is then compared to detect the presence of any diagonal in the character matrix and to determine the positioning of the character rounding half dots.

For small characters, rounding is always referenced in the same direction (i.e., row before in even fields and row after in odd fields as determined by the CRS signal).

For double height characters, rounding is always referenced alternately up and down, changing every line using an internally-generated signal. (The CRS signal is '0' for the odd field and '1' for the even field of an interlaced TV picture).

Graphics Decoder

The 64 graphic characters are decoded directly from the character data inputs and appear on a 2 × 3 matrix. Figure 7 gives details of the graphics decoding.

APPLICATION DATA

The function is quoted against the corresponding pin numbers.

1 V_{SS} Ground — 0V.

2 $\overline{SI}$ Superimpose — This is a dual purpose input/output pin. The output is an open drain transistor (capable of sinking current to V_{SS}), which is in the conducting state when superimpose mode is selected. This allows contrast reduction of the TV picture in superimpose mode, if required. If the pin is held low, the internal 'TV mode' flip-flop is held in the 'text' state. This is for VDU applications when the remote control is not used.

3 $\overline{DATA}$ Remote Control Data — This input accepts a 7-bit serial data stream from the remote control decoder. This data contains the teletext and viewdata remote control functions. The nominal data rate is 32μs/bit. The command codes used in the SAA5050 are shown in Table 2.

4, 5, 6, 7, 8, 9, 10 D1 to D7 Character Data — These inputs accept a 7-bit parallel data code from the page memory. This data selects the alphanumeric characters, the graphics characters and the control characters. The alphanumeric addresses are ROM column addresses, the graphics and control data are decoded internally.

11 DLIM — This input receives a clock signal from the remote control decoder and this signal is used to clock remote control data into the SAA5050. The positive-going edge of every second clock pulse is nominally in the center of each remote control data bit (Figure 6).

12 GLR General Line Reset — This input signal from the SAA5020 Timing Chain is required for internal synchronization of remote control data signals.

13 DEW Data Entry Window — This input signal from the SAA5020 Timing Chain is required to reset the internal ROM row address counter prior to the display period. It is also used internally to derive the 'flash' period.

14 CRS Character Rounding Select — This input signal from the SAA5020 Timing Chain is required for correct character rounding of displayed characters (normal height characters only).

15 $\overline{BCS}$ Big Character Select — This input from the SAA5040 Teletext Acquisition and Control device allows selection of large characters by remote control.

16 $\overline{TLC}$ Transmitted Large Characters — This output to the SAA5020 Timing Chain enables double height characters to be displayed as a result of control characters stored in the page memory.

18 V_{DD} +5V Supply — This is the power supply input to the circuit.

19 TR6 — This input is a 6MHz signal from the SAA5020 Timing Chain used as a character dot rate clock.

20 F1 — This input is a 1MHz equal mark/space ratio signal from the SAA5020 Timing Chain. It is used to latch the 7-bit parallel character data into the input latches. It is also used to synchronize an internal divide-by-6 counter. The F1 signal is internally synchronized with TR6.

21 Y Output — This is a video output signal which is active in the high state containing character dot information for TV display. The output is an open drain transistor capable of sinking current to V_{SS}.

22, 23, 24 B, G, R Outputs — These are the Blue, Green and Red Character video outputs to the TV display circuits. They are active high and contain both character and background color information. The outputs are open drain transistors capable of sinking current to V_{SS}.

25 BLAN Blanking — This active high output signal provides TV picture video blanking. It is active for the duration of a box when Picture On and Display Enable are high. It is also activated permanently for normal teletext display when no TV picture is required (PO low). The output is an open drain transistor capable of sinking current to V_{SS}. Full details are given in Table 3.

26 LOSE Load Output Shift Register Enable — This input signal from the SAA5020 Timing Chain resets the internal control character flip-flops prior to the start of each display line. It also defines the character display period.

27 PO Picture On — This input signal from the SAA5040 Teletext Acquisition and Control device is used to control the character video and blanking outputs. When PO is high, only text in boxes is displayed unless in superimpose mode. The input is high for TV picture video on, low for picture off (see Table 3).

28 DE Display Enable — This input signal from the SAA5040 Teletext Acquisition and Control device is used to enable the teletext display. The input is high for teletext display enabled. Low for display cancelled (see Table 3).

13

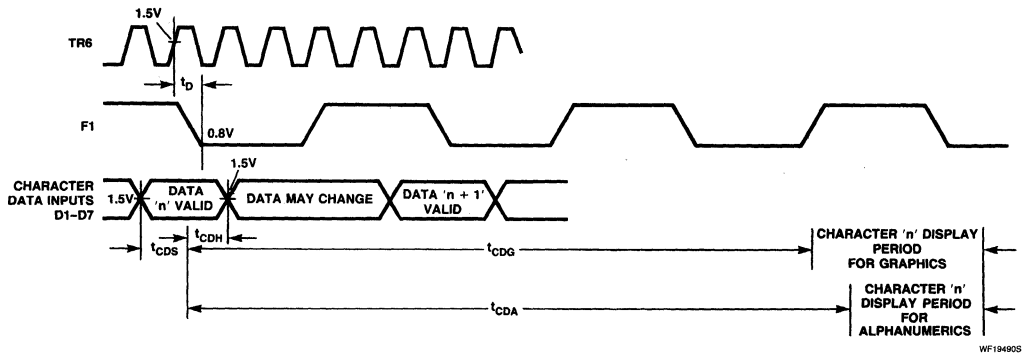


Figure 2. Character Data Timing (for Typical 40-Character Display)

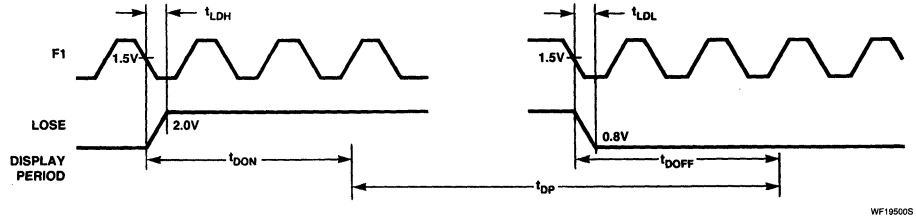
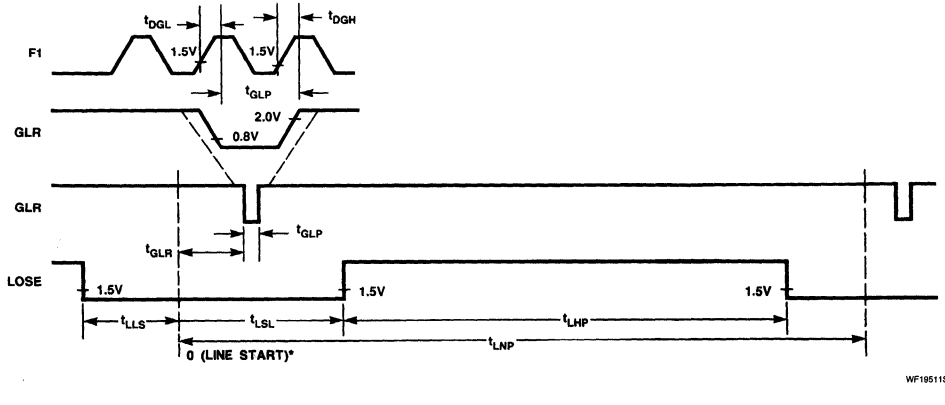


Figure 3. Character Period Timing (for Typical 40-Character Display)



NOTE:
*Taken as falling edge of line sync pulse.

Figure 4. Line Rate Clocks (for Line Period of 64μs)

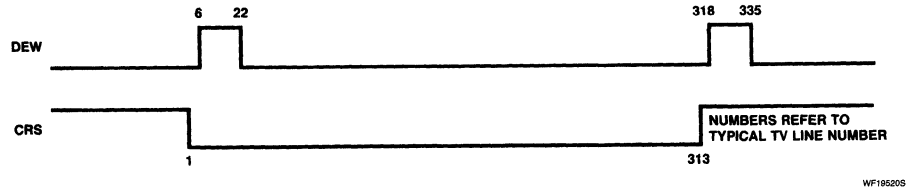


Figure 5. Field Rate Clocks (for Field Period of 20ms, 312½ Lines per Field)

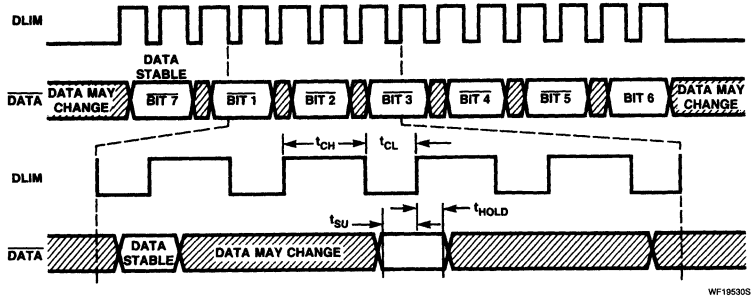
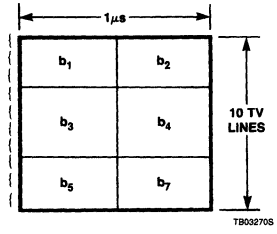


Figure 6. Remote Control Input Timing



NOTES:
Each cell is illuminated if the particular 'bit' (b_1, b_2, b_3, b_4, b_5, or b_7) is a '1'.
For graphics characters b_6 is always a '1' (see Table 1).

Figure 7. Graphics Character

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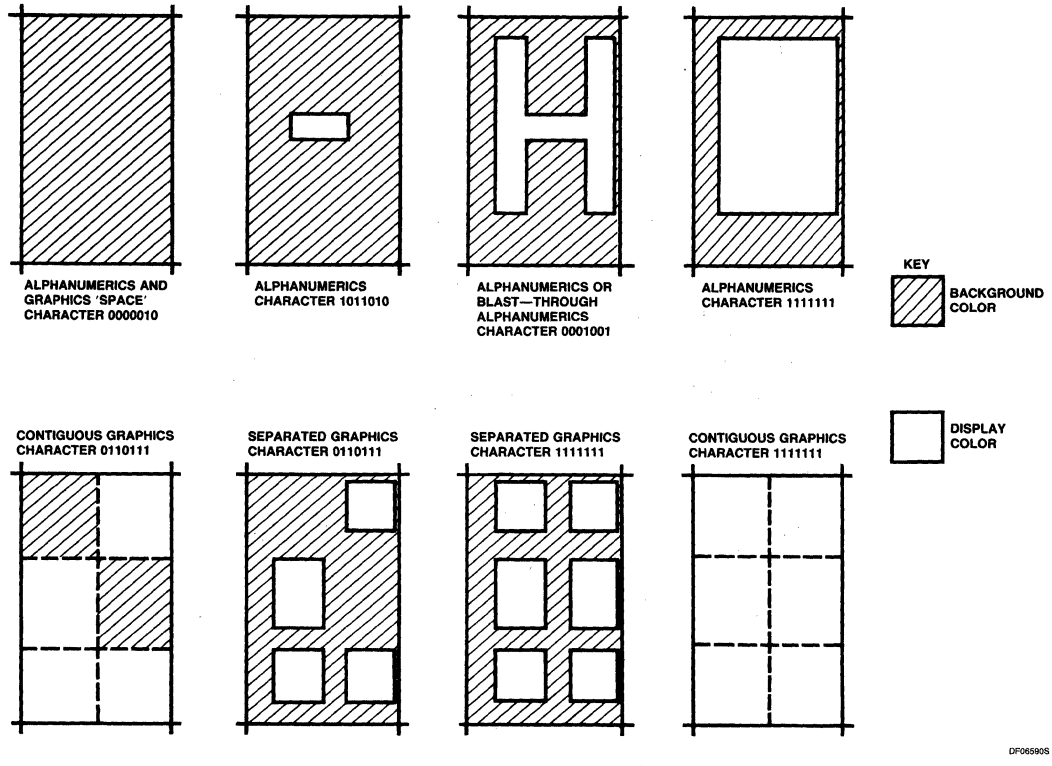

Figure 8. Character Format

Table 1. Character Data Input Decoding

Bits b_7 b_6 b_5 / Col					0_0	0_1	1_0		0_1		1_0	1_1	1_0		1_1	
b_4	b_3	b_2	b_1	Row	0	1	2	2a	3	3a	4	5	6	6a	7	7a
0	0	0	0	0	NUL*	DLE*			0		@	P	–		p	
0	0	0	1	1	Alpha Red	Graphics Red	!		1		A	Q	a		q	
0	0	1	0	2	Alpha Green	Graphics Green	"		2		B	R	b		r	
0	0	1	1	3	Alpha Yellow	Graphics Yellow	£		3		C	S	c		s	
0	1	0	0	4	Alpha Blue	Graphics Blue	$		4		D	T	d		t	
0	1	0	1	5	Alpha Magenta	Graphics Magenta	%		5		E	U	e		u	
0	1	1	0	6	Alpha Cyan	Graphics Cyan	&		6		F	V	f		v	
0	1	1	1	7	Alpha White**	Graphics White	'		7		G	W	g		w	
1	0	0	0	8	Flash	Conceal Display	(		8		H	X	h		x	
1	0	0	1	9	Steady**	Contiguous Graphics**	)		9		I	Y	i		y	
1	0	1	0	10	End Box**	Separated Graphics	*		:		J	Z	j		z	
1	0	1	1	11	Start Box	ESC*	+		;		K	←	k		¼	
1	1	0	0	12	Normal Height**	Black Background**	,		<		L	½	l		‖	
1	1	0	1	13	Double Height	New Background	–		=		M	→	m		¾	
1	1	1	0	14	SO*	Hold Graphics	.		>		N	↑	n		÷	
1	1	1	1	15	SI*	Release Graphics**	/		?		O	#	o		■	

TB03500S

NOTES:
Control characters shown in columns 0 and 1 are normally displayed as spaces.
The SAA5050 character set is shown as example. Details of character sets are given in Figures 9 and 10.
* These control characters are reserved for compatability with other data codes.
** These control characters are presumed before each row begins.
Codes may be referred to by their column and row, e.g., 2/5 refers to %.

Character rectangle
Black represents display color.
White represents background.

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Table 2. Remote Control Command Codes Used in the SAA5050

CODE b_7	b_6	b_5	b_4	b_3	b_2	b_1	COMMAND	FUNCTION
0	X	X	X	X	X	X	'TV' mode	Allows text on top row of display only
1	X	X	X	X	X	X	'Text' mode	Allows text throughout display period
1	0	1	1	1	1	0	Superimpose	Sets Superimpose mode
1	0	1	1	1	1	1	Teletext	Resets Superimpose mode
0	X	X	X	X	X	X	'TV' mode	Resets Superimpose mode
1	1	X	X	X	X	X	Viewdata mode	Resets Superimpose mode
1	X	0	0	1	1	0	Reveal	Reveals for time-out[3]
1	X	0	1	0	1	1	Reveal set	Sets Reveal mode[3]
Any command apart from reveal set								Resets Reveal mode[3]

NOTES:
X = Don't care.
1. When the power is applied, the SAA5050 is set into the 'TV' mode and reset out of Superimpose and Reveal modes.
2. 'Text' mode is selected when $\overline{SI}$ (Pin 2) is held low.
3. Reveal mode allows display of text previously concealed by 'conceal display' control characters.

Table 3. Conditions Affecting Display[3]

INPUTS		CONTROL DATA		OUTPUTS	
Picture On (PO)	Display Enable (DE)	Superimpose Mode	Box	Text Display Enabled (i.e., R, G, B, Y outputs)	Blanking
(a) 1	0	1 or 0	1 or 0	0	0
(b) 0	1	1 or 0	1 or 0	1	1
(c) 0	0	1 or 0	1 or 0	0[2]	1
(d) 1	1	0	0	0	0
(e) 1	1	1	0	1	0
(f) 1	1	1	1	1	1
(g) 1	1	0	1	1	1

NOTES:
1. For TV mode (Picture On = '1', Superimpose mode not allowed) rows (a), (d), and (g) of Table 3 refer to display row 0 only. For all other rows text display is disabled and Blanking = '0'.
2. The R, G, B outputs may contain character and background color information. The only exception is that background colors are inhibited when Blanking = '0'.
3. Valid during display period only (see Figure 5); otherwise no character or background information is displayed as blanking is determined by the Picture On. (No blanking if PO = '1').

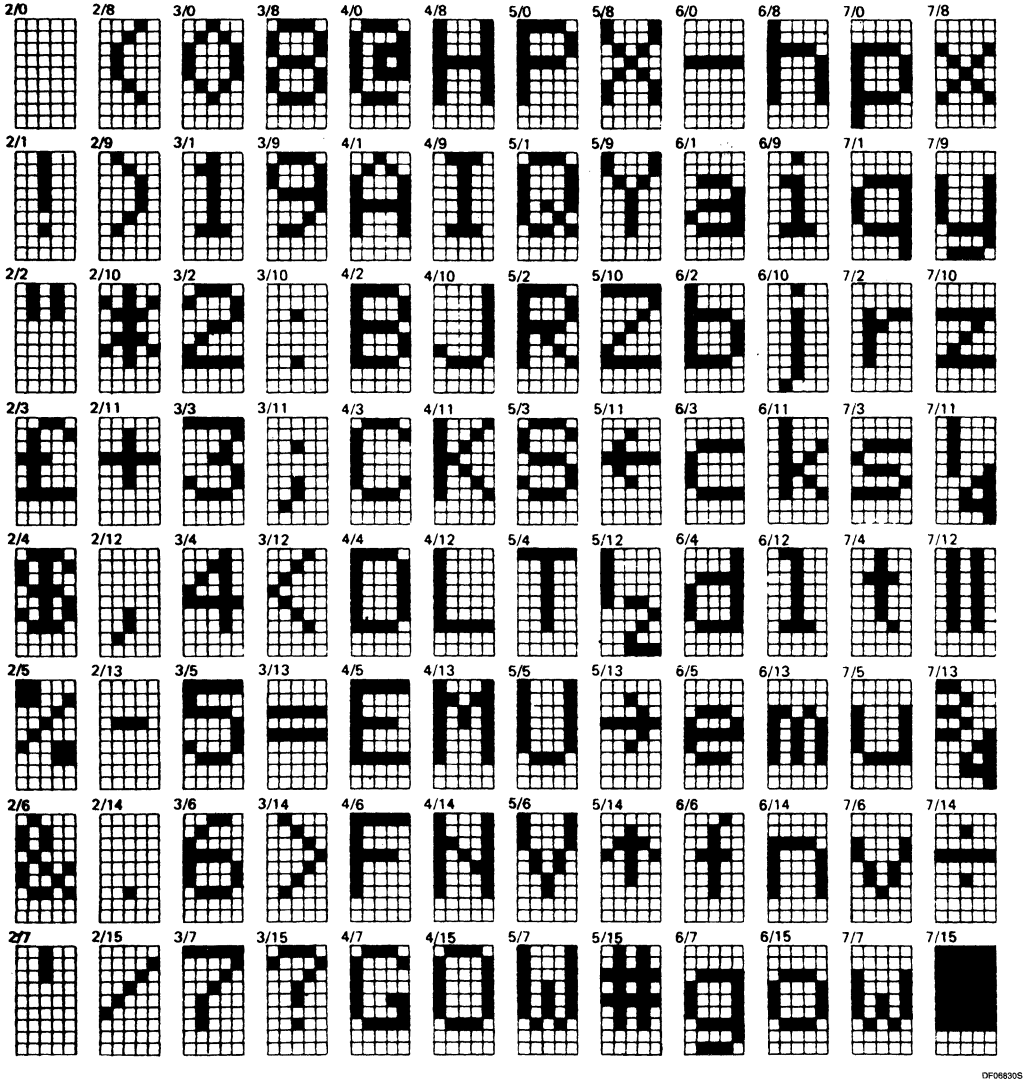

Figure 9. SAA5050 Character Set (English)

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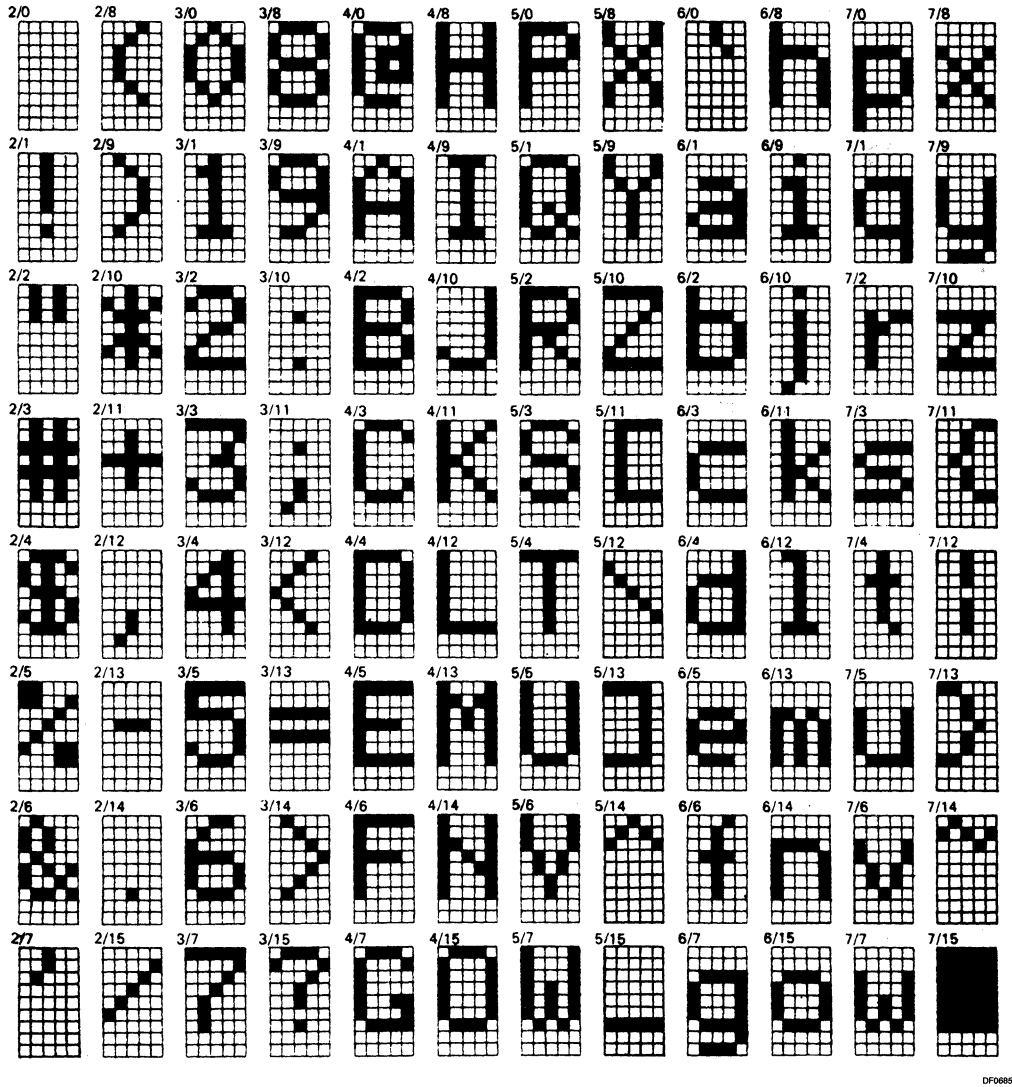


Figure 10. SAA5050 Character Set (US ASCII)

Signetics

SAA5230
Teletext Video Processor

Product Specification

Linear Products

DESCRIPTION

The SAA5230 is a bipolar integrated circuit intended as a successor to SAA5030. It extracts teletext data from the video signal, regenerates teletext clock, and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (SAA5040, Computer Controlled Teletext), EUROM SAA5350 or other compatible devices.

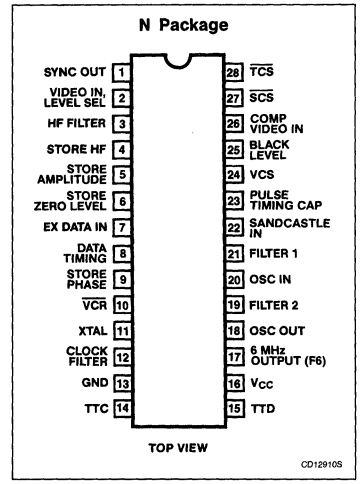
FEATURES

- **Adaptive data slicer**
- **Data clock regenerator**
- **Sync separator, line phase detector, and 6MHz VCO forming display phase-locked loop (PLL)**
- **Performs all of the functions of the SAA5030 except field sync integration and signal quality detection**
- **When used with the SAA5240, a microprocessor-controlled teletext/data acquisition system can be easily implemented**
- **Good data slicing capability in the presence of echoes and noise with high-frequency loss compensation**
- **On-chip clock regeneration circuitry can operate with different data rates**
- **On-chip PLL allows display to be easily locked to a VCR**
- **Minimal number of external components/adjustments**

APPLICATIONS

- **Teletext**
- **Data slicing and clock regeneration**
- **Phase locking with incoming video**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP (SOT-117)	−25°C to +70°C	SAA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (Pin 16)	13.2	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−25 to +70	°C

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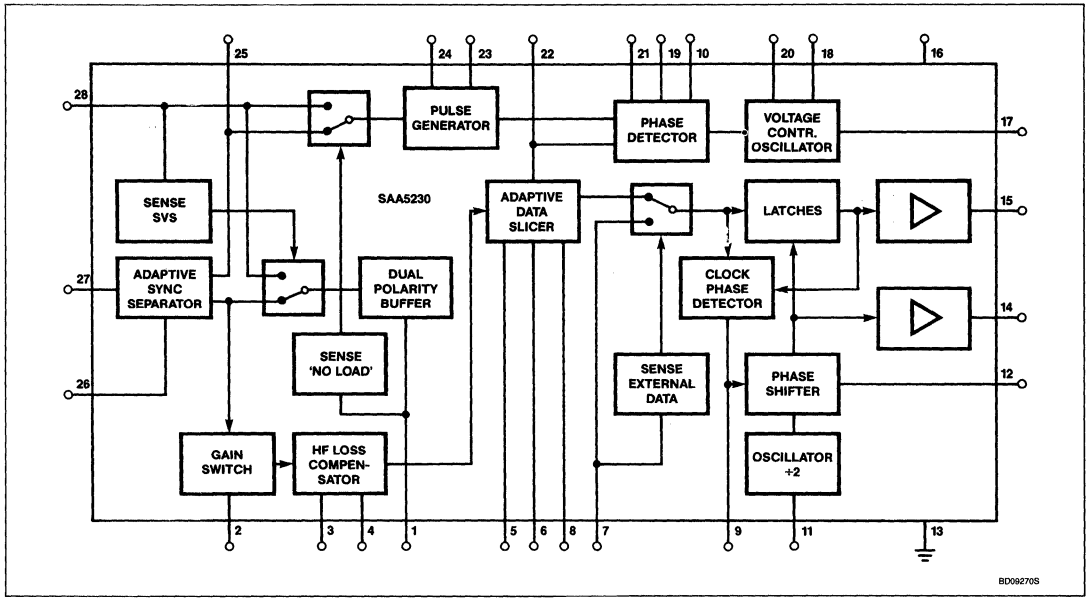
BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; T_A = 25°C with external components as shown in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	10.8	12.0	13.2	V
I_{CC}	Supply current		70		mA
Video input and sync separator					
	Video input amplitude (sync to white)				
$V_{27-13(P-P)}$	Pin 2 Low	0.7	1	1.4	V
$V_{27-13(P-P)}$	Pin 2 High	1.75	2.5	3.5	V
$\|Z_S\|$	Source impedance			250	Ω
$V_{27-13(P-P)}$	Sync amplitude			1	V
Video level select input					
V_{2-13}	Input voltage Low	0		0.8	V
V_{2-13}	Input voltage High	2.0		5.5	V
I_2	Input current Low	0		−150	μA
I_2	Input current High	0		1	mA
Text composite sync input ($\overline{TCS}$)					
V_{28-13}	Input voltage Low	0		0.8	V
V_{28-13}	Input voltage High	2.0		7.0	V
Scan composite sync input ($\overline{SCS}$)					
V_{28-13}	Input voltage Low	0		1.5	V
V_{28-13}	Input voltage High	3.5		7.0	V
Select video sync from Pin 1					
	Input current				
I_{28}	V_I = 0 to 7V	−40	−70	−100	μA
I_{28}	V_I = 10V to V_{CC}	−5		+5	μA
Video composite sync output (VCS)					
V_{25-13}	Output voltage Low	0		0.4	V
V_{25-13}	Output voltage High	2.4		5.5	V
I_{25}	Output DC current Low			0.5	mA
I_{25}	Output DC current High			−1.5	mA
t_D	Sync separator delay time		0.5		μs
Dual polarity buffer output					
$V_{1(P-P)}$	$\overline{TCS}$ sync amplitude		0.45		V
$V_{1(P-P)}$	Video sync amplitude			1	V
I_1	Output current	−3		+3	mA
	DC output voltage				
V_1	R_L to ground (0V)		1.4		V
V_1	R_L to V_{CC} (12V)		10.1		V

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DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V; T_A = 25°C with external components as shown in Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Sandcastle input					
	Phase-lock pulse				
V_{22}	PL on (Low)	0		3	V
V_{22}	PL off (High)	3.9		5.5	V
	Blanking pulse				
V_{22}	CBB on (Low)	0		0.5	V
V_{22}	CBB off (High)	1.0		5.5	V
I_{22}	Input current	−10		+10	μA
PLL					
	Line sync timing				
t_P	pulse width (using composite video)		2		μs
t_P	pulse width (using scan composite sync)		3		μs
	Pulse duration				
t_P	period PL must be Low to make VCO free-run	100			μs
6MHz-VCO (F6)					
$V_{17(P-P)}$	AC output voltage	1	2	3	V
V_{17-13}	DC output voltage	4		8	V
t_R, t_F	Rise and fall time	20		40	ns
C_{17-13}	Load capacitance			40	pF
$\overline{VCR}$					
V_{10-13}	VCR-mode on (Low)	0		0.8	V
V_{10-13}	VCR-mode off (High)	2.0		V_{CC}	V
I_{10}	Input current	−10		+10	μA
Data slicer					
	Data amplitude of video input				
V_{27}	Pin 2 Low	0.30	0.46	0.70	V
V_{27}	Pin 2 High	0.75	1.15	1.75	V
Teletext clock output					
$V_{14(P-P)}$	AC output voltage	2	3	4	V
V_{14-13}	DC output voltage	4		8	V
C_L	Load capacitance			40	pF
t_R, t_F	Rise and fall times	20	30	45	ns
t_D	Delay of falling edge relative to other edges of TTD	−20	0	+20	ns
Teletext data output					
$V_{15(P-P)}$	AC output voltage	2.0	3.0	4.0	V
V_{15-13}	DC output voltage	4		8	V
C_L	Load capacitance			40	pF
$t_R = t_F$	Rise and fall times	20	30	45	ns

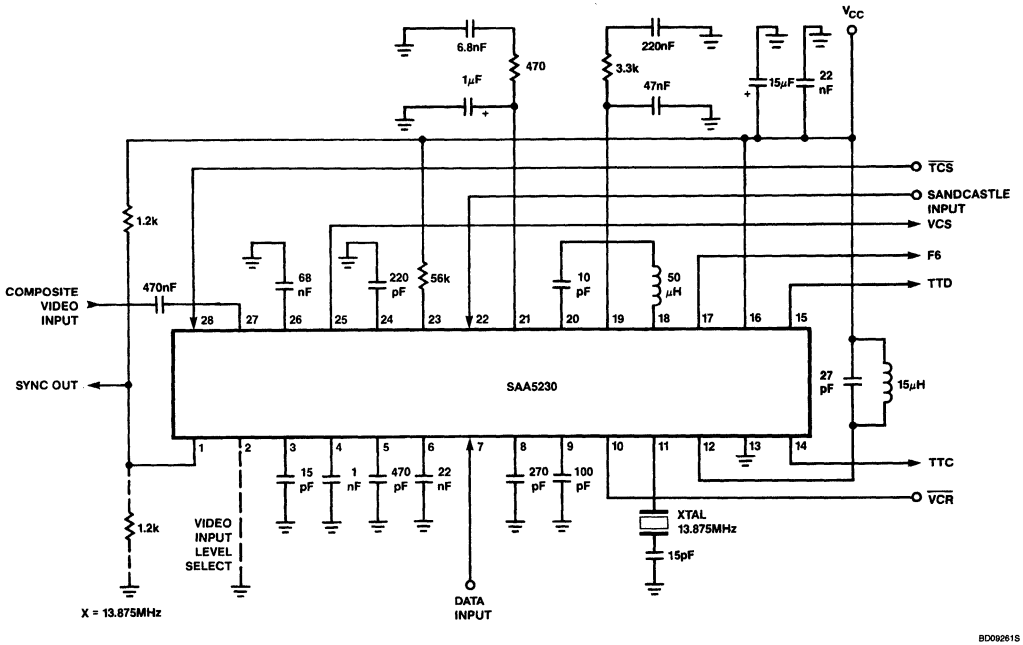

Figure 1. Test and Application Circuit

APPLICATION DATA

The function is quoted against the corresponding pin number.

1 Sync output to TV — Output with dual polarity buffer, a load resistor to 0V or +12V selects positive-going or negative-going syncs.

2 Video Input Level Select — Low level selects 1V input video level. With no connection, level floats High, selecting 2.5V level.

3 HF Filter — A capacitor connected to this pin filters the video signal for the HF loss compensator.

4 Store HF — The HF amplitude is stored by a capacitor connected to this pin.

5 Store Amplitude — Store capacitor stores the amplitude for the adaptive data slicer.

6 Store Zero Level — Store capacitor stores the zero level for the adaptive data slicer.

7 External Data Input — Current input for sliced teletext data from external device. Active High level (current), low impedance input.

8 Data Timing — A capacitor is connected to this pin for timing of the adaptive data slicer.

9 Store Phase — A capacitor connected to this pin stores the output signal from the clock phase detector.

10 Video Tape Recorder Mode ($\overline{VCR}$) — Signal input to command PLL into (short time constant mode), enable text to synchronize to a video tape recorder. Active is Low. If not connected, the level is High.

11 Crystal — A 13.875MHz crystal (2 × data rate) in series with a capacitor is connected to this pin.

12 Clock Filter — A filter for the clock signal is connected to this pin (6.938MHz).

13 Ground (0V)

14 Teletext Clock Output — TTC for CCT (Computer Controlled Teletext).

15 Teletext Data Output — TTD for CCT.

16 Supply Voltage V_{CC} — Typical value +12V.

17 F6 — 6MHz output clock for timing and sandcastle generation in CCT.

18 Oscillator Output (6MHz) — A series-resonant circuit is connected between this pin and Pin 20 to control the nominal frequency of the VCO.

19 Filter 2 — A filter for the line phase detector is connected to this pin. The filter has a short time constant and is used in video recorder mode and while the loop is locking up.

20 Oscillator Input (6MHz) — See Pin 18.

21 Filter 1 — A long time constant filter for the line phase detector is connected to this pin.

22 Sandcastle Input — This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. For signal timing, see Figure 2.

23 Pulse Timing Resistor — A connected resistor defines the current for the pulse generator.

24 Pulse Timing Capacitor — A connected capacitor is used for timing of the pulse generator.

25 VCS Output — Video composite sync output signal for CCT.

26 Black Level — A capacitor connected to this pin stores the black level for the adaptive sync separator.

27 Composite Video Input — The composite video is fed to this input via a clamp capacitor.

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28 Sync Input — Input for text composite sync ($\overline{TCS}$) from CCT or $\overline{SCS}$ from external sync circuit. $\overline{SCS}$ is expected if there is no load resistor at Pin 1.

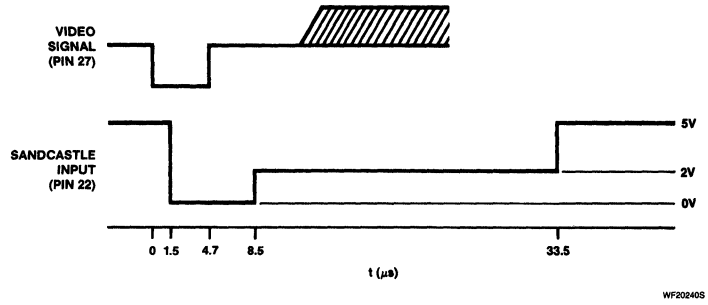


Figure 2. Sandcastle Waveform and Timing

Signetics

SAA5350
Single-Chip Color CRT Controller (625-Line System)

Product Specification

Linear Products

DESCRIPTION

The SAA5350 EUROM1 is a single-chip VLSI NMOS CRT controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM — the simplest configuration needs just a microcontroller and 4kB of display memory.

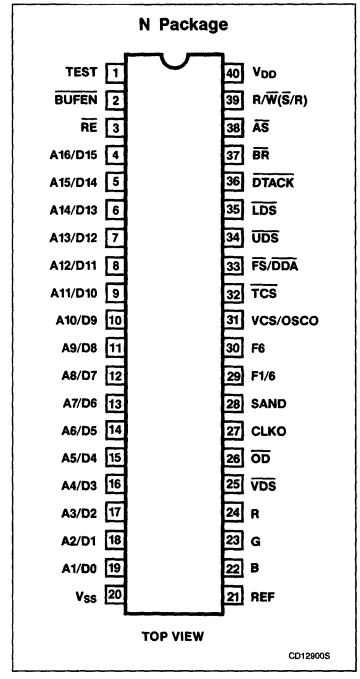
FEATURES

- **Minimal additional hardware required**
- **Screen formats of 40/80 character by 1-to-25 row display**
- **512 alphanumeric or graphic characters on-chip or extendable off-chip**
- **Serial attribute storage (STACK) and parallel attribute storage**
- **Dynamically redefinable character (DRCS) capability over full field**
- **Interfaces with 8/16-bit microprocessors with optional direct memory access**
- **On-chip scroll map minimizes data to be transferred when scrolling**
- **On-chip color map RAM followed by three non-linear digital-to-analog converters which compensate for CRT non-linearity**
- **Memory interface capable of supporting multi-page terminals. EUROM can access up to 128kB of display memory**
- **Programmable cursor**
- **Programmable local status row**
- **Three synchronization modes:**
  - *stand-alone:* built-in oscillator operating with an external 6MHz crystal
  - *simple slave:* directly synchronized from the source of text composite sync
  - *phase-locked slave:* indirect synchronization allows picture-in-text displays (e.g., VCR/VLP video with text overlay)
- **On-chip timing composite sync output**
- **Zoom feature which allows the height of any group of rows to be increased to enhance legibility**

APPLICATIONS

- **Videotex**
- **Teletext**
- **Microprocessor-controlled display systems**
- **General purpose CRT controller applications**
- **Display systems requiring the display of text, graphics, and analog video in the same video frame**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
40-Pin Plastic DIP (SOT-129)	−20°C to +70°C	SAA5350N

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NOTE:
1. For a 525-line system, please use the SAA5355. Data sheets are available upon request.

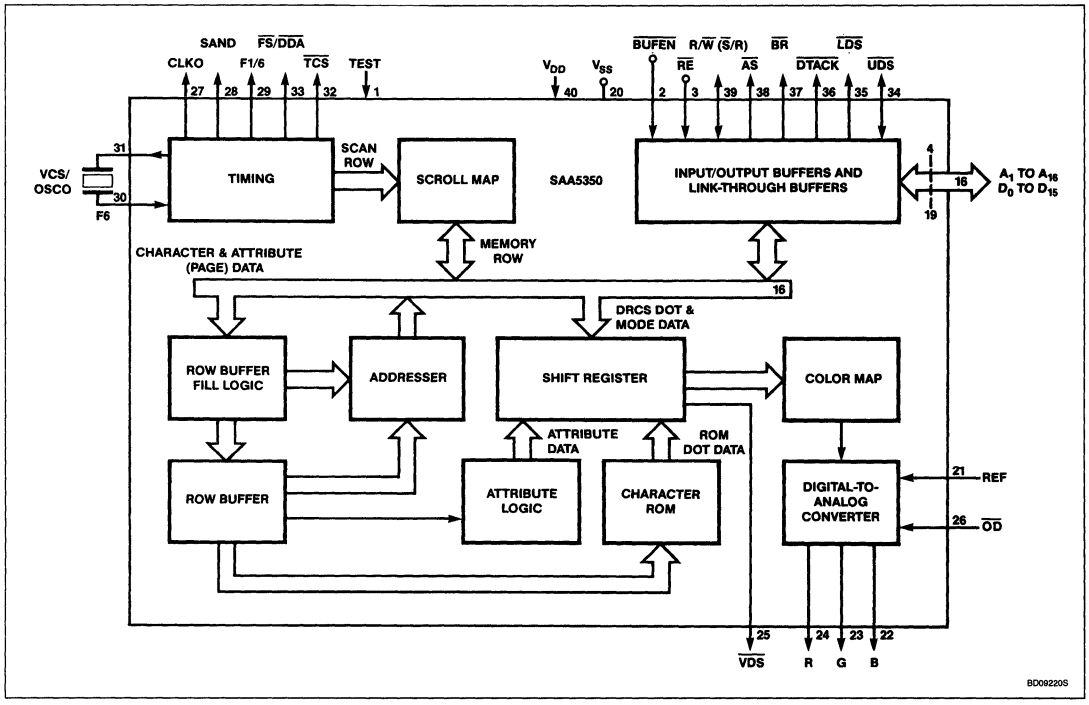
NOTICE: *The SAA5350 will be replaced during 1987 by an upgraded SAA5351. Please consult factory for production status*

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	TEST	Input to be connected to V_{SS}
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs
4 to 19	A16 to A1/D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer
20	V_{SS}	Ground (0V)
21	REF	Analog reference input
22 23 24	B G R	Analog outputs (signals are gamma-corrected)
25	$\overline{VDS}$	Switching output for dot, screen (row), box, and window video data; for use when video signal is present (e.g., from TV, VLP, alpha + photographic layer). This output is Low for TV display and High for text and will interface directly with a number of color decoder ICs (e.g., TDA3560, TDA3505)
26	$\overline{OD}$	Output disable causing R, G, B, and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate
27	CLKO	12MHz clock output for hard-copy dot synchronization (referenced to output dots)
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g., VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop
29	F1/6	1MHz or 6MHz output
30	F6	6MHz clock input (e.g., from SAA5230). Internal AC coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g., from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g., VLP) or in stand-alone sync mode, output from internal oscillator circuit (fixed frequency)
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots)
34	$\overline{UDS}$	Upper data strobe input/output
35	$\overline{LDS}$	Lower data strobe output
36	DTACK	Data transfer acknowledge (open drain output)
37	$\overline{BR}$	Bus request to microprocessor (open drain output)
38	$\overline{AS}$	Address strobe output to external address latches
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer
40	V_{DD}	Positive supply voltage (+ 5V)

Single-Chip Color CRT Controller (625-Line System) SAA5350

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pin 40)	−0.3 to +7.5	V
V_{IMAX}	Maximum input voltage (except F6, $\overline{TCS}$, REF)	−0.3 to +7.5	V
V_{IMAX}	Maximum input voltage (F6, $\overline{TCS}$)	−0.3 to +10.0	V
V_{REF}	Maximum input voltage (REF)	−0.3 to +3.0	V
V_{OMAX}	Maximum output voltage	−0.3 to +7.5	V
I_{OMAX}	Maximum output current	10	mA
T_A	Operating ambient temperature range	−20 to +70	°C
T_{STG}	Storage temperature range	−65 to +125	°C

NOTE:
Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$; $T_A = -20$ to $+70°C$, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pin 40)	4.5	5.0	5.5	V
I_{DD}	Supply current (Pin 40)			350	mA
Inputs F6[1]					
Slave modes (Figure 1)					
$V_{I(P-P)}$	Input voltage (peak-to-peak value)	1.0		7.0	V
$\pm V_{CC}$	Input peaks relative to 50% duty factor	0.2		3.5	V
I_{LI}	Input leakage current at $V_I = 0$ to 10V; $T_A = 25°C$			20	μA
C_I	Input capacitance			12	pF
Stand-alone mode (Figure 2)					
C_1	Series capacitance of crystal		28		pF
C_0	Parallel capacitance of crystal		7.1		pF
R_R	Resonance resistance of crystal			60	Ω
G	Gain of circuit			TBD	V/V
$\overline{BUFEN}$, $\overline{RE}$, $\overline{OD}$					
V_{IL}	Input voltage Low	0		0.8	V
V_{IH}	Input voltage High	2.0		6.5	V
I_I	Input current at $V_I = 0$ to $V_{DD} + 0.3V$; $T_A = 25°C$	−10		+10	μA
C_I	Input capacitance			7	pF
REF (Figure 3)					
V_{REF}	Input voltage	0	1 to 2	2.7	V
R_{REF}	Resistance (Pin 21 to Pin 20) with REF supply and R, G, B outputs OFF		125		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = −20 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Outputs					
SAND					
V_{OH}	Output voltage high level at I_O = 0 to −30μA	4.2		V_{DD}	V
V_{OI}	Output voltage intermediate level at I_O = −30 to +30μA	1.3	2.0	2.7	V
V_{OL}	Output voltage low level at I_O = 0.2mA	0		0.2	V
C_L	Load capacitance			30	pF
F1/6, CLKO, $\overline{DDA}$/$\overline{FS}$					
V_{OH}	Output voltage High at I_{OH} = −200μA	2.4		V_{DD}	V
V_{OL}	Output voltage Low at I_{OL} = 3.2mA	0		0.4	V
C_L	Load capacitance			50	pF
$\overline{LDS}$, $\overline{AS}$					
V_{OH}	Output voltage High at I_{OH} = −200μA	2.4		V_{DD}	V
V_{OL}	Output voltage Low at I_{OL} = 3.2mA	0		0.4	V
C_L	Load capacitance			200	pF
$\overline{DTACK}$, $\overline{BR}$ (open-drain outputs)					
V_{OL}	Output voltage Low at I_{OL} = 3.2mA	0		0.4	V
C_L	Load capacitance			150	pF
C_{OFF}	Capacitance (OFF state)			7	pF
R, G, B[2]					
V_{OH}	Output voltage High at I_{OH} = −100μA; V_{REF} = 2.7V[3]	2.4			V
V_{OL}	Output voltage Low at I_{OL} = 2mA			0.4	V
R_{OBL}	Output resistance during line blanking			150	Ω
C_{OFF}	Output capacitance (OFF state)			12	pF
I_{OFF}	Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0.3V; T_A = 25°C	−10		+10	μA
$\overline{VDS}$					
V_{OH}	Output voltage High AT I_{OH} = −250μA	2.4		V_{DD}	V
V_{OL}	Output voltage Low at I_{OL} = 2mA	0		0.4	V
V_{OL}	Output voltage Low at I_{OL} = 1mA	0		0.2	V
I_{OFF}	Output leakage current (OFF state) at V_I = 0 to V_{DD}+0.3V; T_A = 25°C	−10		+10	μA
Input/Outputs					
VCS/OSCO					
V_{IH}	Input voltage High	2.0		6.0	V
V_{IL}	Input voltage Low	0		0.8	V
I_I	Input current (output OFF) at V_I = 0 to V_{DD} + 0.3V; T_A = 25°C	−10		+10	μA
C_I	Input capacitance			10	pF

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DC ELECTRICAL CHARACTERISTICS (Continued) V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = −20 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
$\overline{TCS}$					
V_{IH}	Input voltage High	3.5		10.0	V
V_{IL}	Input voltage Low	0		1.5	V
I_I	Input current at V_I = 0 to V_{DD} + 0.3V; T_A = 25°C	−10		+10	μA
C_I	Input capacitance			10	pF
V_{OH}	Output voltage High at I_{OH} = −200 to 100μA	2.4		6.0	V
V_{OL}	Output voltage Low at I_{OL} = 3.2mA	0		0.4	V
C_L	Load capacitance			50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
V_{IL}	Input voltage Low	0		0.8	V
V_{IH}	Input voltage High	2.0		6.0	V
I_I	Input current at V_I = 0 to V_{DD} + 0.3V; T_A = 25°C	−10		+10	μA
C_I	Input capacitance			10	pF
V_{OH}	Output voltage High at I_{OH} = −200μA	2.4		V_{DD}	V
V_{OL}	Output voltage Low at I_{OL} = 3.2mA	0		0.4	V
C_L	Load capacitance			200	pF

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing F6 (Figure 1)					
t_R, t_F	Rise and fall times	10		80	ns
f_{F6}	Frequency	5.9		6.1	MHz
CLKO, F1/6, R, G, B, $\overline{VDS}$, $\overline{FS}/\overline{DDA}$, $\overline{OD}$[4, 5] (see Figure 4)					
t_{CLKH}	CLKO High time	30			ns
t_{CLKL}	CLKO Low time	20			ns
t_{CLKR} t_{CLKF}	CLKO rise and fall times			10	ns
t_{VCH}	CLKO High to R, G, B, $\overline{VDS}$ change	10			ns
t_{VOC}	R, G, B, $\overline{VDS}$ valid to CLKO rise	10			ns
t_{COV}	CLKO High to R, G, B, $\overline{VDS}$ valid			60	ns
t_{FOD}	CLKO High to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall			30	ns
t_{VS}	Skew between outputs R, G, B, $\overline{VDS}$			20	ns
t_{VR}, t_{VF}	R, G, B, $\overline{VDS}$ rise and fall times			30	ns
t_{AOD}	CLKO High to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	0			ns
t_{COD}	CLKO High to $\overline{FS}/\overline{DDA}$ change			55	ns
t_{DOC}	$\overline{FS}/\overline{DDA}$ valid to CLKO rise	5			ns
t_{F1H}	F1 High time[6]		500		ns
t_{F1L}	F1 Low time[6]		500		ns
t_{F6H}	F6 High time		83		ns
t_{F6L}	F6 Low time		83		ns
t_{ODS}	$\overline{OD}$ to CLKO rise setup			45	ns
t_{ODH}	$\overline{OD}$ to CLKO High hold			0	ns
Memory access timing[7, 8, 9] (see Figure 5)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
t_{CYC}	Cycle time		500		ns
t_{SAA}	$\overline{UDS}$ High to bus-active for address output	75			ns
t_{ASU}	Address valid setup to $\overline{AS}$ fall	20			ns
t_{ASH}	Address valid hold from $\overline{AS}$ Low	20			ns
t_{AFS}	Address float to $\overline{UDS}$ fall	0			ns
t_{ATD}	$\overline{AS}$ Low to $\overline{UDS}$ fall delay	50			ns
t_{HDS}	$\overline{UDS}$, $\overline{LDS}$ High time	220			ns
t_{LDS}	$\overline{UDS}$, $\overline{LDS}$ Low time	200			ns
t_{HAS}	$\overline{AS}$ High time	125			ns
t_{LAS}	$\overline{AS}$ Low time	320			ns
t_{AUH}	$\overline{AS}$ Low to $\overline{UDS}$ High	305			ns
t_{DSU}	Data valid setup to $\overline{UDS}$ rise	30			ns
t_{DSH}	Data valid hold from $\overline{UDS}$ High	0			ns
t_{UAS}	$\overline{UDS}$ High as $\overline{AS}$ rise delay	0			ns
t_{AFA}	$\overline{AS}$ Low to data valid			270	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Link-through buffers[7, 8] (see Figure 6)					
t_{BEA}	$\overline{BUFEN}$ Low to output valid			100	ns
t_{LTD}	Link-through delay time			85	ns
t_{IFR}	Input data float prior to direction change	0			ns
t_{OFR}	Output float after direction change			60	ns
t_{BED}	Output float after $\overline{BUFEN}$ High			60	ns
Microprocessor READ from EUROM (Figure 7)					
t_{RUD}	R/$\overline{W}$ High setup to $\overline{UDS}$ fall	0			ns
t_{UDA}	$\overline{UDS}$ Low to returned-data access time			210	ns
t_{REA}	$\overline{RE}$ LOW to returned data access time			210	ns
t_{DTL}	Data valid to $\overline{DTACK}$ Low delay	20			ns
t_{DLU}	$\overline{DTACK}$ Low to $\overline{UDS}$ rise	0			ns
t_{DTR}	$\overline{UDS}$ High to $\overline{DTACK}$ rise	0		50	ns
t_{DSA}	$\overline{UDS}$ High to address hold	0			ns
t_{DSH}	$\overline{UDS}$ High to data hold	10			ns
t_{SRE}	$\overline{UDS}$ High to $\overline{RE}$ rise	10			ns
t_{UDR}	$\overline{UDS}$ High to R/$\overline{W}$ fall	0			ns
t_{DSD}	$\overline{UDS}$ Low to $\overline{DTACK}$ Low	190		260	ns
t_{AUL}	Address valid to $\overline{UDS}$ fall	0			ns
Microprocessor WRITE to EUROM (Figure 8)					
t_{WCY}	Write cycle time[10]	500			ns
t_{WUD}	R/$\overline{W}$ Low setup to $\overline{UDS}$ fall	0			ns
t_{RES}	$\overline{RE}$ Low to $\overline{UDS}$ fall	30			ns
t_{ASS}	Address valid to $\overline{UDS}$ fall	30			ns
t_{LUS}	$\overline{UDS}$ Low time	100			ns
t_{DSS}	Data valid to $\overline{UDS}$ rise	80			ns
t_{DTA}	$\overline{UDS}$ Low to $\overline{DTACK}$ Low	0		60	ns
t_{DLU}	$\overline{DTACK}$ Low to $\overline{UDS}$ rise	0			ns
t_{DTR}	$\overline{UDS}$ High to $\overline{DTACK}$ rise	0		50	ns
t_{DSH}	$\overline{UDS}$ High to data hold	0			ns
t_{DSA}	$\overline{UDS}$ High to address hold	0			ns
t_{SRE}	$\overline{UDS}$ High to $\overline{RE}$ rise	10			ns
t_{UDW}	$\overline{UDS}$ High to R/$\overline{W}$ rise	0			ns
F1/6 to memory access cycle (Figure 9)					
t_{UF6}	$\overline{UDS}$ High to F6 (component of F1/6) rise	20			ns
t_{F6U}	F6 (component of F1/6) High to $\overline{UDS}$ rise	40			ns

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Synchronization and blanking $\overline{TCS}$, SAND, $\overline{FS/DDA}$					
	See Figure 10 for timing relationships and Figure 11 for vertical sync and blanking waveforms.				

NOTES:
1. Pin 30 must be biased externally as it is internally AC-coupled.
2. 16-level analog voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, R, G, B, F1/6, $\overline{VDS}$: C_L = 25pF; $\overline{FS/DDA}$: C_L = 50pF.
5. CLKO, F1/6, $\overline{VDS}$, $\overline{FS/DDA}$: reference levels = 0.8 to 2.0V; R, G, B: reference levels = 0.8 to 2.0V with V_{REF} = 2.7V.
6. These times may momentarily be reduced to a nominal 83ns in slave-sync mode at the moment of resynchronization.
7. C_L = 150pF.
8. Reference levels = 0.8 to 2.0V.
9. F6 input at 6MHz.
10. Microprocessor write cycle times of less than 500ns are permitted but often result in wait states being generated; the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.

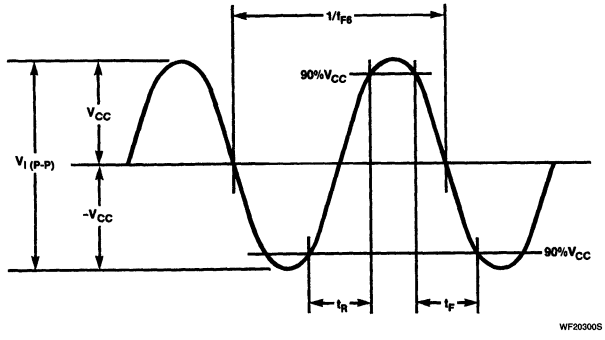
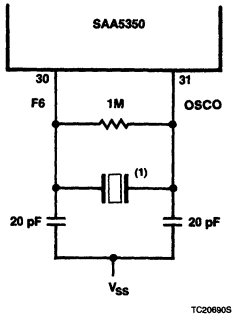
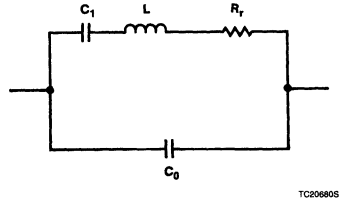


Figure 1. F6 Input Waveform



NOTE:
1. Catalog number of crystal: 4322 143 04101.

a. Oscillator Circuit for SAA5350 Stand-Alone Sync Mode



b. Equivalent Circuit of Crystal at Resonance (see Characteristics for Values)

Figure 2

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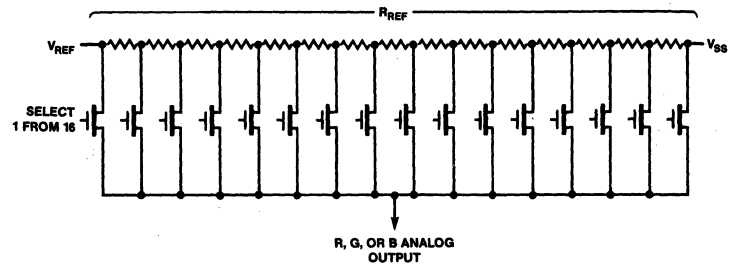


Figure 3. Circuit Arrangement Giving One-of-Sixteen Reference Voltage Levels for the R, G or B Analog Outputs

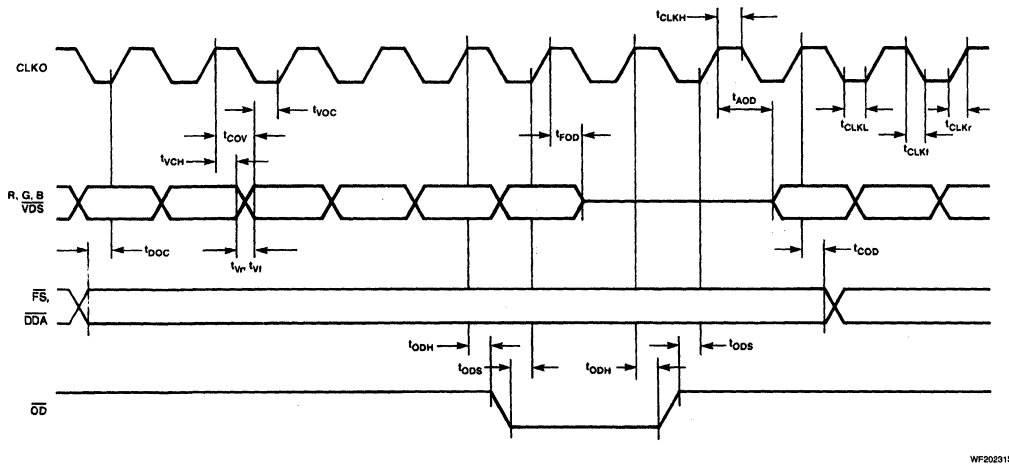


Figure 4. Video Timing

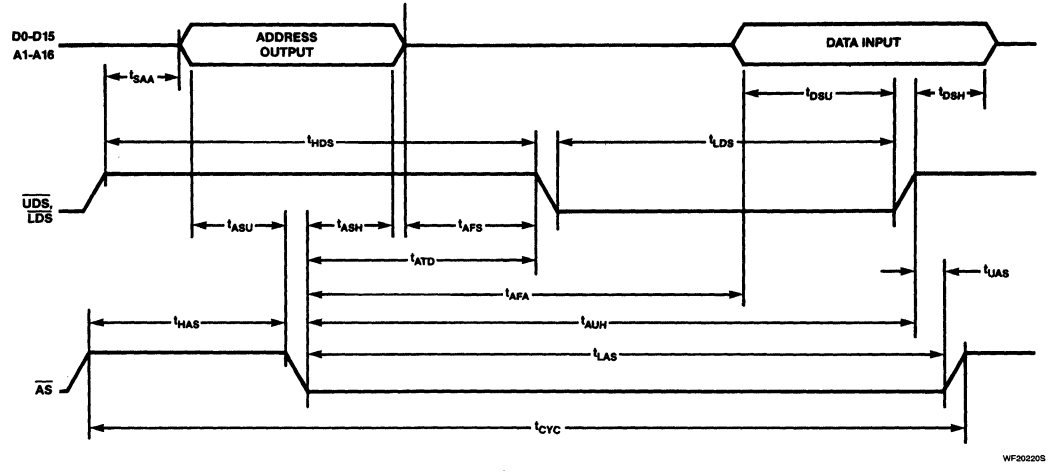


Figure 5. Memory Access Timing

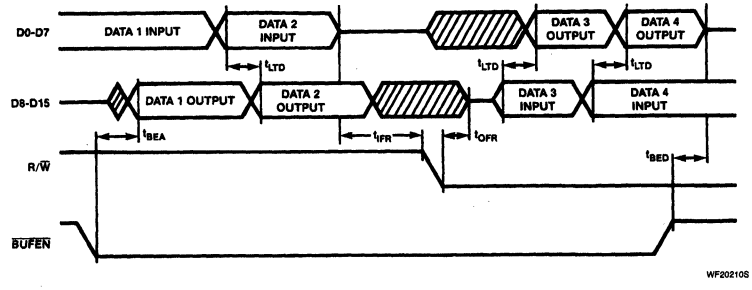


Figure 6. Timing of Link-Through Buffers

13

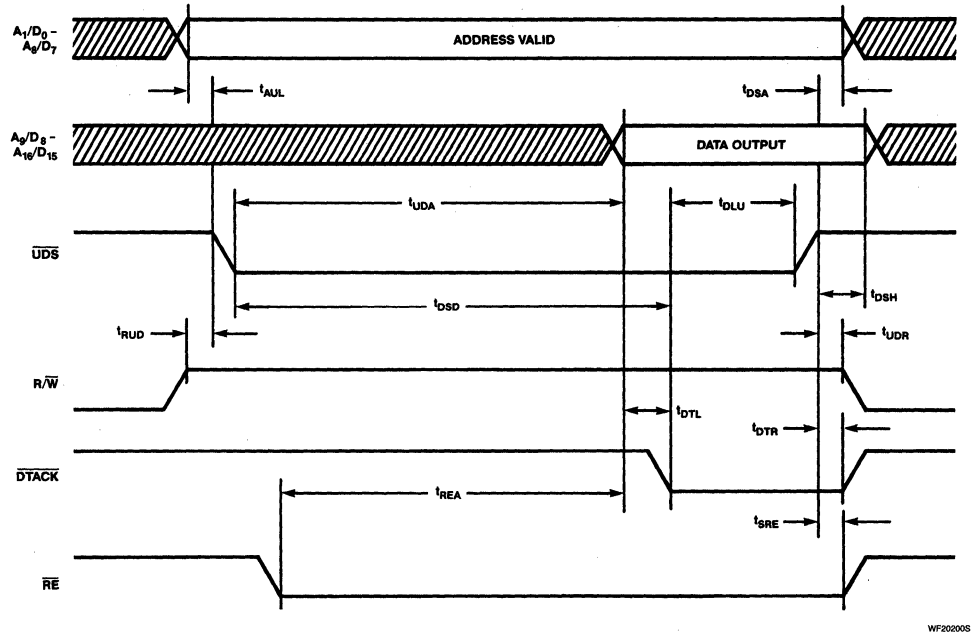


Figure 7. Timing of Microprocessor Read From EUROM

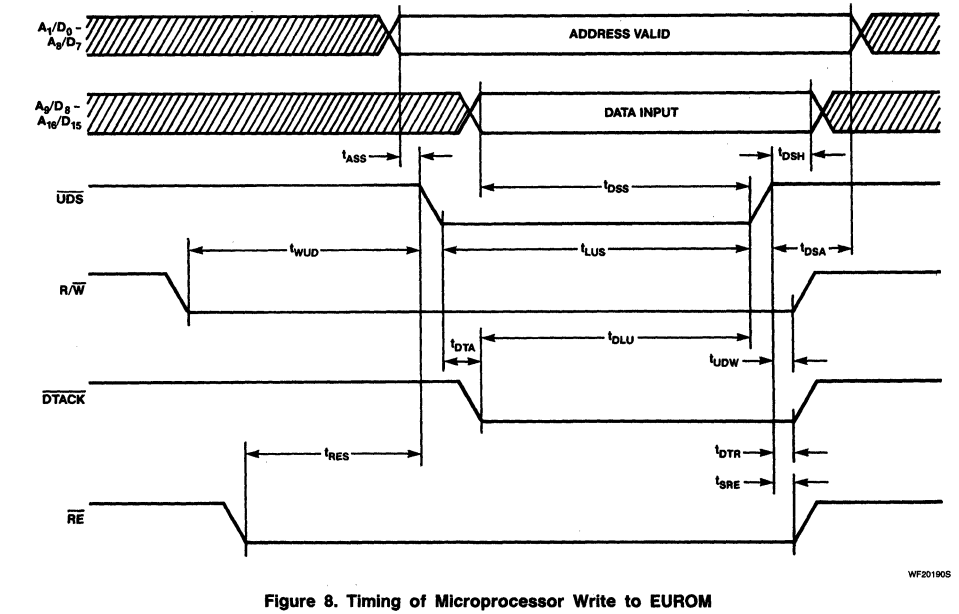


Figure 8. Timing of Microprocessor Write to EUROM

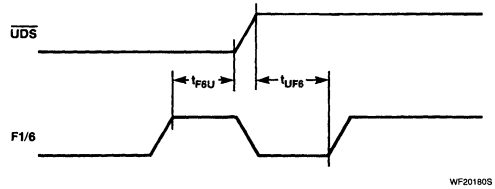
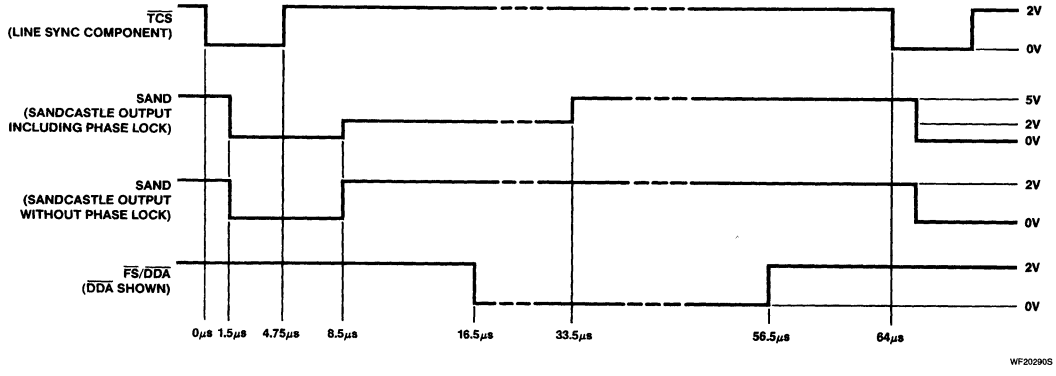
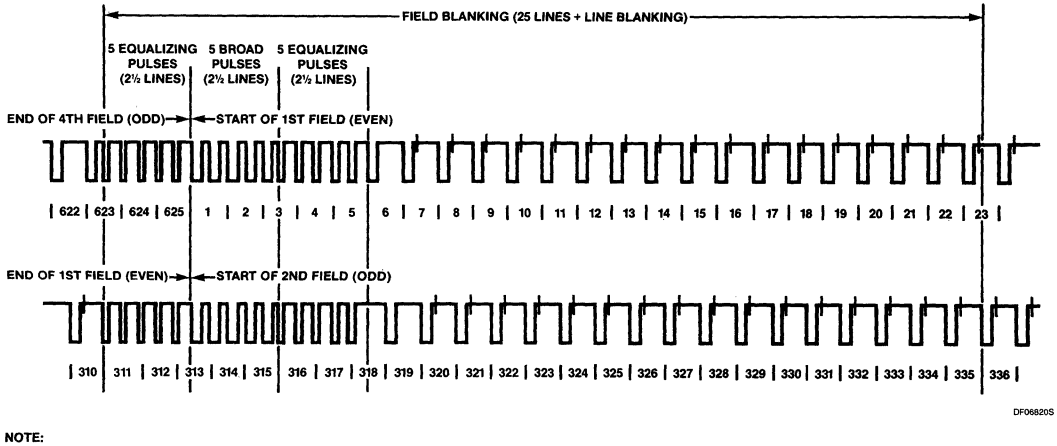


Figure 9. Timing of F1/6 to Memory Access Cycle



NOTE:
1. All timings are nominal and assume f_{F6} = 6MHz.

Figure 10. Timing of Synchronization and Blanking Outputs



NOTE:
1. Separation of broad pulses = 4.75μs; equalizing pulse widths = 2.25μs.

Figure 11. Vertical Synchronization and Blanking Waveforms

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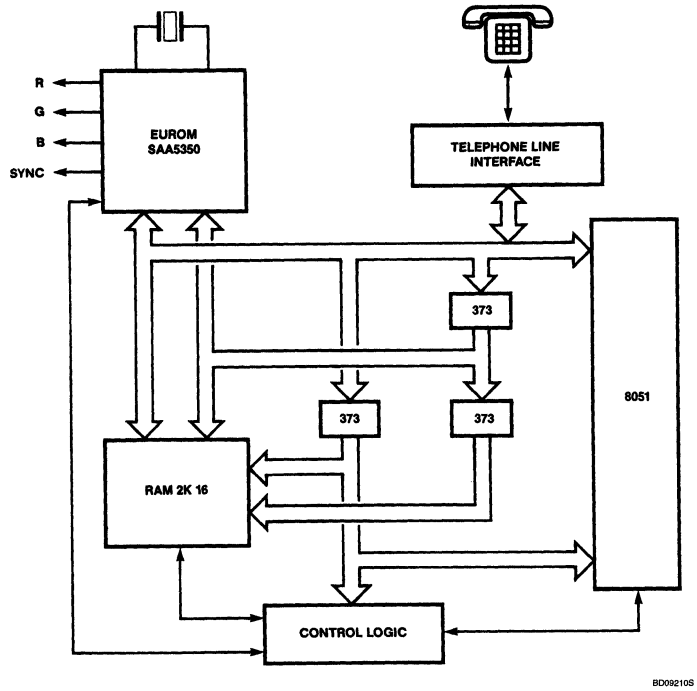


Figure 12. Basic Videotex Decoder Configuration

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Figure 12. Reference should also be made to the Block Diagram.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows — each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colors, and during the display time it is also used for addressing DRCS characters.

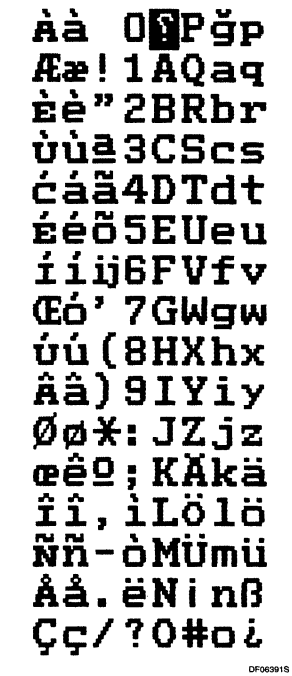
Timing

The timing chain operates from an external 6MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page, and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background color only for ROM-based alphanumeric characters. DRCS characters, block and smooth mosaics, and line drawing characters occupy all 12 lines.

The display is generated to the normal 625-line/50Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (Pin 32) for conventional timebases, a clock output at 1MHz or 6MHz (Pin 29) is available for driving other videotex devices, and a 12MHz clock (Pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (Pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

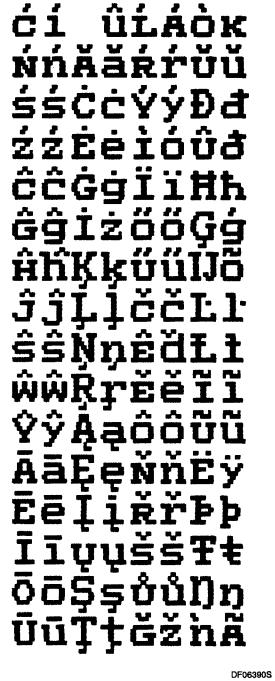
Character Generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters, and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figures 13 and 14.



DF06391S

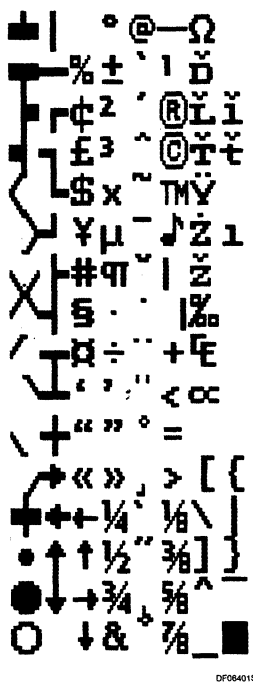
a. Table 0



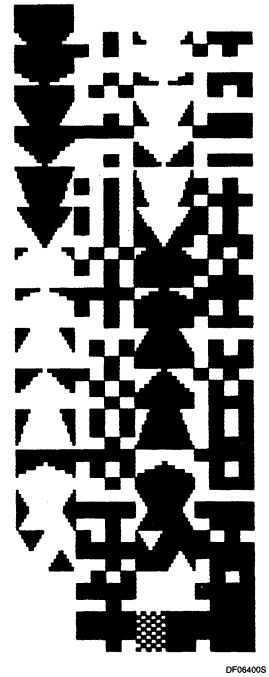
DF06390S

b. Table 1

Figure 13. On-Chip Characters



a. Table 2



b. Table 3

Figure 14. On-Chip Characters

The 128 most commonly used characters are contained in Table 0. These are the standard upper- and lower-case letters of the Roman alphabet, numerals, punctuation, and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set, and accents without associated symbols, are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll Map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row, thereby allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.

Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Color Map and Digital-to-Analog Converters

The color map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D/A converter. The resulting R, G, and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at Pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground color, background color, lining, and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-videotex applications, the device will also support the following operating modes:

Explicit fill mode — An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required, but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode — When operating with 80 characters per row, the available display attributes are eight foreground colors, eight (potentially different) background colors (including transparent), as well as underline and blink.

Full field DRCS mode — This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes, but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

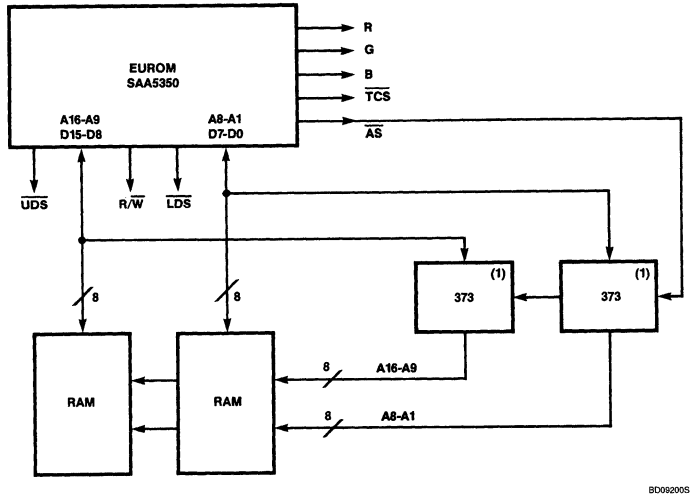
- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map

- The microprocessor accesses the display memory

EUROM Access to Display Memory (Figures 15 and 16)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most significant) and lower (least significant) display information, and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included, although EUROM only reads from the display memory.

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even-numbered bytes use the upper (most significant) part of the bus as shown in Figure 17. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.



NOTE:
1. 74LS373 octal transparent latch (3-State)

Figure 15. Simple RAM Interface Circuit for Display Memory Access

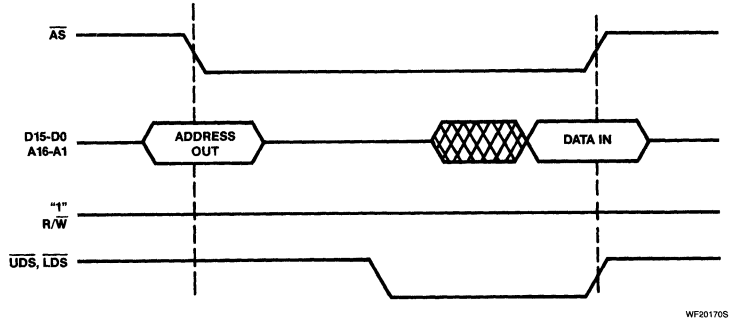


Figure 16. Bus Timing for Display Memory Access

13

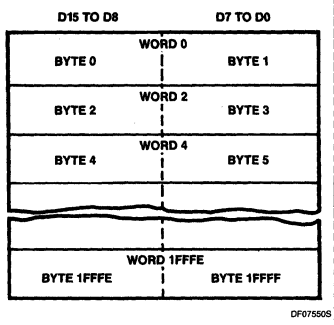


Figure 17. Display Memory Word/Byte Organization.

Warning Time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access, plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23μs.

Microprocessor Access to Register Map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit-wide RAM connected to the upper part of the data bus (Figure 18). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs, and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

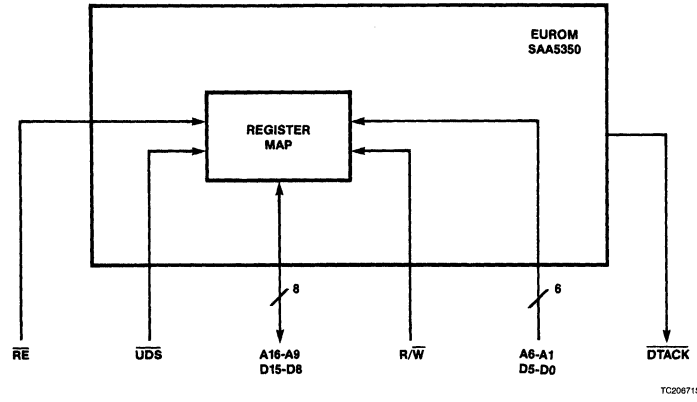


Figure 18. Microprocessor Access to Register Map

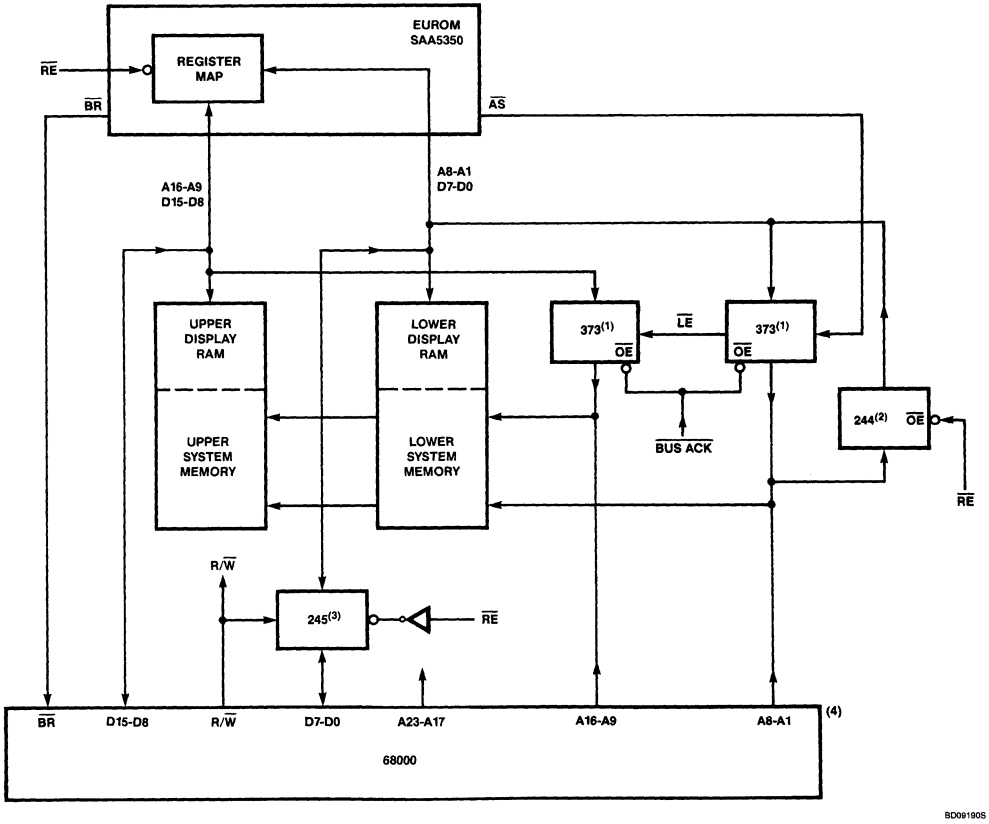
The main data and address paths used in a connected 68000 interface are shown in Figure 19. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed, data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time, the bidirectional buffers (74LS245) disable the signals from the low-order data bus of the 68000.

The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here, it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-Bit Microprocessors

Although the control bus is optimized for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8- or 16-bit or more microprocessors or microcontrollers (e.g., SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit-wide display memory is made simple by EUROM's on-chip, link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}/R$.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Figure 20. The interface is similar to that of the 16-bit system, but here the display memory does not receive A0 as an address — rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when High).



NOTE:
1. 74LS373 octal transparent latch (3-State).
2. 74LS244 octal buffer (3-State).
3. 74LS245 octal bus transceiver (3-State).
4. SCN68000 microprocessor unit.

Figure 19. Connected 16-Bit Microprocessor System

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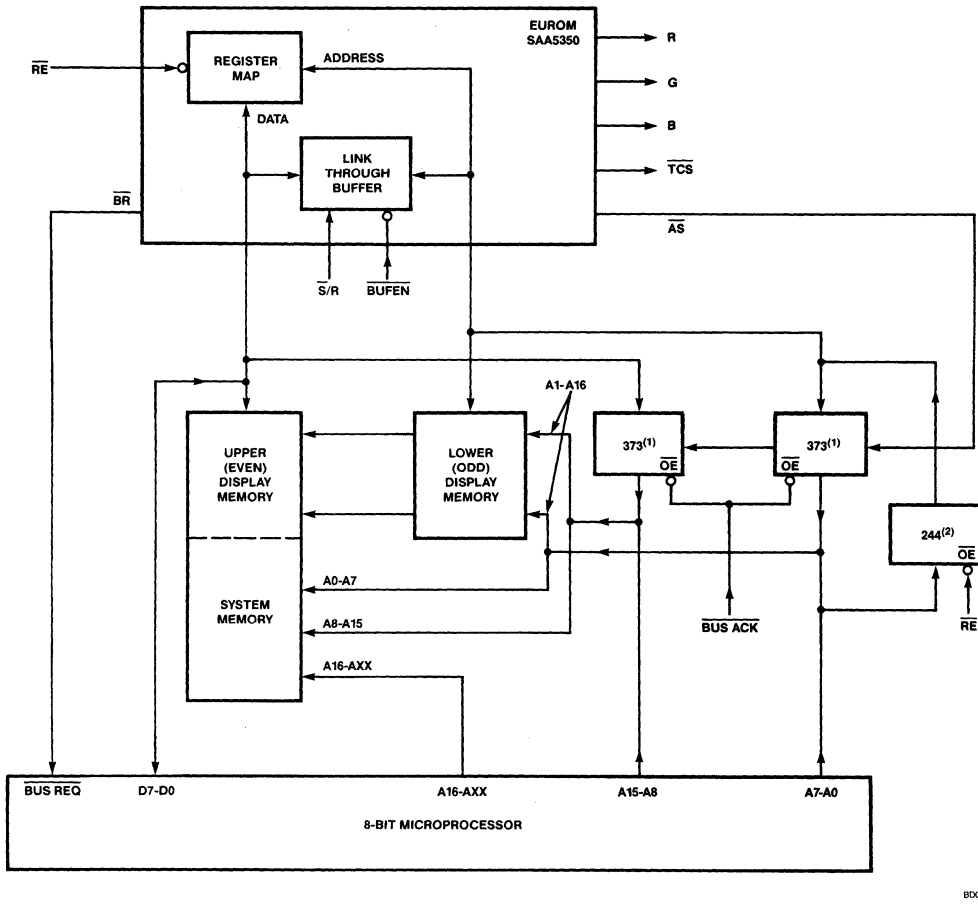
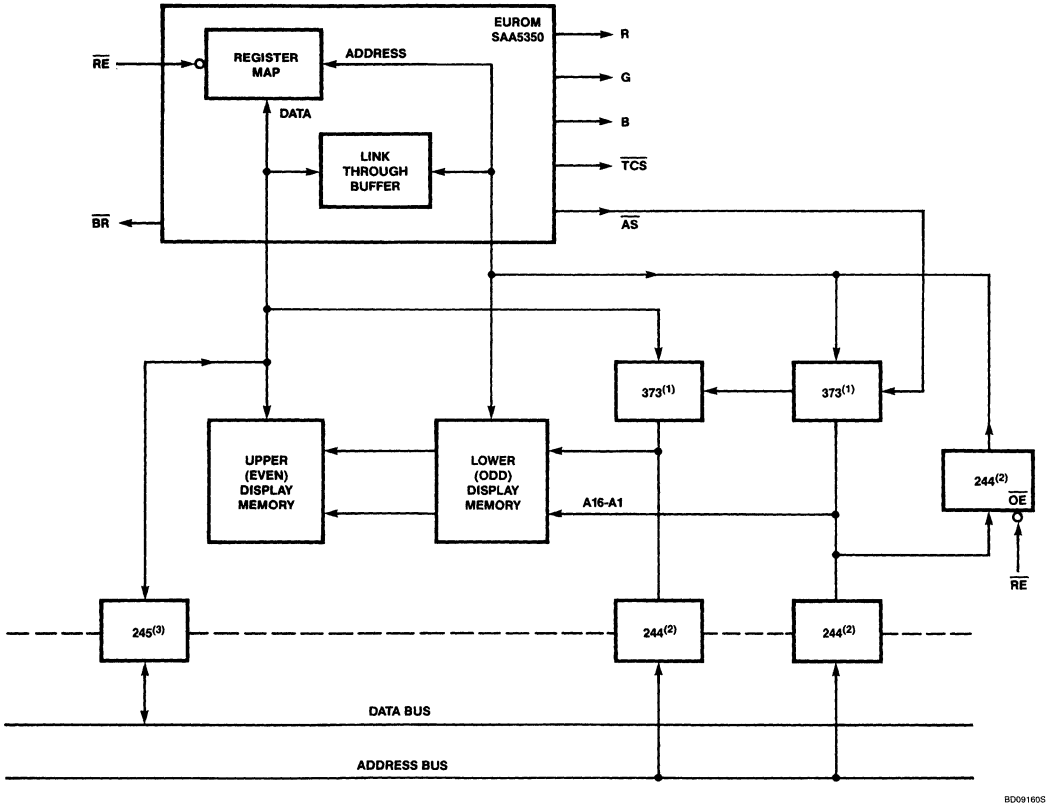


NOTES:
1. 74LS373 octal transparent latch (3-State).
2. 74LS244 octal buffer (3-State).

Figure 20. Connected 8-Bit Microprocessor System

Disconnected Systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM, and other peripherals by using isolating buffers as shown in Figure 21. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



NOTES:
1. 74LS373 octal transparent latch (3-State).
2. 74LS244 octal buffer (3-State).
3. 75LS245 octal bus transceiver (3-State).

Figure 21. Disconnected 8-Bit System

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Synchronization

Stand-Alone Mode

As a stand-alone device (e.g., in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6MHz on-chip oscillator using an external crystal as shown in Figure 22.

Simple-Slave

In the simple-slave mode, EUROM synchronizes directly to another device — such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT), or from another EUROM as shown in Figure 23. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250ns is built in to avoid resetting the counter at every TV line, and so prevents screen jitter. Field synchronization is made using EUROM's internal field sync separator.

Phase-Locked Slave

The phase-locked slave (indirect sync) mode is shown in Figure 24. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop — a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a TV source or a local VLP player, thus giving picture-in-text display possibilities.

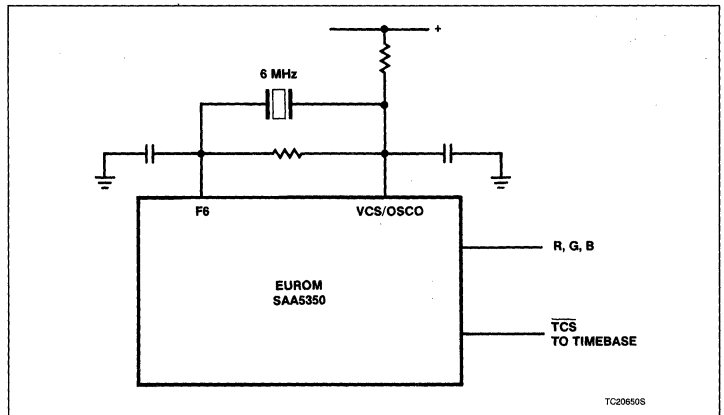

Figure 22. Stand-Alone Synchronization Mode

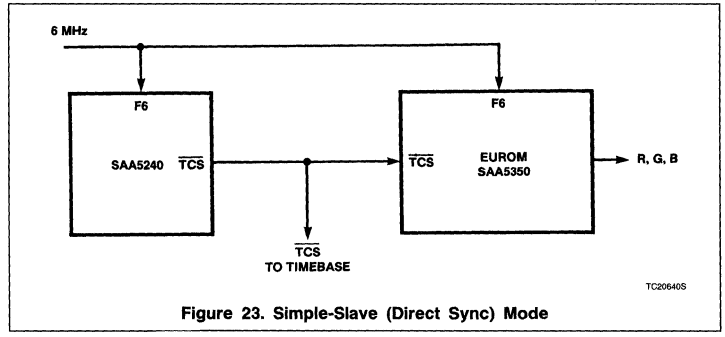

Figure 23. Simple-Slave (Direct Sync) Mode

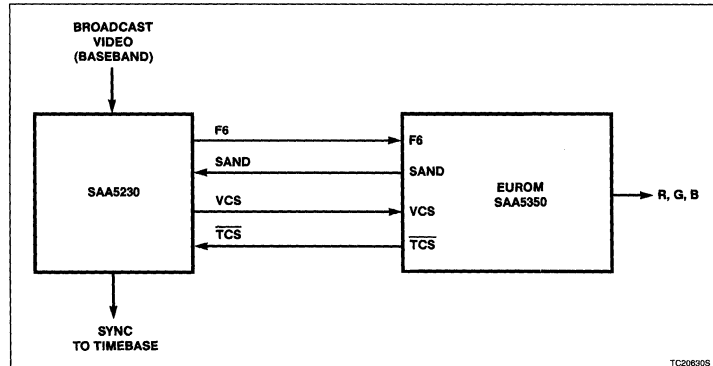

Figure 24. Phase-Locked Slave (Indirect Sync) Mode

Signetics

AN152
SAA5350: A Single-Chip CRT Controller

Application Note

Linear Products

The SAA5350 is a VLSI Advanced Peripheral Display Controller (APDC) containing approximately 120,000 transistors in advanced NMOS technology.

The APDC may be used for many display terminal applications such as color video monitors, personal computers, medical/industrial equipment, picture-telephones, videotex terminals, dot color printers, workstations and more.

Video systems design is made simple when using the APDC. The APDC can easily interface to a general purpose 8- or 16-bit microprocessor and act as a DMA device when accessing the display memory. Due to stack coding technique and the on-chip character ROM, external display memory requirements are minimal; 4kbytes is sufficient to create a high resolution, full-color, animated display. Figure 1 depicts a typical Videotex terminal implementation using the SAA5350. The 4kbytes include a 2kbytes user-defined Dynamically Redefinable Character Set (DRCS). The DRCS Concept is a powerful technique which allows each pixel of a character cell to be individually set, permitting almost unlimited expansion of the character repertoire and the display of more complex alphabets (Cyrillic, Arabic, Katakana, etc.) simple pictures, company logos, and other symbols (Figure 2).

The main features of the APDC are:

- 40/80 column by 20/24 row display
- On-chip ROM containing 512 alphanumeric characters
- Dynamically Redefinable Character Set (DRCS) capability
- On-chip scroll map
- On-chip color look-up table RAM and three D/A converters with gamma corrected outputs (32 colors/row-total color palette of 4,096 colors)
- Various flashing modes
- Many display attributes: double-height, double-width, double-size, invert, conceal, window, . . .etc.
- Easy interface to 8- or 16-bit microprocessors
- DMA capability to system display memory (this IC has a 16-bit multiplexed address and data bus.)
- Three synchronization modes: standalone, simple slave or phase-locked slave, allowing easy implementation of text-in-picture or picture-in-text type displays.
- Composite sync output
- Supports both interlaced and non-interlaced type displays
- Designed for 625 line systems
- Single 5V supply, 40-pin DIP

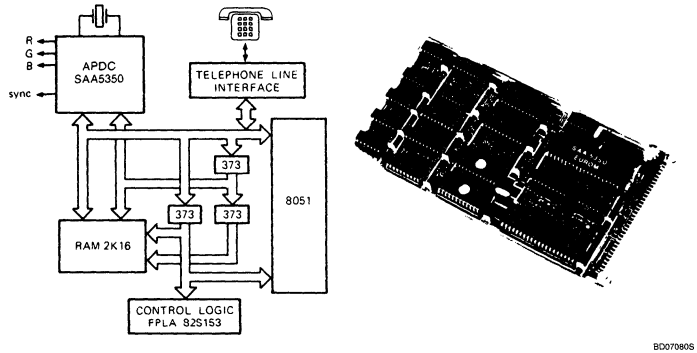

Figure 1. Videotex Decoder Using the SAA5350

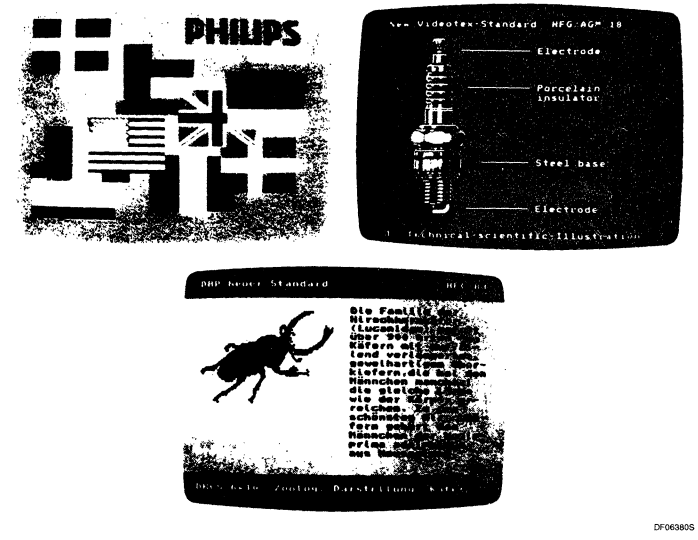

Figure 2. Examples of Displays Using DRCS

This application note outlines how the APDC operates, summarizes its attributes and gives examples of how it interfaces with microprocessors and display memory. The concepts of stack coding and DRCS are also briefly described.

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SAA5350: A Single-Chip CRT Controller AN152

SAA5350 CRT Controller IC APDC

A block diagram of APDC is shown in Figure 3. The APDC contains the following general functions: timing chain, character generator, attribute logic, scroll map, screen color logic, DRCS logic, and microprocessor interface.

To optimize system cost, APDC also incorporates a color map RAM and D/A converters providing RGB outputs corrected for CRT non-linearity. The on-chip scroll map eliminates the need for massive data transfer when scrolling.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (when in Stack Mode), and then fed into one half of the dual display row buffer. The data fetch process takes place during one line flyback period (per row), and since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows; each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colors; during the display time it is also used for addressing DRCS characters.

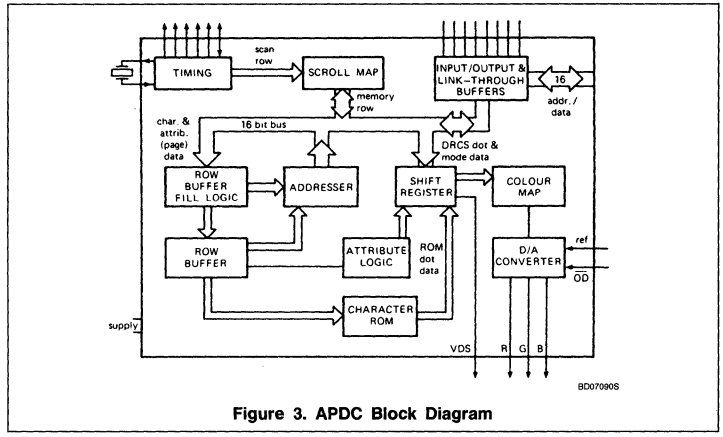


Figure 3. APDC Block Diagram

Timing

The timing chain operates from an external 6MHz clock or the on-chip fixed-frequency crystal oscillator. The basic format is 40 characters per row, 24/25 rows per page, 10 video lines per row.

APDC will also operate with 20/21 rows per page, 12 video lines per row.

The two extra lines per row are added symmetrically, and contain background color only for ROM-based alphanumeric characters. DRCS characters, block and smooth mosaics, and line drawing characters, however, occupy all 12 lines.

The display is generated to the normal 625-line/50Hz scanning standard, interlaced or non-interlaced. In addition to composite sync for conventional timebases, a clock output at 1MHz or 6MHz is available for driving other videotex devices, and a 12MHz clock is available for hardcopy dot synchronization. A Defined Display Area timing signal simplifies the application of external peripherals such as a light pen. This signal is nominally coincident with the character dot information.

Character Generation

APDC supports eight character tables, each of nominally 128 characters. Four are in on-chip ROM and contain fixed characters, and four for DRCS are stored in external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figures 4 and 5.

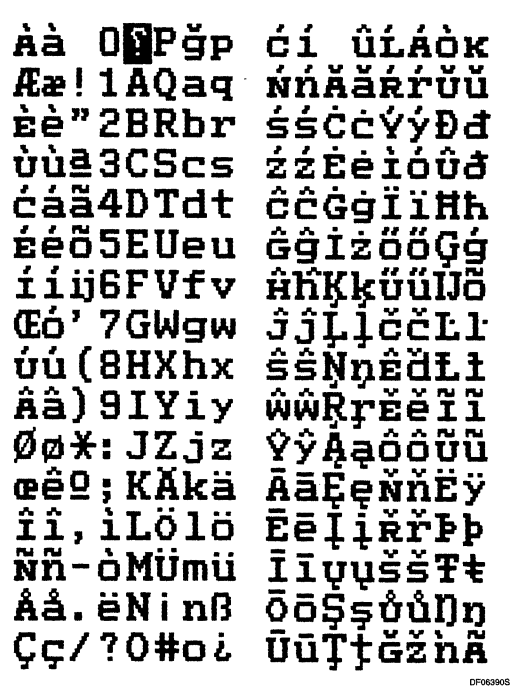
Table 0 contains the 128 most commonly used characters: standard upper- and lower-case Roman alphabet, numerals, punctuation, and the more common accented characters. In normal text transmission, Table 0 is used most of the time.

Table 1 contains further accented characters.

Table 2 contains a number of miscellaneous characters, mathematical symbols, the line drawing character set, and accents without associated characters.

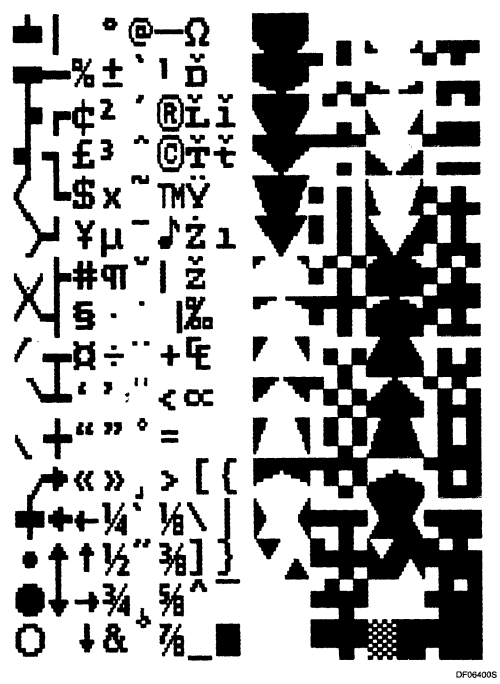
Table 3 contains the block mosaics for the basic alphamosaic service, together with the new smooth mosaics. The two sets are complementary and can readily be combined to create pleasing graphic displays such as maps, some examples of which are shown in Figure 6. Although the editorial need for these characters has decreased somewhat with the availability of DRCS, being predefined and resident on-chip, their use makes for savings in transmission time and avoids the waiting times associated with the downloading of DRCS characters.

Tables 4, 5, 6 and 7 are stored in external memory and are used for DRCS.



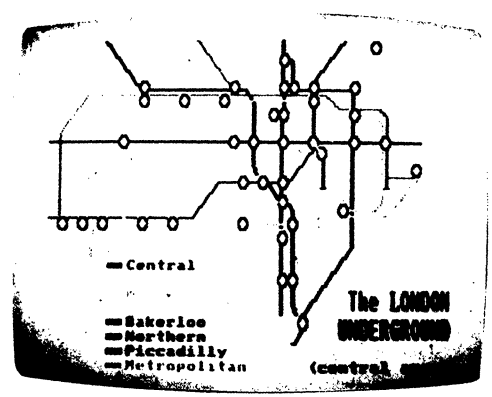
DF06390S

Figure 4. On-chip Characters: Tables 0 and 1



DF06400S

Figure 5. On-chip Characters: Tables 2 and 3



DF06410S

Figure 6. Examples of Displays Using Smooth and Mosaic Line Drawing Characters

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Scroll Map

Associated with the timing chain is the scroll map, an area of on-chip RAM of 26 bytes. It maps the scan row onto the fetched memory row, allowing the stored page to be displayed in any row order. For each row, a one-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to or from side storage. Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Color Map and D/A Converters

The on-chip color map and D/A converters considerably simplify the external circuitry. The color map RAM contains 32 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a nonlinear (gamma-corrected) D/A converter. The resulting R, G, and B outputs are low impedance with peak-to-peak amplitudes controlled by the voltage applied to the Reference Pin.

Cursor

A cursor is available in Stack Mode. Its position, character code, character table, foreground color, background color, lining and flash attributes are all software programmable via internal register bits.

DISPLAY ATTRIBUTES

APDC provides the following attributes for any character displayed.

Foreground Color

Foreground color is coded in five bits, implying a total of 32 colors. Of these, 31 represent specific locations in the color map; the last is interpreted as transparent.

When a pixel is set to transparent, the display color pointer is set to the value of the screen color at this location. If the screen color attribute is also transparent, the underlying TV picture, if any, is unblanked (i.e., displayed).

The 32nd location is also used during line or field flyback to output blanking level (black).

Background Color

Background color operates in exactly the same way as foreground color, with five bits defining 31 colors plus transparent.

Screen Color

The color of the screen may also be set to any one of the 31 color map locations, or transparent. The screen is notionally divided into 27 areas corresponding to the 25 rows and the upper and lower border areas. Each of these 27 areas can refer to a different location in the color map.

Flash

There are three states and six rates of flash. Other combinations such as 3-phase flash at 1Hz are not required but nonetheless are available with APDC.

Three flash states are:

- normal flash (active pixels alternating between foreground and background colors)
- inverted flash (in antiphase with normal flash)
- color table flash, where the active pixels alternate between two colors in the color map

The six flash rates are:

- 2-phase 1Hz flash (even flashing at 1Hz)
- each phase of 3-phase 2Hz flash
- ICF (increment flash)
- DCF (decrement flash)

If the image of an object is given sequential phases in adjacent character cells, three-phase flash gives the impression of movement along a row. Three-phase flash can also be used with DRCS to produce dynamic displays without the need for continuous transmission.

The ICF and DCF attributes cause objects to appear to move right or left, respectively, in the same way as with 3-phase flash. It avoids the need to specify flash phase explicitly on a per-character basis. In Stack Mode, APDC automatically supplies the correct phase. This method of specifying object motion reduces transmission time and serial attribute memory utilization.

Character Size

Double-height is available in the basic alpha-mosaic service, with certain restrictions. For example, a single row can contain only top or bottom halves of characters, not both, and so double-height characters cannot be interleaved. APDC provides double-width and double-size in addition to double-height, with no restrictions on horizontal or vertical interleaving.

In Stack Mode, APDC applies 'size rules' to determine the displayed output when conflicts occur; these rules apply, for example, when the bottom half of a double-height character would occupy the same position as the right-hand half of a double-width character. Part characters are never displayed. See separate section on Stack Coding.

Lining

For alphanumeric characters, the Lining attribute underlines the character. For mosaics and line drawing characters, it separates the character into six blocks or sub-squares (mosaic separation).

Conceal

The Conceal attribute makes the foreground and background colors the same until a local reveal function is activated. The local reveal function can be applied either to the whole field or on a row-by-row basis, allowing progressive reveal in response to user interaction.

Invert

This attribute exchanges the foreground and background colors and is included for compatibility with Teletel transmission codes. It also applies to Flash, giving antiphase instead of normal flash.

Box/Window

If the basic frame begins in TV mode, this attribute superimposes a box containing text (Foreground and Background or Screen colors) on the TV picture. It is compatible with the Box function used in the basic alphamosaic teletext service.

If the basic frame begins in text mode, the attribute provides a Window. That is, it sets the screen color to transparent at the character positions where it applies, so that the underlying TV picture is visible at pixels that are not obscured by foreground or background colors.

White Button

Various attributes and combinations of attributes can cause on-screen data to be obscured — double-height/double-width, conceal, foreground and background colors the same, etc. It is a requirement that this effect can be negated by a user function, colloquially known as the 'white button', which sets all the attributes to their default values without affecting the display memory contents. This function is implemented in APDC by a microprocessor-defined register bit which is active in Stack, Explicit Fill, and 80 Characters/Row modes.

ADDITIONAL FEATURES

APDC offers a number of features which are outside the specification, giving the IC a wider range of application.

Explicit Fill

In Explicit Fill mode, the page memory is not stack coded, and no processing is carried out during the Row Buffer Fill operation. Data from the memory is transferred directly to the row buffer.

Since there is then an explicit representation of all the attributes at every character location, there is no limit to the number of attribute changes on a given row. However, this mode requires a larger amount of external RAM (6kbytes/page including DRCS memory). Also, enlarged characters are not

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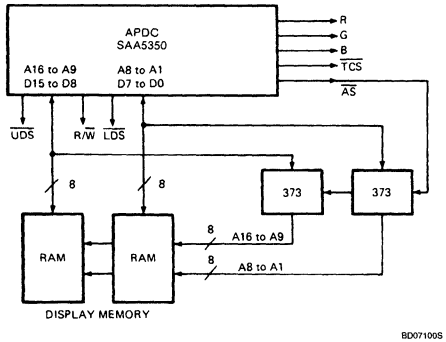

Figure 7. APDC Access to Display Memory

checked, so the rules concerning the size attributes must be implemented in software.

80 Characters/Row

The 80-character mode is also an explicit fill mode without stack coding. No additional circuitry is required; the row buffer is effectively rearranged as 80 16-bit words, each containing:

- 8 character bits
- 3 foreground color bits
- 3 background color bits
- 1 underline bit
- 1 flash bit

Dot data is fetched from external memory in the same way that DRCS data is retrieved. All characters are displayed as a 6×10 dot matrix, with both one and two bits/dot modes available. In the one bit/dot mode, the external dot memory need only be eight bits wide. When using 10 lines/row, 204 different character matrices may be stored in a 2K8 memory.

The flash mode incorporates color table flash. For maximum flexibility of display the foreground and background colors are applied to different areas of the color map.

Full-Field DRCS

For alphageometric and similar applications, a bit-map display is desirable, where each pixel on the screen corresponds to a location in the memory. APDC implements this indirectly by expanding the DRCS character repertoire so that the entire defined display area can be covered with fully random data.

One chapter (1K16) of DRCS memory can contain data for 51 $6 \times 10 \times 4$ (6 pixels wide, 10 pixels high, 4 bits per pixel) characters, sufficient for two complete character columns. If after these two columns have been scanned, the DRCS chapter is incremented to a new area of memory, a further two columns can be covered with different random data.

This method of using 20 contiguous chapters of display memory and incrementing the DRCS chapter latch in synchronism with the horizontal scan forms the basis of the full-field DRCS mode. All DRCS modes, on-chip ROM-based characters, and attributes are still available.

If, for example, a less memory-intensive DRCS mode, such as $12 \times 10 \times 1$, is desired, then the necessary 10 chapters can be addressed by omitting the least significant chapter bit (A11) from the memory address.

MICROPROCESSOR AND RAM INTERFACE

Three types of data transfer take place at the bus interface:

- APDC fetches data from the display memory
- The microprocessor reads from, or writes to, APDC internal register map
- The microprocessor accesses the display memory

APDC Access to Display Memory

APDC accesses the external display memory via a 16-bit multiplexed address and data bus with a 500ns cycle time. Figure 7 shows a rudimentary RAM interface circuit and bus timing diagram. When APDC accesses the display memory, its Address Strobe signal $\overline{AS}$ flags the bus cycle and writes the address into the '373 latches. The display RAMs, shown in Figure 10 as two 8-bit blocks, are enabled with Upper Data Strobe, $\overline{UDS}$, and Lower Data Strobe, $\overline{LDS}$, respectively. (APDC never actually fetches a single byte from memory; $\overline{UDS}$ and $\overline{LDS}$ are always asserted together to fetch a 16-bit word.) The Read/Write control signal, R/$\overline{W}$, is included for completeness although APDC only reads the display memory.

Although the APDC data bus is 16 bits wide, the data fetched is often considered to exist in terms of bytes and so the byte addressing convention is important. The standard adopted is that of the 68000 microprocessor where the even-numbered bytes exist on the left or upper (most significant) part of the bus, as shown in Figure 8. The word addresses are numerically the same as the upper byte they contain — there are no odd-numbered word addresses.

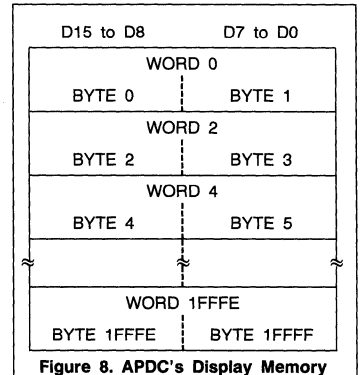

Figure 8. APDC's Display Memory Word/Byte Organization

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Warning Time

Because APDC is a real-time display device, it must have direct access to the display memory with priority over the controlling microprocessor or other peripheral devices. To achieve this, APDC issues a Bus Request $\overline{BR}$ signal for the duration of the memory access plus a programmable advance warning time to allow the microprocessor to complete its current bus cycle.

In systems where the microprocessor's bus and APDC's bus are intimately connected, (a 'connected' system), $\overline{BR}$ may be used to suspend all microprocessor activity so that APDC acts as a dedicated DMA controller. In systems where the two buses are separated by buffers ('disconnected' systems), the $\overline{BR}$ signal may be used either to generate an interrupt or as a directly testable signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of APDC's bus activity is programmable from 0 to 23μs.

Microprocessor Access to APDC's Register Map

The set of internal registers, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of APDC's bus (see Figure 9). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled with Register Enable, $\overline{RE}$. Addresses are input via the lower portion of the bus. A Data Transfer Acknowledge signal $\overline{DTACK}$, is also generated to indicate to the microprocessor that data transfer is complete.

Figure 10 shows the main data and address paths used in a 'connected' 68000 interface. The outputs of the '373 latches are only enabled when the 68000 has yielded the bus in response to Bus Request, $\overline{BR}$. When the register map is accessed, data is transferred via the upper part of the bus, and the microprocessor's low-order address is passed to APDC via the '244 buffer. Simultaneously, the '245 bidirectional buffer disables the signals from the low-order data bus of the 68000.

The '244 and '245 buffers may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by APDC as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of APDC's scroll map contents at some location in main memory.

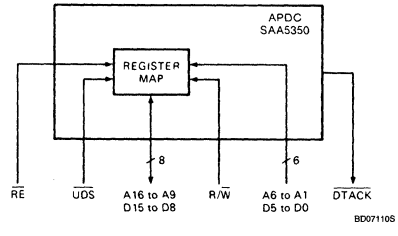


Figure 9. Processor Access to APDC's Internal Register Map

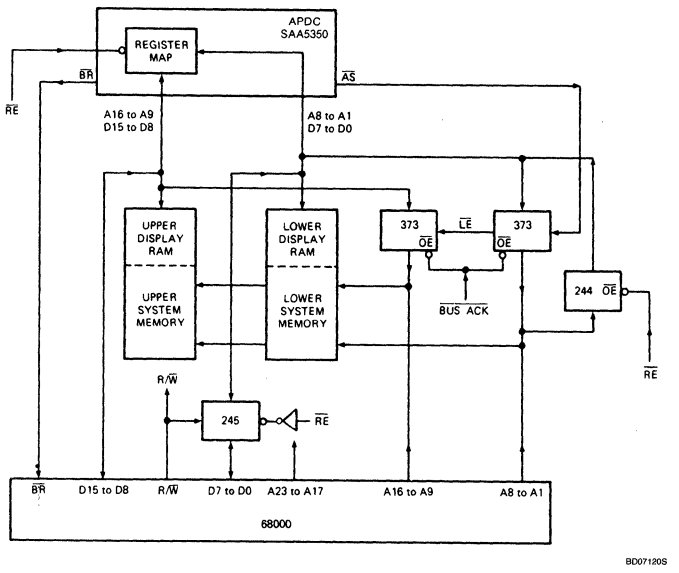


Figure 10. 'Connected' 68000 Interface

8-Bit Microprocessors

Although the control bus is optimized for the 68000, APDC will operate with a number of widely different industry-standard 8- and 16-(or more) bit microprocessors such as 80(1)88, 68008, 8051, etc. The interfacing of 8-bit microprocessors to the 16-bit wide display memory is simplified by APDC's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd byte) half of the display RAM. The link-through buffer is enabled with Buffer Enable, $\overline{BUFEN}$, and its Send/Receive direction is controlled by $\overline{S}$/R which is physically the same APDC pin as R/$\overline{W}$.

Figure 11 shows the main data and address paths used in a 'connected' 8-bit microprocessor interface. This is very similar to the 68000 interface but it should be noted that the display memory does not receive A0 as an address, rather A0 (when high) is used as the major enabling signal for $\overline{BUFEN}$.

Disconnected Systems

For many applications it may be desirable to 'disconnect' APDC and the display RAM from the microprocessor and its ROM, RAM, and peripherals. The two parts of the system then operate independently and communicate only when the microprocessor accesses APDC's register map or the display memory. Figure 12 shows the rudiments of such an 8-bit system; it can be seen that the main data and address paths are essentially the same as those described above, the only difference being the addition of a set of isolating buffers.

Synchronization

APDC has three synchronization modes. As a stand-alone device (in terminal applications for example, it can output a composite sync signal $\overline{TCS}$ to the display timebase IC or to a monitor. Timing is derived from a 6MHz on-chip oscillator with an external crystal as shown in Figure 13a.

APDC can also sync directly to another device, such as the $\overline{TCS}$ signal from the SAA5240 teletext IC or another APDC, as

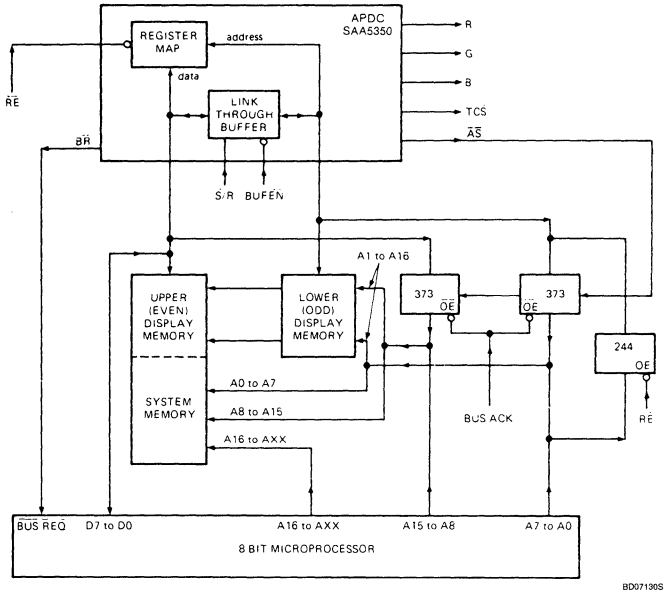


Figure 11. 'Connected' 8-Bit Microprocessor Interface

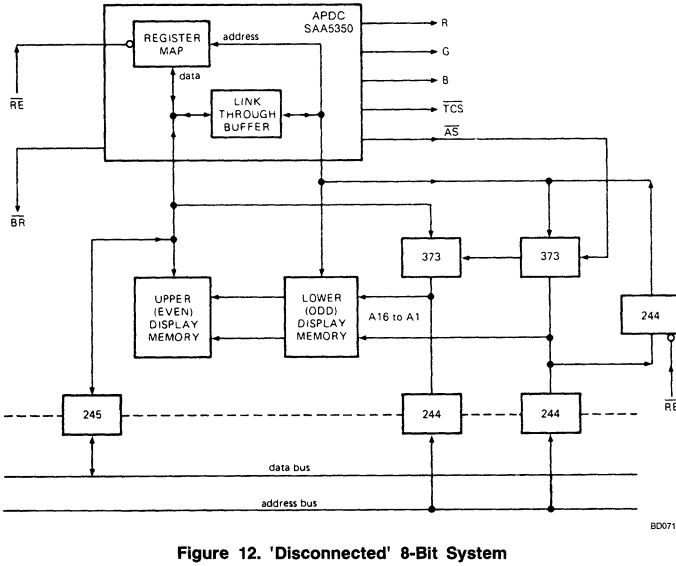
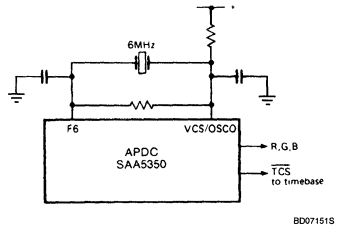


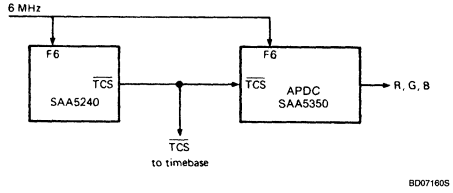
Figure 12. 'Disconnected' 8-Bit System

shown in Figure 13b. APDC's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250ns is built-in to avoid resetting the counter on every TV line, so that screen jitter does not occur. Field synchronization is achieved with APDC's internal field sync separator.

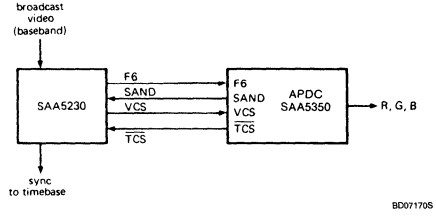
The third mode is phase-locked slave operation, as in Figure 13c. In the SAA5230 video input processor IC, an internal phase-locked VCO provides a 6MHz clock. When APDC is active, its horizontal counter is part of the phase control loop; a horizontal reference is fed back to the SAA5230 via the SAND pin and the vertical reference is generated by feeding separated composite sync via the VCS pin into APDC's field sync separator. In this mode, the display derived from APDC can sync with that from a TV source or a local VLP (laser disc) player, to allow picture-in-text displays, as might be used, for example, in the travel industry.



a. Stand-alone



b. Simple Slave (Direct Sync)



c. Phase-locked Slave (Indirect Sync)

Figure 13. Synchronization Modes

10 lines/row

MODE	PIXEL CONFIGURATION (h × v)	BITS/PIXEL	MAXIMUM NUMBER OF CHARACTERS/CHAPTER*
1	12 × 10	1	102
2	12 × 10	2	51
3	6 × 10	1	2 × 102
4	6 × 10	2	102
5	6 × 10	4	51
6	6 × 5	2	2 × 102
7	6 × 5	4	102

*one chapter contains 1024 16-bit words

12 lines/row

MODE	PIXEL CONFIGURATION	BITS/PIXEL	MAXIMUM NUMBER OF CHARACTERS/CHAPTER*
8	12 × 12	1	85
9	12 × 12	2	42
10	6 × 12	1	2 × 85
11	6 × 12	2	85
12	6 × 12	4	42
13	6 × 6	2	2 × 85
14	6 × 6	4	85

DYNAMICALLY REDEFINABLE CHARACTER SETS (DRCS)

In a basic alphamosaic system, the shape of each character is stored as a dot (pixel) pattern within a defined matrix. Since the repertoire of possible characters within the matrix is finite, simple and inexpensive decoders can be designed. The use of DRCS, however, enormously extends the display repertoire. Using DRCS, additional characters can be defined by the information provider, and then used as part of the character set for a specific page or group of pages. The additional characters can be used singly, or as alphanumerics in a different alphabet, or as symbols in time-tables, etc. They can also be used in groups to create simple designs such as company logos.

In essence DRCS requires the transmission of the dot pattern for each character matrix and the allocation of a code to that matrix. When transmitting a page containing DRCS, the DRCS data can be transmitted independently of the page information and stored in DRCS RAM. For display, both the fixed and the DRCS character tables are used, depending on the character code stored in the page memory.

The DRCS character cell is based on a 12-pixel horizontal resolution. When operating with 10 lines/row, the following modes, each representing different combinations of horizontal, vertical, and color resolutions, are available.

APDC can also operate in a 6 × 10, 4 bits/pixel mode with a memory organization more suited to bit-map implementation.

When operating with 12 lines/row, fewer characters are available per chapter.

All attributes apply to DRCS in the same manner as to normal characters, but for multi-color DRCS (that is, the modes with more than one data bit per pixel) the following rules apply:

- The whole character cell is treated as foreground color
- When the Conceal (or Flash, Invert) attribute is used, the background color that would otherwise be pertaining is displayed
- The Underline attribute has no effect (the one-bit/pixel DRCS modes are underlined as normal alphanumeric characters).

When operating with 2 bits/pixel color DRCS, the DCLUT (DRCS Color Look-up Table) is used. This behaves as a small RAM that maps the four combinations of two bits onto any four of the 32 locations in the color map.

When operating with 4 bits/pixel color DRCS, the 16 combinations can be taken either from locations 0 to 15 or from locations 16 to 31 of the color map depending on the value of a register bit.

The physical organization of APDC's DRCS memory is 1K16 (1024 16-bit words) for Tables 4 and 5, and a further 1K16 for Tables 6 and 7. In addition to the page memory pointer, two independent memory pointers in APDC indicate the beginning of each 1K16 'chapter' of DRCS memory.

STACK CODING

For full implementation of all the required functions in APDC, 32 bits per character location are necessary. This means that to display a full screen of 25 rows of 40 characters, 4kbytes of external memory are required — four times the capacity of a basic alphamosaic decoder memory, excluding any DRCS requirements.

- 7 Bits Character Code
- 3 Bits Character Table
- 5 Bits Foreground Color
- 5 Bits Background Color
- 5 Bits Flash
- 3 Bits Size (D.HT., Top/Bot., D.Width)
- 1 Bit Lining (Underline or Mosaic Separation)
- 1 Bit Conceal
- 1 Bit Invert
- 1 Bit Window/Box

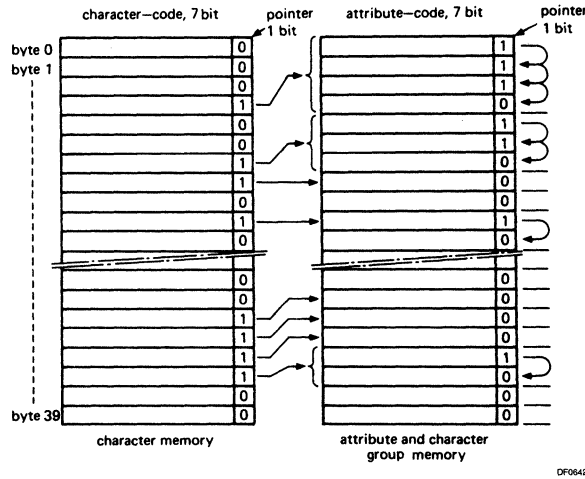
32 Bits per character position

To reduce the amount of memory required, attributes in APDC are coded using a Stack architecture. Such a system exploits the natural redundancy of normal text by allocating memory dynamically. It allows the external memory to be reduced to 2kbytes per screen. This has beneficial side effects; for example, it reduces the memory bandwidth for a given display, reducing the memory speed required or increasing the time available for microprocessor operations.

In the stack coding system used in APDC, the page memory is divided into character and attribute sections, each organized as 40-byte groups. The 40 character bytes and 40 attribute bytes together make up one displayed row.

Each 8-bit byte includes a pointer bit. When the pointer bit of a character byte is set, it indicates the presence of one or more attributes set at the same character position. When the pointer bit of an attribute byte is set, it indicates that there are further attributes in that group. At the beginning of a row, default attributes are set, which are then updated by the attribute bytes fetched from the stack.

An example of stack coding is given in the Figure. The first three characters of the row have clear pointer bits. These characters will be taken from the default group of 128 (on-chip) characters, and will be displayed white on black, normal size, not underlined, etc.



Example of Dynamic Allocation of Memory Using Coding Stack

Stack coding used in APDC

B7	B6	B5	B4	B3	B2	B1	B0	COMMENTS
P	0	0	F4	F3	F2	F1	F0	Foreground color (PIBGR) Transparent = 000000
P	0	1	B4	B3	B2	B1	B0	Background color (PIBGR) Transparent = 00000
P	1	0	H4	H3	H2	H1	H0	Flash
P	1	1	0	L	T2	T1	T0	Character table and lock bit
P	1	1	1	0	0	G	D	Size. double height and width
P	1	1	1	0	1	0	U	Underline (Lining)
P	1	1	1	0	1	1	I	Invert
P	1	1	1	1	0	0	C	Conceal
P	1	1	1	1	0	1	W	Window/Box
P	1	1	1	1	1	0	H	Marked area (not a display attribute)
P	1	1	1	1	1	1	P	Protected area (not a display attribute)

The fourth character in the row has its pointer bit set, and so the first (or, generally, the next) attribute byte is fetched from memory. This byte also has its pointer bit set, and so the next attribute byte is also fetched, and so on.

The fourth attribute byte has a clear pointer bit indicating that it is the last in the group. The next character byte is now fetched. The pointer being clear, this character is displayed with the same attributes as those set for the previous one.

The stack system records only the position in a row where attribute-changes occur, with no restriction upon how many attribute-changes apply to any one character. The restriction to 40 attribute-changes in a row has been carefully studied, and not found in practice to be an editorial limitation.

The actual coding of attributes, a form of Huffman coding, is shown below.

NOTE:
Previously published as "Technical Information 137," ELCOMA, October 1984.

Signetics

Linear Products

Section 14
SMPS for TV/Monitor

INDEX

March, 1987

TDA2582
Control Circuit For Power Supplies

Product Specification

Linear Products

DESCRIPTION

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.

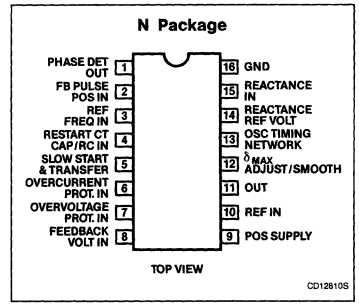
FEATURES

- Voltage-controlled horizontal oscillator
- Phase detector
- Duty factor control for the negative-going transient of the output signal
- Duty factor increases from zero to its normal operation value
- Adjustable maximum duty factor
- Overvoltage and overcurrent protection with automatic restart after switch-off
- Counting circuit for permanent switch-off when n-times overcurrent or overvoltage is sensed
- Protection for open-reference voltage
- Protection for too-low supply voltage
- Protection against loop faults
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1.5V
- Normal and "smooth" remote ON/OFF possibility

APPLICATIONS

- Video monitors
- Power supplies

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−25°C to +80°C	TDA2582N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{9-16}	Supply voltage at Pin 9	14	V
V_{11-16}	Voltage at Pin 11	0 to 14	V
I_{11M}	Output current (peak value)	40	mA
P_{TOT}	Total power dissipation	280	mW
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature	−25 to +80	°C

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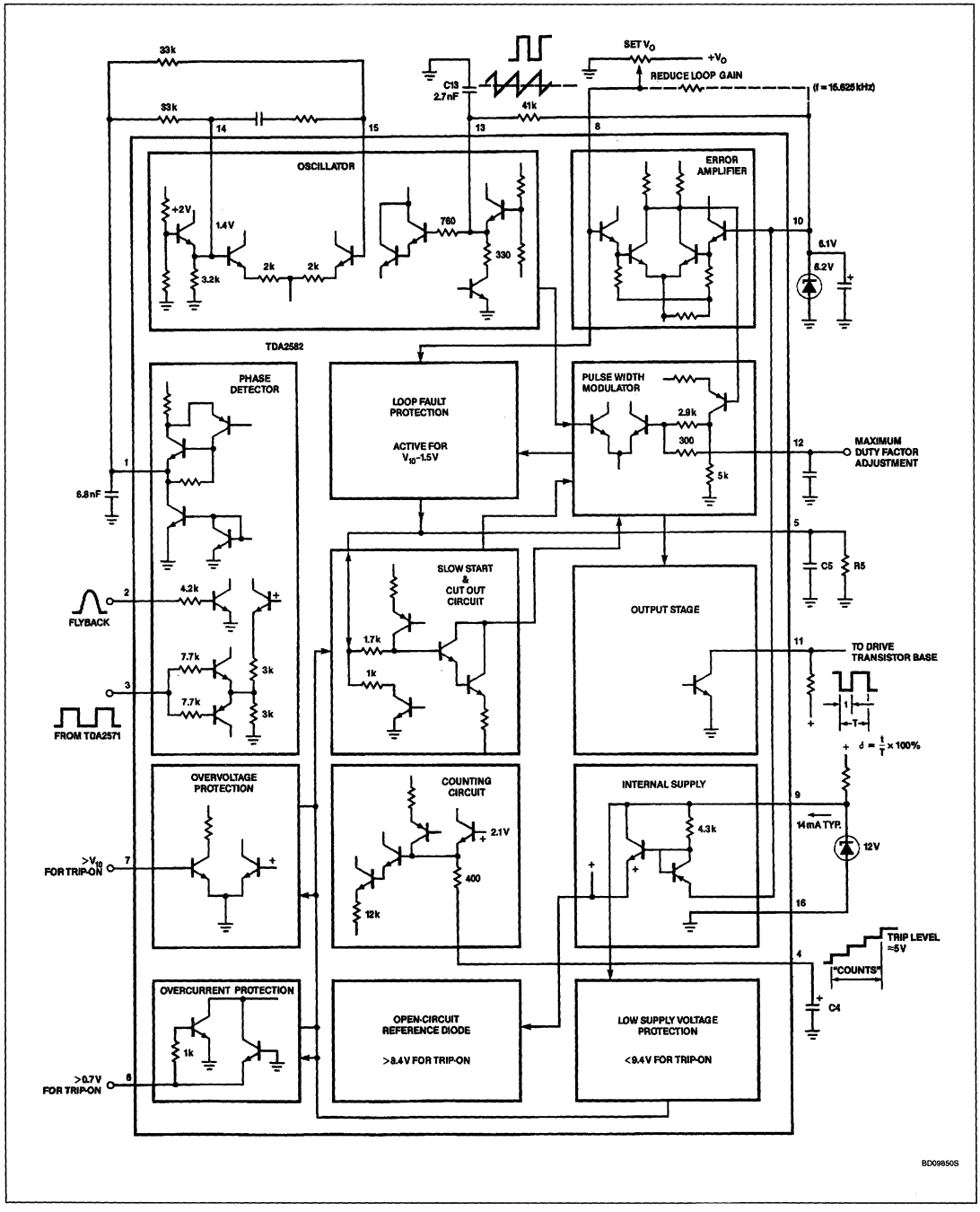
Control Circuit For Power Supplies TDA2582

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; V_{10-16} = 6.1V; T_A = 25°C, measured in Figure 3.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{9-16}	Supply voltage range	10	12	14	V
V_{9-16}	Protection voltage too-low supply voltage	8.6	9.4	9.9	V
I_9	Supply current at δ = 50%		14		mA
I_9	Supply current during protection		14		mA
I_9	Minimum required supply current[1]			17	mA
P	Power consumption		170		mW
Required input signals					
V_{10-16}	Reference voltage[2]	5.6	6.1	6.6	V
$\lvert Z_{8-16} \rvert$	Feedback input impedance		200		kΩ
V_{10-16}	High reference voltage protection: threshold voltage	7.9	8.4	8.9	V
	Horizontal reference signal (square-wave or differentiated; negative transient is reference)				
$V_{3-16(P-P)}$	voltage-driven (peak-to-peak value)	5		12	V
I_{3M}	current-driven (peak value)	−1		1.5	mA
$\pm I_3$	switching-level current			100	μA
V_{2-16}	Flyback pulse or differential deflection current	1		5	V
I_{2M}	Flyback pulse current (peak value)			1.5	mA
$-V_{6-16}$	Overcurrent protection:[3] threshold voltage	600	640	695	mV
$+V_{6-16}$		640	680	735	mV
V_{7-16}	Overvoltage protection: ($V_{REF} = V_{10-16}$) threshold voltage	$V_{REF}-130$	$V_{REF}-60$	$V_{REF}-0$	mV
V_{4-16}	Remote-control voltage; switch-off[4]	5.6			V
V_{4-16}	Remote-control voltage; switch-on			4.5	V
V_{5-16}	'Smooth' remote control; switch-off[5]	4.5			V
V_{5-16}	'Smooth' remote control; switch-on			3	V
I_4	Remote-control switch-off current			1	mA
Delivered output signals					
$V_{11-16(P-P)}$	Horizontal drive pulse (loaded with a resistor of 560Ω to +12V peak-to-peak value	11.6			V
I_{11M}	Output current; peak value			40	mA
	Saturation voltage of output transistor				
V_{CESAT}	at I_{11} = 20mA		200	400	mV
V_{CESAT}	at I_{11} = 40mA			525	mV
δ	Duty factor of output pulse[6]	0		98 ±0.8	%
I_4	Charge current for capacitor on Pin 4		110		μA
I_5	Charge current for capacitor on Pin 5		120		μA
I_{10}	Supply current for reference	0.6	1	1.45	mA

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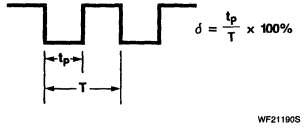
DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 12V; V_{10-16} = 6.1V; T_A = 25°C, measured in Figure 3.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Oscillator					
	Temperature coefficient		0.0003	0.0004	$°C^{-1}$
	Relative frequency deviation for V_{10-16} changing from 5.6 to 6.6V		−1.4	−2	%
	Oscillator frequency spread (with fixed external components)			3	%
	Frequency control sensitivity at Pin 15 f_{NOM} = 15.625kHz		5		kHz/V
Phase control loop					
	Loop gain of APC-system (automatic phase control)[7]		5		kHz/μs
Δf	Catching range (f_{NOM} = 15,625kHz)	1300		2100	Hz
t	Phase relation between negative transient of sync pulse and middle of flyback		1		μs
Δt	Tolerance of phase relation			±0.4	μs

NOTES:

1. This value refers to the minimum required supply current that will start all devices under the following conditions: V_{9-16} = 10V; V_{10-16} = 6.2V; δ = 50%.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical − 1.85mV/°C.
4. See application information Pin 4.
5. See application information Pin 5.
6. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$ (see Figure 1). After switch-on, the duty factor rises gradually from 0% to the steady value. The relationship between V_{8-16} and the duty factor is given in Figure 6 and the relationship between V_{12-16} and the duty factor is shown in Figure 8.
7. For component values, see Block Diagram.



NOTE:

$\delta = \frac{t_p}{T} \times 100\%$.

Figure 1

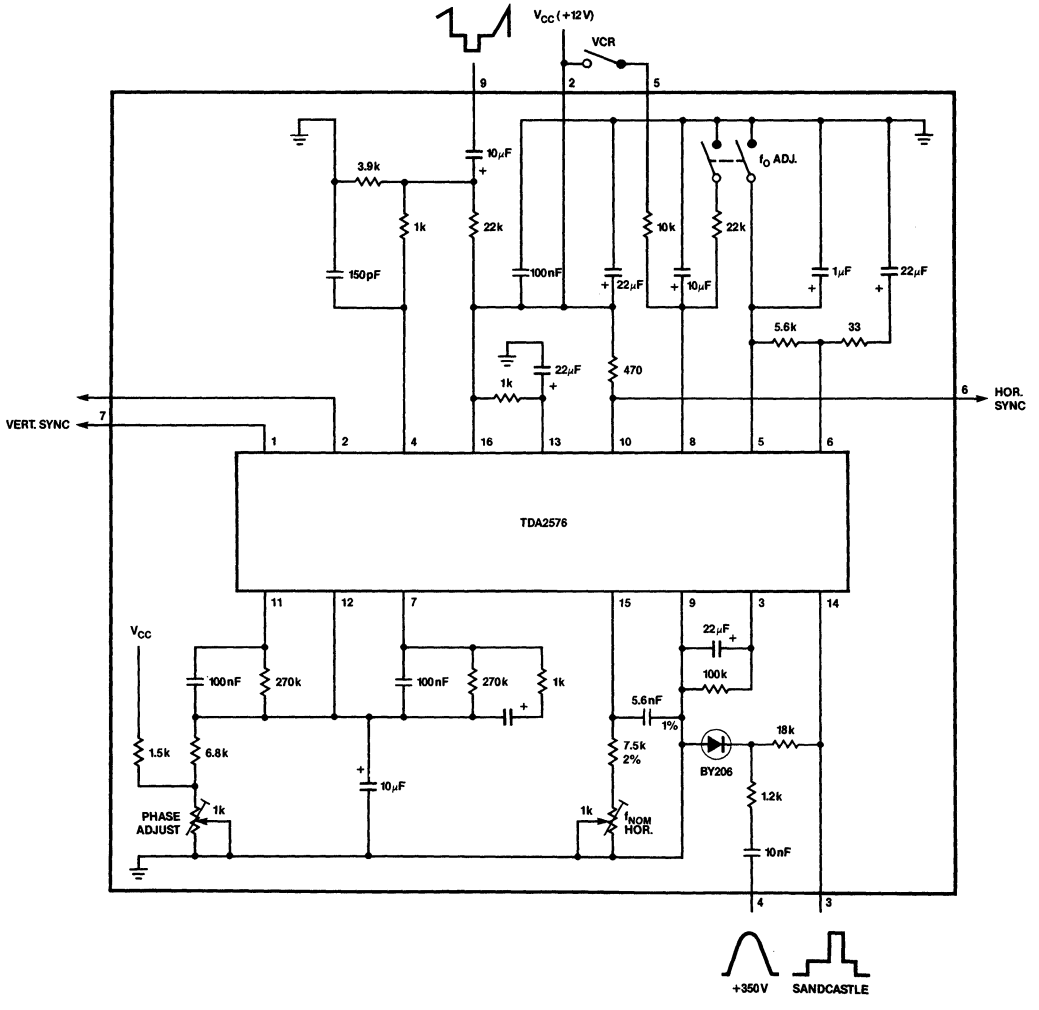


Figure 2a. Lead 6 (Pin 10) of Circuit TDA2576 Connected to Lead 2 (Pin 14) of Circuit TDA2582

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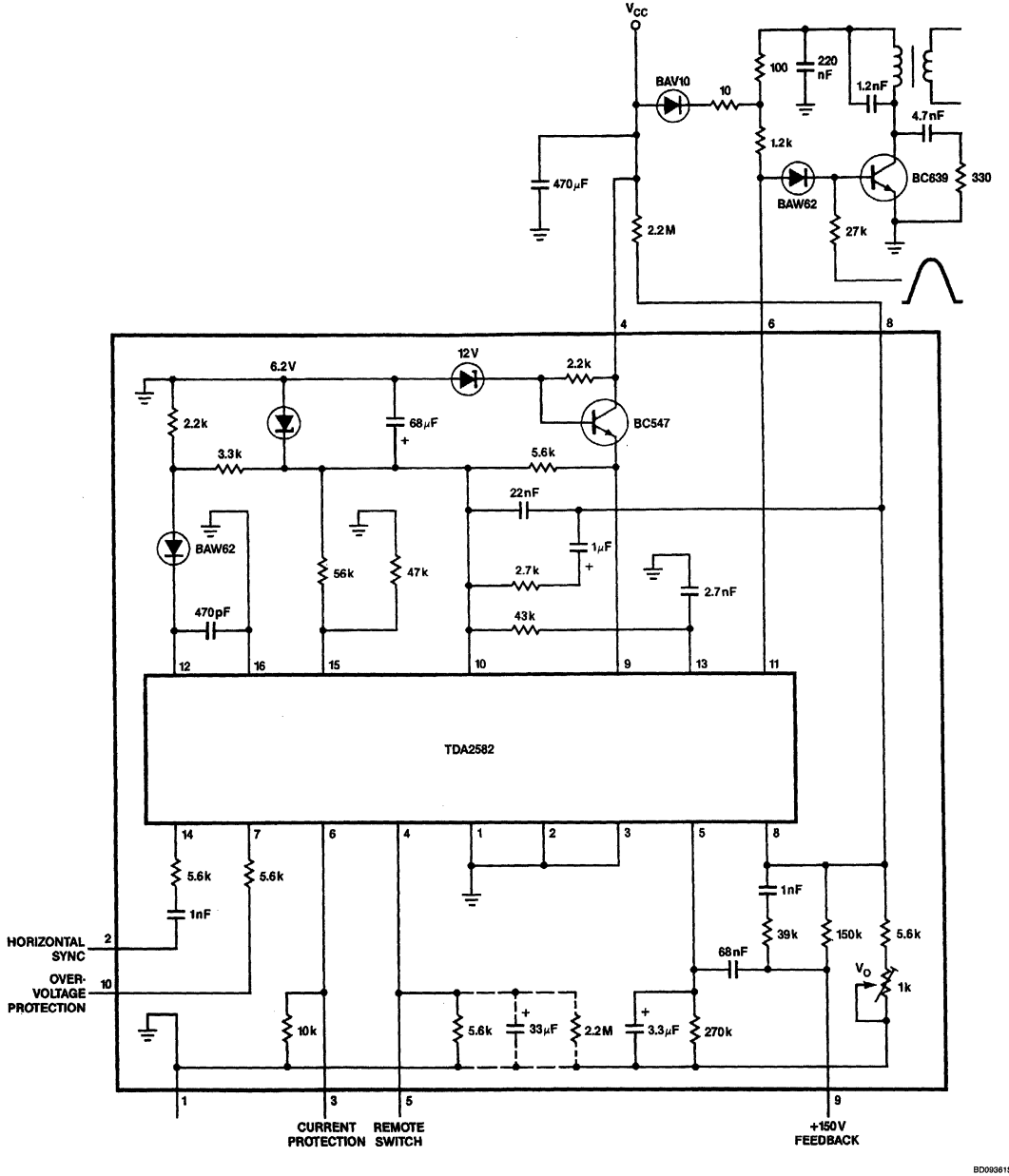
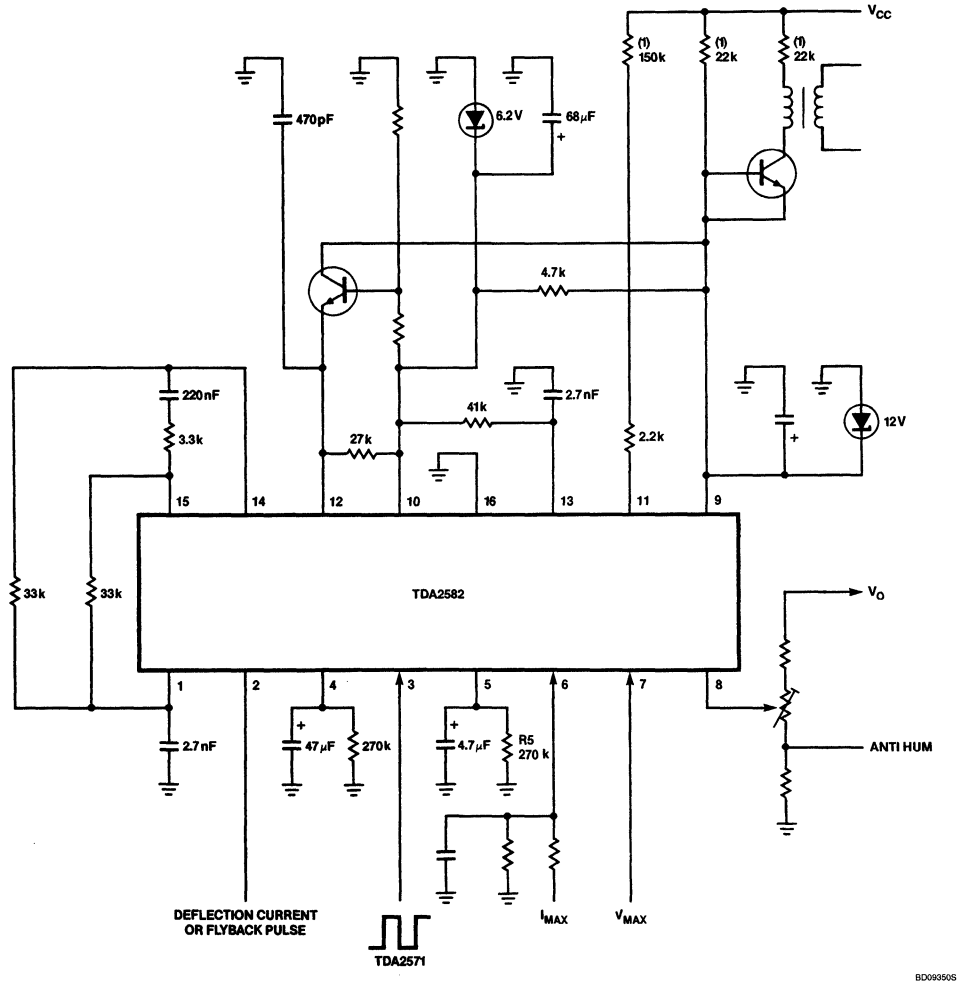


Figure 2b. Lead 6 (Pin 10) of Circuit TDA2576 Connected to Lead 2 (Pin 14) of Circuit TDA2582



NOTE:
1. Values depend on V_{CC}.

Figure 3. Circuit Diagram

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APPLICATION INFORMATION

The function is described beside the corresponding pin number.

1 Phase Detector Output — The output circuit consists of a bidirectional current source which is active for the time that the signal on Pin 2 exceeds 1V.

The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to Pin 3.

With a resistor of 2 × 33kΩ and a capacitor of 2.7nF, the control steepness is 0.55V/μs (Figure 3).

2 Flyback Pulse Input — The signal applied to Pin 2 is normally a flyback pulse with a duration of about 12μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3μs).

The toroidal transformer in Figure 4a is for obtaining a pulse representing the midflyback from the deflection current. The connection of the picture phase information is shown in Figure 4b.

3 Reference Frequency Input — The input circuit can be driven directly by the square-wave output voltage from Pin 8 of the TDA2571.

The negative-going transient switches the current source connected to Pin 1 from positive to negative.

The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables power line isolation). The input circuit switching level is about 3V and the input impedance is about 8kΩ.

4 Restart Count Capacitor/Remote-Control Input —

Counting

An external capacitor (C4 = 47μF) is connected between Pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.

If the protection circuits are required to operate, e.g., overcurrent at Pin 6, the duty factor will be set to zero, thus turning off the power supply.

After a short interval (determined by the time constant on Pin 5), the power supply will be restarted via the slow-start circuit.

If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

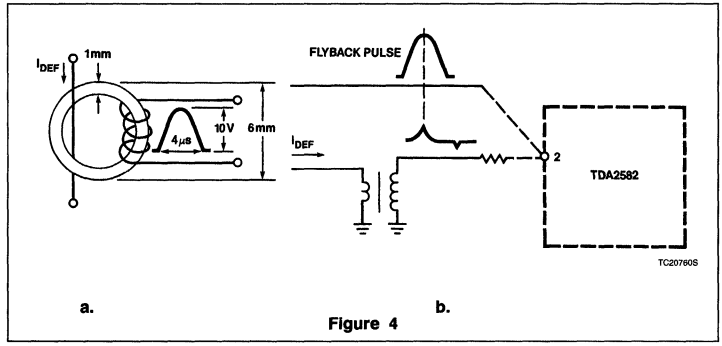

Figure 4

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

Remote Control Input

For this application, the capacitor on Pin 4 has to be replaced by a resistor with a value between 4.7 and 18kΩ. When the externally-applied voltage $V_{4\text{-}16}$ > 5.6V, the circuit switches off; switching on occurs when $V_{4\text{-}16}$ < 4.5V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1.5V.

5 Slow-Start and Transfer Characteristics for Low Feedback Voltage —

Slow-Start

An external shunt capacitor (C5 = 4.7μF) and resistor (R5 = 270kΩ) are connected between Pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer Characteristic for Low Feedback Voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5.

The transfer for three different resistor values is given in Figure 6.

'Smooth' Remote ON/OFF

The ON/OFF information should be applied to Pin 5 via a high-ohmic resistor; a high OFF-level gives a slow rising voltage at Pin 5, which results in a slowly decreasing duty factor.

6 Overcurrent Protection Input — A voltage proportional to the current in the power switching device is applied to the integrated circuit between Pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

7 Over voltage Protection Input — When the voltage applied to this pin exceeds the threshold level, the protection circuit will operate.

The tripping level is about the same as the reference voltage on Pin 10.

8 Feedback Voltage Input — The control loop input is applied to Pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on Pin 10.

Under normal operating conditions, the voltage on Pin 8 will be about equal to the reference voltage on Pin 10. For further information refer to Figures 6 and 7.

9 12V Positive Supply — The maximum voltage that may be applied is 14V. Where this is derived from an unstabilized supply rail, a regulator diode (12V) should be connected between Pins 9 and 16 to ensure that the maximum voltage does not exceed 14V. When the voltage on this pin falls below a minimum of 8.6V (typically 9.4V), the protection circuit will switch off the power supply.

10 Reference Input — An external reference diode must be connected between this pin and Pin 16.

The reference voltage must be between 5.6 and 6.6V. The IC delivers about 1mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between Pins 9 and 10. A higher reference-voltage value up to 7.5V is allowed when use is made of a duty factor limiting resistor < 27kΩ between Pins 12 and 16.

11 Output — An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an NPN transistor with 3 series-connected clamping diodes to the internal 12V supply rail. This provides a low-impedance in the "ON" state, that is, with the drive transistor turned off.

12 Maximum Duty-Factor Adjustment/ Smoothing

Maximum Duty-Factor Adjustment

Pin 12 is connected to the output voltage of the amplitude comparator (V_{10-8}). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on Pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting Pin 12 to the emitter of an NPN transistor used as a voltage source.

Figure 8 plots the maximum duty factor as a function of the voltage applied to Pin 12. If some spread is acceptable, the maximum duty factor can also be limited by connecting a resistor from Pin 12 to Pin 16. A resistor of 12kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470pF between Pins 12 and 16.

13 Oscillator Timing Network — The timing network comprises a capacitor between Pins 13 and 16, and a resistor between Pin 13 and the reference voltage on Pin 10.

The charging current for the capacitor (C13) is derived from the voltage reference diode connected to Pin 10 and discharged via an internal resistor of about 330Ω.

14 Reactance-Stage Reference Voltage — This pin is connected to an emitter-follower which determines the nominal reference voltage for the reactance stage (1.4V for reference voltage $V_{10-16} = 6.1V$). Free-running frequency is obtained when Pins 14 and 15 are short-circuited.

15 Reactance-Stage Input — The output voltage of the phase detector (Pin 1) is connected to Pin 15 via a resistor. The voltage applied to Pin 15 shifts the upper level of the voltage sensor of the oscillator, thus changing the oscillator frequency and phase. The time-constant network is connected between Pins 14 and 15. Control sensitivity is typically 5kHz/V.

16 Negative Supply (Ground)

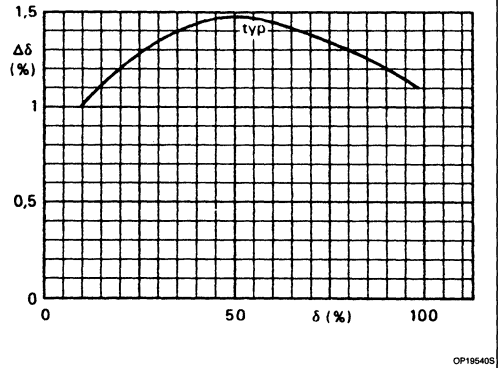

Figure 5. Duty Factor Change as a Function of Initial Duty Factor; at 1mV Error Amplifier Input Change; $\Delta V_{8-10(P-P)} = 1mV$

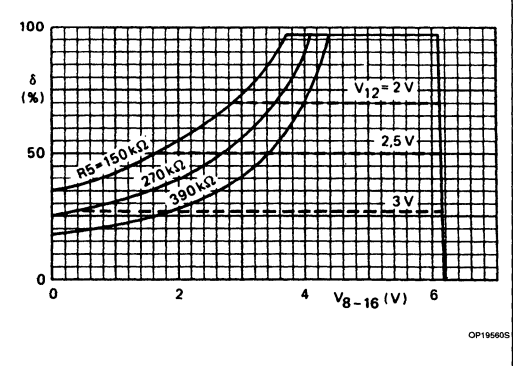

Figure 6. Duty Factor of Output Pulses as a Function of Feedback Input Voltage (V_{8-16}) With R5 as a Parameter and V_{12-16} as a Limiting Value; $V_{10-16} = 6.1V$

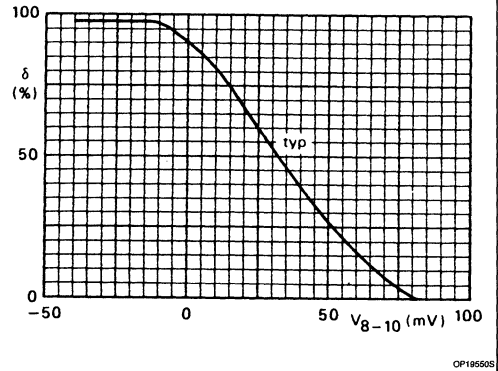

Figure 7. Duty Factor of Output Pulses as a Function of Error Amplifier Input (V_{8-10}); $V_{10-16} = 6.1V$

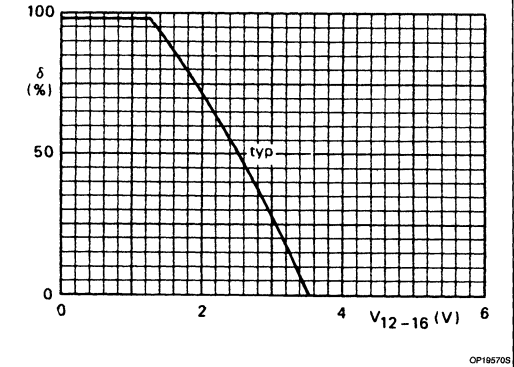

Figure 8. Maximum Duty Factor Limitation as a Function of the Voltage Applied to Pin 12; $V_{10-16} = 6.1V$

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Signetics

TEA1039
Control Circuit for Switched-Mode Power Supply

Product Specification

Linear Products

DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g., a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

FEATURES

- **Wide frequency range**
- **Adjustable input sensitivity**
- **Adjustable minimum frequency or maximum duty factor limit**
- **Adjustable overcurrent protection limit**
- **Supply voltage out-of-range protection**
- **Slow-start facility**

APPLICATIONS

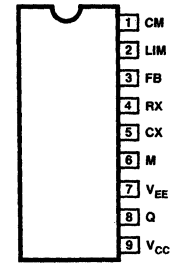
- **Home appliances**
- **Frequency regulation**
- **Flyback converters**
- **Forward converters**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
9-Pin Plastic SIP	−25°C to +125°C	TEA1039U

PIN CONFIGURATION

U Package

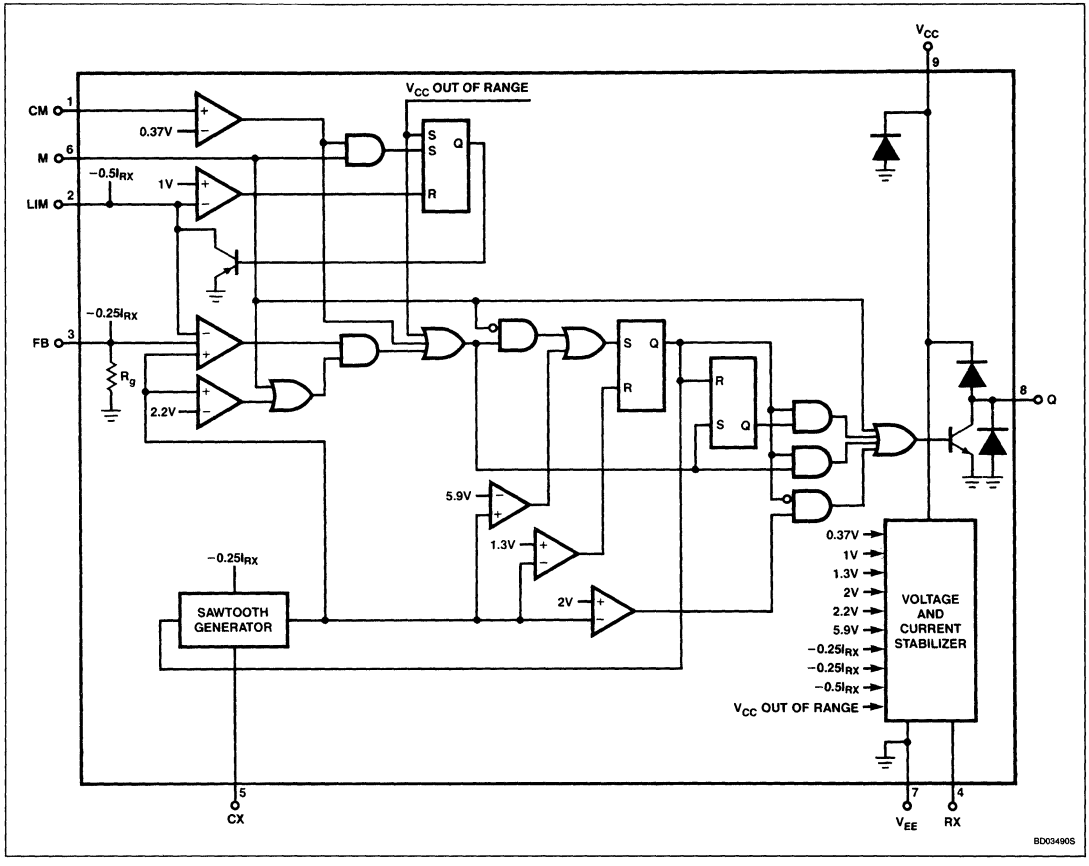


TOP VIEW

CD10370S

PIN NO.	SYMBOL	DESCRIPTION
1	CM	Overcurrent protection input
2	LIM	Limit setting input
3	FB	Feedback input
4	RX	External resistor connection
5	CX	External capacitor connection
6	M	Mode input
7	V_{EE}	Common
8	Q	Output
9	V_{CC}	Positive supply connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range, voltage source	−0.3 to +20	V
I_{CC}	Supply current range, current source	−30 to +30	mA
V_I	Input voltage range, all inputs	−0.3 to +6	V
I_I	Input current range, all inputs	−5 to +5	mA
V_{8-7}	Output voltage range	−0.3 to +20	V
	Output current range		
I_8	output transistor ON	0 to 1	A
I_8	output transistor OFF	−100 to +50	mA
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range (see Figure 1)	−25 to +125	°C
F_D	Power dissipation (see Figure 1)	max. 2	W

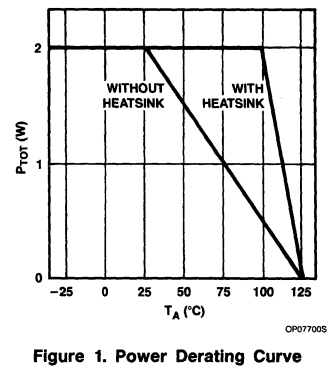


Figure 1. Power Derating Curve

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DC ELECTRICAL CHARACTERISTICS $V_{CC} = 14$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Supply V_{CC} (Pin 9)					
V_{CC}	Supply voltage, operating	11	14	20	V
I_{CC} I_{CC} $\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	Supply current at $V_{CC} = 11V$ at $V_{CC} = 20V$ variation with temperature		7.5 9 −0.3	11 12	mA mA %/°C
V_{CC} $\Delta V_{CC}/\Delta T$	Supply voltage, internally limited at $I_{CC} = 30mA$ variation with temperature	23.5	 18	28.5	V mV/°C
V_{CCmin} $\Delta V_{CC}/\Delta T$	Low supply threshold voltage variation with temperature	9	10 −5	11	V mV/°C
V_{CCmax} $\Delta V_{CC}/\Delta T$	High supply threshold voltage variation with temperature	21	23 10	24.6	V mV/°C
Feedback input FB (Pin 3)					
$V_{3\ 7}$	Input voltage for duty factor = 0; M input open	0		0.3	V
$-I_{FB}$	Internal reference current		0.5 I_{RX}		mA
R_g	Internal resistor R_g		130		kΩ
Limit setting input LIM (Pin 2)					
$V_{2\ 7}$	Threshold voltage		1		V
$-I_{LIM}$	Internal reference current		0.25 I_{RX}		mA
Overcurrent protection input CM (Pin 1)					
$V_{1\ 7}$ $\Delta V_{1\ 7}/\Delta T$	Threshold voltage variation with temperature	300	370 0.2	420	mV mV/°C
t_{PHL}	Propagation delay, CM input to output		500		ns
Oscillator connections RX and CX (Pins 4 and 5)					
$V_{4\ 7}$ $\Delta V_{4\ 7}/\Delta T$	Voltage at RX connection at $-I_4 = 0.15$ to 1mA variation with temperature	6.2	7.2 2.1	8.1	V mV/°C
V_{LS}	Lower sawtooth level		1.3		V
V_{FT}	Threshold voltage for output H to L transition in F mode		2		V
V_{FM}	Threshold voltage for maximum frequency in F mode		2.2		V
V_{HS}	Higher sawtooth level		5.9		V
$-I_{CX}$	Internal capacitor charging current, CX connection		0.25 I_{RX}		mA
f_{OSC}	Oscillator frequency (output pulse repetition frequency)	1		10^5	Hz
$\Delta f/f$ $\frac{\Delta f/f}{\Delta T}$	Minimum frequency in F mode, initial deviation variation with temperature	−10	 0.034	10	% %/°C
$\Delta f/f$ $\frac{\Delta f/f}{\Delta T}$	Maximum frequency in F mode, initial deviation variation with temperature	−15	 −0.16	15	% %/°C

DC ELECTRICAL CHARACTERISTICS (Continued) V_{CC} = 14, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$\Delta t/t$	Output LOW time in F mode, initial deviation	−15		15	%
$\frac{\Delta t/t}{\Delta T}$	variation with temperature		0.2		%/°C
$\Delta f/f$	Pulse repetition frequency in D mode, initial deviation	−10		10	%
$\frac{\Delta f/f}{\Delta T}$	variation with temperature		0.034		%/°C
t_{OLmin}	Minimum output LOW time in D mode at C_5 = 3.6nF		1		µs
$\frac{\Delta t/t}{\Delta T}$	variation with temperature		0.2		%/°C
Output Q (Pin 8)					
$V_{8\ 7}$	Output voltage LOW at I_8 = 100mA		0.8	1.2	V
$\Delta V_{8\ 7}/\Delta T$	variation with temperature		1.5		mV/°C
$V_{8\ 7}$	Output voltage LOW at I_8 = 1A		1.7	2.1	V
$\Delta V_{8\ 7}/\Delta T$	variation with temperature		−1.4		mV/°C

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e., when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (Pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary DC voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode Input M (Pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, Pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

Oscillator Resistor and Capacitor Connections RX and CX (Pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (Pin 5) and ground (V_{EE}, Pin 7), and an external resistor R4 connected between the RX connection (Pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Figure 2). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2.2V. As soon as the capacitor voltage reaches 5.9V the capacitor is discharged rapidly to 1.3V and a new cycle is initiated (see Figures 3 and 4).

For voltages on the FB and LIM inputs lower than 2.2V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1.3V to 5.9V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figures 5 and 6). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback Input FB (Pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit Setting Input LIM (Pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (Pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{MAX} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

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Overcurrent Protection Input CM (Pin 1)

A voltage on the CM input exceeding 0.37V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (Pin 8)

The output is an open-collector NPN transistor, only capable of sinking current. It requires an external resistor to drive an NPN transistor in the SMPS (see Figures 7 and 8).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Figure 1).

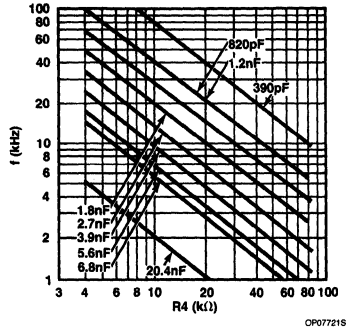
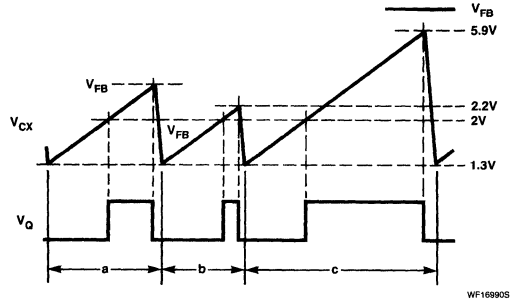
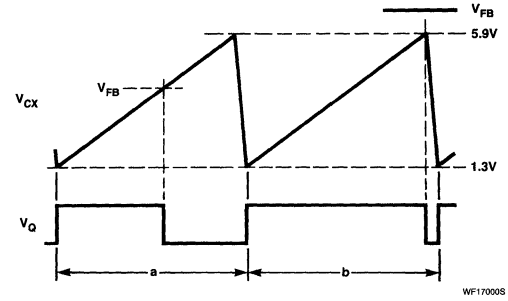


Figure 2. Minimum Pulse Repetition Frequency in the Frequency Regulation Mode, and Working Pulse Repetition Frequency in the Duty Factor Regulation Mode, as a Function of External Resistor R4 Connected Between RX and Ground with External Capacitor C5 Connected Between CX and Ground as a Parameter



NOTES:
a. The voltages on inputs FB or LIM are between 2.2V and 5.9V. The circuit is in its normal regulation mode.
b. The voltage on input FB or input LIM is lower than 2.2V. The circuit works at its maximum frequency.
c. The voltages on inputs FB and LIM are higher than 5.9V. The circuit works at its minimum frequency.

Figure 3. Timing Diagram for the Frequency Regulation Mode Showing the Voltage on External Capacitor C5 Connected between CX and Ground and the Output Voltage as a Function of Time for Three Combinations of Input Signals



NOTES:
a. The voltages on inputs FB or LIM are below 5.9V. The circuit is in its normal regulation range.
b. The voltages on inputs FB and LIM are higher than 5.9V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

Figure 5. Timing Diagram for the Duty Factor Regulation Mode Showing the Voltage on External Capacitor C5 Connected Between CX and Ground and the Output Voltage as a Function of Time for Two Combinations of Input Signals

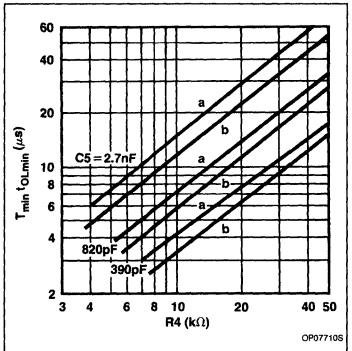


Figure 4. Minimum Output Pulse Repetition Time t_{MIN} (Curves a) and Minimum Output LOW Time t_{OLmin} (Curves b) in the Frequency Regulation Mode as a Function of External Resistor R4 Connected Between RX and Ground with External Capacitor C5 Connected Between CX and Ground as a Parameter

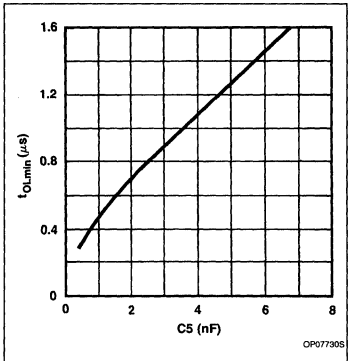


Figure 6. Minimum Output LOW Time t_{OLmin} in the Duty Factor Regulation Mode as a Function of External Capacitor C5 Connected Between CX and Ground. In This Mode the Minimum Output LOW Time is Independent of R4 for Values of R4 Between 4kΩ and 80kΩ

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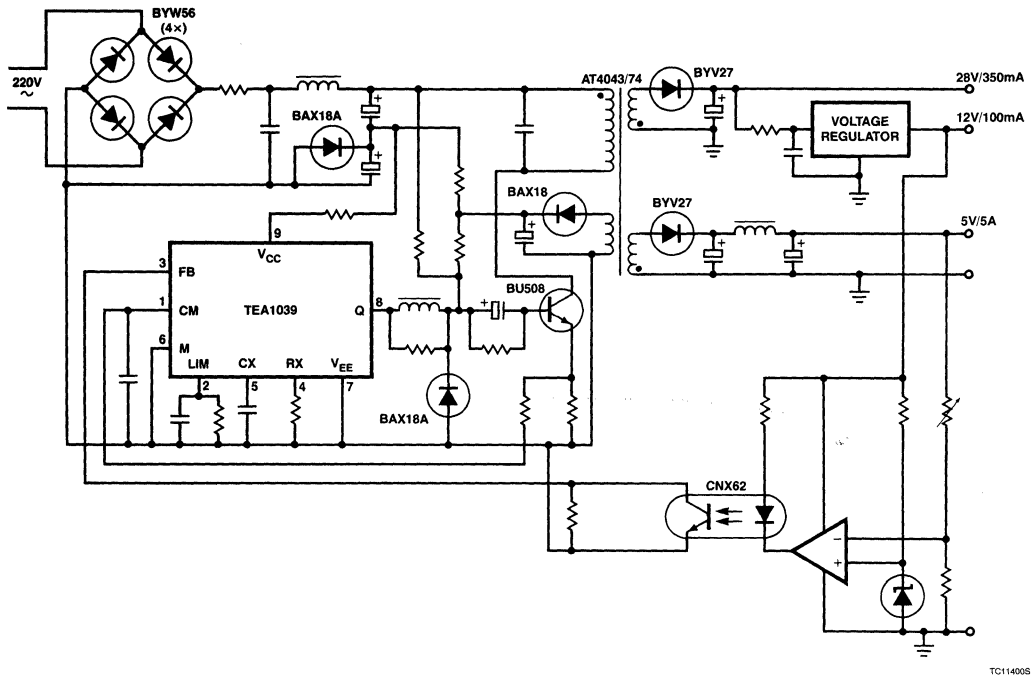
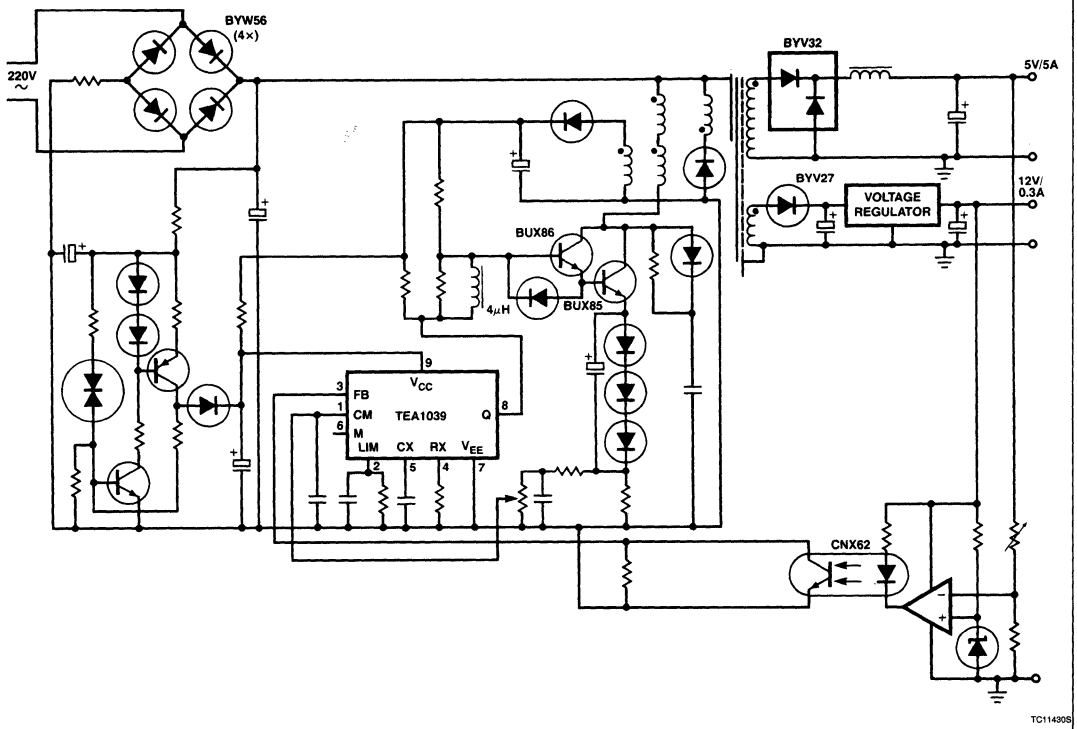


NOTE:
An Optocoupler CNX62 is Used for Voltage Separation.

Figure 7. Typical Application of the TEA1039 in a Variable-Frequency Flyback Converter Switched-Mode Power Supply



NOTE:
An Optocoupler CNX62 is Used for Voltage Separation.

Figure 8. Typical Application of the TEA21039 in a Fixed-Frequency Variable Duty Factor Forward Converter Switched-Mode Power Supply

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Linear Products

Section 15
Packaging Information

INDEX

Substrate Design Guidelines for Surface-Mounted Devices

INTRODUCTION

SMD technology embodies a totally new automated circuit assembly process using a new generation of electronic components: surface-mounted devices (SMDs). Smaller than conventional components, SMDs are placed onto the surface of the substrate, not through it like leaded components. And from this, the fundamental difference between SMD assembly and conventional through-hole component assembly arises; SMD component positioning is relative, not absolute.

When a through-hole (leaded) component is inserted into a PCB, either the leads go through the holes, or they don't. An SMD, however, is placed onto the substrate surface, its position only relative to the solderlands, and placement accuracy is therefore influenced by variations in the substrate track pattern, component size, and placement machine accuracy.

Other factors influence the layout of SMD substrates. For example, will the board be a mixed-print (a combination of through-hole components and SMDs) or an all-SMD design? Will SMDs be on one side of the substrate or both? And there are process considerations, such as: what type of machine will place the components and how will they be soldered?

Using our expertise in the world of SMD technology, this section draws upon applied research in the area of substrate design and manufacture, and presents the basic guidelines to assist the designer in making the transition from conventional through-hole PCB assembly to SMD substrate manufacture.

Designing With SMD

SMD technology is penetrating rapidly into all areas of modern electronic equipment manufacture — in professional, industrial, and consumer applications. Boards are made with conventional print-and-etch PCBs, multilayer boards with thick film ceramic substrates, and with a host of new materials specially developed for SMD assembly.

However, before substrate layout can be attempted, footprints for all components must be defined. Such a footprint will include the combination of patterns for the copper solderlands, the solder resist, and, possibly, the solder paste. So the design of a substrate breaks down into two distinct areas: the SMD footprint definition, and the layout and track routing for SMDs on the substrate.

Each of these areas is treated individually; first, the general aspects of SMD technology, including substrate configurations, placement machines, and soldering techniques, are discussed.

Substrate Configurations

SMD substrate assembly configurations are classified as:

Type I — Total surface mount (all-SMD); substrates with no through-hole components at all. SMDs of all types (SM integrated circuits, discrete semiconductors, and passive devices) can be mounted either on one side, or both sides, of the substrate. See Figure 1a.

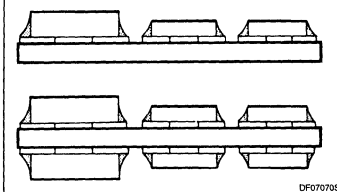
Type IIA — Double-sided mixed-print; substrates with both through-hole components and SMDs of all types on the top, and smaller SMDs (transistors and passives) on the bottom. See Figure 1b.

Type IIB — Underside attachment mixed-print; the top of the substrate is dedicated exclusively to through-hole components, with smaller SMDs (transistor and passives) on the bottom. See Figure 1c.

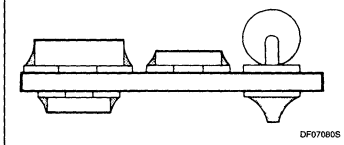
Although the all-SMD substrate will ultimately be the cheapest and smallest variation as there are no through-hole components, it's the mixed-print substrate that many manufacturers will be looking to in the immediate future, for this technique enjoys most of the advantages of SMD assembly and overcomes the problem of non-availability of some components in surface-mounted form.

The underside attachment variation of the mixed-print (type IIB — which can be thought of as a conventional through-hole assembly with SMDs on the solder side) has the added advantages of only requiring a single-sided, print-and-etch PCB and of using the established wave soldering technique. The all-SMD and mixed-print assembly with SMDs on both sides require reflow or combination wave/reflow soldering, and, in most cases, a double-sided or multilayer substrate.

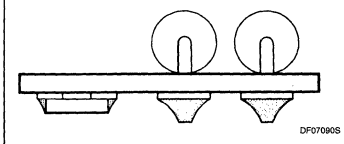
The relatively small size of most SMD assemblies compared with equivalent through-hole designs means that circuits can often be repeated several times on a single substrate. This multiple-circuit substrate technique (shown in Figure 2) further increases production efficiency.



a. Type I — Total Surface-Mount (all-SMD) Substrates



b. Type IIA — Mixed-Print (Double-Sided) Substrate



c. Type IIB — Mixed-Print (Underside Attachment) Substrate

Figure 1

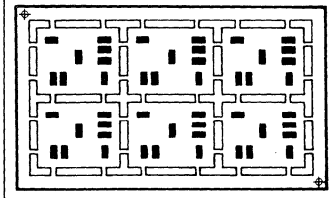


Figure 2. Multiple-Circuit Substrate

Mixed Prints

The possibility of using a partitioned design should be investigated when considering the mixed-print substrate option. For this, part of the circuit would be an all-SMD substrate, and the remainder a conventional through-hole

Substrate Design Guidelines for Surface-Mounted Devices

PCB or mixed-print substrate. This allows the circuit to be broken down into, for example, high and low power sections, or high and low frequency sections.

Automated SMD Placement Machines

The selection of automated SMD placement machines for manufacturing requirements is an issue reaching far beyond the scope of this section. However, as a guide, the four main placement techniques are outlined. They are:

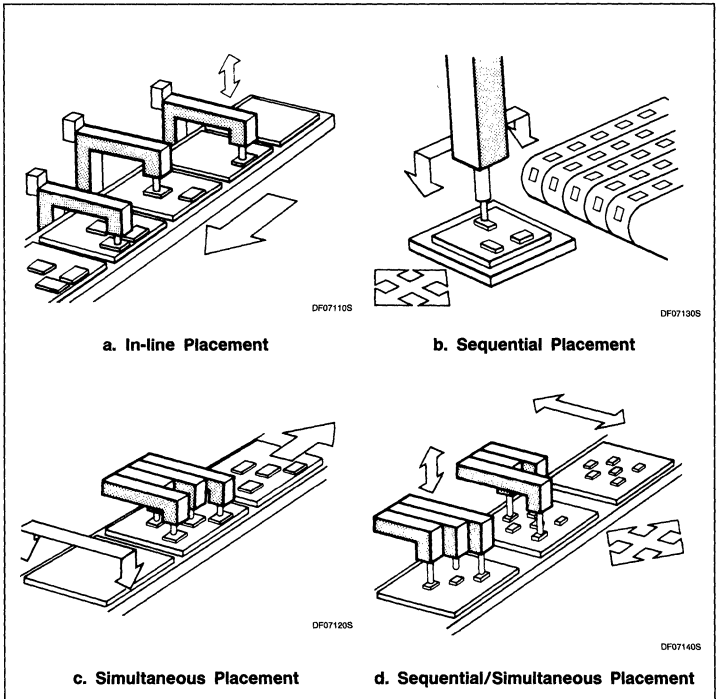
In-Line Placement — a system with a series of dedicated pick-and-place units, each placing a single SMD in a preset position on the substrate. Generally used for small circuits with few components. See Figure 3a.

Sequential Placement — a single pick-and-place unit sequentially places SMDs onto the substrate. The substrate is positioned below the pick-and-place unit using a computer-controlled X-Y moving table (a "software programmable" machine). See Figure 3b.

Simultaneous Placement — places all SMDs in a single operation. A placement module (or station), with a number of pick-and-place units, takes an array of SMDs from the packaging medium and simultaneously places them on the substrate. The pick and place units are guided to their substrate location by a program plate (a "hardware programmable" machine), or by software-controlled X-Y movement of substrate and/or pick-and-place units. See Figure 3c.

Sequential/Simultaneous Placement — a complete array of SMDs is transferred in a single operation, but the pick-and-place units within each placement module can place all devices simultaneously, or individually (sequentially). Positioning of the SMDs is software-controlled by moving the substrate on an X-Y moving table, by X-Y movement of the pick-and-place units, or by a combination of both. See Figure 3d.

All four techniques, although differing in detail, use the same two basic steps: picking the SMD from the packaging medium (tape, magazine, or hopper) and placing it on the substrate. In all cases, the exact location of each SMD must be programmed into the automated placement machine.



a. In-line Placement

b. Sequential Placement

c. Simultaneous Placement

d. Sequential/Simultaneous Placement

Figure 3

Soldering Techniques

The SMD-populated substrate is soldered by conventional wave soldering, reflow soldering, or a combination of both wave and reflow soldering. These techniques are covered at length in another publication entitled *SMD Soldering Techniques*, but, briefly, they can be described as follows:

Wave Soldering — the conventional method of soldering through-hole component assemblies where the substrate passes over a wave (or more often, two waves) of molten solder. This technique is favored for mixed-print assemblies with through-hole components on the top of the substrate, and SMDs on the bottom.

Reflow Soldering — a technique originally developed for thick-film hybrid circuits using a solder paste or cream (a suspension of fine solder particles in a sticky resin-flux base) applied to the substrate which, after component placement, is heated and causes the solder to melt and coalesce. This method is predominantly used for Type I (all-SMD) assemblies.

Combination Wave/Reflow Soldering — a sequential process using both the foregoing techniques to overcome the problems of soldering a double-sided mixed-print substrate with SMDs and through-hole components on the top, and SMDs only on the bottom. (Type IIB).

Footprint Definition

An SMD footprint, as shown in Figure 4, consists of:

- A pattern for the (copper) solderlands
- A pattern for the solder resist
- If applicable, a pattern for the solder cream.

The design for the footprint can be represented as a set of nominal coordinates and dimensions. In practice, the actual coordinates of each pattern will be distributed around these nominal values due to positioning and processing tolerances. Therefore, the coordinates are stochastic; the actual values form a probability distribution, with a mean value (the nominal value) and a standard deviation.

The coordinates of the SMD are also stochastic. This is due to the tolerances of the actual component dimensions and the positional errors of the automated placement machine.

The relative positions of solderland, solder resist pattern, and SMD, are not arbitrary. A number of requirements may be formulated concerning clearances and overlaps. These include:

- Limiting factors in the production of the patterns (for example, the spacing between solderlands or tracks has a minimum value)

Substrate Design Guidelines for Surface-Mounted Devices

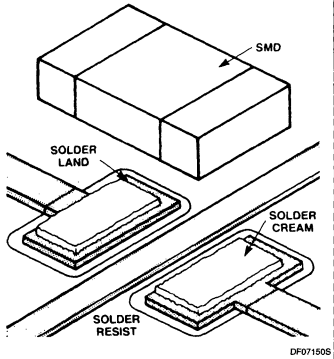


Figure 4. Component Lead, Solder Land, Solder Resist, and Solder Cream "Footprint"

- Requirements concerning the soldering process (for example, the solderlands must be free of solder resist)
- Requirements concerning the quality of the solder joint (for example, the solderland must protrude from the SMD metallization to allow an appropriate solder meniscus)

Mathematical elaboration of these requirements and substitution of values for all tolerances and other parameters lead to a set of inequalities that have to be solved simultaneously. To do this manually using worst-case design is not considered realistic. A better approach is to use a statistical analysis; although this requires a complex computer program, it can be done.

Such an approach may deliver more than one solution, and, if this is so, then the optimal solution must be determined. Optimization is achieved by setting the following objective — find the solution that:

- Minimizes the area occupied by the footprint
- Maximizes the number of tracks between adjacent solderlands.

The final SMD footprint design also depends on the soldering process to be used. The requirements for a wave-soldered substrate differ from those for a reflow-soldered substrate, so each is discussed individually.

Footprints for Wave Soldering

To determine the footprint of an SMD for a wave-soldered substrate, consider four main interactive factors:

- The component dimensions plus tolerances — determined by the component manufacturer
- The substrate metallization — positional tolerance of the solderland with respect to a reference point on the substrate
- The solder resist — positional tolerance of the solder resist pattern with respect to the same reference point
- The placement tolerance — the ability of an automated placement machine to accurately position the SMD on the substrate.

The coordinates of patterns and SMDs have to meet a number of requirements. Some of these have a general validity (the minimum overlap of SMD metallization and solderland) and available space for solder meniscus. Others are specifically required to allow successful wave soldering. One has to take into account factors like the "shadow effect" (missing of joints due to high component bodies), the risk of solder bridging, and the available space for a dot of adhesive.

The "Shadow Effect"

In wave soldering, the way in which the substrate addresses the wave is important. Unlike wave soldering of conventional printed boards where there are no component bodies to restrict the wave's freedom to traverse across the whole surface, wave soldering of SMD substrates is inhibited by the presence of SMDs on the solder-side of the board. The solder is forced around and over the SMDs as shown in Figure 5a, and the surface tension of the molten solder prevents its reaching the far end of the component, resulting in a dry-joint downstream of the solder flow. This is known as the "shadow effect."

The shadow effect becomes critical with high component bodies. However, wetting of the solderlands during wave soldering can be improved by enlarging each land as shown in Figure 5b. The extended substrate metallization makes contact with the solder and allows it to flow back and around the component metallization to form the joint.

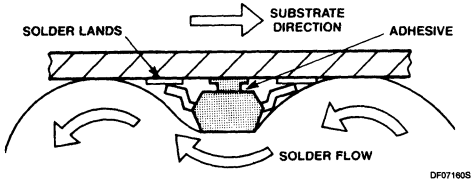
The use of the dual-wave soldering technique also partially alleviates this problem because the first, turbulent wave has sufficient upward pressure to force solder onto the component metallization, and the second, smooth wave "washes" the substrate to form good fillets of solder. Similarly, oil on the surface of the solder wave lowers the surface tension, (which lessens the shadow effect), but this technique introduces problems of contaminants in the solder when the oil decomposes.

Footprint Orientation

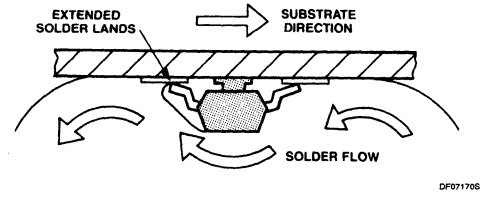
The orientation of SO (small outline) and VSO (very small outline) ICs is critical on wave-soldered substrates for the prevention of solder bridge formation. Optimum solder penetration is achieved when the central axis of the IC is parallel to the flow of solder as shown in Figure 6a. The SO package may also be transversely oriented, as shown in Figure 6b, but this is totally unacceptable for the VSO package.

Solder Thieves

Even with parallel mounted SO and VSO packages, solder bridges have a tendency to form on the leads downstream of the solder flow. The use of solder thieves (small squares of substrate metallization), shown in Figure 7 for a 40-pin VSO, further reduces the likelihood of solder-bridge formation.



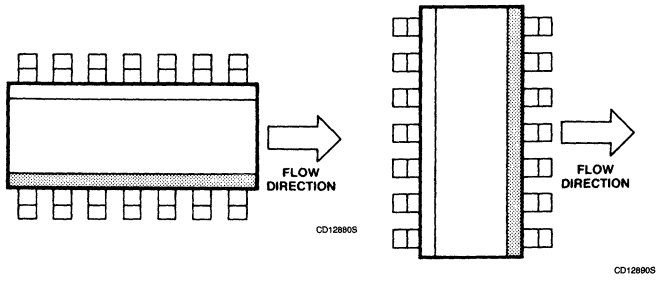
a. Surface Tension Can Prevent the Molten Solder From Reaching the Downstream End of the SMD, Known as the "Shadow Effect"



b. Extending the Solder Lands to Overcome the Shadow Effect

Figure 5

Substrate Design Guidelines for Surface-Mounted Devices



a. Parallel Orientation for SO and VSO Packages

b. Transverse Orientation for SO Packages Only

Figure 6

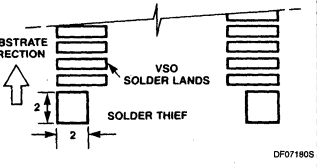


Figure 7. Example of Solder Thieves for VSO-40 Footprints (Dims in mm)

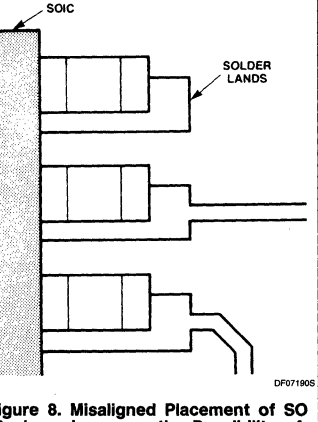


Figure 8. Misaligned Placement of SO Package Increases the Possibility of Solder Bridging

Placement Inaccuracy

Another major cause of solder bridges on SO ICs and plastic leaded chip carriers (PLCCs) is a slight misalignment as shown in Figure 8. The close spacing of the leads on these devices means that any inaccuracy in placement drastically reduces the space between adjacent pins and solderlands, thus increasing the chance of solder bridges forming.

Dummy Tracks for Adhesive Application

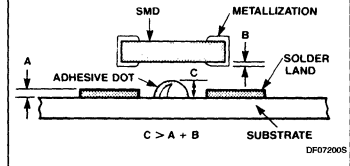
For wave soldering, an adhesive to affix components to the substrate is required. This is necessary to hold the SMDs in place between the placement operation and the soldering process (this technique is covered at length in another publication entitled *Adhesive Application and Curing*).

The amount of adhesive applied is critical for two reasons: first, the adhesive dot must be high enough to reach the SMD, and, second, there mustn't be too much adhesive which could foul the solderland and prevent the formation of a solder joint. The three parameters governing the height of the adhesive dot are shown in Figure 9. Although this diagram illustrates that the minimum requirement is $C > A + B$, in practice, $C > 2(A + B)$ is more realistic for the formation of a good strong bond.

Taking these parameters in turn, the substrate metallization height (A) can range from about 35μm for a normal print-and-etch PCB to 135μm for a plated through-hole board. And the component metallization height (B) (on 1206-size passive devices, for example) may differ by several tens of microns. Therefore, A + B can vary considerably, but it is desirable to keep the dot height (C) constant for any one substrate.

The solution to this apparent problem is to route a track under the device as shown in Figure 10. This will eliminate the substrate metallization height (A) from the adhesive dot-height criteria. Quite often, the high component density of SMD substrates necessitates the routing of tracks between solderlands, and, where it does not, a short dummy track should be introduced.

For bonding small outline (SO) ICs to the substrate, two dots of adhesive are sufficient for SO-8, -14, and -16 packages, but the SOL-20, -24, -28, and VSO-40 packages need three dots. The through-tracks (or dummy tracks) must be positioned beneath the IC accordingly to support the adhesive dots.



NOTES:
A = Substrate metallization height
B = SMD metallization height
C = Height of adhesive dot

Figure 9. Adhesive Dot Height Criteria

Footprints for Reflow Soldering

To determine the footprint of an SMD for a reflow-soldered substrate, there are now five interactive factors to consider: the four that affect the wave solder footprints (although the solder resist may be omitted), plus an additional factor relating to the solder cream application (the positional tolerance of the screen-printed solder cream with respect to the solderlands).

Solder Cream Application

In reflow soldering, the solder cream (or paste) is applied by pressure syringe dispensing or by screen printing. For industrial purposes, screen printing is the favored technique because it is much faster than dispensing.

Screen Printing

A stainless steel mesh coated with emulsion (except for the solderland pattern where cream is required) is placed over the substrate. A squeegee passes across the screen and forces solder cream through the uncoated areas of the mesh and onto the solderland. As a result, dots of solder cream of a given height and density (in mg/mm^2) are produced.

There is an optimum amount of solder cream for each joint. For example, the solder cream requirements for the C1206 SM capacitor are around 1.5mg per end; the SO IC requires between 0.5 and 0.75mg per lead.

The solder cream density, combined with the required amount of solder, makes a demand upon the area of the solderland (in mm^2). The footprint dimensions for the solder cream pattern are typically identical to those for the solderlands.

Substrate Design Guidelines for Surface-Mounted Devices

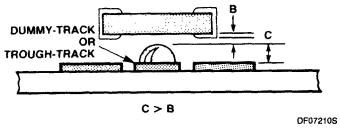


Figure 10. Through-Track or Dummy Track to Modify Dot Height Criteria

Floating

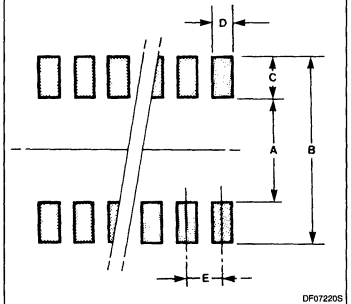
One phenomenon sometimes observed on reflow-soldered substrates is that known as "floating" (or "swimming"). This occurs when the solder paste reflows, and the force exerted by the surface tension of the now molten solder "pulls" the SMD to the center of the solderland.

When the solder reflows at both ends simultaneously, the swimming phenomenon results in the SMD self-centering on the footprint as the forces of surface tension fight for equilibrium. Although this effect can remove minor positional errors, it's not a dependable feature and cannot be relied upon. Components must always be positioned as accurately as possible.

Footprint Dimensions

The following diagrams (Fig. 11 to 19) show footprint dimensions for SO ICs, the VSO-40 package, PLCC packages, and the range of surface-mounted transistors, diodes, resistors, and capacitors. All dimensions given are based on the criteria discussed in these guidelines.

Please note — these footprints are based on our experience with both experimental and actual production substrates and are reproduced for guidance only. Research is constantly going on to cover all SMDs currently available and those planned for in the future, and data will be published when in it becomes available.



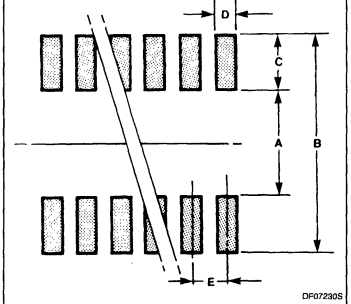
PACKAGE OUTLINE	INCHES A	B	C	D	E
SO-8, 14, 16	.155	.275	.060	.024	.050
SOL-16, 20, 24, 28	.310	.450	.070	.024	.050

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
SO SMALL	4.0	7.0	1.5	.6	1.27
SO LARGE	7.8	11.4	1.8	.6	1.27

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
SOL-8	9.0	13.2	2.1	.6	1.27

PACKAGE OUTLINE	INCHES A	B	C	D	E
SOL-8	.36	.528	.084	.024	.050

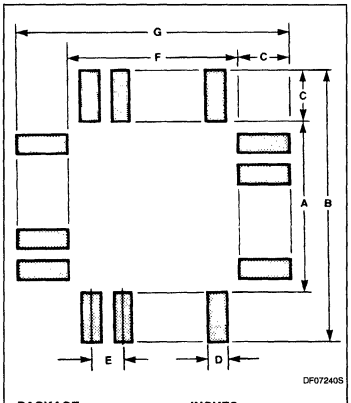
Figure 11. Footprints for SO ICs



PACKAGE OUTLINE	INCHES A	B	C	D	E
VSO-40	.32	.536	.108	.02	.030
VSO-56	.46	.676	.108	.02	.030

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E
VSO-40	8.0	13.4	2.7	.5	.762
VSO-56	11.5	16.9	2.7	.5	.75

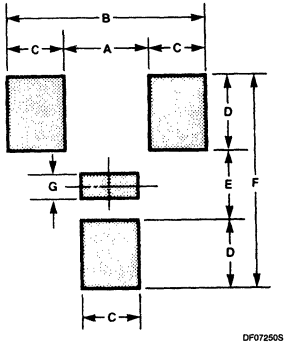
Figure 12. Footprints for VSO ICs



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
PLCC-20	.260	.440	.090	.024	.050	.260	.440
PLCC-28	.360	.540	.090	.024	.050	.360	.540
PLCC-44	.560	.740	.090	.024	.050	.560	.740
PLCC-52	.660	.840	.090	.024	.050	.660	.840
PLCC-68	.860	1.040	.090	.024	.050	.860	1.040
PLCC-84	1.060	1.240	.090	.024	.050	1.060	1.240
PLCC-32	.360	.540	.090	.024	.050	.460	.640

Figure 13. Footprints for PLCCs

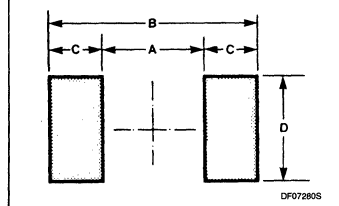
Substrate Design Guidelines for Surface-Mounted Devices



SOT-23	INCHES A	B	C	D	E	F
Reflow	0.048	0.104	0.028	0.044	0.104	—
Wave	0.032	0.136	0.052	0.052	0.048	0.152

SOT-23	METRIC (mm) A	B	C	D	E	F
Reflow	1.2	2.6	0.7	1.1	2.6	—
Wave	0.8	3.4	1.3	1.3	1.2	3.8

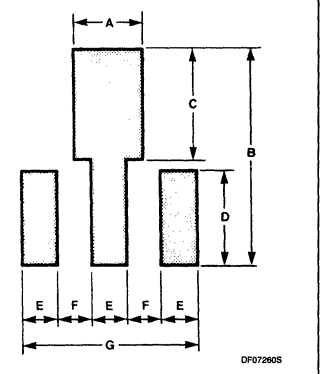
Figure 14. Footprints for SOT-23 Transistors



SOD-80	INCHES A	B	C	D
Reflow	0.096	0.208	0.056	0.056
Wave	0.10	0.2	0.05	0.08

SOD-80	METRIC (mm) A	B	C	D
Reflow	2.4	5.2	1.4	1.4
Wave	2.5	5.0	1.25	2.0

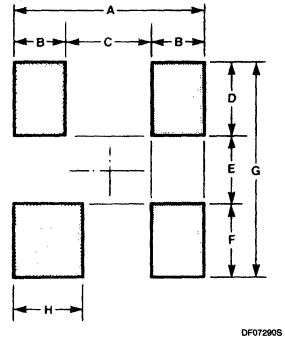
Figure 15. Footprints for SOD-80 Diodes



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G
SOT-89	0.08	0.184	0.104	0.048	0.032	0.028	0.152

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E	F	G
SOT-89	2.0	4.6	2.6	1.2	0.8	0.7	3.8

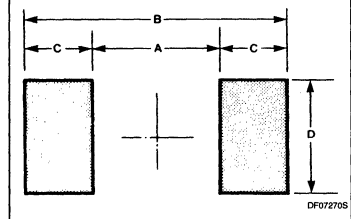
Figure 16. Footprints for Reflow-Soldered SOT-89 Transistors



PACKAGE OUTLINE	INCHES A	B	C	D	E	F	G	H
SOT-143	0.104	0.028	0.048	0.036	0.044	0.036	0.116	0.044

PACKAGE OUTLINE	METRIC (mm) A	B	C	D	E	F	G	H
SOT-143	2.6	0.7	1.2	0.9	1.1	0.9	2.0	1.1

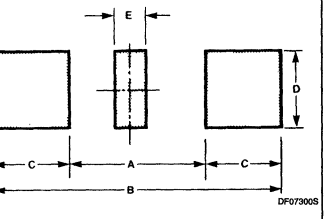
Figure 17. Footprints for Reflow-Soldered SOT-143 Transistors



CODE	SIZE	INCHES A	B	C	D
C0805	0.08 × 0.05	0.032	0.136	0.052	0.056
R/C1206	0.128 × 0.064	0.072	0.184	0.056	0.068
C1210	0.128 × 0.1	0.072	0.184	0.056	0.104
C1808	0.18 × 0.08	0.112	0.248	0.068	0.084
C1812	0.18 × 0.128	0.112	0.248	0.068	0.132
C2220	0.228 × 0.2	0.16	0.296	0.068	0.204

CODE	SIZE	METRIC (mm) A	B	C	D
C0805	2.0 × 1.25	0.8	3.4	1.3	1.4
R/C1206	3.2 × 1.6	1.8	4.6	1.4	1.7
C1210	3.2 × 2.5	1.8	4.6	1.4	2.6
C1808	4.5 × 2.0	2.8	6.2	1.7	2.1
C1812	4.5 × 3.2	2.8	6.2	1.7	3.3
C2220	5.7 × 5.0	4.0	7.4	1.7	5.1

Figure 18. Footprints for Reflow-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors



CODE	SIZE	INCHES A	B	C	D	E
C0805	0.08 × 1.05	0.048	0.144	0.048	0.048	0.016
R/C1206	0.128 × .064	0.08	0.192	0.056	0.056	0.020

CODE	SIZE	METRIC (mm) A	B	C	D	E
C0805	2.0 × 1.25	1.2	3.6	1.2	1.2	0.4
R/C1206	3.2 × .6	2.0	4.8	1.4	1.4	0.5

Figure 19. Footprints for Wave-Soldered Surface-Mounted Resistors and Ceramic Multilayer Capacitors

Substrate Design Guidelines for Surface-Mounted Devices

Layout Considerations

Component orientation plays an important role in obtaining consistent solder-joint quality. The substrate layout shown in Figure 20 will result in significantly better solder joints than a substrate with SMD resistors and capacitors positioned parallel to the solder flow.

Component Pitch

The minimum component pitch is governed by the maximum width of the component and the minimum distance between adjacent components. When defining the maximum component width, the rotational accuracy of the placement machine must also be considered. Figure 21 shows how the effective width of the SMD is increased when the component is rotated with respect to the footprint by angle $\phi°$. (For clarity, the rotation is exaggerated in the illustration.)

The minimum permissible distance between adjacent SMDs is a figure based upon the gap required to avoid solder-bridging during the wave soldering process. Figure 22 shows how this distance and the maximum component width are combined to derive the basic expression for calculating the minimum pitch (F_{MIN}).

As a guide, the recommended minimum pitches for various combinations of two sizes of SMDs, the R/C1206 and C0805 (R or C designating resistor or capacitor respectively; the number referring to the component size), are given in Table 1. These figures are statistically derived under certain assumed boundary conditions as follows:

- Positioning error (Δp)± 0.3mm; (± 0.012")
- Pattern accuracy (Δq)± 0.3mm; (± 0.012")
- Rotational accuracy (ϕ)± 3°
- Component metallization/solderland overlap (M_{MIN}) 0.1mm (0.004") (Note this figure is only valid for wave soldering)
- The figure for the minimum permissible gap between adjacent components (G_{MIN}) is taken to be 0.5mm (0.020").

As these calculations are not based on worst-case conditions, but on a statistical analysis of all boundary conditions, there is a certain flexibility in the given data.

For example, it is possible to position R/C1206 SMDs on a 2.5mm pitch, but the probability of component placements occurring with G_{MIN} smaller than 0.5mm will increase; hence, the likelihood of solder-bridging also increases. Each application must be assessed on individual merit with regard to acceptable levels of rework, and so on.

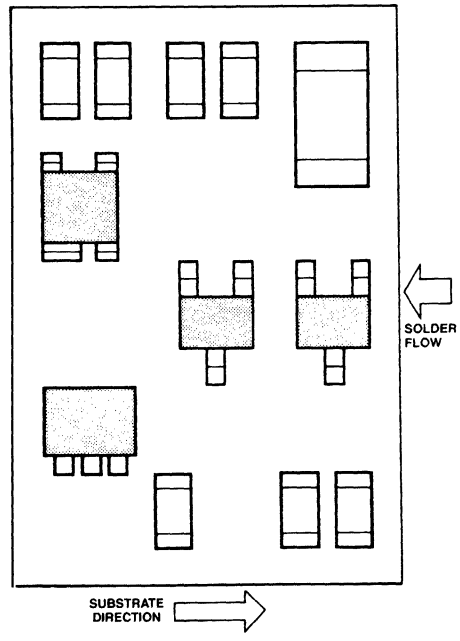
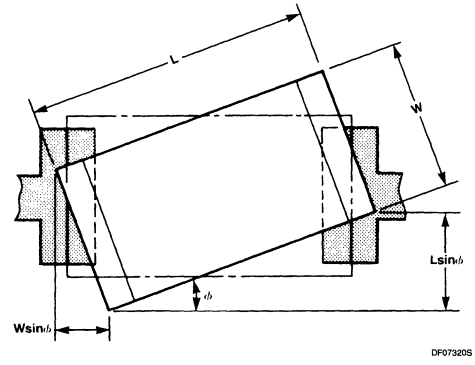


Figure 20. Recommended Component Orientation for Wave-Soldered Substrates



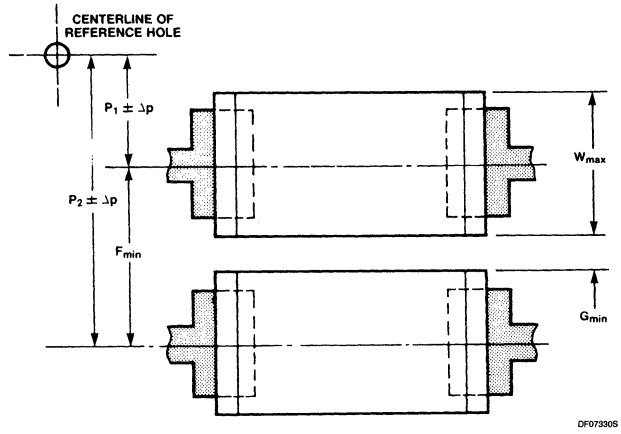
NOTES:
ϕ = Component rotation with respect to footprint
L sin ϕ = Effective increase in width
W sin ϕ = Effective increase in length

Figure 21. The Influence of Rotation of the SMD With Respect to the Footprint

Solderland/Via Hole Relationship

With reflow-soldered multilayer and double-sided, plated through-hole substrates, there must be sufficient separation between the via holes and the solderlands to prevent a solder well from forming. If too close to a solder joint, the via hole may suck the molten solder away from the component by capillary action; this results in insufficient wetting of the joint.

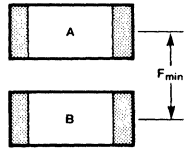
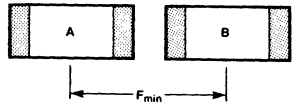
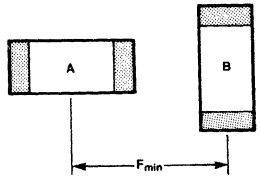
Substrate Design Guidelines for Surface-Mounted Devices



NOTES:
W_{MAX} = Maximum width of component
G_{MIN} = Minimum permissible gap
F_{MIN} = Minimum pitch
P_1 = Nominal position of component 1 (tolerance Δp)
P_2 = Nominal position of component 2 (tolerance Δp)
$F_{MIN} = W_{MAX} + 2\Delta p + G_{MIN}$

Figure 22. Criteria for Determining the Minimum Pitch of SMDs

Table 1. Recommended Pitch For R/C1206 and C0805 SMDs

Combination	Component A	Component B	
		R/C1206	C0805
	R/C1206 C0805	3.0(0.12") 2.8(0.112")	2.8(0.112") 2.6(0.0104")
	R/C1206 C0805	5.8(0.232") 5.3(0.212")	5.3(0.212") 4.8(0.192")
	R/C1206 C0805	4.1(0.164") 3.6(0.144")	3.7(0.148") 3.0(0.12")

Solderland/Component Lead Relationship

Of special consideration for mixed-print substrate layout is the location of leaded components with respect to the SMD footprints and the minimum distance between a protruding clinched lead and a conductor or SMD. Figure 23 shows typical configurations for R/C1206 SMDs mounted on the underside of a substrate with respect to the clinched leads of a leaded component. Minimum distances between the clinched lead ends and the SMDs or substrate conductors are 1mm (0.04") and 0.5 (0.02") respectively.

Placement Machine Restrictions

There are two ways of looking at the distribution of SMDs on the substrate: uniform SMD placement and non-uniform SMD placement. With nonuniform placement, center-to-center dimensions of SMDs are not exact multiples of a predetermined dimension as shown in Figure 24a, so the location of each is difficult to program into the machine.

Uniform placement uses a modular grid system with devices placed on a uniform center-to-center spacing. (For example, 2.5 (0.1") or 5mm (0.2") as shown in Figure 24b.) This placement has the distinct advantage of establishing a standard and enables the use of other automated placement machines for future production requirements without having to redesign boards.

Substrate Population

Population density of SMDs over the total area of the substrate must also be carefully considered, as placement machine limitations can create a "lane" or "zone" that restricts the total number of components which can be placed within that area on the substrate.

For example, on a hardware-programmable simultaneous placement machine (see Figure 3c), each pick-and-place unit within the placement module can only place a component on the substrate in a restricted lane (owing to

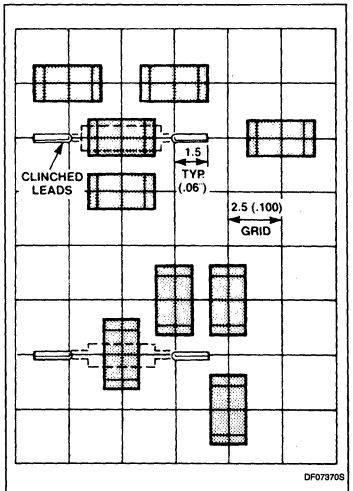
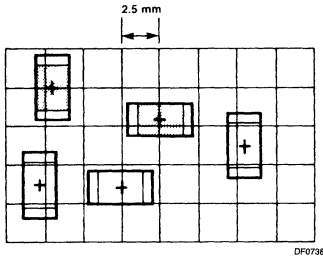
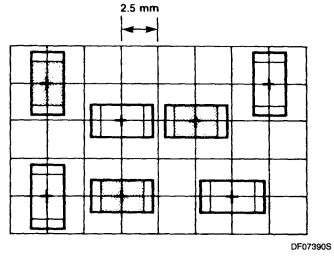


Figure 23. Location of R/C1206 SMDs on the Underside of a Mixed-Print Substrate with Respect to the Clinched Leads of Through-Hole Components (Dimensions in mm)

Substrate Design Guidelines for Surface-Mounted Devices



a. Non-Uniform Component Placement



b. Uniform Component Placement

Figure 24

adjacent pick-and-place units), typically 10 to 12mm (0.4" to 0.48") wide, as shown in Figure 25.

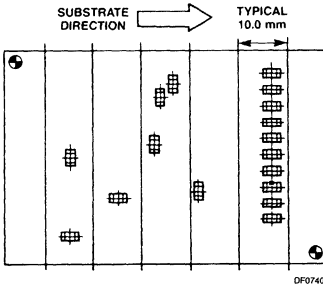


Figure 25. Substrate "Lanes" From Use of a Simultaneous Placement Machine

Placement of the 10 components in the lane on the right of the substrate shown will require a machine with 10 placement modules (or ten passes beneath a single placement module), an inefficient process considering that there are no more than three SMDs in any other lane.

Test Points

Siting of test points for in-circuit testing of SMD substrates presents problems owing to the fewer via holes, higher component densities, and components on both sides of SMD substrates. On conventional double-sided PCBs, the via holes and plated-through component lead-holes mean that most test-points are accessible from one side of the board. However, on SMD substrates, extra provision for test-points may have to be made on both sides of the substrate.

Figure 26a shows the recommended approach for positioning test-points in tracks close to components, and Figure 26b shows an acceptable (though not recommended) alternative where the solderland is extended to accommodate the test pin. This latter method avoids sacrificing too much board space, thus maintaining a high-density layout, but can introduce the problem of components moving ("floating") when reflow-soldered. The approach shown in Figure 26c is totally unacceptable since the pressure applied by the test pin can make an open-circuit soldered joint appear to be good, and, more importantly, the test pin can damage the metallization on the component, particularly with small SMDs.

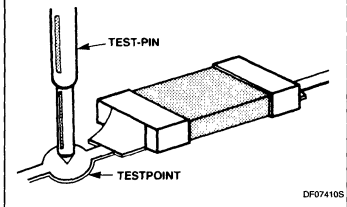
CAD Systems for SMD Substrate Layout

At present, about half of all PCBs are laid out using computer-aided design (CAD) techniques, and this proportion is expected to rise to over 90% by 1988. Of the many current CAD systems available for designing PCB layouts for conventional through-hole components and ICs in DIL packages, few are SMD-compatible, and systems dedicated exclusively to SMD substrate layout are still comparatively rare. There are two main reasons for this: some CAD suppliers are waiting for SMD technology to fully mature before updating their systems to cater to SMD-loaded substrates, and others are holding back until standard package outlines are fully defined.

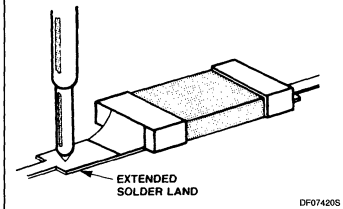
However, updating CAD systems used for through-hole printed boards is not simply a case of substituting SMD footprints for conventional component footprints, since SMD-populated substrates impose far tougher restraints on PCB layout and require a total rethink of the layout programs. For example, systems must deal with higher component densities, finer track widths, devices on both sides of the substrate (possibly occupying corresponding positions on opposite sides), and even SMDs under conventional DILs on the same side of the substrate.

The amount of reworking that a program requires depends on whether it's an interactive (manual) system, or one with fully automatic routing and placement capabilities. For interactive systems, where the user positions the components and routes the tracks manually on-screen, program modifications will be minimal. Automatic systems, however, must contend with the stricter design rules for SMD substrate layout. For example, many autorouting programs assume that every solderland is a plated through-hole and, therefore, can be used as a via hole. This is not applicable for SMD-populated substrates.

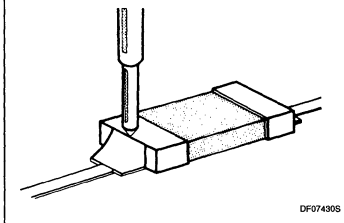
CAD programs base the substrate layout on a regular grid. This method, analogous to drawing the layout on graph paper, must have the grid lines on a pitch that is no larger than the smallest component or feature (track width, pitch, and so on). For conventional DIL boards, this is typically 0.635mm (0.025"), but with the much smaller SMDs, a grid spacing of 0.0254mm (0.001") is required. Consequently, for the same area of substrate, a CAD system based on this finer grid requires



a. RECOMMENDED Test Point Location Close to an SMD



b. Acceptable Test Point Location



c. UNACCEPTABLE Test Point Location

Figure 26

Substrate Design Guidelines for Surface-Mounted Devices

a resolution more than 600 times greater than that required for conventional-layout CAD systems.

To handle this, extra memory capacity can be added, or the allowable substrate area can be limited. In fact, the small size of SMDs, and the high-density layouts possible, generally result in a smaller substrate. However, high-density layout gives rise to additional complications not directly related to the SMD substrate design guidelines. Most CAD systems, for instance, cannot always completely route all interconnects, and some traces have to be routed manually. This can be particularly difficult with the fewer via holes and smaller component spacing of SMD boards.

Ideally, the CAD program should have a "tear-up and start again" algorithm that allows it to restart autorouting if a previous attempt reaches a position where no further traces can be routed before an acceptable percentage of interconnects (and this percentage must first be determined) have been made. This minimizes the manual reworking required.

CAE/CAD/CAM Interaction

Computer-aided production of printed boards has evolved from what was initially only a computer-aided manufacturing process (CAM — digitizing a manually-generated layout and using a photoplotter to produce the artwork) to fully-interactive computer-aided engineering, design, and manufacture using a common database. Figure 27 illustrates how this multi-dimensional interaction is particularly well-suited to SMD-populated substrate manufacture in its highly-automated environment of pick-and-place assembly machines and test equipment.

Using a fully-integrated system, linked by local area network to a central database, will make it possible to use the initial computer-aided engineering (CAE — schematic design, logic verification, and fault simulation) in the generation of the final test patterns at the end of the development process. These test patterns can then be used with the automatic test equipment (ATE) for functional testing of the finished substrates.

Such a system is particularly useful for testing SMD-populated substrates, as their high component density and fewer via-holes make in-circuit testing ("bed of nails" approach) difficult. Consequently, manufacturers are turning to functional testing as an alternative. These aspects are covered in another publication entitled *Functional Testing and Repair.*

Substrate Design Guidelines for Surface-Mounted Devices

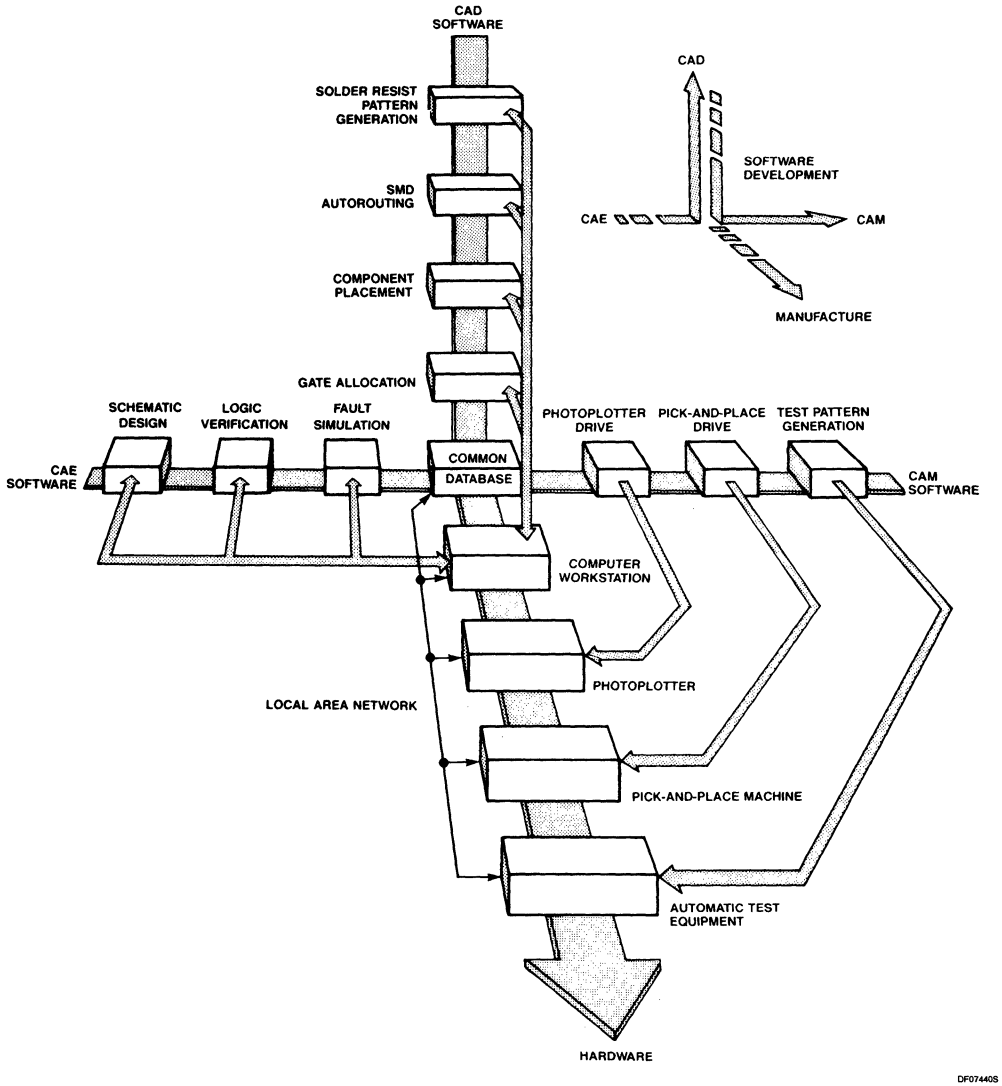


Figure 27. The Software-Hardware Interaction for the Computer-Aided Engineering, Design, and Manufacture of SMD Substrates

15

AN INTRODUCTION

The key questions that must be asked of any electronic circuit are "does it work, and will it continue to do so over a specified period of time?" Until zero-defect soldering is achieved, and all components are guaranteed serviceable by the vendors, manufacturers can only answer these questions by carrying out some form of test on the finished product.

The types of tests, and the depth to which they are carried out, are determined by the complexity of the circuit and the customer's requirements. The amount of rework to be performed on the circuit will depend on the results of these tests and the degree of reliability demanded. The criteria are true of all electronic assemblies, and the test engineer must formulate test schedules accordingly.

Substrates loaded with surface mounted devices (SMDs), however, pose additional problems to the test engineer. The devices are much smaller, and substrate population density is greater, leading to difficulty in accessing all circuit nodes and test points. Also SMD substrate layout designs often have fewer via and component lead holes, so test points may not all be on one side of the substrate and double-sided test fixtures become necessary.

To achieve the high throughput rates made possible by using highly automated SMD placement machines and volume soldering techniques, automatic testing becomes a necessity. Visual inspection of the finished substrate by trained inspectors can normally detect about 90% of defects. With the correct combination of automatic test equipment, the remainder can be eliminated. In this publication, we hope to provide the manufacturer with information to enable him to evaluate and select the best combination of test equipment and the most effective test methods for his product.

BARE-BOARD TESTING

Although SMD substrates will undoubtedly be smaller than conventional through-hole substrates and have less space between conductors, the principles of bare-board testing remain the same. Many of the testers already in use can, with little or no modification, be used for SMD substrates. As this is already a well-established and well-documented practice, it will not be discussed further in this publication, but it is recommended that bare-board testing always be used as the first step in assuring board integrity.

POST-ASSEMBLY TESTING

Testing densely populated substrates is no easy task, as the components may occupy both sides of the board and cover many of the circuit nodes (see Figure 1 for the three main types of SMD-populated substrates). Unlike conventional substrates, on which all test points are usually accessible from the bottom, SMD assemblies must be designed from the start with the siting of test points in mind. Probing SMD substrates is particularly difficult owing to the very close spacing of components and conductors.

Mixed print or all-SMD assemblies with components on both sides further aggravate the testing problems, as not all test points are present on the same side of the board. Although two-sided test fixtures are feasible, they are expensive and require considerable time to build.

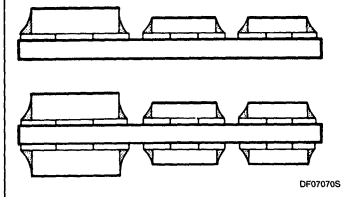
The application of a test probe to the top of an SMD termination could damage it, and probe pressure on a poor or open solder joint can force contact and thus allow a defective joint to be assessed as good. Figure 2a illustrates the recommended siting of test points close to SMD terminations, and Figure 2b shows an alternative, though not recommended, option. Here, problems could arise from reflow soldering (solder migrating from the joint) unless the test point area is separated from the solder land area with a stripe of solder resist. Excessive mechanical pressure caused by too many probes concentrated in a small area may also result in substrate damage.

It is good practice for substrates to have test points on a regular grid so that conventional, rather than custom, testers may be used. If the substrate has tall components or heat-sinks, the test points must be located far enough away to allow the probes to make good contact. All test points should be solder coated to provide good electrical contact. Via holes may also be used as test points, but the holes must be filled with solder to prevent the probe from sticking.

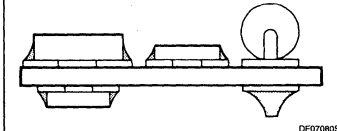
AUTOMATIC TEST EQUIPMENT (ATE)

As manufacturers strive to increase production, the question becomes not whether to use automatic test engineering (ATE), but which ATE system to use and how much to spend on it. Because of the rapid fall in price of computers, memories, and peripherals, today's low-cost ATE equals the performance of the high-cost equipment of just two or three years ago. For factory automation, manufacturers must consider many factors, such as production volume, product complexity, and availability of skilled personnel.

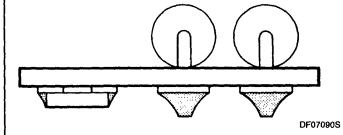
One question is whether the ATE system can be used not only for production testing but also for service and repair to reduce the high cost of keeping a substrate inventory in the field. Another is whether assembly and process-induced faults represent a significant percentage of production defects, rather than out-of-tolerance components. These questions need to be answered before deciding on the type of ATE system required.



a. Type I — Total Surface Mount (All-SMD) Substrates



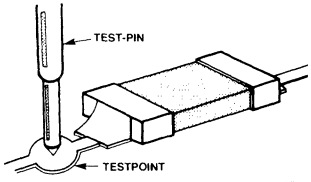
b. Type IIA — Mixed Print (Double-Sided) Substrate



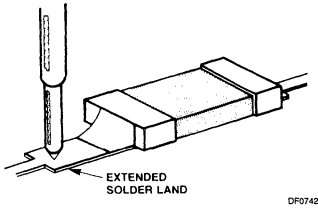
c. Type IIB — Mixed Print (Underside Attachment) Substrate

Figure 1

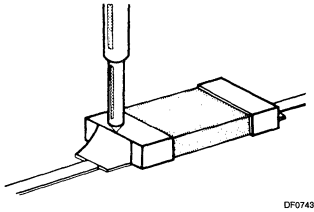
Test and Repair



a. Recommended Location of Test Points Close to SMDs



b. Acceptable, Though Not Recommended, Location of Test Points Close to SMDs



c. Unacceptable Location of Test Points Close to SMDs

Figure 2

Several systems are currently available to the manufacturer, including short-circuit testers, in-circuit testers, in-circuit analyzers, and functional testers. Figure 3 shows a bar-chart giving a comparison of percent fault detection and programming time for various ATE systems.

A loaded-board, short-circuit tester takes from two to six hours to program and its effective fault coverage is between 35% and 65%. It has the advantage of being operationally fast and comparatively inexpensive. On the negative side, however, it is limited to the detection of short-circuits and may require a double-sided, bed-of-nails test fixture (see Figure 4), which for SMD substrates may be expensive and take time to produce. Careful

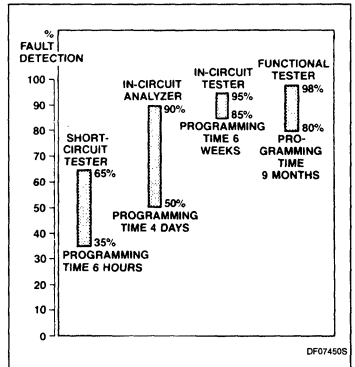


Figure 3. Bar Chart Showing a Comparison of Percent Fault Detection and Programming Time for Various ATE Systems

design can, however, often eliminate the need for double-sided test probe fixtures.

In-circuit testers power the assembly and check for open or short-circuits, circuit parameters, and can pinpoint defective components. They can provide around 90% fault coverage, but are more expensive than short-circuit testers and programming can take more than six weeks.

In-circuit analyzers are relatively simple to program and can detect manufacturing-induced faults in one third of the time required by an in-circuit tester. Fault coverage is between 50% and 90%. Because they do not power the assembly, they cannot detect digital logic faults, unlike an in-circuit tester or functional tester.

Functional testers, on the other hand, check the assembly's performance and simply make a go or no-go decision. Either the assembly performs its required function or it does not. They are much more expensive, but their fault coverage is between 80% and 98%. Their major disadvantages, apart from cost, are that they cannot locate defective components, and programming for a high-capacity system can take as long as nine months.

ATE Systems

An analysis of defects on a finished substrate will determine which combination of ATE will best meet the test requirements with regard to fault coverage and throughput rate.

If most defects are short-circuits, a loaded-board short-circuit tester, in tandem with an in-circuit tester, will pre-screen the substrate for short-circuits twice as fast as the in-circuit tester. This allows more time for the in-circuit tester to handle the more complex test requirements. This combination of ATE, instead of an in-circuit tester alone, improves the throughput rate.

Combining a short-circuit tester with a functional tester produces even more dramatic results. If most defects are manufacturing-produced shorts, the use of a short-circuit tester to relieve the functional tester of this task can increase throughput five-fold while maintaining a fault coverage of up to 98%.

If manufacturing faults and analog component defects are responsible for the majority of failures, a relatively low-cost, in-circuit analyzer can be used in tandem with an in-circuit tester or functional tester to reduce testing costs and improve throughput. The in-circuit analyzer is three times faster than an in-circuit tester in detecting manufacturing-induced faults, offers test and diagnostics usually within 10 seconds each, and is relatively simple to program. But because it is unpowered, an in-circuit analyzer cannot test digital logic faults; either an in-circuit tester or functional tester following the in-circuit analyzer must be used to locate this type of defect.

POLLUTED POWER SUPPLIES

Today's electronic components and the equipment used to test them are susceptible to electrical noise. Erroneous measurements on pass-or-fail tests could lower test throughput or, even more seriously, allow defective products to pass inspection. Semiconductor chips under test can also be damaged or destroyed as high-energy pulses or line-voltage surges stress the fine-line geometrics separating individual cells.

Noise pulses can be either in the normal (line-to-line) mode or common (line-to-ground) mode. Common-mode electrical noise poses a special threat to modern electronic circuitry since the safety ground line to which common-mode noise is referenced is often used as the system's logic reference point. Since parasitic capacitance exists between safety ground and the reference point, at high frequencies these points are essentially tied together, allowing noise to directly enter the system's logic.

MANUAL REPAIR

The repair of SMD-populated substrates will entail either the resoldering of individual joints and the removal of shorts or the replacement of defective components.

The reworking of defective joints will invariably involve the use of a manual soldering iron. Bits are commercially available in a variety of shapes, including special hollow bits used for desoldering and for the removal of solder bridges. The criteria for the inspec-

Test and Repair

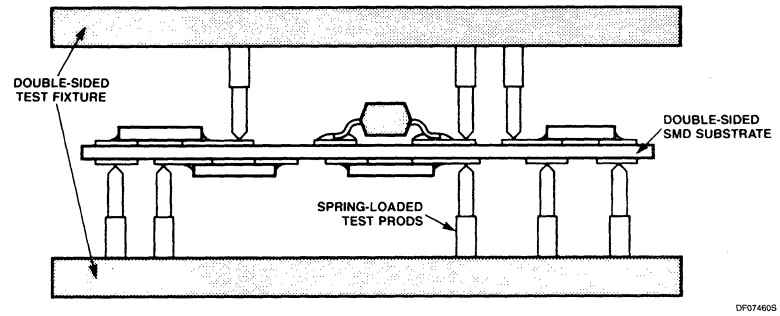


Figure 4. Double-Sided, Bed-of-Nails Test Fixture

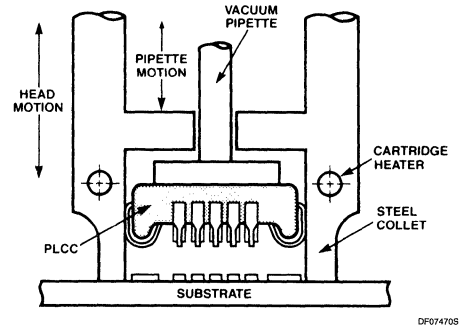


Figure 5. Heated Collet for the Removal and Replacement of Multi-Leaded SMDs (a PLCC is Shown Here)

tion of reworked soldered joints are the same as those for machine soldering.

Special care must be taken when reworking or replacing electrostatic sensitive devices. Soldering irons should be well grounded via a safety resistor of minimum 100kΩ. The ground connection to the soldering iron should be welded rather than clamped. This is because oxidation occurs beneath the clamp, thus isolating the ground connection. Voltage spikes caused by the switching of the iron can be avoided by using either continuously-powered irons, or irons that switch only at zero voltage on the AC sine curve.

To remove defective leadless SMDs, a variety of soldering iron bits are available that will apply the correct amount of heat to both ends of the component simultaneously and allow it to be removed from the substrate. If the substrate has been wave soldered, an adhesive will have been used, and the bond can be broken by twisting the bit. Any adhesive residue must then be removed. The same tool is then used to place and solder the new component, using either solder cream or resin-cored solder.

When a multi-leaded component, such as a plastic leaded chip carrier (PLCC), has to be removed, a heated collet can be used (see Figure 5). The collet is positioned over the PLCC, heat is applied to the leads and solder lands automatically until the solder reflows. The collet, complete with the PLCC, is then raised by vacuum. Solder cream is then re-applied to the solder lands by hand. No adhesive is required in this operation.

The collet is positioned over the replacement PLCC, which is held in place by the slight spring pressure of the PLCC leads against the walls of the collet. The collet, complete with PLCC, is then raised pneumatically and positioned over the solder lands. Using air pressure, the center pin of the collet then pushes the PLCC into contact with the substrate where it is maintained with the correct amount of force. Heat is then applied through the walls of the collet to reflow the solder paste. The center pin maintains pressure on the PLCC until the solder has solidified, then the center pin is raised and the replacement is complete.

Another method, well-suited to densely populated SMD substrates, uses a stream of heated air, directed onto the SMD terminations. Once the solder has been reflowed, the component can be removed with the aid of tweezers. While the hot air is being directed onto the component, cooler air is played onto the bottom of the substrate to protect it from heat damage. During removal, the component should be twisted sideways slightly in order to break the surface tension of the solder and any adhesive bond between the component and the substrate. This prevents damage to the substrate when the component is lifted.

To fit a new component, the solder lands are first retinned and fluxed, the new component accurately placed, and the solder reflowed with hot air. Substituting superheated argon, nitrogen, or a mixture of nitrogen and hydrogen for the hot air stream removes any risk of contaminating or oxidizing the solder.

Focused infrared light has also been used successfully to reflow the solder on densely populated substrates.

In general, the equipment and procedures used for the replacement of PLCCs can be used for leadless ceramic chip carriers (LCCCs) and small-outline packages (SO ICs). SO ICs are somewhat easier to replace, as the leads are more accessible and only on two sides of the component.

Fluxing and Cleaning

INTRODUCTION

The adoption of mass soldering techniques by the electronics industry was prompted not only by economics, and a requirement for high throughput levels, but also by the need for a consistent standard of quality and reliability in the finished product unattainable by using manual methods. With surface-mounted device (SMD) assembly, this need is even greater.

The quality of the end-product depends on the measures taken during the design and manufacturing stages. The foundations of a high-quality electronic circuit are laid with good design, and with correct choice of components and substrate configuration. It is, however, at the manufacturing stage where the greatest number of variables, both with respect to materials and techniques, have to be optimized to produce high-quality soldering, a prerequisite for reliability.

Of the two most commonly-used soldering techniques, wave and reflow, wave soldering is by far the most widely used and understood. Many factors influence the outcome of the soldering operation, some relating to the soldering process itself, and others to the condition of components and substrate to which they are to be attached. These must be collectively assessed to ensure high-quality soldering.

One of the most important, most neglected, and least understood of these processes is the choice and application of flux. This section outlines the fluxing options available, and discusses the various cleaning techniques that may be required, for SMD substrate assembly.

FLUXES

Populating a substrate involves the soldering of a variety of terminations simultaneously. In one operation, a mixture of tinned copper, tin/lead-or gold-plated nickel-iron, palladium-silver, tin/lead-plated nickel-barrier, and even materials like Kovar, each possessing varying degrees of solderability, must be attached to a common substrate using a single solder alloy.

It is for this reason that the choice of the flux is so important. The correct flux will remove surface oxides, prevent reoxidization, help to transfer heat from source to joint area, and leave non-corrosive, or easily removable corrosive residues on the substrate. It will also improve wettability of the solder joint surfaces.

The wettability of a metal surface is its ability to promote the formation of an alloy at its interface with the solder to ensure a strong, low-resistance joint.

However, the use of flux does not eliminate the need for adequate surface preparation. This is very important in the soldering of SMD substrates, where any temptation to use a highly-active flux in order to promote rapid wetting of ill-prepared surfaces should be avoided because it can cause serious problems later when the corrosive flux residues have to be removed. Consequently, optimum solderability is an essential factor for SMD substrate assembly.

Flux is applied before the wave soldering process, and during the reflow soldering process (where flux and solder are combined in a solder cream). By coating both bare metal and solder, flux retards atmospheric oxidization which would otherwise be intensified at soldering temperature. In the areas where the oxide film has been removed, a direct metal-to-metal contact is established with one low-energy interface. It is from this point of contact that the solder will flow.

Types of Flux

There are two main characteristics of flux. The first is efficacy—its ability to promote wetting of surfaces by solder within a specified time. Closely related to this is the activity of the flux, that is, its ability to chemically clean the surfaces.

The second is the corrosivity of the flux, or rather the corrosivity of its residues remaining on the substrate after soldering. This is again linked to the activity; the more active the flux, the more corrosive are its residues.

Although there are many different fluxes available, and many more being developed, they fall into two basic categories; those with residues soluble in organic liquids, and those with residues soluble in water.

Organic Soluble Fluxes

Most of the fluxes soluble in organic liquids are based on colophony or rosin (a natural product obtained from pine sap that has been distilled to remove the turpentine content). Solid colophony is difficult to apply to a substrate during machine soldering, so it is dissolved in a thinning agent, usually an alcohol. It has a very low efficacy, and hence limited cleaning power, so activators are added in varying quantities to increase it. These take the form of either organic acids, or organic salts that are chemically active at soldering temperatures. It is therefore convenient to classify the colophony-based fluxes by their activator content.

Non-Activated Rosin (R) Flux

These fluxes are formed from pure colophony in a suitable solvent, usually isopropanol or ethyl alcohol. Efficacy is low and cleaning action is weak. Their uses in electronic soldering are limited to easily-wettable materials with a high level of solderability. They are used mainly on circuits where no risk of corrosion can be tolerated, even after prolonged use (implanted cardiac pacemakers, for example). Their flux residues are noncorrosive and can remain on the substrate, where they will provide good insulation.

Rosin, Mildly-Activated (RMA) Flux

These fluxes are also composed of colophony in a solvent, but with the addition of activators, either in the form of di-basic organic acids (such as succinc acid), or organic salts (such as dimethylammonium chloride or diethylammonium chloride). It is customary to express

the amount of added activator as mass percent of the chlorine ion on the colophony content, as the activator-to-colophony ratio determines the activity, and, hence, the corrosivity. In the case of RMA activated with organic salts, this is only some tenths of one percent.

When organic acids are used, a higher percentage of activator must be added to produce the same efficacy as organic salts, so frequently both salts and acids are added. The cleaning action of RMA fluxes is stronger than that of the R type, although the corrosivity of the residues is usually acceptable. These residues may be left on the substrate as they form a useful insulating layer on the metal surfaces. This layer can, however, impede the penetration of test probes at a later stage.

Rosin, Activated (RA) Flux

The RA fluxes are similar to the RMA fluxes, but contain a higher proportion of activators. They are used mainly when component or substrate solderability is poor and corrosion-risk requirements are less stringent. However, as good solderability is considered essential for SMD assembly, highly-activated rosin fluxes should not be necessary. The removal of

Fluxing and Cleaning

flux residues is optional and usually dependent upon the working environment of the finished product and the customer's requirements.

Water-Soluble Fluxes

The water-soluble fluxes are generally used to provide high fluxing activity. Their residues are more corrosive and more conductive than the rosin-based fluxes, and, consequently, must always be removed from the finished substrate. Although termed water soluble, this does not necessarily imply that they contain water; they may also contain alcohols or glycols. It is the flux residues that are water soluble. The usual composition of a water-soluble flux is shown below.

1. A chemically-active component for cleaning the surfaces.
2. A wetting agent to promote the spreading of flux constituents.
3. A solvent to provide even distribution.
4. Substances such as glycols or water-soluble polymers to keep the activator in close contact with the metal surfaces.

Although these substances can be dissolved in water, other solvents are generally used, as water has a tendency to spatter during soldering. Solvents with higher boiling points, such as ethylene glycol or polyethylene glycol are preferred.

Water-Soluble Fluxes With Inorganic Salts

These are based on inorganic salts such as zinc chloride, or ammonium chloride, or inorganic acids such as hydrochloric. Those with zinc or ammonium chloride must be followed by very stringent cleaning procedures as any halide salts remaining on the substrate will cause severe corrosion. These fluxes are generally used for non-electrical soldering. Although the hydrazine halides are among the best active fluxing agents known, they are highly suspect from a health point of view and are therefore no longer used by flux manufacturers.

Water-Soluble Fluxes With Organic Salts

These fluxes are based on organic hydrohalides such as dimethylammonium chloride, cyclo hexalamine hydrochloride, and aniline hydrochloride, and also on the hydrohalides of organic acids. Fluxes with organic halides usually contain vehicles such as glycerol or polyethylene glycol, and non-ionic surface-active agents such as nonylphenol polyoxyethylene. Some of the vehicles, such as the polyethylene glycols, can degrade the insulation resistance of epoxy substrate material and, by rendering the substrate hydrophilic, make it susceptible to electrical leakage in high-humidity environments.

Water-Soluble Fluxes With Organic Acids

Based on acids such as lactic, melonic, or citric, these fluxes are used when the presence of any halide is prohibited. However, their fluxing action is weak, and high acid concentrations have to be used. On the other hand, they have the advantage that the flux residues can be left on the substrate for some time before washing without the risk of severe corrosion.

Solder Creams

For reflow soldering, both the solder and the flux are applied to the substrate before soldering and can be in the form of solder creams (or pastes), preforms, electro-deposit, or a layer of solder applied to the conductors by dipping. For SMD reflow soldering, solder cream is generally used.

Solder cream is a suspension of solder particles in flux to which special compounds have been added to improve the rheological properties. The shape of the particles is important and normally spherical particles are used, although non-spherical particles are now being added, particularly in very fine-line soldering.

In principle, the same fluxes are used in solder creams as for wave soldering. However, due to the relatively large surface area of the solder particles (which can oxidize), more effective fluxing is required and, in general, solder creams contain a higher percentage of activators than the liquid fluxes. The drying of the solder paste during preheating (after component placement) is an important stage as it reduces any tendency for components to become displaced during soldering.

Flux Selection

Choosing an appropriate flux is of prime importance to the soldering system for the production of high-quality, reliable joints. When solderability is good, a mildly-activated flux will be adequate, but when solderability is poorer, a more effective, more active flux will be required. The choice of flux, moreover, will be influenced by the cleaning facilities available, and if, in fact, cleaning is even feasible.

With water-soluble fluxes, aqueous cleaning of the substrate after soldering is mandatory. If thorough cleaning is not carried out, severe problems may arise in the field, due to corrosion or short circuits caused by too low a surface resistance of the conductive residues.

For rosin-based fluxes, the need for cleaning will depend on the activity of the flux. Mildly-activated rosin residues can, in most cases, remain on the substrate where they will afford protection and insulation. In practice, for the great majority of electronic circuits, the choice will be between an RA or an RMA rosin-based flux.

Application of Flux

Three basic factors determine the method of applying flux: the soldering process (wave or reflow), the type of substrate being processed (all-SMD or mixed print), and the type of flux.

For wave soldering, the flux must be applied in liquid form before soldering. While it is possible to apply the flux at a separate fluxing station, with the high throughput rates demanded to maximize the benefits of SMD technology, today's wave-soldering machines incorporate an integral fluxing station prior to the preheat stage. This enables the preheat stage to be used to dry the flux as well as preheat the substrate to minimize thermal shock.

The most commonly-used methods of applying flux for wave soldering are by foam, wave, or spray.

Foam Fluxing

Foam flux is generated by forcing low-pressure clean air through an aerator immersed in liquid flux (see Figure 1). The fine bubbles produced by the aerator are guided to the surface by a chimney-shaped nozzle. The substrates are passed across the top of the nozzle so that the solder side comes in contact with the foam and an even layer of flux is applied. As the bubbles burst, flux penetrates any plated-through holes in the substrate.

Wave Fluxing

A double-sided wave can also be used to apply flux, where the washing action of the wave deposits a layer of flux on the solder side of the substrate (see Figure 2). Wave-height control is essential and a soft, wipe-off brush should be incorporated on the exit side of the fluxing station to remove excess flux from the substrate.

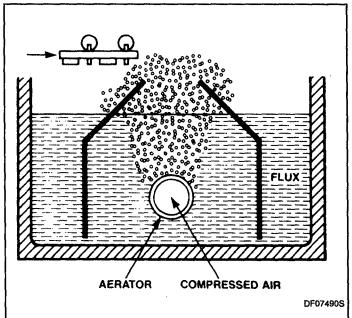


Figure 1. Schematic Diagram of Foam Fluxer

Fluxing and Cleaning

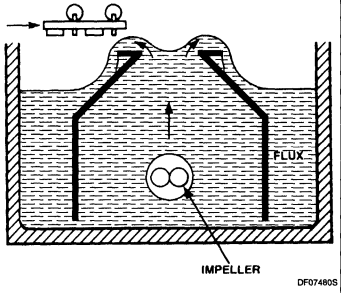


Figure 2. Schematic Diagram of Wave Fluxer

Spray Fluxing

Several methods of spray fluxing exist; the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate (see Figure 3). Four parameters affect the amount of flux deposited: conveyor speed, drum rotation, air pressure, and flux density. The thickness of the flux layer can be controlled using these parameters, and can vary between 1 and 10μm.

The advantages and disadvantages of these three flux application techniques are outlined in Table 1.

Flux Density

One of the main control factors for fluxes used in machine soldering is the flux density. This provides an indication of the solids content of the flux, and is dependent on the nature of the solvents used. Automatic control systems, which monitor flux density and inject more solvent as required, are commercially available, and it is relatively simple to incorporate them into the fluxing system.

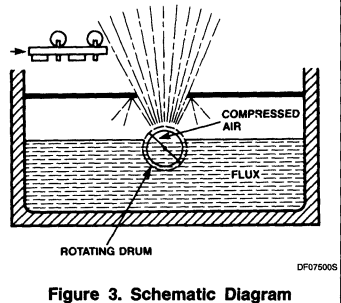


Figure 3. Schematic Diagram of Spray Fluxer

PREHEATING

Preheating the substrate before soldering serves several purposes. It dries the flux to evaporate most of the solvent, thus increasing the viscosity. If the viscosity is too low, the flux may be prematurely expelled from the substrate by the molten solder. This can result in poor wetting of the surfaces, and solder spatter.

Drying the flux also accelerates the chemical action of the flux on the surfaces, and so speeds up the soldering process. During the preheating stage, substrate and components are heated to between 80°C and 90°C (solvent-based fluxes) or to between 100°C and 110°C (water-based systems). This reduces the thermal shock when the substrate makes contact with the molten solder, and minimizes any likelihood of the substrate warping.

The most common methods of preheating are: convection heating with forced air, radiation heating using coils, infrared quartz lamps or heated panels, or a combination of both convection and radiation. The use of forced air has the added advantage of being more effective for the removal of evaporated solvent. Optimum preheat temperature and duration will depend on the nature and design of the substrate and the composition of the flux.

Figure 4 shows a typical method of preheat temperature control. The desired temperature is set on the control panel, and the microprocessor regulates preheater No. 1 to provide approximately 60% of the required heat. The IR detector scans the substrate immediately following No. 1 heater and reads the surface temperature. By taking into account the surface temperature, conveyor speed, and the thermal characteristics of the substrate, the microprocessor then calculates the amount of additional heat required to be provided by heater No. 2 in order to attain the preset temperature. In this way, each substrate will have the same surface temperature on reaching the solder bath.

POSTSOLDERING CLEANING

Now that worldwide efforts in both commercial and industrial electronics are converting old designs from conventional assembly to surface mounting, or a combination of both, it can also be expected that high-volume cleaning systems will convert from in-line aqueous cleaners to in-line solvent cleaners or in-line saponification systems (a technique that uses an alkaline material in water to react with the rosin so that it becomes water soluble). These systems may, however, become subject to environmental objections, and new governmental restrictions on the use of halogenated hydrocarbons.

The major reason for this is that the water-soluble flux residues, containing a higher concentration of activators, or showing hygroscopic behavior, are much more difficult to remove from SMD-populated substrates than rosin-based flux residues. This is primarily because the higher surface tension of water, compared to solvents, makes it difficult for the cleaning agents to penetrate beneath SMDs, especially the larger ones, with their greatly reduced off-contact distance (the distance between component and substrate).

Postsoldering cleaning removes any contamination, such as surface deposits, inclusions, occlusions, or absorbed matter which may degrade to an unacceptable level the chemical, physical, or electrical properties of the assembly. The types of contaminant on substrates that can produce either electrical or mechanical failure over short or prolonged periods are shown in Table 2.

All these contaminants, regardless of their origin, fall into one of two groups: polar and non-polar.

Polar Contaminants

Polar contaminants are compounds that dissociate into free ions which are very good conductors in water, quite capable of causing circuit failures. They are also very reactive with metals and produce corrosive reactions. It is essential that polar contaminants be removed from the substrates.

Non-Polar Contaminants

Non-polar contaminants are compounds that do not dissociate into free ions or carry an electrical current and are generally good insulators. Rosin is a typical example of a non-polar contaminant. In most cases, non-polar contamination does not contribute to corrosion or electrical failure and may be left on the substrate. It may, however, impede functional testing by probes and prevent good conformal coat adhesion.

Solvents

The solvents currently used for the post-soldering cleaning of substrates are normally organic based and are covered by three classifications: hydrophobic, hydrophillic, and azeotropes of hydrophobic/hydrophillic blends.

Azeotropic solvents are mixtures of two or more different solvents which behave like a single liquid insomuch that the vapor produced by evaporation has the same composition as the liquid, which has a constant boiling point between the boiling points of the two solvents that form the azeotrope. The basic ingredients of the azeotropic solvents are combined with alcohols and stabilizers. These stabilizers, such as nitromethane, are included to prevent corrosive reaction be-

Fluxing and Cleaning

Table 1. Advantages and Disadvantages of Flux Application Methods

Method	Advantages	Disadvantages
Foam Fluxing	• Compatible with continuous soldering process • Foam crest height not critical • Suitable for mixed-print substrates	• Not all fluxes have good foaming capabilities • Losses throught evaporation may be appreciable • Prolonged preheating because of high boiling point of solvents
Wave Fluxing	• Can be used with any liquid flux • Compatible with continuous soldering process • Suitable for densely-populated mixed print	• Wave crest height is critical to ensure good contact with bottom of substrate without contaminating the top
Spray fluxing	• Can be used with most liquid fluxes • Short preheat time if appropriate alcohol solvents are used • Layer thickness is controllable	• High flux losses due to non-recoverable spray • System requires frequent cleaning

tween the metallization of the substrate and the basic solvents.

Hydrophobic solvents do not mix with water at concentrations exceeding 0.2%, and consequently have little effect on ionic contamination. They can be used to remove non-polar contaminants such as rosin, oils, and greases.

Hydrophillic solvents do mix with water and can dissolve both polar and non-polar contamination, but at different rates. To overcome these differences, azeotropes of the various solvents are formulated to maximize the dissolving action for all types of contamination.

Solvent Cleaning

Two types of solvent cleaning systems are in use today: batch and conveyorized systems, either of which can be used for high-volume production. In both systems, the contaminated substrates are immersed in the boiling solvents, and ultrasonic baths or brushes may also be used to further improve the cleaning capabilities.

The washing of rosin-based fluxes offers advantages and disadvantages. Washed substrates can usually be inserted into racks easier, as there will be no residues on their edges; test probes can make better contact without a rosin layer on the test points, and the removal of the residues makes it easier to visually examine the soldered joints. On the other hand, washing equipment is expensive, and so are the solvents, and some solvents present a health or environmental hazard if not correctly dealt with.

Aqueous Cleaning

For high-volume production, special machines have been developed in which the substrates are conveyor-fed through the various stages of spraying, washing, rinsing, and drying. The final rinse water is blown from the substrates to prevent any deposits from the water being left on the substrate.

Where water-soluble fluxes have been used in the soldering process, substrate cleaning is mandatory. For the rosin-based fluxes, it is optional, and is often at the discretion of the customer.

Conformal Coatings

A conformal, or protective coating on the substrate, applied at the end of processing, prevents or minimizes the effects of humidity and protects the substrate from contamination by airborne dust particles. Substrates that are to be provided with a conformal coating (dependent on the environmental conditions to which the substrate will be subjected) must first be washed.

Environmental and Ecological Aspects of Fluxes and Solvents

Fumes and vapors produced during soldering processes, or during cleaning, will not, under normal circumstances, present a health hazard, if relevant health and safety regulations are observed.

Fumes originating from colophony can cause respiratory problems, so an efficient fume-extraction system is essential. The extraction system must cover the fluxing, preheating, and soldering stations, remain operational for at least one hour after machine shutdown, and conform to local regulations. Today, the problem of noxious fumes is unlikely to concern the cleaning station, as all commercial systems are equipped to condense the vapors back into the system. In the future, however, it can be expected that a much lower degree of escape of noxious fumes from any system will be allowed, and all systems may have to be reviewed.

Certain fluxes, particularly some water-soluble ones, contain highly aggressive substances, and must not be allowed to come into contact with the skin or eyes. Any contamination should immediately be removed with plenty of clean, fresh water. Deionized water should also be readily available as an eye-wash. Should contamination occur, a qualified medical practitioner should be consulted. Protective clothing should be worn during cleaning or maintenance of the fluxing station.

Conclusion

SMD technology imposes tougher restraints on fluxing and cleaning of substrate assemblies. Traditionally, rosin-based fluxes have been used in electronic soldering where residues were considered "safe" and could be left on the board. However, increased SMD packing density, fine-line tracks, and more rigid specifications have resulted in changes to this basic philosophy.

There is now a demand for surfaces free from residues; test probes are more efficient when they do not have to penetrate rosin flux residues, and conformal coating and board inspection benefit from the absence of such residues.

Cleaning also poses problems for SMD substrates. The close proximity of component and substrate means that solvents cannot effectively clean beneath devices. Components must also be compatible with the cleaning process. They must, for example, be resistant to the solvents used and to the temperatures of the cleaning process. They must also be sealed to prevent cleaning fluids from entering the devices and degrading performance.

So, eliminating the need for cleaning is better than poor or incomplete cleaning. And in a well-balanced system, mildly-activated rosin-based fluxes, leaving only non-corrosive residues, can be successfully used for SMD substrate soldering without subsequent cleaning.

Much research into fluxes and solder creams is presently being done — for example, the production of synthetic resin, with qualities superior to colophony at a lower cost. Another area of research is that of solder creams with non-melting additives, such as lead or ceramic spheres, that increase the distance

Fluxing and Cleaning

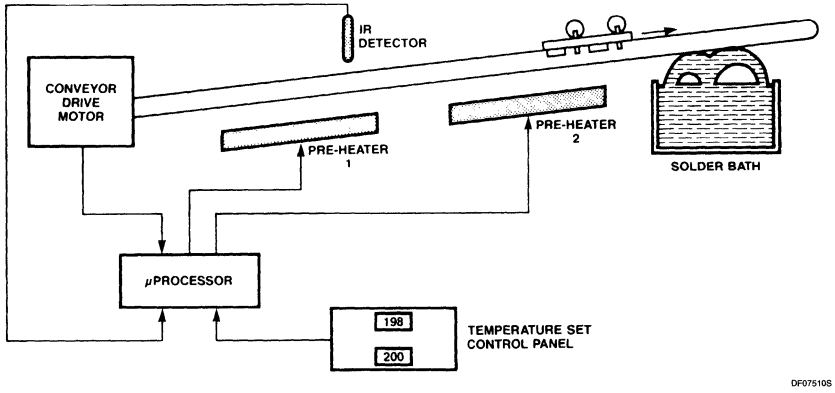


Figure 4. Schematic Diagram of a Typical Controlled Preheat System

Table 2. Substrate Contaminants

Contaminant	Origin
Organic compounds	Fluxes, solder mask
Inorganic insoluble compounds	Photo-resists, substrate processing
Organo-metallic compounds	Fluxes, substrate processing
Inorganic soluble compounds	Fluxes
Particle matter	Dust, fingerprints

between component and substrate, thus making it easier for cleaning fluids to penetrate beneath the component. It also increases the joint's ability to withstand thermal cycling.

Rosin-free and halide-free fluxes are also being developed with similar activities to conventional rosin-based fluxes. These new types will combine the "safety" of rosin fluxes with easier removal in conventional solvents. Using non-polar materials, ionizable or corrosive residues are eliminated, and the need for cleaning immediately after soldering is avoided.

Thermal Considerations for Surface-Mounted Devices

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long-term operating life of an IC. As will be shown in this section, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. **Some of the VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface-Mount Device (SMD) technology, management of thermal characteristics remains a valid concern, not only because the SMD packages are much smaller, but also because the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface-mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

POWER DISSIPATION

Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

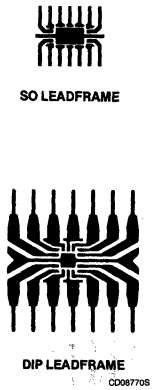
THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

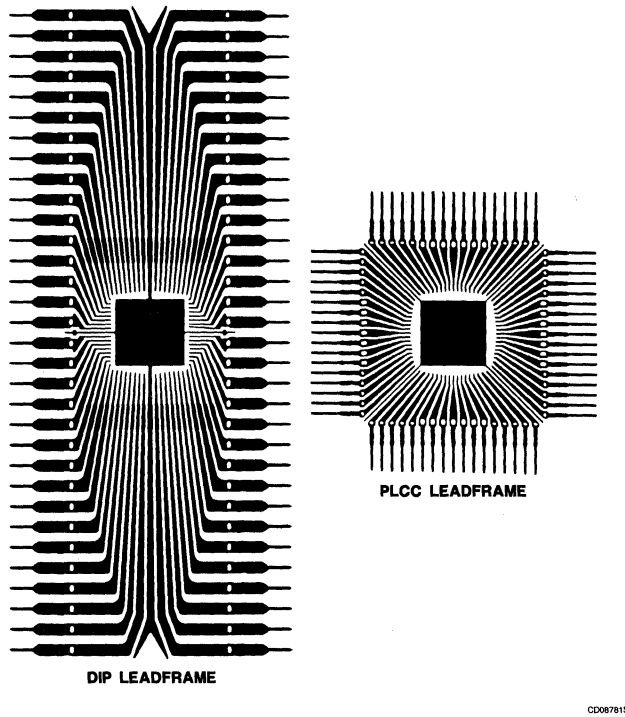
$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the



a. SO-14 Leadframe Compared to a 14-Pin DIP Leadframe



b. PLCC-68 Leadframe Compared to a 64-Pin DIP Leadframe

Figure 1

Thermal Considerations for Surface-Mounted Devices

substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and, to a lesser extent, other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally-conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years, the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However, three to five years ago the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package. Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die-size, die-attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small it makes the difference insignificant.

Gold-wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller than in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards. It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts, or compositions may give different results from this data. Each SMD user should compare his system to the Signetics test system and determine if the data is appropriate or needs adjustment for his application.

Test Method

Signetics uses what is commonly called the TSP (temperature-sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant-temperature oil bath and constant-current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating; data given here used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}} \Bigg|\ I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

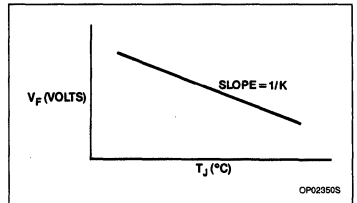


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

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Thermal Considerations for Surface-Mounted Devices

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K(V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)

V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)

V_H = Heating Voltage (V)

I_H = Heating Current (A)

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size — SO Small
1.12″ × 0.75″ × 0.059″
— SO Large:
1.58″ × 0.75″ × 0.059″
— PLCC:
2.24″ × 2.24″ × 0.062″

Board Material — Glass epoxy, FR-4 type with 1oz. sq.ft. copper solder coated

Board Trace Configuration — See Figure 3.

SO devices are set at 8 – 9mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 – 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board, and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still-air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air-flow tests were run in a 4″ × 4″ cross-section by 26″ long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16″ stand-off. Figure 6 shows the air-flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water-cooled block approximately 4″ × 7″ × 0.75″) to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040″ diameter sheath, grounded junction type K) mounted flush with heat-sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook-up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

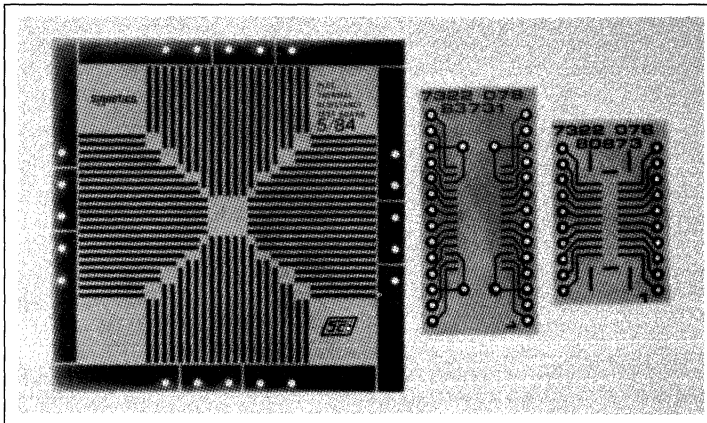


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

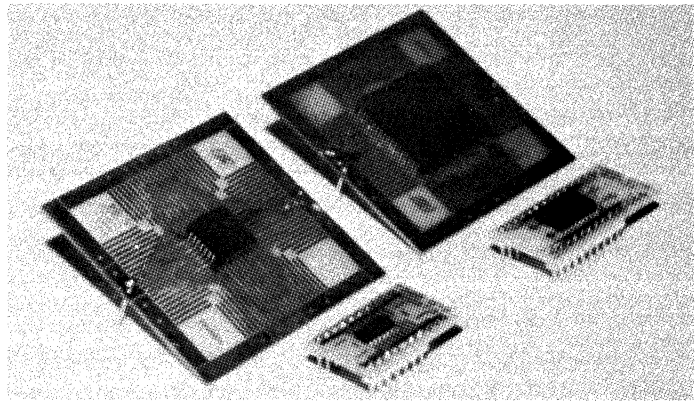


Figure 4. Device/Board Assemblies

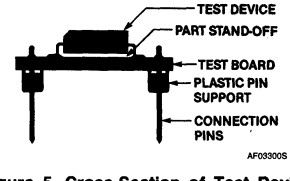
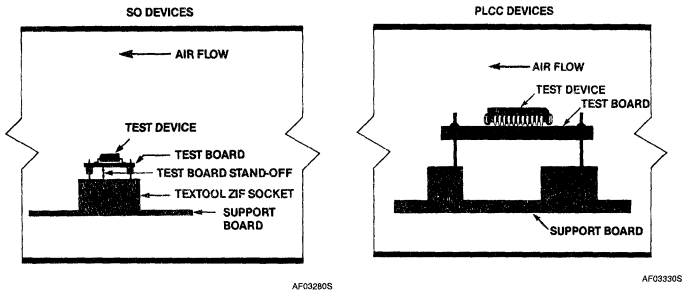


Figure 5. Cross-Section of Test Device Soldered to Test Board

Thermal Considerations for Surface-Mounted Devices



SO Devices PLCC Devices

Figure 6. Air-Flow Test Setup

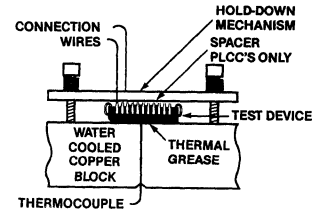


Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)

θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)

P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)

T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air-flow ambients. Given $T_A = 30°C$,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data — SOL-20 graph.

   Answer: 88°C/W @ 0.7W

2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.

   Percent change in Power

   $$= \frac{0.5W - 0.7W}{0.7W} \times 100$$

   $$= -28.6\%$$

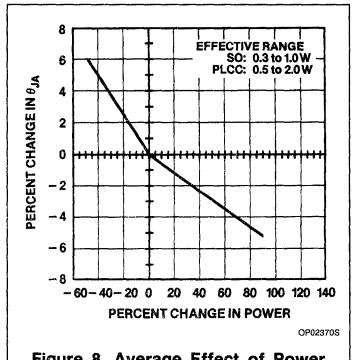


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

From Figure 8:
28.6% change in power gives
3.5% increase in θ_{JA}

Answer:
88°C/W + (88 × 0.035)
= 91°C/W @ 0.5W

3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.

From Figure 9: 200 LFPM air flow gives 14% decrease in θ_{JA}

Answer:
91°C/W – (91 × 0.14) = 78°C/W

4. Calculate approximate junction temperature

Answer:
T_J (still-air)
= (91°C/W × 0.5W) + 30
= 76°C
T_J (200 LFPM)
= (78°C/W × 0.5W) + 30
= 69°C

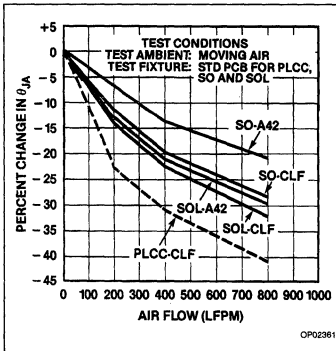
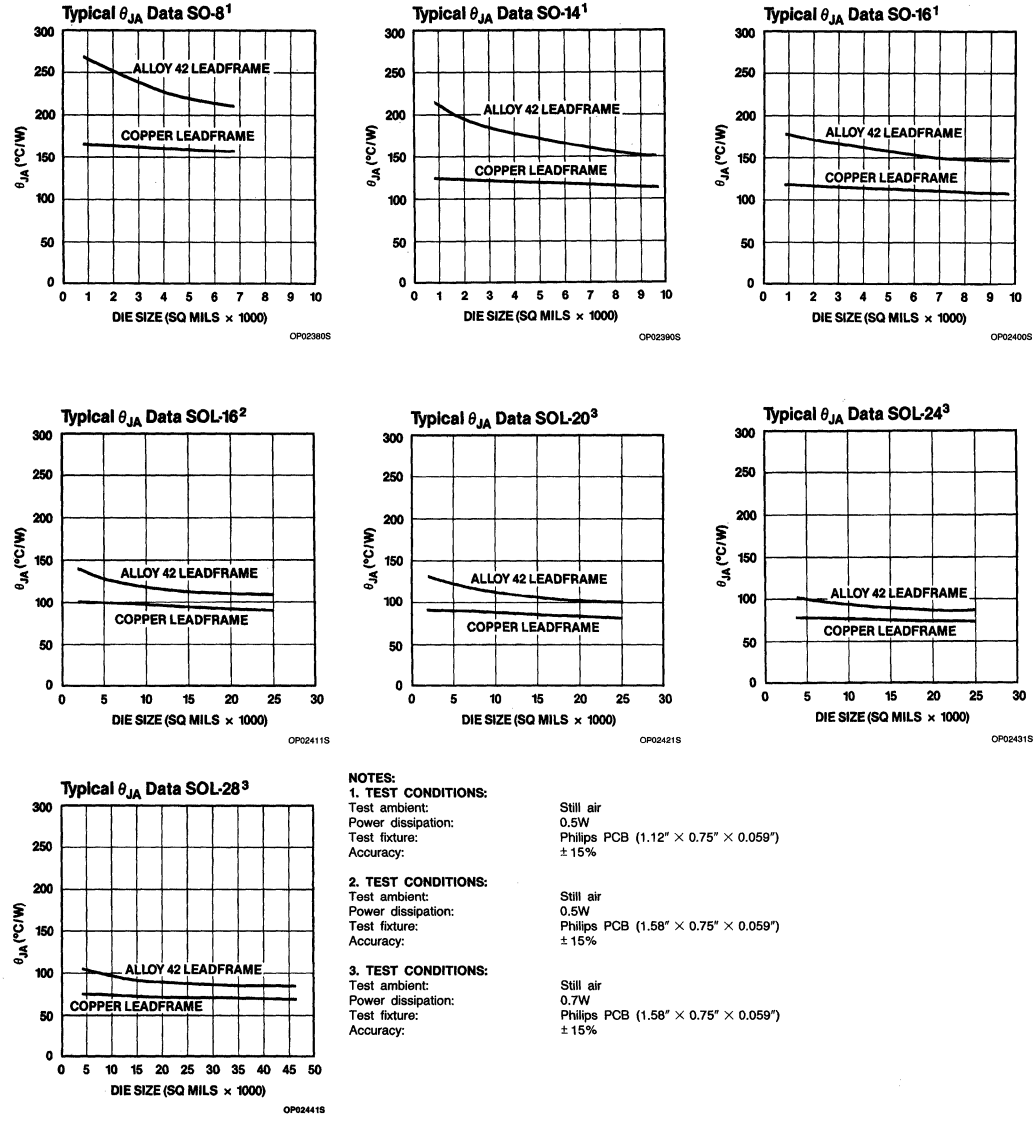


Figure 9. Average Effect of Air Flow on SMD θ_{JA}

Thermal Considerations for Surface-Mounted Devices



NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12″ × 0.75″ × 0.059″)
Accuracy:	±15%

2. TEST CONDITIONS:

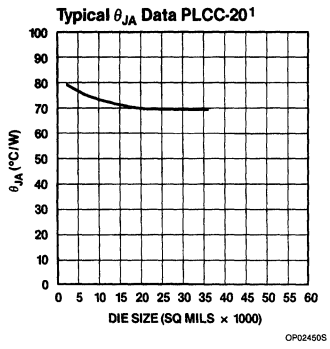
Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy:	±15%

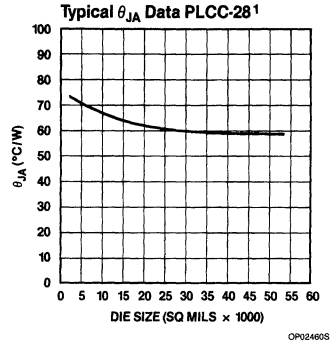
3. TEST CONDITIONS:

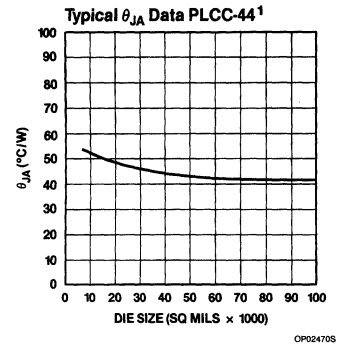
Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58″ × 0.75″ × 0.059″)
Accuracy:	±15%

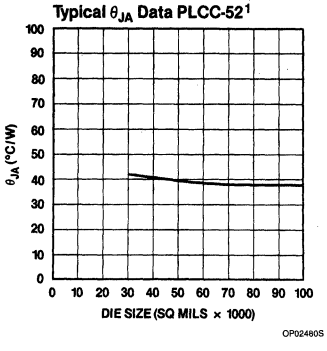
Figure 10. Typical SMD Thermal (θ_{JA}) Characteristics

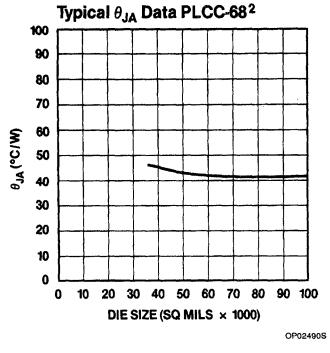
Thermal Considerations for Surface-Mounted Devices

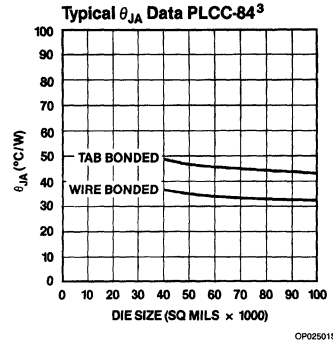












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

2. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

3. TEST CONDITIONS:

Test ambient	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24″ × 2.24″ × 0.062″)
Accuracy:	±15%

Figure 11. Typical SMD Thermal (θ_{JA}) Characteristics

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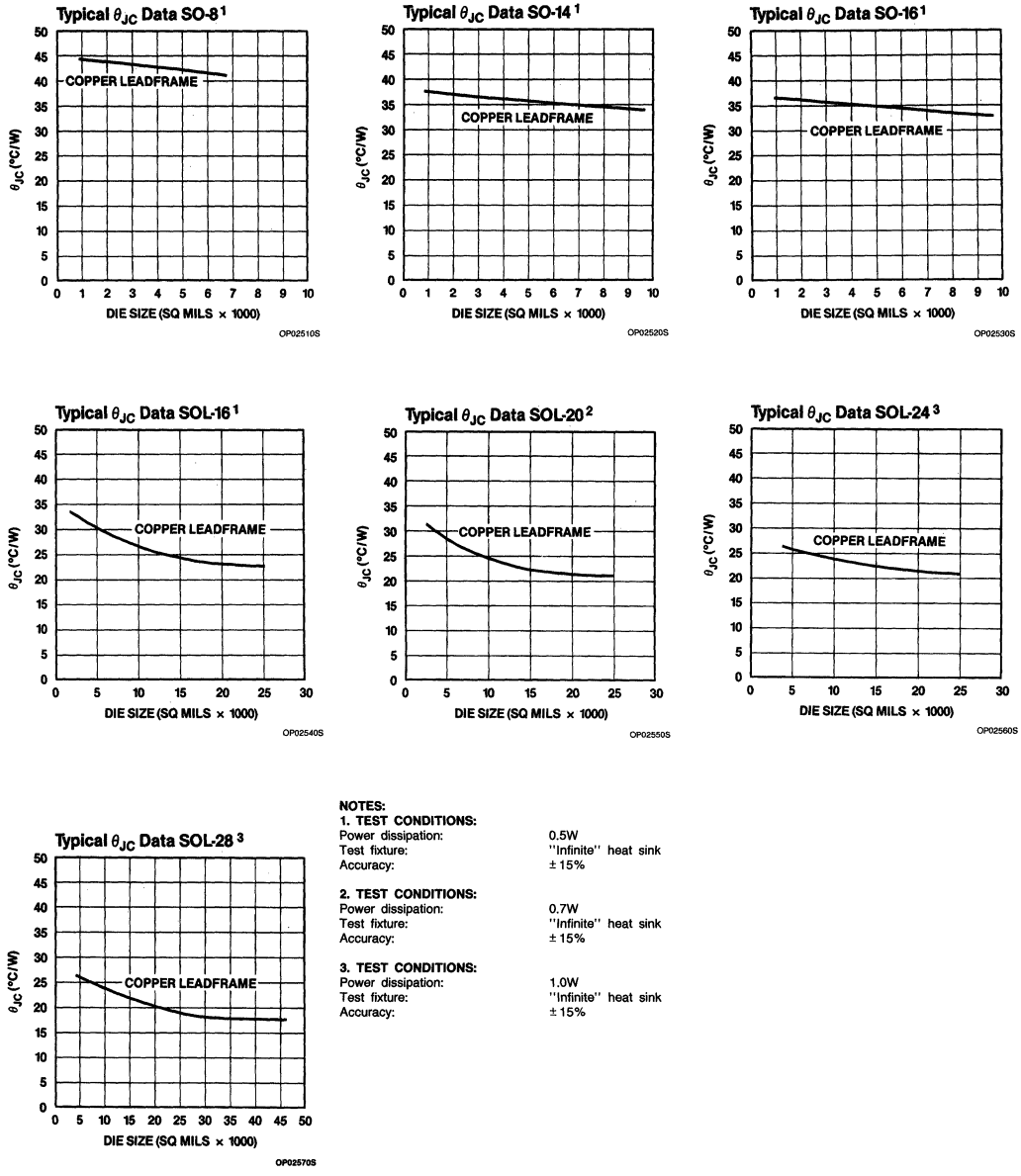
Thermal Considerations for Surface-Mounted Devices



NOTES:

1. TEST CONDITIONS:

Power dissipation:	0.5W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

2. TEST CONDITIONS:

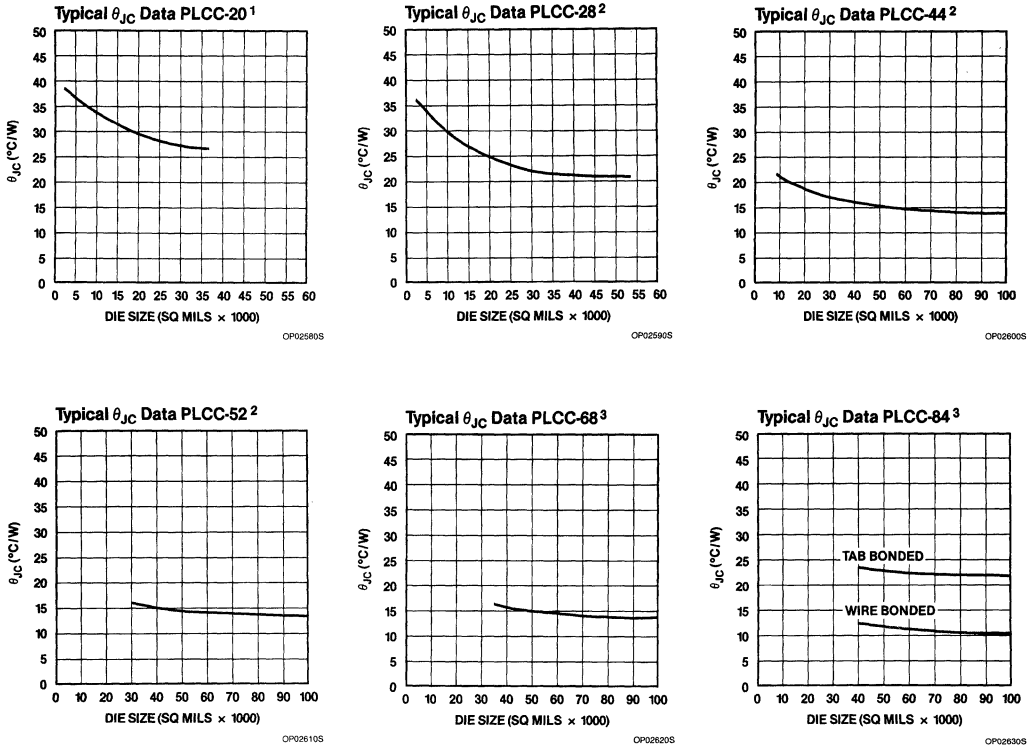
Power dissipation:	0.7W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

3. TEST CONDITIONS:

Power dissipation:	1.0W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

Figure 12. Typical SMD Thermal (θ_{JC}) Characteristics

Thermal Considerations for Surface-Mounted Devices



NOTES:

1. TEST CONDITIONS:

Power dissipation:	0.75W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

2. TEST CONDITIONS:

Power dissipation:	1.0W
Test fixture:	"infinite" heat sink
Accuracy:	±15%

3. TEST CONDITIONS:

Power dissipation:	2.0W
Test fixture:	"Infinite" heat sink
Accuracy:	±15%

Figure 13. Typical SMD Thermal (θ_{JC}) Characteristics

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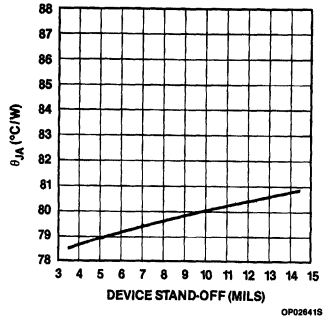
Thermal Considerations for Surface-Mounted Devices

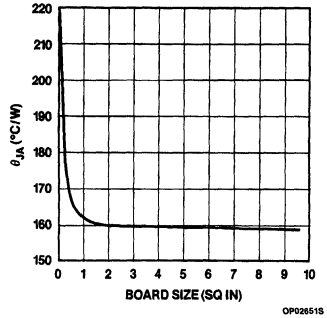
Effect of Device Stand-Off on SO θ_{JA} [1]



NOTES:
1. TEST CONDITIONS

Package type:	SOL-20 CLF
Die size:	11,322sq.mils
Test Ambient:	Still-air
Power dissipation:	0.75W
Test fixture:	Phillips PCB (1.58" × 0.75" × 0.059")

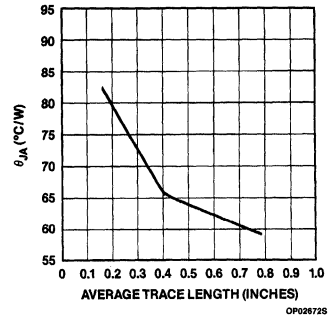
Effect of Board Size on SO θ_{JA} [2]



NOTES:
2. TEST CONDITIONS

Package type:	SOL-14 CLF
Die size:	5,040sq.mils
Test Ambient:	Still-air
Power dissipation:	0.6W
Test fixture:	0.062" thick PCB with "no traces" 8 – 9mil stand-off

Effect of Trace Length on 28-Lead PLCC θ_{JA} [3]



NOTES:
3. TEST CONDITIONS

Package type:	PLCC-28 CLF
Die size:	10,445sq.mils
Test Ambient:	Still-air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062") trace 27mil-wide 1oz sq.ft copper

Figure 14

Thermal Considerations for Surface-Mounted Devices

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations, and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection-molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a surface-mounted assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduce the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

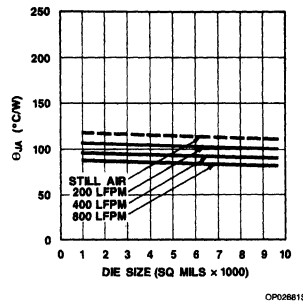


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

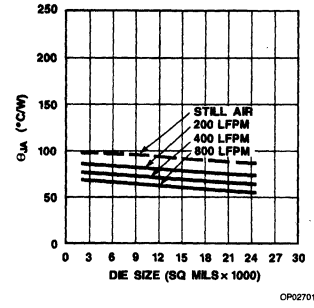


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

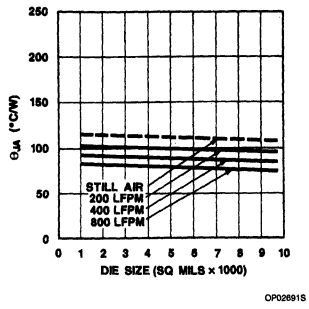


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

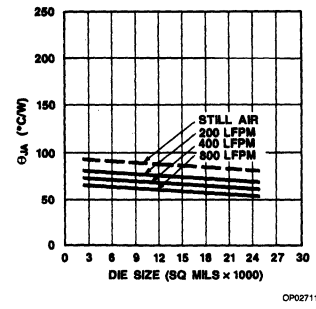


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be set up in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/°C soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/°C. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

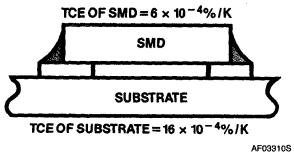
The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, is normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses set up in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its

Thermal Considerations for Surface-Mounted Devices

most critical in applications requiring large LCCCs with high pin counts.



NOTE:
Data provided by N.V. Philips

Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL, and PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e., SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO, can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metallic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate, can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar® or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed, in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability, and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates, however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates, traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely-used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 $\times 10^{-6}$/°C. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill, and is prone to resin microcracking and water absorption.

Polyimide quartz substrates have a TCE between 6 and 12, making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

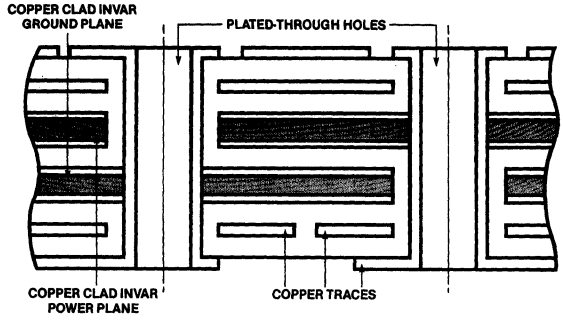
Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate,

Thermal Considerations for Surface-Mounted Devices

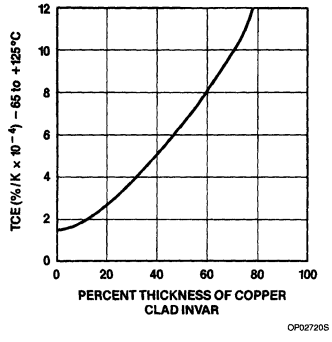
making it possible to mount LCCCs with confidence.

Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness and shows the TCE range of each of several other materials to which the clad material can be matched. For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.



NOTE:
Data provided by N.V. Philips

Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-Clad Invar Ground and Power Planes, Interconnected via Plated-Through Holes



NOTE:
Data provided by N.V. Philips

Figure 21. The TCE Range of Copper-Clad Invar as a Function of Copper Thickness

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Thermal Considerations for Surface-Mounted Devices

Table 1. Substrate Material Properties

SUBSTRATE MATERIAL	TCE (10^{-6}/°C)	THERMAL CONDUCTIVITY (W/m^{3}K)
Glass-epoxy (FR-4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper-clad Invar	6.4 (typical)	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material.
Data provided by N.V. Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart . . . even with copper leadframes. That is the major trade-off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

Package Outlines
For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

INTRODUCTION
The following information applies to all packages unless otherwise specified on individual package outline drawings.

GENERAL
1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across / the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120mils square die for plastic packages and a 90mils square die in the smallest available cavity for hermetic packages. All units were solder-mounted to PC boards, with standard stand-off, for measurement.

PLASTIC ONLY
5. Lead material: Alloy 42 (Nickel/Iron Alloy), Olin 194 (Copper Alloy), or equivalents, solder-dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO packages/microminiature packages:
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY
10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated, tin-plated, or solder-dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent — tin-plated, gold-plated or solder-dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent — gold-plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent — gold- or tin-plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel- or tin-plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold-plated, alloy seal.
    d. BeO ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb 0.010 inches.
16. Maximum glass climb or lid skew is 0.010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PLASTIC PACKAGES

DESCRIPTION	PACKAGE CODE	θ_{JA}/θ_{JC} (°C/W)	PACKAGE TYPE
Standard Dual-in-Line Packages			
8-Pin	N	99/50	
14-Pin	N	86/48	TO-116/MO-001
16-Pin	N	83/42	MO-001
18-Pin	N	63/29	
20-Pin	N	61/24	
22-Pin	N	51/23	
24-Pin	N	52/23	MO-015
28-Pin	N	52/23	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO-5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side-Brazed Lead			
16-Pin	I	90/25	DIP Laminate

SO Package Thermal Data

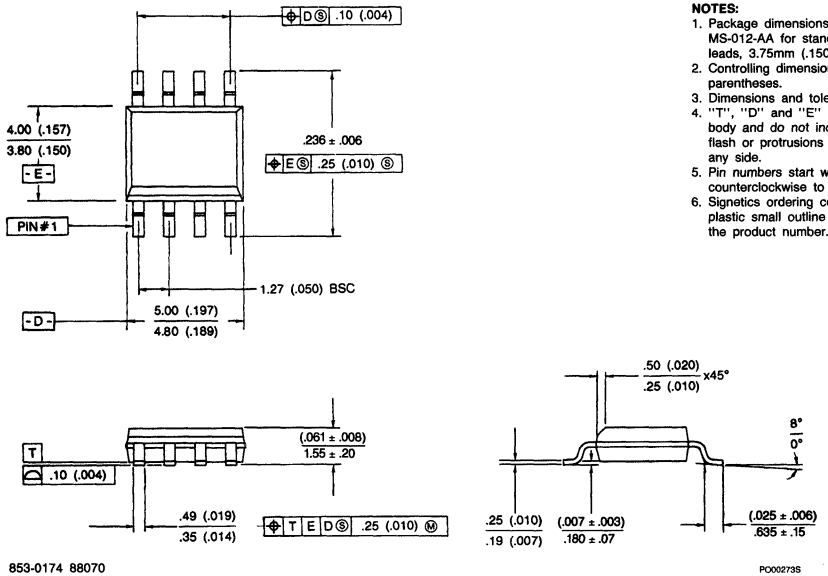
PACKAGE TYPE	PACKAGE MOUNTING TECHNIQUE*	MAX. ALLOWABLE POWER DISS. (mW) AT 25°C	MAX. ALLOWABLE POWER DISS. (mW) AT 70°C	THERMAL RESISTANCE (θ_{JA}°C/WATT)	
				Average	Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

PCB = Printed circuit board
Ceramic = Ceramic substrate
Ceramic w/H.S. = Ceramic substrate with heat sink and/or Thermal compound
*Air gap is 0.006 inches unless thermal compound is used

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

8-PIN PLASTIC SO (D PACKAGE)

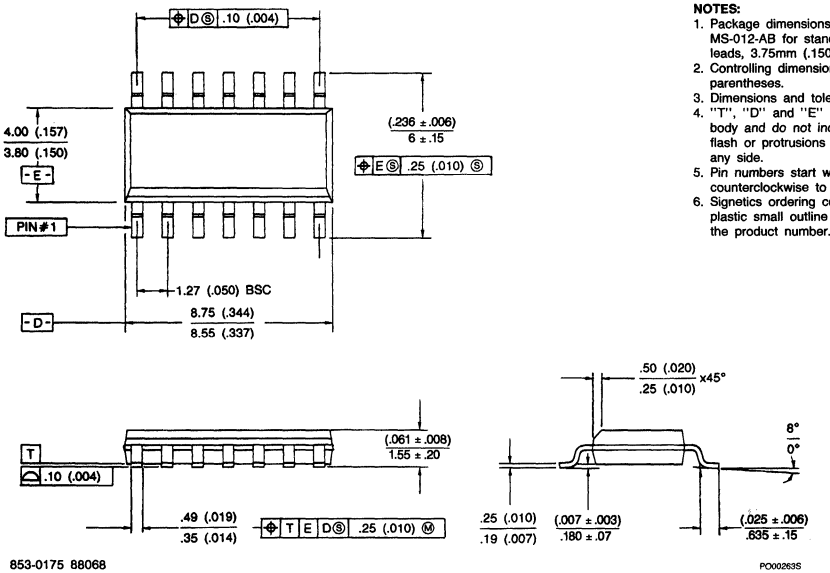


853-0174 88070

PO00273S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

14-PIN PLASTIC SO (D PACKAGE)



853-0175 88068

PO00263S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

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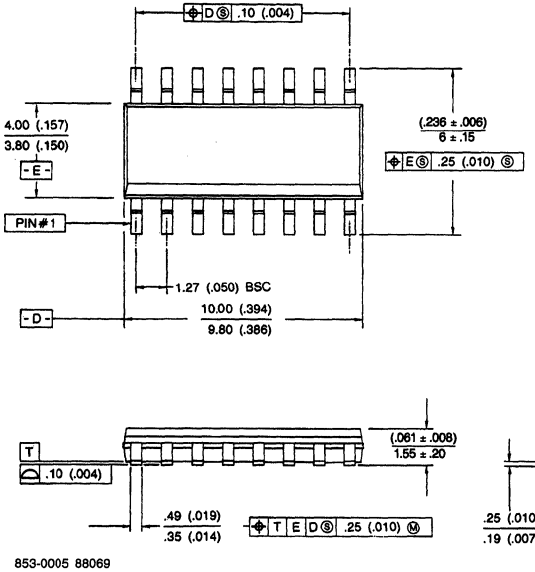
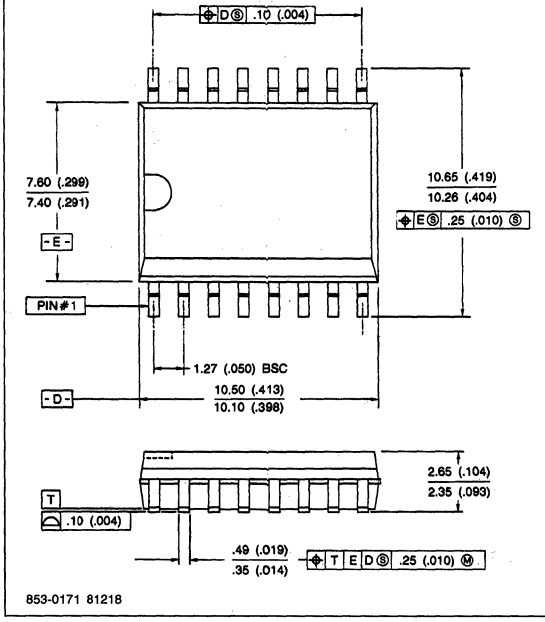
16-PIN PLASTIC SO (D PACKAGE)



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SOL (D PACKAGE)

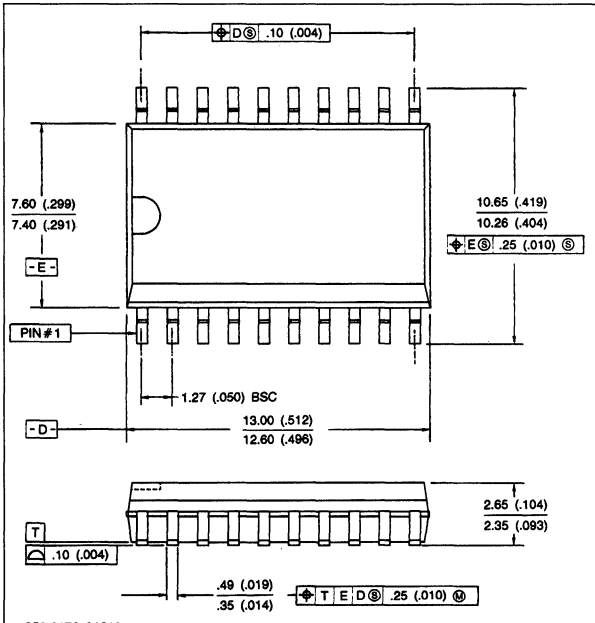


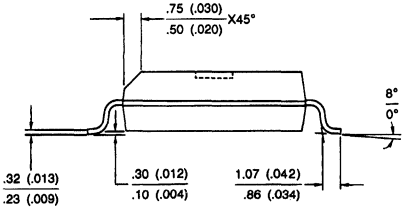
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

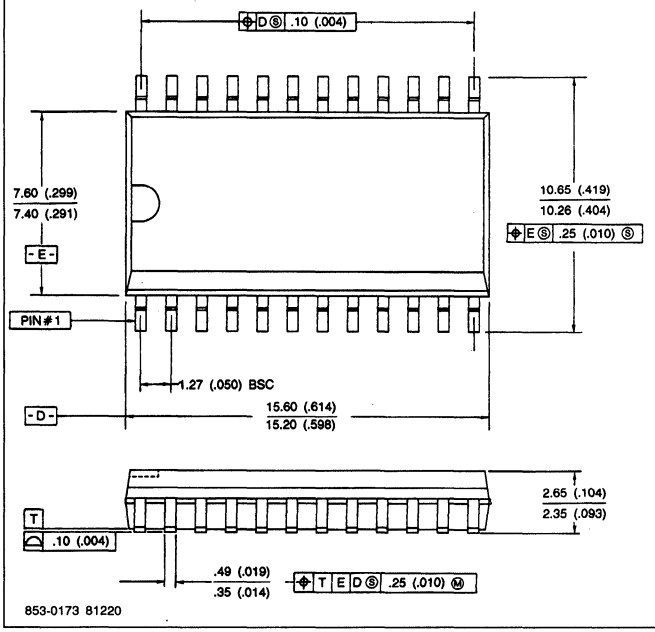
20-PIN PLASTIC SOL (D PACKAGE)

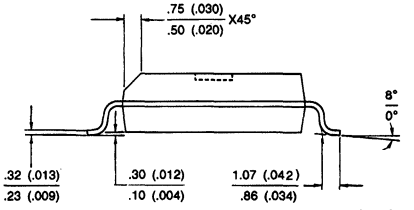




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

24-PIN PLASTIC SOL (D PACKAGE)



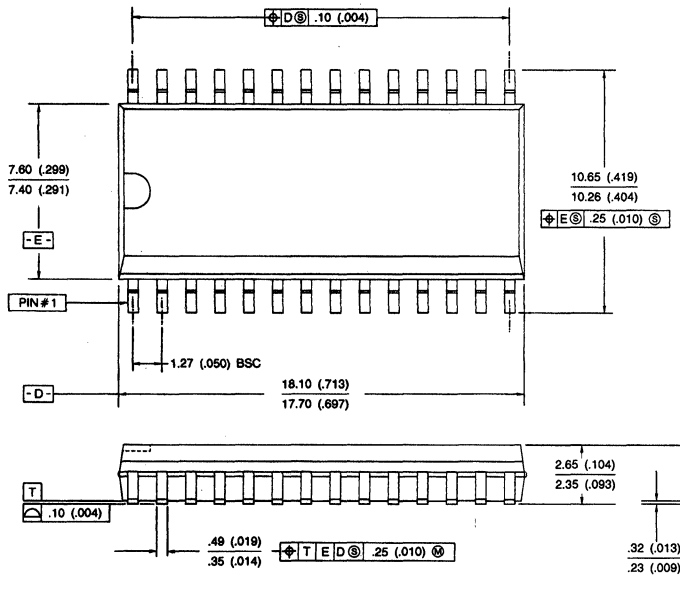


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

28-PIN PLASTIC SOL (D PACKAGE)



NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

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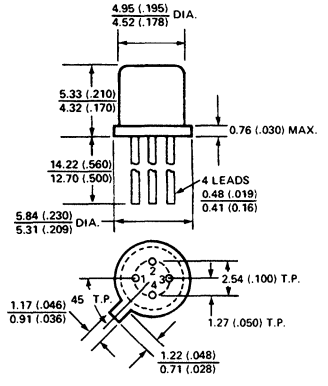
PO00212S

4-PIN HERMETIC TO-72 HEADER (E PACKAGE)

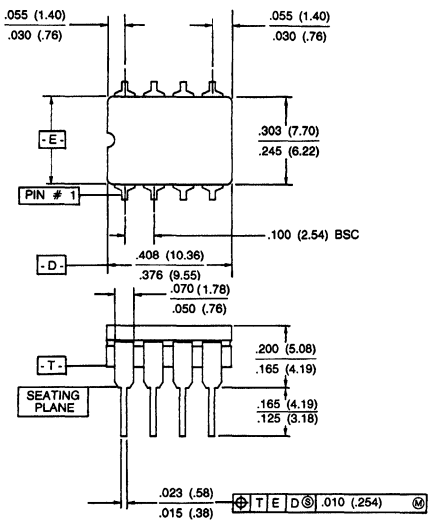


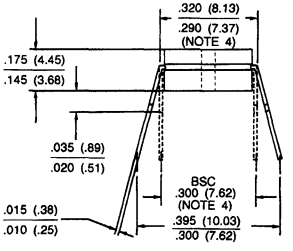
PO00970S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

8-PIN CERDIP (FE PACKAGE)



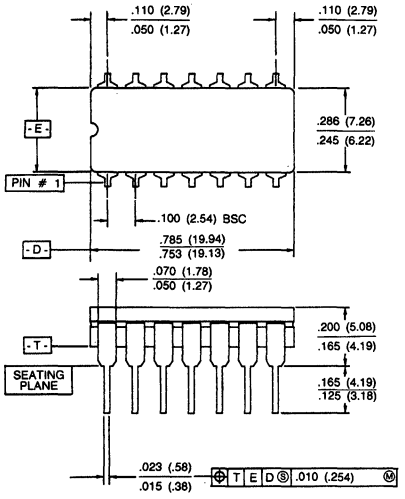


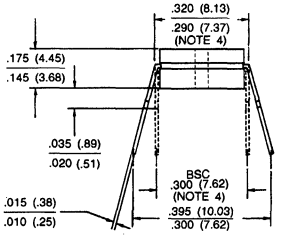
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0580 81594

PO00480S

14-PIN CERDIP (F PACKAGE)





NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0581 81594

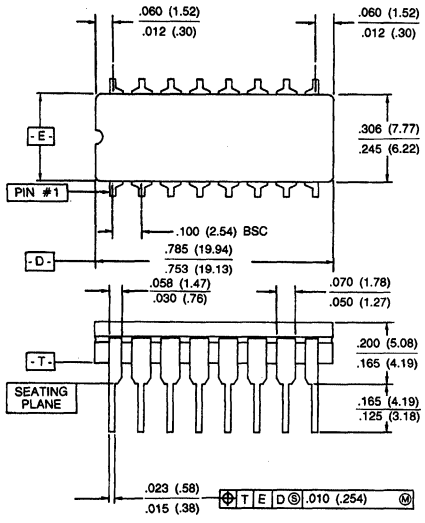
PO00440S

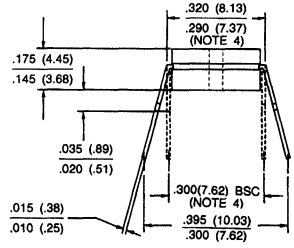
15

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

16-PIN CERDIP (F PACKAGE)



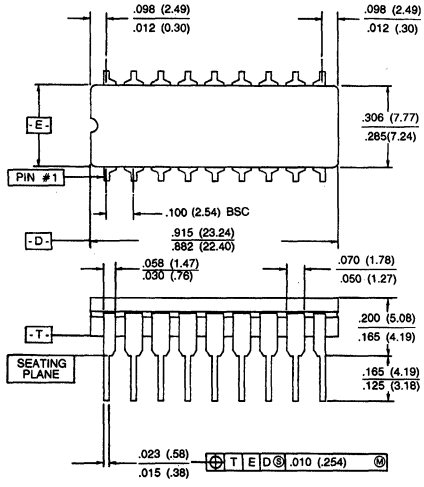


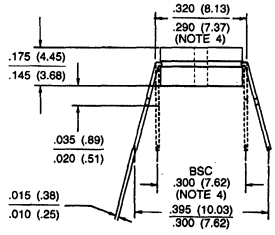
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0582 81594

PO00490S

18-PIN CERDIP (F PACKAGE)



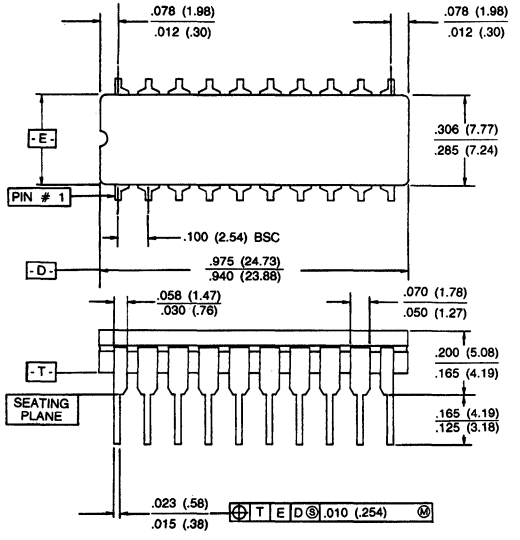


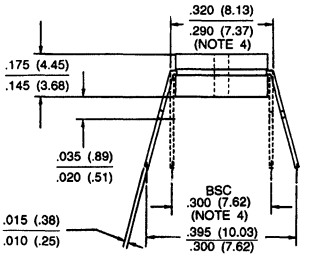
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

853-0583 81594

PO00470S

20-PIN CERDIP (F PACKAGE)



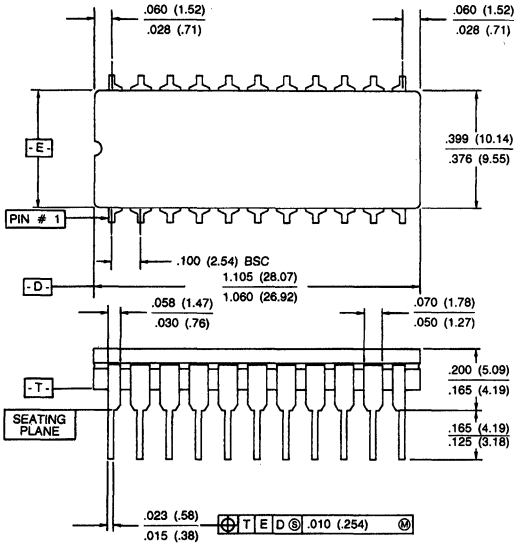


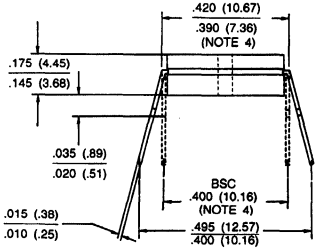
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0584 81594

PO00430S

22-PIN CERDIP (F PACKAGE)





NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

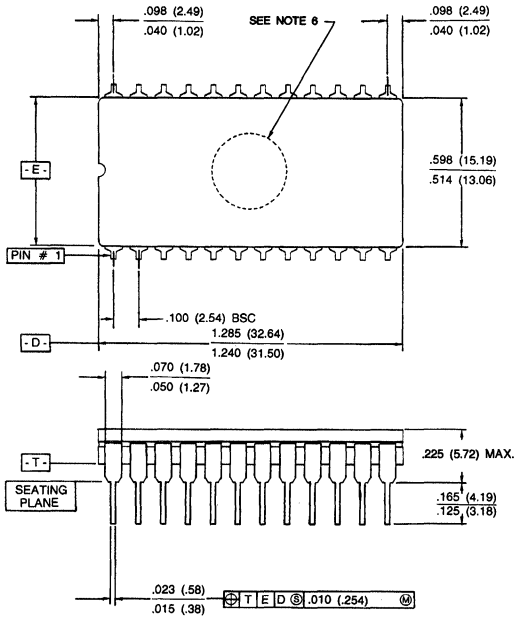
853-0585 81594

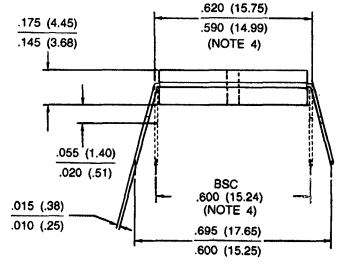
PO00420S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

24-PIN CERDIP (F PACKAGE)



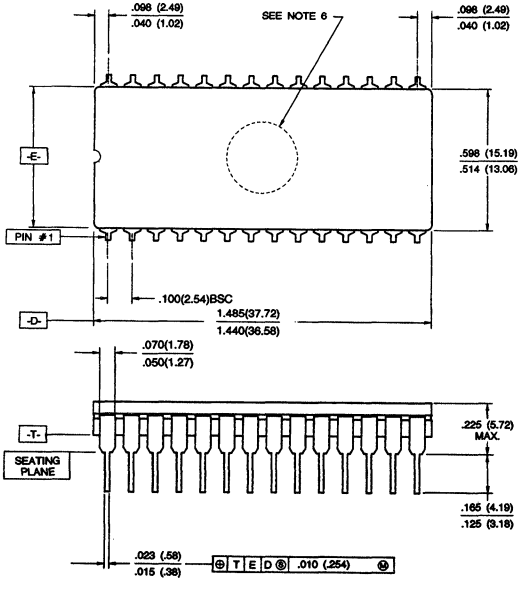


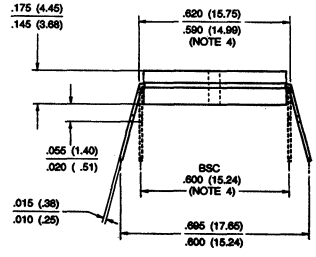
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0588 84221

PO00464S

28-PIN CERDIP (F PACKAGE)



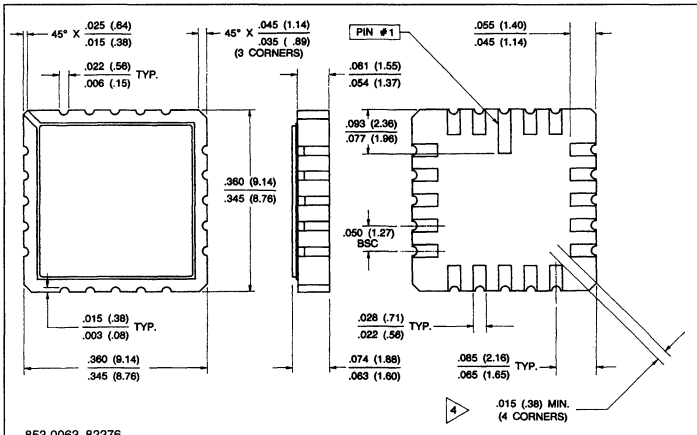


NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM Products.

853-0589 84000

PO00660S

20-PIN PGA (G PACKAGE)

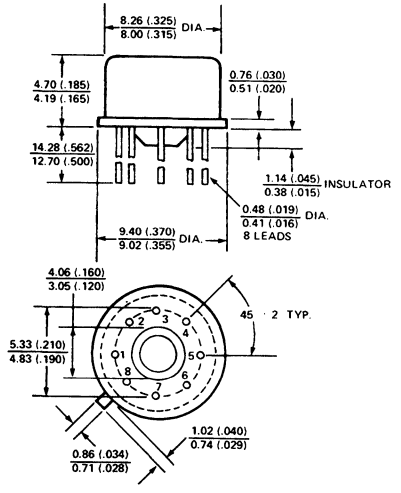


853-0063 82276

PO00870S

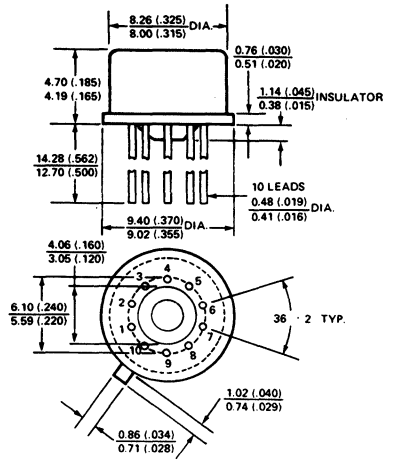
NOTES:
1. Package dimensions conform to Mil-M-38510, outline NO. C – 2, 20 leads, square ceramic leadless chip carrier.
2. Controlling dimension: inches, millimeters are shown in parenthesis.
3. Dimension and tolerancing per ANSI Y14.5M – 1982.
4. This dimension represents the minimum spacing between the corner contact pads. These corner pads may have a .020 inch by 45 degree maximum chamfer to accomplish the .015 minimum spacing.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.
6. Signetics order code for product packaged in a CCCL is the suffix "G" after the product number.

8-PIN HERMETIC TO-5 HEADER (H PACKAGE)

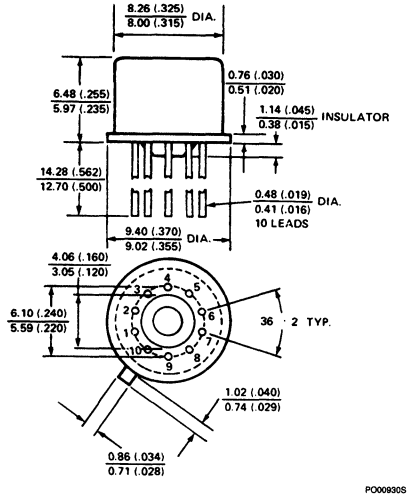


PO00910S

10-PIN HERMETIC TO-5/100 HEADER SHORT CAN (H PACKAGE)



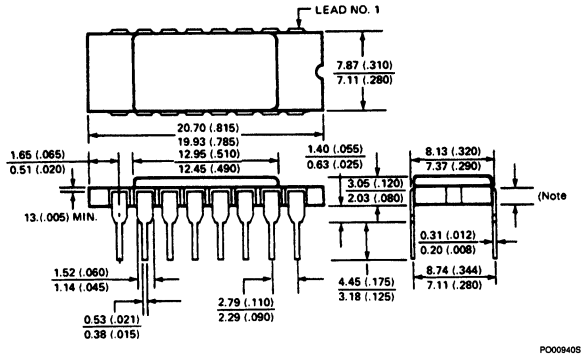
10-PIN HERMETIC TO-5/100 HEADER TALL CAN (H PACKAGE)



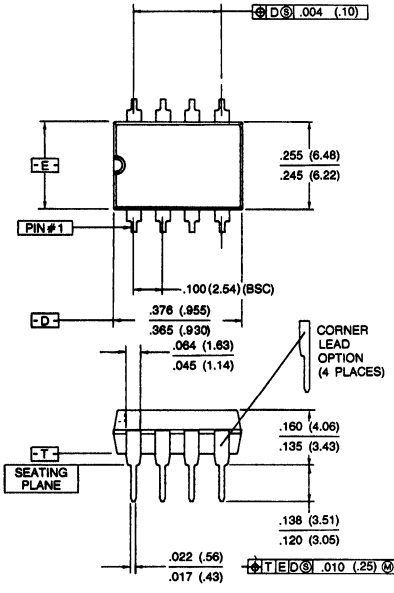
For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

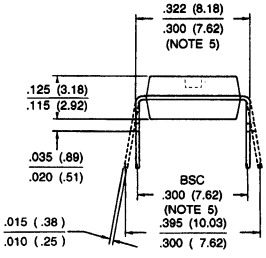
Package Outlines

16-PIN HERMETIC SDIP (I PACKAGE)



8-PIN PLASTIC PDIP (N PACKAGE)





853-0404 81230

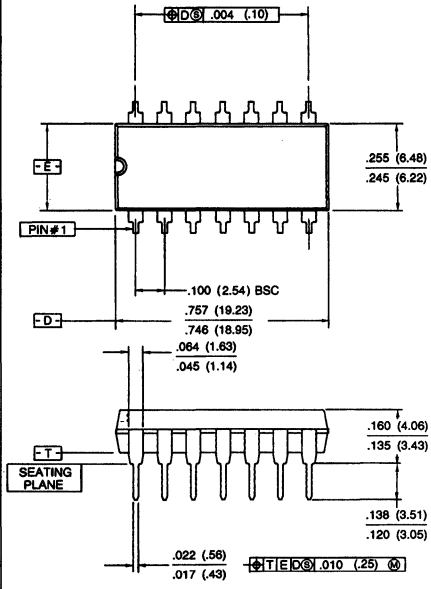
PO00312S

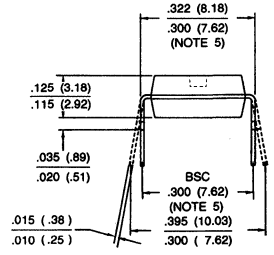
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

14-PIN PLASTIC DIP (N PACKAGE)



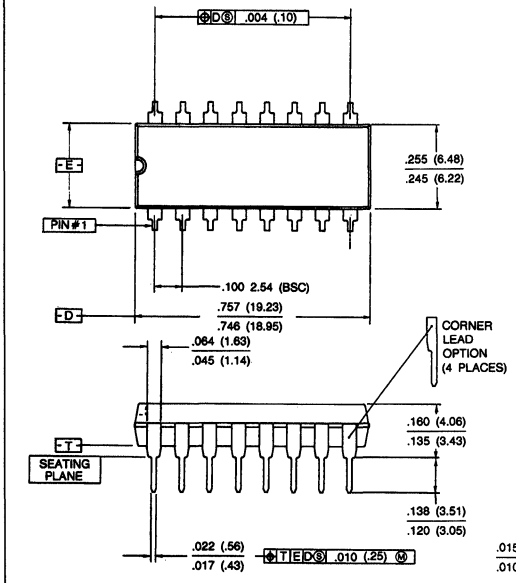


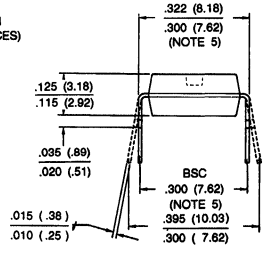
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405 81231

PO00330S

16-PIN PLASTIC DIP (N PACKAGE)



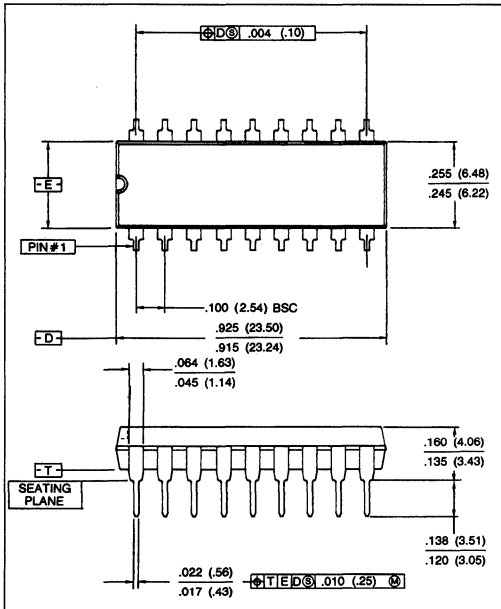


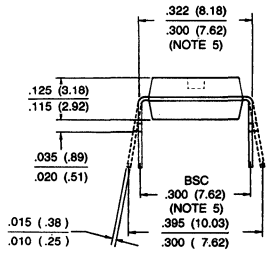
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO00280S

18-PIN PLASTIC DIP (N PACKAGE)



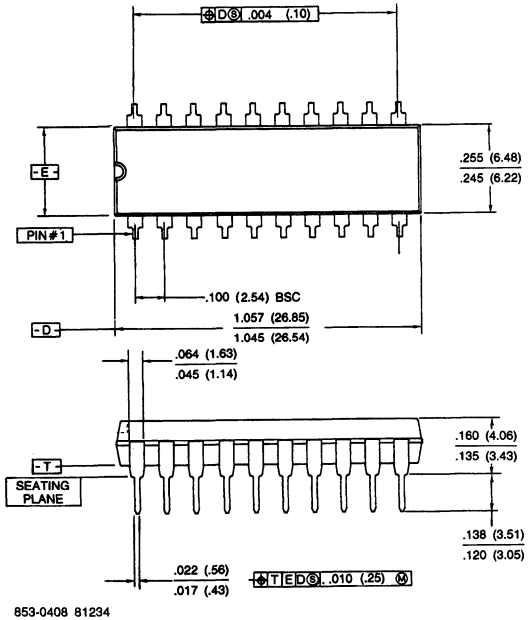


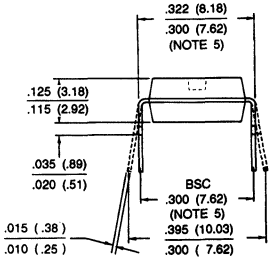
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AD for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

853-0407 81233

PO00300S

20-PIN PLASTIC DIP (N PACKAGE)





NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

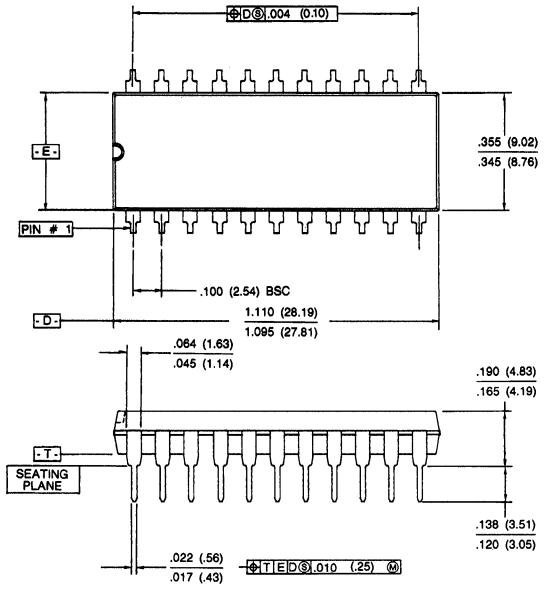
853-0408 81234

PO00290S

For Prefixes ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

Package Outlines

22-PIN PLASTIC DIP (N PACKAGE)

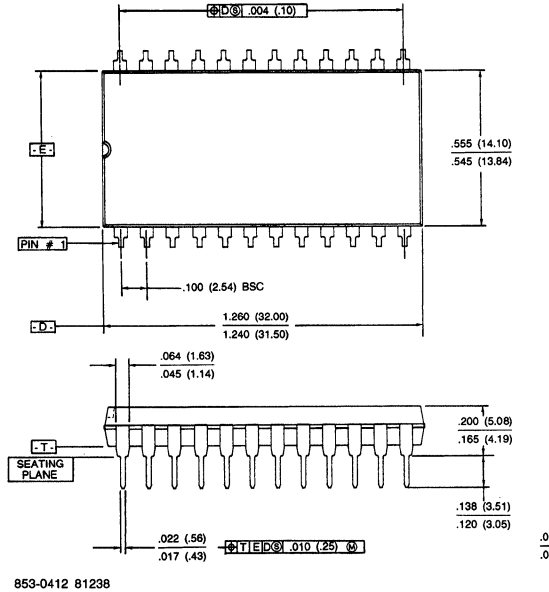


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-010-AA for standard dual in-line (DIP) package .400 inch row spacing (PLASTIC) 22 leads (issue A. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

853-0409 81235

PO00341S

24-PIN PLASTIC DIP (N PACKAGE)

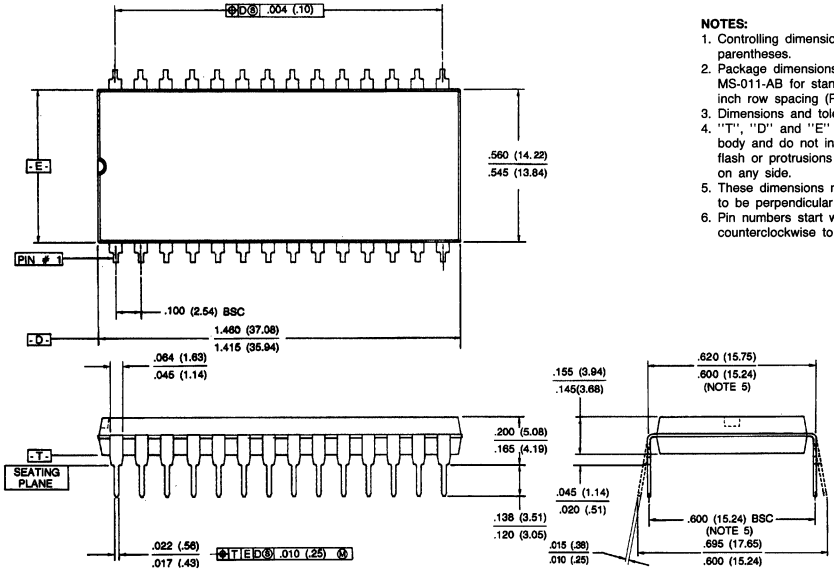


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0412 81238

PO00361S

28-PIN PLASTIC DIP (N PACKAGE)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413 84099

PO00372S

Package Outlines
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

INTRODUCTION

Soldering

1. By hand
Apply the soldering iron below the seating plane (or not more than 2mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300°C and 400°C, for not more than 5 seconds.

2. By dip or wave
The maximum permissible temperature of the solder is 260°C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints
The same precautions and limits apply as in (1) above.

SMALL OUTLINE (SO) PACKAGES

The Reflow Solder Technique

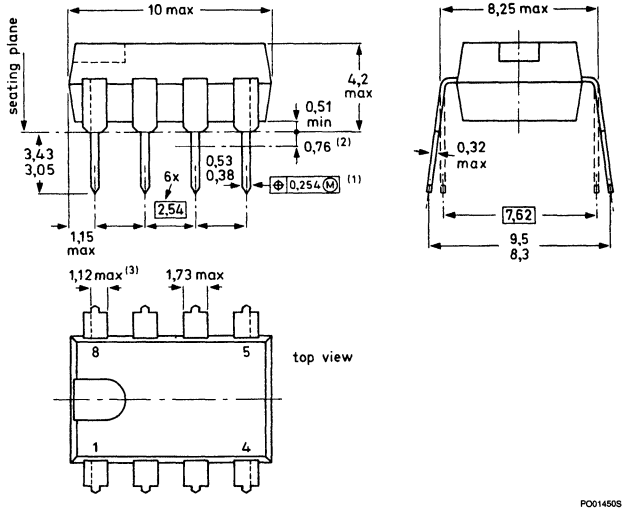
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230°C when a mild flux is used.

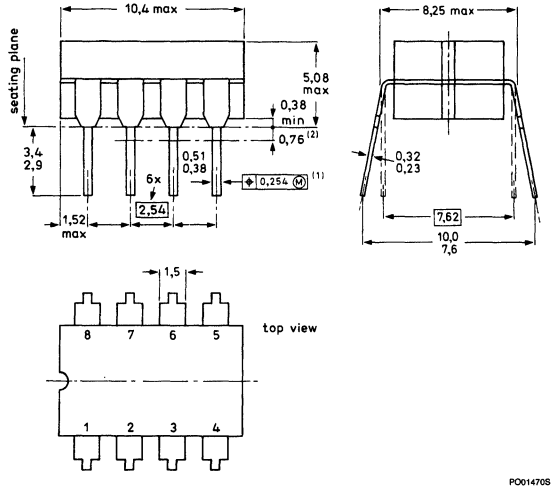
For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105μm is used for which the emulsion thickness should be about 50μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.

8-PIN PLASTIC SO (SOT-97A)



8-PIN CERDIP (SOT-151A)



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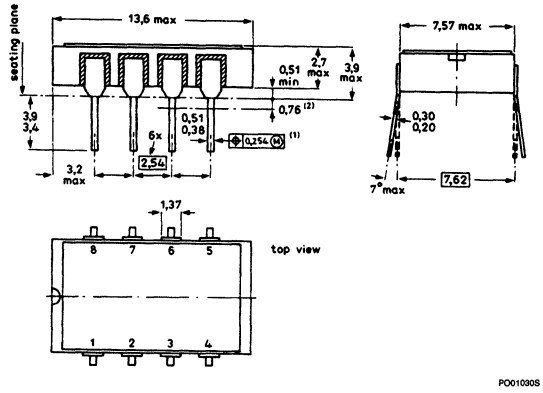
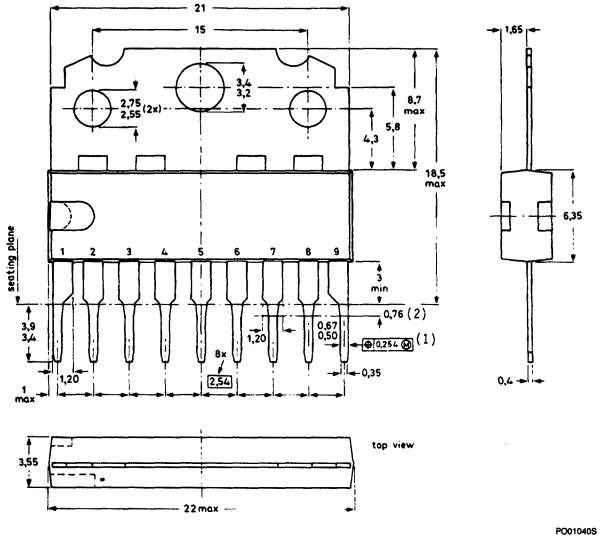
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

8-PIN METAL CERDIP (SOT-153B)



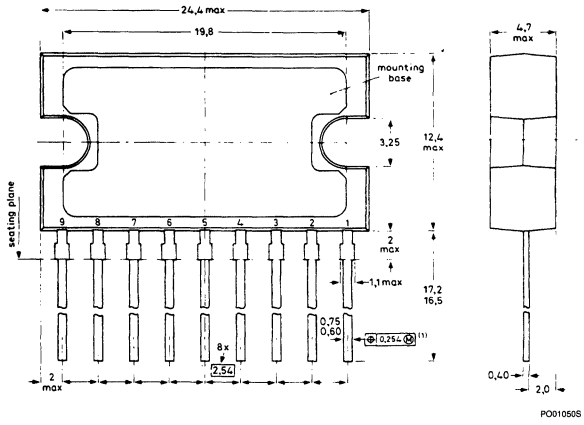
9-PIN PLASTIC SIP (SOT-110B)



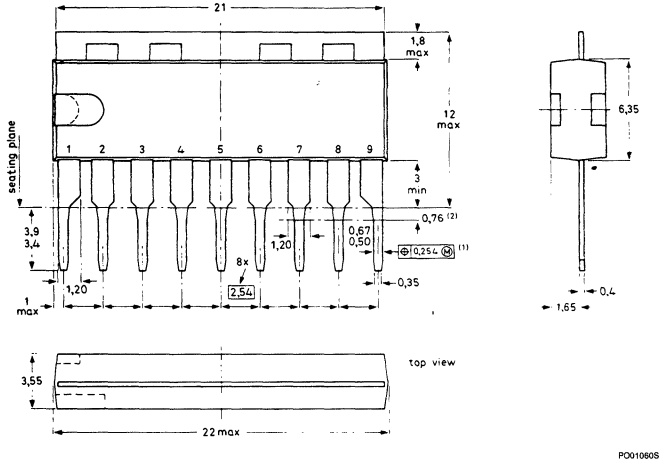
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

9-PIN PLASTIC POWER SIP (SOT-131A, B)



9-PIN PLASTIC SIP (SOT-142)



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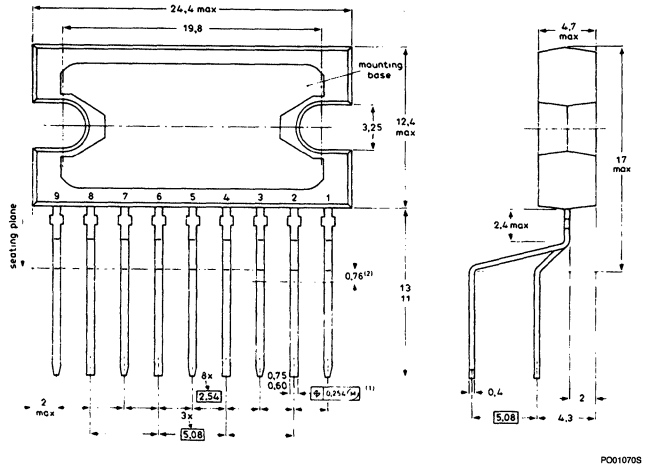
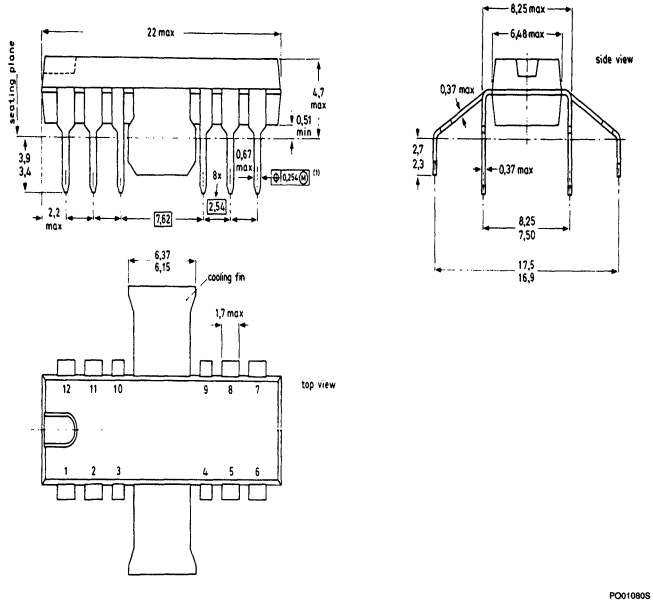
9-PIN PLASTIC POWER SIP-BENT-TO-DIP (SOT-157B)



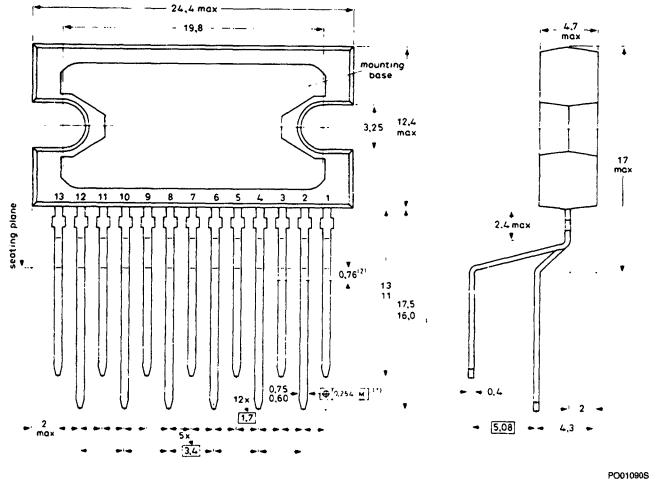
12-PIN PLASTIC DIP WITH METAL COOLING FIN (SOT-150)



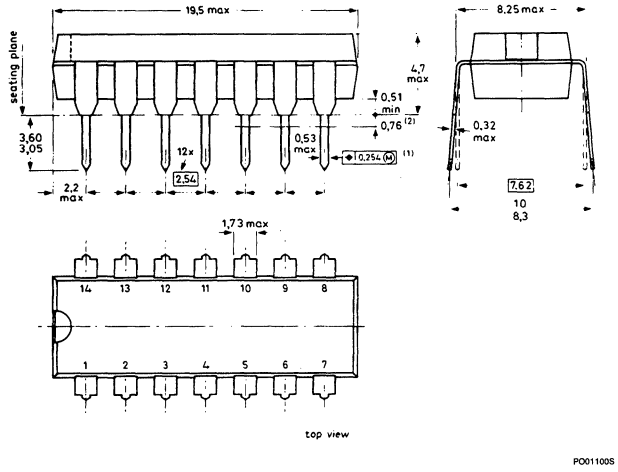
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

13-PIN PLASTIC POWER SIP-BENT-TO-DIP (SOT-141B)



14-PIN PLASTIC DIP (SOT-27K, M, T)



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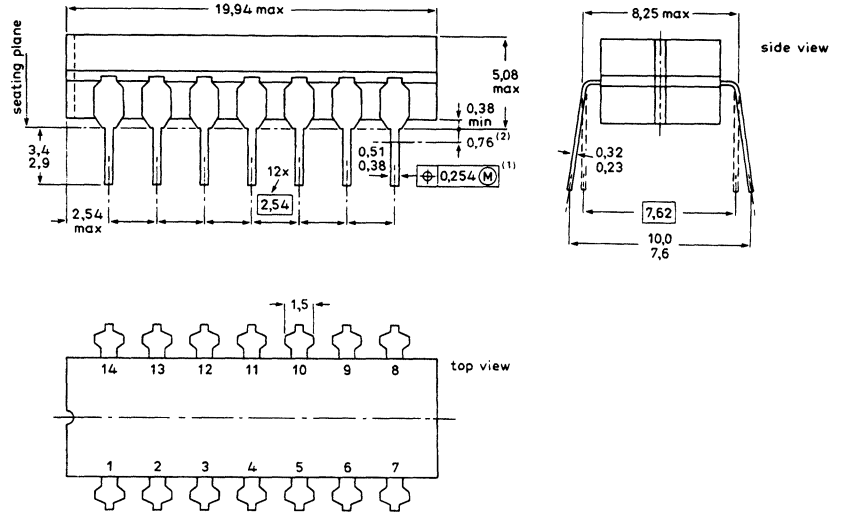
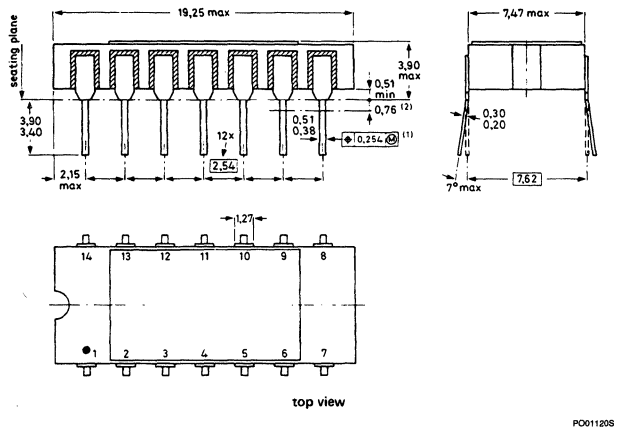
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

14-PIN CERDIP (SOT-73A, B, C)



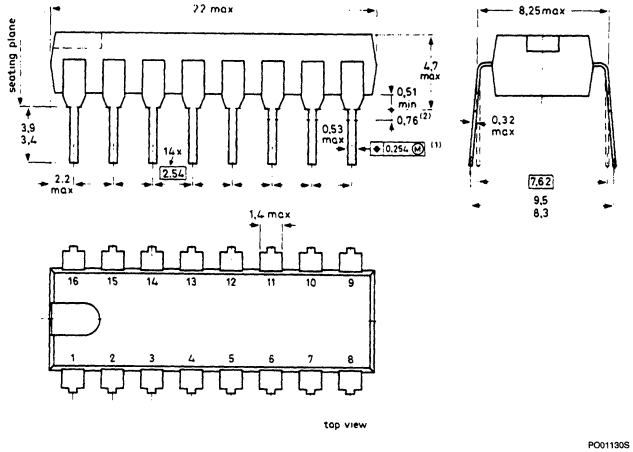
14-PIN METAL CERDIP (SOT-83B)



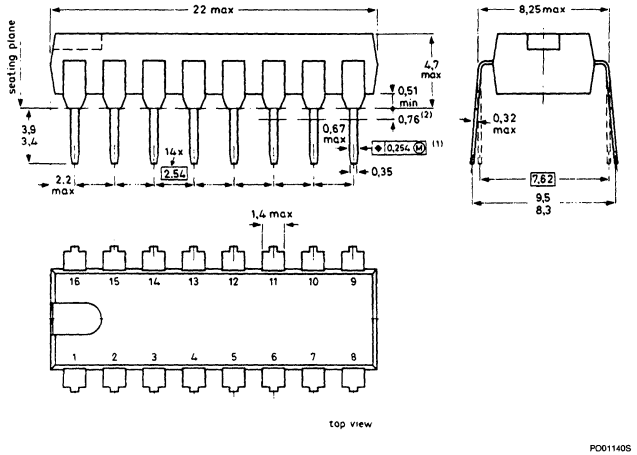
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

16-PIN PLASTIC DIP (SOT-38)



16-PIN PLASTIC DIP (SOT-38A)



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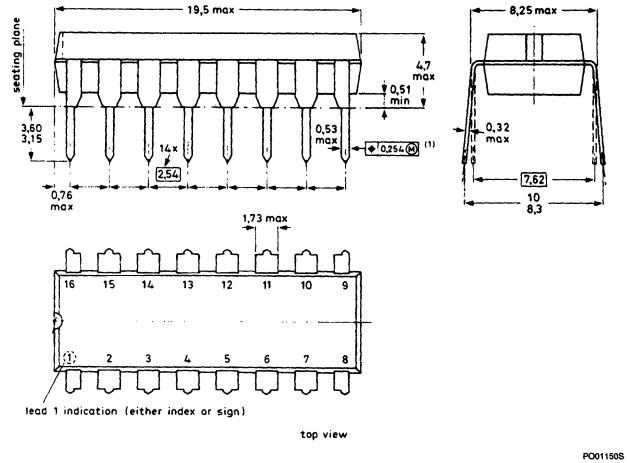
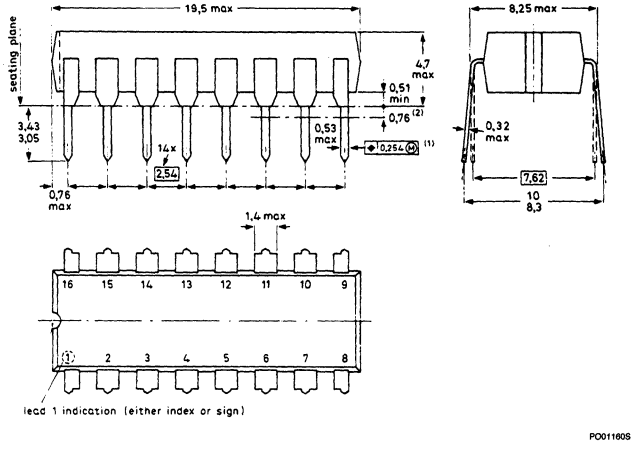
16-PIN PLASTIC DIP (SOT-38D, DE)



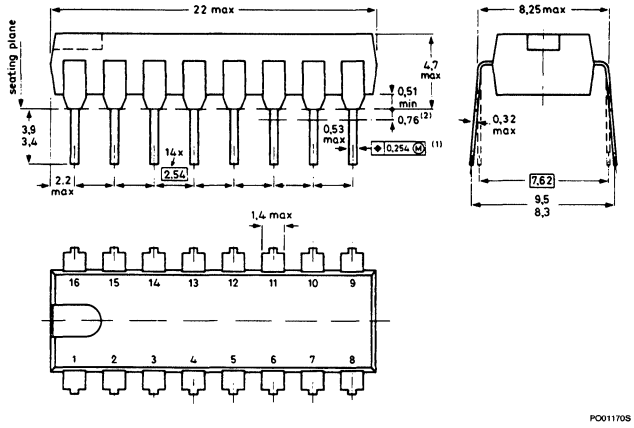
16-PIN PLASTIC DIP (SOT-38Z)



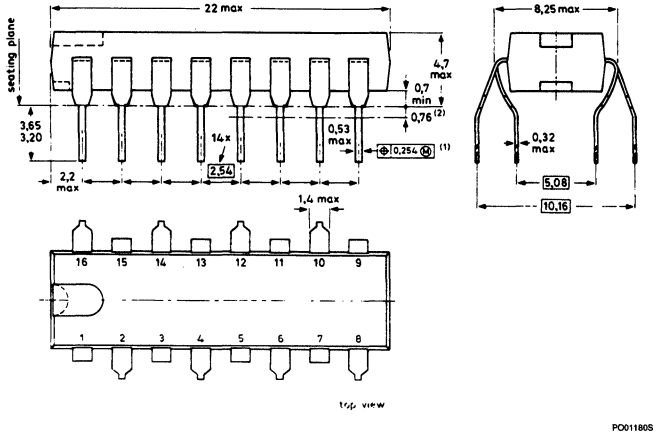
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

16-PIN PLASTIC DIP WITH INTERNAL HEAT SPREADER (SOT-38WE-2)



16-PIN PLASTIC QIP (SOT-58)



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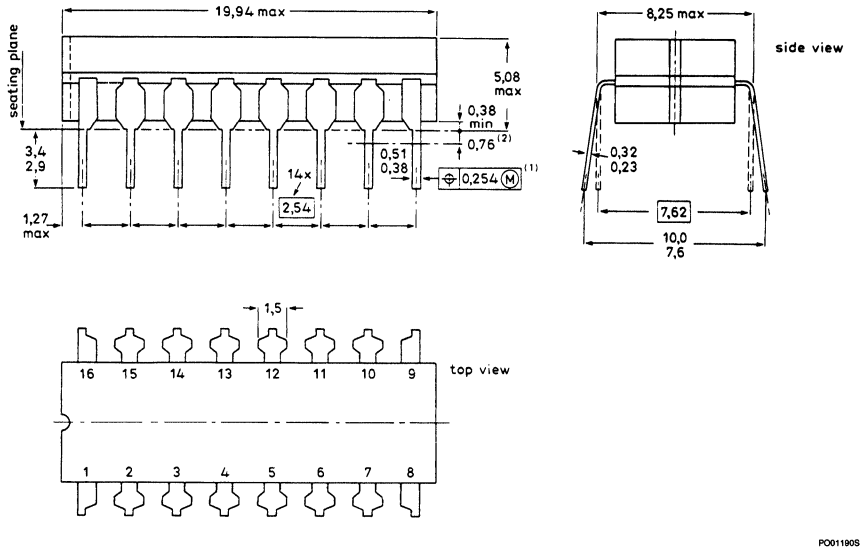
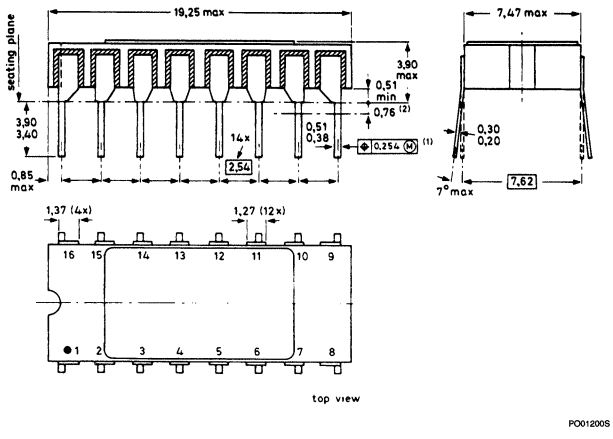
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

16-PIN CERDIP (SOT-74A, B, C)

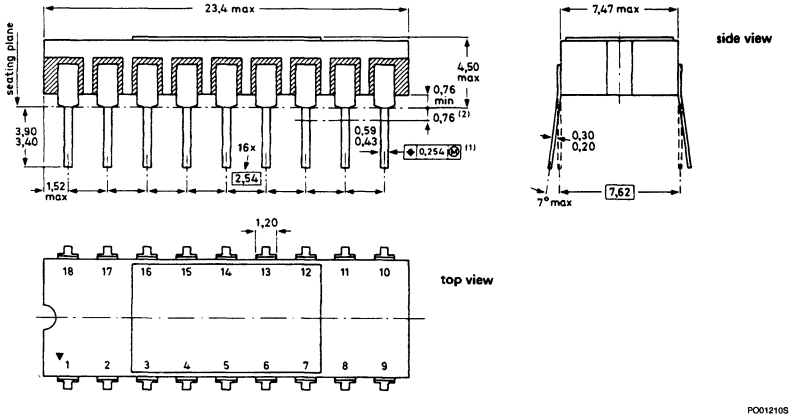


16-PIN METAL CERDIP (SOT-84B)

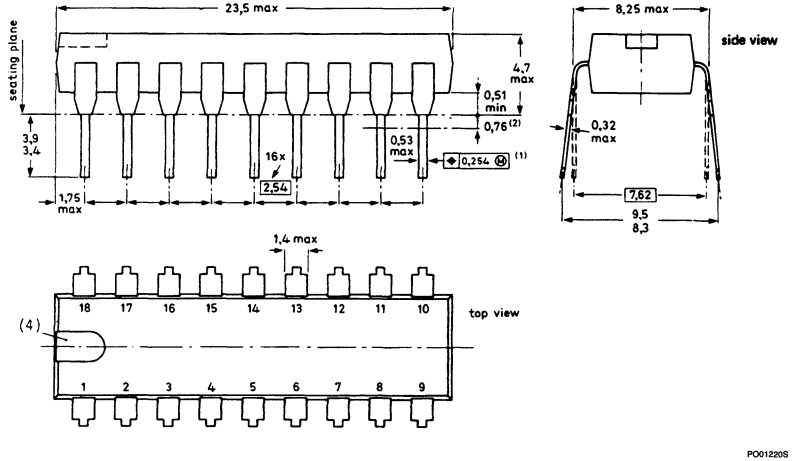


For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA — Package Outlines

18-PIN METAL CERDIP (SOT-85B)



18-PIN PLASTIC DIP (SOT-102A)



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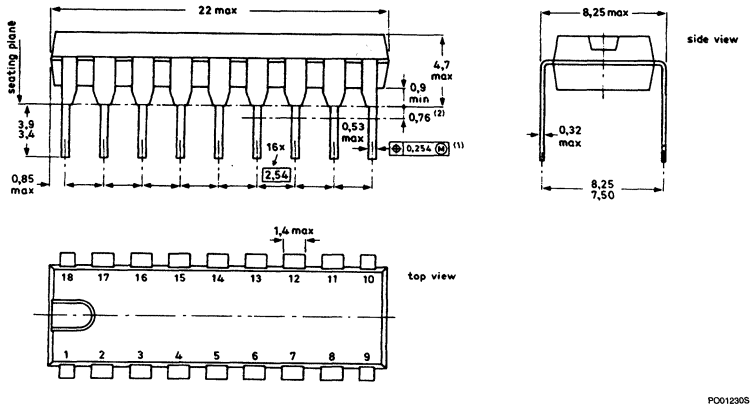
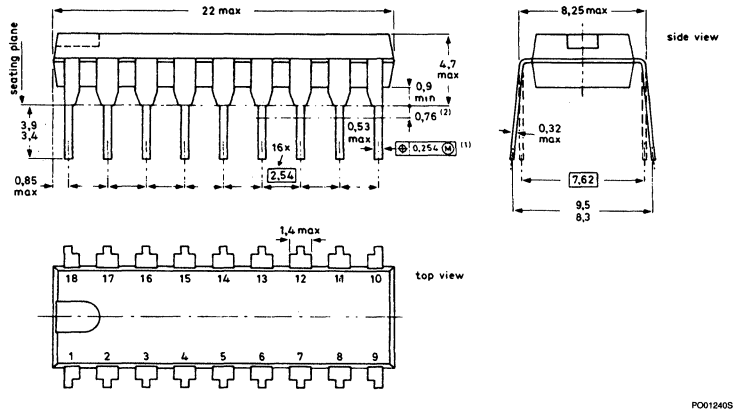
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

18-PIN PLASTIC DIP (SOT-102C)



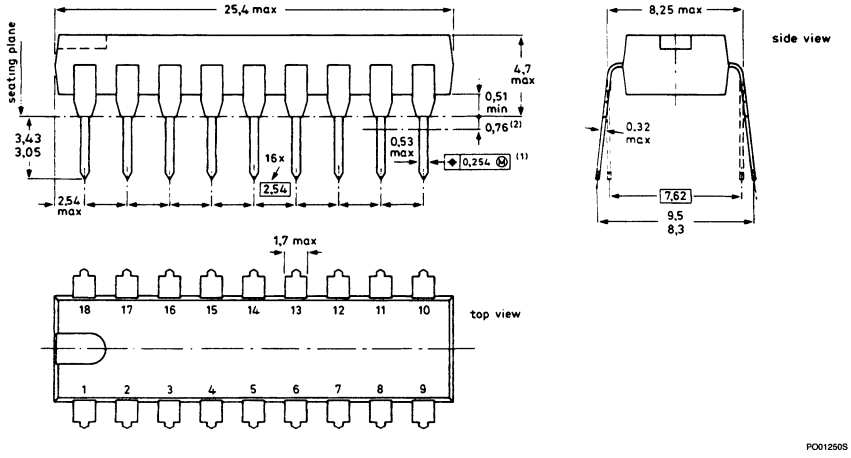
18-PIN PLASTIC DIP (SOT-102CS)



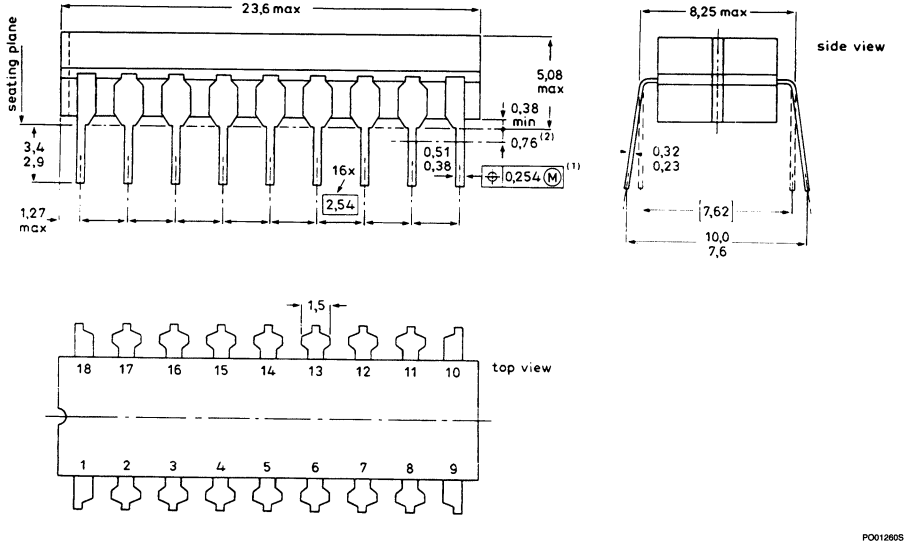
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

18-PIN PLASTIC DIP (SOT-102G)



18-PIN CERDIP (SOT-133A, B)



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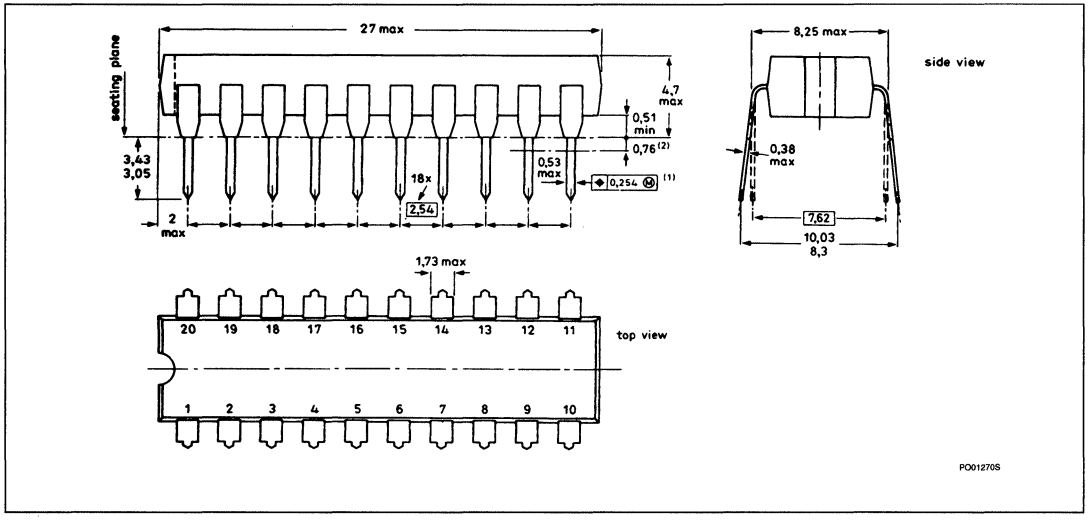
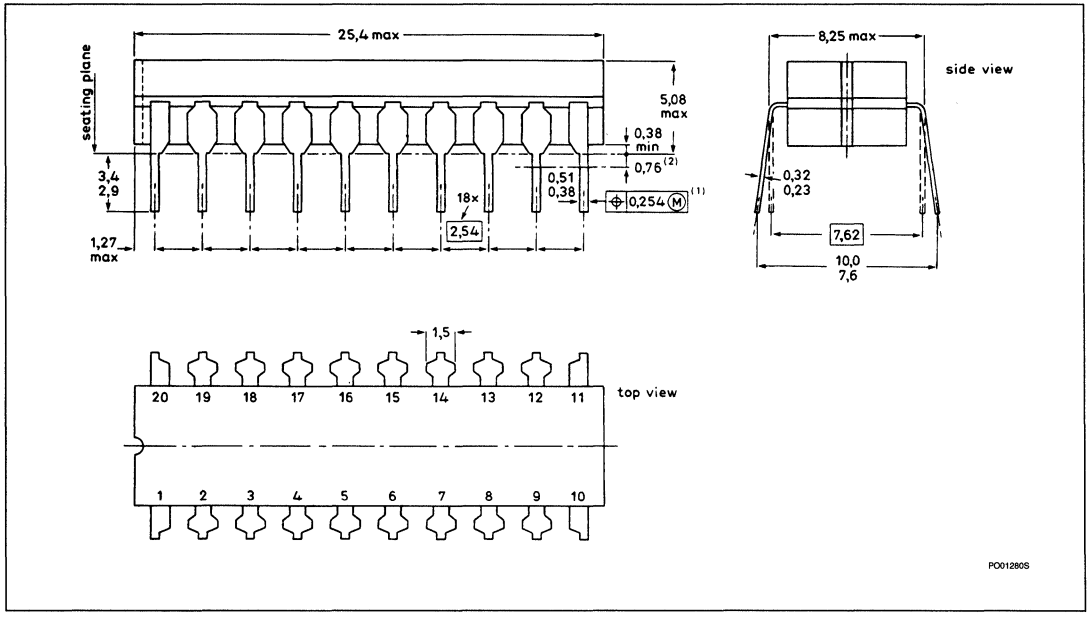
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

20-PIN PLASTIC DIP (SOT-146)



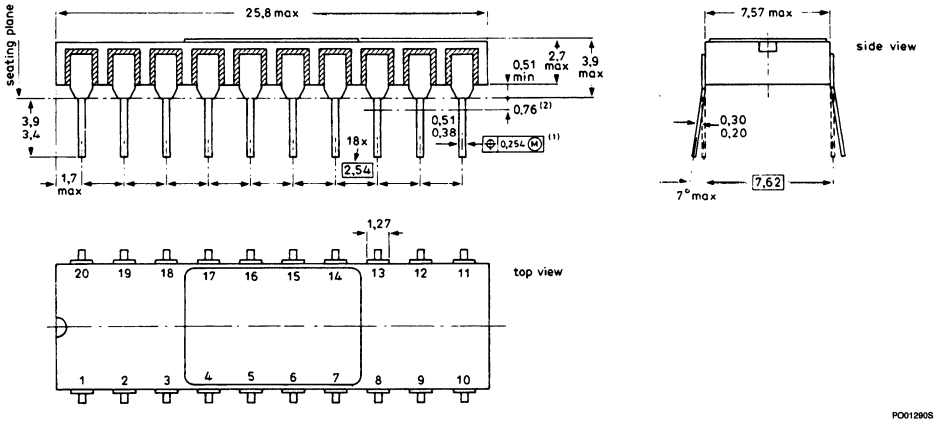
20-PIN CERDIP (SOT-152B, C)



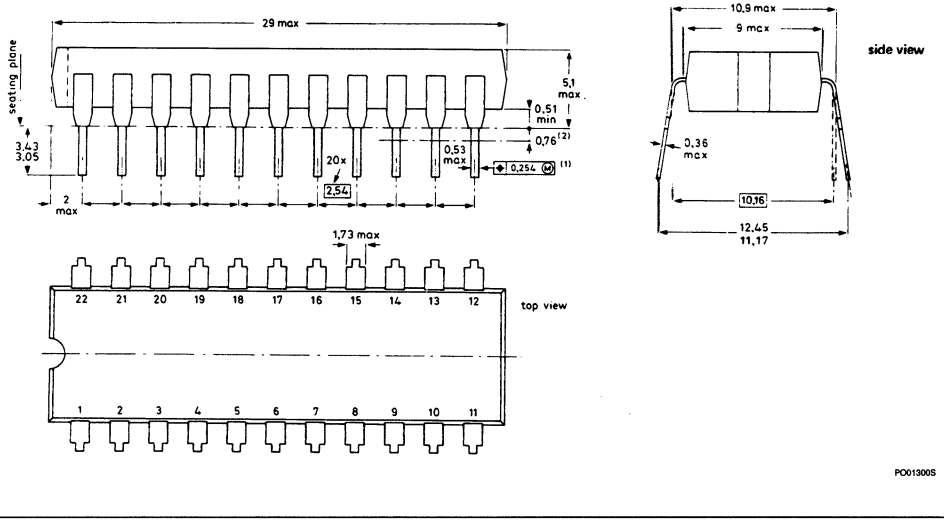
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

20-PIN METAL CERDIP (SOT-154B)



20-PIN PLASTIC DIP (SOT-116)



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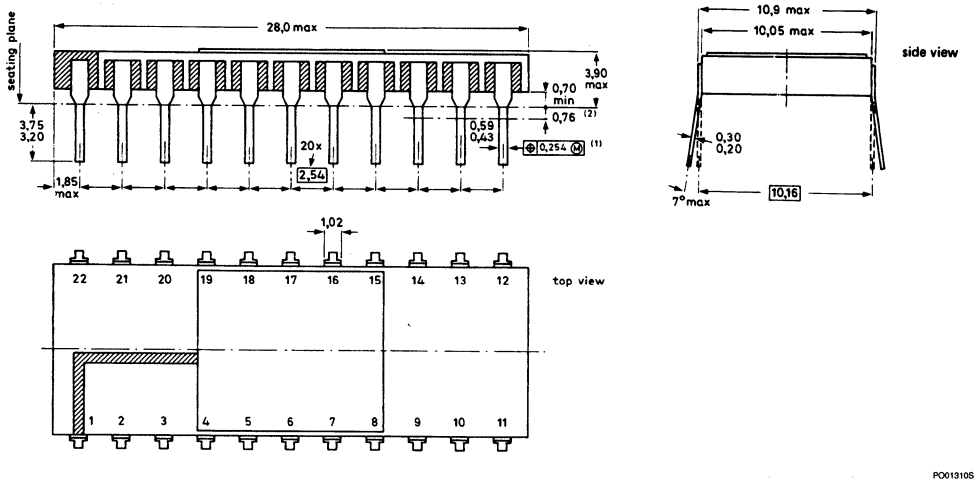
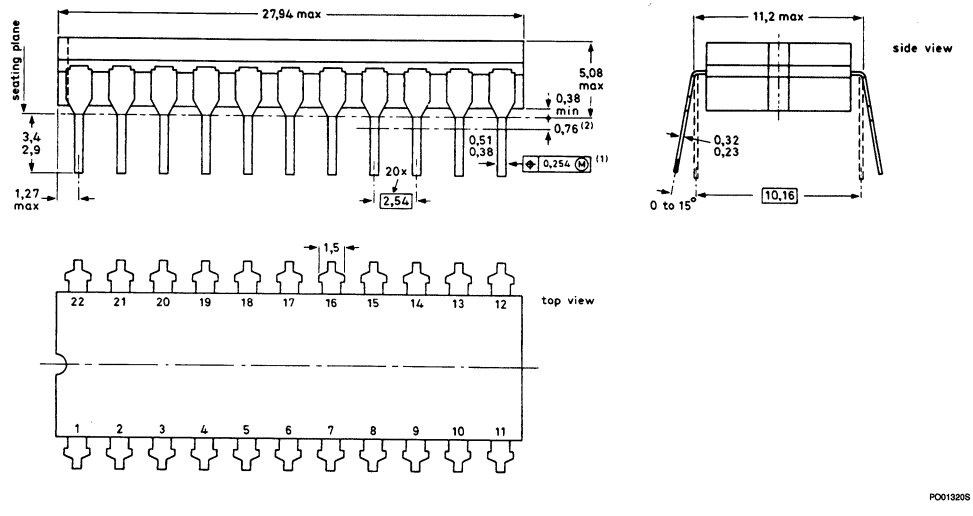
22-PIN METAL CERDIP (SOT-118B)



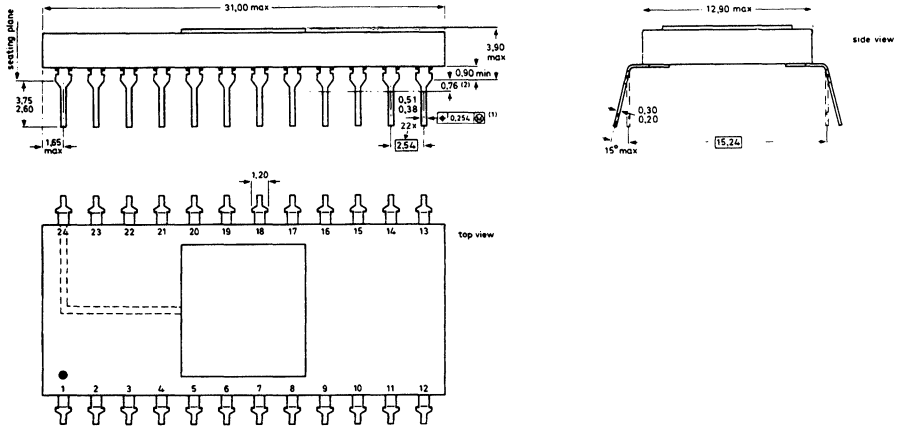
22-PIN CERDIP (SOT-134A)



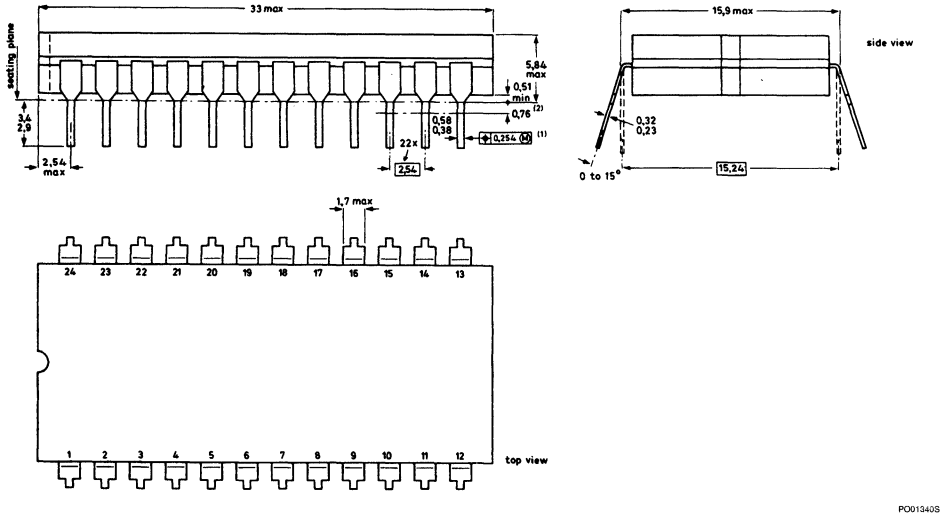
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

24-PIN METAL CERDIP (SOT-86A)



24-PIN CERDIP (SOT-94)



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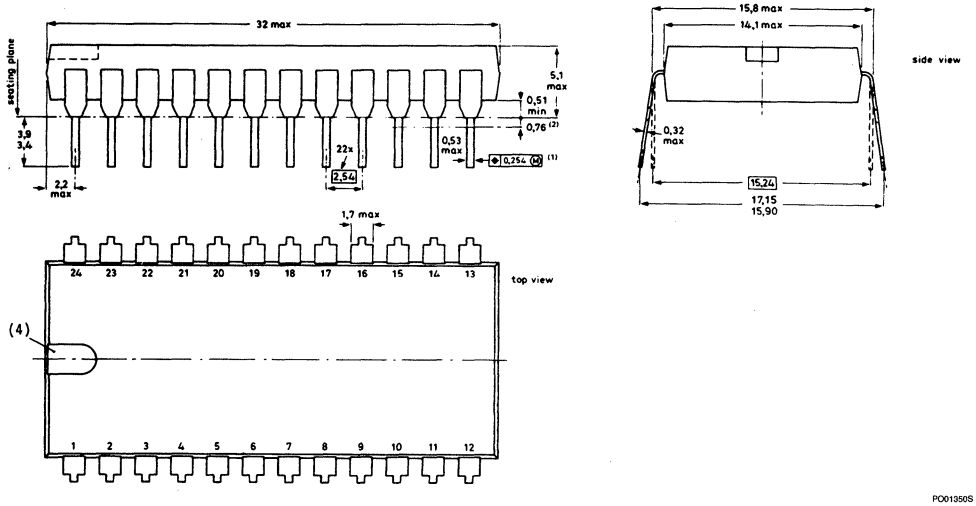
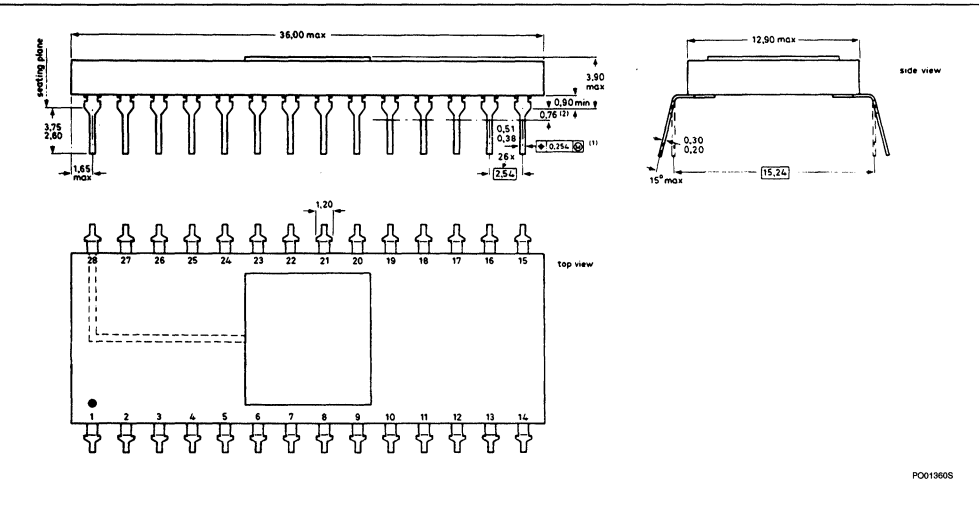
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

24-PIN PLASTIC DIP WITH INTERNAL HEAT SPREADER (SOT-101A, B)



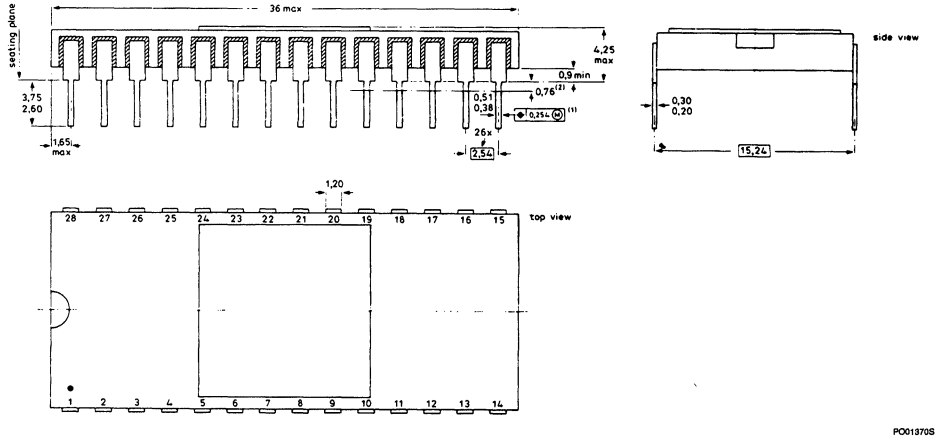
28-PIN METAL CERDIP (SOT-87A)



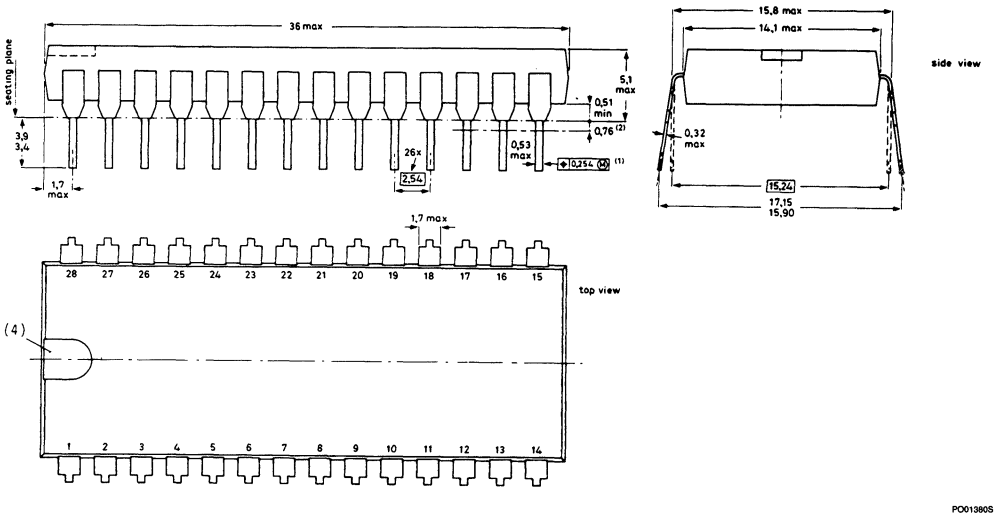
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

28-PIN METAL CERDIP (SOT-87B)



28-PIN PLASTIC DIP (SOT-117)



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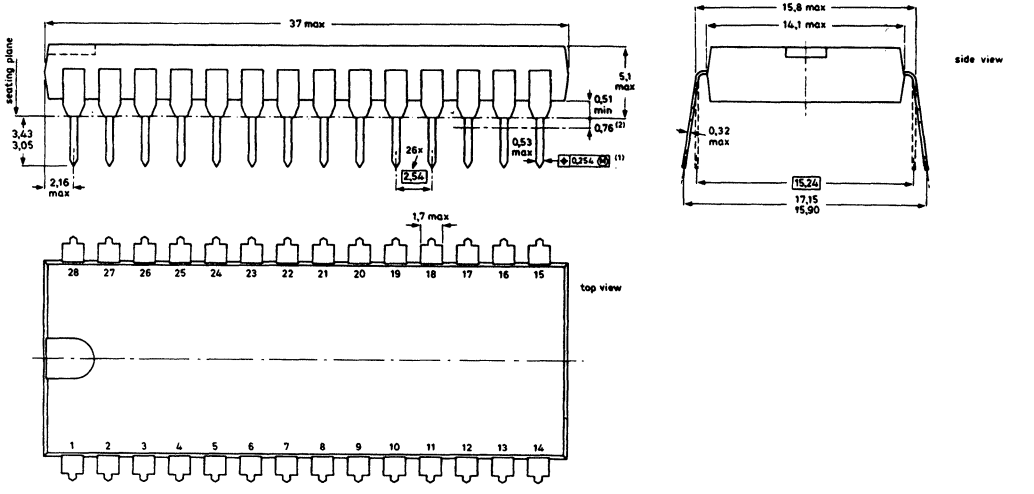
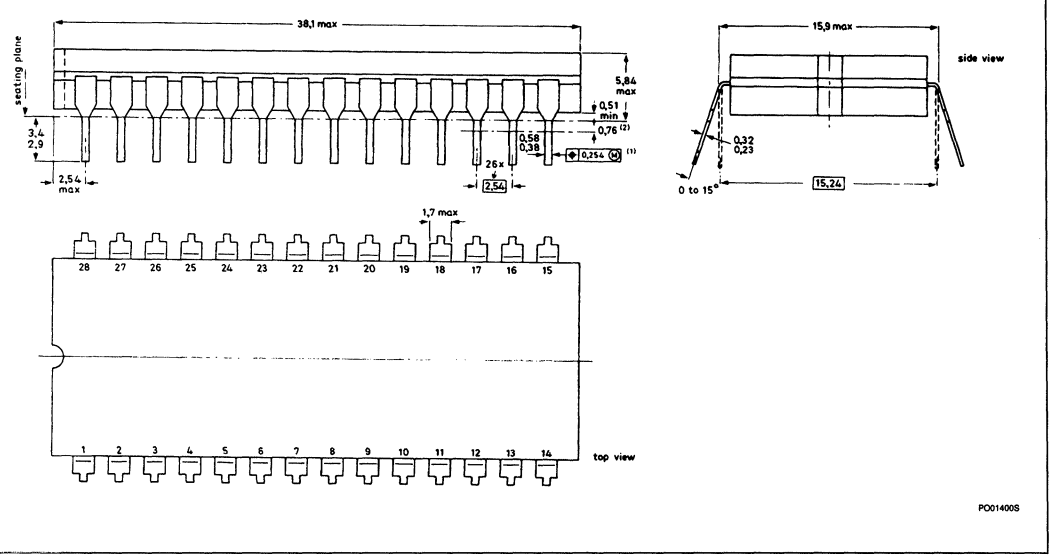
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

28-PIN PLASTIC DIP (SOT-117D)



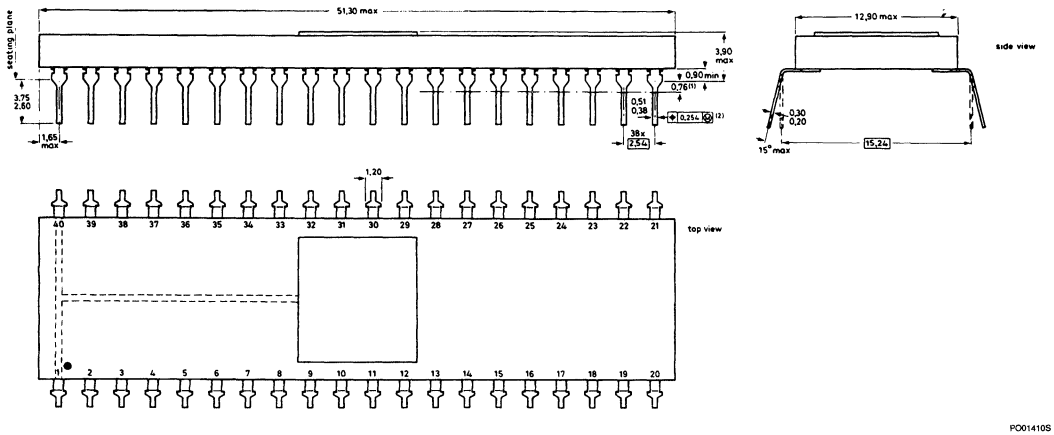
28-PIN CERDIP (SOT-135A)



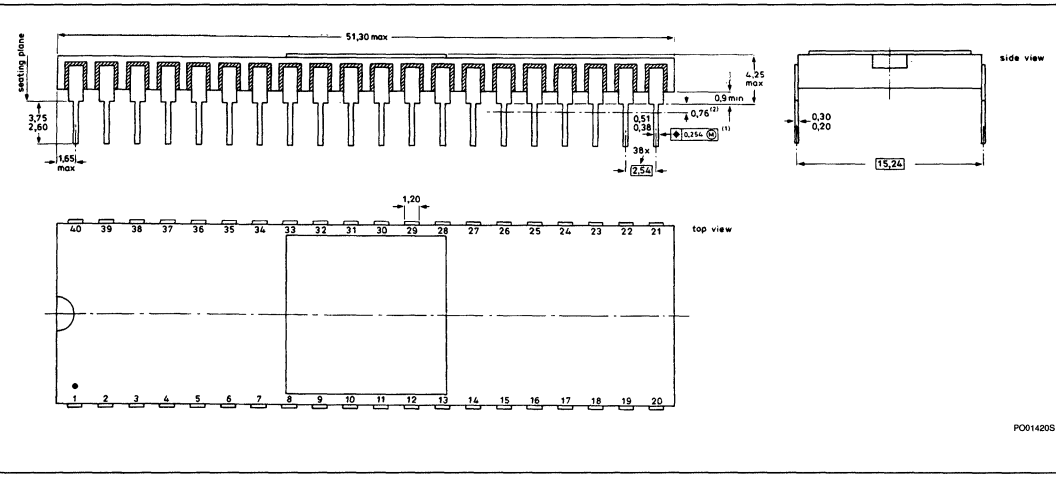
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

40-PIN METAL CERDIP (SOT-88)



40-PIN METAL CERDIP (SOT-88B)



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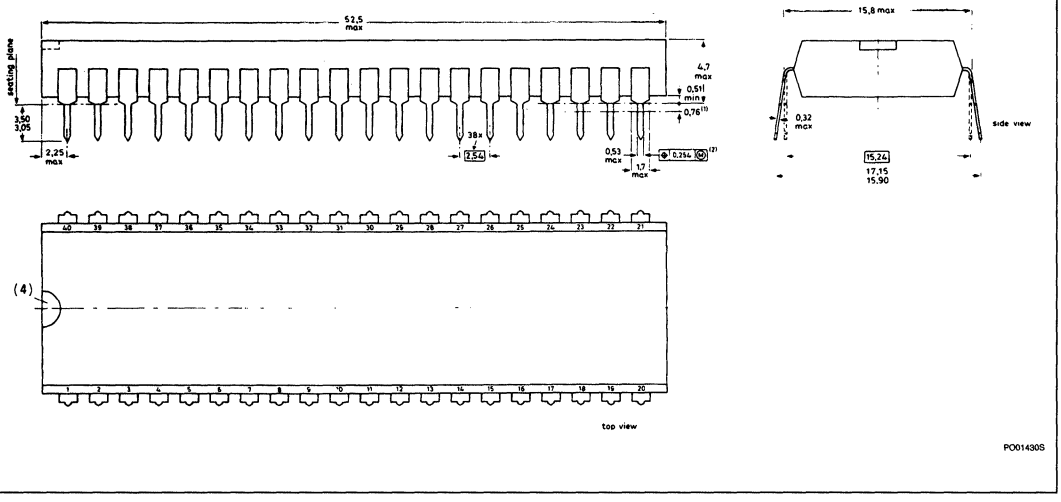
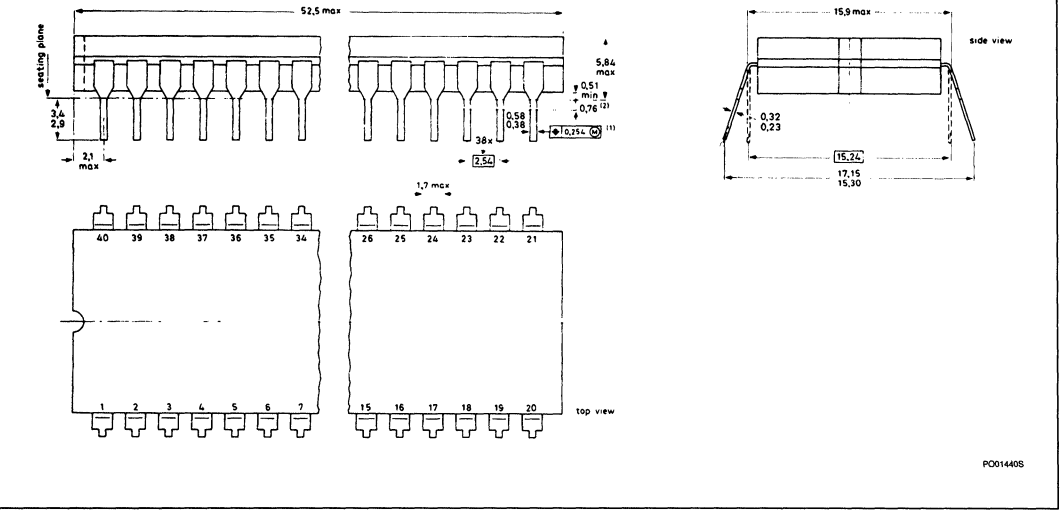
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

40-PIN PLASTIC DIP (SOT-129)



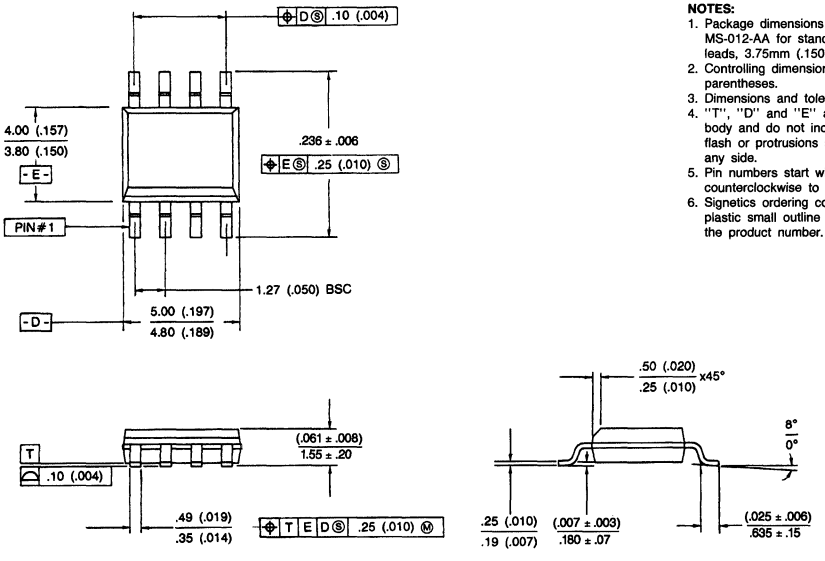
40-PIN CERDIP (SOT-145)



For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

8-PIN PLASTIC SO (D PACKAGE) (SO-8, SOT-96A)

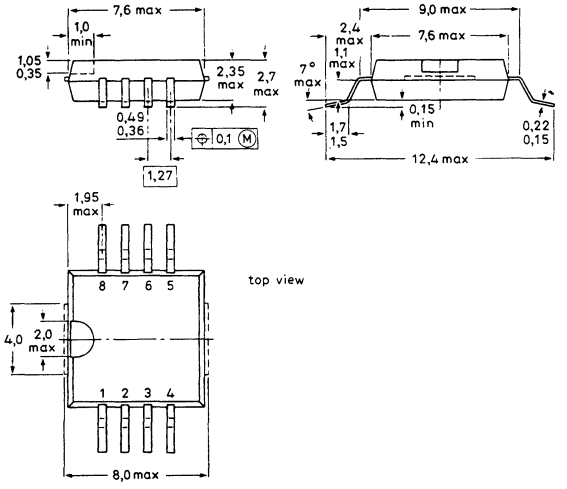


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0174 88070

PO00273S

8-PIN PLASTIC SO (VSO-8, SOT-176)



PO00980S

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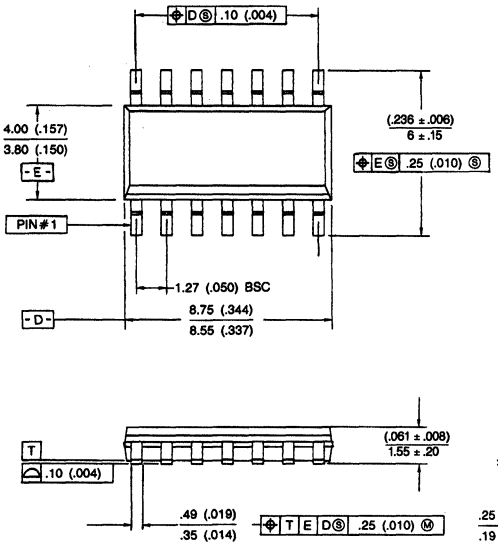
For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

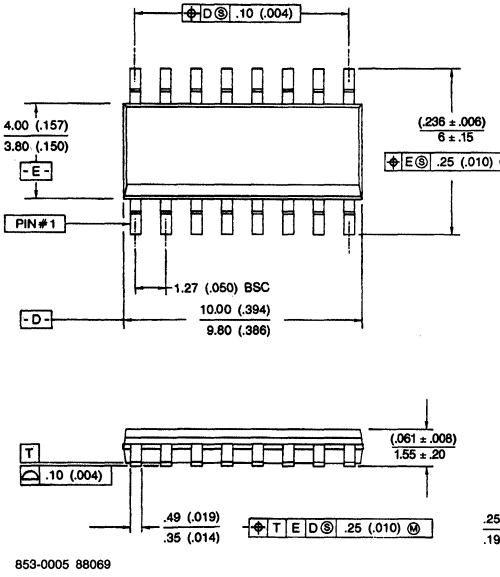
Package Outlines

14-PIN PLASTIC SO (D PACKAGE) (SO-14, SOT-108A)



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE) (SO-16, SOT-109A)

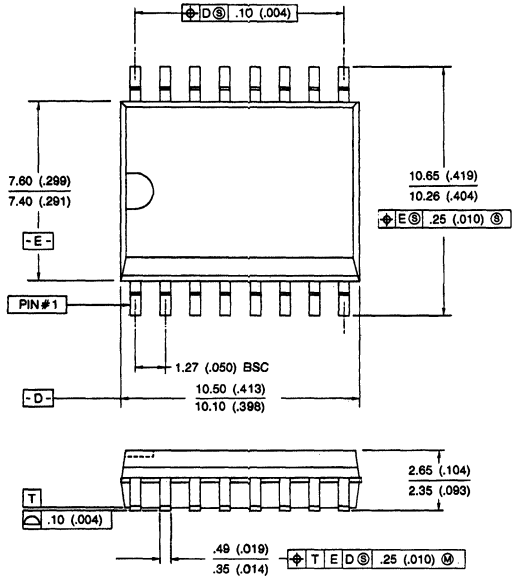


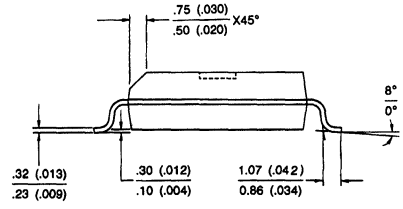
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

For Prefixes HEF, OM, MEA, PCD, PCF, PNA, SAA, SAB, SAF, TBA, TCA, TDA, TDD, TEA

Package Outlines

16-PIN PLASTIC SOL (D PACKAGE) (SOL-16, SOT-162A)



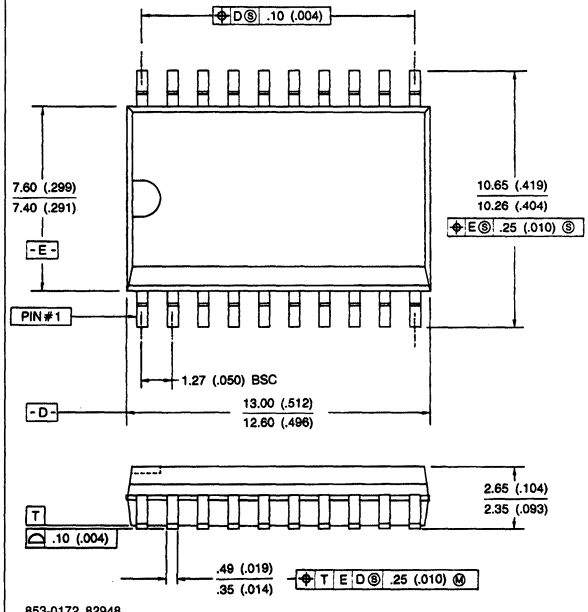


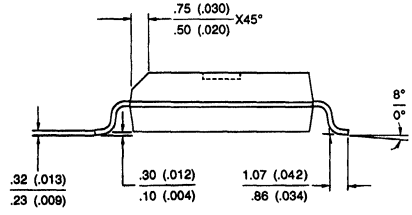
853-0171 81218

PO00241S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

20-PIN PLASTIC SOL (D PACKAGE) (SOL-20, SOT-163A)



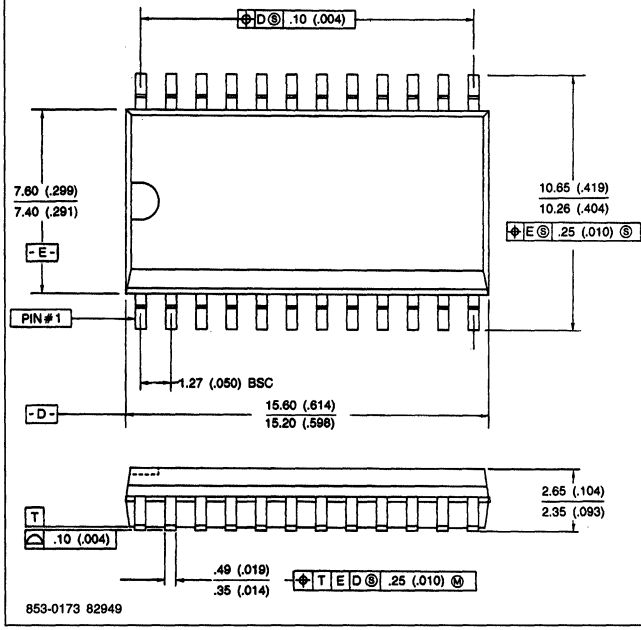


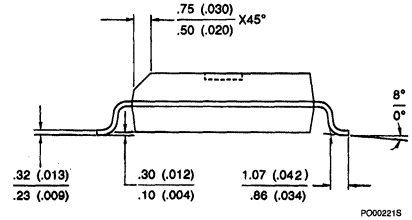
853-0172 82948

PO00231S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

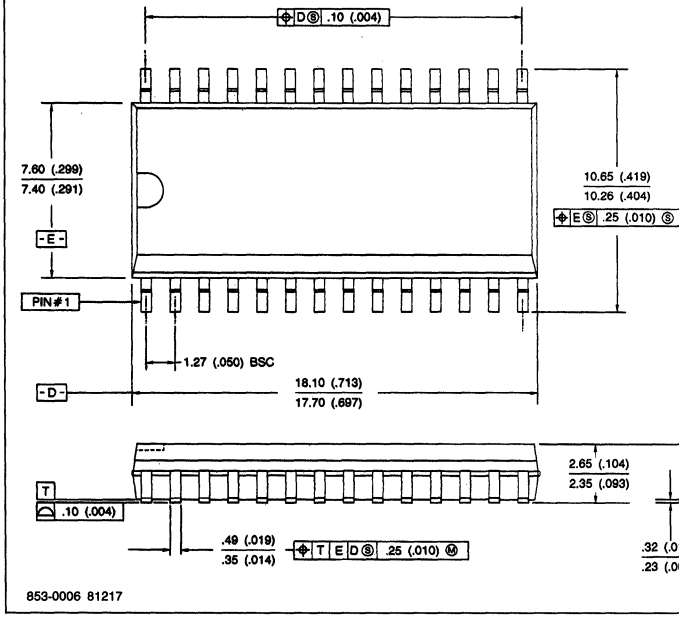
24-PIN PLASTIC SOL (D PACKAGE) (SOL-24, SOT-137A)

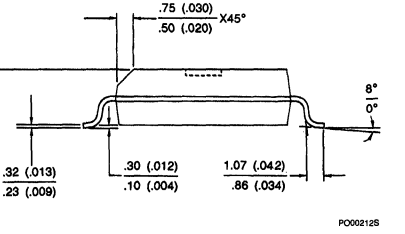




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

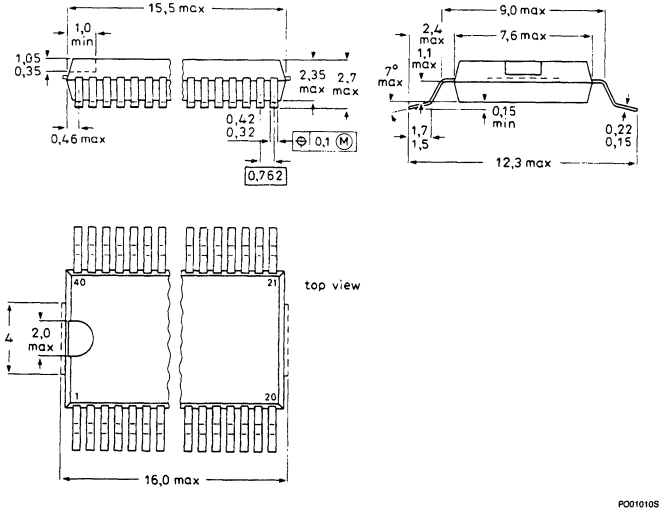
28-PIN PLASTIC SOL (D PACKAGE) (SOL-28, SOT-136A)





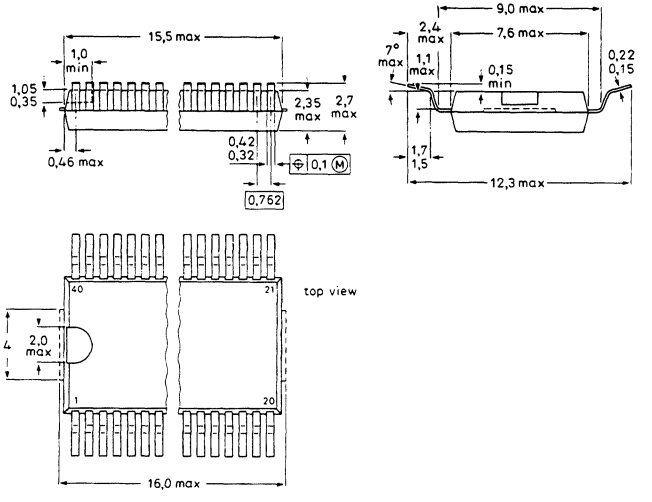
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

40-PIN PLASTIC SO (VSO-40, SOT-158A)



PO01010S

40-PIN PLASTIC SO (OPPOSITE BENT LEADS) (VSO-40, SOT-158B)



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Signetics

Linear Products

Section 16
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