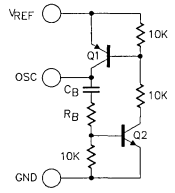
DEADBAND WITH THE SG1524 REGULATING PULSE WIDTH MODULATOR CIRCUIT

ABSTRACT

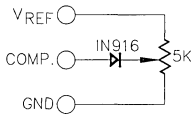
The SG1524 Regulating P.W.M. integrated circuit provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the beginning of each period to provide a deadband so that there cannot be a condition where both output transistors are on at the same time. The deadtime duration is determined by the width of the blanking pulse appearing on Pin 3, as measured at the ±0.7 volt level, and can be controlled by three techniques:

1. For the 0.3 to 1.0 microseconds, the deadband is controlled by the timing capacitor, C_T, on Pin 7. The relationship between C_T and deadband is shown in Figure 3 on the SG1524 data sheet. Of course, since C_T also determines the oscillator frequency, the range of control is somewhat limited.

2. Above 1.0 microsecond, a simple one-shot latch similar to the circuit shown below should be used.
   When this circuit is triggered by the positive-going pulse from the oscillator output, it will latch for a period determined by C_BR_B, providing a well-defined deadtime.



3. Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage of the error amplifier. A simple way of achieving this clamp is with the circuit below:



This circuit will limit the error amplifier's voltage range since its current source output will supply only 100μa. Another advantage of this circuit is that it does not change the programmedoscillator frequency.

In general, it is not recommended to stretch the deadtime by using external capacitors on Pin 3. There are several reasons for this:

a. It is difficult to obtain well-controlled, repeatable deadtimes with this approach, since the logic threshold is +0.7 volts. The normal exponential fall of the pulse trailing edge due to the external capacitor and internal 3K pull-down resistor results in a poorly-defined crossing of the logic threshold.

b. The external capacitor degrades the rise and fall times of the clock to the internal flip-flop. For sufficiently high values of capacitance, the flip-flop will cease to toggle properly, especially at higher temperatures.

In general, if a simple means of stretching deadtime is required, the best solution is to use the SG1524B device instead of the earlier 1524. Up to 1000pF can be connected to the OSC pin with no degradation of the flip-flop operation, since the clock to the toggle flip-flop in the 1524B is generated by the internal double-pulse suppression logic.