SiI0680A PCI to IDE/ATA
Data Sheet

Document # SiI-DS-0069-C

Revision History:

Version	Comment	Date
Rev. 0.1	First draft (from Engineering Design Specification)	08/07/00
Rev. 0.2	Additional register definitions added	10/09/00
Rev. 0.3	Changed package type to TQFP	10/10/00
Rev. 0.4	Changed TQFP drawing: minor changes to pinout and PLL external component values	10/13/00
Rev. 0.5	Completely re-written from technical standpoint	01/23/01
Rev. 0.5A	PRELIMINARY markings removed: submitted for review/comment	01/26/01
Rev 0.90	Major Content Changes	07/05/01
Rev. 0.91	More content changes	08/08/01
Rev. 0.92	Content corrections	08/09/01
Rev. 0.93	Made Minor corrections	08/10/01
Rev. 0.99	Corrections made in preparation of releasing Rev 1.0 version including adding references to ATA/133	
Rev. 1.0	Final corrections made, errata added	09/24/01
Rev. 1.05	Errata for chip Revision 00, marked “680 CES”, removed	11/15/01
Rev. 1.1	Changed Register defaults and Resistor Values consistent with chip Revision 01. Clarified OS support.	11/29/01
Rev. 1.2	Changed Document Number	01/09/02
Rev. 1.3	Made minor corrections and change the document name from 680 to 680A	05/16/02
Rev. A3	Updated part ordering number at section 4 package drawing	02/01/05
Rev. B	Updated Formatting	10/24/06
Rev. C	Removed confidential markings	11/29/06

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1. Overview

The Silicon Image PCI-680 is a single-chip solution for a PCI to ATA controller. It accepts host commands through the PCI bus, processes them and transfers data between the host and ATA devices. It can be used to control two independent ATA channels: primary and secondary. Each channel has its own ATA bus and will support up to two ATA/ATAPI devices for a maximum of four devices. The PCI-680 supports up to a 133 MB/sec transfer rate exceeding that which is specified in ATA/ATAPI-6.

This controller provides OEMs with an enabling solution for interfacing to storage media such as hard disk drives. For personal computer manufacturers, using the PCI-680 will differentiate them from the competition by allowing for the addition of more drives and incorporating the newest drive standards, all at a lower cost. For embedded applications, the SiI 0680A provides a high performance and cost effective interface for storage and ATAPI device support.

1.1 Key Benefits

The Silicon Image PCI-680 stand-alone Ultra ATA/133 PCI to ATA host controller is the perfect single-chip solution for designs based on chipsets without an integrated ATA host controller, or designs which need to expand the number of ATA channels to accommodate the growing number of storage peripherals with ATA interface.

The PCI-680 comes complete with drivers for Windows 98, Windows Millennium, Windows NT 4.0, Windows 2000, Windows XP and Linux. It is also fully operational and compatible with default IDE drivers from Microsoft.

Comprehensive RAID (0, 1, 0+1) software support is also provided for Windows 98, NT 4.0, Windows Me, Windows 2000 and Windows XP.

1.2 Features

1.2.1 Overall Features

- Standalone PCI to ATA host controller chip
- Compliant with PCI Specification, revision 2.2.
- Compliant with PCI IDE Controller Specification, revision 1.0.
- Compliant with Programming Interface for Bus Master IDE Controller, revision 1.0.
- Compliant with ATA/ATAPI-6 specifications.
- Compliant with UDMA6 ATA/133 Specification
- Driver support for Win98, WinME, NT4, Win2K and XP.(IDE and RAID including Linux IDE support)
- Supports up to 4Mbit external FLASH or EPROM for BIOS expansion.
- Supports an external EEPROM, FLASH or serial EPROM for programmable subsystem vendor ID and subsystem product ID.
- Supports all necessary test requirements for WHQL.
- Supports the Microsoft driver protocols for PIO and bus master DMA operations.
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- Fabricated in a 0.35µ CMOS process with a 3.3 volt core and 5 volt tolerant I/Os.
- Available in a 144-pin LQFP package.

1.2.2 PCI Features

- Supports PCI 33 MHz with 32-bit data.
- Supports PCI PERR and SERR reporting.
- Supports PCI bus master operations: Memory Read, Memory Read Multiple, and Memory Write.
- Supports PCI bus target operations: Configuration Read, Configuration Write, I/O Read, I/O Write, Memory Read, Memory Write, Memory Read Line (Memory Read), Memory Read Multiple (Memory Read), Memory Write and Invalidate (Memory Write).
- Supports byte alignment for odd-byte PCI address access.
- Supports jumper configurable PCI class code.
- Supports programmable and EEPROM, FLASH and EPROM loadable PCI class code.
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Supports IDE native mode (non-legacy) functions only.

1.2.3 ATA Features

- Supports two independent ATA channels.
- Supports ATA 133.
- Supports full speed burst transfers on the ATA bus.
- Supports software-controlled ATA bus tri-state.
- Supports device specific timing registers.
- Supports device read-ahead and write-ahead capability under Virtual DMA.

1.2.4 Other Features

- Features one 256-byte FIFO (32-bit x 64 deep) per IDE channel for host reads and writes.
- Features ATA to PCI interrupt masking.
- Features command buffering from the PCI to ATA.
- Features Virtual DMA: Bus master transfer on the PCI bus and PIO transfer on the ATA bus.
- Features Watch Dog Timer for fault resiliency.

1.3 PCI-680 Technical Description

The PCI-680A is available in a 144-pin LQFP (Thin Quad Flat Package) including more ground pins in order to accommodate the new higher data transfer rate specified in the ATA/ATAPI-6 specification. The chip has an internal phase lock loop that will provide the 100/133MHz (selectable) internal clock, allowing a data transfer rate of 100/133MB/sec (selectable) on ATA interface. A built-in 80-pin cable detector provides users the ability to determine whether a cable can support the latest Ultra ATA/100/133 (selectable) transfer rate. The PCI-680 is capable of supporting Native mode, external BIOS, Enhanced IDE mode (ultra DMA and multiword DMA mode) and PIO mode.

1.4 References

For more details about the ATA technology, the reader is referred to the following industry specifications:

- ATA/ATAPI-6 (at time of publication, ATA/ATAPI-6 has not been formally approved)
- PCI Local Bus Specification Revision 2.2
- Advanced Power Management Specification Revision 1.0
- PCI IDE Controller Specification Revision 1.0
- Programming Interface for Bus Master IDE Controller, Revision 1.0

1.5 Functional Description

PCI-680 is more than a PCI-to-ATA bridge chip that transfers data between the PCI bus and storage media (e.g hard disk drive, etc) over the ATA bus. As a host controller, it also performs functions associated with the host, such as storing configuration information, and processing data for errors. The PCI-680 can be described in the following functional blocks:

- PCI Interface. Provides the interface to any system that has a PCI bus. Instructions and system clocks are based on this interface.
- ATA Interface. Two separate channels (Primary and Secondary) to access storage media such as hard disk drives, CD-ROM's etc.
- Controller Interface. Additional hardware interface for controlling and configuring the Host Controller.

1.6 Functional Block Diagram

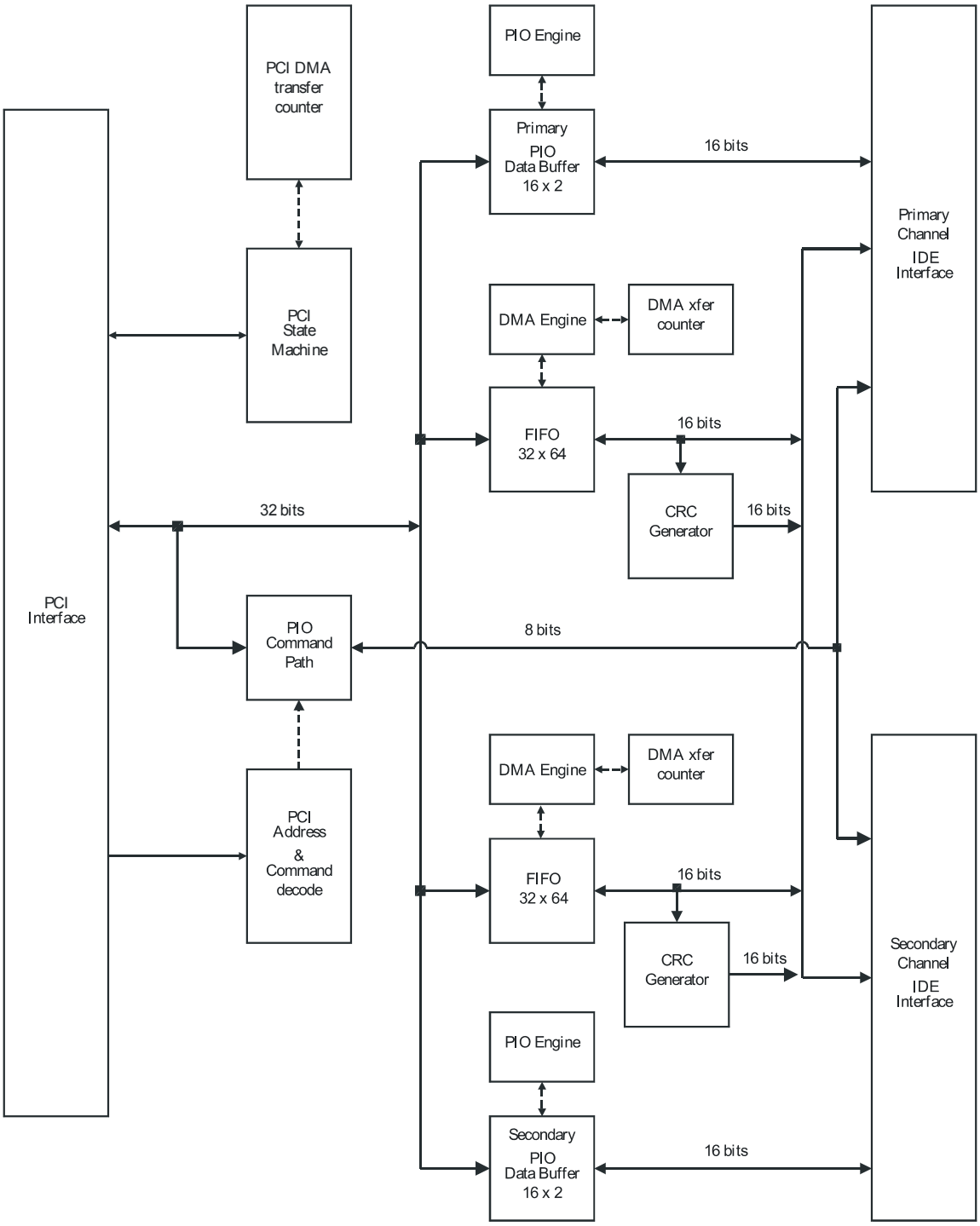


Figure 1-1: Sil 0680A Functional Block Diagram

1.7 PCI Interface

The PCI-680 PCI interface is compliant with the PCI Local Bus Specification (Revision 2.2). PCI stands for Peripheral Component Interconnect, a high-performance and robust interconnect bus that provides a processor-independent data path between the CPU and high-speed peripherals. The PCI Specification is monitored by the PCI Special Interest Group (PCI-SIG). The PCI-SIG is an unincorporated association of members of the microcomputer industry created to monitor and enhance the development of PCI architecture and is governed by PCI-SIG bylaws (HTTP://www.pcisig.com/).

The PCI-680 can act as a PCI master and a PCI slave, and contains the PCI-680 PCI configuration space and internal registers. When the PCI-680 needs to access shared memory, it becomes the bus master of the PCI bus and completes the memory cycle without external intervention. In the mode when it acts as a bridge between the PCI bus and the IDE/ATA bus it will behave as a PCI slave.

1.8 PCI Initialization

Generally, when a system initializes a module containing a PCI device, the configuration manager reads the configuration space of each PCI device on the PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If a device that is addressed (via signal lines) responds to the configuration cycle by claiming the bus, then that function's configuration space is read out from the device during the cycle. Since any PCI device can be a multifunction device, every supported function's configuration space needs to be read from the device. Based on the information read, the configuration manager will assign system resources to each supported function within the device. Sometimes new information needs to be written into the function's configuration space. This is accomplished with a configuration write cycle.

1.9 PCI Bus Operations

PCI-680 behaves either as a PCI master or a PCI slave device at any time and switches between these modes as required during device operation.

As a PCI slave, the PCI-680 responds to the following PCI bus operations:

- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Memory Read
- Memory Write

  All other PCI cycles are ignored by the PCI-680.

As a PCI master, the PCI-680 generates the following PCI bus operations:

- Memory Read Multiple
- Memory Read Line
- Memory Read
- Memory Write

1.10 PCI Configuration Space

This section describes how the PCI-680 implements the required PCI configuration register space. The intent is to provide an appropriate set of configuration registers that satisfy the needs of current and anticipated system configuration mechanisms, without specifying those mechanisms or otherwise placing constraints on their use. These registers allow for:

- Full device relocation (including interrupt binding)
- Installation, configuration, and booting without user interventions
- System address map construction by device-independent software

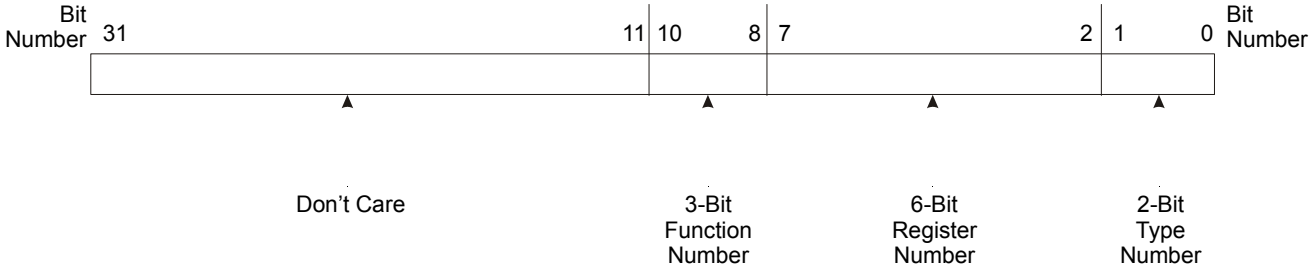


Figure 1-2: Address Lines During Configuration Cycle

PCI-680 only responds to Type 0 configuration cycles. Type 1 cycles, which pass a configuration request on to another PCI bus, are ignored.

The address phase during a PCI-680 configuration cycle indicates the function number and register number being addressed which can be decoded by observing the status of the address lines AD[31:0].

The value of the signal lines AD[7:2] during the address phase of configuration cycles selects the register of the configuration space to access. Valid values are between 0 and 15, inclusive. Accessing registers outside this range results in an all-0s value being returned on reads, and no action being taken on writes.

The Class Code register contains the Class Code, Sub-Class Code, and Register-Level Programming Interface registers.

All writable bits in the configuration space are reset to 0 by the hardware reset, PCI RESET (RST#) asserted. After reset, PCI-680 is disabled and will only respond to PCI configuration write and PCI configuration read cycles.

1.11 Deviations from the Specification

The PCI-680 product has been developed and tested to the specification listed in this document. As a result of testing and customer feedback, we may become aware of deviations to the specification that could affect the component's operation. To ensure awareness of these deviations by anyone considering the use of the PCI-680, we will include them in this document.

2. Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for temperature range, 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDD_H	Supply Voltage	3.6	V
V_{IN}	Input Voltage	-0.3 ~ 6.0	V
I_{OUT}	DC Output Current	16	mA
T_{STG}	Storage Temperature	-65 ~ 150	°C

Table 2-1: Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDD	Supply Voltage	-	-	3.0	3.3	3.6	V
IDD	Supply Current (See Sec. 2.5)	Quiescent	-	-	250	-	mA
		Operating	-	-	350	-	
V_{IH}	Input High Voltage	-	3.3V PCI	0.5xVDD	-	-	V
		-	Non-PCI	2.0	-	-	
V_{IL}	Input Low Voltage	-	3.3V PCI	-	-	0.3xVDD	V
		-	Non-PCI	-	-	0.8	
V+	Input High Voltage	-	Schmitt	-	1.8	2.3	V
V-	Input Low Voltage	-	Schmitt	0.5	0.9	-	V
V_H	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I_{IH}	Input High Current	V_{IN} = VDD	-	-10	-	10	µA
I_{IL}	Input Low Current	V_{IN} = VSS	-	-10	-	10	µA
V_{OH}	Output High Voltage	-	-	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	-	-	0.4	V
I_{OZ}	3-State Leakage Current	-	-	-10	-	10	µA

Table 2-2: DC Specifications

2.2 PCI 33 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	11.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	11.0	ns
T_{ON}	Float to Active Delay	2.0	-	ns
T_{OFF}	Active to Float Delay	-	28.0	ns
T_{SU}	Input Setup Time – Bussed Signals	7.0	-	ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	10.0	-	ns
T_H	Input Hold Time	0.0	-	ns

Table 2-3: PCI 33 MHz Timing Specifications

2.3 ATA/ATAPI-6 Slew Rate Specifications

Symbol	Parameter	Condition	Limits		Unit
			Min	Max	
S_{RISE}	Output Slew Rate – Rising	Refer to ATA Specification for specific test condition requirements	0.4	1	V/ns
S_{FALL}	Output Slew Rate – Falling	Refer to ATA Specification for specific test condition requirements	0.4	1	V/ns

Table 2-4: ATA /ATAPI-6 Slew Rate Specifications

2.4 ATA/ATAPI-6 AC/DC Specifications

Symbol	Parameter	Condition	Limits		Unit
			Min	Max	
I_{OL}	Output Sink Current	-	4	-	mA
I_{OH}	Output Source Current	-	400	-	µA
V+	Low-to-High Input Threshold	-	1.5	2.0	V
V-	High-to-Low Input Threshold	-	1.0	1.5	V
V_{OH}	Output Voltage High	-6 mA < I_{OUT} < 3 mA	VDD - 0.51	VDD+ 0.3	V
V_{OL}	Output Voltage Low	I_{OUT} = 6 mA	-	0.51	V

Table 2-5: ATA/ATAPI-6 DC Specifications

2.5 Power Supply Bypass Considerations

It is recommended that a 4-layer board (minimum) with internal Power and Ground Planes be used when i integrating the SiI 0680A . Good high-speed layout techniques should be used and proper power supply bypassing is essential. Both bulk and local (high frequency) bypass capacitors should be used.

Bulk bypassing is intended to reduce the voltage noise (droop) induced by changes in load current and the inductance in the power distribution system (wires and/or etch). Since the currents vary greatly from no activity to worst case data patterns, a significant amount of capacitance is required.

All bypass capacitors should be connected to the power and ground plane with a low inductance connection (short, wide traces connecting component pad to plane).

The bulk bypass capacitor(s) should have good high frequency characteristics. A capacitor with low ESR (Equivalent Series Resistance) should be used. It should be located close to the source of +3.3V (output pin of regulator or connector pin for off board regulators). The following minimum values are recommended:

Low ESR Tantalum – 100uF
Low ESR Aluminum Electrolytic – 600uF

Local high frequency 0bypass should also be implemented. Capacitors should be located on all four sides of the chip close to the VDD/VSS pins. Three caps per side are recommended (12 total). Additional capacitors (x6) should be distributed evenly around the board area.

The following capacitor is recommended for local bypass:

Ceramic X7R Dielectric - 0.01uF

For a slight improvement in high frequency impedance of the bypass capacitors, two capacitors in parallel can be used for Local Bypass. The paired caps must be located as close as possible to each other. The following values are recommended for the capacitor pairs:

Ceramic X7R Dielectric - 0.1uF
Ceramic X7R Dielectric – 1000pF

3. Pin Definition

3.1 PCI-680 Pin Listing

This section describes the pin-out of the SiI 0680A PCI-to-ATA host controller ASIC.

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
1	VSS	GND	-	-	Ground
2	PLL_VDD	PWR	-	-	PLL 3.3 Volt Power
3	PLL_CPBIAS	Analog	-	-	PLL Charge Pump Bias
4	PLL_VCOBIAS	Analog	-	-	PLL VCO Bias
5	PLL_LOOPFLT	Analog	-	-	PLL Loop Filter
6	PLL_GND	GND	-	-	PLL Ground
7	TEST_MODE	I	-	PD – 20k	ASIC Test Mode Enable
8	IDE0_DD00	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 0 / FLASH memory address bit 18
9	IDE0_DD01	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 1 / FLASH memory address bit 17
10	IDE0_DD02	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 2 / FLASH memory address bit 16
11	IDE0_DD03	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 3 / FLASH memory address bit 15
12	IDE0_DD04	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 4 / FLASH memory address bit 14
13	IDE0_DD05	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 5 / FLASH memory address bit 13
14	IDE0_DD06	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 6 / FLASH memory address bit 12
15	IDE0_DD07	I/O	ATA Buffer	PD – 100k	IDE #0 Data Bus bit 7 / FLASH memory address bit 11
16	VDD	PWR	-	-	3.3 Volt Power
17	VSS	GND	-	-	Ground
18	IDE0_DD08	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 8 / FLASH memory address bit 10
19	IDE0_DD09	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 9 / FLASH memory address bit 9

Table 3-1: SiI 0680A Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
20	IDE0_DD10	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 10 / FLASH memory address bit 8
21	IDE0_DD11	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 11 / FLASH memory address bit 7
22	IDE0_DD12	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 12 / FLASH memory address bit 6
23	IDE0_DD13	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 13 / FLASH memory address bit 5
24	IDE0_DD14	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 14 / FLASH memory address bit 4
25	IDE0_DD15	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 15 / FLASH memory address bit 3
26	VDD	PWR	-	-	3.3 Volt Power
27	VSS	GND	-	-	Ground
28	IDE0_CS0_N	I/O	12 mA	-	IDE #0 Chip Select / FLASH memory read strobe
29	IDE0_CS1_N	I/O	12 mA	-	IDE #0 Chip Select / FLASH memory write strobe
30	IDE0_DA0	I/O	12 mA	-	IDE #0 Device Address / FLASH memory address bit 2
31	IDE0_DA1	I/O	12 mA	-	IDE #0 Device Address / FLASH memory address bit 1
32	IDE0_DA2	I/O	12 mA	-	IDE #0 Device Address / FLASH memory address bit 0
33	IDE0_DIOR_N	I/O	ATA Buffer	-	IDE #0 Device I/O Read
34	IDE0_DIOW_N	I/O	ATA Buffer	-	IDE #0 Device I/O Write
35	IDE0_DMACK_N	I/O	ATA Buffer	-	IDE #0 DMA Acknowledge
36	VDD	PWR	-	-	3.3 Volt Power
37	VSS	GND	-	-	Ground
38	IDE0_CBLID_N	I-Schmitt	-	PU – 100k	IDE #0 Cable ID
39	IDE0_INTRQ	I-Schmitt	-	PD – 100k	IDE #0 Interrupt Request
40	IDE0_IORDY	I-Schmitt	-	PU – 100k	IDE #0 I/O Ready
41	IDE0_AT_REXT	Analog	-	-	IDE #0 External Bias Circuit
42	IDE0_DMARQ	I-Schmitt	-	PD – 100k	IDE #0 DMA Request
43	IDE0_RST_N	I/O	12 mA	-	IDE #0 Reset

Table 3-1: SiI 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
44	IDE1_DD00	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 0 / FLASH memory data bit 0
45	IDE1_DD01	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 1 / FLASH memory data bit 1
46	IDE1_DD02	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 2 / FLASH memory data bit 2
47	IDE1_DD03	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 3 / FLASH memory data bit 3
48	IDE1_DD04	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 4 / FLASH memory data bit 4
49	IDE1_DD05	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 5 / FLASH memory data bit 5
50	IDE1_DD06	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 6 / FLASH memory data bit 6
51	VDD	PWR	-	-	3.3 Volt Power
52	VSS	GND	-	-	Ground
53	IDE1_DD07	I/O	ATA Buffer	PD – 100k	IDE #0 Data Bus bit 7 / FLASH memory data bit 7
54	IDE1_DD08	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
55	IDE1_DD09	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
56	IDE1_DD10	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
57	IDE1_DD11	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
58	IDE1_DD12	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
59	IDE1_DD13	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
60	IDE1_DD14	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
61	VDD	PWR		-	3.3 Volt Power
62	VSS	GND	-	-	Ground
63	IDE1_DD15	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
64	IDE1_CS0_N	I/O	12 mA	-	IDE #1 Chip Select / EEPROM SCLK
65	IDE1_CS1_N	I/O	12 mA	-	IDE #1 Chip Select / EEPROM SDAT
66	IDE1_DA0	I/O	12 mA	-	IDE #1 Device Address
67	IDE1_DA1	I/O	12 mA	-	IDE #1 Device Address
68	IDE1_DA2	I/O	12 mA	-	IDE #1 Device Address

Table 3-1: Sil 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
69	IDE1_DIOR_N	I/O	ATA Buffer	-	IDE #1 Device I/O Read
70	IDE1_DIOW_N	I/O	ATA Buffer	-	IDE #1 Device I/O Write
71	IDE1_CBLID_N	I-Schmitt	-	PU – 100k	IDE #1 Cable ID
72	VDD	PWR	-	-	3.3 Volt Power
73	VSS	GND	-	-	Ground
74	IDE1_DMACK_N	I/O	ATA Buffer	-	IDE #1 DMA Acknowledge
75	IDE1_INTRQ	I-Schmitt	-	PD – 100k	IDE #1 Interrupt Request
76	IDE1_IORDY	I-Schmitt	-	PU – 100k	IDE #1 I/O Ready
77	IDE1_AT_REXT	Analog	-	-	IDE #1 External Bias Circuit
78	IDE1_DMARQ	I-Schmitt	-	PD – 100k	IDE #1 DMA Request
79	IDE1_RST_N	I/O	12 mA	-	IDE #1 Reset
80	JP	I	-	PU – 20k	IDE Configuration Jumper
81	PCI_AD31	I/O	PCI	-	PCI Address/Data
82	PCI_AD30	I/O	PCI	-	PCI Address/Data
83	PCI_AD29	I/O	PCI	-	PCI Address/Data
84	PCI_AD28	I/O	PCI	-	PCI Address/Data
85	PCI_AD27	I/O	PCI	-	PCI Address/Data
86	PCI_AD26	I/O	PCI	-	PCI Address/Data
87	VDD	PWR	-	-	3.3 Volt Power
88	VSS	GND	-	-	Ground
89	PCI_AD25	I/O	PCI	-	PCI Address/Data
90	PCI_AD24	I/O	PCI	-	PCI Address/Data
91	PCI_CBE3	I/O	PCI	-	PCI Command/Byte Enable
92	PCI_IDSEL	I	-	-	PCI ID Select
93	PCI_AD23	I/O	PCI	-	PCI Address/Data
94	PCI_AD22	I/O	PCI	-	PCI Address/Data
95	PCI_AD21	I/O	PCI	-	PCI Address/Data
96	PCI_AD20	I/O	PCI	-	PCI Address/Data
97	PCI_AD19	I/O	PCI	-	PCI Address/Data
98	VDD	PWR	-	-	3.3 Volt Power
99	VSS	GND	-	-	Ground

Table 3-1: SiI 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
100	PCI_AD18	I/O	PCI	-	PCI Address/Data
101	PCI_AD17	I/O	PCI	-	PCI Address/Data
102	PCI_AD16	I/O	PCI	-	PCI Address/Data
103	PCI_CBE2	I/O	PCI	-	PCI Command/Byte Enable
104	PCI_FRAME_N	I/O	PCI	-	PCI Frame
105	PCI_IRDY_N	I/O	PCI	-	PCI Initiator Ready
106	PCI_TRDY_N	I/O	PCI	-	PCI Target Ready
107	PCI_DEVSEL_N	I/O	PCI	-	PCI Device Select
108	VDD	PWR	-	-	3.3 Volt Power
109	VSS	GND	-	-	Ground
110	PCI_STOP_N	I/O	PCI	-	PCI Stop
111	PCI_PERR_N	I/O	PCI	-	PCI Parity Error
112	PCI_SERR_N	OD	PCI	-	PCI System Error
113	PCI_PAR	I/O	PCI	-	PCI Parity
114	PCI_CBE1	I/O	PCI	-	PCI Command/Byte Enable
115	PCI_AD15	I/O	PCI	-	PCI Address/Data
116	PCI_AD14	I/O	PCI	-	PCI Address/Data
117	PCI_AD13	I/O	PCI	-	PCI Address/Data
118	VDD	PWR	-	-	3.3 Volt Power
119	VSS	GND	-	-	Ground
120	PCI_AD12	I/O	PCI	-	PCI Address/Data
121	PCI_AD11	I/O	PCI	-	PCI Address/Data
122	PCI_AD10	I/O	PCI	-	PCI Address/Data
123	PCI_AD09	I/O	PCI	-	PCI Address/Data
124	PCI_AD08	I/O	PCI	-	PCI Address/Data
125	PCI_CBE0	I/O	PCI	-	PCI Command/Byte Enable
126	PCI_AD07	I/O	PCI	-	PCI Address/Data
127	PCI_AD06	I/O	PCI	-	PCI Address/Data
128	VDD	PWR	-	-	3.3 Volt Power
129	VSS	GND	-	-	Ground
130	PCI_AD05	I/O	PCI	-	PCI Command/Byte Enable

Table 3-1: Sil 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
131	PCI_AD04	I/O	PCI	-	PCI Command/Byte Enable
132	PCI_AD03	I/O	PCI	-	PCI Command/Byte Enable
133	PCI_AD02	I/O	PCI	-	PCI Command/Byte Enable
133	PCI_AD02	I/O	PCI	-	PCI Command/Byte Enable
134	PCI_AD01	I/O	PCI	-	PCI Command/Byte Enable
135	PCI_AD00	I/O	PCI	-	PCI Command/Byte Enable
136	PCI_REQ_N	T	PCI	-	PCI Bus Request
137	PCI_GNT_N	I	-	-	PCI Bus Grant
138	PCI_INTA_N	OD	PCI	-	PCI Interrupt
139	BA5_EN	I	-	-	Base Address 5 Enable Jumper
140	PCI_CLK	I	-	-	PCI Clock
141	PCI_RST_N	I-Schmitt	-	-	PCI Reset
142	SCAN_EN	I	-	PD – 20k	Internal Scan Enable
143	MEM_CS_N	I/O	4 mA	-	Memory Chip Select
144	VDD	PWR	-	-	3.3 Volt Power

Table 3-1: Sil 0680A Pin Listing (continued)

Pin Type	Pin Description
I	**Input Pin with LVTTL Thresholds**
I-Schmitt	**Input Pin with Schmitt Trigger**
O	**Output Pin**
T	**Tri-state Output Pin**
I/O	**Bidirect Pin**
OD	**Open Drain Output Pin**

3.2 PCI-680 Pin Diagram

The PCI-680 pin diagram is shown in Figure 3-1.

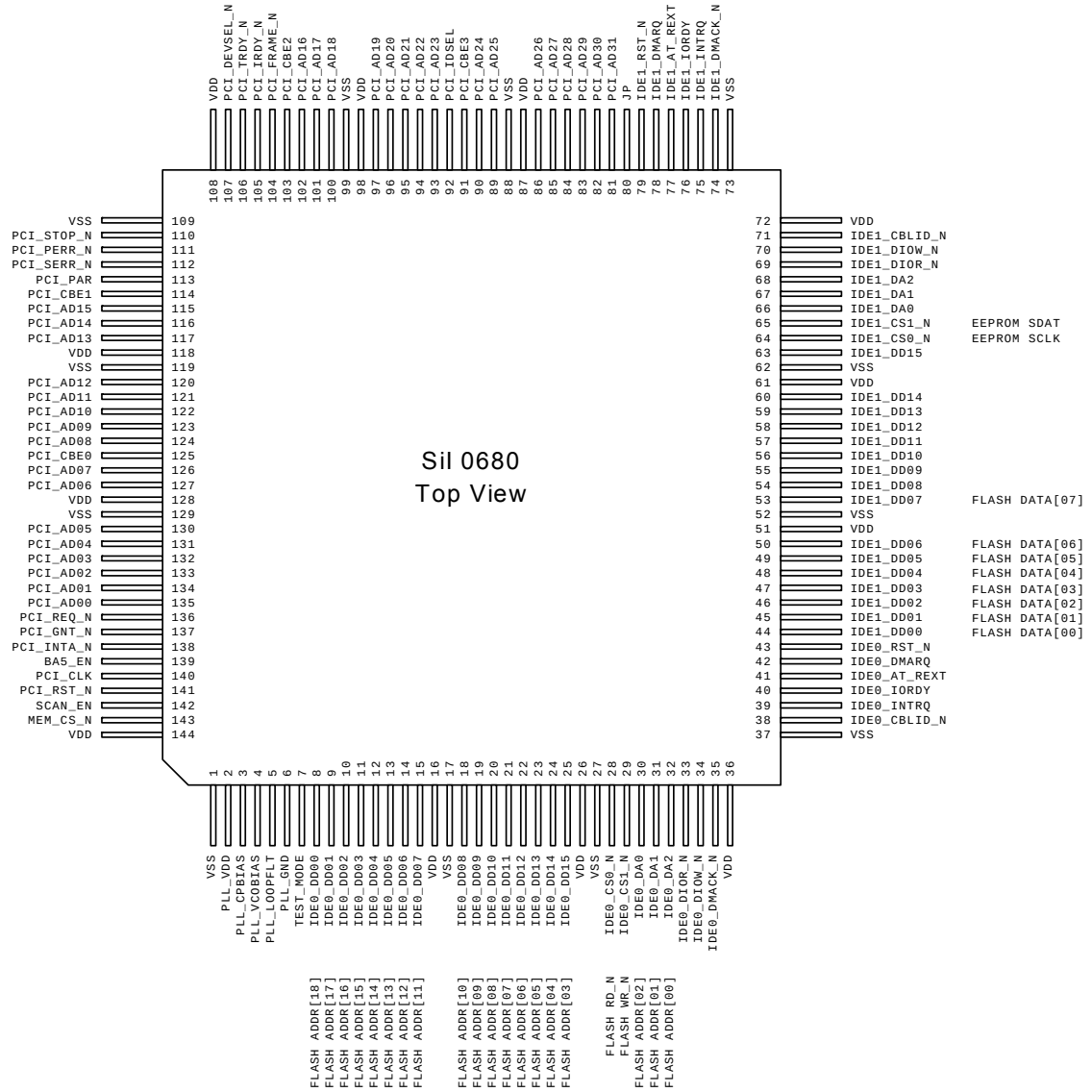


Figure 3-1: PCI-680 Pin Diagram

3.3 PCI-680 Pin Descriptions

3.3.1 IDE/ATA Primary Channel

IDE0 Disk Data Bus

Pin Names: IDE0_DD[15..0]
Pin Numbers: 25, 24, 23, 22, 21, 20, 19, 18, 15, 14, 13, 12, 11, 10, 9, 8
Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which connects to the ATA device(s). IDE0_DD[15:0] are data signals to the primary Channel. IDE0_DD[7:0] defines the low byte while IDE0_DD[15:8] defines the high byte of this 16-bit data register. The data bus is normally in a high impedance state and is driven by the SiI 0680A during the IDE0_DIOW_N command pulse in either single/multi-word DMA mode, or valid at every edge of IDE0_DIOR_N (HSTROBE) or IDE0_IORDY (DSTROBE) in Ultra DMA mode. IDE0_DD[7] is a multifunction pin which allows a host to recognize the absence of an ATA/ATAPI device at power-up. It is recommended that a 10kΩ pull-down resistor be connected to this pin.

IDE0 Chip Select

Pin Names: IDE0_CS0_N; IDE0_CS1_N
Pin Numbers: 28, 29
These are the chip select signals from the host used to select the Command Block or Control Block registers. When IDE0_DMACK_N is asserted, IDE0_CS0_N and IDE0_CS1_N shall be negated and transfers shall be 16 bits wide.

IDE0 Disk Address

Pin Names: IDE0_DA[2..0]
Pin Numbers: 32, 31, 30
Disk Address bits 0 through 2 are normally outputs to the ATA connector selecting the register in the drive's Command Block register. IDE0_DA[2:0] sends address signals to the primary channel. These address signals are decoded from the PCI_AD[2:0] and PCI_CBE[3:0] inputs.

IDE0 Disk I/O Read

Pin Name: IDE0_DIOR_N
Pin Number: 33
Primary Channel Disk I/O Read is an active low output which enables data to be read from the drive. The duration and repetition rate of IDE0_DIOR_N cycles is determined by SiI 0680A programming. IDE0_DIOR_N to the primary channel is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the primary channel drive. This signal is also defined as primary channel HDMARDY_N in Ultra DMA read mode.

IDE0 Disk I/O Write

Pin Name: IDE0_DIOW_N
Pin Number: 34
Primary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition of IDE0_DIOW_N cycles is determined by SiI 0680A Programming. IDE0_DIOW_N to the primary channel is driven high when inactive. This signal is defined as primary channel STOP in ultra DMA mode.

IDE0 DMA Acknowledge

Pin Name: IDE0_DMACK_N
Pin Number: 35
This signal is normally used by the SiI 0680A in response to IDE0_DMARQ to either acknowledge that the primary channel is ready to accept data, or that data is available. This signal is also used to write CRC code to the primary channel drive at the end of each Ultra DMA burst transfer.

IDE0 Cable Detect

Pin Names: IDE0_CBLID_N
Pin Numbers: 38
IDE0_CBLID_N (Cable Detect) determines the type of cable attached to the primary channel. In general, a low on this pin indicates that an 80 conductor cable is attached. A high indicates that a 40 conductor cable is attached. Refer to the ATA/ATAPI-6 Specification for complete details.

IDE0 Interrupt Request

Pin Name: IDE0_INTRQ
Pin Number: 39
Primary channel interrupt request is an input signal used to generate the PCI_INTA_N output. This input should have a 10kΩ pull-down resistor connected to it.

IDE0 I/O Ready

Pin Name: IDE0_IORDY
Pin Number: 40
The Primary channel drive I/O ready is an active high input. It indicates that the IDE/ATA disk drive has completed the current command cycle. A 4.7kΩ pull-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the currently selected drive to the primary channel. This signal is also defined as DDMARDY_N in Ultra DMA write mode.

IDE0 External Bias Circuit

Pin Name: IDE0_AT_REXT
Pin Number: 41
IDE0_AT_REXT is an analog pin for connection to an external bias circuit. Connect (in parallel) an 1.74KΩ, 1% resistor and an 820 pF, 5% capacitor between this pin and ground. This pin is sensitive to noise and must be routed carefully. Keep the trace length on this pin as short as possible and away from any sources of noise.

IDE0 DMA Request

Pin Name: IDE0_DMARQ
Pin Number: 42
This signal is used in a handshake manner with IDE0_DMACK_N, and shall be asserted high by the currently selected drive attached to the primary IDE/ATA Channel when it is ready to transfer data to or from the host. This pin should have a 5.6 KΩ pull-down resistor connected to it.

IDE0 Disk Reset

Pin Name: IDE0_RST_N
Pin Number: 43
IDE0 Disk Reset is an active low output which signals the IDE/ATA drive to initialize its control register. IDE0_RST_N is a buffered version of the PCI_RST_N input. It can also be generated by programming the SiI 0680A register and connects directly to the ATA connector. IDE0_RST_N asserts reset to the primary IDE/ATA channel.

3.3.2 IDE/ATA Secondary Channel

IDE1 Disk Data Bus

Pin Names: IDE1_DD[15..0]
Pin Numbers: 63, 60, 59, 58, 57, 56, 55, 54, 53, 50, 49, 48, 47, 46, 45, 44
Disk Data bits 0 through 15 are the 16-bit bi-directional data bus, which connects to the IDE/ATA device(s). IDE1_DD[15:0] are data signals to the secondary channel. IDE1_DD[7:0] defines the low data byte while IDE1_DD[15:8] defines the high data byte of this 16-bits data register. The data bus is normally in a high impedance state and is driven by the SiI 0680A during the IDE1_DIOW_N command pulse in either single/multi-word DMA mode, or valid at every edge of IDE1_DIOR_N (HSTROBE) or IDE1_IORDY (DSTROBE) in Ultra DMA mode. IDE1_DD07 is a multifunction pin, which allows a host to recognize the

absence of an ATA/ATAPI device at power-up. It is recommended that a 10kΩ pull-down resistor is recommended to be connected to this pin.

IDE1 Chip Select

Pin Names: IDE1_CS0_N; IDE1_CS1_N
Pin Numbers: 64, 65
These are the chip select signals from the host used to select the Command Block or Control Block registers. When IDE1_DMACK_N is asserted, IDE1_CS0_N and IDE1_CS1_N shall be negated and transfers shall be 16 bits wide.

IDE1 Disk Address

Pin Names: IDE1_DA[2..0]
Pin Numbers: 68, 67, 66
Disk Address bits 0 through 2 are normally outputs to the ATA connector to select the register in the drive's Command Block register. IDE1_DA [2:0] sends address signals to the secondary channel. These address signals are decoded from the PCI_AD[2:0] and PCI_CBE[3:0] inputs.

IDE1 Disk I/O Read

Pin Name: IDE1_DIOR_N
Pin Number: 69
This is an active low output which enables data to be read from the drive. The duration and repetition rate of IDE1_DIOR_N cycles is determined by programming the SiI 0680A PIO timing registers. IDE1_DIOR_N to the secondary channel is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the secondary channel drive. This signal is also defined as secondary channel HDMARDY_N in Ultra DMA read mode.

IDE1 Disk I/O Write

Pin Name: IDE1_DIOW_N
Pin Number: 70
This is an active low output that enables data to be written to the drive. The duration and repetition rate of IDE1_DIOW_N cycles is determined by programming the SiI 0680A PIO timing registers. IDE1_DIOW_N to the Secondary channel is driven high when inactive. This signal is also defined as secondary channel STOP in Ultra DMA mode.

IDE1 Cable Detect

Pin Names: IDE1_CBLID_N
Pin Number: 71
IDE1_CBLID_N (Cable Detect) determines the type of cable attached to the primary channel. In general, a low on this pin indicates that a 40 conductor cable is attached. A high indicates that an 80 conductor cable is attached. Refer to the ATA/ATAPI-6 Specification for complete details.

IDE1 DMA Acknowledge

Pin Name: IDE1_DMACK_N
Pin Number: 74
This signal is normally used by the SiI 0680A in response to IDE1_DMARQ to either acknowledge that the secondary channel is ready to accept data, or that data is available. This signal is also used to write CRC code to the secondary channel drive at the end of each Ultra DMA burst transfer.

IDE1 Interrupt Request

Pin Name: IDE1_INTRQ
Pin Number: 75
Primary channel interrupt request is an input signal used to generate the PCI_INTA_N output. This input should have a 10kΩ pull-down resistor connected to it.

IDE1 I/O Ready

Pin Name: IDE1_IORDY
Pin Number: 76
The Secondary Channel Drive Channel's Initiator Ready is an active high input. It indicates that the ATA disk drive has completed the current command cycle. A 4.7KΩ pull-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the currently selected drive attached to the secondary channel. This signal is also defined as DDMARDY_N in Ultra DMA write mode.

IDE1 External Bias Circuit

Pin Name: IDE1_AT_REXT
Pin Number: 77
IDE1_AT_REXT is an analog pin for connection to an external bias circuit. Connect (in parallel) an1.74K, 1% resistor and an 820 pF, 5% capacitor between this pin and ground. This pin is sensitive to noise and must be routed carefully. Keep the trace length on this pin as short as possible and away from any sources of noise.

IDE1 DMA Request

Pin Name: IDE1_DMARQ
Pin Number: 78
This signal is used in a handshake manner with IDE1_DMACK_N and shall be asserted high by the currently selected drive attached to the secondary IDE/ATA channel when it is ready to transfer data to or from the host. . This pin should have a 5.6 KΩ pull-down resistor connected to it.

IDE1 Disk Reset

Pin Name: IDE1_RST_N
Pin Number: 79
Disk Reset is an active low output which signals the IDE/ATA drive to initialize its control register. IDE1_RST_N is a buffered version of the PCI_RST_N input. It can also be generated by programming the SiI 0680A register, and connects directly to the ATA connector. IDE1_RST_N asserts reset to the secondary ATA channel.

3.3.3 PCI 33MHz 32-bit Section

PCI Address and Data

Pin Names: PCI_AD[31..0]
Pin Numbers: 81~86, 89, 90, 93~97, 100~102, 115~117, 120~124, 126, 127, 130~135
Address and Data buses are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the first clock cycle in which PCI_FRAME_N signal is asserted. During the address phase, PCI_AD[31:0] contain a physical address (32 bits). For I/O, this can be a byte address. For configuration and memory it is a DWORD address. During data phases, PCI_AD[7:0] contain the least significant byte (LSB) and PCI_AD[31:24] contain the most significant byte (MSB). Write data is stable and valid when PCI_IRDY_N is asserted; read data is stable and valid when PCI_TRDY_N is asserted. Data is transferred during those clocks where both PCI_IRDY_N and PCI_TRDY_N are asserted.

PCI Command and Byte Enables

Pin Names: PCI_CBE[3..0]
Pin Numbers: 91, 103, 114, 125
Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCI_CBE[3:0]_N define the bus command. During the data phase, PCI_CBE[3:0]_N are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.

PCI ID Select

Pin Name: PCI_IDSEL
Pin Number: 92
This signal is used as a chip select during configuration read and write transactions.

PCI Frame Cycle

Pin Name: PCI_FRAME_N
Pin Number: 104
Cycle Frame is driven by the current master to indicate the beginning and duration of an access. PCI_FRAME_N is asserted to indicate that a bus transaction is beginning. While PCI_FRAME_N is asserted, data transfers continue. When PCI_FRAME_N is de-asserted, the transaction is in the final data phase or has completed.

PCI Initiator Ready

Pin Name: PCI_IRDY_N
Pin Number: 105
Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with PCI_TRDY_N. A data phase is completed on any clock when both PCI_IRDY_N and PCI_TRDY_N are sampled as asserted. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together.

PCI Target Ready

Pin Name: PCI_TRDY_N
Pin Number: 106
Target Ready indicates the target agent's ability to complete the current data phase of the transaction. PCI_TRDY_N is used with PCI_IRDY_N. A data phase is completed on any clock when both PCI_TRDY_N and PCI_IRDY_N are sampled asserted. During a read, PCI_TRDY_N indicates that valid data is present on PCI_AD[31:0]. During a write, it indicates the target is prepared to accept data.

PCI Device Select

Pin Name: PCI_DEVSEL_N
Pin Number: 107
Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, PCI_DEVSEL_N indicates to a master whether any device on the bus has been selected.

PCI Stop

Pin Name: PCI_STOP_N
Pin Number: 110
PCI_STOP_N indicates the current target is requesting that the master stop the current transaction.

PCI Parity Error

Pin Name: PCI_PERR_N
Pin Number: 111
PCI_PERR_N indicates a data parity error between the current master and target on PCI. On a write transaction, the target always signals data parity errors back to the master on PCI_PERR_N. On a read transaction, the master asserts PCI_PERR_N to indicate to the system that an error was detected.

PCI System Error

Pin Name: PCI_SERR_N
Pin Number: 112
System Error is for reporting address parity errors, data parity errors on Special Cycle Command, or any other system error where the result will be catastrophic. The PCI_SERR_N is a pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of PCI_SERR_N is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI_SERR_N to the de-asserted state is accomplished by a weak pull-up. Note that if an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

PCI Parity

Pin Name: PCI_PAR

Pin Number: 113
PCI_PAR is even parity across PCI_AD[31:0] and PCI_CBE[3:0]_N. Parity generation is required by all PCI agents. PCI_PAR is stable and valid one clock after the address phase. For data phases PCI_PAR is stable and valid one clock after either PCI_IRDY_N is asserted on a write transaction or PCI_TRDY_N is asserted on a read transaction. Once PCI_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI_PAR has the same timing as PCI_AD[31:0] but delayed by one clock.)

PCI Request

Pin Name: PCI_REQ_N
Pin Number: 136
This signal indicates to the arbiter that this agent desires use of the PCI bus.

PCI Grant

Pin Name: PCI_GNT_N
Pin Number: 137
This signal indicates to the agent that access to the PCI bus has been granted. In response to a PCI request, this is a point-to-point signal. Every master has its own PCI_GNT_N, which must be ignored while PCI_RST_N is asserted.

PCI Interrupt A

Pin Name: PCI_INTA_N
Pin Number: 138
Interrupt A is used to request an interrupt on the PCI bus. PCI_INTA_N is open collector and is an open drain output.

PCI Clock Signal

Pin Names: PCI_CLK
Pin Number: 140
Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals (except PCI_RST_N, and PCI_INTA_N) are sampled on the rising edge of PCI_CLK. All other timing parameters are defined with respect to this edge.

PCI Reset

Pin Name: PCI_RST_N
Pin Number: 141
PCI_RST_N is an active low input that is used to set the internal registers to their initial state. PCI_RST_N is typically the system power-on reset signal as distributed on the PCI bus.

3.3.4 Miscellaneous I/O

Ground

Pin Name: VSS
Pin Number: 1, 17, 27, 37, 52, 62, 73, 88, 99, 109, 119, 129
Ground reference point to power supply.

PLL VDD

Pin Name: PLL_VDD
Pin Number: 2
Dedicated PLL Power supply (3.3 Volts +/- 10%). Refer to section 7.1 for PLL connections.

PLL Charge Pump Bias

Pin Name: PLL_CPBIAS
Pin Number: 3
Dedicated PLL analog pin for charge pump bias. Refer to section 7.1 for PLL connections.

PLL VCO Bias

Pin Name: PLL_VCOBIAS
Pin Number: 4
Dedicated PLL analog pin for VCO bias. Refer to section 7.1 for PLL connections.

PLL Loop Filter

Pin Name: PLL_LOOPFLT
Pin Number: 5
Dedicated PLL analog input for off-chip loop filter. Refer to section 7.1 for PLL connections.

PLL Ground

Pin Name: PLL_GND
Pin Number: 6
Dedicated PLL Ground (Power supply reference). Refer to section 7.1 for PLL connections.

Test Mode

Pin Name: TEST_MODE
Pin Number: 7
This pin, in conjunction with other pins, enables various test functions within the device. This pin should tied to ground for normal operation.

Power Supply

Pin Name(s): VDD
Pin Number(s): 16, 26, 36, 51, 61, 72, 87, 98, 108, 118, 128and144
Power Supply Input (3.3 volts +/- 10%)

IDE Configuration

Pin Names: JP
Pin Numbers: 80
IDE Configuration Jumper Pin.

JP Pin	CONFIGURATION
0	RAID Class, PCI Class Code = 010400h
1	IDE Class, PCI Class Code = 010185h

Table 3-2: ATA Configuration

This pin has an internal pull-up resistor, and if left unconnected, will default to ‘1’. Otherwise, tie this pin high (1,) or low (0) to select the desired mode.

It is recommended that this pin to be tied to low (RAID Class) when Silicon Image drivers (RAID or Non-RAID) are used.

Base Address 5 Enable

Pin Name: BA5_EN
Pin Number: 139
Base Address 5 Enable Jumper Pin.

BA5_EN Pin	CONFIGURATION
0	Base Address 5 Disabled (Note 1)
1	Base Address 5 Enabled

Table 3-3: Base Address 5 Configuration

Note 1: Reading Base Address 5 returns all zeroes.

This pin does not have an internal resistor and therefore must be tied high (1) or low (0) to select the desired mode.

It is recommended that this pin is enabled (tied high)() for all configurations.

Internal Scan Enable

Pin Name: SCAN_EN
Pin Number: 142
This pin when active (high) will place all scan flip-flops into a scan mode. This pin should be tied to ground for normal operation.

Memory Chip Select

Pin Name: MEM_CS_N
Pin Number: 143
This pin is used to select and enable the external memory. It is active low

4. Package Drawing

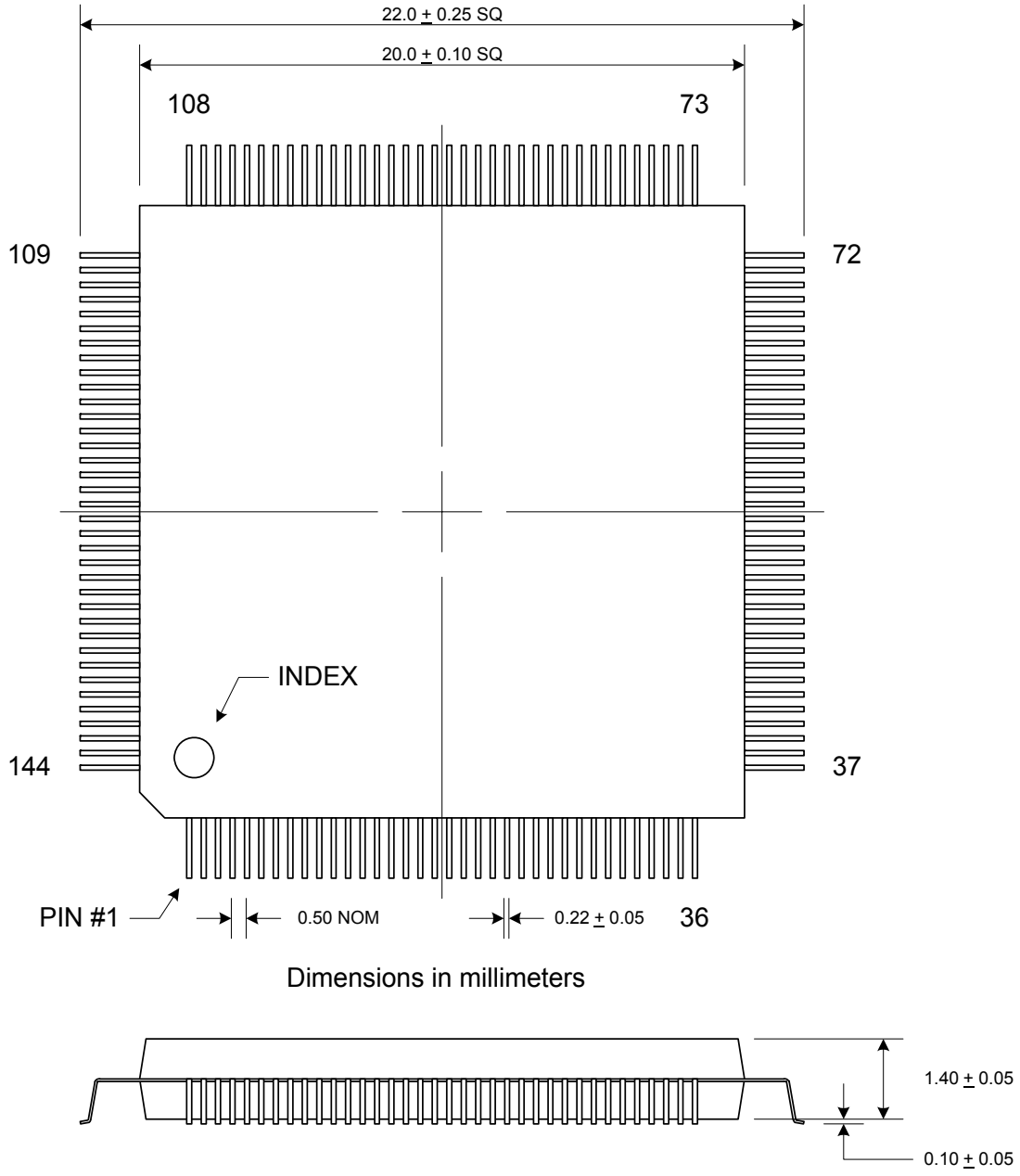


Figure 3-2: Package Drawing – 144 LQFP

Part Ordering Number:
SiI0680ACLU144 (144pin LQFP lead free package)
SiI0680ACL144 (144pin LQFP standard package)

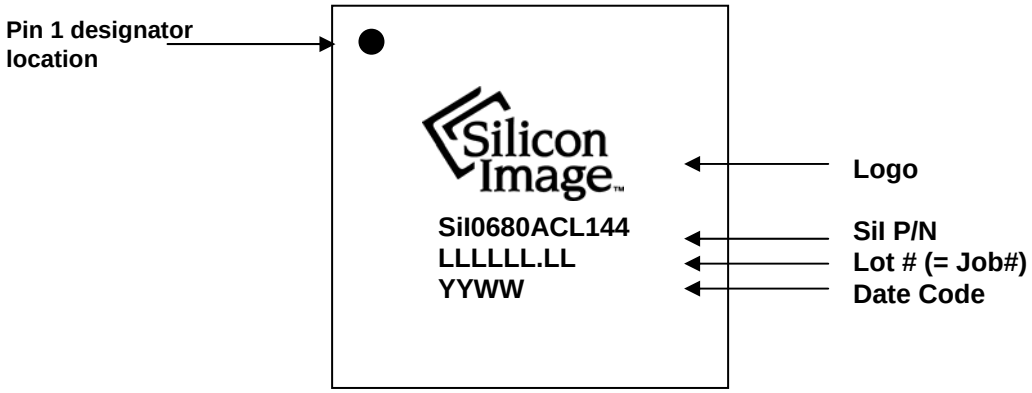


Figure 3-3: Marking Specification – Sil0680ACL144

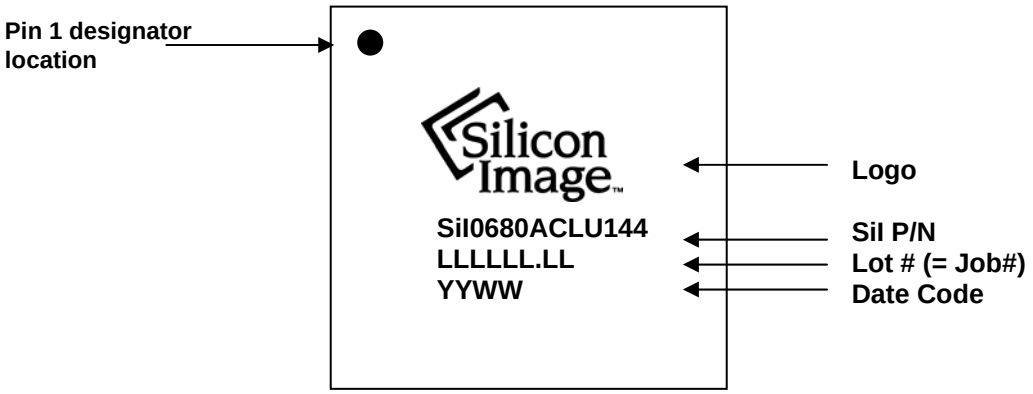


Figure 3-4: Marking Specification – Sil0680ACLU144

5. ASIC Block Diagram

The PCI-680 ASIC contains the major logic modules shown in Figure 5-1.

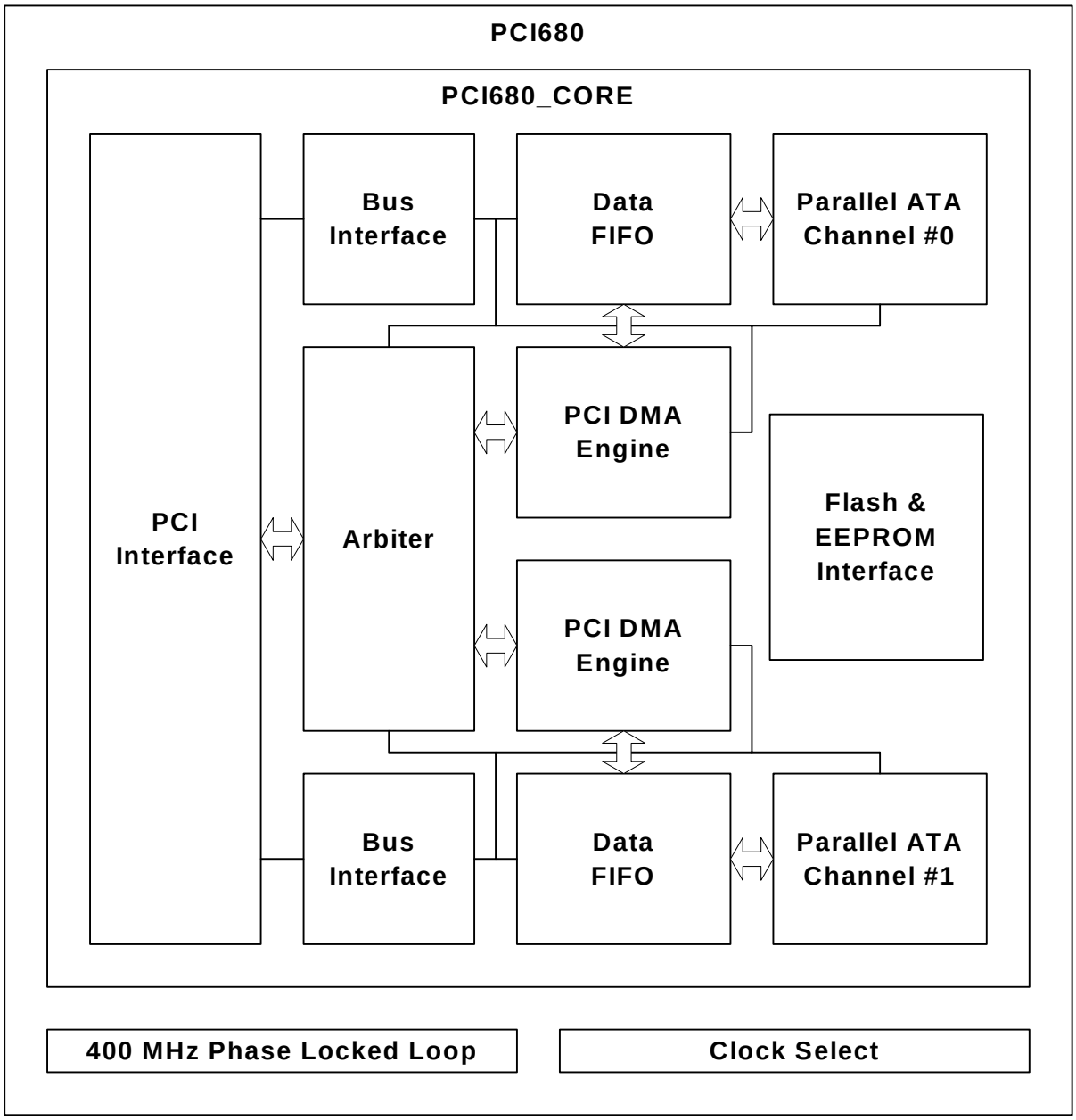


Figure 5-1: PCI-680 ASIC Block Diagram

PCI Bus	Bits	Type	Description
PCI_AD[31:00]	32	I/O	PCI address/data bus
PCI_CBE[3:0]	4	I/O	PCI command/byte enables
PCI_IDSEL	1	I	PCI ID select
PCI_FRAME_N	1	I/O	PCI FRAME# signal
PCI_IRDY_N	1	I/O	PCI IRDY# signal
PCI_TRDY_N	1	I/O	PCI TRDY# signal
PCI_STOP_N	1	I/O	PCI STOP# signal
PCI_DEVSEL_N	1	I/O	PCI DEVSEL# signal
PCI_PAR	1	I/O	PCI parity bit
PCI_PERR_N	1	I/O	PCI parity error signal
PCI_SERR_N	1	OD	PCI system error signal
PCI_REQ_N	1	T	PCI bus request
PCI_GNT_N	1	I	PCI bus grant
PCI_M66EN	1	I	PCI 66 MHz enable
PCI_CLK	1	I	PCI clock
PCI_RST_N	1	I	PCI bus reset

Table 5-1: PCI Bus Signals Group

IDE Channel #0	Bits	Type	Description
IDE0_DD[15:00]	16	I/O	IDE data bus
IDE0_CS0_N	1	I/O	IDE chip select
IDE0_CS1_N	1	I/O	IDE chip select
IDE0_DA0	1	I/O	IDE device address
IDE0_DA1	1	I/O	IDE device address
IDE0_DA2	1	I/O	IDE device address
IDE0_DIOR_N	1	I/O	IDE device IO read
IDE0_DIOW_N	1	I/O	IDE device IO write
IDE0_DMACK_N	1	I/O	IDE DMA acknowledge
IDE0_CBLID_N	1	I	IDE cable ID
IDE0_INTRQ	1	I	IDE interrupt request
IDE0_IORDY	1	I	IDE IO channel ready
IDE0_AT_REXT	1	I/O	IDE external bias circuit
IDE0_DMARQ	1	I	IDE DMA request
IDE0_RST_N	1	I/O	IDE reset

Table 5-2: IDE Channel #0 Signals Group

IDE Channel #1	Bits	Type	Description
IDE1_DD[15:00]	16	I/O	IDE data bus
IDE1_CS0_N	1	I/O	IDE chip select
IDE1_CS1_N	1	I/O	IDE chip select
IDE1_DA0	1	I/O	IDE device address
IDE1_DA1	1	I/O	IDE device address
IDE1_DA2	1	I/O	IDE device address
IDE1_DIOR_N	1	I/O	IDE device IO read
IDE1_DIOW_N	1	I/O	IDE device IO write
IDE1_DMACK_N	1	I/O	IDE DMA acknowledge
IDE1_CBLID_N	1	I	IDE cable ID
IDE1_INTRQ	1	I	IDE interrupt request
IDE1_IORDY	1	I	IDE IO channel ready
IDE1_AT_REXT	1	I/O	IDE external bias circuit
IDE1_DMARQ	1	I	IDE DMA request
IDE1_RST_N	1	I/O	IDE reset

Table 5-3: IDE Channel #1 Signals Group

FLASH Interface	Bits	Type	Description
IDE0_DD[07]	1	O	FLASH memory address bit 18
IDE0_DD[05]	1	O	FLASH memory address bit 17
IDE0_DD[08]	1	O	FLASH memory address bit 16
IDE0_DD[09]	1	O	FLASH memory address bit 15
IDE0_DD[04]	1	O	FLASH memory address bit 14
IDE0_DD[03]	1	O	FLASH memory address bit 13
IDE0_DD[10]	1	O	FLASH memory address bit 12
IDE0_DD[00]	1	O	FLASH memory address bit 11
IDE0_DA2	1	O	FLASH memory address bit 10
IDE0_DD[01]	1	O	FLASH memory address bit 09
IDE0_DD[02]	1	O	FLASH memory address bit 08
IDE0_DD[11]	1	O	FLASH memory address bit 07
IDE0_DD[12]	1	O	FLASH memory address bit 06
IDE0_DD[13]	1	O	FLASH memory address bit 05
IDE0_DD[14]	1	O	FLASH memory address bit 04
IDE0_DD[15]	1	O	FLASH memory address bit 03
IDE0_DA0	1	O	FLASH memory address bit 02
IDE0_CS0_N	1	O	FLASH memory address bit 01
IDE0_CS1_N	1	O	FLASH memory address bit 00
IDE1_DD[07]	1	I/O	FLASH memory data bit 07
IDE1_DD[06]	1	I/O	FLASH memory data bit 06
IDE1_DD[05]	1	I/O	FLASH memory data bit 05
IDE1_DD[04]	1	I/O	FLASH memory data bit 04
IDE1_DD[11]	1	I/O	FLASH memory data bit 03
IDE1_DD[10]	1	I/O	FLASH memory data bit 02
IDE1_DD[09]	1	I/O	FLASH memory data bit 01
IDE1_DD[08]	1	I/O	FLASH memory data bit 00
IDE0_DA1	1	O	FLASH memory read strobe
IDE0_DD[06]	1	O	FLASH memory write strobe
MEM_CS_N	1	O	FLASH memory chip select

Table 5-4: PCI-680 FLASH Memory Signals Group – Shared Signals

EEPROM Interface	Bits	Type	Description
IDE1_CS1_N	1	O	EEPROM serial data
IDE1_CS0_N	1	O	EEPROM serial clock

Table 5-5: PCI-680 EEPROM Memory Signals Group – Shared Signals

Test Mode Signals	Bits	Type	Description
SCAN_EN	1	I	ASIC internal scan mode enable
TEST_MODE	1	I	ASIC test mode enable

Table 5-6: PCI-680 Test Signals Group

6. Clocking System

The SiI 0680A ASIC utilizes an on-chip 400 MHz PLL to synthesize the clock frequencies required to support the various ATA modes. The clock frequency for the ATA UDMA mode logic is software programmable for 66, 100 or 133 MHz. The ATA clock can also be disabled. The clock frequency for the PCI interface logic and most of the device is derived from the 33 MHz PCI bus clock.

The clock tree for ATA Channel #1 is offset by 5 nsec relative to the clock tree for IDE Channel #0. This reduces the amount of simultaneous switching activity within the core and on external pins.

Several test modes within the clocking system are required for PLL and internal scan testing. These topics are covered in Chapter 10.

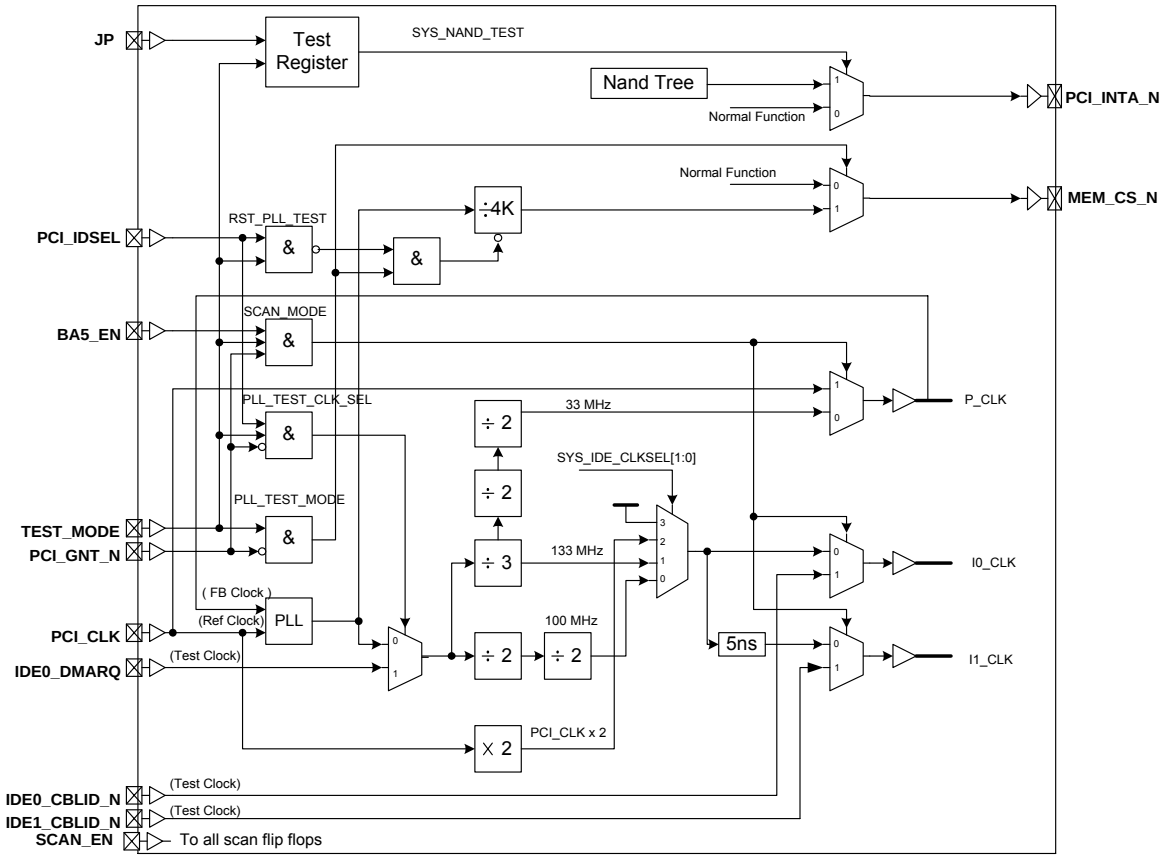


Figure 6-1: SiI 0680A Clocking System and Test Feature Diagram

7. Phased Locked Loop (PLL)

7.1 PLL Connections

The SiI 0680A ASIC utilizes an on-chip Phase Locked Loop (PLL) for high frequency clock synthesis. The PLL is designed to generate a 400 MHz internal clock, which is divided down to produce the clocks for the ATA UDMA interface logic, and is further divided down to produce 33 MHz for the system logic.

7.1.1 PLL Schematic

The schematic of PLL related components are shown in Figure 7-1. Reference Designators shown are for illustration purposes only and do not reflect those on the evaluation board. The values are subject to change. Please contact Silicon Image for the latest revision of the schematic for current reference designators and component values used on evaluation boards.

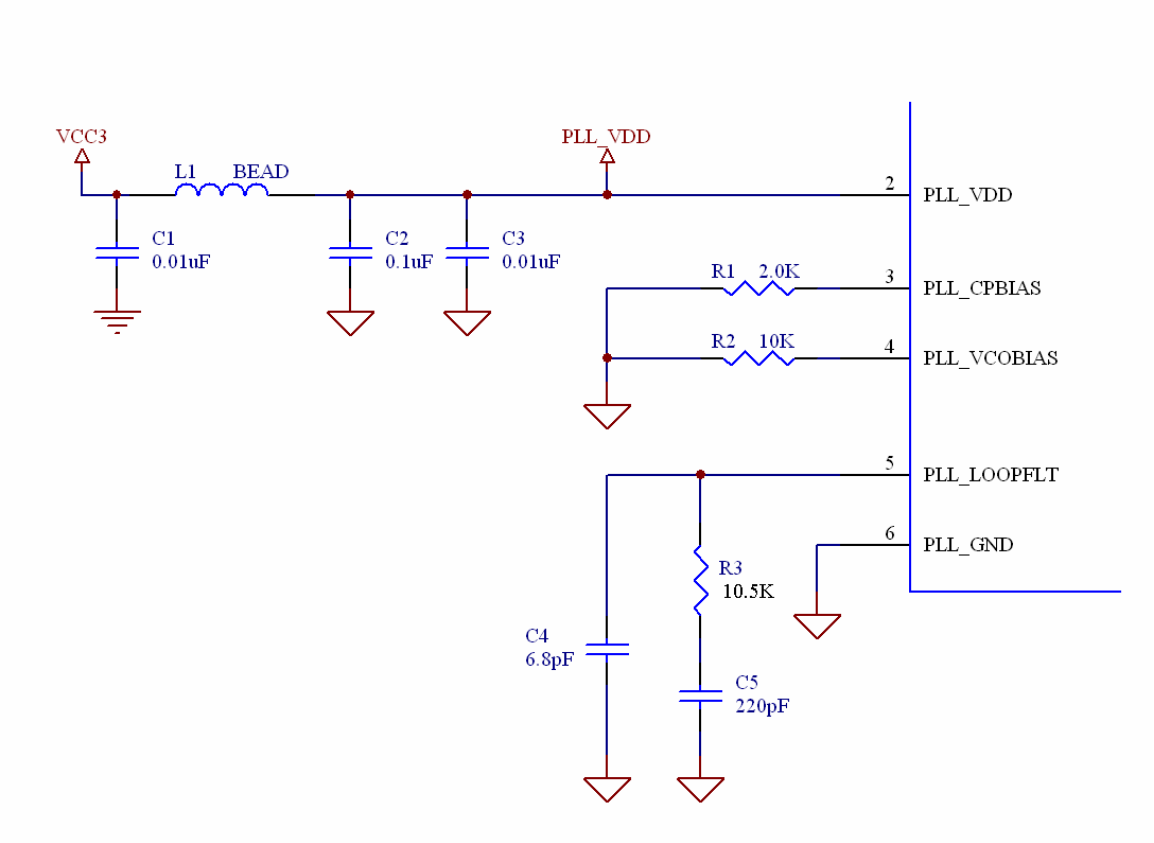


Figure 7-1: Schematic of PLL Circuitry

7.1.2 PLL Components

Recommended part specifications:

1.) Ferrite Bead = 40 Ohm, 300ma, 0805
Qty = 1
Ref Des. = L1
Example Part Numbers: ACT DCB-0805
Steward-USA LI0805E400R
AEM MCB0805F400

2.) Resistor = Metal Film, 10.5K Ohm, 1%, 1/10W, 0805
Qty = 1
Ref Des. = R3
Example Part Numbers: Rohm – MCR10-EZHM-F-1052
KOA – RM73-B-2A-T-1052-F
Meritek – CR10-1052-F
Dale – CRCW0805-1052FT

3.) Resistor = Metal Film, 10.0K Ohm, 1%, 1/10W, 0805
Qty = 1
Ref Des. = R2
Example Part Numbers: Rohm – MCR10-EZHM-F-1002
KOA – RM73-B-2A-T-1002-F
Meritek – CR10-1002-F
Dale – CRCW0805-1002FT

4.) Resistor = Metal Film, 2.0K Ohm, 1%, 1/10W, 0805
Qty = 1
Ref Des. = R1
Example Part Numbers: Rohm – MCR10-EZHM-F-2001
KOA – RM73-B-2A-T-2001-F
Meritek – CR10-2001-F
Dale – CRCW0805-2001FT

5.) Capacitor = Ceramic, 6.8pF, 50V, 5%, NPO, 0805
Qty = 1
Ref Des. = C4
Example Part Numbers: AVX – 0805-5-A-689-J
Rohm – MCH21-5A-6R8-JK
Johanson – 101-R15-N-6R8-J-V4E
Kemet – C0805C689J5GAC

6.) Capacitor = Ceramic, 220pF, 50V, 5%, NPO, 0805
Qty = 1
Ref Des. = C5
Example Part Numbers: AVX – 0805-5-A-221-J
Rohm – MCH21-5A-221-JK
Johanson – 101-R15-N-221-J-V4E
Kemet – C0805C221J5GAC

7.) Capacitor = Ceramic, 0.01uF, 50V, 20%, Y5V, 0805
Qty = 2
Ref Des. = C1, C3
Example Part Numbers: AVX – 0805-5-G-103-M
Rohm – MCH21-5-C-103-KK
Johanson – 500-R15-Z-103-M-V6E
Kemet – C0805C103M5UAC

8.) Capacitor = Ceramic, 0.1uF, 50V, 20%, X7R, 0805
Qty = 1
Ref Des. = C2
Example Part Numbers: AVX – 0805-5-C-104-KATMA
Rohm – MCH21-5-E-104-M
Johanson – 500-R15-W-104-M-V4E

Kemet – C0805C104M5UAC

7.1.3 PLL Layout Requirements

The SiI 0680A uses a high speed Phase Lock Loop (PLL) for clock generation. The layout of this high-speed analog circuit is critical to the proper operation of the circuit. Power and Ground Planes should be used with the Ground Plane located directly under the top external layer.

Isolated “islands” for power and ground plane should be used to isolate high-speed digital currents from the PLL circuitry. The isolated planes should be identical in size and shape. Figures 7-2 and 7-3 show an example 4-layer layout.

The SiI 0680A’s pin PLL_VDD (pin 2) should be connected to the isolated PLL_VDD plane. This plane should be completely isolated with no connection to the main power plane.

The SiI 0680A’s pin PLL_GND (pin 6) should be connected to the isolated PLL_GND plane. The “island” should be connected to the ground plane with a narrow “bridge” of at least 0.015” width of copper. Locate this “bridge” directly under L1 as shown in Figure 7-2.

The PLL components (C2, C3, C4, C5, R1, R2, and R3) should be mounted on top of the PLL_GND “island”. The island should cover all areas under the components, their pads and connected traces. No PLL circuitry should be exposed (be located on top of) to either the main ground plane or cut in the planes. Only the listed PLL components should connect to the “island”. No other ground connections should be made there.

It is important to keep the trace lengths short. No high-speed digital signals should be allowed to pass through, above or below, any portion of the power and ground “islands”. Take extra care to make sure the data bits located on pins 8 through 15 are routed clear of the “islands”.

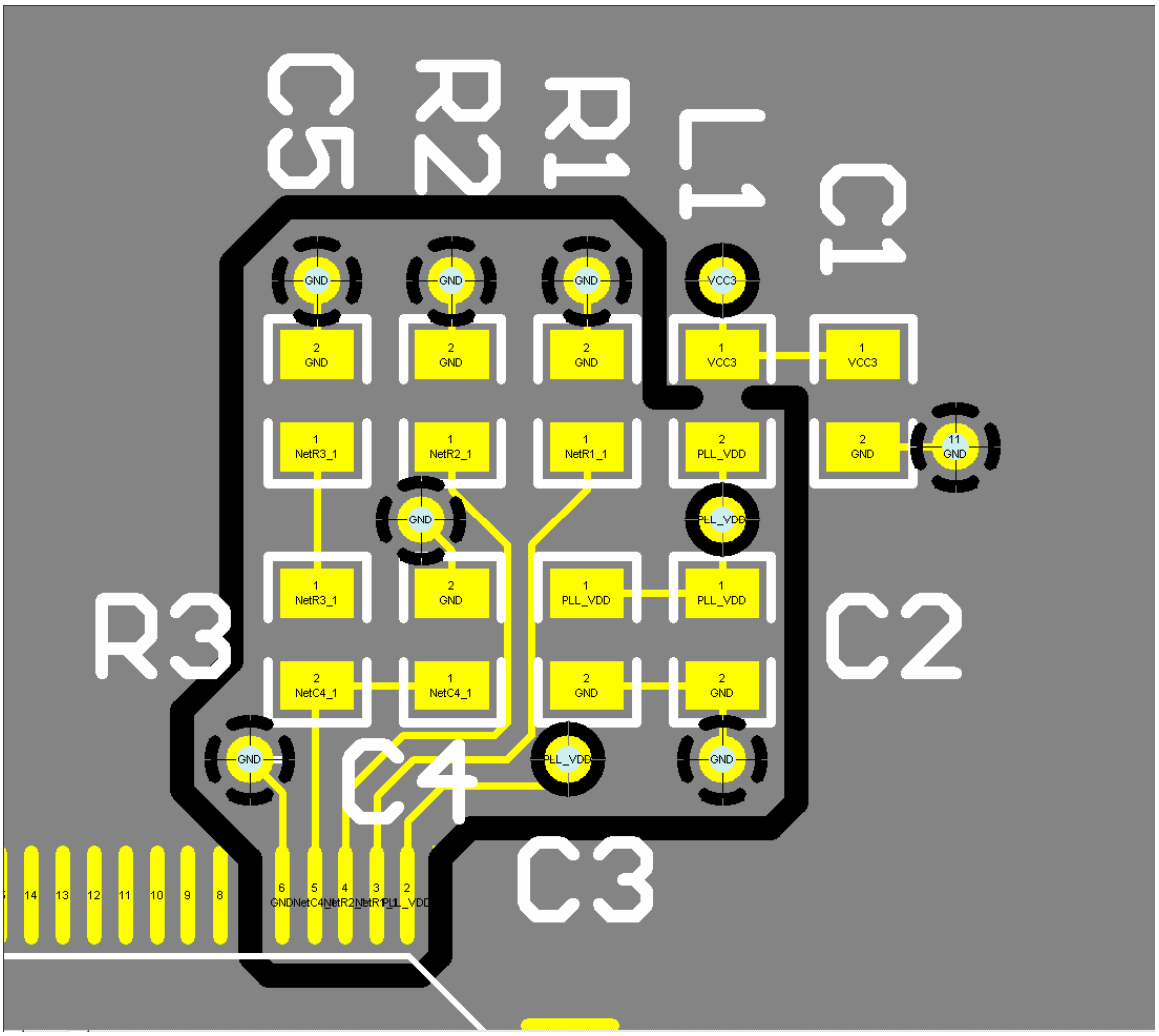


Figure 7-2: Example Layout – Ground Plane

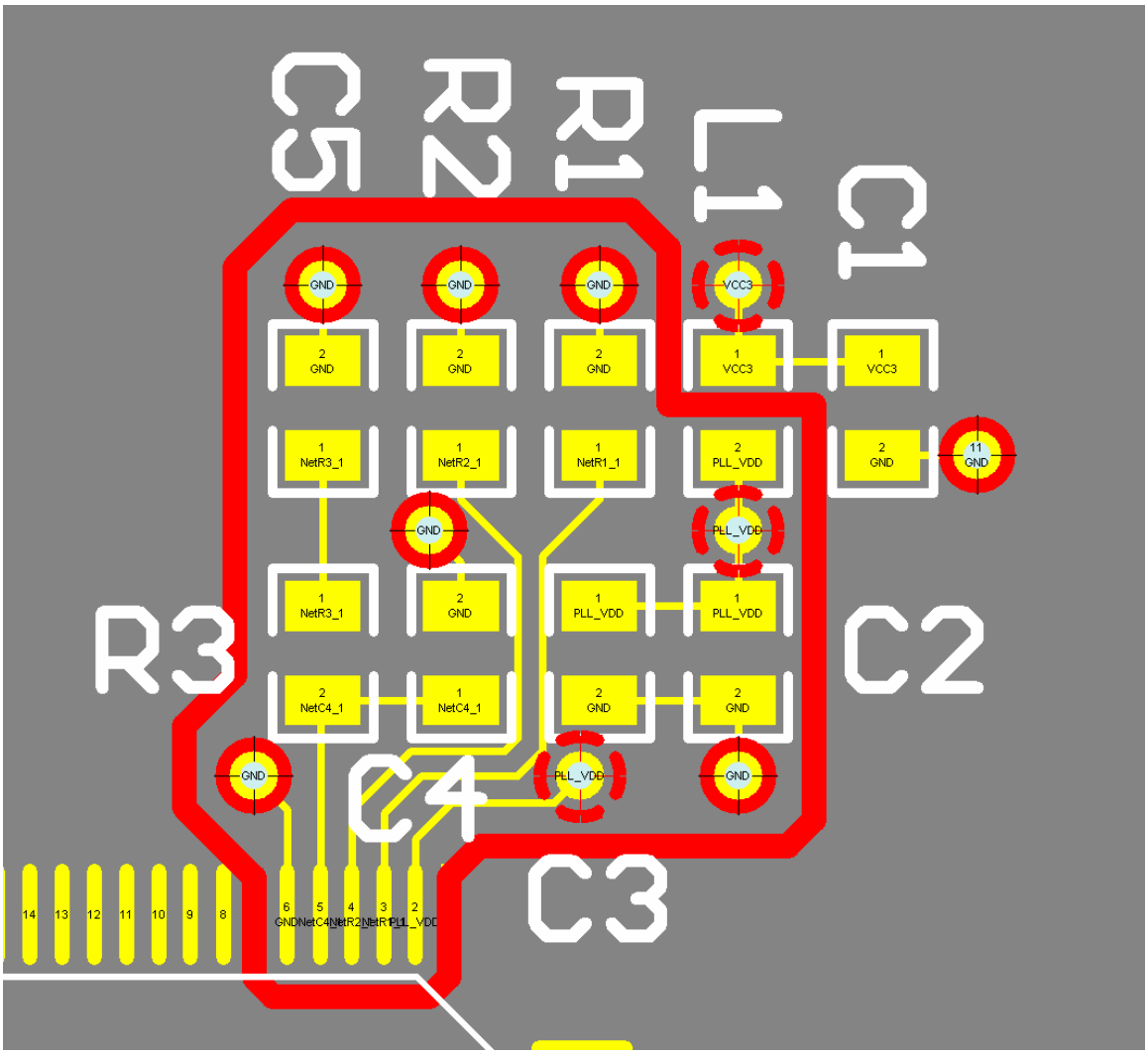


Figure 7-2: Example Layout – Power Plane

8. Auto-Initialization

The SiI 0680A ASIC supports an external FLASH and/or EEPROM device for BIOS extensions and user-defined PCI configuration header data. Interface to either memory device is performed through a set of special function ATA pins. These pins are active in the SiI 0680A auto-initialization mode after release of PCI_RST_N, and return to normal ATA function mode after the auto-initialization is complete.

8.1 Auto-Initialization from FLASH

The SiI 0680A initiates the FLASH detection and configuration space loading sequence upon the release of PCI_RST_N. It begins by reading the highest two addresses ($7FFFF_H$ and $7FFFE_H$), checking for the correct data signature pattern – AA_H and 55_H, respectively. If the data signature pattern is correct, the SiI 0680A continues to sequence the address downward, reading a total of twelve bytes. If the Data Signature is correct (55_H at $7FFFC_H$), the last eight bytes are loaded into the PCI Configuration Space registers.

Note: If both Flash and EEPROM are installed, the PCI Configuration Space registers will be loaded with EEPROM's data. While the sequence is active, the SiI 0680A responds to all PCI bus accesses with a Target Retry.

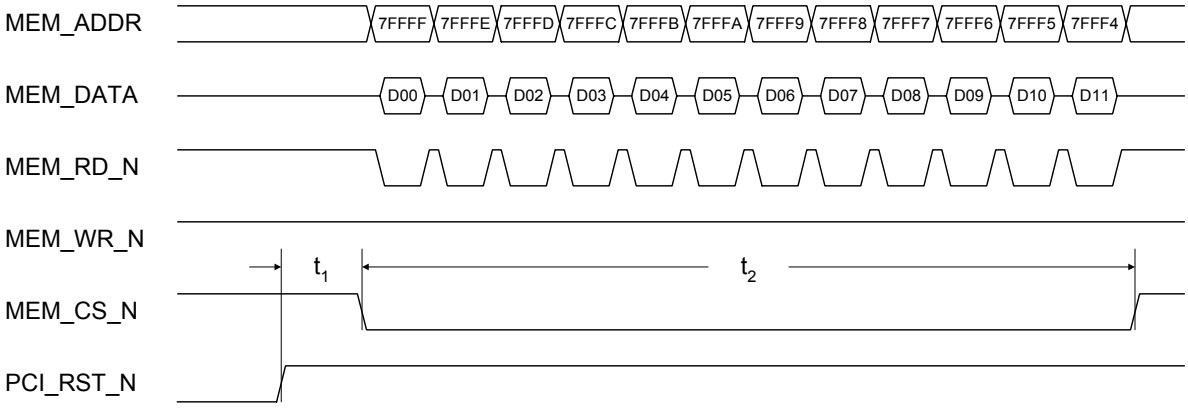


Figure 8-1: Auto-Initialization from Flash Timing

Parameter	Value	Description
t_1	660 ns	PCI reset to Flash Auto-Initialization cycle begin
t_2	7200 ns	Flash Auto-Initialization cycle time

Table 8-1: Auto-Initialization from Flash Timing

Address	Data Byte	Description
$7FFFF_H$	D00	Data Signature = AA_H
$7FFFE_H$	D01	Data Signature = 55_H
$7FFFD_H$	D02	AA = 120 ns FLASH device / Else, 240 ns FLASH device
$7FFFC_H$	D03	Data Signature = 55_H
$7FFFB_H$	D04	PCI Device ID [23:16]
$7FFFA_H$	D05	PCI Device ID [31:24]
$7FFF9_H$	D06	PCI Class Code [15:08]
$7FFF8_H$	D07	PCI Class Code [23:16]
$7FFF7_H$	D08	PCI Sub-System Vendor ID [07:00]
$7FFF6_H$	D09	PCI Sub-System Vendor ID [15:08]
$7FFF5_H$	D10	PCI Sub-System ID [23:16]
$7FFF4_H$	D11	PCI Sub-System ID [31:24]

Table 8-2: FLASH Data Description

8.2 Auto-Initialization from EEPROM

The SiI 0680A initiates the EEPROM detection and configuration space loading sequence after the FLASH read sequence. The SiI 0680A supports up to 256 byte EEPROM with a 2-wire serial interface. The sequence of operations consists of the following.

1) START condition defined as a high-to-low transition on SDAT while SCLK is high.
2) Control byte = 1010 (Control Code) + 000 (Chip Select) + 0 (Write Address)
3) Acknowledge
4) Starting address field = 00000000.
5) Acknowledge
6) Sequential data bytes separated by Acknowledges.
7) STOP condition.

While the sequence is active, the SiI 0680A responds to all PCI bus accesses with a Target Retry.

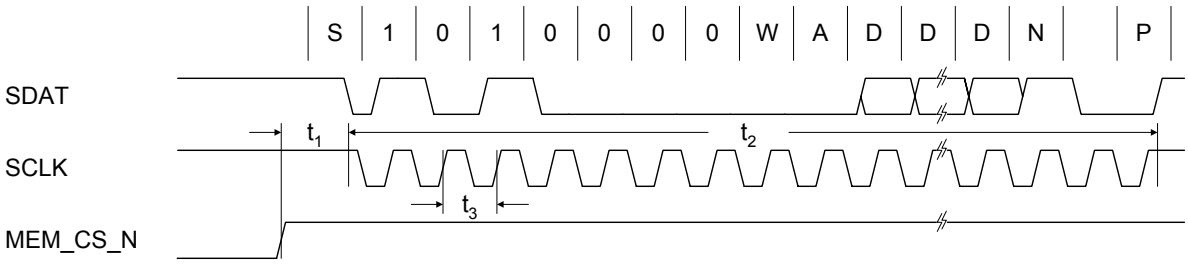


Figure 8-2: Auto-Initialization from EEPROM Timing

Parameter	Value	Description
t_1	26.00 µs	End of Auto-Initialization from FLASH to start of Auto-Initialization from EEPROM
t_2	2.66 ms	Auto-Initialization from EEPROM cycle time
t_3	19.26 µs	EEPROM serial clock period

Table 8-3: Auto-Initialization from EEPROM Timing

Parameter	Description
S	START condition
W	R/W 0 = Write Command, 1 = Read Command
A	Acknowledge
D	Serial data
N	No-Acknowledge
P	STOP condition

Table 8-4: Auto-Initialization from EEPROM Timing Symbols

Address	Data Byte	Description
00_H	D00	Memory Present Pattern = AA_H
01_H	D01	Memory Present Pattern = 55_H
02_H	D02	Data Signature = AA_H
03_H	D03	Data Signature = 55_H
04_H	D04	PCI Device ID [23:16]
05_H	D05	PCI Device ID [31:24]
06_H	D06	PCI Class Code [15:08]
07_H	D07	PCI Class Code [23:16]
08_H	D08	PCI Sub-System Vendor ID [07:00]
09_H	D09	PCI Sub-System Vendor ID [15:08]
$0A_H$	D0A	PCI Sub-System ID [23:16]
$0B_H$	D0B	PCI Sub-System ID [31:24]

Table 8-5: EEPROM Data Description

9. Register Definitions

This section describes the registers within the SiI 0680A PCI-ATA host controller ASIC.

9.1 PCI Configuration Space

The PCI Configuration Space registers define the operation of the SiI 0680A on the PCI bus. These registers are accessible only when the SiI 0680A detects a Configuration Read or Write operation, with its IDSEL asserted, on the 32-bit PCI bus.

Table 9-1, outlines the PCI Configuration space for the SiI 0680A.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Device ID (0680h)		Vendor ID (1095h)		R/W
04_H	PCI Status		PCI Command		R/W
08_H	PCI Class Code			Revision ID	R/W
$0C_H$	BIST	Header Type	Latency Timer	Cache Line Size	R/W
10_H	Base Address Register 0				R/W
14_H	Base Address Register 1				R/W
18_H	Base Address Register 2				R/W
$1C_H$	Base Address Register 3				R/W
20_H	Base Address Register 4				R/W
24_H	Base Address Register 5				R/W
28_H	Reserved				-
$2C_H$	Subsystem ID (0680h)		Subsystem Vendor ID (1095h)		R/W
30_H	Expansion ROM Base Address				R/W
34_H	Reserved			Capabilities Ptr	R
38_H	Reserved				R/W
$3C_H$	Max Latency	Min Grant	Interrupt Pin	Interrupt Line	R/W
40_H	Reserved			Configuration	R/W
44_H	Software Data Register				R/W
48_H	Reserved				-
$4C_H$	Reserved				-
50_H	Reserved				-

Table 9-1: PCI-680 PCI Configuration Space

Address Offset	Register Name				Access Type
	31 16		15 00		
54_H	Reserved				-
58_H	Reserved				-
$5C_H$	Reserved				-
60_H	Power Management Capabilities		Next Item Pointer	Capability ID	R/W
64_H	Data	Reserved	Functions Control and Status		R/W
68_H	Reserved				-
$6C_H$	Reserved				-
70_H	Reserved	PCI Bus Master Status – IDE0	Reserved	PCI Bus Master Command – IDE0	R/W
74_H	PRD Table Address – IDE0				R/W
78_H	Reserved	PCI Bus Master Status – IDE1	Reserved	PCI Bus Master Command – IDE1	R/W
$7C_H$	PRD Table Address – IDE1				R/W
80_H	Reserved			IDE0 Data Transfer Mode	R/W
84_H	Reserved			IDE1 Data Transfer Mode	R/W
88_H	System Configuration Status		System Command		R/W
$8C_H$	System Software Data				R/W
90_H	FLASH Memory Address – Command + Status				R/W
94_H	Reserved			Flash Memory Data	R/W
98_H	EEPROM Memory Address – Command + Status				R/W
$9C_H$	Reserved			EEPROM Memory Data	R/W
$A0_H$	IDE0 TF Timing		IDE0 Config + Status	IDE0 Cmd + Status	R/W
$A4_H$	IDE0 Device 1 PIO Timing		IDE0 Device 0 PIO Timing		R/W
$A8_H$	IDE0 Device 1 DMA Timing		IDE0 Device 0 DMA Timing		R/W
AC_H	IDE0 Device 1 UDMA Timing		IDE0 Device 0 UDMA Timing		R/W
$B0_H$	IDE1 TF Timing		IDE1 Config + Status	IDE1 Cmd + Status	R/W
$B4_H$	IDE1 Device 1 PIO Timing		IDE1 Device 0 PIO Timing		R/W
$B8_H$	IDE1 Device 1 DMA Timing		IDE1 Device 0 DMA Timing		R/W
BC_H	IDE1 Device 1 UDMA Timing		IDE1 Device 0 UDMA Timing		R/W

Table 9-1: Sil 0680A PCI Configuration Space (continued)

9.1.1 Device ID – Vendor ID

Address Offset: 00_H
Access Type: Read /Write
Reset Value: 0x0680_1095

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device ID																Vendor ID															

This register defines the Device ID and Vendor ID associated with the SiI 0680A. The register bits are defined below.

- **Bit [31:16]**: Device ID (R/W) – Device ID. This value in this bit field is determined by any one of three options:
  - 1) This field defaults to 0x0680 to identify the device as a Silicon Image SiI 0680A.
  - 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the PCI Class Code is loaded from that device after reset. The correct signature for an EEPROM device is the data pattern $55AA_H$ at addresses [03_H:02_H] and $55AA_H$ at addresses [01_H:00_H]. The correct signature for a FLASH device is the data pattern $AA55_H$ at addresses [$7FFFF_H$:$7FFFE_H$] and 55_H at address $7FFFC_H$. See chapter 8 for details.
  - 3) system programmable : If Bit 0 of the Configuration register (40_H) is set, to enables writes, the three bytes are system programmable.
- **Bit [15:00]**: Vendor ID (R) – Vendor ID. This field defaults to 0x1095 to identify the vendor as Silicon Image/CMD Technology.

9.1.2 PCI Status – PCI Command

Address Offset: 04_H
Access Type: Read/Write/Write-One-to-Clear
Reset Value: 0x0290_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Det Par Err	Sig Sys Err	Rcvd M Abort	Rcvd T Abort	Sig T Abort	Devsel Timing		Det M Data Par Err	Fast B-to-B	Reserved	66 MHz Capable	Capabilities List	Reserved										Fast B-to-B	SERR Enable	Address Stepping	Par Error	VGA Palette	Memory Wr & Inv	Special Cycles	Bus Master	Memory Space	IO Space

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit 31**: Det. Par Err (R/W1C) – Detected Parity Error. This bit set indicates that the SiI 0680A detected a parity error on the PCI bus-address or data parity error-while responding as a PCI target.
- **Bit 30**: Sig. Sys Err (R/W1C) – Signaled System Error. This bit set indicates that the SiI 0680A signaled SERR on the PCI bus.
- **Bit 29**: Rcvd M Abort (R/W1C) – Received Master Abort. This bit set indicates that the SiI 0680A terminated a PCI bus operation with a Master Abort.
- **Bit 28**: Rcvd T Abort (R/W1C) – Received Target Abort. This bit set indicates that the SiI 0680A received a Target Abort termination.
- **Bit 27**: Sig. T Abort (R/W1C) – Signaled Target Abort. This bit set indicates that the SiI 0680A terminated a PCI bus operation with a Target Abort.
- **Bit [26:25]**: Devsel Timing (R) – Device Select Timing. This bit field indicates the DEVSEL timing supported by the SiI 0680A. The hardwired value is 01_B for Medium decode timing.
- **Bit 24**: Det M Data Par Err (R/W1C) – Detected Master Data Parity Error. This bit set indicates that the SiI 0680A, as bus master, detected a parity error on the PCI bus. The parity error may be either reported by the target device via PERR# on a write operation or by the SiI 0680A on a read operation.
- **Bit 23**: Fast B-to-B Capable (R) – Fast Back-to-Back Capable. This bit is hardwired to 1 to indicate that the SiI 0680A is Fast Back-to-Back capable as a PCI target.
- **Bit 22**: Reserved (R).

- **Bit 21**: 66 MHz Capable (R) – 66 MHz PCI Operation Capable. This bit is hardwired to 0 to indicate that the SiI 0680A is not 66 MHz capable.
- **Bit 20**: Capabilities List (R) – PCI Capabilities List. This bit is hardwired to 1 to indicate that the SiI 0680A has a PCI Power Management Capabilities register linked at offset 34_H.
- **Bit [19:10]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit 09**: Fast B-to-B Enable (R) – Fast Back-to-Back Enable. This bit is hardwired to 0 to indicate that the SiI 0680A does not support Fast Back-to-Back operations as bus master.
- **Bit 08**: SERR Enable (R/W) – SERR Output Enable. This bit set enables the SiI 0680A to drive the PCI SERR# pin when it detects an address parity error. The Parity Error Response bit (06) must also be set to enable SERR# reporting.
- **Bit 07**: Address Stepping (R) – Address Stepping Enable. This bit is hardwired to 0 to indicate that the SiI 0680A does not support Address Stepping.
- **Bit 06**: Par Error Response (R/W) – Parity Error Response Enable. This bit set enables the SiI 0680A to respond to parity errors on the PCI bus. If this bit is cleared, the SiI 0680A will ignore PCI parity errors.
- **Bit 05**: VGA Palette (R) – VGA Palette Snoop Enable. This bit is hardwired to 0 to indicate that the SiI 0680A does not support VGA Palette Snooping.
- **Bit 04**: Mem Wr & Inv (R) – Memory Write and Invalidate Enable. This bit is hardwired to 0 to indicate that the SiI 0680A does not support Memory Write and Invalidate.
- **Bit 03**: Special Cycles (R) – Special Cycles Enable. This bit is hardwired to 0 to indicate that the SiI 0680A does not respond to Special Cycles.
- **Bit 02**: Bus Master (R/W) – Bus Master Enable. This bit set enables the SiI 0680A to act as PCI bus master.
- **Bit 01**: Memory Space (R/W) – Memory Space Enable. This bit set enables the SiI 0680A to respond to PCI memory space access.
- **Bit 00**: IO Space (R/W) – IO Space Enable. This bit set enables the SiI 0680A to respond to PCI IO space access.

9.1.3 PCI Class Code – Revision ID

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0101_8501

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PCI Class Code																PCI Prog Int				IDE1 Mode Prog	IDE1 Pwr-Up Mode	IDE0 Mode Prog	IDE0 Pwr-Up Mode	Revision ID							

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:08]**: PCI Class Code (R) – PCI Class Code. This value in this bit field is determined by any one of three options:
  - 1) the default value, set by an external jumper:
    - If JP = 0, the value is 010400h for RAID mode
    - If JP = 1, the value is 010185h for ATA mode
  - 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the PCI Class Code is loaded from that device after reset. The correct signature for an EEPROM device is the data pattern $55AA_H$ at addresses [03_H:02_H] and $55AA_H$ at addresses [01_H:00_H]. The correct signature for a FLASH device is the data pattern $AA55_H$ at addresses [$7FFFF_H$:$7FFFE_H$] and 55_H at address $7FFFC_H$. See chapter 8 for details.
  - 3) system programmable : If Bit 0 of the Configuration register (40_H) is set, to enables writes, the three bytes are system programmable.
- **Bit [07:00]**: Revision ID (R) – Chip Revision ID. This bit field is hardwired to 01_H to indicate the first revision silicon.

9.1.4 BIST – Header Type – Latency Timer – Cache Line Size

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BIST								Header Type								Latency Timer								Cache Line Size							

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: BIST (R). This bit field is hardwired to 00_H.
- **Bit [23:16]**: Header Type (R). This bit field is hardwired to 00_H.
- **Bit [15:08]**: Latency Timer (R/W). This bit field is used to specify the time in number of PCI clocks, the SiI 0680A as a master is still allowed to control the PCI bus after its GRANT_L is deasserted. The lower four bits [0B:08] are hardwired to 0_H, resulting in a time granularity of 16 clocks.
- **Bit [07:00]**: Cache Line Size (R/W). This bit field is used to specify the system cacheline size in terms of 32-bit words. The upper 2 bits are not used, resulting a maximum size of 64 32-bit words. With the SiI 0680A as a master, initiating a read transaction, it issues PCI command Read Multiple in place , when empty space in its FIFO is larger than the value programmed in this register.

9.1.5 Base Address Register 0

Address Offset: 10_H
Access Type: Read/Write
Reset Value: 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 0																													Not Used		

This register defines the addressing of various control functions within the SiI 0680A. The register bits are defined below.

- **Bit [31:03]**: Base Address Register 0 (R/W). This register defines the I/O Space base address for the IDE Channel #0 task file registers.
- **Bit [02:00]**: Base Address Register 0 (R). This bit field is not used and is hardwired to 001_B

9.1.6 Base Address Register 1

Address Offset: 14_H
Access Type: Read/Write
Reset Value: 0x0000_0001

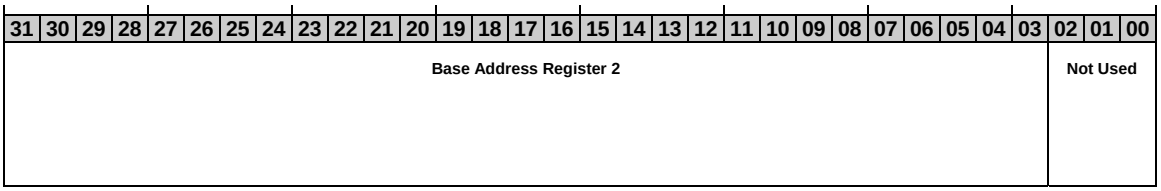
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 1																														Not Used	

This register defines the addressing of various control functions within the SiI 0680A. The register bits are defined below.

- **Bit [31:02]**: Base Address Register 1 (R/W). This register defines the I/O Space base address for the IDE Channel #0 Device Control- Alternate Status register.
- **Bit [01:00]**: Base Address Register 1 (R). This bit field is not used and is hardwired to 01_B.

9.1.7 Base Address Register 2

Address Offset: 18_H
Access Type: Read/Write
Reset Value: 0x0000_0001

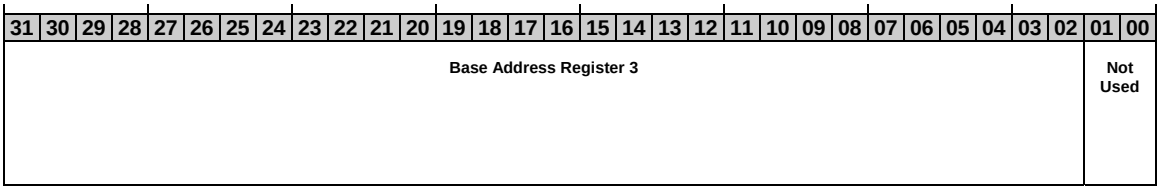


This register defines the addressing of various control functions within the SiI 0680A. The register bits are defined below.

- **Bit [31:03]**: Base Address Register 2 (R/W). This register defines the I/O Space base address for the IDE Channel #1 task file registers.
- **Bit [02:00]**: Base Address Register 2 (R). This bit field is not used and is hardwired to 001_B.

9.1.8 Base Address Register 3

Address Offset: $1C_H$
Access Type: Read/Write
Reset Value: 0x0000_0001

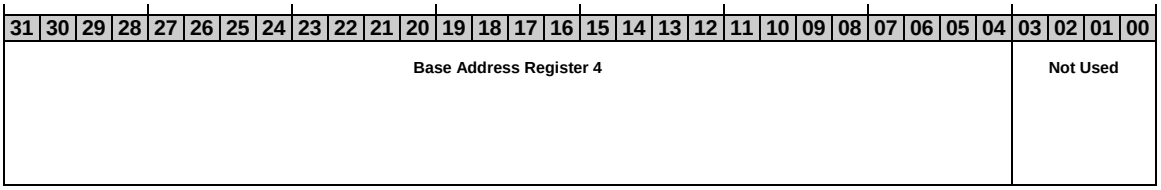


This register defines the addressing of various control functions within the SiI 0680A. The register bits are defined below.

- **Bit [31:02]**: Base Address Register 3 (R/W). This register defines the I/O Space base address for the IDE Channel #1 Device Control- Alternate Status register.
- **Bit [01:00]**: Base Address Register 3 (R). This bit field is not used and is hardwired to 01_B.

9.1.9 Base Address Register 4

Address Offset: 20_H
Access Type: Read/Write
Reset Value: 0x0000_0001

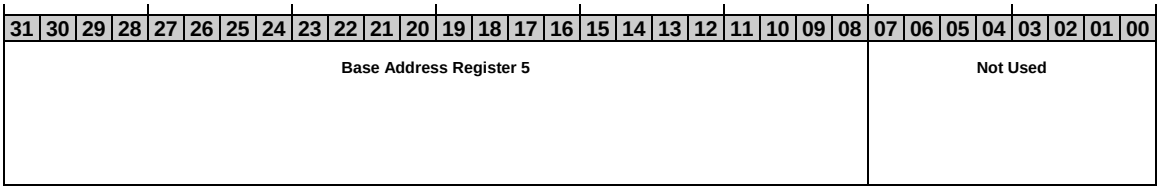


This register defines the addressing of various control functions within the SiI 0680A. The register bits are defined below.

- **Bit [31:04]**: Base Address Register 4 (R/W). This register defines the I/O Space base address for the PCI bus master registers.
- **Bit [03:00]**: Base Address Register 4 (R). This bit field is not used and is hardwired to 0001_B.

9.1.10 Base Address Register 5

Address Offset: 24_H
Access Type: Read/Write
Reset Value: 0x0000_0000

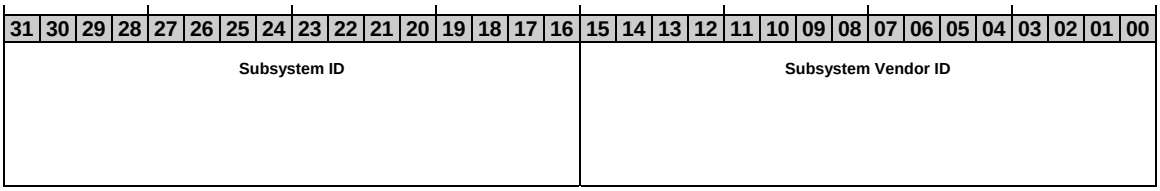


This register defines the addressing of various control functions within the SiI 0680A. This register is enabled when input BA5_EN is set to one. See section 3.1.5 for descriptions. The register bits are defined below.

- **Bit [31:08]**: Base Address Register 5 (R/W). This register defines the Memory Space base address for all Silicon Image driver specific functions.
- **Bit [07:00]**: Base Address Register 5 (R). This bit field is not used and is hardwired to 00_H.

9.1.11 Subsystem ID – Subsystem Vendor ID

Address Offset: $2C_H$
Access Type: Read/Write
Reset Value: 0x0680_1095



This register defines the Subsystem ID fields associated with the PCI bus. See chapter 8 for details. The register bits are defined below.

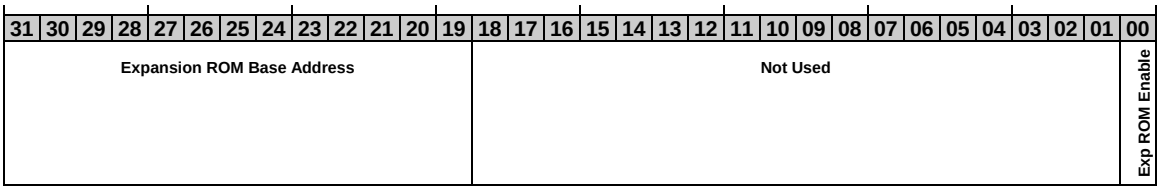
- **Bit [31:16]**: Subsystem ID (R) – Subsystem ID.
- **Bit [15:00]**: Subsystem Vendor ID (R) – Subsystem Vendor ID.

The value in this bit field is determined by any one of three options:

- 1) **Bit [31:16]**: Subsystem ID (R) – Subsystem ID defaults to $0680A_H$. **Bit [15:00]**: Subsystem Vendor ID (R) – Subsystem Vendor ID defaults to 1095_H.
- 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the PCI Class Code is loaded from that device after reset. The correct signature for an EEPROM device is the data pattern $55AA_H$ at addresses [03_H:02_H] and $55AA_H$ at addresses [01_H:00_H]. The correct signature for a FLASH device is the data pattern $AA55_H$ at addresses [$7FFFF_H$:$7FFFE_H$] and 55_H at address $7FFFC_H$. See chapter 8 for details.
- 3) system programmable : If Bit 0 of the Configuration register (40_H) is set, to enables writes, the three bytes are system programmable.

9.1.12 Expansion ROM Base Address

Address Offset: 30_H
Access Type: Read/Write
Reset Value: 0x0000_0000

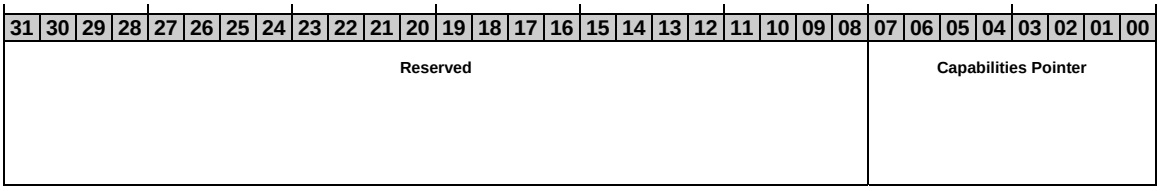


This register defines the Expansion ROM base address associated with the PCI bus. The register bits are defined below.

- **Bit [31:19]**: Expansion ROM Base Address (R/W) – Expansion ROM Base Address. This bit field defines the upper bits of the Expansion ROM base address.
- **Bit [18:01]**: Not Used (R). This bit field is hardwired to 00000_H. The minimum Expansion ROM address range is 512K bytes.
- **Bit [00]**: Exp ROM Enable (R/W) – Expansion ROM Enable. This bit is set to enable the Expansion ROM access.

9.1.13 Capabilities Pointer

Address Offset: 34_H
Access Type: Read
Reset Value: 0x0000_0060

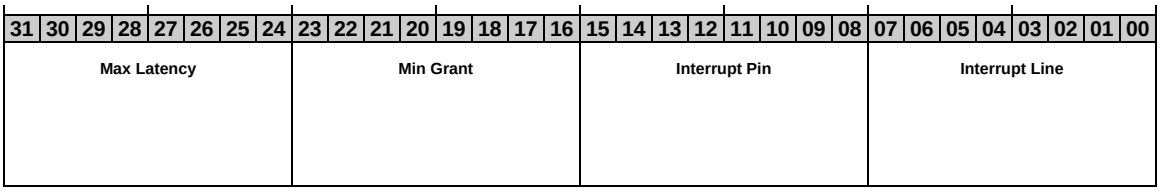


This register defines the link to a list of new capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:00]**: Capabilities Pointer (R) – Capabilities Pointer. This bit field defaults to 60_H to define the address for the 1st entry in a list of PCI Power Management capabilities.

9.1.14 Max Latency – Min Grant – Interrupt Pin – Interrupt Line

Address Offset: $3C_H$
Access Type: Read/Write
Reset Value: 0x0000_0100

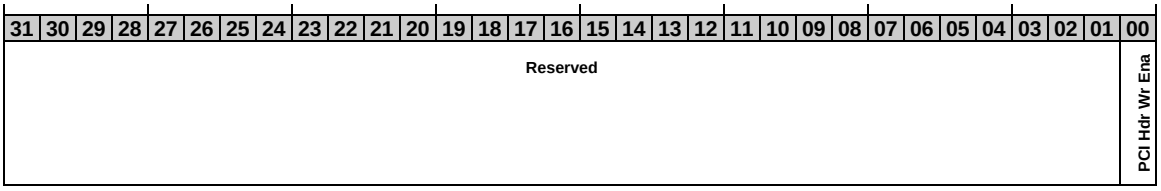


This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: Max Latency (R) – Maximum Latency. This bit field is hardwired to 00_H.
- **Bit [23:16]**: Min Grant (R) – Minimum Grant. This bit field is hardwired to 00_H.
- **Bit [15:08]**: Interrupt Pin (R) – Interrupt Pin Used. This bit field is hardwired to 01_H to indicate that the SiI 0680A uses the INTA# interrupt.
- **Bit [07:00]**: Interrupt Line (R/W) – Interrupt Line. This bit field is used by the system to indicate interrupt line routing information. The SiI 0680A does not use this information.

9.1.15 Configuration

Address Offset: 40_H
Access Type: Read/Write
Reset Value: 0x0000_0000

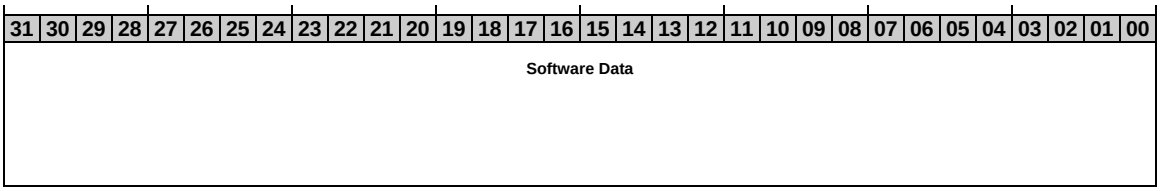


This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:01]**: Reserved (R). This bit field is hardwired to 00000000_H.
- **Bit [00]**: PCI Hdr Wr Ena (R/W) – PCI Configuration Header Write Enable. This bit is set to enable write access to the following registers in the PCI Configuration Header: Device ID ($03\text{-}02_H$), PCI Class Code ($09\text{-}0B_H$), Subsystem Vendor ID ($2D\text{-}2C_H$), and Subsystem ID ($2F\text{-}2E_H$).

9.1.16 Software Data Register

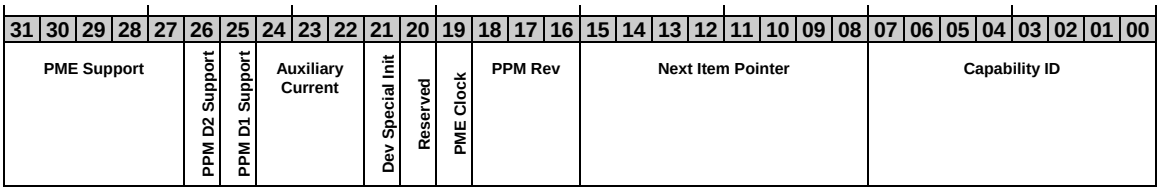
Address Offset: 44_H
Access Type: Read/Write
Reset Value: Undefined



This register is used by the software for non-resettable data storage. The contents are unknown on power-up and are never cleared by any type of reset.

9.1.17 Power Management Capabilities

Address Offset: 60_H
Access Type: Read Only
Reset Value: 0x0622_0001



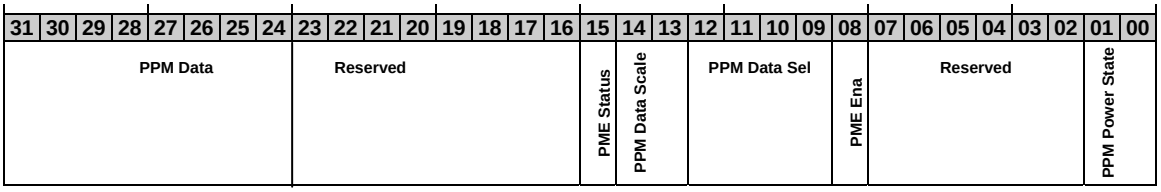
This register defines the power management capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:27]**: PME Support (R) – Power Management Event Support. This bit field is hardwired to 00_H to indicate that the SiI 0680A does not support PME.
- **Bit [26]**: PPM D2 Support (R) – PCI Power Management D2 Support. This bit is hardwired to 1 to indicate support for the D2 Power Management State.
- **Bit [25]**: PPM D1 Support (R) – PCI Power Management D1 Support. This bit is hardwired to 1 to indicate support for the D1 Power Management State.
- **Bit [24:22]**: Auxiliary Current (R) – Auxiliary Current. This bit field is hardwired to 000_B.
- **Bit [21]**: Dev Special Init (R) – Device Special Initialization. This bit is hardwired to 1 to indicate that the SiI 0680A does not require special initialization
- **Bit [20]**: Reserved (R). This bit is reserved and returns zero on a read.

- **Bit [19]**: PME Clock (R) – Power Management Event Clock. This bit is hardwired to 0. The SiI 0680A does not support PME.
- **Bit [18:16]**: PPM Rev (R) – PCI Power Management Revision. This bit field is hardwired to 010_B to indicate compliance with the PCI Power Management Interface Specification revision 1.1.
- **Bit [15:08]**: Next Item Pointer (R) – PCI Additional Capability Next Item Pointer. This bit field is hardwired to 00_H to indicate that there are no additional items on the Capabilities List.
- **Bit [07:00]**: Capability ID (R) – PCI Additional Capability ID. This bit field is hardwired to 01_H to indicate that this Capabilities List is a PCI Power Management definition.

9.1.18 Power Management Control + Status

Address Offset: 64_H
Access Type: Read/Write
Reset Value: 0x6400_4000

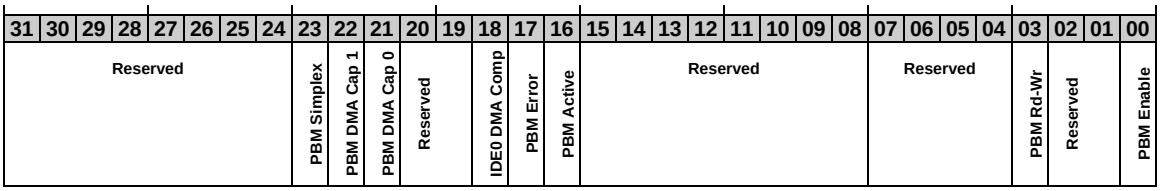


This register defines the power management capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: PPM Data (R) – PCI Power Management Data. This bit field is hardwired to 64h.
- **Bit [23:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15]**: PME Status (R) – PME Status. This bit field is hardwired to 0. The SiI 0680A does not support PME.
- **Bit [14:13]**: PPM Data Scale (R) – PCI Power Management Data Scale. This bit field is hardwired to 11_B to indicate a scaling factor of one.
- **Bit [12:09]**: PPM Data Sel (R/W) – PCI Power Management Data Select. This bit field is set by the system to indicate which data field is to be reported through the PPM Data bits.
- **Bit [08]**: PME Ena (R) – PME Enable. This bit field is hardwired to 0. The SiI 0680A does not support PME.
- **Bit [07:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: PPM Power State (R/W) – PCI Power Management Power State. This bit field is set by the system to dictate the current Power State: 00 = D0 (Normal Operation), 01 = D1, 10 = D2, and 11 = D3 Hot.

9.1.19 PCI Bus Master – IDE0

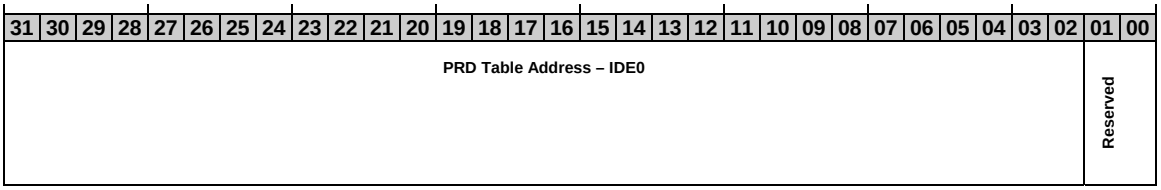
Address Offset: 70_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the PCI bus master register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 4, Offset 00_H, Base Address 5, Offset 00_H, and Base Address 5, Offset 10_H. See Section 9.7.1 for bit definitions.

9.1.20 PRD Table Address – IDE0

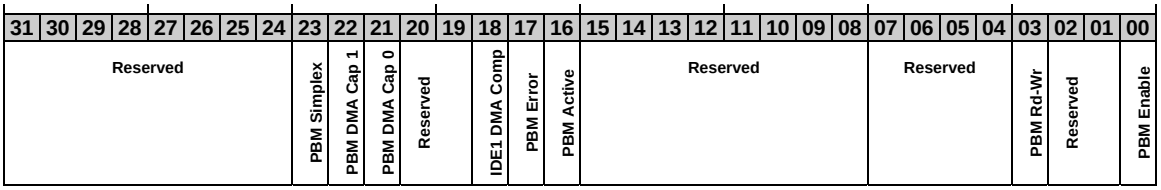
Address Offset: 74_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the PRD Table Address register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 4, Offset 04_H and Base Address 5, Offset 04_H. See Section 9.7.2 for bit definitions.

9.1.21 PCI Bus Master – IDE1

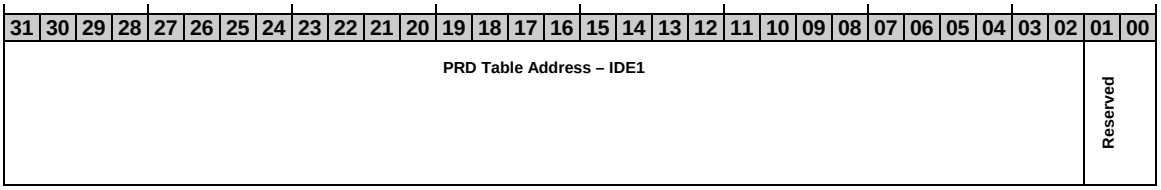
Address Offset: 78_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the PCI bus master register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 4, Offset 08_H, Base Address 5, Offset 08_H, and Base Address 5, Offset 18_H. See Section 9.7.3 for bit definitions.

9.1.22 PRD Table Address – IDE1

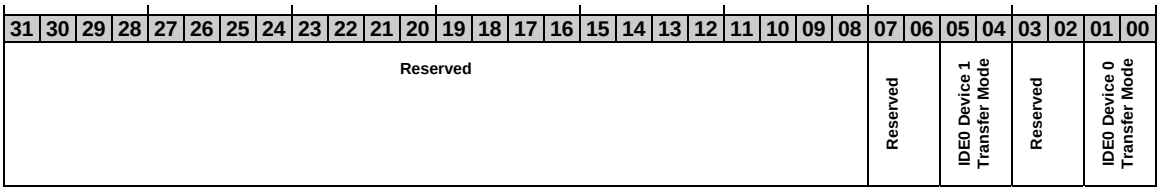
Address Offset: $7C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the PRD Table Address register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 4, Offset $0C_H$ and Base Address 5, Offset $0C_H$. See Section 9.7.4 for bit definitions.

9.1.23 Data Transfer Mode – IDE0

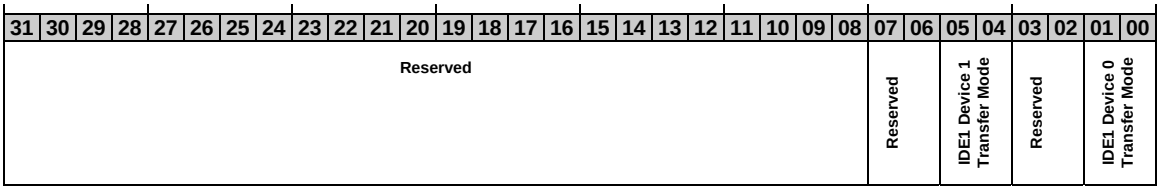
Address Offset: 80_H
Access Type: Read/Write
Reset Value: 0x0000_0022



This register defines the transfer mode register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $B4_H$. See Section 9.7.38 for bit definitions.

9.1.24 Data Transfer Mode – IDE1

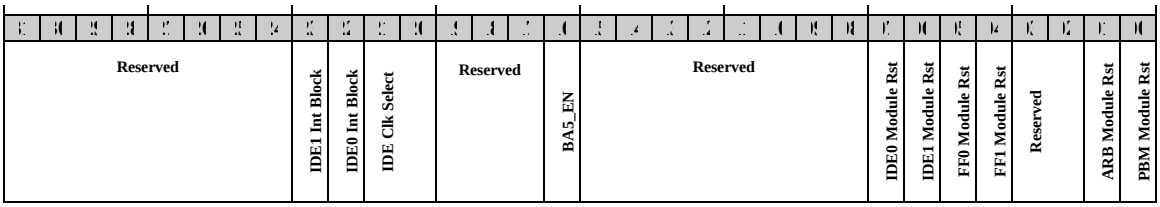
Address Offset: 84_H
Access Type: Read/Write
Reset Value: 0x0000_0022



This register defines the transfer mode register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $F4_H$. See Section 9.7.52 for bit definitions.

9.1.25 System Configuration Status – Command

Address Offset: 88_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the system configuration status and command register for the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 48_H. See Section 9.7.13 for bit definitions.

9.1.26 System Software Data Register

Address Offset: $8C_H$
Access Type: Read/Write
Reset Value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
System Software Data																															

This register is used by the software for non-resettable data storage. The contents are unknown on power-up and are never cleared by any type of reset. The register bits are also mapped to Base Address 5, Offset $4C_H$. See Section 9.7.14 for bit definitions.

9.1.27 FLASH Memory Address – Command + Status

Address Offset: 90_H
Access Type: Read/Write
Reset Value: 0x0000_0000

This register defines the address and command/status register for FLASH memory interface in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 50_H. See Section 9.7.15 for bit definitions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved				Mem Init Done	Reserved	Mem Access Start	Mem Access Type	Reserved					Memory Address																		

9.1.28 FLASH Memory Data

Address Offset: 94_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Memory Data							

This register defines the data register for FLASH memory interface in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 54_H. See Section 9.7.16 for bit definitions.

9.1.29 EEPROM Memory Address – Command + Status

Address Offset: 98_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved			Mem Error	Mem Init Done	Reserved	Mem Access Start	Mem Access Type	Reserved								Mem Address															

This register defines the address and command/status register for EEPROM memory interface in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 58_H. See Section 9.7.17 for bit definitions.

9.1.30 EEPROM Memory Data

Address Offset: $9C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Memory Data							

This register defines the data register for EEPROM memory interface in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $5C_H$. See Section 9.7.18 for bit definitions.

9.1.31 IDE0 Task File Timing + Configuration + Status

Address Offset: $A0_H$
Access Type: Read/Write
Reset Value: 0x6515_0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Addr Setup Count				Active Count						Recovery Count						Reserved	Watchdog Int Ena	Watchdog Ena	Watchdog Timeout	Interrupt Status	Virtual DMA Int	IORDY Monitoring	Reserved	Reserved				Channel Tri-State	Channel Rst	Buffered Cmd	Cable 80

This register defines the task file timing register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $A0_H$. See Section 9.7.33 for bit definitions.

9.1.32 IDE0 PIO Timing

Address Offset: $A4_H$
Access Type: Read/Write
Reset Value: 0x62DD_62DD

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
Device 1 Addr Setup Count	Device 1 Active Count	Device 1 Recovery Count		Device 0 Addr Setup Count	Device 0 Active Count		Device 0 Recovery Count

This register defines the PIO timing register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $A4_H$. See Section 9.7.34 for bit definitions.

9.1.33 IDE0 DMA Timing

Address Offset: $A8_H$
Access Type: Read/Write
Reset Value: 0x4392_4392

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
Device 1 Addr Setup Count	Device 1 Active Count	Device 1 Recovery Count		Device 0 Addr Setup Count	Device 0 Active Count		Device 0 Recovery Count

This register defines the DMA timing register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $A8_H$. See Section 9.7.35 for bit definitions.

9.1.34 IDE0 UDMA Timing

Address Offset: AC_H
Access Type: Read/Write
Reset Value: 0x4009_4009

31 30	29 28	27 26 25	24	23 22 21 20	19 18 17 16	15 14	13 12	11 10 09	08	07 06 05 04	03 02 01 00
Device 1 Data Input Delay	Device 1 DSTROBE Delay	Device 1 HSTROBE Delay	Reserved	Device 1 Cycle Time Count		Device 0 Data Input Delay	Device 0 DSTROBE Delay	Device 0 HSTROBE Delay	Reserved		Device 0 Cycle Time Count

This register defines the UDMA timing register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset AC_H. See Section 9.7.36 for bit definitions.

9.1.35 IDE1 Task File Timing + Configuration + Status

Address Offset: $B0_H$
Access Type: Read/Write
Reset Value: 0x6515_0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Addr Setup Count				Active Count						Recovery Count						Reserved	Watchdog Int Ena	Watchdog Ena	Watchdog Timeout	Interrupt Status	Virtual DMA Int	IORDY Monitoring	Reserved					Channel Tri-State	Channel Rst	Buffered Cmd	Cable 80

This register defines the task file timing register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $E0_H$. See Section 9.7.47 for bit definitions.

9.1.36 IDE1 PIO Timing

Address Offset: $B4_H$
Access Type: Read/Write
Reset Value: 0x62DD_62DD

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Addr Setup Count				Device 1 Active Count						Device 1 Recovery Count						Device 0 Addr Setup Count				Device 0 Active Count								Device 0 Recovery Count			

This register defines the PIO timing register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $E4_H$. See Section 9.7.48 for bit definitions.

9.1.37 IDE1 DMA Timing

Address Offset: $B8_H$
Access Type: Read/Write
Reset Value: 0x4392_4392

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Addr Setup Count				Device 1 Active Count						Device 1 Recovery Count						Device 0 Addr Setup Count				Device 0 Active Count								Device 0 Recovery Count			

This register defines the DMA timing register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $E8_H$. See Section 9.7.48 for bit definitions.

9.1.38 IDE1 UDMA Timing

Address Offset: BC_H
Access Type: Read/Write
Reset Value: 0x4009_4009

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Data Input Delay		Device 1 DSTROBE Delay		Device 1 HSTROBE Delay			Reserved			Device 1 Cycle Time Count						Device 0 Data Input Delay		Device 0 DSTROBE Delay		Device 0 HSTROBE Delay			Reserved			Device 0 Cycle Time Count					

This register defines the UDMA timing register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset EC_H. See Section 9.7.50 for bit definitions.

9.2 Internal Register Space – Base Address 0

These registers are 32-bits wide and define the internal operation of the SiI 0680A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	IDE0 TF Starting Sector Number	IDE0 TF Sector Count	IDE0 TF Features IDE0 TF Error	IDE0 TF Data	R/W
04_H	IDE0 TF Command+Status	IDE0 TF Device+Head	IDE0 TF Cylinder High	IDE0 TF Cylinder Low	R/W

Table 9-2: SiI 0680A Internal Register Space – Base Address 0

9.2.1 IDE0 Task File Register 0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
IDE0 Task File Starting Sector Number	IDE0 Task File Sector Count	IDE0 Task File Features (W) IDE0 Task File Error (R)	IDE0 Task File Data

This register defines one of the IDE Channel #0 Task File registers in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 80_H. See Section 9.7.25 for bit definitions.

9.2.2 IDE0 Task File Register 1

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
IDE0 Task File Command + Status	IDE0 Task File Device+Head	IDE0 Task File Cylinder High	IDE0 Task File Cylinder Low

This register defines one of the IDE Channel #0 Task File registers in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 84_H. See Section 9.7.26 for bit definitions.

9.3 Internal Register Space – Base Address 1

These registers are 32-bits wide and define the internal operation of the SiI 0680A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	IDE0 TF Device Control Auxiliary Status	Reserved	Reserved	R/W

Table 9-3: SiI 0680A Internal Register Space – Base Address 1

9.3.1 IDE0 Task File Register 2

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE0 Task File Device Control IDE0 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #0 Task File registers in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset 88_H. See Section 9.7.27 for bit definitions.

9.4 Internal Register Space – Base Address 2

These registers are 32-bits wide and define the internal operation of the SiI 0680A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	IDE1 TF Starting Sector Number	IDE1 TF Sector Count	IDE1 TF Features IDE1 TF Error	IDE1 TF Data	R/W
04_H	IDE1 TF Command+Status	IDE1 TF Device+Head	IDE1 TF Cylinder High	IDE1 TF Cylinder Low	R/W

Table 9-4: SiI 0680A Internal Register Space – Base Address 2

9.4.1 IDE1 Task File Register 0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
IDE1 Task File Starting Sector Number	IDE1 Task File Sector Count	IDE1 Task File Features (W) IDE1 Task File Error (R)	IDE1 Task File Data

This register defines one of the IDE Channel #1 Task File registers in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $C0_H$. See Section 9.7.39 for bit definitions.

9.4.2 IDE1 Task File Register 1

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
IDE1 Task File Command + Status	IDE1 Task File Device+Head	IDE1 Task File Cylinder High	IDE1 Task File Cylinder Low

This register defines one of the IDE Channel #1 Task File registers in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $C4_H$. See Section 9.7.40 for bit definitions.

9.5 Internal Register Space – Base Address 3

These registers are 32-bits wide and define the internal operation of the SiI 0680A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	IDE1 TF Device Control Auxiliary Status	Reserved	Reserved	R/W

Table 9-5: SiI 0680A Internal Register Space – Base Address 3

9.5.1 IDE1 Task File Register 2

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Task File Device Control IDE1 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #1 Task File registers in the SiI 0680A. The register bits are also mapped to Base Address 5, Offset $C8_H$. See Section 9.7.41 for bit definitions.

9.6 Internal Register Space – Base Address 4

These registers are 32-bits wide and define the internal operation of the SiI 0680A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	PCI Bus Master Status – IDE0	Software Data	PCI Bus Master Command – IDE0	R/W
04_H	PRD Table Address – IDE0				R/W
08_H	Reserved	PCI Bus Master Status – IDE1	Reserved	PCI Bus Master Command – IDE1	R/W
$0C_H$	PRD Table Address – IDE1				R/W

Table 9-6: SiI 0680A Internal Register Space – Base Address 4

9.6.1 PCI Bus Master – IDE0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_XX00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE0 DMA Comp	PBM Error	PBM Active	IDE Watchdog	IDE1 DMA Comp	Software							Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #0 in the SiI 0680A. See Section 9.7.1 for bit definitions.

9.6.2 PRD Table Address – IDE0

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE0																														Reserved	

This register defines the PRD Table Address register for IDE Channel #0 in the SiI 0680A. The register bits are also mapped to PCI Configuration Space, Offset 74_H and Base Address 5, Offset 04_H. See Section 9.7.2 for bit definitions.

9.6.3 PCI Bus Master – IDE1

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #1 in the SiI 0680A. See Section 9.7.3 for bit definitions.

9.6.4 PRD Table Address – IDE1

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE1																														Reserved	

This register defines the PRD Table Address register for IDE Channel #1 in the SiI 0680A. The register bits are also mapped to PCI Configuration Space, Offset $7C_H$ and Base Address 5, Offset $0C_H$. See Section 9.7.4 for bit definitions.

9.7 Internal Register Space – Base Address 5

These registers are 32-bits wide and define the internal operation of the SiI 0680A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI Memory space. The Base Address 5 can be disabled by setting input BA5_EN to low

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	PCI Bus Master Status – IDE0	Software Data	PCI Bus Master Command – IDE0	R/W
04_H	PRD Table Address – IDE0				R/W
08_H	Reserved	PCI Bus Master Status – IDE1	Reserved	PCI Bus Master Command – IDE1	R/W
$0C_H$	PRD Table Address – IDE1				R/W
10_H	PCI Bus Master Status – IDE1	PCI Bus Master Status2 – IDE0	Software Data	PCI Bus Master Command2 – IDE0	R/W
14_H	Reserved				-
18_H	Reserved	PCI Bus Master Status2 – IDE1	Reserved	PCI Bus Master Command2 – IDE1	R/W
$1C_H$	Reserved				-
20_H	PRD Address – IDE0				R
24_H	PCI Bus Master Byte Count – IDE0				R
28_H	PRD Address – IDE1				R
$2C_H$	PCI Bus Master Byte Count – IDE1				R
30_H	Reserved				-
34_H	Reserved				-
38_H	Reserved				-
$3C_H$	Reserved				-
40_H	FIFO Valid Byte Count – IDE0		FIFO Wr Request Control – IDE0	FIFO Rd Request Control – IDE0	R/W
44_H	FIFO Valid Byte Count – IDE1		FIFO Wr Request Control – IDE1	FIFO Rd Request Control – IDE1	R/W
48_H	System Configuration Status		System Command		R/W
$4C_H$	System Software Data				R/W
50_H	FLASH Memory Address – Command and Status				R/W
54_H	Reserved			Flash Memory Data	R/W
58_H	EEPROM Memory Address – Command and Status				R/W
$5C_H$	Reserved			EEPROM Memory Data	R/W
60_H	FIFO Port – IDE0				R/W

Address Offset	Register Name				Access Type
	31 16		15 00		
64_H	Reserved				-
68_H	FIFO Byte1 Write Pointer – IDE0	FIFO Byte1 Read Pointer – IDE0	FIFO Byte0 Write Pointer – IDE0	FIFO Byte0 Read Pointer – IDE0	R
$6C_H$	FIFO Byte3 Write Pointer – IDE0	FIFO Byte3 Read Pointer – IDE0	FIFO Byte2 Write Pointer – IDE0	FIFO Byte2 Read Pointer – IDE0	R
70_H	FIFO Port – IDE1				R/W
74_H	Reserved				-
78_H	FIFO Byte1 Write Pointer – IDE1	FIFO Byte1 Read Pointer – IDE1	FIFO Byte0 Write Pointer – IDE1	FIFO Byte0 Read Pointer – IDE1	R
$7C_H$	FIFO Byte3 Write Pointer – IDE1	FIFO Byte3 Read Pointer – IDE1	FIFO Byte2 Write Pointer – IDE1	FIFO Byte2 Read Pointer – IDE1	R
80_H	IDE0 TF Starting Sector Number	IDE0 TF Sector Count	IDE0 TF Features IDE0 TF Error	IDE0 TF Data	R/W
84_H	IDE0 TF Command+Status	IDE0 TF Device+Head	IDE0 TF Cylinder High	IDE0 TF Cylinder Low	R/W
88_H	Reserved	IDE0 TF Device Control Auxiliary Status	Reserved	Reserved	R/W
$8C_H$	IDE0 Read Ahead Data				R/W
90_H	IDE0 TF Starting Sector Number2	IDE0 TF Sector Count2	IDE0 TF Features2 IDE0 TF Error2	Reserved	R/W
94_H	IDE0 TF Cmd+Sts2	IDE0 TF Device+Head2	IDE0 TF Cylinder High2	IDE0 TF Cylinder Low2	R/W
98_H	Reserved				-
$9C_H$	IDE0 Virtual DMA/PIO Read Ahead Byte Count				R/W
$A0_H$	IDE0 TF Timing		IDE0 Config + Status	IDE0 Cmd + Status	R/W
$A4_H$	IDE0 Device 1 PIO Timing		IDE0 Device 0 PIO Timing		R/W
$A8_H$	IDE0 Device 1 DMA Timing		IDE0 Device 0 DMA Timing		R/W
AC_H	IDE0 Device 1 UDMA Timing		IDE0 Device 0 UDMA Timing		R/W
$B0_H$	IDE0 Test Register				R/W
$B4_H$	Reserved			IDE0 Data Transfer Mode	R/W
$B8_H$	Reserved				-
BC_H	Reserved				-
$C0_H$	IDE1 TF Starting Sector Number	IDE1 TF Sector Count	IDE1 TF Features IDE1 TF Error	IDE1 TF Data	R/W
$C4_H$	IDE1 TF Command+Status	IDE1 TF Device+Head	IDE1 TF Cylinder High	IDE1 TF Cylinder Low	R/W
$C8_H$	Reserved	IDE1 TF Device Control Auxiliary Status	Reserved		R/W

Address Offset	Register Name				Access Type
	31 16		15 00		
CC_H	IDE1 Read Ahead Data				R/W
$D0_H$	IDE1 TF Starting Sector Number2	IDE1 TF Sector Count2	IDE1 TF Features2 IDE1 TF Error2	Reserved	R/W
$D4_H$	IDE1 TF Cmd+Sts2	IDE1 TF Device+Head2	IDE1 TF Cylinder High2	IDE1 TF Cylinder Low2	R/W
$D8_H$	Reserved				-
DC_H	IDE1 Virtual DMA/PIO Read Ahead Byte Count				R/W
$E0_H$	IDE1 TF Timing		IDE1 Config + Status	IDE1 Cmd + Status	R/W
$E4_H$	IDE1 Device 1 PIO Timing		IDE1 Device 0 PIO Timing		R/W
$E8_H$	IDE1 Device 1 DMA Timing		IDE1 Device 0 DMA Timing		R/W
EC_H	IDE1 Device 1 UDMA Timing		IDE1 Device 0 UDMA Timing		R/W
$F0_H$	IDE1 Test Register				R/W
$F4_H$	Reserved			IDE1 Data Transfer Mode	R/W
$F8_H$	Reserved				-
FC_H	Reserved				-

Table 9-7: SiI 0680A Internal Register Space – Base Address 5

9.7.1 PCI Bus Master – IDE0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_XX00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE0 DMA Comp	PBM Error	PBM Active	IDE Watchdog	IDE1 DMA Comp	Software						Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #0 in the SiI 0680A. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18]**: IDE0 DMA Comp (R/W1C) – IDE0 DMA Completion Interrupt. During write DMA operation, This bit set indicates that the IDE0 interrupt has been asserted and all data has been written to system memory. During Read DMA, This bit set indicates that the IDE0 interrupt has been asserted.

This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE0 interrupt line.

- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE0. This bit set indicates that a PCI bus error occurred while the SiI 0680A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE0. This bit set indicates that the SiI 0680A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit[15]** : IDE Watchdog Timer Status (R) – This bit is an Ored result of bit 12 in IDE0 Task File Timing + Configuration + Status and bit 12 of IDE1 Task File Timing + Configuration + Status registers. When set indicates that either IDE0 or IDE1 Watchdog timer has expired.
- **Bit[14]** : IDE1 Interrupt Status (R) – This bit is a copy of Bit[18] IDE1 DMA Completion Interrupt in PCI Bus Master – IDE1.
- **Bit [13:08]**: Software Data (R/W) – System Software Data Storage. This bit field is used for read/write data storage by the system. The properties of this bit field are detailed below.

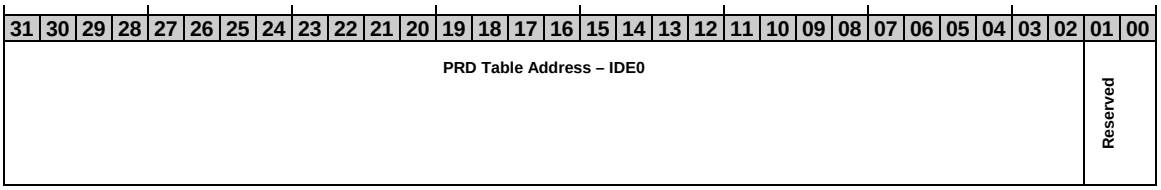
Bit Location	Default	Description
[13:12]	XX_B	Not cleared by any reset
[11:10]	00_B	Cleared by PCI reset
[09:08]	XX_B	Cleared only by a D0-D3 power state change

Table 9-8: Software Data Byte, Base Address 5, Offset 00_H

- **Bit [07:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE0 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE0 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE0. This bit is set to enable PCI bus master operations for IDE Channel #0. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE0 Task File or PIO data registers will be terminated with Target-Abort.

9.7.2 PRD Table Address – IDE0

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the PRD Table Address register for IDE Channel #0 in the SiI 0680A. The register bits are defined below.

- **Bit [31:02]**: PRD Table Address (R/W) – Physical Region Descriptor Table Address. This bit field defines the Descriptor Table base address.
- **Bit [01:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

9.7.3 PCI Bus Master – IDE1

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #1 in the SiI 0680A. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18]**: IDE1 DMA Comp (R/W1C) – IDE1 DMA Completion Interrupt. During write DMA operation, this bit set indicates that the IDE1 interrupt has been asserted and all data has been written to system memory. During Read DMA, this bit set indicates that the IDE1 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE1 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE1. This bit set indicates that a PCI bus error occurred while the SiI 0680A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE1. This bit set indicates that the SiI 0680A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE1 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE1 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE1. This bit is set to enable PCI bus master operations for IDE Channel #1. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE1 Task File or PIO data registers will be terminated with Target-Abort.

9.7.4 PRD Table Address – IDE1

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE1																														Reserved	

This register defines the PRD Table Address register for IDE Channel #1 in the SiI 0680A. The register bits are defined below.

- **Bit [31:02]**: PRD Table Address (R/W) – Physical Region Descriptor Table Address. This bit field defines the Descriptor Table base address.
- **Bit [01:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

9.7.5 PCI Bus Master2 – IDE0

Address Offset: 10_H
Access Type: Read/Write
Reset Value: 0x0008_xx00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 PBM Simplex	IDE1 PBM DMA Cap 0	IDE1 PBM DMA Cap 1	IDE1 Buffer Empty	IDE1 Watchdog	IDE1 DMA Comp	IDE1 PBM Error	IDE1 PBM Active	IDE0 PBM Simplex	IDE0 PBM DMA Cap 1	IDE0 PBM DMA Cap 0	IDE0 Watchdog IDE0	IDE0 Buffer Empty	IDE0 DMA Comp	IDE0 PBM Error	IDE0 PBM Active	IDE Watchdog	IDE0 DMA Comp	Software							Reserved			PBM Rd-Wr	Reserved		PBM Enable

This register defines the second PCI bus master register for IDE Channel #0 in the SiI 0680A. The system must access these register bits through this address to enable the Large Block Transfer Mode.

The register bits are defined below.

- **Bit [31:29]**: (R) These bits are copy of PCI Bus Master IDE1 bits [23:21].
- **Bit [28]**: IDE1 Watchdog (R) . This bit is a copy of bit 12 in IDE1 Task File Timing + Configuration + Status register. Refer to chapter 9.7.47 for detail information.
- **Bit [27]** : IDE1 Buffer empty (R). This bit set indicates IDE1 FIFO is empty.
- **Bit [26**:24]: (R) These bits are copy of PCI Bus Master IDE1 bits [18:16].
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20]**: IDE0 Watchdog (R) : This bit is a copy of bit 12 in IDE0 Task File Timing + Configuration + Status register. Refer to chapter 9.7.33 for detail information.
- **Bit [19]** : IDE0 Buffer empty (R). This bit set indicates IDE0 FIFO is empty.
- **Bit [18]**: IDE0 DMA Comp (R/W1C) – IDE0 DMA Completion Interrupt. During write DMA operation, This bit set indicates that the IDE0 interrupt has been asserted and all data has been written to system memory. During Read DMA, This bit set indicates that the IDE0 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE0 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE0. This bit set indicates that a PCI bus error occurred while the SiI 0680A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE0. This bit set indicates that the SiI 0680A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit[15]** : IDE Watchdog Timer Status (R) – This bit is an Ored result of bit 12 in IDE1 Task File Timing + Configuration + Status and bit 12 of IDE0 Task File Timing + Configuration + Status registers. When set indicates that either IDE0 or IDE1 Watchdog timer has expired.
- **Bit[14]** : IDE1 Interrupt Status (R) – This bit is a copy of Bit[18] IDE1 DMA Completion Interrupt in PCI Bus Master – IDE1.
- **Bit [13:08]**: Software Data (R/W) – System Software Data Storage. This bit field is used for read/write data storage by the system. The properties of this bit field are detailed below.

Bit Location	Default	Description
[13:12]	XX_B	Not cleared by any reset
[11:10]	00_B	Cleared by PCI reset
[09:08]	XX_B	Cleared only by a D0-D3 power state change

Table 9-9: Software Data Byte, Base Address 5, Offset 10_H

- **Bit [07:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.

- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE0 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE0 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE0. This bit is set to enable PCI bus master operations for IDE Channel #0. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE0 Task File or PIO data registers will be terminated with Target-Abort.

9.7.6 PCI Bus Master2 – IDE1

Address Offset: 18_H
Access Type: Read/Write
Reset Value: 0x0008_xx00

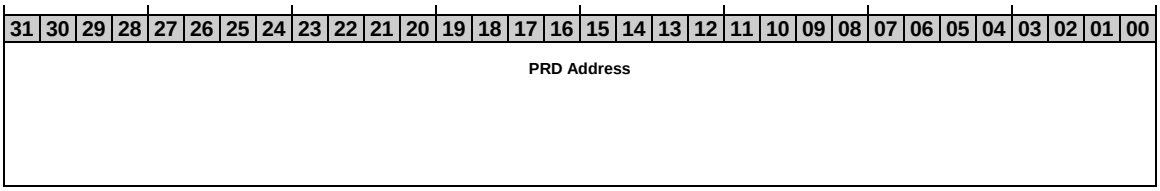
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	IDE1 Watchdog	IDE1 Buffer Empty	IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the second PCI bus master register for IDE Channel #1 in the SiI 0680A. The system must access these register bits through this address to enable the Large Block Transfer Mode.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20]**: IDE1 Watchdog (R) . This bit is a copy of bit 12 in IDE1 Task File Timing + Configuration + Status register. Refer to chapter 9.7.47 for detail information.
- **Bit [19]** : IDE1 Buffer empty (R). This bit set indicates IDE1 FIFO is empty.
- **Bit [18]**: IDE1 DMA Comp (R/W1C) – IDE1 DMA Completion Interrupt. During write DMA operation, this bit set indicates that the IDE1 interrupt has been asserted and all data has been written to system memory. During Read DMA, this bit set indicates that the IDE1 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE1 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE1. This bit set indicates that a PCI bus error occurred while the SiI 0680A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE1. This bit set indicates that the SiI 0680A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE1 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE1 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE1. This bit is set to enable PCI bus master operations for IDE Channel #1. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE1 Task File or PIO data registers will be terminated with Target-Abort.

9.7.7 PRD Address – IDE0

Address Offset: 20_H
Access Type: Read Only
Reset Value: 0x0000_0000

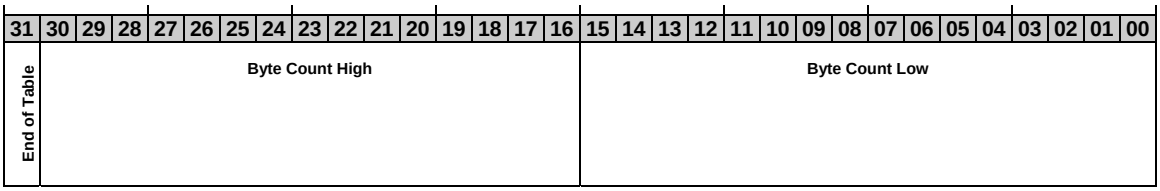


This register reflects the current DMA address and uses for diagnostic purposes only.

- **Bit [31:00]**: PRD Address (R) – This field is the current DMA0 Address.

9.7.8 PCI Bus Master Byte Count – IDE0

Address Offset: 24_H
Access Type: Read Only
Reset Value: 0x0000_0000

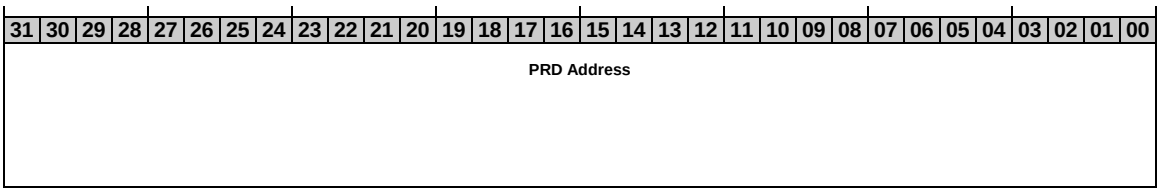


This register defines the byte count register in the PCI bus master logic for IDE Channel #0 in the SiI 0680A. The register bits are defined below.

- **Bit [31]**: End of Table (R). This bit set indicates that this is the last entry in the PRD table.
- **Bit [30:16]** Byte Count High (R). This bit field is the PRD entry byte count extension for Large Block Transfer Mode. Under generic mode, this bit field is reserved and returns zeros on a read.
- **Bit [15:00]** Byte Count Low (R). This bit field reflects the current DMA0 byte count value.

9.7.9 PRD Address – IDE1

Address Offset: 28_H
Access Type: Read Only
Reset Value: 0x0000_0000



This register reflects the current DMA1 Address and uses for diagnostic purposes only.

- **Bit [31:00]**: PRD Address (R) – This field is the current DMA1 Address.

9.7.10 PCI Bus Master Byte Count – IDE1

Address Offset: $2C_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
End of Table	Byte Count High															Byte Count Low															

This register defines the byte count register in the PCI bus master logic for IDE Channel #1 in the SiI 0680A. The register bits are defined below.

- **Bit [31]**: End of Table (R). This bit set indicates that this is the last entry in the PRD table.
- **Bit [30:16]** Byte Count High (R). This bit field is the PRD entry byte count extension for Large Block Transfer Mode. Under generic mode, this bit field is reserved and returns zeros on a read.
- **Bit [15:00]** Byte Count Low (R). This bit field reflects the current DMA1 byte count value.

9.7.11 FIFO Valid Byte Count and Control – IDE0

Address Offset: 40_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								FIFO Valid Byte Count – IDE0								Reserved		FIFO Wr Req Ctrl – IDE0						Reserved		FIFO Rd Req Ctrl – IDE0					

This register defines the FIFO valid byte count register and PCI bus request control for IDE Channel #0 in the SiI 0680A. The register bits are defined below.

- **Bit [31:25]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [24:16]**: FIFO Valid Byte Count – IDE0 (R). This bit field provides the valid byte count for the data FIFO for IDE Channel #0. A value of 000_H indicates empty, while a value of 100_H indicates a full FIFO with 256 bytes.
- **Bit [15:14]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [13:08]**: FIFO Wr Req Ctrl – IDE0 (R/W) – FIFO Write Request Control. This bit field defines the FIFO threshold to assign DMA0 priority when requesting a PCI bus for a write operation. A value of 00_H indicates that DMA0 write request priority is set to 1 whenever the FIFO contains greater than zero DWords, while a value of $3F_H$ indicates that DMA0 write request priority is set to 1 whenever the FIFO contains greater than 63 Dwords. This bit field is useful when two DMA channels are competing for accessing PCI bus.

  When the two DMA channels request the PCI bus at the same time, the one with the higher priority will have the bus when it's granted to the SiI 0680A. If the two DMA channels have the same priority, the channel that had the bus last will have the bus when it's granted to the SiI 0680A.

  When one DMA channel is controlling the PCI bus, and the other channel requests the PCI bus, if the channel currently controlling the PCI bus has the same or higher priority, it remains controlling the bus. However, if the channel requesting the PCI bus has higher priority, the lower priority channel terminates the PCI transaction, yielding the bus to the channel with the higher priority.

- **Bit [07:06]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [05:00]**: FIFO Rd Req Ctrl – IDE0 (R/W) – FIFO Read Request Control. This bit field defines the FIFO threshold to assign DMA0 priority when requesting a PCI for a read operation. A value of 00_H indicates that DMA0 read request priority is set to 1 whenever the FIFO has greater than zero Dwords available space , while a value of 3F indicates that DMA0 read request priority is set to 1 whenever the FIFO has greater than 63 Dwords available space. This bit field is useful when two DMA channels are competing for accessing the PCI bus.

When the two DMA channels request the PCI bus at the same time, the one with the higher priority will have the bus when it's granted to the SiI 0680A. If the two DMA channels have the same priority, the channel that had the bus last will have the bus when it's granted to the SiI 0680A.

When one DMA channel is controlling the PCI bus, and the other channel requests the PCI bus, if the channel currently controlling the PCI bus has the same or higher priority, it remains controlling the bus. However, if the channel requesting the PCI bus has higher priority, the lower priority channel terminates the PCI transaction, yielding the bus to the channel with the higher priority.

9.7.12 FIFO Valid Byte Count and Control – IDE1

Address Offset: 44_H
Access Type: Read /Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								FIFO Valid Byte Count – IDE1								Reserved		FIFO Wr Req Ctrl – IDE1						Reserved		FIFO Rd Req Ctrl – IDE1					

This register defines the FIFO valid byte count register and PCI bus request control for IDE Channel #1 in the SiI 0680A. The register bits are defined below.

- **Bit [31:25]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [24:16]**: FIFO Valid Byte Count – IDE1 (R). This bit field provides the valid byte count for the data FIFO for IDE Channel #1. A value of 000_H indicates empty, while a value of 100_H indicates a full FIFO with 256 bytes.
- **Bit [15:14]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [13:08]**: FIFO Wr Req Ctrl – IDE1 (R/W) – FIFO Write Request Control. This bit field defines the FIFO threshold to assign DMA1 priority when requesting a PCI for a write operation. A value of 00_H indicates that DMA1 write request priority is set to 1 whenever the FIFO contains greater than zero DWords, while a value of $3F_H$ indicates that DMA1 write request priority is set to 1 whenever the FIFO contains greater than 63 Dwords. This bit field is useful when two DMA channels are competing for accessing PCI bus.

  When the two DMA channels request the PCI bus at the same time, the one with the higher priority will have the bus when it's granted to the SiI 0680A. If the two DMA channels have the same priority, the channel that had the bus last will have the bus when it's granted to the SiI 0680A.

  When one DMA channel is controlling the PCI bus, and the other channel requests the PCI bus, if the channel currently controlling the PCI bus has the same or higher priority, it remains controlling the bus. However, if the channel requesting the PCI bus has higher priority, the lower priority channel terminates the PCI transaction, yielding the bus to the channel with the higher priority.

- **Bit [07:06]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [05:00]**: FIFO Rd Req Ctrl – IDE1 (R/W) – FIFO Read Request Control. This bit field defines the FIFO threshold to assign DMA1 priority when requesting a PCI for a read operation. A value of 00_H indicates that DMA1 read request priority is set to 1 whenever the FIFO has greater than zero Dwords available space , while a value of 3F indicates that DMA1 read request priority is set to 1 whenever the FIFO has greater than 63 Dwords available space. This bit field is useful when two DMA channels are competing for accessing the PCI bus.

  When the two DMA channels request the PCI bus at the same time, the one with the higher priority will have the bus when it's granted to the SiI 0680A. If the two DMA channels have the same priority, the channel that had the bus last will have the bus when it's granted to the SiI 0680A.

  When one DMA channel is controlling the PCI bus, and the other channel requests the PCI bus, if the channel currently controlling the PCI bus has the same or higher priority, it remains controlling the bus. However, if the channel requesting the PCI bus has higher priority, the lower priority channel terminates the PCI transaction, yielding the bus to the channel with the higher priority.

9.7.13 System Configuration Status – Command

Address Offset: 48_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Int Block	IDE0 Int Block	IDE Clk Select		Reserved			BA5_EN	Reserved								IDE0 Module Rst	IDE1 Module Rst	FF0 Module Rst	FF1 Module Rst	Reserved		ARB Module Rst	PBM Module Rst

This register defines the system configuration status and command register for the SiI 0680A. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: IDE1 Int Block (R/W) – IDE1 Interrupt Block. This bit is set to block interrupts from the IDE Channel #1 to the PCI bus.
- **Bit [22]**: IDE0 Int Block (R/W) – IDE0 Interrupt Block. This bit is set to block interrupts from the IDE Channel #0 to the PCI bus.
- **Bit [21:20]**: IDE Clk Select (R/W) – IDE Clock Frequency Select. This bit field is used set the IDE clock frequency for both IDE modules: 00_B = 100 MHz; 01_B = 133 MHz; 10_B = PCI Clock x 2; and, 11_B = IDE Clock Disabled.
- **Bit [19:17]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [16]**: BA5_EN (R) – Base Address 5 Enable. This bit reflects input pin BA5_EN.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07]**: IDE0 Module Rst (R/W) – IDE0 Module Reset. This bit is set to reset the interface logic for the IDE Channel #0.
- **Bit [06]**: IDE1 Module Rst (R/W) – IDE1 Module Reset. This bit is set to reset the interface logic for the IDE Channel #1.
- **Bit [05]**: FF0 Module Rst (R/W) – FF0 Module Reset. This bit is set to reset the logic in the FIFO for IDE Channel #0.
- **Bit [04]**: FF1 Module Rst (R/W) – FF1 Module Reset. This bit is set to reset the logic in the FIFO for IDE Channel #1.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01]**: ARB Module Rst (R/W) – ARB Module Reset. This bit is set to reset the internal logic for the PCI-IDE arbiter.
- **Bit [00]**: PBM Module Rst (R/W) – PBM Module Reset. This bit is set to reset the internal logic for the PCI bus master state machine.

9.7.14 System Software Data Register

Address Offset: $4C_H$
Access Type: Read/Write
Reset Value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
System Software Data																															

This register is used by the software for non-resettable data storage. The contents are unknown on power-up and are never cleared by any type of reset.

9.7.15 FLASH Memory Address – Command + Status

Address Offset: 50_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved				Mem Init Done	Reserved	Mem Access Start	Mem Access Type	Reserved					Memory Address																		

This register defines the address and command/status register for FLASH memory interface in the SiI 0680A. The register bits are defined below.

- **Bit [31:28]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [27]**: Memory Init Done (R) – This bit set indicates that the memory initialization sequence is done. The memory sequence is activated upon the release of reset.
- **Bit [26]**: Reserved (R) – This bit is reserved and returns an indeterminate value on a read.
- **Bit [25]**: Mem Access Start (R/W) – Memory Access Start. This bit is set to initiate an operation to FLASH memory. This bit is cleared by the chip when the operation is complete.
- **Bit [24]**: Mem Access Type (R/W) – Memory Access Type. This bit is set to define a read operation from FLASH memory. This bit is cleared to define a write operation to FLASH memory.
- **Bit [23:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18:00]**: Memory Address (R/W). This bit field is programmed with the address for a FLASH memory read or write access.

9.7.16 FLASH Memory Data

Address Offset: 54_H
Access Type: Read/Write
Reset Value: 0x0000_0000

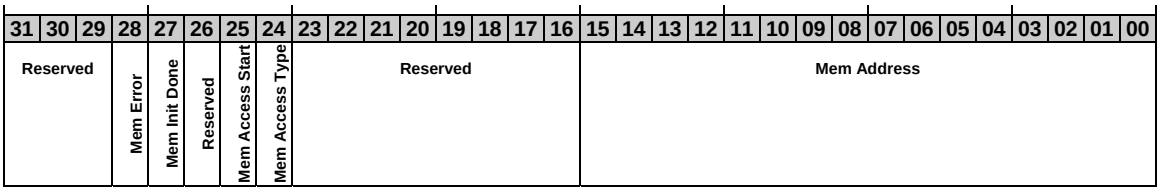
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Memory Data							

This register defines the data register for FLASH memory interface in the SiI 0680A. The system writes to this register for a write operation to FLASH memory, and reads from this register on a read operation from FLASH memory.

- **Bit [31:08]**: Reserved (R).
- **Bit [07:00]**: Memory Data (R/W) – FLASH Memory Data. This bit field is used for FLASH write data on a write operation, and returns the FLASH read data on a read operation.

9.7.17 EEPROM Memory Address – Command + Status

Address Offset: 58_H
Access Type: Read/Write
Reset Value: 0x0000_0000

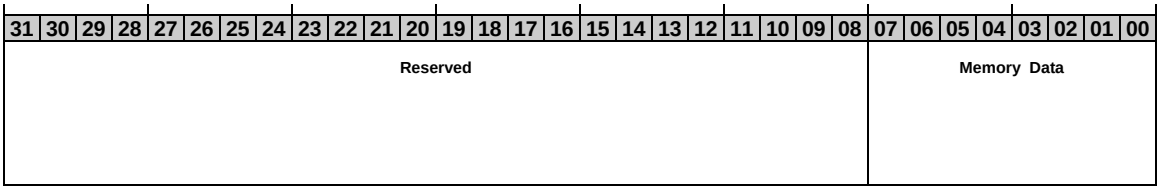


This register defines the address and command/status register for EEPROM memory interface in the SiI 0680A. The register bits are defined below.

- **Bit [31:29]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [28]**: Mem Error (R/W1C) – Memory Access Error. This bit set indicates that the EEPROM interface logic detects three NAKs from the memory device.
- **Bit [27]**: Mem Init Done (R) – Memory Initialization Done. This bit set indicates that the memory initialization sequence is done. The memory initialization sequence is activated upon the release of reset.
- **Bit [26]**: Reserved (R) This bit is reserved and returns an indeterminate value on a read.
- **Bit [25]**: Mem Access Start (R/W) – Memory Access Start. This bit is set to initiate an operation to EEPROM memory. This bit is cleared by the chip when the operation is complete.
- **Bit [24]**: Mem Access Type (R/W) – Memory Access Type. This bit is set to define a read operation from EEPROM memory. This bit is cleared to define a write operation to EEPROM memory.
- **Bit [23:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15:00]**: Memory Address (R/W). This bit field is programmed with the address for an EEPROM memory read or write access.

9.7.18 EEPROM Memory Data

Address Offset: $5C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the data register for EEPROM memory interface in the SiI 0680A. The system writes to this register for a write operation to EEPROM memory, and reads from this register on a read operation from EEPROM memory. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:00]**: Memory Data (R/W) – EEPROM Memory Data. This bit field is used for EEPROM write data on a write operation, and returns the EEPROM read data on a read operation.

9.7.19 FIFO Port – IDE0

Address Offset: 60_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Port – IDE0																															

This register defines the direct access register for the FIFO port of IDE Channel #0 in the SiI 0680A. This register is used for hardware debugging purposes only. The system can read from or write to this register for direct access to the data FIFO between the PCI bus and IDE Channel #0. While DMA0 is active, reading this register will be terminated with Target-Abort.

9.7.20 FIFO Pointers1– IDE0

Address Offset: 68_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 1 Wr Pointer – IDE0								FIFO Byte 1 Rd Pointer – IDE0								FIFO Byte 0 Wr Pointer – IDE0								FIFO Byte 0 Rd Pointer – IDE0							

This register provides visibility into the data FIFO for IDE Channel #0 in the SiI 0680A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 1 Wr Pointer – IDE0 (R) FIFO Byte 1 Write Pointer. This bit field provides the status on the write pointer for Byte 1.
- **Bit [23:16]**: FIFO Byte 1 Rd Pointer – IDE0 (R) FIFO Byte 1 Read Pointer. This bit field provides the status on the read pointer for Byte 1.
- **Bit [15:08]**: FIFO Byte 0 Wr Pointer – IDE0 (R) FIFO Byte 0 Write Pointer. This bit field provides the status on the write pointer for Byte 0.
- **Bit [07:00]**: FIFO Byte 0 Rd Pointer – IDE0 (R) FIFO Byte 0 Read Pointer. This bit field provides the status on the read pointer for Byte 0.

9.7.21 FIFO Pointers2– IDE0

Address Offset: $6C_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 3 Wr Pointer – IDE0								FIFO Byte 3 Rd Pointer – IDE0								FIFO Byte 2 Wr Pointer – IDE0								FIFO Byte 2 Rd Pointer – IDE0							

This register provides visibility into the data FIFO for IDE Channel #0 in the SiI 0680A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 3 Wr Pointer – IDE0 (R) FIFO Byte 3 Write Pointer. This bit field provides the status on the write pointer for Byte 3.
- **Bit [23:16]**: FIFO Byte 3 Rd Pointer – IDE0 (R) FIFO Byte 3 Read Pointer. This bit field provides the status on the read pointer for Byte 3.
- **Bit [15:08]**: FIFO Byte 2 Wr Pointer – IDE0 (R) FIFO Byte 2 Write Pointer. This bit field provides the status on the write pointer for Byte 2.
- **Bit [07:00]**: FIFO Byte 2 Rd Pointer – IDE0 (R) FIFO Byte 2 Read Pointer. This bit field provides the status on the read pointer for Byte 2.

9.7.22 FIFO Port – IDE1

Address Offset: 70_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Port – IDE1																															

This register defines the direct access register for the FIFO port of IDE Channel #1 in the SiI 0680A. This register is used for hardware debugging purposes only. The system can read from or write to this register for direct access to the data FIFO between the PCI bus and IDE Channel #1. While DMA1 is active, reading this register will be terminated with Target-Abort.

9.7.23 FIFO Pointers1– IDE1

Address Offset: 78_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 1 Wr Pointer – IDE1								FIFO Byte 1 Rd Pointer – IDE1								FIFO Byte 0 Wr Pointer – IDE1								FIFO Byte 0 Rd Pointer – IDE1							

This register provides visibility into the data FIFO for IDE Channel #1 in the SiI 0680A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 1 Wr Pointer – IDE1 (R) FIFO Byte 1 Write Pointer. This bit field provides the status on the write pointer for Byte 1.
- **Bit [23:16]**: FIFO Byte 1 Rd Pointer – IDE1 (R) FIFO Byte 1 Read Pointer. This bit field provides the status on the read pointer for Byte 1.
- **Bit [15:08]**: FIFO Byte 0 Wr Pointer – IDE1 (R) FIFO Byte 0 Write Pointer. This bit field provides the status on the write pointer for Byte 0.
- **Bit [07:00]**: FIFO Byte 0 Rd Pointer – IDE1 (R) FIFO Byte 0 Read Pointer. This bit field provides the status on the read pointer for Byte 0.

9.7.24 FIFO Pointers2– IDE1

Address Offset: $7C_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 3 Wr Pointer – IDE1								FIFO Byte 3 Rd Pointer – IDE1								FIFO Byte 2 Wr Pointer – IDE1								FIFO Byte 2 Rd Pointer – IDE1							

This register provides visibility into the data FIFO for IDE Channel #1 in the SiI 0680A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 3 Wr Pointer – IDE1 (R) FIFO Byte 3 Write Pointer. This bit field provides the status on the write pointer for Byte 3.
- **Bit [23:16]**: FIFO Byte 3 Rd Pointer – IDE1 (R) FIFO Byte 3 Read Pointer. This bit field provides the status on the read pointer for Byte 3.
- **Bit [15:08]**: FIFO Byte 2 Wr Pointer – IDE1 (R) FIFO Byte 2 Write Pointer. This bit field provides the status on the write pointer for Byte 2.
- **Bit [07:00]**: FIFO Byte 2 Rd Pointer – IDE1 (R) FIFO Byte 2 Read Pointer. This bit field provides the status on the read pointer for Byte 2.

9.7.25 IDE0 Task File Register 0

Address Offset: 80_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Starting Sector Number								IDE0 Task File Sector Count								IDE0 Task File Features (W) IDE0 Task File Error (R)								IDE0 Task File Data							

This register defines one of the IDE Channel #0 Task File registers in the SiI 0680A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE0 Task File Data (R/W). This bit field defines the IDE0 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 0 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE0 Task File Starting Sector Number (R/W). This bit field defines the IDE0 Task File Starting Sector Number register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [23:16]**: IDE0 Task File Sector Count (R/W). This bit field defines the IDE0 Task File Sector Count register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE0 Task File Features (W). This write-only bit field defines the IDE0 Task File Features register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE0 Task File Error (R). This read-only bit field defines the IDE0 Task File Error register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.

9.7.26 IDE0 Task File Register 1

Address Offset: 84_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Command + Status								IDE0 Task File Device+Head								IDE0 Task File Cylinder High								IDE0 Task File Cylinder Low							

This register defines one of the IDE Channel #0 Task File registers in the SiI 0680A. Access to these bit field is permitted if the PCI bus Byte Enable is active for one byte only.

The register bits are defined below.

- **Bit [31:24]**: IDE0 Task File Command (W). This write-only bit field defines the IDE0 Task File Command register.
- **Bit [31:24]**: IDE0 Task File Status (R). This read-only bit field defines the IDE0 Task File Status register.
- **Bit [23:16]**: IDE0 Task File Device+Head (R/W). This bit field defines the IDE0 Task File Device and Head register.
- **Bit [15:08]**: IDE0 Task File Cylinder High (R/W). This bit field defines the IDE0 Task File Cylinder High register.
- **Bit [07:00]**: IDE0 Task File Cylinder Low (R/W). This bit field defines the IDE0 Task File Cylinder Low register.

9.7.27 IDE0 Task File Register 2

Address Offset: 88_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE0 Task File Device Control IDE0 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #0 Task File registers in the SiI 0680A. Access to these bit fields is permitted if the PCI bus Byte Enable is active for one byte only.

The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23:16]**: IDE0 Task File Device Control (W). This bit field defines the IDE0 Task File Device Control register.
- **Bit [23:16]**: IDE0 Task File Auxiliary Status (R). This bit field defines the IDE0 Task File Auxiliary Status register.
- **Bit [15:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

9.7.28 IDE0 Read Ahead Data

Address Offset: $8C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Read Ahead Data																															

This register defines the read ahead data port for PIO transfers on IDE Channel #0 in the SiI 0680A. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned.

9.7.29 IDE0 Task File Register 0 – Command Buffering

Address Offset: 90_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
IDE0 Task File Starting Sector Number	IDE0 Task File Sector Count	IDE0 Task File Features (W) IDE0 Task File Error (R)	IDE0 Task File Data

This register defines one of the IDE Channel #0 Task File registers used for Command Buffered accesses in the SiI 0680A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE0 Task File Data (R/W). This bit field defines the IDE0 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 0 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE0 Task File Starting Sector Number (R/W). This bit field defines the IDE0 Task File Starting Sector Number register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 3 is active.
- **Bit [23:16]**: IDE0 Task File Sector Count (R/W). This bit field defines the IDE0 Task File Sector Count register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 2 is active.
- **Bit [15:08]**: IDE0 Task File Features (W). This write-only bit field defines the IDE0 Task File Features register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.
- **Bit [15:08]**: IDE0 Task File Error (R). This read-only bit field defines the IDE0 Task File Error register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.

9.7.30 IDE0 Task File Register 1 – Command Buffering

Address Offset: 94_H
Access Type: Read/Write
Reset Value: 0x0000_0000

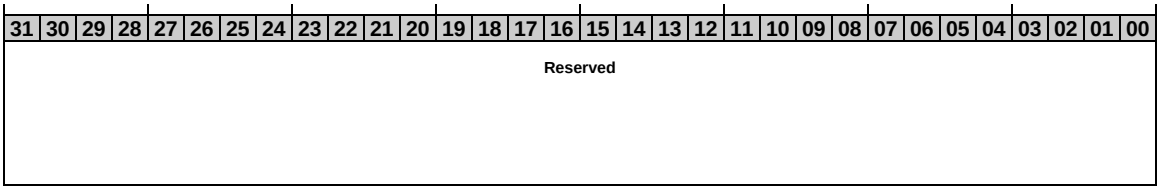
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00
IDE0 Task File Command + Status	IDE0 Task File Device+Head	IDE0 Task File Cylinder High	IDE0 Task File Cylinder Low

This register defines one of the IDE Channel #0 Task File registers used for Command Buffered accesses in the SiI 0680A. The register bits are defined below.

- **Bit [31:24]**: IDE0 Task File Command (W). This write-only bit field defines the IDE0 Task File Command register.
- **Bit [31:24]**: IDE0 Task File Status (R). This read-only bit field defines the IDE0 Task File Status register.
- **Bit [23:16]**: IDE0 Task File Device+Head (R/W). This bit field defines the IDE0 Task File Device and Head register.
- **Bit [15:08]**: IDE0 Task File Cylinder High (R/W). This bit field defines the IDE0 Task File Cylinder High register.
- **Bit [07:00]**: IDE0 Task File Cylinder Low (R/W). This bit field defines the IDE0 Task File Cylinder Low register.

9.7.31 IDE0 UDMA Control

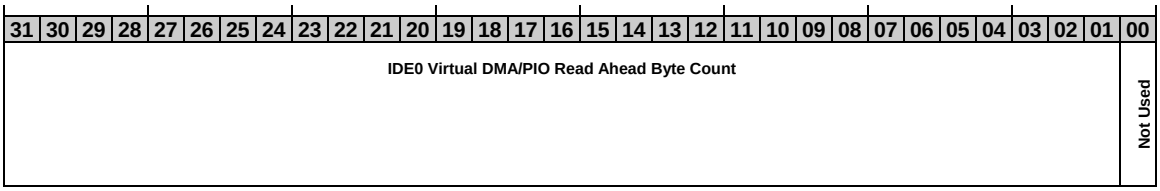
Address Offset: 98_H
Access Type: Read Only
Reset Value: 0x0000_0000



- This bit field is reserved and returns an indeterminate value on a read.

9.7.32 IDE0 Virtual DMA/PIO Read Ahead Byte Count

Address Offset: $9C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the read ahead byte count register for Virtual DMA and PIO Read Ahead transfers on IDE Channel #0 in the SiI 0680A. In Virtual DMA mode (PCI bus master DMA with PIO transfers on the IDE), all 32 bits are used as the word-aligned byte count. In PIO Read Ahead mode, only the lower 16 bits are used as the word-aligned byte count. The higher 16 bits must be programmed 0x0000.

9.7.33 IDE0 Task File Timing + Configuration + Status

Address Offset: $A0_H$
Access Type: Read/Write
Reset Value: 0x6515_0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Addr Setup Count				Active Count						Recovery Count						Reserved	Watchdog Int Ena	Watchdog Ena	Watchdog Timeout	Interrupt Status	Virtual DMA Int	IORDY Monitoring	Reserved	Reserved				Channel Tri-State	Channel Rst	Buffered Cmd	Cable 80

This register defines the task file timing register for IDE Channel #0 in the SiI 0680A. The register bits are defined below.

- **Bit [31:28]**: Addr Setup Count (R/W) – IDE0 Address Setup Time Count. This bit field is used for adjusting the address setup time relative to IDE0_DIOR_N and IDE0_DIOW_N. See Chapter 11 for details on programming the timing register.
- **Bit [27:22]**: Active Count (R/W) – IDE0 DIOR_N and DIOW_N Active Time Count. This bit field is used for adjusting the active time of IDE0_DIOR_N and IDE0_DIOW_N. See Chapter 11 for details on programming this timing register.
- **Bit [21:16]**: Recovery Count (R/W) – IDE0 DIOR_N and DIOW_N Recovery Time Count. This bit field is used for adjusting the recovery time of IDE0_DIOR_N and IDE0_DIOW_N. See Chapter 11 for details on programming this timing register.
- **Bit [15]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [14]** : Watchdog Int Ena (R/W) – IDE0 Watchdog Interrupt Enable. This bit is set to enable Interrupt when Watchdog timer expired.
- **Bit [13]**: Watchdog Ena (R/W) – IDE0 Watchdog Timer Enable. This bit is set to enable the watchdog timer for IDE0. This bit is cleared to disable the watchdog timer.
- **Bit [12]**: Watchdog Timeout (R/W1C) – IDE0 Watchdog Timer Timeout. This bit set indicates that the watchdog timer for IDE0 timed out. When enabled, and IORDY monitoring bit is also enabled, during IDE0 PIO opeartion, the watchdog counter starts counting when IORDY signal is deasserted. If after 256 PCI clocks cycles, the IORDY signal is still deasserted, the Watchdog Timer is expires, and this bit is set and the SiI 0680A continue its operation and stop monitoring IORDY signal. Software writes one to clear this bit. Once this bit is cleared, the SiI 0680A starts monitoring IORDY on channel 0 again.
- **Bit [11]**: Interrupt Status (R) – IDE0 Interrupt Status. This bit set indicates that an interrupt is pending on IDE0. This bit provides real-time status of the IDE0 interrupt pin.
- **Bit [10]**: Virtual DMA Int (R) – IDE0 Virtual DMA Completion Interrupt. This bit set indicates that the Virtual DMA data transfer has completed. This bit is cleared when bit[0] PBM enable in PCI Bus Master – IDE0 is cleared .
- **Bit [09]**: IORDY Monitoring (R/W) – IDE0 IORDY Monitoring. When this bit is set, IORDY line is monitored for Task File accesses on channel 0.
- **Bit [08:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: Channel Tri-State (R/W) – IDE0 Channel Tri-State. This bit is set to tri-state the IDE Channel #0 bus. This bit is cleared for normal operations.
- **Bit [02]**: Channel Rst (R/W) – IDE0 Channel Reset. When this bit is set, IDE Channel #0 RST signal is asserted.
- **Bit [01]**: Buffered Cmd (R) – IDE0 Buffered Command Active. This bit set indicates that a Buffered Command is currently active. This bit is set when the first command byte is written to the command buffer. This bit is cleared when all of the task file bytes, including the command byte, have been written to the device.
- **Bit [00]**: Cable 80 (R) – IDE0 Cable 80 Detection. This bit provides real-time status of the inverted version of the IDE0_CBLID_N pin. When set, it indicates that 80 pin cable is detected.

9.7.34 IDE0 PIO Timing

Address Offset: $A4_H$
Access Type: Read/Write
Reset Value: 0x62DD_62DD

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Addr Setup Count				Device 1 Active Count						Device 1 Recovery Count						Device 0 Addr Setup Count				Device 0 Active Count						Device 0 Recovery Count			

This register defines the PIO timing register for IDE Channel #0 in the SiI 0680A. See chapter 11 for details on programming this timing register. The register bits are defined below.

- **Bit [31:28]**: Device 1 Addr Setup Count (R/W) – IDE0 Device 1 Address Setup Time Count for PIO Mode. This bit field is used for programming the address setup time relative to IDE0_DIOR_N and IDE0_DIOW_N in PIO mode.
- **Bit [27:22]**: Device 1 Active Count (R/W) – IDE0 Device 1 DIOR_N and DIOW_N Active Time Count for PIO Mode. This bit field is used for programming the active time of IDE0_DIOR_N and IDE0_DIOW_N in PIO mode.
- **Bit [21:16]**: Device 1 Recovery Count (R/W) – IDE0 Device 1 DIOR_N and DIOW_N Recovery Time Count for PIO Mode. This bit field is used for programming the recovery time of IDE0_DIOR_N and IDE0_DIOW_N in PIO mode.
- **Bit [15:12]**: Device 0 Addr Setup Count (R/W) – IDE0 Device 0 Address Setup Time Count for PIO Mode. This bit field is used for programming the address setup time relative to IDE0_DIOR_N and IDE0_DIOW_N in PIO mode
- **Bit [11:06]**: Device 0 Active Count (R/W) – IDE0 Device 0 DIOR_N and DIOW_N Active Time Count for PIO Mode. This bit field is used for programming the active time of IDE0_DIOR_N and IDE0_DIOW_N in PIO mode.
- **Bit [05:00]**: Device 0 Recovery Count (R/W) – IDE0 Device 0 DIOR_N and DIOW_N Recovery Time Count for PIO Mode. This bit field is used for programming the recovery time of IDE0_DIOR_N and IDE0_DIOW_N in PIO mode.

9.7.35 IDE0 DMA Timing

Address Offset: $A8_H$
Access Type: Read/Write
Reset Value: 0x4392_4392

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Addr Setup Count				Device 1 Active Count						Device 1 Recovery Count						Device 0 Addr Setup Count				Device 0 Active Count						Device 0 Recovery Count			

This register defines the DMA timing register for IDE Channel #0 in the SiI 0680A. See chapter 13 for details on programming this timing register. The register bits are defined below.

- **Bit [31:28]**: Device 1 Addr Setup Count (R/W) – IDE0 Device 1 Address Setup Time Count for DMA Mode. This bit field is used for programming the address setup time relative to IDE0_DIOR_N and IDE0_DIOW_N in DMA mode.
- **Bit [27:22]**: Device 1 Active Count (R/W) – IDE0 Device 1 DIOR_N and DIOW_N Active Time Count for DMA Mode. This bit field is used for programming the active time of IDE0_DIOR_N and IDE0_DIOW_N in DMA mode.
- **Bit [21:16]**: Device 1 Recovery Count (R/W) – IDE0 Device 1 DIOR_N and DIOW_N Recovery Time Count for DMA Mode. This bit field is used for programming the recovery time of IDE0_DIOR_N and IDE0_DIOW_N in DMA mode.
- **Bit [15:12]**: Device 0 Addr Setup Count (R/W) – IDE0 Device 0 Address Setup Time Count for DMA Mode. This bit field is used for programming the address setup time relative to IDE0_DIOR_N and IDE0_DIOW_N in DMA mode.
- **Bit [11:06]**: Device 0 Active Count (R/W) – IDE0 Device 0 DIOR_N and DIOW_N Active Time Count for DMA Mode. This bit field is used for programming the active time of IDE0_DIOR_N and IDE0_DIOW_N in DMA mode.
- **Bit [05:00]**: Device 0 Recovery Count (R/W) – IDE0 Device 0 DIOR_N and DIOW_N Recovery Time Count for DMA Mode. This bit field is used for programming the recovery time of IDE0_DIOR_N and IDE0_DIOW_N in DMA mode.

9.7.36 IDE0 UDMA Timing

Address Offset: AC_H
Access Type: Read/Write
Reset Value: 0x4009_4009

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Data Input Delay				Device 1 DSTROBE Delay				Device 1 HSTROBE Delay				Reserved				Device 1 Cycle Time Count															
Device 0 Data Input Delay				Device 0 DSTROBE Delay				Device 0 HSTROBE Delay				Reserved				Device 0 Cycle Time Count															

This register defines the UDMA timing register for IDE Channel #0 in the SiI 0680A. See chapter 11 for details on programming this timing register. The register bits are defined below.

- **Bit [31:30]**: Device 1 Data Input Delay (R/W) – IDE0 Device 1 Data Input Delay for UDMA Mode. This bit field is used for programming the data input delay in increments of 2 nsec in UDMA mode.
- **Bit [29:28]**: Device 1 DSTROBE Delay (R/W) – IDE0 Device 1 DSTROBE Delay for UDMA Mode. This bit field is used for programming the DSTROBE output delay in increments of 2 nsec in UDMA mode.
- **Bit [27:25]**: Device 1 HSTROBE Delay (R/W) – IDE0 Device 1 HSTROBE Delay for UDMA Mode. This bit field is used for programming the HSTROBE output delay in increments of 2 nsec in UDMA mode.
- **Bit [24:23]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [22]**: Reserved (R/W) – This bit field is reserved.
- **Bit [21:16]**: Device 1 Cycle Time Count (R/W) – IDE0 Device 1 UDMA Cycle Time Count. This bit field is used for programming the UDMA Active and Recovery Time.
- **Bit [15:14]**: Device 0 Data Input Delay (R/W) – IDE0 Device 0 Data Input Delay for UDMA Mode. This bit field is used for programming the data input delay in increments of 2 nsec in UDMA mode.
- **Bit [13:12]**: Device 0 DSTROBE Delay (R/W) – IDE0 Device 0 DSTROBE Delay for UDMA Mode. This bit field is used for programming the DSTROBE output delay in increments of 2 nsec in UDMA mode
- **Bit [11:09]**: Device 0 HSTROBE Delay (R/W) – IDE0 Device 0 HSTROBE Delay for UDMA Mode. This bit field is used for programming the HSTROBE output delay in increments of 2 nsec in UDMA mode.
- **Bit [08:07]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [06]**: Reserved (R/W) – This bit field is reserved.
- **Bit [05:00]**: Device 0 Cycle Time Count (R/W) – IDE0 Device 0 UDMA Cycle Time Count. This bit field is used for programming the UDMA Active and Recovery Time

9.7.37 Test Register – IDE0

Address Offset: $B0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Module Select				Nibble Select				Sub-Module Select								Data Field															

This register defines the test register for IDE Channel #0 in the SiI 0680A. This register is for chip-level simulation and verification purposes only. The register bits are defined below.

- **Bit [31:28]**: Module Select (R/W) – IDE0 Test Module Select. This bit field is used to select the logic module for testing: 0001_B = DIF module; 0010_B = TMR module; 0011_B = PIF module; and, 0100_B = DUW module.
- **Bit [27:24]**: Nibble Select (R/W) – IDE0 Test Control Nibble Select. This bit field is used to select the control nibble for testing. A value of 0001_B selects the least significant nibble, while a value of 1000_B selects the most significant nibble.
- **Bit [23:16]**: Sub-Module Select (R/W) – IDE0 Test Sub-Module Select. This bit field is used to select the logic sub-module for testing. The valid selections are listed below.

Module Select	Sub-Module Select	Description
0001_B	0001_B	FIFO Data
0010_B	0001_B	Timer 1
0010_B	0010_B	Timer 2
0010_B	0011_B	Timer 3
0010_B	0100_B	Timer 4
0011_B	0001_B	PBM_BYTE_CNT
0011_B	0010_B	WD_TMO
0100_B	0001_B	DUW_TMR_CNT

Table 9-10: IDE0 Test Register Selections

- **Bit [15:00]**: Data Field (R/W) – IDE0 Test Data Field. This bit field is used to write a preload value to the selected counter or read the current value of the selected counter.

9.7.38 Data Transfer Mode – IDE0

Address Offset: $B4_H$
Access Type: Read/Write
Reset Value: 0x0000_0022

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Reserved		IDE0 Device 1 Transfer Mode		Reserved		IDE0 Device 0 Transfer Mode	

This register defines the transfer mode register for IDE Channel #0 in the SiI 0680A. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:06]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [05:04]**: Device 1 Transfer Mode (R/W) – IDE0 Device 1 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B = PIO transfer with IORDY not monitored; 01_B = PIO transfer with IORDY monitored; 10_B = normal DMA; and, 11_B = Ultra DMA.
  When this bit field is set to value other than 00_B, SiI 0680A will monitor IORDY for normal PIO transfer.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: Device 0 Transfer Mode (R/W) – IDE0 Device 0 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B = PIO transfer with IORDY not monitored; 01_B = PIO transfer with IORDY monitored; 10_B = normal DMA; and, 11_B = Ultra DMA.

  When this bit field is set to value other than 00_B, SiI 0680A will monitor IORDY for normal PIO transfer.

9.7.39 IDE1 Task File Register 0

Address Offset: $C0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Starting Sector Number								IDE1 Task File Sector Count								IDE1 Task File Features (W) IDE1 Task File Error (R)								IDE1 Task File Data							

This register defines one of the IDE Channel #1 Task File registers in the SiI 0680A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE1 Task File Data (R/W). This bit field defines the IDE1 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 0 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE1 Task File Starting Sector Number (R/W). This bit field defines the IDE1 Task File Starting Sector Number register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [23:16]**: IDE1 Task File Sector Count (R/W). This bit field defines the IDE1 Task File Sector Count register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE1 Task File Features (W). This write-only bit field defines the IDE1 Task File Features register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE1 Task File Error (R). This read-only bit field defines the IDE1 Task File Error register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.

9.7.40 IDE1 Task File Register 1

Address Offset: $C4_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Command + Status								IDE1 Task File Device+Head								IDE1 Task File Cylinder High								IDE1 Task File Cylinder Low							

This register defines one of the IDE Channel #1 Task File registers in the SiI 0680A. Access to these bit fields is permitted if the PCI bus Byte Enable is active for one byte only. The register bits are defined below.

- **Bit [31:24]**: IDE1 Task File Command (W). This write-only bit field defines the IDE1 Task File Command register.
- **Bit [31:24]**: IDE1 Task File Status (R). This read-only bit field defines the IDE1 Task File Status register.
- **Bit [23:16]**: IDE1 Task File Device+Head (R/W). This bit field defines the IDE1 Task File Device and Head register.
- **Bit [15:08]**: IDE1 Task File Cylinder High (R/W). This bit field defines the IDE1 Task File Cylinder High register.
- **Bit [07:00]**: IDE1 Task File Cylinder Low (R/W). This bit field defines the IDE1 Task File Cylinder Low register.

9.7.41 IDE1 Task File Register 2

Address Offset: $C8_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Task File Device Control IDE1 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #1 Task File registers in the SiI 0680A. Access to these bit fields is permitted if the PCI bus Byte Enable is active for one byte only. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23:16]**: IDE1 Task File Device Control (W). This bit field defines the IDE1 Task File Device Control register.
- **Bit [23:16]**: IDE1 Task File Auxiliary Status (R). This bit field defines the IDE1 Task File Auxiliary Status register.
- **Bit [15:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

9.7.42 IDE1 Read/Write Ahead Data

Address Offset: CC_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Read Ahead Data																															

This register defines the read ahead data port for PIO transfers on IDE Channel #1 in the SiI 0680A.

This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus byte enables. The data written to this register must be zero-aligned.

9.7.43 IDE1 Task File Register 0 – Command Buffering

Address Offset: $D0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Starting Sector Number								IDE1 Task File Sector Count								IDE1 Task File Features (W) IDE1 Task File Error (R)								IDE1 Task File Data							

This register defines one of the IDE Channel #1 Task File registers used for Command Buffered accesses in the SiI 0680A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE1 Task File Data (R/W). This bit field defines the IDE1 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus byte enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 3 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE1 Task File Starting Sector Number (R/W). This bit field defines the IDE1 Task File Starting Sector Number register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 3 is active.
- **Bit [23:16]**: IDE1 Task File Sector Count (R/W). This bit field defines the IDE1 Task File Sector Count register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 2 is active.
- **Bit [15:08]**: IDE1 Task File Features (W). This write-only bit field defines the IDE1 Task File Features register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.
- **Bit [15:08]**: IDE1 Task File Error (R). This read-only bit field defines the IDE1 Task File Error register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.

9.7.44 IDE1 Task File Register 1 – Command Buffering

Address Offset: $D4_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Command + Status								IDE1 Task File Device+Head								IDE1 Task File Cylinder High								IDE1 Task File Cylinder Low							

This register defines one of the IDE Channel #1 Task File registers used for Command Buffered accesses in the SiI 0680A. The register bits are defined below.

- **Bit [31:24]**: IDE1 Task File Command (W). This write-only bit field defines the IDE1 Task File Command register.
- **Bit [31:24]**: IDE1 Task File Status (R). This read-only bit field defines the IDE1 Task File Status register.
- **Bit [23:16]**: IDE1 Task File Device+Head (R/W). This bit field defines the IDE1 Task File Device and Head register.
- **Bit [15:08]**: IDE1 Task File Cylinder High (R/W). This bit field defines the IDE1 Task File Cylinder High register.
- **Bit [07:00]**: IDE1 Task File Cylinder Low (R/W). This bit field defines the IDE1 Task File Cylinder Low register.

9.7.45 Rserved Register

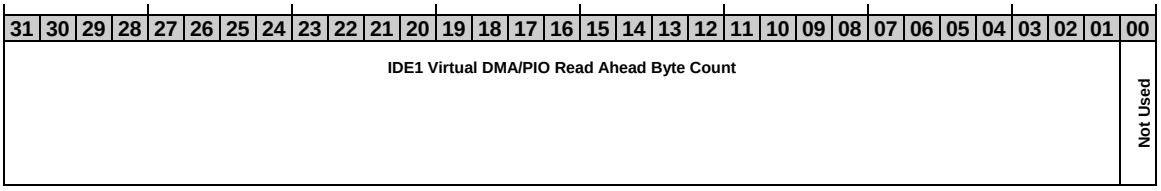
Address Offset: $D8_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																															

- This bit field is reserved and returns an indeterminate value on a read.

9.7.46 IDE1 Virtual DMA/PIO Read Ahead Byte Count

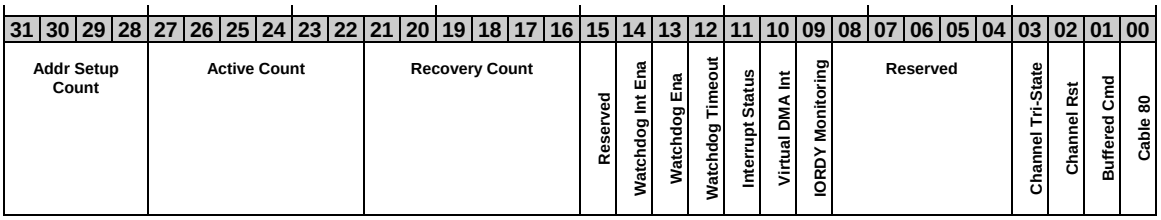
Address Offset: DC_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the read ahead byte count register for Virtual DMA and PIO Read Ahead transfers on IDE Channel #1 in the SiI 0680A. In Virtual DMA mode (PCI bus master DMA with PIO transfers on the IDE), all 32 bits are used as the word-aligned byte count. In PIO Read Ahead mode, only the lower 16 bits are used as the word-aligned byte count. The higher 16 bits must be programmed 0x0000.

9.7.47 IDE1 Task File Timing + Configuration + Status

Address Offset: $E0_H$
Access Type: Read/Write
Reset Value: 0x6515_0100



This register defines the task file timing register for IDE Channel #1 in the SiI 0680A. See chapter 11 for details on programming this timing register. The register bits are defined below.

- **Bit [31:28]**: Addr Setup Count (R/W) – IDE1 Address Setup Time Count. This bit field is used for programming the address setup time relative to IDE1_DIOR_N and IDE1_DIOW_N.
- **Bit [27:22]**: Active Count (R/W) – IDE1 DIOR_N and DIOW_N Active Time Count. This bit field is used for programming the active time of IDE1_DIOR_N and IDE1_DIOW_N.
- **Bit [21:16]**: Recovery Count (R/W) – IDE1 DIOR_N and DIOW_N Recovery Time Count. This bit field is used for programming the recovery time of IDE1_DIOR_N and IDE1_DIOW_N.
- **Bit [15]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [14]** : Watchdog Int Ena (R/W) – IDE1 Watchdog Interrupt Enable. This bit is set to enable Interrupt when Watchdog timer expired.
- **Bit [13]**: Watchdog Ena (R/W) – IDE1 Watchdog Timer Enable. This bit is set to enable the watchdog timer for IDE1. This bit is cleared to disable the watchdog timer.
- **Bit [12]**: Watchdog Timeout (R) – IDE1 Watchdog Timer Timeout. This bit set indicates that the watchdog timer for IDE1 timed out. When enabled, and IORDY monitoring bit is also enabled, during IDE0 PIO opeartion, the watchdog counter starts counting when IORDY signal is deasserted. If after 256 PCI clocks cycles, the IORDY signal is still deasserted, the Watchdog Timer is expires, and this bit is set and the SiI 0680A continue its operation and stop monitoring IORDY signal. Software writes one to clear this bit. Once this bit is cleared, the SiI 0680A starts monitoring IORDY on channel 1 again.
- **Bit [11]**: Interrupt Status (R) – IDE1 Interrupt Status. This bit set indicates that an interrupt is pending on IDE1. This bit provides real-time status of the IDE1 interrupt pin.
- **Bit [10]**: Virtual DMA Int (R) – IDE1 Virtual DMA Completion Interrupt. This bit set indicates that the Virtual DMA data transfer has completed. This bit is cleared when bit[0] PBM enable in PCI Bus Master – IDE1 is cleared .
- **Bit [09]**: IORDY Monitoring (R/W) – IDE1 IORDY Monitoring. When this bit is set, IORDY line is monitored for Task File accesses on channel 1.
- **Bit [08:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: Channel Tri-State (R/W) – IDE1 Channel Tri-State. This bit is set to tri-state the IDE Channel #1 bus. This bit is cleared for normal operations.
- **Bit [02]**: Channel Rst (R/W) – IDE1 Channel Reset. When this bit is set, IDE Channel # 1 RST signal is asserted.

- **Bit [01]**: Buffered Cmd (R) – IDE1 Buffered Command Active. This bit set indicates that a Buffered Command is currently active. This bit is set when the first command byte is written to the comand buffer. This bit is cleared when all of the task file bytes, including the command byte, have been written to the device.
- **Bit [00]**: Cable 80 (R) – IDE1 Cable 80 Detection. This bit provides real-time status of the inverted version of the IDE1_CBLID_N pin. When set, it indicates that 80 pin cable is detected.

9.7.48 IDE1 PIO Timing

Address Offset: $E4_H$
Access Type: Read/Write
Reset Value: 0x62DD_62DD

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
Device 1 Addr Setup Count	Device 1 Active Count	Device 1 Recovery Count		Device 0 Addr Setup Count	Device 0 Active Count		Device 0 Recovery Count

This register defines the PIO timing register for IDE Channel #1 in the SiI 0680A. See chapter 11 for details on programming this timing register. The register bits are defined below.

- **Bit [31:28]**: Device 1 Addr Setup Count (R/W) – IDE1 Device 1 Address Setup Time Count for PIO Mode. This bit field is used for programming the address setup time relative to IDE1_DIOR_N and IDE1_DIOW_N in PIO mode.
- **Bit [27:22]**: Device 1 Active Count (R/W) – IDE1 Device 1 DIOR_N and DIOW_N Active Time Count for PIO Mode. This bit field is used for programming the active time of IDE1_DIOR_N and IDE1_DIOW_N in PIO mode.
- **Bit [21:16]**: Device 1 Recovery Count (R/W) – IDE1 Device 1 DIOR_N and DIOW_N Recovery Time Count for PIO Mode. This bit field is used for programming the recovery time of IDE1_DIOR_N and IDE1_DIOW_N in PIO mode.
- **Bit [15:12]**: Device 0 Addr Setup Count (R/W) – IDE1 Device 0 Address Setup Time Count for PIO Mode. This bit field is used for programming the address setup time relative to IDE1_DIOR_N and IDE1_DIOW_N in PIO mode.
- **Bit [11:06]**: Device 0 Active Count (R/W) – IDE1 Device 0 DIOR_N and DIOW_N Active Time Count for PIO Mode. This bit field is used for programming the active time of IDE1_DIOR_N and IDE1_DIOW_N in PIO mode.
- **Bit [05:00]**: Device 0 Recovery Count (R/W) – IDE1 Device 0 DIOR_N and DIOW_N Recovery Time Count for PIO Mode. This bit field is used for programming the recovery time of IDE1_DIOR_N and IDE1_DIOW_N in PIO mode.

9.7.49 IDE1 DMA Timing

Address Offset: $E8_H$
Access Type: Read/Write
Reset Value: 0x4392_4392

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Addr Setup Count				Device 1 Active Count						Device 1 Recovery Count						Device 0 Addr Setup Count				Device 0 Active Count						Device 0 Recovery Count			

This register defines the DMA timing register for IDE Channel #1 in the SiI 0680A. See chapter 11 for details on programming this timing register. The register bits are defined below.

- **Bit [31:28]**: Device 1 Addr Setup Count (R/W) – IDE1 Device 1 Address Setup Time Count for DMA Mode. This bit field is used for programming the address setup time relative to IDE1_DIOR_N and IDE1_DIOW_N in DMA mode.
- **Bit [27:22]**: Device 1 Active Count (R/W) – IDE1 Device 1 DIOR_N and DIOW_N Active Time Count for DMA Mode. This bit field is used for programming the active time of IDE1_DIOR_N and IDE1_DIOW_N in DMA mode.
- **Bit [21:16]**: Device 1 Recovery Count (R/W) – IDE1 Device 1 DIOR_N and DIOW_N Recovery Time Count for DMA Mode. This bit field is used for programming the recovery time of IDE1_DIOR_N and IDE1_DIOW_N in DMA mode.
- **Bit [15:12]**: Device 0 Addr Setup Count (R/W) – IDE1 Device 0 Address Setup Time Count for DMA Mode. This bit field is used for programming the address setup time relative to IDE1_DIOR_N and IDE1_DIOW_N in DMA mode.
- **Bit [11:06]**: Device 0 Active Count (R/W) – IDE1 Device 0 DIOR_N and DIOW_N Active Time Count for DMA Mode. This bit field is used for programming the active time of IDE1_DIOR_N and IDE1_DIOW_N in DMA mode.
- **Bit [05:00]**: Device 0 Recovery Count (R/W) – IDE1 Device 0 DIOR_N and DIOW_N Recovery Time Count for DMA Mode. This bit field is used for programming the recovery time of IDE1_DIOR_N and IDE1_DIOW_N in DMA mode.

9.7.50 IDE1 UDMA Timing

Address Offset: EC_H
Access Type: Read/Write
Reset Value: 0x4009_4009

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device 1 Data Input Delay		Device 1 DSTROBE Delay		Device 1 HSTROBE Delay			Reserved			Device 1 Cycle Time Count						Device 0 Data Input Delay		Device 0 DSTROBE Delay		Device 0 HSTROBE Delay			Reserved			Device 0 Cycle Time Count			

This register defines the UDMA timing register for IDE Channel #1 in the SiI 0680A. See chapter 11 for details on programming this timing register. The register bits are defined below.

- **Bit [31:30]**: Device 1 Data Input Delay (R/W) – IDE1 Device 1 Data Input Delay for UDMA Mode. This bit field is used for programming the data input delay in increments of 2 nsec in UDMA mode.
- **Bit [29:28]**: Device 1 DSTROBE Delay (R/W) – IDE1 Device 1 DSTROBE Delay for UDMA Mode. This bit field is used for programming the DSTROBE output delay in increments of 2 nsec in UDMA mode.
- **Bit [27:25]**: Device 1 HSTROBE Delay (R/W) – IDE1 Device 1 HSTROBE Delay for UDMA Mode. This bit field is used for programming the HSTROBE output delay in increments of 2 nsec in UDMA mode.
- **Bit [24:23]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [22]**: Reserved (R/W) – This bit field is reserved.
- **Bit [21:16]**: Device 1 Cycle Time Count (R/W) – IDE1 Device 1 UDMA Cycle Time Count. This bit field is used for programming the UDMA Active and Recovery Time.
- **Bit [15:14]**: Device 0 Data Input Delay (R/W) – IDE1 Device 0 Data Input Delay for UDMA Mode. This bit field is used for programming the data input delay in increments of 2 nsec in UDMA mode.
- **Bit [13:12]**: Device 0 DSTROBE Delay (R/W) – IDE1 Device 0 DSTROBE Delay for UDMA Mode. This bit field is used for programming the DSTROBE output delay in increments of 2 nsec in UDMA mode.

- **Bit [11:09]**: Device 0 HSTROBE Delay (R/W) – IDE1 Device 0 HSTROBE Delay for UDMA Mode. This bit field is used for programming the HSTROBE output delay in increments of 2 nsec in UDMA mode
- **Bit [08:07]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [22]**: Reserved (R/W) – This bit field is reserved.
- **Bit [05:00]**: Device 0 Cycle Time Count (R/W) – IDE1 Device 0 UDMA Cycle Time Count. This bit field is used for programming the UDMA Active and Recovery Time.

9.7.51 Test Register – IDE1

Address Offset: $F0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Module Select				Nibble Select				Sub-Module Select								Data Field															

This register defines the test register for IDE Channel #1 in the SiI 0680A. This register is for chip-level simulation and verification purposes only. The register bits are defined below.

- **Bit [31:28]**: Module Select (R/W) – IDE1 Test Module Select. This bit field is used to select the logic module for testing: 0001_B = DIF module; 0010_B = TMR module; 0011_B = PIF module; and, 0100_B = DUW module.
- **Bit [27:24]**: Nibble Select (R/W) – IDE1 Test Control Nibble Select. This bit field is used to select the control nibble for testing. A value of 0001_B selects the least significant nibble, while a value of 1000_B selects the most significant nibble.
- **Bit [23:16]**: Sub-Module Select (R/W) – IDE1 Test Sub-Module Select. This bit field is used to select the logic sub-module for testing. The valid selections are listed below.

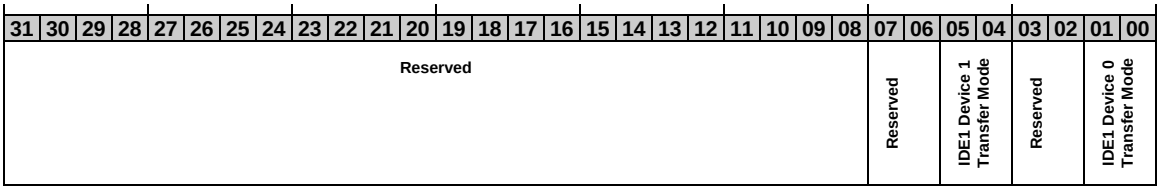
Module Select	Sub-Module Select	Description
0001_B	0001_B	FIFO Data
0010_B	0001_B	Timer 1
0010_B	0010_B	Timer 2
0010_B	0011_B	Timer 3
0010_B	0100_B	Timer 4
0011_B	0001_B	PBM_BYTE_CNT
0011_B	0010_B	WD_TMO
0100_B	0001_B	DUW_TMR_CNT

Table 9-11: IDE1 Test Register Selections

- **Bit [15:00]**: Data Field (R/W) – IDE1 Test Data Field. This bit field is used to write a preload value to the selected counter or read the current value of the selected counter.

9.7.52 Data Transfer Mode – IDE1

Address Offset: $F4_H$
Access Type: Read/Write
Reset Value: 0x0000_0022



This register defines the transfer mode register for IDE Channel #1 in the SiI 0680A. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:06]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [05:04]**: Device 1 Transfer Mode (R/W) – IDE1 Device 1 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B = PIO transfer with IORDY not monitored; 01_B = PIO transfer with IORDY monitored; 10_B = normal DMA; and, 11_B = Ultra DMA.
  When this bit field is set to value other than 00_B, SiI 0680A will monitor IORDY for normal PIO transfer.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: Device 0 Transfer Mode (R/W) – IDE0 Device 0 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B = PIO transfer with IORDY not monitored; 01_B = PIO transfer with IORDY monitored; 10_B = normal DMA; and, 11_B = Ultra DMA.

  When this bit field is set to value other than 00_B, SiI 0680A will monitor IORDY for normal PIO transfer.

10. Design for Testability

The SiI 0680A chip features internal scan for testability and fault coverage at the ASIC level, and a NAND tree for testability of the I/O pins at the board level. Test logic to support testing of the on-chip PLL is also included. Internal scan testing and PLL testing requires several bypass modes in the ASIC clocking system. These operational and bypass modes are illustrated in Fig. 10-1.

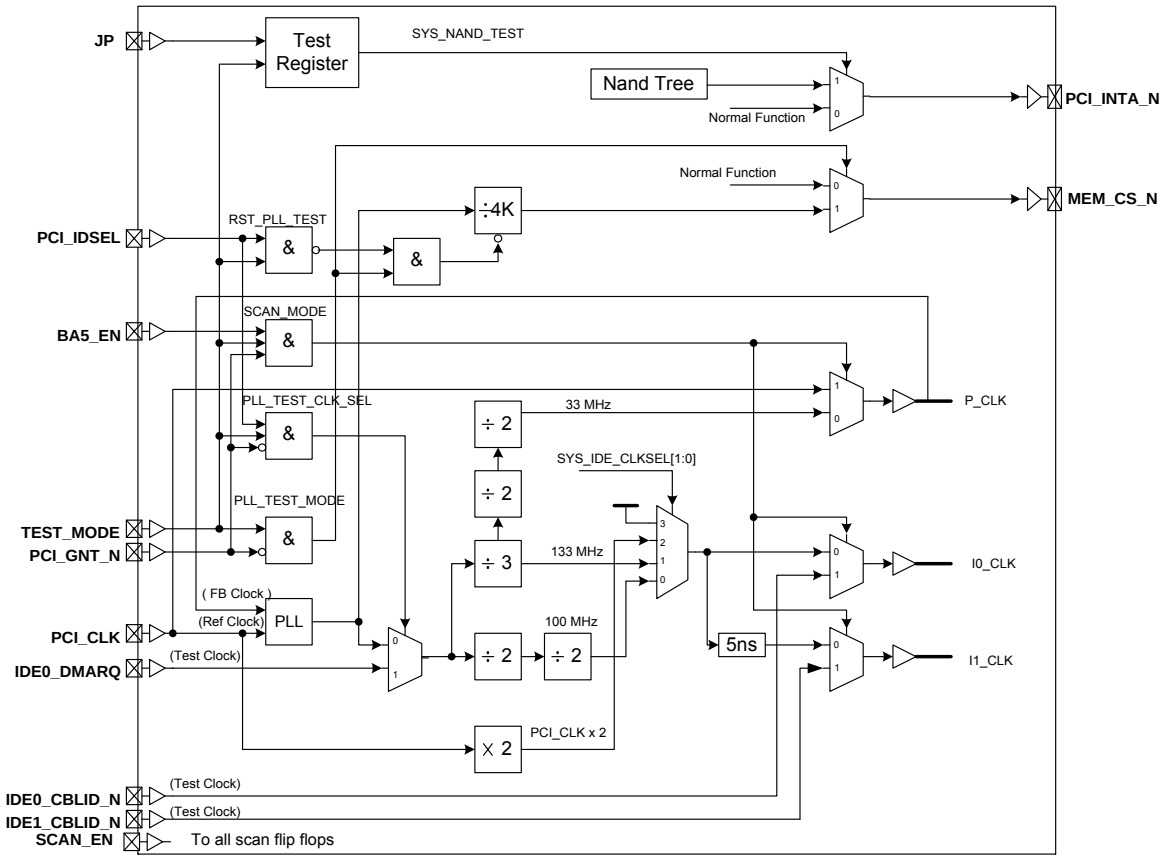


Figure 10-1: SiI 0680A Clocking System and Test Feature Diagram

10.1 Test Mode Register

The test mode register selects the type of test to be performed and sets the I/O pins in the proper states. The test mode register in the SiI 0680A is programmed through the JP and TEST_MODE input pins. The test mode register is cleared by PCI reset. Table 10-1 lists the valid test mode settings. Register settings outside of those listed are ignored, and the chip operates in normal mode.

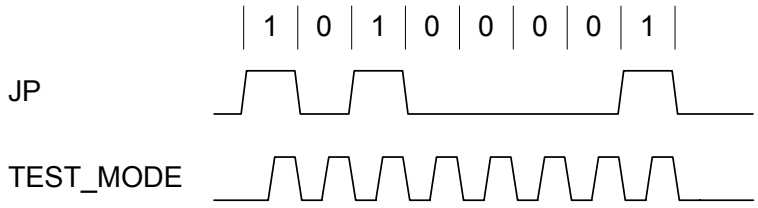


Figure 10-2: Test Mode Register Programming ($A1_H$)

Test Mode Register	Description
$A0_H$	Simulation test mode #0
$A1_H$	Simulation test mode #1
AA_H	NAND tree test mode

Table 10-1: Test Mode Register Selections

10.2 NAND Tree Test

The SiI 0680A features a NAND tree for parametric testing of the I/O pins. NAND tree testing allows the ASIC foundry to validate input voltage thresholds and wire bond connections. At the board level, the NAND tree provides connectivity checks between the PCB and package pins (signal pins only), in lieu of full JTAG boundary scan.
When the SiI 0680A is programmed for NAND tree test mode, all outputs and bi-directional pins are set to input mode. A logic representation of the NAND tree is shown in Fig. 10-2. Refer to Table 10-2 for the NAND tree order.

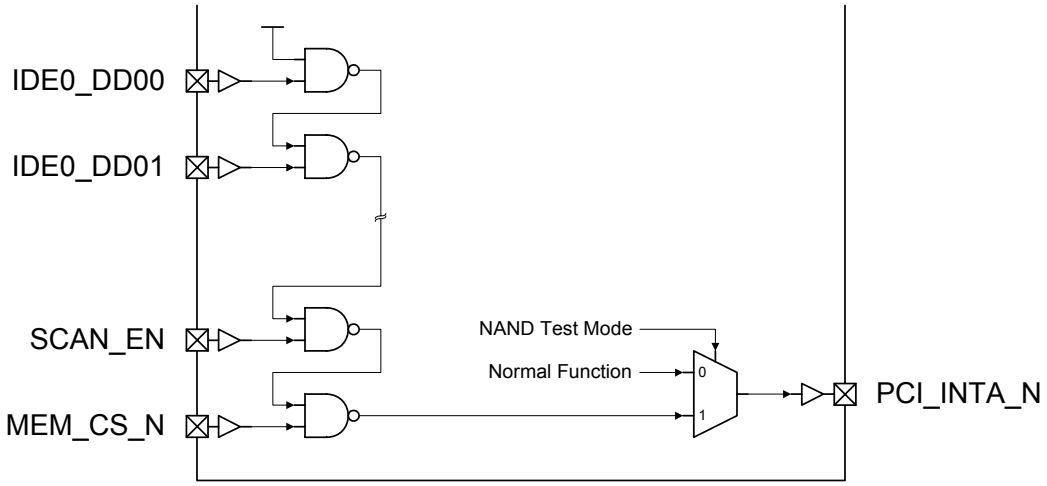


Figure 10-3: Sil 0680A NAND Tree

Order	Pin Name	Order	Pin Name	Order	Pin Name
1	IDE0_DD00	33	IDE1_DD03	65	PCI_AD26
2	IDE0_DD01	34	IDE1_DD04	66	PCI_AD25
3	IDE0_DD02	35	IDE1_DD05	67	PCI_AD24
4	IDE0_DD03	36	IDE1_DD06	68	PCI_CBE3
5	IDE0_DD04	37	IDE1_DD07	69	PCI_IDSEL
6	IDE0_DD05	38	IDE1_DD08	70	PCI_AD23
7	IDE0_DD06	39	IDE1_DD09	71	PCI_AD22
8	IDE0_DD07	40	IDE1_DD10	72	PCI_AD21
9	IDE0_DD08	41	IDE1_DD11	73	PCI_AD20
10	IDE0_DD09	42	IDE1_DD12	74	PCI_AD19
11	IDE0_DD10	43	IDE1_DD13	75	PCI_AD18
12	IDE0_DD11	44	IDE1_DD14	76	PCI_AD17
13	IDE0_DD12	45	IDE1_DD15	77	PCI_AD16
14	IDE0_DD13	46	IDE1_CS0_N	78	PCI_CBE2
15	IDE0_DD14	47	IDE1_CS1_N	79	PCI_FRAME_N
16	IDE0_DD15	48	IDE1_DA0	80	PCI_IRDY_N
17	IDE0_CS0_N	49	IDE1_DA1	81	PCI_TRDY_N
18	IDE0_CS1_N	50	IDE1_DA2	82	PCI_DEVSEL_N
19	IDE0_DA0	51	IDE1_DIOR_N	83	PCI_STOP_N
20	IDE0_DA1	52	IDE1_DIOW_N	84	PCI_PERR_N

Table 10-2: Sil 0680A NAND Tree Order

21	IDE0_DA2	53	IDE1_CBLID_N	85	PCI_SERR_N
22	IDE0_DIOR_N	54	IDE1_DMACK_N	86	PCI_PAR
23	IDE0_DIOW_N	55	IDE1_INTRQ	87	PCI_CBE1
24	IDE0_DMACK_N	56	IDE1_IORDY	88	PCI_AD15
25	IDE0_CBLID_N	57	IDE1_DMARQ	89	PCI_AD14
26	IDE0_INTRQ	58	IDE1_RST_N	90	PCI_AD13
27	IDE0_IORDY	59	JP	91	PCI_AD12
28	IDE0_DMARQ	60	PCI_AD31	92	PCI_AD11
29	IDE0_RST_N	61	PCI_AD30	93	PCI_AD10
30	IDE1_DD00	62	PCI_AD29	94	PCI_AD09
31	IDE1_DD01	63	PCI_AD28	95	PCI_AD08
32	IDE1_DD02	64	PCI_AD27	96	PCI_CBE0
97	PCI_AD07	102	PCI_AD02	107	BA5_EN
98	PCI_AD06	103	PCI_AD01	108	PCI_CLK
99	PCI_AD05	104	PCI_AD00	109	SCAN_EN
100	PCI_AD04	105	PCI_REQ_N	110	MEM_CS_N
101	PCI_AD03	106	PCI_GNT_N		

Table 10-2, SiI 0680A NAND Tree Order (continued)

10.3 Full Chip Internal Scan

The SiI 0680A generates SCAN_MODE internal signal by asserting logic “1” on the following input pins TEST_MODE, BA5_EN, and PCI_GNT_N.
The SCAN_MODE signal selects the source for the scan clocks and sets internal latches open during scan. The internal clocks for scan are provided as shown in Fig. 10-1, by the following pins:

External Input Pins:	Internal Scan Clock:
PCI_CLK	P_CLK
IDE0_CBLID	I0_CLK
IDE1_CBLID	I1_CLK

Additionally, SCAN_EN selects between normal inputs and scan inputs at all the scan flip-flops is provided by the input pin SCAN_EN.

There are six scan chains with input pins and output pins as follows:

SCAN CHAIN	SCAN INPUT PIN	SCAN OUTPUT PIN
1	IDE0_DMARQ	PCI_AD0
2	IDE0_INTRQ	PCI_AD1
3	IDE0_IORDY	PCI_AD2
4	IDE1_DMARQ	PCI_AD3
5	IDE1_INTRQ	PCI_AD4
6	IDE1_IORDY	PCI_AD5

10.4 PLL TEST

10.4.1 BYPASSING the VCO

The VCO in the analog phase-locked loop must be bypassed during digital logic simulation, to allow direct control of the PLL output clock. When PLL_CPBIAS is forced high the reference clock (PCI_CLK) is muxed to the PLL output. Automatic test equipment at the foundry also requires this test functionality to run the digital test vectors.

10.4.2 TESTING the VCO

A divide-by-4K counter is used to measure the VCO frequency for any controlled voltage at the PLL_LOOPFLT pin.

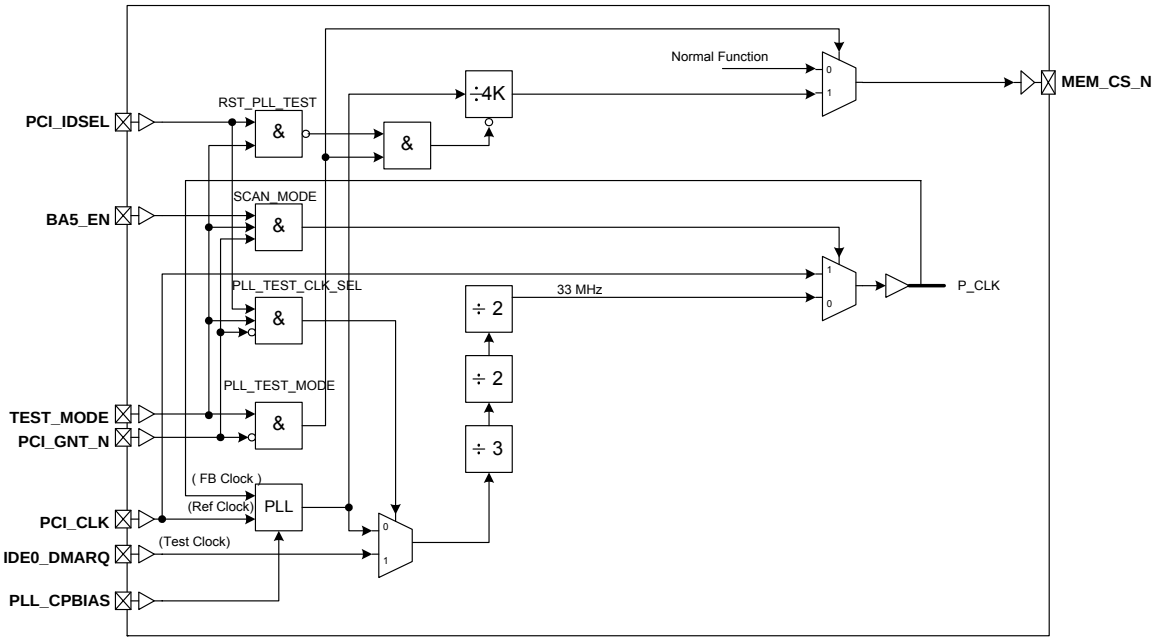


Figure 10-4: PLL Test Logic

11. Programming Sequences

11.1 Recommended Initialization Sequence for the SiI 0680A

The recommended initialization sequence for the SiI 0680A is detailed below.

Initialize PCI Configuration Space registers

- Initialize Base Address Register 0 with the address of an 8-byte range in I/O space.
- Initialize Base Address Register 1 with the address of a 4-byte range in I/O space.
- Initialize Base Address Register 2 with the address of an 8-byte range in I/O space.
- Initialize Base Address Register 3 with the address of a 4-byte range in I/O space.
- Initialize Base Address Register 4 with the address of a 16-byte range in I/O space.
- Initialize Base Address Register 5 with the address of a 256-byte range in memory space.
- To enable the bios expansion ROM, initialize the Expansion ROM Base Address Register with the address of a 512KB range in memory space.
- Enable I/O space access, memory space access, and bus master operation by setting bits [2:0] of the PCI Command register.

NOTE: The preceding configuration space register initialization is normally done by the motherboard BIOS in PC type systems.

Set IDE clock frequency by programming bits [21:20] of the System Configuration Status and Command register at offset 88_H in configuration space, or at base address 5, offset 48_H.

If the PCI-IDE arbiter's default FIFO read/write request thresholds are not suitable for the application they may be changed via the FIFO Valid Byte Count and Control IDEx register. The read threshold is defined by bits [05:00], and the write threshold is defined by bits [13:08] in the FIFO Valid Byte Count and Control – IDEx register. In most environments, setting these bit fields to zero results in the best utilization of the PCI bus by the 680A controller.

If interrupt driven operation is **not** desired, set bits [23:22] of the System Configuration Status and Command register to block IDE interrupts from reaching the PCI bus.

11.2 ATA/ATAPI Device Initialization

This section provides a general overview of the steps necessary to initialize an ATA/ATAPI device before it can be used for read/write operations.

Select the ATA/ATAPI device. The device is selected by programming bits [23:16] in the IDEx Task File Register 1 register.

If interrupt driven operation is desired, ensure that IDE interrupts are enabled by writing 0 to bits [23:16] of the IDEx Task File Register 2 register.

For ATA devices only:

Issue the Initialize Device Parameters command by

- Programming bits [23:16] in the IDEx Task File 0 register with the number of logical sectors per logical track.
- Programming bits [23:16] in the IDEx Task File 1 register with the maximum head number.
- Programming bits [31:24] in the IDEx Task File Register 1 register with the value = 91_H.
- Wait for the command to complete. This can be accomplished by waiting for an interrupt if interrupts have been enabled at both the controller and the device. If interrupts are not

enabled, command completion can be detected by polling bits [31:24] of the IDEx Task File Register 1 register until the BUSY bit is no longer asserted.

If device supports read/write multiple commands, issue the Set Multiple Mode command by:

- Programming bits [23:16] in the IDEx Task File 0 register with the number of sectors per block to use on the following Read/Write Multiple commands.
- Programming bits [31:24] in the IDEx Task File Register 1 register with the value = $C6_H$.
- Wait for the command to complete (see above).

For both ATA and ATAPI devices:

Set device transfer mode by:

- Programming bits [15:08] in the IDEx Task File 0 register with the value 03_H to "Set the transfer mode based on value in Sector Count Register".
- Programming bits [23:16] in the IDEx Task File 0 register to the desired transfer mode. The settings are defined below:

  08_H = PIO Mode 0
  09_H = PIO Mode 1
  $0A_H$ = PIO Mode 2
  $0B_H$ = PIO Mode 3
  $0C_H$ = PIO Mode 4
  20_H = Multiword DMA Mode 0
  21_H = Multiword DMA Mode 1
  22_H = Multiword DMA Mode 2
  40_H = Ultra DMA Mode 0
  41_H = Ultra DMA Mode 1
  42_H = Ultra DMA Mode 2
  43_H = Ultra DMA Mode 3
  44_H = Ultra DMA Mode 4
  45_H = Ultra DMA Mode 5
  46_H = Ultra DMA Mode 6

- Programming bits [31:24] in the IDEx Task File Register 1 register with the value = EF_H.
- Wait for the command to complete (see above).

NOTE: An 80-pin cable is required to ensure signal quality can be maintained for transfer modes higher than Ultra DMA mode 2. When bit 0 of the IDEx Task File Timing + Configuration + Status register is set, an 80-pin cable may be present (see the ATA/ATAPI specification for details on how this bit should be interpreted).

11.3 Initialization of Controller Channel Timing Registers

There are four types of timing registers associated with a channel.

The IDEx Task File Timing + Configuration + Status register controls the timing of ATA/ATAPI device task file register accesses (except for accesses to the data register). Since this register controls the task file access timing for all devices attached to the channel, it is important to program this register with values that do not exceed the capabilities of the slowest device attached to the channel.

The IDEx PIO Timing register controls the access timing of the task file data register when programmed I/O is used to transfer data to or from the device.

The IDEx DMA Timing register controls the data transfer timing when the device and controller have been setup to use a multiword DMA transfer mode.

The IDEx UDMA Timing register controls the data transfer timing when the device and controller have been setup to use an Ultra DMA transfer mode.

Data transfer timing can be set independently for each device. The following steps need to be performed to configure the controller timing to match the transfer mode selected for the ATA/ATAPI device:

Set the task file register access timing. The task file register timing is set by programming bits [31:16] of the IDEx Task File Timing + Configuration + Status register. See section 13.2.1 for recommended values to

program into this register for each PIO mode. If there is more than one device attached to the channel, select the PIO mode of the slowest device. If PIO mode 3 or 4 is selected, bit 9 of the IDEx Task File Timing + Configuration + Status register must also be set to enable the controller to monitor the state of the IORDY signal.

Set the PIO data transfer timing. The PIO data transfer timing is set by programming bits [15:0] for device 0, or bits [31:16] for device 1, of the IDEx PIO Timing register. See section 13.2.2 for recommended values to program into this register for each PIO mode. The default value of this register sets the timing slow enough to work with any ATA/ATAPI device, so this step is optional if the ATA/ATAPI device will not be used in PIO mode.

Set the multiword DMA data transfer timing. This step is necessary only if the ATA/ATAPI device will be operated in a multiword DMA mode. The multiword DMA timing is set by programming bits [15:0] for device 0, or bits [31:16] for device 1, of the IDEx DMA Timing register. See section 13.2.3 for recommended values to program into this register for each multiword DMA mode.

Set the Ultra DMA data transfer timing. This step is necessary only if the ATA/ATAPI device will be operated in an Ultra DMA mode. The Ultra DMA timing is set by programming bits [15:0] for device 0, or bits [31:16] for device 1, of the IDEx UDMA Timing register. See sections 13.2.4 and 13.2.5 for recommended values to program into this register for each Ultra DMA mode.

In order to use the controller's DMA capability to perform the data transfer for an ATA/ATAPI command, the controller needs to be configured for the transfer mode to use when transferring data to or from the ATA bus. The data transfer mode is set by programming bits [1:0] for device 0, or bits [5:4] for device 1, of the IDEx Data Transfer Mode register. The transfer mode select values are listed below:

00_B = PIO Mode without IORDY monitoring
01_B = PIO Mode with IORDY monitoring
10_B = Multiword DMA
11_B = Ultra DMA

NOTE: When using PIO to perform a data transfer, this register only instructs the controller as to whether or not it should monitor the IORDY signal when the task file data register is accessed. Any value other than 00_H will cause the controller to monitor the IORDY signal.

11.4 Issue ATA Command

The following describes the sequence to issue a read/write type command to an ATA device.

Select the IDE device. The IDE device is selected by programming bits [23:16] in the IDEx Task File Register 1 register.

Set the number of sectors to be transferred by programming bits [23:16] of the IDEx Task File Register 0 register.

Set the location of data to be transferred. The location is defined by programming the following.
Bits [31:24] in the IDEx Task File Register 0 register define the Starting Sector.
Bits [23:16] in the IDEx Task File Register 1 register define the Device and Head value.
Bits [15:08] in the IDEx Task File Register 1 register define the Cylinder High value.
Bits [07:00] in the IDEx Task File Register 1 register define the Cylinder Low value.

Issue the Read/Write PIO/DMA command by programming bits [31:24] in the IDEx Task File Register 1 register with the command desired.

11.5 IDE PIO Mode Read/Write Operation

Once the SiI 0680A is initialized via the initialization sequence described in Section 11.1, the ATA device has been initialized for PIO mode data transfer per the guidelines in section 11.2, and the controller channel has been initialized for PIO mode data transfer per the instructions in section 11.3, PIO read/write operations may be performed by following the programming sequence described below.

Issue a PIO Read/Write command to device following the steps in section 11.4.

Read Operation

Wait until an IDE channel interrupt (bit 11 in the IDEx Task File Timing + Configuration + Status register is set).

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was error.

If no error, continue to read IDE data via the IDEx Task File Register 0 register, until the expected number of sectors of data per interrupt are read.

Repeat the above three steps until all data for the read command has been transferred or an error has been detected.

Write Operation

Wait until bit 27(DRQ) in the IDEx Task File Register 1 register is set.

Continue to write IDE data via the IDEx Task File Register 0 register until the expected number of sectors of data per interrupt are written.

Wait until an IDE channel interrupt (bit 11 in the IDEx Task File Timing + Configuration + Status register is set).

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was error.

If no error, repeat the previous four steps until all data for the write command has been transferred or an error has been detected.

11.6 Watchdog Timer Operation

The purpose of the watchdog timer is to prevent the host system from hanging because a device operating in PIO mode stopped responding to task file accesses. In PIO modes 0, 1, and 2, device access is completely controlled by the values programmed into the Task File Timing and PIO Timing registers. In these modes it is not possible for a non-responsive device to hang-up the host system. However, in PIO modes 3 and 4, device task file accesses are not regulated by the timing registers alone, but can also be controlled by the device through the use of the IORDY signal. If, during a task file access by the host, the device negates IORDY and then stops responding, the host will hang waiting for the access to complete. It is this type of hang, that the watchdog timer is designed to protect against.

The watchdog timer monitors the length of time the IORDY signal is negated. If the watchdog timer detects that the the IORDY signal has remained negated longer than the watchdog timeout period (approximately 7.75us), the watchdog timer will force the task file access cycle to complete, and set the watchdog timeout bit in the IDEx Task File Timing + Configuration + Status register. The data associated with a timed out access should be considered invalid. Additionally, the watchdog timer can be configured to generate an interrupt when a timeout is detected by setting bit 14 of the IDEx Task File Timing + Configuration + Status register.

The watchdog timer feature is disabled by default.

In addition to the controller channel initialization specified in section 11.3, add the following two steps to enable the watchdog timer:

Enable the watchdog timer by setting bit 13 of the IDEx Task File Timing + Config + Status register.

If an interrupt is desired whenever the watchdog times out, enable the watchdog interrupt by setting bit 14 of the IDEx Task File Timing + Config + Status register.

The following programming sequences are needed for each PIO Mode 3 or 4 Read/Write Operation with the watchdog timer enabled:

Issue a Read/Write PIO Command to the ATA drive following the steps in section 11.4.

Read Operation

Wait for an IDE channel interrupt.

If controller interrupts are disabled, poll for the IDE interrupt by reading the IDEx Task File Timing + Configuration + Status register. If bit 12 is set, a watchdog timeout has occurred. If bit 11 is set, the ATA device is interrupting.

If the watchdog timeout bit is set,

Write 1 to bit 12 in the IDEx Task File Timing + Configuration + Status register to clear watchdog timeout status.

The watchdog timeout represents a fatal error as far as the current ATA command is concerned. A course of action that might be appropriate at this point might be to reset and reinitialize the ATA channel and then retrying the command that failed.

If the ATA device interrupt bit is set,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx Register to i clear the latched interrupt status. Note that clearing the PCI interrupt does not clear bit 18 as this bit needs to be cleared separately.

If the ATA device is not reporting an error, continue to read IDE data via the IDEx Task File Register 0 register, until the expected number of sectors of data per interrupt are read.

Repeat the read operation steps until all data for the read command has been transferred or an error has been detected.

Write Operation

Wait until bit 27(DRQ) in the IDEx Task File Register 1 register is set.

Continue to write IDE data via the IDEx Task File Register 0 register until the expected number of sectors of data per interrupt are written.

Wait for an IDE channel interrupt.

If controller interrupts are disabled, poll for the IDE interrupt by reading the IDEx Task File Timing + Configuration + Status register. If bit 12 is set, a watchdog timeout has occurred. If bit 11 is set, the ATA device is interrupting.

If the watchdog timeout bit is set,

Write 1 to bit 12 in the IDEx Task File Timing + Configuration + Status register to clear watchdog timeout status.

The watchdog timeout represents a fatal error as far as the current ATA command is concerned. A course of action that might be appropriate at this point might be to reset and reinitialize the ATA channel and then retrying the command that failed.

If the ATA device interrupt bit is set,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx Register to clear the ATA interrupt.

If no error, repeat the write operation steps until all data for the write command has been transferred or an error has been detected.

11.7 IDE PIO Mode Read Ahead Operation

Read ahead operation allows the controller to "pre-fetch" data from the IDE bus and store it in the controller's channel fifo, where it will later be retrieved by the host. This mode of operation has the potential to speed-up PIO data transfers by not forcing the host to wait the programmed PIO cycle time for every access to the task file data register. The amount of any speed increase will depend on the PIO mode in use, the characteristics of the host PCI bus, as well as the speed of the host processor.

To use the controller's PIO read ahead capability, make the following changes to the "Read Operation" portion of sections 11.5 and 11.6.

Just prior to retrieving the read data, set the read ahead byte count by programming bits [15:00] in the IDEx Virtual DMA/PIO Read Ahead Byte Count register with the exact number of bytes to be read for the interrupt.

Instead of reading the IDEx Task File Register 0 register to retrieve the data, read the IDEx Read Ahead Data register instead.

11.8 IDE MDMA/UDMA Read/Write Operation

Once the SiI 0680A is initialized via the initialization sequence described in Section 11.1, the ATA device has been initialized for MDMA/UDMA mode data transfer per the guidelines in section 11.2, and the controller channel has been initialized for MDMA/UDMA mode data transfer per the instructions in section 11.3, DMA read/write operations may be performed by following the programming sequence described below.

Issue a DMA read/write command to the device following steps in section 11.4.

Program Bus Master Registers

Clear bit 17 in the PCI Bus Master – IDEx register. This bit is set if an error occurred during the previous DMA access.
Clear bit 18 in the PCI Bus Master – IDEx register. This bit is set if an IDE interrupt occurred during the previous DMA access.

Create a Physical Region Descriptor (PRD) Table.
A PRD table is an array where each entry describes the location and size of a physical memory buffer that will be used during the DMA operation. Each PRD table entry is 64-bits in length, formatted as follows; bits [31:0] contain the 32-bit starting address of the memory buffer, bits [47:32] contain the 16-bit size of the memory buffer, bits [62:48] are normally unused (see section 11.10 for details of how these bits may be used), bit 63 flags the end of the PRD table and therefore should only be set in the last entry of the PRD table. The PRD table itself must be constructed in a memory region that can be directly accessed by the 680A controller. Once the PRD table is built, the controller must be informed of its location. This is accomplished by writing the 32-bit address of the PRD table to the PRD Table Address – IDEx register.

Enable DMA transfer.
DMA is enabled by writing bits [7:0] of the PCI Bus Master – IDEx register. Bit 3 of this register controls the direction of the DMA transfer; 1 = write to memory, 0 = read from memory. Setting bit 0 of the register enables the controller to perform DMA operations.
Note: Task file registers are inaccessible as long as bit 0 is set.

Wait for a PCI interrupt.

When a PCI interrupt occurs, read the PCI Master – IDEx status register and check the DMA status bits. The possible combinations of the status bits [18:16] are defined below.

000_B = If the IDE device does not report an error, then the PRD table specified a size that is smaller than the IDE transfer size.
001_B = DMA transfer in progress.

010_B = The controller had a problem transferring data to/from memory.
100_B = Normal completion.

101_B = If the IDE device does not report an error, then the PRD specified a size that is larger than the IDE transfer size.

Make sure PCI bus master operation of the SiI 0680A is stopped by clearing bit 0 of the PCI Bus Master – IDEx register.
Note: The task file registers are not accessible as long as bit 0 is set. Clearing bit 0 causes bit 16 to be cleared as well.

Read the device status at bits [13:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was error.

Write '1' to bit 18 (write-one-to-clear) in the PCI Bus Master – IDEx register to clear the PCI Interrupt.

11.9 IDE Virtual DMA Read/Write Operation

In virtual DMA operation the controller uses a PIO data transfer mode to move data between an ATA/ATAPI device and the controller, and uses DMA to move that same data between the controller and the host memory. For ATA/ATAPI devices that cannot operate in a "true" DMA mode, virtual DMA provides two benefits; first, using DMA to move data reduces the demand on the host CPU, and second, systems that use virtual memory often require that data buffers that will be accessed directly by low level device drivers be "mapped" into the operating system's address space, in virtual DMA mode the CPU does not access the data buffer directly, so the overhead of obtaining the mapping to operating system address space is eliminated.

11.9.1 Using Virtual DMA with Non-DMA Capable Devices

Once the SiI 0680A is initialized via the initialization sequence described in Section 11.1, the ATA device has been initialized for PIO mode data transfer per the guidelines in section 11.2, and the controller channel has been initialized for PIO mode data transfer per the instructions in section 11.3, virtual DMA read/write operations may be performed by following the programming sequence described below.

NOTE: The watchdog timer feature is compatible with virtual DMA operation. See section 11.7 for details about using the watchdog timer.

Issue a PIO read/write command to the device following steps in section 11.4.

Read Operation

Wait for a PCI interrupt.

Read the DMA status bits [18:16] of the PCI Bus Master – IDEx register, and check that bit 18 is set to make sure the interrupt was generated by the expected channel.

If expected channel interrupted, read bits [11:10] of the channel's IDEx Task File Timing + Configuration + Status register to determine the cause of the interrupt. Bit 11 is set if the ATA/ATAPI device has an interrupt pending, bit 10 is set if a virtual DMA operation completed.

If a virtual DMA operation completed,

Write 00_H to bits [7:0] of the PCI Bus Master – IDEx register to disable DMA operation.

Write 1 to bits [18:17] of the PCI Bus Master –IDEx register to reset the DMA status and virtual DMA interrupt bits, and the PCI interrupt.

Check the previously read DMA status bits to ensure the DMA completed successfully. See section 11.8 for more information about interpreting the DMA status bits.

Because ATA/ATAPI commands that transfer data using PIO can generate several interrupts during the data transfer phase of the command, a race condition is created between the interrupt indicating the completion of a virtual DMA operation, and the interrupt from the ATA/ATAPI device indicating it is ready to perform the next part of the data transfer. To prevent missing an ATA/ATAPI device interrupt due to this race condition, it is necessary to re-read the channel's IDEx Task File Timing + Configuration + Status register after disabling DMA operation and examining bit

11. If bit 11 is set, the ATA/ATAPI device is interrupting and should be serviced by following the steps below (assuming that the virtual DMA operation completed successfully).

If the ATA/ATAPI device has interrupted,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx register to clear the DMA Complete bit (NOTE: The DMA Complete bit acts as a latched copy of the ATA interrupt line when the channel is not performing a DMA operation).

If the ATA/ATAPI device is not reporting an error, and DRQ is asserted (bit 27 of IDEx Task File Register 1), then the device is interrupting to transfer data to the host. To transfer the data, the DMA registers are setup to only perform that part of the data transfer expected for this interrupt. The DMA is setup similarly to the way it is when performing a normal read DMA command, but with one additional step. Before the DMA is enabled, the IDEx Virtual DMA/PIO Read Ahead Byte Count register must be written with the 32-bit count of the number of bytes to be transferred for this interrupt.

Repeat the above steps until all data for the read command has been transferred or an error has been detected.

Write Operation

Poll the IDEx Task File Register 1 bits [31:24] until either bit 27 (DRQ) is set indicating the device is ready for write data transfer, or bit 24 (ERR) is set indicating the device has detected an error with the write command.

If no error, and DRQ is asserted (bit 27 of IDEx Task File Register 1), then the device is waiting for write data transfer. To transfer the data, the DMA registers are setup to only perform that part of the data transfer expected at this time. For example, a Write Sectors command would expect to transfer 1 sector (512 bytes), while a Write Multiple command would expect to transfer the lesser of the number of sectors set by the Set Multiple Mode command or the total number of sectors specified by the Write Multiple command. The DMA is setup similarly to the way it is when performing a normal write DMA command, but with one additional step. Before the DMA is enabled, the IDEx Virtual DMA/PIO Read Ahead Byte Count register must be written with the 32-bit count of the number of bytes to be transferred.

Wait for a PCI interrupt.

Read the DMA status bits [18:16] of the PCI Bus Master – IDEx register, and check that bit 18 is set to make sure the interrupt was generated by the expected channel.

If expected channel interrupted, read bits [11:10] of the channel's IDEx Task File Timing + Configuration + Status register to determine the cause of the interrupt. Bit 11 is set if the ATA/ATAPI device has an interrupt pending, bit 10 is set if a virtual DMA operation completed.

If a virtual DMA operation completed,

Write 00_H to bits [7:0] of the PCI Bus Master – IDEx register to disable DMA operation.

Write 1 to bits [18:17] of the PCI Bus Master –IDEx register to reset the DMA status and virtual DMA interrupt bits, and PCI interrupt.

Check the previously read DMA status bits to ensure the DMA completed successfully. See section 11.8 for more information about interpreting the DMA status bits.

Because ATA/ATAPI commands that transfer data using PIO can generate several interrupts during the data transfer phase of the command, a race condition is created between the interrupt indicating the completion of a virtual DMA operation, and the interrupt from the ATA/ATAPI device indicating it is ready to perform the next part of the data transfer. To prevent missing an ATA/ATAPI device interrupt due to this race condition, it is necessary to re-read the channel's IDEx Task File Timing + Configuration + Status register after disabling DMA operation and examining bit 11. If bit 11 is set, the ATA/ATAPI device is interrupting and should be serviced by following the steps below (assuming that the virtual DMA operation completed successfully).

If the ATA/ATAPI device has interrupted,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx register to clear the DMA Complete bit (NOTE: The DMA Complete bit acts as a latched copy of the ATA interrupt line when the channel is not performing a DMA operation).

If the ATA/ATAPI device is not reporting an error, and DRQ is asserted (bit 27 of IDEx Task File Register 1), then the device is interrupting to transfer data to the device. To transfer the data, the DMA registers are setup to only perform that part of the data transfer expected for this interrupt. The DMA is setup similarly to the way it is when performing a normal write DMA command, but with one additional step. Before the DMA is enabled, the IDEx Virtual DMA/PIO Read Ahead Byte Count register must be written with the 32-bit count of the number of bytes to be transferred for this interrupt.

Repeat the above steps starting at "Wait for PCI interrupt" until all data for the write command has been transferred or an error has been detected.

11.9.2 Using Virtual DMA with DMA Capable Devices

Even though a device may be DMA capable, there are ATA/ATAPI commands that require that a PIO mode be used to transfer data. For these commands, virtual DMA can be used to perform the data transfer. Using virtual DMA with an ATA/ATAPI device that has already been configured to use DMA for normal read/write operation is performed very much like the sequence described above for PIO mode only devices, but with the following additional considerations:

- The Data Transfer Mode – IDEx register associated with the ATA/ATAPI device needs to be programmed for a PIO type transfer mode **before** DMA operation is enabled, and must be re-programmed with the DMA/UDMA transfer type used during normal DMA operation once the virtual DMA operation is complete.

- A PIO mode compatible with the device should be programmed into the appropriate IDEx – PIO Timing register. This register does not have to be written for every command that uses virtual DMA, instead it should be written as part of the controller initialization sequence.

11.10 Second PCI Bus Master Registers Usage

In order to provide backward compatibility with existing drivers, the Physical Region Descriptor (PRD) tables used by the 680A controller when performing DMA transfers suffer the following limitations; a PRD table entry cannot represent a memory area greater than 64k, nor can a PRD table entry represent a memory area that spans a 64k address boundary. Whenever DMA is initiated via the PCI Bus Master – IDEx registers, the foregoing limitations are enforced by the 680A controller.

A feature known as Large Block Transfer has been added to the SiI 0680A controller to allow new drivers to get around the 64k size and address limits of PRD table entries expected by existing drivers. Large Block Transfer simplifies the creation of PRD tables by reducing the number of table entries that need to be created and eliminating the need to make sure a memory region does not cross a 64k boundary. Large Block Transfer mode is enabled whenever DMA is initiated by writing to the PCI Bus Master **2** – IDEx registers (base address 5, offset 10_H or 18_H). When performing DMA in Large Block Transfer mode, the 680A controller interprets the fields of a PRD table entry differently. In all other respects, DMA interrupt generation, DMA status bit interpretation, etc…, Large Block Transfer mode behaves identically to a non-Large Block Transfer mode DMA operation. The following table describes the format of a PRD table entry:

Bits 31:0	32-bit starting address of the memory region.
Bits 47:32	When not operating in Large Block Transfer mode, this field specifies the size of the memory region. If the size of the memory region is greater than 64k, or crosses a 64k address boundary, then two or more PRD table entries will need to be created to describe it. If operating in Large Block Transfer mode, this field contains the least significant 16-bits of the size of the memory region.
Bits 62:48	If not operating in Large Block Transfer mode, this field is unused.

	If operating in Large Block Transfer mode, this field contains the most significant 15-bits of the size of the memory region.
Bit 63	When set, this bit indicates that this is the last entry in the PRD table.

Table 11-1, Physical Region Descriptor (PRD) Format

12. FLASH and EEPROM Programming Sequences

12.1 FLASH Memory Access

The SiI 0680A supports an external FLASH memory device up to 4 Mbits in capacity. Access to the FLASH memory is available through two means: PCI Direct Access and Register Access.

12.1.1 PCI Direct Access

Access to the Expansion Rom is enabled by setting bit 0 in the Expansion Rom Base Address register at Offset 30h of the PCI Configuration Space. When this bit is set, bits [31:19] of the same register are programmable by the system to set the base address for all FLASH memory accesses. Read and write operations with the FLASH memory are initiated by Memory Read and Memory Write commands on the PCI bus. Accesses may be as Bytes, Words, or DWords.

12.2.2 Register Access

This type of FLASH memory access is carried out through a sequence of internal register read and write operations. The proper programming sequences are detailed below.

FLASH Write Operation

Verify that bit 25 is cleared in the register at Offset 50_H of Base Address 5. The bit reads one when a memory access is currently in progress.

It reads zero when the memory access is complete and ready for another operation.

Program the write address for the FLASH memory access. The address field is defined by bits [18:00] in the FLASH Memory Address – Command + Status register.

Program the write data for the FLASH memory access. The data field is defined by bits [07:00] in the FLASH Memory Data register at Offset 54 of Base Address 5.

Program the memory access type . The memory access type is defined by bit 24 in the FLASH Memory Address – Command + Status register. The bit must be cleared for a memory write access.

Initiate the FLASH memory access by setting bit 25 in the FLASH Memory Address – Command + Status register.

FLASH Read Operation

Verify that bit 25 is cleared in the FLASH Memory Address – Command + Status register at Offset 50_H of Base Address 5. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete and ready for another operation.

Program the read address for the FLASH memory access. The address field is defined by bits [18:00] in the FLASH Memory Address – Command + Status register.

Program the memory access type. The memory access type is defined by bit 24 in the FLASH Memory Address – Command + Status register. The bit must be set for a memory read access.

Initiate the FLASH memory access by setting bit 25 in the FLASH Memory Address – Command + Status register.

Verify that bit 25 is cleared in the FLASH Memory Address – Command + Status register. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete.

Read the data from the FLASH memory access. The data field is defined by bits [07:00] in the FLASH Memory Data register at Offset 54_H of Base Address 5.

12.2 EEPROM Memory Access

The SiI 0680A supports an external 256-byte EEPROM memory device. Access to the EEPROM memory is available through internal register operations in the SiI 0680A.

EEPROM Write Operation

Verify that bit 25 is cleared in the EEPROM Memory Address – Command + Status register at Offset 58_H of Base Address 5. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete and ready for another operation.

Write '1' to clear bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

Program the write address for the EEPROM memory access. The address field is defined by bits [07:00] in the EEPROM Memory Address – Command + Status register. Program bits [15:08] to zero.

Program the write data for the EEPROM memory access. The data field is defined by bits [07:00] in the EEPROM Memory Data register at Offset $5C_H$ of Base Address 5.

Program the memory access type. The memory access type is defined by bit 24 in the EEPROM Memory Address – Command + Status register. The bit must be cleared for a memory write access.

Initiate the EEPROM memory access by setting bit 25 in the EEPROM Memory Address – Command + Status register.

Poll bit 25 in the EEPROM Memory Address – Command + Status register. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete.

Check bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

EEPROM Read Operation

Verify that bit 25 is cleared in the EEPROM Memory Address – Command + Status register at Offset 58_H of Base Address 5. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete and ready for another operation.

Write '1' to clear bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

Program the read address for the EEPROM memory access. The address field is defined by bits [07:00] in the EEPROM Memory Address – Command + Status register. Program bits [15:08] to zero.

Program the memory access type. The memory access type is defined by bit 24 in the EEPROM Memory Address – Command + Status register. The bit must be set for a memory read access.

Initiate the EEPROM memory access by setting bit 25 in the EEPROM Memory Address – Command + Status register.

Poll bit 25 in the EEPROM Memory Address – Command + Status register. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete.

Check bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

Read the data from the EEPROM memory access. The data field is defined by bits [07:00] in the EEPROM Memory Data register at Offset $5C_H$ of Base Address 5.

13. SiI 0680A Timing Registers

13.1 Timing Register Definition

RECOVERY COUNT TIMING

Bits [21:16] IDE0 Task File Timing + Configuration + Status
Bits [05:00] IDE0 PIO Timing
Bits [21:06] IDE0 PIO Timing
Bits [05:00] IDE1 PIO Timing
Bits [21:06] IDE1 PIO Timing

ACTIVE COUNT TIMING

Bits [27:22] IDE0 Task File Timing + Configuration + Status
Bits [11:06] IDE0 PIO Timing
Bits [27:22] IDE0 PIO Timing
Bits [11:06] IDE1 PIO Timing
Bits [27:22] IDE1 PIO Timing

Value	Active Time in PCI Clock
00h	1
01h	1
02h	2
03h	3
...	
3Fh	63

ADDRESS SETUP COUNT TIMING

Bits [31:28] IDE0 Task File Timing + Configuration + Status
Bits [15:12] IDE0 PIO Timing
Bits [31:28] IDE0 PIO Timing
Bits [15:12] IDE1 PIO Timing
Bits [31:28] IDE1 PIO Timing

Value	Active Time in PCI Clock
0h	1
1h	1
2h	2
3h	3

UDMA Cycle Time Count Timing

Value	Cycle Time in IDE Clock
00h	2
01h	2
02h	3
03h	4
...	
3Fh	64

In the UDMA timing register. the number of clocks is always 1 greater than the value loaded for the cycle time count. The only exception is that value "0" requires two cycles.

13.2 Timing Registers Programming Suggestion

13.2.1 TF Timing Register Programming in Number of 33 MHz PCI clock

	TF 0	TF 1	TF 2	TF 3	TF 4
Address Setup	3	2	1	1	1
Active Count	10	10	10	3	3
Recovery Count	10	3	1	3	1
TF Timing Register	328Ah	2283h	1281h	10C3h	10C1h

13.2.2 PIO Timing Register Programming in Number of 33 MHz PCI clock

	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4
Address Setup	3	2	1	1	1
Active Count	10	10	4	3	3
Recovery Count	10	3	4	3	1
PIO Timing Register	328Ah	2283h	1104h	10C3h	10C1h

13.2.3 DMA Timing Register Programming in Number of 33 MHz PCI clock

	MDMA 0	MDMA 1	MDMA 2
Address Setup	2	1	1
Active Count	8	3	3
Recovery Count	8	2	1
PIO Timing Register	2208h	10C2h	10C1h

13.2.4 UDMA Timing Register Programming in Number of 100 MHz IDE clock

	UDMA 0	UDMA 1	UDMA 2	UDMA 3	UDMA 4	UDMA 5
Cycle	11	7	5	4	2	1

13.2.4 UDMA Timing Register Programming in Number of 133 MHz IDE clock

	UDMA 0	UDMA 1	UDMA 2	UDMA 3	UDMA 4	UDMA 5	UDMA 6
Cycle	15	11	7	5	3	2	1

14. Errata

The 680A returns Target Abort when CBE#[3:0] = 1111

When an access is made to the 680A memory region with Data Byte Enable = 0FH (no data to be transferred) and the address is within the 680A Delay-Transaction Region, instead of terminating the transaction normally, terminates the transaction with Target Abort. This does not comply with the PCI specification and may result in system errors in some systems.

This may happen when the 680A is on a 64-bit PCI bus and the host issues a 64-bit transaction with only low or high Dword bytes enabled. Since 680A only supports 32-bit transactions, the host may break the 64-bit transaction into two 32-bit transactions in which, one of the transactions is a dummy transaction with all Byte Enables set to 1111.

The Delay-Transaction Region on the 680A includes: the FIFO region (BA5 + (60h-7Fh)); the IDE0 Task File Region (BA5 + (80h-8Fh)); and the IDE1 Task File Region (BA5 + (C0h-CFh)).

Impact: May result in system errors in some systems.

Workaround: At present this has only been observed in an environment in which conditions have been forced with a PCI bridge device. No tested motherboards have experienced problems.

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