Siliconix

FET Data Book

Siliconix

Field Effect Transistors

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Siliconix SEMICONDUCTOR DEVICES

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how to use the
FET cross reference and substitution guide

The following examples illustrate how the FET Cross Reference and Substitution Guide should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3458	N JFET	2N3458

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison.

Case (3) Recommended replacement is presently offered by Siliconix as an Industry Part Number only in Europe.

Industry Part Number	Type and Classification	Recommended Replacement
BF244A	N JFET	BF244A*

Part numbers in this category *also* offered on demand through Siliconix sales outlets in the U.S.A.

Type and calssification abbreviations are described as follows:

CL (Current Limiter)
D (Dual)
DEPL (Depletion-Mode Normally-On)
ENH (Enhancement-Mode Normally-Off)
FF (Photo FET)
4 (Quad Array FETs)
G (Gate)
N (N-Channel)
P (P-Channel)
PAD (Pico Ampere Diode)
TMP (Transducer Microphone Preamplifier)
VMOS (Vertical MOSFET)

FET cross reference and substitution guide

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
1N5283	CL N JFET	CR022	3-65	4-29
1N5284	CL N JFET	CR024	3-65	4-29
1N5285	CL N JFET	CR027	3-65	4-29
1N5286	CL N JFET	CR030	3-65	4-29
1N5287	CL N JFET	CR033	3-65	4-29
1N5288	CL N JFET	CR039	3-65	4-29
1N5289	CL N JFET	CR043	3-65	4-29
1N5290	CL N JFET	CR047	3-65	4-29
1N5291	CL N JFET	CR056	3-65	4-29
1N5292	CL N JFET	CR062	3-65	4-29
1N5293	CL N JFET	CR068	3-65	4-30
1N5294	CL N JFET	CR075	3-65	4-30
1N5295	CL N JFET	CR082	3-65	4-30
1N5296	CL N JFET	CR091	3-65	4-30
1N5297	CL N JFET	CR100	3-65	4-30
1N5298	CL N JFET	CR110	3-65	4-30
1N5299	CL N JFET	CR120	3-65	4-30
1N5300	CL N JFET	CR130	3-65	4-30
1N5301	CL N JFET	CR140	3-65	4-30
1N5302	CL N JFET	CR150	3-65	4-30
1N5303	CL N JFET	CR160	3-65	4-31
1N5304	CL N JFET	CR180	3-65	4-31
1N5305	CL N JFET	CR200	3-65	4-31
1N5306	CL N JFET	CR220	3-65	4-31
1N5307	CL N JFET	CR240	3-65	4-31
1N5308	CL N JFET	CR270	3-65	4-31
1N5309	CL N JFET	CR300	3-65	4-31
1N5310	CL N JFET	CR330	3-65	4-31
1N5311	CL N JFET	CR360	3-65	4-31
1N5312	CL N JFET	CR390	3-65	4-31
1N5313	CL N JFET	CR430	3-65	4-31
1N5314	CL N JFET	CR470	3-65	4-31
2N2386	P JFET	2N2608		
2N2386A	P JFET	2N2609		
2N2497	P JFET	2N3329		
2N2498	P JFET	2N3330		
2N2499	P JFET	2N3331		
2N2500	P JFET	2N3332		
2N2506	P JFET	2N2608		
2N2606JAN	P JFET	2N2608JAN		
2N2607	P JFET	2N2608		
2N2607JAN	P JFET	2N2608JAN		
2N2608	P JFET	2N2608	3-1	4-54
2N2608JAN	P JFET	2N2608JAN	3-1	4-54
2N2609	P JFET	2N2609	3-1	4-55
2N2609JAN	P JFET	2N2609JAN	3-1	4-55
2N2841	P JFET	2N2843		
2N2842	P JFET	2N2843		
2N2843	P JFET	2N2843	3-2	4-54
2N2844	P JFET	2N2844	3-2	4-55
2N3066	N JFET	2N4340		
2N3067	N JFET	2N4338		
2N3068	N JFET	2N4338		
2N3069	N JFET	2N4341		
2N3070	N JFET	2N4339		
2N3071	N JFET	2N4338		
2N3084	N JFET	2N3459		
2N3085	N JFET	2N3459		
2N3086	N JFET	2N3459		
2N3087	N JFET	2N3459		
2N3088	N JFET	2N3460		
2N3088A	N JFET	2N3460		
2N3089	N JFET	2N3460		
2N3089A	N JFET	2N3460		
2N3112	P JFET	–		
2N3113	P JFET	2N2843		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N3277	P JFET	2N2608		
2N3278	P JFET	2N2608		
2N3328	P JFET	2N3438		
2N3329	P JFET	2N3329	3-3	4-54
2N3330	P JFET	2N3330		
2N3331	P JFET	2N3331		
2N3332	P JFET	2N3332		
2N3365	N JFET	2N4340		
2N3366	N JFET	2N4338		
2N3367	N JFET	2N4338		
2N3368	N JFET	2N3368	3-4	4-36
2N3369	N JFET	2N3369	3-4	4-36
2N3370	N JFET	2N3370	3-4	4-36
2N3376	P JFET	2N3329		
2N3377	P JFET	–		
2N3378	P JFET	2N3330		
2N3379	P JFET	–		
2N3380	P JFET	2N3331		
2N3381	P JFET	–		
2N3382	P JFET	2N3382	3-5	4-56
2N3383	P JFET	–		
2N3384	P JFET	2N3384	3-5	4-56
2N3385	P JFET	–		
2N3386	P JFET	2N3386	3-5	4-56
2N3436	N JFET	2N3436	3-6	4-36
2N3437	N JFET	2N3437	3-6	4-36
2N3438	N JFET	2N3438	3-6	4-36
2N3452	N JFET	2N4340		
2N3453	N JFET	2N4338		
2N3454	N JFET	2N4338		
2N3455	N JFET	2N4340		
2N3456	N JFET	2N4338		
2N3457	N JFET	2N4338		
2N3458	N JFET	2N3458	3-7	4-36
2N3459	N JFET	2N3459	3-7	4-36
2N3460	N JFET	2N3460	3-7	4-36
2N3574	P JFET	2N2843		
2N3575	P JFET	2N2843		
2N3578	P JFET	2N2608		
2N3608	P MOS ENH	3N163		
2N3609	D P MOS ENH	–		
2N3631	N MOS DEPL	2N3631	3-8	4-1
2N3684	N JFET	2N3684	3-9	4-23
2N3684A	N JFET	–		
2N3685	N JFET	2N3685	3-9	4-23
2N3685A	N JFET	–		
2N3686	N JFET	2N3686	3-9	4-23
2N3686A	N JFET	–		
2N3687	N JFET	2N3687	3-9	4-23
2N3687A	N JFET	–		
2N3819	N JFET	2N3819*	3-10	4-42
2N3820	P JFET	J270		
2N3821	N JFET	2N3821	3-11	4-42
2N3821JAN	N JFET	–	3-11	4-42
2N3822	N JFET	2N3822	3-11	4-42
2N3822JAN	N JFET	–	3-11	4-42
2N3823	N JFET	2N3823	3-12	4-42
2N3823JAN	N JFET	–	3-12	4-42
2N3824	N JFET	2N3824	3-13	4-42
2N3909	P JFET	2N3909	3-14	4-54
2N3909A	P JFET	2N3909		
2N3921	D N JFET	2N3921	3-15	4-34
2N3922	D N JFET	2N3922	3-15	4-34
2N3954	D N JFET	2N3954	3-16	4-23
2N3954A	D N JFET	2N3954A	3-16	4-23
2N3955	D N JFET	2N3955	3-16	4-23
2N3955A	D N JFET	2N3955A	3-16	4-23

***Siliconix European Part Number *also* Available Through U.S.A. Sales Outlets**

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N3956	D N JFET	2N3956	3-17	4-23
2N3957	D N JFET	2N3957	3-17	4-23
2N3958	D N JFET	2N3958	3-17	4-23
2N3966	N JFET	2N3966	3-18	4-25
2N3967	N JFET	2N4221		
2N3967A	N JFET	2N4221		
2N3968	N JFET	2N3685		
2N3968A	N JFET	2N3685		
2N3969	N JFET	2N3686		
2N3969A	N JFET	2N3686		
2N3970	N JFET	2N3970	3-19	4-20
2N3971	N JFET	2N3971	3-19	4-20
2N3972	N JFET	2N3972	3-19	4-20
2N3993	P JFET	2N3386		
2N3993A	P JFET	2N3386		
2N3994	P JFET	2N3382		
2N3994A	P JFET	2N3382		
2N4038	N MOS ENH	–		
2N4065	P MOS ENH	M104		
2N4066	D P MOS ENH	–		
2N4067	D P MOS ENH	–		
2N4082	D N JFET	–		
2N4083	D N JFET	–		
2N4084	D N JFET	2N4084	3-15	4-34
2N4085	D N JFET	2N4085	3-15	4-34
2N4091	N JFET	2N4091	3-21	4-20
2N4091A	N JFET	2N4091		
2N4092	N JFET	2N4092	3-21	4-20
2N4092A	N JFET	2N4092		
2N4093	N JFET	2N4093	3-21	4-20
2N4093A	N JFET	2N4093		
2N4117	N JFET	2N4117	3-22	4-46
2N4117A	N JFET	2N4117A	3-22	4-46
2N4118	N JFET	2N4118	3-22	4-46
2N4118A	N JFET	2N4118A	3-22	4-46
2N4119	N JFET	2N4119	3-22	4-46
2N4119A	N JFET	2N4119A	3-22	4-46
2N4120	P MOS ENH	3N163		
2N4139	N JFET	2N3822		
2N4220	N JFET	2N4220	3-24	4-42
2N4220A	N JFET	2N4220A	3-24	4-42
2N4221	N JFET	2N4221	3-24	4-42
2N4221A	N JFET	2N4221A	3-24	4-42
2N4222A	N JFET	2N4222A	3-24	4-42
2N4223	N JFET	2N4223	3-25	4-42
2N4224	N JFET	2N4224	3-25	4-42
2N4267	P MOS ENH	3N163		
2N4268	P MOS ENH	–		
2N4302	N JFET	2N4302	3-26	4-36
2N4303	N JFET	2N4303	3-26	4-36
2N4304	N JFET	2N4304	3-26	4-36
2N4338	N JFET	2N4338	3-27	4-36
2N4339	N JFET	2N4339	3-27	4-36
2N4340	N JFET	2N4340	3-27	4-36
2N4341	N JFET	2N4341	3-27	4-36
2N4342	P JFET	–		
2N4343	P JFET	–		
2N4351	N MOS ENH	M117		
2N4352	P MOS ENH	3N163		
2N4353	P MOS ENH	M103		
2N4360	P JFET	–		
2N4381	P JFET	2N2609		
2N4382	P JFET	2N5115		
2N4391	N JFET	2N4391	3-29	4-20
2N4392	N JFET	2N4392	3-29	4-20
2N4393	N JFET	2N4393	3-29	4-20
2N4416	N JFET	2N4416	3-30	4-25
2N4416A	N JFET	2N4416A	3-30	4-25
2N4416AJAN	N JFET	–		
2N4416AJANTX	N JFET	–		
2N4417	N JFET	PN4417	3-31	4-25
2N4445	N JFET	2N5432		
2N4446	N JFET	2N5433		
2N4447	N JFET	2N5432		
2N4448	N JFET	2N5433		
2N4856	N JFET	2N4856	3-32	4-20
2N4856A	N JFET	2N4856A	3-33	4-20
2N4856JAN	N JFET	2N4856JAN	3-32	4-20
2N4856JANTX	N JFET	2N4856JANTX	3-32	4-20
2N4856JANTXV	N JFET	2N4856JANTXV	3-32	4-20
2N4857	N JFET	2N4857	3-32	4-20
2N4857A	N JFET	2N4857A	3-33	4-20
2N4857JAN	N JFET	2N4857JAN	3-32	4-20
2N4857JANTX	N JFET	2N4857JANTX	3-32	4-20
2N4857JANTXV	N JFET	2N4857JANTXV	3-32	4-20
2N4858	N JFET	2N4858	3-32	4-20
2N4858A	N JFET	2N4858A	3-33	4-20
2N4858JAN	N JFET	2N4858JAN	3-32	4-20
2N4858JANTX	N JFET	2N4858JANTX	3-32	4-20
2N4858JANTXV	N JFET	2N4858JANTXV	3 32	4-20
2N4859	N JFET	2N4859	3-32	4-20
2N4859A	N JFET	2N4859A	3-33	4-20
2N4859JAN	N JFET	2N4859JAN	3-32	4-20
2N4859JANTX	N JFET	2N4859JANTX	3-32	4-20
2N4859JANTXV	N JFET	2N4859JANTXV	3-32	4-20
2N4860	N JFET	2N4860	3-32	4-20
2N4860A	N JFET	2N4860A	3 33	4-20
2N4860JAN	N JFET	2N4860JAN	3-32	4-20
2N4860JANTX	N JFET	2N4860JANTX	3-32	4-20
2N4860JANTXV	N JFET	2N4860JANTXV	3-32	4-20
2N4861	N JFET	2N4861	3-32	4-20
2N4861A	N JFET	2N4861A	3-33	4-20
2N4861JAN	N JFET	2N4861JAN	3-32	4-20
2N4861JANTX	N JFET	2N4861JANTX	3-32	4-20
2N4861JANTXV	N JFET	2N4861JANTXV	3-32	4-20
2N4867	N JFET	2N4867	3-34	4-44
2N4867A	N JFET	2N4867A	3-34	4-44
2N4868	N JFET	2N4868	3-34	4-44
2N4868A	N JFET	2N4868A	3-34	4-44
2N4869	N JFET	2N4869	3-34	4-44
2N4869A	N JFET	2N4869A	3-34	4-44
2N4881	N JFET	–		
2N4882	N JFET	–		
2N4883	N JFET	–		
2N4884	N JFET	–		
2N4885	N JFET	–		
2N4886	N JFET	–		
2N4977	N JFET	2N5432		
2N4978	N JFET	2N5433		
2N4979	N JFET	2N5434		
2N5018	P JFET	2N5018	3-35	4-57
2N5019	P JFET	2N5019	3-35	4-57
2N5020	P JFET	2N2843		
2N5021	P JFET	2N2608		
2N5033	P JFET	2N2608		
2N5045	D N JFET	2N5045	3-36	4-34
2N5046	D N JFET	2N5046	3-36	4-34

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5047	D N JFET	2N5047	3-36	4-34
2N5078	N JFET	2N5078		
2N5103	N JFET	2N4416		
2N5104	N JFET	2N4416		
2N5105	N JFET	2N4416		
2N5114	P JFET	2N5114	3-37	4-57
2N5114JAN	P JFET	--	3-37	4-57
2N5114JANTX	P JFET	--	3-37	4-57
2N5115	P JFET	2N5115	3-37	4-57
2N5115JAN	P JFET	--	3-37	4-57
2N5115JANTX	P JFET	--	3-37	4-57
2N5116	P JFET	2N5116	3-37	4-57
2N5116JAN	P JFET	--	3-37	4-57
2N5116JANTX	P JFET	--	3-37	4-57
2N5158	N JFET	2N5434		
2N5159	N JFET	2N5433		
2N5163	N JFET	2N5163	3-38	
2N5196	D N JFET	2N5196	3-39	4-32
2N5197	D N JFET	2N5197	3-39	4-32
2N5198	D N JFET	2N5198	3-39	4-32
2N5199	D N JFET	2N5199	3-39	4-32
2N5245	N JFET	E4416		
2N5246	N JFET	E305		
2N5247	N JFET	E304		
2N5248	N JFET	2N5486		
2N5257	N JFET	2N5457		
2N5258	N JFET	2N5458		
2N5259	N JFET	2N5459		
2N5260	P JFET	--		
2N5265	P JFET	2N2608		
2N5266	P JFET	2N2608		
2N5267	P JFET	2N2608		
2N5268	P JFET	2N2608		
2N5269	P JFET	2N3331		
2N5270	P JFET	2N3331		
2N5277	N JFET	--		
2N5278	N JFET	--		
2N5358	N JFET	2N3686		
2N5359	N JFET	2N3686		
2N5360	N JFET	2N3685		
2N5361	N JFET	2N3684		
2N5362	N JFET	2N3684		
2N5363	N JFET	2N4222A		
2N5364	N JFET	2N4224		
2N5391	N JFET	2N4867A		
2N5392	N JFET	2N4868A		
2N5393	N JFET	2N4869A		
2N5394	N JFET	2N4869A		
2N5395	N JFET	2N4869A		
2N5396	N JFET	2N4869A		
2N5397	N JFET	U310		
2N5398	N JFET	U312		
2N5432	N JFET	2N5432	3-40	4-27
2N5433	N JFET	2N5433	3-40	4-27
2N5434	N JFET	2N5434	3-40	4-27
2N5452	D N JFET	2N5452	3-41	4-23
2N5453	D N JFET	2N5453	3-41	4-23
2N5454	D N JFET	2N5454	3-41	4-23
2N5457	N JFET	2N5457	3-42	4-42
2N5458	N JFET	2N5458	3-42	4-42
2N5459	N JFET	2N5459	3-42	4-42
2N5460	P JFET	--		
2N5461	P JFET	--		
2N5462	P JFET	--		
2N5463	P JFET	--		
2N5464	P JFET	--		
2N5465	P JFET	--		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5471	P JFET	--		
2N5472	P JFET	--		
2N5473	P JFET	--		
2N5474	P JFET	--		
2N5475	P JFET	--		
2N5476	P JFET	--		
2N5484	N JFET	2N5484	3-43	4-25
2N5485	N JFET	2N5485	3-43	4-25
2N5486	N JFET	2N5486	3-43	4-25
2N5515	D N JFET	2N5515	3-44	4-44
2N5516	D N JFET	2N5516	3-44	4-44
2N5517	D N JFET	2N5517	3-44	4-44
2N5518	D N JFET	2N5518	3-44	4-44
2N5519	D N JFET	2N5519	3-44	4-44
2N5520	D N JFET	2N5520	3-44	4-44
2N5521	D N JFET	2N5521	3-44	4-44
2N5522	D N JFET	2N5522	3-44	4-44
2N5523	D N JFET	2N5523	3-44	4-44
2N5524	D N JFET	2N5524	3-44	4-44
2N5543	N JFET	--		
2N5544	N JFET	--		
2N5545	D N JFET	2N5545	3-45	4-32
2N5545JAN	D N JFET	--	3-45	4-32
2N5545JANTX	D N JFET	--	3-45	4-32
2N5546	D N JFET	2N5546	3-45	4-32
2N5546JAN	D N JFET	--	3-45	4-32
2N5546JANTX	D N JFET	--	3-45	4-32
2N5547	D N JFET	2N5547	3-45	4-32
2N5547JAN	D N JFET	--	3-45	4-32
2N5547JANTX	D N JFET	--	3-45	4-32
2N5549	N JFET	2N4302		
2N5555	N JFET	2N5555	3-46	4-25
2N5556	N JFET	2N3685	3-47	4-42
2N5557	N JFET	2N3684	3-47	4-42
2N5558	N JFET	2N3684	3-47	4-42
2N5561	D N JFET	U401		
2N5562	D N JFET	U402		
2N5563	D N JFET	U404		
2N5564	D N JFET	2N5564	3-48	4-20
2N5565	D N JFET	2N5565	3-48	4-20
2N5566	D N JFET	2N5566	3-48	4-20
2N5592	N JFET	2N3822		
2N5593	N JFET	2N3822		
2N5594	N JFET	2N3822		
2N5638	N JFET	2N5638	3-49	4-20
2N5639	N JFET	2N5639	3-49	4-20
2N5640	N JFET	2N5640	3-49	4-20
2N5647	N JFET	2N4117A		
2N5648	N JFET	2N4117A		
2N5649	N JFET	2N4117A		
2N5653	N JFET	2N5653	3-50	4-20
2N5654	N JFET	2N5654	3-50	4-20
2N5668	N JFET	2N5668	3-51	4-25
2N5669	N JFET	2N5669	3-51	4-25
2N5670	N JFET	2N5670	3-51	4-25
2N5716	N JFET	--		
2N5717	N JFET	--		
2N5718	N JFET	--		
2N5797	P JFET	2N2608		
2N5798	P JFET	2N2608		
2N5799	P JFET	2N2608		
2N5800	P JFET	2N2608		
2N5801	N JFET	2N4393		
2N5802	N JFET	2N4393		
2N5803	N JFET	2N4392		
2N5902	D N JFET	2N5902	3-52	4-46
2N5903	D N JFET	2N5903	3-52	4-46

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5904	D N JFET	2N5904	3-52	4-46
2N5905	D N JFET	2N5905	3-52	4-46
2N5906	D N JFET	2N5906	3-52	4-46
2N5907	D N JFET	2N5907	3-52	4-46
2N5908	D N JFET	2N5908	3-52	4-46
2N5909	D N JFET	2N5909	3-52	4-46
2N5911	D N JFET	2N5911	3-54	4-52
2N5912	D N JFET	2N5912	3-54	4-52
2N5949	N JFET	U1837E		
2N5950	N JFET	U1837E		
2N5951	N JFET	U1837E		
2N5952	N JFET	E305		
2N5953	N JFET	E305		
2N6449	N JFET	–		
2N6450	N JFET	–		
2N6451	N JFET	2N4393		
2N6452	N JFET	2N4393		
2N6453	N JFET	2N4393		
2N6454	N JFET	2N4393		
2N6483	D N JFET	U401		
2N6484	D N JFET	U402		
2N6485	D N JFET	U404		
2N6550	N JFET	–		
2N6568	N JFET	U290		
2N6656	V MOS N ENH	2N6656		
2N6657	V MOS N ENH	2N6657		
2N6658	V MOS N ENH	2N6658		
2N6659	V MOS N ENH	2N6659		
2N6660	V MOS N ENH	2N6660		
2N6661	V MOS N ENH	2N6661		
2SJ17	P JFET	–		
2SJ18	P JFET	–		
2SJ19	P JFET	–		
2SJ20	P JFET	–		
2SJ22	P JFET	–		
2SK11	N JFET	–		
2SK12	N JFET	–		
2SK15	N JFET	–		
2SK16	N JFET	–		
2SK19	N JFET	–		
2SK23A	N JFET	–		
2SK30A	N JFET	–		
2SK33	N JFET	–		
2SK34	N JFET	–		
2SK37	N JFET	–		
2SK38A	N MOS DEPL	–		
2SK40	N JFET	–		
2SK41	N JFET	–		
2SK42	N JFET	–		
2SK43	N JFET	–		
2SK44	N JFET	–		
2SK45	N JFET	–		
2SK46	N JFET	–		
2SK47	N JFET	–		
2SK48	N JFET	–		
2SK49	N JFET	–		
2SK50	N JFET	–		
2SK54	N JFET	–		
2SK55	N JFET	–		
2SK59	N JFET	–		
2SK60	N JFET	–		
2SK61	N JFET	–		
2SK63	N JFET	–		
2SK65	N JFET	–		
2SK66	N JFET	–		
2SK68	N JFET	–		
2SK68A	N JFET	–		
2SK69	N JFET	–		
2SK70	N JFET	–		
2SK83	N JFET	–		
2SK84	N JFET	–		
2SK85	N JFET	–		
3N89	D G P JFET	–		
3N128	N MOS DEPL	–		
3N140	D G N MOS DEPL	–		
3N141	D G N MOS DEPL	–		
3N142	N MOS DEPL	–		
3N145	P MOS ENH	3N163		
3N146	P MOS ENH	3N163		
3N147	D P MOS ENH	M107		
3N148	D P MOS ENH	M107		
3N149	P MOS ENH	–		
3N150	P MOS ENH	–		
3N151	D P MOS ENH	–		
3N152	N MOS DEPL	–		
3N153	N MOS DEPL	–		
3N154	N MOS	–		
3N155	P MOS ENH	3N163		
3N155A	P MOS ENH	3N163		
3N156	P MOS ENH	3N163		
3N156A	P MOS ENH	3N163		
3N157	P MOS ENH	3N163		
3N157A	P MOS ENH	3N163		
3N158	P MOS ENH	3N163		
3N158A	P MOS ENH	3N163		
3N159	D N MOS DEPL	–		
3N160	P MOS ENH	–		
3N161	P MOS ENH	–		
3N162	P MOS ENH	–		
3N163	P MOS ENH	3N163	3-55	4-16
3N164	P MOS ENH	3N164	3-55	4-16
3N165	D P MOS ENH	M108		
3N166	D P MOS ENH	M108		
3N167	P MOS ENH	–		
3N168	P MOS ENH	–		
3N169	N MOS ENH	–		
3N170	N MOS ENH	–		
3N171	N MOS ENH	3N163		
3N172	P MOS ENH	M103		
3N173	P MOS ENH	M103		
3N174	P MOS ENH	3N163		
3N175	N MOS	–		
3N176	N MOS	–		
3N177	N MOS	–		
3N178	P MOS ENH	–		
3N179	P MOS ENH	–		
3N180	P MOS ENH	–		
3N181	P MOS ENH	–		
3N182	P MOS ENH	–		
3N183	P MOS ENH	–		
3N184	P MOS ENH	–		
3N185	P MOS ENH	–		
3N186	P MOS ENH	–		
3N187	D G N MOS DEPL	3N187	3-56	4-13
3N188	D P MOS ENH	M107		
3N189	D P MOS ENH	M107		
3N190	D P MOS ENH	M108		
3N191	D P MOS ENH	M108		
3N192	D G N MOS DEPL	–		
3N193	D G N MOS DEPL	–		
3N200	D G N MOS DEPL	3N201		
3N201	D G N MOS DEPL	3N201	3-58	4-13
3N202	D G N MOS DEPL	3N202	3-58	4-13
3N203	D G N MOS DEPL	3N203	3-58	4-13

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
3N204	D G N MOS DEPL	–		
3N205	D G N MOS DEPL	–		
3N206	D G N MOS DEPL	–		
2N307	D P MOS ENH	M108		
3N208	D P MOS ENH	–		
3N209	D G N MOS DEPL	–		
3N210	D G N MOS DEPL	–		
3N211	D G N MOS DEPL	–		
3N212	D G N MOS DEPL	–		
3N213	D G N MOS DEPL	–		
3N214	N MOS DEPL	–		
3N215	N MOS DEPL	–		
3N216	N MOS DEPL	–		
3N217	N MOS DEPL	–		
3SJ11A	P MOS ENH	–		
3SK14	D G N MOS DEPL	–		
3SK20	D G N MOS DEPL	–		
3SK21	N MOS DEPL	–		
3SK22	DG N JFET	–		
3SK28	DG N MOS DEPL	–		
3SK29	N MOS DEPL	–		
3SK30	D G N JFET	–		
3SK30A	D G N JFET	–		
3SK35	D G N NOS DEPL	–		
3SK38A	D G N MOS DEPL	–		
3SK39	D G N MOS DEPL	–		
3SK40	D G N MOS DEPL	–		
3SK44	D G N MOS DEPL	–		
3SK45	D G N MOS DEPL	–		
3SK49	4 N MOS DEPL	–		
3SK55	D G N MOS DEPL	–		
3SK59	D G N MOS DEPL	–		
3SK61	D G N MOS DEPL	–		
14T	N JFET	2N4224		
42T	N JFET	KE4392		
58T	N JFET	2N4302		
59T	N JFET	KE4416		
100S	N JFET	2N4304		
100U	N JFET	2N3684		
101S	N JFET	–		
102M	N JFET	2N5486		
102S	N JFET	2N4302		
103M	N JFET	2N5457		
103S	N JFET	2N5459		
104M	N JFET	2N5458		
105M	N JFET	2N5459		
105U	N JFET	2N4222		
106M	N JFET	2N5485		
107M	N JFET	2N5486		
110U	N JFET	2N3685		
115U	N JFET	2N4340		
120U	N JFET	2N3686		
125U	N JFET	2N4339		
130U	N JFET	2N3687		
135U	N JFET	2N4339		
155U	N JFET	2N4416		
182S	N JFET	2N4391		
183S	N JFET	2N3823		
197S	N JFET	2N4338		
198S	N JFET	2N4340		
199S	N JFET	2N4341		
200S	N JFET	2N4392		
200U	N JFET	2N3824		
201S	N JFET	2N4391		
202S	N JFET	2N4392		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
203S	N JFET	2N3821		
204S	N JFET	2N3821		
210U	N JFET	2N4416		
231S	D N JFET	2N3954		
232S	D N JFET	2N3955		
233S	D N JFET	2N3956		
234S	D N JFET	2N3957		
235S	D N JFET	2N3958		
241U	N JFET	2N4869		
250U	N JFET	2N4091		
251U	N JFET	2N4392		
588U	N JFET	2N4417		
703U	N JFET	2N4220		
704U	N JFET	2N4220		
705U	N JFET	2N4224		
707U	N JFET	2N4860		
714U	N JFET	2N3822		
734U	N JFET	2N4416		
734EU	N JFET	KE4416		
751U	N JFET	2N4340		
752U	N JFET	2N4340		
753U	N JFET	2N4341		
754U	N JFET	2N4340		
755U	N JFET	2N4341		
756U	N JFET	2N4340		
1277A	N JFET	2N3822		
1278A	N JFET	2N3821		
1279A	N JFET	2N3821		
1280A	N JFET	2N4224		
1281A	N JFET	2N3822		
1282A	N JFET	2N4341		
1283A	N JFET	2N4340		
1284A	N JFET	2N4222		
1285A	N JFET	2N3821		
1286A	N JFET	2N4220		
1325A	N JFET	2N4222		
1714A	N JFET	2N4340		
2000M	N JFET	2N3823		
2001M	N JFET	2N3823		
2078A	D N JFET	2N3955		
2079A	D N JFET	2N3955		
2080A	D N JFET	2N5546		
2081A	D N JFET	2N5546		
2093M	N JFET	2N3687		
2094M	N JFET	2N3686		
2095M	N JFET	2N3686		
2098A	D N JFET	2N5545		
2099A	D N JFET	2N5546		
2130U	D N JFET	2N5452		
2132U	D N JFET	2N3955		
2134U	D N JFET	2N3956		
2136U	D N JFET	2N3957		
2138U	D N JFET	2N3958		
2139U	D N JFET	2N3958		
2147U	D N JFET	2N3958		
2148U	D N JFET	2N3958		
2149U	D N JFET	2N3958		
4360TP	P JFET	–		
5033TP	P JFET	–		
40467A	N MOS	–		
40468	N MOS	–		
40468A	N MOS	–		
40559	N MOS	–		
40559A	N MOS	–		

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
40600	D G N MOS DEPL	–		
40601	N MOS	–		
40602	N MOS	–		
40603	N MOS	–		
40604	N MOS	–		
40673	D G N MOS DEPL	3N201		
40819	D G N MOS DEPL	–		
40820	D G N MOS DEPL	–		
40821	D G N MOS DEPL	–		
40822	D G N MOS DEPL	–		
40823	D G N MOS DEPL	–		
40841	D G N MOS DEPL	3N201		
A5T3821	N JFET	E305		
A5T3822	N JFET	E305		
A5T3823	N JFET	KE4416		
A5T3824	N JFET	E203		
A5T5460	P JFET	–		
A5T5461	P JFET	–		
A5T5462	P JFET	–		
A5T6449	N JFET	–		
A5T6450	N JFET	–		
A192	N JFET	2N4416		
AD830	D N JFET	U421		
AD831	D N JFET	U421		
AD832	D N JFET	U422		
AD833	D N JFET	U426		
AD833A	D N JFET	U423		
AD835	D N JFET	2N3921		
AD836	D N JFET	2N3921		
AD837	D N JFET	2N3922		
AD838	D N JFET	2N4085		
AD839	D N JFET	2N4085		
AD840	D N JFET	2N5196		
AD841	D N JFET	2N5197		
AD842	D N JFET	2N5199		
AD3954	D N JFET	2N3954		
AD3954A	D N JFET	2N3954A		
AD3955	D N JFET	2N3955		
AD3956	D N JFET	2N3956		
AD3957	D N JFET	2N3957		
AD3958	D N JFET	2N3958		
BC264	N JFET	2N4304		
BC264A	N JFET	2N4302		
BC264B	N JFET	2N4304		
BC264C	N JFET	2N4304		
BC264D	N JFET	KE4416		
BF244A	N JFET	BF244A*	3-60	4-25
BF244B	N JFET	BF244B*	3-60	4-25
BF244C	N JFET	BF244C*	3-60	4-25
BF245A	N JFET	BF244A*		
BF245B	N JFET	BF244B*		
BF245C	N JFET	BF244C*		
BF246	N JFET	BF246	3-61	4-20
BF246A	N JFET	BF246A*	3-61	4-20
BF246B	N JFET	BF246B*	3-61	4-20
BF246C	N JFET	BF246C*	3-61	4-20
BF247	N JFET	BF247	3-61	4-20
BF247A	N JFET	BF247A*	3-61	4-20
BF247B	N JFET	BF247B*	3-61	4-20
BF247C	N JFET	BF247C*	3-61	4-20
BF256LA	N JFET	BF256LA*	3-62	4-25
BF256LB	N JFET	BF256LB*	3-62	4-25
BF256LC	N JFET	BF256LC*	3-62	4-25
BF320	P JFET	–		
BF348	N JFET	2N5555		
BF800	N JFET	–		
BF801	N JFET	–		
BF802	N JFET	–		
BF900	D G N MOS DEPL	BF900	3-63	4-13
BFR45	N JFET	2N4416		
BFS21	D N JFET	2N5199		
BFS21A	D N JFET	2N5199		
BFS28	D G N MOS DEPL	3N201		
BFS67	N JFET	2N3821		
BFS67P	N JFET	2N4303		
BFS68	N JFET	2N3823		
BFS68P	N JFET	KE4416		
BFS70	N JFET	2N3821		
BFS71	N JFET	2N3822		
BFS72	N JFET	2N3823		
BFS73	N JFET	2N3821		
BFS74	N JFET	2N4856		
BFS75	N JFET	2N4857		
BFS76	N JFET	2N4858		
BFS77	N JFET	2N4859		
BSF78	N JFET	2N4860		
BFS79	N JFET	2N4861		
BFS80	N JFET	2N4416A		
BFW10	N JFET	2N3823		
BFW11	N JFET	2N3822		
BFW54	N JFET	2N3822		
BFW55	N JFET	2N3822		
BFW56	N JFET	2N4869		
BFW61	N JFET	2N4224		
BSV22	N JFET	2N4416		
BSV78	N JFET	2N4856A		
BSV80	N JFET	2N4858A		
BSV81	N MOS DEPL	2N3631		
C413N	N JFET	2N5434		
C673	N JFET	2N4341		
C674	N JFET	2N4341		
C680	N JFET	2N4338		
C680A	N JFET	2N4338		
C681	N JFET	2N4338		
C681A	N JFET	2N4338		
C682	N JFET	2N4339		
C682A	N JFET	2N4339		
C683	N JFET	2N4339		
C683A	N JFET	2N4339		
C684	N JFET	2N4220		
C684A	N JFET	2N4220		
C685	N JFET	2N4220		
C685A	N JFET	2N4220		
C6690	N JFET	2N3458		
C6691	N JFET	2N3458		
C6692	N JFET	2N3459		
CM600	N JFET	2N4092		
CM601	N JFET	2N4091		
CM602	N JFET	2N4091		
CM603	N JFET	2N4091		
CM640	N JFET	2N4093		
CM641	N JFET	2N4093		
CM642	N JFET	2N4093		
CM643	N JFET	2N4092		
CM644	N JFET	2N4092		
CM645	N JFET	2N4092		
CM646	N JFET	2N4092		
CM647	N JFET	2N4091		
CM650	N JFET	2N5432		
CM651	N JFET	2N5433		
CM652	N JFET	2N5432		
CM653	N JFET	2N5433		

*Siliconix European Part Number *also* Available Through U.S.A. Sales Outlets

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP600	N JFET	–		
CP601	N JFET	–		
CP602	N JFET	–		
CP603	N JFET	–		
CP640	N JFET	U296		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		
CP643	N JFET	2N5434		
CR022 Thru CR470 Referenced Under 1N Series				
DPAD1	D PAD N JFET	DPAD1	3-67	
DPAD2	D PAD N JFET	DPAD2	3-67	
DPAD5	D PAD N JFET	DPAD5	3-67	
DPAD10	D PAD N JFET	DPAD10	3-67	
DPAD20	D PAD N JFET	DPAD20	3-67	
DPAD50	D PAD N JFET	DPAD50	3-67	
DPAD100	D PAD N JFET	DPAD100	3-67	
DU4339	D N JFET	U235		
DU4340	D N JFET	U235		
E100	N JFET	E203		
E101	N JFET	E201		
E102	N JFET	E202		
E103	N JFET	E203		
E105	N JFET	E105	3-68	4-48
E106	N JFET	E106	3-68	4-48
E107	N JFET	E107	3-68	4-48
E108	N JFET	E108	3-69	4-27
E109	N JFET	E109	3-69	4-27
E110	N JFET	E110	3-69	4-27
E111	N JFET	E111	3-70	4-20
E111A	N JFET	E111A*	3-71	4-20
E112	N JFET	E112	3-70	4-20
E112A	N JFET	E112A*	3-71	4-20
E113	N JFET	E113	3-70	4-20
E113A	N JFET	E113A*	3-71	4-20
E114	N JFET	E114	3-72	4-52
E174	P JFET	E174	3-73	4-57
E175	P JFET	E175	3-73	4-57
E176	P JFET	E176	3-73	4-57
E177	P JFET	E177	3-73	4-57
E201	N JFET	E201	3-74	4-36
E202	N JFET	E202	3-74	4-36
E203	N JFET	E203	3-74	4-36
E204	N JFET	E204	3-75	4-36
E210	N JFET	E210	3-76	4-52
E211	N JFET	E211	3-76	4-52
E212	N JFET	E212	3-76	4-52
E230	N JFET	E230	3-77	4-44
E231	N JFET	E231	3-77	4-44
E232	N JFET	E232	3-77	4-44
E270	P JFET	E270	3-78	4-57
E271	P JFET	E271	3-78	4-57
E300	N JFET	E300	3-79	4-52
E304	N JFET	E304	3-80	4-25
E305	N JFET	E305	3-80	4-25
E308	N JFET	J308		
E309	N JFET	J309		
E310	N JFET	J310		
E400	D N JFET	E400	3-81	4-38
E401	D N JFET	E401	3-81	4-38
E402	D N JFET	E402	3-81	4-38
E410	D N JFET	E410	3-82	4-38
E411	D N JFET	E411	3-82	4-38
E412	D N JFET	E412	3-82	4-38
E413	D N JFET	E410		
E414	D N JFET	E411		
E415	D N JFET	E412		
E420	D N JFET	E420	3-83	4-52
E421	D N JFET	E421	3-83	4-52
E430	D N JFET	E430	3-84	4-50
E431	D N JFET	E431	3-84	4-50
E500	CL N JFET	E500	3-85	4-22
E501	CL N JFET	E501	3-85	4-22
E502	CL N JFET	E502	3-85	4-22
E503	CL N JFET	E503	3-85	4-22
E504	CL N JFET	E504	3-85	4-22
E505	CL N JFET	E505	3-85	4-22
E506	CL N JFET	E506	3-85	4-22
E507	CL N JFET	E507	3-85	4-22
EPAD50	DD N JFET	EPAD50*	3-86	
EPAD100	DD N JFET	EPAD100*	3-86	
EPAD200	DD N JFET	EPAD200*	3-86	
EPAD500	DD N JFET	EPAD500*	3-86	
FE100	N JFET	2N3821		
FE100A	N JFET	2N3821		
FE102	N JFET	2N4119		
FE102A	N JFET	2N4119		
FE104	N JFET	2N4118		
FE104A	N JFET	2N4118		
FE200	N JFET	2N3821		
FE202	N JFET	2N3821		
FE204	N JFET	2N3821		
FE300	N JFET	2N3822		
FE302	N JFET	2N3821		
FE304	N JFET	2N3821		
FEO654A	N JFET	2N5486		
FEO654B	N JFET	2N5485		
FE3819	N JFET	2N3819		
FE5245	N JFET	–		
FE5246	N JFET	–		
FE5247	N JFET	–		
FE5457	N JFET	2N5457		
FE5458	N JFET	2N5458		
FE5459	N JFET	2N5459		
FE5484	N JFET	2N5484		
FE5485	N JFET	2N5485		
FE5486	N JFET	2N5486		
FF102	FF N JFET	–		
FF108	FF N JFET	–		
FF400	FF N JFET	–		
FF409	FF N JFET	–		
FF411	FF N JFET	–		
FF600	FF N JFET	–		
FF617	FF N JFET	–		
FM1100	D N JFET	–		
FM1100A	D N JFET	–		
FM1101	D N JFET	–		
FM1101A	D N JFET	–		
FM1102	D N JFET	–		
FM1102A	D N JFET	–		
FM1103	D N JFET	–		
FM1103A	D N JFET	–		
FM1104	D N JFET	–		
FM1104A	D N JFET	–		
FM1105	D N JFET	–		
FM1105A	D N JFET	–		
FM1106	D N JFET	–		
FM1106A	D N JFET	–		
FM1107	D N JFET	–		

*Siliconix European Part Number *also* Available Through U.S.A. Sales Outlets

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
FM1107A	D N JFET	–		
FM1108A	D N JFET	–		
FM1109	D N JFET	–		
FM1109A	D N JFET	–		
FM1110	D N JFET	–		
FM1110A	D N JFET	–		
FM1111	D N JFET	–		
FM1111A	D N JFET	–		
FM1200	D N JFET	–		
FM1201	D N JFET	–		
FM1202	D N JFET	–		
FM1203	D N JFET	–		
FM1204	D N JFET	–		
FM1205	D N JFET	–		
FM1206	D N JFET	–		
FM1207	D N JFET	–		
FM1208	D N JFET	–		
FM1209	D N JFET	–		
FM1210	D N JFET	–		
FM1211	D N JFET	–		
FM3954	D N JFET	2N3954		
FM3954A	D N JFET	2N3954A		
FM3955	D N JFET	2N3955		
FM3955A	D N JFET	2N3955A		
FM3956	D N JFET	2N3956		
FM3957	D N JFET	2N3957		
FM3958	D N JFET	2N3958		
FT0654A	N JFET	2N5486		
FT0654B	N JFET	2N5486		
FT0654C	N JFET	2N4221		
FT0654D	N JFET	2N4221		
FT701	D P MOS ENH	–		
FT703	P MOS ENH	–		
FT704	P MOS ENH	3N163		
FT3820	P JFET	–		
GET5457	N JFET	2N5457		
GET5458	N JFET	2N5458		
GET5459	N JFET	2N5459		
HDIG1030	P MOS ENH	3N163		
ID100	D PAD N JFET	DPAD1		
ID101	D PAD N JFET	DPAD10		
IMF3954	D N JFET	2N3954		
IMF3954A	D N JFET	2N3954A		
IMF3955	D N JFET	2N3955		
IMF3955A	D N JFET	2N3955A		
IMF3956	D N JFET	2N3956		
IMF3957	D N JFET	2N3957		
IMF3958	D N JFET	2N3958		
IMF6485	D N JFET	U405		
IT100	P JFET	2N5116		
IT101	P JFET	2N5114		
IT108	N JFET	2N5486		
IT109	N JFET	U310		
IT110	P JFET	–		
IT111	P JFET	–		
IT1700	P MOS ENH	3N163		
IT1701	P MOS ENH	M103		
IT1702	P MOS ENH	3N163		
IT1750	N MOS ENH	M117		
IT2700	D P MOS ENH	M108		
IT2701	D P MOS ENH	M108		
ITE500	CL N JFET	E500		
ITE501	CL N JFET	E501		
ITE502	CL N JFET	E502		
ITE503	CL N JFET	E503		
ITE504	CL N JFET	E504		
ITE505	CL N JFET	E505		
ITE506	CL N JFET	E506		
ITE507	CL N JFET	E507		
ITE3066	N JFET	E202		
ITE3067	N JFET	E201		
ITE3068	N JFET	E201		
ITE4117	N JFET	2N4117		
ITE4118	N JFET	2N4118		
ITE4119	N JFET	2N4119		
ITE4338	N JFET	E201		
ITE4339	N JFET	E201		
ITE4340	N JFET	E202		
ITE4341	N JFET	E203		
ITE4391	N JFET	E111		
ITE4392	N JFET	E112		
ITE4393	N JFET	E113		
ITE4416	N JFET	KE4416		
ITE4867	N JFET	E230		
ITE4868	N JFET	E231		
ITE4869	N JFET	E232		
J108	N JFET	J108	3-87	4-27
J109	N JFET	J109	3-87	4-27
J110	N JFET	J110	3-87	4-27
J111	N JFET	J111	3-88	4-20
J112	N JFET	J112	3-88	4-20
J113	N JFET	J113	3-88	4-20
J174	P JFET	J174	3-89	4-57
J175	P JFET	J175	3-89	4-57
J176	P JFET	J176	3-89	4-57
J177	P JFET	J177	3-89	4-57
J270	P JFET	J270	3-90	4-57
J271	P JFET	J271	3-90	4-57
J308	N JFET	J308	3-91	4-50
J309	N JFET	J309	3-91	4-50
J310	N JFET	J310	3-91	4-50
J401	D N JFET	J401	3-92	4-34
J402	D N JFET	J402	3-92	4-34
J403	D N JFET	J403	3-92	4-34
J404	D N JFET	J404	3-92	4-34
J405	D N JFET	J405	3-92	4-34
J406	D N JFET	J406	3-92	4-34
J410	D N JFET	J410	3-94	4-38
J411	D N JFET	J411	3-94	4-38
J412	D N JFET	J412	3-94	4-38
J1401	D N JFET	J1401	3-95	4-34
J1402	D N JFET	J1402	3-95	4-34
J1403	D N JFET	J1403	3-95	4-34
J1404	D N JFET	J1404	3-95	4-34
J1405	D N JFET	J1405	3-95	4-34
J1406	D N JFET	J1406	3-95	4-34
KE3684	N JFET	2N3684		
KE3685	N JFET	2N3685		
KE3686	N JFET	2N3686		
KE3687	N JFET	2N3687		
KE3823	N JFET	E304		
KE3970	N JFET	KE4391		
KE3971	N JFET	KE4392		
KE3972	N JFET	KE4393		
KE4091	N JFET	KE4391		
KE4092	N JFET	KE4392		
KE4093	N JFET	KE4393		
KE4220	N JFET	2N5457		
KE4221	N JFET	2N5457		
KE4222	N JFET	2N5459		
KE4223	N JFET	E304		
KE4224	N JFET	E304		
KE4391	N JFET	KE4391	3-96	4-20
KE4392	N JFET	KE4392	3-96	4-20

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
KE4393	N JFET	KE4393	3-96	4-20
KE4416	N JFET	KE4416	3-97	4-25
KE4856	N JFET	KE4391		
KE4857	N JFET	KE4392		
KE4858	N JFET	KE4393		
KE4859	N JFET	KE4391		
KE4860	N JFET	KE4392		
KE4861	N JFET	KE4393		
KE5103	N JFET	E305		
KE5104	N JFET	E304		
KE5105	N JFET	E304		
LDF603	N JFET	2N4221A		
LDF604	N JFET	2N4221A		
LDF605	N JFET	2N4221A		
M100	N MOS DEPL	M100	3-98	4-1
M101	N MOS DEPL	M101	3-98	4-1
M103	P MOS ENH	M103	3-99	4-5
M104	P MOS ENH	M104	3-100	4-18
M106	D P MOS ENH	M106	3-101	4-2
M107	D P MOS ENH	M107	3-101	4-3
M108	D P MOS ENH	M108	3-101	4-4
M113	P MOS ENH	M113	3-102	4-8
M114	P MOS ENH	M114	3-103	4-6
M116	N MOS ENH	M116	3-104	4-9
M117	N MOS ENH	M117	3-104	4-11
M119	P MOS ENH	–		
M163	P MOS ENH	3N163		
M164	P MOS ENH	3N164		
M511	P MOS ENH	MEM511C		
M517	P MOS ENH	M103		
MEM511	P MOS ENH	MEM511	3-105	4-15
MEM511C	P MOS ENH	MEM511C	3-106	4-5
MEM517	P MOS ENH	–		
MEM517A	P MOS ENH	–		
MEM517B	P MOS ENH	–		
MEM517C	P MOS ENH	–		
MEM520	P MOS ENH	3N164		
MEM520C	P MOS ENH	3N164		
MEM550	D P MOS ENH	–		
MEM550C	D P MOS ENH	M107		
MEM550F	P MOS ENH	–		
MEM551	D P MOS ENH	M108		
MEM551C	D P MOS ENH	M108		
MEM554	D G N MOS DEPL	3N203		
MEM554C	D G N MOS DEPL	3N203		
MEM556	P MOS ENH	M104		
MEM556C	P MOS ENH	M104		
MEM557	N MOS DEPL	–		
MEM557C	N MOS DEPL	–		
MEM560	P MOS DEPL	M113		
MEM560C	P MOS DEPL	M113		
MEM561	P MOS ENH	3N163		
MEM561C	P MOS ENH	3N163		
MEM562	N MOS ENH	M117		
MEM562C	N MOS ENH	M117		
MEM563	N MOS ENH	M117		
MEM563C	N MOS ENH	M117		
MEM564C	D G N MOS DEPL	3N201		
MEM571C	N MOS DEPL	–		
MEM575	P MOS ENH	–		
MEM614	D G N MOS DEPL	–		
MEM615A	D G N MOS DEPL	–		
MEM616	D G N MOS DEPL	–		
MEM617	D G N MOS DEPL	–		
MEM618	D G N MOS DEPL	–		
MEM630	D G N MOS DEPL	–		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
MEM631	D G N MOS DEPL	–		
MEM632	D G N MOS DEPL	–		
MEM655	N MOS DEPL	–		
MEM656A	N MOS DEPL	–		
MEM660	N MOS ENH	–		
MEM711	N MOS ENH	–		
MEM712	P MOS ENH	–		
MEM804	N MOS ENH	–		
MEM806	P MOS ENH	3N163		
MEM806A	P MOS ENH	3N163		
MEM807	P MOS ENH	M103		
MEM807A	P MOS ENH	M103		
MEM809	P MOS ENH	–		
MEM814	P MOS ENH	M103		
MEM954	D P MOS ENH	–		
MEM954A	D P MOS ENH	–		
MEM954B	D P MOS ENH	–		
MEM955	D P MOS ENH	–		
MEM955A	D P MOS ENH	–		
MEM955B	D P MOS ENH	–		
MFE120	D G N MOS DEPL	–		
MFE121	D G N MOS DEPL	–		
MFE122	D G N MOS DEPL	–		
MFE130	D G N MOS DEPL	3N201		
MFE131	D G N MOS DEPL	3N201		
MFE132	D G N MOS DEPL	3N201		
MFE590	D G N DMOS ENH	–		
MFE591	D G N DMOS ENH	–		
MFE823	P MOS ENH	MFE823	3-107	4-16
MFE824	N MOS ENH	M100		
MFE2000	N JFET	2N4416		
MFE2001	N JFET	2N4416		
MFE2004	N JFET	2N4093		
MFE2005	N JFET	2N4092		
MFE2006	N JFET	2N4091		
MFE2007	N JFET	2N4860		
MFE2008	N JFET	2N4859		
MFE2009	N JFET	2N4859		
MFE2010	N JFET	2N5434		
MFE2011	N JFET	2N5433		
MFE2012	N JFET	2N5432		
MFE2093	N JFET	2N3687		
MFE2094	N JFET	2N3686		
MFE2095	N JFET	2N3685		
MFE3001	N MOS DEPL	M100		
MFE3002	N MOS ENH	M117		
MFE3003	P MOS ENH	3N164		
MFE3004	N MOS DEPL	–		
MFE3005	N MOS DEPL	–		
MFE3006	D G N MOS DEPL	3N203		
MFE3007	D G N MOS DEPL	3N203		
MFE3008	D G N MOS DEPL	3N203		
MFE3020	D P MOS ENH	M107		
MFE3021	D P MOS ENH	M107		
MFE4007	P JFET	2N2608		
MFE4008	P JFET	2N2608		
MFE4009	P JFET	2N3329		
MFE4009A	P JFET	–		
MFE4010A	P JFET	–		
MFE4010	P JFET	2N3330		
MFE4011	P JFET	2N3330		
MFE4012A	P JFET	–		
MFE4012	P JFET	2N3331		
MK10	N JFET	2N4416		
MMF1	D N JFET	2N3921		
MMF2	D N JFET	2N3921		

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
MMF3	D N JFET	2N3921		
MMF4	D N JFET	2N3921		
MMF5	D N JFET	2N3921		
MMF6	D N JFET	2N3921		
MMT3823	N JFET	2N3823		
MPF102	N JFET	MPF102	3-108	4-25
MPF103	N JFET	2N5457		
MPF104	N JFET	2N5458		
MPF105	N JFET	2N5459		
MPF106	N JFET	2N5485		
MPF107	N JFET	2N5486		
MPF108	N JFET	MPF108	3-109	4-25
MPF109	N JFET	MPF109	3-110	4-42
MPF111	N JFET	MPF111	3-111	4-42
MPF112	N JFET	MPF112	3-112	4-25
MPF130	D G N MOS DEPL	—		
MPF131	D G N MOS DEPL	—		
MPF161	P JFET	—		
MPF256	N JFET	J309		
MPF820	N JFET	U310		
MPF970	P JFET	J174		
MPF971	P JFET	J176		
MPF1000	D G N MOS DEPL	—		
MPF4391	N JFET	J111		
MPF4392	N JFET	J112		
MPF4393	N JFET	J113		
NF500	N JFET	2N4416		
NF501	N JFET	2N4416		
NF506	N JFET	2N4416		
NF510	N JFET	2N4393		
NF511	N JFET	2N4393		
NF520	N JFET	2N3684		
NF521	N JFET	2N3686		
NF522	N JFET	2N3684		
NF523	N JFET	2N3686		
NF530	N JFET	2N4341		
NF531	N JFET	2N4339		
NF532	N JFET	2N4341		
NF533	N JFET	2N4339		
NF580	N JFET	2N5432		
NF581	N JFET	2N5432		
NF582	N JFET	2N5433		
NF583	N JFET	2N5434		
NF584	N JFET	2N5433		
NF585	N JFET	2N4859		
NF4302	N JFET	2N4302		
NF4303	N JFET	2N4303		
NF4304	N JFET	2N4304		
NF4445	N JFET	2N5432		
NF4446	N JFET	2N5433		
NF4447	N JFET	2N5432		
NF4448	N JFET	2N5433		
NF5163	N JFET	2N5163		
NF5457	N JFET	2N5457		
NF5458	N JFET	2N5458		
NF5459	N JFET	2N5459		
NF5484	N JFET	2N5484		
NF5485	N JFET	2N5485		
NF5486	N JFET	2N5486		
NF5555	N JFET	2N5555		
NF5638	N JFET	2N5638		
NF5639	N JFET	2N5639		
NF5640	N JFET	2N5640		
NF5653	N JFET	2N5653		
NF5654	N JFET	2N5654		
NPD8301	D N JFET	NPD8301	3-113	4-38
NPD8302	D N JFET	NPD8302	3-113	4-38
NPD8303	D N JFET	NPD8303	3-113	4-38
P102	FF P JFET	—		
P236	FF N JFET	—		
P237	FF N JFET	—		
P238	FF N JFET	—		
P1086E	P JFET	P1086E	3-115	4-57
P1087E	P JFET	P1087E	3-115	4-57
P1117E	P JFET	—		
P1118E	P JFET	—		
P1119E	P JFET	—		
PAD1	PAD N JFET	PAD1	3-116	
PAD2	PAD N JFET	PAD2	3-116	
PAD5	PAD N JFET	PAD5	3-116	
PAD10	PAD N JFET	PAD10	3-116	
PAD20	PAD N JFET	PAD20	3-116	
PAD50	PAD N JFET	PAD50	3-116	
PAD100	PAD N JFET	PAD100	3-116	
PF510	P JFET	2N5018		
PF511	P JFET	2N5014		
SU2078	D N JFET	U425		
SU2079	D N JFET	U425		
SU2098	D N JFET	2N5197		
SU2098A	D N JFET	2N5197		
SU2098B	D N JFET	2N5196		
SU2099	D N JFET	2N5197		
SU2099A	D N JFET	2N5197		
SU2365	D N JFET	U401		
SU2365A	D N JFET	U401		
SU2366	D N JFET	U402		
SU2366A	D N JFET	U402		
SU2367	D N JFET	U403		
SU2367A	D N JFET	U403		
SU2368	D N JFET	U404		
SU2368A	D N JFET	U404		
SU2369	D N JFET	U405		
SU2369A	D N JFET	U405		
SU2410	D N JFET	U424		
SU2411	D N JFET	U425		
SU2412	D N JFET	U426		
T100	N JFET TMP	T100	3-117	4-49
T300	N JFET TMP	T300	3-117	4-49
TD5902	D N JFET	2N5902		
TD5902	D N JFET	2N5902		
TD5902A	D N JFET	2N5902		
TD5903	D N JFET	2N5903		
TD5903A	D N JFET	2N5903		
TD5904	D N JFET	2N5904		
TD5904A	D N JFET	2N5904		
TD5905	D N JFET	2N5905		
TD5905A	D N JFET	2N5905		
TD5906	D N JFET	2N5906		
TD5906A	D N JFET	2N5906		
TD5907	D N JFET	2N5907		
TD5907A	D N JFET	2N5907		
TD5908	D N JFET	2N5908		
TD5908A	D N JFET	2N5908		
TD5909	D N JFET	2N5909		
TD5909A	D N JFET	2N5909		
TD5911	D N JFET	2N5911		
TD5911A	D N JFET	2N5911		
TD5912	D N JFET	2N5912		
TD5912A	D N JFET	2N5912		
TIS14	N JFET	2N4340		
TIS25	D N JFET	U401		
TIS26	D N JFET	U402		
TIS27	D N JFET	U404		
TIS41	N JFET	2N4859		
TIS58	N JFET	E305		
TIS59	D N JFET	U1837E		
TIS73	N JFET	KE4391		

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
TIS74	N JFET	KE4392		
TIS75	N JFET	KE4393		
TIS78	N JFET	—		
TIS79	N JFET	—		
TIS88	N JFET	2N5486		
TIS88A	N JFET	TIS88A*	3-120	4-25
TIXS33	N JFET	—		
TIXS41	N JFET	2N4859		
TIXS42	N JFET	KE4393		
TN4117	N JFET	2N4117		
TN4117A	N JFET	2N4117A		
TN4118	N JFET	2N4118		
TN4118A	N JFET	2N4118A		
TN4119	N JFET	2N4119		
TN4119A	N JFET	2N4119A		
TN4338	N JFET	2N4338		
TN4339	N JFET	2N4339		
TN4340	N JFET	2N4340		
TN4341	N JFET	2N4341		
TP5114	P JFET	2N5114		
TP5115	P JFET	2N5115		
TP5116	P JFET	2N5116		
U89	D G P JFET	—		
U110	P JFET	2N2608		
U112	P JFET	2N2608		
U133	P JFET	2N2608		
U146	P JFET	2N2608		
U147	P JFET	2N2608		
U148	P JFET	2N2608		
U149	P JFET	2N2609		
U168	P JFET	2N2609		
U182	N JFET	2N4857		
U183	N JFET	2N3824		
U184	N JFET	2N5078		
U197	N JFET	2N4339		
U198	N JFET	2N4340		
U199	N JFET	2N4341		
U200	N JFET	U200	3-121	4-20
U201	N JFET	U201	3-121	4-20
U202	N JFET	U202	3-121	4-20
U221	N JFET	2N4391		
U222	N JFET	2N4391		
U231	D N JFET	U231	3-122	4-32
U232	D N JFET	U232	3-122	4-32
U233	D N JFET	U233	3-122	4-32
U234	D N JFET	U234	3-122	4-32
U235	D N JFET	U235	3-122	4-32
U240	N JFET	2N5432		
U241	N JFET	2N5433		
U242	N JFET	2N5432		
U243	N JFET	2N5433		
U244	N JFET	—		
U248	D N JFET	2N5902		
U248A	D N JFET	2N5906		
U249	D N JFET	2N5903		
U249A	D N JFET	2N5907		
U250	D N JFET	2N5904		
U250A	D N JFET	2N5908		
U251	D N JFET	2N5905		
U251A	D N JFET	2N5909		
U254	N JFET	2N4859		
U255	N JFET	2N4860		
U256	N JFET	2N4861		
U257	D N JFET	U257	3-123	4-52
U266	N JFET	—		
U273	N JFET	2N4118A		
U273A	N JFET	2N4118A		
U274	N JFET	2N4119A		
U274A	N JFET	2N4119A		
U275	N JFET	2N4119A		
U275A	N JFET	2N4119A		
U280	D N JFET	U231		
U281	D N JFET	U231		
U282	D N JFET	U232		
U283	D N JFET	U232		
U284	D N JFET	U233		
U285	D N JFET	U234		
U290	N JFET	U290	3-124	4-48
U291	N JFET	U291	3-124	4-48
U295	N JFET	U295	3-125	4-48
U296	N JFET	U296	3-125	4-48
U300	P JFET	2N5114		
U301	P JFET	2N5115		
U304	P JFET	U304	3-126	4-57
U305	P JFET	U305	3-126	4-57
U306	P JFET	U306	3-126	4-57
U308	N JFET	U308	3-127	4-50
U309	N JFET	U309	3-127	4-50
U310	N JFET	U310	3-127	4-50
U311	N JFET	U311	3-129	4-50
U312	N JFET	U312	3-130	4-52
U314	N JFET	U314	3-131	4-52
U315	N JFET	U315	3-131	4-52
U316	N JFET	U316	3-133	4-50
U317	N JFET	U317	3-133	4-50
U320	N JFET	U320	3-134	4-27
U321	N JFET	U321	3-134	4 27
U322	N JFET	U322	3-134	4-27
U328	N JFET	—		
U329	N JFET	—		
U330	N JFET	—		
U331	N JFET	—		
U350	4 N JFET	U350	3-136	4-50
U401	D N JFET	U401	3-138	4-34
U402	D N JFET	U402	3-138	4-34
U403	D N JFET	U403	3-138	4-34
U404	D N JFET	U404	3-138	4-34
U405	D N JFET	U405	3-138	4-34
U406	D N JFET	U406	3-138	4-34
U421	D N JFET	U421	3-140	4-40
U422	D N JFET	U422	3-140	4-40
U423	D N JFET	U423	3-140	4-40
U424	D N JFET	U424	3-140	4-40
U425	D N JFET	U425	3-140	4-40
U426	D N JFET	U426	3-140	4-40
U430	D N JFET	U430	3-142	4 50
U431	D N JFET	U431	3-142	4-50
U508	N JFET	U508	3-143	4-29
U1177	N JFET	2N4220A		
U1178	N JFET	2N3821		
U1179	N JFET	2N3821		
U1180	N JFET	2N4221A		
U1181	N JFET	2N4220A		
U1182	N JFET	2N3821		
U1277	N JFET	2N3684		
U1278	N JFET	2N3685		
U1279	N JFET	2N3686		
U1280	N JFET	2N3684		
U1281	N JFET	2N3822		
U1282	N JFET	2N4341		
U1283	N JFET	2N4340		
U1284	N JFET	2N4341		

*Siliconix European Part Number *also* Available Through U.S.A. Sales Outlets

FET cross reference and substitution guide (cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U1285	N JFET	2N4220		
U1286	N JFET	2N4341		
U1287	N JFET	2N4092		
U1321	N JFET	2N3966		
U1322	N JFET	2N4221A		
U1323	N JFET	2N4221A		
U1324	N JFET	2N4220A		
U1325	N JFET	2N4222		
U1420	N JFET	2N3821		
U1421	N JFET	2N3822		
U1422	N JFET	2N3822		
U1714	N JFET	2N4340		
U1715	N JFET	—		
U1837E	N JFET	U1837E	3-144	4-25
U1897E	N JFET	U1897E	3-145	4-20
U1898E	N JFET	U1898E	3-145	4-20
U1899E	N JFET	U1899E	3-145	4-20
U1994E	N JFET	U1994E	3-146	4-25
U2047E	N JFET	KE4416		
U3000	N JFET	2N4341		
U3001	N JFET	2N4339		
U3002	N JFET	2N4338		
U3010	N JFET	2N4341		
U3011	N JFET	2N4340		
U3012	N JFET	2N4338		
UC20	N JFET	2N3686		
UC21	N JFET	2N3687		
UC40	P JFET	2N2608		
UC41	P JFET	2N2608		
UC100	N JFET	2N3684		
UC110	N JFET	2N3685		
UC115	N JFET	2N4340		
UC120	N JFET	2N3686		
UC130	N JFET	2N3687		
UC155	N JFET	2N4416		
UC200	N JFET	2N3824		
UC201	N JFET	2N3824		
UC210	N JFET	2N4416		
UC220	N JFET	2N3822		
UC240	N JFET	2N4869		
UC241	N JFET	2N4869		
UC250	N JFET	2N4091		
UC251	N JFET	2N4392		
UC300	P JFET	2N2608		
UC310	P JFET	2N2843		
UC320	P JFET	2N2843		
UC330	P JFET	2N2843		
UC340	P JFET	2N2843		
UC400	P JFET	2N3331		
UC401	P JFET	2N5116		
UC410	P JFET	2N3330		
UC420	P JFET	2N3329		
UC450	P JFET	2N5114		
UC451	P JFET	2N5116		
UC588	N JFET	2N4417		
UC703	N JFET	2N4220		
UC704	N JFET	2N4220		
UC705	N JFET	2N4224		
UC707	N JFET	2N4860		
UC714	N JFET	2N3822		
UC714E	N JFET	E203		
UC734	N JFET	2N4416		
UC734E	N JFET	KE4416		
UC751	N JFET	2N4340		
UC752	N JFET	2N4340		
UC753	N JFET	2N4341		
UC754	N JFET	2N4340		
UC755	N JFET	2N4341		
UC756	N JFET	2N4340		
UC805	P JFET	2N3331		
UC807	N JFET	2N4860		
UC814	P JFET	2N3331		
UC851	P JFET	2N2608		
UC853	P JFET	2N2608		
UC854	P JFET	2N2608		
UC855	P JFET	2N2609		
UC1700	P MOS ENH	3N163		
UC1764	P MOS ENH	3N163		
UC2130	D N JFET	2N5452		
UC2132	D N JFET	2N3955		
UC2134	D N JFET	2N3956		
UC2136	D N JFET	2N3957		
UC2138	D N JFET	2N3958		
UC2139	D N JFET	2N3958		
UC2147	D N JFET	2N3958		
UC2148	D N JFET	2N3958		
UC2149	D N JFET	2N3958		
UC2766	D P MOS ENH	—		
VCR2N	N JFET	VCR2N	3-147	4-20
VCR3P	P JFET	VCR3P	3-147	4-56
VCR4N	N JFET	VCR4N	3-147	4-36
VCR5P	P JFET	VCR5P	3-147	4-54
VCR6P	P JFET	2N5116		
VCR7N	N JFET	VCR7N	3-147	4-46
VCR10N	N JFET	—		
VCR11N	D N JFET	—		
VCR12N	4 N JFET	—		
VCR13N	4 N JFET	—		
VCR20N	4 N JFET	—		
VMP1	V MOS N ENH	2N6657		
VMP2	V MOS N ENH	2N6660		
VMP4	V MOS N ENH	VMP4		
VMP11	V MOS N ENH	2N6656		
VMP12	V MOS N ENH	2N6658		
VMP21	V MOS N ENH	2N6659		
VMP22	V MOS N ENH	2N6661		
W245A	N JFET	W245A*	3-149	4-25
W245B	N JFET	W245B*	3-149	4-25
W245C	N JFET	W245C*	3-149	4-25
W300	N JFET	W300*	3-150	4-52
W300A	N JFET	W300A*	3-150	4-52
W300B	N JFET	W300B*	3-150	4-52
W300C	N JFET	W300C*	3-150	4-52
W300D	N JFET	W300D*	3-150	4-52
WK5457	N JFET	2N5457		
WK5458	N JFET	2N5458		
WK5459	N JFET	2N5459		

***Siliconix European Part Number *also* Available Through U.S.A. Sales Outlets**

product information

Siliconix products are divided into three basic categories:

Standard Products, Modified Standard Products, Custom Products

- **Standard Products** — All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391". It will also appear in that form on the price list, published separately.

- **Examples of Modified Standard Products are:**

Electrical Specials — Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

Mechanical Specials — Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

High Reliability Specials — Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-750B. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** — Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to customer products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 246-8000.

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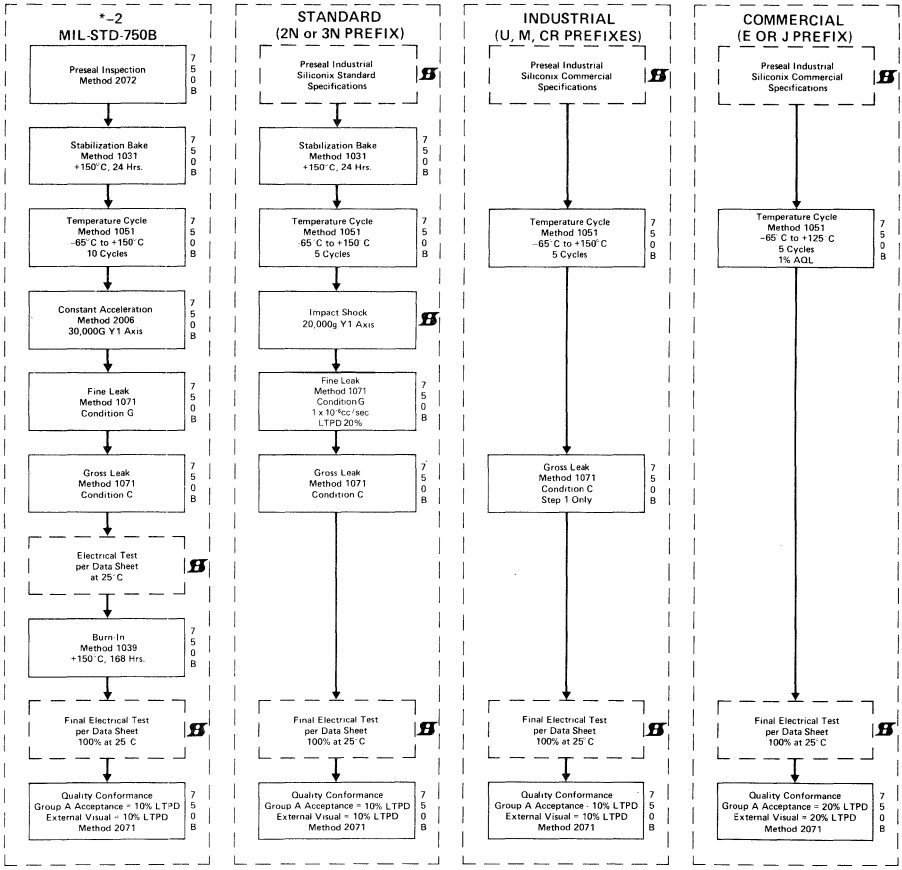
Device identification table

FETs

Prefix	XXX	XXXX	Prefix	XXX	XXXX
BF	European Transistor Standard		SU	Special P-Channel JFET	
CR	Si Standard N-Channel Current Regulator		T	Si Standard N-Channel Trans/MIC Preamp	
DPAD	Si Standard Dual JFET Diode		U	Si Standard FET	
E	Si Standard Epoxy Cased FET	Special Epoxy Cased FET	VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
FN		Special N-Channel JFET			
J	Si Standard TO-92 Cased FET Si Standard 8 Lead Dual In-Line Package – Plastic	Special TO-92 Cased FET Special 8 Lead Dual In-Line Package – Plastic	VMP	VMOS Power FET N-Channel	
KE		Si Standard Epoxy	VN		VMOS Power FET N-Channel
M	Si Standard MOSFET		2N		JEDEC-Registered Device
MU	Si Special MOSFET		3N	JEDEC-Registered Device	
PAD	Si Standard JFET Diode				

The above prefix list does not include some second source products supplied by Siliconix. Refer to FET Cross Reference and Substitution Guide or current price list for availability of these devices.

process option flow chart



*SIMILAR TO JANTXV SCREENING PER MIL-S-19500.

selector guides

index 2

tips on selecting the right FET for your application

The "Preferred Parts Selector Guide" will provide you direct reference to Siliconix part numbers for very general categories of application.

IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 2-2 "How to Choose the Correct FET for Your Application". Using this guide, determine the important FET parameters.

2. Next, turn to page 2-3 "JFET Geometry Selector Guide". Using this guide, choose the appropriate geometry.

3. Once you have chosen a geometry, turn to the "Geometry Characteristics" section 4 of the catalog. Here you make the choice of a suitable part number.

4. Now that you have the part number, you will find complete electrical specifications of these products in the "Data Sheets" section 3 of the catalog.

IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Preferred Parts Selector Guide", pages 2-6, 7, 8, and 9 to determine the proper part number(s).

2. Double-check your choices against the data sheets, and select the part most suited for your application.

how to choose the correct FET for your application

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters	
AMPLIFIER	Audio	Low noise ($\overline{e_n}$), g_{fs}/g_{os}	Voltage amplification factor μ = g_{fs}/g_{os} = $\Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times	Noise, $\overline{e_n}$, NF while using high level signals RF parameters while operating below RF frequencies Capacitance & switching times while operating in audio and lower frequencies
	Buffer	Low I_G, high g_{fs}			
	Differential	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	High Input Impedance	Very low I_G (eg., MOSFET)			
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters			
	FET Input Op Amp	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude			
	Low Supply Voltage	Low $V_{GS(off)}$			
	Low Noise	Low $\overline{e_n}$, $\overline{i_n}$, low 1/f noise, low NF			
	Preamplifier	Operate near I_{DZO}, high g_{fs}/I_D ratio			
	Video	High g_{fs}/C_{iss} ratio, NF			
CONSTANT CURRENT SOURCE	Current Limiting	Low g_{oss}, low $V_{GS(off)}$, high BV_{GSS}		g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters capacitance	
	Reference Current Source				
	Biasing				
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}		$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$	
	UHF				
	Double Balanced	Matching characteristics			
OSCILLATORS	Class A	Good g_{fs} at operating frequency			
	Class C	Low C_{iss} for VHF operation			
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs Capacitance	g_{fs} g_{os}	
	Choppers	$r_{DS}/I_{D(off)}$ switching efficiency			
	Commutators	Low C_{rss}			
	Digital	Fast switching time			
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}			
	Sample and Hold	Low C_{rss}			
VOLTAGE CONTROLLED RESISTORS	Gain Control	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}	
	Amplitude Stability				
	Attenuators				

JFET geometry selector guide

Once you have chosen the major FET parameters, you will find selecting the optimum JFET geometry is easy. If you are familiar with Field Effect Transistors, start your selection using the characteristic graphs on page 2-4. You will find the $V_{GS(off)}$ vs I_{DSS} graph the most meaningful, since it shows – in order of ascending active area – the complete line of Siliconix junction FETs.

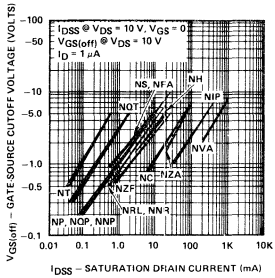
To give you an idea how this guide works, let's find the most suitable geometry for a 70 ohm ON-resistance analog switch which will be required to operate as close as 5 volts from the negative power supply. The power supply restraint requires a maximum $V_{GS(off)}$ of 5 volts. Examining the $R_{DS(on)}$ vs $V_{GS(off)}$ figure, you will find the NC, NIP, and NVA geometries meet the R_{on} and $V_{GS(off)}$ requirements. In order to minimize your cost, choose the geometry having the least chip area, that is the NC. You will find characteristic data and part numbers in the Geometry Characteristics section of the catalog. Below are the most important parameter inter-relationships expressed in analytical form.

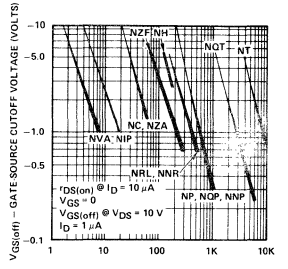
USEFUL JFET PARAMETER RELATIONSHIPS (APPROX.)

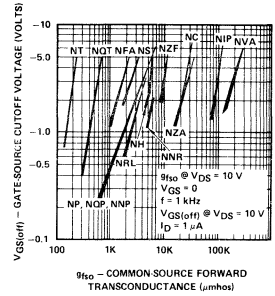
g_{fso}	$= K \frac{I_{DSS}}{V_{GS(off)}}$	Forward transconductance as a function of I_{DSS} and $V_{GS(off)}$ at zero gate-source voltage (K = 1.1 to 2.5; typically = 2 for N-channel junction FET)
g_{fs}	$= g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$	Variation of g_{fs} with gate bias
g_{fs}	$= g_{fso}\sqrt{I_D/I_{DSS}}$	Variation of g_{fs} with drain current
$V_{GS(off)}$	$= \frac{2\, I_{DSS}}{g_{fso}}$	Gate-Source cutoff voltage in terms of I_{DSS} and g_{fso}
V_{DS}	$\approx V_{GS(off)} \left(\frac{I_D}{I_{DSS}}\right)^{1/2}$	Drain voltage at which drain current saturates
r_{DS}	$\simeq \frac{1}{g_{fs}}$	Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e. in the triode region
r_{DS}	$\simeq \frac{K\,\lvert V_{GS(off)}\rvert^2}{I_{DSS}\,\lvert V_{GS(off)} - V_{GS}\rvert}$	K = 0.4 to 0.9 Variation of drain resistance in the triode region
I_D	$= I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$	Variation of drain current with gate-source voltage. The square law transfer characteristic.

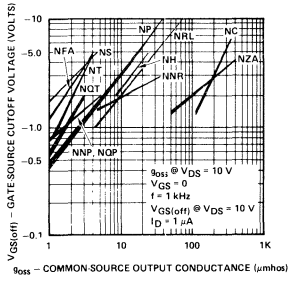
JFET geometry selector guide (cont'd)

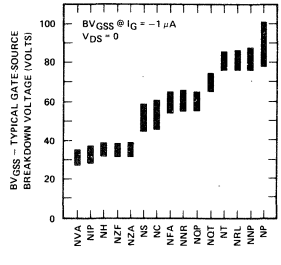
n-channel JFETs

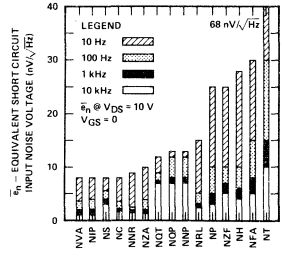


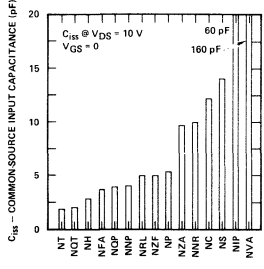


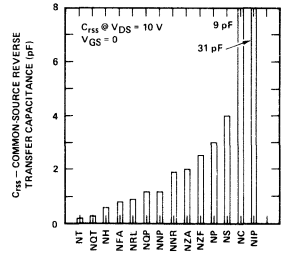






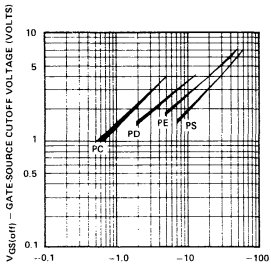


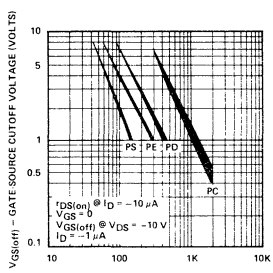


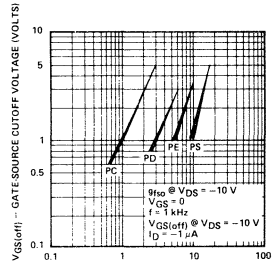


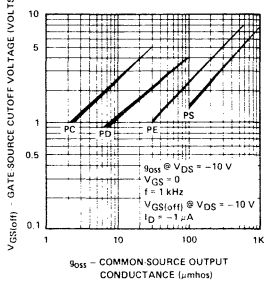
JFET geometry selector guide (cont'd)

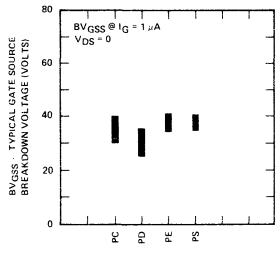
p-channel JFET

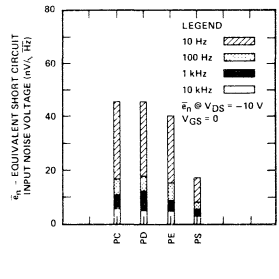


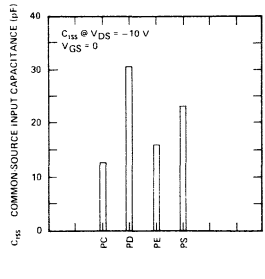


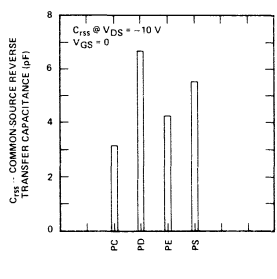






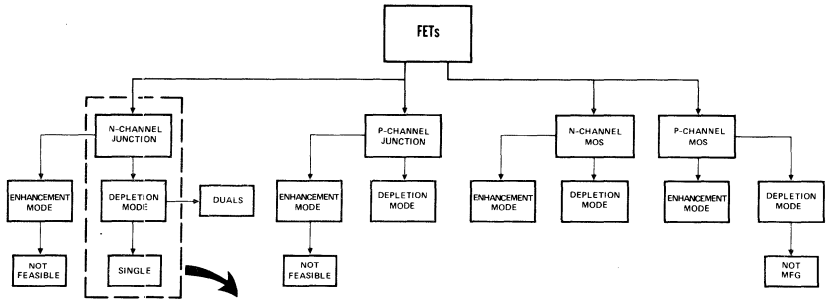






2

preferred parts selector guide



N-CHANNEL, DEPLETION MODE, JUNCTION FET(2)

SINGLE

Low Leakage $I_{G(max)}$	Low Noise $\bar{e}_n$ max at 10 Hz	VHF/UHF Amplifier Mixer/Oscillator	Switches $R_{DS(max)}$		General Purpose $g_{fs(min)}$ µmhos	Miscellaneous
1 pA 2N4117-19A **10 pA** 2N4117-19	**10 nV/√Hz** 2N4867A-69A **20 nV/√Hz** 2N4867-69 **30 nV/√Hz** E230-32(1)	**Low Gain** 2N3823 2N4416-16A PN4417(3) 2N5484-86(1) 2N5668-70 E304-5(1) KE4416(1) MPF102(1) **Med Gain** 2N5078 E114(1) E210-12(1) E300(1) U312 J315 **High Gain** J308-10(1) U308-10 J316-17(3) U320-22	**2.5 Ω** U290 U295 **3 Ω** E105(1) **5 Ω** 2N5432 **6 Ω** E106(1) **7 Ω** 2N5433 U291 U296 **8 Ω** J108(1) E107-8(1) **10 Ω** 2N5434 **12 Ω** J109(1) E109(1) **18 Ω** J110(1) E110(1) **25 Ω** 2N4856-56A 2N4859-59A **30 Ω** 2N3970 2N4091 2N4391 2N5638(1) J111(1) E111(1) KE4391(1) U1897E(1)	**40 Ω** 2N4857-57A 2N4860-60A **50 Ω** 2N4092 2N5653 J112(1) E112(1) U202 U1898E(1) **60 Ω** 2N3971 2N4392 2N4858-58A 2N4861-61A 2N5639(1) KE4392(1) **75 Ω** U201 **80 Ω** 2N4093 U1899E(1) **100 Ω** 2N3972 2N4393 2N5640(1) 2N5654(1) J113(1) E113(1) KE4393(1) **150 Ω** 2N5555(1) **250 Ω** 2N3824	**500 µmhos** 2N3687 E201(1) **600 µmhos** 2N4338 **800 µmhos** 2N4339 **1,000 µmhos** 2N3686 2N4220-20A 2N4302, 4(1) 2N5457(1) E202(1) **1,300 µmhos** 2N4340 **1,500 µmhos** 2N3685 2N3821 2N5458(1) E203(1) **2,000 µmhos** 2N3684 2N4221-21A 2N4303(1) 2N4341 2N5163(1) 2N5459(1) **2,500 µmhos** 2N4222-22A **3,000 µmhos** 2N3822 For higher g_{fs}, refer to VHF/UHF amplifiers	**Voltage Controlled Resistors** VCR2N, 4N, 7N **Current Limiter/Regulator** CR022 through CR470 E500-7(1) **Low Leakage Diodes** PAD1, 2, 5, 10, 20, 50, 100 **Transducer Preamplifier** T100-T300

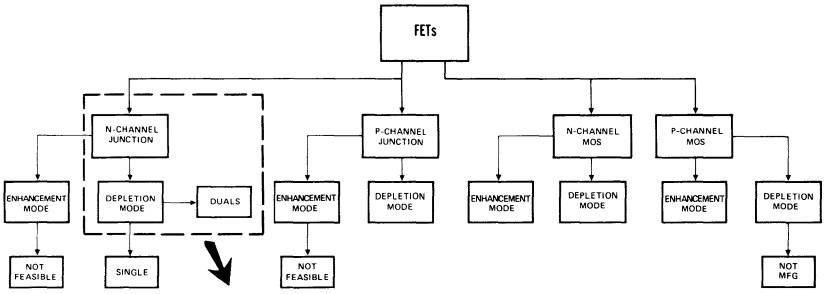
Notes

(1) Plastic case

(2) Customer specials of all parts are available through factory

(3) Strip-line package

preferred parts selector guide (cont'd)



N-CHANNEL, DEPLETION MODE, JUNCTION FET(2)

DUAL

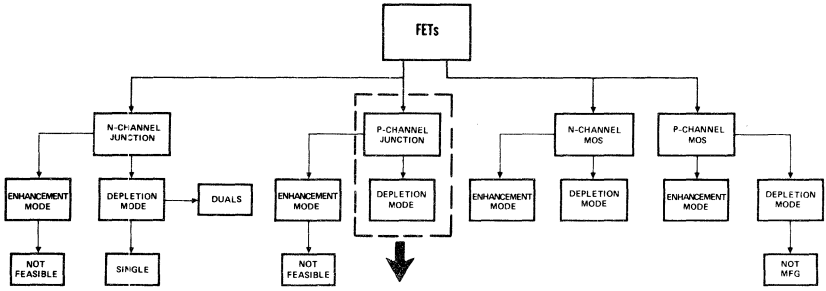
Low Leakage $I_{G(max)}$	Low Noise $\overline{e}_{n(max)}$	VHF/UHF Amp	Switch	General Purpose	Miscellaneous
0.1 pA U421-3 **0.5 pA** U424-6 **1 pA** 2N5902-5 **3 pA** 2N5906-9 **15 pA** 2N5196-99 **50 pA** 2N3954-58 U231-35	**15 nV** 2N5520-24 **20 nV** U401-6 **30 nV** 2N5515-19 **50 nV** 2N5564-66	2N5564-66 2N5911-12 U257 U430-31 E430-31(1) E420-21(1)	2N5564-66	2N3921-22 2N4084-85 2N5196-99 2N5045-47 2N5545-47 J401-6 J410-12 J1401-6 U401-6 U231-35 E400-2(1) E410-12(1) 2N3954-58 2N3954A-55A	**Dual Low Leakage Diodes** DPAD1-100

Notes

(1) Plastic case

(2) Customer specials of all parts are available through factory

preferred parts selector guide (cont'd)



P-CHANNEL, DEPLETION MODE, JUNCTION FET(2)

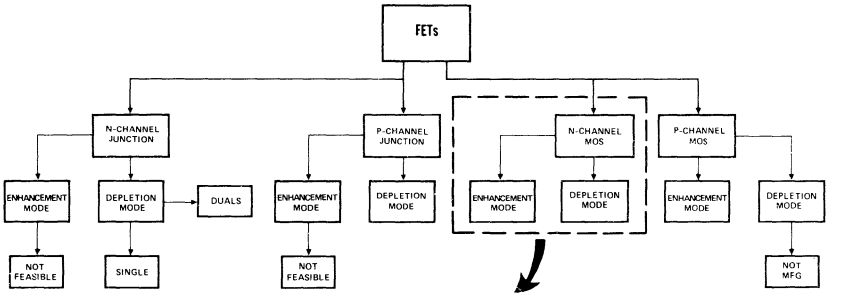
SINGLE

Low Leakage	Low Noise	VHF/UHF Amplifier	Switches $R_{DS(max)}$	General Purpose	Miscellaneous by Application
Not a usual application for P-Channel Junction FETs Suggest using N-Channel Junction FET	E270-1(1) J270-1(1) U304-6	E270-71(1) J270-71(1)	**75 Ω** 2N5018 2N5114 P1086E(1) **85 Ω** U304 J174(1) E174(1) **100 Ω** 2N5115 **110 Ω** U305 **125 Ω** J175(1) E175(1) **150 Ω** 2N3386 2N5019 2N5116 P1087E(1) **180 Ω** U306 2N3384 **250 Ω** J176(1) E176(1) **300 Ω** J177(1) E177(1)	**Low g_{fs}** 2N2608 2N2843 **Med. g_{fs}** 2N2609 2N2844 U149 **High g_{fs}** 2N3382, 84, 86 E270-1(1) J270-71(1)	**Voltage Controlled Resistors** VCR3P, 5P **Current Limiter** (None) **Current Regulator** (None)

Notes
(1) Plastic case
(2) Customer specials of all parts are available through factory

DUAL Not Available

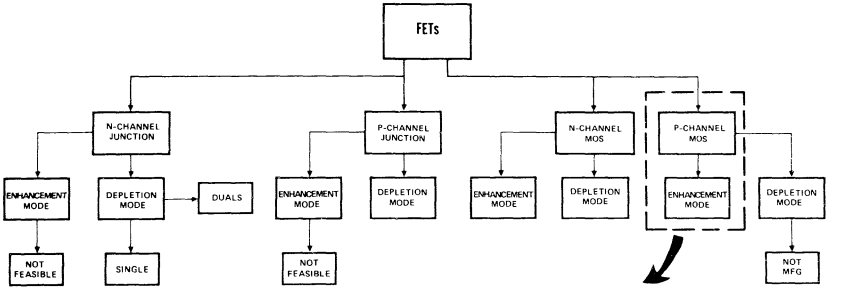
preferred parts selector guide (cont'd)



N-CHANNEL, MOSFET(2)

ENHANCEMENT MODE			
Switch	**VHF/UHF Amplifier**	**General Purpose**	**Dual**
M116(3) M117	None	M116(3) M117	None

DEPLETION MODE		
Switch	**General Purpose**	**Dual-Gate VHF/UHF**
M100 M101	2N3631 M100 M101	3N187(3) 3N201(3) 3N202(3) 3N203(3) BF900(1)



P-CHANNEL, ENHANCEMENT MODE, MOSFET(2)

Switch	VHF/UHF Amplifier	General Purpose	Dual*
Low R_{DS} M103(3) M113(3) M114(3) 3N163-4 High R_{DS} M104(3)	None	MEM511-11C(3) 3N163-4	M106(3) M107(3) M108

Notes
(1) Plastic case
(2) Customer specials of all parts are available thru factory
(3) Gate protective diode(s)

* The M106 and M107 both have common sources
The M108 has separate sources

JFET and MOSFET chips and wafers selector guide

Introduction

Most JFETs and MOSFETs listed in this catalog are available in chip and wafer form. Siliconix is a large volume supplier of chips to the Hybrid industry. Purchasers of Siliconix FET chips range from High Reliability to Commercial users.

Purchase Options

Standard chips packed in flat cavity containers. – Refer to the current Price List for those chips that can be supplied. Certain dual FETs are not available in chip form because their parameter limits cannot be tested, or guaranteed in chip form.

Wafer form. – Most standard available chips can be supplied. Consult the factory or local sales office for ordering information.

Special selections. – Chips and wafers with many variations of electrical parameters and methods of packing can be supplied. Consult the factory or local sales office for details.

Visual Inspection

Standard. – All standard FET chips are supplied with 100% visual sort to the criteria of MIL-STD-750B Method 2072. Wafers are supplied to MIL-STD-750B visual screen to the extent that it is applicable.

Special. – Chips and wafers can be supplied with Level A visual or other similar criteria as a special selection from the factory. Consult the factory or local sales office for details.

Incoming Inspection Criteria

Siliconix guarantees visual and electrical criteria to the LTPD specified above under Electrical Test Capability. Acceptance of chips and wafers shall be based only on incoming inspection. Copies of detailed recommended incoming inspection procedures are available upon request from Siliconix.

Physical Data

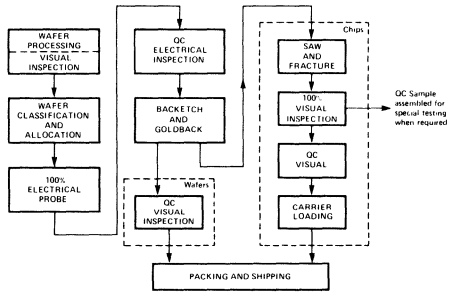
Chips are supplied with nominal length and width dimensions. The standard thickness is .007 inches (.178 mm) plus or minus .001 inches (.025 mm). Special detail on length and width dimensions and bonding pad orientation is given in the geometry description section of this catalog.

All standard chips are gold backed. This gold backing is approximately 1500 angstroms thick.

All chips are covered with passivation except on the scribe line and bonding pad areas. The passivation is silicon dioxide (non-crystalline glass) approximately 8000 angstroms thick on the covered area of the chip.

All chip metalization is aluminum. The approximate thickness is 12,000 angstroms. The basic material of chips is silicon.

Chip and Wafer Processing



Chip and Wafer Packaging

Standard FET chips are packed as individual chips, individual pairs, or individual quads in the flat waffle carrier illustrated in Figure 1.

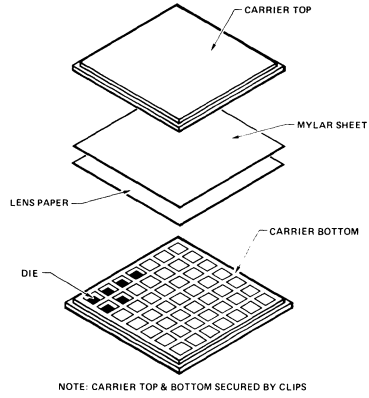


Figure 1

Wafers are packed in the configuration in Figure 2.

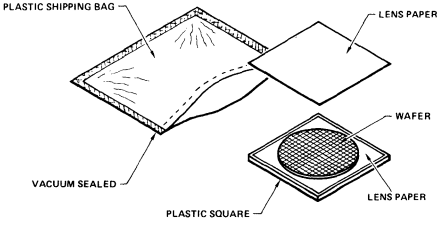


Figure 2

JFET and MOSFET chips and wafers selector guide (cont'd)

Electrical Test Capability

In general 100% electrical probe on wafers is limited to dc parameters plus small signal forward transconductance (g_{fs}) which are specified at 25°C ambient temperature. High and low temperature tests, small signal parameters other than forward transconductance, capacitances, and RF parameters, cannot be tested in chip form. These parameters are either guaranteed or qualified to an LTPD based upon characterization of an assembled sample from wafers or diffusion lots.

Recommended Chip Assembly Procedure

Chips supplied in chip form do not require cleaning prior to assembly. Chips supplied in wafer form should be cleaned after sawing or scribing, and fracturing. Contact Siliconix if you have any questions on cleaning procedures.

Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides. When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases handling precautions may be necessary for junction FET chips.

Chips can be die attached either eutectically, or by conductive epoxy when lower temperatures are necessary. Gold-silicon eutectic occurs at temperatures between 385°C and 425°C.

Bonding of wires from chip pads to posts can be thermocompression using gold wire or ultrasonic using aluminum wire.

The table indicates the method of guaranteeing the specification, and the sampling plan used at final Q.C. inspection. Siliconix will select test method when more than one method exists.

Parameter	100% Probed	Guaranteed by Test Margins	Wafer Prescreen	Measured On Packaged Sample	Guaranteed by Process Sample Test on Request
Breakdown Voltages	X				
Leakage Currents	⩾100 pA		<100 pA		
I_{DSS}, $I_{D(on)}$	⩽40 mA	>40 mA	>40 mA		
$V_{GS(off)}$ V_{GS}, $V_{gs(th)}$	X				
$I_{D(off)}$	⩾100 pA		<100 pA		
g_{fs}	<8.0 mmho	<8.0 mmho			
g_{os}		X	X		
$r_{ds(on)}$	⩾5 Ω	⩾5 Ω	<5 Ω		
$\bar{e}_N$			X	If Required	
$\lvert V_{GS1} - V_{GS2}\rvert$	Monolithic Duals		Two Chip Duals		
$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$				50% LTPD	
g_{fs1}/g_{fs2}			X		
I_{DSS1}/I_{DSS2}			X		
$g_{os1} - g_{os2}$			X		
CMRR				20% LTPD	
Capacitance					X
Switching Times					X
QC Inspection	**15% LTPD**	**20% LTPD**	**20% LTPD**		

2

pc board layout and construction for low leakage applications

In order to realize the full capability of these devices in circuits that are sensitive to very low currents, considerable care should be exercised in PC board layout and construction techniques. If proper care is not taken, board leakage currents can easily become much larger than the leakage currents of the devices themselves, especially under conditions of high temperature and humidity. Excessive leakage currents can be produced by poor quality boards, socket leakage, poor board layout, imperfectly cleaned boards, or improperly applied or cured protective coatings.

It is important to start with quality PC boards which have high resistivity and low susceptance to moisture. Boards of teflon or polycarbonate composition exhibit these attributes and are preferred. Glass-epoxy boards are less desirable because they will absorb moisture, and if used must be protected with a conformal coating.

The use of sockets should be avoided wherever possible since the pin-to-pin isolation is often not great enough to prevent small leakage currents from occurring. These currents can significantly degrade device performance in low leakage applications. If sockets cannot be avoided use the highest quality available, preferably teflon.

In laying out PC boards, care should be taken to keep pins and runs which are sensitive to very low currents away from pins and runs which will be at significantly higher or lower voltages. The most common leakage current problems occur between pins sensitive to low current levels and nearby pins at or near one of the supply voltages. Thus, if the isolation between critical pins and nearby high or low voltage pins is increased, leakage is minimized.

In order to reduce leakage currents, it is very important that all PC boards and experimental breadboards be thoroughly cleaned with a solvent after construction. A recommended procedure is to wash each board in an ultrasonic cleaning bath of alcohol, trichloroethylene, or some other commercial solvent, and to blow dry with compressed air. The purpose of this is to remove all skin oils (the greatest cause of leakage in improperly cleaned boards), solder fluxes, and other films and residues left over from the construction process which can cause gross leakage problems and erratic device behavior, especially at temperatures above 85°C.

For best results, the thoroughly cleaned boards should be protected against dirt, conductive films, and humidity by the application of a conformal coating. Urethane and Dow Corning's R-4-3117 Silicone are easy to use and offer sufficient protection under most operating conditions. Epoxy results in a more durable coating but care must be taken to insure that it is cured properly; an improperly cured layer of epoxy will make the high temperature leakage problem worse. Union Carbide's Parylene also results in a relatively durable coating.

The ultimate leakage protection method consists of printed circuit metalization guard rings driven from a low impedance buffer amplifier whose output is at the same potential as the pin being protected. This completely eliminates board surface leakage at critical pins by removing any difference in potential, but it is difficult to implement due to the extra buffer amplifier required and the tight PC board metalization spacings encountered.

Pin-to-pin resistance of a typical 8 pin MINI-DIP mounted in a two sided glass-epoxy PC board under various conditions of board cleanliness.

Condition of Board	Resistance @ 25°C (Ω)	Resistance @ 70°C (Ω)
Dirty	2×10^9	1×10^8
Cleaned	8×10^9	2×10^9
Cleaned and then contaminated	2×10^9	1×10^8
Cleaned and coated	6×10^9	1×10^9
Cleaned and coated and then contaminated	6×10^9	1×10^9

data sheets

index 3

p-channel JFETs *designed for . . .*

■ General Purpose Amplifiers

Performance Curves PC PD
See Section 4

BENEFITS

- JAN Approved Version Available

TO-18
See Section 5

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) . . . . . 30 V
Gate Current, Forward Biased (Note 1) . . . . . 50 mA
Total Device Dissipation (Derate 2 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . −65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2608 Min	2N2608 Max	2N2609 Min	2N2609 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	nA	V_{GS} = 30 V, V_{DS} = 0 V	
2					10		30	μA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	1	4	1	4	V	V_{DS} = -5 V, I_D = 1 μA	
5		I_{DSS}	Saturation Drain Current	-0.90	-4.50	-2	-10	mA	V_{DS} = -5 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		2500		μmho	V_{DS} = -5 V, V_{GS} = 0 V	f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8		NF	Noise Figure		3		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1MΩ	f = 1 kHz

*JEDEC Registered Data

PC PD

NOTES:
1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

p-channel JFETs *designed for . . .*

■ Small-Signal Amplifiers

Performance Curves PC PD See Section 4

BENEFITS

- Low Supply Voltage Operation $V_{GS(off)}$ Typically 1.2 V

TO-18
See Section 5

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) . . . . . 30 V
Gate Current, Forward Biased (Note 1) . . . . . 50 mA
Total Device Dissipation (Derate 2mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2843 Min	2N2843 Max	2N2844 Min	2N2844 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	nA	V_{GS} = 30 V, V_{DS} = 0	
2					10		30	μA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		1.7		1.7	V	V_{DS} = -5 V, I_D = -1 μA	
5		I_{DSS}	Saturation Drain Current	-200	-1000	-440	-2200	μA	V_{DS} = -5 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	540		1400		μmho	V_{DS} = -5 V, V_{GS} = 0	f = 1 kHz
7		C_{iss}	Common-Source Capacitance		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8		NF	Noise Figure		3		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
				PC		PD				

*JEDEC Registered Data

NOTES:
1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V.
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

p-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **Analog Multipliers**
- **Modulators**

Performance Curves PC See Section 4

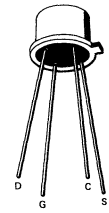
BENEFITS

- Ease of Amplifier Design
  I_{DSS} & G_{fs} Closely Specified

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 1) . . . . . 20 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below)
25°C Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 230°C

TO-72
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3329 Min	2N3329 Max	2N3330 Min	2N3330 Max	2N3331 Min	2N3331 Max	2N3332 Min	2N3332 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		0.01		0.01		0.01		0.01	pA	V_{GS} = 10 V, V_{DS} = 0	
2					10		10		10		10		V_{GS} = 10 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	20		20		20		20		V	I_G = 10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		5		6		8		6		V_{DS} = -15 V, I_D = -10 μA	
5		I_{DSS}	Saturation Drain Current	-1	-3	-2	-6	-5	-15	-1	-6	mA	V_{DS} = -10 V, V_{GS} = 0	
6		$r_{DS(on)}$	Drain-Source ON Resistance		1000		800		600			Ω	I_D = -100 μA, V_{GS} = 0	
7	DYNAMIC	g_{is}	Common-Source Input Conductance		0.2		0.2		0.2		0.2	μmho	V_{DS} = -10 V; 2N3329: I_D = -1 mA; 2N3330: I_D = -2 mA; 2N3331: I_D = -5 mA; 2N3332: I_D = -1 mA	f = 1 kHz
8		g_{rs}	Common-Source Reverse Transfer Conductance		0.1		0.1		0.1		0.1			
9		g_{os}	Common-Source Output Conductance		20		40		100		20			
10		g_{fs}	Common-Source Forward Transconductance	1000	2000	1500	3000	2000	4000	1000	2200			
11				900		1350		1800		900				f = 10MHz
12		C_{iss}	Common-Source Input Capacitance		20		20		20		20	pF	V_{DS} = -10 V, V_{GS} = 1 V	f = 1 MHz
13		NF	Noise Figure		3		3		4		1	dB	V_{DS} = -5 V, I_D = -1 mA, R_{gen} = 1 MΩ	f = 1 kHz
14		NF	Noise Figure								5		V_{DS} = -5 V, I_D = -1 mA, R_{gen} = 10 MΩ	f = 10 Hz

*JEDEC registered data

PC

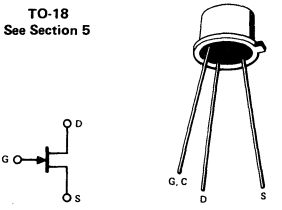
NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2.0 mW/°C

n-channel JFETs *designed for . . .*

Performance Curves NP
See Section 4

■ Small-Signal Low Power Applications

TO-18
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . –40 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . –65 to +175°C
Maximum Operating Temperature . . . . . 150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3368 Min	2N3368 Max	2N3369 Min	2N3369 Max	2N3370 Min	2N3370 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-5		-5	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1.5		-1.5		-1.5	μA		100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-11.5		-6.5		-3.2		V_{DS} = 20 V, I_D = 1 μA	
5		$I_{D(off)}$	Drain Cutoff Current		5 (-12.0)		5 (-7.0)		5 (-3.5)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
6		I_{DSS}	Saturation Drain Current	2.0	12.0	0.5	2.5	0.1	0.6	mA	V_{DS} = 30 V (Note 3), V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	600	2500	300	2500	μmho	V_{DS} = 30 V (Note 3), V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		80		30		15		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		3		3		3	pF		
10		C_{iss}	Common-Source Input Capacitance		20		20		20		V_{DS} = 8 V, V_{GS} = 0	

*JEDEC registered data. **NP**

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 150°C free-air temperature at rate of 2.1 mW/°C.
3. To minimize heating on high I_{DSS} units, this parameter is measured during a 2 ms interval 100 ms after power is applied. **(Not a JEDEC condition.)**

p-channel JFETs *designed for . . .*

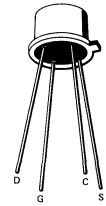
- **Analog Switches**
- **Choppers**
- **Commutators**
- **Amplifiers**

Performance Curves PE See Section 4

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 150\ \Omega$ (2N3386)

TO-72
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain Voltage (Note 1) . . . . . 30 V
Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Storage Temperature Range . . . . . -65 to +200°C
Total Dissipation at 25°C T_A (Note 2) . . . . . 300 mW

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3382 Min	2N3382 Max	2N3384 Min	2N3384 Max	2N3386 Min	2N3386 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		15		15		15	nA	V_{GS} = 30 V V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		15		15		15	μA	V_{GS} = 5 V V_{DS} = 0	T_A = 150°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 μA V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 3)	1.0	5.0	4.0	5.0	4.0	9.5	V	V_{DS} = -5 V I_D = -1 μA	
5	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-3.0	-30.0	-15.0	-30.0	-15.0	-50.0	mA	V_{DS} = -10 V V_{GS} = 0	
6	STATIC	$I_{D(off)}$	Drain Cutoff Current		-2 (6)		-2 (6)		-2.5 (10)	nA (V)	V_{DS} = -5 V V_{GS} = ( )	
7	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		300		180		150	Ω	V_{GS} = 0 V_{DS} = 0	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	4500	12,500	7500	12,500	7500	15,000	μmho	V_{DS} = -10 V V_{GS} = 0	
9	DYNAMIC	C_{sgs} + C_{dgs}	Source-Gate Capacitance Plus Drain-Gate Capacitance		6.0		6.0		6.0	pF	V_{DS} = 0 V_{GS} = 10 V	f = 140 kHz
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance	16 Typ							V_{DS} = -5 V V_{GS} = 1 V	

PE

*JEDEC registered data.

NOTE:
1. Due to symmetrical geometry, units may be operated with source and drain leads interchanged.
2. Derate linearly to +175°C at 2 mW/°C
3. Pulsewidth = 2 ms, duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

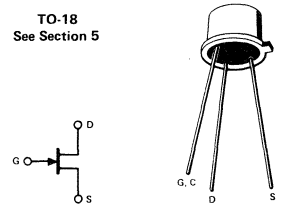
- **Small-Signal Amplifiers**
- **Switches**

Performance Curves NP
See Section 4

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-18
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . −50 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . −65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3436 Min	2N3436 Max	2N3437 Min	2N3437 Max	2N3438 Min	2N3438 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.5		-0.5		-0.5	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1.0		-1.0		-1.0	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		1.0 (-10.0)		1.0 (-5.0)		1.0 (-2.5)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-9.8		-4.8		-2.3	V	V_{DS} = 20 V, I_D = 1 μA	
6		I_{DSS}	Saturation Drain Current	3.0	15.0	0.8	4.0	0.2	1.0	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500	10,000	1500	6000	800	4500	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		35		20		5		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		6		6		6	pF		
10		C_{iss}	Common-Source Input Capacitance		18 (10)		18 (6)		18 (4)	pF (V)	V_{GS} = 0 V, V_{DS} = ( )	
11		NF	Noise Figure		2		2		2	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 6 Hz	f = 1 kHz

*JEDEC Registered Data.

NP

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

n-channel JFETs *designed for . . .*

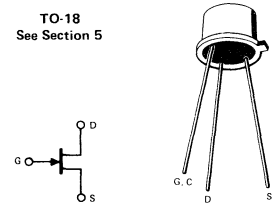
■ Small-Signal Low Noise Amplifiers

Performance Curves NP
See Section 4

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-18
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -50 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3458		2N3459		2N3460		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.5		-0.5		-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		1 (-8)		1 (-4)		1 (-2)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-7.8		-3.4		-1.8	V	V_{DS} = 20 V, I_D = 1 μA	
6		I_{DSS}	Drain Current at Zero Gate Voltage	3.0	15.0	0.8	4.0	0.2	1.0	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500	10,000	1500	6000	800	4500	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		35		20		5		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		5		5		5	pF		
10		C_{iss}	Common-Source Input Capacitance		18 (10)		18 (6)		18 (4)	pF (V)	V_{GS} = 0 V, V_{DS} = ( ),	f = 1 MHz
11		NF	Noise Figure		6		4		4	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 6 Hz	f = 20 Hz

* JEDEC registered data.

NP

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

depletion-type n-channel MOSFET *designed for . . .*

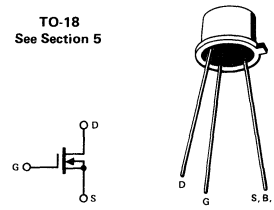
- **Small-Signal Amplifiers**
- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke detectors**
  - **pH Meters**

Performance Curves MA See Section 4

BENEFITS

- Insignificant Loading in High Impedance Circuits
  $R_{IN} > 10^{15}\ \Omega$
- High Off-Isolation as a Switch
  $I_{D(off)} < 100$ pA

TO-18
See Section 5



SUBSTRATE AND CASE CONNECTION TO SOURCE PIN

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . 20 V
Gate-to-Channel Voltage (Note 1). . . . . ±60 V
Drain Current . . . . . 20 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2). . . . . 300 mW
Storage Temperature Range . . . . . -65 to 200°C
Lead Temperature 1/16" From Case For 10 Sec . . . . 255°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSX}	Drain-Source Breakdown Voltage	20			V	$I_D = 1\ \mu A$, $V_{GS} = -10$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3.5	-6.0		$V_{DS} = 10$ V, $I_D = 1\ \mu A$	
3		V_{GS}	Gate-Source Voltage	-0.7		-5.5		$V_{DS} = 10$ V, $I_D = 200\ \mu A$	
4		I_{DSS}	Saturation Drain Current	2		10	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current			100	pA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6		r_{GS}	Common-Source Parallel Input Resistance	10^{15}	10^{16}		Ω	$V_{DS} = 10$ V, $I_D = 0.15$ mA	
7	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance (Note 3)		300	550	Ω	$V_{GS} = 0$, $V_{DS} = 0$	f = 1 kHz
8					100			$V_{GS} = 10$ V, $V_{DS} = 0$	
9		g_{os}	Common-Source Output Conductance			120	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
10		g_{fs}	Common-Source Forward Transconductance	1,400	2,000	2,800			
11		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1,400					f = 50 MHz
12		C_{iss}	Common-Source Input Capacitance (Output Shorted)		6.8	7.5	pF		f = 140 kHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance			1.6			f = 1 MHz

*JEDEC registered data

MA

NOTES:

1. Permanent damage may result if voltages greater than ±60 volts are applied to the gate
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C
3. Not JEDEC registered data

n-channel JFETs *designed for . . .*

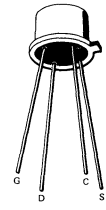
- **Low Noise Amplifiers**
- **Choppers**
- **Switches**

Performance Curves NFA
See Section 4

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-72
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 2) . . . −50 V
Gate Current or Drain Current . . . . . 50 mA
Total Device Dissipation
(Derate 2 mW/°C to 175°C) . . . . . 350 mW
Storage Temperature Range . . . . . −65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	2N3684 Min	2N3684 Max	2N3685 Min	2N3685 Max	2N3686 Min	2N3686 Max	2N3687 Min	2N3687 Max	Unit	Test Conditions	
1	STATIC	I_{GSS} Gate Reverse Current		−0.1		−0.1		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
2	STATIC	I_{GSS} Gate Reverse Current		−0.5		−0.5		−0.5		−0.5	μA	V_{GS} = −30 V, V_{DS} = 0	150°C
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	−50		−50		−50		−50		V	I_G = −1 μA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	−2	−5	−1	−3.5	−0.6	−2	−0.3	−1.2	V	V_{DS} = 20 V, I_D = 1 nA	
5	STATIC	I_{DSS} Saturation Drain Current	2.5	7.5	1	3	0.4	1.2	0.1	0.5	mA	V_{DS} = 20 V, V_{GS} = 0	
6		$r_{DS(on)}$ Drain-Source ON Resistance (Note 1)		600		800		1200		2400	ohm	V_{DS} = 0 V, V_{GS} = 0	
7	DYNAMIC	g_{fs} Common-Source Forward Transconductance	2000	3000	1500	2500	1000	2000	500	1500	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	g_{os} Common-Source Output Conductance		50		25		10		5	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
10	DYNAMIC	C_{iss} Common-Source Input Capacitance		4		4		4		4	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
11	DYNAMIC	$\bar{e}_n$ Equivalent Short Circuit Input Spot Noise Voltage		0.15		0.15		0.15		0.15	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 20 Hz
12	DYNAMIC	NF Noise Figure		0.5		0.5		0.5		0.5	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 10 meg, BW = 6 Hz	f = 100 Hz

NFA

*JEDEC registered data

NOTES:
1. Not JEDEC registered data
2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

2N3819

n-channel JFET
designed for . . .

- **General Purpose Amplifiers**
- **Analog Switching**

Performance Curves NRL See Section 4

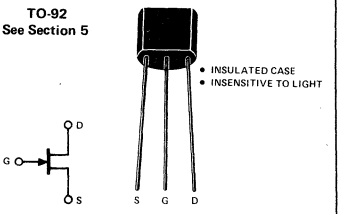
BENEFITS

- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

*ABSOLUTE MAXIMUM RATINGS

Drain-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Reverse Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) . . . . . 200 mW
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature
(1/16" from Case for 10 seconds) . . . . . 260°C

TO-92
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2	STATIC	I_{GSS}	Gate Reverse Current		−2	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3	STATIC	I_{GSS}	Gate Reverse Current		−2	μA	$V_{GS} = -15$ V, $V_{DS} = 0$	$T_A = 100°C$
4	STATIC	I_{DSS}	Saturation Drain Current	2	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	
5	STATIC	V_{GS}	Gate-Source Voltage	−0.5	−7.5	V	$V_{DS} = 15$ V, $I_D = 200\ \mu A$	
6	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage		−8	V	$V_{DS} = 15$ V, $I_D = 2$ nA	
7	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transfer Admittance	2000	6500	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	f = 1 kHz
8	DYNAMIC	$\lvert y_{os} \rvert$	Common Source Output Admittance		50	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	f = 1 kHz
9	DYNAMIC	C_{iss}	Common Source Input Capacitance		8	pF	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 MHz
10	DYNAMIC	C_{rss}	Common Source Reverse Transfer Capacitance		4	pF	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 MHz
11	DYNAMIC	$\lvert y_{fs} \rvert$	Common Source Forward Transfer Admittance	1600		μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 100 MHz

*JEDEC registered data **NRL**

NOTES:

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

n-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **Oscillators**

Performance Curves NRL See Section 4

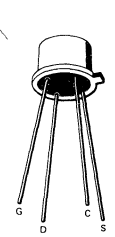
BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3821		2N3822		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2				V_{DS} = 15 V, I_D = 50 μA	
						-1	-4		V_{DS} = 15 V, I_D = 200 μA	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	2.5	2	10	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1500	4500	3000	6500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
12		NF	Noise Figure		5		5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

*JEDEC Registered Data. NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

2N3823

n-channel JFET *designed for . . .*

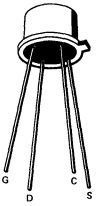
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NRL See Section 4

BENEFITS

- Low Noise
  NF < 2.5 dB @ 100 MHz

TO-72
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -30 V
Gate Current ..... 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature (1/16" From Case for 10 Sec) ... 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30			I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-8	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	-1.0	-7.5		V_{DS} = 15 V, I_D = 400 μA	
6		I_{DSS}	Saturation Drain Current	4	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 3)	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,500	6,500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz (Note 3)
8		$\|y_{fs}\|$	Common-Source Forward Transadmittance	3,200				f = 200 MHz
9		g_{os}	Common-Source Output Conductance		35			f = 1 kHz (Note 3)
10		g_{iss}	Common-Source Input Conductance		800			f = 200 MHz
11		g_{oss}	Common-Source Output Conductance		200			
12		C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 kΩ	f = 100 MHz

NRL

*JEDEC Registered Data

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFET *designed for . . .*

- **High Speed Commutators**
- **Choppers**

Performance Curves NRL See Section 4

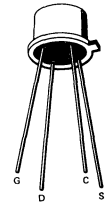
BENEFITS

- Low Insertion Loss
  $r_{ds(on)} < 250\ \Omega$
- High Off-Isolation
  $I_{D(off)} < 0.1$ nA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
2					−0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	I_G = −1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15 V, V_{GS} = −8 V	
					0.1	μA		150°C
5	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
6		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
7		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF	V_{GS} = −8 V, V_{DS} = 0	

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

p-channel JFET
designed for . . .

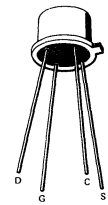
Performance Curves PC
See Section 4

■ General Purpose Amplifiers

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... 20 V
Drain-Source Voltage ..... -20 V
Gate Current ..... 10 mA
Total Device Dissipation at (or below)
25°C Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature 1/16" From Case For 10 Sec .... 300°C

TO-72
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3909 Min	2N3909 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		10	nA	V_{GS} = 10 V, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		1	μA	V_{GS} = 10 V, V_{DS} = 0	T = 100°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	20		V	I_G = 10 μA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage		8.0	V	V_{DS} = -10 V, I_D = -10 μA	
5	STATIC	V_{GS}	Gate-Source Voltage	0.3	7.9	V	V_{DS} = -10 V, I_D = -30 μA	
6	STATIC	I_{DSS}	Saturation Drain Current	-0.3	-15	mA	V_{DS} = -10 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000	5,000	μmho	V_{DS} = -10 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	g_{os}	Common-Source Output Conductance		100	μmho	V_{DS} = -10 V, V_{GS} = 0	f = 1 kHz
9	DYNAMIC	$\|y_{fs}\|$	Common-Source Forward Transadmittance	900		μmho	V_{DS} = -10 V, V_{GS} = 0	f = 10 MHz
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance		32	pF	V_{DS} = -10 V, V_{GS} = 0	f = 1 MHz
11	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		16	pF	V_{DS} = -10 V, V_{GS} = 0	f = 1 MHz

PC

*JEDEC registered data

Notes
1 Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2 Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

monolithic dual n-channel JFETs *designed for . . .*

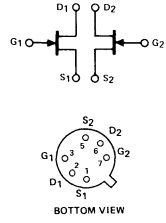
■ Differential Amplifiers

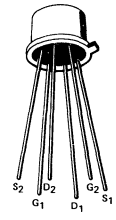
Performance Curves NNR See Section 4

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 5





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C to 200°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1	μA		100°C
3		BV_{DGO}	Drain-Gate Breakdown Voltage	50			I_D = 1 μA, I_S = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3	V	V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-2.7		V_{DS} = 10 V, I_D = 100 μA	
6		I_G	Gate Operating Current		-250	pA	V_{DG} = 10 V, I_D = 700 μA	
7					-25	nA		100°C
8		I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35			
11		C_{iss}	Common-Source Input Capacitance		18	pF		
12		C_{rss}	Common-Source Reverse Transfer Capacitance		6			
13		g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10 V, I_D = 700 μA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		20			
15		NF	Spot Noise Figure		2	dB	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz, R_G = 1 meg

		Characteristic		2N3921		2N3922		2N4084		2N4085		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCH	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		15		15	mV	V_{DG} = 10 V, I_D = 700 μA	
17		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		10		25		10		25	μV/°C		T_A = 0°C, T_B = 100°C
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data.

NOTES:
1. Pulse test duration = 2 ms.
2. Measured at end points, T_A and T_B.
3. Assumes smaller value in numerator.

NNR

matched dual n-channel JFETs *designed for . . .*

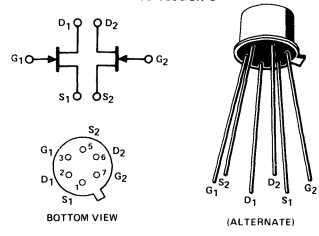
- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

Performance Curves NFA See Section 4

BENEFITS

- High Accuracy & Stability
  Offset Less Than 5 mV (2N3954, 54A)
  Drift Less Than 5 μV/°C (2N3954A)
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

TO-71
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Case-To-Lead Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3954		2N3954A		2N3955		2N3955A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100		-100	pA	V_{GS} = -30 V,	
2					-500		-500		-500		-500	nA	V_{DS} = 0	T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		V_{DS} = 0, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		V_{DS} = 20 V	I_D = 50 μA
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0			I_D = 200 μA
8		I_G	Gate Operating Current		-50		-50		-50		-50	pA	V_{DS} = 20 V,	
9					-250		-250		-250		-250	nA	I_D = 200 μA	T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common Source Spot Noise Figure		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Current		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA,	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V V_{GS} = 0	
20		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2			T = 25°C to -55°C
22					1.0		0.5		2.5		1.5			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data

NQP

NOTE:

1. Assumes smaller value in numerator.

matched dual n-channel JFETs *designed for . . .*

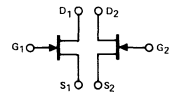
- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

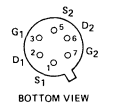
Performance Curves NFA
See Section 4

BENEFITS

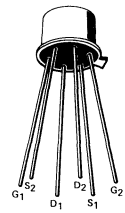
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

TO-71
See Section 5





BOTTOM VIEW



(ALTERNATE)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +250°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3956 Min	2N3956 Max	2N3957 Min	2N3957 Max	2N3958 Min	2N3958 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500		-500		-500	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		V_{DS} = 0 V, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		V_{DS} = 20 V, I_D = 50 μA	
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0		V_{DS} = 20 V, I_D = 200 μA	
8		I_G	Gate Operating Current		-50		-50		-50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					-250		-250		-250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Reverse Current		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	-	V_{DS} = 20 V, V_{GS} = 0	
20		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\lvert V_{GS1} - V_{GS2} \rvert$	Gate-Source Voltage Differential Change With Temperature		4.0		6.0		8.0			T = 25°C to -55°C
22					5.0		7.5		10.0			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	-		f = 1 kHz

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NQP

n-channel JFET
designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NH
See Section 4

BENEFITS

- Low Insertion Loss, No Offset Voltage
  $R_{DS(on)} < 220\ \Omega$
- Short Switching Aperture Times
  $C_{rss} < 1.5$ pF
  $t_{(on)} + t_{(off)} < 50$ ns Typical

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −30 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 300 mW
Power Derating . . . . . 1.7 mW/°C
Storage Temperature Range . . . . . −55 to +200°C
Operating Temperature Range . . . . . −55 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

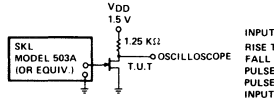
TO-72
See Section 5

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current			-0.1	nA	V_{GS} = -20 V, V_{DS} = 0	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4		-6.0	V	V_{DS} = 10 V, I_D = 10 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30				I_G = -1 μA, V_{DS} = 0	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 1)	2.0			mA	V_{DS} = 20 V, V_{GS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current			1.0	nA	V_{DS} = 10 V, V_{GS} = -7 V	
6						2.0	μA		T_A = 150°C
7		$r_{DS(on)}$	Static Drain-Source ON Resistance			220	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
8		$V_{DS(on)}$	Drain-Source ON Voltage			0.25	V	I_D = 1 mA, V_{GS} = 0	
9		I_{DGO}	Drain Reverse Current			0.1	nA	V_{DG} = 20 V, I_S = 0	
10						0.2	μA		T_A = 150°C
11		$r_{ds(on)}$	Drain-Source ON Resistance			220	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
12	DYN	C_{iss}	Common-Source Input Capacitance		3.1	6.0	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	1.5		V_{DS} = 0, V_{GS} = -7 V	
14		$t_{d(on)}$	Turn ON Delay Time		3.0	20	ns	V_{DD} = 1.5 V $I_{D(on)}$ = 1.0 mA $V_{GS(on)}$ = 0 $V_{GS(off)}$ = -6 V R_L = 1.25k Ω	See Circuit Below
15	SWITCH	t_r	Rise Time		10.0	100			
16		t_{off}	Turn OFF Time		30.0	100			
17		$t_{d(off)}$	Turn OFF Delay Time (Note 2)		10.0				
18		t_f	Fall Time (Note 2)		20.0				

*JEDEC registered parameters unless otherwise noted (apply to min/max only).

NOTES:
1. Pulse test duration ≤ 2 ms.
2. Non-JEDEC registered parameters:
   $t_{d(off)} + t_f = t_{off}$.



NH

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Amplifiers**

Performance Curves NC
See Section 4

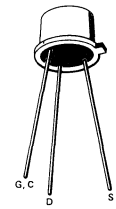
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (2N3970)
- Good Off-Isolation
  $I_{D(off)} < 250$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Note 1) . . . . . 1.8 W
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 5

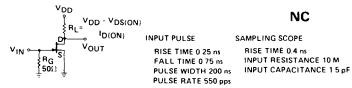


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

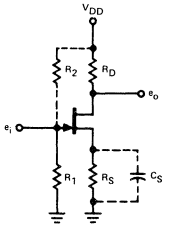
		Characteristic	2N3970 Min	2N3970 Max	2N3971 Min	2N3971 Max	2N3972 Min	2N3972 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate Reverse Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
2		I_{DGO} Drain Reverse Current		250		250		250	pA	V_{DG} = 20 V, I_S = 0	
3				500		500		500	nA		150°C
4		$I_{D(off)}$ Drain Cutoff Current		250		250		250	pA	V_{DS} = 20 V, V_{GS} = -12 V	
5				500		500		500	nA		150°C
6		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	V_{DS} = 20 V, I_D = 1 nA	
7		I_{DSS} Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0	
8		$V_{DS(on)}$ Drain-Source ON Voltage						2	V	V_{GS} = 0	I_D = 5 mA
9						1.5					I_D = 10 mA
10				1							I_D = 20 mA
11		$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
13		C_{iss} Common-Source Input Capacitance		25		25		25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance		6		6		6		V_{DS} = 0, V_{GS} = -12 V	
15	SW	$t_{d(on)}$ Turn-On Delay Time		10		15		40	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0	
16		t_r Rise Time		10		15		40		$I_{D(on)}$ R_L $V_{GS(off)}$	
17		t_{off} Turn-Off Time		30		60		100		2N3970 20 mA 450 Ω -10 V	
										2N3971 10 mA 850 Ω - 5 V	
										2N3972 5 mA 1.6KΩ - 3 V	

*JEDEC registered data.

NOTE:
1. Derate linearly at the rate of 10 mW/°C.



APPLICATIONS



Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

V_{DD} (V)	R_S (Ω)	R_1 (MΩ)	R_2 (MΩ)	C_S (μF)	I_{DD} (mA)	R_D (Ω)	e_o Max (V)	A_V
2N3970								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
V_{DD} = 15 V_{SS} = -15	3K	1	Source Follower		7	0	8.5	0.96
	7.5K	1			6	0	8.5	0.96
V_{DD} = 15 V_{SS} = -15	7.5K	1	Source Follower		6	0	15	0.97
2N3971								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97
2N3972								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-55
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		2.5	0	13	0.98
	7.5K	1			1.5	0	13	0.98

n-channel JFETs *designed for . . .*

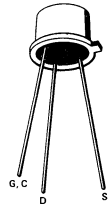
- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  $R_{ON} < 30\ \Omega$ (2N4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (2N4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

TO-18
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-55 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

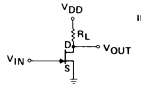
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4091		2N4092		2N4093		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V	
5									400	nA			150°C
6							200			pA		$V_{GS} = -8$ V	
7	S						400			nA			150°C
8	T				200					pA		$V_{GS} = -12$ V	
9	A				400					nA			150°C
10	T	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA		
11	I	I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
12	C	$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA	
13							0.2					$I_D = 4$ mA	
14					0.2							$I_D = 6.6$ mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
16		$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
17	D	C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
18	Y	C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V		
19	N	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$		
20	S	t_r	Rise Time		10		20		40				
21	W	t_{off}	Turn-OFF Time		40		60		80				

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4091	6.6 mA	-12 V	425 Ω
2N4092	4	-8	700
2N4093	2.5	-6	1120

*JEDEC registered data.

NOTE:
1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE < 10%
PULSE GENERATOR IMPEDANCE 50Ω

NC
SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

n-channel JFETs *designed for . . .*

■ Ultra-High Input Impedance Amplifiers

Electrometers
pH Meters
Smoke Detectors

Performance Curves NT
See Section 4

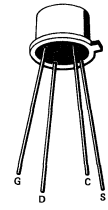
BENEFITS

- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (2N4117A Series)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -40 V
Gate-Current . . . . . 50 mA
Total Device Dissipation
(Derate 2 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 255°C

TO-72
See Section 5



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

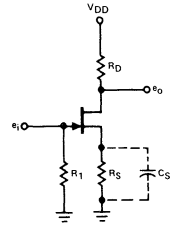
		Characteristic		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current 2N4117 Series Only		-10		-10		-10	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-25		-25		-25	nA		150°C
3		I_{GSS}	Gate Reverse Current 2N4117A Series Only		-1		-1		-1	pA	V_{GS} = -20 V, V_{DS} = 0	
4					-2.5		-2.5		-2.5	nA		150°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 10 V, I_D = 1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0.03	0.09	0.08	0.24	0.20	0.60	mA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	210	80	250	100	330	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		3		5		10			
10		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

NT

*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

APPLICATIONS



Amplifier Design Chart

V_{DD} (V)	R_S (kΩ)	C_S	I_{DD} (μA)	R_D (kΩ)	e_o Max (pK V)	A_V
2N4117						
10	10		45	120	1	5.7
20	10		45	270	1.5	12
				360	1	15
30	10		45	420	4	17
				620	1	22
V_{DD} = +15 V_{SS} = -15	510	Source Follower	35	0	8	0.97
2N4118						
10	8.2		120	36	0.6	2.2
				50	0.2	3.5
20	8.2		120	120	1	7.5
30	8.2		120	180	2	10
V_{DD} = +15 V_{SS} = -15	510	Source Follower	35	0	8	0.97
2N4119						
20	56	5 μF* at 5 V	70	150	1	10
30	56		70	240	3	17
				330	1	17-23
20	6.8		300	27	1	1.8
30	6.8		300	68	2	4.5
V_{DD} = +15 V_{SS} = -15	510	Source Follower	40	0	10	0.97

*AC Amplifier

n-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NRL
See Section 4

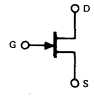
BENEFITS

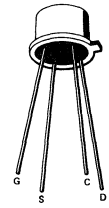
- High Gain
- Low Receiver Noise Figure

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V
Gate Current . . . . . 10 mA
Drain Current . . . . . 15 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-72
See Section 5





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4220, 2N4220A		2N4221, 2N4221A		2N4222, 2N4222A		Units	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-0.1		-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		V_{DS} = 15 V, I_D = 0.1 nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V	V_{DS} = 15 V, I_D = ( )	
				(50)	(50)	(200)	(200)	(500)	(500)	(μA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg	f = 100 Hz

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs *designed for . . .*

- **VHF Amplifiers**
- **Mixers**

Performance Curves NRL See Section 4

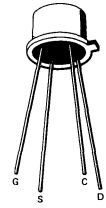
BENEFITS

- Low Noise
  NF = 3 dB Typical @ 200 MHz
- Easy Tuning
  $C_{rss} < 2$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V
Gate Current . . . . . 10 mA
Drain Current . . . . . 20 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-72
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	2N4223 Min	2N4223 Max	2N4224 Min	2N4224 Max	Unit	Test Conditions	
1		I_{GSS} Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2				-0.25		-0.5	µA		150°C
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 µA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15 V, I_D = ( )	
			(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
5	STATIC	V_{GS} Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5	V		
			(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
6	STATIC	I_{DSS} Saturation Drain Current (Note 3)	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYN	g_{fs} Common-Source Forward Transconductance (Note 3)	3000	7000	2000	7500	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8	DYN	C_{iss} Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
9	DYN	C_{rss} Common-Source Reverse Transfer Capacitance		2		2			
10	HIGH FREQ	$\lvert y_{fs} \rvert$ Common-Source Forward Transadmittance	2700		1700		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
11	HIGH FREQ	g_{iss} Common-Source Input Conductance (Output Shorted)		800		800			
12	HIGH FREQ	g_{oss} Common-Source Output Conductance (Input Shorted)		200		200			
13	HIGH FREQ	G_{ps} Small Signal Power Gain	10				dB		
14	HIGH FREQ	NF Noise Figure		5				V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs *designed for . . .*

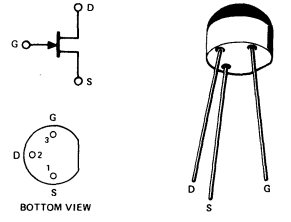
■ General Purpose Amplifiers

Performance Curves NP
See Section 4

BENEFITS

- Low Cost
- High Input Impedance
  I_G = 35 pA Typically
- Low Noise
  $\overline{e_n}$ = 5 nV/$\sqrt{Hz}$ Typically @ 1 kHz

TO-106
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... −30V
Gate Current ..... 50 mA
Total Device Dissipation
(25°C Free-Air Temperature)..... 350 mW
Power Derating (to +125°C)..... 3.5 mW/°C
Storage Temperature Range..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4302		2N4303		2N4304		Unit	Test Conditons	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		1		−1		−1	nA	V_{GS} = −10 V, V_{DS} = 0	
2					0.1		−0.1		−0.1	μA		T_A = 85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		−30		V	I_G = −1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4.0		−6.0		−10		V_{DS} = 20 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current (Note 3)	0.5	5.0	4.0	10	0.5	15	mA	V_{DS} = 20 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000		2000		1000		μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		50		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		C_{DG}	Drain-Gate Capacitance		2		2		2		V_{DG} = 10 V, I_S = 0	f = 140 kHz
11		NF	Noise Figure		2.0		2.0		3.0	dB	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz, R_{gen} = 1.0M Ω
12		$\lvert y_{fs} \rvert$	Common-Source Short Circuit Forward Transadmittance (Note 3)	700		1400		700		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 10 MHz

*JEDEC registered data

NP

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs *designed for . . .*

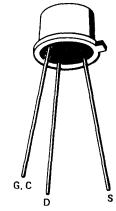
- **Small-Signal Amplifiers**
- **Choppers**
- **Voltage-Controlled Resistors**

Performance Curves NP
See Section 4

BENEFITS

- Low Noise
  NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages
  $V_{GS(off)}$ < 1 V (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances
  3:1 I_{DSS}, V_P, g_{fs} Ranges
- High Off-Isolation as a Switch
  $I_{D(off)}$ < 50 pA

TO-18
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Maximum Operating Temperature . . . . . 175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

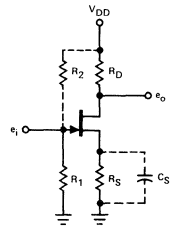
		Characteristic		2N4338		2N4339		2N4340		2N4341		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1		-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 15 V, I_D = 0.1 μA	
5		$I_{D(off)}$	Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	V_{DS} = 15 V V_{GS} = ( )	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		5		15		30		60			
9		$r_{ds(on)}$	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
10		C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
12		NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

*JEDEC registered data

NP

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 125 msec (I_{DSS}) and 625 msec (g_{fs}) after d-c power is applied. (Not a JEDEC condition.)

APPLICATIONS



Amplifier Design Chart

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4338								
15	1500	1M	∞	0	0.25	36	2.5	9-12
				30		36	1.5	16-24
						47	2.0	20-30
	5100	1M	∞	0	0.12	82	3.0	10-10.5
				25		82	1.5	24-37
	36K	1M	2M	30	0.15	27	1.0	13-18.5
30	1500	1M	∞	0	0.25	82	4.0	21.5-27
				30		82	2.5	32-49
						100	3.0	43-64
	5100	1M	∞	0	0.12	150	4.5	14.5-16
				25		150	2.5	38-54
						200	1.5	40-50
	36K	1M	5M	30	0.15	82	5.0	37-52
45	1500	1M	∞	0	0.25	120	6.5	27-33
				30		120	4.0	45-68
	5100	1M	∞	0	0.12	270	10	28-31
				25		270	5.0	76-105
	36K	1M	8.2M	0	0.15	120	14	2.8
				30		120	7.0	54-76
V_{DD} = +15 V_{SS} = -15	100K	1M	∞	0	0.15	0	9.0	0.98
2N4339								
15	1800	1M	∞	0	0.42	20	3.0	7-7.5
				40		20	2.0	17-22
						27	2.0	23-27
	9100	1M	6.8M	35	0.32	18	2.0	17-19
						30	2.5	26-28
	27K	1M	3M	25	0.2	22	1.0	16-18
						43	2.0	28-30
30	1800	1M	∞	0	0.42	47	6.5	15-17
				40		47	4.0	38-47
						51	4.5	40-50
	9100	1M	13M	0	0.32	43	8.0	4.5
				35		43	5.0	40-43
						68	4.5	53-60
	27K	1M	7.5M	25	0.2	68	4.0	49-52
						100	7.0	66-70
45	1800	1M	∞	0	0.42	75	7.5	23-25
				40		75	5.0	58-70
						100	7.0	73-77
	9100	1M	22M	0	0.32	68	7.0	7.0
				25		68	6.5	59-64
						120	7.0	80-85
	27K	1M	12M	0	0.2	100	12	3.3
				25		100	5.0	65-68
						180	8.0	100-115
V_{DD} = +15 V_{SS} = -15	75K	1M	∞	0	0.22	0	10	0.98

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4340								
15	680	1M	∞	0	1.5	5.1	3.0	3.5-4
				65		5.1	1.5	7-8.5
						6.8	2.0	9-10.5
	1200	1M	∞	0	1.1	7.5	2.5	3.5-4
				60		7.5	2.0	9-11
						10	2.0	11-13
	3900	1M	∞	0	0.4	18	4.0	3.5-4
				40		18	1.5	15-18
						22	1.0	19-22
30	680	1M	∞	0	1.5	12	6.0	9.5-10
				65		12	3.0	17-22
						18	1.0	24-26
	1200	1M	∞	0	1.1	18	6.0	9-9.5
				60		18	4.0	21-26
						24	2.0	29
	3900	1M	∞	0	0.4	39	7.0	7.5-8
				40		39	7.0	30-36
						62	0.5	34-45
	20K	1M	6.8M	35	0.35	30	3.0	25-27
						56	6.5	40
45	680	1M	∞	0	1.5	20	10.5	14-15.5
				65		20	8.0	27-32
						27	4.0	35
	1200	1M	∞	0	1.1	27	12.5	16-18
				60		27	5.0	30-37
						39	2.0	39-42
	3900	1M	∞	0	0.4	68	12	12-13
				40		68	7.0	52-61
						91	3.0	56-63
	20K	2M	3M	55	1.0	10	5.0	15
						20	4.0	27-28
V_{DD} = +15 V_{SS} = -15	22K	1M	∞	0	0.75	0	12	0.96
2N4341								
15	1000	1M	∞	70	2.7	2	1.0	3-3.5
						2.7	2.0	4-4.5
	1200	1.2M	7.5M	80	3.5	1.2	2.0	2.5
						2.2	3.0	3-4.5
	2000	1M	∞	65	1.8	3	2.0	4-4.5
						4.7	1.5	6-6.5
30	1000	1M	∞	0	2.7	6.2	7.0	4.0
				70		6.2	3.5	10
						9.1	1.5	11-13
	1200	1.1M	15M	80	3.5	3.9	4.0	7.5-8
	2000	1M	∞	0	1.8	9.1	6.0	3.0
				65		9.1	4.0	12
						15	1.0	13-19
	15K	1M	3.3M	50	0.7	18	3.0	16-21
45	1000	1M	∞	0	2.7	10	8.5	6.3
				70		10	6.0	16
	1200	1M	22M	80	3.5	6.8	7.0	13
	2000	1M	∞	0	1.8	15	8.5	5.5
				65		15	5.0	20-21
	15K	1M	5.6M	50	0.7	30	9.0	28-35
V_{DD} = +15 V_{SS} = -15	10K	1M	∞	0	1.9	0	13.5	0.94

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss, High Accuracy in Test Systems $r_{ON} < 30\ \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

TO-18
See Section 5

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . .300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

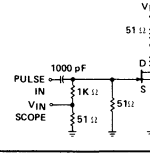
		Characteristic	2N4391 Min	2N4391 Max	2N4392 Min	2N4392 Max	2N4393 Min	2N4393 Max	Unit	Test Conditions		
1	STATIC	I_{GSS} Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0		
2				-200		-200		-200	nA			150°C
3		BV_{GSS} Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$I_{D(off)}$ Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = -5 V	
5								200	nA			150°C
6						100			pA		V_{GS} = -7 V	
7						200			nA			150°C
8				100					pA		V_{GS} = -12 V	
9				200					nA			150°C
10		$V_{GS(f)}$ Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
11		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA		
12		I_{DSS} Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
13		$V_{DS(on)}$ Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
14						0.4					I_D = 6 mA	
15				0.4							I_D = 12 mA	
16		$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
17		$r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
18	DYN	C_{iss} Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		
19		C_{rss} Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = - 5 V	f = 1 MHz
20						3.5					V_{GS} = - 7 V	
21				3.5							V_{GS} = -12 V	
22	SW	$t_{d(on)}$ Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
23		t_r Rise Time		5		5		5				
24		$t_{d(off)}$ Turn-OFF Delay Time		20		35		50				
25		t_f Fall Time		15		20		30				

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4391	12 mA	-12 V	800 Ω
2N4392	6	-7	1.6K Ω
2N4393	3	-5	3.2K Ω

*JEDEC registered data.

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ⩽ 3%.

NC



n-channel JFETs *designed for . . .*

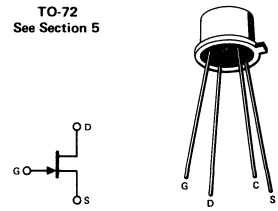
- **VHF Amplifiers**
- **Mixers**

Performance Curves NH See Section 4

BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

TO-72
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage, 2N4416 . . . . . -30 V
Gate-Drain or Gate-Source Voltage, 2N4416A . . . . . -35 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -20 V, V_{DS} = 0 V	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0 V	2N4416
				-35				2N4416A
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
				-2.5	-6			2N4416A
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50	μmho		
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4	pF		
10		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
13		g_{oss}	Common-Source Output Conductance		75		100	μmho	
14		b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
15		g_{fs}	Common-Source Forward Transconductance			4000		μmho	
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

*JEDEC Registered data

NH

NOTES:
1. Pulse test duration = 300 μs.

n-channel JFET
designed for . . .

- **VHF Amplifier**
- **Mixers**

Performance Curves NH
See Section 4

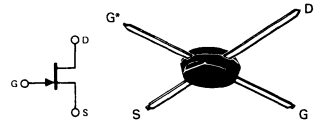
BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage . . . . . -30 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.4 mW/°C) . . . . . 175 mW
Operating Temperature Range . . . . . -65 to +150°C
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

OD-84
See Section 5



Note: G* is back Gate contact.

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50	μmho		
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		
9		C_{iss}	Common-Source Input Capacitance		3.5	pF		f = 1 MHz
10		C_{oss}	Common-Source Output Capacitance		1.3	pF		

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
11	HIGH FREQ	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
12		b_{iss}	Common-Source Input Susceptance		2000		8000		
13		g_{oss}	Common-Source Output Conductance		75		100		
14		b_{oss}	Common-Source Output Susceptance		800		3000		
15		g_{fs}	Common-Source Forward Transconductance (Note 1)			4000			
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ

*JEDEC Registered Data.

NH

NOTE:

1. Pulse test duration = 300 μs.

n-channel JFETs *designed for . . .*

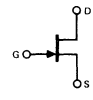
- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856, 59)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- High Speed
  $t_{ON} < 9$ ns
- Fully Qualified
  JAN, JANTX and JANTXV Available

TO-18
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

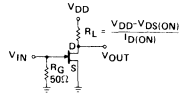
Reverse Gate-Drain or Gate-Source Voltage, 2N4856-58 ..... -40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859-61 ..... -30 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C) ..... 1.8 W
Storage Temperature Range ..... -65 to +200°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			2N4856 2N4859 Min	2N4856 2N4859 Max	2N4857 2N4860 Min	2N4857 2N4860 Max	2N4858 2N4861 Min	2N4858 2N4861 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	40		40		40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2				2N4859-61	30		30		30				
3		I_{GSS}	Gate Reverse Current	2N4856-58		-250		250		-250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4						-500		-500		-500	nA		150°C
5				2N4859-61		250		250		250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6						-500		500		-500	nA		150°C
7		$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8						500		500		500	nA		150°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
15	SWITCHING	$t_{d(on)}$	Turn-ON Delay Time			6 (20) [-10]		6 (10) [-6]		10 (5) [-4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ )$, $V_{GS(off)} = [\ ]$, $R_L =$ 464 Ω, 2N4856, 59; 953 Ω, 2N4857, 60; 1910 Ω, 2N4858, 61	
16		t_r	Rise Time			3 (20) [-10]		4 (10) [-6]		10 (5) [-4]	ns (mA) [V]		
17		t_{off}	Turn-OFF Time			25 (20) [-10]		50 (10) [-6]		100 (5) [-4]	ns (mA) [V]		

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

NC

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856A, 59A)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF
- High Speed
  $t_{ON} < 8$ ns

TO-18
See Section 5

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage,
2N4856A-58A . . . . . −40 V
Reverse Gate-Drain or Gate-Source Voltage,
2N4859A-61A . . . . . −30 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

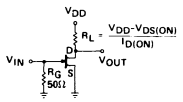
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4856A 2N4859A Min	2N4856A 2N4859A Max	2N4857A 2N4860A Min	2N4857A 2N4860A Max	2N4858A 2N4861A Min	2N4858A 2N4861A Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	2N4856A-58A	40		40		40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		Gate-Source Breakdown Voltage	2N4859A-61A	30		30		30				
3		I_{GSS}	2N4856A-58A		250		250		250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4		Gate Reverse Current			500		500		500	nA		150°C
5			2N4859A-61A		250		250		250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6					500		500		500	nA		150°C
7		$I_{D(off)}$			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8		Drain Cutoff Current			500		500		500	nA		150°C
9		$V_{GS(off)}$		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS}		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
12	DYN	$r_{ds(on)}$			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}			10		10		10	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss}			4		3.5		3.5			
15	SWITCHING	$t_{d(on)}$			5 (20) [10]		6 (10) [6]		8 (5) [4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ )$, $V_{GS(off)} = [\ ]$, $R_L =$ 464 Ω, 2N4856A, 59A; 953 Ω, 2N4857A, 60A; 1910 Ω, 2N4858A, 61A	
16		t_r			3 (20) [10]		4 (10) [6]		8 (5) [4]	ns (mA) [V]		
17		t_{off}			20 (20) [10]		40 (10) [6]		80 (5) [4]	ns (mA) [V]		

NC

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE = 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

n-channel JFETs *designed for . . .*

■ Audio and Sub-Audio Amplifiers

Performance Curves NS See Section 4

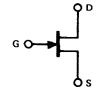
BENEFITS

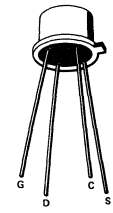
- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/√Hz Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/√Hz Typical at 1 kHz

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate Current or Drain Current ..... 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) .....300°C

TO-72
See Section 5





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.25		-0.25		-0.25	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20 V, I_D = 1 μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5		4		10			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		25		25		25			
10		$\overline{e_n}$	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/√Hz	V_{DS} = 10 V, V_{GS} = 0 — 2N4867 Series	f = 10 Hz
11					10		10		10		2N4867A Series	
12					10		10		10		2N4867 Series	f = 1 kHz
13					5		5		5		2N4867A Series	
14		NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 20 K, 2N4867 Series; 5 K, 2N4867A Series	f = 1 kHz

*JEDEC registered data. NS

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves PS
See Section 4

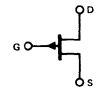
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 75\ \Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . .50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature (1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 5



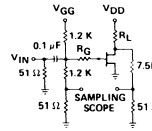
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5018 Min	2N5018 Max	2N5019 Min	2N5019 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15$ V, $V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		−10		−10	nA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5018)	
4					−10		−10	μA	$V_{GS} = 7$ V (2N5019)	150°C
5	STATIC	I_{DGO}	Drain Reverse Current		−2		−2	nA	$V_{DG} = -15$ V, $I_S = 0$	
6					−3		−3	μA		150°C
7		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
8		I_{DSS}	Saturation Drain Current	−10		−5		mA	$V_{DS} = -20$ V, $V_{GS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		−0.5		−0.5	V	$V_{GS} = 0$, $I_D = -6$ mA (2N5018), $I_D = -3$ mA (2N5019)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1$ mA, $V_{GS} = 0$	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
12	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5018), $V_{GS} = 7$ V (2N5019)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6$ V, $V_{GS(on)} = 0$	
15		t_r	Rise Time		20		75			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
17		t_f	Fall Time		50		100			

	$V_{GS(off)}$	$I_{D(on)}$	R_L
2N5018	12 V	−6 mA	910 Ω
2N5019	7 V	−3 mA	1.8K Ω

*JEDEC registered data.

NOTE:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



PS

INPUT PULSE
RISE TIME 1 ns
FALL TIME 1 ns
PULSE WIDTH 100 ns
REPETITION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

monolithic dual n-channel JFETs *designed for . . .*

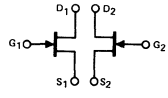
■ High Gain Differential Amplifiers

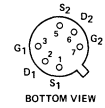
Performance Curves NNR See Section 4

BENEFITS

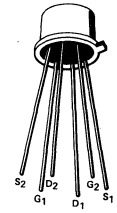
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5045)
- Low Drift
  5 mV Drift Maximum (2N5045)

TO-71
See Section 5





BOTTOM VIEW



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Forward Gate Current . . . . . 30 mA
Total Dissipation (25°C Free Air Temp.) . . . . . 400 mW
Power Derating (to 175°C) . . . . . 2.67 mW/°C
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic (Note 1)		2N5045		2N5046		2N5047		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	μA	V_{GS} = -50 V, V_{DS} = 0 V	
2					-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0 V	
3					-250		-250		-250			T = 150°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5	-0.5	-4.5	-0.5	-4.5	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		I_{DSS}	Drain Saturation Current	0.5	8.0	0.5	8.0	0.5	8.0	mA		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1.5	6.0	1.5	6.0	1.5	6.0	mmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		$\lvert y_{fs} \rvert$	Common-Source Forward Admittance	1.5		1.5		1.5				f = 100 MHz
8		g_{os}	Common-Source Output Conductance		25		25		25	μmho		f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
11		NF	Spot Noise Figure		5.0		5.0			dB		f = 10 Hz, R_G = 1 MΩ
12		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200			$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
13	MATCHING	$\lvert I_{GSS1} - I_{GSS2} \rvert$	Differential Gate Current		10		10		10	nA	V_{GS} = -15 V, V_{DS} = 0 V	T_A = 100°C
14		I_{DSS1}/I_{DSS2}	Drain Current Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{GS} = 0 V, V_{DS} = 15 V	
15		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DS} = 15 V	I_D = 50 μA
16					5		10		15			I_D = 200 μA
17		$\Delta\lvert V_{GS1} - V_{GS2} \rvert$	Gate-Source Voltage Differential Drift (Note 3)		5		10		15		V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C	T_B = -25°C
18					5		10		15			T_B = 100°C
19		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{DS} = 15 V, I_D = 200 μA	f = 1 kHz
20		$\lvert g_{os1} - g_{os2} \rvert$	Diff. Output Conductance		1.0		2.0		3.0	μmho		

*JEDEC registered data.

NNR

NOTES:
1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements..
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves PS
See Section 4

BENEFITS

- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . .50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature (1/16" from case for 10 seconds) . . . . . 300°C

TO-18
See Section 5

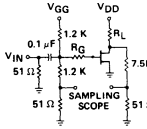
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	2N5114 Min	2N5114 Max	2N5115 Min	2N5115 Max	2N5116 Min	2N5116 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS} Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	
3				1.0		1.0		1.0	μA		150°C
4		$I_{D(off)}$ Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5114)	
5				-1.0		-1.0		-1.0	μA	$V_{GS} = 7$ V (2N5115), $V_{GS} = 5$ V (2N5116)	150°C
6		$V_{GS(off)}$ Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	$V_{DS} = -15$ V, $I_D = -1$ nA	
7		I_{DSS} Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{GS} = 0$, $V_{DS} = -18$ V (2N5114) $V_{DS} = -15$ V (2N5115, 2N5116)	
8		$V_{GS(f)}$ Forward Gate-Source Voltage		-1		-1		-1	V	$I_G = -1$ mA, $V_{DS} = 0$	
9		$V_{DS(on)}$ Drain-Source ON Voltage		-1.3		-0.8		-0.6		$V_{GS} = 0$, $I_D = -15$ mA (2N5114) $I_D = -7$ mA (2N5115), $I_D = -3$ mA (2N5116)	
10		$r_{DS(on)}$ Static Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = -1$ mA	
11	DYN	$r_{ds(on)}$ Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
12		C_{iss} Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = -15$, $V_{GS} = 0$	f = 1 MHz
13		C_{rss} Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5114) $V_{GS} = 7$ V (2N5115), $V_{GS} = 5$ V (2N5116)	

										2N5114	2N5115	2N5116
14	SWITCH	$t_{d(on)}$ Turn-ON Delay Time		6		10		12	ns	V_{DD}	-10 V	-6 V	-6 V
15		t_r Rise Time		10		20		30		$V_{GS(off)}$	12 V	7 V	5 V
16		$t_{d(off)}$ Turn-OFF Delay Time		6		8		10		R_L	580 Ω	743 Ω	1800 Ω
17		t_f Fall Time		15		30		50		$V_{GS(on)}$	0	0	0
										$I_{D(on)}$	-15 mA	-7 mA	-3 mA

*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse Test PW 300 μs, duty cycle ≤ 3%.



PS

INPUT PULSE
RISE TIME ≤ 1 ns
FALL TIME ≤ 1 ns
PULSE WIDTH 100 ns
REPETITION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

n-channel JFET
designed for . . .

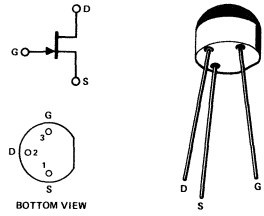
- **Low and Medium Frequency Amplifiers**

BENEFITS
- Low Cost

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . –55 to +125°C
Operating Temperature Range . . . . . –55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS} Gate Reverse Current		–10	nA	V_{GS} = –15 V, V_{DS} = 0		
2				–0.6	μA			T_A = 85°C
3		BV_{GSS} Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0		
4		$V_{GS(off)}$ Gate-Source Cutoff Voltage	–0.4	–8.0		V_{DS} = 15 V, I_D = 1 μA		
5		V_{GS} Gate-Source Voltage		–7.5		V_{DS} = 15 V, I_D = 100 μA		
6		I_{DSS} Saturation Drain Current	1.0	40	mA	V_{DS} = 15 V, V_{GS} = 0		
7	DYNAMIC	$r_{ds(on)}$ Drain-Source ON Resistance		500	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
8		g_{fs} Common-Source Forward Transconductance	2000	9000	μmho	V_{DS} = 15 V, V_{GS} = 0		
9		g_{os} Common-Source Output Conductance		200				
10		g_{fs} Common-Source Forward Transconductance	1800					f = 1 MHz
11		C_{iss} Common-Source Input Capacitance		20	pF			
12		C_{rss} Common-Source Reverse Transfer Capacitance		5.0				
13		NF Common-Source Spot Noise Figure		3.0	dB	V_{DS} = 15 V, I_D = 1 mA	R_G = 150k Ω	f = 1 kHz NBW = 150 Hz
14		$\overline{e_N}$ Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$			

*JEDEC registered data

monolithic dual n-channel JFETs *designed for . . .*

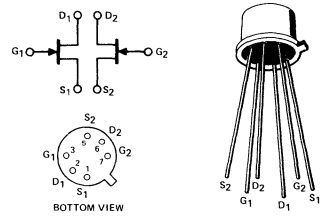
- **Differential Amplifiers**
- **FET Input Op Amps**

Performance Curves NNP
See Section 4

BENEFITS

- Minimum System Error and Calibration
  5 mV Maximum Offset (2N5196, 97)
- Low Drift
  5 μV/°C Maximum (2N5196)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.56 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 4.3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-50	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-3.8			
6		I_G	Gate Operating Current		-15	pA	V_{DG} = 20 V, I_D = 200 μA	
					-15	nA		125°C
7		I_{DSS}	Saturation Drain Current	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	700	1600		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
15		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

		Characteristic		2N5196		2N5197		2N5198		2N5199		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
19		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
20		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
21					5		10		20		40			T_A = -55°C, T_B = 25°C
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

*JEDEC registered data.

NNP

NOTES:
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

2N5432 2N5433 2N5434

n-channel JFETs *designed for . . .*

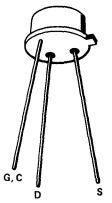
- **Low ON Resistance Analog Switches**
- **Commutators**
- **Chochoppers**
- **Integrator Reset Capacitors**
- **Low Noise Audio Amplifiers**

Performance Curves NIP See Section 4

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 5\ \Omega$ (2N5432)
- Small Error in Measurement Systems
  $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{d(on)} < 4$ ns
- Low Noise Audio-Frequency Amplification
  $e_n < 2\ nV/\sqrt{Hz}$ at 1 kHz Typical

TO-52
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 100 mA
Drain Current . . . . . 400 mA
Total Device Dissipation at 25°C
Free-Air Temperature (Note 1) . . . . . 300 mW
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

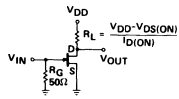
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5432		2N5433		2N5434		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-200		-200		-200	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-200		-200		-200	nA		150°C
3		BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = -10 V	
5					200		200		200	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V_{DS} = 5 V, I_D = 3 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
9		$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
10		$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
13	SW	$t_{d(on)}$	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -12 V, $I_{D(on)}$ = 10 mA, R_L = 145 Ω (2N5432), 143 Ω (2N5433), 140 Ω (2N5434)	
14		t_r	Rise Time		1		1		1			
15		$t_{d(off)}$	Turn-OFF Delay Time		6		6		6			
16		t_f	Fall Time		30		30		30			

*JEDEC registered data.

NIP

NOTES:
1. Derate linearly at the rate of 2.3 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

matched dual n-channel JFETs *designed for . . .*

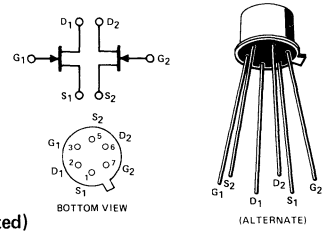
■ Low and Medium Frequency Differential Amplifiers

Performance Curves NFA See Section 4

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design
  Output Conductance Less that 1 μmho

TO-71
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +250°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5452 Min	2N5452 Max	2N5453 Min	2N5453 Max	2N5454 Min	2N5454 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0 V	
2					-200		-200		-200	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2		V_{DS} = 20 V, I_D = 50 μA	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2		V_{DS} = 0 V, I_G = 1 mA	
7		I_{DSS}	Drain Saturation Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
9				1000		1000		1000				f = 100 MHz
10		g_{os}	Common-Source Output Conductance		3.0		3.0		3.0			f = 1 kHz
11					1.0		1.0		1.0		V_{DS} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
14		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0 V	
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
16		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
17	MATCHING	I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
19		$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
20					0.5		1.0		2.5			T = 25°C to +125°C
21		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NQP

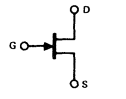
n-channel JFETs *designed for . . .*

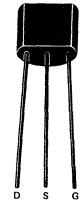
- **General Purpose Amplifiers**
- **Switches**

Performance Curves NRL See Section 4

BENEFITS
- Low Cost
- Automated Insertion Package

TO-92
See Section 5





- INSULATED CASE
- DRAIN AND SOURCE CAN BE INTERCHANGED
- INSENSITIVE TO LIGHT

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature	135°C
Storage Temperature Range	-65 to +150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5457			2N5458			2N5459			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-.01	-1.0		-.01	-1.0		-.01	-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
2						-200			-200			-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		-25	-60		-25	-60		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-6.0	-1.0		-7.0	-2.0		-8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0		5.0	2.0		9.0	4.0		16	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		5,000	1,500		5,500	2,000		6,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		10	50		15	50		20	50			
8		C_{iss}	Common-Source Input Capacitance		4.5	7.0		4.5	7.0		4.5	7.0	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0		1.0	3.0		1.0	3.0			
10		NF	Noise Figure		.04	3.0		.04	3.0		.04	3.0	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 MΩ, NBW = 1 Hz	f = 1 kHz

*JEDEC registered data

NOTE:

1. Pulse test pulsewidth = 2 ms.

NRL

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**
- **Analog Switches**

Performance Curves NH See Section 4

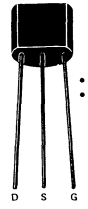
BENEFITS

- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch
  Very Little Charge Coupling
  $C_{rss} < 1.0$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source Gate Voltage . . . . . 25 V
Drain Current . . . . . 30 mA
Forward Gate Current . . . . . 10 mA
Total Device Dissipation @ 25°C . . . . . 360 mW
Derate above 25°C . . . . . 3.27 mW/°C
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 240°C

TO-92
See Section 5



- INSULATED CASE
- INSENSITIVE TO LIGHT

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5484 Min	2N5484 Max	2N5485 Min	2N5485 Max	2N5486 Min	2N5486 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} -20 V, V_{DS} 0	
2					-200		-200		-200			T_A +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I_G -1 μA, V_{DS} 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0		V_{DS} 15 V, I_D 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} 15 V, V_{GS} 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,000	6,000	3,500	7,000	4,000	8,000	μmhos	V_{DS} 15 V, V_{GS} 0	f 1 kHz
7		g_{os}	Common-Source Output Conductance		50		60		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	2,500								f 100 MHz
9						3,000		3,500				f 400 MHz
10		$Re(y_{os})$	Common-Source Output Conductance		75							f 100 MHz
11							100		100			f 400 MHz
12		$Re(y_{is})$	Common-Source Input Conductance		100							f 100 MHz
13							1,000		1,000			f 400 MHz
14		C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
16		C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
17		NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} 15 V, V_{GS} 0, R_G 1 MΩ	f 1 kHz
18					3.0						V_{DS} 15 V, I_D 1 mA, R_G 1 kΩ	f 100 MHz
19							2.0		2.0		V_{DS} 15 V, I_D 4 mA, R_G 1 kΩ	
20							4.0		4.0			f 400 MHz
21		G_{ps}	Common-Source Power Gain	16	25						V_{DS} 15 V, I_D 1 mA	f 100 MHz
22						18	30	18	30		V_{DS} 15 V, I_D 4 mA	
23						10	20	10	20			f 400 MHz

* JEDEC registered data

NH

NOTE:
1 Pulse Test PW 300 μs, duty cycle ≤ 3%

2N5515 2N5516 2N5517 2N5518 2N5519
2N5520 2N5521 2N5522 2N5523 2N5524

matched dual n-channel JFETs *designed for . . .*

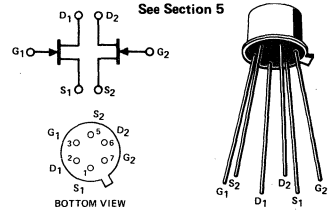
■ Differential Amplifiers

Performance Curves NS See Section 4

BENEFITS

- Ultra-Low Noise
  $\overline{e_n}$ = 8 nV/√Hz at 10 Hz (Typical)
  $\overline{e_n}$ = 2 nV/√Hz at 1 kHz (Typical)
- Minimum System Error and Calibration
  5 mV Offset Maximum
  CMRR > 100 dB

See SI-71 or TO-71 Alternative See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -40 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.0 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 3.0 mW/°C) . . . . . 375 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 30 seconds) . . . . . .300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-250	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage	-0.2	-3.8			
6		I_G	Gate Operating Current		-100	pA	V_{DG} = 20 V, I_D = 200 μA	
					-100	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	500	1000		V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		10		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		1		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		5			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage 2N5515-19		30	nV/√Hz	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
			2N5520-24		15			f = 10 Hz
			2N5515-24		10			f = 1 kHz

		Characteristic		2N5515,20 Min	2N5515,20 Max	2N5516,21 Min	2N5516,21 Max	2N5517,22 Min	2N5517,22 Max	2N5518,23 Min	2N5518,23 Max	2N5519,24 Min	2N5519,24 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	–	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV		
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
					5		10		20		40		80			T_A = -55°C, T_B = 25°C
19		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho		f = 1 kHz
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	–		
21		CMRR	Common Mode Rejection Ratio (Note 4)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA	

*JEDEC registered data.

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.
4. CMRR = $20\log_{10}\left(\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right)$, ΔV_{DD} = 10 V.

NS

monolithic dual n-channel JFETs *designed for . . .*

■ General Purpose Differential Amplifiers

Performance Curves NNP See Section 4

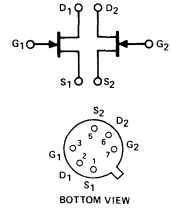
BENEFITS

- High Input Impedance
  $I_G < 50$ pA
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5545)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –50 V
Gate Current . . . . . 30 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 1.67 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 25°C
(Derate 2.67 mW/°C) . . . . . 400 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 30 seconds) . . . . . 300°C

TO-71
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0		
2					-150	nA		T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 15 V, I_D = 0.5 nA		
5		I_G	Gate Operating Current		-50	pA	V_{DG} = 15 V, I_D = 200 μA		
6		I_{DSS}	Saturation Drain Current	0.5	8	mA	V_{DS} = 15 V, V_{GS} = 0		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0		f = 1 kHz
8		g_{os}	Common-Source Output Conductance		25				
9		C_{iss}	Common-Source Input Capacitance		6	pF			f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		2				
11		NF	Spot Noise Figure		3.5	dB	V_{DG} = 15 V, I_D = 200 μA	2N5545	f = 10 Hz, R_G = 1 MΩ
					5			2N5546	
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		180	$\frac{nV}{\sqrt{Hz}}$		2N5545	f = 10 Hz
					200			2N5546	

		Characteristic		2N5545		2N5546		2N5547		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
13	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5	nA	V_{DG} = 15 V, I_D = 200 μA	T_A = 125°C
14		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.90	1	0.90	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 15 V	I_D = 50 μA
					5		10		15			I_D = 200 μA
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		10		20		40	μV/°C	V_{DG} = 15 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
					10		20		40			T_A = -55°C, T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.95	1	0.90	1	–		f = 1 kHz
18		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		2		3	μmho		

*JEDEC registered data.

NNP

NOTES:
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

2N5555

n-channel JFET
designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NH
See Section 4

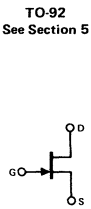
BENEFITS

- Low Cost
- Automatic Insertion Package
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
- Low Charge Coupling from Driver to Load
  C_{rss} = 0.8 pF Typically

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or Below) T_A = 25°C . . 360 mW
(Derate 3.27 mW/°C to 135°C)
Operating Temperature Range. . . . . –55 to +135°C
Storage Temperature Range . . . . . –65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .240°C

TO-92
See Section 5



- INSULATED CASE
- INSENSITIVE TO LIGHT

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.2	μA		T_A = 100°C
3		I_{DGO}	Drain Leakage Current		1.0	nA	V_{DG} = 15 V, I_S = 0	
4					0.2	μA		T_A = 100°C
5		$I_{D(off)}$	Drain Cutoff Current		10	nA	V_{DS} = 12 V, V_{GS} = –10 V	
6					2.0	μA		T_A = 100°C
7		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0	
8		$V_{GS(f)}$	Gate-Source Forward Voltage		1.0		I_G = 1 mA, V_{DS} = 0	
9		$V_{DS(on)}$	Drain-Source ON Voltage		1.5		I_D = 7 mA, V_{GS} = 0	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		150	Ω	I_D = 0.1 mA, V_{GS} = 0	
11		I_{DSS}	Saturation Drain Current	15		mA	V_{DS} = 15 V, V_{GS} = 0	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance		5.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		V_{DS} = 0, V_{GS} = –10 V	
15	SWITCH	$t_{d(on)}$	Turn ON Delay Time		5	ns	V_{DD} = 10 V, $I_{D(on)}$ = 7 mA, R_L = 1.21K Ω $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 V	
16		t_r	Rise Time		5			
17		$t_{d(off)}$	Turn OFF Delay Time		15			
18		t_f	Fall Time		10			

*JEDEC registered data

NH

n-channel JFETs *designed for . . .*

Performance Curves NRL See Section 4

■ General Purpose Amplifiers

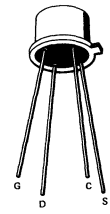
BENEFITS

- Low Noise
- Low Output Conductance

*ABSOLUTE MAXIMUM RATINGS (at 25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 300 mW
Power Derating (to +175°C) . . . . . 2.0 mW/°C
Storage Temperature Range . . . . . -65 to +200°C
Operating Temperature Range . . . . . -65 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 240°C

TO-72
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5556		2N5557		2N5558		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2					-100		-100		-100			T = 150°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.2	-4.0	-0.8	5.0	-1.5	-6.0	V	V_{DS} = 15 V, I_D = 1 nA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30			I_G = -10 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	2.5	2.0	5.0	4.0	10.0	mA	V_{DG} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6500	1500	6500	1500	6500	μmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		20		20		20			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		$\overline{e}_n$	Common-Source Equivalent Short Circuit Input Noise Voltage		35		35		35	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
11					20		20		20			f = 100 Hz
12		NF	Noise Figure		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 V, BW = 1.0 Hz	f = 10 Hz
13					1		1		1			f = 100 Hz

*JEDEC registered data NRL

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Pulse test duration ≤ 2 ms.

matched dual n-channel JFETs *designed for . . .*

- **Wideband Differential Amplifiers**
- **Commutators**

Performance Curves NC
See Section 4

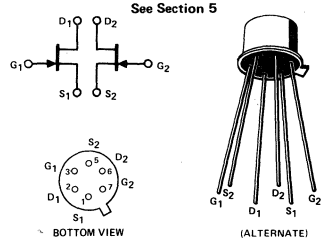
BENEFITS

- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate–Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, T_A = 25°C (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 5



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		1.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	30	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
9				7000				f = 100 MHz
10		g_{os}	Common-Source Output Conductance		45			f = 1 kHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
12		C_{iss}	Common-Source Input Capacitance		12			
13		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		2N5564 Min	2N5564 Max	2N5565 Min	2N5565 Max	2N5566 Min	2N5566 Max	Unit	Test Conditions	
15	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
16		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
17		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C T_B = 125°C
18					10		25		50			T_A = -55°C T_B = 25°C
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

*JEDEC registered data.

NC

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B.

n-channel JFETs *designed for . . .*

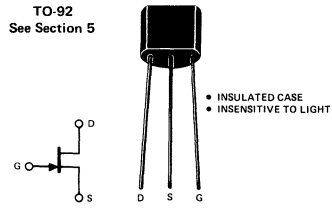
- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NC
See Section 4

BENEFITS

- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching
  $t_{rise} < 5$ ns (2N5638)
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (2N5638)
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF

TO-92
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at T_{LEAD} = 25°C	625 mW
Derate above 25°C	5.68 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

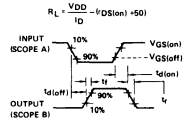
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5638		2N5639		2N5640		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
3					-1.0		-1.0		-1.0	μA		T_A = +100°C
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = -12 V (2N5638)	
5					1.0		1.0		1.0	μA	V_{GS} = -8 V (2N5639), V_{GS} = -6 V (2N5640)	T_A = +100°C
6		I_{DSS}	Saturation Drain Current	50		25		5.0		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	V_{GS} = 0, I_D = 12 mA (2N5638), I_D = 6 mA (2N5639), I_D = 3 mA (2N5640)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	I_D = 1 mA, V_{GS} = 0	
9		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0	f = 1 kHz
10	DYN	C_{iss}	Common-Source Input Capacitance		10		10		10	pF	V_{GS} = -12 V, V_{DS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
12	SW	$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	nsec	V_{DD} = 10 V $I_{D(on)}$ = 12 mA (2N5638) R_L = 800 Ω (2N5638)	
13		t_r	Rise Time		5.0		8.0		10		$V_{GS(on)}$ = 0 $I_{D(on)}$ = 6 mA (2N5639) R_L = 1.6k Ω (2N5639)	
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		15		$V_{GS(off)}$ = -10 V $I_{D(on)}$ = 3 mA (2N5640) R_L = 3.2k Ω (2N5640)	
15		t_f	Fall Time		10		20		30			

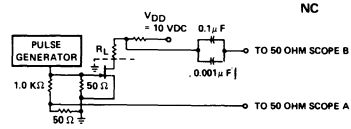
* JEDEC registered data

NOTE:

1 Pulse test PW ≤ 300 μsec, duty cycle ≤ 3.0%



NC



n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NC
See Section 4

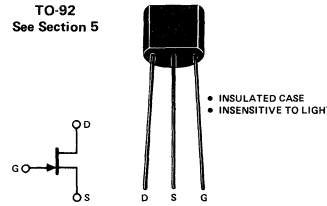
BENEFITS

- Low Cost
- Automatic Insertion Package
- High Speed
  $t_{ON} + t_{OFF}$ = 24 ns Max (2N5653)
- Low Insertion Loss
  $R_{DS(on)}$ = 50 Ω Max (2N5653)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage . . . . . 30 V
Drain-Gate Voltage . . . . . 30 V
Source-Gate Voltage . . . . . 30 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at (or Below) T_A = 25°C
(Derate 2.82 mW/°C to 135°C) . . . . . 310 mW
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C

TO-92
See Section 5

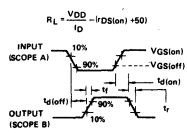


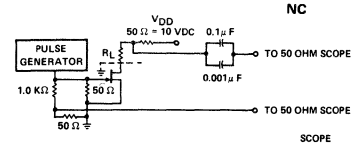
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5653 Min	2N5653 Max	2N5654 Min	2N5654 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		V	I_G = −10 μA, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		−1.0		−1.0	nA	V_{GS} = −15 V, V_{DS} = 0	
3	STATIC	I_{GSS}	Gate Reverse Current		−1.0		−1.0	μA	V_{GS} = −15 V, V_{DS} = 0	T_A = +100°C
4	STATIC	$I_{D(off)}$	Drain Cutoff Current		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = −12 V (2N5653)	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current		1.0		1.0	μA	V_{GS} = −8 V (2N5654)	T_A = +100°C
6	STATIC	I_{DSS}	Saturation Drain Current	40		15		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.75		0.75	V	V_{GS} = 0, I_D = 10 mA (2N5653), I_D = 5 mA (2N5654)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		50		100	Ω	I_D = 1 mA, V_{GS} = 0	
9		$r_{ds(on)}$	Drain-Source ON Resistance		50		100	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
10	DYN	C_{iss}	Common-Source Input Capacitance		10		10	pF	V_{GS} = −12 V, V_{DS} = 0	f = 1 MHz
11	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5	pF	V_{GS} = −12 V, V_{DS} = 0	f = 1 MHz
12	SW	$t_{d(on)}$	Turn-ON Delay Time		4.0		6.0	nsec	V_{DD} = 10 V, $I_{D(on)}$ = 10 mA (2N5653)	
13	SW	t_r	Rise Time		5.0		8.0	nsec	$V_{GS(on)}$ = 0, $I_{D(on)}$ = 5 mA (2N5654)	
14	SW	$t_{d(off)}$	Turn-OFF Delay Time		5.0		10	nsec	$V_{GS(off)}$ = −12 V, R_L = 925 Ω (2N5653)	
15	SW	t_f	Fall Time		10		20	nsec	R_L = 1.85K Ω (2N5654)	

*JEDEC registered data

NOTE:
1. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.





n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

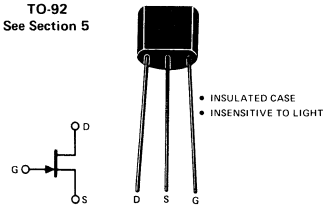
Performance Curves NH
See Section 4

BENEFITS
- Low Cost
- Automatic Insertion Package
- Specified for 100 MHz Operation

***ABSOLUTE MAXIMUM RATINGS**

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation
at (or Below) T_A = 25°C
(Derate 2.82 mW/°C to 135°C) . . . . . 310 mW
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C

TO-92
See Section 5



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N5668		2N5669		2N5670		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−2.0		−2.0		−2.0	nA	V_{GS} = −15 V, V_{DS} = 0	
2					−2.0		−2.0		−2.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		−25		V	I_G = −10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.2	4.0	1.0	6.0	2.0	8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6500	2000	6500	3000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		20		50		75			
8		$Re(Y_{fs})$	Common-Source Forward Transconductance	1000		1600		2500				f = 100 MHz
9		$Re(Y_{os})$	Common-Source Output Conductance		50		100		150			
10		$Re(Y_{is})$	Common-Source Input Conductance		800		800		800			
11		C_{iss}	Common-Source Input Capacitance		7.0		7.0		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0			
13		C_{oss}	Common-Source Output Capacitance		4.0		4.0		4.0			
14		NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 100 MHz
15		G_{ps}	Common-Source Power Gain	16		16		16			V_{DS} = 15 V, V_{GS} = 0	

*JEDEC registered data

NH

NOTE:
1. Pulse test PW = 300 μs, duty cycle ≤ 3%.

2N5902 2N5903 2N5904 2N5905
2N5906 2N5907 2N5908 2N5909

matched dual n-channel JFETs *designed for . . .*

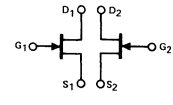
- **Differential Amplifiers**
- **High Input Impedance Amplifiers**

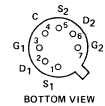
Performance Curves NT
See Section 4

BENEFITS

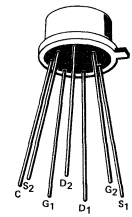
- Matching Characteristics Specified
- High Input Impedance
  I_G = 1 pA Max (2N5906–9)

TO-78
See Section 5





BOTTOM VIEW



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3 mW/°C)	367 mW
Total Device Dissipation, T_A = 25°C (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5902-5 Min	2N5902-5 Max	2N5906-9 Min	2N5906-9 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-2	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-10		-5	nA		125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage		-4		-4		V_{DG} = 10 V, I_D = 30 μA	
6		I_G	Gate Operating Current		-3		-1	pA		
7					-3		-1	nA		125°C
8		I_{DSS}	Saturation Drain Current	30	500	30	500	μA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho		f = 1 kHz
10		g_{os}	Common-Source Output Conductance		5		5			
11		C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
13		g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	V_{DG} = 10 V, I_D = 30 μA	
14		g_{os}	Common-Source Output Conductance		1		1			f = 1 kHz
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
16		NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 M

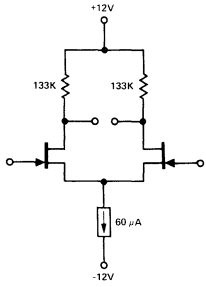
		Characteristic		2N5902, 6 Min	2N5902, 6 Max	2N5903, 7 Min	2N5903, 7 Max	2N5904, 8 Min	2N5904, 8 Max	2N5905, 9 Min	2N5905, 9 Max	Unit	Test Conditions	
17	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	V_{DG} = 10 V, I_D = 30 μA, T_A = 125°C	2N5902-5
18					0.2		0.2		0.2		0.2			2N5906-9
19		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
21		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
22		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
23					5		10		20		40			T_A = -55°C, T_B = 25°C
24		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

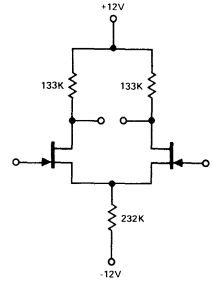
*JEDEC registered data.

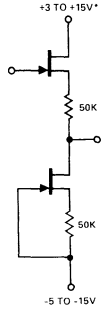
NOTES:
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

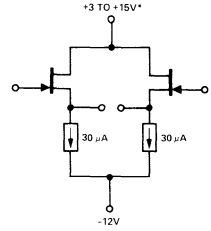
NT

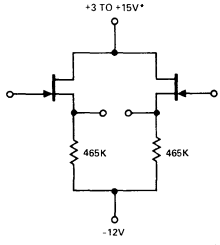
APPLICATIONS

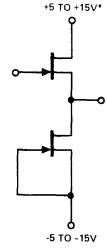












*Use lower voltages for minimum I_G

3

matched dual n-channel JFETs *designed for . . .*

■ Wideband Differential Amplifiers

Performance Curves NZF See Section 4

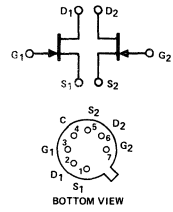
BENEFITS

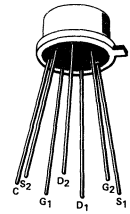
- High Gain through 100 MHz $g_{fs} > 5000$ μmho
- Matching Characteristics Specified

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation, (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-78
See Section 5





*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4			
6		I_G	Gate Operating Current		-100	pA	V_{DG} = 10 V, I_D = 5 mA	
					-100	nA		T_A = 125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K

		Characteristic		2N5911 Min	2N5911 Max	2N5912 Min	2N5912 Max	Unit	Test Conditions	
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	T_A = 125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
19		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		20		40	μV/°C		T_A = 25°C T_B = 125°C
20					20		40			T_A = -55°C T_B = 25°C
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.95	1	0.95	1	–		f = 1 kHz

*JEDEC registered data.

NZF

NOTES:

1. Pulsewidth ≤ 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

enhancement-type p-channel MOSFETs *designed for . . .*

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke Detectors**
  - **pH Meters**
- **Digital Switching Interfaces**
- **Analog Switching**

Performance Curves MRA
See Section 4

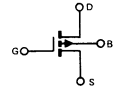
BENEFITS

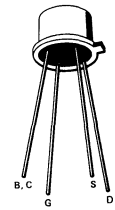
- Rugged MOS Gate Minimizes Handling Problems
  ±150 V Transient Capability
- Low Gate-Leakage
  Typically 0.02 pA
- High Off-Isolation as a Switch
  $I_{DSS} < 200$ pA

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Source or Gate-Source Voltage 3N163 . . . . . -40 V
Drain-Source or Gate-Source Voltage 3N164 . . . . . -30 V
Transient Gate-Source Voltage (Note 1) . . . . . ±150 V
Drain Current . . . . . -50 mA
Storage Temperature . . . . . -65 to +200°C
Operating Junction Temperature . . . . . -55 to +150°C
Total Device Dissipation
(Derate 3.0 mW/°C to 150°C) . . . . . 375 mW
Lead Temperature 1/16" From Case For 10 Seconds . .265°C

TO-72
See Section 5



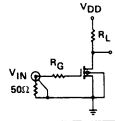


***ELECTRICAL CHARACTERISTICS (25°C and V_{BS} = 0 unless otherwise noted)**

		Characteristic		3N163 Min	3N163 Max	3N164 Min	3N164 Max	Unit	Test Conditions	
1		I_{GSS}	Gate-Body Leakage Current		-10			pA	V_{GS} = -40 V, V_{DS} = 0	
2					-25					T_A = 125°C
3							-10		V_{GS} = -30 V, V_{DS} = 0	
4							-25			T_A = 125°C
5	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	I_D = -10 μA, V_{GS} = 0	
6		BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			I_S = -10 μA, V_{GD} = V_{BD} = 0	
7		V_{GS}	Gate Source Voltage	-3	-6.5	-2.5	-6.5		V_{DS} = -15 V, I_D = -0.5 mA	
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2	-5	-2	-5		V_{DS} = V_{GS}, I_D = -10 μA	
9		I_{DSS}	Drain Cutoff Current		-200		-400	pA	V_{DS} = -15 V, V_{GS} = 0	
10		I_{SDS}	Source Cutoff Current		-400		-800		V_{SD} = -20 V, V_{GD} = 0, V_{DB} = 0	
11		$I_{D(on)}$	ON Drain Current	-5	-30	-3	-30	mA	V_{DS} = -15 V, V_{GS} = -10 V	
12		$r_{DS(on)}$	Drain-Source ON Resistance		250		300	Ω	V_{GS} = -20 V, I_D = -100 μA	
13	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000	4,000	1,000	4,000	μmho	V_{DS} = -15 V, I_D = -10 mA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		250		250			
15		C_{iss}	Common-Source Input Capacitance		2.5		2.5	pF	V_{DS} = -15 V, I_D = -10 mA	f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		0.7		0.7			
17		C_{oss}	Common-Source Output Capacitance		3		3			
18	SW	$t_{d(on)}$	Turn-ON Delay Time		12		12	ns	V_{DD} = -15 V	
19		t_r	Rise Time		24		24		$I_{D(on)}$ = -10 mA	
20		t_{off}	Turn-OFF Time		50		50		R_G = R_L = 1.5 kΩ	

*JEDEC registered data

NOTE:
1. Transient gate-source voltage JEDEC registered as ±125 V.



INPUT PULSE
RISE TIME ≤ 2 ns
PULSE WIDTH > 200 ns

SAMPLING SCOPE
t_r ≤ 0.2 ns
C_{IN} ≤ 2 pF
R_{IN} ≥ 10 MΩ

MRA

depletion-type n-channel dual gate MOSFET

designed for . . .

Performance Curves MCB See Section 4

- **VHF Amplifiers**
- **IF Amplifiers**
- **Mixers**

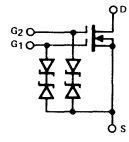
*ABSOLUTE MAXIMUM RATINGS (25°C)

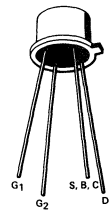
Drain-to-Gate Voltage . . . . . 20 V
Gate Current, Forward & Reverse . . . . . 1 mA
Drain-to-Source Voltage . . . . . 20 V
Drain Current, Continuous . . . . . 50 mA
Device Dissipation at T_{CASE} = 25°C . . . . . 1.2 W
Device Dissipation at T_A = 25°C. . . . . 330 mW
Free Air Temperature above 25°C derate linearly 2.2 mW/°C
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature 1/16" From Case for 10 Seconds . . 300°C

BENEFITS

- High Gain
  g_{fs} Typically 12 mmhos
- No Neutralization Required
  Low $C_{rss} < 0.03$ pF
- Automatic Gain Control with Second Gate

TO-72
See Section 5





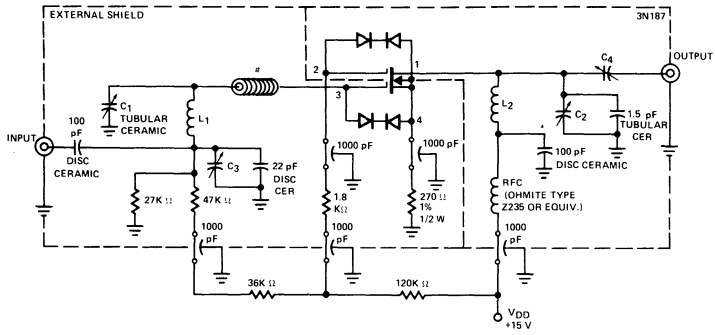
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{G1SS}	Gate One to Source Leakage Current			±50	nA	V_{G1S} = ±6 V, V_{G2S} = V_{DS} = 0	
2		I_{G2SS}	Gate Two to Source Leakage Current			±50		V_{G2S} = ±6 V, V_{G1S} = V_{DS} = 0	
3		I_{G1SS}	Gate One to Source Leakage Current			±5	μA	V_{G1S} = ±6 V, V_{G2S} = V_{DS} = 0	T_A = 100°C
4		I_{G2SS}	Gate Two to Source Leakage Current			±5		V_{G2S} = ±6 V, V_{G1S} = V_{DS} = 0	
5		BV_{G1SS}	Gate One to Source Breakdown Voltage	±6.5		±13	V	I_{G1} = ±100 μA, V_{G2S} = V_{DS} = 0	
6		BV_{G2SS}	Gate Two to Source Breakdown Voltage	±6.5		±13		I_{G2} = ±100 μA, V_{G1S} = V_{DS} = 0	
7		$V_{G1S(off)}$	Gate One to Source Cutoff Voltage	-.5		-4		V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 50 μA	
8		$V_{G2S(off)}$	Gate Two to Source Cutoff Voltage	-.5		-4		V_{DS} = 15 V, V_{G1S} = 0, I_D = 50 μA	
9		I_{DS}	Zero Gate One Voltage Drain Current	5	15	30	mA	V_{DS} = 15 V, V_{G2S} = 4 V, V_{G1S} = 0	
10	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 1)	7		18	mmho	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 kHz
11		C_{iss}	Common Source Input Capacitance		6	8.5	pF	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 MHz
12		C_{rss}	Common Source Reverse Transfer Capacitance		.02	.03			
13		C_{oss}	Common Source Output Capacitance		2.5				
14	HI FREQ	G_{ps}	Common Source Power Gain (Note 2)	16		22	dB	V_{DD} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 200 MHz
15		NF	Noise Figure (Note 2)			4.5			
16		G_{ps}	Common Source Power Gain (Notes 3 and 4)		12				f = 450 MHz
17		NF	Noise Figure (Notes 3 and 4)		5.5				

*JEDEC registered data

MCB

NOTES:
1. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.
2. See Figure 1.
3. See Figure 2.
4. Non-JEDEC registered data.



200 MHz Power Gain and Noise Figure Test Circuit
Figure 1

C_1 – 1.8 – 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2 – 1.5 – 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

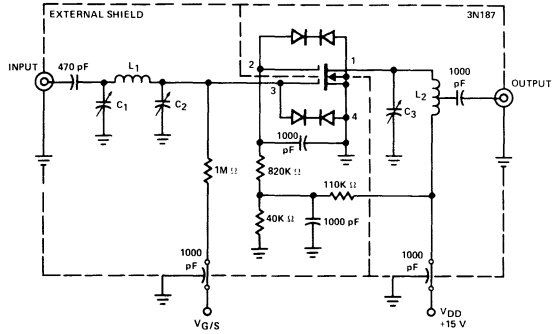
C_3 – 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4 – 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1 – 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in., winding length approx. 0.08 in.

L_2 – 4 1/2 turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil = .90 in. long.

– Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.



450 MHz Power Gain and Noise Figure Test Circuit
Figure 2

C_1 – 2 – 20 pF piston-type variable air capacitor; E.F. Johnson Type MVM 020.

C_2 – 1 – 10 pF piston-type variable air capacitor; E.F. Johnson Type VAM-010; Johanson Type 4335.

C_3 – 1 – 10 pF piston-type variable air capacitor; E.F. Johnson Type VAM-010; Johanson Type 4335.

L_1 – 1/2 turns No. 18 AWG.

L_2 – 1" No. 16 AWG tapped 1/4" from cold end.

depletion-type n-channel dual gate MOSFETs *designed for . . .*

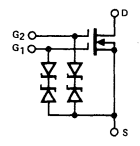
- **VHF Amplifiers**
- **Mixers**
- **IF Amplifiers**

Performance Curves MCB See Section 4

BENEFITS

- High Gain
  g_{fs} Typically 12 mmhos
- No Neutralization Required
  Low $C_{rss} < 0.03$ pF
- Automatic Gain Control with Second Gate

TO-72
See Section 5



*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Gate Voltage	30 V
Gate Current, Forward and Reverse	±10 mA
Drain-to-Source Voltage	25 V
Drain Current, Continuous	50 mA
Device Dissipation at T_{CASE} = 25°C	1.2 W
Device Dissipation at T_A = 25°C	360 mW
Free Air Temperature above 25°C	
Derate Linearly	2.2 mW/°C
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	3N201 Min	3N201 Typ	3N201 Max	3N202 Min	3N202 Typ	3N202 Max	3N203 Min	3N203 Typ	3N203 Max	Unit	Test Conditions	
1	STATIC	I_{G1SS} Gate One to Source Leakage Current			±10			±10			±10	nA	V_{G1S} = ±5 V, V_{G2S} = V_{DS} = 0	
2		I_{G2SS} Gate Two to Source Leakage Current			±10			±10			±10		V_{G2S} = ±5 V, V_{G1S} = V_{DS} = 0	
3		I_{G1SS} Gate One to Source Reverse Leakage Current			-10			-10			-10	µA	V_{G1S} = −5 V, V_{G2S} = V_{DS} = 0	
4		I_{G2SS} Gate Two to Source Reverse Leakage Current			-10			-10			-10		V_{G2S} = −5 V, V_{G1S} = V_{DS} = 0	T_A = 150°C
5		BV_{G1SS} Gate One to Source Breakdown Voltage	±6		±30	±6		±30	±6		±30	V	I_{G1} = ±10 mA, V_{G2S} = V_{DS} = 0	
6		BV_{G2SS} Gate Two to Source Breakdown Voltage	±6		±30	±6		±30	±6		±30		I_{G2} = ±10 mA, V_{G1S} = V_{DS} = 0	
7		BV_{DS} Drain to Source Breakdown Voltage	25			25			25				I_D = 10 µA, V_{G1S} = V_{G2S} = −5 V	
8		$V_{G1S(off)}$ Gate One to Source Cutoff Voltage	-0.5		-5	-0.5		-5	-0.5		-5		V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 20 µA	
9		$V_{G2S(off)}$ Gate Two to Source Cutoff Voltage	-0.2		-5	-0.2		-5	-0.2		-5		V_{DS} = 15 V, V_{G1S} = 0, I_D = 20 µA	
10		I_{DS} Zero Gate One Voltage Drain Current (Note 1)	6		30	6		30	3		15	mA	V_{DS} = 15 V, V_{G2S} = 4 V, V_{G1S} = 0,	
11		g_{fs} Common-Source Forward Transconductance (Note 1)	8		20	8		20	7		15	mmho		f = 1 kHz
12	DYNAMIC	C_{iss} Common-Source Input Capacitance (Note 2)		6			6			6		pF	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 MHz
13		C_{rss} Common-Source Reverse Transfer Capacitance		0.02	0.03		0.02	0.03		0.02	0.03			
14		C_{oss} Common-Source Output Capacitance (Note 2)		2.5			2.5			2.5				
15	HIGH FREQUENCY	NF Common-Source Spot Noise Figure			4.5							dB	V_{DD} = 18 V, V_{GG} = 7 V, f = 200 MHz See Figure 1	
16		G_{ps} Small-Signal Common-Source Insertion Power Gain	15		25							dB		
17		BW Bandwidth	5		9							MHz		
18		$V_{GG(GC)}$ Gain-Control Gate-Supply Voltage	0		3							V	V_{DD} = 18 V, ΔG_{ps} = −30 dB, (Note 3), f = 200 MHz, See Figure 1	
19		$G_{ps(conv)}$ Small-Signal Conversion Power Gain				15		25				dB	V_{DD} = 18 V, f_{LO} = 245 MHz (Note 4), f_{RF} = 200 MHz, See Figure 2	
20		BW Bandwidth				4.5		7.5				MHz		
21		NF Common-Source Spot Noise Figure									6	dB	V_{DD} = 18 V, V_{GG} = 6 V, f = 45 MHz, See Figure 3	
22		G_{ps} Small-Signal Common-Source Insertion Power Gain							20		30	dB		
23		BW Bandwidth							3		6	MHz		
24		$V_{GG(GC)}$ Gain-Control Gate-Supply Voltage							0		-3	V	V_{DD} = 18 V, ΔG_{ps} = −30 dB, (Note 5), f = 45 MHz, See Figure 3	

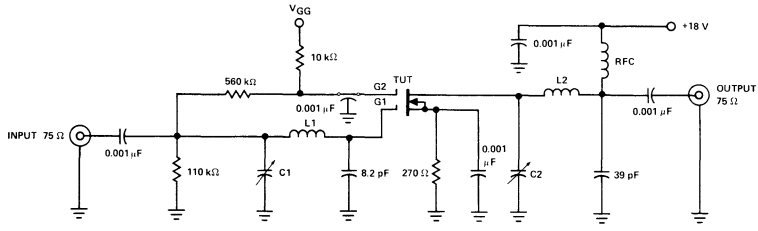
*JEDEC registered data.

2. Non-JEDEC registered data.
3. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7 V.
4. Amplitude at input from local oscillator is 3V rms.
5. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6 V.

NOTES:
1. Pulse test pulsewidth = 300 µs, duty cycle ≈ 3%.

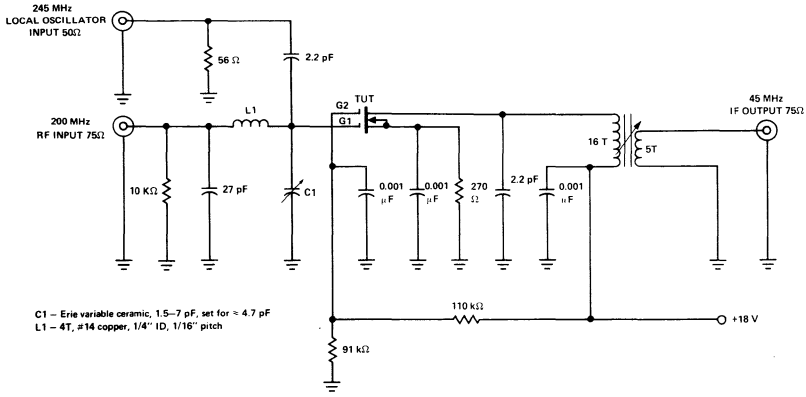
MCB

HIGH FREQUENCY TEST CIRCUITS



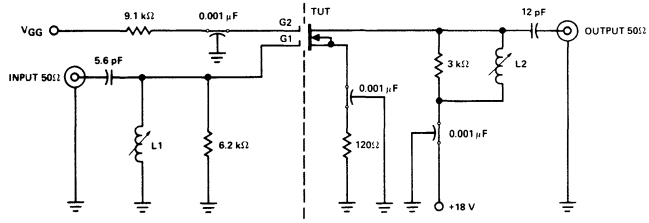
C1 – Erie variable ceramic, 4–30 pF, set for ≈ 22 pF
C2 – Erie variable ceramic, 4–30 pF, set for ≈ 10 pF
L1 – 4T, #14 copper, 1/4" ID, 1/6" pitch
L2 – 3T, #14 copper, 1/4" ID, 1/8" pitch
RFC – Delevan No. 153712 1μH

200 MHz Power Gain, Gain-Control Voltage and Noise Figure Test Circuit for 3N201
Figure 1



C1 – Erie variable ceramic, 1.5–7 pF, set for ≈ 4.7 pF
L1 – 4T, #14 copper, 1/4" ID, 1/16" pitch

200 MHz-to-45 MHz Circuit for Conversion Power Gain for 3N202
Figure 2



L1 – 14 T, #30 copper, close wound on 7/32" OD form with Arnold Engineering type "J" tuning core
L2 – 10 T, #30 copper, close-wound on 7/32" OD form with Arnold Engineering type "J" tuning core

45 MHz Power Gain, Gain-Control Voltage, and Noise Figure Test Circuit for 3N203
Figure 3

3

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NH
See Section 4

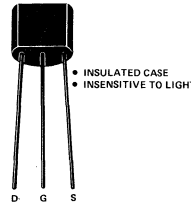
BENEFITS

- Wide Band
  High y_{fs}/C_{iss} Ratio
- Low Feedback Capacitance
  C_{rss} = 0.85 pF Typical
- Selected I_{DSS} and V_{GS} Ranges

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 30 V
Drain-Source Voltage . . . . . 30 V
Reverse Gate-Source Voltage. . . . . 30 V
Forward Gate Current. . . . . 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) . . . . . 200 mW
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic			Min	Typ	Max	Unit	Test Conditions
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage		−30			V	I_G = −1 μA, V_{DS} = 0
2		I_{GSS}	Gate Reverse Current				−5	nA	V_{GS} = −20 V, V_{DS} = 0
3		I_{DSS}	Saturation Drain Current		2		25	mA	V_{DS} = 15 V, V_{GS} = 0
4		I_{DSS}	Selected into Following Groups (Note 2)	BF244A	2.0		6.5	mA	V_{DS} = 15 V, V_{GS} = 0
5				BF244B	6.0		15	mA	
6				BF244C	12		25	mA	
7		V_{GS}	Corresponding to I_{DSS} groups	BF244A	−0.4		−2.2	V	V_{DS} = 15 V, I_D = 200 μA
8				BF244B	−1.6		−3.8	V	
9				BF244C	−3.2		−7.5	V	
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−0.5		−8	V	V_{DS} = 15 V, I_D = 10 μA
11	DYNAMIC	g_{fs}	Small-Signal Common-Source Forward Transconductance		3	5.5	6.5	mmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance			0.85		pF	V_{DS} = 20 V, V_{GS} = −1 V
13		$\frac{1}{g_{is}}$	Input Resistance			25		kΩ	V_{DS} = 20 V, V_{GS} = −1 V, f = 100 MHz
14						10		kΩ	f = 200 MHz
15		C_{iss}	Common-Source Input Capacitance			4		pF	V_{DS} = 20 V, V_{GS} = −1 V
16		C_{oss}	Common-Source Output Capacitance			1.6		pF	V_{DS} = 20 V, V_{GS} = −1 V

NOTE: NH

1. Derate linearly to 125° C free-air temperature at the rate of 2.5 mW/° C.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

- **VHF Amplifier**
- **Oscillators**
- **Mixers**

Performance Curves NC
See Section 4

BENEFITS

- Wide Band
  High y_{fs}/C_{iss} Ratio
- Low IMD

TO-92
See Section 5

TO-92 Variant
See Section 5

BF246

BF247
(Staggered Lead)

- INSULATED CASE
- INSENSITIVE TO LIGHT

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Reverse Gate-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) . . . . . 250 mW
Storage Temperature Range . . . . . −55° C to +150°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic			Min	Typ	Max	Unit	Test Conditions
1	BV_{GSS}	Gate-Source Breakdown Voltage		−25			V	$I_G = -1\ \mu A$, $V_{DS} = 0$
2	I_{GSS}	Gate Reverse Current				−5 −5	nA μA	$V_{GS} = -15$ V, $V_{DS} = 0$ $T_A = 100°C$
3	I_{DSS}	Saturation Drain Current (Note 2)	BF246 BF247	10		300	mA	$V_{DS} = 10$ V, $V_{GS} = 0$
			BF246A BD247A	30		80		
			BF246B BF247B	60		140		
			BF246C BF247C	110		250		
4	V_{GS}	Gate-Source Voltage	BF246 BF247	0.5		14	V	$V_{DS} = 15$ V, $I_D = 200\ \mu A$
			BF246A BF247A	1.5		4.0		
			BF246B BF247B	3.0		7.0		
			BF246C BF247C	5.5		12		
5	$V_{GS(off)}$	Gate-Source Cutoff Voltage		0.6		14.5	V	$V_{DS} = 15$ V, $I_D = 10$ nA
6	g_{fs}	Small-Signal Common-Source Forward Transconductance (Note 2)			25		mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz
7	C_{iss}	Common-Source Short-Circuit Input Capacitance				12	pF	$V_{DS} = 10$ V, $V_{GS} = -1$ V, f = 1 MHz
8	C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance				2.5	pF	$V_{DS} = 10$ V, $V_{GS} = -4$ V, f = 1 MHz

NOTES: NC

1. Derate linearly to 125°C free air temperature at the rate of 2.5 mW/°C.
2. These parameters must be measured using pulse techniques $t_p \leq 300\ \mu s$, duty cycle ≤ 2%.

n-channel JFETs *designed for . . .*

- **UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH See Section 4

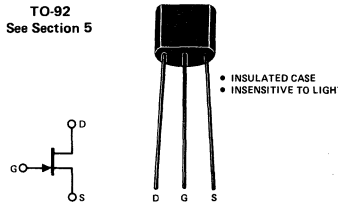
BENEFITS

- High Gain
  G_{pg} = 14 dB Typical at 800 MHz
- Selected I_{DSS} Ranges

ABSOLUTE MAXIMUM RATINGS

Drain-Gate Voltage . . . . . 30 V
Drain-Source Voltage . . . . . 30 V
Reverse Gate-Source Voltage. . . . . 30 V
Forward Gate Current. . . . . 50 mA
Total Device Dissipation @ 25°C. . . . . 350 mW
Derate above 25°C . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	BV_{DGO}	Drain-Gate Breakdown Voltage	−30			V	I_G = −1 μA, V_{DS} = 0
2		I_{GSS}	Gate-Reverse Current			−5	nA	V_{GS} = −20 V, V_{DS} = 0
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−7.5	V	V_{DS} = 15 V, I_D = 10 nA
4		I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	3	12	18	mA	V_{DS} = 15 V, V_{GS} = 0
5		I_{DSS} Selected into Following Groups (Note 1)	BF256LA	3		7	mA	
6			BF256LB	6		13	mA	
7			BF256LC	11		18	mA	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4.5	5.5		mmho	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		50		μmho	
10		C_{iss}	Common-Source Input Capacitance			4.5	pF	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.2	pF	
12		$f(y_{fs})$	Cutoff Frequency (Note 2)		1000		MHz	
13		G_{pg}	Common-Gate Neutralized Insertion Power Gain		14		dB	V_{DS} = 10 V, R_S = 47 Ω, f = 800 MHz
14		NF	Noise Figure		7.5		dB	V_{DS} = 15 V, R_S = 47 Ω, f = 800 MHz

NH

NOTES:
1. Pulse test PW ≤ 300 μs, duty cycle ≤ 2%.
2. Frequency at which the real part of the forward transconductance falls 3 dB relative to the value at 1 kHz.

depletion-type n-channel dual gate MOSFET

designed for . . .

- **Tuners—FM and TV**
- **General Common Source RF Amplifier Usage to 600 MHz**
- **UHF Mixer Circuits Up to 900 MHz**

Performance Curves MCB See Section 4

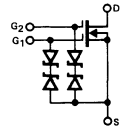
BENEFITS

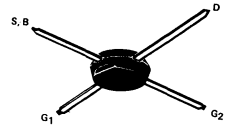
- High Gain
  g_{fs} Typically 14 mmhos
- No Neutralization Required
  Low C_{rss} Typically 0.025 pF
- Automatic Gain Control with Second Gate
- Rugged
  Zener Diode Input Protection

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . 20 V
Drain-to-Gate Voltage . . . . . 20 V
Gate-to-Source Voltage . . . . . ±6 V
Gate-to-Gate Voltage . . . . . ±12 V
Continuous Drain Current . . . . . 50 mA
Gate Current . . . . . ±10 mA
Total Continuous Device Dissipation
at (or Below) T_A = 25°C
(Derate 1.5 mW/°C to 125°C) . . . . . 150 mW
Operating Temperature Range . . . . . −55 to +125°C
Storage Temperature Range . . . . . −55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

OD-84
See Section 5



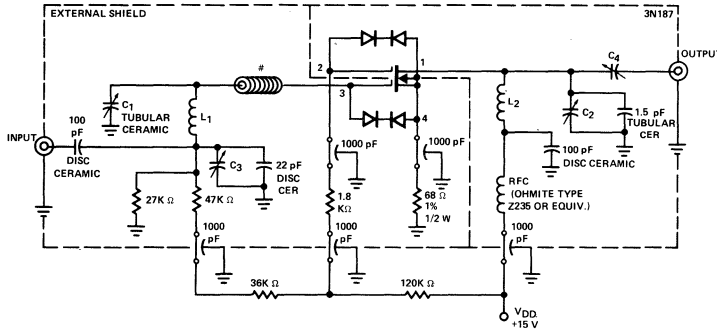


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{G1SS}	Gate One to Source Leakage Current			±100	nA	V_{G1S} = ±5 V, V_{G2S} = V_{DS} = 0	
2		I_{G2SS}	Gate Two to Source Leakage Current			±100		V_{G2S} = ±5 V, V_{G1S} = V_{DS} = 0	
3		BV_{DS}	Drain to Source Breakdown Voltage	20			V	I_D = 10 μA, V_{G1S} = V_{G2S} = −4 V	
4		BV_{G1SS}	Gate One to Source Breakdown Voltage	±6		±30		I_{G1} = ±10 mA, V_{G2S} = V_{DS} = 0	
5		BV_{G2SS}	Gate Two to Source Breakdown Voltage	±6		±30		I_{G2} = ±10 mA, V_{G1S} = V_{DS} = 0	
6		$V_{G1S(off)}$	Gate One to Source Cutoff Voltage			−5		V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 20 μA	
7		$V_{G2S(off)}$	Gate Two to Source Cutoff Voltage			−5		V_{DS} = 15 V, V_{G1S} = 0, I_D = 20 μA	
8		I_{DS}	Zero Gate One Voltage Drain Current (Note 1)	3	15	30	mA	V_{DS} = 15 V, V_{G2S} = 4 V, V_{G1S} = 0	
9	DYNAMIC	g_{fs} (Note 1)	Common Source Forward Transconductance	8	14		mmho	V_{DS} = 15 V, V_{G2S} = 4 V, V_{G1S} = 0	f = 1 kHz
10		C_{iss}	Common Source Input Capacitance		4.0		pF	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 10 mA	f = 1 MHz
11		C_{rss}	Common Source Reverse Transfer Capacitance		0.025				
12		C_{oss}	Common Source Output Capacitance		2.0				
13	HF	G_{ps} (Note 2)	Common-Source Power Gain		20		dB	V_{DD} = 15 V, V_{G2S} = 4 V, R_S = 68 Ω	f = 200 MHz, BW = 12 MHz
14		NF (Note 2)	Noise Figure		2.0	4.5			f = 200 MHz

NOTES:
1. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.
2. See Figure 1.

MCB



200 MHz Power Gain and Noise Figure Test Circuit for BF900
Figure 1

C_1 – 1.8 – 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2 – 1.5 – 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3 – 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4 – 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1 – 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in., winding length approx. 0.8 in.

L_2 – 4 1/2 turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈ .90 in. long.

= – Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.

current regulator diodes designed for . . .

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

Performance Curves
NKL NKM NKO See Section 4

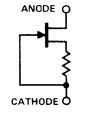
BENEFITS

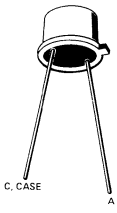
- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  Temperature Coefficient Better Than 1500 ppm/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at T_C = 25°C	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55 to +200°C

TO-18
See Section 5





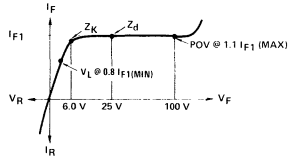
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	I_{F1}			Z_d		Z_k		V_L		POV	η_1			GEOM
Parameter	Regulator Current			Dynamic Impedance		Knee Impedance		Limiting Voltage		Peak Operating Voltage	Temperature Coefficient			
Test Conditions	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)		V_F = 6 V		I_F = 0.8 $I_{F1(Min)}$ (Note 3)		I_F = 1.1 $I_{F1(Max)}$ (Note 4)	V_F = 25 V 55°C ≤ T_A ≤ 25°C	V_F = 25 V 0°C ≤ T_A ≤ 50°C	V_F = 25 V 25°C ≤ T_A ≤ 125°C	
Units	(mA)			MΩ		MΩ		Volts		Min Volts	Typ ppm/°C	Typ ppm/°C	Typ ppm/°C	
	Nom	Min	Max	Min	Typ	Min	Typ	Max	Typ					
CR022	0.22	0.198	0.242	13.0	16.0	2.75	3.5	1.0	0.40	100	+1350	+1050	+750	
CR024	0.24	0.216	0.264	10.0	14.0	2.35	3.0	1.0	0.45	100	+1200	+900	+600	
CR027	0.27	0.243	0.297	9.0	13.0	1.95	2.8	1.0	0.50	100	+1000	+700	+400	
CR030	0.30	0.270	0.330	8.0	12.0	1.60	2.5	1.0	0.55	100	+800	+500	+200	
CR033	0.33	0.297	0.363	6.6	11.0	1.35	2.2	1.0	0.60	100	+600	+300	50	N K L
CR039	0.39	0.351	0.429	4.10	9.5	1.00	1.90	1.05	0.70	100	+300	+50	-300	
CR043	0.43	0.387	0.473	3.30	8.6	0.87	1.65	1.05	0.78	100	+150	-150	-450	
CR047	0.47	0.423	0.517	2.70	8.0	0.75	1.50	1.10	0.85	100	-50	-300	-600	
CR056	0.56	0.504	0.616	1.90	6.5	0.56	1.25	1.20	0.98	100	-300	-600	-900	
CR062	0.62	0.558	0.682	1.55	6.2	0.47	1.15	1.30	1.10	100	-500	-800	-1100	
CR068	0.68	0.612	0.748	1.35	8.5	0.400	1.70	1.15	0.70	100	+850	+400	-50	
CR075	0.75	0.675	0.825	1.15	7.2	0.335	1.50	1.20	0.75	100	+650	+200	-250	
CR082	0.82	0.738	0.902	1.00	6.0	0.290	1.30	1.25	0.80	100	+450	+50	-450	
CR091	0.91	0.819	1.001	0.88	5.2	0.240	1.10	1.29	0.85	100	+300	-150	-600	
CR100	1.00	0.900	1.100	0.80	4.4	0.205	0.95	1.35	0.95	100	+150	-300	-750	N K M
CR110	1.10	0.990	1.210	0.70	3.8	0.180	0.80	1.40	1.05	100	+50	-450	-900	
CR120	1.20	1.08	1.32	0.64	3.3	0.155	0.71	1.45	1.15	100	-150	-600	-1050	
CR130	1.30	1.17	1.43	0.58	3.2	0.135	0.60	1.50	1.25	100	-300	-750	-1200	
CR140	1.40	1.26	1.54	0.54	2.5	0.115	0.52	1.55	1.30	100	-400	-850	-1300	
CR150	1.50	1.35	1.65	0.51	2.2	0.105	0.46	1.60	1.35	100	-500	-950	-1400	
CR160	1.60	1.44	1.76	0.475	1.00	0.092	0.35	1.65	0.50	100	+650	+350	+50	
CR180	1.80	1.62	1.98	0.420	0.95	0.074	0.30	1.75	0.55	100	+500	+200	-100	
CR200	2.00	1.80	2.20	0.395	0.88	0.061	0.25	1.85	0.60	100	+350	+50	-250	
CR220	2.20	1.98	2.42	0.370	0.80	0.052	0.22	1.95	0.65	100	+200	-100	-350	
CR240	2.40	2.16	2.64	0.345	0.75	0.044	0.20	2.00	0.70	100	+50	-200	-450	N K O
CR270	2.70	2.43	2.97	0.320	0.68	0.035	0.18	2.15	0.75	100	-100	-300	-550	
CR300	3.00	2.70	3.30	0.300	0.60	0.029	0.14	2.25	0.85	100	-250	-450	-700	
CR330	3.30	2.97	3.63	0.280	0.56	0.024	0.13	2.35	0.90	100	-400	-600	-800	
CR360	3.60	3.24	3.96	0.265	0.52	0.020	0.11	2.50	0.95	100	-550	-750	-900	
CR390	3.90	3.51	4.29	0.255	0.48	0.017	0.10	2.60	1.00	100	-700	-850	-1000	
CR430	4.30	3.87	4.73	0.245	0.45	0.014	0.09	2.75	1.10	100	-850	-950	-1100	
CR470	4.70	4.23	5.17	0.235	0.40	0.012	0.08	2.90	1.40	100	-1000	-1100	-1200	

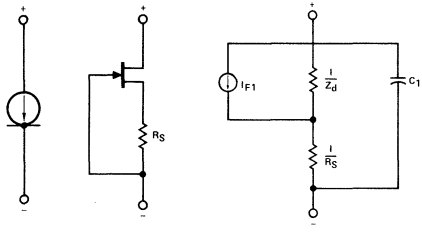
NOTES:
1. Pulse test – steady state currents may vary.
2. Pulse test – steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F1(min)}$.
4. Max V_F where $I_F < 1.1\ I_{F1(max)}$ is guaranteed.

NKL, NKM, NKO

Current-Limiter Diode V-I Characteristic



EQUIVALENT CIRCUIT



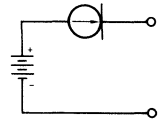
SYMBOLS AND DEFINITIONS

A	Anode (Drain)
C	Cathode (Source and Gate Shorted)
I_F	Forward Current (Anode Positive)
I_{F1}	Current at a specified Test Voltage, V_F
POV	Peak Operating Voltage
θ_I	Current Temperature Coefficient
θ_{JC}	Thermal Resistance Junction to Case
θ_{JA}	Thermal Resistance Junction to Ambient
Z_K	Knee AC Impedance at specified V_F. Z_K should be as high as possible and is specified as a minimum.
Z_d	Dynamic Impedance at specified V_F. Z_d is specified as a minimum.

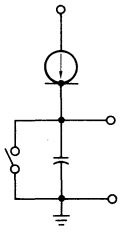
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

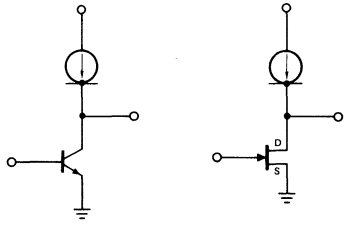
Constant-Current Supply or Current-Limiting Element



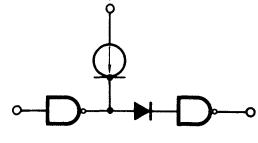
Constant-Current Timing Circuits



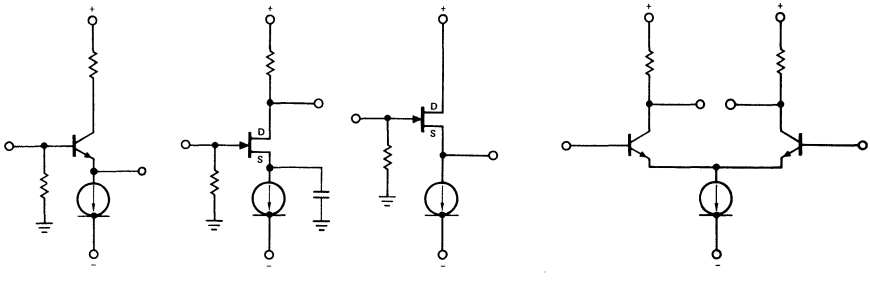
Collector or Drain Hi-Z Load Resistors



Logic Circuit Pull-Up Current Source



Emitter or Source Biasing



dual pico ampere diodes

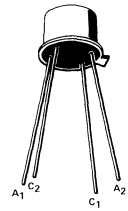
designed for . . .

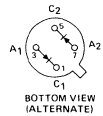
- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

- Very High Off-Isolation 1 pA Max (DPAD1)
- High Isolation Between Diodes 20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

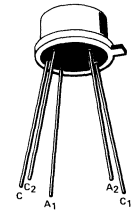
SI-71 or TO-71
(Pins 2 and 6 Removed)
See Section 5

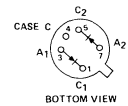




BOTTOM VIEW
(ALTERNATE)

TO-78
(DPAD1 Only)
See Section 5





BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (25°C)

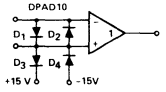
Forward Gate Current, Each Side. . . . . 50 mA
Total Device Dissipation @ T_A = 25°C
Derate 4.0 mW/°C to 125°C. . . . . 400 mW
Storage Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

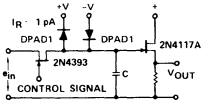
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION	
1	STATIC	I_R	Reverse Current			−1	pA	V_R = −20 V	DPAD1
2						−2			DPAD2
3						−5			DPAD5
4						−10			DPAD10
5						−20			DPAD20
6						−50			DPAD50
7						−100			DPAD100
8		B_{VR}	Reverse Breakdown Voltage	−45		−120	V	I_R = −1 μA	DPAD1, 2, 5
9				−35					DPAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		I_F = 1 mA	DPAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	V_R = −5 V, f = 1 MHz	DPAD1, 2, 5
12						2.0			DPAD10, 20, 50, 100
13	MAT	$\lvert C_{R1}-C_{R2}\rvert$	Differential Capacitance		0.1	0.2	pF	$V_{R1} = V_{R2}$ = −5 V, f = 1 MHz	DPAD1, 2, 5, 10, 20, 50, 100

APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS D_1 and D_2 Common mode input voltage limited by DPADS D_3 and D_4 to ±15 V.



Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



n-channel JFETs *designed for . . .*

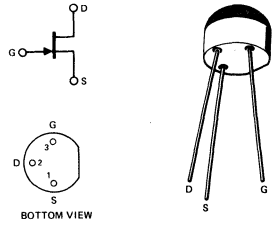
- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NVA See Section 4

BENEFITS

- Very Low Insertion Loss
  $R_{DS(on)} < 3\ \Omega$ (E105)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-30 V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	-55 to +125°C
Operating Temperature Range	-55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E105			E106			E107			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-30			-30			-30			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	500			200			100			mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160	pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions	
11	DYNAMIC	t_r	Rise Time		20			20			20		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		15			15			15		ns		
13	DYNAMIC	t_f	Fall Time		20			20			20		ns		

Switching Time Test Conditions	E105	E106	E107
V_{DD}	1.5 V	1.5 V	1.5 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	50 Ω	50 Ω	50 Ω

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NVA

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

Performance Curves NIP
See Section 4

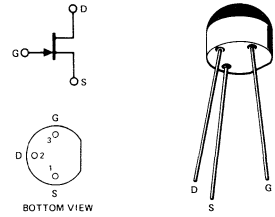
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 8\ \Omega$ (E108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 5$ ns Typical
- Low Noise
  $\overline{e_n} = 6\ nV/\sqrt{Hz}$ at 10 Hz, Typical (E110)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E108			E109			E110			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	$V_{DS} = 0$, $V_{GS} = -15$ V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	-2		-6	-0.5		-4	V	$V_{DS} = 5$ V, $I_D = 1\ \mu$A
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	$V_{DS} = 0$, $I_G = -1\ \mu$A
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	80			40			10			mA	$V_{DS} = 15$ V, $V_{GS} = 0$
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			8			12			18	Ω	$V_{DS} \leq 0.1$ V, $V_{GS} = 0$
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0$, $V_{GS} = -10$ V, f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0$, $V_{GS} = -10$ V, f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85	pF	$V_{DS} = V_{GS} = 0$, f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		4			4			4		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		1			1			1		ns	E108 / E109 / E110
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		6			6			6		ns	V_{DD}: 1.5 V / 1.5 V / 1.5 V
13	DYNAMIC	t_f	Fall Time		30			30			30		ns	$V_{GS(off)}$: -12 V / -7 V / -5 V; R_L: 150 Ω / 150 Ω / 150 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NIP

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 4

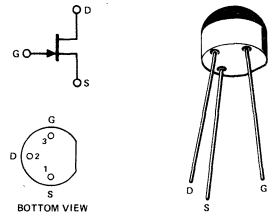
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (E111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -35 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics	E111 Min	E111 Typ	E111 Max	E112 Min	E112 Typ	E112 Max	E113 Min	E113 Typ	E113 Max	Unit	Test Conditions
1	STATIC	I_{GSS} Gate Reverse Current (Note 1)			-1			-1			-1	nA	$V_{DS} = 0$, $V_{GS} = -15$ V
2	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-3		-10	-1		-5	-0.5		-3	V	$V_{DS} = 5$ V, $I_D = 1\ \mu$A
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	-35			-35			-35			V	$V_{DS} = 0$, $I_G = -1\ \mu$A
4	STATIC	I_{DSS} Saturation Drain Current (Note 2)	20			5			2			mA	$V_{DS} = 15$ V, $V_{GS} = 0$
5	STATIC	$I_{D(off)}$ Drain Cutoff Current (Note 1)			1			1			1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance			30			50			100	Ω	$V_{DS} \leq 0.1$ V, $V_{GS} = 0$
7	DYNAMIC	$C_{dg(off)}$ Drain-Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0$, $V_{GS} = -10$ V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$ Source-Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0$, $V_{GS} = -10$ V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance			28			28			28	pF	$V_{DS} = V_{GS} = 0$; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$ Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions
11	DYNAMIC	t_r Rise Time		6			6			6		ns	
12	DYNAMIC	$t_{d(off)}$ Turn Off Delay Time		20			20			20		ns	
13	DYNAMIC	t_f Fall Time		15			15			15		ns	

Switching Time Test Conditions	E111	E112	E113
V_{DD}	10 V	10 V	10 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	800 Ω	1,600 Ω	3,200 Ω

NC

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 4

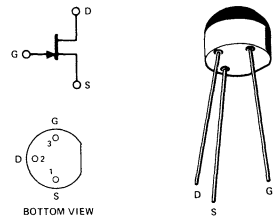
BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (E111A)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- No Error or Offset Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Drain Current . . . . . 400 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E111A		E112A		E113A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)		−200		−200		−200	pA	V_{DS} = 0, V_{GS} = −15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5	−10	−2	−7	−1	−5	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	30		15		8		mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)		200		200		200	pA	V_{DS} = 5 V, V_{GS} = −10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance		30		50		80	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYN	$C_{dg(off)}$	Drain Gate OFF Capacitance		5		5		5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
8	DYN	$C_{sg(off)}$	Source-Gate OFF Capacitance		5		5		5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
9	DYN	$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance		28		28		28	pF	$V_{DS} = V_{GS}$ = 0	f = 1 MHz

NOTES: NC
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

n-channel JFET
designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NZF
See Section 4

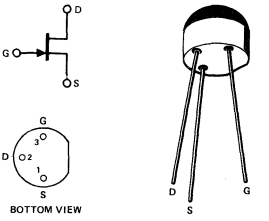
BENEFITS

- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Very Fast Switching
  - $t_{D(on)} + t_r = 6$ ns Typical
- Short Sample and Hold Aperture Time
  - $C_{gd(off)} < 2$ pF
  - $C_{gs(off)} < 2$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	-55 to +125°C
Operating Temperature Range	-55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E114 Min	E114 Typ	E114 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1	nA	$V_{DS} = 0$, $V_{GS} = -15$ V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	V	$V_{DS} = 5$ V, $I_D = 1$ μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	$V_{DS} = 0$, $I_G = -1$ μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	15			mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			150	Ω	$V_{DS} \leq 0.1$ V, $V_{GS} = 0$	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			2	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance			2	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			8	pF	$V_{DS} = V_{GS} = 0$	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		3		ns	Switching Time Test Conditions: $V_{DD} = 10$ V, $V_{GS(off)} = -12$ V, $R_L = 1$ KΩ, $V_{GS(on)} = 0$	
11	DYNAMIC	t_r	Rise Time		3		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		12		ns		
13	DYNAMIC	t_f	Fall Time		8		ns		

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NZF

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 4

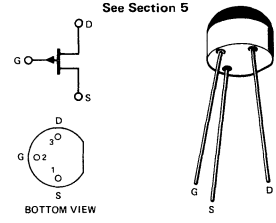
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (E174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)}$ = 5.5 pF Typical
  $C_{dg(off)}$ = 5.5 pF Typical
- Fast Switching
  $t_{d(on)} + t_r$ = 7 ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics	E174 Min	E174 Typ	E174 Max	E175 Min	E175 Typ	E175 Max	E176 Min	E176 Typ	E176 Max	E177 Min	E177 Typ	E177 Max	Unit	Test Conditions
1	STATIC	I_{GSS} Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20 V
2	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15 V, I_D = -10 nA
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1 μA
4	STATIC	I_{DSS} Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V_{DS} = -15 V, V_{GS} = 0
5	STATIC	$I_{D(off)}$ Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15 V, V_{GS} = 10 V
6	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1 V
7	DYNAMIC	$C_{dg(off)}$ Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$ Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance		40			40			40			40		pF	V_{DS} = V_{GS} = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$ Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions
11	DYNAMIC	t_r Rise Time		5			10			20			25		ns	
12	DYNAMIC	$t_{d(off)}$ Turn Off Delay Time		5			10			15			20		ns	
13	DYNAMIC	t_f Fall Time		10			20			20			25		ns	

Switching Time Test Conditions	E174	E175	E176	E177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

PS

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

■ General Purpose Amplifiers

Performance Curves NP
See Section 4

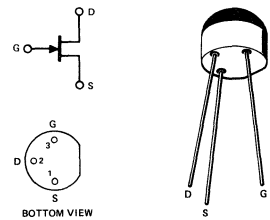
BENEFITS

- High Input Impedance
  I_G = 35 pA Typical
- Good for Low Power Supply Operation
  $V_{GS(off)} < 1.5$ V (E201)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate Current ..... 50 mA
Total Device Dissipation
(25°C Free-Air Temperature)..... 350 mW
Power Derating (to +125°C)..... 3.5 mW/°C
Storage Temperature Range..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E201			E202			E203			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	V	V_{DS} = 20 V, I_D = 10 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		-35			-35			-35		pA	V_{DG} = 20 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	500			1,000			1,500			μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance		1			3.5			10		μmho		f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		5			5			5		pF		f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		2			2			2		pF		f = 1 MHz
10	DYNAMIC	$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		5			5			5		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES: **NP**

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration - 2 ms.

n-channel JFETs *designed for . . .*

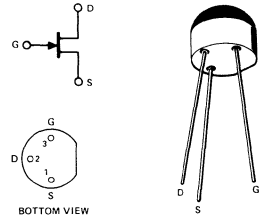
■ General Purpose Switching

Performance Curves NP
See Section 4

BENEFITS

- Very Low Leakage

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−25 V
Gate Current	50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55 to +125°C
Operating Temperature Range	−55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E204 Min	E204 Typ	E204 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			−100	pA	V_{DS} = 0, V_{GS} = −20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−2.0	V	V_{DS} = 20 V, I_D = 10 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25			V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)		1.2		mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		−35		pA	V_{DG} = 20 V, I_D = 200 μA	
6	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 3)		1500		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance		2.5		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		2		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES:

NP

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs *designed for . . .*

■ General Purpose Amplifiers

Performance Curves NZF See Section 4

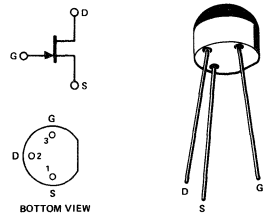
BENEFITS

- High Gain
  G_{FS} = 7000 μmho Minimum (E211, E212)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -25 V
Gate Current ..... 10 mA
Total Device Dissipation
(25°C Free-Air Temperature) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E210			E211			E212			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2.5		-4.5	-4		-6	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	V_{DS} = 15 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 1 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	7,000		12,000	7,000		12,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			150			200			200			
8		C_{iss}	Common-Source Input Capacitance		5.0			5.0			5.0		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5			1.5			1.5				
10		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NZF

n-channel JFETs *designed for . . .*

■ Audio and Sub-Audio Amplifiers

Performance Curves NS See Section 4

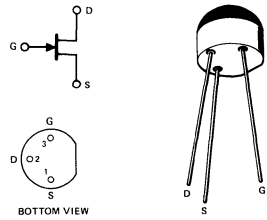
BENEFITS

- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate Current ..... 50 mA
Total Device Dissipation .....
(25°C Free-Air Temperature)..... 350 mW
Power Derating (to +125°C)..... 3.5 mW/°C
Storage Temperature Range..... -55 to +125°C
Operating Temperature Range..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E230			E231			E232			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-250			-250			-250	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2		-5	-4		-6	V	V_{DS} = 20 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	0.7		3	2		6	5		10	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 0.5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1,000		2,500	1,500		3,000	2,500		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			2			4			6	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		15			15			15		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		2			2			2		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		8	30		8	30		8	30	nV/√Hz	V_{DS} = 10 V, V_{GS} = 0	f = 10 Hz
11	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		2			2			2		nV/√Hz	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES: NS
1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

p-channel JFETs *designed for . . .*

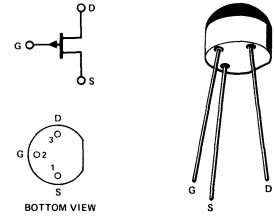
■ General Purpose Amplifiers

Performance Curves PS See Section 4

BENEFITS

- High Gain Amplifiers
  g_{fs} = 14,000 μmho Typical (E271)
- Low Noise
  $\overline{e_n}$ = 10 nV/√Hz at 1 kHz Typical

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	-50 mA
Total Device Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55 to +125°C
Operating Temperature Range	−55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E270 Min	E270 Typ	E270 Max	E271 Min	E271 Typ	E271 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V_{DS} = -15 V, I_D = -1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			V	V_{DS} = 0, I_G = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-2		-15	-6		-50	mA	V_{DS} = -15 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = -15 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	μmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			200			500	μmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		20			20		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		5			5		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	e_n	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = -10 V, I_D = $I_{DSS(min)}$	f = 1 kHz

NOTES: PS

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFET
designed for . . .

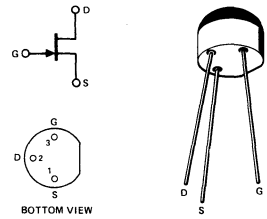
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZF
See Section 4

BENEFITS

- High Power Gain
  22 dB Typical at 100 MHz
  Common-Source
  17 dB Typical at 100 MHz
  Common-Gate
- Low Noise
  NF = 2 dB Typical at 100 MHz
- High Dynamic Range Greater than 100 dB

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E300 Min	E300 Typ	E300 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500	pA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	V	V_{DS} = 10 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25				V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5	STATIC	$V_{GS(f)}$	Gate-Source Forward Voltage			1	V	I_G = 1 mA, V_{DS} = 0	
6	DYN	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		9,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7	DYN	g_{os}	Common-Source Output Transconductance			200			
8	DYN	C_{iss}	Common-Source Input Capacitance		3.5	5.5	pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
9	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	1.7			
10	DYN	C_{oss}	Common-Source Output Capacitance		1.5				
11	HI FREQ	$\lvert y_{fs} \rvert$	Common-Source Forward Transcadmittance		6,200		μmho	V_{DG} = 15 V, I_D = 5 mA	f = 100 MHz
12	HI FREQ				6,000				f = 450 MHz
13	HI FREQ	$\lvert y_{fg} \rvert$	Common-Gate Forward Transcadmittance		6,000				f = 100 MHz
14	HI FREQ				5,500				f = 450 MHz
15	HI FREQ	G_{fg}	Common-Gate Power Gain		17		dB		f = 100 MHz (Note 3)
16	HI FREQ	NF	Noise Figure (Single Sideband)		2				

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Typical values for performance at 100 MHz in a common-gate circuit operating 3 dB bandwidth is 2 MHz.

NZF

n-channel JFETs *designed for . . .*

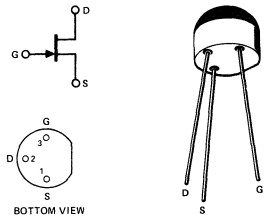
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NH See Section 4

BENEFITS

- Characterized for Operation at 100 and 400 MHz
- Low Noise
  NF = 1.7 dB Typical at 100 MHz

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E304			E305			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	-2		-6	-0.5		-3	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate Source Breakdown Voltage	-30			-30				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Transconductance			50			50			
7		C_{iss}	Common-Source Input Capacitance		3.0			3.0		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8				
9		C_{oss}	Common-Source Output Capacitance		1.0			1.0				
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
11					4,200							f = 400 MHz
12		g_{oss}	Common-Source Output Conductance		60			60				f = 100 MHz
13					80							f = 400 MHz
14		b_{oss}	Common-Source Output Susceptance		800			800				f = 100 MHz
15					3,600							f = 400 MHz
16		g_{iss}	Common-Source Input Conductance		80			80				f = 100 MHz
17					800							f = 400 MHz
18		b_{iss}	Common-Source Input Susceptance		2,000			2,000				f = 100 MHz
19					7,500							f = 400 MHz
20		G_{ps}	Common-Source Power Gain		20					dB	V_{DS} = 15 V, I_D = 5 mA	f = 100 MHz
21					11							f = 400 MHz
22		NF	Noise Figure (Single Sideband)		1.7						V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ	f = 100 MHz
23					3.8							f = 400 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

monolithic dual n-channel JFETs *designed for . . .*

- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**

Performance Curves NQP
See Section 4

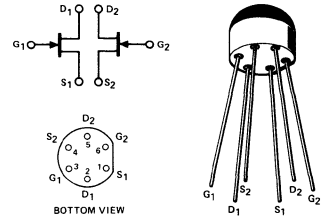
BENEFITS

- Minimum System Error and Calibration
  10 mV Offset Maximum (E400, E401)
  80 dB Typical CMRR
- Low Drift with Temperature
  10 μV/°C (E400)
- Simplifies Amplifier Design
  Output Conductance < 10 μmho

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage ..... ±40 V
Gate-Drain or Gate-Source Voltage ..... -40 V
Gate Current ..... 50 mA
Total Package Dissipation
(25°C Free-Air Temperature) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... -55 to +125°C
Operating Temperature Range ..... -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

Si-200
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E400 Min	E400 Typ	E400 Max	E401 Min	E401 Typ	E401 Max	E402 Min	E402 Typ	E402 Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current (Note 1)			-200			-200			-200	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-4.5	-1.0		-4.5	-1.0		-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)			-200			-200			-200	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	-0.2		-4.0	-0.2		-4.0	-0.2		-4.0	V	V_{DG} = 20 V, I_D = 200 μA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	600		1,600	600		1,600	600		1,600	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			35			35			35	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			10			10			10	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		13			13			13		$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			10			20	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)			10			25			50	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V, I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP

monolithic dual n-channel JFETs *designed for . . .*

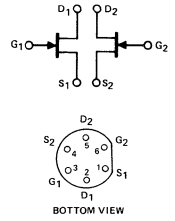
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

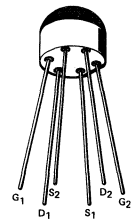
Performance Curves NQP
See Section 4

BENEFITS

- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (E410)
  70 dB Minimum CMRR (E410)
- Low Drift with Temperature
  10 μV/°C Maximum (E410)
- Simplifies Amplifier Design
  Low Output Conductance

Si-200
See Section 5





ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±40 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Package Dissipation (25°C Free-Air) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range . . . . . −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E410			E411			E412			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-250			-250			-250	pA	V_{DS} = 0, V_{GS} = −30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-3.5	-0.5		-3.5	-0.5		-3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5		6.0	0.5		6.0	0.5		6.0	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)			-250			-250			-250	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	−0.2		−3.0	−0.2		−3.0	−0.2		−3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	600		1,200	600		1,200	600		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0	
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2		pF		
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		13	50		13	50		13	50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			25			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)	70	80		80			70			dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP

matched dual n-channel JFETs *designed for . . .*

■ VHF/UHF Amplifiers

Performance Curves NZF
See Section 4

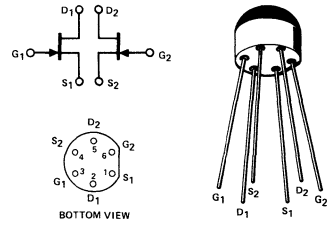
BENEFITS

- High Gain
  g_{fs} = 4500 μmho Minimum
- Dual Version of E300 with Matched Gate-to-Source Voltage

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±50 V
Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Total Package Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

Si-200
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E420 Min	E420 Typ	E420 Max	E421 Min	E421 Typ	E421 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500			-500	pA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	-1		-6	V	V_{DS} = 10 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)			-500			-500	pA	V_{DG} = 10 V, I_D = 5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			200			200	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8		pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
10	MAT	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20	mV	V_{DG} = 10 V, I_D = 5 mA	

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.

matched dual n-channel JFETs *designed for . . .*

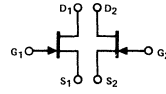
- **Cascode Amplifiers**
- **Balanced Mixers**

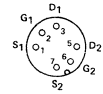
Performance Curves NZA See Section 4

BENEFITS

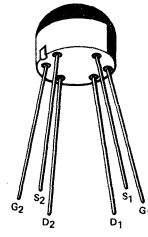
- Low Noise Figure
- Very Low Distortion +30 dBm Intercept Point

TO-105
See Section 5





BOTTOM VIEW



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range. . . . . −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds). . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		E430			E431			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150	pA	V_{GS} = -15 V, V_{DS} = 0	
2						-150			-150	nA		T = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-4.0	-2.0		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0	V	V_{DS} = 0, I_G = 10 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10		20	10		20	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			150			150	μmho		
9		C_{gs}	Gate Source Capacitance			5.0			5.0	pF	V_{GS} = -10 V, V_{DS} = 0	f = 1 MHz
10		C_{gd}	Drain Gate Capacitance			2.5			2.5			
11		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HIGH FREQ	g_{fs}	Common-Source Forward Transconductance		12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
13		g_{os}	Common-Source Output Conductance		0.15			0.15				
14		g_{ig}	Power-Match Source Admittance		12			12				
15		G_c	Conversion Gain (Note 2)		3.0			3.0		dB	V_{DS} = 20 V, V_{GS} = 1/2 $V_{GS(off)}$	f = 100 MHz
16		IMD	Intercept Point (Notes 2 and 3)		+30			+30		dBm		
17	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 4)	0.9		1.0	0.9		1.0		V_{DS} = 10 V	V_{GS} = 0
18		$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	Gate-Source Cutoff Voltage Ratio (Note 4)	0.9		1.0	0.9		1.0			I_D = 1 nA
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 4)	0.9		1.0	0.9		1.0			I_D = 10 mA

NOTES:
1. Pulse test duration = 300 μs, duty cycle ≤ 3%.
2. VHF single-balanced mixer drain load impedance 2K Ω.
3. 2-tone 3rd-order IMD.
4. Assumes smaller value in numerator.

NZA

current regulator diodes

designed for . . .

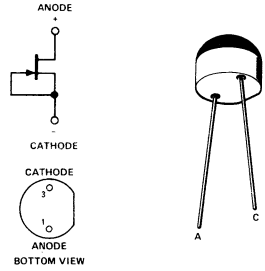
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

Performance Curves NCL
See Section 4

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources
  No Power Supplies Required
- Good Operating Current Tolerance
  ±20%

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation (25°C Free Air Temperature)	350 mW
Power Derating (to +125°C)	3.5 mW/°C
Storage Temperature Range	−55 to +125°C
Operating Temperature Range	−55 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

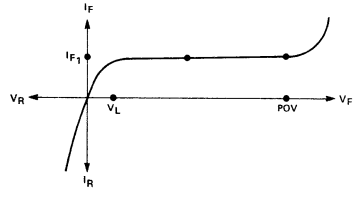
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			E500	E501	E502	E503	E504	E505	E506	E507	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	192	264	344	448	600	800	1120	1440	μA	V_F = 25 V
2				Nominal	240	330	430	560	750	1000	1400	1800		
3				Max	288	396	516	672	900	1200	1680	2160		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	50	50	V	I_F = 1.1 $I_{FI(Max)}$
5		V_L	Limiting Voltage (Note 3)	Max	1.2	1.3	1.5	1.7	1.9	2.1	2.5	2.8		I_F = 0.9 $I_{FI(Min)}$
6				Typ	0.8	0.9	1.1	1.2	1.4	1.5	1.8	2.0		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	5.0	3.0	2.0	1.4	1.0	0.6	0.4	0.25	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	8.0	6.0	4.4	3.4	2.5	1.9	1.4	1.0		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NOTES:
1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

NCL

Current-Limiter Diode
V-I Characteristic



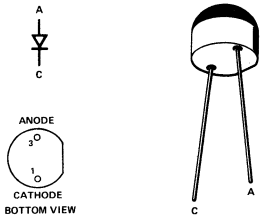
low-leakage pico-amp diodes *designed for . . .*

- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

BENEFITS

- Low Cost

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS

Forward Current . . . . . 10 mA
Total Device Dissipation . . . . . 250 mW
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic			Min	Typ	Max	Unit	Test Conditions
1	STATIC	I_R	Reverse Current (Note 1)	EPAD50			−50	pA	V_R = −20 V
2				EPAD100			−100		
3				EPAD200			−200		
4				EPAD500			−500		
5		BV_R	Breakdown Voltage (Reverse)		−35	−80		V	I_R = −1 μA
6		V_F	Forward Voltage Drop			0.8	1.5	V	I_F = 5 mA
7	DYN	C_R	Capacitance			1.5	2.0	pF	V_R = −5 V, f = 1 MHz

NOTE:
1. The EPAD type number denotes its maximum reverse current value in pico amps. Devices with I_R values intermediate to those shown are also available on request.

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

Performance Curves NIP See Section 4

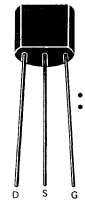
BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $R_{DS(on)} < 8\ \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r = 5$ ns Typical
- Low Noise
  $\overline{e_n} = 6\ nV/\sqrt{Hz}$ at 10 Hz, Typ (J110)

ABSOLUTE MAXIMUM RATINGS (@ 25°C)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current (FWD)	50 mA
Total Device Dissipation (T_{LEAD} = 25°C)	625 mW
Power Derating (to +135°C)	5.68 mW/°C
Storage Temperature Range	−55°C to +135°C
Operating Temperature Range	−55°C to +135°C
Lead Temperature (1/16" from case for 10 seconds)	+260°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	J108 Min	J108 Typ	J108 Max	J109 Min	J109 Typ	J109 Max	J110 Min	J110 Typ	J110 Max	Unit	Test Conditions
1		I_{GSS} Gate Reverse Current (Note 1)			−3			−3			−3	nA	V_{DS} = 0 V, V_{GS} = −15 V
2	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	−3		−10	−2		−6	−0.5		−4	V	V_{DS} = 5 V, I_D = 1 μA
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	−25			−25			−25			V	V_{DS} = 0 V, I_G = −1 μA
4	STATIC	I_{DSS} Drain Saturation Current (Note 2)	80			40			10			mA	V_{DS} = 15 V, V_{GS} = 0 V
5	STATIC	$I_{D(off)}$ Drain Cutoff Current (Note 1)			−3			−3			−3	nA	V_{DS} = −5 V, V_{GS} = −10 V
6		$r_{DS(on)}$ Drain-Source ON Resistance			8			12			18	Ω	V_{DS} ≤ 0.1 V, V_{GS} = 0 V
7		$C_{dg(off)}$ Drain-Gate OFF Capacitance			15			15			15	pF	V_{DS} = 0 V, V_{GS} = −10 V; f = 1 MHz
8		$C_{sg(off)}$ Source-Gate OFF Capacitance			15			15			15	pF	V_{DS} = 0 V, V_{GS} = −10 V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance			85			85			85	pF	V_{DS} = V_{GS} = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$ Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions
11	DYNAMIC	t_r Rise Time		1			1			1		ns	V_{DD} 1.5 V / 1.5 V / 1.5 V
12	DYNAMIC	$t_{d(off)}$ Turn OFF Delay Time		6			6			6		ns	$V_{GS(off)}$ −12 V / −7 V / −5 V
13	DYNAMIC	t_f Fall Time		30			30			30		ns	R_L 150 Ω / 150 Ω / 150 Ω

NIP

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

n-channel FETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 4

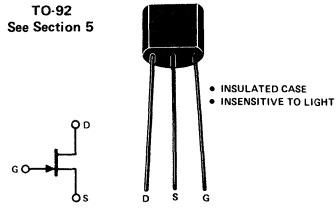
BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (@ 25°C)

Gate-Drain or Gate-Source Voltage . . . . . −35 V
Gate Current . . . . . 50 mA
Total Device Dissipation (T_{LEAD} = 25°C) . . . . . 625 mW
Power Derating (to +135°C) . . . . . 5.68 mW/°C
Storage Temperature Range . . . . . −55°C to +135°C
Operating Temperature Range . . . . . −55°C to +135°C
Lead Temperature (1/16" from case for 10 seconds) . . . . . +300°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111			J112			J113			UNIT	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1		I_{GSS}	Gate Reverse Current (Note 1)			1			1			1	nA	V_{DS} = 0 V, V_{GS} = 15 V	
2	STATIC	$V_{GS(off)}$	Gate Source Cutoff Voltage	3		10	1		5	0.5		3	V	V_{DS} = 5 V, I_D = 1 μA	
3		BV_{GSS}	Gate Source Breakdown Voltage	35			35			35				V_{DS} = 0 V, I_G = 1 μA	
4		I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	V_{DS} = 15 V, V_{GS} = 0 V	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			1			1			1	nA	V_{DS} = 5 V, V_{GS} = 10 V	
6		$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	V_{DS} = 0.1 V, V_{GS} = 0 V	
7		$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0 V, V_{GS} = 10 V	f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5			
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28		V_{DS} = V_{GS} = 0	
10		$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions	
11		t_r	Rise Time		6			6			6				J111 J112 J113
12		$t_{d(off)}$	Turn Off Delay Time		20			20			20			V_{DD}	10 V 10 V 10 V
13		t_f	Fall Time		15			15			15			$V_{GS(off)}$	−12 V −7 V −5 V
														R_L	800 Ω 1,600 Ω 3,200 Ω

NC

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

p-channel JFETs *designed for . . .*

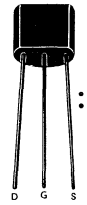
- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 4

BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when when Combined with J113, its N-Chan-Channel Complement
- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)} < 5.5$ pF
  $C_{dg(off)} < 5.5$ pF
- Fast Switching
  $t_{d(on)} + t_r = 7$ ns Typical

TO-92
See Section 5



- INSULATED CASE
- INSENSITIVE TO LIGHT

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics	J174 Min	J174 Typ	J174 Max	J175 Min	J175 Typ	J175 Max	J176 Min	J176 Typ	J176 Max	J177 Min	J177 Typ	J177 Max	Unit	Test Conditions
1		I_{GSS} Gate Reverse Current (Note 2)			1			1			1			1	nA	$V_{DS} = 0$, $V_{GS} = 20$ V
2	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	$V_{DS} = -15$ V, $I_D = -10$ nA
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	30			30			30			30			V	$V_{DS} = 0$, $I_G = 1\ \mu$A
4	STATIC	I_{DSS} Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	$V_{DS} = -15$ V, $V_{GS} = 0$
5	STATIC	$I_{D(off)}$ Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	$V_{DS} = -15$ V, $V_{GS} = 10$ V
6	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance			85			125			250			300	Ω	$V_{GS} = 0$, $V_{DS} = -0.1$ V
7	DYNAMIC	$C_{dg(off)}$ Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	$V_{DS} = 0$, $V_{GS} = 10$ V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$ Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	$V_{DS} = 0$, $V_{GS} = 10$ V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance		40			40			40			40		pF	$V_{DS} = V_{GS} = 0$; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$ Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions
11	DYNAMIC	t_r Rise Time		5			10			20			25		ns	
12	DYNAMIC	$t_{d(off)}$ Turn Off Delay Time		5			10			15			20		ns	
13	DYNAMIC	t_f Fall Time		10			20			20			25		ns	

Switching Time Test Conditions	J174	J175	J176	J177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A. **PS**
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.

p-channel JFETs *designed for . . .*

■ General Purpose Amplifiers

Performance Curves PS See Section 4

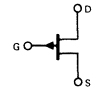
BENEFITS

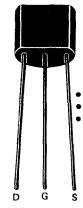
- Low Cost
- Automatic Insertion Package
- High Gain Amplifiers
  g_{fs} = 14,000 μmho Typical (J271)
- Low Noise
  $\overline{e_n}$ = 6 nV/$\sqrt{Hz}$ at 1 kHz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . -50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 5





- INSULATED CASE
- INSENSITIVE TO LIGHT
- DRAIN AND SOURCE CAN BE INTERCHANGED

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J270			J271			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V_{DS} = -15 V, I_D = -1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			V	V_{DS} = 0, I_G = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-2		-15	-6		-50	mA	V_{DS} = -15 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = -15 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	μmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			200			500	μmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		20			20		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		5			5		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	e_n	Equivalent Short-Circuit Input Noise Voltage		6			6		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = -10 V, I_D = $I_{DSS(min)}$	f = 1 kHz

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

PS

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA
See Section 4

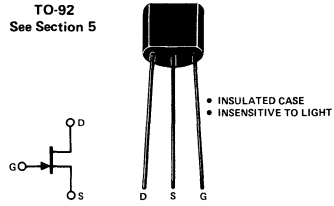
BENEFITS

- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation (T_{LEAD} = 25°C) . . . . 625 mW
Derate above 25°C . . . . . 5.68 mW/°C
Storage Temperature Range . . . . . -55 to +150°C
Operating Junction Temperature Range . . . -55 to +135°C

TO-92
See Section 5



- INSULATED CASE
- INSENSITIVE TO LIGHT

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J308			J309			J310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 μA, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current			-1.0			-1.0			-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
3	STATIC	I_{GSS}	Gate Reverse Current			-1.0			-1.0			-1.0	μA	V_{GS} = -15 V, V_{DS} = 0	T = +125°C
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.5	-1.0		-4.0	-2.0		-6.5	V	V_{DS} = 10 V, I_D = 1 nA	
5	STATIC	I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6	STATIC	$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	V_{DS} = 0, I_G = 1 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8	DYNAMIC	g_{os}	Common-Source Output Conductance			200			150			200	μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
9	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000		μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
10	DYNAMIC	g_{og}	Common-Gate Output Conductance		150			100			150		μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
11	DYNAMIC	C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
12	DYNAMIC	C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
15	HI FREQ	$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
16	HI FREQ	$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
17	HI FREQ	$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
18	HI FREQ	G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
19	HI FREQ	NF	Noise Figure		1.5			1.5			1.5		dB	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
20	HI FREQ	G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11		dB	V_{DS} = 10 V, I_D = 10 mA	f = 450 MHz
21	HI FREQ	NF	Noise Figure		2.7			2.7			2.7		dB	V_{DS} = 10 V, I_D = 10 mA	f = 450 MHz

NOTE:
1. Pulse test PW 300 μs, duty cycle ≤ 3%.

NZA

monolithic dual n-channel JFETs *designed for . . .*

- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NNR See Section 4

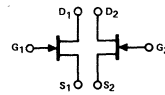
BENEFITS

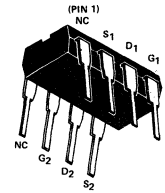
- Low Cost, Automated Insertion Package
- Minimum System Error and Calibration
  - 5 mV Offset Maximum (J401)
  - 95 dB Minimum CMRR (J401-04)
- Low Drift with Temperature
  - 10 μV/°C Maximum (J401, 02)
- Operates from Low Power Supply Voltages
  - $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  - Output Conductance < 2 μmho
- Low Noise
  - $\overline{e_n}$ = 6 nV/√Hz at 10 Hz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side) @ T_A = 85°C derate 7.5 mW/°C	300 mW
Total Device Dissipation @ T_A = 85°C derate 11 mW/°C	500 mW
Storage Temperature Range	−55 to +150°C

8-Pin Mini DIP
See Section 5





ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

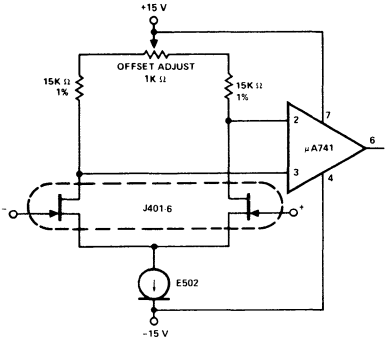
		Characteristic		J401 Min	J401 Max	J402 Min	J402 Max	J403 Min	J403 Max	J404 Min	J404 Max	J405 Min	J405 Max	J406 Min	J406 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		−100		−100		−100		−100		−100		−100	pA	V_{DS} = 0, V_{GS} = −30 V	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4		V_{GS}	Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3		V_{DG} = 15 V, I_D = 200 μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G	Gate Current (Note 1)		−100		−100		−100		−100		−100		−100	pA	V_{DG} = 15 V,	
7					−60		−60		−60		−60		−60		−60	nA	I_D = 200 μA	T_A = 125°C
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
11		g_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		V_{DG} = 15 V, I_D = 200 μA	
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		$\overline{e_N}$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55°, T_B = +25°, T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

NNR

APPLICATIONS

Inexpensive All-Epoxy
General Purpose FET Input Op Amp



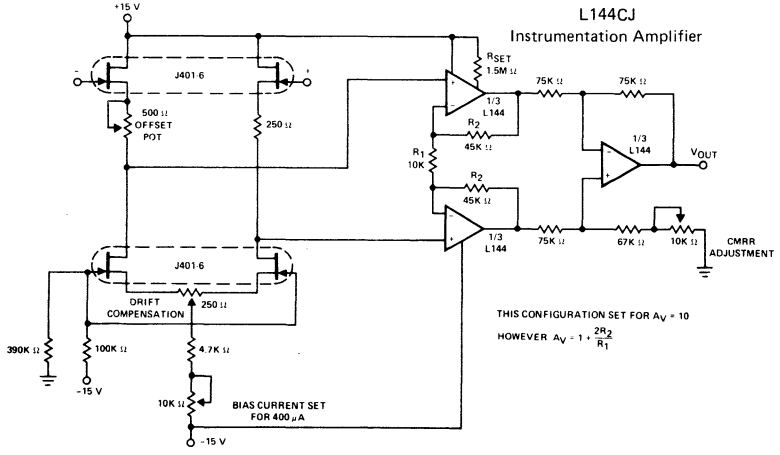
For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

FET Input Instrumentation Amplifier

L144CJ
Instrumentation Amplifier



monolithic dual n-channel JFETs *designed for . . .*

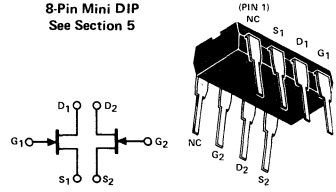
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NQP
See Section 4

BENEFITS

- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (J410)
  70 dB Minimum CMRR (J410)
- Low Drift with Temperature
  10 μV/°C Maximum (J410)
- Simplifies Amplifier Design
  Low Output Conductance
- Automatic Insertion Package

8-Pin Mini DIP
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage ..... ±40 V
Gate-Drain or Gate-Source Voltage ..... −40 V
Gate Current ..... 50 mA
Total Package Dissipation (25°C Free-Air) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... −55 to +125°C
Operating Temperature Range ..... −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) ... 260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J410 Min	J410 Typ	J410 Max	J411 Min	J411 Typ	J411 Max	J412 Min	J412 Typ	J412 Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current (Note 1)			−250			−250			−250	pA	V_{DS} = 0 V_{GS} = −30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−3.5	−0.5		−3.5	−0.5		−3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40			−40			−40				V_{DS} = 0 I_G = −1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	0.5		6.0	0.5		6.0	0.5		6.0	mA	V_{DS} = 20 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)			−250			−250			−250	pA	V_{DG} = 20 V, I_D = 200 μA	
6		V_{GS}	Gate-Source Voltage	−0.2		−3.0	−0.2		−3.0	−0.2		−3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4 000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8				600		1,200	600		1,200	600		1,200		V_{DG} = 20 V, I_D = 200 μA	
9		g_{os}	Common-Source Output Conductance			20			20			20		V_{DS} = 20 V, V_{GS} = 0	
10						5			5			5		V_{DS} = 20 V, I_D = 200 μA	
11		C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2				
13		$\bar{e}_N$	Equivalent Short-Circuit Input Noise Voltage		13	50		13	50		13	50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			25			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16		CMRR	Common-Mode Rejection Ratio (Note 4)	70	80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP

monolithic dual n-channel JFETs *designed for . . .*

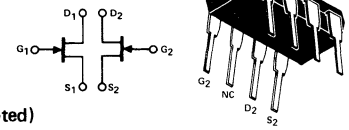
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NNR See Section 4

BENEFITS

- Low Cost
- Automatic Insertion Package
- Symmetrical Pin-Out Allows Socket Insertion in Either Direction
- Minimum System Error and Calibration
  5 mV Offset Maximum (J1401)
  95 dB Minimum CMRR (J1401–4)
- Operates from Low Power Supply Voltages
  $V_{GS(off)} < 2.5V$
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  e_n = 6 nV/√Hz at 10 Hz Typical

8-Pin Mini DIP
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 50 V
Forward Gate Current . . . . . 10 mA
Device Dissipation (each side)
@ T_A = 85°C derate 7.5 mW/°C . . . . . 300 mW
Total Device Dissipation
@ T_A = 85°C derate 11 mW/°C . . . . . 500 mW
Storage Temperature Range . . . . . −55 to +150°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		Characteristic	J1401 Min	J1401 Max	J1402 Min	J1402 Max	J1403 Min	J1403 Max	J1404 Min	J1404 Max	J1405 Min	J1405 Max	J1406 Min	J1406 Max	Unit	Test Conditions
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA
2		I_{GSS} Gate Reverse Current (Note 1)		−100		−100		−100		−100		−100		−100	pA	V_{DS} = 0, V_{GS} = −30 V
3		$V_{GS(off)}$ Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA
4		V_{GS} Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3		V_{DG} = 15 V, I_D = 200 μA
5		I_{DSS} Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0
6		I_G Gate Current (Note 1)		−100		−100		−100		−100		−100		−100	pA	V_{DG} = 15 V,
7				−60		−60		−60		−60		−60		−60	nA	I_D = 200 μA; T_A = 125°C
8		BV_{G1-G2} Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0; f = 1 kHz
10		g_{os} Common-Source Output Conductance		20		20		20		20		20		20		
11		g_{fs} Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		V_{DG} = 15 V, I_D = 200 μA; f = 1 kHz
12		g_{os} Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0		
13		C_{iss} Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0		
15		$\bar{e}_N$ Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0; f = 10 Hz
16	MATCHING	CMRR Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA
17		$\lvert V_{GS1} - V_{GS2}\rvert$ Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA
18		$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$ Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA; T_A = −55° T_B = +25° T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta V_{GS1}-V_{GS2}}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

NNR

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NC
See Section 4

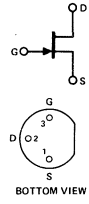
BENEFITS

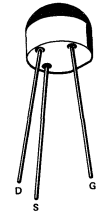
- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Forward Gate Current . . . . . 50 mA
Total Device Dissipation at (or Below) T_A = 25°C
(Derate 3.5 mW/°C to +125°C) . . . . . 350 mW
Storage Temperature Range . . . . . –55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-106
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	KE4391 Min	KE4391 Max	KE4392 Min	KE4392 Max	KE4393 Min	KE4393 Max	Unit	Test Conditions	
1		I_{GSS} Gate Reverse Current		–1.0		–1.0		–1.0	nA	V_{GS} = –20 V, V_{DS} = 0	
2				–200		–200		–200			100°C
3		BV_{GSS} Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 μA, V_{DS} = 0	
4		$I_{D(off)}$ Drain Cutoff Current						1.0	nA	V_{DS} = 20 V	V_{GS} = –5 V
5								200			100°C
6	STATIC					1.0					V_{GS} = –7 V
7						200					100°C
8				1.0							V_{GS} = –12 V
9				200							100°C
10		$V_{GS(f)}$ Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0	
11		$V_{GS(off)}$ Gate-Source Cutoff Voltage	–4	–10	–2	–5	–0.5	–3		V_{DS} = 20 V, I_D = 1 nA	
12		I_{DSS} Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0	
13		$V_{DS(on)}$ Drain-Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA
14						0.4					I_D = 6 mA
15				0.4							I_D = 12 mA
16		$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA	
17		$r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, V_{DS} = 0	f = 1 kHz
18		C_{iss} Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0	
19	DYN	C_{rss} Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = –5 V
20						3.5					V_{GS} = –7V
21				3.5							V_{GS} = –12 V
22		$t_{d(on)}$ Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0	
23	SW	t_r Rise Time		5		5		5		$I_{D(on)}$ / $V_{GS(off)}$ / R_L	
24		$t_{d(off)}$ Turn-OFF Delay Time		20		35		50		KE4391: 12 mA / –12 V / 800 Ω	
25		t_f Fall Time		15		20		30		KE4392: 6 / –7 / 1.6K; KE4393: 3 / –5 / 3.2K	

NC

NOTE:
1. Pulse test required, pulse width ≈ 300 μs, duty cycle ≤ 3%.

n-channel JFET
designed for . . .

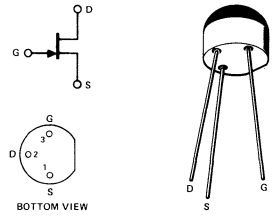
- **VHF Amplifiers**
- **Mixers**

Performance Curves NH
See Section 4

BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Bandwidth
- Low Cost

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −30 V
Forward Gate Current . . . . . 10 mA
Total Continuous Device Dissipation
at (or Below) T_A = 25°C
(Derate 3.5 mW/°C to 125°C) . . . . . 350 mW
Storage Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STA	I_{GSS}	Gate Reverse Current		−1.0	nA	V_{GS} = −15 V, V_{DS} = 0	
2	STA	BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = −1 μA, V_{DS} = 0	
3	STA	$V_{GS(off)}$	Gate-Source Cutoff Voltage		−6	V	V_{DS} = 15 V, I_D = 1 nA	
4	STA	I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYN	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6	DYN	g_{os}	Common-Source Output Conductance		50	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
8	DYN	C_{iss}	Common-Source Input Capacitance		4	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
9	DYN	C_{oss}	Common-Source Output Capacitance		2	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz

		Characteristic		100 MHz		400 MHz		Unit	Test Conditions	
				Min	Max	Min	Max			
10	HI FREQ	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0	
11	HI FREQ	b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	V_{DS} = 15 V, V_{GS} = 0	
12	HI FREQ	g_{oss}	Common-Source Output Conductance		75		100	μmho	V_{DS} = 15 V, V_{GS} = 0	
13	HI FREQ	b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	V_{DS} = 15 V, V_{GS} = 0	
14	HI FREQ	g_{fs}	Common-Source Forward Transconductance (Note 1)			4000		μmho	V_{DS} = 15 V, V_{GS} = 0	
15	HI FREQ	G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA	
16	HI FREQ	NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA	R_G = 1K Ω

NOTE:
1. Pulse test duration = 300 μs.

NH

3

depletion-type n-channel MOSFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke Detectors**
  - **pH Meters**
- **Low-Level Chopper Amplifiers**

Performance Curves MA See Section 4

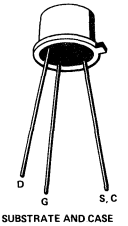
BENEFITS

- Insignificant Loading in High Impedance Circuits
  $R_{IN} > 10^{15}\ \Omega$
- Minimum Error in Low-Level Choppers
  $r_{DS(on)} < 100\ \Omega$ (M101)
- Good Off-Isolation as a Switch
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . 20 V
Gate-to-Channel Voltage (Note 1) . . . . . ±60 V
Drain Current . . . . . 20 mA
Total Device Dissipation at (or below)
25°C Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Operating Junction Temperature. . . . . -55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .255°C

TO-18
See Section 5



SUBSTRATE AND CASE INTERNALLY CONNECTED TO SOURCE PIN.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		M100 Min	M100 Typ	M100 Max	M101 Min	M101 Typ	M101 Max	Unit	Test Conditions	
1	STATIC	BV_{DSX}	Drain-Source Breakdown Voltage	20			20			V	I_D = 1 μA, V_{GS} = -10 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage			-5			-8		V_{DS} = 10 V, I_D = 1 μA	
3		I_{DSS}	Saturation Drain Current	1.5		4.5	4.0		12.0	mA	V_{DS} = 10 V, V_{GS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current			1			1	nA	V_{DS} = 5 V, V_{GS} = -10 V	
5		r_{GS}	Common-Source Parallel Input Resistance	10^{13}	10^{16}		10^{13}	10^{16}		Ω	V_{GS} = 30 V, V_{DS} = 0	
6		$r_{DS(on)}$	Drain-Source ON Resistance		350			300			V_{GS} = 0, V_{DS} = 0	
7					150			100			V_{GS} = 10 V, V_{DS} = 0	
8	DYN	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,500		5,000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		3.0	7.5		3.0	7.5	pF		f = 140 kHz

MA

NOTES:

1. Permanent damage may result if voltages greater than ±60 V are applied to the gate.
2. Derate linearly to 150°C free-air temperature at rate of 2.4 mW/°C.

enhancement-type p-channel MOSFET *designed for . . .*

- **Analog Switches**
- **Digital Switching**

Performance Curves MB See Section 4

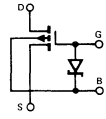
BENEFITS

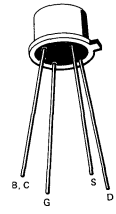
- High Off-Isolation
  $I_{D(off)} < 200$ pA
  $I_{S(off)} < 200$ pA
- Low Insertion Loss
  $r_{DS(on)} < 100\ \Omega$
- Rugged
  Zener Diode Input Protection

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	-30 V
Gate-to-Source Voltage	-30 V
Gate-to-Drain Voltage	-30 V
Drain Current	-50 mA
Gate Current (Forward Direction for Zener Clamp)	+0.1 mA
Storage Temperature	-65 to +150°C
Operating Junction Temperature	-55 to +125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = V_{BS} = 0	
2		BV_{GBS}	Gate- Body Breakdown Voltage	-30	-90	V	I_G = -10 μA, V_{SB} = V_{DB} = 0	
3		BV_{SDS}	Source-Drain Breakdown Voltage	-30			I_S = -1 μA, V_{DG} = V_{BD} = 0	
4		BV_{DSS}	Drain-Source Breakdown Voltage	-30			I_D = -1 μA, V_{GS} = V_{BS} = 0	
5		$V_{GS(th)}$	Gate Threshold Voltage	-2.5	-5.5		V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
6		$I_{S(off)}$	Source Cutoff Current		-200	pA	V_{SD} = -20 V, V_{GD} = V_{BD} = 0	
7		$I_{D(off)}$	Drain Cutoff Current		-200		V_{DS} = -20 V, V_{GS} = V_{BS} = 0	
8		$r_{DS(on)}$	Drain Source ON Resistance		130	Ω	V_{GS} = -15 V, I_D = -100 μA, V_{BS} = 0	
9					100		V_{GS} = -20 V, I_D = -100 μA, V_{BS} = 0	
10	DYNAMIC	C_{gs}	Gate-Source Capacitance		4	pF	V_{GB} = V_{DB} = V_{SB} = 0 Body Guarded	f = 1 MHz
11		C_{gd}	Gate-Drain Capacitance		4			
12		C_{sb}	Source-Body Capacitance		5		V_{GB} = 0, V_{DB} = V_{SB} = -5 V	
13		C_{db}	Drain-Body Capacitance		4			
14		C_{ds}	Drain-Source Capacitance		0.5		V_{GB} = 0, V_{DB} = V_{SB} = -5 V, Body Guarded	

MB

M104

enhancement-type p-channel MOSFET *designed for . . .*

- **Analog Switches**
- **Digital Switching**

Performance Curves MT
See Section 4

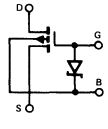
BENEFITS

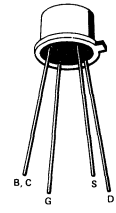
- High Off-Isolation
  $I_{D(off)} < 100$ pA
  $I_{S(off)} < 100$ pA
- Very High Input Impedance
  $C_{gs} < 0.5$ pF
  $I_{GSS} < 100$ pA
- Rugged
  Zener Protected Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . -30 V
Gate-to-Source Voltage . . . . . -30 V
Gate-to-Drain Voltage . . . . . -30 V
Drain Current . . . . . -50 mA
Gate Current (Forward Direction for Zener Clamp) +0.1 mA
Operating Junction Temperature . . . . . −55 to +125°C
Total Device Dissipation
(Derate 2.25 mW/°C to 125°C) . . . . . 225 mW
Storage Temperature . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .260°C

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Unit Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30			V	I_D = -1 μA, V_{GS} = V_{BS} = 0	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-30				I_S = -1 μA, V_{GD} = V_{BD} = 0	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-30		-90		I_G = -10 μA, V_{SB} = V_{BD} = 0	
4		I_{GSS}	Gate-Body Leakage			−100	pA	V_{GS} = -20 V, V_{DS} = V_{BS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current			−100		V_{DS} = -20 V, V_{GS} = V_{BS} = 0	
6		$I_{S(off)}$	Source Cutoff Current			−100		V_{SD} = -20 V, V_{GD} = V_{BD} = 0	
7		$V_{GS(th)}$	Gate Threshold Voltage	-3		-6	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
8		$r_{DS(on)}$	Drain Source ON Resistance			1,200	Ω	V_{GS} = -20 V, I_D = -100 μA, V_{BS} = 0	
9						2,500		V_{GS} = -10 V, I_D = -10 μA, V_{BS} = 0	
10	DYN	C_{gs}	Gate-Source Capacitance			0.5	pF	V_{GB} = V_{DB} = V_{SB} = 0 Body Guarded	f = 1 MHz
11		C_{gd}	Gate-Drain Capacitance			0.5			
12		C_{sb}	Source-Body Capacitance			1.7		V_{GB} = 0, V_{SB} = -5 V	
13		C_{db}	Drain-Body Capacitance			1.7			
14		C_{ds}	Drain-Source Capacitance		0.1			V_{GB} = 0, V_{DB} = V_{SB} = -5 V Body Guarded	

MT

dual enhancement-type p-channel MOSFETs *designed for . . .*

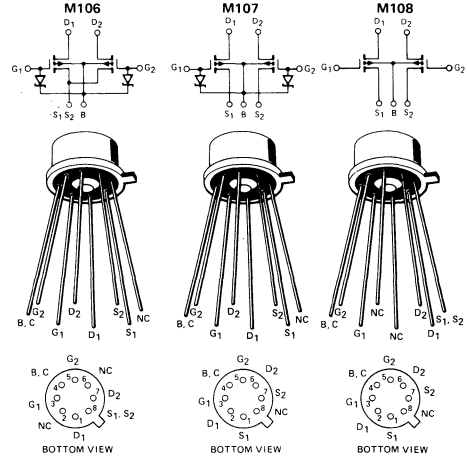
- **Analog Switches**
- **Differential Amplifiers**
- **Impedance Converters**

Performance Curves MACA MACB MACC See Section 4

BENEFITS

- High Input Impedance at High Temperature
  I_{GSS} = 30 pA Typical, T = 125°C (M108)
- High Off-Isolation
  $I_{D(off)}$ = 200 pA Maximum

TO-99
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . -30 V
Gate-to-Source Voltage (M106/7) . . . . . -30 V
Gate-to-Source Voltage (M108) . . . . . -50 V
Gate-to-Drain Voltage (M106/7) . . . . . -30 V
Gate-to-Drain Voltage (M108) . . . . . -50 V
Drain Current . . . . . -50 mA
Gate Zener Current . . . . . ±1.0 mA
Storage Temperature . . . . . -65 to 150°C
Operating Junction Temperature. . . -55 to 125°C
Total Dissipation at 25°C Ambient Temperature (Derate 5 mW/°C to 125°C) . . . . . 500 mW
Lead Temperature (1/16" from case for 10 seconds) . . . . . 260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		M106, M107		M108		Unit	Test Conditions
				Min	Max	Min	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30		-30		V	I_D = -1 μA, V_{GS} = V_{BS} = 0
2		BV_{SDS}	Source-Drain Breakdown Voltage	-30		-30			I_S = -1 μA, V_{GD} = V_{BD} = 0
3		BV_{GBS}	Gate-Body Breakdown Voltage	-30		±100*			I_G = -10 μA, V_{SB} = V_{DB} = 0
4		I_{GSS}	Gate-Body Leakage		-100		-1	pA	V_{GS} = -20 V, V_{DS} = V_{BS} = 0
5		$I_{D(off)}$	Drain Cutoff Current		-200		-200		V_{DS} = -20 V, V_{GS} = V_{BS} = 0
6		$I_{S(off)}$	Source Cutoff Current		-200		-200		V_{SD} = -20 V, V_{GD} = V_{BD} = 0
7		$V_{GS(th)}$	Gate Threshold Voltage	-2	-6	-2	-8	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0
8		$I_{D(on)}$	Drain Current	-10		-10		mA	V_{DS} = -10 V, V_{GS} = -10 V, V_{BS} = 0
9		$r_{DS(on)}$	Drain Source ON Resistance		150		150	Ω	V_{GS} = -15 V, I_D = -100 μA, V_{BS} = 0
10					120		120		V_{GS} = -20 V, I_D = -100 μA, V_{BS} = 0
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000		2,000		μmho	V_{DS} = -10 V, V_{GS} = -10 V, V_{BS} = 0 f = 1 kHz
12		C_{gs}	Gate-Source Capacitance		4		4	pF	V_{GB} = V_{DB} = 0, f = 1 MHz, Body Guarded
13		C_{gd}	Gate-Drain Capacitance		4		4		
14		C_{sb}	Source-Body Capacitance		5.5		5.5		V_{GB} = 0, V_{DB} = V_{SB} = -5 V, f = 1 MHz
15		C_{db}	Drain-Body Capacitance		5.5		5.5		
16		C_{ds}	Drain-Source Capacitance		0.5		0.5		V_{GB} = 0, V_{DB} = V_{SB} = -5 V, f = 1 MHz, Body Guarded
*Gate-Oxide Breakdown Voltage				MACA	MACB	MACC			

M113

enhancement-type p-channel MOSFET *designed for . . .*

- **Analog Switches**
- **Digital Switching**

Performance Curves MBL See Section 4

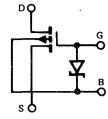
BENEFITS

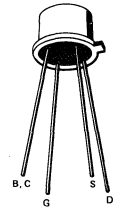
- High Off-Isolation
  $I_{D(off)} < 200$ pA
  $I_{S(off)} < 200$ pA
- Rugged
  Zener Diode Input Protection

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	-30 V
Gate-to-Source Voltage	-30 V
Gate-to-Drain Voltage	-30 V
Drain Current	-50 mA
Gate Current (Forward Direction for Zener Clamp)	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	-55 to 125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30		V	$I_D = -1\ \mu A$, $V_{GS} = V_{BS} = 0$	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-30			$I_S = -1\ \mu A$, $V_{GD} = V_{BD} = 0$	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-30	-90		$I_G = -10\ \mu A$, $V_{SB} = V_{DB} = 0$	
4		I_{GSS}	Gate-Body Leakage		-100	pA	$V_{GS} = -20$ V, $V_{DS} = V_{BS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current		-200		$V_{DS} = -20$ V, $V_{GS} = V_{BS} = 0$	
6		$I_{S(off)}$	Source Cutoff Current		-200		$V_{SD} = -20$ V, $V_{GD} = V_{BD} = 0$	
7		$V_{GS(th)}$	Gate Threshold Voltage	-1	-3	V	$V_{GS} = V_{DS}$, $I_D = -10\ \mu A$, $V_{BS} = 0$	
8		$r_{DS(on)}$	Drain Source ON Resistance		400	Ω	$V_{GS} = -5$ V, $I_D = -100\ \mu A$, $V_{BS} = 0$	
9					200		$V_{GS} = -10$ V, $I_D = -100\ \mu A$, $V_{BS} = 0$	
10	DYN	C_{gs}	Gate-Source Capacitance		4	pF	$V_{GB} = V_{DB} = V_{SB} = 0$ Body Guarded	f = 1 MHz
11		C_{gd}	Gate-Drain Capacitance		4			
12		C_{sb}	Source-Body Capacitance		5		$V_{GB} = 0$, $V_{DB} = V_{SB} = -5$ V	
13		C_{db}	Drain-Body Capacitance		5			
14		C_{ds}	Drain-Source Capacitance		0.3		$V_{GB} = 0$, $V_{DB} = V_{SB} = -5$ V Body Guarded	

MBL

enhancement-type p-channel MOSFET *designed for . . .*

- **General Purpose Amplifiers**
- **Analog Switches**
- **Digital Switching**

Performance Curves MBH
See Section 4

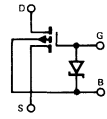
BENEFITS

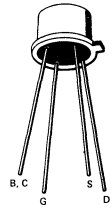
- High Gain
  g_{fs} = 4000 μmho Typical
- High Input Impedance
  I_{GSS} = 6 pA Typical
- High Off-Isolation
  $I_{D(off)}$ = 15 pA Typical
- Rugged
  Zener Protected Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . -40 V
Gate-to-Source Voltage . . . . . -40 V
Gate-to-Drain Voltage . . . . . -40 V
Drain Current . . . . . -50 mA
Gate Zener Current . . . . . ±0.1 mA
Storage Temperature . . . . . -65 to +150°C
Operating Junction Temperature . . . . . -55 to +125°C
Total Dissipation at 25°C Ambient Temperature
(Derate 2.25 mW/°C) . . . . . 225 mW
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .260°C

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-40			V	I_D = -1 μA, V_{GS} = 0, V_{BS} = 0	
2		BV_{SDS}	Source-Drain Breakdown Voltage	-40				I_S = -1 μA, V_{GD} = 0, V_{BD} = 0	
3		BV_{GBS}	Gate-Body Breakdown Voltage	-40		-110		I_G = -1 μA, V_{SB} = 0, V_{DB} = 0	
4		I_{GSS}	Gate-Body Leakage		-6	-100	pA	V_{GS} = -20 V, V_{DS} = 0, V_{BS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current		-15	-200		V_{DS} = -20 V, V_{GS} = 0, V_{BS} = 0	
6		$I_{S(off)}$	Source Cutoff Current		-16	-200		V_{SD} = -20 V, V_{GD} = 0, V_{BD} = 0	
7		$V_{GS(th)}$	Gate Threshold Voltage	-1.5	-2.9	-4.5	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
8		$I_{D(on)}$	Drain Current	-8	-20	-35	mA	V_{DS} = -10 V, V_{GS} = -10 V, V_{BS} = 0	
9		$r_{DS(on)}$	Drain-Source ON Resistance		70	240	Ω	V_{GS} = -40 V, I_{DS} = -0.1 mA, V_{BS} = 0	
10					100	275		V_{GS} = -25 V, I_{DS} = -0.1 mA, V_{BS} = 15 V	
11					320	500		V_{GS} = -10 V, I_{DS} = -0.1 mA, V_{BS} = 30 V	
12		$V_{DS(on)}$	Drain- Source ON Voltage			900	mV	V_{GS} = -10 V, I_D = -2 mA, V_{BS} = 0	
13	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000	4,000		μmho	V_{DS} = -10 V, V_{GS} = -10 V, V_{BS} = 0	f = 1 kHz
14		C_{gs}	Gate-Source Capacitance		2	4	pF	V_{GB} = 0, V_{DB} = 0, V_{SB} = 0 Body Guarded	f = 1 MHz
15		C_{gd}	Gate-Drain Capacitance		1.5	4			
16		C_{sb}	Source-Body Capacitance		4	5		V_{GB} = 0, V_{DB} = -5 V, V_{SB} = -5 V	
17		C_{db}	Drain-Body Capacitance		2.5	4		V_{GB} = 0, V_{DB} = -5 V, V_{SB} = -5 V	
18		C_{ds}	Drain-Source Capacitance			0.3		V_{CB} = 0, V_{DB} = -5V, V_{SB} = -5V, Body Guarded	
19	SW	$t_{d(on)}$	Turn-ON Delay Time			12	ns	V_{DD} = -15 V	
20		t_r	Rise Time			24		$I_{D(on)}$ = -10 mA	
21		t_{off}	Turn-OFF Time			50		R_L = 1.5k Ω	

MBH

enhancement-type n-channel MOSFET *designed for . . .*

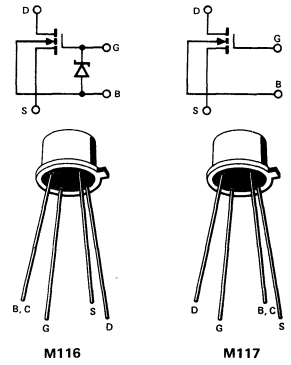
- **General Purpose Amplifiers**
- **Analog Switches**
- **Digital Switching**

Performance Curves
MBN MBNA See Section 4

BENEFITS

- High Input Impedance
  1 pA Maximum (M117)
- Low Insertion Loss
  $R_{DS(on)}$ = 100 Ω Maximum
- Rugged
  Zener Diode Input Protection

TO-72
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	30 V
Gate-to-Source Voltage M116	30 V
Gate-to-Source Voltage M117	±50 V
Gate-to-Drain Voltage M116	30 V
Gate-to-Drain Voltage M117	±50 V
Drain Current	50 mA
Gate Zener Current . . . M116	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	−55 to +125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		M116 Min	M116 Max	M117 Min	M117 Max	Unit	Test Condition	
1	STATIC	I_{GSS}	Gate-Body Leakage		100		1.0	pA	V_{GS} = 20 V, V_{DS} = V_{BS} = 0	
2		$V_{GS(th)}$	Gate Threshold Voltage	1	5	1	5	V	V_{GS} = V_{DS}, I_D = 10 μA, V_{BS} = 0	
3		BV_{DSS}	Drain-Source Breakdown Voltage	30		30			I_D = 1 μA, V_{GS} = V_{BS} = 0	
4		BV_{SDS}	Source-Drain Breakdown Voltage	30		30			I_S = 1 μA, V_{GD} = V_{BD} = 0	
5		BV_{GBS}	Gate-Body Breakdown Voltage	30	60	±100[1]			I_G = 10 μA, V_{SB} = V_{DB} = 0	
6		$I_{D(off)}$	Drain Cutoff Current		10		10	nA	V_{DS} = 20 V, V_{GS} = V_{BS} = 0	
7		$I_{S(off)}$	Source Cutoff Current		10		10		V_{SD} = 20 V, V_{GD} = V_{BD} = 0	
8		$I_{D(on)}$	ON Drain Current	2	20	2	20	mA	V_{GS} = V_{DS} = +10V, V_{BS} = 0	
9		$r_{DS(on)}$	Drain Source ON Resistance		100		100	Ω	V_{GS} = 20 V, I_D = 100 μA, V_{BS} = 0	
10					200		200		V_{GS} = 10 V, I_D = 100 μA, V_{BS} = 0	
11	DYN	C_{iss}	Input Capacitance		10		8	pF	V_{GB} = 0, V_{DB} = 10 V, V_{BS} = 0	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		2.5		2.5		V_{GB} = V_{DB} = 0 Body Guarded	
13		C_{gd}	Gate-Drain Capacitance		2.5		2.5			
14		C_{db}	Drain-Body Capacitance		7		7		V_{GB} = 0, V_{DB} = 10 V	
				MBN		MBNA				

NOTE:
1. Gate-oxide breakdown voltage. Permanent damage may result if voltages greater than ±100 are applied to the gate.

enhancement-type p-channel MOSFET *designed for . . .*

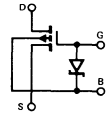
Performance Curves MKA
See Section 4

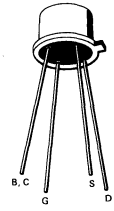
- **Audio Amplifiers**
- **Choppers**
- **Commutators**

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . -30 V
Gate-to-Source Voltage . . . . . -30 V
Gate-to-Drain Voltage . . . . . -30 V
Drain Current . . . . . -50 mA
Gate Current (Forward Direction for Zener Clamp) . ±0.1 mA
Storage Temperature . . . . . -65 to 150°C
Operating Junction Temperature . . . . . -55 to 125°C
Total Dissipation at 25°C Ambient Temperature
(Derate 2.25 mW/°C) . . . . . 225 mW
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .260°C

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Leakage Current			-1	nA	V_{GS} = -15 V, V_{DS} = V_{BS} = 0	
2	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-30			V	I_D = -10 μA, V_{GS} = V_{BS} = 0	
3	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	-3		-6	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
4	STATIC	$I_{D(off)}$	Drain Cutoff Current		-0.5	-10	nA	V_{DS} = -20 V, V_{GS} = V_{BS} = 0	
5	STATIC	$I_{D(on)}$	Drain Current	-3	-6		mA	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			300	Ω	V_{GS} = -15 V, I_D = -0.1 mA, V_{BS} = 0	
7	DYN	g_{fs}	Common Source Forward Transconductance	1,000			μmho	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 kHz
8	DYN	g_{fs}	Common Source Forward Transconductance	1,000			μmho	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 10 MHz
9	DYN	C_{gs}	Gate-Source Capacitance			3	pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz
10	DYN	C_{gd}	Gate-Drain Capacitance			2.5	pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz
11	DYN	C_{ds}	Drain-Source Capacitance		0.15		pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz

MKA

enhancement-type p-channel MOSFET *designed for . . .*

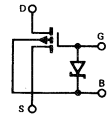
Performance Curves MB
See Section 4

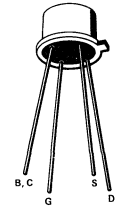
- **Audio Amplifiers**
- **Choppers**
- **Commutators**

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage . . . . . -25 V
Gate-to-Source Voltage . . . . . -25 V
Gate-to-Drain Voltage. . . . . -25 V
Drain Current . . . . . -50 mA
Gate Current (Forward Direction For Zener Clamp). .+0.1 mA
Storage Temperature . . . . . -65 to +150°C
Operating Junction Temperature Range. . . . . -55 to +125°C
Total Dissipation at 25°C Ambient Temperature
(Derate 2.25 mW/°C) . . . . . 225 mW
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .260°C

TO-72
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Leakage Current			-1	nA	V_{GS} = -15 V, V_{DS} = V_{BS} = 0	
2	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-25			V	I_D = -10 μA, V_{GS} = V_{BS} = 0	
3	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	-3		-6	V	V_{GS} = V_{DS}, I_D = -10 μA, V_{BS} = 0	
4	STATIC	$I_{D(off)}$	Drain Cutoff Current			-10	nA	V_{DS} = -20 V, V_{GS} = V_{BS} = 0	
5	STATIC	$I_{D(on)}$	Drain Current	-3			mA	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		150		Ω	V_{GS} = -15 V, I_D = -1 mA, V_{BS} = 0	
7	DYN	9_{fs}	Common-Source Forward Transconductance	1,000			μmho	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 kHz
8	DYN	9_{fs}	Common-Source Forward Transconductance	1,000			μmho	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 10 MHz
9	DYN	C_{gs}	Gate-Source Capacitance			4	pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz
10	DYN	C_{gd}	Gate-Drain Capacitance			4	pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz
11	DYN	C_{ds}	Drain-Source Capacitance		0.15		pF	V_{GS} = V_{DS} = -10 V, V_{BS} = 0	f = 1 MHz

MB

enhancement-type p-channel MOSFET *designed for . . .*

Performance Curves MRA See Section 4

- **High-Input Impedance Amplifiers**

  Smoke Detectors
  Electrometers
  pH Meters

BENEFITS

- High Input Impedance
  I_{GSS} = 30 Femto Amp Typical
- High Gain
  g_{fs} = 1000 μmho Minimum

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage . . . . . 25 V
Gate-Source Voltage . . . . . ±10 V
Drain Current . . . . . 30 mA
Total Device Dissipation at (Or Below) T_A = 25°C
(Derate 3 mW/°C to +150°C) . . . . . 375 mW
Operating Junction Temperature. . . . . −55 to +150°C
Storage Temperature. . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 265°C

TO-18
See Section 5

ELECTRICAL CHARACTERISTICS (25°C)

			Characteristic	Min	Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate-Source Leakage Current		−1.0	pA	V_{GS} = −10 V, V_{DS} = 0
2		BV_{DSS}	Drain-Source Breakdown Voltage	−25		V	I_D = −10 μA, V_{GS} = 0
3		V_{GS}	Gate-Source Voltage	−2.0	−6.0	V	V_{DS} = −10 V, I_D = −10 μA
4		I_{DSS}	Drain Cutoff Current		−20	nA	V_{DS} = −10 V, V_{GS} = 0
5		$I_{D(on)}$	ON Drain Current	−3.0		mA	V_{DS} = −10 V, V_{GS} = −10 V
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		μmhos	V_{DS} = −10 V, I_D = −2 mA, f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		6.0	pF	V_{DS} = −10 V, V_{GS} = −10 V, f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		

MRA

MPF102

n-channel JFET *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH
See Section 4

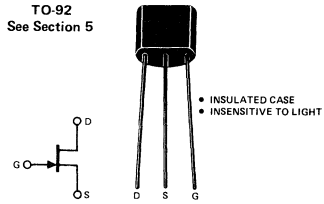
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation @ T_A = 25°C . . . . . 310 mW
Derate above 25°C . . . . . 2.82 mW/°C
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−2.0	nA	V_{GS} = −15 V, V_{DS} = 0	
2					−2.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	I_G = −10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−8.0		V_{DS} = 15 V, I_D = 2 nA	
5		I_{DSS}	Saturation Drain Current	2.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6		V_{GS}	Gate-Source Voltage	−0.5	−7.5	V	V_{DS} = 15 V, I_D = 200 μA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$Re_{(y_{fs})}$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re_{(y_{os})}$	Common-Source Output Conductance		200			
10		$Re_{(y_{is})}$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0			

NOTE:
1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

n-channel JFET
designed for . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

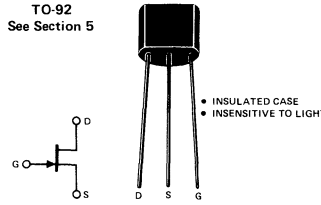
Performance Curves NH
See Section 4

BENEFITS
- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation @ T_A = 25°C . . . . . 310 mW
Derate above 25°C . . . . . 2.82 mW/°C
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−1.0	nA	V_{GS} = −15 V, V_{DS} = 0	
2					−1.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	I_G = −10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−8.0		V_{DS} = 15 V, I_D = 10 μA	
5		I_{DSS}	Saturation Drain Current	1.5	24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.5	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.5			
13		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
14					3.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 100 MHz

NOTE:
1. Pulse test, pulse width = 300 μs, duty cycle ≤ 3%.

NH

MPF109

n-channel JFET
designed for . . .

- **General Purpose Amplifiers**
- **Analog Switches**

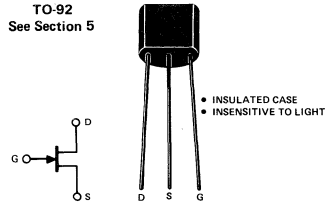
Performance Curves NRL See Section 4

BENEFITS
- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at T_A = 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	−65 to +135°C
Storage Temperature Range	−65 to +150°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.01	−1.0	nA	V_{GS} = −15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25	−60		V	I_G = −10 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.2		−8.0	V	V_{DS} = 15 V, I_D = 10 μA	
4	STATIC	I_{DSS}	Saturation Drain Current	0.5		24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	800		6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6	DYNAMIC	g_{os}	Common-Source Output Conductance		10	75	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5	7.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
8	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	NF	Noise Figure		0.04	2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

NOTE:
1. Pulse test PW ≤ 630 ms, duty cycle ≤ 10%.

NRL

n-channel JFET
designed for . . .

- **General Purpose Amplifiers**
- **Analog Switches**

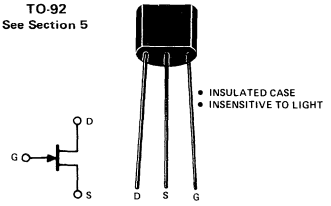
Performance Curves NRL
See Section 4

BENEFITS
- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage . . . . . 20 V
Drain-Gate Voltage . . . . . 20 V
Source-Gate Voltage . . . . . 20 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C . . . . . 310 mW
Derate above 25°C . . . . . 2.82 mW/°C
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		−.01	−100	nA	V_{GS} = −10 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−20			V	I_G = −10 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−10.0	V	V_{DS} = 10 V, I_D = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current	0.5		20	mA	V_{DS} = 10 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	500			μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6	DYNAMIC	g_{os}	Common-Source Output Conductance		10		μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5		pF	V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz
8	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		pF	V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz

NRL

NOTE:
1. Pulse test PW ≤ 630 msec, duty cycle ≤ 10%.

MPF112

n-channel JFET *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH See Section 4

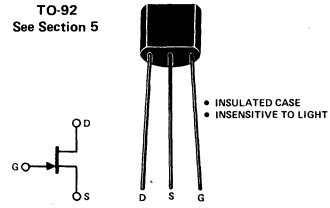
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C . . . . . 310 mW
Derate above 25°C . . . . . 2.82 mW/°C
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C

TO-92
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.01	−100	nA	V_{GS} = −10 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25			V	I_G = −10 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−10.0	V	V_{DS} = 10 V, I_D = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current	1		25	mA	V_{DS} = 10 V, V_{GS} = 0, (Note 1)	
5	STATIC	g_{fs}	Common-Source Forward Transconductance	1000		7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6	DYN	$Re_{(y_{fs})}$	Common-Source Forward Transconductance	800			μmho	V_{DS} = 10 V, V_{GS} = 0	f = 100 MHz
7	DYN	C_{iss}	Common-Source Input Capacitance		3.5		pF	V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz
8	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		0.8		pF	V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz

NH

NOTE:
1. Pulse test PW = 300 μs, duty cycle ≤ 3%.

monolithic dual n-channel JFETs *designed for . . .*

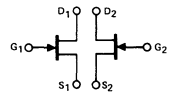
- **FET Input Amplifiers**
- **Low and Medium Frequency Differential Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

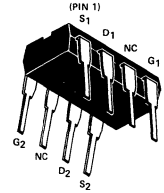
Performance Curves NQP
See Section 4

BENEFITS

- Low Cost
- Automatic Insertion Package
- Symmetrical Pin Out Allows Socket Insertion in Either Direction
- Isolated Gate Leads Minimize Stray Leakages
- Minimum System Error and Calibration
  5 mV Offset Maximum (NPD8301)
  CMRR 80 dB Typically
- Simplifies Amplifier Design
  Low Output Conductance

8-Pin Mini DIP
See Section 5





ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±40 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Package Dissipation (25°C Free-Air) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −55 to +125°C
Operating Temperature Range . . . . . −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) . . . 260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

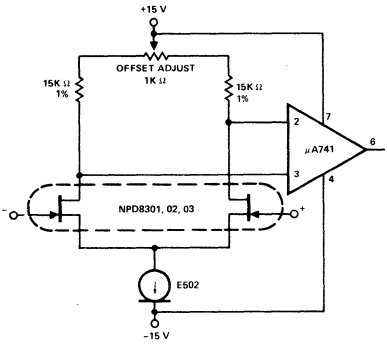
		Characteristic		NPD8301			NPD8302			NPD8303			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			−100			−100			−100	pA	V_{DS} = 0, V_{GS} = −20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−3.5	−0.5		−3.5	−0.5		−3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40			−40			−40			V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5		6.0	0.5		6.0	0.5		6.0	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)			−100			−100			−100	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	−0.3		−3.0	−0.3		−3.0	−0.3		−3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	700		1,200	700		1,200	700		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DS} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2		pF		
13	DYNAMIC	$\overline{e_N}$	Equivalent Short-Circuit Input Noise Voltage		13	50		13	50		13	50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			5			10			15	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			15			25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)	70	80			80			80		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V.

NQP

APPLICATIONS

Inexpensive All-Epoxy
General Purpose FET Input Op Amp



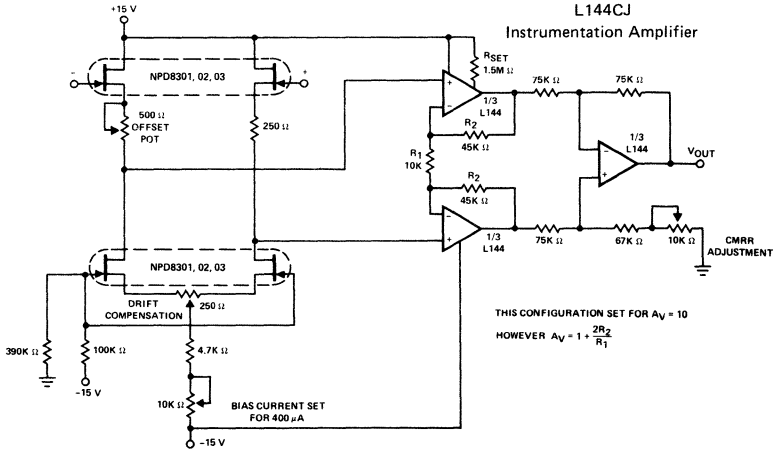
For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

FET Input Instrumentation Amplifier

L144CJ
Instrumentation Amplifier



p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 4

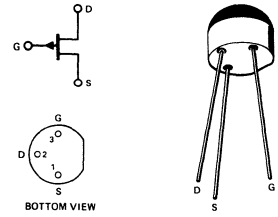
BENEFITS

- Low Insertion Loss
  $R_{DS(on)}$ = 75 Ω Maximum (P1086E)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		P1086E Min	P1086E Max	P1087E Min	P1087E Max	Unit	Test Conditions	
1		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		2		2	nA	V_{GS} = 15 V, V_{DS} = 0	
3		$I_{D(off)}$	Drain Cutoff Current		−10		−10	nA	V_{DS} = −15 V, V_{GS} = 12 V (P1086E)	
4	STATIC				−0.5		−0.5	μA	V_{GS} = 7 V (P1087E)	T_A = 85°C
5		I_{DGO}	Drain Reverse Current		2		2	nA	V_{DG} = −15 V, I_S = 0	
					0.1		0.1	μA		T_A = 85°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	V_{DS} = −15 V, I_D = −1 μA	
7		I_{DSS}	Saturation Drain Current	−10		−5		mA	V_{DS} = −20 V, V_{GS} = 0	
8		$V_{DS(on)}$	Drain-Source ON Voltage		−0.5		−0.5	V	V_{GS} = 0, I_D = −6 mA (P1086E), I_D = −3 mA (P1087E)	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	I_D = −1 mA, V_{GS} = 0	
10		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	V_{DS} = −15 V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		V_{DS} = 0, V_{GS} = 12 V (P1086E) V_{GS} = 7 V (P1087E)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = −6 V, $V_{GS(on)}$ = 0	
14		t_r	Rise Time		20		75			
15		$t_{d(off)}$	Turn-OFF Delay Time		15		25		P1086E: $V_{GS(off)}$ = 12 V, $I_{D(on)}$ = −6 mA, R_L = 910 Ω	
16		t_f	Fall Time		50		100		P1087E: $V_{GS(off)}$ = 7 V, $I_{D(on)}$ = −3 mA, R_L = 1.8K Ω	

NOTE:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

PS

low-leakage pico-amp diodes *designed for . . .*

- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

- Very High Off-Isolation 1 pA Max (PAD1)

TO-18
See Section 5

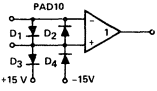
CASE LEAD FOR PAD1, 2, 5 ONLY

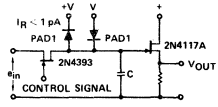
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . . 50 mA
Total Device Dissipation . . . . . 300 mW
Storage Temperature Range . . . . . -55°C to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_R Reverse Current			-1	pA	V_R = -20 V	PAD1
2					-2			2
3					-5			5
4					-10			PAD10
5					-20			20
6					-50			50
7					-100			PAD100
8		BV_R Breakdown Voltage (Reverse)	-45		-120	V	I_R = -1 μA	PAD1, 2, 5
9			-35					PAD10, 20, 50, 100
10		V_F Forward Voltage Drop		0.8	1.5		I_F = 5 mA	PAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R Capacitance			0.8	pF	V_R = -5 V, f = 1 MHz	PAD1, 2, 5
12					2			PAD10, 20, 50, 100





APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D_1 and D_2 Common mode input voltage limited by PADS D_3 and D_4 to ±15 V.

Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

n-channel transducer/microphone preamplifiers *designed for . . .*

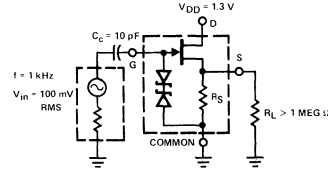
- **Hearing Aid Input Stages**
- **High Impedance Transducer Buffer Amplifiers**
  - **Electret-Condenser**
  - **Ceramic**
  - **Piezo-Electric**
  - **Capacitive**
  - **Air Condenser**
- **Self-Biased General Purpose High Impedance Source Followers**

Performance Curves NYFA NYFC See Section 4

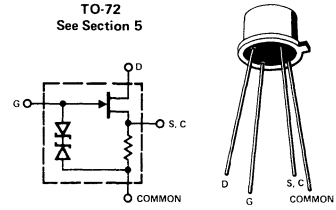
BENEFITS

- Complete Preamplifier, Requires No External Components
- Compact for Placement at Transducer
- Operates on Single Battery
- Ultra-High Input Impedance $5 \times 10^9\ \Omega$ Typical
- Available in Chip Form for Hybrid Systems

TEST CONFIGURATION



TO-72
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source and Drain-Gate Voltage	30 V
Gate Voltage (With Respect to Common)	±2.0 V
Forward Gate Current	1 mA
Total Device Dissipation (25°C Free-Air)	180 mW
Linear Derating Factor (to 85°C)	3.0 mW/°C
Storage Temperature Range	−55 to +150°C
Operating Temperature Range	−25 to +85°C
Lead Temperature (1/16" from Case for 10 Sec.)	260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	T100 Min	T100 Typ	T100 Max	T300 Min	T300 Typ	T300 Max	Unit	TEST CONDITIONS All characteristics (unless otherwise specified) are measured in Test Configuration with V_{in} = 100 mV (RMS), f = 1 kHz, C_c = 10 pF, V_{DD} = 1.3 V, R_L = 1 MEG Ω
1	STATIC	BV_{DSS} Drain-Source (Drain-Gate) Breakdown[1]	30			30			V	I_D = 1 μA, V_{IN} = 0, C_c Shorted
2	STATIC	I_D Operating Drain Current Range	10		50	70		350	μA	V_{IN} = 0, C_c Shorted
3	STATIC	R_{in} Input Resistance[2]	200M	5G		200M	5G		Ω	V_{IN} = 100 mV DC Measurement, C_c Shorted
4	STATIC	R_{out} Output Resistance	1500		3500	500		1300	Ω	V_{IN} = 0, C_c Shorted
5	DYNAMIC	A_V Voltage Gain	0.40	0.60		0.30	0.45		V/V	
6	DYNAMIC	THD Total Harmonic Distortion		1.0			1.0		%	
7	DYNAMIC	e_{out} Broadband Output Noise Voltage			4.0			2.0	μV	V_{IN} = 0, f = 10 Hz to 10 kHz, C_c Shorted
8	DYNAMIC	C_{in} Input Capacitance		3.0	4.0		3.0	4.0	pF	V_{DD} 20 V, V_{IN} 0,
9	DYNAMIC	C_{out} Output Capacitance		4.4	6.0		4.4	6.0		f = 1 MHz, C_c Shorted
			NYFC			NYFA				

NOTES:
1. Drain-Gate Breakdown Guaranteed by Drain-Source Breakdown Test.
2. M = 10^6, G = 10^9.

APPLICATIONS

Basic JFET Source Follower Equations are:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (1)$$

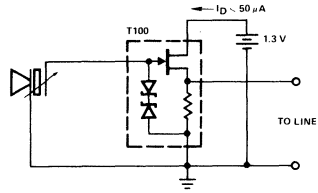
where $V_{GS} = -I_D R_S$ (2)

$$g_{fs} = \frac{-2 I_{DSS}}{V_P}\left(\frac{I_D}{I_{DSS}}\right)^{1/2} \quad (3)$$

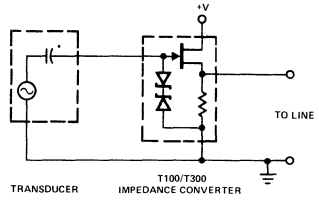
$$R_{OUT} = \frac{R_S}{1 + g_{fs} R_S} \quad (4)$$

$$A_V = g_{fs} R_{OUT} \quad (5)$$

T100 as a Micropower Preamplifier – As in a Hearing Aid Input

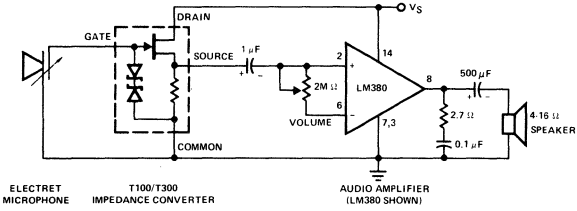


T100/T300 as an Impedance Converter for Transducer Input

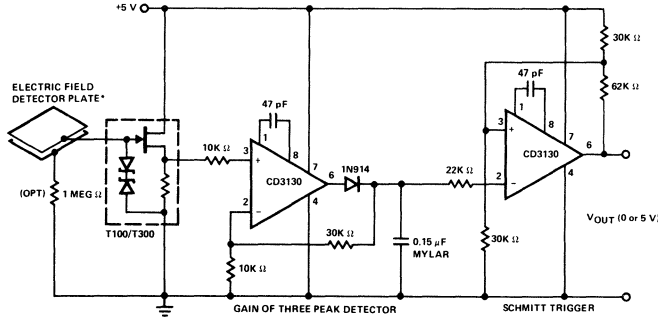


*NO CAPACITOR ISOLATION IS REQUIRED FOH CAPACITIVE TRANSDUCERS OR HIGH-IMPEDANCE PURE VOLTAGE SOURCES.

T100/T300 as a Preamplifier in a Microphone Amplifier Circuit



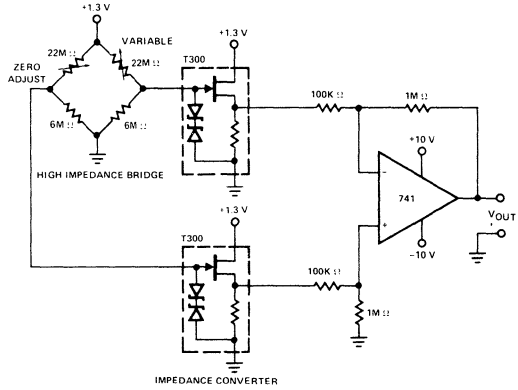
T100/T300 as a Self-Biased Proximity Sensor Works on Detected Changing Field



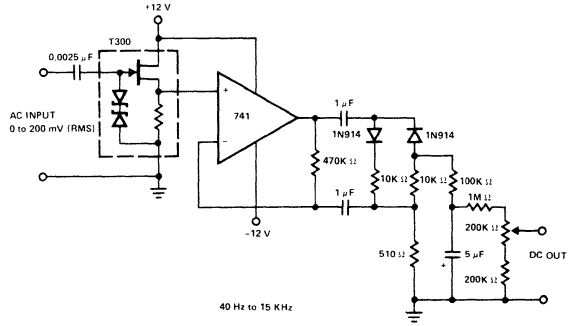
*DETECTOR PLATE MAY BE DOUBLE-SIDED PC BOARD OR ANY INSULATED METAL SHEET

APPLICATIONS (Cont'd)

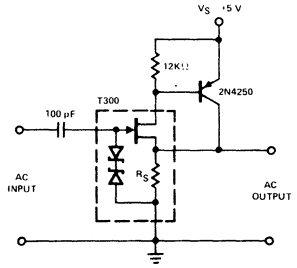
T300's as Low Signal Level, High Impedance Instrumentation Amplifier



T100 in a High Impedance Precision Rectifier for AC/DC Converter



Source Follower with Voltage Gain Typically Greater Than 0.95 V/V and Z_{OUT} Typically Less Than 60 Ω



n-channel JFET *designed for . . .*

- **VHF/UHF Amplifier**
- **Oscillators**
- **Mixers**

Performance Curves NH
See Section 4

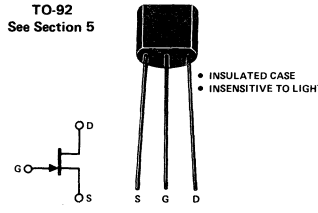
BENEFITS

- Specified for 100 MHz and 400 MHz Operation
- Low Cost
- Automated Insertion Package

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage . . . . . 30 V
Drain-Gate Voltage . . . . . 30 V
Reverse Gate-Source Voltage. . . . . −30 V
Forward Gate Current. . . . . 50 mA
Total Device Dissipation @ 25°C. . . . . 360 mW
Derate above 25°C . . . . . 2.88 mW/°C
Storage Temperature Range . . . . . −65 to +150°C
Operating Junction Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 5



- INSULATED CASE
- INSENSITIVE TO LIGHT

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		−1.0	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
3					−0.5	μA		$T_A = 100°C$
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−6	V	$V_{DS} = 15$ V, $I_D = 10$ nA	
5		I_{DSS}	Saturation Drain-Current (Note 1)	5	15	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
6	DYNAMIC	$\lvert y_{fs}\rvert$	Common-Source Forward Transfer Admittance	4.5	7.5	mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz	
7		$\lvert y_{os}\rvert$	Common-Source Output Admittance		0.05	mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 kHz	
8		C_{iss}	Common-Source Input Capacitance		4.5	pF	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1 MHz	
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	pF		
10		$Re(Y_{is})$	Common-Source Input Conductance		0.1	mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 100 MHz	
11		$Im(Y_{is})$	Common-Source Input Susceptance		3	mmho		
12		$Re(Y_{os})$	Common-Source Output Conductance		0.075	mmho		
13		$Im(Y_{os})$	Common-Source Output Susceptance		0.9	mmho		
14		$Re(Y_{is})$	Common-Source Input Conductance		1	mmho	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 400 MHz	
15		$Im(Y_{is})$	Common-Source Input Susceptance		12	mmho		
16		$Re(Y_{fs})$	Common-Source Forward Transfer Conductance		4	mmho		
17		$Re(Y_{os})$	Common-Source Output Conductance		0.1	mmho		
18		$Im(Y_{os})$	Common-Source Output Conductance		4	mmho		
19		G_{ps}	Common-Source Neutralized Insertion Power Gain	18		dB	$V_{DS} = 15$ V, $I_D = 5$ mA	f = 100 MHz
20				10		dB		f = 400 MHz
21		NF	Noise Figure		2	dB	$V_{DS} = 15$ V, $I_D = 5$ mA, $R_G = 1K\ \Omega$	f = 100 MHz
22					4	dB		f = 400 MHz

NOTE:
1. Pulse tested: pulse width = 300 μs, duty cycle ≤ 2%.

NH

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 50\ \Omega$ (U202)
- Good Off-Isolation
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-18
See Section 5

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U200 Min	U200 Max	U201 Min	U201 Max	U202 Min	U202 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-1		-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		V_{DS} = 20 V, I_D = 10 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	V_{DS} = 10 V, V_{GS} = -12 V	
					1		1		1	μA		150°C
6		I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		8		8		8		V_{DS} = 0, V_{GS} = -12 V	

NOTE: NC
1. Pulse test required, pulsewidth = 300 μsec, duty cycle ≤ 3%.

monolithic dual n-channel JFETs *designed for . . .*

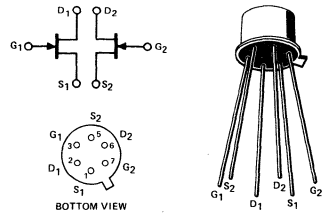
■ Differential Amplifiers

Performance Curves NNP
See Section 4

BENEFITS

- Good Matching Characteristics

TO-71
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C
(Derate 1.7 mW/°C to 200°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4.0			
6		I_G	Gate Operating Current		-50	pA	V_{DG} = 20 V, I_D = 200 μA	
					-250	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
				1000				f = 100 MHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		10		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	10	10	10	10	10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV	V_{DG} = 20 V, I_D = 200 μA	T_A = 25°C T_B = 125°C
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	μV/°C		
19				10	25	50	75	100			T_A = -55°C T_B = 25°C
20		$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance	5	5	5	5	5	μmho		

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle ⩽ 3%.
2. Measured at end points, T_A and T_B.

NNP

matched dual n-channel JFET *designed for . . .*

■ Wideband Differential Amplifiers

Performance Curves NZF See Section 4

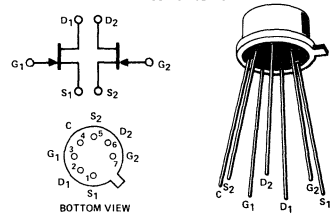
BENEFITS

- High Gain through 100 MHz
  g_{fs} = 5000 μmho Minimum
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 3.85 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 7.7 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-78
See Section 5



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{fs}	Common-Source Forward Transconductance	5000	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
8		g_{os}	Common-Source Output Conductance		150		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		150		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
10		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
13	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
14		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
15		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.85	1			f = 1 kHz
16		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTES:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 30%.
2. Assumes smaller value in numerator.

NZF

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NVA
See Section 4

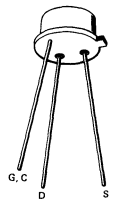
BENEFITS

- Ultra-Low Insertion Loss
  $R_{DS(on)} < 2.5\ \Omega$ (U290)
- High Off-Isolation
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 100 mA
Drain Current . . . . . 1.5 A
Total Device Dissipation at 25°C
Free-Air Temperature (Note 1) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-52
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U290 Min	U290 Max	U291 Min	U291 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-1.5	-4.5		V_{DS} = 15 V, I_D = 3 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6					1		1	μA		150°C
7		$V_{DS(on)}$	Drain-Source ON Voltage		25		70	mV	V_{GS} = 0, I_D = 10 mA	
8		I_{DSS}	Saturation Drain Current (Note 2)	500		200		mA	V_{DS} = 10 V, V_{GS} = 0	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V_{GS} = 0 V, I_D = 10 mA	
10	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{SGO}	Source-Gate OFF Capacitance		30		30	pF	V_{SG} = 15 V, I_D = 0	f = 1 MHz
12		C_{DGO}	Drain-Gate OFF Capacitance		30		30		V_{DG} = 15 V, I_S = 0	
13		$C_{SG}+C_{DG}$	Source Gate Plus Drain Gate On Capacitance		160		160		V_{DS} = 0, V_{GS} = 0	
14	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = 1.5 V, $I_{D(on)}$ = 30 mA, R_L = 50 Ω, $V_{GS(on)}$ = 0 V, $V_{GS(off)}$ = -12 V (U290) $V_{GS(off)}$ = - 7 V (U291)	
15		t_r	Rise Time		20		20			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		15			
17		t_f	Fall Time		20		20			

NOTES: NVA

1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

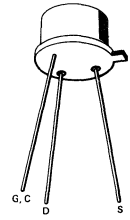
- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NVA
See Section 4

BENEFITS

- Ultra-Low Insertion Loss
  $R_{DS(on)} < 2.5\ \Omega$ (U295)
- High Off-Isolation
  $I_{D(off)} < 1$ nA
- Higher Power Dissipation Package than U290, 1
- No Offset or Error Voltage Generated by Closed Switch
  Purely Resistive

TO-39
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –30 V
Gate Current . . . . . 100 mA
Drain Current . . . . . 1.5 A
Total Continuous Free Air Device Dissipation
at (or Below) T_A = 25°C
(Derate 6.4 mW/°C to 150°C) . . . . . 800 mW
Total Continuous Device Dissipation
at (or Below) T_C = 25°C
(Derate 24 mW/°C to 150°C) . . . . . .3 W
Storage Temperature Range . . . . . –65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	U295 Min	U295 Max	U296 Min	U296 Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current		–1		–1	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–1		–1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		–30		V	I_G = –1 μA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–4	–10	–1.5	–4.5		V_{DS} = 15 V, I_D = 3 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1	nA	V_{DS} = 5 V, V_{GS} = –10 V	
6					1		1	μA		150°C
7		$V_{DS(on)}$	Drain Source ON Voltage		25		70	mV	V_{GS} = 0, I_D = 10 mA	
8		I_{DSS}	Saturation Drain Current (Note 1)	500		200		mA	V_{DS} = 10 V, V_{GS} = 0	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V_{GS} = 0 V, I_D = 10 mA	
10	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{SGO}	Source-Gate OFF Capacitance		30		30	pF	V_{SG} = 15 V, I_D = 0	f = 1 MHz
12		C_{DGO}	Drain-Gate OFF Capacitance		30		30		V_{DG} = 15 V, I_S = 0	
13		$C_{SG}+C_{DG}$	Source-Gate Plus Drain-Gate ON Capacitance		160		160		V_{DS} = 0, V_{GS} = 0	
14	SWITCHING	$t_{d(on)}$	Turn ON Delay Time		15		15	ns	V_{DD} = 1.5 V, $I_{D(on)}$ = 30 mA	
15		t_r	Rise Time		20		20		$V_{GS(on)}$ = 0, R_L = 50 Ω	
16		$t_{d(off)}$	Turn OFF Delay Time		15		15		$V_{GS(off)}$ = –12 V (U295)	
17		t_f	Fall Time		20		20		$V_{GS(off)}$ = –7 V (U296)	

NVA

NOTES:
1. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves PS See Section 4

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (U304)
- High Off-Isolation
  $I_{D(off)} < 500$ pA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation, Free-Air
(Derate 2.8 mW/°C) . . . . . 350 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 5

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0	
2					1.0		1.0		1.0	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 μA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		V_{DS} = -15 V, I_D = -1 μA	
5		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		V_{GS} = 0, I_D = -15 mA (U304), I_D = -7 mA (U305), I_D = -3 mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	V_{DS} = -15 V, V_{GS} = 0	
7		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15 V, V_{GS} = 12 V (U304), V_{GS} = 7 V (U305), V_{GS} = 5 V (U306)	
8					-1.0		-1.0		-1.0	μA		150°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0 V, I_D = -1 mA	
10		$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		27		27		27	pF	V_{DS} = -15 V, V_{GS} = 0	
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		V_{DS} = 0, V_{GS} = 12 V (U304) V_{GS} = 7 V (U305), V_{GS} = 5 V (U306)	f = 1 MHz
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns		
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn-OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

PS

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

- **VHF Amplifiers**
- **Front End High Sensitivity Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA See Section 4

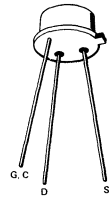
BENEFITS

- Industry Standard
- High Power Gain
  16 dB at 105 MHz, Common-Gate
  11 dB at 450 MHz, Common-Gate
- Low Noise
  2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- 75 Ω Input Match Common Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 20 mA
Total Power Dissipation at T_A = 25°C . . . . . 500 mW
Power Derating to 150°C . . . . . 4.0 mW/°C
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-52
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

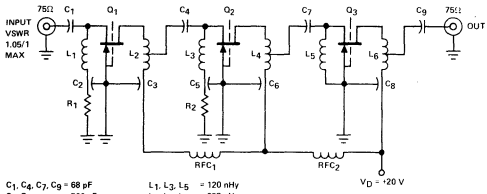
		Characteristic		U308			U309			U310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current			–150			–150			–150	pA	V_{GS} = –15 V, V_{GS} = 0	
2						–150			–150			–150	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–6.0	–1.0		–4.0	–2.5		–6.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
7	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance			150			150			150	μmho		
9		C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = –10 V, V_{DS} = 10 V	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
11		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
13					14			14			14				f = 450 MHz
14		g_{og}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 105 MHz
15					0.32			0.32			0.32				f = 450 MHz
16		G_{pg}	Common-Gate Power Gain (Note 2)	14	16		14	16		14	16		dB		f = 105 MHz
17				10	11		10	11		10	11				f = 450 MHz
18		NF	Noise Figure		1.5	2.0		1.5	2.0		1.5	2.0			f = 105 MHz
19					2.7	3.5		2.7	3.5		2.7	3.5			f = 450 MHz

NOTES:
1. Pulse test duration = 2 ms.
2. Gain (G_{pg}) measured at optimum input noise match.

NZA

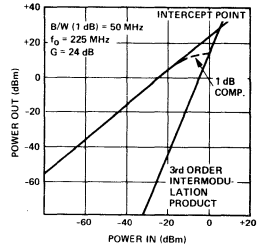
APPLICATIONS

200-250 MHz Wideband Amplifer (1 dB Ripple) 3-Stage Amplifier Circuit

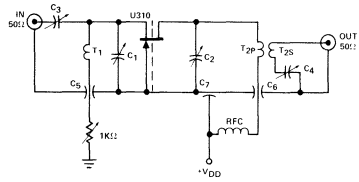


C_1, C_4, C_7, C_9 = 68 pF
C_2, C_5 = 500 pF
C_3, C_6, C_8 = 1,000 pF
Q_1, Q_2, Q_3 = Siliconix U310
L_1, L_3, L_5 = 120 nHy
L_2, L_4, L_6 = 222 nHy
RFC_1, RFC_2 = 2.2 μHy
R_1, R_2 = 51 Ω

2 Tone Intercept & Compression Point Measurement

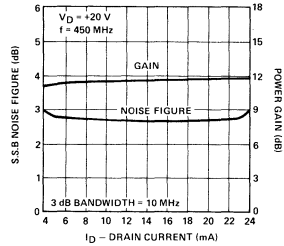


450 MHz Common Gate Amplifier

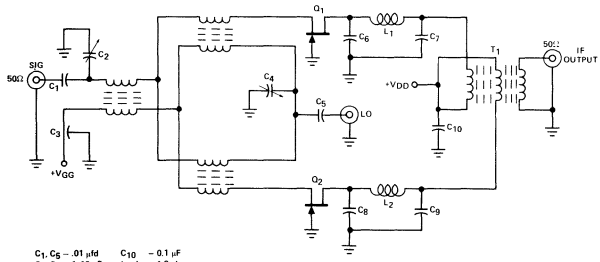


C_1, C_2 – 0.8–10 pF JFD model MVM 010W
C_3, C_4 – 8–35 pF Erie series 539 002D
C_5, C_6 – 5000 pF Erie (2443-000)
C_7 – 1000 pF ALLEN-BRADLEY type FA5C
RFC – 33 μH MILLER type (9230-30)
T_1 – one turn, #16 copper wire, ¼" I.D. (Air Core)
T_{2P} – one turn, #16 copper wire, ¼" I.D. (Air Core)
T_{2S} – one turn, #16 copper wire, ¼" I.D. (Air Core)

Noise Figure vs. Power Gain



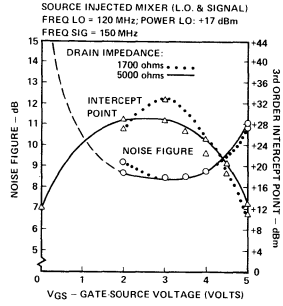
Prototype Active Balanced Mixer*



C_1, C_6 – .01 μfd
C_2, C_4 – 1-10 pF
C_3 – 1000 pF
C_5, C_8 – 30 pF
C_7, C_9 – 68 pF
C_{10} – 0.1 μF
L_1, L_2 – 1.3 μhy
Q_1, Q_2 – U310
T_1 – RELCOM BT-9

*Reference Siliconix Application Note AN71-2.

Comparison of Mixer IM Characteristics



n-channel JFET
designed for . . .

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA
See Section 4

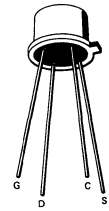
BENEFITS

- High Power Gain
  16 dB Typ @ 105 MHz, Common-Gate
  11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure
  1.5 dB Typ @ 105 MHz
  2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... -25 V
Gate Current ..... 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

TO-72
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-150	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-150	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	20	60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		1	V	I_G = 1 mA, V_{DS} = 0	
7	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000	20,000	μmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance		150			
9		C_{gd}	Gate-Drain Capacitance		2.5	pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance		5.0			

NZA

NOTE:
1. Pulse test duration = 2 ms.

3

n-channel JFET
designed for . . .

- **VHF/UHF Common-Gate Amplifiers**
- **Mixers**

Performance Curves NZF
See Section 4

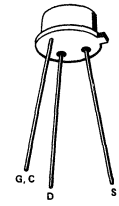
BENEFITS

- High Power Gain
  10 dB Typical at 450 MHz, Common Gate
- Low Noise
  NF = 3.5 dB Typical at 450 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Power Dissipation at or below 25°C
Free-Air Temperature . . . . . 500 mW
Power Derating . . . . . 4.0 mW/°C
Operating Temperature Range . . . . . -65 to +150°C
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-52
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6	V	V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	10	30	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	6000	10,000	μmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
7		g_{og}	Common-Gate Output Conductance		200	μmho		
8		C_{gd}	Gate-Drain Capacitance		1.2	pF	V_{DG} = 10 V, I_D = 10 mA	f = 1 MHz
9		C_{gs}	Gate-Source Capacitance		3.8	pF		

NOTE:
1. Pulse test duration = 2 ms.

NZF

n-channel JFETs *designed for . . .*

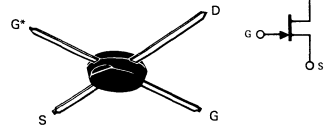
■ UHF Amplifiers

Performance Curves NZF
See Section 4

BENEFITS

- High Power Gain
  10 dB Typical at 450 MHz
- Low Noise
  3.4 dB Typical at 450 MHz
- Low Intermodulation Distortion
- Hermetic Stripline Package

OD-84
See Section 5



Note: G* is back Gate contact.

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.0 mW/°C) . . . . . 175 mW
Storage Temperature Range . . . . . -65 to +200°C
Operating Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

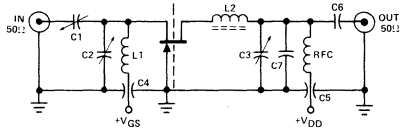
		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	10	30	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	6000	10,000	μmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		200			
8		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			

NOTE:
1. Pulse test duration = 2 ms.

NZF

3

450 MHz Gain and Noise Figure Test Circuit for J315



C1 2.5-11 ERIE N650
C2, C3 .8-10pF JFD MVM010W
C4, C5 1000pF AB FASC
C6 100pF
C7 10pF
L1 17 r hy 3/4" 28 AWG
L2 100nhy, 2T 1/4 OD #18 AWG
RFC .33 hy Miller 9230-30

n-channel JFETs *designed for . . .*

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA
See Section 4

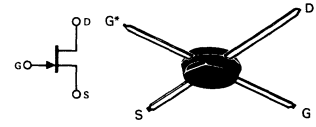
BENEFITS

- Hermetic Strip Line Package
- High Power Gain
  16 dB Typical at 105 MHz, Common-Gate
  11 dB Typical at 450 MHz, Common-Gate
- Low Noise Figure
  1.5 dB Typical at 105 MHz
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range—Greater than 100 dB
- Worst Case Input Power Match (75 Ω) VSWR 1.25:1

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 20 mA
Total Device Dissipation . . . . . 175 mW
Derate . . . . . 1 mW/°C
Surface Temperature Range . . . . . -65°C to +200°C
Lead Temperature 1/16 From Case (max 10 Sec). . . . 300°C

OD-84
See Section 5



Note: G* is back Gate contact.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J316 Min	J316 Max	J317 Min	J317 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-1		-1	μA		T = 125°C
3		BV_{GSS}	Gate Source Breakdown Volt.	-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4	-2.5	-6		V_{DS} = 10 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		I_G = 10 mA, V_{DS} = 0	
6		I_{DSS}	Saturation Drain Current	12	30	24	60	mA	V_{DS} = 10 V, V_{GS} = 0 (Note 1)	
7	DYN	g_{fg}	Common-Gate Forward Transconductance	10	20	10	18	m mho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz (Note 1)
8		g_{og}	Common-Gate Output Conductance		150		150	μ mho		
9		C_{gd}	Gate-Drain Capacitance		3		3	pF	V_{DS} = 10 V V_{GS} = -10 V	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance		3		3			

NZA

NOTE:
1 Pulsed (test duration 2 mS)

n-channel JFETs *designed for . . .*

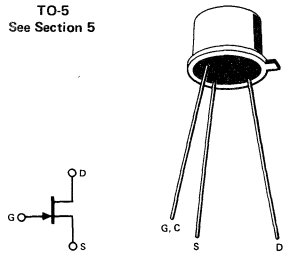
- **VHF Buffer Amplifiers**
- **IF Amplifiers**

Performance Curves NIP See Section 4

BENEFITS

- High Gain
  g_{fs} = 120,000 μmho Typical
- Wide Dynamic Range
- Low Intermodulation Distortion

TO-5
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

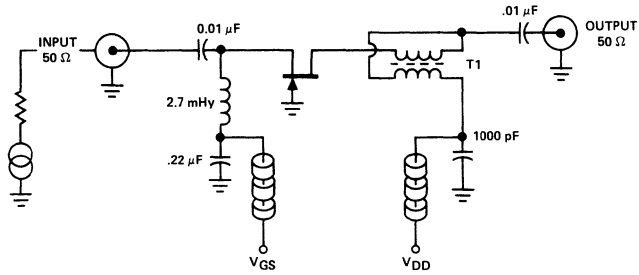
Gate-Drain or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 100 mA
Total Device Dissipation (25°C Case Temperature) . . . . . 3 W
Power Derating (to 150°C) . . . . . 24 mW/°C
Storage Temperature Range . . . . . −55 to +150°C
Operating Temperature Range . . . . . −55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U320			U321			U322			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-0.5			-0.5			-0.5	μA		T = 100°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2		-10	-1		-4	-3		-10	V	V_{DS} = 5 V, I_D = 1 mA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				I_G = -1 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	100		500	80		250	200		700	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1			1			1	V	I_G = 1 mA, V_{DS} = 0 V	
7		$r_{DS(on)}$	Drain-Source ON Resistance			10			11			8	Ω	V_{GS} = 0 V, I_D = 10 mA	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	75	120	200	75	120	200	75	130	200	mmhos	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance			30			30			30	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance			15			15			15			
11		C_{gs}	Gate-Source Capacitance		12			12			12			V_{GS} = -10 V, I_D = 0	
12		C_{gd}	Gate-Drain Capacitance		12			12			12			V_{GD} = -10 V, I_S = 0	
13		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		2			2			2		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 5 V, I_D = 10 mA	f = 1 kHz
14	HIGH FREQ	g_{fg}	Common Gate Forward Transconductance		55			55			55		mmho	V_{DG} = 20 V, I_D = 25 mA	f = 50 MHz
15		g_{ig}	Common-Gate Input Conductance		56			56			56				
16		g_{og}	Common-Gate Output Conductance		0.5			0.5			0.5				
17		G_{PS}	Power Gain (Note 3)		9			9			9		dB		
18		F_t	Gain-Bandwidth (Note 4)		400			400			400		MHz	V_{DS} = 15 V, V_{GS} = 0 V	
19		NF	Noise Figure (Note 3)		2.5			2.5			2.5		dB	V_{DG} = 20 V, I_D = 25 mA	f = 30 MHz

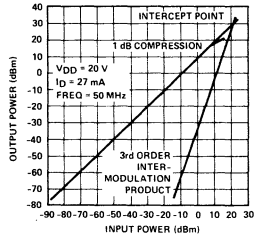
NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Noise figure (SSB) and power gain measured in circuit shown in Figure 1.
4. Computed as g_{fs}/C_{rss}.

NIP



T1–6 TURNS #22 AWG TWISTED PAIR WIRE ON 0.375 INCH DIAMETER INDIANA GENERAL F625-9Q2 TOROID CORE.

50 MHz Power Gain and Noise Figure Test Circuit for U320, U321 and U322
Figure 1



Gain – Intermodulation Characteristics
Figure 2

quad-ring demodulator designed for . . .

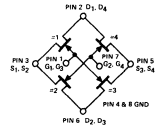
- **VHF Double-Balanced Mixers**
- **Analog Multipliers**

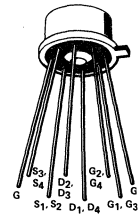
Performance Curves NZA
See Section 4

BENEFITS

- Four Matched U310 FETs
- High IMD Intercept Point
- Low Turn-ON Resistance
- Conversion Gain
- High 1 dB Compression
- Suitable for PC Board Construction

TO-99
See Section 5





ABSOLUTE MAXIMUM RATINGS (25°C)

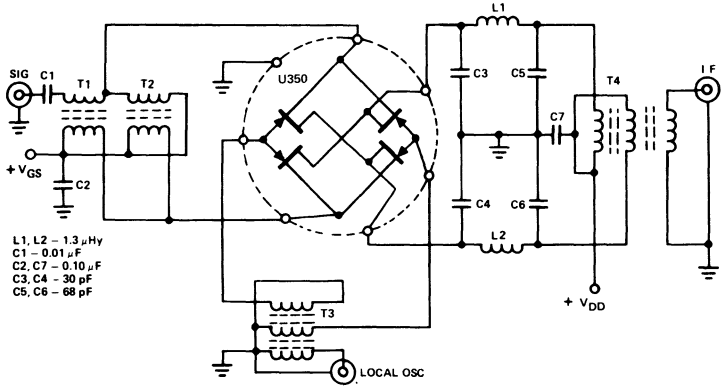
Gate-Drain or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 25 mA
Total Continuous Power Dissipation
at (or Below) 25°C Free Air Temperature
(Derate 8.0 mW/°C to 150°C) . . . . . 1 W
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U350 Min	U350 Typ	U350 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-1	nA	V_{GS} = -15 V, V_{DS} = 0	
2						-1	μA	(Note 1)	T_A = +125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2		-6		I_D = 1 nA, V_{DS} = 10 V (Note 1)	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1		I_G = 1 mA, V_{DS} = 0 (Note 1)	
6		I_{DSS}	Drain Saturation Current	24		60	mA	V_{DS} = 15 V, V_{GS} = 0 (Notes 1 and 2)	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10		18	m℧	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz (Note 1)
8		g_{os}	Common-Source Output Conductance			150	μ℧		
9		C_{gs}	Gate-Source Capacitance			5	pF	V_{GS} = -10 V, I_D = 0	f = 1 MHz (Note 1)
10		C_{gd}	Drain Gate Capacitance			2.5		V_{GD} = -10 V, I_S = 0	
11		$R_{ds(on)}$	Drain-Source ON Resistance		50	90	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
12	HF	G_c	(Conversion Gain)		4		dB	V_{DS} = 20 V, V_{GS} = ½$V_{GS(off)}$, R_D = 1,700 Ω	f = 100 MHz (Note 3)
13		NF	Noise Figure		7				
14	MATCH	I_{DSS}/I_{DSS}	Saturation Drain Current Ratio	0.9		1.0		V_{DS} = 15 V, V_{GS} = 0 (Note 2)	
15		$V_{GS(off)}/V_{GS(off)}$	Gate-Source Cutoff Voltage Ratio	0.9		1.0		V_{DS} = 15 V, I_D = 1 nA	
16		g_{fs}/g_{fs}	Common-Source Forward Transconductance	0.9		1.0		V_{DS} = 15 V, I_D = 10 mA	f = 1 kHz
17		g_{os}/g_{os}	Differential Output Conductance	0.9		1.0			

NZA

NOTES:
1. Other gate terminal clamped to -8 V
2. Pulse test: PW 300 μsec DC ≤ 3 %.
3. See Figure 1.



Double-Balanced Mixer using U350*
Figure 1

*Reference Siliconix application note AN73-4

U401 U402 U403 U404 U405 U406

monolithic dual n-channel JFETs *designed for . . .*

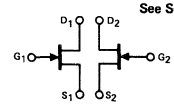
- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

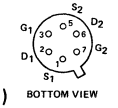
Performance Curves NNR See Section 4

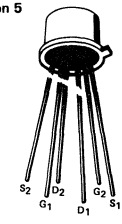
BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (U401)
  95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
  10 μV/°C Maximum (U401, 02)
- Operates from Low Power Supply Voltages
  $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\overline{e_n}$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

TO-71
See Section 5







ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side) @ T_A = 85°C derate 2.6 mW/°C	300 mW
Total Device Dissipation @ T_A = 85°C (derate 5 mW/°C)	500 mW
Storage Temperature Range	−65 to 200°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

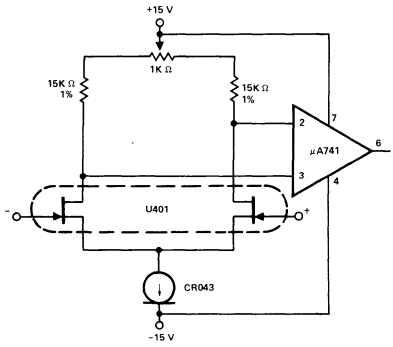
		Characteristic		U401 Min	U401 Max	U402 Min	U402 Max	U403 Min	U403 Max	U404 Min	U404 Max	U405 Min	U405 Max	U406 Min	U406 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		−25		−25		−25		−25		−25		−25	pA	V_{DS} = 0, V_{GS} = −30 V	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4	STATIC	$V_{GS(on)}$	Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3	V	V_{DG} = 15 V, I_D = 200 μA	
5	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6	STATIC	I_G	Gate Current (Note 1)		−15		−15		−15		−15		−15		−15	pA	V_{DG} = 15 V,	
7	STATIC	I_G	Gate Current (Note 1)		−10		−10		−10		−10		−10		−10	nA	I_D = 200 μA	T_A = 125°C
8	STATIC	BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance		20		20		20		20		20		20	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	μmho	V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
12	DYNAMIC	g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0	μmho	V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
13	DYNAMIC	C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF	V_{DG} = 15 V, I_D = 200 μA	f = 1 MHz
14	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0	pF	V_{DG} = 15 V, I_D = 200 μA	f = 1 MHz
15	DYNAMIC	$\overline{e_N}$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17	MATCHING	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18	MATCHING	$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4).		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55°C, T_B = +25°C T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300 μs; duty cycle ≤ 3%. 3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

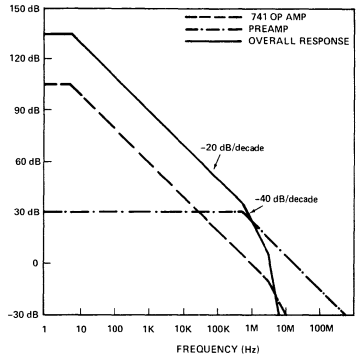
NNR

APPLICATIONS

General Purpose FET Input Op Amp



Open Loop Gain and Frequency Response of Op Amp



Typical Specs for General Purpose FET Input Op Amp*

Common Mode Range . . . . . +6.7 to -8.8 Volts
Worst Case Drift Referred to the Input . . ≈ 12 μV/°C
Broad Band Noise Referred to
the Input (0.1 to 1 kHz) . . . . . ≈ 188 nV/Rms
Gain and Bandwidth . . . . . (see graph)

*These specs depend upon the specifications of the Operational amplifier IC used.

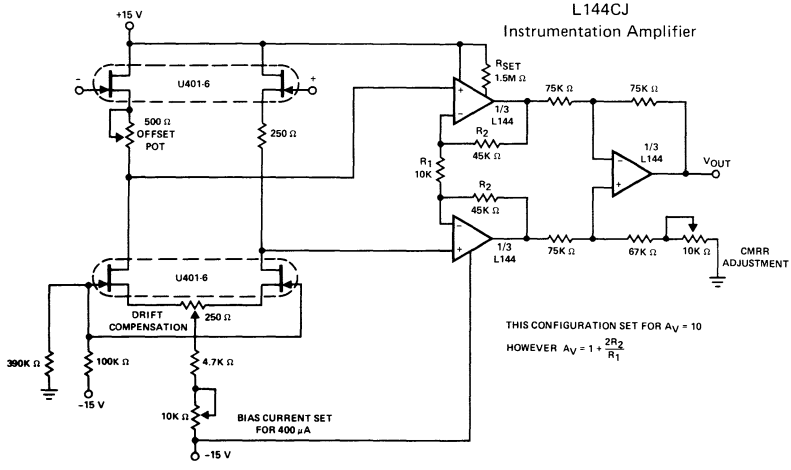
For futher design information, write for:

DESIGNING FET-INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included. (16 pages).

FET Input Instrumentation Amplifier

L144CJ
Instrumentation Amplifier



monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Performance Curves NQT See Section 4

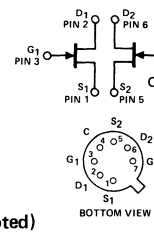
BENEFITS

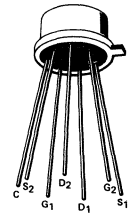
- High Input Impedance
  I_G = 0.1 pA Maximum (U421-3)
- High Gain g_{fs} = 140 μmho Minimum @ I_D = 30 μA (U421-3)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150°C

TO-78
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U421-3 Min	U421-3 Typ	U421-3 Max	U424-6 Min	U424-6 Typ	U424-6 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1 μA, V_{DS} = 0	
2	STATIC	BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40			V	I_G = −1 μA, I_D = 0, I_S = 0	
3	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			0.2			1.0	pA	T = +25°C	V_{GS} = −20 V, V_{DS} = 0
						0.5			1.0	nA	T = +125°C	
4	STATIC	I_G	Gate Operating Current (Note 1)			0.1			0.5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 μA
						-100			-500		T = +125°C	
5	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.4		-2.0	-0.4		-3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6	STATIC	V_{GS}	Gate-Source Voltage			-1.8			-2.9	V	V_{DG} = 10 V, I_D = 30 μA	
7	STATIC	I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1000	μ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			3.0			5.0	μ℧		
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5	pF		
12	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	140		250	135		300	μ℧	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
13	DYNAMIC	g_{os}	Common-Source Output Conductance			0.5			1.0	μ℧		
14	DYNAMIC	$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	nV/√Hz		f = 10 Hz
					10			10	50	nV/√Hz		f = 1 kHz
15	DYNAMIC	NF	Noise Figure			1.0			1.0	dB		f = 10 Hz, R_G = 10M Ω

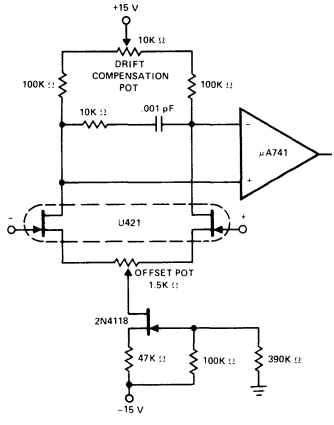
		Characteristic		U421, 4 Min	U421, 4 Typ	U421, 4 Max	U422, 5 Min	U422, 5 Typ	U422, 5 Max	U423,6 Min	U423,6 Typ	U423,6 Max	Unit	Test Conditions
16	MATCH	$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10 V, I_D = 30 μA
17	MATCH	$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = −55°C, T_B = 25°C, T_C = 125°C
18	MATCH	CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V

NOTES.
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQT

APPLICATIONS

Very Low Leakage FET Input Op Amps



I_G	= 0.1 pA at V_{cm} = 0
Offset	= Can be nulled to 0 volts
Drift	= Can be nulled to 2 μV/°C
Slew Rate	= 0.5 V/μs

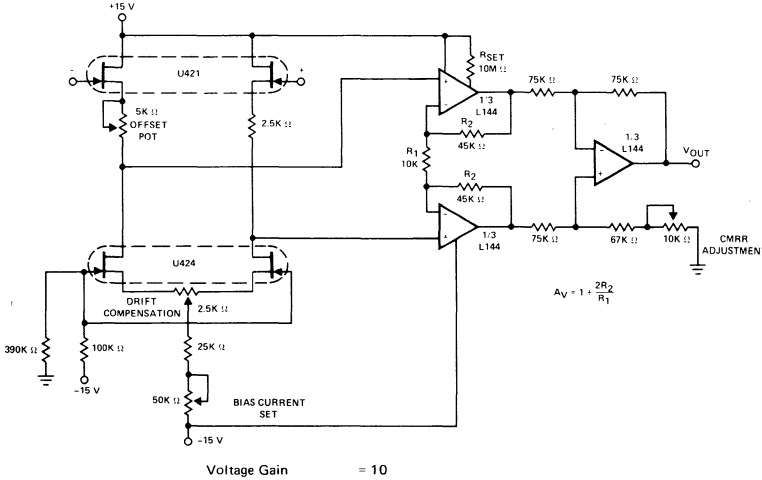
For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

Electrometer Amplifier

L144CJ Instrumentation Amplifier



Voltage Gain	= 10
Input Current	= 0.1 pA
Compensated Drift	= 3 μV/°C
Nulled Offset	= 0 mV
CMRR	= 80 dB typical
Power Consumption	= Approx. 30 Volt x 120 μA = 3.6 mW

3

matched dual n-channel JFETs *designed for . . .*

- **Balanced Mixers**
- **Differential Amplifiers**

Performance Curves NZA
See Section 4

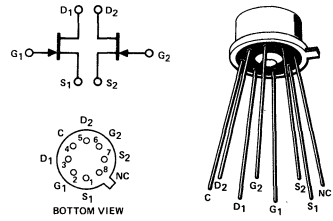
BENEFITS

- Low Noise Figure
- Low IMD
  30 dBm Intercept Point

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Continuous Power Dissipation at
(or Below) 25°C Free Air Temperature
Derate 4 mW/°C to 150°C. . . . . 500 mW
Continuous Device Dissipation (Each Side) at
(or Below) 25°C Free Air Temperature
Derate 2.4 mW/°C to 150°C . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-99
See Section 5



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		U430 Min	U430 Typ	U430 Max	U431 Min	U431 Typ	U431 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150	pA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-150			-150	nA		T = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	I_G = -1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-4.0	-2.0		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0		V_{DS} = 0 V, I_G = 10 mA	
6		I_{DSS}	Saturation Drain Current (Note 4)	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0 V	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10		20	10		20	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			150			150	μmho		
9		C_{gs}	Gate-Source Capacitance			5.0			5.0	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{gd}	Drain Gate Capacitance			2.5			2.5			
11		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fs}	Common-Source Forward Transconductance		12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
13		g_{os}	Common-Source Output Conductance		0.15			0.15				
14		g_{ig}	Power-Match Source Admittance		12			12				
15		G_c	Conversion Gain (See Note 1)		3.0			3.0		dB	V_{DS} = 20 V, V_{GS} = 1/2 $V_{GS(off)}$	
16		IMD	Intercept Point (See Notes 1 and 2)		+30			+30		dBm		
17	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 3)	0.9		1.0	0.9		1.0		V_{DS} = 10 V	V_G = 0 V
18		$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	Gate-Source Cutoff Voltage Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 1 nA
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 10 mA

NOTES: NZA

1. VHF single-balanced mixer drain load impedance 2k Ω.
2. 2-tone 3rd-order IMD.
3. Assumes smaller value in numerator.
4. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

current regulator diode

designed for . . .

Performance Curves NKL
See Section 4

- **LD130 A/D Converter Interface Circuits**

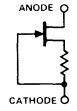
BENEFITS

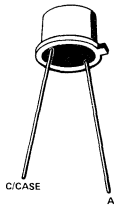
- TO-18 Package for Improved Current Control
- Low Drift with Temperature Temperature Coefficient ±0.05%/°C
- Peak Operating Voltage = 60 V

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	60 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at T_C = 25°C	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 5





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC	MIN	TYP	MAX	UNIT	TEST CONDITIONS
1	STA	I_{F1} Regulator Current (Note 1)	240		390	μA	V_F = 25 V
2	STA	V_L Limiting Voltage		0.6	1.1	V	I_F = 200 μA
3	STA	POV Peak Operating Voltage	60	100		V	I_F = 468 μA
4	STA	θ_I Temperature Coefficient		±.05		%/°C	V_F = 25 V, T_A = +25 to +125°C
5	DYN	Z_d Dynamic Impedance (Note 2)	4.1	12.0		MΩ	V_F = 25 V
6	DYN	Z_k Knee Impedance	1.0	2.5		MΩ	V_F = 6 V

NOTES:
1. Pulse Test—Steady State Current may vary.
2. Pulse Test—Steady State Impedance may vary.

NKL

3

n-channel JFET
designed for . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH
See Section 4

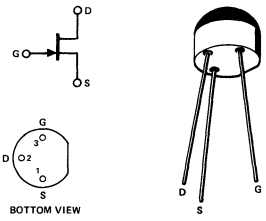
BENEFITS

- Specified for 200 MHz Operation

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 30 V
Source-Gate Voltage . . . . . 30 V
Drain-Source Voltage . . . . . 30 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation @ T_A = 25°C . . . . . 350 mW
Derate above 25°C . . . . . 3.5 mW/°C
Operating Junction Temperature Range . . . . . −55 to +125°C
Storage Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−250	pA	V_{GS} = −20 V, V_{DS} = 0	
2					−15	nA		T_A = +85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = −1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−8.0		V_{DS} = 15 V, I_D = 1 μA	
5		I_{DSS}	Saturation Drain Current	4.0	25	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6		$r_{DS(on)}$	Drain-Source ON Resistance		300	Ω	I_D = 1 mA, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500	10,000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$Re(y_{fs})$	Common-Source Forward Transconductance	4,000				f = 200 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		150			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.0			
13		NF	Noise Figure		3.0	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 200 MHz
14					5.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω, BW = 5 Hz	f = 10 Hz
15		G_{PS}	Common-Source Power Gain	15			V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz

NOTE:
1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

n-channel JFETs *designed for . . .*

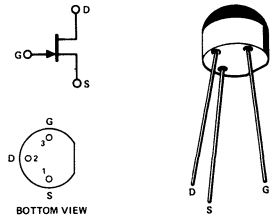
- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (U1897E)
- No Error or Offset Voltage Generated by Closed Switch
  Purely Resistive

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –40 V
Forward Gate Current . . . . . 10 mA
Total Continuous Device Dissipation
at (or Below) T_A = 25°C
(Derate 3.5 mW/°C to 125°C) . . . . . 350 mW
Storage Temperature Range . . . . . –55 to +125°C
Operating Temperature Range . . . . . –55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U1897E Min	U1897E Max	U1898E Min	U1898E Max	U1899E Min	U1899E Max	Unit	Test Conditions
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 μA, V_{DS} = 0
2		BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40			I_G = –1 μA, I_S = 0
3		BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40			I_G = –1 μA, I_D = 0
4		I_{GSS}	Gate Reverse Current		–400		–400		–400	pA	V_{GS} = –20 V, V_{DS} = 0
5		I_{DGO}	Drain-Gate Leakage Current		200		200		200		V_{DG} = 20 V, I_S = 0
6		I_{SGO}	Source-Gate Leakage Current		200		200		200		V_{SG} = 20 V, I_D = 0
7		$I_{D(off)}$	Drain Cutoff Current		200		200		200		V_{DS} = 20 V, V_{GS} = –12 V (U1897E)
8					10		10		10	nA	V_{GS} = –8 V (U1898E) / V_{GS} = –6 V (U1899E), T_A = 85°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–5.0	–10	–2.0	–7.0	–1.0	–5.0	V	V_{DS} = 20 V, I_D = 1 nA
10		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	V_{DS} = 20 V, V_{GS} = 0
11		$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	V_{GS} = 0, I_D = 6.6 mA (U1897E); I_D = 4.0 mA (U1898E), I_D = 2.5 mA (U1899E)
12		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	I_D = 1 mA, V_{GS} = 0
13	DYNAMIC	C_{DG}	Drain-Gate Capacitance		5		5		5	pF	V_{DG} = 20 V, I_S = 0
14		C_{SG}	Source-Gate Capacitance		5		5		5		V_{SG} = 20 V, I_D = 0
15		C_{iss}	Common-Source Input Capacitance		16		16		16		V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5		
17		$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions
18		t_r	Rise Time		10		20		40		
19		t_{off}	Turn OFF Time		40		60		80		

Switching Time Test Conditions	U1897E	U1898E	U1899E
V_{DD}	3 V	3 V	3 V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	–12 V	–8 V	–6 V
R_L	430 Ω	700 Ω	1100 Ω
$I_{D(on)}$	6.6 mA	4 mA	2.5 mA

NC

NOTE:
1. Pulse test pulsewidth = 300 μs; duty cycle ≤ 3%.

n-channel silicon JFET

designed for . . .

- **VHF Amplifiers**
- **Mixers**

Performance Curves NH
See Section 4

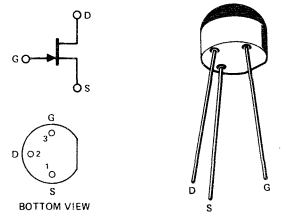
BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wideband
  High G_{fs}/C_{iss} Ratio
- Specified for Operation at 400 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −30 V
Forward Gate Current . . . . . 10 mA
Total Continuous Device Dissipation
at (or Below) T_A = 25°C
(Derate 3.5 mW/°C to 125°C) . . . . . 350 mW
Storage Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−100	pA	V_{GS} = −20 V, V_{DS} = 0	
2					−10	nA		T_A = 100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = −1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−6	V	V_{DS} = 15 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	−1.0	−5.5	V	V_{DS} = 15 V, I_D = 500 μA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		50	μmho		
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1	pF		f = 1 MHz
10		C_{iss}	Common-Source Input Capacitance		4	pF		
11		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
12	HI FREQ	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
13		b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
14		g_{oss}	Common-Source Output Conductance		75		100	μmho	
15		b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
16		g_{fs}	Common-Source Forward Transconductance (Note 1)			4000		μmho	
17		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
18		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

NOTE: NH

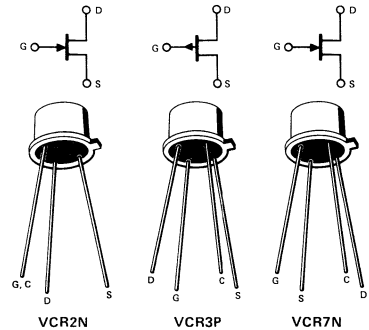
1. Pulse test duration = 300 μs.

voltage-controlled resistor FETs *designed for . . .*

Performance Curves NC NP NT PC PE See Section 4

- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**

TO-18 See Section 5 | TO-72 See Section 5



VCR2N VCR4N | VCR3P VCR5P | VCR7N

ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 15 V
Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

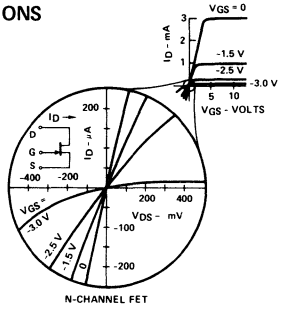
N-Channel VCR FETs

		Characteristic		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5	V	I_D = 1 μA, V_{DS} = 10 V	
4	STATIC	$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		7.5		3		1.5	pF	V_{GS} = -10 V, I_D = 0	f = 1 MHz
				NC		NP		NT				

P-Channel VCR FETs

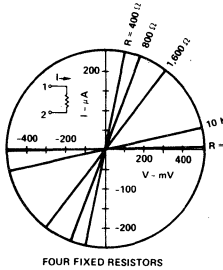
				VCR3P		VCR5P			
1	STATIC	I_{GSS}	Gate Reverse Current		20		10	nA	V_{GS} = 15 V, V_{DS} = 0
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	15		15		V	I_G = 1 μA, V_{DS} = 0
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7	3.5	7	V	I_D = -1 μA, V_{DS} = -10 V
4	STATIC	$r_{ds(on)}$	Drain-Source ON Resistance	70	200	300	900	Ω	V_{GS} = 0, I_D = 0 f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		6		3	pF	V_{GD} = 10 V, I_S = 0 f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		6		3	pF	V_{GS} = 10 V, I_D = 0 f = 1 MHz
				PE		PC			

APPLICATIONS



N-CHANNEL FET

N-Channel JFET Output Characteristic Enlarged Around V_{DS} = 0
Figure 1



FOUR FIXED RESISTORS

V-I Characteristic of Four Fixed Resistors
Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around V_{DS} = 0, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when V_{GS} = 0 and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around V_{DS} = 0. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at I_D/I_{DSS} = 0.001. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at $V_{DS} = V_{GS} = 0$) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

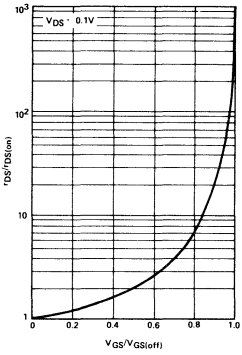


Fig. 3

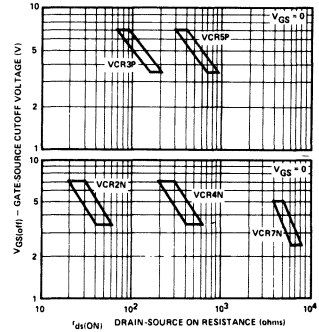


Fig. 4

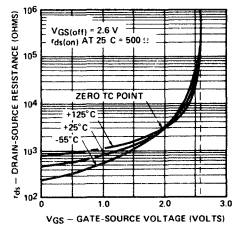


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

n-channel JFETs *designed for . . .*

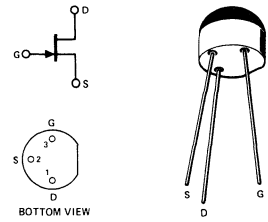
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NH
See Section 4

BENEFITS

- Selected I_{DSS} and V_{GS} Ranges
- Low C_{rss} 0.75 pF Typical
- High Y_{fs}/C_{iss} Ratio
- High Dynamic Range Greater than 100 dB

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 30 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate at 2.5 mW/°C) . . . . 350 mW
Operating Temperature . . . . . −65 to +125°C
Storage Temperature . . . . . −65 to +125°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		Min	Typ	Max	Units	Test Conditions
1		I_{GSS} Gate Reverse Current				−5	nA	V_{GS} = −20 V, V_{DS} = 0
2		BV_{GSS} Gate-Source Breakdown Voltage		−30			V	I_G = −1 μA, V_{DS} = 0
3		$V_{GS(off)}$ Gate-Source Cutoff Voltage		−0.5		−8	V	V_{DS} = 15 V, I_D = 10 μA
4	STATIC	I_{DSS} Saturation Drain Current (Note 1)		2		25	mA	V_{DS} = 15 V, V_{GS} = 0
5		I_{DSS} Saturation Drain Current (Note 1)	W245A	2		6.5	mA	V_{DS} = 15 V, V_{GS} = 0
6			W245B	6		15	mA	
7			W245C	12		25	mA	
8		V_{GS} Gate-Source Voltage (Note 1)	W245A	−0.4		−2.2	V	I_D = 200 μA, V_{DG} = 15 V
9			W245B	−1.6		−3.8	V	
10			W245C	−3.2		−7.5	V	
11		g_{fs} Common-Source Forward Transconductance		3	5.5	6.5	mmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz
12	DYN	C_{rss} Common-Source Reverse Transfer Capacitance			0.75		pF	V_{DS} = 20 V, V_{GS} = −1 V, f = 1 MHz
13		C_{iss} Common-Source Input Capacitance			3.5		pF	V_{DS} = 20 V, V_{GS} = −1 V, f = 1 MHz
14		C_{oss} Output Capacitance			1.6		pF	V_{DS} = 20 V, V_{GS} = −1 V, f = 1 MHz

NOTE:
1. Pulse test PW ≤ 300 μs, duty cycle ≤ 2%.

NH

n-channel JFETs *designed for . . .*

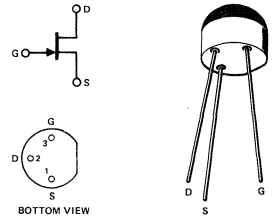
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZF See Section 4

BENEFITS

- High Power Gain
  20–23 dB Typical at 100 MHz, Common-Source
  17.5–20.5 dB Typical at 100 MHz, Common-Gate
- Low Noise Figure
  1.3 dB Typical at 100 MHz
- High Dynamic Range
  Greater than 100 dB
- Selected I_{DSS} and $V_{GS(off)}$ ranges

TO-106
See Section 5



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate at 2.5 mW/°C) . . . . 250 mW
Operating Temperature . . . . . −65 to +125°C
Storage Temperature . . . . . −65 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .260°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.5	nA	V_{GS} = −15 V, V_{DS} = 0	
2					−0.1	μA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	I_G = −1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 1)	−1.5	−7.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1, 2)	4	45	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	9000	μmho	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	
7		g_{os}	Common-Source Output Conductance		200			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.7	pF	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	
9		C_{iss}	Common-Source Input Capacitance		5.5			

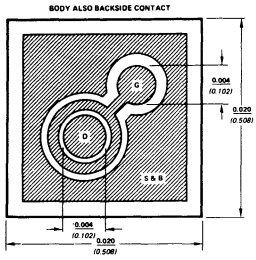
Characteristic		W300		W300A		W300B		W300C		W300D		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
I_{DSS} (Note 2)	Saturation Drain Current	4.0	45	4	9	7	15	12	25	21	45	mA	V_{DS} = 10 V, V_{GS} = 0
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.5	−7.0	−1.5	−3.0	−2.0	−4.0	−2.5	−5.0	−3.5	−7.0	V	V_{DS} = 10 V, I_D = 1 nA

NOTES:
1. I_{DSS} and $V_{GSS(off)}$ are selected into 5 ranges and labeled according to above table.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NZF

geometry characteristics

index 4



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

depletion-type n-channel MOSFET

designed for . . .

- High and Low Frequency Amplifiers
- Ultra-High Input Impedance Amplifiers for Such Circuits as:
  - Proximity Detectors
  - Smoke Detectors
  - Transducer Amplifiers
  - pH Detectors

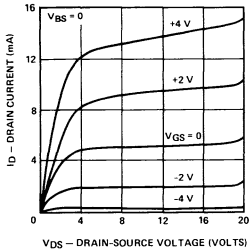
BENEFITS:

- No Gate Protective Diode Which Results in Ultra-High Input Impedance
- Ultra-Low Gate Leakage
- Normally ON

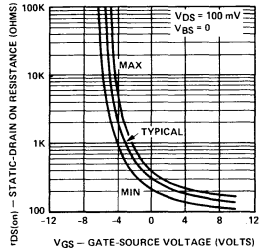
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3631, M100, M101
Single	Chip	2N3631CHP, M100CHP, M101CHP

PERFORMANCE CURVES (25°C and V_{BS} = 0 unless otherwise noted)

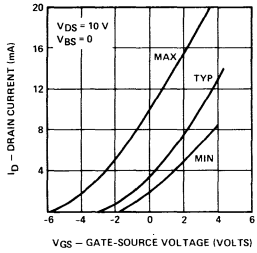
Output Characteristics



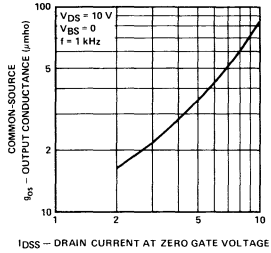
Drain-Source Static Resistance vs Gate-Source Bias



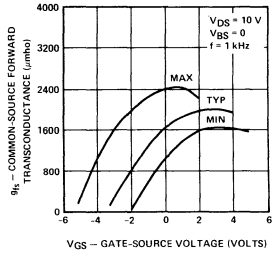
Transfer Characteristics

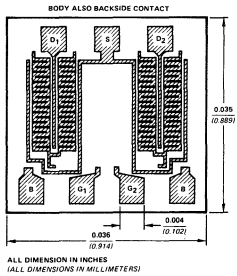


Output Conductance



Forward Transconductance vs Gate-Source Voltage





ALL DIMENSION IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

dual enhancement-type p-channel MOSFET
designed for . . .

- Operational Amplifiers
- Audio Amplifiers
- Commutating Circuits
- Multiplexer Circuits
- Analog Switches

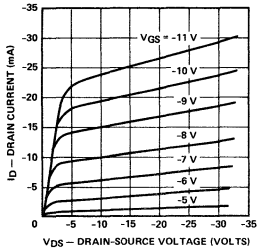
BENEFITS:

- Common Sources
- Integrated Zener Clamp Protects the Gates
- Low I_{GSS}
- Normally OFF

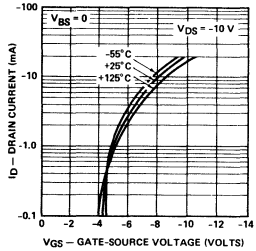
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-89	M106
Dual	Chip	M106CHP

PERFORMANCE CURVES (25°C and V_{BS} = 0 unless otherwise noted)

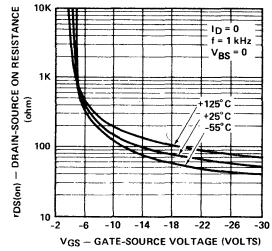
Output Characteristic



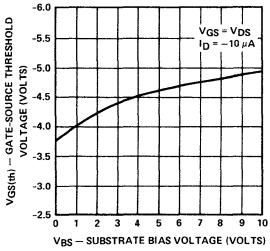
Transfer Characteristics



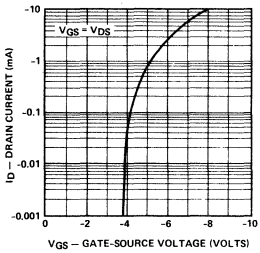
Drain-Source ON Resistance vs Gate-Source Bias



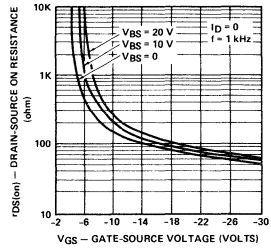
Gate Threshold Voltage vs Substrate Bias Voltage



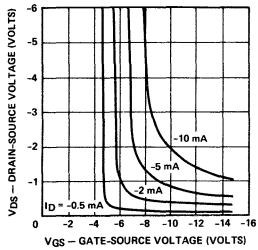
Gate-Source Voltage vs Drain Current



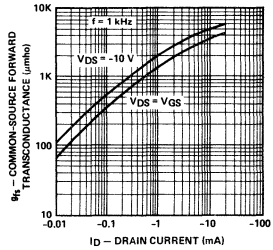
Drain-Source ON Resistance vs Gate-Source Bias

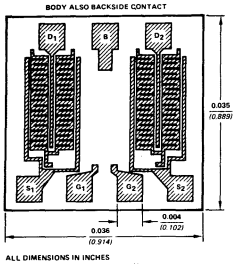


Low Level ON Drain-Source Voltage vs Gate-Source Bias



Transconductance Characteristics





dual enhancement-type p-channel MOSFET

designed for . . .

- Audio Amplifiers
- Operational Amplifiers
- Commutating Circuits
- Multiplexer Circuits
- Analog Switches

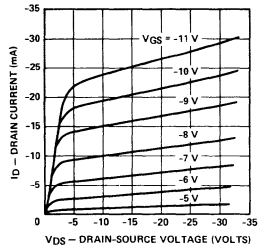
BENEFITS:

- Integrated Zener Clamp Protects the Gates
- Low I_{GSS}
- Normally OFF

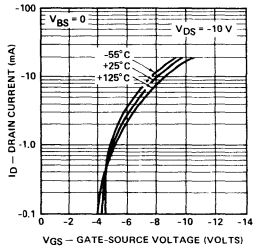
TYPE	PACKAGE	PRINCIPAL DEVICE
Dual	TO-99	M107
Dual	Chip	M107CHP

PERFORMANCE CURVES (25°C and V_{BS} = 0 unless otherwise noted)

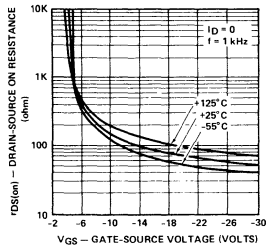
Output Characteristics



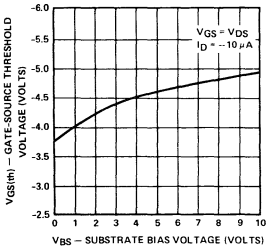
Transfer Characteristics



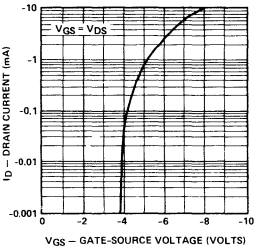
Drain-Source ON Resistance vs Gate-Source Bias



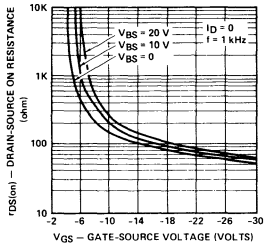
Gate Threshold Voltage vs Substrate Bias Voltage



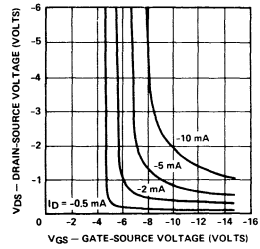
Gate-Source Voltage vs Drain Current



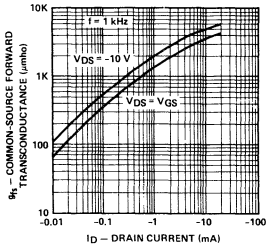
Drain-Source ON Resistance vs Gate-Source Bias

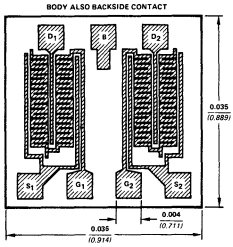


Low Level ON Drain-Source Voltage vs Gate-Source Bias



Transconductance Characteristics





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

dual enhancement-type p-channel MOSFET

designed for . . .

- Operational Amplifiers
- Ultra-High Input Impedance
  - Proximity Detector Amplifiers
  - Smoke Detector
  - pH Detectors
  - Electrometers
- Multiplexer Circuits
- Analog Switches

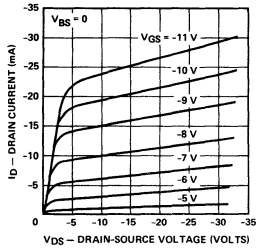
BENEFITS:

- No Gate Protection Results in Ultra-High Input Impedance
- Ultra-Low Leakage
- Normally OFF

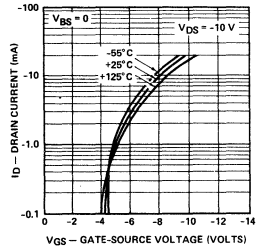
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-99	M108
Dual	Chip	M108CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

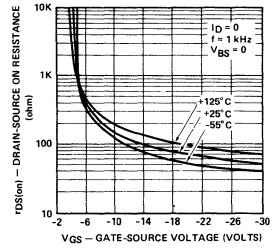
Transfer Characteristics



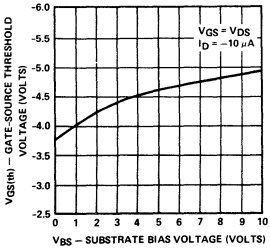
Transfer Characteristics



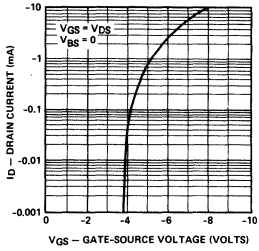
Drain-Source ON Resistance vs Gate-Source Bias



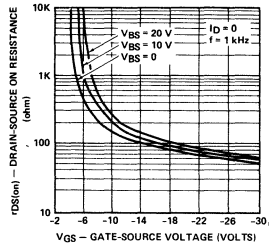
Gate-Source Voltage vs Substrate Bias



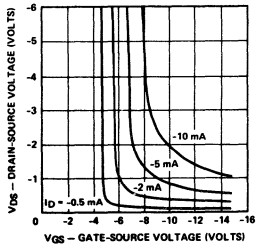
Gate-Source Voltage vs Drain Current



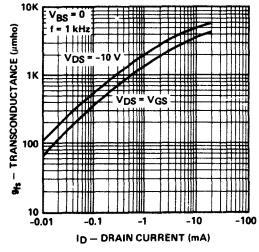
Drain-Source ON Resistance vs Gate-Source Bias

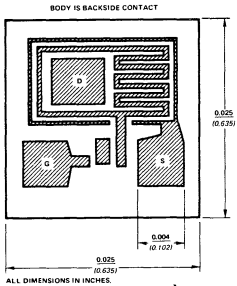


Low-Level ON Drain-Source Voltage vs Gate-Source Bias



Transconductance Characteristics





enhancement-type p-channel MOSFET *designed for . . .*

- Audio and RF Amplifiers
- Analog Switches
- Logic Circuits
- Multiplexers

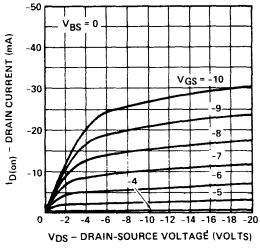
BENEFITS:

- $10^{10}\Omega$ Input Resistance
- Integrated Zener Clamp Protects the Gate
- Source Law Transfer Characteristics
- Normally OFF
- Low $I_{D(off)}$ and $I_{S(off)}$

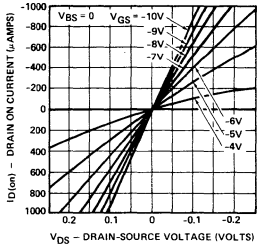
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	MEM511C, M103
Single	Chip	MEM511CCHP, M103CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

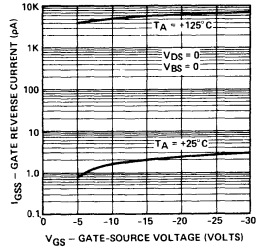
Output Characteristic



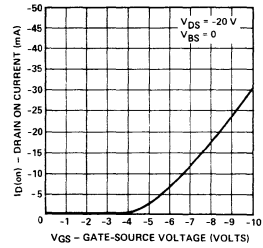
Low Voltage Output Characteristics



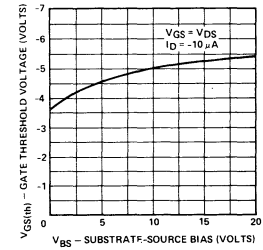
Gate Leakage Current vs Gate-Source Bias



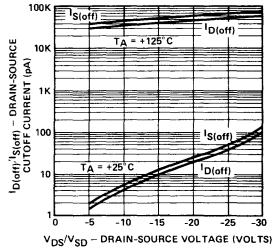
Transfer Characteristic



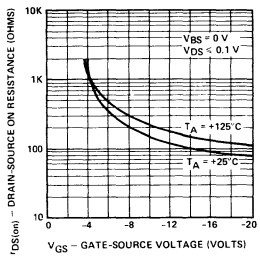
Gate Threshold Voltage vs Substrate Bias



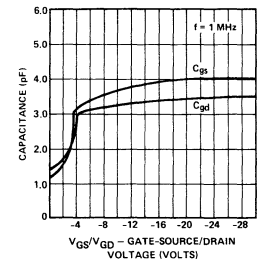
Source-Drain Leakage Currents vs Voltage



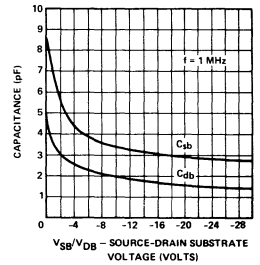
Drain-Source ON State Resistance vs Gate-Source Bias

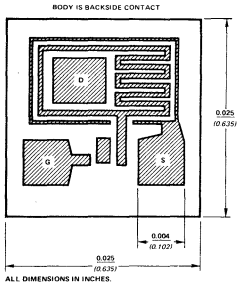


Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage





enhancement-type p-channel MOSFET *designed for . . .*

- Analog and Digital Switching

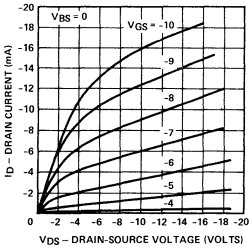
BENEFITS:

- Integrated Zener Clamp Protects the Gate
- Low $I_{D(off)}/I_{S(off)}$
- High Breakdown Voltage
- Low Leakage
- Normally OFF

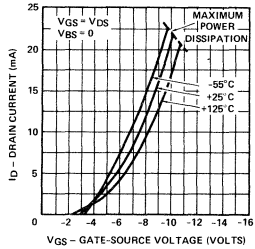
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	M114
Single	Chip	M114CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

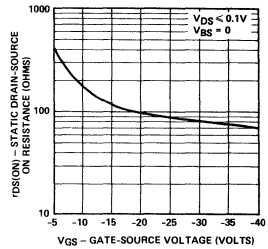
Output Characteristic



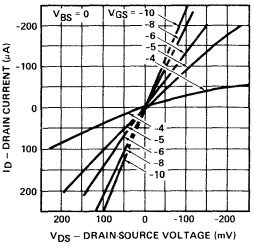
Transfer Characteristics



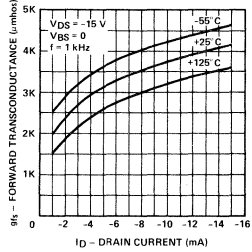
Drain-Source ON State Resistance vs Gate-Source Bias



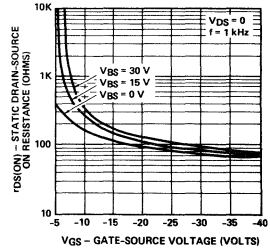
Low Voltage Output Characteristics



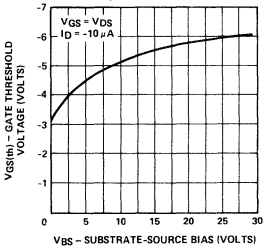
Forward Transconductance vs Drain Current



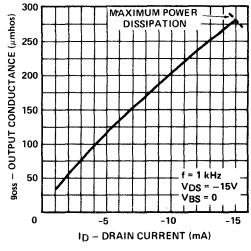
Drain-Source ON State Resistance vs Gate-Source Bias



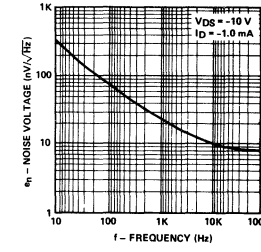
Gate-Threshold Voltage vs Substrate Bias



Output Conductance vs Drain Current

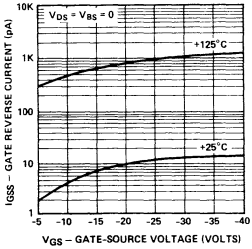


Short Circuit Equivalent Input Noise Voltage vs Frequency

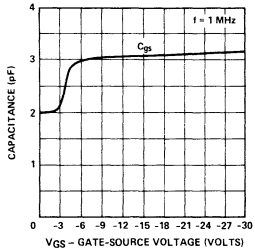


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

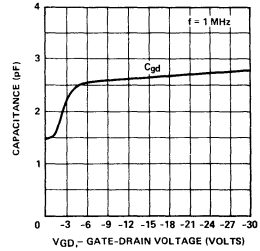
Gate Leakage Current vs Gate-Source Bias



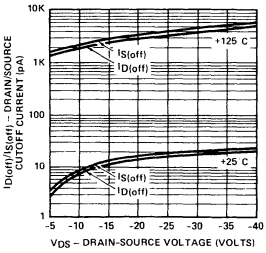
Gate-Source Capacitance vs Gate-Source Bias



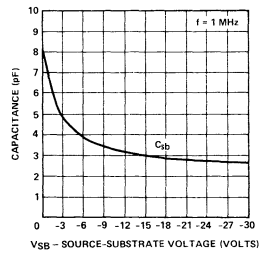
Gate-Drain Capacitance vs Voltage



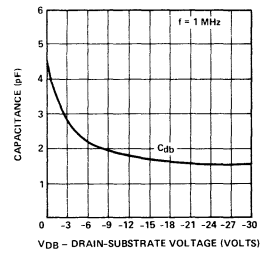
Source-Drain Leakage Currents vs Voltage

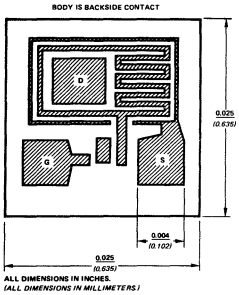


Substrate Capacitance vs Voltage



Substrate Capacitance vs Voltage





enhancement-type p-channel MOSFET *designed for . . .*

- Analog and Switching Circuits
- Audio Amplifiers

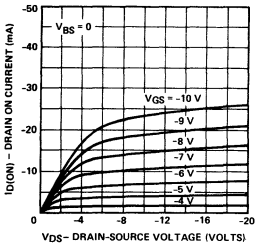
BENEFITS:

- Integrated Zener Clamp Protects the Gate
- Low $V_{GS(th)}$
- Normally OFF

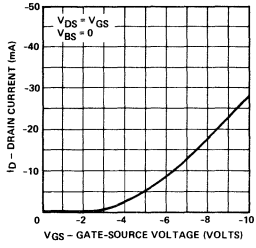
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	M113
Single	Chip	M113CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

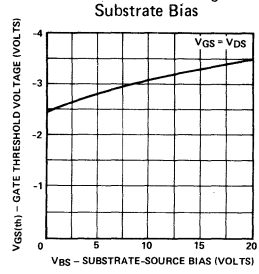
Output Characteristics



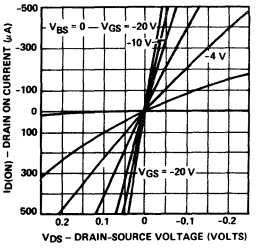
Transfer Characteristic



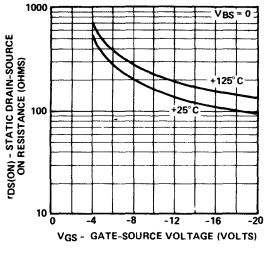
Gate-Threshold Voltage vs Substrate Bias



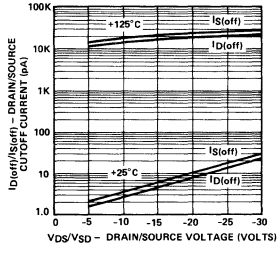
Low Voltage Output Characteristics



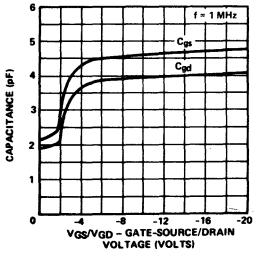
Drain-Source ON-State Resistance vs Gate-Source Bias



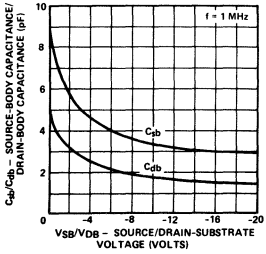
Leakage Currents vs Voltage



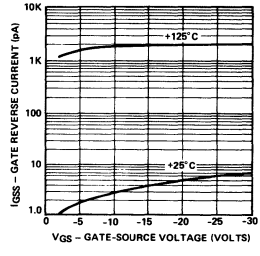
Gate Capacitance vs Voltage

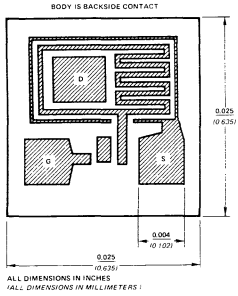


Substrate Capacitance vs Voltage



Gate Leakage Current vs Gate-Source Bias





enhancement-type n-channel MOSFET

designed for . . .

- Audio Amplifiers
- Analog Circuits
- Digital Switching Circuits
- Commutating Circuits

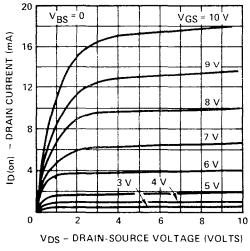
BENEFITS:

- Integrated Zener Clamp Protects the Gate
- Normally OFF

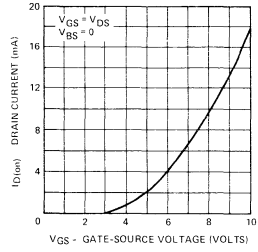
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	M116
Single	Chip	M116CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

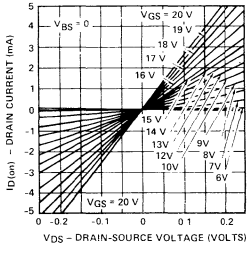
Output Characteristics



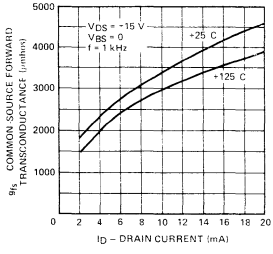
Transfer Characteristic



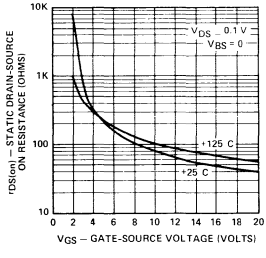
Low Voltage Output Characteristics



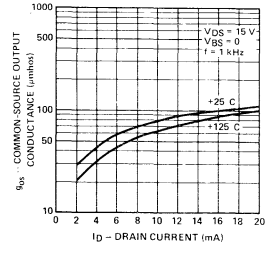
Forward Transconductance vs Drain Current



Drain-Source ON State Resistance vs Gate-Source Bias

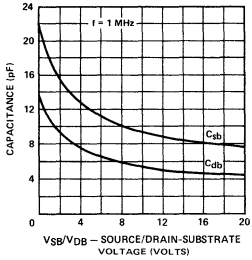


Output Conductance vs Drain Current

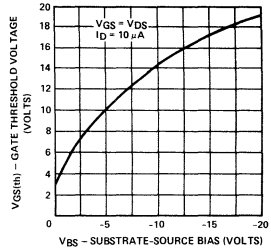


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

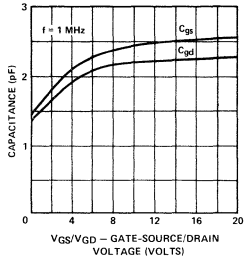
Substrate Capacitance vs Voltage



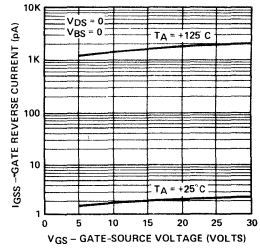
Gate Threshold Voltage vs Substrate Bias



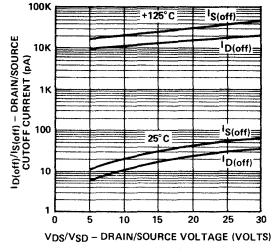
Gate Capacitance vs Voltage

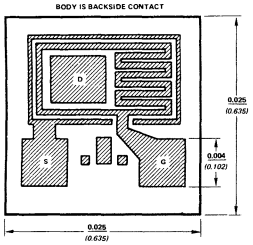


Gate Leakage Current vs Gate-Source Bias



Source-Drain Leakage Currents vs Voltage





ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

enhancement-type n-channel MOSFET

designed for . . .

- Audio Amplifiers
- Analog Circuits
- Digital Switching Circuits
- Commutating Circuits

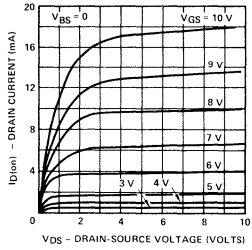
BENEFITS:

- Ultra-Low Gate Leakage
- Normally OFF

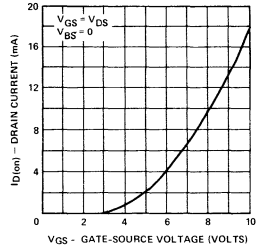
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	M117
Single	Chip	M117CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

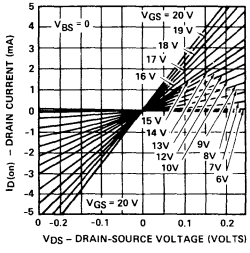
Output Characteristics



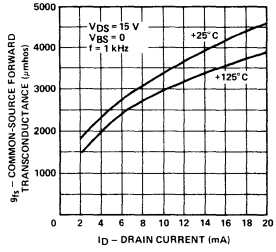
Transfer Characteristic



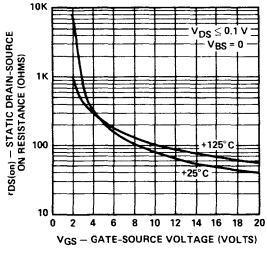
Low Voltage Output Characteristics



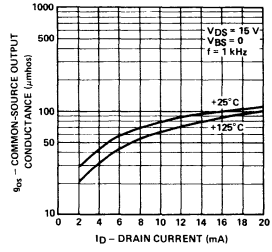
Forward Transconductance vs Drain Current



Drain-Source ON State Resistance vs Gate-Source Bias

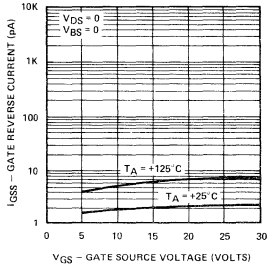


Output Conductance vs Drain Current

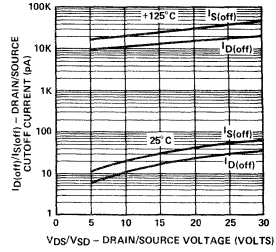


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

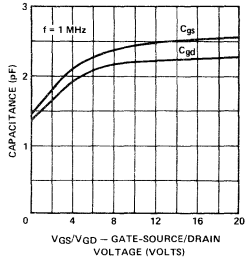
Gate Leakage Current vs Gate-Source Bias



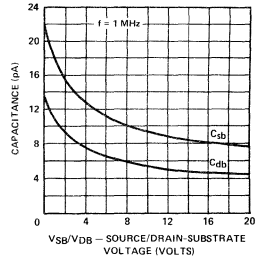
Source-Drain Leakage Currents vs Voltage



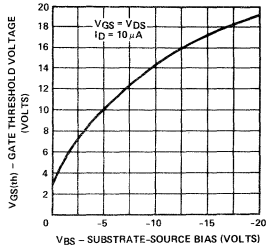
Gate Capacitance vs Voltage

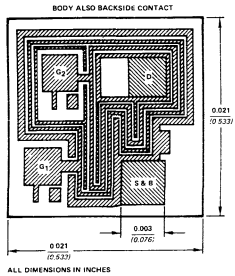


Substrate Capacitance vs Voltage



Gate Threshold Voltage vs Substrate Bias





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

depletion-type n-channel MOSFET

designed for . . .

- VHF Amplifiers
- Mixers
- IF Amplifiers

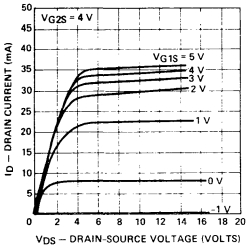
BENEFITS

- High Gain
  g_{fs} Typically 12 mmhos
- No Neutralization Required
  Low $C_{rss} < 0.03$ pF
- Automatic Gain Control with Second Gate

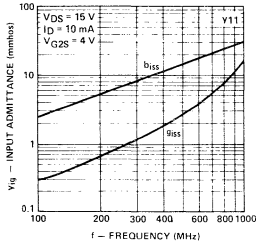
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	3N187, 3N201-3
Single	OD-84	BF900
Single	Chip	3N187CHP, 3N201CHP-3CHP, BF900CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

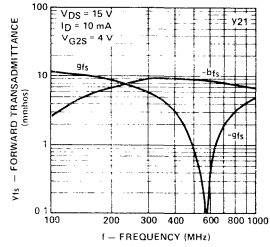
Output Characteristics



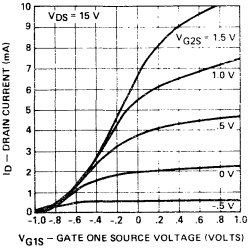
Common-Source Input Admittance vs Frequency



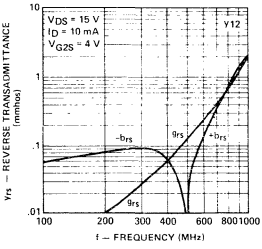
Common-Source Forward Transadmittance vs Frequency



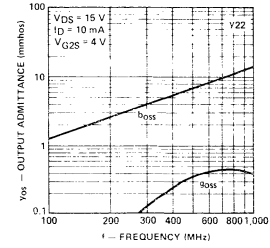
Transfer Characteristics



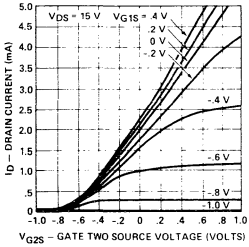
Common-Source Reverse Transadmittance vs Frequency



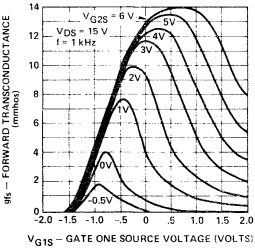
Common-Source Output Admittance vs Frequency



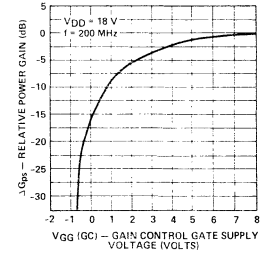
Transfer Characteristics



Forward Transconductance vs Gate One-Source Voltage



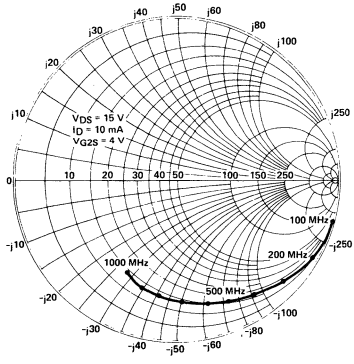
Relative Power Gain vs Gain Control Gate-Supply Voltage



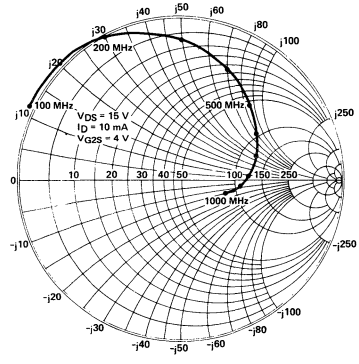
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

S Parameters (Plotted on 50 ohm Smith Chart)

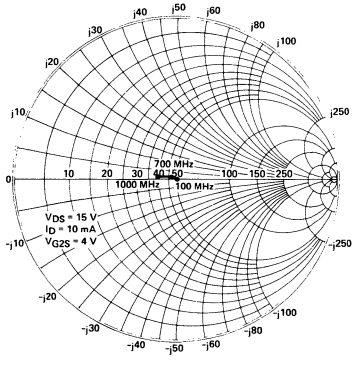
s11



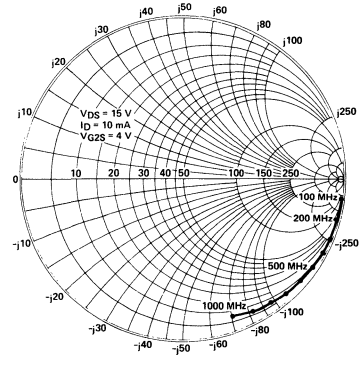
s21

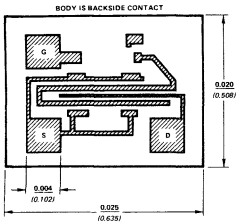


s12



s22





enhancement-type p-channel MOSFET

designed for . . .

- Audio and RF Amplifiers
- Analog Switches
- Logic Circuits
- Multiplexers

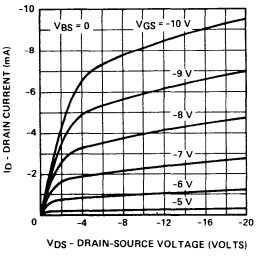
BENEFITS:

- 10^{10} Ω Input Resistance
- Integrated Zener Clamp Protects the Gate
- Square Low Transfer Characteristics
- Normally OFF

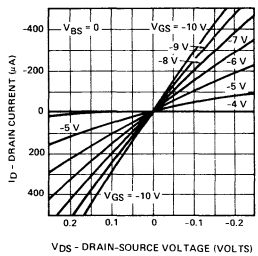
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	MEM511
Single	Chip	MEM511CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

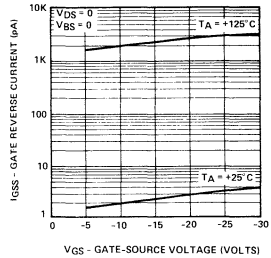
Output Characteristics



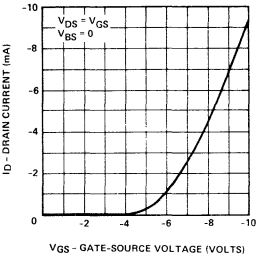
Low Voltage Output Characteristics



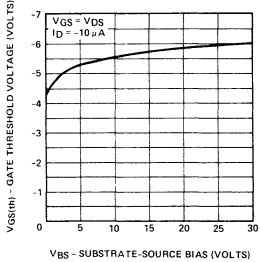
Gate Leakage Current vs Gate-Source Bias



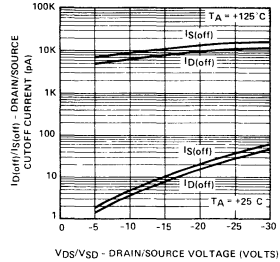
Transfer Characteristic



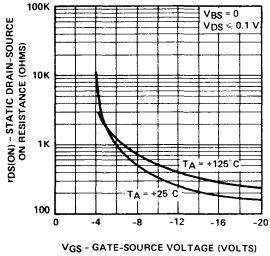
Gate Threshold Voltage vs Substrate Bias



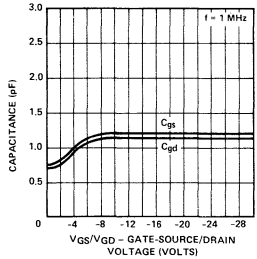
Source-Drain Leakage Currents vs Voltage



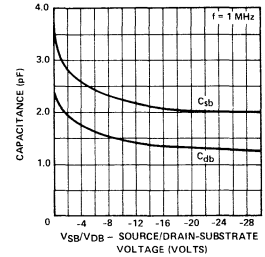
Drain-Source ON State Resistance vs Gate-Source Bias

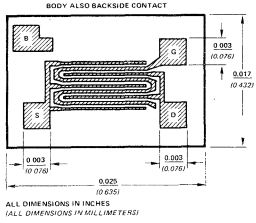


Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage





enhancement-type p-channel MOSFET *designed for . . .*

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

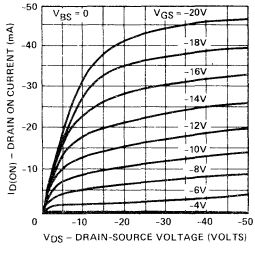
BENEFITS:

- **High Gate Transient Voltage Breakdown Eliminates Need for Gate Protective Diode**
- **Ultra-High Input Impedance**
- **Low Leakage**
- **Normally OFF**

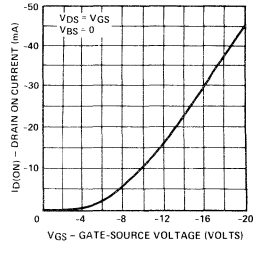
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	MFE823
Single	TO-72	3N163-64
Single	Chip	3N163-64CHP, MFE823CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

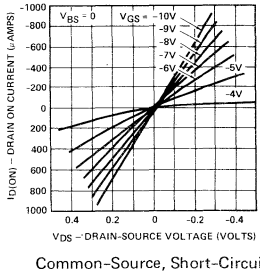
Output Characteristics



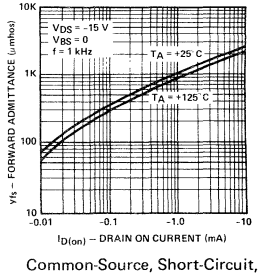
Transfer Characteristic



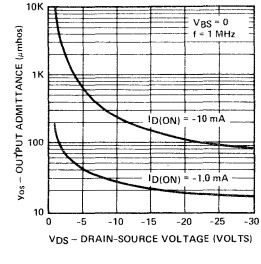
Low-Level Output Characteristics



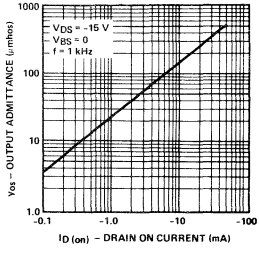
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

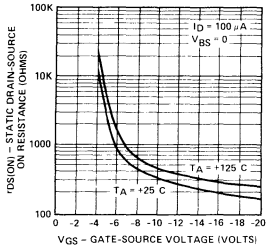


Common-Source, Short-Circuit, Output Admittance vs Drain Current

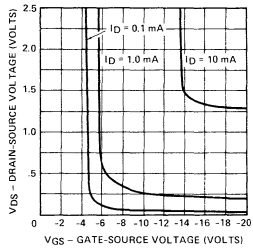


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

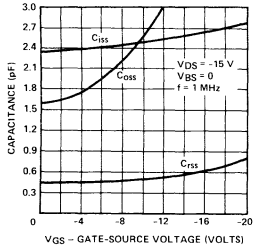
Drain-Source ON Resistance vs Gate-Source Voltage



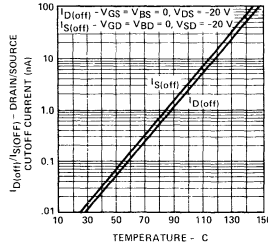
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage

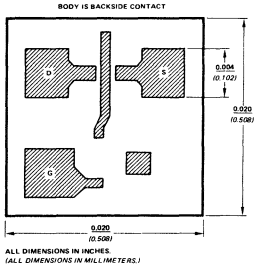


Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature





enhancement-type p-channel MOSFET *designed for . . .*

- Analog and Switching Circuits

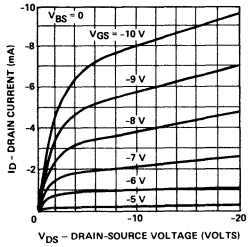
BENEFITS:

- Integrated Zener Clamp Protects the Gate
- C_{gs} Less Than 0.5 pF
- Very Low $I_{D(off)}$ and $I_{S(off)}$
- Normally OFF

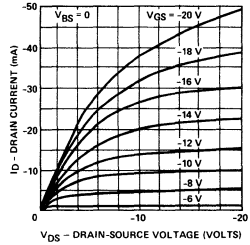
TYPE	PACKAGE	PRINCIPAL DEVICE
Single	TO-72	M104
Single	Chip	M104CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

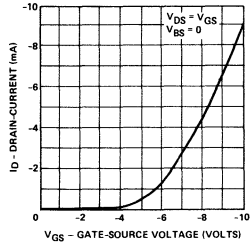
Output Characteristic



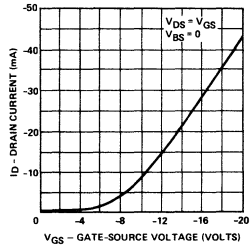
Output Characteristic



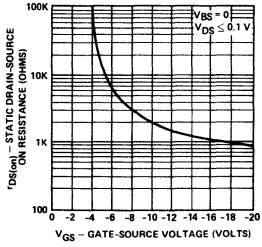
Transfer Characteristic



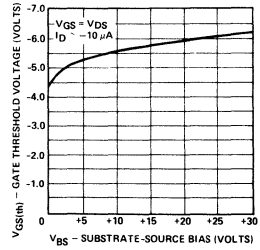
Transfer Characteristic



Drain-Source ON Resistance vs Gate-Source Bias

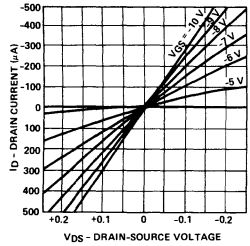


Gate Threshold Voltage vs Substrate Bias

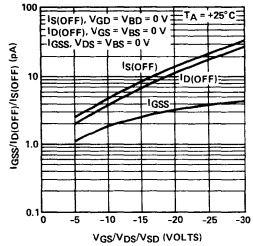


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

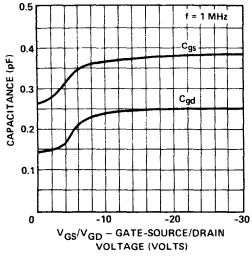
Low Voltage Output Characteristics



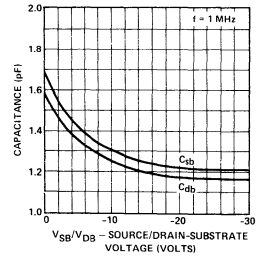
Leakage Currents vs Voltage



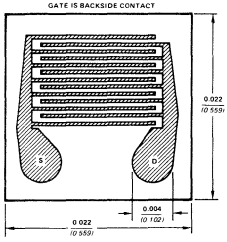
Gate Capacitance vs Voltage



Substrate Capacitance vs Voltage



NC



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFETs
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

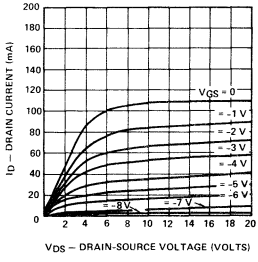
BENEFITS:

- **No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance From Driver**
- **High Off-Isolation $I_{D(off)} < 100$ pA**
- **High Speed $t_{ON} < 20$ ns**

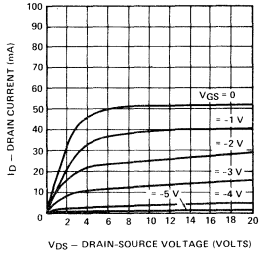
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3970-72, 2N4091-93, 2N4391-93, 2N4856-61, 2N4856A-61A, U200-02, VCR2N
Dual	TO-71	2N5564-66
Single	TO-92	2N5638-40, 2N5653-54, J111-13
Single	TO-106	E111-13, KE4391-93, U1897E-99E
Single	Chip	All of the above single devices
Dual	Chip	2N5566CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

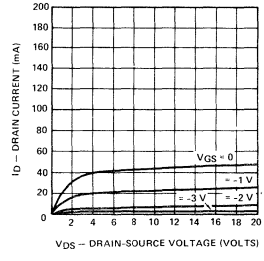
Output Characterstic



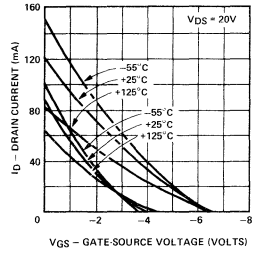
Output Characteristic



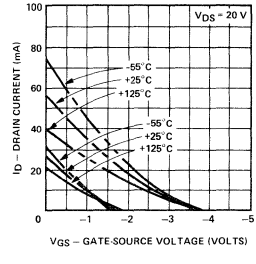
Output Characteristic



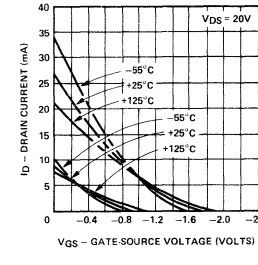
Transfer Characteristics



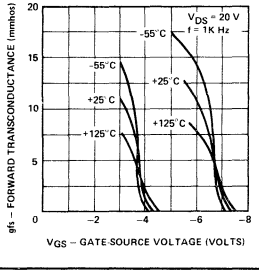
Transfer Characteristics



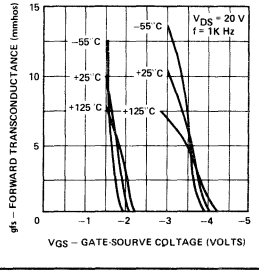
Transfer Characteristics



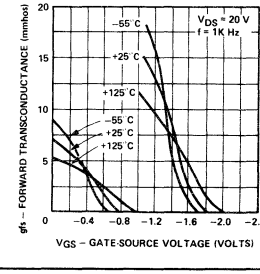
Transconductance Characteristics



Transconductance Characteristics

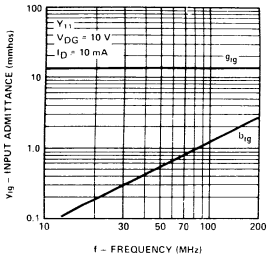


Transconductance Characteristics

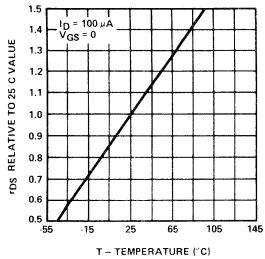


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

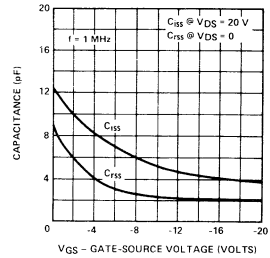
Common-Gate Input Admittance vs Frequency



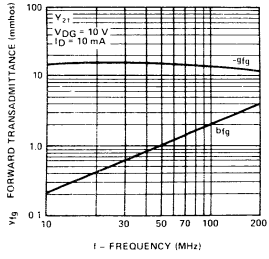
ON Resistance vs Ambient Temperature



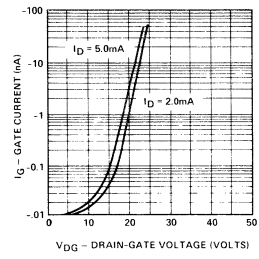
Common-Source Capacitances vs Gate-Source Voltage



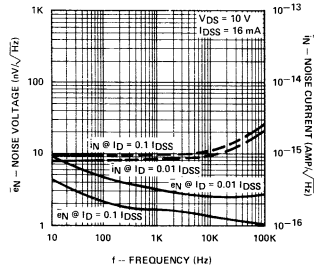
Common-Gate Forward Transadmittance vs Frequency



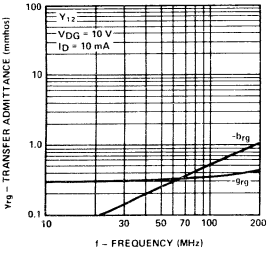
Gate Operating Current vs Drain-Gate Voltage



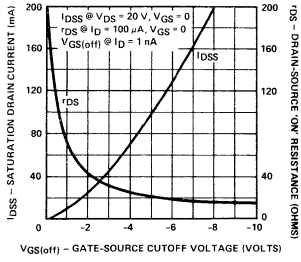
Equivalent Input Noise Voltage and Noise Current vs Frequency



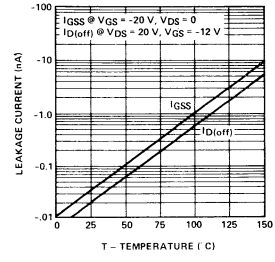
Common-Gate Reverse Transfer Admittance vs Frequency



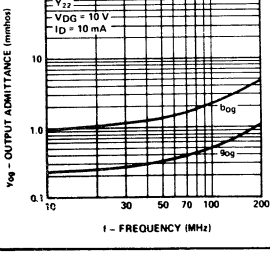
Drain Current & ON Resistance vs Gate-Source Cutoff Voltage



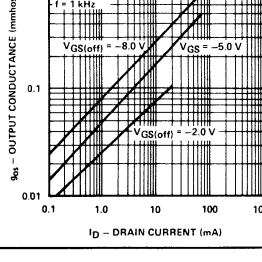
Leakage Current vs Ambient Temperature

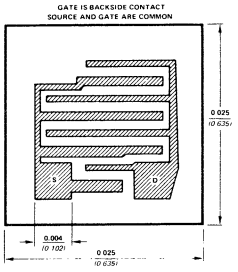


Common-Gate Output Admittance vs Frequency



Common-Source Output Conductance vs Drain Current





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing

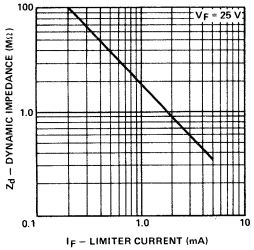
BENEFITS:

- Simple Two Lead Current Source
- Simplifies Floating Current Sources
  No Power Supplies Required
- Low Cost

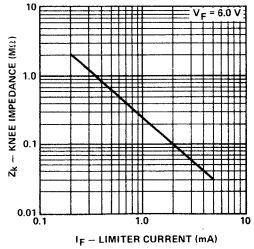
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-106	E500-507
Single	Chip	E500CHP-507CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

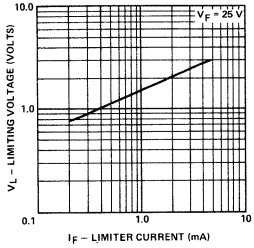
Dynamic Impedance vs Limiter Current



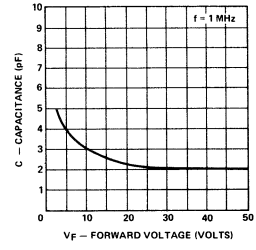
Knee Impedance vs Limiter Current



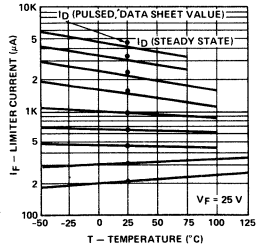
Limiting Voltage at 0.9 I_D vs Limiter Current

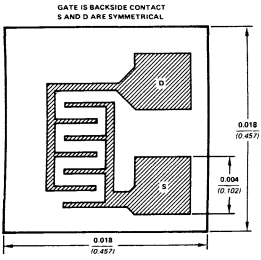


Capacitance vs Forward Voltage



Typical Variation of I_D with Temperature
Steady State and Pulsed Value





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

- Low and Medium Frequency Single and Differential Amplifiers
- High Input Impedance Amplifiers

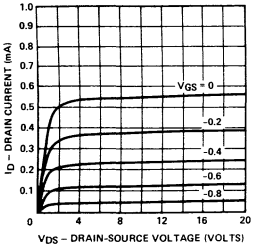
BENEFITS:

- Wide Dynamic Range
  I_G Specified @ V_{DG} = 20 V
- Low Capacitance $C_{iss} < 4$ pF
- Low Output Conductance

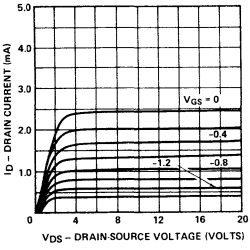
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3684-7
Single	Chip	2N3684CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

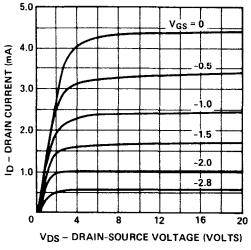
Output Characteristic



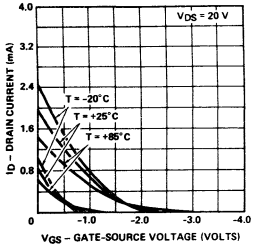
Output Characteristic



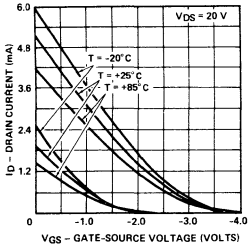
Output Characteristic



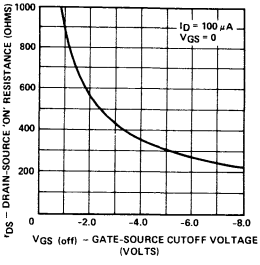
Transfer Characteristics



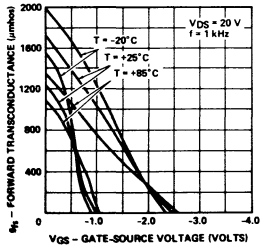
Transfer Characteristics



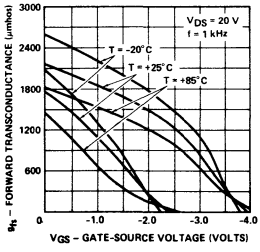
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



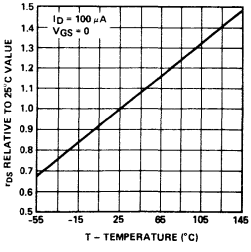
Transconductance Characteristics



Transconductance Characteristics

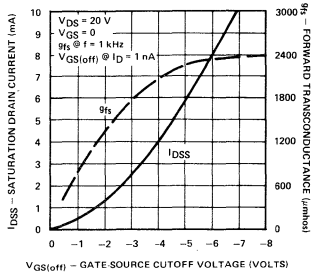


'ON' Resistance vs Ambient Temperature

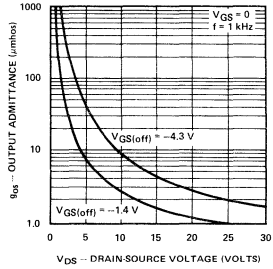


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

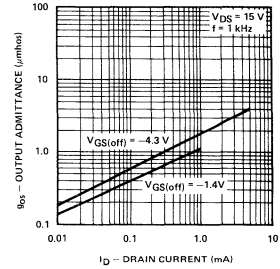
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



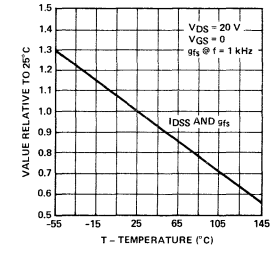
Common-Source Output Conductance vs Drain-Source Voltage



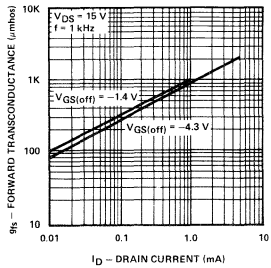
Common-Source Output Conductance vs Drain Current



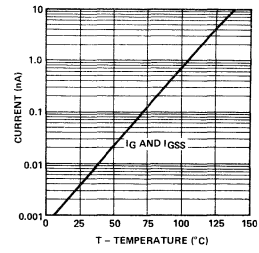
Drain Current and Transconductance vs Ambient Temperature



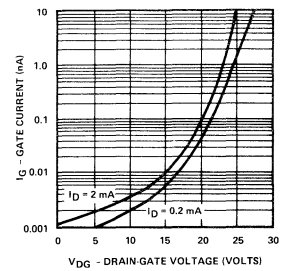
Common-Source Forward Transconductance vs Drain Current



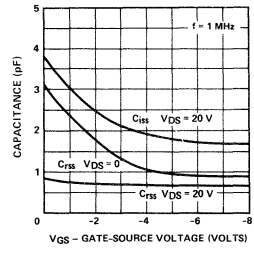
Leakage Currents vs Ambient Temperature



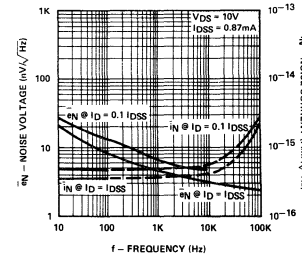
Gate Operating Current vs Drain-Gate Voltage

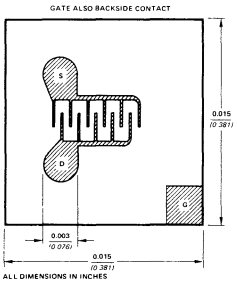


Common-Source Input Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency





n-channel JFET
designed for . . .

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

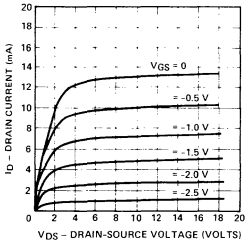
BENEFITS:

- **Low Noise**
  NF = 3 dB Typical @ 400 MHz
- **Wideband**
  High g_{fs}/C_{iss} Ratio

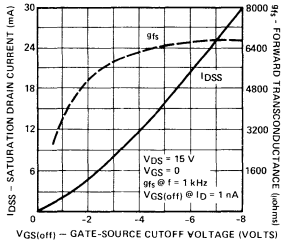
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3966, 2N4416-16A
Single	TO-92	2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108, MPF112
Single	TO-106	E304-5, KE4416, U1837E, U1994E
Single	OD-81	2N4417
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

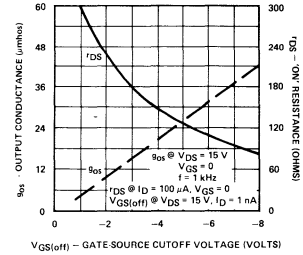
Output Characteristic



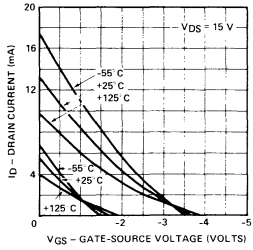
Drain Current & Transconductance vs Gate-Source Voltage



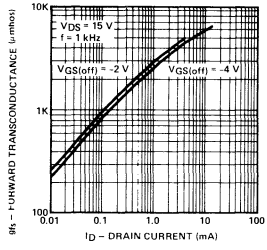
'ON' Resistance & Output Conductance vs Gate-Source Cutoff Voltage



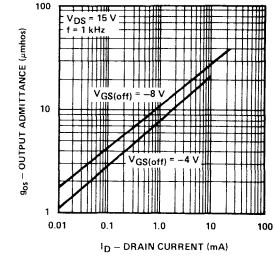
Transfer Characteristics



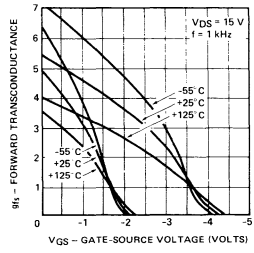
Common-Source Forward Transconductance vs Drain Current



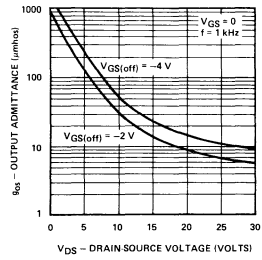
Common-Source Output Conductance vs Drain Current



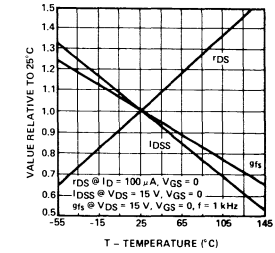
Transconductance Characteristics



Common-Source Output Conductance vs Drain-Source Voltage

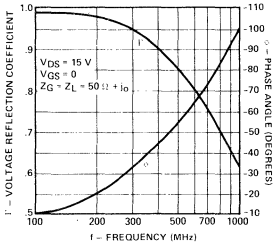


Drain Current, Transconductance and 'ON' Resistance vs Ambient Temperature

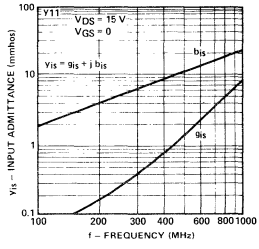


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

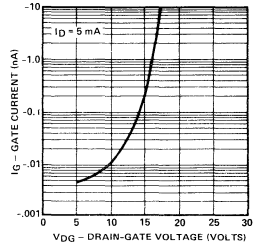
S Parameters S_{11} Common-Source vs Frequency



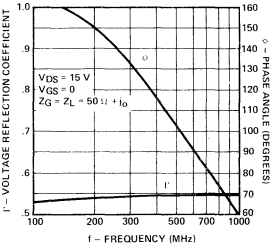
Common-Source Input Admittance vs Frequency



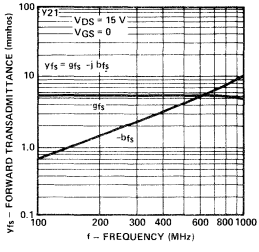
Gate Operating Current vs Drain-Gate Voltage



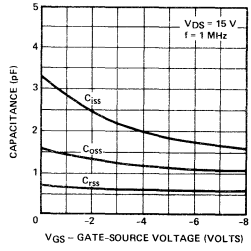
S Parameters S_{21} Common-Source vs Frequency



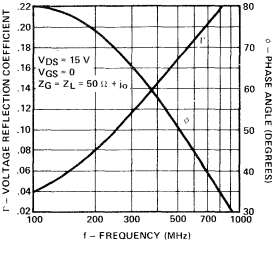
Common-Source Forward Transadmittance vs Frequency



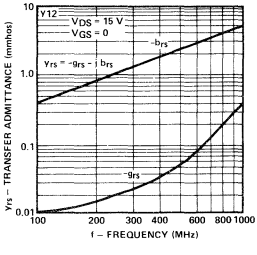
Common-Source Capacitances vs Gate-Source Voltage



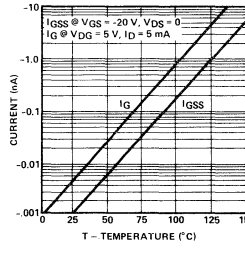
S Parameters S_{12} Common-Source vs Frequency



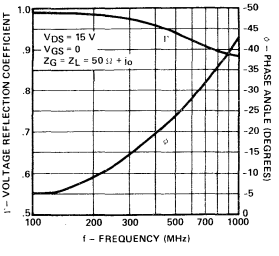
Common-Source Reverse Transfer Admittance vs Frequency



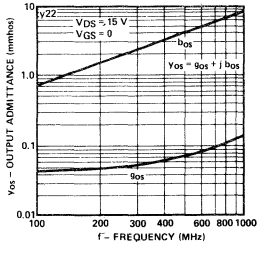
Gate Current vs Ambient Temperature



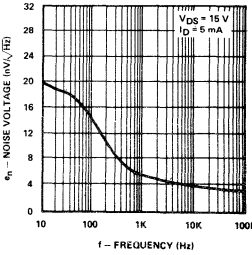
S Parameters S_{22} Common-Source vs Frequency

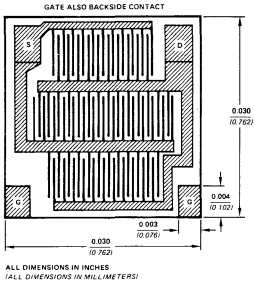


Common-Source Output Admittance vs Frequency



Equivalent Input Noise Voltage vs Frequency





n-channel JFET

designed for . . .

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

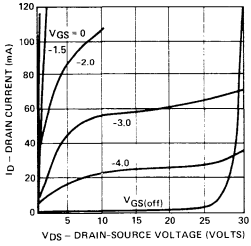
BENEFITS:

- Low Insertion Loss
- Small Error in Measurement Systems
  $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation $I_{D(off)} < 200$ pA
- High Speed $t_{d(on)} < 4$ ns
- Low Noise Audio-Freq Amplification
  $e_N < 2\ nV/\sqrt{Hz}$ at 1 kHz

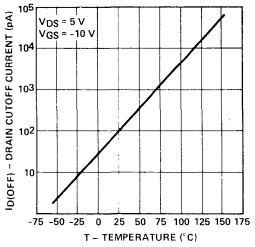
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-39	U320-2
Single	TO-52	2N5432-34
Single	TO-92	J108-10
Single	TO-106	E108-10
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

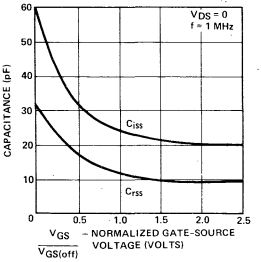
Output Characteristic



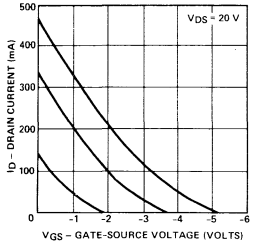
Drain Cutoff Current vs Ambient Temperature



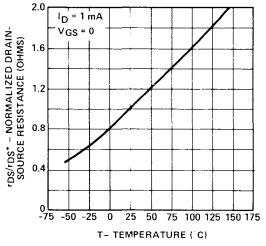
Common-Source Capacitance vs Normalized Gate-Source Voltage



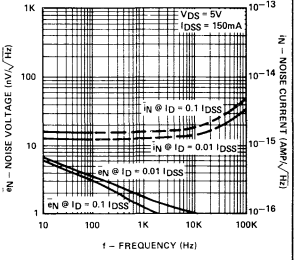
Transfer Characteristics



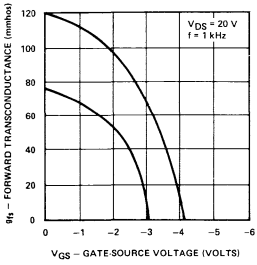
ON Resistance vs Ambient Temperature



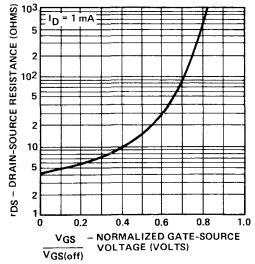
Equivalent Input Noise Voltage and Noise Current vs Frequency



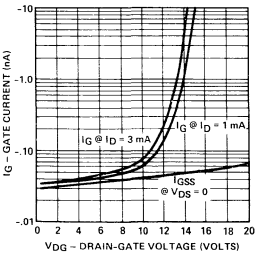
Forward Transconductance vs Drain Current



Resistance vs Normalized Gate-Source Voltage

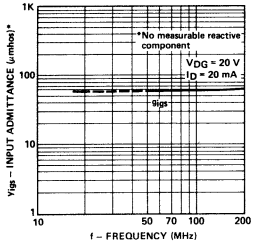


Gate Currents vs Drain-Gate Voltage

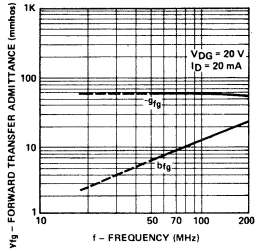


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

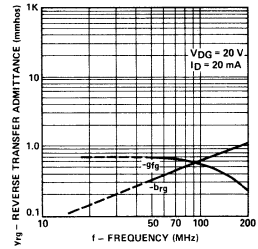
Input Admittance Common Gate vs Frequency



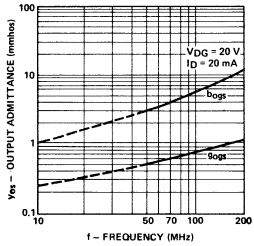
Forward Transfer Admittance Common Gate vs Frequency



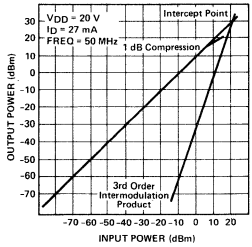
Reverse Transfer Admittance Common Gate vs Frequency



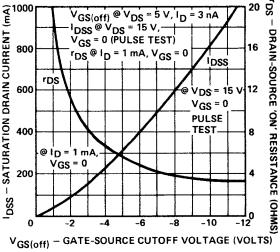
Output Admittance Common Gate vs Frequency

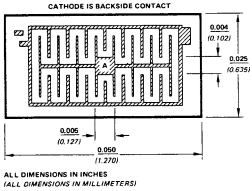


Gain – Intermodulation Characteristics



Drain Current & 'ON' Resistance vs Gate-Source Voltage





n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

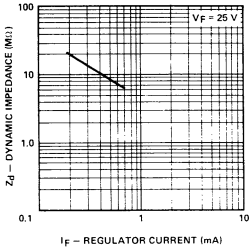
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

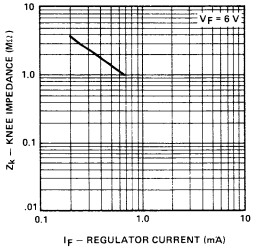
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR022 Thru CR062, U508
Single	Chip	CR022CHP Thru CR062CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

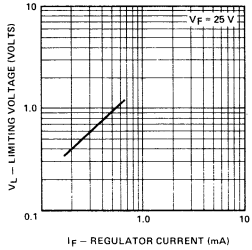
Dynamic Impedance vs Regulator Current



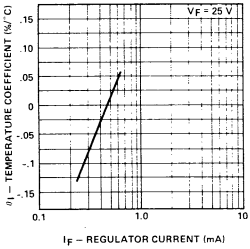
Knee Impedance vs Regulator Current



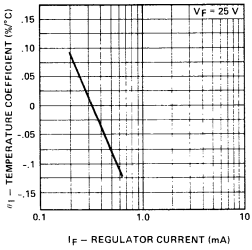
Limiting Voltage @ 0.8 I_F vs Regulator Current



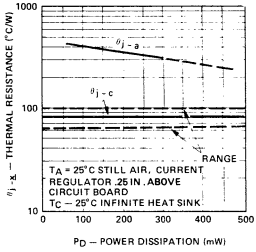
Temperature Coefficient -55°C ≤ T_j ≤ 25°C vs Regulator Current



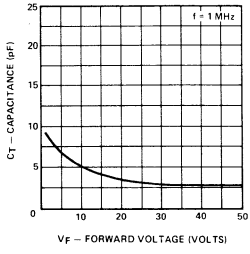
Temperature Coefficient 25°C ≤ T_j ≤ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation

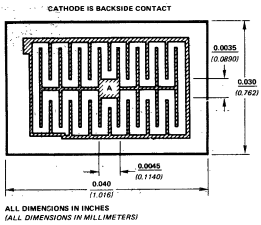


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times |1 + \theta_I (T_j - 25°C)|$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} P_D = T_{case} + \theta_{j\text{-}c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



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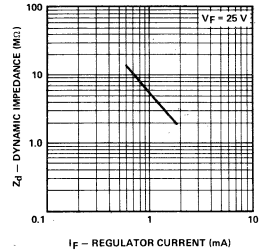
- Simplifies Floating Current Sources No Power Supplies Required

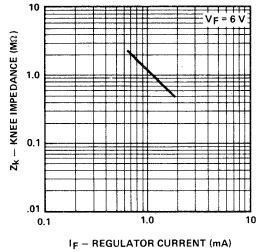
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR068 Thru CR150
Single	Chip	CR068CHP Thru CR150CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

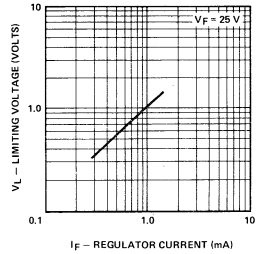
Dynamic Impedance vs Regulator Current



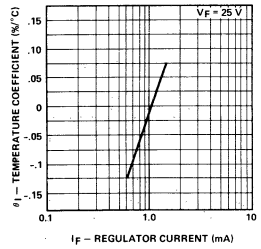
Knee Impedance vs Regulator Current



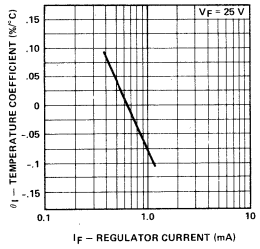
Limiting Voltage @ 0.8 I_F vs Regulator Current



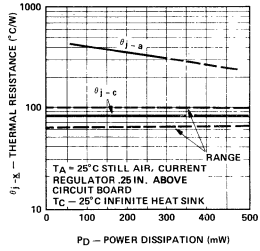
Temperature Coefficient $-55°C \leq T_j \leq 25°C$ vs Regulator Current



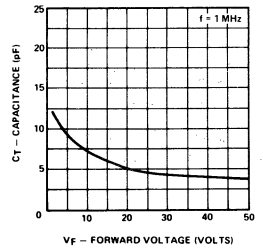
Temperature Coefficient $25°C \leq T_j \leq 125°C$ vs Regulator Current



Thermal Resistance vs Power Dissipation

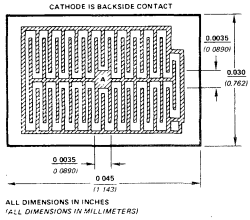


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times |1 + \theta_I (T_j - 25°C)|$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a}P_D = T_{case} + \theta_{j\text{-}c}P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

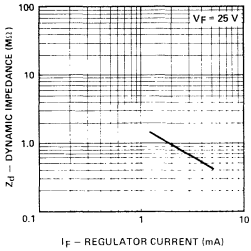
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

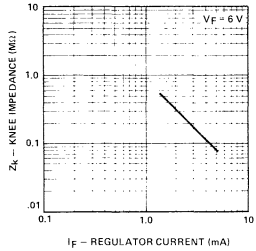
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR160 Thru CR470
Single	Chip	CR160CHP Thru CR470CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

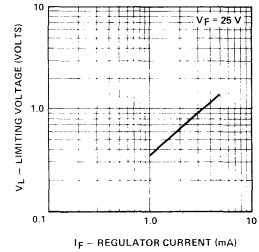
Dynamic Impedance vs Regulator Current



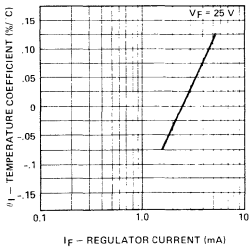
Knee Impedance vs Regulator Current



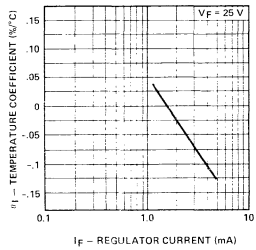
Limiting Voltage @ 0.8 I_F vs Regulator Current



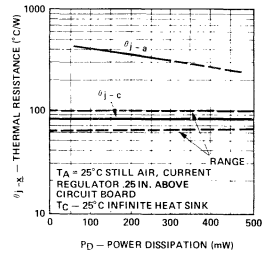
Temperature Coefficient $-55°C \leq T_j \leq 25°C$ vs Regulator Current



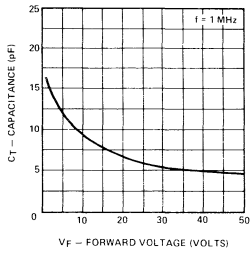
Temperature Coefficient $25°C \leq T_j \leq 125°C$ vs Regulator Current



Thermal Resistance vs Power Dissipation

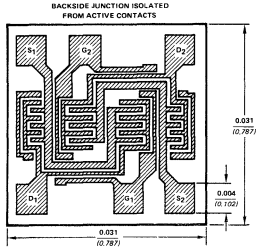


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times |1 + \theta_I (T_j - 25°C)|$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a}P_D = T_{case} + \theta_{j\text{-}c}P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET

designed for . . .

- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

BENEFITS:

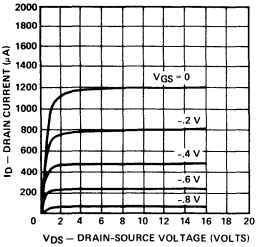
- **Minimum System Error and Calibration**
  5 mV Offset Maximum (2N5196)
- **Low Drift With Temperature**
  5 μV/°C Maximum (2N5196)

TYPE	PACKAGE
Dual	TO-71
Dual	Chip

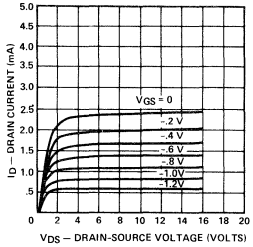
PRINCIPAL DEVICES
2N5196-9, U231-35
2N5199CHP, U232CHP-35CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

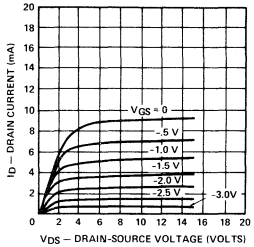
Output Characteristics
Low $V_{GS(off)}$ Unit



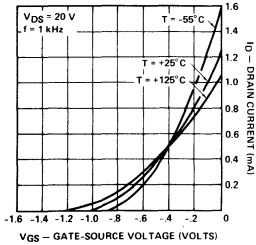
Output Characteristics
Medium $V_{GS(off)}$ Unit



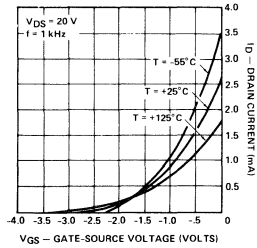
Output Characteristics
High $V_{GS(off)}$ Unit



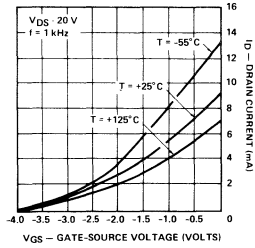
Transfer Characteristics
Low $V_{GS(off)}$



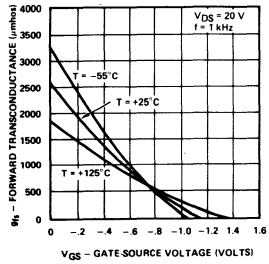
Transfer Characteristics
Medium $V_{GS(off)}$



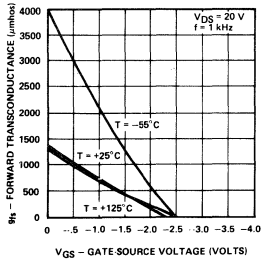
Transfer Characteristics
High $V_{GS(off)}$



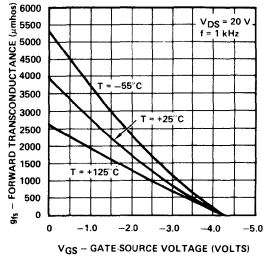
Transconductance Characteristics
Low $V_{GS(off)}$



Transconductance Characteristics
Medium $V_{GS(off)}$

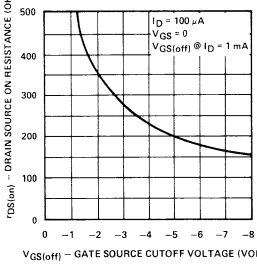


Transconductance Characteristics
High $V_{GS(off)}$

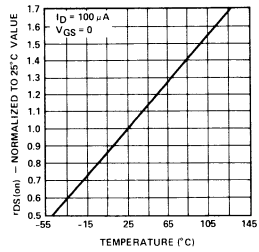


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

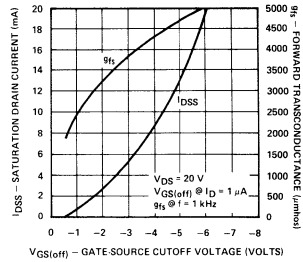
Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage



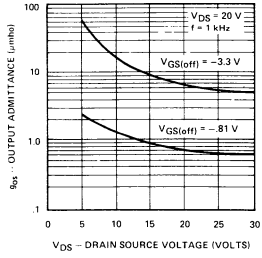
Normalized ON Resistance vs Ambient Temperature



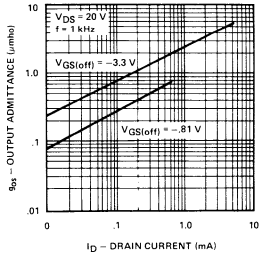
I_{DSS} and g_{fs} vs Gate-Source Cutoff Voltage



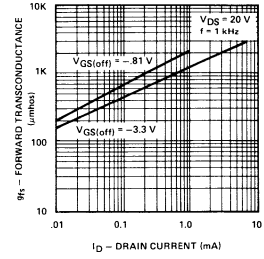
Common-Source Output Conductance vs Drain-Source Voltage



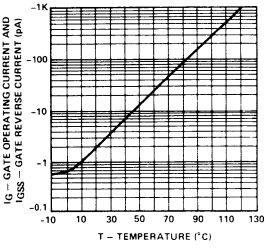
Common-Source Output Conductance vs Drain Current



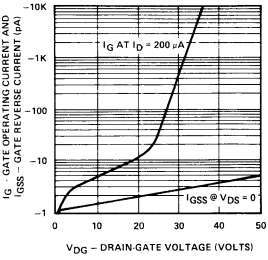
Common Source Forward Transconductance vs Drain Current



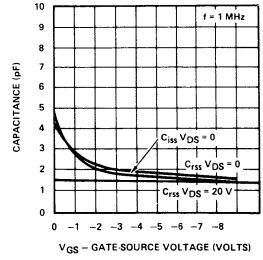
Gate Leakage Currents vs Ambient Temperature



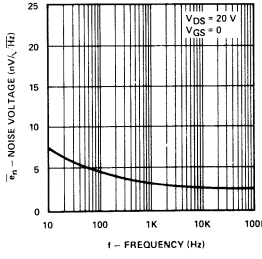
Gate Leakage Currents vs Drain-Gate Voltage

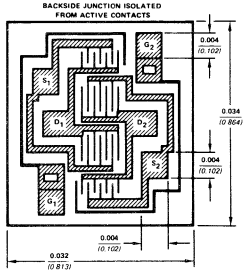


Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage vs Frequency





monolithic dual n-channel JFET

designed for . . .

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

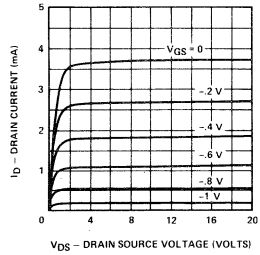
BENEFITS:

- **Minimum System Error and Calibration**
  5 mV Offset Maximum (J401)
  95 dB Minimum CMRR
- **Low Drift With Temperature**
  10 μV/°C (J401)
- **Simplifies Amplifier Design**
  Output Conductance < 2 μmho
- **Low Noise**
  $\overline{e}_n$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

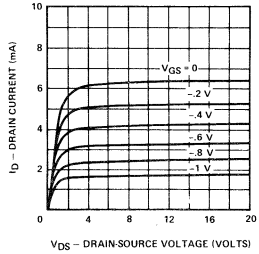
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N3921-2, 2N4084-5, 2N5045-7, U401-6
Dual	Mini-DIP (1)	J401-6
Dual	Mini-DIP (2)	J1401-6
Dual	Chip	2N4085CHP, 2N5046CHP-47CHP, U405CHP-06CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

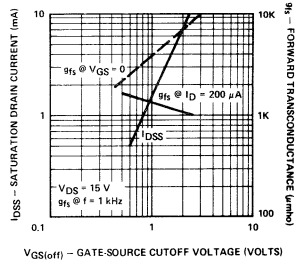
Output Characteristics
Low $V_{GS(off)}$ Unit (−1.5 V)



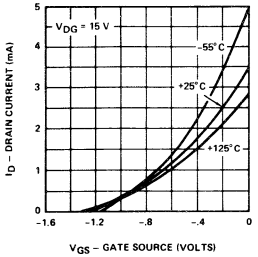
Output Characteristics
Medium $V_{GS(off)}$ Unit (−2.2 V)



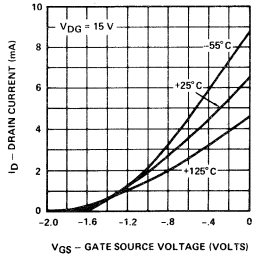
Drain Current and Transconductance vs
Gate-Source Cutoff Voltage



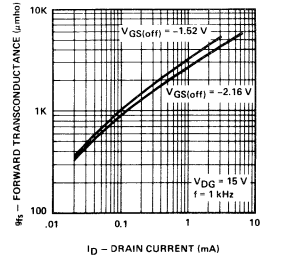
Transfer Characteristics
Low $V_{GS(off)}$ Unit (−1.5 V)



Transfer Characteristics
Medium $V_{GS(off)}$ Unit (−2.2 V)

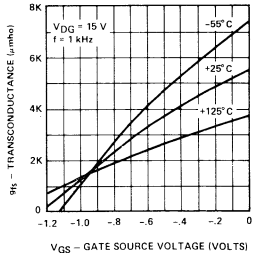


Forward Transconductance
vs Drain Current

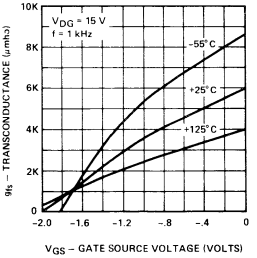


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

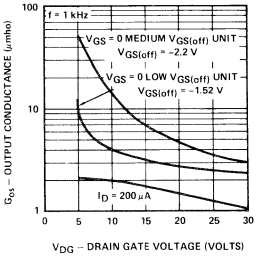
Transconductance vs Gate Source Voltage
Low $V_{GS(off)}$ Unit (−1.5 V)



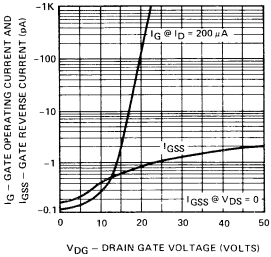
Transconductance vs Gate Source Voltage
Medium $V_{GS(off)}$ Unit (−2.2 V)



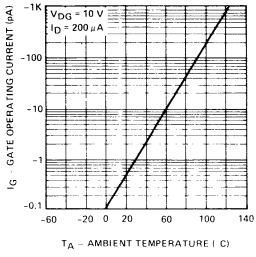
Output Conductance
vs Drain Gate Voltage



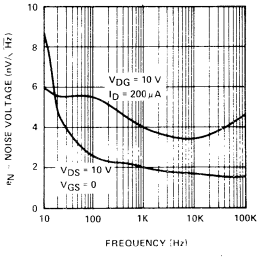
Gate Operating Current
vs Drain Gate Voltage



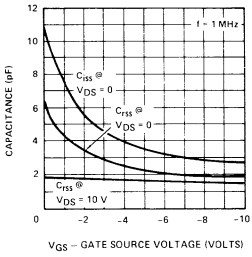
Gate Operating Current
vs Ambient Temperature



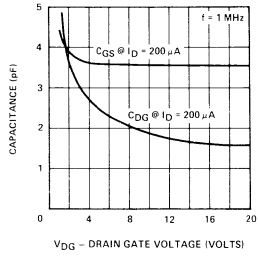
Equivalent Short Circuit Input Noise
vs Frequency

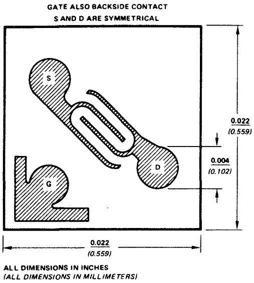


Capacitance vs Gate Source Voltage



Capacitance vs Drain to Gate Voltage





n-channel JFET
designed for . . .

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

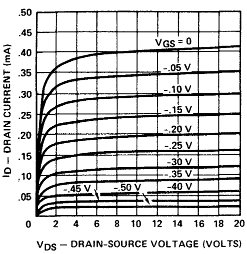
BENEFITS:

- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages, $V_{GS(off)} < 1$ V (2N4338)
- High Off-Isolation As a Switch $I_{D(off)} < 50$ pA
- High Input Impedance

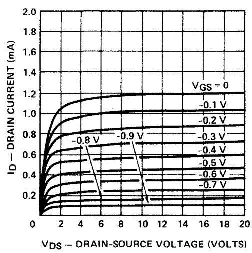
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3368-70, 2N3436-8, 2N3458-60, 2N4338-41, VCR4N
Single	TO-106	2N4302-4, E201-4
Single	Chip	All of the above

PERFORMANCE CURVES (25°C unless otherwise noted)

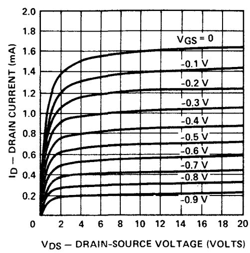
Output Characteristic



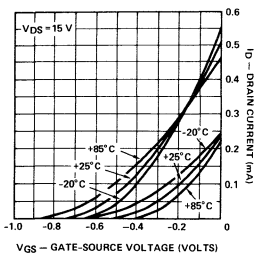
Output Characteristic



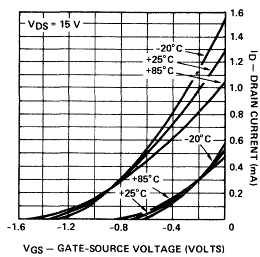
Output Characteristic



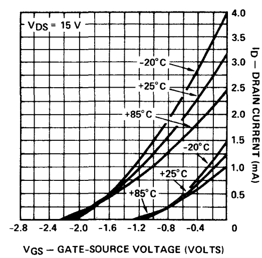
Transfer Characteristics



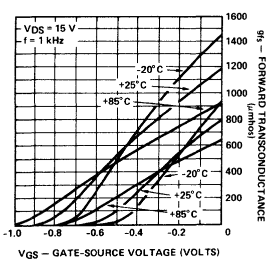
Transfer Characteristics



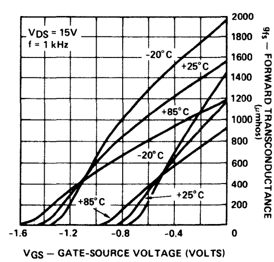
Transfer Characteristics



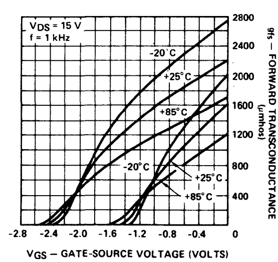
Transconductance Characteristics



Transconductance Characteristics

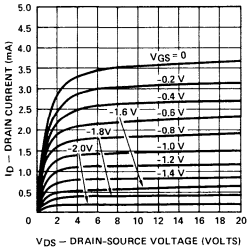


Transconductance Characteristics

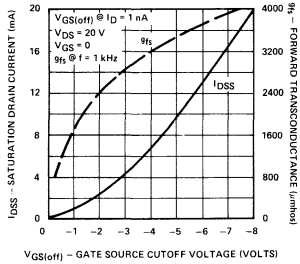


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

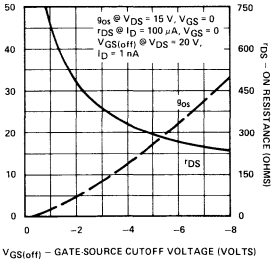
Output Characteristic



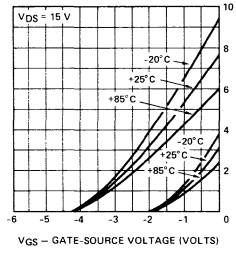
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



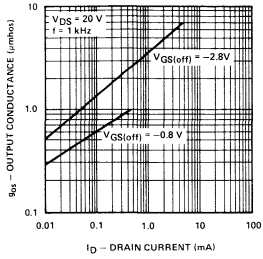
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



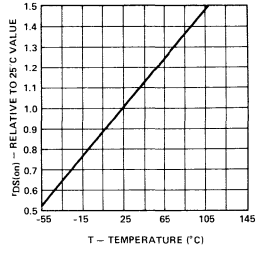
Transfer Characteristics



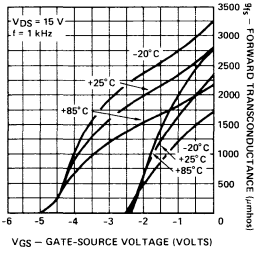
Common-Source Output Conductance vs Drain Current



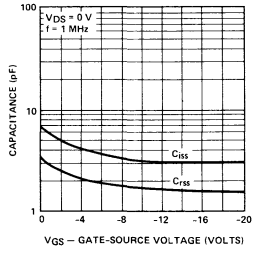
ON Resistance vs Ambient Temperature



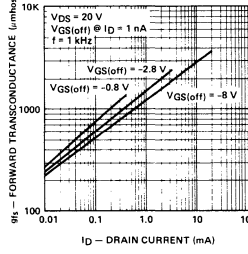
Transconductance Characteristics



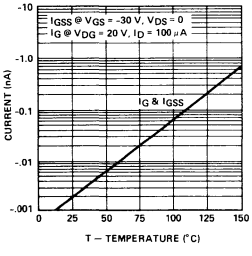
Common-Source Capacitances vs Gate-Source Voltage



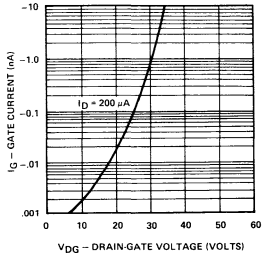
Common-Source Forward Transconductance vs Drain Current



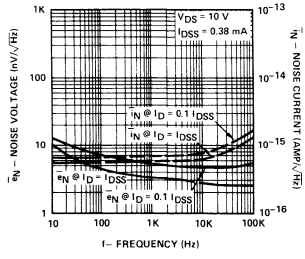
Gate Currents vs Ambient Temperature



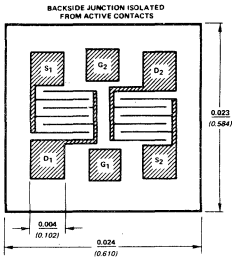
Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency



NQP



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET

designed for . . .

- General Purpose Differential Amplifiers

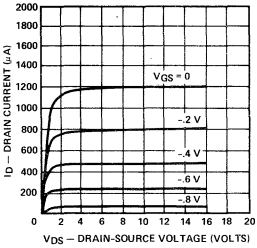
BENEFITS:

- Low Cost
- High Input Impedance

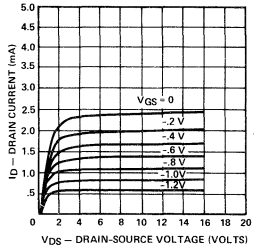
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	Mini-DIP (1)	J410-12
Dual	Mini-DIP (2)	NPD8301-3
Dual	SI-200	E400-2, E410-12
Dual	TO-71	2N3954, 2N3954A, 2N3955, 2N3955A, 2N3956-8, 2N5452-54
Dual	Chip	E401CHP-2CHP, E411CHP-12CHP 2N3955CHP, 2N3956CHP-8CHP, 2N5454CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

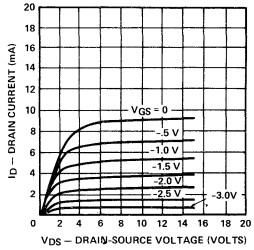
Output Characteristics
Low $V_{GS(off)}$ Unit



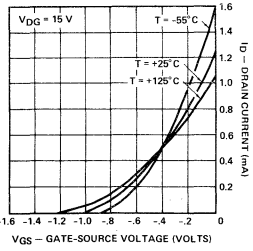
Output Characteristics
Medium $V_{GS(off)}$ Unit



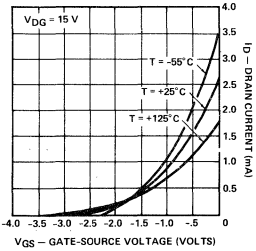
Output Characteristics
High $V_{GS(off)}$ Unit



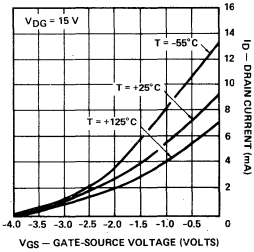
Transfer Characteristics
Low $V_{GS(off)}$



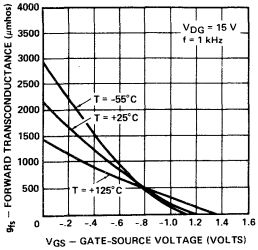
Transfer Characteristics
Medium $V_{GS(off)}$



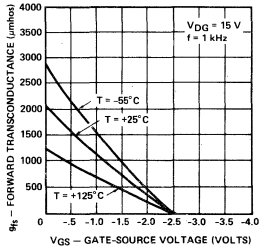
Transfer Characteristics
High $V_{GS(off)}$



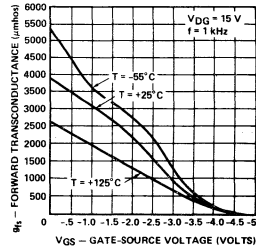
Transconductance Characteristics
Low $V_{GS(off)}$

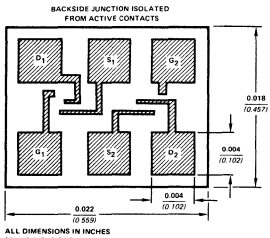


Transconductance Characteristics
Medium $V_{GS(off)}$



Transconductance Characteristics
High $V_{GS(off)}$





monolithic dual n-channel JFETs

designed for . . .

- Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

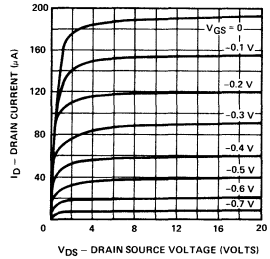
BENEFITS:

- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

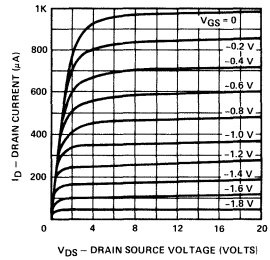
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-78	U421-6
Dual	Chip	U423CHP, U426CHP

PERFORMANCE CURVES (25° C unless otherwise noted)

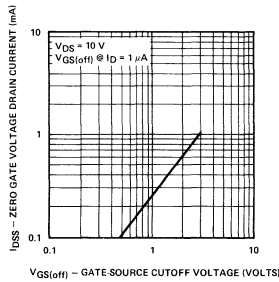
Output Characteristics
Low $V_{GS(off)}$ Unit (1.0 V)



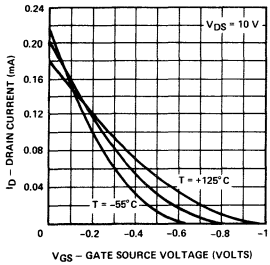
Output Characteristics
High $V_{GS(off)}$ Unit (2.5 V)



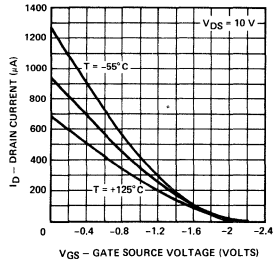
I_{DSS} vs Gate Source Cutoff Voltage



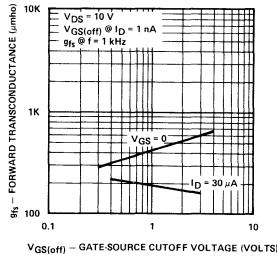
Transfer Characteristics
Low $V_{GS(off)}$ Unit (1.0 V)



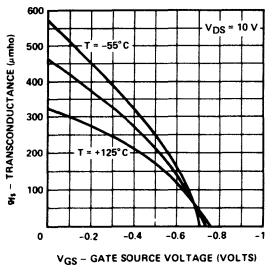
Transfer Characteristics
High $V_{GS(off)}$ Unit (2.5 V)



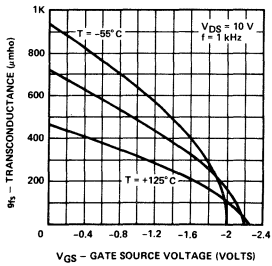
Forward Transconductance vs
Gate Source Cutoff Voltage



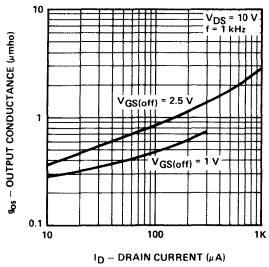
Transconductance vs Gate Source Voltage
Low $V_{GS(off)}$ Unit (1.0 V)



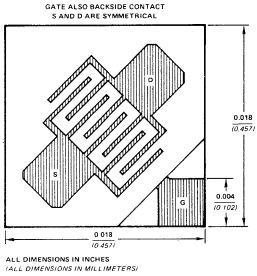
Transconductance vs Gate Source Voltage
High $V_{GS(off)}$ Unit (2.5 V)



Common-Source Output Conductance
vs Drain Current



NRL



n-channel JFET
designed for . . .

- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

BENEFITS:

- Wide Input Dynamic Range
  High I_G Breakpoint Voltage
- High Gain
- Low Insertion Loss Switches

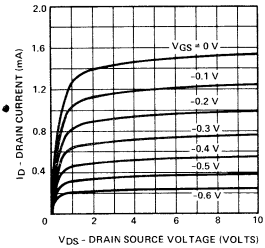
TYPE	PACKAGE
Single	TO-72
Single	TO-92
Single	Chip

PRINCIPAL DEVICES

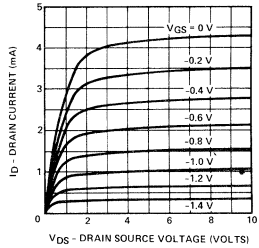
2N3821-4, 2N4220-2, 2N4220A-22A, 2N4223-24, 2N5556-58
2N5457-9, MPF109, MPF111
All of the above

PERFORMANCE CURVES (25°C unless otherwise noted)

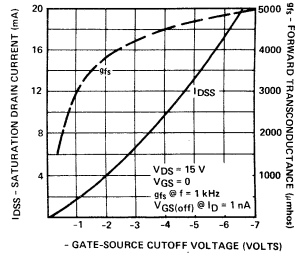
Output Characteristic



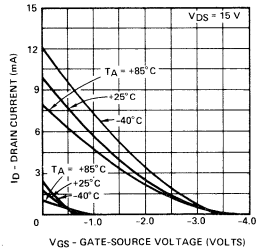
Output Characteristic



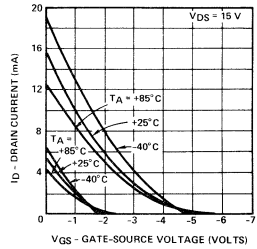
Drain Current & Transconductance vs Gate-Source Voltage



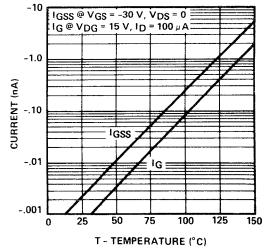
Transfer Characteristic



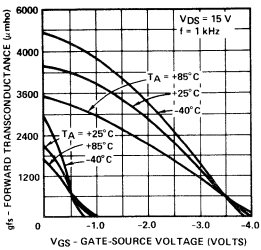
Transfer Characteristics



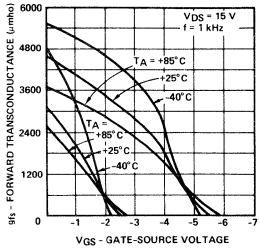
Leakage Currents vs Ambient Temperature



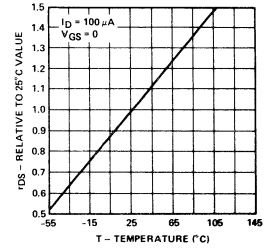
Transconductance Characteristics



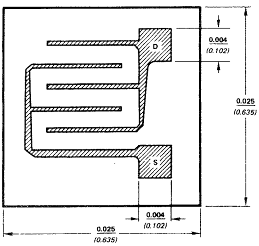
Transconductance Characteristics



'ON' Resistance vs Ambient Temperature



GATE IS BACKSIDE CONTACT
S AND D ARE SYMMETRICAL



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

- Low Noise Amplifiers
- Single and Differential Amplifiers

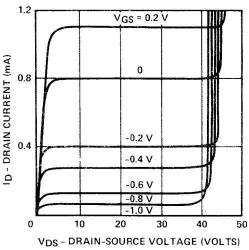
BENEFITS:

- Simplifies Amplifier Design
- Low Output Conductance
- Low 1/f Noise

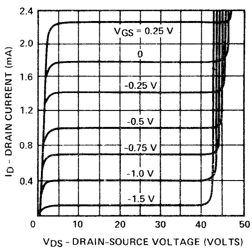
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N5515-24
Single	TO-72	2N4867-9, 2N4867A-69A
Single	TO-106	E230-2
Dual	Chip	2N5518CHP-9CHP, 2N5523CHP-4CHP
Single	Chip	All of the above single devices

PERFORMANCE CURVES (25°C unless otherwise noted)

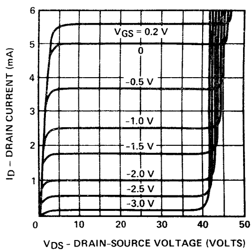
Output Characteristics



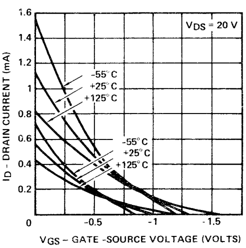
Output Characteristics



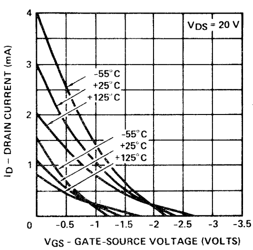
Output Characteristics



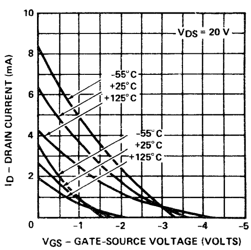
Transfer Characteristics



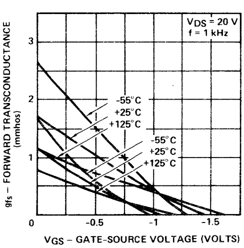
Transfer Characteristics



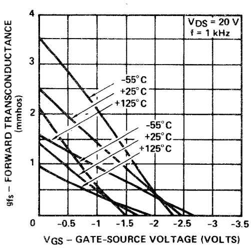
Transfer Characteristics



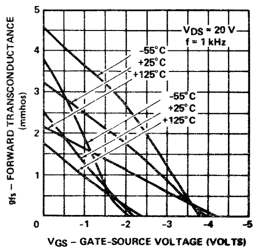
Transconductance Characteristics

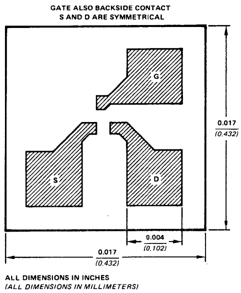


Transconductance Characteristics



Transconductance Characteristics





n-channel JFET
designed for . . .

- Ultra-High Input Impedance Amplifiers
  - Electrometers
  - pH Meters
  - Smoke Detectors

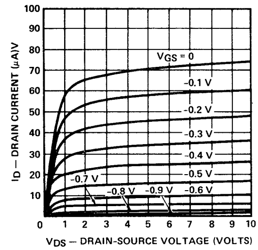
BENEFITS:

- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- High Input Impedance
  $I_G < 1$ pA (2N5906-09)

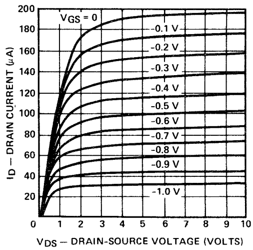
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N4117-9, 2N4117A-9A, VCR7N
Dual	TO-78	2N5902-9
Single	Chip	2N4117CHP-9CHP, 2N4117ACHP-9ACHP, VCR7NCHP
Dual	Chip	2N5905CHP, 2N5909CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

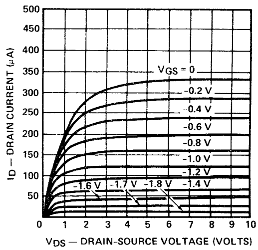
Output Characteristic



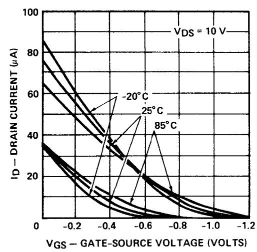
Output Characteristic



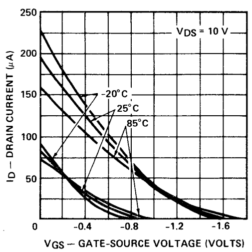
Output Characteristic



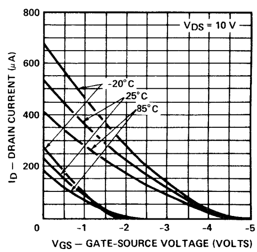
Transfer Characteristics



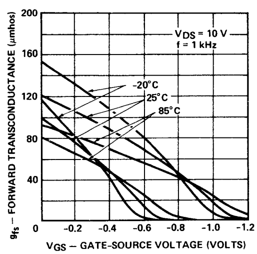
Transfer Characteristics



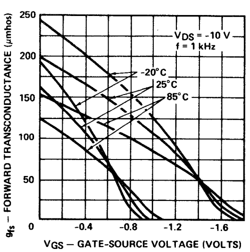
Transfer Characteristics



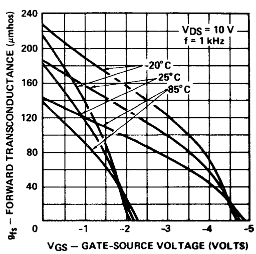
Transconductance Characteristics

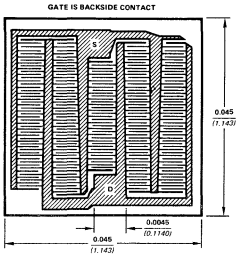


Transconductance Characteristics



Transconductance Characteristics





n-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers

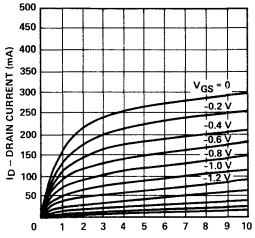
BENEFITS:

- **Very Low Insertion Loss**
  $R_{DS(on)}$ < 2.5 Ohms (U290, U294)
- **High Off-Isolation**

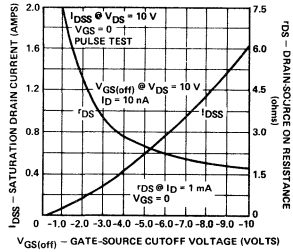
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-39	U294-95
Single	TO-52	U290-1
Single	TO-106	E105-7
Single	Chip	U290CHP-1CHP, E105CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

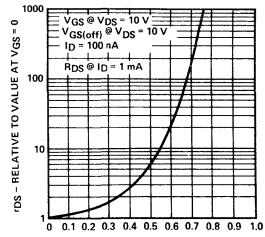
Output Characteristic



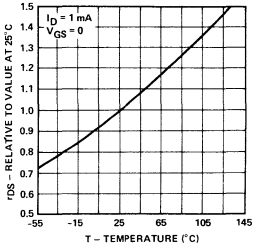
Saturation Drain Current and Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



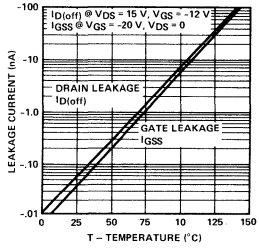
Drain-Source Resistance vs Normalized Gate-Source Voltage



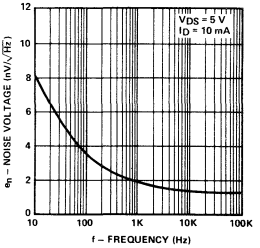
Drain-Source 'ON' Resistance vs Ambient Temperature



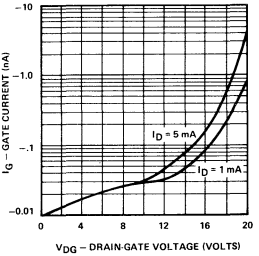
Leakage Currents vs Ambient Temperature



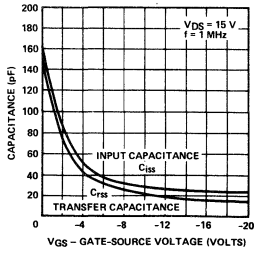
Equivalent Input Noise Voltage vs vs Frequency

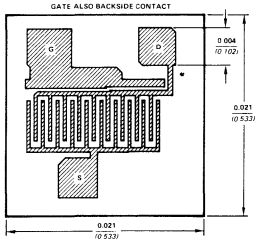


Leakage Current vs Drain-Gate Voltage



Common-Source Capacitance vs Gate-Source Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

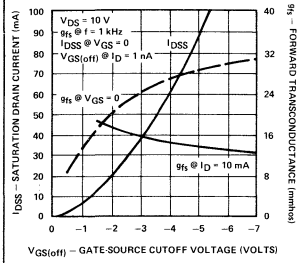
BENEFITS

- **Industry Standard**
- **High Power Gain**
  16 dB at 100 MHz, Common Gate
  11 dB at 450 MHz, Common Gate
- **Low Noise**
  3 dB Noise Figure at 450 MHz
- **Wide Dynamic Range**
  Greater Than 100 dB
- **75 Ohm Input Match Common Gate**

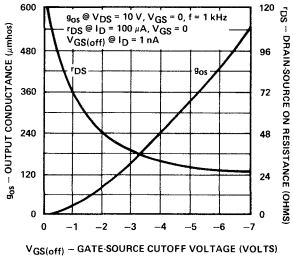
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U308-10
Single	TO-72	U311
Single	TO-92	J308-10
Dual	TO-99	U430-1
Quad	TO-99	U350
Dual	TO-105	E430-1
Single	OD-81	U316-17
Single	Chip	J308CHP-10CHP, U308CHP-10CHP, U311CHP, U316CHP-17CHP
Dual	Chip	E430CHP-1CHP, U430CHP-1CHP
Quad	Chip	U350CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

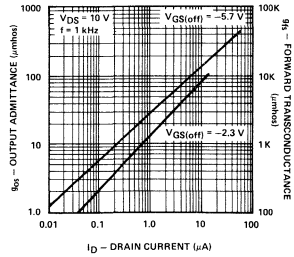
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



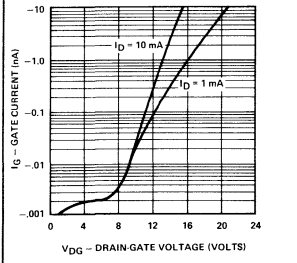
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



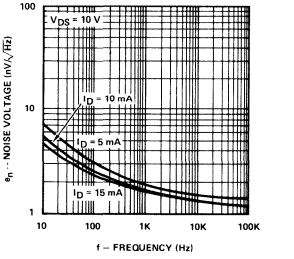
Common-Source Output Conductance vs Drain Current



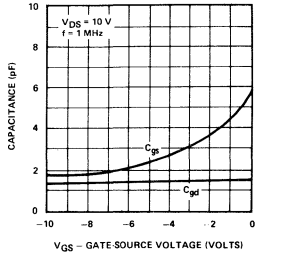
Gate Operating Current vs Drain-Gate Voltage

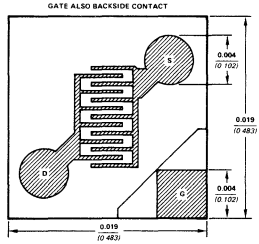


Equivalent Input Noise Voltage vs Frequency



Junction Capacitance vs Gate-Source Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

- High Frequency Amplifiers
- Mixers
- Oscillators

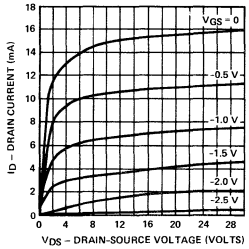
BENEFITS:

- High Power Gain
- Low Input Capacitance

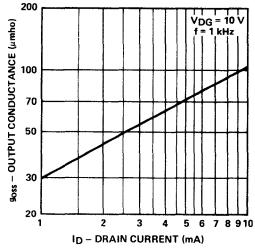
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U312
Dual	TO-78	2N5911-12, U257
Single	TO-106	E114, E210-12, E300
Dual	SI-200	E420-1
Single	Chip	E114CHP, E210CHP-12CHP, E300CHP, U312CHP, U314CHP-15CHP
Single	OD-81	U314
Single	OD-82	U315
Dual	Chip	2N5912CHP, E420CHP-1CHP, U257CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

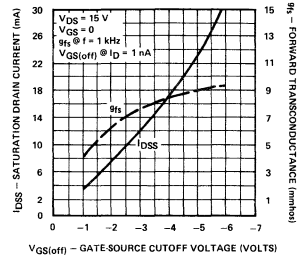
Output Characteristic



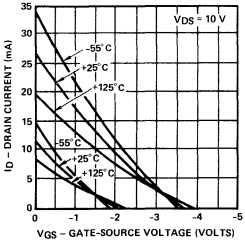
Common-Source Output Conductance vs Drain Current



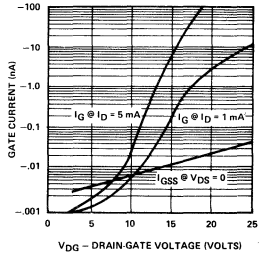
Saturation Drain Current and Forward Transconductance vs Gate-Source Cutoff Voltage



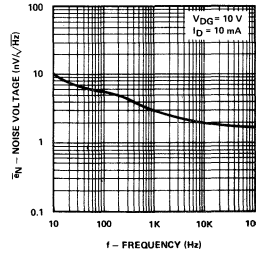
Transfer Characteristics



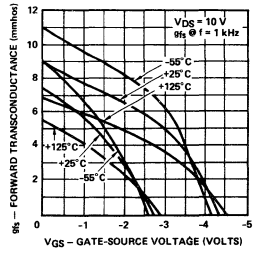
Leakage Currents vs Drain-Gate Voltage



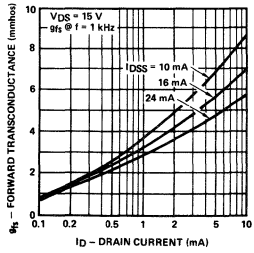
Equivalent Input Noise Voltage vs Frequency



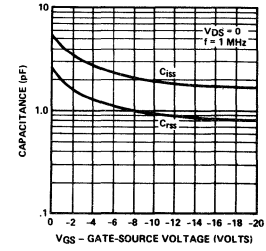
Transconductance Characteristics

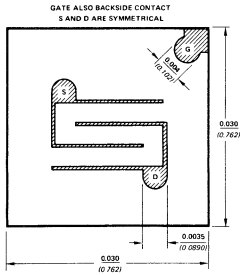


Forward Transconductance vs Drain Current



Common-Source Capacitances vs Gate-Source Voltage





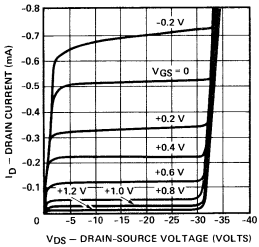
p-channel JFET
designed for . . .

- **General Purpose Amplifiers and Attenuators**

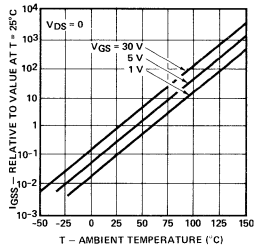
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N2608, 2N2608JAN, 2N2843
Single	TO-72	2N3329-32, 2N3909, VCR5P
Single	Chip	2N2608CHP, 2N2843CHP, 2N3329CHP-32CHP, 2N3909CHP VCR5PCHP

PERFORMANCE CURVES (25°C unless otherwise noted)

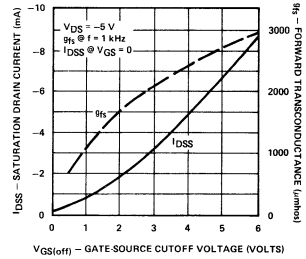
Output Characteristic



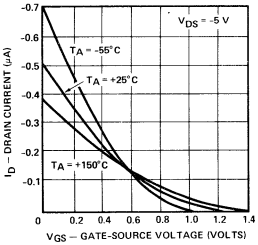
Gate Reverse Current vs Ambient Temperature



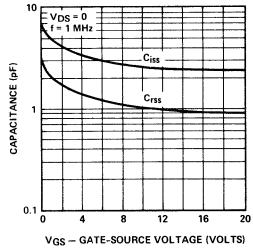
Drain Current & Transconductance vs Gate-Source Voltage



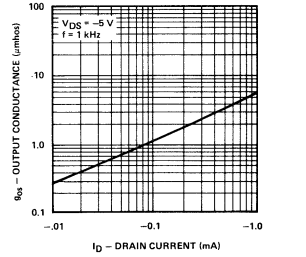
Transfer Characteristic



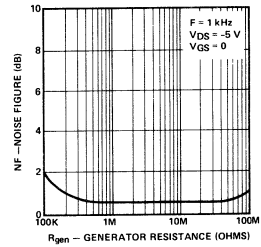
Common-Source Capacitances vs Gate-Source Voltage



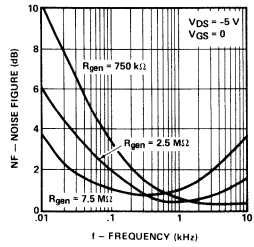
Common-Source Output Conductance vs Drain Current



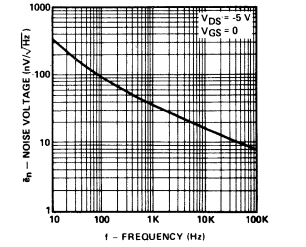
Noise Figure vs Generator Resistance

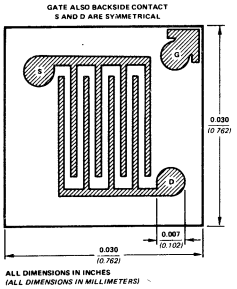


Noise Figure vs Frequency



Equivalent Input Noise Voltage vs Frequency





p-channel JFET
designed for . . .

- General Purpose Amplifiers
- Switches

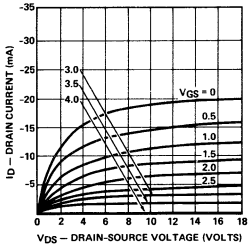
BENEFITS:

- Wide Range of Transconductance

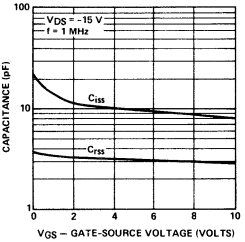
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3382, 2N3384, 2N3386, VCR3P
Single	Chip	2N3382CHP-86CHP, VCR3PCHP

PERFORMANCE CURVES (25°C unless otherwise noted)

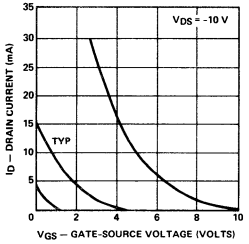
Output Characteristic



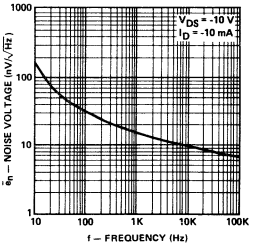
Common-Source Capacitances vs Gate-Source Voltage



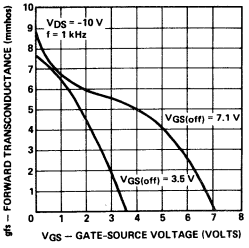
Transfer Characteristics



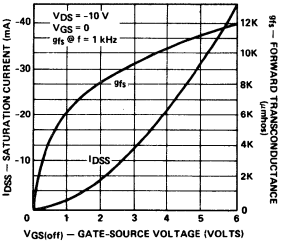
Equivalent Input Noise Voltage vs Frequency



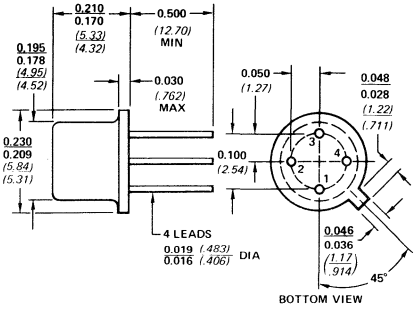
Transconductance Characteristics



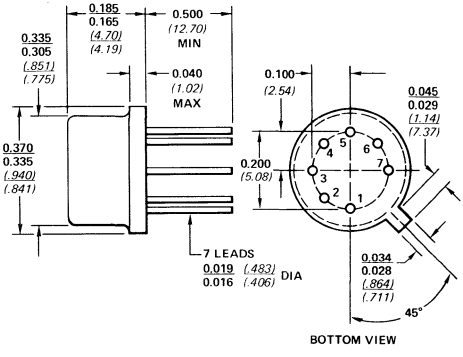
Drain Current & Transconductance vs Gate-Source Voltage



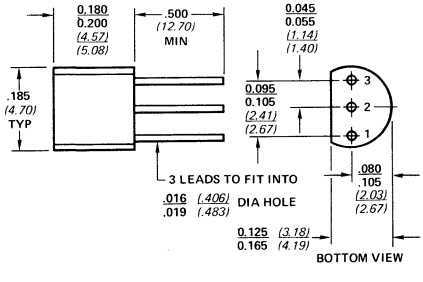
mechanical data (cont'd)



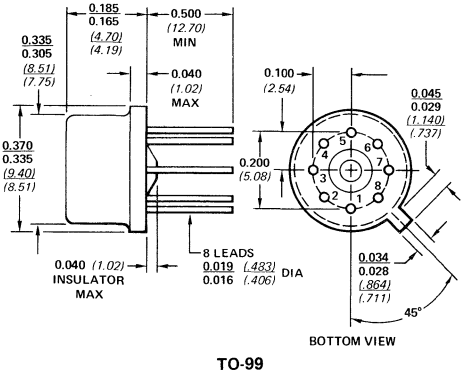
TO-72



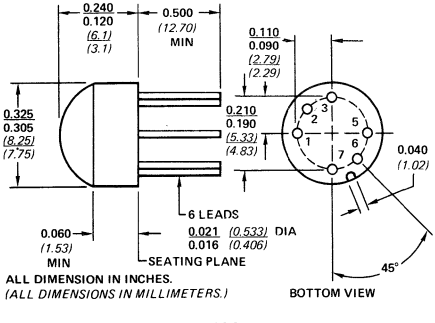
TO-78



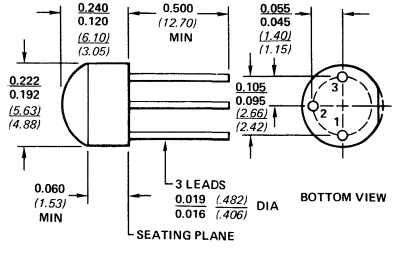
TO-92



TO-99



TO-105



TO-106

glossary of terms and abbreviations

1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e., V_G = Gate Voltage; or simply help define the symbol, i.e., t_f = Fall Time, t_r = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example: BV_{GSS} = Breakdown Voltage from gate to source with the drain shorted to the source.

b_{fg} = Common-Gate Forward Susceptance

b_{fs} = Common-Source Forward Susceptance

b_{igs} = Common-Gate Input Susceptance

b_{iss} = Common-Source Input Susceptance

b_{ogs} = Common-Gate Output Susceptance

b_{oss} = Common-Source Output Susceptance

b_{rg} = Common-Gate Reverse Susceptance

b_{rs} = Common-Source Reverse Susceptance

BV_{DGO} = Drain-Gate Breakdown Voltage

BV_{DSS} = Drain-Source Breakdown Voltage

BV_{SDX} = Drain-Source Breakdown Voltage

BV_{G1G2} = Gate-Gate Breakdown Voltage

BV_{G1SS} = Gate 1 to Source Breakdown Voltage

BV_{G2SS} = Gate 2 to Source Breakdown Voltage

BV_{GBS} = Gate-Body Breakdown Voltage

BV_{GSS} = Gate-Source Breakdown Voltage

BV_{SDS} = Source-Drain Breakdown Voltage

BV_{SGO} = Source-Gate Breakdown Voltage

C_{db} = Drain-Body Capacitance

C_{dgo} = Drain-Gate Capacitance

C_{gb} = Gate-Body Capacitance

C_{gd} = Gate-Drain Capacitance

C_{gs} = Gate- Source Capacitance

C_{iss} = Common-Source Input Capacitance

C_{oss} = Common-Source Output Capacitance

C_{rss} = Common-Source Reverse Transfer Capacitance

C_{sb} = Source-Body Capacitance

C_{sd} = Source-Drain Capacitance

C_{sgo} = Source-Gate Capacitance

D = Drain

$\bar{e}_N$ = Equivalent Short Circuit Input Noise Voltage

f_m = Figure of Merit

G = Gate

g_{fg} = Common-Gate Forward Transconductance

g_{fs} = Common-Source Forward Transconductance

g_{fso} = Common-Source Forward Transconductance @ $V_{GS} = 0$

g_{fs1}/g_{fs2} = Common-Source Forward Transconductance Ratio

g_{ig} = Common-Gate Input Conductance

g_{is} = Common-Source Input Conductance

g_{og} = Common- Gate Output Conductance

g_{os} = Common-Source Output Conductance

g_{oss} = Common Source Output Conductance @ $V_{GS} = 0$

$g_{os1}-g_{os2}$ = Differential Output Conductance

G_{pg} = Common-Gate Power Gain

G_{ps} = Common-Source Power Gain

$I_{D(off)}$ = Drain Cutoff Current

$I_{D(on)}$ = Drain ON Current

I_{DGO} = Drain-Gate Leakage

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