1994 Synergy Product Data Book

UltraFast Usable Speed

SYNERGY SEMICONDUCTOR

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UltraFast Usable Speed™

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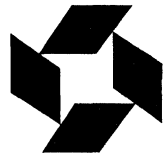

1994
Synergy
Product Data Book

UltraFast Usable Speed℠

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Static voltage or electric fields can occasionally damage small geometry bipolar ICs. Precautions should, therefore, be taken to avoid application of any voltage higher than the maximum rated voltage to this device.

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GENERAL INFORMATION

SYNERGY SEMICONDUCTOR

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Translators

Ultra-Fast & Low-Power RAMs

LOGIC TABLE OF CONTENTS CLASSIFIED BY PRODUCT FUNCTIONALITY

COMPANY PROFILE:

Synergy Semiconductor, a leader in the high-performance market, designs and manufactures the industry's fastest logic, clock control, translator, memory and semicustom products. Synergy utilizes a unique proprietary process, combined with design innovations, to provide the very best in *UltraFast Usable Speed* products.

A key factor in the company's early success has been the *synergy* between a highly experienced and motivated team, in-house wafer fabrication and state-of-the-art technology and test capabilities. These components will continue to keep Synergy in the forefront of the high-performance market.

TECHNOLOGY:

Synergy has implemented a world leadership bipolar-based technology which incorporates the most advanced process modules and isolation techniques to produce the industry's fastest speeds at lower power levels than previously achievable. Unlike other bipolar technologies, Synergy's proprietary ASSET™ (All Spacer Separated Element Transistor) technology is optimized to produce both memory and logic products offering superior performance compared to all domestic and international competitors.

Synergy's patented architectural innovations produce significant customer benefits in both performance and density:

- Spacers allow element (i.e., base/emitter/collector) separations to be determined by the thickness of a film rather than by a lithographic space, resulting in a dramatic reduction in element separation;
- ASSET's trench isolation results in transistors which are 40% smaller than competitive transistors produced under similar lithographic conditions.

ASSET is a fully self-aligned technology which is scalable to submicron levels. Using the current 1.2µ version of ASSET, Synergy is producing 16Kx4 SRAMs, an Advanced Self-Timed 2Kx9 STRAM, and the System Elements™ family. In the next twelve months, the company will introduce the first products designed in its ASSET-based BiCMOS, ASSET II technology (offering further advancements in density and performance), and an exciting array of new products.

The result of combining Synergy's patented circuit design and processing technologies is the highest-performance, manufacturable system solutions.

PRODUCTS:

Synergy currently offers a complete series of ultra-fast 1K, 4K, 16K, 64K and Advanced Self-Timed 2Kx9 ECL SRAMs, the ECLinPS™ Logic Family (including ECLinPS Lite), the Super-300K™ Logic Family; and both RAM-Intensive and Universal System Elements (RISE™ and USE™, respectively). With speeds to 3ns (1K and 4K) and 5ns (16K and 64K), all SRAMs are designed for alpha-particle immunity and feature balanced read and write times. Additional customer benefits include tighter skews, 2000V ESD protection and 10KH/100K I/O options.

New products introduced in 1993, include ultra-fast FIFOs, PECL Clock Distribution circuits (Positive ECL with TTL outputs) for TTL systems operating at 50MHz and above, 9-bit high-speed translators and an increasing range of RISE and USE semicustom System Elements. Synergy will continue to develop unique and complementary product families which will increase the usable speed available to the high-performance system designer.

STRATEGIC ALLIANCE:

Synergy Semiconductor entered into a comprehensive strategic alliance with Toshiba Corporation in early 1991. The strategic alliance incorporates four closely-linked agreements:

- a joint R&D pact,
- a manufacturing agreement,
- a technology licensing agreement, and
- an equity investment.

Under terms of the manufacturing agreement, Toshiba is providing Synergy with the use of a new high-volume (6-inch, submicron) IC fabrication line which processes Synergy's high-performance bipolar ASSET and BiCMOS technologies. This fab allows Synergy to utilize world class manufacturing capabilities to produce its current SRAM and logic products, as well as future products.

Through its equity investment in Synergy, Toshiba has recognized Synergy's leadership in bipolar-based process and design technologies. Toshiba is a minority shareholder (<10%).

EUROPEAN JOINT VENTURE:

Synergy is also the managing partner of System Microelectronic Innovation GmbH (SMI). SMI is a joint venture between Synergy Semiconductor and the German government, and is located in Frankfurt (Oder). The plant houses a large wafer fab facility, as well as plastic and hermetic package assembly lines, a large CAD design capability and production test areas. Synergy has licensed its ASSET technology to the new venture.

The new venture will continue to market its existing products into consumer, computer, industrial and telecom markets. It will also market Synergy's family of ultra-fast ECL SRAMs, logic, clock control, translator and semicustom products into the European sector. Manufacturing capability for ASSET products will be on-line in late 1993, and the two

companies will continue working together on the development of new products primarily aimed at high-performance telecommunications and computation applications emerging throughout Europe. The company has also established foundry relationships to produce both digital and analog products for both North American and European customers.

FACILITIES:

Synergy is headquartered in Santa Clara, California. The company's operations are housed in a 48,000 square foot facility which incorporates all aspects of its business from research and development to design, wafer fabrication, test, shipping and administration. This facility incorporates a 7,000 square foot modern wafer fabrication clean room with equipment operating in a sub-Class 10 environment. The fabrication area incorporates state-of-the-art high resolution steppers, dry etchers, films deposition systems, etc. The company's test area utilizes advanced test equipment capable of holding uniquely tight picosecond level testing accuracies.

INNOVATIVE INDUSTRY LEADERSHIP

Synergy is a manufacturer of leading edge products in both pure bipolar and BiCMOS technologies.

Synergy's original ASSET technology is an advanced bipolar technology which uses several innovative architectural features to achieve industry leadership performance with somewhat modest lithography.

These features include:

- trench isolation for maximum packing density;
- field walled base/emitter for minimum parasitics;
- ASSET transistor structure for minimum inter-element spacings;
- double silicided poly for emitter and base with metal interpoly via for low resistance local interconnect and maximum layout flexibility;
- poly on insulator resistors — zero TCR, ±5% lot-to-lot control;
- shallow junctions, very thin epi, high relative breakdown;
- walled sinker/collector contact.

These features result in an unmatched combination of performance and die size for a given lithography.

Further shrinkability and new features, such as slot-walled emitter/base, permit a technology roadmap to almost unimaginably small transistors, even at Synergy's current conservative lithography.

ASSET was architected not only for performance, but with manufacturability and reliability as paramount considerations. The result is consistently high yields, industry leadership performance and reliability second to none. This is complemented by design and layout flexibility which permits the design of RAM, logic, ASIC and programmable products in both ECL and TTL configurations with the same basic process.

The ASSET technology was an ideal base from which to evolve a BiCMOS technology which advantageously used the ASSET features to, once again, get leadership performance from somewhat modes feature sizes, i.e.

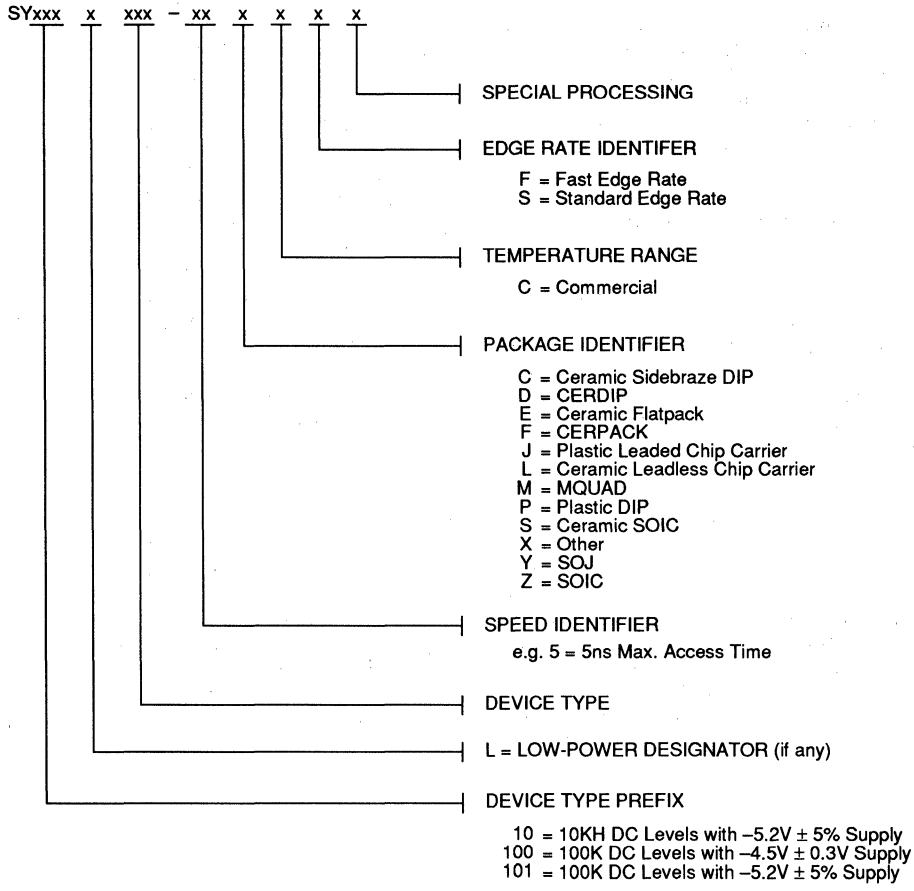
- The silicided emitter poly becomes a very low resistance gate element.
- The base conductance implant/spacer becomes an LDD structure.
- The silicided base contact becomes a self-aligned source drain contact.
- The trench isolated blanket buried layer allows a fully isolated P-well for both vertical PNP transistors and N-channel MOS.

The technology's versatility has been demonstrated by using the basic ingredients to create vertical PNPs, Schottky diodes, thin film resistors and a variety of capacitors. Trench isolation allows lithography-limited packing of P-/N-channel devices without creating any latch-up jeopardy.

These features result in extremely small devices which can be very tightly packed, as well as a highly versatile technology which is suitable for a wide variety of high-speed analog, digital or mixed-signal devices.

GENERIC ORDERING INFORMATION

GENERAL ORDERING INFORMATION(1)



NOTE:
See individual chapters for product-specific ordering information trees.

SYSTEM ELEMENTS™– SEMICUSTOM

2

SYNERGY SEMICONDUCTOR

SYSTEM ELEMENT™ FAMILY

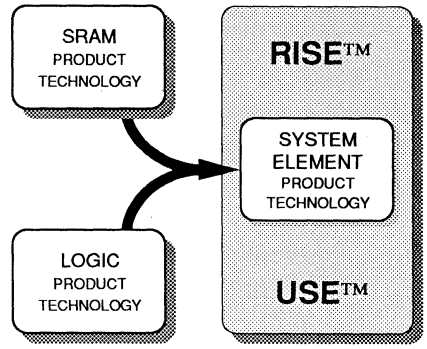
2

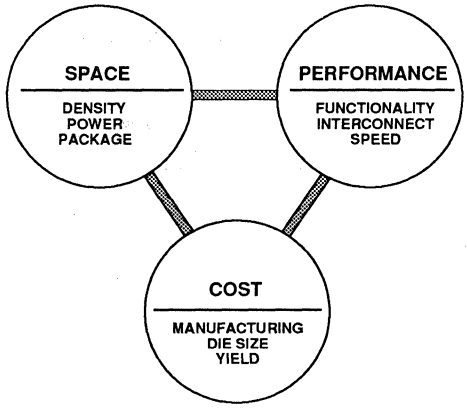
	Device P/N	Max. Gates	SRAM Block Size	SRAM # Blocks	Analog Capable?	I/O Pins	Package Size (Max.)	Available Date	Page No.
USE	SY1BP00	1,665	—	—	Yes	32	68	Now	2-12
	SY2BP00	3,640	—	—	Yes	56	128	Now	2-15
	SY4BP00	9,065	—	—	Yes	80	128	Now	2-18
	SY11BP00	19,550	—	—	Yes	108	160	Now	2-21
	SY21BP00	33,605	—	—	Yes	144	208	Now	2-24
	SY34BP00	63,090	—	—	Yes	184	304	Now	2-27
RISE	SY8BP4R2	12,630	64x32	4	Yes	108	160	Now	2-30
	SY9BP6R4	12,480	1Kx4	6	Yes	144	208	Now	2-33
	SY15BP10R4	23,946	1Kx4	10	Yes	192	304	Now	2-36

SYSTEM ELEMENT FAMILY

PRODUCT OVERVIEW

In keeping with our overriding commitment to provide our customers with the most innovative **high-performance solutions**, Synergy now offers Systems Designers a *completely new generation* of architectural building blocks — **SYNERGY SYSTEM ELEMENTS™**. By combining our ultra-fast, dense, *proven* SRAM product technology onto the same silicon with our high-speed, high-density logic technology — at surprisingly low power dissipation — Synergy moves another step ahead of its competition in the evolution of high-performance solutions. By simultaneously addressing the three "Imperatives of High-Performance Systems" (below), Synergy System Elements provide a dimension of system design integration never before possible.





Combining our unique OCEAN OF CELLS™ architecture with optimized SRAM, the designer can now achieve a *functional partitioning* while minimizing interconnect delays — all in a process technology with a proven track record. Further, the architecture of the basic cell allows straightforward implementation of powerful **Mixed-Signal** functions such as Phase-Locked-Loops (PLLs), Digital-to-Analog Convertors (DACs) and comparators.

For the **first time**, the high-performance system designer can combine ultra-fast digital, *mixed-signal* and 3ns SRAM onto the **same chip**!

While Synergy System Elements may just be the designers' dream family, we have not neglected the manufacturability aspects — Synergy's ASSET™ process has the longest track record of *any* ultra-high-performance bipolar process.

SYSTEM ELEMENT BENEFITS

- **Fastest, highest-density, *proven* SRAM (3ns)**
- **Fastest, highest-density logic cells**
- **Mixed-signal capability via ANALOG ZONE™**
- **Reduced interconnect delays — logic and memory on *same* chip**
- **Production-proven process technology**
- **Density approaching hand-crafted**
- **Ultra-fast speed — 70ps gates**
- **Lower power than competing products**
- **Interface flexibility — ECL, TTL and Analog I/O**
- **State-of-the-art CAD/CAE tool set (DAVE™)**
- **Major second-source**

SYSTEM ELEMENT ORGANIZATION

Memory Blocks

The SRAM blocks are direct functional and topological equivalents to Synergy's SY10474 ECL SRAM — the world's *fastest* memory. Each block has independent address, data and control lines, allowing the greatest flexibility. Asynchronous or synchronous operation is facilitated; data inputs and control lines are latched on the rising edge of the clock (CLK); if CLK is held low, latches are transparent and all operation is asynchronous. In the synchronous mode, the RAM can cycle continuously at 333MHz.

Logic Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, eliminating old style fixed "routing channels." Synergy's ASSET Technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device-to-device isolation; high interconnect density and routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains a bonding pad, input protection and configurable circuitry to accommodate a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be optionally configured for TTL levels.

Using these three building block types, new "base die" could be customized for particular customer requirements (contact factory for details).

Analog Zone

Yet another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple *analog* functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as Phase-Locked Loops, Digital-to-Analog Converters and Comparators may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. The *Analog Zone* makes high-performance **MIXED-SIGNAL ICs** a reality. Please review our list of macrocells in the Macrocell Library on page 2-6 of this data book.

SPEED/POWER PROGRAMMING

To provide the designer with the greatest flexibility, each logic macro may be programmed for any one of five *discrete* current switch/emitter-follower drive combinations (see Table 1). No inter-macro rerouting is necessitated when changing current levels.

Synergy's PEP/P™ design tools allow the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized. The speed/power options are initially assigned during schematic entry; default is option #1.

Option No.	I_{SW} (μA)	I_{OEF} (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 1.

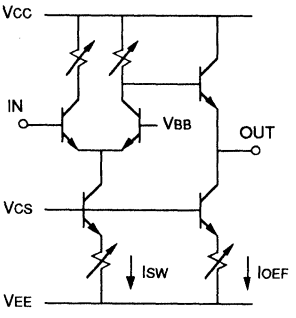


Figure 1.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 2 the typical propagation delays associated with the 2-input multiplexer shown in Figure 2 (speed/power option #4; ref. Table 1, above). Customized macrocells may be developed to suit specialized customer requirements. Contact factory for more information.

2-INPUT MUX
(MUX2C)

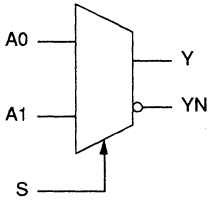


Figure 2.

From Input	To Output	Prop.Delay (ps, typ.)
A0	Y ↗	140
A0	Y ↘	142
A0	YN ↗	134
A0	YN ↘	133
A1	Y ↗	142
A1	Y ↘	142
A1	YN ↗	126
A1	YN ↘	130
S	Y ↗	190
S	Y ↘	221
S	YN ↗	194
S	YN ↘	211

Table 2.

DESIGN TOOLS

Synergy's highly integrated Design and Verification Environment (DAVE™) provides the designer with unprecedented levels of flexibility and completeness in a highly "engineer friendly" framework. This open and ever improving system, based on the Cadence tool suite, features highly accurate timing models. Particular attention has been paid to the area of clock distribution within the IC.

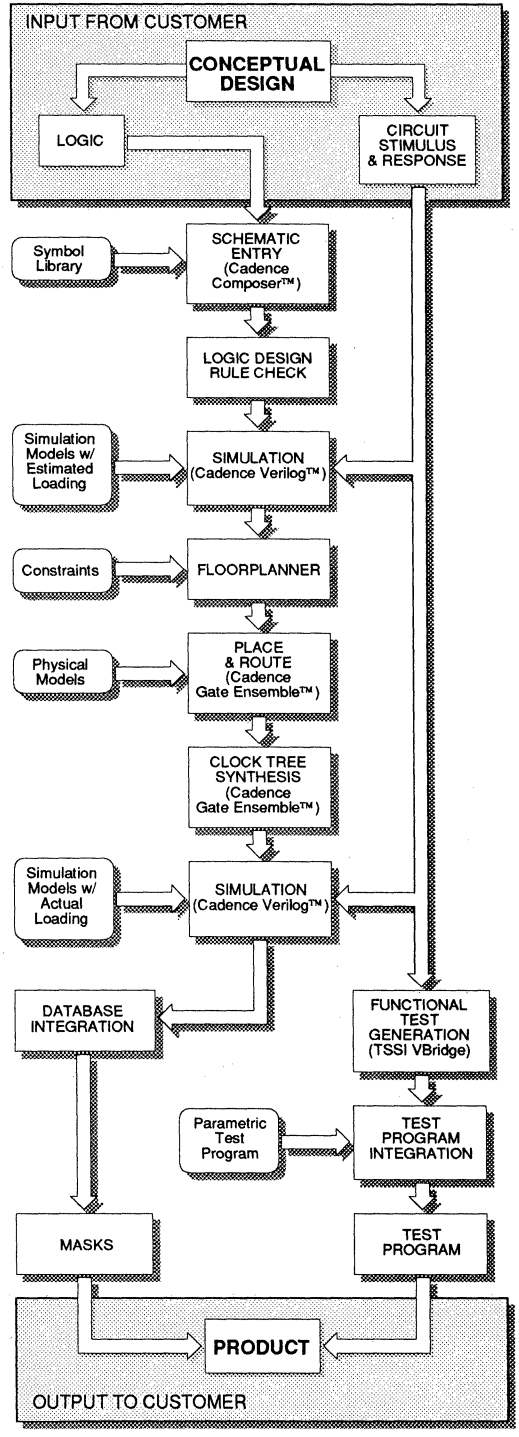
Synergy offers the customer a range of technical support services, up to and including complete "turnkey" design on both the RISE and USE series of devices.

Shown at right with references to the appropriate Cadence and Synergy software packages, DAVE also offers advanced RAM compilation capabilities (in *addition* to SRAM blocks), PEP/P power management and improved floorplanning. Future developments include the capabilities to support schematic entry and simulation using Mentor software tools.

PACKAGING

To best preserve the ultra-high-frequency capabilities of the System Element family, Synergy has developed new *molded* packages which feature the same junction/air thermal impedance (θ_{JA}) as a conventional co-fired ceramic package of the same physical size, but with only **one-third** of the package-imposed propagation delay.

System Elements are available in either Pin Grid Arrays (PGA) for through-hole mounting, or in Quad Flatpacks (QFP) for surface mounting. Some packages feature an integral copper heat spreader; for increased power dissipation, an external heat sink may be directly attached to the spreader. Optionally available is an integral TapePak® carrier ring to facilitate test and burn-in, and provide the QFPs with an additional level of handling protection.



INTRODUCTION

We make it easy to design SYSTEM ELEMENTS™. Synergy's customers are offered a variety of interfaces to meet a range of needs. Our Semicustom engineering staff can provide anything you may require; from applications assistance through a full *turnkey* solution, we're at your *service.*

DESIGN INTERFACE

Synergy offers three basic design interfaces:

— Turnkey
— Joint
— External

The selection of interface is made by the customer after considering his/her available resources, access to the necessary design environment, unusual circuit requirements, and scheduling demands. "Customized" interfaces can be developed to meet specialized needs.

For each type of interface, the respective responsibilities of each party are outlined in the table below. During *any* design interface, Synergy's Semicustom applications engineers are available to aid, guide and assist you in any way required.

FACILITIES

Conveniently located in the heart of Silicon Valley, Synergy's Customer Design Center is available to customers implementing Semicustom designs using our powerful new family of System Elements. Private design offices are assigned for the duration of a project, and are accessible 24 hours per day, 365 days per year. Each office contains a Sun SPARCstation and a 19-inch high-resolution color monitor. And, of course, applications engineering support is on-site.

The software which implements the front-end of Synergy's Design Automation & Verification Environment (DAVE™) system is installed on the Design Center network and may be readily accessed by any workstation in the Center. The available software products include the following:

— Synergy **DAVE**
— Cadence **Composer** Design Entry
— Cadence HDL Simulator Interface
— Cadence **VERILOG XL** Logic Simulator
— Cadence **Design Framework II**
— Synergy **Logic Design Rule Checker** (LDRC)
— Synergy **ORCA**™ RAM Compiler

	Customer	Synergy
Turnkey	Supplies logic diagrams/circuit schematics and simulation vectors Provides guidance and consultation Approves final simulation	 Performs schematic entry Performs pre-route simulation Performs Place and Route Performs post-route (final) simulation
Joint	Supplies logic diagrams/circuit schematics and simulation vectors Performs schematic entry Performs pre-route simulation Provides placement constraints Performs final simulation Approves final simulation	Provides aid, guidance and assistance Performs Place and Route Provides actual RC values via back-annotated netlist
External	Performs schematic entry Performs pre-route simulation Performs Place and Route Performs post-route (final) simulation Provides final data tape	Provides aid, guidance and assistance

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OR/NOR FAMILY

Name	Description	BC	OPT
OR1	1-Input OR	2	5
OR2	2-Input OR	2	5
OR3	3-Input OR	2	5
OR4	4-Input OR	2	5
NOR1	1-Input NOR	2	5
NOR2	2-Input NOR	2	5
NOR3	3-Input NOR	2	5
NOR4	4-Input NOR	2	5
OR1C	1-Input OR/NOR	3	5
OR2C	2-Input OR/NOR	3	5
OR3C	3-Input OR/NOR	3	5
OR4C	4-Input OR/NOR	3	5
OR6C	6-Input OR/NOR	3	5
OR8C	8-Input OR/NOR	4	5
OR12C	12-Input OR/NOR	5	5
OR16C	16-Input OR/NOR	6	5
OR1D	1-Input OR, Diff. – Diff.	3	5
OR2D	2-Input OR, Diff. – Diff.	4	5
OR1AD	1-Input OR, S.E. – Diff.	3	5
OR2AD	2-Input OR, S.E. – Diff.	3	5
OR1BD	1-Input OR/NOR, Diff. – Cmpl.	3	5
OR2BD	2-Input OR/NOR, Diff. – Cmpl.	4	5

OR-AND/NAND FAMILY

Name	Description	BC	OPT
OA11	1-1 OR-AND	2	5
OA21	2-1 OR-AND	2	5
OA22	2-2 OR-AND	3	5
OA22	3-3 OR-AND	3	5
OA22222	2-2-2-2-2 OR-AND	5	5
OA222222	2-2-2-2-2-2 OR-AND	6	5
OAI11	1-1 OR-NAND	2	5
OAI21	2-1 OR-NAND	2	5
OAI22	2-2 OR-NAND	3	5
OAI33	3-3 OR-NAND	3	5
OA11C	1-1 OR-AND/NAND	3	5
OA21C	2-1 OR-AND/NAND	4	5
OA22C	2-2 OR-AND/NAND	4	5

OR-AND/NAND FAMILY (CONT'D.)

Name	Description	BC	OPT
OA33C	3-3 OR-AND/NAND	4	5
OA44C	4-4 OR-AND/NAND	4	5
OA111C	1-1-1 OR-AND/NAND	4	5
OA222C	2-2-2 OR-AND/NAND	5	5
OA333C	3-3-3 OR-AND/NAND	5	5
OA444C	4-4-4 OR-AND/NAND	6	5
OA1111C	1-1-1-1 OR-AND/NAND	5	5
OA2222C	2-2-2-2 OR-AND/NAND	6	5
OA3333C	3-3-3-3 OR-AND/NAND	6	5
OA4321C	4-3-2-1 OR-AND/NAND	6	5
OA54321C	5-4-3-2-1 OR-AND/NAND	8	5

XOR/XNOR FAMILY

Name	Description	BC	OPT
XOR2C	2-Input XOR/XNOR	4	5
XOR2	2-Input XOR	3	5
XOR3	3-Input XOR	4	5
XOR4	4-Input XOR	5	5
XNR2	2-Input XNOR	3	5
XNR3	3-Input XNOR	4	5
XNR4	4-Input XNOR	5	5
XOR22C	2-2 OR-XOR/XNOR	4	5

MUX FAMILY

Name	Description	BC	OPT
MUX2C	2-Input MUX, Cmpl.	3	5
MUX4	4-Input MUX	6	5
MUX2D	2-Input MUX, Diff.	4	5
MUX2E	2-Input MUX w/ENA	3	5

DECODER FAMILY

Name	Description	BC	OPT
DCD24	2-4 Decoder (High)	8	5
DCD24E	2-4 Decoder (High) w/ENA (High)	10	5
DCD24A	2-4 Decoder (Low)	5	5
DCD24AE	2-4 Decoder (Low) w/ENA (Low)	7	5

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ADDER FAMILY

Name	Description	BC	OPT
ADDH	1-Bit Half Adder	4	5
ADDF	1-Bit Full Adder	5	5

CLOCK DISTRIBUTION BUFFER FAMILY

Name	Description	BC	OPT
CBUF	Clock Dist. Buffer, S.E.	3	1
CBUFD	Clock Dist. Buffer, Diff. – Diff.	4	1
CBUFI	Clock Dist. Buffer, S.E., Inv.	3	1
CBUFAD	Clock Dist. Buffer, S.E. - Diff.	4	1
CBUFBD	Clock Dist. Buffer, Diff. – S.E.	3	1

DELAY BUFFER FAMILY

Name	Description	BC	OPT
DLYE	Fixed Delay w/Enab., Diff – Diff.	3	5
DLY1	Delay Buffer, 800ps	3	1
DLY1D	Diff. Delay Buffer, 800ps	3	1
ADJ40D	Diff. Delay Buffer, Adj.	4	3

MEGACELL FAMILY

Name	Description	BC	OPT
PLL	Phase-Locked Loop	*	*
DAC3	3-Bit Digital-to-Analog Converter	*	*
DAC4	4-Bit Digital-to-Analog Converter	*	*
DAC5	5-bit Digital-to-Analog Converter	*	*
DAC6	6-Bit Digital-to-Analog Converter	*	*
DAC8	8-Bit Digital-to-Analog Converter	*	*
ADJDAC8	Adjustable 8-Bit DAC	*	*
RAM4K	4K-Bit 1-Port Embedded RAM	—	1
RAM1P	Single-Port Compiled RAM	*	*
REGFILE	Compiled Register File	*	*
ROM	Compiled Read-Only Memory	*	*
ACTEST	AC Delay Chain Monitor	20	1

*Contact factory for more information

LATCH FAMILY

Name	Description	BC	OPT
DLATRC	D-Latch w/Reset, Cmpl.	4	5
DLAT1D	DLATRC w/Reset & Diff. Ck.	7	5
SRLATD	Diff. S-R Latch	6	5

FLIP-FLOP FAMILY

Name	Description	BC	OPT
DFFRC	D-FF w/Reset, Cmpl.	6	5
DFFRSC	D-FF w/Set & Reset Cmpl.	6	5
DFF1D	D-FF w/Reset & Diff. Ck.	7	5
DFFRD	D-FF w/Reset & Diff. D, Ck., Out	7	5

ANALOG FAMILY

Name	Description	BC	OPT
VCO	Voltage-Controlled OSC	*	*
QPUMP	Charge Pump	*	*
PHDETL	Phase/Freq. Detector (LO-F)	*	*
PHDETH	Phase/Freq. Detector (HI-F)	*	*
COMPHI	Hi-Gain Voltage Comparator	*	*
COMPLO	Lo-Gain Voltage Comparator	*	*
LINVRMP	Linear Voltage-Ramp Generator	*	*
AGAMP20	AGC Amplifier (20db)	*	*
SUMAMP	Summing Amplifier	*	*
PEAKDET	Peak Detector	*	*
AGCTRLR	AGC Amp Controller	*	*
IVCONV	Current-to-Voltage Converter	*	
VDLY	Variable Delay, Diff. – Diff.	*	*
VDLYE	Variable Delay w/Enab., Diff. – Diff.	*	*
TMPMON	Int. Temp. Monitor Diode	1	1
GNDMON	GND Bus Sense Monitor	1	1
VEEMON	VEE Bus Sense Monitor	1	1

*Contact factory for more information.

I/O MACROCELLS

ECL BUFFER FAMILY — 10KH

Name	Description	IO	OPT
IBE	ECL Input	1	1
IBED	ECL Input, Diff. – Diff.	2	1
IBEAD	ECL Input, S.E. – Diff.	1	1
IBECK	ECL Input, Clock	1	1
IBECKD	ECL Input, Clock Diff. – Diff.	2	1
IBECKAD	ECL Input, Clock S.E. – Diff.	1	1
IBECKBD	ECL Input, Clock, Diff. – Cmpl.	1	1
OBE	ECL Output, 50 Ohm	1	1
OBED	ECL Output, Diff. – Diff.	2	1
OBEAD	ECL Output, Single – Diff.	2	1
OBEBD	ECL Output, Diff. – Single	1	1
OBER	ECL Output, OBE w/Edge Rate	1	1
OBERD	OBED w/Edge Rate	2	1
OBEARD	OBEAD w/Edge Rate	2	1
OBEBRD	OBEBD w/Edge Rate	1	1
OBET	ECL Output, Cut-Off w/Enable	1	1
OBETR	OBET w/Edge Rate	1	1
OBEMUX	ECL MUX Output	1	1
BBE	ECL Bi-Directional	1	1
BBER	ECL Bi-Directional, Edge Rate	1	1
BBED	ECL Bi-Di., Diff. – S.E. – Diff.	1	1
BBERD	BBED w/Edge Rate	1	1

TTL BUFFER FAMILY

Name	Description	IO	OPT
IBT	TTL Input	1	1
OBT8	TTL Output, 8mA	1	1
OBT8T	TTL Output, Tri-State, 8mA	1	1
BBT8	TTL Bi-Directional, 8mA	1	1

PSEUDO-TTL BUFFER FAMILY

Name	Description	IO	OPT
IBP	Pseudo-TTL Input	1	1
OBP8	Pseudo-TTL Output, 8mA	1	1
OBP8T	Pseudo-TTL Output, Tri-St., 8mA	1	1
BBP8	Pseudo-TTL Bi-Directional, 8mA	1	1

ECL BUFFER FAMILY — 100KH

Name	Description	IO	OPT
IBE1	ECL Input	1	1
IBE1D	ECL Input, Diff. – Diff.	2	1
IBE1AD	ECL Input, S.E. – Diff.	1	1
IBE1CKD	ECL Input, Clock Diff. – Diff.	2	1
IBE1CKBD	ECL Input, Clock, Diff. – Cmpl.	1	1
OBE1	ECL Output, 50 Ohm	1	1
OBE1D	ECL Output, Diff. – Diff.	2	1
OBE1AD	ECL Output, Single – Diff.	2	1
OBE1BD	ECL Output, Diff. – Single	1	1
OBE1R	ECL Output, OBE1 w/Edge Rate	1	1
OBE1RD	OBE1D w/Edge Rate	2	1
OBE1ARD	OBE1AD w/Edge Rate	2	1
OBE1BRD	OBE1BD w/Edge Rate	1	1
OBE1T	ECL Output, Cut-Off w/Enable	1	1
OBE1TR	OBE1T w/Edge Rate	1	1
BBE1	ECL Bi-Directional	1	1
BBE1R	ECL Bi-Directional, Edge Rate	1	1
BBE1D	ECL Bi-Di., Diff. – S.E. – Diff.	1	1
BBE1RD	BBE1D w/Edge Rate	1	1

ANALOG I/O FAMILY

Name	Description	IO	OPT
OBA1X	Hi-Current Coax Driver	*	*
BBPAD	Direct Pad Connection	1	1
BBTEMP	Temperature Monitor Diode	1	1
BBPADP	BBPAD for VCC ± 5V	1	1
BBPADN	BBPAD for VEE ± 5V	1	1
OBVBB	10KH VBB Ref. Generator	1	1
OBVBB1	100K VBB Ref. Generator	1	1

TIE FAMILY

Name	Description	BC	OPT
TIE0	Tie Low	1	3
TIE1	Tie High	1	3
TIE0D	Tie Low, Differential	2	3

CLOCK LOAD FAMILY

Name	Description	BC	OPT
LOAD2	2X Clock Load Cell	1	1
LOAD4	4X Clock Load Cell	1	1
LOAD2D	2X Diff. Clock Load	2	1
LOAD4D	4X Diff. Clock Load	2	1

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8 to 0	V_{dc}
V_I	Input Voltage (V_{CC} = 0V)	0 to V_{EE}	V_{dc}
I_{OUT}	Output Current Continuous Surge	 50 100	mA
T_A	Operating Temperature Range	0 to +85	°C
V_{EE}	Operating Range (2)	–5.7 to –4.2	V

NOTES:

1. Beyond which device life may be impaired unless specified otherwise on individual data sheet.
2. Parametric values specified at 100E Series: –4.2V to –5.46V, 10E Series: –4.94V to –5.46V.

10KH DC ELECTRICAL CHARACTERISTICS

V_{EE} = -5.2V ± 5%; V_{CC} = V_{CCO} = GND(1)

		T_A = 0°C		T_A = +25°C		T_A = +75°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1020	–840	–980	–810	–920	–735	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1630	–1950	–1630	–1950	–1600	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1070	–735	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	–1950	–1445	mV
I_{IL}	Input LOW Current	—	120	—	120	—	120	—	120	µA

NOTE:

1. 10K series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts, except bus outputs which, where specified, are terminated into 25Ω.

100K DC ELECTRICAL CHARACTERISTICS

V_{EE} = -4.5V ±5%; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–995	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL} (Min.)	50Ω to –2.0V
V_{OHA}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	
V_{OLA}	Output LOW Voltage	—	—	–1610	mV	or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	—	60	100	µA	V_{IN} = V_{IL} (Min.)	

101K DC ELECTRICAL CHARACTERISTICS

V_{EE} = -5.2V ±5%; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–995	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL} (Min.)	50Ω to –2.0V
V_{OHA}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	
V_{OLA}	Output LOW Voltage	—	—	–1610	mV	or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	—	70	120	µA	V_{IN} = V_{IL} (Min.)	

ECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
I_{IH}	Input HIGH Current[1]	—	150	—	150	—	150	µA
I_{EE}	Power Supply Current 10KH, 100K, 101K I/O	(Refer to individual System Element data sheets.)						

NOTE:

1. Each single-ended input has internal 50KΩ pull-down to V_{EE}; Differential inputs have 50KΩ pull-down on non-inverting (+) input and 50KΩ pull-up (to Vcc) on inverting input(-).

TTL DC ELECTRICAL CHARACTERISTICS

Single Supply: V_{CC} = V_{CCO} = +4.75V to +5.25V; V_{EE} = GND
Split Supplies: V_{EE} = –4.2V to –4.8V (100K), –4.94V to –5.46V (10KH, 101K); V_{CC} = V_{CCO} = GND; V_{TT} = +4.75V to +5.25V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input LOW Voltage	—	—	0.8	V	—
V_{IH}	Input HIGH Voltage	2.0	—	—	V	—
I_{IL}	Input LOW Current[1]	—	—	-600	µA	V_{IN} = 0.5V
I_{IH}	Input HIGH Current	—	—	20	µA	V_{IN} = 2.4V
		—	—	200		V_{IN} = 5.5V
V_{OL}	Output LOW Voltage					
	OBT8, OBT8T, BBT8	—	—	0.5	V	I_{OL} = 8mA, Split Supplies, V_{TT} = 4.75V
	OBP8, OBP8T, BBP8	—	—	0.5	V	I_{OL} = 8mA, Single Supply, V_{CC} = 4.75V
	OBT16, OBT16T, BBT16[2]	—	—	0.5	V	I_{OL} = 16mA, Split Supplies, V_{TT} = 4.75V
	OBP16, OBP16T, BBP16[2]	—	—	0.5	V	I_{OL} = 16mA, Single Supply, V_{CC} = 4.75V
V_{OH}	Output HIGH Voltage	2.4	—	—	V	I_{OH} = –2.0mA, V_{CC} or V_{TT} = Min.
I_{OS}	Output Short Circuit Current[3]				mA	V_O = 0.5V, V_{CC} or V_{TT} = Max.
	8mA Outputs	–40	—	–100		
	16mA Outputs	–80	—	–160		
V_{IC}	Input Clamp Voltage	–0.1	—	–1.5	V	I_C = –18mA, V_{CC} or V_{TT} = Min.
I_{OZ}	Output Hi-Z Leakage Current					V_O = 0.5 – 2.4V, V_{CC} or V_{TT} = Max.
	OBTxT, OBPxT	—	—	–100	µA	
	BBTx, BBPx	—	—	–120	µA	

NOTE:

1. Each input has internal 15KΩ pull-up to positive supply.
2. These buffers consume two I/O cells each.
3. Only ONE output at a time may be shorted for more than one second.

UNIVERSAL SYSTEM ELEMENT (USE™)

FEATURES

- **Highest density logic via unique 6-transistor cell:**
  + greatest functionality per unit area
  + shortest propagation delays
- **888 core cells yield up to 1,665 *routeable* (equivalent) gates or 111 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) or in JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **32 I/O pins *plus* up to 32 power and ground pins**
- **Compatible with RAM-Intensive System Elements (RISE™)**

DESCRIPTION

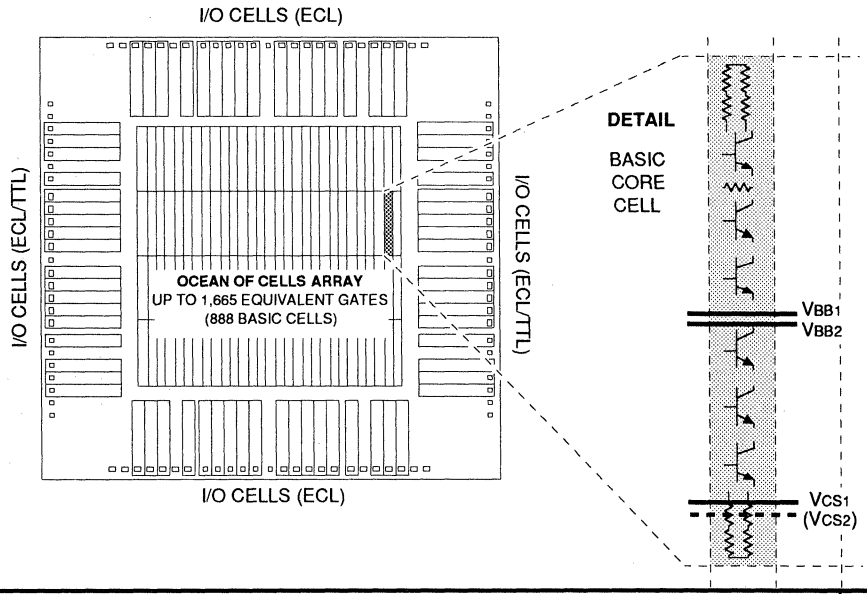
The SY1BP00 Universal System Element is the smallest member of Synergy's new System Element family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY1BP00 features up to 1,665 equivalent 2-input gates of 70ps logic and routinely achieves logic density in excess of 450 gates/square millimeter. The 32 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, hereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

With system clock frequencies above 1GHz, the Synergy System Element™ (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



Rev.: B Amendment: /0
Issue Date: February, 1994

SYSTEM ELEMENT ORGANIZATION

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 4 pins (e.g.: left = 4, right = 0; left = 4, right = 4; left = 0, right = 8; etc.).

Using these two building block types, new "base die" may be custom-configured to meet a customer's special requirements. Contact the factory for further details.

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Fast, highly-efficient SRAM blocks may be created for inclusion in the SY1BP00 by usig Synergy's unique ORCA™ RAM compiler; blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of USE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The SY1BP00 USE is available in 28-, 44- and 68-pin JEDEC-standard leaded chip carriers in either plastic (PLCC), ceramic (CERQUAD) or metal, all with conventional "J" leads with a 50mil (0.050") pitch. Also available are 48- and 64-pin Quad Flatpacks in either plastic (PQFP) or ceramic (CQFP). QFPs feature leads on a 25mil (0.025") pitch with "gull-wing" lead forming as standard.

Some packages feature an integral copper heat spreader. For increased power dissipation capability, an external heat sink may be readily attached to the spreader. Other packages could be made available for special customer requirements; contact Synergy for details.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

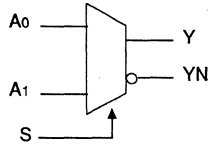


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output		Propagation Delay (ps, typical)
A0	Y	↓	140
A0	Y	↑	142
A0	YN	↓	134
A0	YN	↑	133
A1	Y	↓	142
A1	Y	↑	142
A1	YN	↓	126
A1	YN	↑	130
S	Y	↓	190
S	Y	↑	221
S	YN	↓	194
S	YN	↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

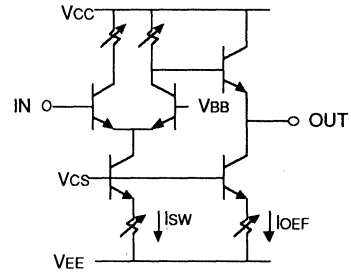


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

UNIVERSAL SYSTEM ELEMENT (USE™)

SY2BP00

FEATURES

- **Highest density logic via unique 6-transistor cell:**
  + greatest functionality per unit area
  + shortest propagation delays
- **2,184 core cells yield up to 3,640 *routeable* (equivalent) gates or 242 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) or in JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **56 I/O pins *plus* up to 32 power and ground pins**
- **Compatible with RAM-Intensive System Elements (RISE™)**

DESCRIPTION

The SY2BP00 Universal System Element is the smallest member of Synergy's new System Element family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY2BP00 features up to 3,640 equivalent 2-input gates of 70ps logic and routinely achieves logic density in excess of 450 gates/square millimeter. The 56 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, hereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

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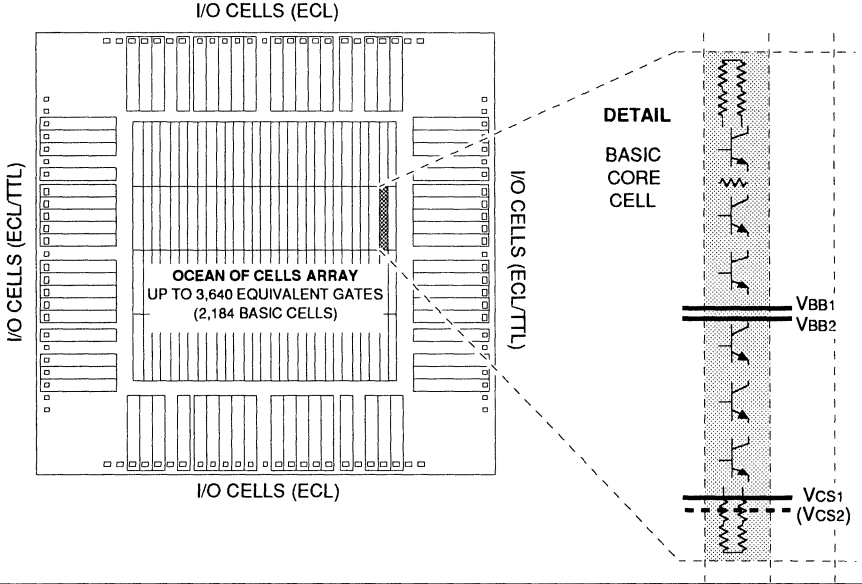

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I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (VEE). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 7 pins (e.g.: left = 7, right = 0; left = 7, right = 7; left = 0, right = 14; etc.).

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The SY2BP00 USE is available in 44- and 68-pin JEDEC-standard leaded chip carriers in either plastic (PLCC), ceramic (CERQUAD) or metal, all with conventional "J" leads with a 50mil (0.050") pitch. Also available are 48- and 64-pin Quad Flatpacks in either plastic (PQFP) or ceramic (CQFP) with leads on a 25mil (0.025") pitch , and 128-pin Quad Flatpacks in either plastic (PQFP) or metal (MQFP) with leads on a 0.8mm pitch. "Gull-wing" lead forming is standard on all QFPs.

Some packages feature an integral copper heat spreader. For increased power dissipation capability, an external heat sink may be readily attached to the spreader. Other packages could be made available for special customer requirements; contact Synergy for details.

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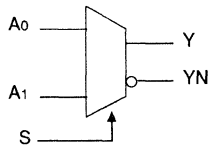

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A0	YN ↑	133
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A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

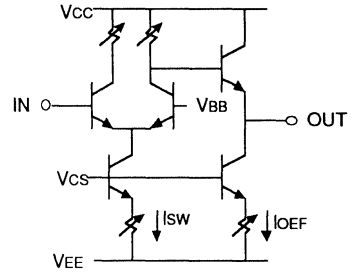


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

SYNERGY SEMICONDUCTOR

UNIVERSAL SYSTEM ELEMENT (USE™)

SY4BP00

FEATURES

- **Highest density logic via unique 6-transistor cell:**
  + greatest functionality per unit area
  + shortest propagation delays
- **5,180 core cells yield up to 9,065 *routeable* (equivalent) gates or 604 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) or in JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **80 I/O pins *plus* up to 40 power and ground pins**
- **Compatible with RAM-Intensive System Elements (RISE™)**

DESCRIPTION

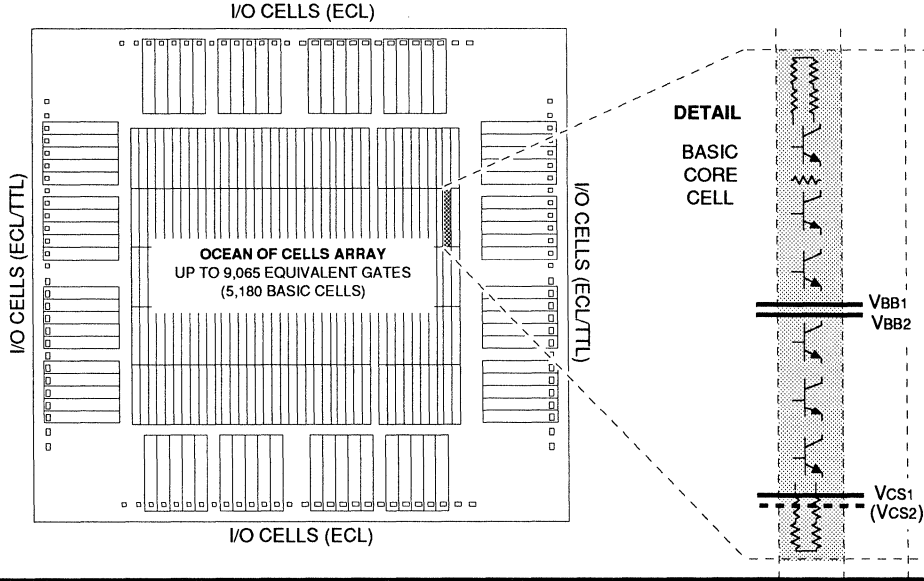
The SY4BP00 Universal System Element is a member of Synergy's new System Element family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY4BP00 features up to 9,065 equivalent 2-input gates of 70ps logic and routinely achieves logic density in excess of 450 gates/square millimeter. The 80 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, hereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

With system clock frequencies above 1GHz, the Synergy System Element™ (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



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SYSTEM ELEMENT ORGANIZATION

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 10 pins (e.g.: left = 10, right = 0; left = 10, right = 10; left = 0, right = 20; etc.).

Using these two building block types, new "base die" may be custom-configured to meet a customer's special requirements. Contact the factory for further details.

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Fast, highly-efficient SRAM blocks may be created for inclusion in the SY11BP00 by usig Synergy's unique ORCA™ RAM compiler; blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of USE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The SY4BP00 USE is available in 64- and 128-pin Quad Flatpacks in either plastic (PQFP), ceramic (CQFP) or metal (MQUAD —128-pin only). The 64-pin has a 0.480" square body with leads on a 25 mil (0.025") pitch. The 128-pin has a 28x28mm body with leads on a 0.80mm pitch. Both offer standard "gull-wing" lead forming. Some packages feature an integral copper heat spreader. For increased power dissipation capability, an external heat sink may be readily attached to the spreader.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

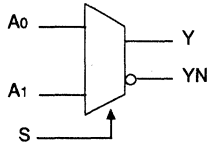


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↓	140
A0	Y ↑	142
A0	YN ↓	134
A0	YN ↑	133
A1	Y ↓	142
A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

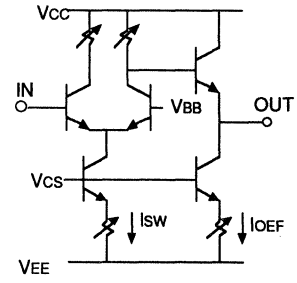


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

UNIVERSAL SYSTEM ELEMENT (USE™)

FEATURES

- **Highest density logic via unique 6-transistor cell:**
  + greatest functionality per unit area
  + shortest propagation delays
- **11,730 core cells yield up to 19,550 *routeable* (equivalent) gates or 1,303 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) or in JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **112 I/O pins *plus* up to 56 power and ground pins**
- **Compatible with RAM-Intensive System Elements (RISE™)**

DESCRIPTION

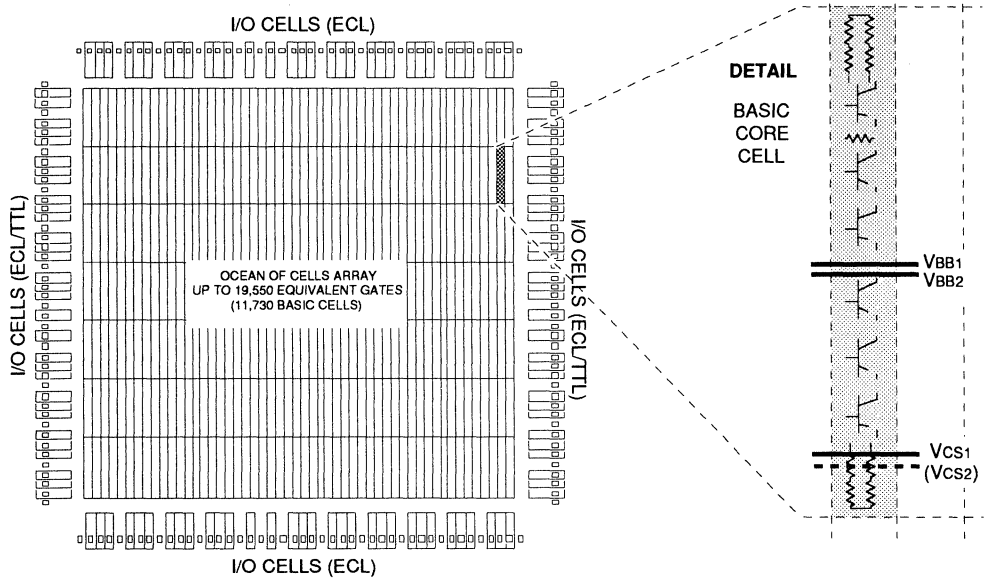
The SY11BP00 Universal System Element is a member of Synergy's new System Element family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY11BP00 features up to 19,550 equivalent 2-input gates of 70ps logic and routinely achieves logic density in excess of 450 gates/square millimeter. The 112 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, hereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

With system clock frequencies above 1GHz, the Synergy System Element™ (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



Rev.: B Amendment:/0
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SYSTEM ELEMENT ORGANIZATION

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 14 pins (e.g.: left = 14, right = 0; left = 14, right = 14; left = 0, right = 28; etc.).

Using these two building block types, new "base die" may be custom-configured to meet a customer's special requirements. Contact the factory for further details.

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Fast, highly-efficient SRAM blocks may be created for inclusion in the SY11BP00 by usig Synergy's unique ORCA™ RAM compiler; blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of USE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The SY11BP00 USE is available in 84-pin JEDEC-standard leaded chip carriers in either plastic (PLCC), ceramic (CERQUAD) or metal (MQUAD), all with conventional "J" leads with a 50mil (0.050") pitch. Also available are 128- and 160-pin Quad Flatpacks in either plastic (PQFP), ceramic (CQFP) or metal (MQUAD). QFPs have a 28x28mm body, leads on a 0.80mm (128-pin) or 0.65mm (160-pin) pitch, and "gull-wing" lead forming as standard.

To increase the power dissipation capability of any of the above packages, an external heat sink may be readily attached. Other packages could be made available for special customer requirements; contact Synergy for details.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

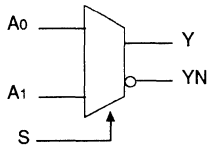


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↓	140
A0	Y ↑	142
A0	YN ↓	134
A0	YN ↑	133
A1	Y ↓	142
A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

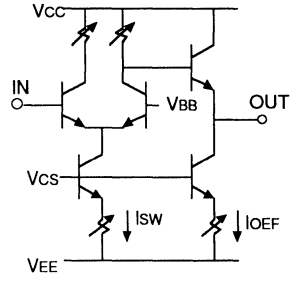


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

SYNERGY SEMICONDUCTOR

UNIVERSAL SYSTEM ELEMENT (USE™)

SY21BP00

FEATURES

- **Highest density logic via unique 6-transistor cell:**
  + greatest functionality per unit area
  + shortest propagation delays
- **20,680 core cells yield up to 33,605 *routeable* (equivalent) gates or 2,240 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) or in JEDEC-standard PLCCs**
- **I/O and V_{EE} compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **144 I/O pins *plus* up to 72 power and ground pins**
- **Compatible with RAM-Intensive System Elements (RISE™)**

DESCRIPTION

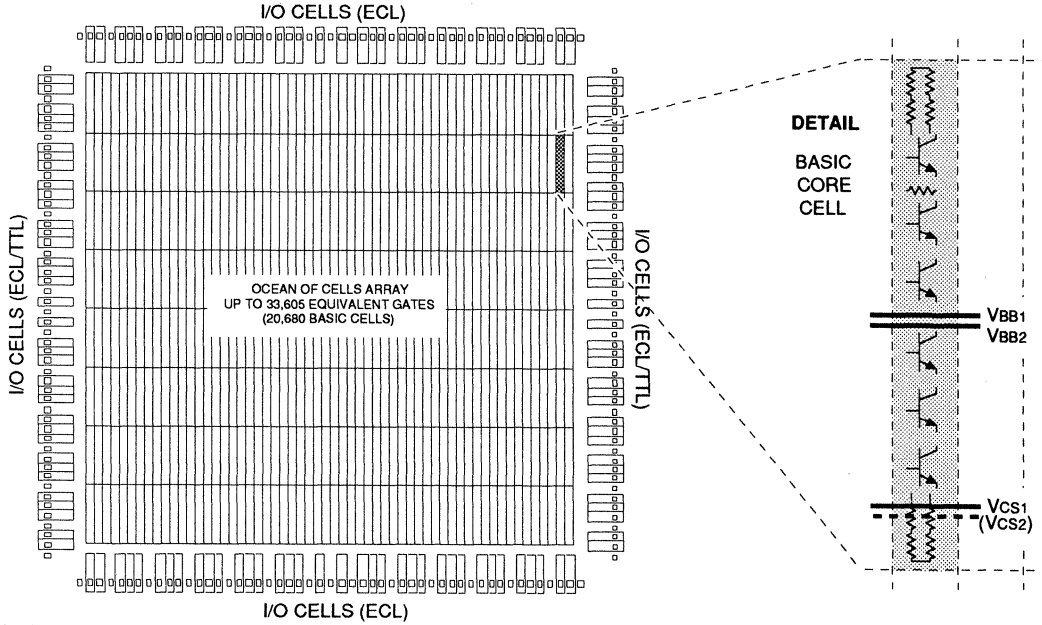
The SY21BP00 Universal System Element is a member of Synergy's new System Element family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY21BP00 features up to 33,605 equivalent 2-input gates of 70ps logic and routinely achieves logic density in excess of 450 gates/square millimeter. The 144 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, hereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

With system clock frequencies above 1GHz, the Synergy System Element™ (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



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SYSTEM ELEMENT ORGANIZATION

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 18 pins (e.g.: left = 18, right = 0; left = 18, right = 18; left = 0, right = 36; etc.).

Using these two building block types, new "base die" may be custom-configured to meet a customer's special requirements. Contact the factory for further details.

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Fast, highly-efficient SRAM blocks may be created for inclusion in the SY21BP00 by usig Synergy's unique ORCA™ RAM compiler; blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of USE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The highest performance would be obtained with the 208-pin PQFP which features an integral copper heat spreader. An external heat sink could be attached for increased power dissipation capability.

Package Type	Plastic	Ceramic	Metal	Body Size	Lead Pitch	Lead Form
Quad Flatpack	PQFP	CQFP	MQUAD			
128	X	X	X	28x28mm	0.8mm	Gull
160	X	X	X	28x28mm	0.65mm	Gull
208	X	X	X	28x28mm	0.5mm	Gull
Leaded Chip Carrier	PLCC	CLCC	—			
84	X	X		JEDEC	0.050"	"J"
Pin Grid Array	PPGA	—	—			
207	X			1.78x1.78"	0.100"	Pin

MACROCELL LIBRARY

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Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

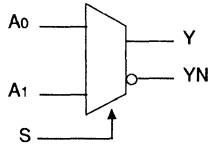

Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↓	140
A0	Y ↑	142
A0	YN ↓	134
A0	YN ↑	133
A1	Y ↓	142
A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

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To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

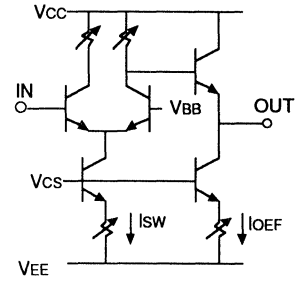


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

UNIVERSAL SYSTEM ELEMENT (USE™)

SY34BP00

FEATURES

- **Highest density logic via unique 6-transistor cell:**
  + greatest functionality per unit area
  + shortest propagation delays
- **37,854 core cells yield up to 63,090 *routeable* equivalent gates or 4,206 D-type flip-flops — largest available**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs)**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ ECAD system**
- **192 I/O pins *plus* up to 104 power and ground pins**
- **Compatible with RAM-Intensive System Elements (RISE™)**

DESCRIPTION

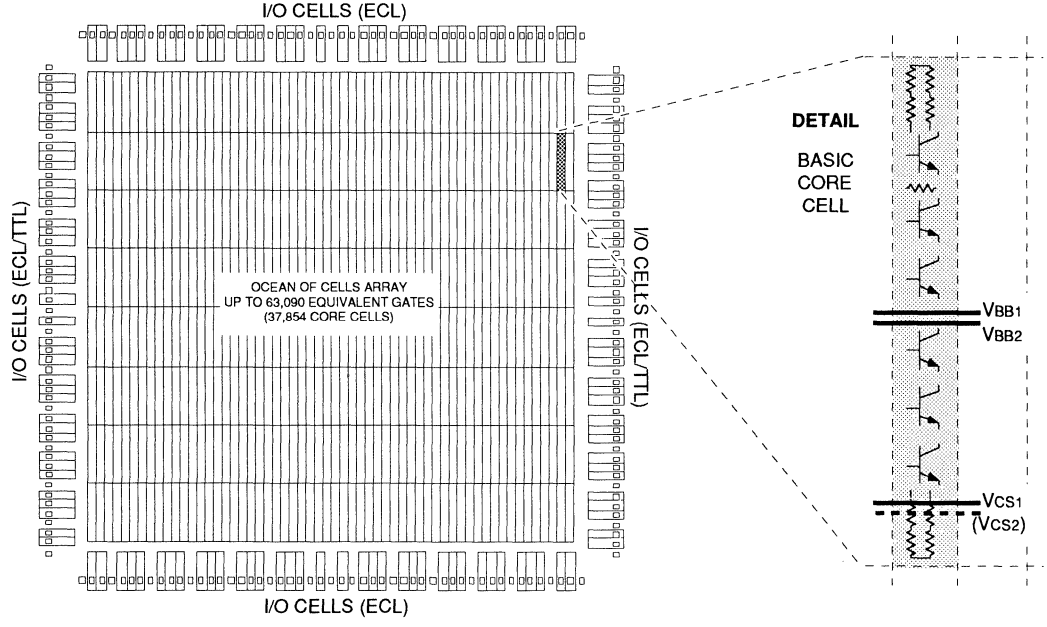
The SY34BP00 Universal System Element is a member of Synergy's System Elements™ family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY34BP00 features up to 63,090 equivalent 2-input gates of 70ps logic and routinely achieves logic density in excess of 450 gates/square millimeter. The 192 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, thereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of many analog functions.

With system clock frequencies above 1GHz, the Synergy System Elements (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



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SYSTEM ELEMENT ORGANIZATION

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 24 pins (e.g.: left = 24, right = 0; left = 24, right = 24; left = 0, right = 48; etc.).

Using these two building block types, new "base die" may be custom-configured to meet a customer's special requirements. Contact the factory for further details.

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Fast, highly-efficient SRAM blocks may be created for inclusion in the SY34BP00 by usig Synergy's unique ORCA™ RAM compiler; blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of USE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The SY34BP00 USE is available in PQFP (Plastic Quad Flatpack) or MQUAD (Metal Quad) with 240 or 304 leads. PQFPs have an embedded heat slug for improved power dissipation and simplified heat sink attachment (as needed). 240-pin packages have a 32x32mm body; the 304-pin packages have a 40x40mm body. All have leads on a 0.50mm pitch. Both PQFP and MQUAD are optionally available with an integral TapePak carrier ring to facilitate test and burn-in, plus providing the package with additional handling protection. The carrier ring is *recommended* to ensure lead co-planarity.

The SY34BP00 is also available in die form. Contact the factory for die details or with special package requirements.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

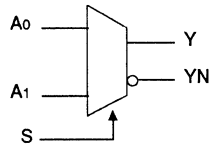


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↗	140
A0	Y ↘	142
A0	YN ↗	134
A0	YN ↘	133
A1	Y ↗	142
A1	Y ↘	142
A1	YN ↗	126
A1	YN ↘	130
S	Y ↗	190
S	Y ↘	221
S	YN ↗	194
S	YN ↘	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

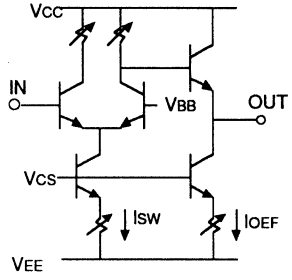


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

SYNERGY SEMICONDUCTOR

RAM INTENSIVE SYSTEM ELEMENT (RISE™)

ADVANCE INFORMATION
SY8BP4R2

FEATURES

- **3ns on-board SRAM; 8,192 bits total — alpha particle immune**
- **Highest density logic via unique 6-transistor cell + greatest functionality per unit area + shortest propagation delays**
- **7,578 core cells yield up to 12,630 *routeable* (equivalent) gates or 842 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) and JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **112 I/O pins *plus* up to 56 power and ground pins**
- **Fully compatible with Universal System Elements (USE™)**

DESCRIPTION

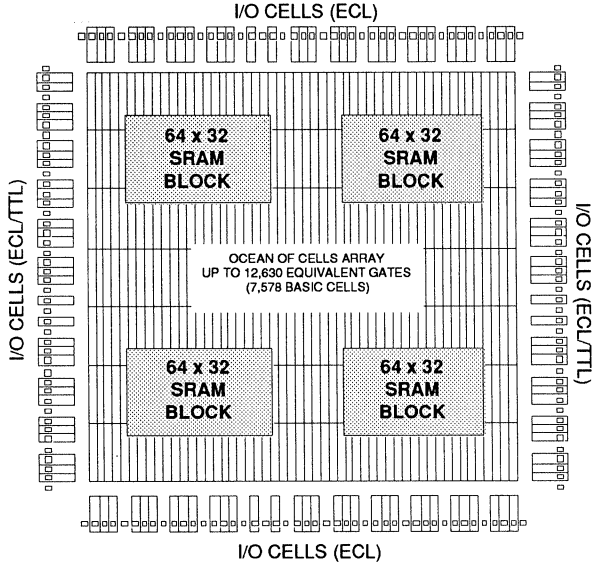
The SY8BP4R2 RAM-Intensive System Element is a member of Synergy's new System Element family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY8BP4R2 features four independent blocks of 3ns SRAM (each organized as 64-words-by-32-bits), plus up to 12,630 equivalent 2-input gates of 70ps logic. The 112 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, hereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

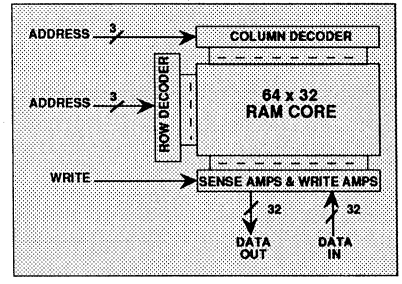
With system clock frequencies above 1GHz, the Synergy System Element™ (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



DETAIL
64 x 32 SRAM BLOCK



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SYSTEM ELEMENT ORGANIZATION

Memory Blocks

The four single-port SRAM blocks utilize a cell design similar to Synergy's SY10/100474 ECL SRAM — the world's fastest 4K memory. Each block features independent address, data in, data out and write control lines, allowing the user the greatest flexibility in design. Implemented in a synchronous system, these SRAMs can cycle continuously at over 300MHz.

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 14 pins (e.g.: left = 14, right = 0; left = 14, right = 14; left = 0, right = 28; etc.).

Using these two building block types, new "base die" may be custom-configured to meet a customer's special requirements. Contact the factory for further details.

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Additional, more specialized SRAM blocks may be created in the SY8BP4R2 by using Synergy's unique ORCA™ RAM compiler. Blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally-programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of RISE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The SY8BP4R2 RISE is available in 128- and 160-pin Quad Flatpacks in either plastic (PLCC), ceramic (CLCC) or metal (MQUAD). QFPs have a 28x28mm body, leads on a 0.80mm (128-pin) or 0.65mm (160-pin) pitch, and "gull-wing" lead forming as standard. Also available is an 84-pin JEDEC-standard leaded chip carrier in either plastic (PLCC), ceramic (CERQUAD), or metal (MQUAD), all with conventional "J" leads on a 50mil (0.050") pitch.

To increase the power dissipation capability of any of the above packages, an external heat sink may be readily attached. Other packages could be made available for special customer requirements; contact Synergy for details.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

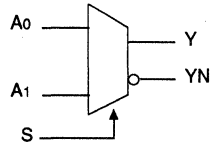


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↓	140
A0	Y ↑	142
A0	YN ↓	134
A0	YN ↑	133
A1	Y ↓	142
A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

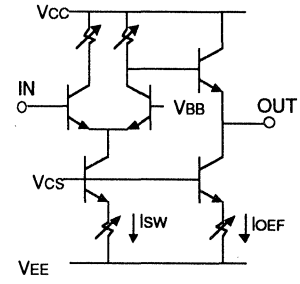


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

RAM INTENSIVE SYSTEM ELEMENT (RISE™)

SY9BP6R4

FEATURES

- **3ns on-board SRAM; 24K bits total — alpha particle immune**
- **Highest density logic via unique 6-transistor cell + greatest functionality per unit area + shortest propagation delays**
- **7,410 core cells yield up to 12,480 *routeable* (equivalent) gates or 832 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) and plastic PGAs, or in JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ CAE system**
- **144 I/O pins *plus* up to 72 power and ground pins**
- **Fully compatible with Universal System Elements (USE™)**

DESCRIPTION

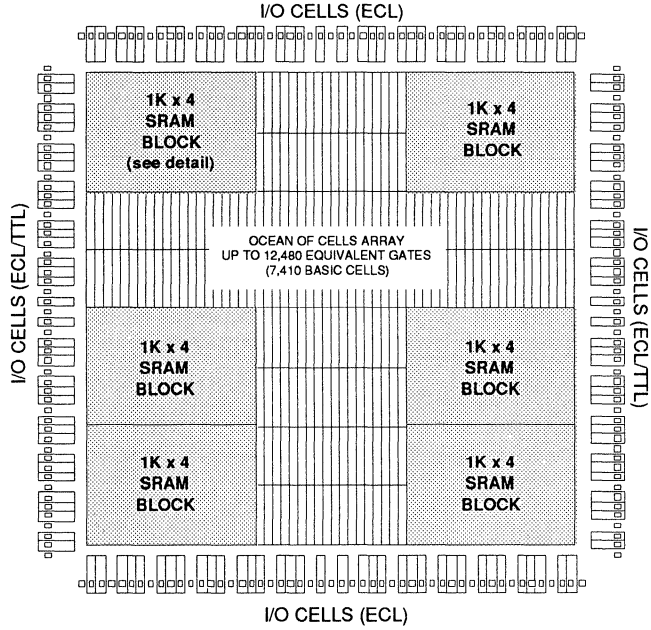
The SY9BP6R4 RAM-Intensive System Element is a member of Synergy's new System Elements™ family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY9BP6R4 features six independent blocks of 3ns SRAM (each organized as 1K-words-by-4-bits), plus up to 12,480 equivalent 2-input gates of 70ps logic. The 144 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, thereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of simple analog functions.

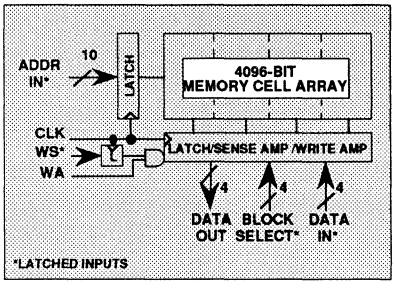
With system clock frequencies above 1GHz, the Synergy System Elements (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



DETAIL
1K x 4 SRAM BLOCK



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Issue Date: February, 1994

SYSTEM ELEMENT ORGANIZATION

Memory Blocks

The six SRAM blocks are direct functional and topological equivalents to Synergy's SY10/100474 ECL SRAM — the world's fastest 4K memory. Each block features independent address, data and control lines, allowing the user the greatest flexibility. Both synchronous and asynchronous operation is facilitated: data inputs and all control lines are latched on the rising edge of the clock (CLK). If CLK is held low, latches are transparent and all operations are asynchronous. In the synchronous mode, the RAM can cycle continuously at 333MHz.

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 18 pins (e.g.: left = 18, right = 0; left = 18, right = 18; left = 0, right = 36; etc.).

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops and/or 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Additional, more specialized SRAM blocks may be created in the SY8BP4R2 by using Synergy's unique ORCA™ RAM compiler. Blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally-programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of RISE, Synergy has developed new molded packages featuring low junction/air thermal impedance — with only one-third the package-imposed propagation delay as a co-fired ceramic package of the same physical size.

The highest performance would be obtained with the 208-pin PQFP, which features an integral copper heat spreader. An external heat sink could be attached for increased power dissipation capability.

Package Type	Plastic	Ceramic	Metal	Body Size	Lead Pitch	Lead Form
Quad Flatpack	PQFP	CQFP	MQUAD			
128	X	X	X	28x28mm	0.8mm	Gull
160	X	X	X	28x28mm	0.65mm	Gull
208	X	X	X	28x28mm	0.5mm	Gull
Leaded Chip Carrier	PLCC	CLCC	—			
84	X	X		JEDEC	0.050"	"J"
Pin Grid Array	PPGA	—	—			
207	X			1.78x1.78"	0.100"	Pin

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

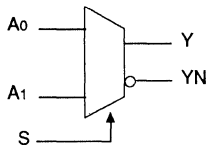


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↓	140
A0	Y ↑	142
A0	YN ↓	134
A0	YN ↑	133
A1	Y ↓	142
A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

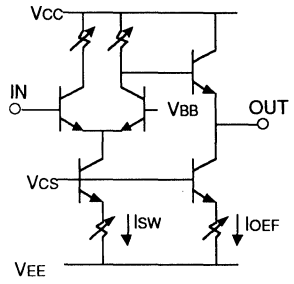


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

Table 2.

SYNERGY SEMICONDUCTOR

RAM INTENSIVE SYSTEM ELEMENT (RISE™)

PRELIMINARY
SY15BP10R4

FEATURES

- **3ns on-board SRAM; 40K bits total — alpha particle immune**
- **Highest density logic via unique 6-transistor cell + greatest functionality per unit area + shortest propagation delays**
- **15,659 core cells yield up to 23,946 *routeable* (equivalent) gates or 1,596 D-type flip-flops**
- **CAD-programmable speed/power options**
- **Available in high-performance Quad Flatpacks (QFPs) and plastic PGAs, or in JEDEC-standard PLCCs**
- **I/O and VEE compatible with 10K or 100K ECL logic**
- **Direct interface with TTL buses and control signals**
- **Mixed-signal capabilities in proprietary ANALOG ZONE™**
- **Advanced ASSET™ technology — 70ps (typ.) gate delay**
- **Higher engineering productivity with DAVE™ ECAD system**
- **192 I/O pins *plus* up to 104 power and ground pins**
- **Fully compatible with Universal System Elements (USE™)**

DESCRIPTION

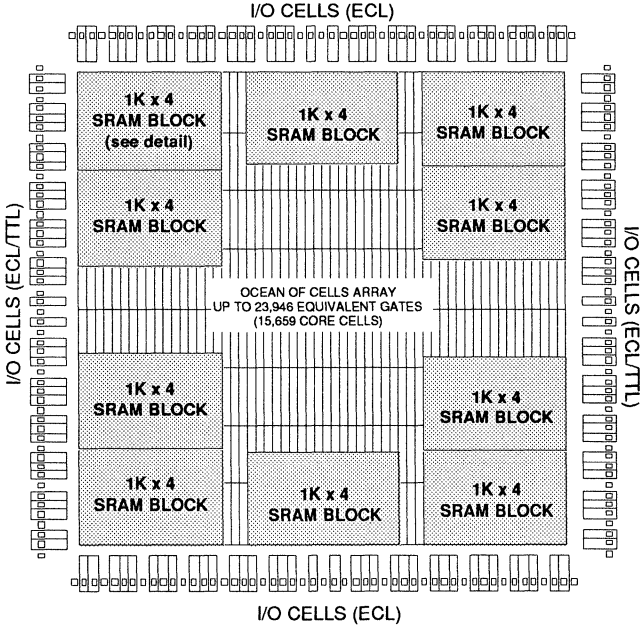
The SY15BP10R4 RAM-Intensive System Element is a member of Synergy's System Elements™ family. Fabricated in the ASSET I bipolar process, these high-performance VLSI components offer an unprecedented combination of circuit density, interface flexibility and minimal propagation delay logic — while dissipating significantly less power than competing products.

The SY15BP10R4 features ten independent blocks of 3ns SRAM (each organized as 1K-words-by-4-bits), plus up to 23,946 equivalent 2-input gates of 70ps logic. The 192 I/O pins may be configured with all pins ECL logic-level-compatible (10K or 100K), or with up to half the pins compatible with TTL levels, thereby eliminating the need for external ECL/TTL translators. Further, the unique OCEAN OF CELLS™ logic structure allows for on-chip implementation of many analog functions.

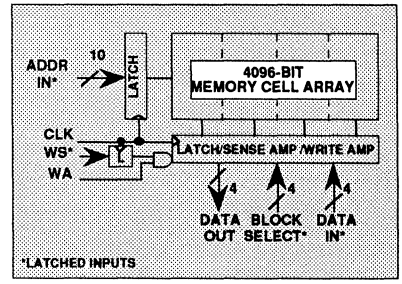
With system clock frequencies above 1GHz, the Synergy System Elements (SSE) family is ideally suited for such demanding high-speed applications as mainframe and supermini computers, graphic workstations and servers, automatic test equipment, optical communications and many military systems.

Supported by Synergy's Design and Verification Environment (DAVE), an advanced system of integrated design tools, these products offer the designer much higher levels of high-performance system integration and design productivity.

BLOCK DIAGRAM



DETAIL
1K x 4 SRAM BLOCK



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SYSTEM ELEMENT ORGANIZATION

Memory Blocks

The ten SRAM blocks are direct functional and topological equivalents to Synergy's SY10/100474 ECL SRAM — the world's fastest 4K memory. Each block features independent address, data and control lines, allowing the user the greatest flexibility. Both synchronous and asynchronous operation is facilitated: data inputs and all control lines are latched on the rising edge of the clock (CLK). If CLK is held low, latches are transparent and all operations are asynchronous. In the synchronous mode, the RAM can cycle continuously at 333MHz.

Core Cells

System Elements use a 6-transistor cell, arranged in an innovative OCEAN OF CELLS, which eliminates "routing channels". Synergy's All Spacer-Separated Element Transistor (ASSET) technology, coupled with an innovative (patent pending) transistor structure, produces several significant advantages: very small, very fast (17GHz) devices; high device/device isolation; and high interconnect density/routing efficiency. Logic macros are normally implemented by combining horizontally adjacent cells.

I/O Cells

Each cell contains bond pad, input protection and configurable circuitry to match a variety of standard logic families. I/O levels conform to 10K standards at –5.2V, and to 100K standards at –4.5V and –5.2V (V_{EE}). Additionally, I/Os located at the left and right sides of the die may be configured for TTL levels. TTL I/O is implemented in groups of 24 pins (e.g.: left = 24, right = 0; left = 24, right = 24; left = 0, right = 48; etc.).

ANALOG ZONE

Another benefit of the OCEAN OF CELLS architecture is the ability to craft the individual ASSET transistors and available resistors into simple analog functions, further reducing external circuitry. In close cooperation with Synergy's applications engineers, such functions as comparators, phase-locked loops, 3- to 8-bit digital-to-analog converters may be implemented. Special care must be taken to ensure testability and adequate digital/analog isolation. Contact the factory for further information on analog capabilities. Refer to our Macrocell Library listing.

DESIGN TOOLS

Synergy's highly-integrated design environment (DAVE) provides the bipolar system designer with unprecedented levels of flexibility and completeness in a highly "engineer-friendly" framework. This open system, based on the Cadence tool suite, features highly-accurate timing models. Synergy offers the customer a range of technical support services, up to (and including) complete "turnkey" designs on both RISE and USE devices.

Additional, more specialized SRAM blocks may be created in the SY15BP10R4 by using Synergy's unique ORCA™ RAM compiler. Blocks from 8x8 to 64x40 (or 128x20) can be implemented using only the normally-programmed (metal) layers of the device.

PACKAGING

To best preserve the high-frequency capabilities of USE, Synergy has developed new molded packages which feature low junction/air thermal impedance with only one-third the package-imposed propagation delay as a conventional co-fired ceramic package of the same physical size.

The SY15BP10R4 USE is available in PQFP (Plastic Quad Flatpack) or MQUAD (Metal Quad) with 240 or 304 leads. PQFPs have an embedded heat slug for improved power dissipation and simplified heat sink attachment (as needed). 240-pin packages have a 32x32mm body; the 304-pin packages have a 40x40mm body. All have leads on a 0.50mm pitch. Both PQFP and MQUAD are optionally available with an integral TapePak carrier ring to facilitate test and burn-in, plus providing the package with additional handling protection. The carrier ring is *recommended* to ensure lead co-planarity.

The SY15BP10R4 is also available in die form. Contact the factory for die details or with special package requirements.

MACROCELL LIBRARY

In the rarefied world of systems clocking at 1GHz and above, Synergy has the view that the most important attribute of a logic macrocell is the accuracy of the cell's timing model as applied to circuit simulation. It is deemed as imperative that the final simulation MUST accurately reflect the behavior of the silicon. Accordingly, Synergy's ever-growing library of macrocells has been painstakingly crafted to ensure absolute timing accuracy. The innovative cell architecture makes possible very compact macros, yielding very high levels of performance. For example, note in Table 1 the typical propagation delays associated with the 2-input multiplexer shown in Figure 1 (speed/power option #4).

Customized macrocells may be developed to suit customers' specialized needs; contact factory for information.

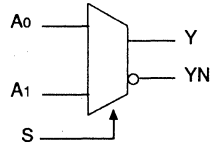


Figure 1. 2-Input MUX (MUX2C)

From Input	To Output	Propagation Delay (ps, typical)
A0	Y ↓	140
A0	Y ↑	142
A0	YN ↓	134
A0	YN ↑	133
A1	Y ↓	142
A1	Y ↑	142
A1	YN ↓	126
A1	YN ↑	130
S	Y ↓	190
S	Y ↑	221
S	YN ↓	194
S	YN ↑	211

Table 1.

SPEED/POWER PROGRAMMABILITY

To provide the designer with the greatest flexibility, each logic macro may be programmed for one of five discrete current-source/emitter-follower drive combinations (see Table 2). No chip rerouting is necessitated when changing current levels. Synergy's PEP/P™ design tool allows the designer to immediately evaluate the propagation delay impact of various current drives; hence, overall power is minimized and critical path(s) speed is maximized. The speed/power options are initially assigned during schematic capture; default is option #1.

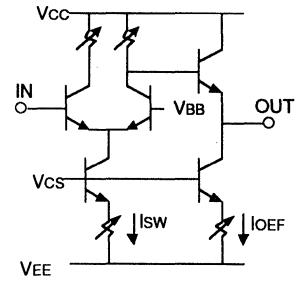


Figure 2.

Option #	Isw (μA)	Ioef (μA)
1	70	70
2	130	130
3	130	240
4	240	240
5	240	470

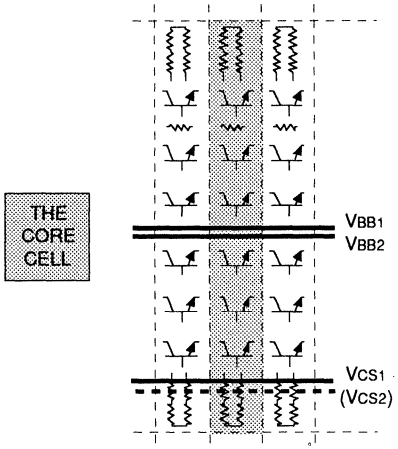
Table 2.

INTRODUCTION

Synergy's SYSTEM ELEMENT™ family provides the high-performance system designer with an unprecedented combination of speed, circuit density and low power dissipation in semi-custom circuits. Adding the flexibility to integrate SRAM blocks (both *embedded* and metal-only *compiled*), and to intermix ECL I/O with TTL I/O, achieves new highs in circuit efficiency. Now, the ultimate: The ANALOG ZONE™ — the unique capability of System Elements to implement true **mixed-signal** designs in metal-mask-personalized (semi-custom) ICs. The ANALOG ZONE is *not a fixed size*; the perimeter is defined by the amount of circuitry. Similarly, there can be more than one zone — it's the *user's* choice.

OCEAN OF CELLS™

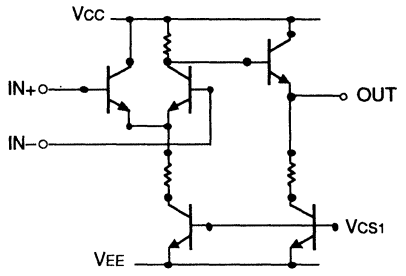
System Elements use a 6-transistor cell as their basic "core tile." These basic cells (below) are arranged in an innovative OCEAN OF CELLS™ which eliminates old-style fixed "routing channels."



Synergy's ASSET™ technology, coupled with a new (patent pending) transistor topology, produces several significant advantages: very small, very fast (17GHz) devices; high device-to-device isolation; high interconnect density and routing efficiency. Logic macros are typically implemented by interconnecting the transistors and resistors in horizontally adjacent cells. Of particular interest here, however, are **analog macros** — by *not* pre-wiring the individual transistors into conventional logic gates, Synergy has built in the capability of connecting the cell components to produce *analog* as well as *digital* functions.

BASIC ANALOG FUNCTIONS

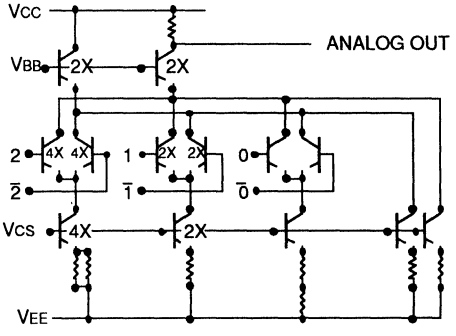
Consider a simple *voltage comparator*: using as few as 5 transistors and 3 resistors, this no-frills building block may be implemented in one basic cell, as shown below.



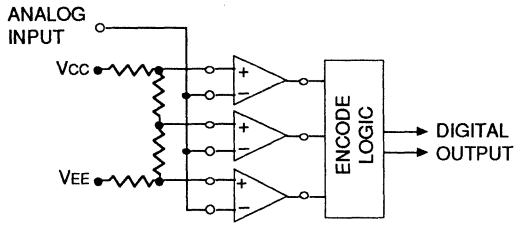
Such a circuit would exhibit an input offset voltage of approximately 10mV and input bias currents in the range of 1-2μA — a very useful building block. This circuit may be enhanced in various ways, depending on the needs of the designer — but all the "pieces" are readily available and, since all interconnects are in the *normally-programmed metal layers*, implementation of such analog functions is as straightforward as is the implementation of digital functions.

MORE COMPLEX FUNCTIONS

As the phrase implies, it's common in *mixed-signal* designs to transition back and forth between the digital and analog domains. The flexibility of the basic cell lends itself to low-to-medium resolution Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs). Below, a basic 3-bit DAC:

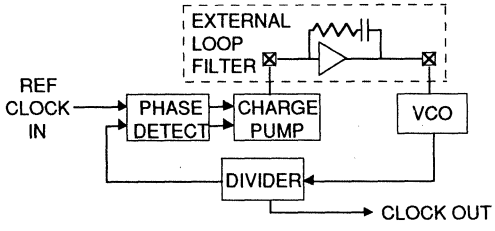


This DAC can be implemented in 5 basic core cells and accepts true and complement digital inputs shifted 2Vbe above VEE. The resolution may be expanded above 3 bits by simply adding more differential current switches (for example, a 4-bit DAC would require nine basic cells). Analog-to-Digital Converters to (at least) 6 bits may be implemented in a variety of topologies. For low resolution ADCs, the "flash" converter is often used. Shown below is a simple 2-bit flash ADC:



In this circuit we've used the basic voltage comparator shown earlier. The Encode Logic is trivial for the 2-bit case, requiring only one AND gate. Higher-resolution designs are straightforward; for example, a 3-bit flash ADC would require 7 comparators and an 8-resistor ladder. Successive approximation topologies also lend themselves well to Synergy's basic cell architecture.

More complex functions are easily implemented in the OCEAN OF CELLS. For example, a Phase-Locked-Loop (PLL) is often used for frequency synthesis or clock recovery. A typical design, such as shown below, requires *less than 200 core cells.*



Transistor Parameters			
Beta (Forward)	β	120	
Emitter Resistance(1)	RE	107	Ω
Collector Resistance	RC	83	Ω
Extrinsic Base Resistance	RBM	150	Ω
Emitter Capacitance	CJE	4.0	fF
Collector Capacitance	CJC	6.1	fF
BVCBO/BVCES(2)		12-20	V
BVEBO		7	V
LVCEO(2)		5-7	V

NOTES:
1. Includes 20 ohms of external resistance.
2. With (normal) 0.7μ EPI.

COMPONENT CHARACTERISTICS

The transistors and resistors in the core cell exhibit very tightly controlled characteristics; in the table to the right are most commonly-used transistor parameters.

Each basic cell contains 9 resistors; eight of these are connected into two "strings" of four 2.86KΩ resistors each. The ninth resistor has a value of 1KΩ. These are polysilicon resistors. Tolerance is ±10% wafer-to-wafer, but much more tightly distributed within any single wafer (i.e., within a die or cell).

ISOLATION

An ANALOG ZONE is isolated from the surrounding digital circuitry in four ways: (1) physically — the "zone" is surrounded by unutilized cells, may have metal guard rings connected to VCC, and is generally located along a core edge or in a corner; (2) power and ground pins — dedicated pins are assigned to the zone and a user may wish to connect them to separate PCB planes, traces or regulators; (3) bias generators — dedicated slave bias generators are not shared with circuits outside the zone; and (4) separate I/O pins (another reason for placing a zone along an edge or in a corner).

MACRO LIBRARY

As Synergy develops and characterizes basic analog functions, they will be released to the user library. Many users, however, will prefer to design their own analog functions — especially the more complex or application-specific ones. In all cases, it is recommended that designers consult closely with Synergy's Applications Engineers before beginning, and during the process of, any mixed-signal design.

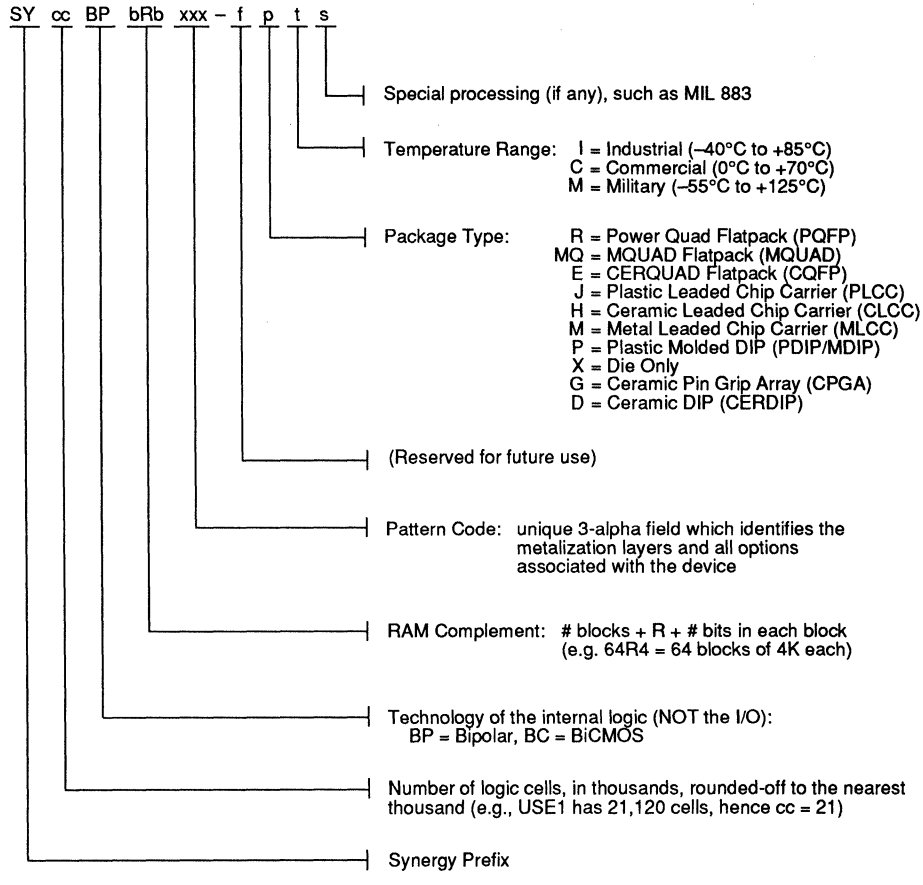
TESTING AND TECHNICAL SUPPORT

As in the design phase, development of production testing capability for mixed-signal ICs requires close cooperation between the designer and Synergy's engineers to ensure that all expectations are met.

The company presents its customers a range of design interfaces. The customer may choose to do all design at their facility, relying on Synergy only for occasional technical consultation. We have trained engineers ready to support this type of "external" project. On the other hand, many customers will choose a full "turnkey" program, where the inputs to Synergy are circuit/logic diagrams and test vectors, plus "as needed" technical consultation. The third alternative is a "joint" program, wherein the designer utilizes Synergy's Customer Design Center facility with its ready-access to technical assistance.

SYSTEM ELEMENTS make mixed-signal a reality. Whatever design interface you choose, **SYNERGY IS READY TO SUPPORT YOU.**

RISE/USE ORDERING INFORMATION



ASSET is a trademark of Synergy Semiconductor Corporation.

ClockWorks™

3

SYNERGY SEMICONDUCTOR

INTRODUCTION TO THE ClockWorks™ FAMILY

The ClockWorks™

(Clock Solutions from Synergy Semiconductor)

Synergy's ClockWorks™ is a family of *Standard Products* that makes designing any high-frequency clock system a manageable task. This family of five extremely easy-to-use and flexible product categories consist of (1) Frequency Synthesizers, (2) Clock Generators, (3) Clock Distribution and Drivers, (4) Programmable Delay Lines and (5) PLLs (Phase Locked Loops). All are adaptable to most (if not all) clock system requirements. Unlike CMOS and GaAs solutions, the ClockWorks designed in Synergy's advanced Bipolar ASSET technology provides plenty of drive for heavy load requirements with superior stability performance and reduced jitter.

Frequency synthesizers and clock distribution and drivers form the backbone of clock networks (or *trees*) in any clock system. Frequency synthesizers are designed for generating the **low jitter**, high frequency clock signal(s) required for high speed systems. Clock distribution and drivers are designed for distributing and driving high-frequency clock signals with **very low skew** in ECL, PECL or CMOS/TTL levels within the system.

Clock generators can be used to regenerate clock signals and lower frequency signals with **very low skew**. For solving more critical timing problems and race conditions, programmable delay lines and PLLs (Phase Locked Loops) can be added to the system design. Programmable delay lines are designed for **de-skewing** (compensating) for timing errors or skewing clock signals. PLLs (Phase Locked Loops) are designed to be used in conjunction with clock distribution and driver devices to produce copies of **phase coherent** clock signals (i.e., zero phase shift relative to inputs and outputs) and 2X frequency multiplied clock signals.

Any system, digital or mixed signal, with clock frequencies higher than 50MHz in CMOS/TTL, PECL or ECL will run into serious system clock generation and distribution design challenges. Designers for Pentium PCs, workstations and larger computers such as high-end graphics and massive parallel computing, or any other high-performance systems will be grateful for the solutions we have to offer. Explore and discuss any ideas or customer-specific issues with any of us on the Standard Products team!

FREQUENCY SYNTHESIZERS

The first two products of this family are SY89429 and SY89424. These two products are designed to generate unlimited choices of very stable, low-jitter clock sources. The products are used independently as a clock source utilizing a low cost 10–20MHz crystal, or used in conjunction with other frequency synthesizers to generate phase coherent clocks using a PECL reference clock signal. A crystal oscillator is provided on each chip for ease of use and to minimize component count.

The SY89429 is a programmable frequency synthesizer that provides 1MHz steps from 24MHz up to 400MHz output using a low cost 16MHz crystal. Both serial and parallel programming interfaces are provided. This product is ideal for graphics applications and any other applications requiring system clocks.

The SY89424 is a programmable frequency synthesizer that generates up to 1GHz output with switchable 40mA output current sources capable of driving heavy series terminated or 20 ohms AC coupled clock loads. This product is ideal for driving heavy CMOS low level signal clock lines.

CLOCK GENERATORS

This product family is designed to produce low skew clock outputs with different divide ratios. The products in this family include the SY10/100EL34, a divide-by-2, -4, -8 clock generator and the SY10/100S834, a divide-by-1, -2 or -3 and divide-by-2, -4 or -6 clock generator.

CLOCK DISTRIBUTION AND DRIVERS

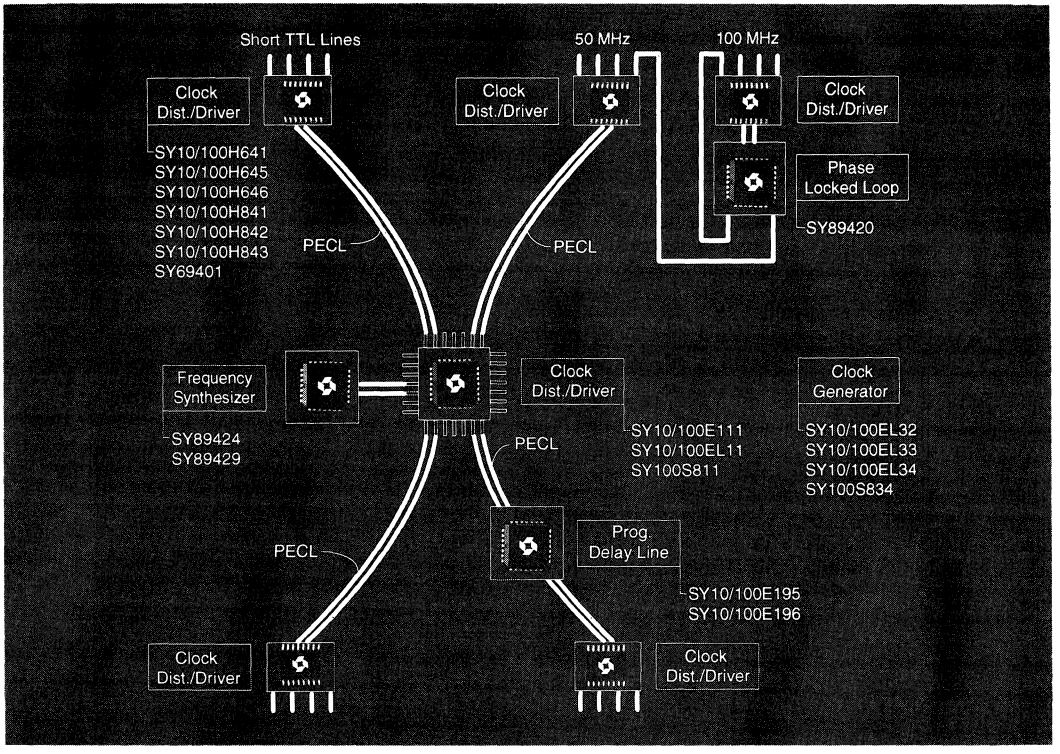
There are many devices to choose from in this family. The SY10/100E111 is the most widely used ultra-low-skew ECL and PECL clock distributor. Most ECL and PECL systems use this device for clock distribution and fanout driver. In CMOS/TTL systems, fanout drivers such as the SY10/100H841, 842, 843, the SY10/100H641, 645, 646 and the CopyClock™ (SY69401) could be used. In systems requiring a large number of copies of the system clock signal, or systems with multiple boards, the SY10/100E111 should still be used for clock distribution, while using the SY10/100H841, 842, 843 and SY10/100H641, 645, 646 for fanout drivers. Synergy's CopyClock employs a clock distribution scheme where all outputs in the same group are phase-aligned. The CopyClock can function alone, or in groups of up to four, to form the clock network.

PROGRAMMABLE DELAY LINES

The first two products in this family are the SY10/100E195 and SY10/100E196. These two products are designed to generate very stable, programmable, digital delays in 20ps steps up to 2ns in delay range. The SY10/100E196 further provides an analog input for finer resolution. Both devices are cascadable to increase the programmable delay range without external gating.

PHASE LOCKED LOOPS

The first product of this family is the SY89420. It is a dual Phase Locked Loop (PLL) packaged in a standard 28-pin PLCC. This product is designed to be used in conjunction with all Synergy clock drivers to provide phase coherent clock signals and an optional 2X frequency multiplication. Operating clock frequencies range from 33MHz to 400MHz.



Synergy Semiconductor's ClockWorks™ Family

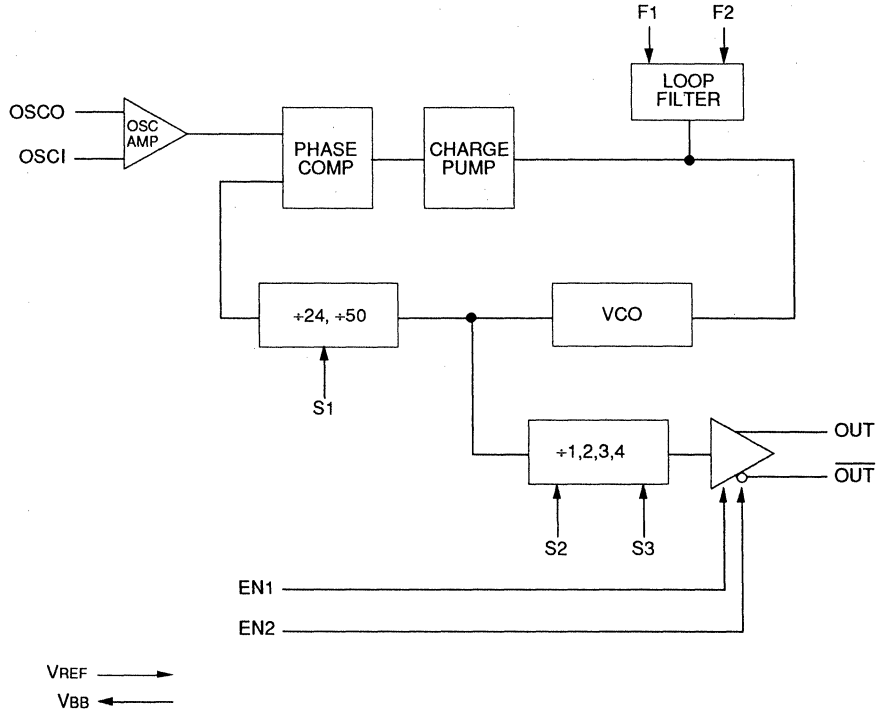
FEATURES

- **Up to 1GHz clock frequencies**
- **Low cost, on-chip crystal oscillator**
- **Low jitter PLL design**
- **On-chip 20 ohms driver**
- **Differential outputs with individual 40mA current switch control**
- **Low power consumption**
- **ESD protection 2000V**
- **16-pin SOIC package**

DESCRIPTION

The SY89424 is a low-power Phase Locked Loop (PLL) based frequency synthesizer. The device is capable of generating up to 1GHz clock frequencies with a low-cost 10–20MHz external quartz crystal. Operation of the chip is controlled by three select pins (S1, S2 and S3). S1 selects the divide ratio for the PLL. S2 and S3 select the output frequency. Two enable pins (EN1 and EN2) are provided for controlling the output driver current source independently. When EN1 and EN2 are low, the output and output driver current source are disabled. The on-chip driver is capable of driving 20 ohm clock lines.

BLOCK DIAGRAM



Rev.: A Amendment: /0
Issue Date: April, 1994

PIN NAMES

Pin	Function	Pin No.(1)
OSCI	Oscillator Input	TBD
OSCO	Oscillator Feedback	TBD
F1	Filter Pin 1	TBD
F2	Filter Pin 2	TBD
V_{REF}	Input Reference Voltage	TBD
S3	Select Input 3	TBD
S1	Select Input 1	TBD
S2	Select Input 2	TBD
OUT	Output	TBD
$\overline{OUT}$	Inverted Output	TBD
V_{CC}	V_{CC}	TBD
V_{CCO}	Output V_{CC}	TBD
V_{BB}	V_{BB}	TBD
V_{EE}	V_{EE}	TBD
EN1	Enable 1	TBD
EN2	Enable 2	TBD

NOTE:
1. TBD = To Be Determined

FREQUENCY SELECTION TABLE

Input	S1	S2	S3	FOUT
FOSC	0	0	0	24X FOSC
	0	0	1	12X FOSC
	0	1	0	8X FOSC
	0	1	1	6X FOSC
	1	0	0	50X FOSC
	1	0	1	25X FOSC
	1	1	0	16.67X FOSC
	1	1	1	12.50X FOSC

DC ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.13	3.3	3.47	V	—
I_{CC}	Power Supply Current	—	—	130	mA	Both EN1 and EN2 = HIGH, No Load
I_{CC}	Power Supply Current	—	—	80	mA	EN1 or EN2 = HIGH, No Load
I_{CCsb}	Power Supply Current	—	—	30	mA	Both EN 1 and EN2 = LOW, No Load
V_O	Output Voltage Swing	0.6	0.8	1.0	V	Peak to Peak
V_{OH}	Output HIGH Voltage	V_{CC}–1.050	—	V_{CC}–0.750	V	EN = HIGH
V_{OL}	Output LOW Voltage	V_{CC}–1.900	—	V_{CC}–1.600	V	EN = HIGH
V_{OHsb}	Output HIGH Voltage	V_{CC}–1.050	—	V_{CC}–0.750	V	EN = LOW
V_{TH}	Input Threshold	V_{REF}–0.050	V_{REF}	V_{REF}+0.050	V	—
V_{REF}	Input Reference Voltage	1.8	2.1	2.4	V	—
Z_O	Clock Line Impedance	18	20	22	Ohm	—

NOTE:

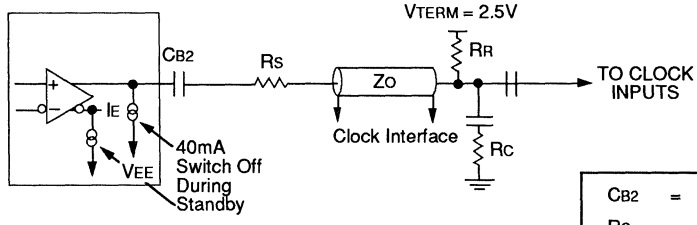
1. Output structure can be designed to minimize the total standby current which includes the DC load current. With the load condition defined below, the DC load current is 40mA.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{JIT}	Jitter	—	—	10	ps	RMS
P_{PW}	Duty Cycle	43%	50%	57%		<500MHz
t_R	Output Rise/Fall Time	300	500	800	ps	—
t_F	20% to 80%	300	500	800		

AC TEST CONDITIONS

Load conditions for 200/250MHz.



V_{EE} = GND

C_{B2}	=	10nF	±20%
R_S	=	6.8 Ohm	±5%
R_C	=	20 Ohm	±1%
R_R	=	5 KOhm	±5%
Z_O	=	20 Ohm	±2 Ohm

FREQUENCY SYNTHESIZER

ClockWorks™
PRELIMINARY
SY89429

FEATURES

- 25 to 400MHz differential PECL outputs
- ±25ps output jitter within 100 cycles
- Minimal frequency over-shoot
- Synthesized architecture
- Serial 3 wire interface
- Parallel interface for power-on
- Internal quartz reference
- PECL output can operate with either +3.3V or +5V V_{CC_OUT} power supply
- 28-pin PLCC package

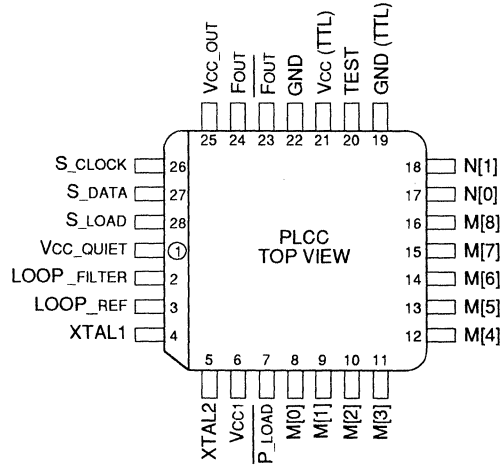
DESCRIPTION

The SY89429 is a general purpose, synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal V_{CO} will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the V_{CO} frequency divided by 2, 4, 8 or 16. With the output configured to divide the V_{CO} frequency by 2, and with a 16MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps.

APPLICATIONS

- Workstations
- Advanced communications
- High end consumer
- High-performance computing
- RISC CPU clock
- Graphics pixel clock
- Test equipment
- Other high-performance processor-based applications

PIN CONFIGURATION



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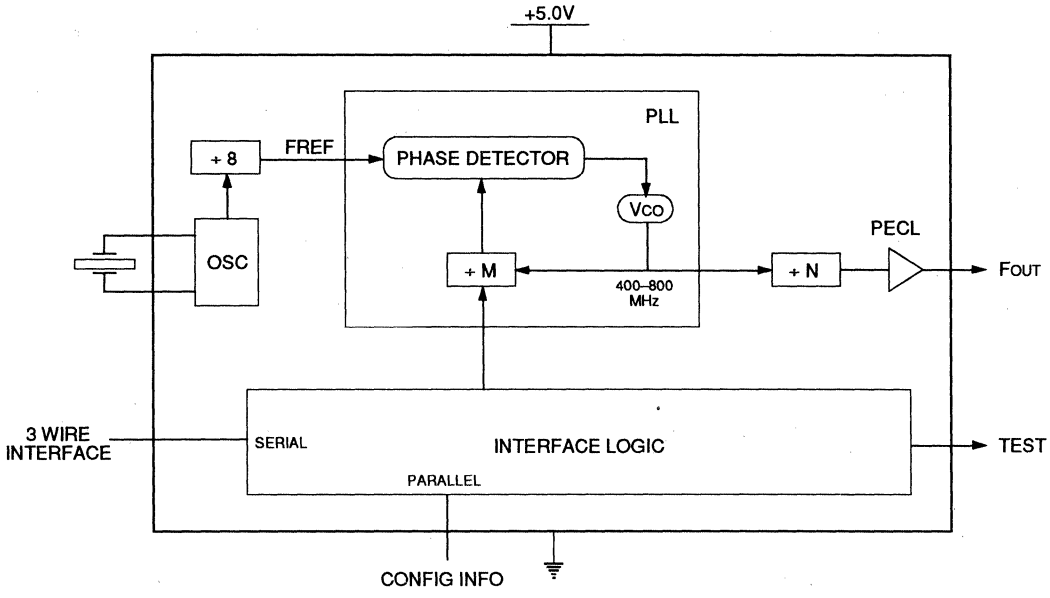
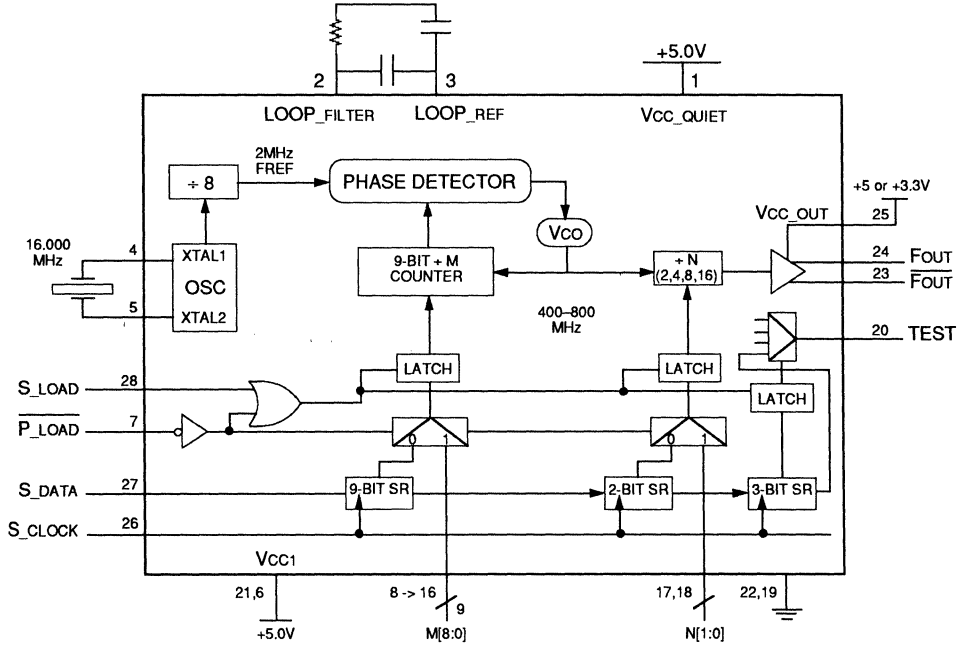
BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUTS

XTAL1, XTAL2

These pins form an oscillator when connected to an external crystal.

S_LOAD

This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the register data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.

S_DATA

This pin acts as the input to the serial configuration shift registers.

S_CLOCK

This pin clocks the serial configuration shift registers. On the rising edge of this signal, data from S_DATA is sampled.

$\overline{\text{P\_LOAD}}$

This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; thus, the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.

M[8:0]

These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB. The binary count on the M pins equates to the divide-by value for the PLL.

N[1:0]

These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$.

N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	16

Frequency		256	128	64	32	16	8	4	2	1
(MHz)	Count	M8	M7	M6	M5	M4	M3	M2	M1	M0
400	200	0	1	1	0	0	1	0	0	0
402	201	0	1	1	0	0	1	0	0	1
404	202	0	1	1	0	0	1	0	1	0
406	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
794	397	1	1	0	0	0	1	1	0	1
796	398	1	1	0	0	0	1	1	1	0
798	399	1	1	0	0	0	1	1	1	1
800	400	1	1	0	0	1	0	0	0	0

PIN DESCRIPTIONS (CONTINUED)

OUTPUTS

FOUT, $\overline{FOUT}$

These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.

TEST

The function of this output is determined by the serial configuration bits T[2:0].

POWER

VCC1

This is the positive supply for the chip and is normally connected to +5.0V.

VCC_OUT

This is the positive reference for the PECL outputs, FOUT and $\overline{FOUT}$. It is constrained to be less than or equal to VCC1.

VCC_QUIET

This is the positive supply for the PLL and should be as noise-free as possible for low-jitter operation.

GND

These pins are the negative supply for the chip and are normally all connected to ground.

OTHER

LOOP_FILTER

This is an analog I/O pin that provides the loop filter for the PLL.

LOOP_REF

This is an analog I/O pin that provides a reference voltage for the PLL.

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Power Supply Voltage	VCC	–0.5 to +7.0	V
Input Voltage	VI	–0.5 to +7.0	V
Output Source Current (Continuous)	IOUT	50	mA
Output Source Current (Surge)	IOUT	100	mA
Storage Temperature	TSTG	–65 to +150	°C
Operating Temperature	TAMB	0 to +75	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by eight before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz.

The VCO within the PLL operates over a range of 400–800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock. External loop filter components are utilized to allow for optimal phase jitter performance.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. The output divider is configured through either the serial or the parallel interfaces and can provide one of four divider ratios (2, 4, 8 or 16). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω. The positive reference for the output driver is provided by a dedicated power pin (VCC_OUT) to reduce noise and provide application flexibility.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the $\overline{P\_LOAD}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{P\_LOAD}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pull-up resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count.

The serial interface logic is implemented with a 14-bit shift register scheme. The register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet set-up and hold timing as specified in the AC parameters section of this data sheet. The configuration latches will capture the value in the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

PROGRAMMING INTERFACE

Programming the device is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$FOUT = \left(\frac{FXTAL}{8}\right) \times M \div N$$

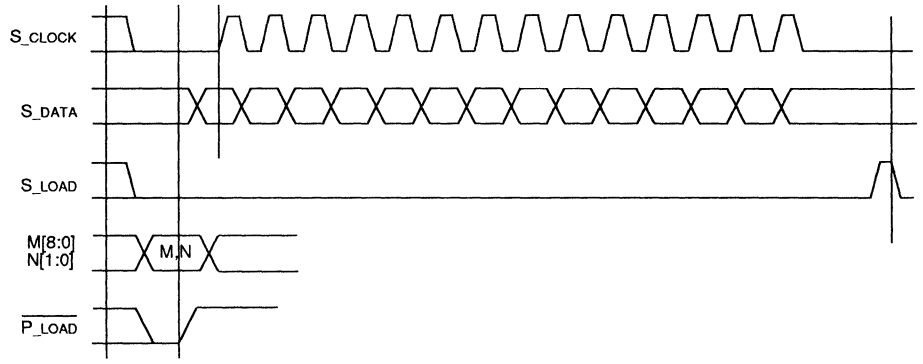
Where FXTAL is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$.

M[8:0] and N[1:0] are normally specified once at power-on, through the parallel interface, and then possibly again through the serial interface. This approach allows the designer to bring up the application at one frequency and then change or fine-tune the clock, as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible.

The TEST output provides visibility for one of several internal nodes (as determined by the T[1:0] bits in the serial configuration stream). It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the TTL output may not be able to toggle fast enough for some of the higher output frequencies. The serial configuration port can be used to select one of the alternate functions for this pin. The serial data sequence is as follows:

Input S_DATA to M0, then M1, then M2, then M3, then M4, then M5, then M6, then M7, then M8, then N0, then N1, then T0, then T1, then T2, to TEST output mux.

T2	T1	T0	TEST (Pin 19)
0	0	0	Data Out – Last Bit SR
0	0	1	HIGH
0	1	0	FREF
0	1	1	M Counter Out
1	0	0	FOUT
1	0	1	LOW
1	1	0	RESERVED
1	1	1	FOUT/4



Input S_DATA to M0 then M1, then M2, etc., as indicated in the verbiage above.

100H ECL DC ELECTRICAL CHARACTERISTICS

V_{CC1} = +5.0V ± 10%; V_{CC_QUIET} = +5.0V ± 10%; V_{CC_OUT} = +3.3V/+5.0V ± 10%; T_A = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC_OUT} –1.025	V_{CC_OUT} –0.880	V	50Ω to V_{CC_OUT} –2V
V_{OL}	Output LOW Voltage	V_{CC_OUT} –1.810	V_{CC_OUT} –1.620	V	50Ω to V_{CC_OUT} –2V

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%; V_{CC_QUIET} = +5.0V ± 10%; V_{CC} = V_{CC_OUT} = +3.3V/+5.0V ± 10%

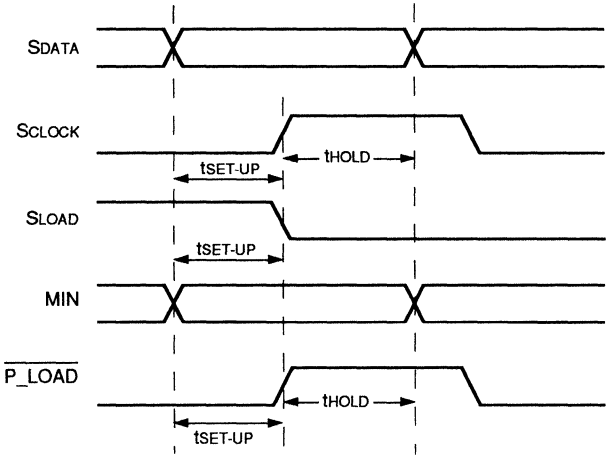
		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	—	50	—	50	—	50	µA	V_{IN} = 2.7V
I_{IL}	Input LOW Current	—	–0.6	—	–0.6	—	–0.6	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	–1.2	—	–1.2	—	–1.2	V	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	—	2.5	—	2.5	—	2.5	V	I_{OH} = –2.0mA
VOL	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 8mA
I_{OS}	Output Short Circuit Current	-80 (Typ.)		-80 (Typ.)		-80 (Typ.)		mA	V_{OUT} = 0V
I_{CC1}	Supply Current							mA	—
	V_{CC1}	—	200	—	200	—	200		
	V_{CC_OUT}	—	10	—	10	—	10		
	V_{CC_QUIET}	—	10	—	10	—	10		

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%; Airflow > 2.5 m/s

Parameter	Min.	Typ.	Max.	Unit
S_CLOCK Max. Frequency	—	—	10.0	MHz
Oscillator Frequency	10	—	20	MHz
S_DATA to S_CLOCK Set-up	20	—	—	ns
S_DATA to S_CLOCK Hold	20	—	—	ns
S_DATA to S_LOAD Set-up	20	—	—	ns
S_LOAD Min. HIGH Time	50	—	—	ns
M,N to $\overline{P\_LOAD}$ Set-up	20	—	—	ns
M,N to $\overline{P\_LOAD}$ Hold	20	—	—	ns
$\overline{P\_LOAD}$ Min. LOW Time	50	—	—	ns
Reference OSC Max. Frequency	—	—	20	MHz
Reference OSC Min. Frequency	10	—	—	MHz
PLL Lock from $\overline{P\_LOAD}$	1	—	10	ms
V_{CO} Max. Frequency	—	—	800	MHz
V_{CO} Min. Frequency	400	—	—	MHz
F_{OUT} Duty Cycle	—	—	45/55	%
F_{OUT} Max. Jitter	—	—	±25	ps

TIMING DIAGRAM



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY89429JC	J28-1	Commercial

FEATURES

- **Low jitter differential design**
- **33–400MHz operating frequency range**
- **2X frequency multiplication**
- **ESD protection of 2000V**
- **28-pin PLCC package**

DESCRIPTION

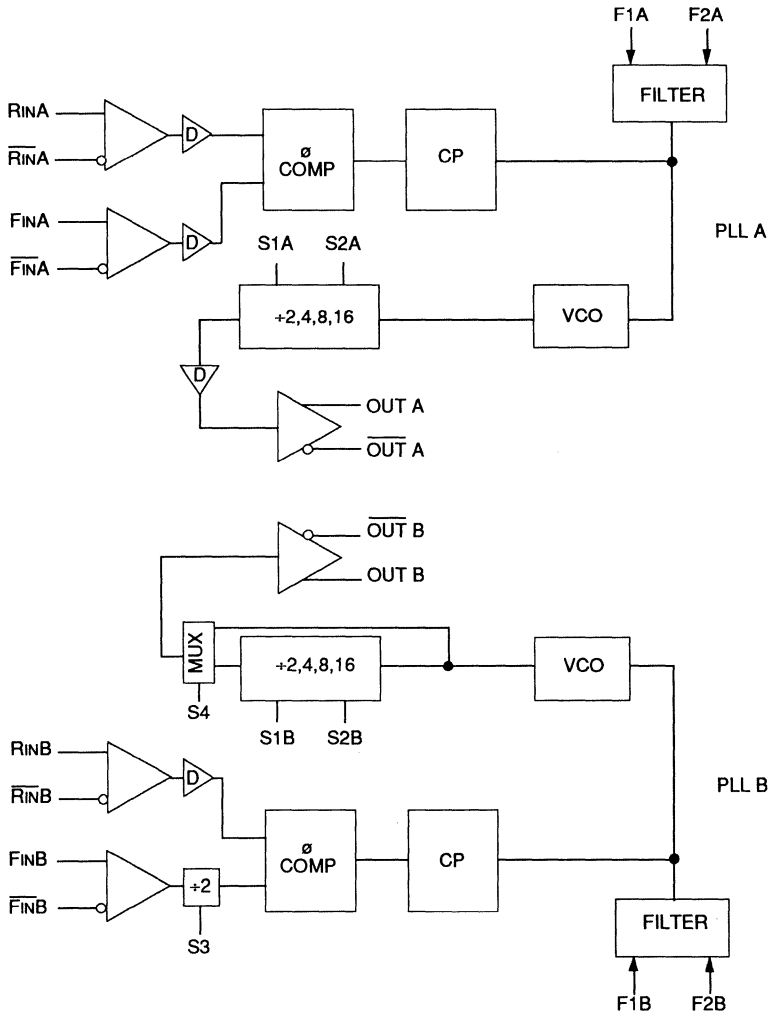
The SY89420 is the first device in the Phase Locked Loop (PLL) category of products created for use with Synergy's ClockWorks™ family of products.

The SY89420 device consists of two low jitter Phase Locked Loops based on Synergy's differential PLL technology. Each of the two PLLs (PLL-A and PLL-B) is capable of operating in 33–400MHz frequency range independently.

Two reference inputs (RINX and $\overline{\text{RINX}}$), two feedback inputs (FINX and $\overline{\text{FINX}}$), two filter pins (F1X and F2X), two control pins (S1X and S2X), and two differential outputs (OUTX and $\overline{\text{OUTX}}$) are provided for each of the two PLLs for independent operation. Reference inputs and feedback inputs can be used as differential inputs or single-ended inputs. When $\overline{\text{RINX}}$ and $\overline{\text{FINX}}$ are connected to V_{BB}, RINX and FINX interface to normal 100K ECL or 100K PECL levels. When $\overline{\text{RINX}}$ and $\overline{\text{FINX}}$ are connected to VTH, RINX and FINX interface to normal TTL levels. S1X and S2X are control pins to program the divider for optimum VCO operation. Control pins S3 and S4 are provided for PLL-B. When both S3 and S4 are low, PLL-B is identical to PLL-A. When S3 is high, the 2X frequency multiplication option is enabled. When S4 is high, the programmable divider is bypassed, enabling the PLL to output the VCO frequency directly.

Rev.: A Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



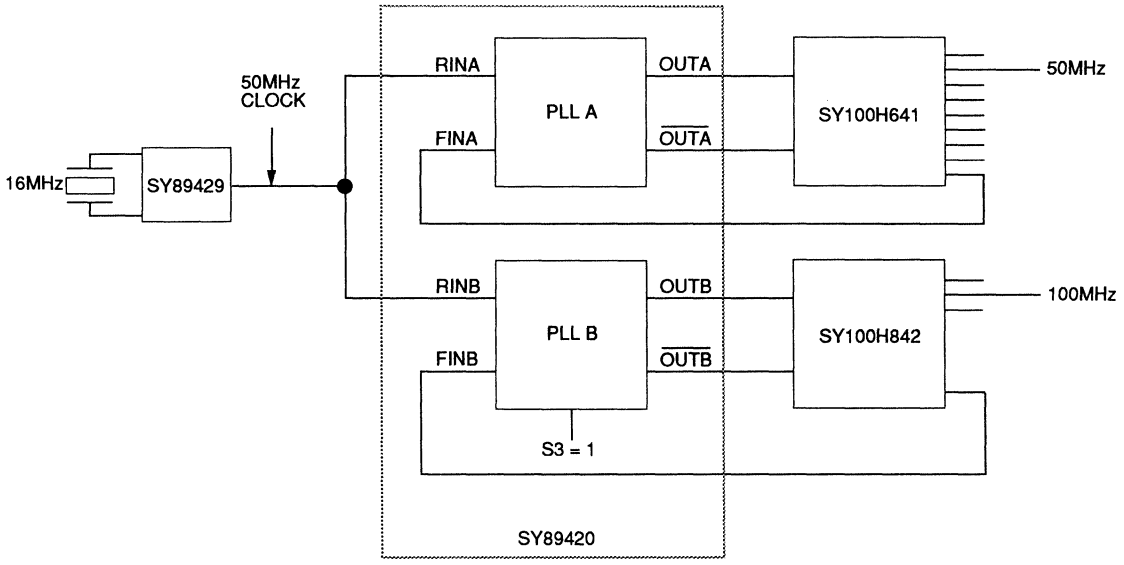
PIN NAMES

Pin	Pin No.(1)
F1A	TBD
F2A	TBD
RINA	TBD
$\overline{\text{RINA}}$	TBD
FINA	TBD
$\overline{\text{FINA}}$	TBD
OUTA	TBD
$\overline{\text{OUTA}}$	TBD
F1B	TBD
F2B	TBD
RINB	TBD
$\overline{\text{RINB}}$	TBD
FINB	TBD
$\overline{\text{FINB}}$	TBD
OUTB	TBD
$\overline{\text{OUTB}}$	TBD
S1A	TBD
S2A	TBD
V_{CCO}	TBD
V_{CC}	TBD
V_{EE}	TBD
V_{CCO}	TBD
S3	TBD
S4	TBD
S1B	TBD
S2B	TBD
V_{BB}	TBD
V_{TH} (TTL)	TBD

NOTE:

1. TBD = To Be Determined

TYPICAL APPLICATION



50MHz Low Skew Clock System with 100MHz Clock to CPU

FEATURES

- **Less than 500ps of edge skew between any two outputs — FOREVER**
- **Master, plus up to 3 slaves, provide up to 32 TTL-compatible outputs per board**
- **Clock frequencies to 125MHz**
- **Dramatically reduces effects of variations in supply voltage, temperature, layout and silicon processing**
- **Differential ECL logic preserves duty cycle of Master Clock**
- **Device functions as Master or Slave**
- **Single +5 volt supply**
- **Compact 28-pin Leaded Chip Carrier (MLCC)**

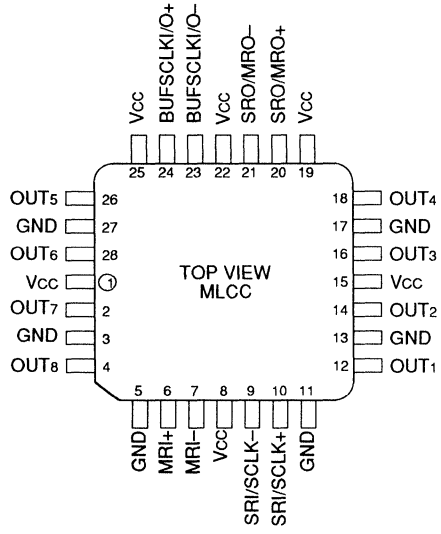
DESCRIPTION

The Synergy SY69401 CopyClock is a high-speed Active De-Skew Clock Distribution System fabricated in Synergy's proprietary ASSET™ I bipolar process.

The SY69401 CopyClock device is designed to operate in conjunction with other CopyClock devices to provide multiple TTL-level output clocks with skews of less than 500ps between all clocks of all CopyClock devices. Each device may operate as either a Master or Slave. In a cluster of CopyClock chips, one chip operates as the Master, and all other chips operate as Slaves. The Slave chips will automatically align their output TTL clocks to the output TTL clock of the Master.

CopyClock is a purely digital circuit with internal differential ECL logic and Positive-ECL (PECL) differential signals among all CopyClock chips. Synergy's circuit design techniques, coupled with ASSET, result in ultra-low skews, while allowing device operation at reduced power levels.

PIN CONFIGURATION



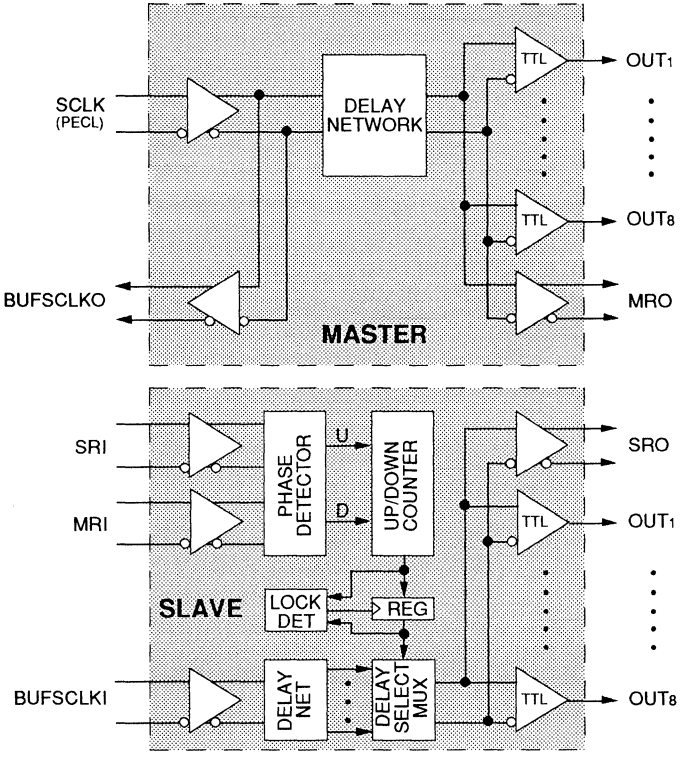
PIN NAMES

Pin	Function
OUT_1 — OUT_8	TTL Outputs
MRI	Master Reference Input
SRI	Slave Reference Input
SCLK	System Clock Input
BUFSCLK	Buffered Copy of System Clock Input
MRO	ECL Copy of Master Output Clock
SRO	ECL Copy of Slave Output Clock

ASSET and CopyClock are trademarks of Synergy Semiconductor Corporation.

Rev.: A Amendment: /0
Issue Date: April, 1994

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CopyClock has been developed specifically in response to the clock distribution needs of dense, high-speed digital systems. The requirements of low total system clock skew, large number of clocks, high immunity to noise (power planes, signal crosstalk, clock jitter), simple layout and wiring, and ease of manufacturing and field repair, form the basis of the CopyClock design.

Low total skew between many clocks dictated that the clock distribution elements incorporate some type of active compensation to reduce the intrinsic delay variations caused by variations in the semiconductor manufacturing process. While Phase-Locked Loops can perform this type of compensation, the associated Voltage-Controlled Oscillator is, itself, a source of noise and jitter. The CopyClock family achieves alignment solely through the use of low-swing differential logic, and uses a common source clock so no additional noise or jitter are generated and duty cycle is always preserved.

The differential digital nature of the CopyClock family provides the tolerance for noise both on-chip and between CopyClock chips. Low internal voltage swings allow for precise measurement and alignment of clocks, while rejecting power plane noise. The differential signals between CopyClock devices also minimize signal crosstalk and reject noise.

No special layout or routing considerations are needed for CopyClock chips. Placement can be made to optimize the usage of the output clocks, with all wiring treated the same as any other digital signal. Since each CopyClock chip will configure itself upon power-up and automatically compensate for board, package and silicon variations, no calibration or measurements are required in the manufacturing and field repair of boards using CopyClock chips.

Each CopyClock chip provides 8 TTL-compatible output clocks. Each chip may operate as a Master or a Slave. In a cluster of CopyClock chips, one chip is designated as the Master and all other chips on the board operate as Slaves.

FUNCTIONAL DESCRIPTION (CONT'D.)

The Slave chips will automatically align their output TTL clocks to the Master's output TTL clocks.

Upon power-up, each CopyClock device in a cluster will examine its phase detector inputs (see INPUT SIGNALS, below) to determine whether to operate as the Master or as a Slave. The Master provides a differential Master Reference Output and a differential Buffered System Clock Output to all Slaves. The Master reference and system clock are connected in daisy-chain fashion to all Slaves in the cluster, with a termination at the end of each line. Each Slave will compare its own reference output (SRO) against the Master reference; the Slave Reference Output is a delayed version of the system clock supplied by the Master. Each Slave will adjust its reference output by adjusting system clock delay until the Master reference (MRI) and the Slave reference (SRI) inputs are exactly aligned. At this point, each Slave's TTL output clocks will be aligned to all other TTL clocks. The external connection between each Slave's reference output and reference input compensates for the difference in location, loading and intrinsic delays between the various Slaves and Master. This external feedback wiring also allows for earlier or later clocks (if desired).

INPUT SIGNALS

All CopyClock inputs are differential PECL (Positive-ECL) signals.

SYSTEM CLOCK (SCLK) — *Master* only. This input is supplied by the system's Clock Generator. A typical CopyClock system presents only one unit load per board to the System Clock lines.

SLAVE REFERENCE INPUT (SRI) — *Slave* only. This input provides an ECL-compatible copy of a Slave's output clock to the Phase Detector. The SRI pins are connected to the Slave Reference Output (SRO) pins on the same Slave chip.

MASTER REFERENCE INPUT (MRI) — On *Slave* chips, this input provides an ECL-compatible copy of the Master's output clock to the Slave's Phase Detector. The board Master's MRO pins are connected to the MRI pins on each Slave in daisy-chain fashion. On *Master* chip, this input is tied to a logic "0" (i.e., MRI+ tied to ground, MRI– tied to V_{CC}).

BUFFERED SYSTEM CLOCK IN (BUFSCLKI) — *Slave* only. The System Clock input to each Slave. The BUFSCLKO pins on the board Master are connected to the BUFSCLKI pins on each Slave in daisy-chain fashion.

OUTPUT SIGNALS

Except as noted, outputs are differential PECL.

OUT_1–OUT_8 — Eight identical, phase-aligned TTL-compatible output clocks.

MASTER REFERENCE OUT (MRO) — *Master* only. This putput provides an ECL-compatible copy of the board Master's output clocks to the phase detector on each Slave. The MRO pins are connected to the MRI pins on each Slave in daisy-chain fashion.

SLAVE REFERENCE OUT (SRO) — *Slave* only. This output provides an ECL-compatible copy of a Slave's output clocks to the Phase Detector on that Slave. The SRO pins are connected to the SRI pins on the same device.

BUFFERED CLOCK OUT (BUFSCLKO) — *Master* only. This is a direct buffered copy of the System Clock input. This output provides System Clock to all Slaves on a board. The BUFSCLKO pins on the Master are connected to the BUFSCLKI pins on each Slave in daisy-chain fashion.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Rating	Unit
V_{CC}	Power Supply (GND = 0V)		0 to +7	VDC
V_I	Input Voltage (GND = 0V)		0 to V_{CC}	VDC
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range		0 to +75	°C
V_{CC}	Operating Range		+4.2 to +5.7	V

NOTE:

1. Beyond which device life may be impaired.

DC ELECTRICAL CHARACTERISTICS — ECL

V_{CC} = 4.75V to 5.25V; GND = 0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	3.98	4.16	4.02	4.19	4.08	4.265	V
V_{OL}	Output LOW Voltage	3.05	3.37	3.05	3.37	3.05	3.4	V
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.93	4.265	V
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.55	V
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.3	—	µA
I_{CC}	V_{CC} Power Supply Current	—	300	—	300	—	300	mA

3

DC ELECTRICAL CHARACTERISTICS — TTL

V_{CC} = 4.75V to 5.25V; GND = 0V, T_A = 0°C to +75°C

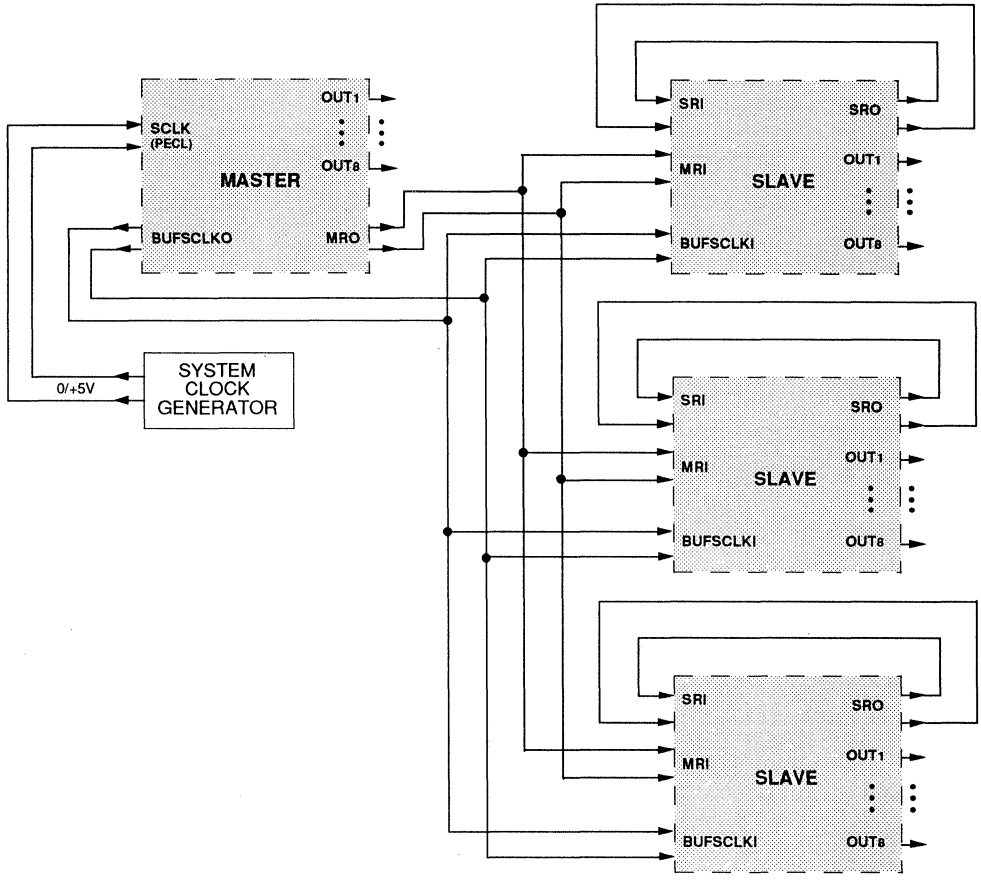
Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	I_{OH} = –16mA
V_{OL}	Output LOW Voltage	—	0.5	V	I_{OL} = 16mA
I_{OS}	Output Short Circuit Current	–150	–60	mA	V_{OUT} = GND
I_{CC}	V_{CC} Power Supply Current	—	300	mA	—

TIMING SPECIFICATIONS

V_{CC} = 4.75V to 5.25V; GND = 0V, T_A = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit
SCLK	System Clock Input	50	125	MHz
$SKEW_{PP}$	Pin-to-Pin Skew	—	300	ps
$SKEW_{AL}$	Alignment Skew	—	100	ps
$SKEW_{OB}$	On-Board Skew	—	100	ps
TSKEW	Total Skew	—	500	ps
T_{STEP}	Delay Adjustment Steps	50	—	ps

SYSTEM IMPLEMENTATION



WIRING RULES

1. Place Master and Slave CopyClock devices on the PC board so as to optimize the connection of the TTL output clocks.
2. Connect the Master's Buffered System Clock Out (BUFSCLKO) to the Buffered System Clock In (BUFSCLKI) on each Slave. Daisy-chaining is suggested.
3. Connect the Master Reference Out (MRO) to the Master Reference In (MRI) on each Slave. Daisy-chaining is suggested.
4. Measure the wire length between the MRO pin and the MRI pin on the first Slave. Use the same length of trace to connect the SRO pins to the SRI pins on that Slave.
5. Repeat Step 4 for each Slave chip.
6. Maintain the *total* length of the Master Reference and Buffered System Clock traces to 60 inches each, maximum.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0V)	0 to –6V	Vdc
I_{OUT}	Output Current Continuous Surge	 50 100	mA
T_A	Operating Temperature Range 10E 100E	 0 to +75 0 to +85	°C
T_{STORE}	Storage Temperature	–65 to +150	°C

NOTE:

1. Beyond which device life may be impaired unless specified otherwise on individual data sheet.

10E SERIES DC CHARACTERISTICS (10KH)

V_{EE} = -5.2V ± 5%; V_{CC} = V_{CCO} = GND; T_A = 0°C to +75°C(1)

		T_A = 0°C		T_A = +25°C		T_A = +75°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1020	–840	–980	–810	–920	–735	–910	–720	mV
V_{OL}	Output LOW Voltage	–950	–1630	–1950	–1630	–1950	–1600	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1070	–735	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.3	—	0.3	—	µA

NOTE:

1. 10E series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts, except bus outputs which, where specified, are terminated into 25Ω.

100E SERIES DC CHARACTERISTICS (100K)

V_{EE} = -4.2V to -5.46V; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–995	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL} (Min.)	50Ω to –2.0V
V_{OHA}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	
V_{OLA}	Output LOW Voltage	—	—	–1610	mV	or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5	—	—	mA	V_{IN} = V_{IL} (Min.)	

NOTE:

1. This table replaces the three tables at different supply voltages in ECL 100K literature. The same DC parametric values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2 to –5.46.

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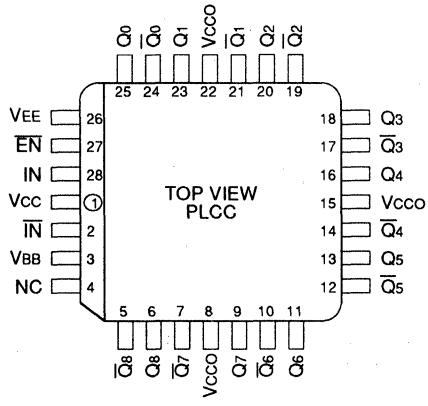
1:9 DIFFERENTIAL CLOCK DRIVER

FEATURES

- **Low skew**
- **Guaranteed skew limits**
- **Differential design**
- **VBB output**
- **Enable input**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E111**

PIN CONFIGURATION



PIN NAMES

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
$\overline{EN}$	Enable Input
Q0, $\overline{Q0}$ — Q8, $\overline{Q8}$	Differential Outputs
VBB	VBB Output

DESCRIPTION

The SY10E111 and SY100E111 are low skew 1-to-9 differential drivers designed for clock distribution in new, high-performance ECL systems. They accept one differential or single-ended input, with VBB used for single-ended operation. The signal is fanned out to nine identical differential outputs. An enable input is also provided such that a logic HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E111 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

The VBB output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01μF capacitor.

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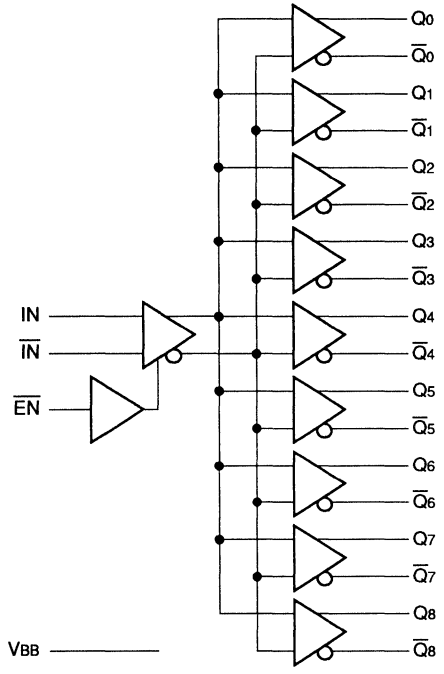
Issue Date: February, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19		
	100E	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	48	60	—	48	60	—	48	60		
	100E	—	48	60	—	48	60	—	55	69		

TIMING DIAGRAMS

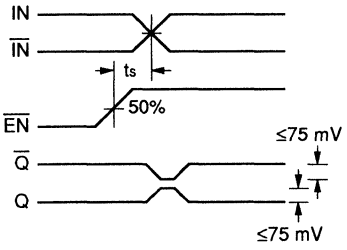


Figure 1. Set-up Time

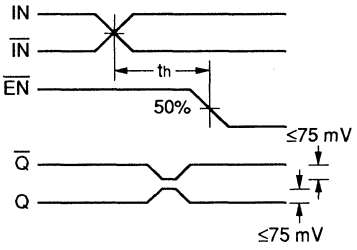


Figure 2. Hold Time

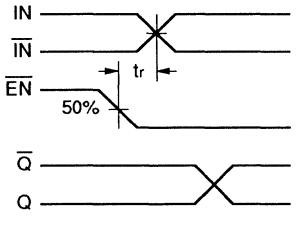


Figure 3. Release Time

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition[1-9]
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	IN (differential)	430	—	630	430	—	630	430	—	630		1
	IN (single-ended)	330	—	730	330	—	730	330	—	730		2
	Enable	450	—	850	450	—	850	450	—	850		3
	Disable	450	—	850	450	—	850	450	—	850		3
t_{SKEW}	Within-Device Skew	—	25	50	—	25	50	—	25	50	ps	4
t_S	Set-up Time, $\overline{EN}$ to IN	200	0	—	200	0	—	200	0	—	ps	5
t_H	Hold Time, IN to $\overline{EN}$	0	–200	—	0	–200	—	0	–200	—	ps	6
t_R	Release Time, $\overline{EN}$ to IN	300	100	—	300	100	—	300	100	—	ps	7
V_{PP}	Minimum Input Swing	250	—	—	250	—	—	250	—	—	mV	8
V_{CMR}	Common Mode Range	-1.6	—	-0.4	-1.6	—	-0.4	-1.6	—	-0.4	V	9
t_r	Rise/Fall Times	275	375	600	275	375	600	275	375	600	ps	—
t_f	20% to 80%											

NOTES:

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on $\overline{EN}$ to the 50% point of a **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from the 50% point of a **positive** transition on $\overline{EN}$ to the 50% point of a **negative** transition on Q (or a positive transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be de-asserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the E111, as a differential input as low as 50mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

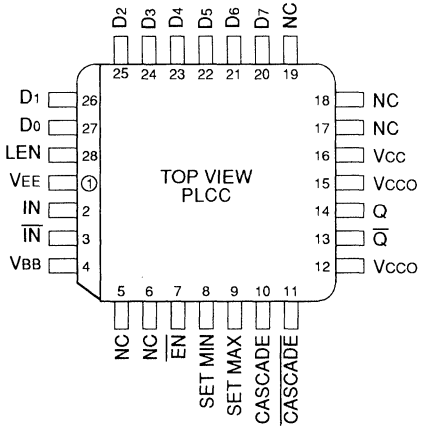
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E111JC	J28-1	Commercial
SY100E111JC	J28-1	Commercial

FEATURES

- **Up to 2ns delay range**
- **≈20ps/digital step resolution**
- **>1GHz bandwidth**
- **On-chip cascade circuitry**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E195**

PIN CONFIGURATION



DESCRIPTION

The SY10/100E195 are programmable delay chips (PDCs) designed primarily for clock de-skewing and timing adjustment. They provide variable delay of a differential ECL input transition.

The delay section consists of a chain of gates organized as shown in the logic diagram. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80ps. These two elements provide the E195 with a digitally-selectable resolution of approximately 20ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on-chip by a high signal on the latch enable (LEN) control.

Because the delay programmability of the E195 is achieved by purely differential ECL gate delays, the device will operate at frequencies of >1GHz, while maintaining over 600mV of output swing.

The E195 thus offers very fine resolution, at very high frequencies, selectable entirely from a digital input, allowing for very accurate system clock timing.

An eighth latched input, D7, is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Minimum Delay Set
SET MAX	Maximum Delay Set
CASCADE	Cascade Signal

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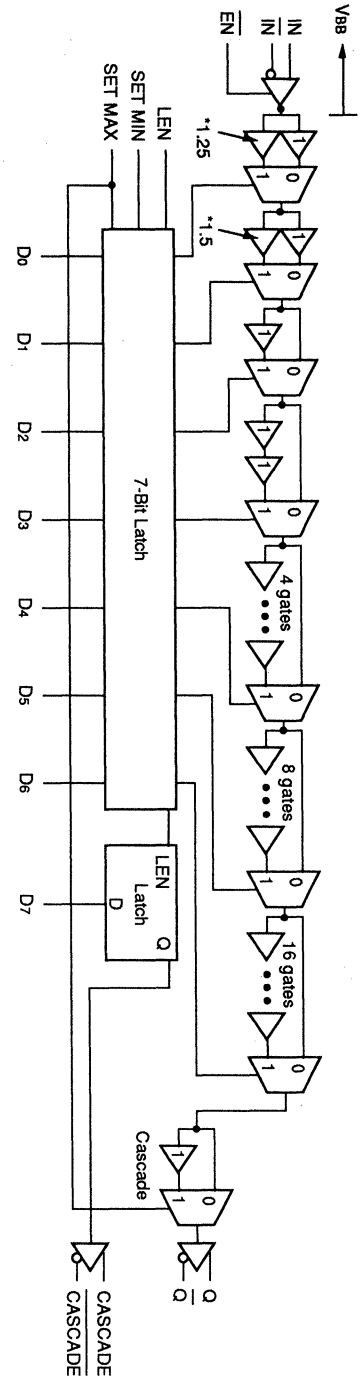
BLOCK DIAGRAM



*Delays are 25% or 50% longer than standard (standard = 80ps).

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	130	156	—	130	156	—	130	156		
	100E	—	130	156	—	130	156	—	150	179		

3

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765		
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D_7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range t_{PD} (max.) – t_{PD} (min.)	2000	2175	—	2050	2240	—	2375	2580	—	ps	—
Δt	Step Delay										ps	6
	D_0 High	—	17	—	—	17.5	—	—	21	—		
	D_1 High	—	34	—	—	35	—	—	42	—		
	D_2 High	55	68	105	55	70	105	65	84	120		
	D_3 High	115	136	180	115	140	180	140	168	205		
	D_4 High	250	272	325	250	280	325	305	336	380		
	D_5 High	505	544	620	515	560	620	620	672	740		
	D_6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D_1	D_0	—	D_1	D_0	—	D_1	D_0	—	—	7
t_{SKEW}	Duty Cycle Skew, t_{PHL}–t_{PLH}	—	±30	—	—	±30	—	—	±30	—	ps	1
t_S	Set-up Time										ps	
	D to LEN	200	0	—	200	0	—	200	0	—		
	D to IN	800	—	—	800	—	—	800	—	—		2
	EN to IN	200	—	—	200	—	—	200	—	—		3
t_H	Hold Time										ps	
	LEN to D	500	250	—	500	250	—	500	250	—		
	IN to $\overline{EN}$	0	—	—	0	—	—	0	—	—		4
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300	—	—	300	—	—	300	—	—		5
	SET MAX to LEN	800	—	—	800	—	—	800	—	—		
	SET MIN to LEN	800	—	—	800	—	—	800	—	—		
t_{jit}	Jitter	—	<5	—	—	<5	—	—	<5	—	ps	8
t_r	Rise/Fall Times										ps	—
t_f	20–80% (Q)	125	225	325	125	225	325	125	225	325		
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650		

NOTES:

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This set-up time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D_0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs D_n). Typically, the device will be monotonic to the D_0 input, however, under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D_0 input is the LSB. With the D_1 input as the LSB, the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

APPLICATIONS INFORMATION

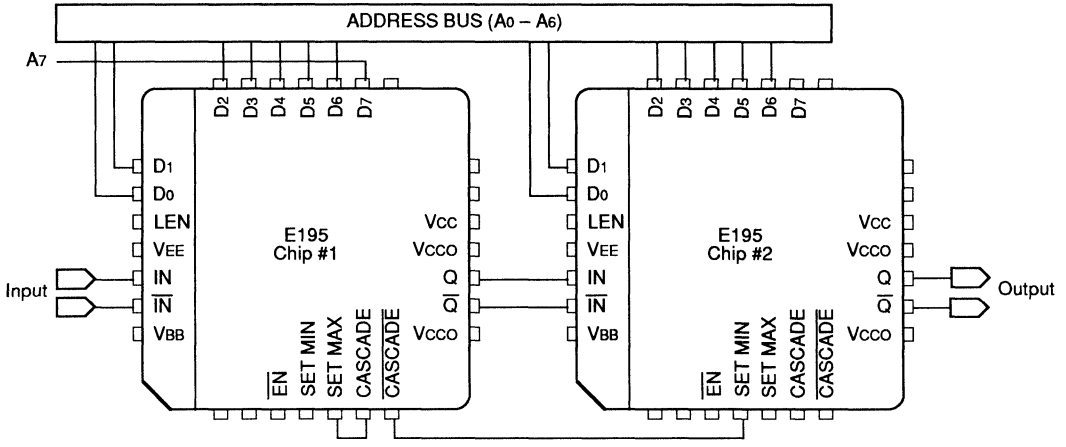


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E195s

To increase the programmable range of the E195, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195s without the need for any external gating. Furthermore, this capability requires only one more address line per added E195. Obviously, cascading multiple PDCs will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195s. As can be seen, this scheme can easily be expanded for larger E195 chains. The D_7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1, when D_7 is asserted, it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D_7 of chip #1 above is low, the cascade output will also be low, while the cascade bar output will be a logical high. In this condition, the SET MIN pin of chip #2 will be asserted and, thus, all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding, any changes on the A_0–A_6 address bus will not affect the operation of chip #2.

Chip #1, on the other hand, will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A_0–A_6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A_0–A_6 address bus), D_7 will be asserted to signal the need to cascade the delay to the next E195 device. When D_7 is asserted, the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A_0–A_6 address bus. Chip #1, on the other hand, will have its SET MAX pin asserted, resulting in the device delay to be independent of the A_0–A_6 address bus.

When the SET MAX pin of chip #1 is asserted, the D_0 and D_1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity, an additional gate delay is selected in the cascade circuitry. As a result, when D_7 of chip #1 is asserted, the delay increases from 31.75 gates to 32 gates. A 32-gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices, one simply needs to connect the D_7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E195JC	J28-1	Commercial
SY100E195JC	J28-1	Commercial

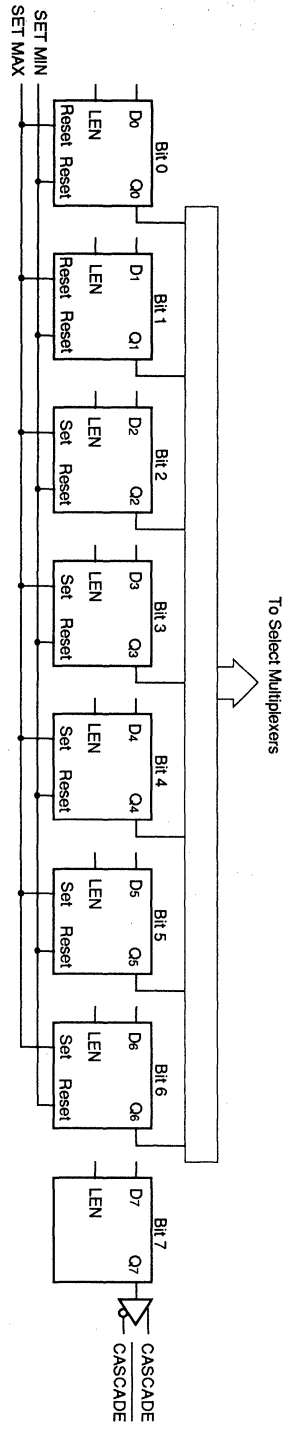


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

PROGRAMMABLE DELAY CHIP

ClockWorks™
SY10E196
SY100E196

FEATURES

- Up to 2ns delay range
- ≈20ps digital step resolution
- Linear input for tighter resolution
- >1GHz bandwidth
- On-chip cascade circuitry
- Extended 100E V_{EE} range of –4.2V to –5.46V
- ESD protection of 2000V
- Fully compatible with Motorola 10E/100E196

DESCRIPTION

The SY10/100E196 are programmable delay chips (PDCs) designed primarily for very accurate differential ECL input edge placement applications.

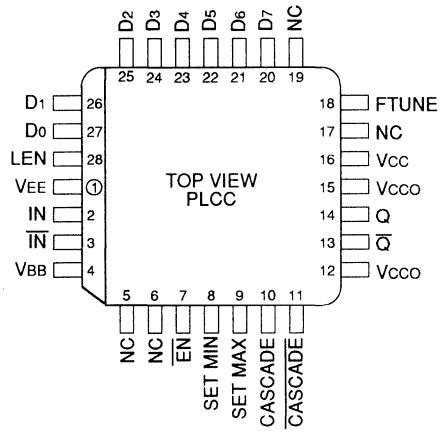
The delay section consists of a chain of gates and a linear ramp delay adjustment organized as shown in the logic diagram. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80ps. These two elements provide the E196 with a digitally-selectable resolution of approximately 20ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on-chip by a high signal on the latch enable (LEN) control.

The FTUNE input takes an analog voltage and applies it to an internal linear ramp for reducing the 20s resolution still further. The FTUNE input is what differentiates the E196 from the E195.

An eighth latched input, D7, is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

3

PIN CONFIGURATION



PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Minimum Delay Set
SET MAX	Maximum Delay Set
CASCADE	Cascade Signal
FTUNE	Linear Voltage Input

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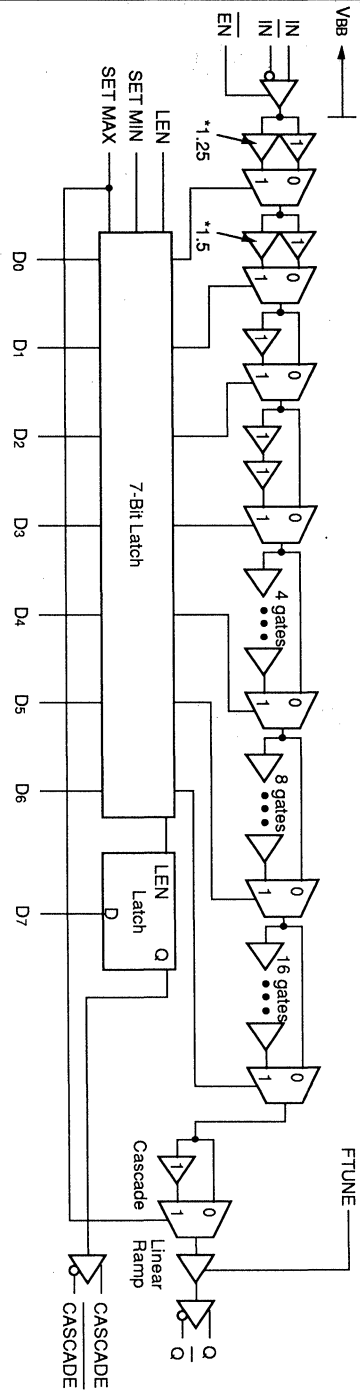
Issue Date: February, 1994

BLOCK DIAGRAM



*Delays are 25% or 50% longer than standard (standard = 80ps).

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	130	156	—	130	156	—	130	156		
	100E	—	130	156	—	130	156	—	150	179		

3

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

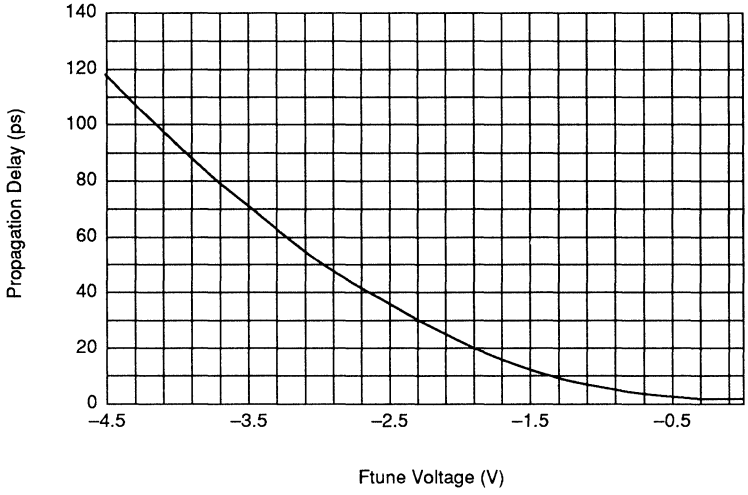
Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765		
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D_7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range t_{PD} (max.) – t_{PD} (min.)	2000	2175	—	2050	2240	—	2375	2580	—	ps	—
Δt	Step Delay										ps	6
	D_0 High	—	17	—	—	17.5	—	—	21	—		
	D_1 High	—	34	—	—	35	—	—	42	—		
	D_2 High	55	68	105	55	70	105	65	84	120		
	D_3 High	115	136	180	115	140	180	140	168	205		
	D_4 High	250	272	325	250	280	325	305	336	380		
	D_5 High	505	544	620	515	560	620	620	672	740		
	D_6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D_1	D_0	—	D_1	D_0	—	D_1	D_0	—	—	7
t_{SKEW}	Duty Cycle Skew, t_{PHL}–t_{PLH}	—	±30	—	—	±30	—	—	±30	—	ps	1
t_s	Set-up Time										ps	
	D to LEN	200	0	—	200	0	—	200	0	—		
	D to IN	800	—	—	800	—	—	800	—	—		2
	EN to IN	200	—	—	200	—	—	200	—	—		3
t_h	Hold Time										ps	
	LEN to D	500	250	—	500	250	—	500	250	—		
	IN to $\overline{EN}$	0	—	—	0	—	—	0	—	—		4
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300	—	—	300	—	—	300	—	—		5
	SET MAX to LEN	800	—	—	800	—	—	800	—	—		
	SET MIN to LEN	800	—	—	800	—	—	800	—	—		
t_{jit}	Jitter	—	<5	—	—	<5	—	—	<5	—	ps	8
t_r	Rise/Fall Times										ps	—
t_f	20–80% (Q)	125	225	325	125	225	325	125	225	325		
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650		

NOTES:

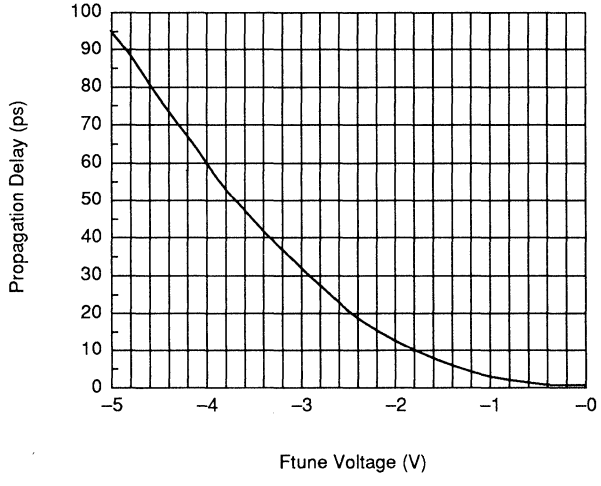
1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This set-up time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D_0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs D_n). Typically, the device will be monotonic to the D_0 input, however, under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D_0 input is the LSB. With the D_1 input as the LSB, the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

APPLICATIONS INFORMATION

Analog Input Charateristics: Ftune = VCC to VEE



Propagation Delay vs Ftune Voltage (100E196)



Propagation Delay vs Ftune Voltage (10E196)

Using the FTUNE Analog Input

The analog FTUNE pin on the E196 device is intended to enhance the 20ps resolution capabilities of the fully digital E195. The level of resolution obtained is dependent on the number of increments applied to the appropriate range on the FTUNE pin.

To provide another level of resolution, the FTUNE pin must be capable of adjusting the delay by greater than the 20ps digital resolution. As shown in the provided graphs, this requirement is easily achieved since a 100ps delay can be achieved over the entire FTUNE voltage range.This extra analog range ensures that the FTUNE pin will be capable, even under worst case conditions, of covering the digital resolution.

Typically, the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, the graphs provided should be used. As an example, if a range of 40ps is selected to cover worst case conditions and ensure coverage of the digital range, from the 100E196 graph a voltage range of –3.25V to –4V would be necessary on the FTUNE pin. Obviously, there are numerous voltage ranges which can be used to cover a given delay range. Users are given the flexibility to determine which one best fits their design.

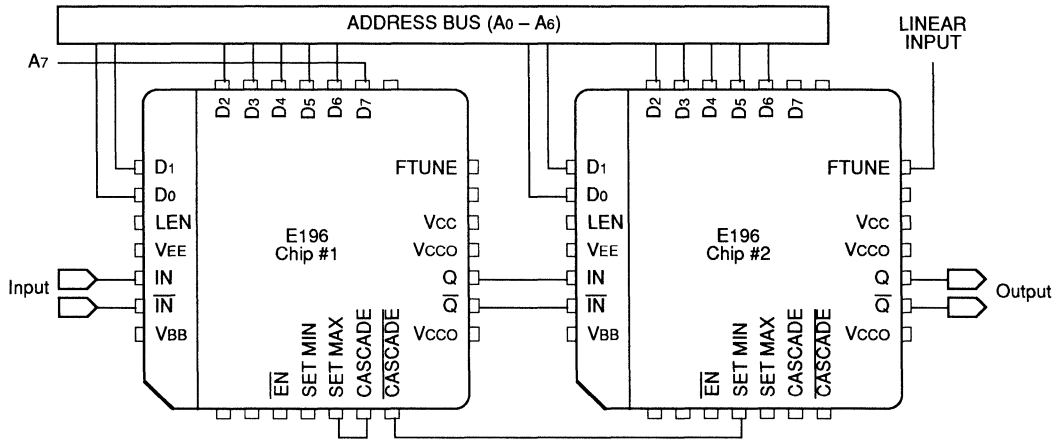


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E196s

To increase the programmable range of the E196, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E196s without the need for any external gating. Furthermore, this capability requires only one more address line per added E196. Obviously, cascading multiple PDCs will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E196s. As can be seen, this scheme can easily be expanded for larger E196 chains. The D7 input of the E196 is the cascade control pin. With the interconnect scheme of Figure 1, when D7 is asserted, it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low, the cascade output will also be low, while the cascade bar output will be a logical high. In this condition, the SET MIN pin of chip #2 will be asserted and, thus, all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding, any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1, on the other hand, will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate

delays (1111111 on the A_0–A_6 address bus), D_7 will be asserted to signal the need to cascade the delay to the next E196 device. When D_7 is asserted, the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A_0–A_6 address bus. Chip #1, on the other hand, will have its SET MAX pin asserted, resulting in the device delay to be independent of the A_0–A_6 address bus.

When the SET MAX pin of chip #1 is asserted, the D_0 and D_1 latches will be reset, while the rest of the latches will be set. In addition, to maintain monotonicity, an additional gate delay is selected in the cascade circuitry. As a result, when D_7 of chip #1 is asserted, the delay increases from 31.75 gates to 32 gates. A 32-gate delay is the maximum delay setting for the E196.

When cascading multiple PDCs, it will prove more cost-effective to use a single E196 for the MSB of the chain, while using E195 for the lower order bits. This is due to the fact that only one fine tune input is needed to further reduce the delay step resolution.

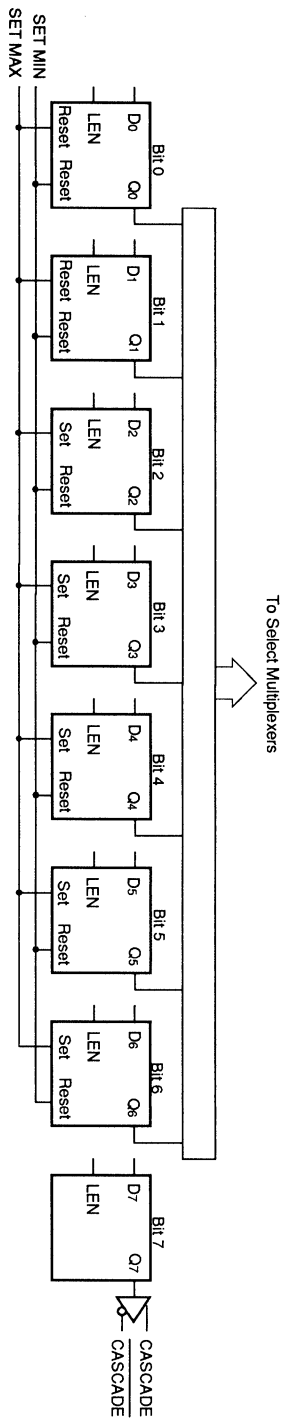


Figure 2. Expansion of the Latch Section of the E196 Block Diagram

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E196JC	J28-1	Commercial
SY100E196JC	J28-1	Commercial

10EL SERIES DC ELECTRICAL CHARACTERISTICS(1)

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND(2)

		–40°C		0°C		+25°C		+85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

NOTE:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

100EL SERIES DC ELECTRICAL CHARACTERISTICS(1)

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND(2)

		–40°C			0°C to +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620		or V_{IL} (Min.)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(Max.)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610		or V_{IL}(Min.)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	—
V_{IL}	Input LOW Voltage	–1810	—	–1475	–1810	—	–1475	mV	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(Max.)

NOTE:

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{OUT}	Output Current: Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}(2)	Operating Range	–5.7 to –4.2	V

NOTES:

1. Absolute maximum rating, beyond which device life may be imparied unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

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Issue Date: April, 1994

1:2 DIFFERENTIAL FANOUT BUFFER

ClockWorks™
PRELIMINARY
SY10/100EL11

FEATURES

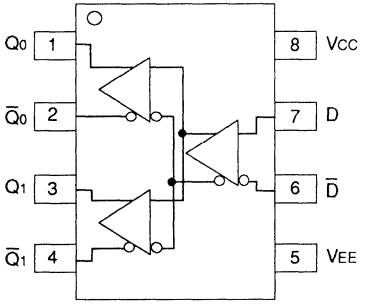
- 265ps propagation delay
- 5ps skew between outputs
- High bandwidth output transitions
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V

DESCRIPTION

The SY10EL/100EL11 are 1:2 differential fanout gates. These devices are functionally similar to the E111 devices, with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the EL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the EL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to VEE), the Q outputs will go LOW.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D	Data Inputs
Q0, Q1	Data Outputs

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	26	—	21	26	31	21	26	31	21	26	31	
	100EL	—	26	—	21	26	31	21	26	31	24	30	36	
VEE	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	260	—	185	260	335	190	265	340	215	290	365	ps
tSKEW	Within-Device Skew(1)	—	5	—	—	5	20	—	5	20	—	5	20	ps
	Duty Cycle Skew(2)	—	5	—	—	5	20	—	5	20	—	5	20	
VPP	Minimum Input Swing(3)	150	—	—	150	—	—	150	—	—	150	—	—	mV
VCMR	Common Mode Range(4)	–0.4	—	(4)	–0.4	—	(4)	–0.4	—	(4)	–0.4	—	(4)	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Within-device skew defined as identical transitions on similar paths through a device.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL11ZC	Z8-1	Commercial
SY100EL11ZC	Z8-1	Commercial

FEATURES

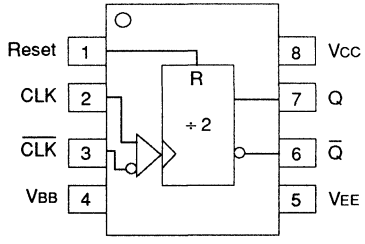
- **510ps propagation delay**
- **3.0GHz toggle frequency**
- **High bandwidth output transistions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL32 are integrated ÷2 dividers. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01µF capacitor. Also note that the VBB is designed to be used as an input bias on the EL32 only; the VBB output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-on, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32s in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
VBB	Reference Voltage Output
Q	Data Outputs

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
IEE	Power Supply Current													mA
	10EL	—	25	—	—	25	30	—	25	30	—	25	30	
	100EL	—	25	—	—	25	30	—	25	30	—	29	35	
VBB	Output Reference Voltage													V
	10EL	–1.43	—	–1.30	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	
	100EL	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
VEE	Power Supply Voltage													V
	10EL	—	–5.2	—	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	—	–4.5	—	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	—	3.0	—	2.6	3.0	—	2.6	3.0	—	2.6	3.0	—	GHz
t_{PLH} t_{PHL}	Prop Delay to Output D Reset to Q	— —	500 540	— —	410 440	500 540	590 640	420 440	510 540	600 640	450 450	540 550	630 650	ps
V_{PP}	Minimum Input Swing[1]	150	—	—	150	—	—	150	—	—	150	—	—	mV
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTE:

1. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL32ZC	Z8-1	Commercial
SY100EL32ZC	Z8-1	Commercial

FEATURES

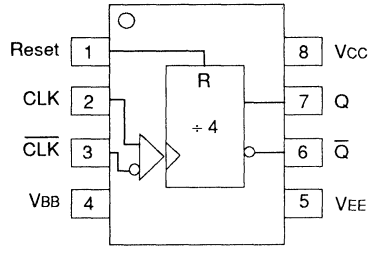
- 650ps propagation delay
- 4.0GHz toggle frequency
- High bandwidth output transistions
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V

DESCRIPTION

The SY10EL/100EL33 are integrated ÷4 dividers. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01µF capacitor. Also note that the VBB is designed to be used as an input bias on the EL33 only; the VBB output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset input allows for the synchronization of multiple EL33s in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
VBB	Reference Voltage Output
Q	Data Outputs

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	27	—	—	27	33	—	27	33	—	27	33	
	100EL	—	27	—	—	27	33	—	27	33	—	31	37	
VBB	Output Reference Voltage 10EL	–1.43	—	–1.30	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V
	100EL	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
VEE	Power Supply Voltage													V
	10EL	—	–5.2	—	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	—	–4.5	—	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	—	4.2	—	3.8	4.2	—	3.8	4.2	—	3.8	4.2	—	GHz
t_{PLH} t_{PHL}	Prop. Delay to Output D Reset to Q	— —	630 460	— —	540 360	630 460	720 560	550 360	640 460	730 560	590 380	670 480	760 580	ps
V_{PP}	Minimum Input Swing[1]	150	—	—	150	—	—	150	—	—	150	—	—	mV
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTE:

1. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL33ZC	Z8-1	Commercial
SY100EL33ZC	Z8-1	Commercial

÷2, ÷4, ÷8 CLOCK GENERATION CHIP

FEATURES

- **50ps output-to-output skew**
- **Synchronous enable/disable**
- **Master Reset for synchronization**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

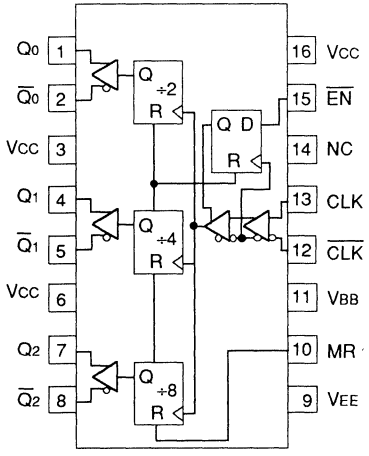
DESCRIPTION

The SY10EL/100EL34 are low skew ÷2, ÷4, ÷8 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL34 under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34s in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
$\overline{EN}$	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0	Differential ÷2 Outputs
Q_1	Differential ÷4 Outputs
Q_2	Differential ÷8 Outputs

TRUTH TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

NOTE:
Z = LOW-to-HIGH transition
ZZ = HIGH-to-LOW transition

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Issue Date: April, 1994

AC/DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	65	—	—	65	—	—	65	—	—	65	—	mA
V_{BB}	Output Reference 10EL Voltage 100EL	–1.43 –1.38	— —	–1.30 –1.26	–1.38 –1.38	— —	–1.27 –1.26	–1.35 –1.38	— —	–1.25 –1.26	–1.31 –1.38	— —	–1.19 –1.26	V
I_{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR	— —	1100 800	—	— —	1100 800	—	— —	1100 800	—	— —	1100 800	—	ps
t_{SKEW}	Within-Device Skew	—	100	—	—	100	—	—	100	—	—	100	—	ps
t_S	Set-up Time $\overline{EN}$	—	150	—	—	150	—	—	150	—	—	150	—	ps
t_H	Hold Time $\overline{EN}$	—	150	—	—	150	—	—	150	—	—	150	—	ps
V_{PP}	Minimum Input Swing	250	—	—	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	Common Mode Range CLK	–2.0	—	–4.0	–2.0	—	–0.4	–2.0	—	–0.4	–2.0	—	–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	—	400	—	—	400	—	—	400	—	—	400	—	ps

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL34ZC	Z16-1	Commercial
SY100EL34ZC	Z16-1	Commercial

DC characteristics for the 100K parametric limits listed below are guaranteed for the entire *SUPER-300K* family **unless specified on the individual data sheet.**

The specified DC limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

GUARANTEED OPERATING CONDITIONS[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{EE}	Supply Voltage	–4.8	–4.5	–4.2	V
T_A	Operating Temperature	0	25	85	°C

NOTE:

1. Referenced to V_{CC}.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{EE}	V_{EE} Pin Potential to Ground Pin	+0.5 to –7.0	V
V_{IN}	Input Voltage	+0.5 to V_{EE}	V
I_{OUT}	DC Output Current (Output HIGH)	–50	mA
T_C	Temperature Under Bias	–55 to +125	°C
T_j	Junction Temperature	+150	°C
T_{store}	Storage Temperature	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V, Output Load = 50Ω to –2.0V, V_{EE} = –4.5V, T_A = 0°C to 85°C

Symbol	Parameter	V_{EE}	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–4.2V	–1020	—	–870	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
		–4.5V	–1025	–955	–880		
		–5.46V	–1035	—	–880		
V_{OL}	Output LOW Voltage	–4.2V	–1810	—	–1605	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
		–4.5V	–1810	–1705	–1620		
		–5.46V	–1830	—	–1620		
V_{OHC}	Output HIGH Voltage	–4.2V	–1030	—	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
		–4.5V	–1035	—	—		
		–5.46V	–1045	—	—		
V_{OLC}	Output LOW Voltage	–4.2V	—	—	–1595	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
		–4.5V	—	—	–1610		
		–5.46V	—	—	–1610		
V_{IH}	Input HIGH Voltage	–4.2V	–1150	—	–870	mV	Guaranteed Input Voltage HIGH for All Inputs
		–4.5V	–1165	—	–880		
		–5.46V	–1165	—	–880		
V_{IL}	Input LOW Voltage	–4.2V	–1810	—	–1475	mV	Guaranteed Input Voltage LOW for All Inputs
		–4.5V	–1810	—	–1475		
		–5.46V	–1830	—	–1490		
I_{IL}	Input LOW Current	–4.5V	+0.5	—	—	µA	V_{IN} = V_{IL} Min.

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Issue Date: April, 1994

SYNERGY SEMICONDUCTOR

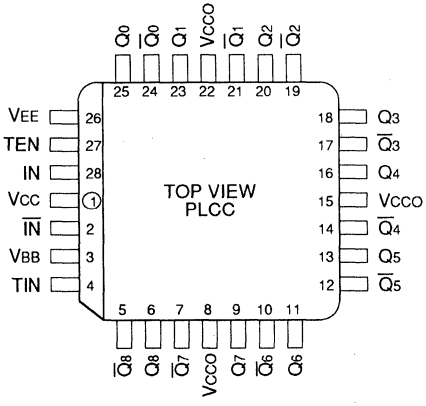
SINGLE SUPPLY PECL 1:9 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY100S811

FEATURES

- PECL version of popular ECLinPS E111
- Low skew
- Guaranteed skew spec
- V_{BB} output
- TTL enable input
- Selectable TTL or PECL clock input
- Single +5V supply
- Differential internal design
- Similar pin configuration to E111
- PECL I/O fully compatible with industry standard
- Internal 75KΩ PECL input pull-down resistors
- ESD protection of 2000V

PIN CONFIGURATION



DESCRIPTION

The SY100S811 is a low skew 1-to-9 PECL differential driver designed for clock distribution in new, high-performance PECL systems. It accepts either a PECL clock input or a TTL input by using the TTL enable pin TEN. When the TTL enable pin is at a TTL logic one level, the TTL input is enabled and the PECL input is disabled. When the enable pin is set to TTL logic zero level, the TTL input is disabled and the PECL input is enabled.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E811 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO} as the pair(s) being used on that side) in order to maintain minimum skew.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of PECL signals to that device only. When using V_{BB} for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01µF capacitor.

PIN NAMES

Pin	Function
EIN, $\overline{EIN}$	Differential PECL Input Pair
TIN	TTL Input
TEN	TTL Input Enable
Q0, $\overline{Q0}$ – Q8, $\overline{Q8}$	Differential PECL Outputs
V_{BB}	V_{BB} Output
V_{CC}	PECL V_{CC} (+5.0V)
V_{EE}	PECL Ground (0V)

TRUTH TABLE

TEN	EIN	TIN	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

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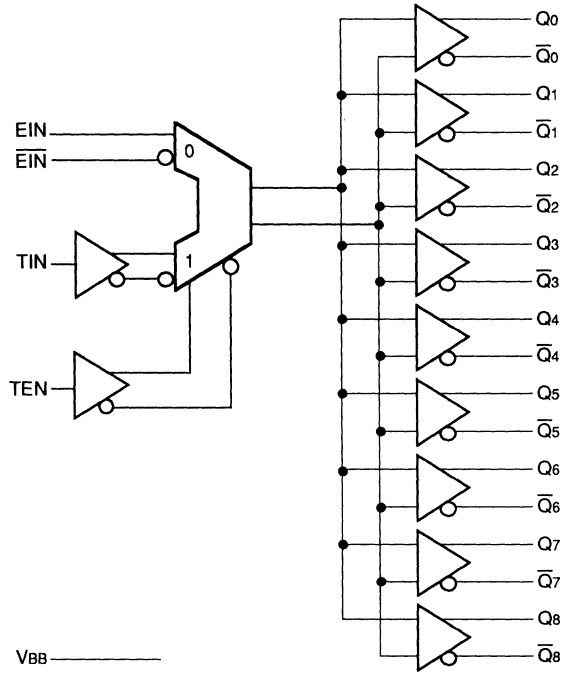
BLOCK DIAGRAM



PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V	$V_{CC} = V_{CCO} = 5.0V$
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.835	—	4.12	3.835	—	4.12	3.835	—	4.12	V	$V_{CC} = V_{CCO} = 5.0V$
V_{IL}	Input LOW Voltage	3.19	—	3.525	3.19	—	3.525	3.19	—	3.525	V	$V_{CC} = V_{CCO} = 5.0V$
I_{CC}	Power Supply Current	—	53	65	—	53	65	—	60	74	mA	All inputs and outputs open

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	—
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	— —	20 100	— —	— —	20 100	— —	— —	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = 5.0V$
I_{IL}	Input LOW Current	—	—	–0.6	—	—	–0.6	—	—	–0.6	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	–1.2	—	—	–1.2	—	—	–1.2	V	$I_{IN} = -18mA$

AC ELECTRICAL CHARACTERISTICS[1–6]

$V_{CC} = V_{CCO} = 5V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output[1] EIN (differential) EIN (single-ended) TIN	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	ps	 2 3
t_{SKEW}	Within-Device Skew	—	25	50	—	25	50	—	25	50	ps	4
V_{PP}	Minimum PECL Input Swing	250	—	—	250	—	—	250	—	—	mV	5
V_{CMR}	PECL Common Mode Range	–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V	6
t_r t_f	Output Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps	—

NOTES:

1. Part-to-part skew is defined as Max. — Min. value at the given temperature.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the S811, as a differential input as low as 50mV will still produce full PECL levels at the output.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

PRODUCT ORDERING CODE

ORDERING CODE	PACKAGE TYPE	OPERATING RANGE
SY100S811JC	J28-1	Commercial

DC SPECIFICATIONS 10H AND 100H

10H ECL DC ELECTRICAL

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	225	—	145	—	145	µA	—
I_{IL}	Input LOW Current	—	1.5	—	1.0	—	1.0	mA	—
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1070	–735	mV	—
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	mV	—
V_{OH}	Output HIGH Voltage	–1020	–840	–980	–810	–920	–735	mV	50Ω to –2.0V
V_{OL}	Output LOW Voltage	–1950	–1630	–1950	–1630	–1950	–1600	mV	50Ω to –2.0V

100H ECL DC ELECTRICAL

V_{CCT} = 5.0V ± 10%; V_{EE} = –4.5V ± 0.3V

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	225	—	145	—	145	µA	—
I_{IL}	Input LOW Current	—	1.5	—	1.0	—	1.0	mA	—
V_{IH}	Input HIGH Voltage	–1165	–880	–1165	–880	–1165	–880	mV	—
V_{IL}	Input LOW Voltage	–1810	–1475	–1810	–1475	–1810	–1475	mV	—
V_{OH}	Output HIGH Voltage	–1025	–880	–1025	–880	–1025	–880	mV	50Ω to –2.0V
V_{OL}	Output LOW Voltage	–1810	–1620	–1810	–1620	–1810	–1620	mV	50Ω to –2.0V

TTL DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version), V_{EE} = –4.5V ± 0.3V (100H Version)

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	20 100	— —	20 100	— —	20 100	µA	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current	—	–0.6	—	–0.6	—	–0.6	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	–1.2	—	–1.2	—	–1.2	V	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	I_{OL} = 48mA

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SINGLE SUPPLY PECL-TTL 1:9 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H641

FEATURES

- PECL–TTL version of popular ECLinPS E111
- Guaranteed low skew specification
- Latch
- Differential internal design
- VBB output for single-ended operation
- Single +5V supply
- ESD protection of 2000V
- Reset/enable
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H641/100H641

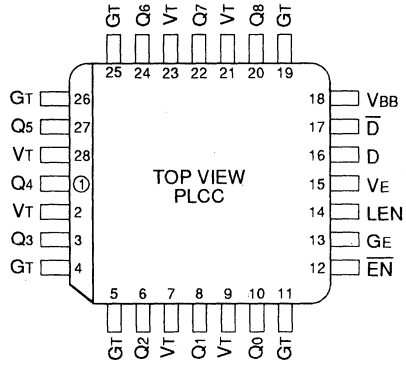
DESCRIPTION

The SY10H641 and SY100H641 are single supply, low skew translating 1:9 clock drivers. Devices in the Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

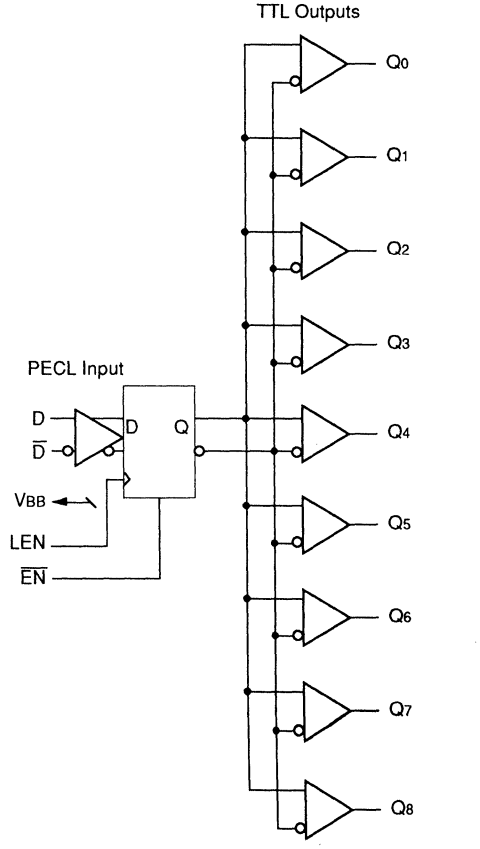
The devices feature a 24mA TTL output stage with AC performance specified into a 50pF load capacitance. A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL VCC (+5.0V)
VE	ECL VCC (+5.0V)
GE	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
VBB	VBB Reference Output (positive ECL)
Q0 - Q8	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)
LEN	Latch Enable Input (positive ECL)

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Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	Vdc
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	Vdc
	V_I (TTL)	–0.5 to +7.0	
Disabled 3-State Output	V_{OUT} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{OUT} (ECL)	50	mAdc
Output Source Current Surge	I_{OUT} (ECL)	100	mAdc
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

NOTE:

1. Do not exceed.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	H	L	Q_0
X	X	H	L

3

DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	30	—	30	—	30	mA	V_E Pin
I_{CCH}		TTL	—	30	—	30	—	30		Total all V_T pins
I_{CCL}			—	35	—	35	—	35		

AC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_8	5.0	6.0	4.8	5.8	5.3	6.3	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew	Q_0–Q_8	—	1.0	—	1.0	—	1.0	ns	C_L = 50pF
t_{skwd}	Within-Device Skew	Q_0–Q_8	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Output	Q_0–Q_8	4.9	6.9	4.9	6.9	5.0	7.0	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_8	5.0	7.0	4.9	6.9	5.0	7.0	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_8	— —	1.7 1.6	— —	1.7 1.6	— —	1.7 1.6	ns	C_L = 50pF
f_{MAX}	Maximum Input Frequency		135	—	135	—	135	—	MHz	C_L = 50pF
—	Pulse Width		1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time		1.25	—	1.25	—	1.25	—	ns	—
t_{SET}(1)	Set-up		0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—
t_{HOLD}(1)	Hold Time		0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—

NOTE:

1. Guaranteed, but not tested.

VCC AND CLOAD

Ranges to meet duty cycle requirement: 0°C ≤ TA ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_{W1}	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \leq 40MHz$	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_{W2}	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \leq 50MHz$	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

PIN DESCRIPTION

Pin	Symbol	Description
1	Q_4	Signal Output (TTL)
2	V_T	TTL V_{CC} (+5.0V)
3	Q_3	Signal Output (TTL)
4	G_T	TTL Ground (0V)
5	G_T	TTL Ground (0V)
6	Q_2	Signal Output (TTL)
7	V_T	TTL V_{CC} (+5.0V)
8	Q_1	Signal Output (TTL)
9	V_T	TTL V_{CC} (+5.0V)
10	Q_0	Signal Output (TTL)
11	G_T	TTL Ground (0V)
12	$\overline{EN}$	Enable Input POS (ECL)
13	G_E	ECL Ground (0V)
14	LEN	Latch Enable Input POS (ECL)

Pin	Symbol	Description
15	V_E	ECL V_{CC} (+5.0V)
16	D	ECL Signal Input (Non-inverting)
17	$\overline{D}$	ECL Signal Input (Inverting)
18	V_{BB}	V_{BB} Reference Output POS (ECL)
19	G_T	TTL Ground (0V)
20	Q_8	Signal Output (TTL)
21	V_T	TTL V_{CC} (+5.0V)
22	Q_7	Signal Output (TTL)
23	V_T	TTL V_{CC} (+5.0V)
24	Q_6	Signal Output (TTL)
25	G_T	TTL Ground (0V)
26	G_T	TTL Ground (0V)
27	Q_5	Signal Output (TTL)
28	V_T	TTL V_{CC} (+5.0V)

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	$I_{OH} = -3.0mA$ $I_{OH} = -15mA$
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	$I_{OL} = 24mA$
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	$V_{OUT} = 0V$

3

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH}(1) V_{IL}(1)	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	$V_E = 5.0V$
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	$V_E = 5.0V$

NOTE:

1. V_{IH} and V_{IL} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for $V_{CC} = 5.0V$.

100H ECL DC ELECTRICAL CHARACTERISTICS

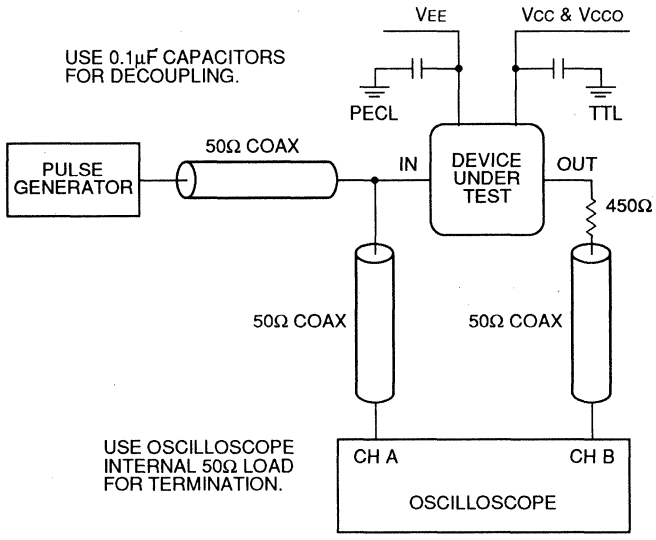
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH}(1) V_{IL}(1)	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	$V_E = 5.0V$
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	$V_E = 5.0V$

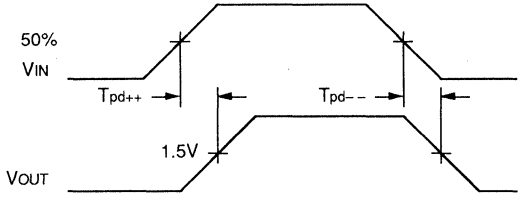
NOTE:

1. V_{IH} and V_{IL} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for $V_{CC} = 5.0V$.

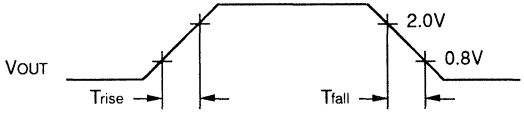
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H641JC	J28-1	Commercial	10KH
SY100H641JC	J28-1	Commercial	100K

FEATURES

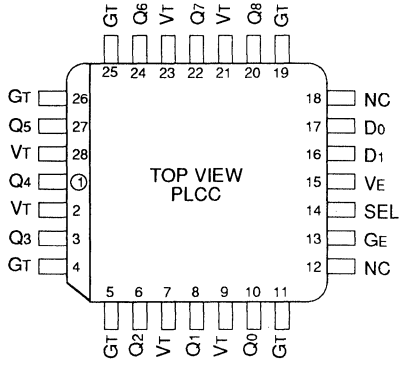
- **Low skew(typically 0.65ns within device)**
- **Guaranteed skew spec 1.25ns part-to-part**
- **Input clock muxing**
- **Differential ECL internal design**
- **Single +5V supply**
- **ESD protection of 2000V**
- **Extra TTL and ECL power/ground pins**
- **Fully compatible with Motorola MC10H645**

DESCRIPTION

The SY10H645 is a single supply, low skew, TTL I/O 1:9 Clock Driver. Devices in the H600 clock driver family utilize the 28-lead PLCC for optimal power and signal pin placement.

The device features a 24mA TTL output stage with AC performance specified into a 50pF load capacitance. A 2:1 input mux is provided on-chip to allow for distributing both system and diagnostic clock signals or designing clock redundancy into a system. With the SEL input held LOW, the D_0 input will be selected, while the D_1 input is selected when the SEL input is forced HIGH.

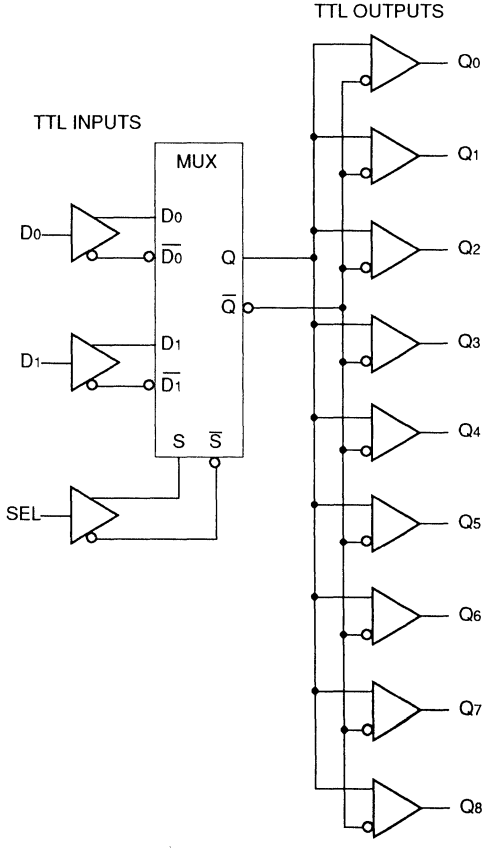
PIN CONFIGURATION



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
Dn	TTL Signal Input
Q0 - Q8	TTL Signal Outputs
SEL	TTL Mux Select

BLOCK DIAGRAM



Rev.: A Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (TTL)	–0.5 to +7.0	V
Disabled 3-State Output	V_{OUT} (TTL)	0.0 to V_T	V
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Do not exceed.

TRUTH TABLE

D_0	D_1	SEL	Q
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	30	—	30	—	30	mA	V_E Pin
I_{CCH}		TTL	—	30	—	30	—	30		Total all V_T pins
I_{CCL}			—	35	—	35	—	35		
V_{OH}	Output HIGH Voltage		2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage		—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current		–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

AC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_0 to Output Only	Q_0–Q_8	5.2	6.2	5.2	6.2	5.6	6.6	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew D_0 to Output Only	Q_0–Q_8	—	1.0	—	1.0	—	1.0	ns	—
t_{skwd}[1]	Within-Device Skew D_0 to Output Only	Q_0–Q_8	—	0.65	—	0.65	—	0.65	ns	—
t_{PLH} t_{PHL}	Propagation Delay SEL to Q	Q_0–Q_8	5.2	7.3	5.2	7.2	5.7	7.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 0.8V to 2.0V	Q_0–Q_8	0.5 0.5	1.7 1.6	0.5 0.5	1.7 1.6	0.5 0.5	1.7 1.6	ns	C_L = 50pF
t_S	Set-up Time, SEL to D	—	1.0	—	1.0	—	1.0	—	ns	—

NOTE:

1. Within-device skew defined as identical transitions on similar paths through a device.

DUTY CYCLE SPECIFICATIONS

0°C ≤ TA ≤ +85°C. Duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
PW	Range of VCC and CL to meet min.	VCC	4.875	5.0	5.125	V	All Outputs
	pulse width (HIGH or LOW) at	CL	10.0	—	50	pF	
	fOUT ≤ 50MHz	PW	9.0	—	11.0	ns	

PIN DESCRIPTION

Pin	Symbol	Description
1	Q4	Signal Output (TTL)
2	VT	TTL VCC (+5.0V)
3	Q3	Signal Output (TTL)
4	GT	TTL Ground (0V)
5	GT	TTL Ground (0V)
6	Q2	Signal Output (TTL)
7	VT	TTL VCC (+5.0V)
8	Q1	Signal Output (TTL)
9	VT	TTL VCC (+5.0V)
10	Q0	Signal Output (TTL)
11	GT	TTL Ground (0V)
12	NC	No Connection
13	GE	ECL Ground (0V)
14	SEL	Select Input (TTL)

Pin	Symbol	Description
15	VE	ECL VCC (+5.0V)
16	D1	ECL Signal Input (Non-inverting)
17	D0	ECL Signal Input (Inverting)
18	NC	No Connection
19	GT	TTL Ground (0V)
20	Q8	Signal Output (TTL)
21	VT	TTL VCC (+5.0V)
22	Q7	Signal Output (TTL)
23	VT	TTL VCC (+5.0V)
24	Q6	Signal Output (TTL)
25	GT	TTL Ground (0V)
26	GT	TTL Ground (0V)
27	Q5	Signal Output (TTL)
28	VT	TTL VCC (+5.0V)

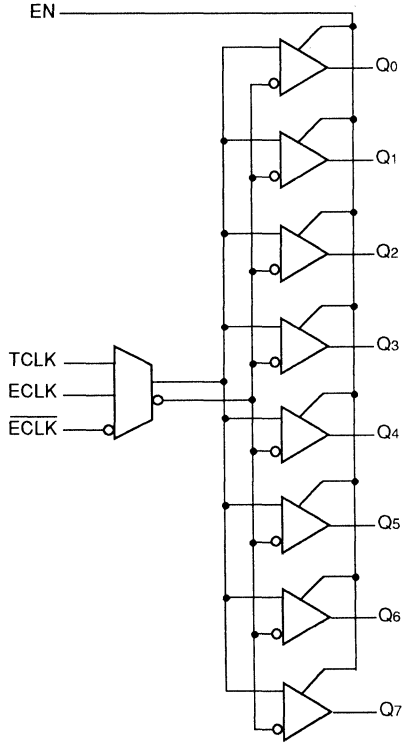
PECL/TTL–TTL 1:8 CLOCK DISTRIBUTION CHIP

ClockWorks™
PRELIMINARY
SY10/100H646

FEATURES

- PECL/TTL–TTL version of popular ECLinPS E111
- Meets specifications required to drive high-performance x86 processors
- Guaranteed low skew specification
- Three-state enable
- Differential internal design
- VBB output for single-ended operation
- Single +5V supply
- ESD protection of 2000V
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: 10H or 100K
- Matched high and low output impedance
- Fully compatible with Motorola MC10/100H646

BLOCK DIAGRAM



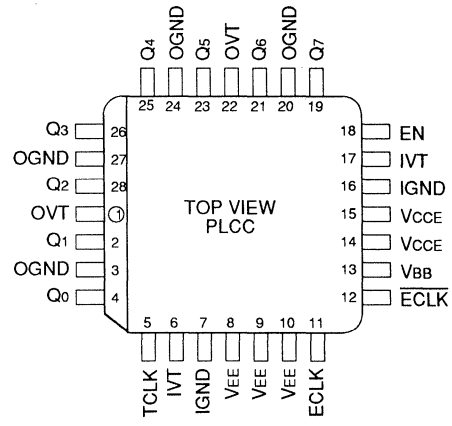
DESCRIPTION

The SY10H646 and SY100H646 are single supply, low skew translating 1:8 clock drivers. Devices in the Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance. The single supply H646 is similar to the H643 which is a dual supply 1:8 version of the same function.

The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

The 10H version is compatible with 10H ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



PIN NAMES

Pin	Function
OGND	TTL Output Ground (0V)
OVT	TTL Output VCC (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL VCC (+5.0V)
VEE	ECL VEE (0V)
VCCE	ECL Ground (+5.0V)
ECLK, $\overline{\text{ECLK}}$	Differential Signal Input (PECL)
VBB	VBB Reference Output
Q0–Q7	Signal Outputs (TTL)
EN	Three-State Enable Input (TTL)
LEN	Signal Input (TTL)

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DC ELECTRICAL CHARACTERISTICS

$V_T = OVT = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.6	—	2.6	—	2.6	—	V	I_{OH} =24mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	—	—	—	—	—	—	mA	Note 1

NOTE:

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting Ios resistor.

3

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = OVT = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	225	—	—	175	—	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.83	—	4.16	3.87	—	4.19	3.94	—	4.28	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{IL}	Input LOW Voltage	3.05	—	3.52	3.05	—	3.52	3.05	—	3.555	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{BB}	Output Reference Voltage	3.62	—	3.73	3.65	—	3.75	3.69	—	3.81	V	IVT = IVO = V_{CCE} = 5.0V(1)

NOTE:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = +5.0V.

100K ECL DC ELECTRICAL CHARACTERISTICS

$V_T = OVT = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	225	—	—	175	—	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.835	—	4.12	3.835	—	4.12	3.835	—	3.835	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{IL}	Input LOW Voltage	3.19	—	3.525	3.19	—	3.525	3.19	—	3.525	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{BB}	Output Reference Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V	IVT = IVO = V_{CCE} = 5.0V(1)

NOTE:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = +5.0V.

DC ELECTRICAL CHARACTERISTICS

IVT = OVT = VCCE = 5.0V ± 5%

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{CCL}	Power Supply Current	—	—	—	—	166	—	—	—	—	mA	Total all OVT,
I_{CCH}		—	—	—	—	154	—	—	—	—		IVT, and VCCE pins

AC ELECTRICAL CHARACTERISTICS

IVT = OVT = VCCE = 5.0V ± 5%

Symbol	Parameter		T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output	Q_0–Q_7	—	—	—	—	6.5	—	—	—	—	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew		—	—	1.0	—	—	1.0	—	—	1.0	ns	
t_{skwd}	Within-Device Skew		—	—	0.5	—	—	0.5	—	—	0.5	ns	
t_W	Pulse Width Out HIGH or LOW @ f_{OUT} = 50MHz	Q_0–Q_7	9.0	—	—	9.0	—	—	9.0	—	—	ns	C_L = 50pF
t_R t_F	Output Rise/Fall Time 0.8V to 2.4V 0.8V to 2.0V	Q_0–Q_7	 — —	 — —	 1.6 1.2	 0.7 0.3	 — —	 1.6 1.2	 — —	 — —	 1.6 1.2	ns	C_L = 50pF

NOTE:

The pre-silicon simulation value for typical propagation delay to all outputs is 6.5ns. Final value will be established as the measured statistical mean after characterization of a sufficient number of lots, and thus may not exactly equal the target. The skew specification is an absolute value that measures the worst case t_{PD} difference between any two of the specified outputs.

TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

NOTE:

X = Don't Care

L = Low Voltage Level

H = High Voltage Level

Z = Three-State

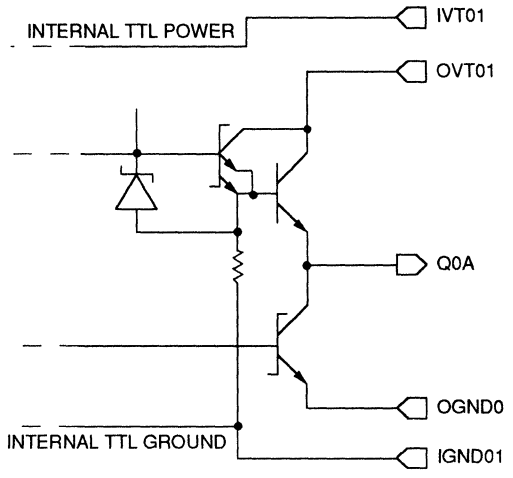


Figure 1. Output Structure

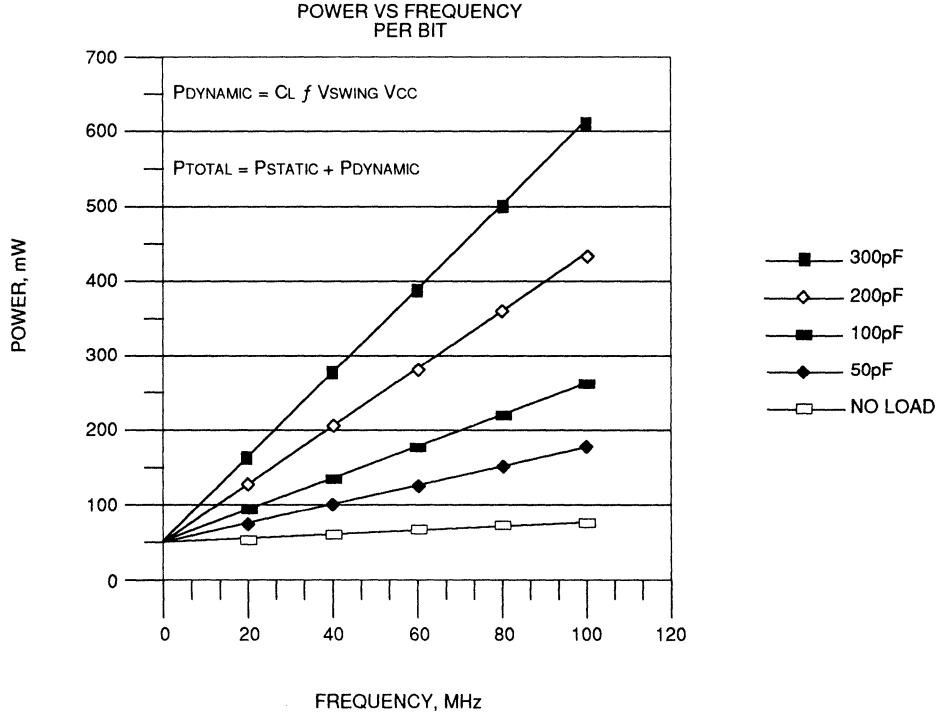


Figure 2. Power Versus Frequency (Typical)

SINGLE SUPPLY PECL-TTL 1:4 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H841

FEATURES

- Translates positive ECL to TTL (PECL-TTL)
- 300ps pin-to-pin skew
- Guaranteed skew spec
- Differential internal design for increased noise immunity and stable threshold inputs
- V_{BB} reference output
- Single supply
- Enable input
- Latch enable input
- Extra TTL and ECL power/ground pins to reduce cross-talk/noise
- High drive capability: 24mA each output
- ESD protection of 2000V
- Fully compatible with industry standard 10K, 100K I/O levels

DESCRIPTION

The SY10H841 and SY100H841 are single supply, low skew translating 1:4 clock drivers.

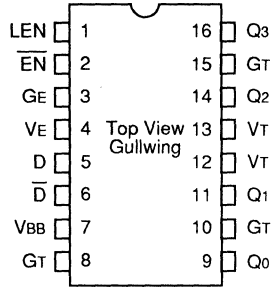
The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

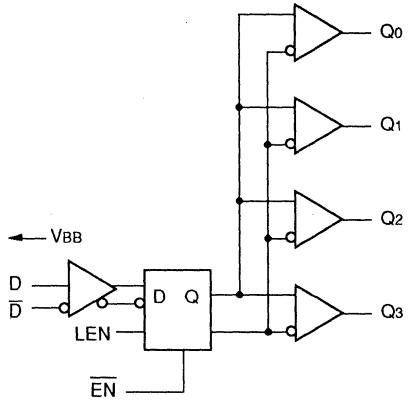
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H841 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
G_T	TTL Ground (0V)
V_T	TTL V_{CC} (+5.0V)
V_E	ECL V_{CC} (+5.0V)
G_E	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output (positive ECL)
Q_0 - Q_3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)
LEN	Latch Enable Input

Rev.: A Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	V
	V_{OUT} (TTL)	0.0 to V_T	
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	$\overline{EN}$	Enable Input Pos (ECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output Pos (ECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+5.0V)
13	V_T	TTL V_{CC} (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skwd++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skwd--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF
—	Pulse Width	Q_0–Q_3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q_0–Q_3	1.0	—	1.0	—	1.0	—	ns	—
t_S	Set-up Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—
t_H	Hold Time D, EN	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—

NOTES:

1. Device-to-Device Skew considering the same transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

V_{CC} AND C_{LOAD}

Ranges to meet duty cycle requirement: 0°C ≤ T_A ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at f_{OUT} ≤ 40MHz	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at f_{OUT} ≤ 50MHz	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	V_{OUT} = 0V

3

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

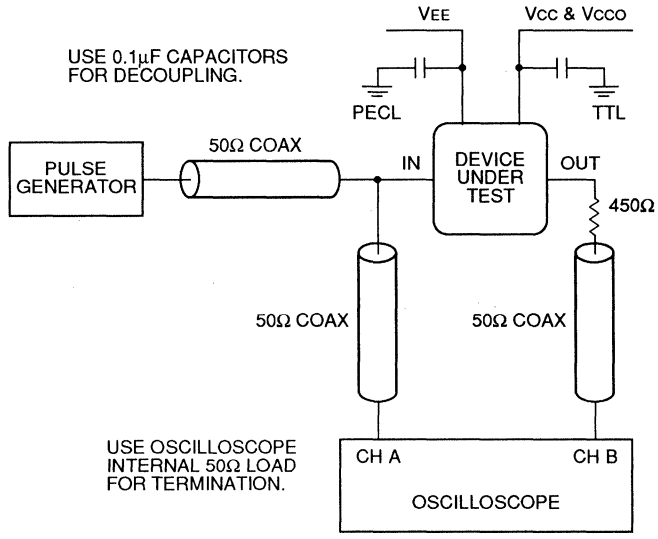
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	V_E = 5.0V

100H ECL DC ELECTRICALCHARACTERISTICS

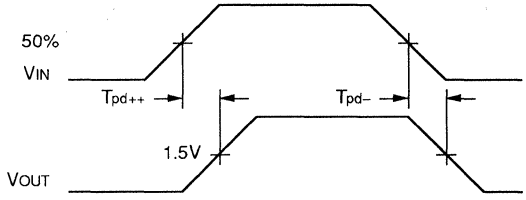
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	V_E = 5.0V

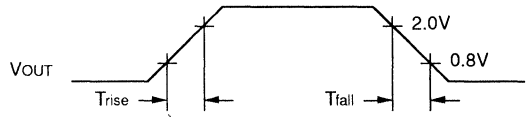
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H841ZC	Z16-1	Commercial	10KH
SY100H841ZC	Z16-1	Commercial	100K

SINGLE SUPPLY PECL-TTL 1:4 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H842

FEATURES

- Translates positive ECL to TTL (PECL-TTL)
- 300ps pin-to-pin skew
- Guaranteed skew spec
- Differential internal design for increased noise immunity and stable threshold inputs
- V_{BB} reference output
- Single supply
- Enable input
- Extra TTL and ECL power/ground pins to reduce cross-talk/noise
- High drive capability: 24mA each output
- ESD protection of 2000V
- Fully compatible with industry standard 10K, 100K I/O levels

DESCRIPTION

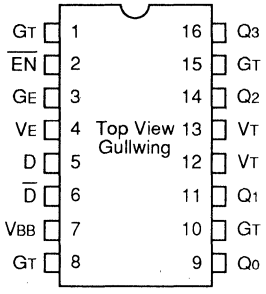
The SY10H842 and SY100H842 are single supply, low skew translating 1:4 clock drivers.

The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

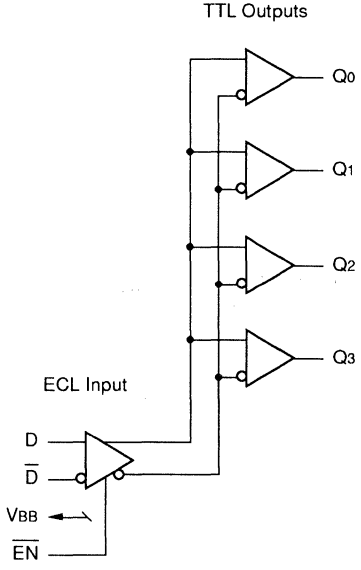
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H842 solves several clock distribution problems such as minimizing skew 300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
VBB	VBB Reference Output (positive ECL)
Q0 - Q3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)

Rev.: A Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	V
	V_{OUT} (TTL)	0.0 to V_T	
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	$\overline{EN}$	Q
L	L	L
H	L	H
X	H	L

PIN DESCRIPTION

Pin	Symbol	Description
1	G_T	TTL Ground (0V)
2	$\overline{EN}$	Enable Input Pos (ECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output Pos (ECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+5.0V)
13	V_T	TTL V_{CC} (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	35	—	35	—	35	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.5	3.5	2.5	3.5	2.5	3.5	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skwd++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skwd--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_3	2.5	3.5	2.5	3.5	2.5	3.5	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF

NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

V_{CC} AND C_{LOAD}

Ranges to meet duty cycle requirement: $0°C \le T_A \le 85°C$. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \le 40MHz$	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \le 50MHz$	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	V_{OUT} = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

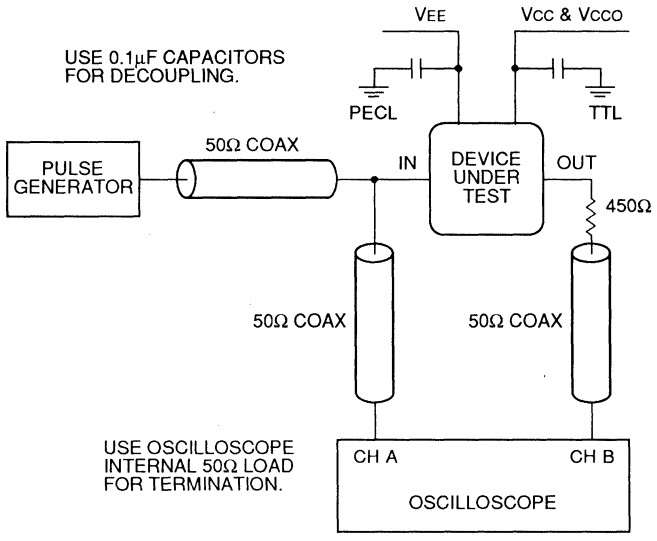
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	V_E = 5.0V

100H ECL DC ELECTRICALCHARACTERISTICS

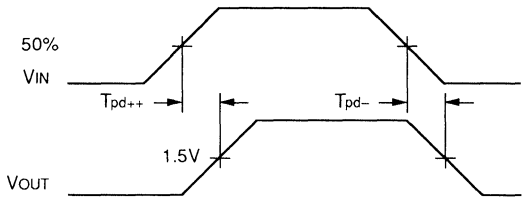
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	V_E = 5.0V

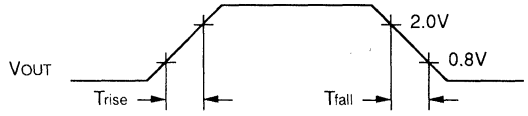
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H842ZC	Z16-1	Commercial	10KH
SY100H842ZC	Z16-1	Commercial	100K

SYNERGY SEMICONDUCTOR

SINGLE SUPPLY PECL-TTL 1:4 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H843

FEATURES

- **Translates positive ECL to TTL (PECL-TTL)**
- **300ps pin-to-pin skew**
- **Guaranteed skew spec**
- **Differential internal design for increased noise immunity and stable threshold inputs**
- **V_{BB} reference output**
- **Single supply**
- **Enable input**
- **Latch enable input**
- **Extra TTL and ECL power/ground pins to reduce cross-talk/noise**
- **High drive capability: 24mA each output**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10K, 100K I/O levels**

DESCRIPTION

The SY10H843 and SY100H843 are single supply, low skew translating 1:4 clock drivers.

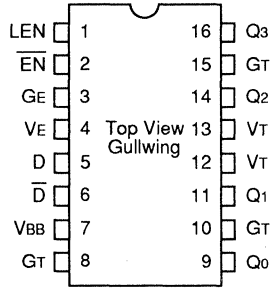
The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs), the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW after completion of the complete HIGH clock cycle. The outputs are kept HIGH by the Disable Timing Synchronizer until the HIGH input clock cycle is complete.

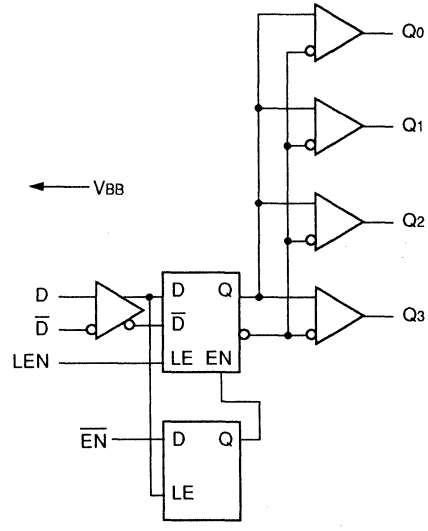
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H843 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

Pin	Function
G_T	TTL Ground (0V)
V_T	TTL Vcc (+5.0V)
V_E	ECL Vcc (+5.0V)
G_E	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output (positive ECL)
Q_0 - Q_3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)
LEN	Latch Enable Input

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ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	V
	V_{OUT} (TTL)	0.0 to V_T	
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	$\overline{EN}$	Enable Input Pos (ECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output Pos (ECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+5.0V)
13	V_T	TTL V_{CC} (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

3

DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skwd++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skwd--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF
—	Pulse Width	Q_0–Q_3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q_0–Q_3	1.0	—	1.0	—	1.0	—	ns	—
t_S	Set-up Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—
t_H	Hold Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—

NOTES:

1. Device-to-Device Skew considering the same transitions at common Vcc level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
3. Within-Device Skew considering LOW-to-LOW transitions at common Vcc level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

VCC AND CLOAD

Ranges to meet duty cycle requirement: $0°C \le T_A \le 85°C$. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \le 40MHz$	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \le 50MHz$	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	V_{OUT} = 0V

3

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

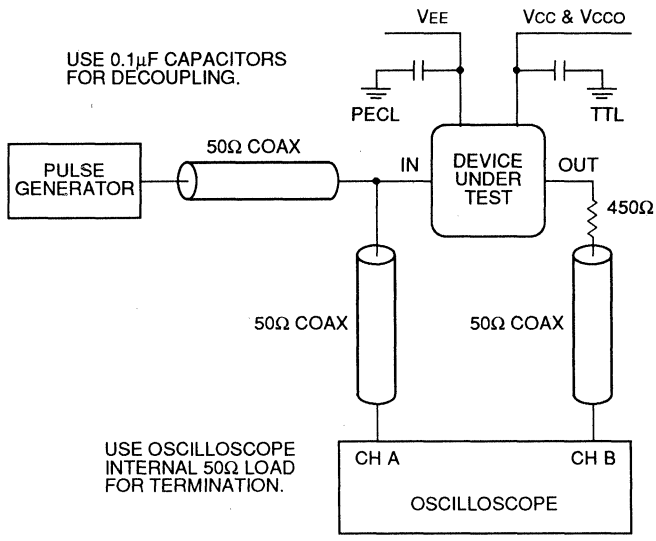
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—		
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	V_E = 5.0V
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.555		
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	V_E = 5.0V

100H ECL DC ELECTRICALCHARACTERISTICS

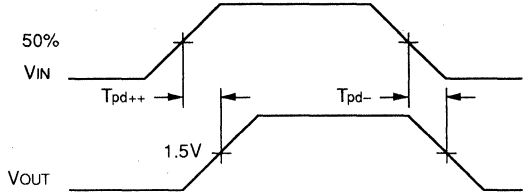
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—		
V_{IH}	Input HIGH Voltage	3.835	4.12	3.835	4.12	3.835	4.12	V	V_E = 5.0V
V_{IL}	Input LOW Voltage	3.19	3.525	3.19	3.525	3.19	3.525		
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	V_E = 5.0V

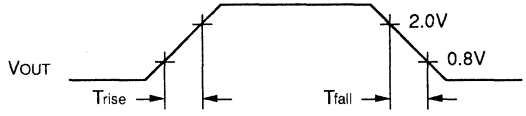
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H843ZC	Z16-1	Commercial	10KH
SY100H843ZC	Z16-1	Commercial	100K

INTRODUCTION

Clock distribution is a significant design challenge for systems operating above 25MHz. The Synergy PECL series of clock chips simplifies designs by significantly reducing clock skew — the source of most problems in high-speed clock distribution design. This application brief examines the various aspects of clock system design using a system design as an example.

Figure 1 shows an example of such a high-speed computer system with a clock subsystem. The system consists of a 32-bit CPU with a memory control subsystem, peripheral chips and a clock subsystem. The clock subsystem drives the various clock pins of the system. The clock subsystem consists of an ECL crystal oscillator, Xtal, an SY10E111 PECL clock distributor, and SY10H842 PECL-to-TTL clock drivers. The SY10E111 PECL clock distributor generates the primary clock signal and drives the SY10H842 PECL-to-TTL clock drivers.

Differential PECL signals, such as those used by the SY10E111 and SY10H842, have unique advantages for clock distribution systems. Differential PECL signals provide good noise rejection. Because they are differential and have low swing, they minimize EM radiation from the board; they can drive low impedance transmission line traces for minimum trace delay; they have equal rise and fall times which preserves the clock duty cycle; and, by exchanging the inputs to the PECL-to-TTL converter, you can get inverted clocks easily with minimum skew.

Synchronous digital systems — such as shown in Figure 1 — use the concept of a single clock coordinating the actions of all system components. In real systems, the low-to-high controlling clock edges do not happen at the same time. The difference in time between the rising edge of one clock pin and another is called clock skew. Clock skew is generated by differences in delay between the clock oscillator and the clock pins. This delay is a combination of the delay through different clock drivers and the time required for the clock to propagate down the PC board trace (or trace delay).

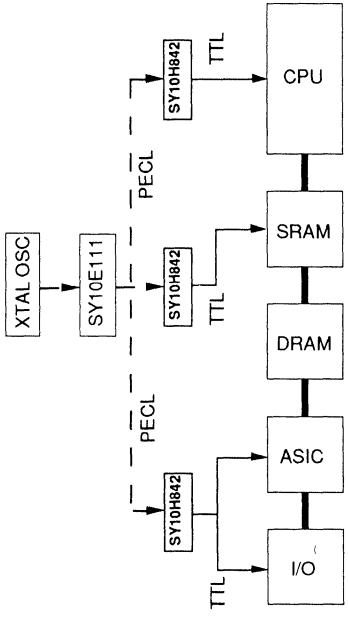


Figure 1. A 32-Bit Microprocessor System

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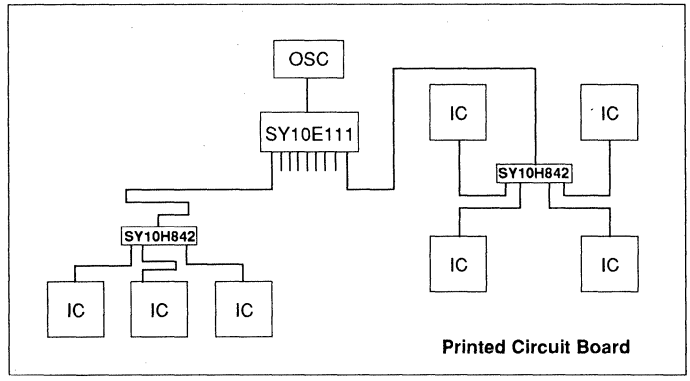


Figure 2. Clock Distribution Board Layout Example

Figure 2 shows what a board layout of the system of Figure 1 might look like. Note that the traces are run in serpentine patterns to keep the trace lengths from the SY10E111 to the SY10H842s and from the SY10H842s to their IC loads equal in length.

THE PECL CLOCK CHIPS

Figures 3 and 4 show block diagrams of the SY10E111 and SY10H842 PECL clock chips, respectively. The SY10E111 is a 1-in, 9-out PECL clock distributor chip. It multiplies the single clock input from the crystal oscillator into 9 copies for distribution to the SY10H842 chips. The SY10E111 has very low output-to-output skew (0.05ns) and low part-to-part skew (0.2ns). The SY10E111 is normally driven by the master clock source — the crystal oscillator in this case — and the SY10E111 outputs drive PECL-to-TTL clock drivers such as the SY10H842. The SY10E111 can also drive other SY10E111 chips. You can make large clock systems with low skew by using the first SY10E111 chip to drive other SY10E111 chips. A single SY10E111 generates 9 PECL clock outputs and up to 36 TTL outputs using SY10H842 PECL-to-TTL clock drivers. Two layers of SY10E111s can generate up to 81 PECL clock outputs and 324 TTL outputs. The SY10E111 is available in a 28-pin PLCC package. The PLCC package allows balanced lead lengths for low skew, and the plastic package minimizes propagation delay.

The SY10H842 is a 4-output PECL-to-TTL converter. The SY10H842 has low output-to-output skew for outputs in the same package (0.3ns) and for outputs in different packages (0.5ns). It has flow-through style pinouts for ease of layout and one TTL ground for each pair of outputs for low ground bounce noise. It is supplied in a 16-pin, low-inductance SOIC package.

Several variations of the SY10H842 are also available. The SY10H841 is a 4-output part, similar to the SY10H842, but has an input latch for holding the clock signal in a

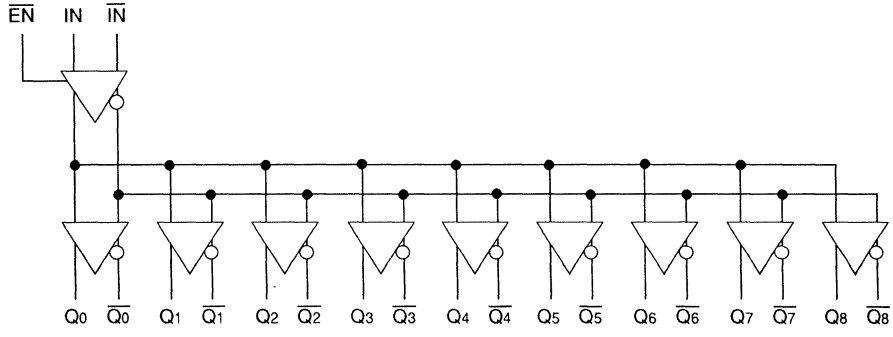


Figure 3. SY10E111 Block Diagram

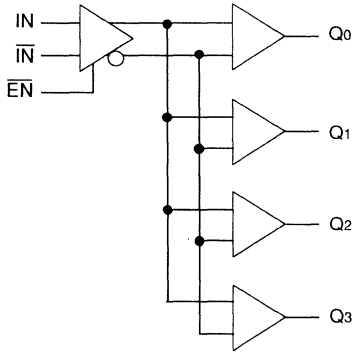


Figure 4. SY10H842 Block Diagram

The delay for the shortest and longest path for the system shown in Figure 1 are given in Table 1.

Delay Element	Skew
SY10E111 Output-to-Output Skew, Max.	0.05
Trace Delay, SY10E111-to-SY10H842, 3/4" Difference at 0.15ns/in	0.10
SY10H842 Package-to-Package Skew, Max.	0.50
Loading Delay, SY10H842, 5pF Difference at 1.5ns/50pF	0.15
Trace Delay, SY10H842-to-Load, 3/4" Difference at 0.25ns/in	0.20
Totals	1.00

Table 1. System Clock Skew Example

specified state. The SY10H843 is similar to the SY10H842 but has a pair of input latches for both the data and enable signals. It has a synchronous enable for stopping the clock without glitches or short pulse effects. The SY10H641 is a 9-output PECL-to-TTL converter in a 28-pin PLCC package. Note that all the PECL-to-TTL clock driver chips in a system design must be of the same type for the specified package-to-package skew specification to apply. All of the clock chips are available with either 10K PECL (e.g. SY10E111) or 100K PECL (e.g. SY100E111) signal level compatibility.

CALCULATING SKEW

Clock skew is defined as the difference in time between the clock edges arriving at a pair of clock input pins. In a perfect system, all clock signals arrive at all the various clock input pins of the system at exactly the same time, and the skew is zero. In real systems, the edges do not arrive at exactly the same time and there is some skew. Clock skew exists because of differences in the delay paths from the master clock oscillator to the various clock input pins. Delay accumulates along each clock path and the delays for the various paths are not equal. The maximum clock skew for the system is the difference in delay between the shortest and longest delay paths.

We can calculate the skew for a system by calculating the differences in delay along the clock paths. In the clock system of Figure 1, each delay path consists of the following elements:

- Delay through the SY10E111
- Trace delay from the SY10E111 to the SY10H842
- Delay through the SY10H842
- Output delay of the SY10H842 due to capacitive loading
- Trace delay from the SY10H842 to the clock input pin

The delay from the master clock oscillator to the SY10E111 does not contribute to clock skew because it is exactly the same for all clock paths: all clocks share this delay path element. The SY10E111 data sheet specifies the maximum skew between outputs on the same chip to be less than 0.05ns. Small clock systems such as this example use a single SY10E111 which adds only 0.05ns to the total skew. Large clock systems using one SY10E111 driving other SY10E111s have 0.05ns of skew for the first SY10E111, plus 0.20ns of package-to-package skew for each layer of SY10E111s.

Trace delay from the SY10E111 to the SY10H842 is determined by the length of the clock trace on the printed circuit board, the material of the board, and the capacitive loading of the SY10H842 input. For glass epoxy printed circuit cards, the unloaded trace delay is 0.144ns/inch. The capacitive loading of the input pins of the SY10H842 increases this delay. A figure of 0.15ns/inch is used in this example.

The skew for outputs within a single SY10H842 is 0.30ns; however, this example uses more than one chip so the chip-to-chip skew value of 0.50ns must be used.

The SY10H842 is specified with a 50pF load. Good design practice dictates that each SY10H842 TTL output drive only one load — typically between 5 and 10pF. The SY10H842 loading factor is 1.5ns per 50pF additional capacitance. If the loads on the outputs differ by 5pF, a corresponding skew of 0.15ns is introduced.

The final element of skew is trace delay from the SY10H842 to the load (i.e., the clock input pin being driven). The TTL trace is typically more heavily loaded than the PECL lines from the SY10E111 to the SY10H842. This means that the TTL trace delay per inch of trace is larger than the 0.144ns/inch of unloaded traces. A typical number is 0.25ns/inch. This number is used in the calculations, and the traces are assumed to be from 1 1/4 inch to 2 inches long from the SY10H842 to the various clock input pins.

The total clock skew for the system is the sum of the skews of the various elements. The total skew in this example is 1.00ns. Note that 0.30ns of this delay is due to trace length differences of 3/4 inch on the PECL and 3/4 inch on the TTL traces. Also, 0.15ns of skew is due to 5pF difference in loading on the various outputs. These values are affected by the system design and board layout. If these differences could be cut in half, for example, the skew could be cut by 0.23ns, reducing the total skew to 0.77ns. The rule of thumb for maximum skew is 10% of a clock cycle. Utilizing Synergy's low skew SY10E111 and SY10H842 PECL clock distribution system, this maximum skew requirement can easily reach levels to above 100MHz.

SYSTEM CLOCK SKEW REQUIREMENTS

Now that we know how to calculate clock skew, we need to know how to calculate the system clock skew requirements (i.e., the system clock skew design budget). Clock skew is the main design parameter in high-speed clock systems. System timing determines clock skew requirements. The system timing diagram of Figure 5 shows the effect of clock skew. In this diagram, we have a data source, such as the CPU, driving a receiver such as an I/O device. The CPU puts data on the bus that is received and clocked in by the I/O device. The CPU makes the data valid on the bus for a set-up time, t_{BS}, before the clock. The CPU holds it valid for a hold time, t_{BH}, after the clock. The I/O device requires that data be present at its inputs for a set-up time, t_{IS}, before the clock, and that it be held valid for a hold time, t_{IH}, after the clock. The timing design margin is the amount of excess time the data is valid before the minimum required set-up time and after the minimum required hold time. The design margin for data set-up is ($t_{BS} - t_{IS}$); for data hold, it is ($t_{BH} - t_{IH}$).

Let us consider the case where the I/O device receives an early version of the clock, called I/O Clock in Figure 5. This clock is early with respect to the CPU clock, the source of the data on the bus. The I/O device input set-up and hold window is relative to its clock. In Figure 5, I/O Clock has moved the I/O input set-up and hold window early enough in the cycle that the data on the bus is not yet valid and its input set-up requirements are violated. A similar situation occurs if the I/O device clock is late. If the I/O clock is too late, the I/O input hold requirement is violated.

Excessive clock skew violates input set-up or hold requirements for control or data signals. The problem is also relative. The clock at the receiver is early or late with respect to the clock at the driver. In the case shown, the CPU is driving an I/O device, and the I/O device clock is early with respect to the CPU clock. If the I/O device is driving the CPU on the next cycle, the CPU clock will be late with respect to the I/O device.

The difference in timing between two clock signals is called clock skew. The difference in time between the rising edges of CPU Clock and I/O Clock in Figure 5 is the clock skew, t_{SKEW}. The maximum value of skew is determined by the set-up time margin ($t_{BS} - t_{IS}$) for I/O Clock arriving early, to the hold time margin ($t_{BH} - t_{IH}$) for I/O Clock arriving late. Since clock skew is relative, all combinations of data output set-up and hold and data input set-up and hold are considered. The allowable clock skew is the minimum of these combinations of set-up and hold margins.

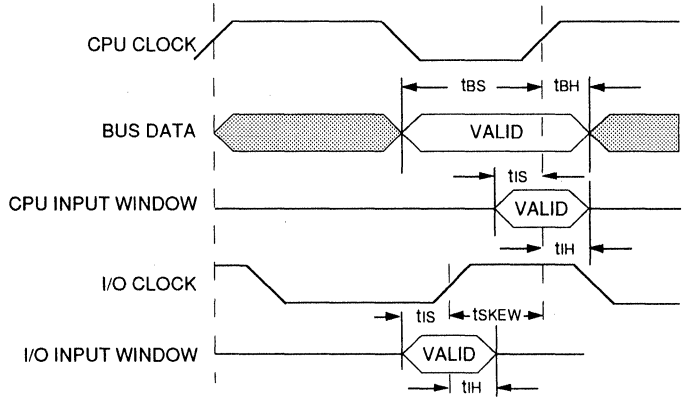


Figure 5. Clock Skew Timing Diagram

DESIGNING WITH SYNERGY PECL CLOCK DISTRIBUTION CHIPS

Designing clock distribution systems with the Synergy PECL series of clock chips is straightforward, as shown above. The simplicity of system design is a result of several advantages of the PECL/TTL clock distribution system approach. The elements of clock skew in the PECL/TTL approach are typically much lower and more predictable than in TTL-only designs.

The delay through a PECL chip is typically 1/5 to 1/10 the corresponding delay through a TTL chip. The SY10E111 PECL clock distributor shown in Figure 3 has a propagation delay of 0.63ns compared to the TTL 74FCT244D at 3.8ns. Lower propagation delay also means lower skew. The PECL SY10E111 has very low on-chip skew (0.05ns) and relatively low chip-to-chip skew (0.20ns) as compared to TTL buffer chips which have typical skews of 1.0ns and 2.5ns, respectively. The speed of PECL technology also applies to the SY10H842 PECL/TTL clock driver. It has a maximum propagation delay of 3.5ns, a maximum output-to-output skew of 0.3ns, and a maximum part-to-part skew of only 0.5ns.

Differential PECL signals minimize the propagation delay per inch of trace between the SY10E111 clock distributor and the SY10H842 PECL/TTL clock drivers. The delay per inch of trace on a PC board is 0.144ns/inch for G-10 glass epoxy boards with a dielectric constant of 4.7. This represents the minimum propagation delay per inch of trace. Adding capacitance to the trace increases this delay per inch value. Reducing the transmission line impedance of the traces reduces the effect of this capacitance. PECL chips such as the SY10E111 are designed to drive low impedance, 50 ohm transmission lines. This low impedance minimizes the effect of the SY10H842 PECL input capacitance at the receiving end of the trace, which keeps the propagation delay per inch of the transmission line low. This combination allows the SY10E111 and SY10H842 combination to achieve a 0.15ns/inch delay.

Differential PECL signals also provide high noise immunity compared to single-ended TTL signals. Crosstalk, ground and power noises tend to affect both PECL signals in the same way. The result is common mode noise on the signal pair. This common mode noise is rejected by the differential PECL input. The result is a clean signal as seen by the PECL inputs. This means no clock jitter due to noise, preservation of clock duty cycle, and no problem with Vcc variations from one part of the board to another. PECL signals for clock distribution also mean low EM radiation because of the lower voltage swing and the fact that voltages and currents of differential PECL transmission lines cancel each other for minimum radiation.

Differential PECL signals provide a third, unique capability: low skew inverted clocks. By simply exchanging the PECL signals to a selected PECL-to-TTL clock driver, the output clock signals output from that driver are inverted with respect to other clocks in the system.

With these advantages in mind, the following is a set of PECL/TTL clock system design recommendations:

- Use the PECL SY10E111-to-SY10H842 lines for clock routing for minimum delay and noise.
- Use 50 ohm stripline (internal) traces for the PECL lines. This gives 50 ohm lines in small size.
- Make the PECL traces equal length for minimum skew. Each inch difference is 0.15ns of skew.
- Put the PECL/TTL converters near their loads: keep the TTL traces short for low noise and delay.
- Use one TTL driver per load and keep the loads as equal as possible for minimum skew and noise.

3

PECL CLOCK DISTRIBUTION LINE TERMINATION

The PECL lines from the SY10E111 to the SY10H842s are transmission lines for traces longer than one inch. These traces must be terminated at the SY10H842 end in the characteristic impedance of the transmission line; otherwise, there will be signal reflection and noise which can distort the clock signal. The SY10E111 is designed to drive 50 ohm transmission lines. You can design printed circuit traces to be 50 ohm transmission lines by properly sizing the width of the trace (see Appendix 1). There remains the requirement of terminating each of the pair of lines in its 50 ohm impedance.

You can terminate the differential PECL signals with 50 ohm resistors to a terminating voltage of 3 volts (i.e., 2.0 volts below Vcc). This requires a separate terminating voltage power supply. A simpler method is to use an RC network, as shown in Figure 6. The RC network of Figure 6 takes advantage of the fact that the signals are differential and always opposite in phase. The two termination resistors, Rt, are connected to a common bias resistor, Rb. The bias resistor provides the current that would normally be supplied by a 3.0 volt terminating voltage power supply.

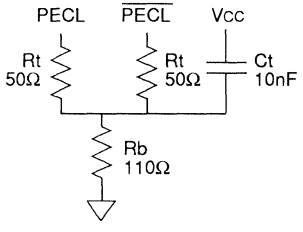


Figure 6. PECL Resistor Termination

The correct size for the Rb bias resistor is 107 ohms; a 110 ohm resistor will work. The decoupling capacitor, Ct, keeps the terminating voltage constant while the signals are switching so that each line sees a 50 ohm terminating

impedance. The RC time constant of Ct and the terminating resistors would be 10 times the round trip delay of the longest transmission line. If this is 5ns, the RC time constant should be larger than 50ns and Ct should be larger than (50ns/25 ohms) = 2nF = 200pF. A value for Ct of 10,000pF (0.01μF) will work nicely. Note that Ct is connected to Vcc. This is because PECL signals are generated relative to Vcc. The Vcc plane for TTL is the "ground" plane for PECL.

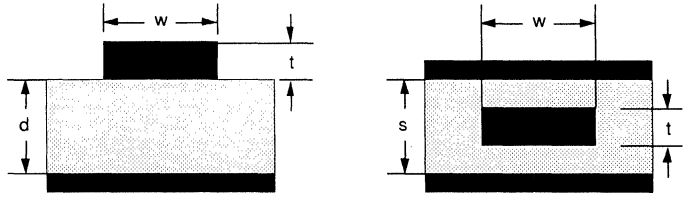
APPENDIX 1

PRINTED CIRCUIT TRACE CHARACTERISTICS

The geometry of printed circuit traces and the dielectric constant of the printed circuit board material holding them determine their transmission line characteristics. Figure A1 shows the two major trace types used on PC boards: the Surface Micro Stripline, and the Internal Stripline. Table A1 gives the equations for calculating their characteristics and some example values. You can use these equations in a spreadsheet to calculate the propagation delays on your circuit board, and you can use the example values to debug the spreadsheet.

Adding load capacitance to a trace increases its effective distributed capacitance. This decreases its impedance and increases the delay per inch. The equations in Table A1 give the effective termination impedance and trace delay for single traces with capacitive loading.

Table A1 gives the unloaded characteristic impedance, propagation delay per inch, capacitance per inch and inductance per inch for various combinations of trace width and board thickness for both Surface Micro Stripline and Internal Stripline traces. Surface traces are on the board surface over a ground plane. The board thickness (d) is the thickness between the trace and the ground plane. A 0.012" thickness corresponds to the surface trace of a typical 6-layer board. Internal traces are between ground planes. The board thickness(s) is the distance between the two ground planes and assumes that the trace is centered between them. The 0.026" thickness is for an internal trace on a 6-layer board where the 0.026" is the distance from a center ground plan to the surface layer of the board. This 0.026" thickness corresponds to 2 times layer spacing (d, as in Micro Stripline), and trace thickness (t).



SURFACE MICRO STRIPLINE INTERNAL STRIPLINE

Figure A1. Printed Circuit Trace Geometries

Surface Micro Stripline

Parameter	Symbol	Unit	Equation	Example
Dielectric Constant	Er	—	—	4.7
Board Thickness	d	inch	—	0.012
Trace Width	w	inch	—	0.010
Trace Thickness	t	inch	—	0.002
Impedance	Z0	ohms	$\frac{87}{\sqrt{Er+1.41}} \ln \frac{5.98\,d}{8\,w+t}$	69.36
Delay/Inch	tPDZ	ns/in	$0.08475\sqrt{0.475\,Er+0.67}$	0.144
Capacitance/Inch	Cz	pF/in	$1000\frac{tPDZ}{Z0}$	2.08
Inductance/Inch	Lz	nH/in	$tPDZZ0$	10.015
Capacitive Load	Cload	pF	—	37
Z with Cap Load	Z	ohms	$Z0\sqrt{\frac{Cz}{Cz+Cload}}$	41.08
tPD/in with Cap Load	tPD	ns/in	$tPDZ\sqrt{\frac{Cz+Cload}{Cz}}$	0.244

Internal Stripline

Parameter	Symbol	Unit	Equation	Example
Dielectric Constant	Er	—	—	4.7
Board Thickness	s	inch	—	0.026
Trace Width	w	inch	—	0.010
Trace Thickness	t	inch	—	0.002
Impedance	Z0	ohms	$\frac{60}{\sqrt{Er}} \ln \frac{4d}{0.536\pi w+0.67\pi t}$	44.21
Delay/Inch	tPDZ	ns/in	$0.08475\sqrt{0.475\,Er+0.67}$	0.144
Capacitance/Inch	Cz	pF/in	$1000\frac{tPDZ}{Z0}$	3.27
Inductance/Inch	Lz	nH/in	$tPDZZ0$	6.38
Capacitive Load	Cload	pF	—	37
Z with Cap Load	Z	ohms	$Z0\sqrt{\frac{Cz}{Cz+Cload}}$	29.94
tPD/in with Cap Load	tPD	ns/in	$tPDZ\sqrt{\frac{Cz+Cload}{Cz}}$	0.213

Table A1. Transmission Line Characteristics for Various Traces

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8 to 0	V_{dc}
V_I	Input Voltage (V_{CC} = 0V)	0 to –6V	V_{dc}
I_{OUT}	Output Current Continuous Surge	 50 100	mA
T_A	Operating Temperature Range 10E 100E	 0 to +75 0 to +85	°C
T_{STORE}	Storage Temperature	–65 to +150	°C

NOTE:

1. Beyond which device life may be impaired unless specified otherwise on individual data sheet.

4

10E SERIES DC CHARACTERISTICS (10KH)

V_{EE} = -5.2V ± 5%; V_{CC} = V_{CCO} = GND; T_A = 0°C to +75°C[1]

		T_A = 0°C		T_A = +25°C		T_A = +75°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1020	–840	–980	–810	–920	–735	–910	–720	mV
V_{OL}	Output LOW Voltage	–950	–1630	–1950	–1630	–1950	–1600	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1070	–735	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.3	—	0.3	—	µA

NOTE:

1. 10E series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts, except bus outputs which, where specified, are terminated into 25Ω.

100E SERIES DC CHARACTERISTICS (100K)

V_{EE} = -4.2V to -5.46V; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–995	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL} (Min.)	50Ω to –2.0V
V_{OHA}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	
V_{OLA}	Output LOW Voltage	—	—	–1610	mV	or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5	—	—	mA	V_{IN} = V_{IL} (Min.)	

NOTE:

1. This table replaces the three tables at different supply voltages in ECL 100K literature. The same DC parametric values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2 to –5.46.

Rev.: B Amendment:/0
Issue Date: February, 1994

8-BIT SYNCHRONOUS BINARY UP COUNTER

FEATURES

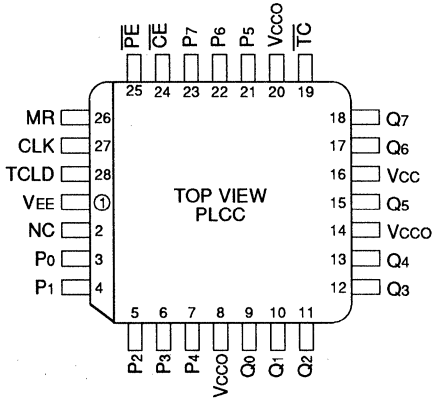
- **700MHz min. count frequency**
- **1000ps CLK to Q, $\overline{TC}$**
- **Internal, gated $\overline{TC}$ feedback**
- **8 bits wide**
- **Fully synchronous counting and $\overline{TC}$ generation**
- **Asynchronous Master Reset**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E016**

DESCRIPTION

The SY10E016 and SY100E016 are high-speed synchronous, presettable and cascadable 8-bit binary counters designed for use in new, high-performance ECL systems. Architecture and operation are the same as the Motorola MC10H016 in the MECL 10KH family, extended to 8 bits, as shown in the logic diagram.

The counters feature internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW, the $\overline{TC}$ feedback is disabled and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-HIGH state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter.

PIN CONFIGURATION

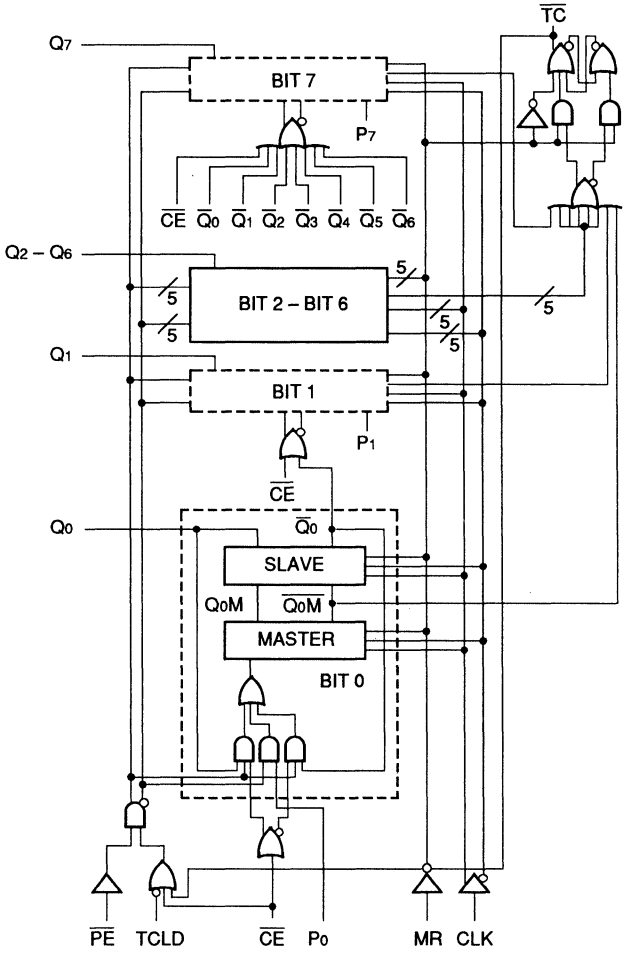


PIN NAMES

Pin	Function
P_0-P_7	Parallel Data (Preset) Inputs
Q_0-Q_7	Data outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC-Load Control Input

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	Function
X	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Master respond, Slaves Hold
X	X	X	H	Z	Reset (Q_n : = LOW, $\overline{TC}$: = HIGH)

NOTE:
1. Z = Clock Pulse (LOW-to-HIGH), ZZ = Clock Pulse (HIGH-to-LOW)

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	151	181	—	151	181	—	151	181		
	100E	—	151	181	—	151	181	—	174	208		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = 25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Ty+p.	Max.	Min.	Typ.	Max.	Unit	Condition
f_{COUNT}	Max. Count Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	CLK to Q	600	725	1000	600	725	1000	600	725	1000		—
	MR to Q	600	775	1000	600	775	1000	600	775	1000		—
	CLK to TC (Qs loaded)	550	775	1050	550	775	1050	550	775	1050		1
	CLK to TC (Qs unloaded)	550	700	900	550	700	900	550	700	900		1
	MR to TC	625	775	1000	625	775	1000	625	775	1000		—
t_s	Set-up Time										ps	—
	Pn	150	–30	—	150	–30	—	150	–30	—		
	$\overline{CE}$	600	400	—	600	400	—	600	400	—		
	$\overline{PE}$	600	400	—	600	400	—	600	400	—		
	TCLD	500	300	—	500	300	—	500	300	—		
t_h	Hold Time										ps	—
	Pn	250	30	—	250	30	—	250	30	—		
	$\overline{CE}$	0	–400	—	0	–400	—	0	–400	—		
	$\overline{PE}$	0	–400	—	0	–400	—	0	–400	—		
	TCLD	100	–300	—	100	–300	—	100	–300	—		
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	
t_{WP}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_r	Rise/Fall Times	300	510	800	300	510	800	300	510	800	ps	—
t_f	20% to 80%											

NOTE:
1. CLK to $\overline{TC}$ propagation delay is dependent on the loading of the Q outputs. With all of the Q outputs loaded, the noise generated in going from a IIII IIII state to a 0000 0000 state causes the CLk to $\overline{TC}$+ delay to increase.

FUNCTION TABLE

Function	$\overline{PE}$	$\overline{CE}$	MR	TCLD	CLK	P_7–P_4	P_3	P_2	P_1	P_0	Q_7–Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E016JC	J28-1	Commercial
SY100E016JC	J28-1	Commercial

APPLICATIONS INFORMATION

Cascading Multiple E016 Devices

For applications which call for larger than 8-bit counters, multiple E016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of E016 devices. Two E016s can be cascaded without the need for external gating; however, for counters wider than 16 bits, external OR gates are necessary for cascade implementations.

Figure 1, below, pictorially illustrates the cascading of 4 E016s to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state), the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit, thus sending their terminal count outputs back to a high state, disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an E016 in the chain to count all of the lower order terminal count outputs, it must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary set-up time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ set-up time). Figure 1 shows E101 gates used to control the count enable inputs; however, if the frequency of operation is lower, a slower ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is 475MHz and that for a 16-bit counter is 625MHz. Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case, estimates of these delays need to be added to the calculations.

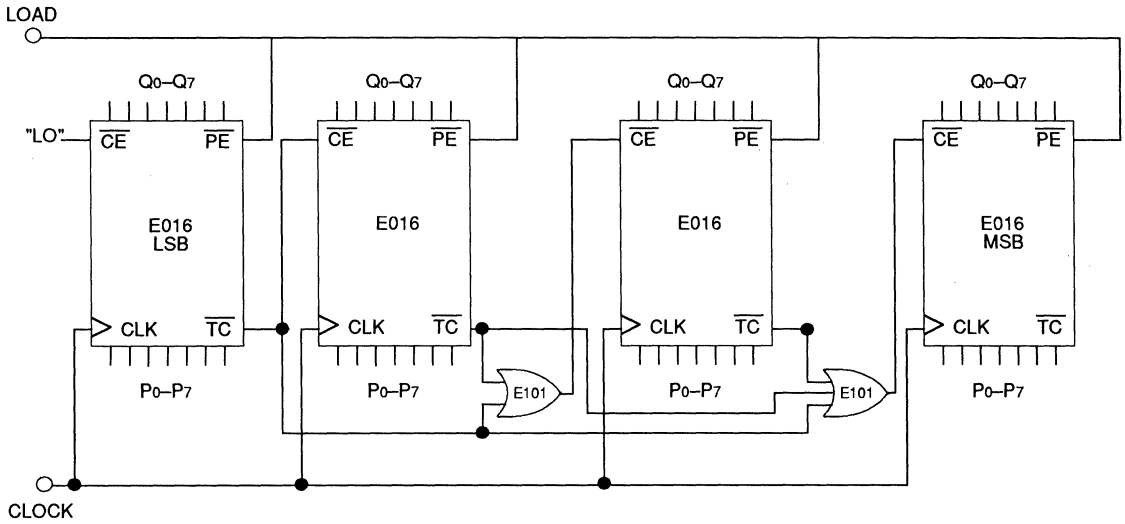


Figure 1. 32-Bit Cascaded E016 Counter

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count), when asserted, reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 2 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio for the binary value for 256. As an example for a divide ration of 113:

$PN's = 256 - 113 = 8F_{16} = 1000\ 1111$

where

P_0 = LSB and P_7 = MSB

Forcing this input condition, as per the set-up in Figure 2, will result in the waveforms of Figure 3. Note that the $\overline{TC}$ output

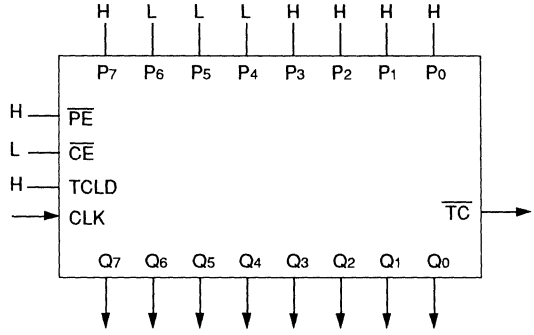


Figure 2. Mod 2 to 256 Programmable Divider

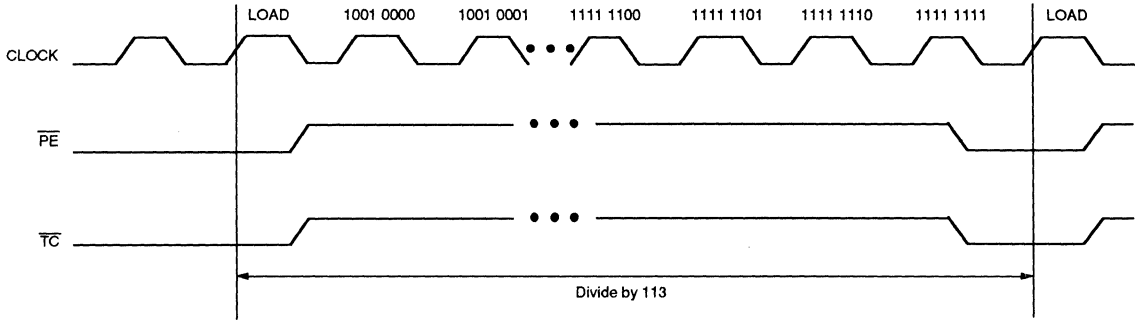


Figure 3. Divide by 113 E016 Programmable Divider Waveforms

Divide Ratio	Preset Data Inputs							
	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

Table 1. Preset Values for Various Divide Ratios

is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios twice the desired divide ratio can be loaded into the E016 and the $\overline{TC}$ output can feed the clock input of a toggle flip-flop to create a signal divided as desired with a 50% duty cycle.

A single E016 can be used to divide by any ratio from 2 to 256, inclusive. If divide ratios of greater than 256 are needed, multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers, the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple E016 divider chains.

Figure 4 on the following page shows a typical block diagram of a 32-bit divider chain. Once again, the maximize the frequency of operation, E101 OR gates were used. For lower frequency applications, a slower OR gate could replace the E101. Note that for a 16-bit divider, the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant E016 must also feed the $\overline{CE}$ input of the most significant E016. If the two $\overline{TC}$ outputs were OR tied, the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Maximizing E016 Count Frequency

The E016 device produces nine fast transitioning single-ended outputs; thus, V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that, if the outputs are not going to be used in the rest of the system, they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system, only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated, but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs, or provide them with an extra margin to the published data book specifications.

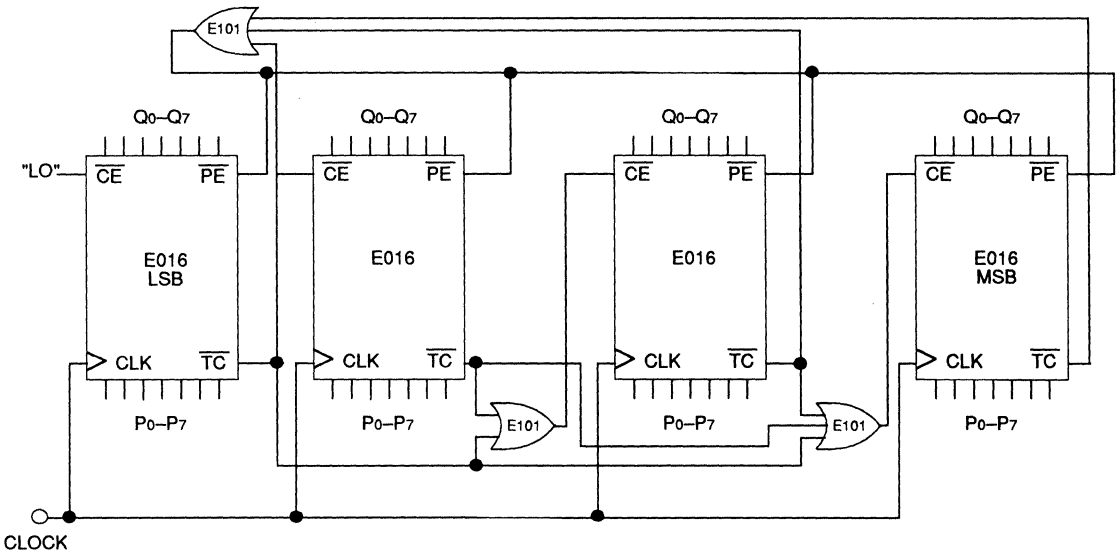


Figure 4. 32-Bit Cascaded E016 Programmable Divider

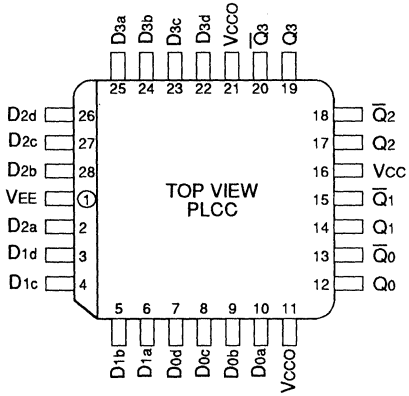
FEATURES

- **500ps max. propagation delay**
- **True and complementary outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E101**

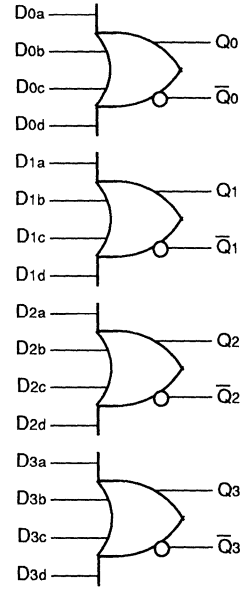
DESCRIPTION

The SY10E101 and SY100E101 are quad 4-input OR/NOR gates designed for use in new, high-performance ECL systems. The E101 features both true and complementary outputs.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
Dna, Dnb, Dnc, Dnd	Data Inputs
Q0-Q3	True Outputs
Q̄0-Q̄3	Inverting Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

LOGIC EQUATION

Qn = Dna + Dnb + Dnc + Dnd

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
IEE	Power Supply Current										mA	—
	10E	—	30	36	—	30	36	—	30	36		
	100E	—	30	36	—	30	36	—	35	42		

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AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay to Output D to Q	200	350	500	200	350	500	200	350	500	ps	—
tSKEW	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
	Within-Gate Skew	—	25	—	—	25	—	—	25	—	ps	2
tr tf	Rise/Fall Time 20% to 80%	300	380	575	300	380	575	300	380	575	ps	—

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagations delays through a single gate when driven from its different inputs.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E101JC	J28-1	Commercial
SY100E101JC	J28-1	Commercial

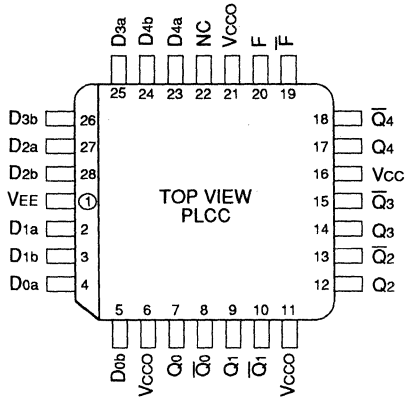
FEATURES

- **600ps max. propagation delay**
- **True and complementary outputs**
- **OR/NOR function outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E104**

DESCRIPTION

The SY10E104 and SY100E104 are quint 2-input AND/NAND gates designed for use in new, high-performance ECL systems. The E104 also features a function output, F, which is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. Both true and complementary outputs are provided.

PIN CONFIGURATION



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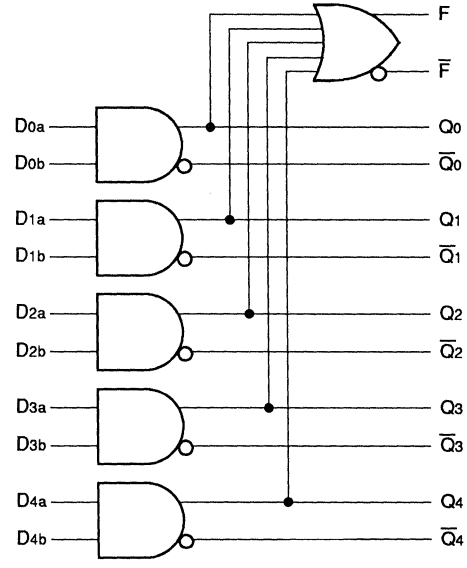

PIN NAMES

Pin	Function
Dna, Dnb	Data Inputs
Q0-Q4	AND Outputs
$\overline{Q}_0$-$\overline{Q}_4$	NAND Outputs
F	OR Output
$\overline{F}$	NOR Output

Rev.: B Amendment: /0
Issue Date: February, 1994

LOGIC EQUATION

$F = (D0a \cdot D0b) + (D1a \cdot D1b) + (D2a \cdot D2b) + (D3a \cdot D3b) + (D4a \cdot D4b)$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
I_{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	38	46	—	38	46	—	38	46		
	100E	—	38	46	—	38	46	—	44	53		

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AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to Q	225	385	600	225	385	600	225	385	600		
	D to F	500	725	1000	500	725	1000	500	725	1000		
t_{SKEW}	Within-Device Skew, D to Q	—	75	—	—	75	—	—	75	—	ps	1
t_r	Rise/Fall Time										ps	—
t_f	20% to 80%											
	Q	275	425	700	275	425	700	275	425	700		
	F	300	475	700	300	475	700	300	475	700		

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E104JC	J28-1	Commercial
SY100E104JC	J28-1	Commercial

FEATURES

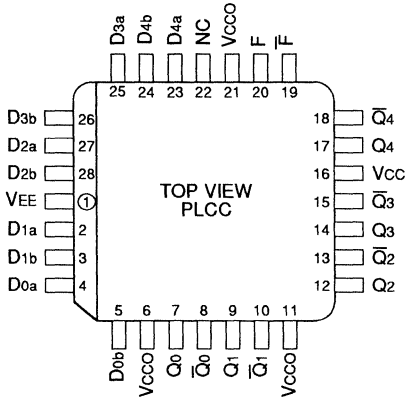
- **600ps max. propagation delay**
- **True and complementary outputs**
- **OR/NOR function outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E107**

DESCRIPTION

The SY10E107 and SY100E107 offer five 2-input XOR/XNOR gates and are designed for use in new, high-performance ECL systems.

The E107 also features a function output, F, which is the OR of all five XOR gate outputs, while $\overline{F}$ is the NOR. Both true and complementary outputs are provided.

PIN CONFIGURATION



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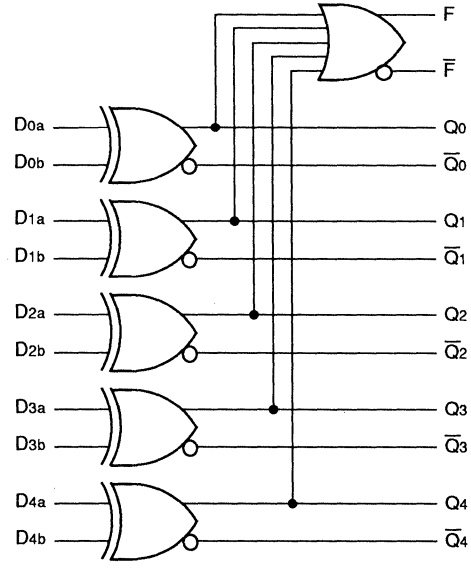

PIN NAMES

Pin	Function
Dna, Dnb	Data Inputs
Q0-Q4	XOR Outputs
$\overline{Q0}$-$\overline{Q4}$	XNOR Outputs
F	OR Output
$\overline{F}$	NOR Output

Rev.: B Amendment: /0
Issue Date: February, 1994

LOGIC EQUATION

$F = (D0a \oplus D0b) + (D1a \oplus D1b) + (D2a \oplus D2b) + (D3a \oplus D3b) + (D4a \oplus D4b)$
$F = Q0 + Q1 + Q2 + Q3 + Q4$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.,) to V_{EE} (Max); $V_{CC} = V_{CCO} = GND$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$				
Symbol	Parameter	Min.	Typ.	Max.	Mlin.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	42	50	—	42	50	—	42	50		
	100E	—	42	50	—	42	50	—	48	58		

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AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

		$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to Q	250	410	600	250	410	600	250	410	600		
	D to F	500	725	1000	500	725	1000	500	725	1000		
t_{SKEW}	Within-Device Skew, D to Q	—	75	—	—	75	—	—	75	—	ps	1
t_r	Rise/Fall Time										ps	—
t_f	20% to 80%											
	Q	275	450	700	275	450	700	275	450	700		
	F	300	475	700	300	475	700	300	475	700		

NOTE:
1. Within-device skew is defined as identical transitions on similar paths through a device.

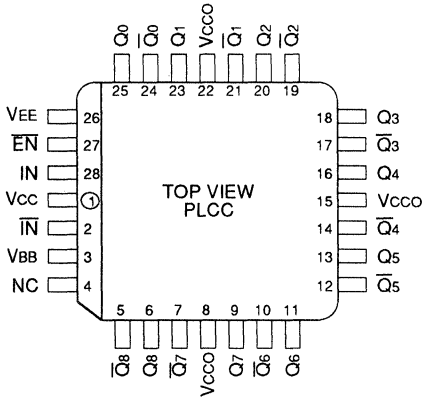
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E107JC	J28-1	Commercial
SY100E107JC	J28-1	Commercial

FEATURES

- Low skew
- Guaranteed skew limits
- Differential design
- VBB output
- Enable input
- ESD protection of 2000V
- Fully compatible with industry standard 10KH, 100K I/O levels
- Extended 100E VEE range of –4.2V to –5.46V
- 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E111

PIN CONFIGURATION



PIN NAMES

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
$\overline{EN}$	Enable Input
Q0, $\overline{Q0}$ — Q8, $\overline{Q8}$	Differential Outputs
VBB	VBB Output

DESCRIPTION

The SY10E111 and SY100E111 are low skew 1-to-9 differential drivers designed for clock distribution in new, high-performance ECL systems. They accept one differential or single-ended input, with VBB used for single-ended operation. The signal is fanned out to nine identical differential outputs. An enable input is also provided such that a logic HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E111 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

The VBB output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01μF capacitor.

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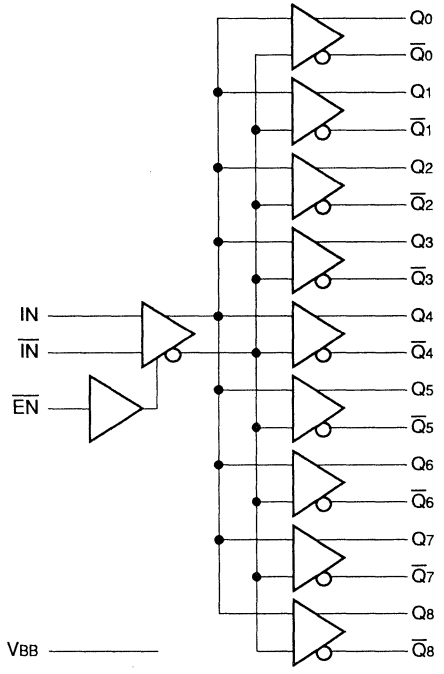
Issue Date: February, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19		
	100E	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	48	60	—	48	60	—	48	60		
	100E	—	48	60	—	48	60	—	55	69		

TIMING DIAGRAMS

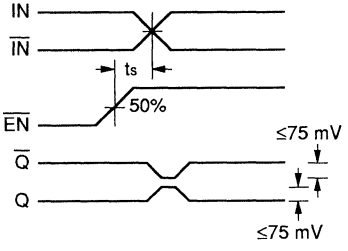


Figure 1. Set-up Time

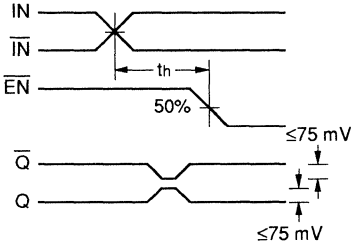


Figure 2. Hold Time

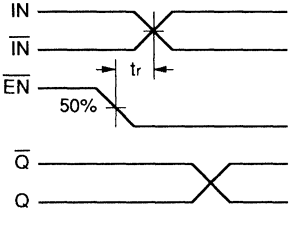


Figure 3. Release Time

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition[1-9]
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	IN (differential)	430	—	630	430	—	630	430	—	630		1
	IN (single-ended)	330	—	730	330	—	730	330	—	730		2
	Enable	450	—	850	450	—	850	450	—	850		3
	Disable	450	—	850	450	—	850	450	—	850		3
t_{SKEW}	Within-Device Skew	—	25	50	—	25	50	—	25	50	ps	4
t_S	Set-up Time, $\overline{EN}$ to IN	200	0	—	200	0	—	200	0	—	ps	5
t_H	Hold Time, IN to $\overline{EN}$	0	–200	—	0	–200	—	0	–200	—	ps	6
t_R	Release Time, $\overline{EN}$ to IN	300	100	—	300	100	—	300	100	—	ps	7
V_{PP}	Minimum Input Swing	250	—	—	250	—	—	250	—	—	mV	8
V_{CMR}	Common Mode Range	-1.6	—	-0.4	-1.6	—	-0.4	-1.6	—	-0.4	V	9
t_r t_f	Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps	—

NOTES:

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on $\overline{EN}$ to the 50% point of a **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from the 50% point of a **positive** transition on $\overline{EN}$ to the 50% point of a **negative** transition on Q (or a positive transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be de-asserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the E111, as a differential input as low as 50mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E111JC	J28-1	Commercial
SY100E111JC	J28-1	Commercial

FEATURES

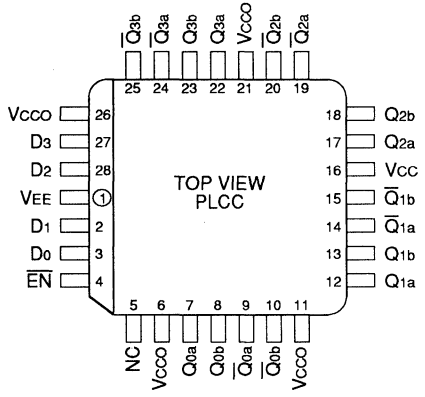
- **600ps max. propagation delay**
- **Common enable input**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E112**

DESCRIPTION

The SY10E112 and SY100E112 are quad drivers designed for use in new, high-performance ECL systems. The E112 has two pairs of OR/NOR outputs from each gate and a common, buffered enable input. The data input can also be used as an ECL memory address fan-out driver, although the E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the SY10/100E212 device.

4

PIN CONFIGURATION



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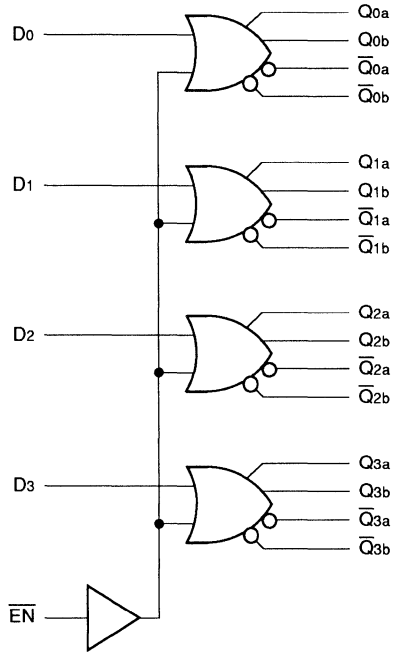

PIN NAMES

Pin	Function
D0-D3	Data Inputs
$\overline{EN}$	Enable Input
Qna, Qnb	True Outputs
$\overline{Q}$na, $\overline{Q}$nb	Inverting Outputs

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TRUTH TABLE

$\overline{EN}$	Q_n	$\overline{Q}_n$
L	D_n	$\overline{D}_n$
H	H	L

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	$\overline{EN}$	—	—	150	—	—	150	—	—	150		
	D	—	—	200	—	—	200	—	—	200		
I_{EE}	Power Supply Current										mA	—
	10E	—	47	56	—	47	56	—	47	56		
	100E	—	47	56	—	47	56	—	54	65		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	200	400	600	200	400	600	200	400	600		
	$\overline{EN}$	275	450	675	275	450	675	275	450	675		
t_{SKEW}	Within-Device Skew										ps	
	D_n to Q_n, $\overline{Q}_n$	—	80	—	—	80	—	—	80	—		1
	Q_{na} to Q_{nb}	—	40	—	—	40	—	—	40	—		2
t_r	Rise/Fall Time	275	425	700	275	425	700	275	425	700	ps	—
t_f	20% to 80%											

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E112JC	J28-1	Commercial
SY100E112JC	J28-1	Commercial

QUINT DIFFERENTIAL LINE RECEIVER

FEATURES

- **450ps max. Propagation Delay**
- **V_{BB} output for single-ended reception**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E116**

DESCRIPTION

The SY10E116 and SY100E116 are quint differential line receivers designed for use in new, high-performance ECL systems. These devices have emitter-follower outputs and an internally generated reference supply (V_{BB}) for single-ended reception.

Active current sources combined with Synergy's ASSET™ technology provide the receivers with excellent common mode noise rejection.

The receiver design features clamp circuitry to cause a defined output state if both the inverting and non-inverting inputs are left open; in this case the Q output goes LOW, while the $\overline{Q}$ output goes HIGH.

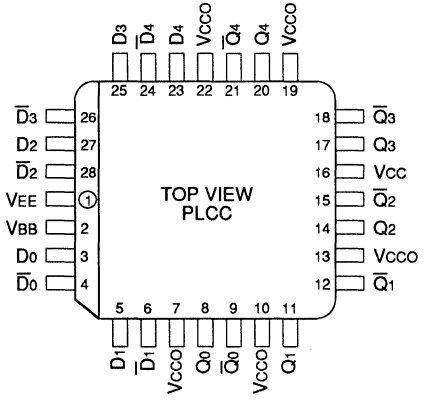
If both inverting and non-inverting inputs are at equal potential, the receiver does *not* go to a defined state, but rather shares current in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using V_{BB} for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 µF capacitor.

For higher bandwidth, please refer to the SY10/100E416 device.

4

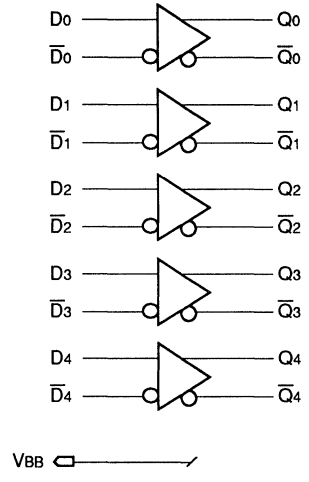
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0, $\overline{D}_0$-D_4, $\overline{D}_4$	Differential Input Pairs
Q_0, $\overline{Q}_0$-Q_4, $\overline{Q}_4$	Differential Output Pairs
V_{BB}	Reference Voltage Output

BLOCK DIAGRAM



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LOGIC EQUATION

$Q_n = D_n$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19		
	100E	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26		
I_{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	29	35	—	29	35	—	29	35		
	100E	—	29	35	—	29	35	—	33	40		
$V_{PP(DC)}$	Input Sensitivity	150	—	—	150	—	—	150	—	—	mV	1
V_{CMR}	Common Mode Range	−2.0	—	−0.6	−2.0	—	−0.6	−2.0	—	−0.6	V	2

NOTES:

1. V_{PP} is the minimum differential input voltage required to assure full ECL levels are present at the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	D	200	300	450	200	300	450	200	300	450		
	D (SE)	150	300	500	150	300	500	150	300	500		
$V_{PP(DC)}$	Input Sensitivity	150	—	—	150	—	—	150	—	—	mV	1
t_{SKEW}	Within-Device Skew Dn to Qn, $\overline{Q}$n	—	50	—	—	50	—	—	50	—	ps	2
t_{SKEW}	Duty Cycle Skew $t_{PLH} - t_{PHL}$	—	±10	—	—	±10	—	—	±10	—	ps	3
t_r t_f	Rise/Fall Time 20% to 80%	275	375	575	275	375	575	275	375	575	ps	—

NOTES:

1. Minimum input swing for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E116JC	J28-1	Commercial
SY100E116JC	J28-1	Commercial

FEATURES

- **500ps max. propagation delay**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K I/O levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E122**

DESCRIPTION

The SY10E122 and SY100E122 are 9-bit buffers designed for use in new, high-performance ECL systems. The E122 provides nine non-inverting buffers.

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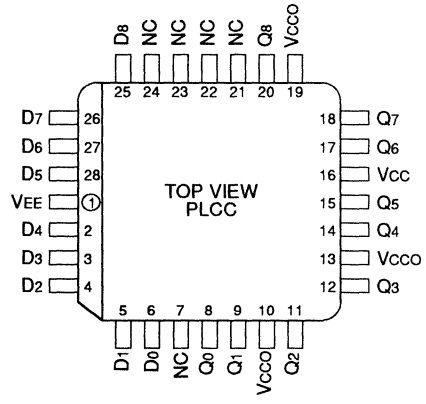
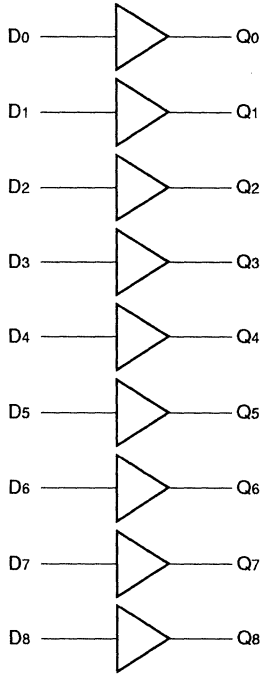
PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0-D8	Data Inputs
Q0-Q8	Data Outputs

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DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	41	49	—	41	49	—	41	49		
	100E	—	41	49	—	41	49	—	47	57		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	150	350	500	150	350	500	150	350	500	ps	—
t_{SKEW}	Within-Device Skew, D to Q	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	425	800	300	425	800	300	425	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E122JC	J28-1	Commercial
SY100E122JC	J28-1	Commercial

FEATURES

- **1100MHz min. toggle frequency**
- **Differential output**
- **Individual and common clocks**
- **Individual asynchronous reset**
- **Paired asynchronous sets**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E131**

DESCRIPTION

The SY10E131 and SY100E131 are high-speed quad master slave D-type flip-flops with differential outputs designed for use in new, high-performance ECL systems. The flip-flops may be individually clocked by holding Cc (Common Clock) at a logic LOW and then using the four individual $\overline{CE}$ (Clock Enable $\overline{CE}_0$–$\overline{CE}_3$) inputs to accomplish such clocking. Alternatively, all four flip-flops can be clocked in common by holding the $\overline{CE}$ inputs LOW and then using Cc to clock the data. In the common clock mode, the $\overline{CE}$ input acts as a control that passes the Cc signal to the flip-flop. Data is clocked into the flip-flop on the rising edge of the output of the logical OR operation between $\overline{CE}$ and Cc (data enters the master when both Cc and $\overline{CE}$ are LOW and data transfers to the slave when either $\overline{CE}$ or Cc, or both, go HIGH).

Asynchronous set and reset controls are provided. The reset controls are individual and the set controls are pairwise.

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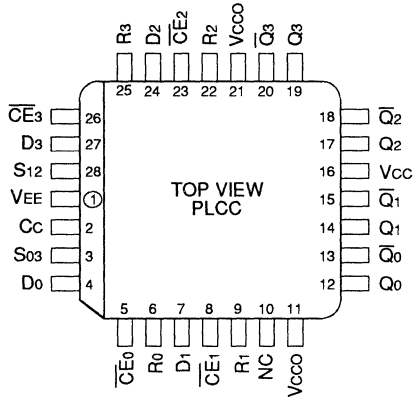
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0-D_3	Data Inputs
$\overline{CE}_0$-$\overline{CE}_3$	Clock Enables (Individual)
R_0-R_3	Resets
Cc	Common Clock
S_{03}, S_{12}	Sets (paired)
Q_0-Q_3	True Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Inverting Outputs

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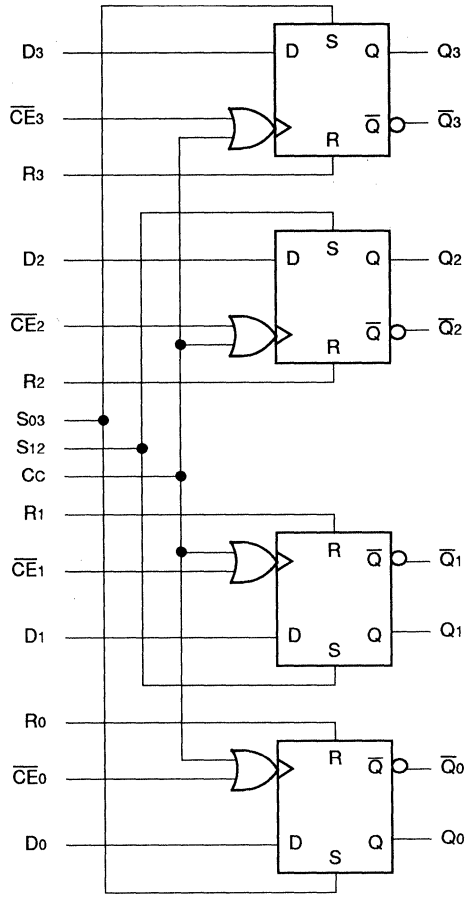
BLOCK DIAGRAM



TRUTH TABLE

Pin	State	Mode
Cc	L	Individual clocking with $\overline{CE}_n$
$\overline{CE}$	L	Common clocking with Cc

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Ty+p.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	Cc	—	—	350	—	—	350	—	—	350		
	S	—	—	450	—	—	450	—	—	450		
	R	—	—	300	—	—	300	—	—	300		
	$\overline{CE}$	—	—	300	—	—	300	—	—	300		
	D	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	58	70	—	58	70	—	58	70		
	100E	—	58	70	—	58	70	—	67	81		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	$\overline{CE}$	360	500	700	360	500	700	360	500	700		
	Cc	325	500	675	325	500	675	325	500	675		
	R	350	550	725	350	550	725	350	550	725		
	S	350	550	725	350	550	725	350	550	725		
t_s	Set-up Time, D	150	20	—	150	20	—	150	20	—	ps	2
t_h	Hold Time, D	175	–20	—	175	–20	—	150	–20	—	ps	2
t_{RR}	Reset Recovery Time	400	150	—	400	150	—	400	150	—	ps	—
t_{PW}	Minimum Pulse Width Clk, S, R	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	480	675	300	480	675	300	480	675	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Set-up/hold times guaranteed for both Cc and $\overline{CE}$.

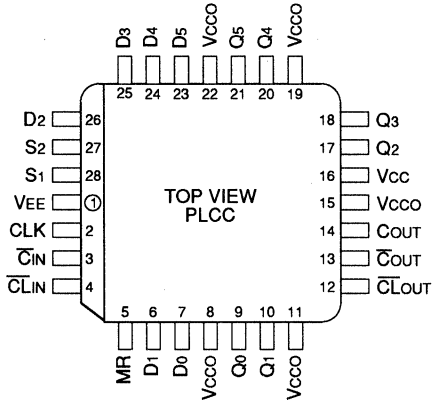
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E131JC	J28-1	Commercial
SY100E131JC	J28-1	Commercial

FEATURES

- **550MHz count frequency**
- **Look-ahead-carry input and output**
- **Fully synchronous up and down counting**
- **Asynchronous Master Reset**
- **Internal 75KΩ input pull-down resistors**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **ESD protection of 2000V**

PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0–D_5	Preset Data Inputs
Q_0–Q_5	Differential Data Outputs
S_1, S_2	Mode Control Pins
MR	Master Reset
CLK	Clock Input
COUT, $\overline{\text{COUT}}$	Carry Out Output (Active LOW)
$\overline{\text{CLOUT}}$	Look-Ahead-Carry Output
$\overline{\text{CIN}}$	Carry-In Input (Active LOW)
$\overline{\text{CLIN}}$	Look-Ahead-Carry Input

DESCRIPTION

The SY10E/100E136 are 6-bit synchronous, presettable, cascadable universal counters. These devices generate a look-ahead-carry output and accept a look-ahead-carry input. These two features allow for the cascading of multiple E136s for wider bit width counters that operate at very nearly the same frequency as the stand-alone counter.

The $\overline{\text{CLOUT}}$ output will pulse LOW for one clock cycle one count before the E136 reaches terminal count. The $\overline{\text{COUT}}$ output will pulse LOW for one clock cycle when the counter reaches terminal count. For more information on utilizing the look-ahead-carry features of the device, please refer to the applications section of this data sheet. The differential COUT output facilitates the E136's use in programmable divider and self-stopping counter applications.

Unlike the H136 and other similar universal counter designs, the E136 carry-out and look-ahead-carry-out signals are registered on chip. This design alleviates the glitch problem seen on many counters where the carry-out signals are merely gated. Because of this architecture, there are some minor functional differences between the E136 and H136 counters. The user, regardless of familiarity with the H136, should read this data sheet carefully. Note specifically (see block diagram) the operation of the carry-out outputs and the look-ahead-carry-in input when utilizing the Master Reset.

When left open, all of the input pins will be pulled LOW via an input pulldown resistor. The Master Reset is an asynchronous signal which, when asserted, will force the Q outputs LOW.

The Q outputs need not be terminated for the E136 to function properly. In fact, if these outputs will not be used in a system, it is recommended that they be left open to save power and minimize noise. This practice will minimize switching noise which can reduce the maximum count frequency of the device, or significantly reduce margins against other noise in the system.

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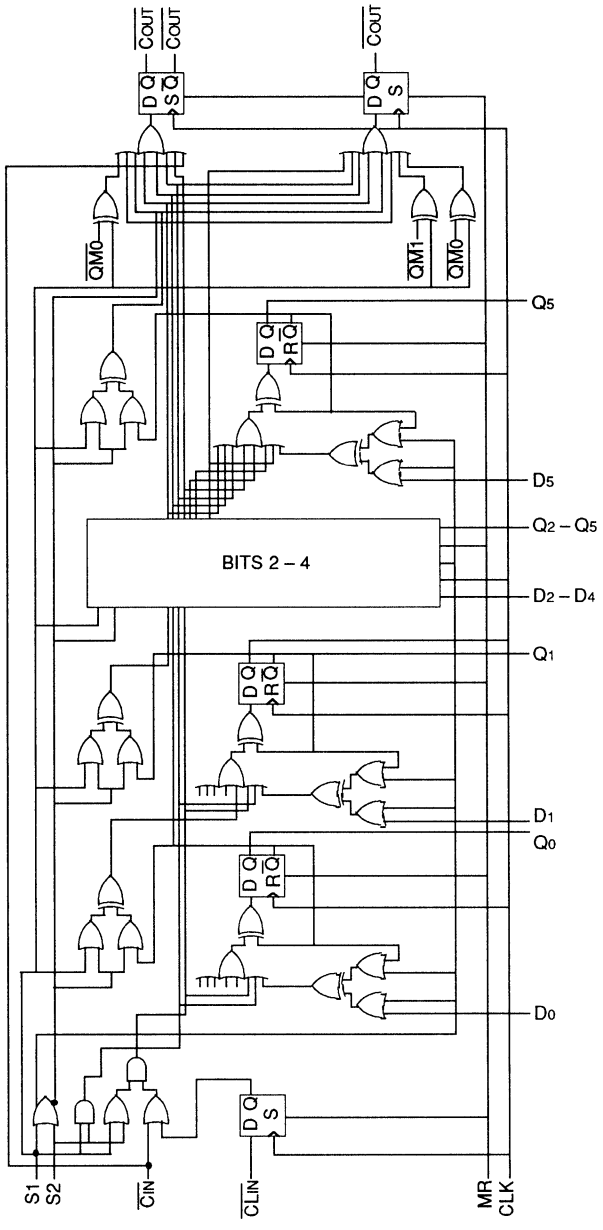
BLOCK DIAGRAM[1]



E136 Universal Up/Down Counter Logic Diagram

NOTE:

1. This diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

TRUTH TABLE[1]

S_1	S_2	$\overline{C}_{IN}$	MR	CLK	Function
L	L	X	L	Z	Preset Parallel Data Inputs
L	H	L	L	Z	Increment (Count Up)
L	H	H	L	Z	Hold Count
H	L	L	L	Z	Decrement (Count Down)
H	L	H	L	Z	Hold Count
H	H	X	L	Z	Hold Count
X	X	X	H	X	Reset (Qn = LOW; C_{OUT} = HIGH)

NOTE:
1. Expanded truth table included on following pages.

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO}$ = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	125	150	—	125	150	—	125	150		
	100E	—	125	150	—	125	150	—	140	170		

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO}$ = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
f_{COUNT}	Maximum Count Frequency	550	650	—	550	650	—	550	650	—	MHz	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK to Q	850	1150	1450	850	1150	1450	850	1150	1450		
	MR to Q	850	1150	1450	850	1150	1450	850	1150	1450		
	CLK to $\overline{C}_{OUT}$	800	1150	1300	800	1150	1300	800	1150	1300		
	CLK to $\overline{CL}_{OUT}$	825	1150	1400	825	1150	1400	825	1150	1400		
t_s	Set-up Time										ps	—
	S_1, S_2	1500	650	—	1500	650	—	1500	650	—		
	D	800	400	—	800	400	—	800	400	—		
	$\overline{CL}_{IN}$	150	0	—	150	0	—	150	0	—		
	$\overline{C}_{IN}$	800	400	—	800	400	—	800	400	—		
t_h	Hold Time										ps	—
	S_1, S_2	150	–200	—	150	–200	—	150	–200	—		
	D	150	–250	—	150	–250	—	150	–250	—		
	$\overline{CL}_{IN}$	300	0	—	300	0	—	300	0	—		
	$\overline{C}_{IN}$	150	–250	—	150	–250	—	150	–250	—		
t_{RR}	Reset Recovery Time	1000	700	—	1000	700	—	1000	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	700	400	—	700	400	—	700	400	—	ps	—
t_r	Rise/Fall Times										ps	—
t_f	20% to 80%											
	$\overline{C}_{OUT}$	275	—	600	275	—	600	275	—	600		
	Other	300	—	700	300	—	700	300	—	700		

EXPANDED TRUTH TABLE[1]

Function	S_1	S_2	MR	$\overline{C_{IN}}$	$\overline{CL_{IN}}$	CLK	D_5	D_4	D_3	D_2	D_1	D_0	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{C_{OUT}}$	$\overline{CL_{OUT}}$
Preset	L	L	L	X	X	Z	L	L	L	L	H	H	L	L	L	L	H	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Hold	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
Hold	H	L	L	L	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
	L	H	L	H	H	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Hold	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	H	H	H
Reset	X	X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	H	H

NOTE:
1. Z = LOW-to-HIGH transition

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E136JC	J28-1	Commercial
SY100E136JC	J28-1	Commercial

APPLICATIONS INFORMATION

Overview

The SY10E/100E136 are 6-bit synchronous, presettable, cascadable universal counters. Using the S_1 and S_2 control pins, the user can select between preset, count up, count down and hold count. The Master Reset pin will reset the internal counter and set the $\overline{C}_{OUT}$, $\overline{CL}_{OUT}$ and $\overline{CL}_{IN}$ flip-flops. Unlike previous 136-type counters, the carry-out outputs will go to a high state during the preset operation. In addition, since the carry-out outputs are registered, they will not go low if terminal count is loaded into the register. The look-ahead-carry-out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry-out functions. This architecture not only reduces the carry-out delay, but is essential to incorporate the registered carry-out functions. In addition to being faster, the resulting carry-out signals are stable and glitch free because these functions are registered.

Cascading Multiple E136 Devices

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications, several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past, cascading several 136-type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result, past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately, these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture, it is minor compared to the impact of the ripple propagate designs. As a result, the E016-type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

Several improvements have been incorporated to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly, these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.

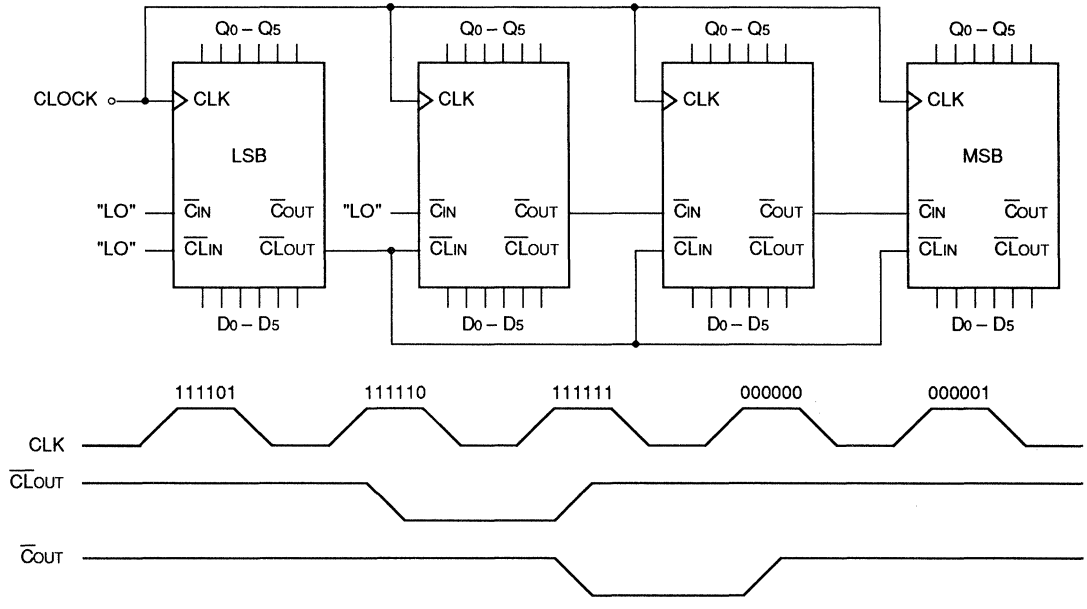


Figure 1. 24-bit Cascaded E136 Counter

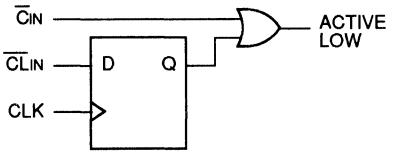


Figure 2. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ($\overline{CLOUT}$) pulses low one clock pulse before the counter reaches terminal count. Also note that both $\overline{CLOUT}$ and the carry-out pin ($\overline{COUT}$) of the device pulse low for only one clock period. The input structure for look-ahead-carry-in ($\overline{CLIN}$) and carry-in ($\overline{CIN}$) is pictured in Figure 2.

The $\overline{CLIN}$ input is registered and then OR'ed with the $\overline{CIN}$ input. From the truth table one can see that both the $\overline{CIN}$ and the $\overline{CLIN}$ inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The $\overline{CLIN}$ inputs are driven by the $\overline{CLOUT}$ output of the lower order E136 and, therefore, are only asserted for a single clock period. Since the $\overline{CLIN}$ input is registered, it must be asserted one clock period prior to the $\overline{CIN}$ input.

If the counter previous to a given counter is at terminal count, its $\overline{COUT}$ output, and thus the $\overline{CIN}$ input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The $\overline{CLOUT}$ output of the LSC will pulse low one clock period before it reaches terminal count. This $\overline{CLOUT}$ signal will be clocked into the $\overline{CLIN}$ input of the higher order counters on the following positive clock transition. Since both $\overline{CIN}$ and $\overline{CLIN}$ are in the LOW state, the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by the $\overline{CIN}$ inputs, to count by one.

During the clock pulse in which the higher order counter is counting by one, the $\overline{CLIN}$ is clocking in the high signal presented by the $\overline{CLOUT}$ of the LSC. The $\overline{CIN}$s in the higher order counter will ripple through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has 2^6-1 or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the set-up time of the $\overline{CLIN}$ input. This limit will consist of the CLK to $\overline{CLOUT}$ delay of the E136, plus the $\overline{CLIN}$ set-up time, plus any path length differences between the $\overline{CLOUT}$ output and the clock.

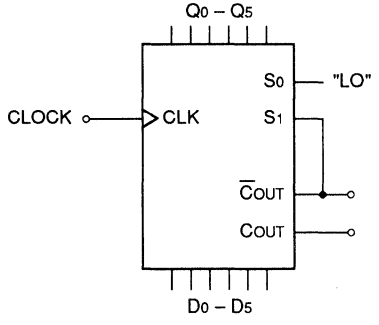


Figure 3. 6-bit Programmable Divider

Programmable Divider

Using external feedback of the $\overline{COUT}$ pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count-down programmable divider. If for some reason a count-up divider is preferred, the $\overline{COUT}$ signal is simply fed back to S2 rather than S1. Examination of the truth table for the E136 shows that when both S1 and S2 are LOW, the counter will parallel load on the next positive transition of the clock. If the S2 input is low and the S1 input is high, the counter will be in the count-down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the $\overline{COUT}$ output, it becomes a trivial matter to build programmable dividers.

For a programmable divider, one must to load a predesignated number into the counter and count to terminal count. Upon terminal count, the counter should automatically reload the divide number. With the architecture shown in Figure 3, when the counter reaches terminal count, the $\overline{COUT}$ output, and thus the S1 input, will go LOW. This, combined with the low on S2 will cause the counter to load the inputs present on D0–D5. Upon loading the divide value into the counter, $\overline{COUT}$ will go HIGH as the counter is no longer at terminal count, thereby placing the counter back into the count mode.

Divide Ratio	Preset Data Inputs					
	D5	D4	D3	D2	D1	D0
2	L	L	L	L	L	H
3	L	L	L	L	H	L
4	L	L	L	L	H	H
5	L	L	L	H	L	L
*	*	*	*	*	*	*
*	*	*	*	*	*	*
36	H	L	L	L	H	H
37	H	L	L	H	L	L
38	H	L	L	H	L	H
*	*	*	*	*	*	*
*	*	*	*	*	*	*
62	H	H	H	H	L	H
63	H	H	H	H	H	L
64	H	H	H	H	H	H

Table 1. Preset Inputs Versus Divide Ratio

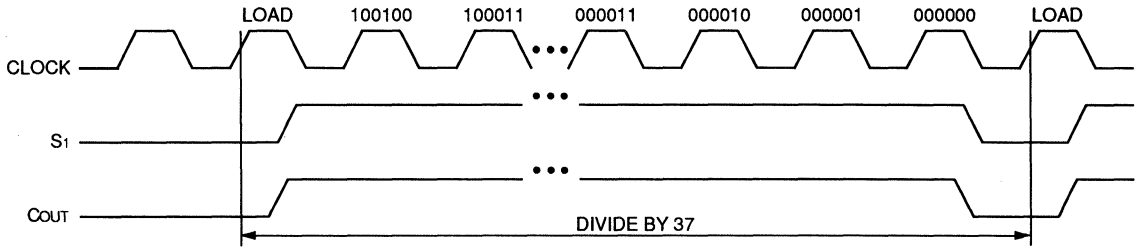


Figure 4. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N-1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64, inclusive. Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complimentary output ($\overline{COUT}$) allows the user to choose the polarity of the divide by output.

For single device programmable counters, the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter. This not only simplifies board design, but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits, the benefits of the E016 diminishes and, in fact, for very wide dividers, the E136 will provide the capability of a faster count frequency. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However, the final decision as to what device to use for external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating, the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.

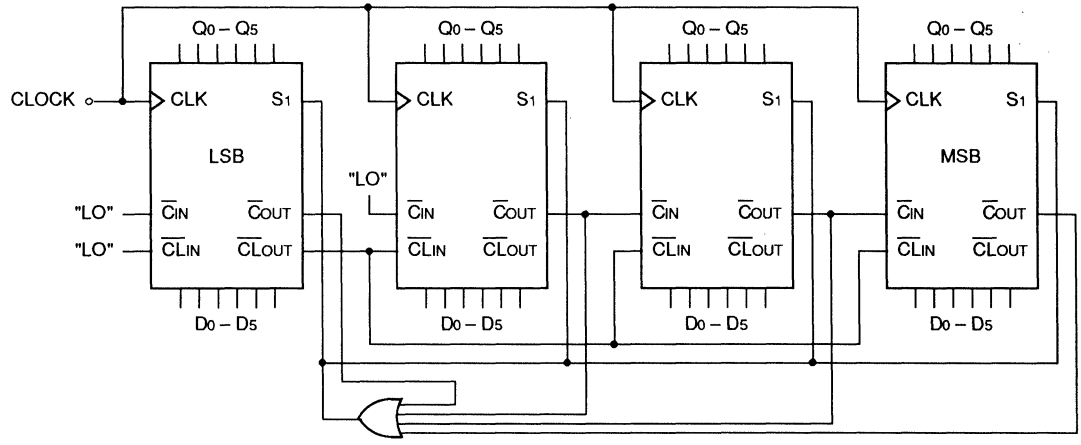


Figure 5. 24-bit Programmable Divider Architecture

FEATURES

- **1.8GHz min. count frequency**
- **Synchronous and asynchronous enable pins**
- **Differential clock input and data output pins**
- **V_{BB} output for single-ended use**
- **Asynchronous Master Reset**
- **Internal 75KΩ input pull-down resistors**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **ESD protection of 2000V**

DESCRIPTION

The SY10E/100E137 are very high speed binary ripple counters. The two least significant bits were designed with very fast edge rates, while the more significant bits maintain standard ECLinPS output edge rates. This allows the counters to operate at very high frequencies, while maintaining a moderate power dissipation level.

The devices are ideally suited for multiple frequency clock generation, as well as for counters in high-performance ATE time measurement boards.

Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted, enables the counter while overriding any synchronous enable signals. The E137 features XOR'ed enable inputs, EN_1 and EN_2, which are synchronous to the CLK input. When only one synchronous enable is asserted, the counter becomes disabled on the next CLK transition. All outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted in order to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. EN_1 (or EN_2) and CLK edges are coincident. Sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip-flop set-up time) to ensure that the synchronous enable signal is clocked correctly; hence, the counter is disabled.

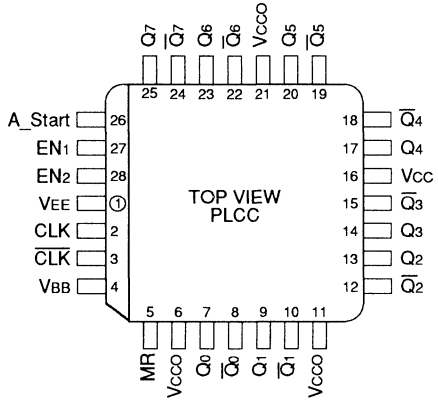
The E137 can also be driven single-endedly utilizing the V_{BB} output supply as the voltage reference for the CLK input signal. If a single-ended signal is to be used, the V_{BB} pin should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. V_{BB} can only source/sink 0.5mA; therefore, it should be used as a switching reference for the E137 only.

All input pins left open will be pulled LOW via an input pull-down resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

4

PIN CONFIGURATION

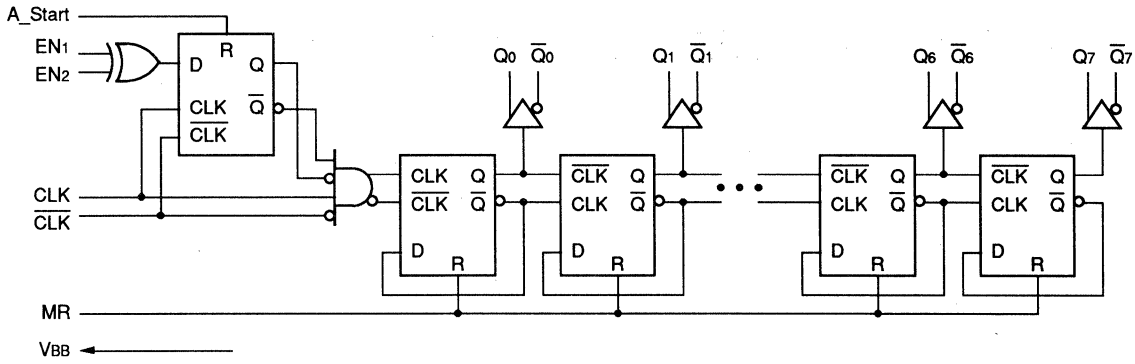


PIN NAMES

Pin	Function
CLK, $\overline{CLK}$	Differential Clock Inputs
Q_0–Q_7, $\overline{Q}_0$–$\overline{Q}_7$	Differential Q Outputs
A_Start	Asynchronous Enable Input
EN_1, EN_2	Synchronous Enable Inputs
MR	Asynchronous Master Reset
V_{BB}	Switching Reference Output

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



SEQUENTIAL TRUTH TABLE(1)

Function	EN1	EN2	A_Start	MR	CLK	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L
Count	L	L	L	L	Z	L	L	L	L	L	L	L	H
	L	L	L	L	Z	L	L	L	L	L	L	H	L
	L	L	L	L	Z	L	L	L	L	L	L	H	H
Stop	H	L	L	L	Z	L	L	L	L	L	L	H	H
	H	L	L	L	Z	L	L	L	L	L	L	H	H
Async. Start	H	L	H	L	Z	L	L	L	L	L	H	L	L
	H	L	H	L	Z	L	L	L	L	L	H	L	H
	L	L	H	L	Z	L	L	L	L	L	H	H	L
Count	L	L	L	L	Z	L	L	L	L	L	H	H	H
	L	L	L	L	Z	L	L	L	L	H	L	L	L
	L	L	L	L	Z	L	L	L	L	H	L	L	H
Stop	L	H	L	L	Z	L	L	L	L	H	L	L	H
	L	H	L	L	Z	L	L	L	L	H	L	L	H
Sync. Start	H	H	L	L	Z	L	L	L	L	H	L	H	L
	H	H	L	L	Z	L	L	L	L	H	L	H	H
	H	H	L	L	Z	L	L	L	L	H	H	L	L
Stop	H	L	L	L	Z	L	L	L	L	H	H	L	L
	H	L	L	L	Z	L	L	L	L	H	H	L	L
Count	L	L	L	L	Z	L	L	L	L	H	H	L	H
	L	L	L	L	Z	L	L	L	L	H	H	H	L
	L	L	L	L	Z	L	L	L	L	H	H	H	H
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L

NOTE:
1. Z = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{EE}	Output Reference Voltage										V	—
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	121	145	—	121	145	—	121	145		
	100E	—	121	145	—	121	145	—	139	167		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{COUNT}	Max. Count Frequency	1800	2200	—	1800	2200	—	1800	2200	—	MHz	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK to Q_0	1300	1700	2150	1300	1700	2150	1350	1750	2200		
	CLK to Q_1	1600	2025	2500	1600	2050	2500	1650	2100	2550		
	CLK to Q_2	1950	2425	2925	1950	2450	2925	2025	2500	3000		
	CLK to Q_3	2275	2750	3350	2275	2775	3350	2350	2850	3425		
	CLK to Q_4	2625	3125	3750	2625	3150	3750	2700	3225	3625		
	CLK to Q_5	2950	3450	4150	2950	3475	4150	3050	3550	4250		
	CLK to Q6	3250	3775	4450	3250	3800	4450	3375	3925	4600		
	CLK to Q_7	3575	4075	4800	3575	4125	4800	3700	4250	4950		
	A_Start to Q_0	950	1325	1700	950	1325	1700	950	1325	1700		
	MR to Q_0	700	1000	1300	700	1000	1300	700	1000	1300		
t_s	Set-up Time (EN_1, EN_2)	0	–150	—	0	–150	—	0	–150	—	ps	—
t_h	Hold Time (EN_1, EN_2)	300	150	—	300	150	—	300	150	—	ps	—
t_{RR}	Reset Recovery Time MR, A_Start	400	200	—	400	200	—	400	200	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR, A_Start	400	—	—	400	—	—	400	—	—	ps	—
V_{PP}	Minimum Input Swing (CLK)	0.25	—	1.0	0.25	—	1.0	0.25	—	1.0	V	1
V_{CMR}	Com. Mode Range (CLK)	–0.4	—	–2.0	–0.4	—	–2.0	–0.4	—	–2.0	V	—
t_r	Rise/Fall Time, 20% to 80%										ps	—
t_f	Q_0, Q_1	150	—	400	150	—	400	150	—	400		
	Q_2–Q_7	275	—	600	275	—	600	275	—	600		

NOTE:

1. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E137JC	J28-1	Commercial
SY100E137JC	J28-1	Commercial

FEATURES

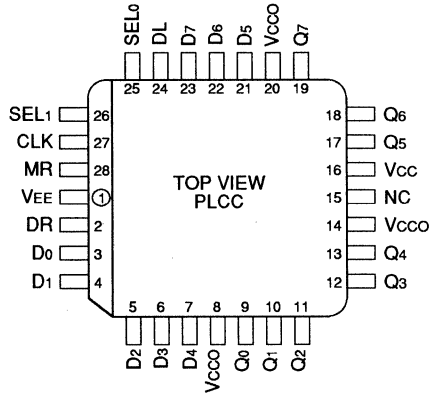
- **700MHz min. shift frequency**
- **8 bits wide**
- **Bi-directional**
- **Four selectable modes for full functionality**
- **Asynchronous Master Reset**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E141**
- **Pin-compatible with E241**

DESCRIPTION

The SY10E141 and SY100E141 are 8-bit, full-function shift registers designed for use in new, high-performance ECL systems. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D_0–D_7 accept parallel input data, while DL/DR accept serial input data for left/right shifting.

The two select pins, SEL_0 and SEL_1 permit four modes of operation: Load, Hold, Shift Left and Shift Right, as shown in the Truth Table. Input data is clocked into the register on the rising clock edge after meeting the minimum set-up time. A logic HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

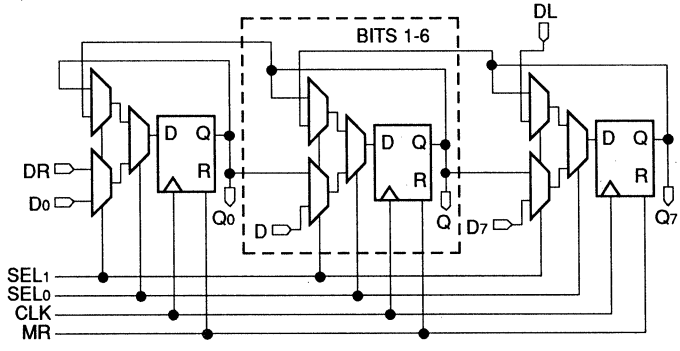
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0-D_7	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL_0, SEL_1	Mode Select Inputs
CLK	Clock
Q_0-Q_7	Data Outputs
MR	Master Reset

BLOCK DIAGRAM



Rev.: B Amendment: /0
Issue Date: February, 1994

TRUTH TABLE

Function	DL	DR	SEL_0	SEL_1	MR	CLK	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Load	X	X	L	L	L	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Shift Right	X	L	L	H	L	Z	L	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6
	X	H	L	H	L	Z	H	L	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5
Shift Left	L	X	H	L	L	Z	L	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L
	H	X	H	L	L	Z	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L	H
Hold	X	X	H	H	L	Z	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L	H
	X	X	H	H	L	Z	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	131	157	—	131	157	—	131	157		
	100E	—	131	157	—	131	157	—	151	181		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
f_{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_s	Set-up Time										ps	—
	D	175	25	—	175	25	—	175	25	—		
	SEL_0	350	200	—	350	200	—	350	200	—		
	SEL_1	300	150	—	300	150	—	300	150	—		
t_h	Hold Time										ps	—
	D	200	–25	—	200	–25	—	200	–25	—		
	SEL_0	100	–200	—	100	–200	—	100	–200	—		
	SEL_1	100	–150	—	100	–150	—	100	–150	—		
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E141JC	J28-1	Commercial
SY100E141JC	J28-1	Commercial

9-BIT SHIFT REGISTER

FEATURES

- **700MHz min. shift frequency**
- **9 bits wide for byte-parity applications**
- **Asynchronous Master Reset**
- **Dual clocks**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E142**

DESCRIPTION

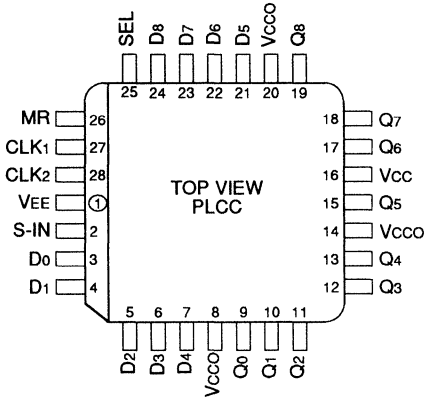
The SY10E142 and SY100E142 are high-speed 9-bit shift registers designed for use in new, high-performance ECL systems. The E142 can accept serial or parallel data to be shifted out in one direction as both serial and parallel outputs. The nine inputs, D_0-D_8, accept parallel input data, while S-IN accepts serial input data.

The SEL (Select) control pin serves to determine the mode of operation, either SHIFT or LOAD. The shift direction is from bit 0 to bit 8. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK_1 or CLK_2. Shifting is also performed on the rising edge of either CLK_1 or CLK_2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E142 is designed for applications such as diagnostic scan registers, parallel-to-serial conversions and is also suitable for byte-wide parity.

4

PIN CONFIGURATION

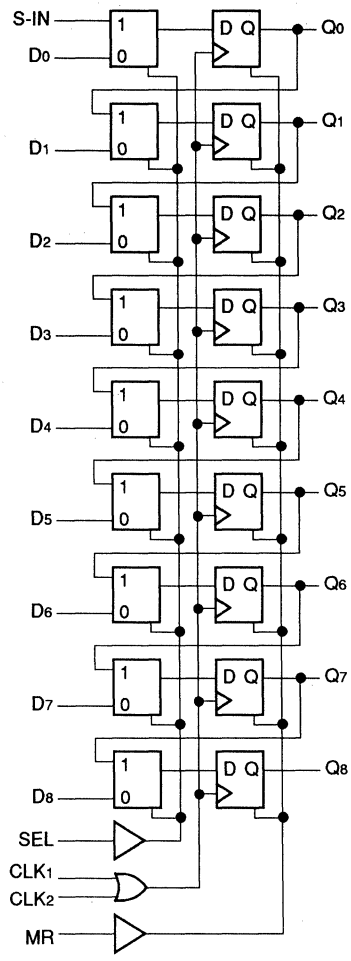


PIN NAMES

Pin	Function
D_0-D_8	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0-Q_8	Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE

SEL	MODE
L	LOAD
H	SHIFT

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	120	145	—	120	145	—	120	145		
	100E	—	120	145	—	120	145	—	138	165		

4

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Set-up Time										ps	—
	D	50	–100	—	50	–100	—	50	–100	—		
	SEL	300	150	—	300	150	—	300	150	—		
t_h	Hold Time										ps	—
	D	300	100	—	300	100	—	300	100	—		
	SEL	75	–150	—	75	–150	—	75	–150	—		
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E142JC	J28-1	Commercial
SY100E142JC	J28-1	Commercial

FEATURES

- **700MHz min. operating frequency**
- **9 bits wide for byte-parity applications**
- **Asynchronous Master Reset**
- **Dual clocks**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75kΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E143**

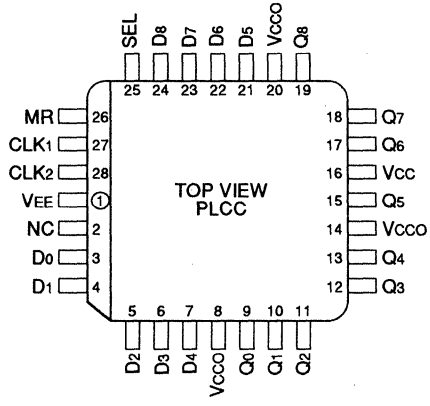
DESCRIPTION

The SY10E143 and SY100E143 are high-speed 9-bit hold registers designed for use in new, high-performance ECL systems. The E143 can hold current data or load new data. The nine inputs, D_0-D_8, accept parallel input data.

The SEL (Select) control pin serves to determine the mode of operation; either HOLD or LOAD. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK_1 or CLK_2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E143 is designed for applications requiring high-speed registers, pipeline registers, synchronous operation, and is also suitable for byte-wide parity.

PIN CONFIGURATION

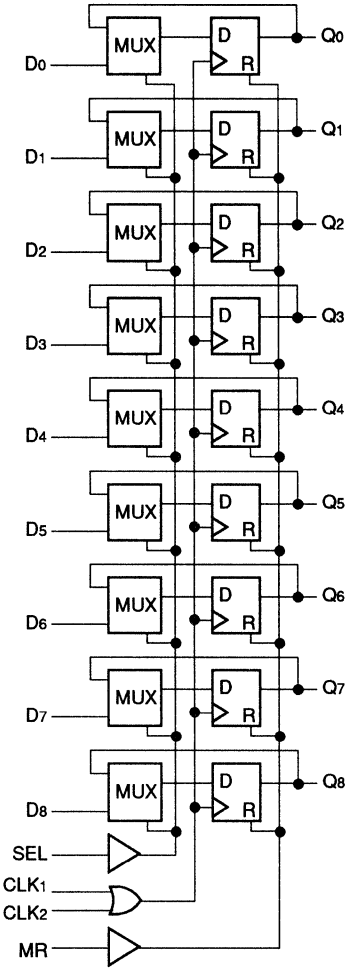


PIN NAMES

Pin	Function
D_0-D_8	Parallel Data Inputs
SEL	Mode Select Input
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0-Q_8	Data Outputs
NC	No Connection

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE

SEL	MODE
L	LOAD
H	HOLD

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	120	145	—	120	145	—	120	145		
	100E	—	120	145	—	120	145	—	138	165		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Set-up Time										ps	—
	D	50	–100	—	50	–100	—	50	–100	—		
	SEL	300	150	—	300	150	—	300	150	—		
t_h	Hold Time										ps	—
	D	300	100	—	300	100	—	300	100	—		
	SEL	75	–150	—	75	–150	—	75	–150	—		
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E143JC	J28-1	Commercial
SY100E143JC	J28-1	Commercial

FEATURES

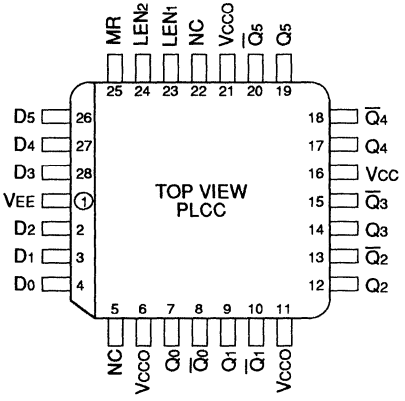
- **700ps max. propagation delay**
- **Differential outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E150**

DESCRIPTION

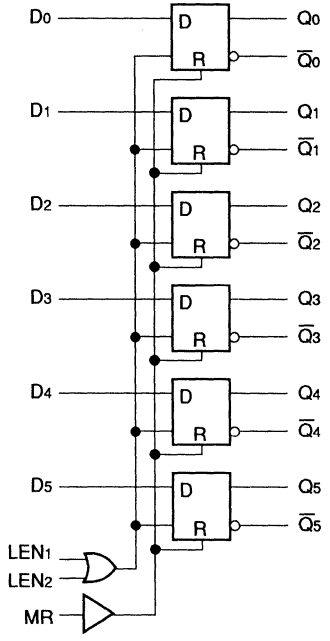
The SY10E150 and SY100E150 are 6-bit D latches with differential outputs designed for use in new, high-performance ECL systems. When both Latch Enables (LEN_1, LEN_2) are at a logic LOW, the latch is in the transparent mode and input data propagates through to the output. A logic HIGH on either LEN_1 or LEN_2 (or both) latches the input data. The Master Reset (MR) overrides all other signals to set the Q outputs to a logic LOW.

4

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_5	True Outputs
$\overline{Q_0}$–$\overline{Q_5}$	Inverting Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

TRUTH TABLE[1]

(Each Latch)

INPUTS				OUTPUTS		OPERATING
D_n	LEN_1	LEN_2	MR	Q_n	$\overline{Q}_n$	MODE
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched[2]	Latched[2]	
X	H	X	L	Latched[2]	Latched[2]	
X	X	X	H	L	H	Asynchronous

NOTES:
1. H = HIGH state
   L = LOW state
   X = Don't care
2. Retains Data that is present before the LEN positive transition.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current										µA	—
	D	—	—	200	—	—	200	—	—	200		
	LEN MR	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	52	62	—	52	62	—	52	62		
	100E	—	52	62	—	52	62	—	60	72		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	D	250	375	550	250	375	550	250	375	550		
	LEN	375	500	700	375	500	700	375	500	700		
	MR	450	625	750	450	625	750	450	625	750		
t_S	Se-tup Time, D	200	50	—	200	50	—	200	50	—	ps	—
t_H	Hold Time, D	200	–50	—	200	–50	—	200	–50	—	ps	—
t_{RR}	Reset Recovery Time	750	650	—	750	650	—	750	650	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	650	300	450	650	300	450	650	ps	—

NOTE:
1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E150JC	J28-1	Commercial
SY100E150JC	J28-1	Commercial

FEATURES

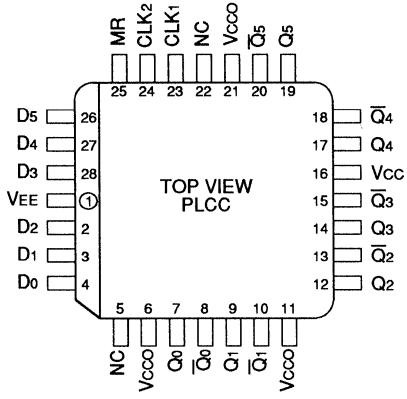
- **1100MHz toggle frequency**
- **Differential outputs**
- **Asynchronous Master Reset**
- **Dual clocks**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E151**

DESCRIPTION

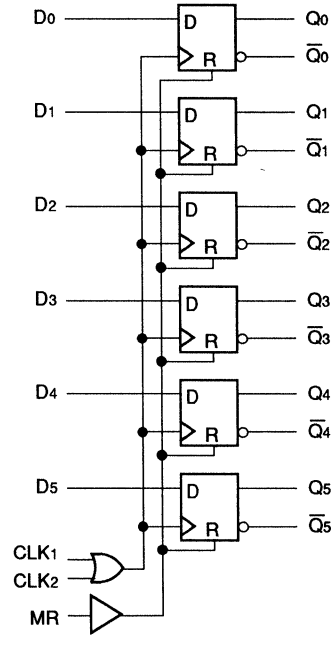
The SY10E151 and SY100E151 offer 6 edge-triggered, high-speed, master-slave D-type flip-flops with differential outputs, designed for use in new, high-performance ECL systems. The two external clock signals (CLK_1, CLK_2) are gated through a logical OR operation before use as clocking control for the flip-flops. Data is clocked into the flip-flops on the rising edge of either CLK_1 or CLK_2 (or both). When both CLK_1 and CLK_2 are at a logic LOW, data enters the master and is transferred to the slave when either CLK_1 or CLK_2 (or both) go HIGH.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0–Q_5	True Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Inverting Outputs

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Issue Date: February, 1994

TRUTH TABLES[1]

Asynchronous Operation

Inputs				Output
D_n	CLK_1	CLK_2	MR	$Q_n(t+1)$
X	X	X	H	L

Synchronous Operation

Inputs				Output
D_n	CLK_1	CLK_2	MR	$Q_n(t+1)$
L	↑	L	L	L
H	↑	L	L	H
L	L	↑	L	L
H	L	↑	L	H
X	H	↑	L	$Q_n(t)$
X	↑	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   t = Time before positive CLK transition
   t+1 = Time after positive CLK transition
   ↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	65	78	—	65	78	—	65	78		
	100E	—	65	78	—	65	78	—	75	90		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	475	650	800	475	650	800	475	650	800		
	MR	475	650	850	475	650	850	475	650	850		
t_S	Set-up Time, D	0	–175	—	0	–175	—	0	–175	—	ps	—
t_H	Hold Time, D	350	175	—	350	175	—	350	175	—	ps	—
t_{RR}	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	65	—	—	65	—	—	65	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	700	300	450	700	300	450	700	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E151JC	J28-1	Commercial
SY100E151JC	J28-1	Commercial

FEATURES

- **750ps max. LEN to output**
- **700ps max. D to output**
- **Differential outputs**
- **Asynchronous Master Reset**
- **Dual latch-enables**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E154**

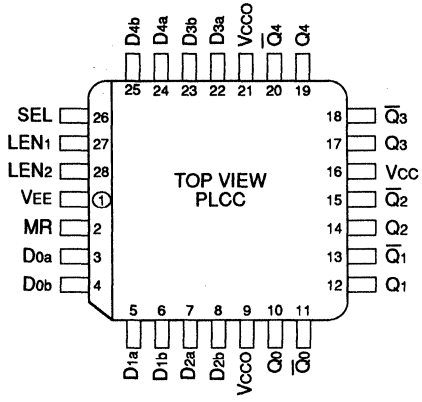
DESCRIPTION

The SY10E154 and SY100E154 offer five 2:1 multiplexers followed by latches with differential outputs, designed for use in new, high-performance ECL systems. The two external Latch-Enable signals (LEN_1, LEN_2) are gated through a logical OR operation before use as control for the five latches. When both LEN_1 and LEN_2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN_1 or LEN_2 (or both) are at a logic HIGH, the outputs are latched.

The multiplexer operation is controlled by the SEL(Select) signal which selects one of the two bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to make all Q outputs go to a logic LOW.

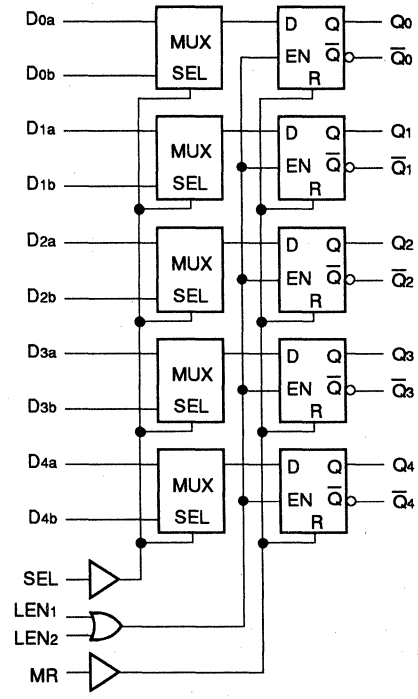
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{0a}–D_{4a}	Input Data a
D_{0b}–D_{4b}	Input Data b
SEL	Data Select Input
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_4	True Outputs
$\overline{Q}_0$–$\overline{Q}_4$	Inverted Outputs

BLOCK DIAGRAM



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TRUTH TABLES

SEL	Data
H	a
L	b

LEN_1	LEN_2	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	76	91	—	76	91	—	76	91		
	100E	—	76	91	—	76	91	—	87	105		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	325	500	700	325	500	700	325	500	700		
	SEL	475	650	925	475	650	925	475	650	925		
	LEN	350	500	750	350	500	750	350	500	750		
	MR	450	600	800	450	600	800	450	600	800		
t_S	Se-tup Time										ps	—
	D	300	100	—	300	100	—	300	100	—		
	SEL	500	250	—	500	250	—	500	250	—		
t_H	Hold Time										ps	—
	D	300	–100	—	300	–100	—	300	–100	—		
	SEL	200	–250	—	200	–250	—	200	–250	—		
t_{RR}	Reset Recovery Time	800	600	—	800	600	—	800	600	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_r	Rise/Fall Time	300	475	800	300	475	800	300	475	800	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E154JC	J28-1	Commercial
SY100E154JC	J28-1	Commercial

FEATURES

- **750ps max. LEN to output**
- **700ps max. D to output**
- **Single-ended outputs**
- **Asynchronous Master Reset**
- **Dual latch-enables**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E155**

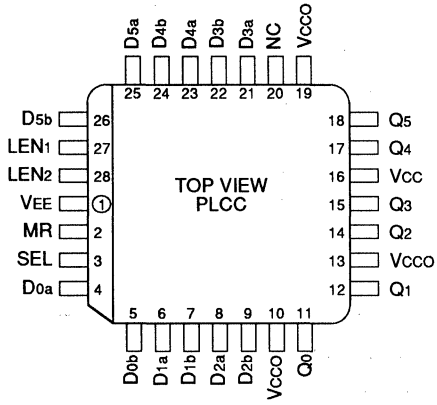
DESCRIPTION

The SY10E155 and SY100E155 offer six 2:1 multiplexers followed by latches with single-ended outputs, designed for use in new, high-performance ECL systems. The two external latch-enable signals (LEN_1 and LEN_2) are gated through a logical OR operation before use as control for the six latches. When both LEN_1 and LEN_2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN_1 or LEN_2 (or both) are at a logic HIGH, the outputs are latched.

The multiplexer operation is controlled by the SEL (Select) signal which selects one of the two bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to take all outputs to a logic LOW.

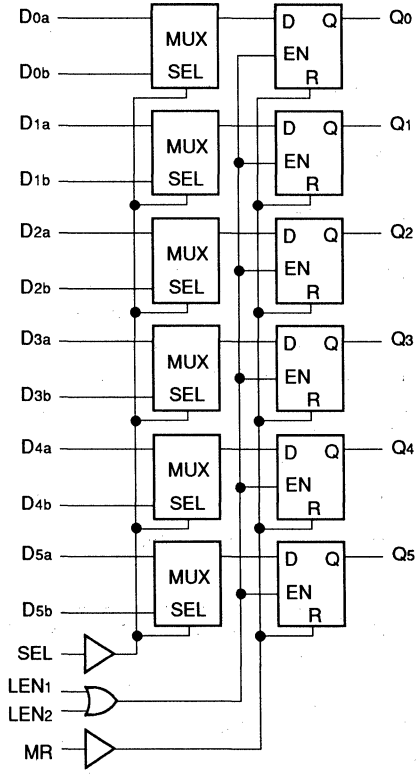
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{0a}–D_{5a}	Input Data a
D_{0b}–D_{5b}	Input Data b
SEL	Data Select Input
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_5	Outputs

BLOCK DIAGRAM



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TRUTH TABLES

SEL	Data
H	a
L	b

LEN_1	LEN_2	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	85	102	—	85	102	—	85	102		
	100E	—	85	102	—	85	102	—	98	117		

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE}$ (Min.) to V_{EE} (Max.); $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	D	325	500	700	325	500	700	325	500	700		
	SEL	475	675	925	475	675	925	475	675	925		
	LEN	350	500	750	350	500	750	350	500	750		
	MR	450	600	850	450	600	850	450	600	850		
t_S	Set-up Time										ps	—
	D	300	100	—	300	100	—	300	100	—		
	SEL	500	250	—	500	250	—	500	250	—		
t_H	Hold Time										ps	—
	D	300	–100	—	300	–100	—	300	–100	—		
	SEL	0	–250	—	0	–250	—	0	–250	—		
t_{RR}	Reset Recovery Time	800	650	—	800	650	—	800	650	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E155JC	J28-1	Commercial
SY100E155JC	J28-1	Commercial

3-BIT 4:1 MUX-LATCH

FEATURES

- **900ps max. D to output**
- **800ps max. LEN to output**
- **Differential outputs**
- **Asynchronous Master Reset**
- **Dual latch enables**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E156**

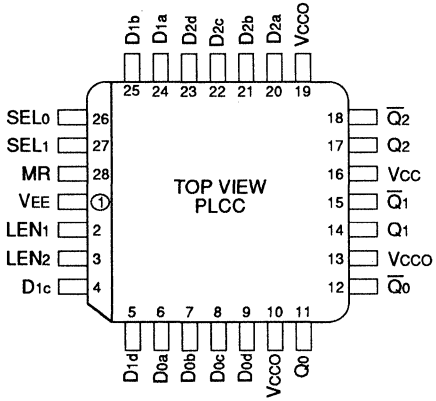
DESCRIPTION

The SY10E156 and SY100E156 offer three 4:1 multiplexers followed by latches with differential outputs, designed for use in new, high-performance ECL systems. The two external latch enable signals (LEN_1 and LEN_2) are gated through a logical OR operation before use as control for the three latches. When both LEN_1 and LEN_2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN_1 or LEN_2 (or both) are at a logic HIGH, the outputs are latched.

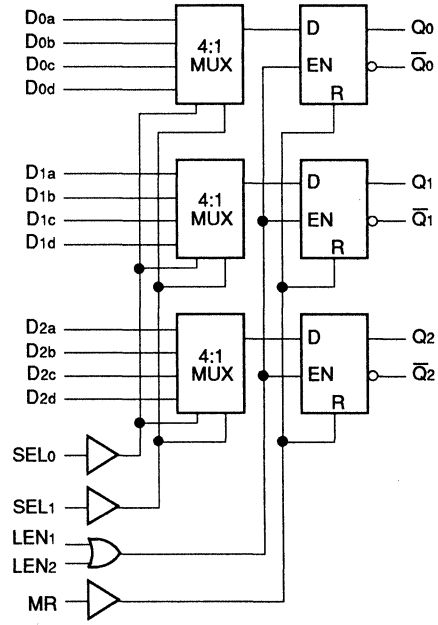
The multiplexer operation is controlled by the Select (SEL_0, SEL_1) signals which select one of the four bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to take all outputs to a logic LOW.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_{0x}–D_{2x}	Input Data
SEL_0, SEL_1	Select Inputs
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_2	True Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Inverted Outputs

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TRUTH TABLES

LEN_1	LEN_2	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

SEL_0	SEL_1	Data
L	L	a
H	L	b
L	H	c
H	H	d

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	75	90	—	75	90	—	75	90		
	100E	—	75	90	—	75	90	—	86	103		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	400	600	900	400	600	900	400	600	900		
	SEL_0	550	775	1050	550	775	1050	550	775	1050		
	SEL_1	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	800		
	MR	350	600	825	350	600	825	350	600	825		
t_s	Set-up Time										ps	—
	D	400	275	—	400	275	—	400	275	—		
	SEL_0	700	300	—	700	300	—	700	300	—		
	SEL_1	600	400	—	600	400	—	600	400	—		
t_h	Hold Time										ps	—
	D	300	–275	—	300	–275	—	300	–275	—		
	SEL_0	100	–300	—	100	–300	—	100	–300	—		
	SEL_1	200	–400	—	200	–400	—	200	–400	—		
t_{RR}	Reset Recovery Time	800	600	—	800	600	—	800	600	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_r	Rise/Fall Time	275	475	700	275	475	700	275	475	700	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E156JC	J28-1	Commercial
SY100E156JC	J28-1	Commercial

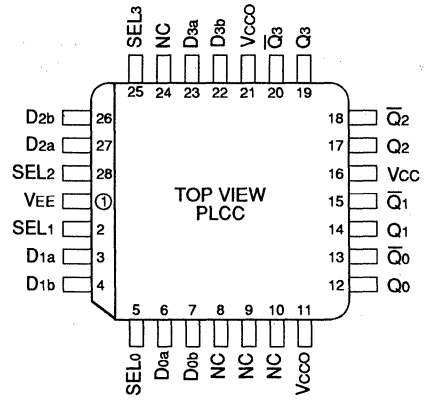
FEATURES

- **Individual select controls**
- **550ps max. D to Output**
- **800ps max. SEL to Output**
- **Internal 75KΩ input pull-down resistors**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**

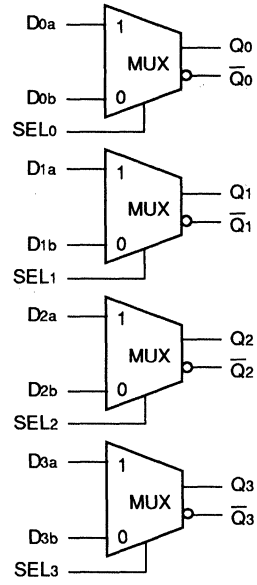
DESCRIPTION

The SY10/100E157 contain four 2:1 multiplexers with differential outputs. The output data are controlled by the individual Select (SEL) inputs. The individual select control makes the devices well suited for random logic designs.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_{0a} – D_{3a}	Input Data a
D_{0b} – D_{3b}	Input Data b
SEL_0 – SEL_3	Select Inputs
Q_0 – Q_3	True Outputs
$\overline{Q}_0$ – $\overline{Q}_3$	Inverted Outputs

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TRUTH TABLE

SEL	Data
H	a
L	b

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	D	—	—	200	—	—	200	—	—	200		
	SEL	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	32	38	—	32	38	—	32	38		
	100E	—	32	38	—	32	38	—	37	44		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	220	380	550	220	380	550	220	380	550		
	SEL	425	600	800	425	600	800	425	600	800		
t_{SKEW}	Within-Device Skew	—	70	—	—	70	—	—	70	—	ps	1
tr	Rise/Fall Times	275	400	650	275	400	650	275	400	650	ps	—
tf	20–80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E157JC	J28-1	Commercial
SY100E157JC	J28-1	Commercial

5-BIT 2:1 MULTIPLEXER

FEATURES

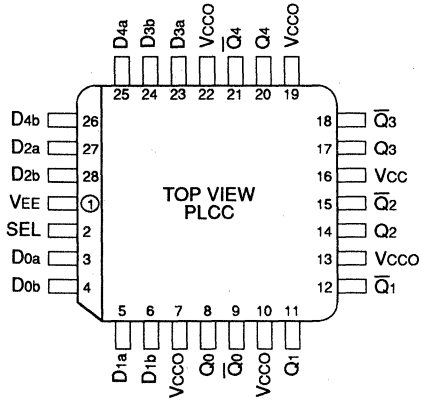
- **550ps max. D to output**
- **775ps max. SEL to output**
- **Differential outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E158**

DESCRIPTION

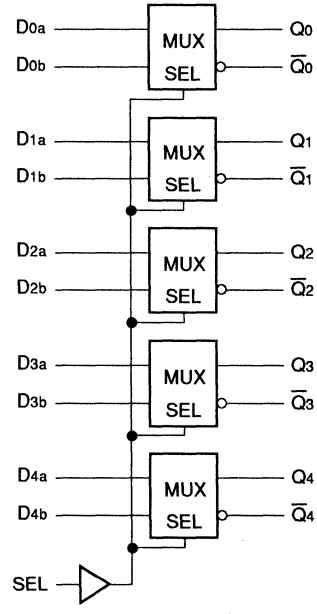
The SY10E158 and SY100E158 offer five 2:1 multiplexers with differential outputs, designed for use in new, high-performance ECL systems.

The multiplexer operation is controlled by the SEL (Select) signal which selects one of the two bits of input data at each mux to be passed through.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_{0a}–D_{4a}	Input Data a
D_{0b}–D_{4b}	Input Data b
SEL	Select Input
Q_0–Q_4	True Outputs
$\overline{Q}_0$–$\overline{Q}_4$	Inverted Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

TRUTH TABLE

SEL	Data
H	a
L	b

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	D	—	—	200	—	—	200	—	—	200		
	SEL	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	33	40	—	33	40	—	33	40		
	100E	—	33	40	—	33	40	—	38	46		

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	225	385	550	225	385	550	225	385	550		
	SEL	400	600	775	400	600	775	400	600	775		
t_{SKEW}	Within-Device Skew	—	60	—	—	60	—	—	60		ps	1
t_r	Rise/Fall Time	275	425	650	275	425	650	275	425	650	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E158JC	J28-1	Commercial
SY100E158JC	J28-1	Commercial

12-BIT PARITY GENERATOR/CHECKER

FEATURES

- **Provides odd-HIGH parity of 12 inputs**
- **Output register with Shift/Hold capability**
- **900ps max. D to Q/$\overline{Q}$ output**
- **Enable control**
- **Asynchronous Register Reset**
- **Differential outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E160**

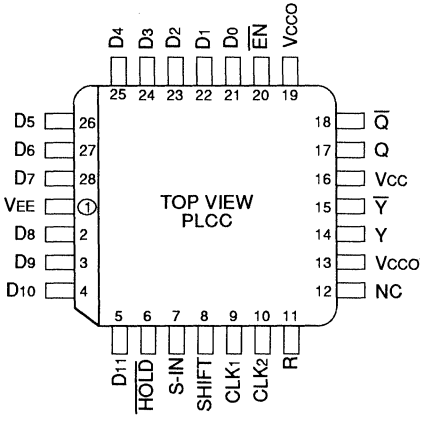
DESCRIPTION

The SY10E160 and SY100E160 are high-speed, 12-bit parity generator/checkers with differential outputs, for use in new, high-performance ECL systems. The output Q takes on a logic HIGH value only when an odd number of inputs are at a logic HIGH. A logic HIGH on the enable input (EN) forces the output Q to a logic LOW.

An additional feature of the E160 is the output register. Two multiplexers and their associated signals control the register input by providing the option of holding present data, loading the new parity data or shifting external data in. To hold the present data, the Hold signal (HOLD) must be at a logic LOW level. If the HOLD signal is at a logic HIGH, the data present at the Q output is passed through the first multiplexer. Taking the Shift signal (SHIFT) to a logic HIGH will shift the data at the S-IN pin into the output register. If the SHIFT signal is at a logic LOW, the output of the first multiplexer is then passed through to the register.

The register itself is clocked on the rising edge of CLK_1 or CLK_2 (or both). The presence of a logic HIGH on the reset pin (R) forces the register output Y to a logic LOW.

PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0–D_{11}	Data Inputs
S-IN	Serial Data Input
EN	Enable, active LOW
HOLD	Hold, active LOW
SHIFT	Shift, active HIGH
CLK_1, CLK_2	Clock Inputs
R	Reset Input
Q, $\overline{Q}$	Direct Output
Y, $\overline{Y}$	Register Output

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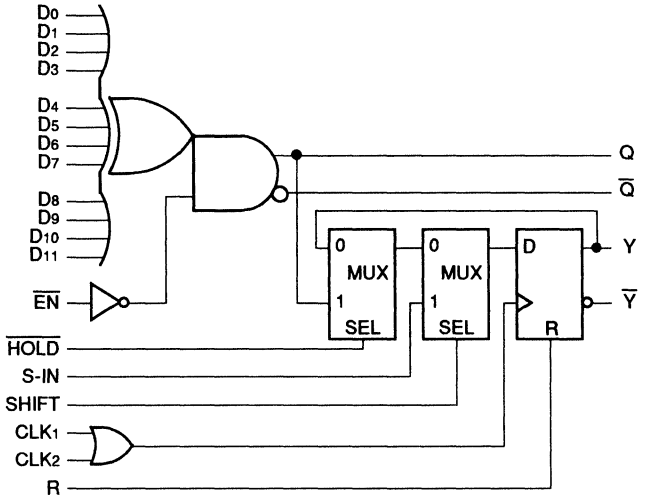
Issue Date: February, 1994

BLOCK DIAGRAM



4

TRUTH TABLE

Number of HIGH Inputs	Output Q
Even	LOW
Odd	HIGH

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current										µA	—
	CLK_1, CLK_2	—	—	200	—	—	200	—	—	200		
	R	—	—	300	—	—	300	—	—	300		
	All Other Inputs	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	82	98	—	82	98	—	82	98		
	100E	—	82	98	—	82	98	—	94	113		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to Q	400	650	950	400	650	950	400	650	950		
	EN to Q	300	550	750	300	550	750	300	550	750		
	CLK to Y	275	500	700	275	500	700	275	500	700		
	R to Y	275	500	725	275	500	725	275	500	725		
t_s	Set-up Time										ps	—
	D	1200	900	—	1200	900	—	1200	900	—		
	HOLD	600	300	—	600	300	—	600	300	—		
	S-IN	350	150	—	350	150	—	350	150	—		
	SHIFT	500	250	—	500	250	—	500	250	—		
t_h	Hold Time										ps	—
	D	–400	–900	—	–400	–900	—	–400	–900	—		
	HOLD	100	–300	—	100	–300	—	100	–300	—		
	S-IN	300	–150	—	300	–150	—	300	–150	—		
	SHIFT	200	–250	—	200	–250	—	200	–250	—		
t_r	Rise/Fall Time	300	450	650	300	450	650	300	450	650	ps	—
t_f	20% to 80%											

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E160JC	J28-1	Commercial
SY100E160JC	J28-1	Commercial

2-BIT 8:1 MULTIPLEXER

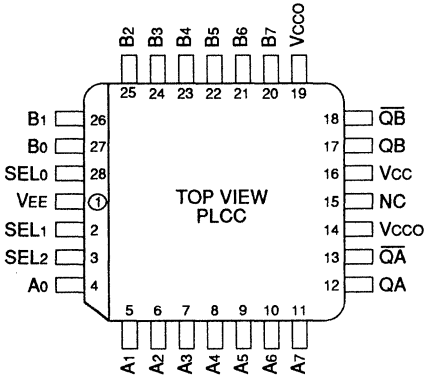
FEATURES

- **850ps max. propagation delay**
- **Differential outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E163**

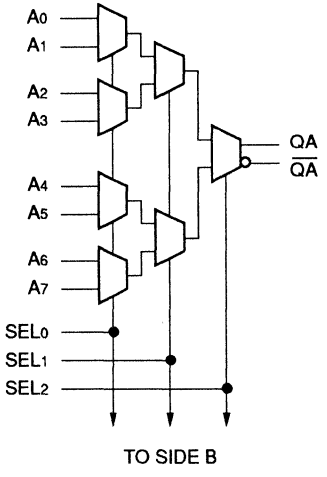
DESCRIPTION

The SY10E163 and SY100E163 offer two 8:1 multiplexers designed for use in new, high-performance ECL systems. The E163 has differential outputs and common select inputs. The select inputs (SEL_0, SEL_1, SEL_2) determine which one of the eight data inputs (A_0–A_7, B_0–B_7) is propagated to the output.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
A_0–A_7	A Data Inputs (D)
B_0–B_7	B Data Inputs (D)
$SEL_{0,1,2}$	Select Inputs
QA, QB	True Outputs
$\overline{QA}$, $\overline{QB}$	Inverting Outputs

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TRUTH TABLE

SEL_2	SEL_1	SEL_0	A/B Data
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	73	88	—	73	88	—	73	88		
	100E	—	73	88	—	73	88	—	83	100		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	400	550	800	400	550	800	400	550	800		
	SEL_0	525	725	950	525	725	950	525	725	950		
	SEL_1	425	625	850	425	625	850	425	625	850		
	SEL_2	350	525	725	350	525	725	350	525	725		
t_{SKEW}	Within-Device Skew										ps	1
	A_n, B_n to Q	—	40	—	—	40	—	—	40	—		
	A_n, A_m to QA	—	30	—	—	30	—	—	30	—		
	B_n, B_m to QB	—	30	—	—	30	—	—	30	—		
t_r	Rise/Fall Time	275	375	575	275	375	575	275	375	575	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transition on similar paths through a device; n = 0-7, m ≠ n, m = 0-7.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E163JC	J28-1	Commercial
SY100E163JC	J28-1	Commercial

FEATURES

- **850ps Data Input to Output**
- **Differential output**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E164**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pull-down resistors**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**

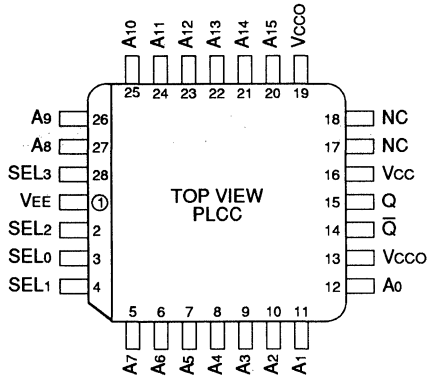
DESCRIPTION

The SY10E164 and SY100E164 are 16:1 multiplexers with a differential output. The select inputs ($SEL_{0,1,2,3}$) control which one of the sixteen data inputs (A_0–A_{15}) is propagated to the output.

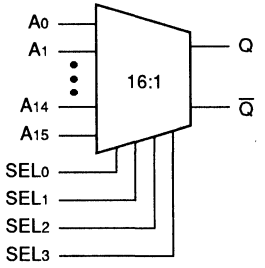
Special attention to the design layout results in a typical skew between the 16 inputs of only 50ps.

4

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
A_0 – A_{15}	Data Inputs
SEL[0:3]	Select Inputs
Q, $\overline{Q}$	Outputs

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TRUTH TABLE

SEL_3	SEL_2	SEL_1	SEL_0	Data
L	L	L	L	A_0
L	L	L	H	A_1
L	L	H	L	A_2
L	L	H	H	A_3
L	H	L	L	A_4
L	H	L	H	A_5
L	H	H	L	A_6
L	H	H	H	A_7

SEL_3	SEL_2	SEL_1	SEL_0	Data
H	L	L	L	A_8
H	L	L	H	A_9
H	L	H	L	A_{10}
H	L	H	H	A_{11}
H	H	L	L	A_{12}
H	H	L	H	A_{13}
H	H	H	L	A_{14}
H	H	H	H	A_{15}

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	59	71	—	59	71	—	59	71		
	100E	—	59	71	—	59	71	—	68	81		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	A Input	350	600	850	350	600	850	350	600	850		
	SEL_0	500	700	900	500	700	900	500	700	900		
	SEL_1	400	675	900	400	675	900	400	675	900		
	SEL_2	400	675	900	400	675	900	400	675	900		
	SEL_3	400	550	700	400	550	700	400	550	700		
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
tr	Rise/Fall Times	275	400	550	275	400	550	275	400	550	ps	—
tf	20–80%											

NOTE:

1. Within-device skew is defined as the difference in the A to Q delay between the 16 different A inputs.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E164JC	J28-1	Commercial
SY100E164JC	J28-1	Commercial

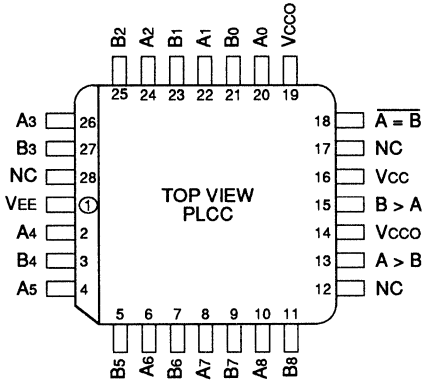
FEATURES

- **1100ps max. Propagation Delay $\overline{A = B}$**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E166**

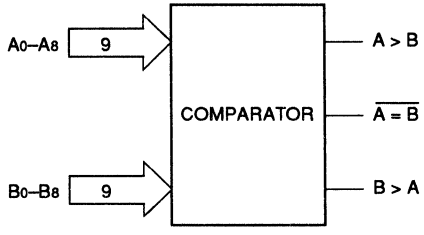
DESCRIPTION

The SY10E166 and SY100E166 are 9-bit magnitude comparators designed for use in new, high-performance ECL systems. The E166 compares the binary value of two 9-bit words and indicates whether one word is greater than or equal to the other.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
A_0–A_8	A Data Inputs
B_0–B_8	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A = B}$	A Equal to B Output (active-LOW)

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DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	113	136	—	113	136	—	113	136		
	100E	—	113	136	—	113	136	—	130	156		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to A = B	500	750	1100	500	750	1100	500	750	1100		
	D to A < B, A > B	500	850	1400	500	850	1400	500	850	1400		
t_r	Rise/Fall Time	300	450	800	300	450	800	300	450	800	ps	—
t_f	20% to 80%											

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E166JC	J28-1	Commercial
SY100E166JC	J28-1	Commercial

FEATURES

- **1000MHz min. operating frequency**
- **800ps max. clock to output**
- **Single-ended outputs**
- **Asynchronous Master Reset**
- **Dual clocks**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E167**

DESCRIPTION

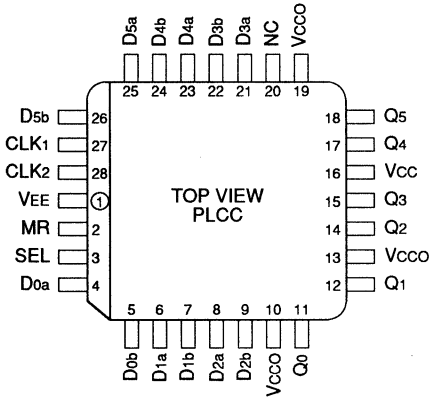
The SY10E167 and SY100E167 offer six 2:1 multiplexers followed by D flip-flops with single-ended outputs, designed for use in new, high-performance ECL systems. The Select (SEL) control allows one of the two data inputs to the multiplexer to pass through. The two external clock signals (CLK_1, CLK_2) are gated through a logical OR operation before use as control for the six flip-flops. The selected data are transferred to the flip-flops on the rising edge of CLK_1 or CLK_2 (or both).

The multiplexer operation is controlled by the Select (SEL) signal which selects one of the two bits of input data at each mux to be passed through.

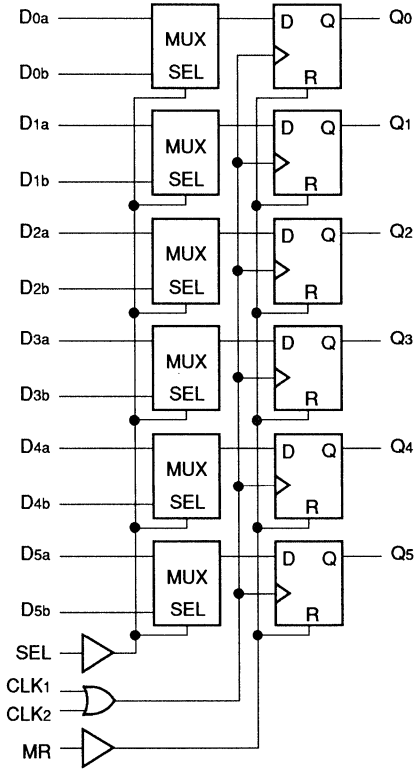
When a logic HIGH is applied to the Master Reset (MR) signal, it operates asychronously to take all outputs Q to a logic LOW.

4

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_{0a}–D_{5a}	Input Data a
D_{0b}–D_{5b}	Input Data b
SEL	Select Input
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0–Q_5	Data Outputs

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TRUTH TABLE

SEL	Data
H	a
L	b

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	94	113	—	94	113	—	94	113		
	100E	—	94	113	—	94	113	—	108	130		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1000	1400	—	1000	1400	—	1000	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	450	650	800	450	650	800	450	650	800		
	MR	450	650	850	450	650	850	450	650	850		
t_s	Set-up Time										ps	—
	D	100	–50	—	100	–50	—	100	–50	—		
	SEL	275	125	—	275	125	—	275	125	—		
t_h	Hold Time										ps	—
	D	300	50	—	300	50	—	300	50	—		
	SEL	75	–125	—	75	–125	—	75	–125	—		
t_{RR}	Reset Recovery Time	750	550	—	750	550	—	750	550	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E167JC	J28-1	Commercial
SY100E167JC	J28-1	Commercial

FEATURES

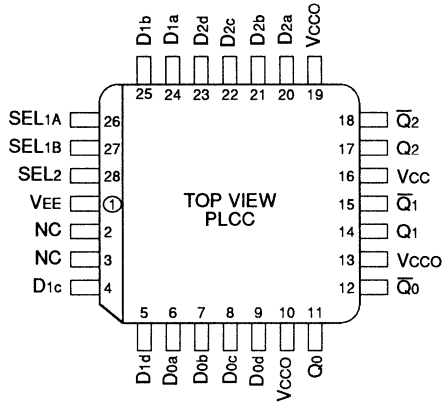
- **725ps max. D to output**
- **Differential outputs**
- **Split select architecture**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E171**

DESCRIPTION

The SY10E171 and SY100E171 offer three 4:1 multiplexers with differential outputs, designed for use in new, high-performance ECL systems. The leading 4-bit multiplexer operation is organized pairwise, with each pair being a 2-bit multiplexer. Separate select (SEL_{1A}, SEL_{1B}) controls are provided within each pair. The SEL_{1A} and SEL_{1B} signals control the leading multiplexers, while the SEL_2 signal controls the output multiplexer. The three select signals can be used to determine which of the four data inputs will be propagated to the corresponding outputs.

4

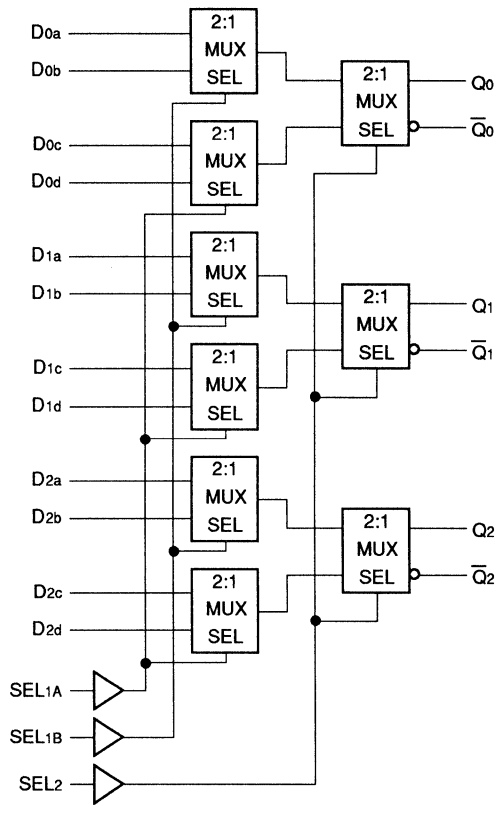
PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{0x}–D_{2x}	Data Inputs
SEL_{1A}, SEL_{1B}	First-stage Select Inputs
SEL_2	Second-stage Select Input
Q_0–Q_2	True Output
$\overline{Q}_0$–$\overline{Q}_2$	Inverted Output

BLOCK DIAGRAM



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TRUTH TABLE

Pin	State	Operation
SEL_2	H	Output c/d data
SEL_{1A}	H	Input d data
SEL_{1B}	H	Input b data

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	56	67	—	56	67	—	56	67		
	100E	—	56	67	—	56	67	—	65	77		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	275	480	650	275	480	650	275	480	650		
	SEL_1	450	650	850	450	650	850	450	650	850		
	SEL_2	350	550	700	350	550	700	350	550	700		
t_{SKEW}	Within-Device Skew										ps	1
	D_{nm}, D_{nm} to Q_n	—	60	—	—	60	—	—	60	—		
	D_a, D_b, D_c, D_d to Q	—	40	—	—	40	—	—	40	—		
t_r	Rise/Fall Time	300	475	650	300	475	650	300	475	650	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device; n = 0, 1, 2 m = a, b, c, d.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E171JC	J28-1	Commercial
SY100E171JC	J28-1	Commercial

9-BIT LATCH WITH PARITY

FEATURES

- **9-bit latch**
- **Parity detection/generation**
- **800ps max. D to Output**
- **Reset**
- **Internal 75KΩ input pull-down resistors**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E175**

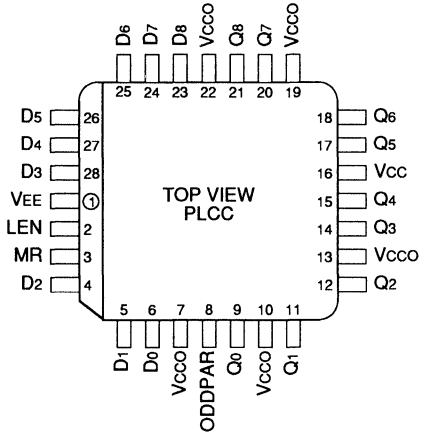
DESCRIPTION

The SY10E175 and SY100E175 are 9-bit latches. They also feature a tenth latched output (ODDPAR) which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

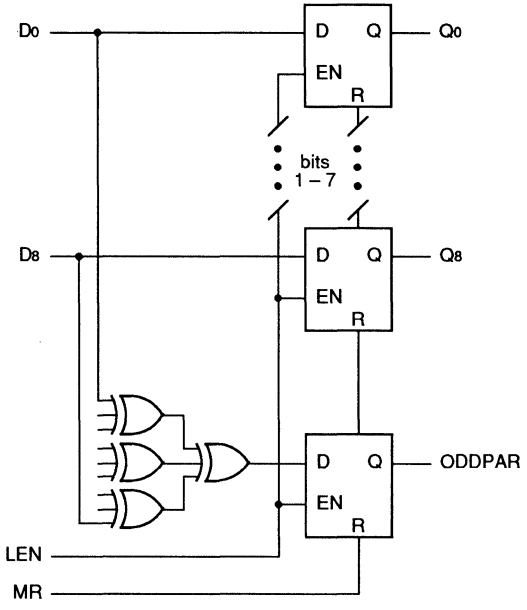
The E175 can also be used to generate byte parity by using D_8 as the parity-type select (L = even parity, H = odd parity) and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_8$	Data Inputs
LEN	Latch Enable
MR	Master Reset
$Q_0 - Q_8$	Data Outputs
ODDPAR	Parity Output

TRUTH TABLE

D	EN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of D_n HIGH
L	L	L	L	H if odd no. of D_n HIGH
X	H	L	Q_0	Q_0
X	X	H	L	L

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DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to Q	450	600	800	450	600	800	450	600	800		
	D to ODDPAR	850	1150	1450	850	1150	1450	850	1150	1450		
	LEN to Q	525	700	900	525	700	900	525	700	900		
	LEN to ODDPAR	525	700	900	525	700	900	525	700	900		
	MR to Q (t_{PHL})	525	700	900	525	700	900	525	700	900		
	MR to ODDPAR (t_{PHL})	525	700	900	525	700	900	525	700	900		
t_S	Set-up Time										ps	—
	D (Q)	275	100	—	275	—	—	275	—	—		
	D (ODDPAR)	900	700	—	900	—	—	900	—	—		
t_H	Hold Time										ps	—
	D (Q)	175	–100	—	175	—	—	175	—	—		
	D (ODDPAR)	–300	–700	—	–300	—	—	–300	—	—		
t_{RR}	Reset Recovery Time	850	600	—	850	600	—	850	600	—	ps	—
t_{SKEW}	Within-Device Skew										ps	1
	LEN, MR	—	75	—	—	75	—	—	75	—		
	D to Q	—	75	—	—	75	—	—	75	—		
	D to ODDPAR	—	200	—	—	200	—	—	200	—		
t_r	Rise/Fall Times	300	500	800	300	500	800	300	500	800	ps	—
t_f	20–80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E175JC	J28-1	Commercial
SY100E175JC	J28-1	Commercial

ERROR DETECTION/ CORRECTION CIRCUIT

FEATURES

- **Hamming code generation**
- **8-bit wide**
- **Expandable for more width**
- **Provides parity register**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.56V**
- **Internal75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E193**

DESCRIPTION

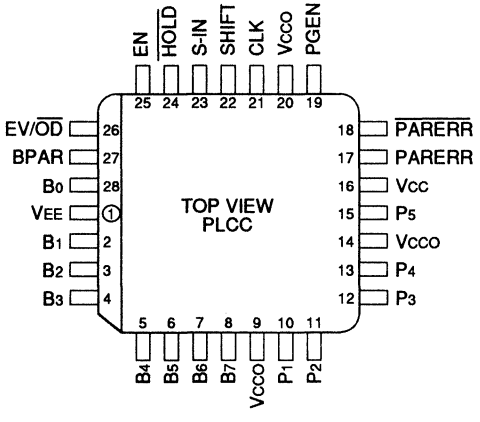
The SY10E193 and SY100E193 are error detection and correction (EDAC) circuits designed for use in new, high-performance ECL systems. The E193 generates hamming parity codes on an 8-bit word as shown in the block diagram. The P_5 output gives the parity of the whole word. PGEN provides word parity after Odd/Even parity control and gating with the BPAR input. PGEN also feeds into a 1-bit shiftable register for use as part of a scan ring.

The combinatorial part of the device generates the same code pattern as the Motorola MC10193.

Used in conjunction with 12-bit parity generators, such as the E160, a SECDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

4

PIN CONFIGURATION

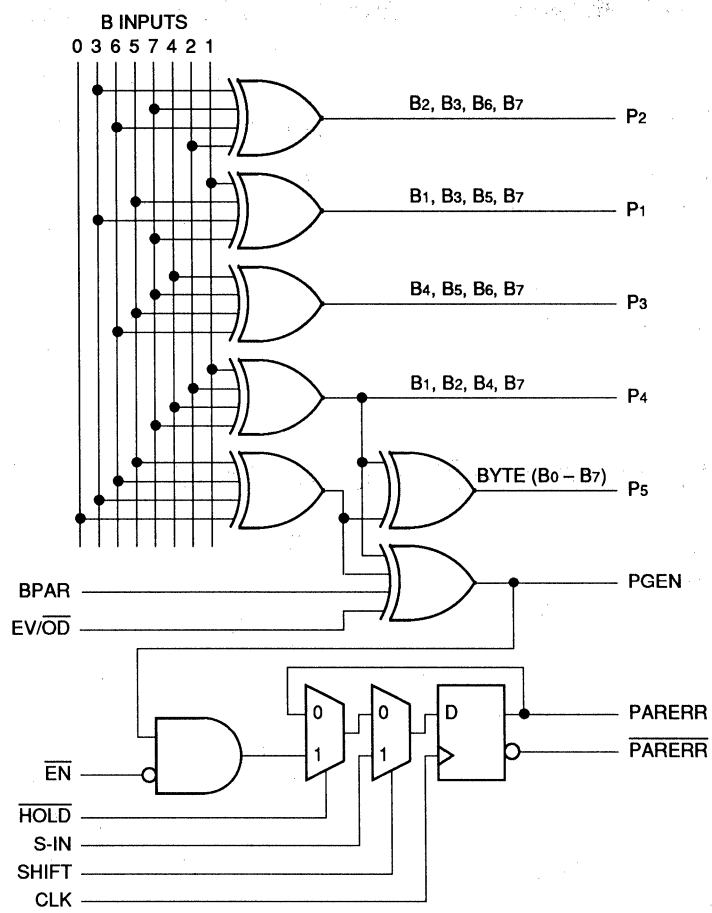


PIN NAMES

Pin	Function
B_0–B_7	Check Bit Inputs
BPAR	Check Bit Parity Input
EV/$\overline{OD}$	Even/Odd Parity Select
$\overline{EN}$	Parity Enable
$\overline{HOLD}$	Syndrome Hold Input
S-IN	Syndrome Bit Input
SHIFT	Syndrome Bit Shift
CLK	Clock Input
P_1–P_5	Parity Output
PGEN	Parity Generate Output
PARERR/$\overline{PARERR}$	Parity Error Output

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	112	134	—	112	134	—	112	134		
	100E	—	112	134	—	112	134	—	129	155		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	B to P_1, P_2, P_3, P_4	350	700	1000	350	700	1000	350	700	1000		
	B to P5	400	775	1150	400	775	1150	400	775	1150		
	EV/$\overline{OD}$, BPAR to PGEN	350	650	850	350	650	850	350	650	850		
	B to PGEN	600	1000	1450	600	1000	1450	600	1000	1450		
	CLK to PARERR	300	550	850	300	550	850	300	550	850		
t_S	Set-up Time										ps	—
	SHIFT	400	150	—	400	150	—	400	150	—		
	S-IN	300	50	—	300	50	—	300	50	—		
	$\overline{HOLD}$	750	350	—	750	350	—	750	350	—		
	$\overline{EN}$	500	250	—	500	250	—	500	250	—		
	EV/$\overline{OD}$	1300	850	—	1300	850	—	1300	850	—		
	BPAR	1300	850	—	1300	850	—	1300	850	—		
	B	1700	1100	—	1700	1100	—	1700	1100	—		
t_h	Hold Time										ps	—
	SHIFT	200	–150	—	200	–150	—	200	–150	—		
	S-IN	300	–50	—	300	–50	—	300	–50	—		
	$\overline{HOLD}$	100	–350	—	100	–350	—	100	–350	—		
	$\overline{EN}$	100	–250	—	100	–250	—	100	–250	—		
	EV/$\overline{OD}$	–200	–850	—	–200	–850	—	–200	–850	—		
	BPAR	–200	–850	—	–200	–850	—	–200	–850	—		
	B	–300	–1100	—	–300	–1100	—	–300	–1100	—		
t_r	Rise/Fall Time	300	700	1100	300	700	1100	300	700	1100	ps	—
t_f	20% to 80%											

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E193JC	J28-1	Commercial
SY100E193JC	J28-1	Commercial

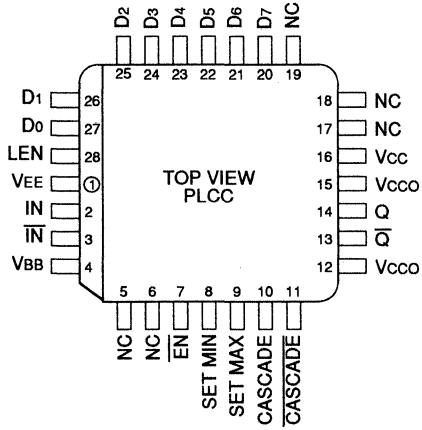
PROGRAMMABLE DELAY CHIP

ClockWorks™
SY10E195
SY100E195

FEATURES

- **Up to 2ns delay range**
- **≈20ps/digital step resolution**
- **>1GHz bandwidth**
- **On-chip cascade circuitry**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E195**

PIN CONFIGURATION



DESCRIPTION

The SY10/100E195 are programmable delay chips (PDCs) designed primarily for clock de-skewing and timing adjustment. They provide variable delay of a differential ECL input transition.

The delay section consists of a chain of gates organized as shown in the logic diagram. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80ps. These two elements provide the E195 with a digitally-selectable resolution of approximately 20ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on-chip by a high signal on the latch enable (LEN) control.

Because the delay programmability of the E195 is achieved by purely differential ECL gate delays, the device will operate at frequencies of >1GHz, while maintaining over 600mV of output swing.

The E195 thus offers very fine resolution, at very high frequencies, selectable entirely from a digital input, allowing for very accurate system clock timing.

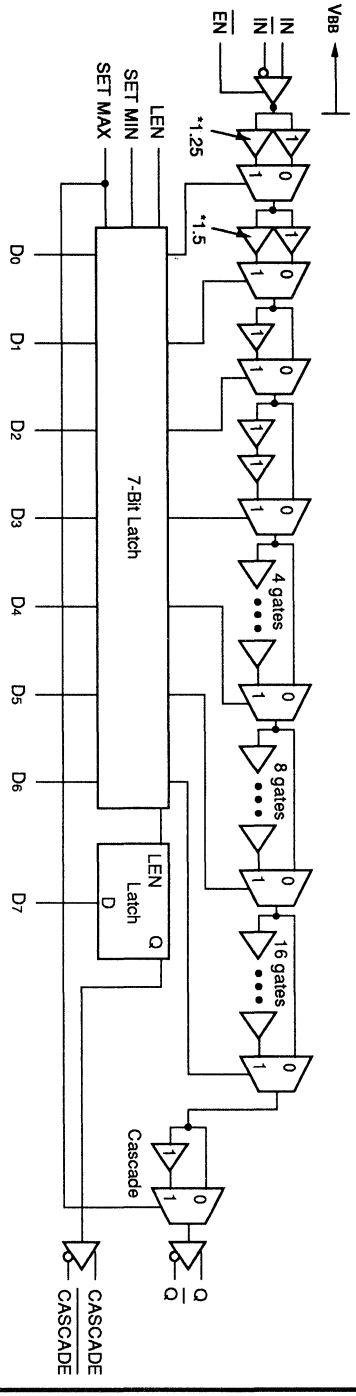
An eighth latched input, D7, is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Minimum Delay Set
SET MAX	Maximum Delay Set
CASCADE	Cascade Signal

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



*Delays are 25% or 50% longer than standard (standard = 80ps).

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	130	156	—	130	156	—	130	156		
	100E	—	130	156	—	130	156	—	150	179		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765	ps	—
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D_7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range t_{PD} (max.) – t_{PD} (min.)	2000	2175	—	2050	2240	—	2375	2580	—	ps	—
Δt	Step Delay										ps	6
	D_0 High	—	17	—	—	17.5	—	—	21	—		
	D_1 High	—	34	—	—	35	—	—	42	—		
	D_2 High	55	68	105	55	70	105	65	84	120		
	D_3 High	115	136	180	115	140	180	140	168	205		
	D_4 High	250	272	325	250	280	325	305	336	380		
	D_5 High	505	544	620	515	560	620	620	672	740		
	D_6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D_1	D_0	—	D_1	D_0	—	D_1	D_0	—	—	7
t_{SKEW}	Duty Cycle Skew, t_{PHL}–t_{PLH}	—	±30	—	—	±30	—	—	±30	—	ps	1
t_S	Set-up Time										ps	
	D to LEN	200	0	—	200	0	—	200	0	—		
	D to IN	800	—	—	800	—	—	800	—	—		2
	EN to IN	200	—	—	200	—	—	200	—	—		3
t_H	Hold Time										ps	
	LEN to D	500	250	—	500	250	—	500	250	—		
	IN to $\overline{EN}$	0	—	—	0	—	—	0	—	—		4
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300	—	—	300	—	—	300	—	—		5
	SET MAX to LEN	800	—	—	800	—	—	800	—	—		
	SET MIN to LEN	800	—	—	800	—	—	800	—	—		
t_{jit}	Jitter	—	<5	—	—	<5	—	—	<5	—	ps	8
t_r t_f	Rise/Fall Times 20–80% (Q)	125	225	325	125	225	325	125	225	325	ps	—
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650		

NOTES:

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This set-up time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D_0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs D_n). Typically, the device will be monotonic to the D_0 input, however, under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D_0 input is the LSB. With the D_1 input as the LSB, the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

APPLICATIONS INFORMATION

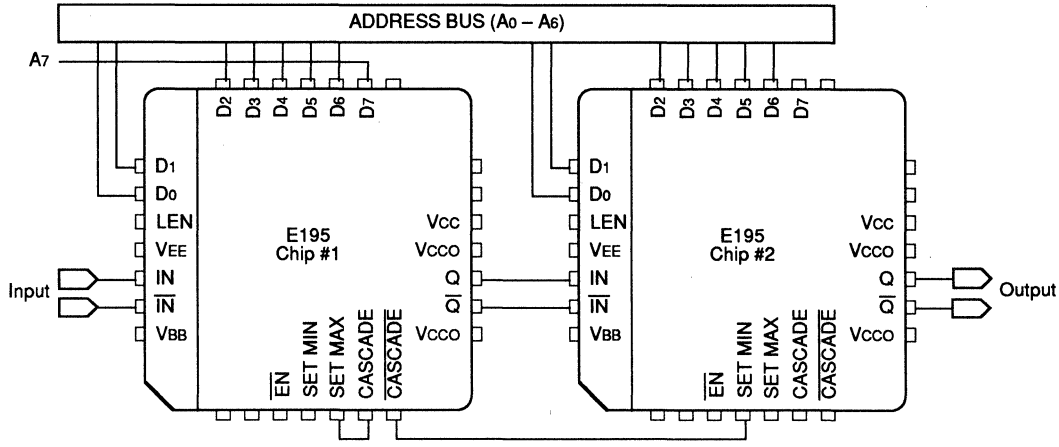


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E195s

To increase the programmable range of the E195, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195s without the need for any external gating. Furthermore, this capability requires only one more address line per added E195. Obviously, cascading multiple PDCs will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195s. As can be seen, this scheme can easily be expanded for larger E195 chains. The D_7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1, when D_7 is asserted, it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D_7 of chip #1 above is low, the cascade output will also be low, while the cascade bar output will be a logical high. In this condition, the SET MIN pin of chip #2 will be asserted and, thus, all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding, any changes on the A_0–A_6 address bus will not affect the operation of chip #2.

Chip #1, on the other hand, will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A_0–A_6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A_0–A_6 address bus), D_7 will be asserted to signal the need to cascade the delay to the next E195 device. When D_7 is asserted, the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A_0–A_6 address bus. Chip #1, on the other hand, will have its SET MAX pin asserted, resulting in the device delay to be independent of the A_0–A_6 address bus.

When the SET MAX pin of chip #1 is asserted, the D_0 and D_1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity, an additional gate delay is selected in the cascade circuitry. As a result, when D_7 of chip #1 is asserted, the delay increases from 31.75 gates to 32 gates. A 32-gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices, one simply needs to connect the D_7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

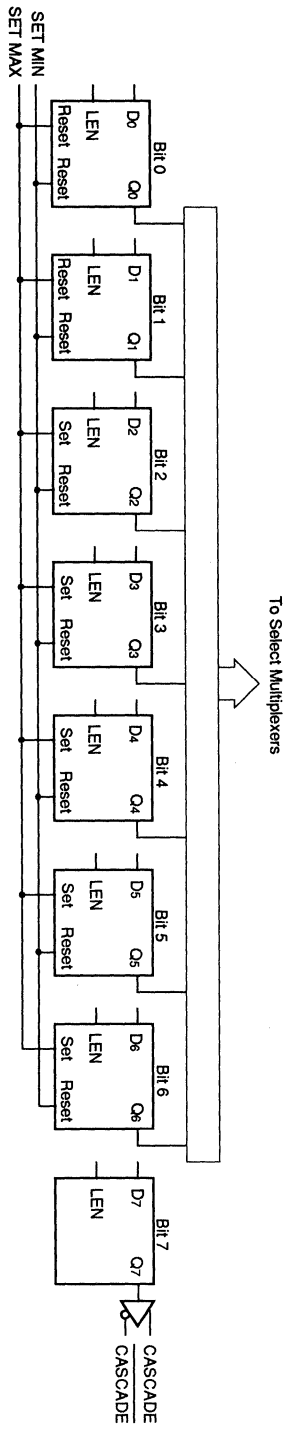


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E195JC	J28-1	Commercial
SY100E195JC	J28-1	Commercial

4

FEATURES

- **Up to 2ns delay range**
- **≈20ps digital step resolution**
- **Linear input for tighter resolution**
- **>1GHz bandwidth**
- **On-chip cascade circuitry**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E196**

DESCRIPTION

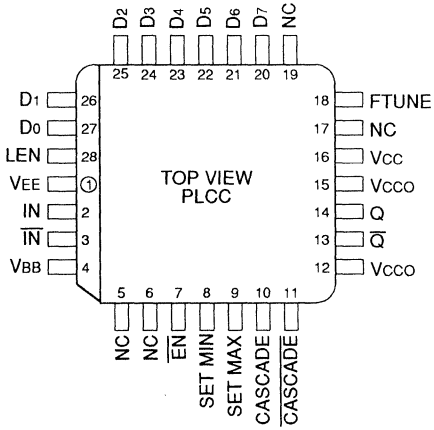
The SY10/100E196 are programmable delay chips (PDCs) designed primarily for very accurate differential ECL input edge placement applications.

The delay section consists of a chain of gates and a linear ramp delay adjustment organized as shown in the logic diagram. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80ps. These two elements provide the E196 with a digitally-selectable resolution of approximately 20ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on-chip by a high signal on the latch enable (LEN) control.

The FTUNE input takes an analog voltage and applies it to an internal linear ramp for reducing the 20s resolution still further. The FTUNE input is what differentiates the E196 from the E195.

An eighth latched input, D7, is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

PIN CONFIGURATION



PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Minimum Delay Set
SET MAX	Maximum Delay Set
CASCADE	Cascade Signal
FTUNE	Linear Voltage Input

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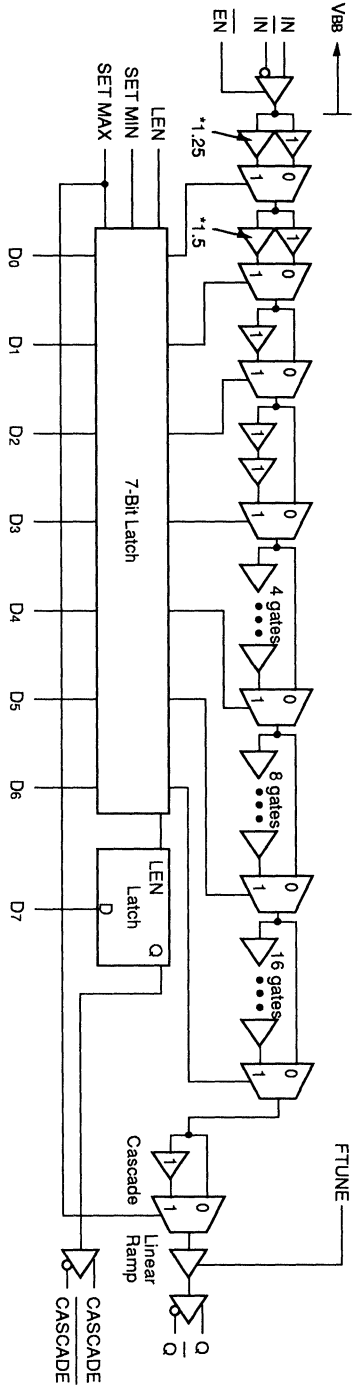
Issue Date: February, 1994

BLOCK DIAGRAM



*Delays are 25% or 50% longer than standard (standard = 80ps).

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	130	156	—	130	156	—	130	156		
	100E	—	130	156	—	130	156	—	150	179		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

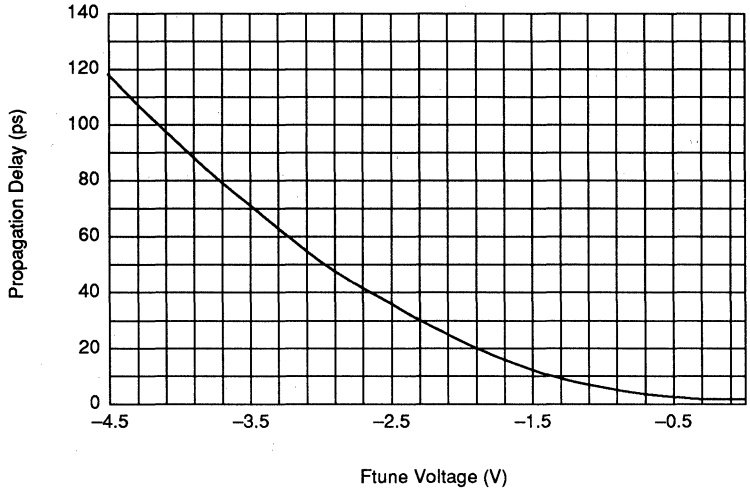
Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output IN to Q; Tap = 0 IN to Q; Tap = 127 $\overline{EN}$ to Q; Tap = 0 D_7 to CASCADE	 1210 3320 1250 300	 1360 3570 1450 450	 1510 3820 1650 700	 1240 3380 1275 300	 1390 3630 1475 450	 1540 3880 1675 700	 1440 3920 1350 300	 1590 4270 1650 450	 1765 4720 1950 700	ps	—
t_{RANGE}	Programmable Range t_{PD} (max.) – t_{PD} (min.)	2000	2175	—	2050	2240	—	2375	2580	—	ps	—
Δt	Step Delay D_0 High D_1 High D_2 High D_3 High D_4 High D_5 High D_6 High	 — — 55 115 250 505 1000	 17 34 68 136 272 544 1088	 — — 105 180 325 620 1190	 — — 55 115 250 515 1030	 17.5 35 70 140 280 560 1120	 — — 105 180 325 620 1220	 — — 65 140 305 620 1240	 21 42 84 168 336 672 1344	 — — 120 205 380 740 1450	ps	6
Lin	Linearity	D_1	D_0	—	D_1	D_0	—	D_1	D_0	—	—	7
t_{SKEW}	Duty Cycle Skew, t_{PHL}–t_{PLH}	—	±30	—	—	±30	—	—	±30	—	ps	1
t_s	Set-up Time D to LEN D to IN EN to IN	 200 800 200	 0 — —	 — — —	 200 800 200	 0 — —	 — — —	 200 800 200	 0 — —	 — — —	ps	 2 3
t_h	Hold Time LEN to D IN to $\overline{EN}$	 500 0	 250 —	 — —	 500 0	 250 —	 — —	 500 0	 250 —	 — —	ps	 4
t_R	Release Time $\overline{EN}$ to IN SET MAX to LEN SET MIN to LEN	 300 800 800	 — — —	 — — —	 300 800 800	 — — —	 — — —	 300 800 800	 — — —	 — — —	ps	 5
t_{jit}	Jitter	—	<5	—	—	<5	—	—	<5	—	ps	8
t_r t_f	Rise/Fall Times 20–80% (Q) 20–80% (CASCADE)	 125 300	 225 450	 325 650	 125 300	 225 450	 325 650	 125 300	 225 450	 325 650	ps	—

NOTES:

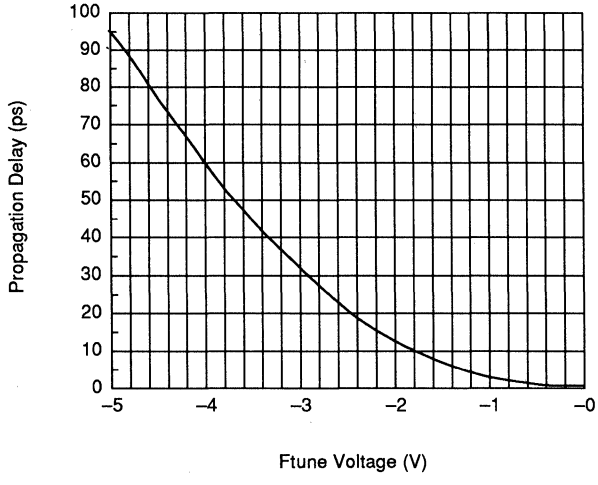
1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This set-up time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D_0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs D_n). Typically, the device will be monotonic to the D_0 input, however, under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D_0 input is the LSB. With the D_1 input as the LSB, the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

APPLICATIONS INFORMATION

Analog Input Charateristics: Ftune = VCC to VEE



Propagation Delay vs Ftune Voltage (100E196)



Propagation Delay vs Ftune Voltage (10E196)

Using the FTUNE Analog Input

The analog FTUNE pin on the E196 device is intended to enhance the 20ps resolution capabilities of the fully digital E195. The level of resolution obtained is dependent on the number of increments applied to the appropriate range on the FTUNE pin.

To provide another level of resolution, the FTUNE pin must be capable of adjusting the delay by greater than the 20ps digital resolution. As shown in the provided graphs, this requirement is easily achieved since a 100ps delay can be achieved over the entire FTUNE voltage range.This extra analog range ensures that the FTUNE pin will be capable, even under worst case conditions, of covering the digital resolution.

Typically, the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, the graphs provided should be used. As an example, if a range of 40ps is selected to cover worst case conditions and ensure coverage of the digital range, from the 100E196 graph a voltage range of –3.25V to –4V would be necessary on the FTUNE pin. Obviously, there are numerous voltage ranges which can be used to cover a given delay range. Users are given the flexibility to determine which one best fits their design.

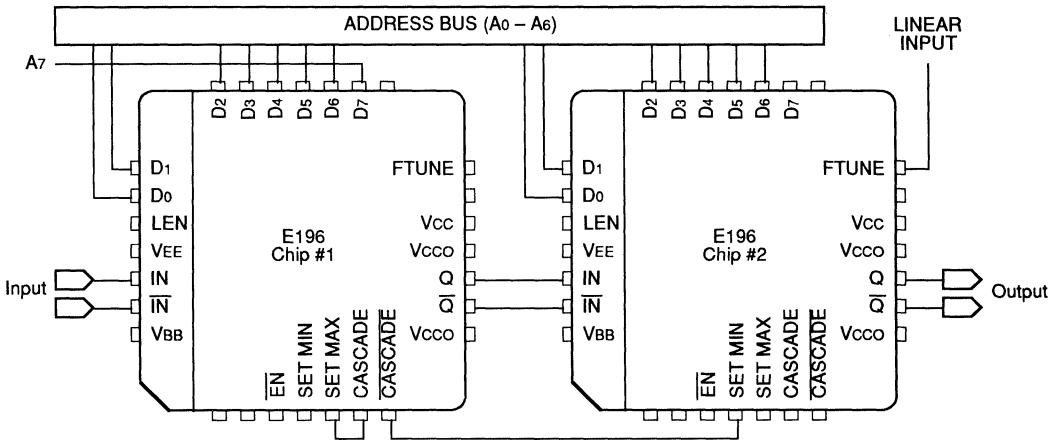


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E196s

To increase the programmable range of the E196, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E196s without the need for any external gating. Furthermore, this capability requires only one more address line per added E196. Obviously, cascading multiple PDCs will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E196s. As can be seen, this scheme can easily be expanded for larger E196 chains. The D7 input of the E196 is the cascade control pin. With the interconnect scheme of Figure 1, when D7 is asserted, it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low, the cascade output will also be low, while the cascade bar output will be a logical high. In this condition, the SET MIN pin of chip #2 will be asserted and, thus, all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding, any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1, on the other hand, will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate

delays (1111111 on the A_0–A_6 address bus), D_7 will be asserted to signal the need to cascade the delay to the next E196 device. When D_7 is asserted, the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A_0–A_6 address bus. Chip #1, on the other hand, will have its SET MAX pin asserted, resulting in the device delay to be independent of the A_0–A_6 address bus.

When the SET MAX pin of chip #1 is asserted, the D_0 and D_1 latches will be reset, while the rest of the latches will be set. In addition, to maintain monotonicity, an additional gate delay is selected in the cascade circuitry. As a result, when D_7 of chip #1 is asserted, the delay increases from 31.75 gates to 32 gates. A 32-gate delay is the maximum delay setting for the E196.

When cascading multiple PDCs, it will prove more cost-effective to use a single E196 for the MSB of the chain, while using E195 for the lower order bits. This is due to the fact that only one fine tune input is needed to further reduce the delay step resolution.

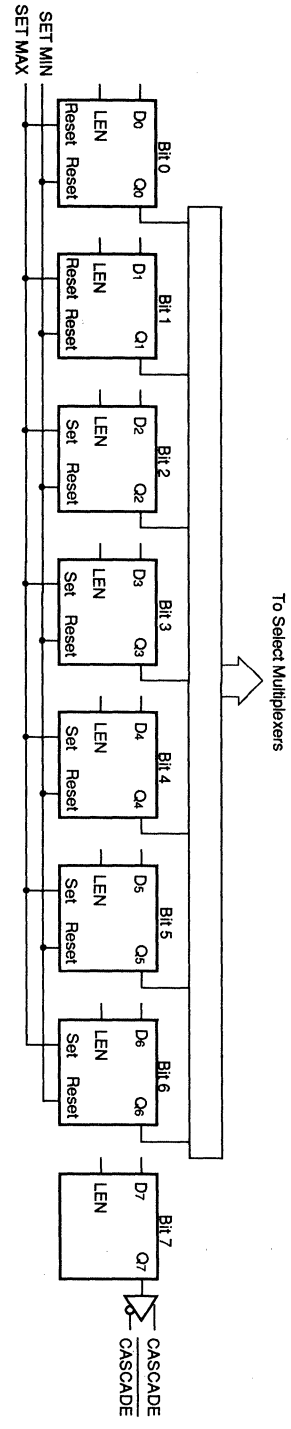


Figure 2. Expansion of the Latch Section of the E196 Block Diagram

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E196JC	J28-1	Commercial
SY100E196JC	J28-1	Commercial

FEATURES

- **2:7 and 1:7 RLL format-compatible**
- **Fully integrated VCO for 50Mb/s operation**
- **External VCO input for higher operating frequency**
- **Anti-equivocation circuitry to ensure PLL lock**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E197**

DESCRIPTION

The SY10E197 is an integrated data separator designed for use in high-speed hard disk drive applications. With data rate capabilities of up to 50Mb/s, the device is ideally suited for today's and future state-of-the-art hard disk designs.

The E197 is typically driven by a pulse detector which reads the magnetic information from the storage disk and changes it into ECL pulses. The device is capable of operating on both 2:7 and 1:7 RLL coding schemes. Note that the E197 does not do any decoding, but rather prepares the disk data for decoding by another device.

For applications with higher data rate needs, such as tape drive systems, the device accepts an external VCO. The frequency capability of the integrated VCO is the factor which limits the device to 50Mb/s.

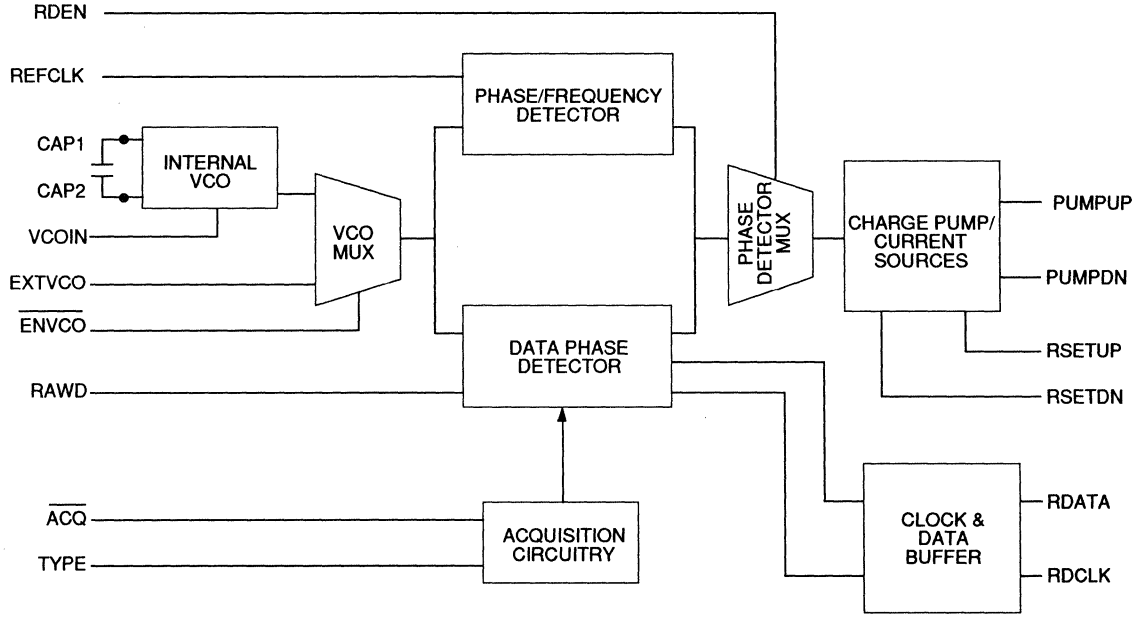
A special anti-equivocation circuit has been employed to ensure timely lock-up when the arriving data and VCO edges are coincident.

Unlike the majority of the devices in the ECLinPS™ family, the E197 is available in only 10KH-compatible ECL. The device is available in the standard 28-lead PLCC.

Since the E197 contains both analog and digital circuitry, separate supply and ground pins have been provided to minimize noise coupling inside the device. The device can operate on either standard negative ECL supplies or, as is more common, on positive voltage supplies.

4

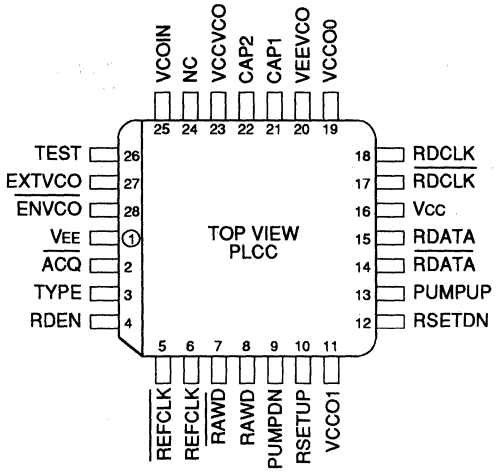
BLOCK DIAGRAM



ASSET is a trademark of Synergy Semiconductor Corporation.
ECLinPS is a trademark of Motorola Inc.

Rev.: B Amendment: /0
Issue Date: February, 1994

PIN CONFIGURATION



PIN NAMES

Pin	Function
REFCLK	Reference clock equivalent to one clock cycle per decoding window.
RDEN	Enable data synchronizer when HIGH. When LOW, enable the phase/frequency detector steered by REFCLK.
RAWD	Data input to synchronizer logic.
VCOIN	VCO control voltage input.
CAP1/CAP2	VCO frequency controlling capacitor inputs.
$\overline{\text{ENVCO}}$	VCO select pin. LOW selects the internal VCO and HIGH selects the external VCO input. Pin floats LOW when left open.
EXTVCO	External VCO pin selected when ENVCO is HIGH.
$\overline{\text{ACQ}}$	Acquisition circuitry select pin. This pin must be driven HIGH at the end of the data sync field for some sync field types.
TYPE	Selects between the two types of commonly used sync fields. When LOW, it selects a sync field interspersed with 3 zeroes (2:7 RLL code). When HIGH, it selects a sync field interspersed with 2 zeroes (1:7 RLL code).
TEST	Input included to initialize the clock flip-flop for test purposes only. Pin should be left open (LOW) in actual application.
PUMPUP	Open collector charge pump output for the signal pump.
PUMPDN	Open collector charge pump output for the reference pump.
RSETUP	Current setting resistor for the signal pump.
RSETDN	Current setting resistor for the reference pump.
RDATA	Synchronized data output.
RDCLK	Synchronized clock output.
VCC, VCCO, VCCVCO	Most positive supply rails. Digital and analog supplies are independent on chip.
VEE, VEEVCO	Most negative supply rails. Digital and analog supplies are independent on chip.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE}(Min.) to V_{EE}(Max.); V_{CC} = GND or V_{CC} = +4.75V to +5.25V; V_{EE} = GND

		0°C			+25°C			+85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{IH}	Input HIGH Current[1]	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current[1]	0.5	—	—	0.5	—	—	0.5	—	—	µA
I_{EE}	Power Supply Current	90	—	180	90	—	180	90	—	180	mA
I_{SET}	Charge Pump Bias Current[2]	0.5	—	5	0.5	—	5	0.5	—	5	mA
I_{OUT}	Charge Pump Output Leakage Current[3]	—	—	1	—	—	1	—	—	1	µA
V_{ACT}	PUMPUP/PUMPDN Active Voltage Range	V_{CC}-2.5	—	V_{CC}	V_{CC}-2.5	—	V_{CC}	V_{CC}-2.5	—	V_{CC}	V

NOTES:

1. Applies to the input current for each input except VCOIN.
2. For a nominal set current of 3.72mA, the resistor values for RSETUP and RSETDN should be 130Ω (0.1%). Assuming no variation between these two resistors, the current match between the PUMPUP and PUMPDN output signals should be within ±3%. I_{SET} is calculated as (V_{EE} + 1.3V – V_{BE})/R; where R is RSETUP or RSETDN and a nominal value for V_{BE} is 0.85 volts.
3. Output leadkage current of the PUMPUP or PUMPDN output signals when at a LOW level.

4

10KH LOGIC LEVELS DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE}(Min.) to V_{EE}(Max.); V_{CC} = V_{CCO} = V_{CCO1} = V_{CCVCO} = GND

		0°C			+25°C			+85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OH}	Output HIGH Voltage	–1020	—	–840	–980	—	–810	–910	—	–720	mV
V_{OL}	Output LOW Voltage	–1950	—	–1630	–1950	—	–1630	–1950	—	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	—	–840	–1130	—	–810	–1060	—	–720	mV
V_{IL}	Input LOW Voltage	–1950	—	–1480	–1950	—	–1480	–1950	—	–1445	mV

POSITIVE ECL LEVELS DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EEVCO} = GND; V_{CC} = V_{CCO0} = V_{CCO1} = V_{CCVCO} = +5V[1]

		0°C			+25°C			+85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OH}	Output HIGH Voltage	3980	—	4160	4020	—	4190	4090	—	4280	mV
V_{OL}	Output LOW Voltage	3050	—	3370	3050	—	3370	3050	—	3405	mV
V_{IH}	Input HIGH Voltage	3830	—	4160	3870	—	4190	3940	—	4280	mV
V_{IL}	Input LOW Voltage	3050	—	3520	3050	—	3050	3050	—	3555	mV

NOTE:

1. V_{OH} and V_{OL} levels will vary 1:1 with V_{CC}.

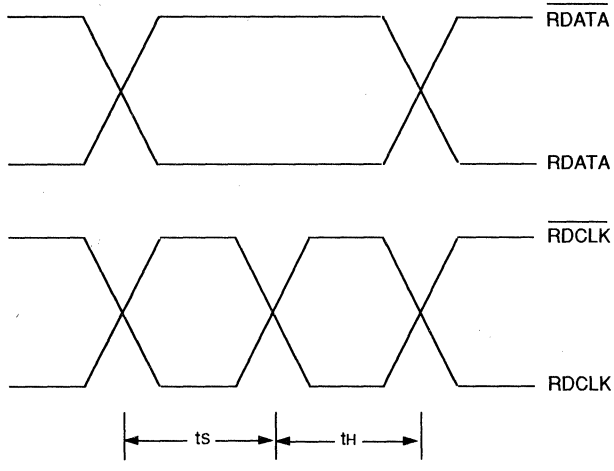
AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE}(Min.) to V_{EE}(Max.); V_{CC} = GND or V_{CC} = +4.75V to +5.25V; V_{EE} = GND

Symbol	Parameter	0°C		+25°C		+85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Time from RDATA Valid to Rising Edge of RDCLK[1,2]	t_{VCO}-500	—	t_{VCO}-500	—	t_{VCO}-500	—	ps
t_H	Time from Rising Edge of RDCLK to RDATA Invalid[1,2]	t_{VCO}	—	t_{VCO}	—	t_{VCO}	—	ps
t_{SKEW}	Skew Between RDATA and $\overline{\text{RDATA}}$	—	300	—	300	—	300	ps
f_{VCO}	Frequency of the VCO[3]	150	—	150	—	150	—	MHz
	Tuning Ratio[4]	1.53	1.87	1.53	1.87	1.53	1.87	

NOTES:

1. t_{VCO} is the period of the VCO.
2. Refer to set-up and hold timing diagrams below.
3. The VCO frequency determined with VCOIN = V_{EE} + 0.5V and using a 10pF tuning capacitor.
4. The tuning ratio is defined as the ratio of f_{VCOMAX} to f_{VCOMIN}, where f_{VCOMIN} is measured at VCOIN = 1.3V + V_{EE} and f_{VCOMAX} is measured at VCOIN = 2.6V + V_{EE}.



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E197JC	J28-1	Commercial
SY100E197JC	J28-1	Commercial

APPLICATIONS INFORMATION

GENERAL OPERATION

Operation

The E197 is a phase-locked loop circuit consisting of an internal VCO, a Data Phase detector with associated acquisition circuitry, and a Phase/Frequency detector (Figure 1). In addition, an enable pin ($\overline{ENVCO}$) is provided to disable the internal VCO and enable the external VCO input. Hence, the user has the option of supplying the VCO signal.

The E197 contains two phase detectors: a data phase detector for synchronizing to the non-periodic pulses in the read data stream during the data read mode of operation, and a phase/frequency detector for frequency (and phase) locking to an external reference clock during the "idle" mode of operation. The read enable (RDEN) pin muxes between these two detectors.

Data Read Mode

The data pins (RAWD) are enabled when the RDEN pin is placed at a logic HIGH level, thus enabling the Data Phase detector (Figure 1) and initiating the data read mode. In this mode, the loop is servoed by the timing information taken from the positive edges of the input data pulses. This phase detector samples positive edges from the RAWD signal and generates both a pump up and pump down pulse from any edge of the input data pulse. The leading edge of the pump up pulse is time modulated by the leading edge of the data signal, whereas the rising edge of the pump up pulse is generated synchronous to the VCO clock. The falling edge of the pump down pulse is synchronous to the rising edge of the VCO clock and the rising edge of the pump down signal is synchronous to the falling edge of the VCO clock. Since both edges of the VCO are used, it generates an internal clock duty cycle of 50%. This pulse width modulation technique is used to generate the servoing signal which drives the VCO. The pump down signal is a reference pulse which is included to provide an evenly balanced differential system, thereby allowing the synthesis of a VCO input control signal after appropriate signal processing by the loop filter.

By using suitable external filter circuitry, a control signal for input into the VCO can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when the data edges lead the clock by a half clock cycle. If the data edges are advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a negative polarity; whereas, if the VCO is advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a positive polarity. If there is no data edge present at the RAWD input, the corresponding pump up and pump down outputs are not generated and the resulting control output is zero.

Acquisition Circuitry

The acquisition circuitry is provided to assist the data phase detector in phase locking to the sync field that precedes the data. For the case in which lock-up is attempted when the data edges are coincident with the VCO edges, the pump down signal may enter an indeterminate state for an unacceptably long period due to the violation of internal set-up and hold times. After an initial pump down pulse, the circuit blocks successive pump down pulses and inserts extra pump up pulses during portions of the sync field that are known to contain zeroes. Thus, the data phase detector is forced to have a non-zero output during the lock-up period and the restoring force ensures correction of the loop within an acceptable time. Hence, this circuitry provides a quasi-deterministic pump down output signal under the condition of coincident data and VCO edges, allowing lock-up to occur without excessive delays.

The $\overline{ACQ}$ line is provided to disable (disable = HIGH) the acquisition circuit during the data portion of a sector block. Typically, this circuit is enabled at the beginning of the sync field by a one-shot timer to ensure a timely lock-up.

The TYPE line allows the choice between two sync field preamble types: transitions interspersed with two zeroes between transitions, or three zeroes between transitions. These types of sync fields are used with the 1:7 and 2:7 RLL coding schemes, respectively.

Idle Mode

In the absence of data, or when the drive is writing to the disk, PLL servoing is accomplished by pulling the read enable line (RDEN) low and providing a reference clock via the REFCLK pins. The condition whereby RDEN is low selects the Phase/Frequency detector (Figure 1) and the E197 is said to be operating in the "idle mode." In order to function as a frequency detector, the input waveform must be periodic. The pump up and pump down pulses from the Phase/Frequency detector will have the same frequency, phase and pulse width only when the two clocks that are being compared have their positive edges aligned and are of the same frequency.

As with the data phase detector, by using suitable external filter circuitry, a VCO input control signal can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when all positive edges of both clocks are coincident. For the case in which the frequencies of the two clocks are the same but the clock edges of the reference clock are slightly advanced with respect to the VCO clock, the control signal is defined to have a positive polarity. A control signal with negative polarity occurs when the edges of the reference clock are delayed with respect to those of the VCO. If the frequencies of the two clocks are different, the clock with the most edges per unit time will initiate the most pulses and the polarity of the detector will reflect the frequency error. Thus, when the reference clock is higher in frequency than the VCO clock, the polarity of the control signal is positive; whereas a control signal with negative polarity occurs when the frequency of the reference clock is lower than the VCO clock.

APPLICATIONS INFORMATION (CONTINUED)

PHASE LOCK LOOP THEORY

Introduction

Phase lock loop (PLL) circuits are fundamentally feedback systems used to synchronize the frequency of an oscillator to an incoming signal. In addition to frequency synchronization, the PLL circuitry is designed to minimize the phase difference between the system input and output signals. A block diagram of a feedback control system is shown in Figure 1.

Where:

A(s) is the product of the feed-forward transfer functions.

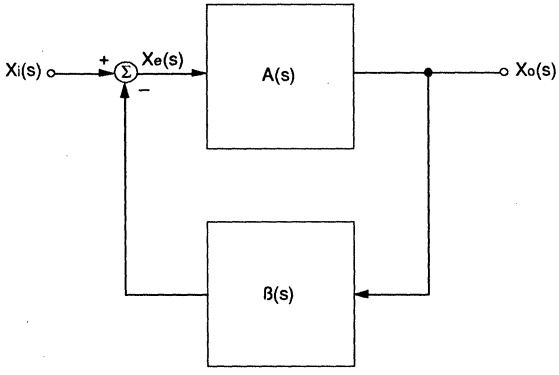


Figure 1. Feedback System

ß(s) is the product of the feedback transfer functions.

The transfer function for this closed loop system is

$$\frac{XO(s)}{Xi(s)} = \frac{A(s)}{1 + A(s)ß(s)}$$

Typically, phase lock loops are modeled as feedback systems connected in a unity feedback configuration (ß(s)=1) with a phase detector, a VCO (voltage controlled oscillator) and a loop filter in the feed-forward path, A(s). Figure 2 illustrates a phase lock loop as a feedback control system in block diagram form.

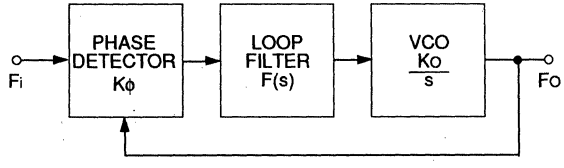


Figure 2. Phase Lock Loop Block Diagram

The closed loop transfer function is:

$$\frac{Xo(s)}{Xi(s)} = \frac{K\phi \frac{Ko}{s} F(s)}{1 + K\phi \frac{Ko}{s} F(s)}$$

where:

Kϕ = the phase detector gain.
KO = the VCO gain. Since the VCO introduces a pole at the origin of the s-plane, KO is divided by s.
F(s) - the transfer function of the loop filter.

The 10E197 is designed to implement the phase detector and VCO functions in a unity feedback loop, while allowing the user to select the desired filter function.

Gain Constants

As mentioned, each of the three sections in the phase lock loop block diagram has an associated open loop gain constant. Further, the gain constant of the filter circuitry is composed of the product of three gain constants, one for each filter subsection. The open loop gain constant of the feed-forward path is given by

$$KOl = K\phi * KO * K1 * KI * Kd \qquad \text{eqt. 1}$$

and obtained by performing a root locus analysis.

Phase Detector Gain Constant

The gain of the phase detector is a function of the operating mode and the data pattern. The 10E197 provides data separation for signals encoded in 2:7 or 1:7 RLL encoding schemes; hence Tables 1 and 2 are coding tables for these schemes. Table 3 lists nominal phase detector gains for both 2:7 and 1:7 sync fields.

NRZ Data Sequence	Code Sequence
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Table 1. 2:7 RLL Encoding Table

APPLICATIONS INFORMATION (CONTINUED)

NRZ Data Sequence	Code Sequence
00	X01
01	010
10	X00
1100	010001
1101	X00000
1110	X00001
1111	010000

An X in the leading bit of a code sequence is assigned the complement of the bit.

Table 2. 1:7 RLL Encldng Table

Sync Pattern	Read Mode	Idle Mode
2:7	121mV/radian	484mV/radian
1:7	161mV/radian	483mV/radian

Table 3. Phase Detector Gain Constants

VCO Gain Constant

The gain of the VCO is a function of the tuning capacitor. For a value of 10pF, a nominal value of the gain, K_o, is 20MHz per volt.

Filter Circuitry Gain Constant(s)

The open loop gain constant of the filter circuitry is given by:

$$K_{fc} = K_1 * K_I * K_d \qquad \text{eqt. 2}$$

The individual gain constants are defined in the appropriate subsections of this document.

Loop Filter

The two major functions of the loop filter are to remove any noise or high frequency components present in the phase detector output signal and, more importantly, to control the characteristics which determine the dynamic response of the phase lock loop, i.e. capture range, loop bandwidth, capture time and transient response.

Although a variety of loop filter configurations exist, this section will only describe a filter capable of performing the signal processing as described in the Data Read Mode and the Idle Mode sections. The loop filter consists of a differential summing amplifier cascaded with an augmenting integrator which drives the VCOIN input to the 10E197 through a resistor divider network (Figure 3).

The transfer function and the element values for the loop filter are derived by dividing the filter into three cascaded subsections: filter input, augmenting integrator and the voltage divider network (Figure 4).

Loop Filter Transfer Function

The open loop transfer function of the phase lock loop is the product of each individual filter subsection,, as well as the phase detector and VCO. Thus, the open loop filter transfer function is:

where:

$$F_o(s) = K\phi * \frac{K_o}{s} * F_1(s) * F_I(s) * F_d(s)$$

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{o-1})\, s + \omega_{o-1}^2]}$$

$$F_I(s) = K_I * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{o-2})\, s + \omega_{o-2}^2]}$$

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

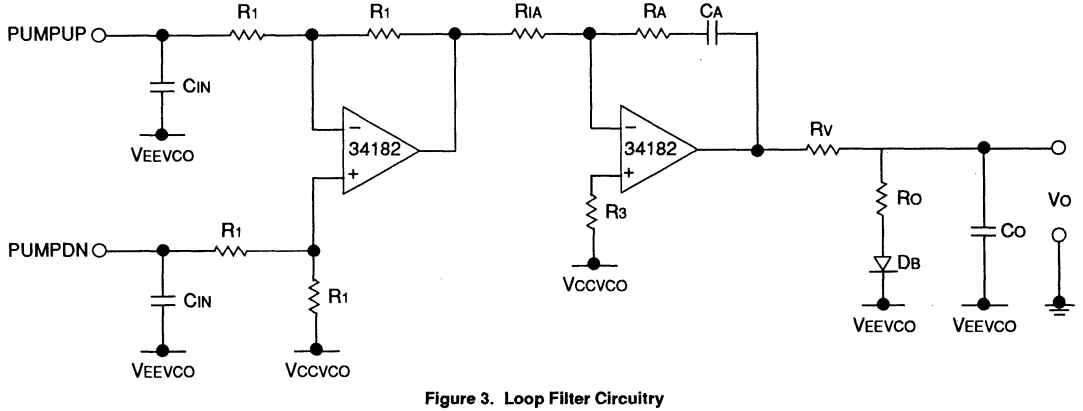


Figure 3. Loop Filter Circuitry

APPLICATIONS INFORMATION (CONTINUED)

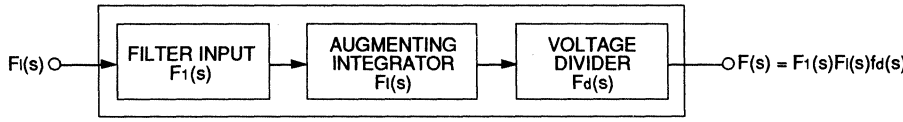


Figure 4. Loop Filter Block Diagram

A root locus analysis is performed on the open loop transfer function to determine the final pole-zero locations and the open loop gain constant for the phase lock loop. Note that the open loop gain constant impacts the crossover frequency and that a lower frequency crossover point means a much more efficient filter. Once these positions and constants are determined, the component values may be calculated.

Filter Input

The primary function of the filter input subsection is to convert the output of the phase detector into a single ended signal for subsequent processing by the integrator circuitry. This subsection consists of the 10E197 charge pump current sinks, two shunt capacitors and a differential summing amplifier (Figure 5).

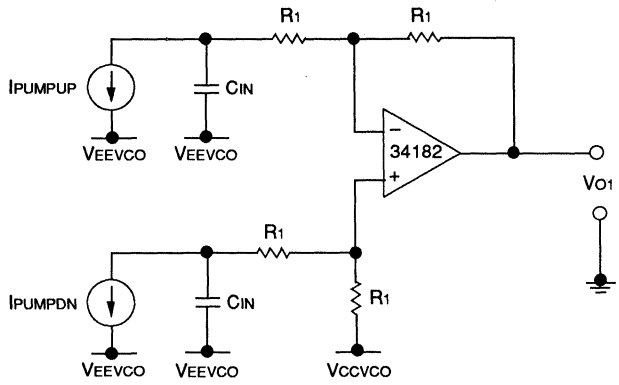


Figure 5. Filter Input Subsection

Hence, this portion of the filter circuit contributes a real pole and two complex poles to the overall loop transfer function F(s). Before these pole locations are selected, appropriate values for the current setting resistors (RSETUP and RSETDN) must be ascertained. The goal in choosing these resistor values is to maximize the gain of the filter input subsection while ensuring the charge pump output transistors operate in the active mode. The filter input gain is maximized for a charge pump current of 1.1mA; a value of 464Ω for both RSETUP and RSETDN yields a nominal charge pump current of 1.1mA.

It should be noted that a dual bandwidth implementation of the phase lock loop may be achieved by modifying the current setting resistors such that an electronic switch enables one of two resistor configurations. Figure 6 shows a circuit configuration capable of providing this dual bandwidth function. Analysis of the filter input circuitry yields the transfer function:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{o1})\, s + \omega_{o1}^2]}$$

The gain constant is defined as:

$$K_1 = A_1 * \frac{1}{C_{IN}} \qquad \text{eqt. 3}$$

where:

A_1 = op-amp gain constant for the selected pole positions.

C_{IN} = phase detector shunt capacitor.

The real pole is a function of the input resistance to the op-amp and the shunt capacitors connected to the phase detector output. For stability, the real pole must be placed beyond the unity gain frequency; hence, this pole is typically placed midway between the unity crossover and phase detector sampling frequency, which should be about ten times greater.

APPLICATIONS INFORMATION (CONTINUED)

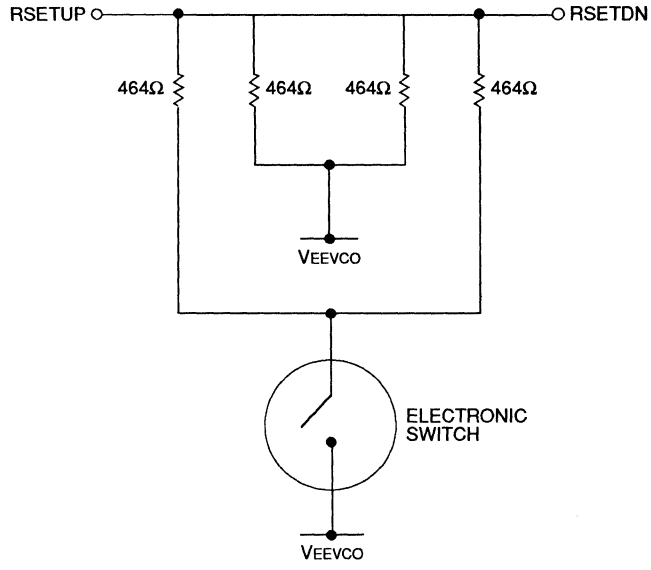


Figure 6. Dual Bandwidth Current Source Implementation

The second order pole set arises from the two pole model for an op-amp. The open loop gain and the first open loop pole for the op-amp are obtained from the data sheets. Typically, op-amp manufacturers do not provide information on the location of the second open loop pole, however it can be approximated by measuring the roll off of the op-amp in the open loop configuration. The second pole is located where the gain begins to decrease at a rate of 40dB per decade. The inclusion of both poles in the differential summing amplifier transfer function becomes important when closing the feedback path around the op-amp because the poles migrate and this migration must be accounted for to accurately determine the phase lock loop transient performance.

Typically, the op-amp poles can be approximated by a pole pair occurring as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane. Two constraints on the selection of the op-amp pole pair are that the poles lie beyond the crossover frequency and they are positioned for near unity gain operation. Performing a root locus analysis on the op-amp open loop configuration and adhering to the two constraints yields the pole positions contributed by the op-amp.

Determination of Element Values

Since the difference amplifier is configured to operate as a differential summer, the resistor values associated with the amplifier are of equal value. Further, the typical input resistance to the summing amplifier is 1KΩ; thus, the op-amp resistors are set at 1KΩ. Having set the input resistance to the op-amp and selected the position of the real pole, the value of the shunt capacitors is determined using the following relationship:

$$|p1| = \frac{1}{2\pi R1 C_{IN}} \qquad \text{eqt. 4}$$

Augmenting Integrator

The augmenting integrator consists of an active filter with a lag-lead network in the feedback path (Figure 7).

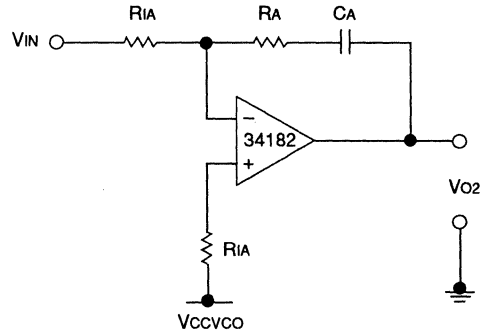


Figure 7. Integrator Subsection

APPLICATIONS INFORMATION (CONTINUED)

Analysis of this portion of the filter circuit yields the transfer function:

$$F_I(s) = K_I * \frac{1}{s} * \frac{(s+z)}{[s^2 + (2\zeta\omega_2)\, s + \omega_{o2}^2]}$$

The gain constant is defined as:

$$K_I = A_I * \frac{R_A}{R_{IA}} \qquad \text{eqt. 5}$$

where:

A_I = op-amp gain constant for selected pole positions.

R_A = integrator feedback resistor.

R_{IA} = integrator input resistor.

The integrator circuit introduces a zero, a pole at the origin and a second order pole set as described by the two pole model for an op-amp. As in the case of the differential summing amplifier, we assume the op-amp pole pair occurs as a complex conjugate pair, making an angle of 45° to the real axis of the complex frequency plane; are positioned for near unity gain operation; and are located beyond the crossover frequency. Since both the summing and integrating op-amps are realized by the same type of op-amp (34182D), the open loop pole positions for both amplifiers will be the same.

Further, the loop transfer function contains two poles located at the origin — one introduced by the integrator and the other by the VCO. Hence, a zero is necessary to compensate for the phase shift produced by these poles and ensure loop stability. The op-amp will be stable if the crossover point occurs before the transfer function phase angle becomes 180°. The zero should be positioned much less than one decade before the unity gain frequency.

As in the case of the filter input circuitry, the poles and zero from this analysis will be used as open loop poles and a zero when performing the root locus analysis for the complete system.

Determination of Element Values

The location of the zero is used to determine the element values for the augmenting integrator. The value of the capacitor, C_A, is selected to provide adequate charge storage when the loop is not sampling data. A value of 0.1µF is sufficient for most applications. This value may be increased when the RDCLK frequency is much lower than 4MHz. The value of R_A is governed by:

$$|z| = \frac{1}{2\pi R_A C_A} \qquad \text{eqt. 6}$$

For unity gain operation of the integrating op-amp, the value of R_{IA} is selected such that:

$$R_{IA} = R_A \qquad \text{eqt. 7}$$

It should be noted that, although the zero can be tuned by varying either R_A or C_A, caution must be exercised when adjusting the zero by varying C_A because the integrator gain is also a function of C_A. Further, the gain of the loop filter can be adjusted by changing the integrator input resistor R_{IA}.

Voltage Divider

The input range to the VCOIN input is from 1.3V + V_{EE} to 2.6V + V_{EE}. Hence, the output from the augmenting amplifier section must be attenuated to meet the VCOIN constraints. A simple voltage divider network provides the necessary attenuation (Figure 8).

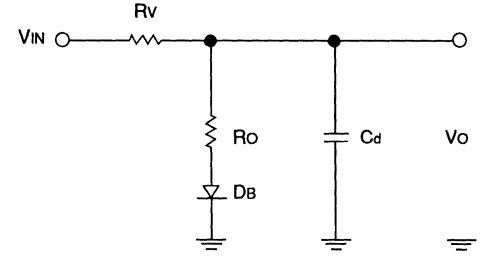


Figure 8. Voltage Divider Subsection

In addition, a shunt filter capacitor connected between the VCOIN input pin and VEE provides the voltage divider subsection with a single time constant transfer function that adds a pole to the overall loop filter. The transfer function for the voltage divider network is:

$$F_d(s) = K_d * \frac{1}{(s + P_2)}$$

The gain constant, K_d, is defined as:

$$K_d = \frac{1}{R_v C_d} \qquad \text{eqt. 9}$$

The value of K_d is easily extracted by rearranging Equation 1:

$$K_d = \frac{K_{OI}}{K_\phi * K_O * K_1 * K_I} \qquad \text{eqt. 10}$$

The gain constant, K_d, is set such that the output from the integrator circuit is within the range 1.3V + V_{EE} to 2.6V + V_{EE}. The pole for the voltage divider network should be positioned an octave beyond that for the filter input.

Determination of Element Values

Once the pole location and the gain constant, Kd, are established, the resistor values for the voltage divider network are determined using the design guidelines mentioned above and from the following relationship:

APPLICATIONS INFORMATION (CONTINUED)

$$\frac{Kd}{2\pi|P2|} = \frac{RO}{RO + RV}$$

Having determined the resistor values, the filter capacitor is calculated by rearranging Equation 9:

$$Cd = \frac{1}{RvKd} \qquad \text{eqt. 9a}$$

Finally, a bias diode is included in the voltage divider network to provide temperature compensation. The finite resistance of this diode is neglected for these calculations.

Calculations for a 2:7 Coding Scheme

Introduction

The circuit component values are calculated for a 2:7 coding scheme employing a data rate of 23 Mbit/sec. Since the number of bits is doubled when the data is encoded, the data clock is at half the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 46 MHz. Further, the pole and zero positions are a function of the data rate; hence, the component values derived by these calculations must be scaled if a different operating frequency is used. Finally, it should be noted that the values are optimized for settling time.

The analysis is divided into three parts: static pole positioning, dynamic pole positioning and dynamic zero positioning. Dynamic poles and zeroes are those which the designer may position to yield the desired dynamic response through the judicious choice of element values. Static poles are not directly controlled by the choice of component values.

Static Poles

Each op-amp introduces a pair of "static" complex conjugate poles which must lie beyond the crossover frequency. As obtained from the data sheets and laboratory measurements, the two open loop poles for the 34182D are:

$P^*1a = -0.1Hz$

$P^*1b = -11.2Hz$

Performing a root locus analysis and following the two guidelines previously stated, an acceptable pole set is:

$P1a = -5.65 + j5.65MHz$

$P1b = -5.65 - j5.65MHz$

Both op-amps introduce a set of static complex conjugate poles at these positions for a total of four poles. Further, the loop gain for each op-amp associated with these pole positions is determined from the root locus analysis to be:

$$A1 = A2 = 2.48\ e15\ \frac{V}{V}$$

In addition to the op-amps, the integrator and the VCO each contribute a static pole at the origin. Thus, there are a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$P^*1 = -1.24$ MHz

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus, the open loop voltage divider pole position is picked to be:

$P^*2 = -2.5$ 7MHz

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency. For this design, the zero is placed at:

$z = -311$ Hz

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot. If the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions, the component values are calculated. From the root locus analysis, the dynamic pole and zero positions are:

$P1 = -573$ KHz

$P2 = -3.06$ MHz

$z = -311$ Hz

Filter Input Subsection

Rearranging Equation 4:

$$CIN = \frac{1}{2\pi\ R1|P1|}$$

and substituting 573KHz for the pole position and 1KΩ for the resistor value yields:

$CIN = 278$ pF

Augmenting Integrator Subsection

Rearranging Equation 6:

$$RA = \frac{1}{2\pi\ |z|CA}$$

APPLICATIONS INFORMATION (CONTINUED)

and substituting 311 Hz for the zero position and 0.1μF for the capacitor value yields:

$R_A = 5.11\ K\Omega$

From Equation 7, the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$R_{IA} = R_A = 5.11\ K\Omega$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9 and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3V + VEE to 2.6V + VEE. Restating Equation 9,

$$K_d = \frac{K_{OI}}{K_\phi * K_O * K_1 * K_I}$$

From the root locus analysis K_{OI} is determined to be:

$$K_{OI} = 1.585\ e51\ \frac{V}{mA\ sec^3}$$

From Equation 3

$$K_I = A_I * \frac{1}{C_{IN}}$$

and the gain constant, K_1, is:

$$K_1 = 8.90\ e21\ \frac{V}{mA\ sec}$$

From Equation 5

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant, K_I, is:

$$K_1 = 2.48\ e15\ \frac{V}{V}$$

Having determined the gain constant, K_d, the value of R_V is selected such that the constraints $R_V > R_O$ and:

$$\frac{K_d}{2\pi|p_2|} = \frac{R_O}{R_O + R_V}$$

are fulfilled. The pole position, P_2, is determined from the root locus analysis to be:

$P_2 = -3.06$ MHz

Hence, R_V is selected to be:

$R_V = 2.15\ K\Omega$

and R_O is calculated to be:

$R_O = 700\ \Omega$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_V K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d, is:

$C_d = 98$ pF

Note that the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 23 Mbit/sec. If the data rate is different from the nominal design value, the reactive elements must be scaled accordingly. The following equations are provided to facilitate scaling and were derived with the assumptions that a 2:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock.

$$C_{IN} = 278 * \frac{46}{f}\ (pF) \qquad \text{eqt. 11}$$

$$C_{IN} = 98 * \frac{46}{f}\ (pF) \qquad \text{eqt. 12}$$

where f is the RDCLK frequency in MHz.

Example for an 11Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 2:7 code are used, but the data rate is 11 Mbit/sec. The dynamic pole positions and, therefore the bandwidth of the loop filter, are a function of the data rate. Thus, a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 11, the value of C_{IN} is:

$C_{IN} = 581$ pF

and from Equation 12, the value of C_d is:

$C_d = 205$ pF

$R_V = 2.15\ K\Omega$

$R_O = 700\ \Omega$

Note the poles, P_1 and P_2, are now located at:

$P_1 = -274$ KHz

$P_2 = -1.47$ MHz

APPLICATIONS INFORMATION (CONTINUED)

And, the open loop filter unity crossover point is at 300 KHz. The gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affecting the dynamic performance of the filter.

Calculations For a 1:7 Coding Scheme

Introduction

The circuit component values are calculated for a 1:7 coding scheme employing a data rate of 20 Mbit/sec. Since the number of bits increases from two to three when the data is encoded, the data clock is at two-thirds the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 30 MHz. As in the case of the 2:7 coding scheme, the pole and zero positions are a function of the data rate, hence the component values derived by these calculations must be scaled if a different operating frequency is used.

Again, the analysis is divided into three parts: static pole positioning, dynamic pole positioning and dynamic zero positioning.

Static Poles

As in the 2:7 coding example, a 34182D op-amp is employed, hence the pole set is:

P_{1a} - –5.65 + j5.65 MHz

P_{1b} = –5.65 – j5.65 MHz

and the open loop gain is:

$$A_1 = A_2 = 2.48\ e15\ \frac{V}{V}$$

Since the op-amps introduce a set of complex conjugate poles, a total of four poles are introduced by the op-amp. In addition, the integrator and the VCO each contribute a pole at the origin for a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

P^*_1 = –1.1 MHz

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus, the open loop voltage divider pole position is selected as:

P^*_2 = –2.28 MHz

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency. For this design, the zero is placed at:

z = –311 Hz

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot. If the phase margin is not sufficient, they dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions, the component values are calculated. From the root locus analysis, the dynamic pole and zero positions are:

P_1 = –541 KHz

P_2 = –2.73 MHz

z = –311 Hz

Filter Input Subsection

Rearranging Equation 4:

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 541 KHz for the pole position and 1 KΩ for the resistor value yields:

C_{IN} = 294 pF

Augmenting Integrator Subsection

Rearranging Equation 6:

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311 Hz for the zero position and 0.1μF for the capacitor value yields:

R_A = 5.11 KΩ

From Equation 7, the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$R_{IA} = R_A$ = 5.11 KΩ

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9 and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3V + V_{EE} to 2.6V

APPLICATIONS INFORMATION (CONTINUED)

+ VEE. Restating Equation 9,

$$K_d = \frac{K_{OI}}{K\phi * K_O * K_1 * K_I}$$

From the root locus analysis, K_{OI} is determined to be:

$$K_{OI} = 1.258\ e51\ \frac{V}{mA\ sec^3}$$

From Equation 3:

$$K_I = A_I * \frac{1}{C_{IN}}$$

and the gain constant K_1:

$$K_1 = 8.42\ e21\ \frac{V}{mA\ sec}$$

From Equation 5:

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant K_I is:

$$K_I = 2.48\ e15\ \frac{V}{V}$$

$$K_d = 2.98\ e6\ sec^{-1}$$

Having determined the gain constant K_d, the value of R_V is selected such that the constraints $R_V > R_O$ and:

$$\frac{K_d}{2\pi|p_2|} = \frac{R_O}{R_O + R_V}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$P_2 = 2.73$ MHz

Hence, R_V is selected to be:

$R_V = 2.15\ K\Omega$

and R_O is calculated to be:

$R_O = 453\ \Omega$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_V K_d} \qquad \text{eqt. 8a}$$

the capacitor value C_d is calculated to be:

$C_d = 156$ pF

Again, note the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 20 Mbit/sec. If the data rate is different from the nominal design value, the reactive elements must be scaled accordingly. The following equations are provided are to facilitate scaling and were derived with the assumptions that a 1:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock:

$$C_{IN} = 294 * \frac{30}{f}\ (pF) \qquad \text{eqt. 13}$$

$$C_d = 156 * \frac{30}{f}\ (pF) \qquad \text{eqt. 14}$$

where f is the RDCLK frequency in MHz.

Example for a 10Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 1:7 code are used, but the data rate is 10 Mbit/sec. The dynamic pole positions and, therefore, the bandwidth of the loop filter, are a function of the data rate. Thus, a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 13, the value of C_{IN} is:

$C_{IN} = 588$ pF

and from Equation 14, the value of C_d is:

$C_d = 312$ pF

Thus, the element values for the filter are:

Filter Input Subsection:

$C_{IN} = 588$ pF

$R_1 = 1\ K\Omega$

Integrator Subsection:

$C_A = 0.1\ \mu F$

$R_A = 5.11\ K\Omega$

$R_{IA} = 5.11\ K\Omega$

Voltage Divider Subsection:

$C_d = 312$ pF

$R_V = 2.15\ K\Omega$

$R_O = 453\ \Omega$

APPLICATIONS INFORMATION (CONTINUED)

Note, the poles P_1 and P_2 are now located at:

$P_1 = -271$ KHz

$P_2 = -1.36$ MHz

and, the open loop filter unity crossover point is at 300 KHz. As in the case of the 2:7 coding scheme, the gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affecting the dynamic performance of the filter.

3-BIT SCANNABLE REGISTERED ADDRESS DRIVER

SY10E212
SY100E212

FEATURES

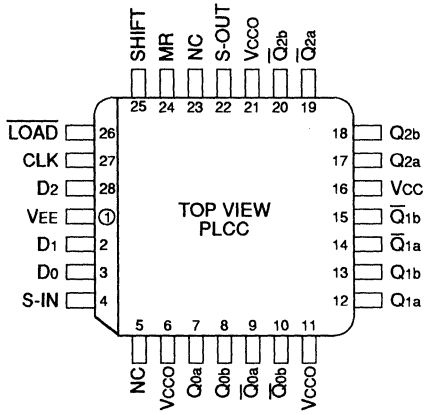
- **Scannable version E112 driver**
- **1025ps max. CLK to Output**
- **Dual differential outputs**
- **Master Reset**
- **Internal 75KΩ input pull-down resistors**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E212**

DESCRIPTION

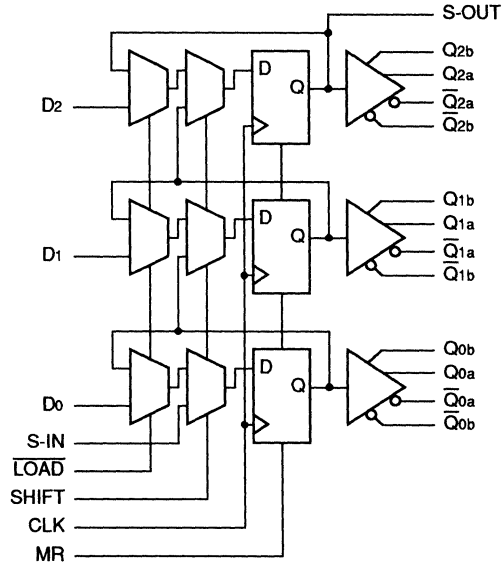
The SY10E212 and SY100E212 are scannable registered ECL drivers typically used as fan-out memory address drivers for ECL cache driving. In a VLSI array-based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0 – D2	Data Inputs
S-IN	Scan Input
$\overline{LOAD}$	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Master Reset
S-OUT	Scan Output
Q[0:2]a, Q[0:2]b	True Outputs
$\overline{Q}$[0:2]a, $\overline{Q}$[0:2]b	Inverting Outputs

TRUTH TABLE

$\overline{LOAD}$	SHIFT	MR	Mode
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

Rev.: B Amendment: /0
Issue Date: February, 1994

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	80	96	—	80	96	—	80	96		
	100E	—	80	96	—	80	96	—	92	110		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK	575	800	1025	575	800	1025	575	800	1025		
	MR	575	800	1025	575	800	1025	575	800	1025		
	CLK to S-OUT	575	800	1025	575	800	1025	575	800	1025		
t_s	Set-up Time										ps	—
	D	175	25	—	175	25	—	175	25	—		
	SHIFT	150	–50	—	150	–50	—	150	–50	—		
	$\overline{LOAD}$	225	50	—	225	50	—	225	50	—		
	S-IN	150	–50	—	150	–50	—	150	–50	—		
t_h	Hold Time										ps	—
	D	250	25	—	250	25	—	250	25	—		
	SHIFT	300	100	—	300	100	—	300	100	—		
	$\overline{LOAD}$	225	0	—	225	0	—	225	0	—		
	S-IN	300	100	—	300	100	—	300	100	—		
t_{RR}	Reset Recovery	600	350	—	600	350	—	600	350	—	ps	—
t_{SKEW}	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	1
t_{SKEW}	Within-Gate Skew	—	50	—	—	50	—	—	50	—	ps	2
t_r	Rise/Fall Times	275	425	650	275	425	650	275	425	650	ps	—
t_f	20% to 80%											

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E212JC	J28-1	Commercial
SY100E212JC	J28-1	Commercial

FEATURES

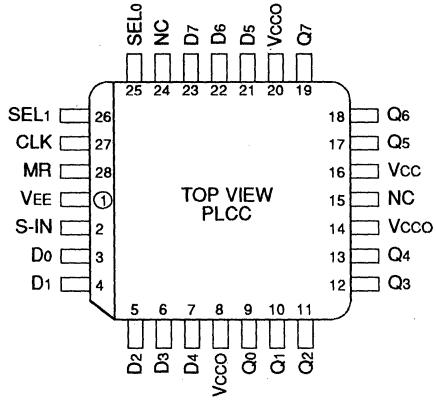
- **1000ps max. CLK to output**
- **SHIFT overrides HOLD/$\overline{\text{LOAD}}$ control**
- **Asynchronous Master Reset**
- **Pin-compatible with E141**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E241**

DESCRIPTION

The SY10E241 and SY100E241 are 8-bit shiftable registers designed for use in new, high-performance ECL systems. Unlike the E141, the E241 features internal data feedback organized such that the SHIFT control overrides the HOLD/$\overline{\text{LOAD}}$ control. Thus, the normal operations of HOLD and LOAD can be toggled with a single control line without the need for external gating. This configuration also enables switching to scan mode with the single SHIFT control line.

The eight inputs D_0–D_7 accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the rising edge of CLK. Shifting is also accomplished on the rising clock edge. A HIGH on the Master Reset pin (MR) asychronously resets all the registers to zero.

PIN CONFIGURATION

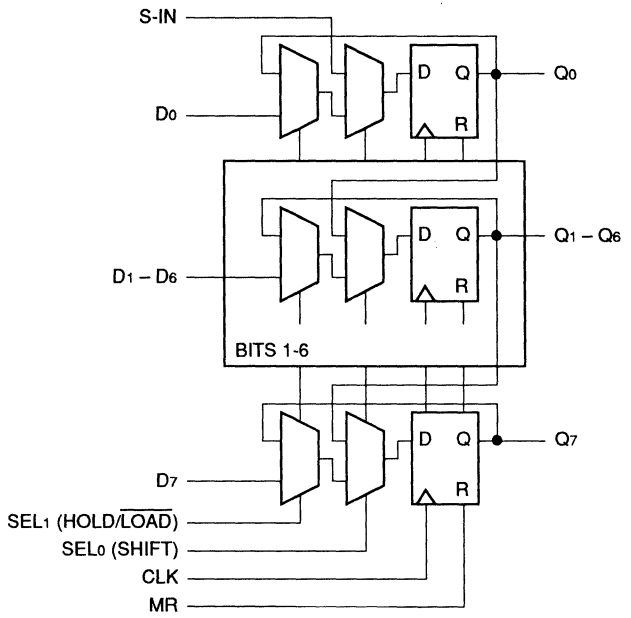


PIN NAMES

Pin	Function
D_0–D_7	Parallel Data Inputs
S-IN	Serial Data Input
SEL_0	SHIFT Control
SEL_1	HOLD/$\overline{\text{LOAD}}$ Control
CLK	Clock
MR	Master Reset
Q_0–Q_7	Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE

SEL_0	SEL_1	Function
L	L	Load
L	H	Hold
H	X	Shift (D_n to D_{n+1})

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	125	150	—	125	150	—	125	150		
	100E	—	125	150	—	125	150	—	144	173		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_s	Set-up Time										ps	—
	D	175	25	—	175	25	—	175	25	—		
	SEL_0 (SHIFT)	350	200	—	350	200	—	350	200	—		
	SEL_1 (HOLD/$\overline{LOAD}$)	400	250	—	400	250	—	400	250	—		
	S-IN	125	–100	—	125	–100	—	125	–100	—		
t_h	Hold Time										ps	—
	D	200	–25	—	200	–25	—	200	–25	—		
	SEL_0 (SHIFT)	100	–200	—	100	–200	—	100	–200	—		
	SEL_1 (HOLD/$\overline{LOAD}$)	50	–250	—	50	–250	—	50	–250	—		
	S-IN	300	100	—	300	100	—	300	100	—		
t_{RR}	Reset Recovery Time	900	600	—	900	600	—	900	600	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t_r	Rise/Fall Time	300	525	800	300	525	800	300	525	800	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E241JC	J28-1	Commercial
SY100E241JC	J28-1	Commercial

3-BIT 4:1 MUX-LATCH

SY10E256
SY100E256

FEATURES

- **950ps max. data to output**
- **850ps max. latch enable to output**
- **Separate select controls**
- **Differential outputs**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E256**

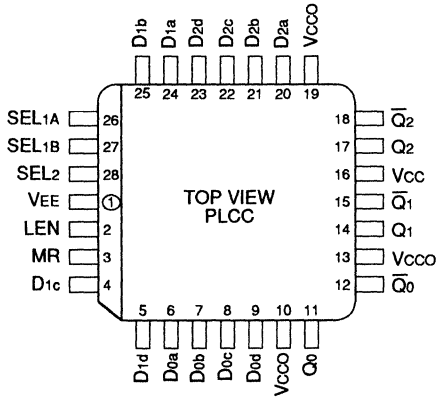
DESCRIPTION

The SY10E256 and SY100E256 offer three 4:1 multiplexers followed by latches with differential outputs designed for use in new, high-performance ECL systems. Separate Select controls are provided for the leading 2:1 mux pairs (see block diagram).

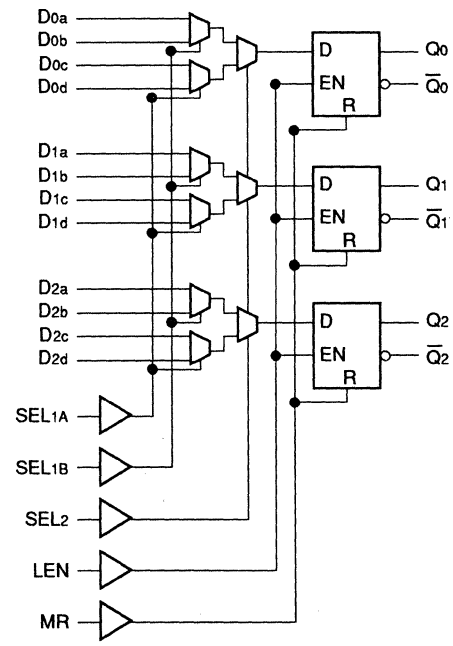
When the Latch Enable (LEN) is at a logic LOW, the latch is transparent and output data is controlled by the multiplexer select controls. A logic HIGH on LEN latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

4

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0x–D2x	Parallel Data Inputs
SEL1A, SEL1B	Fisrt-stage Select Inputs
SEL2	Second-stage Select Input
LEN	Latch Enable
MR	Master Reset
Q0, $\overline{Q0}$–Q2, $\overline{Q2}$	Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

TRUTH TABLE

Pin	State	Operation
SEL_2	H	Output c/d Data
SEL_{1A}	H	Input d Data
SEL_{1B}	H	Input b Data

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	69	83	—	69	83	—	69	83		
	100E	—	69	83	—	69	83	—	79	96		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D	400	600	900	400	600	900	400	600	900		
	SEL_1	550	775	1050	550	775	1050	550	775	1050		
	SEL_2	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	800		
	MR	350	600	825	350	600	825	350	600	825		
t_s	Set-up Time										ps	—
	D	400	275	—	400	275	—	400	275	—		
	SEL_1	600	300	—	600	300	—	600	300	—		
	SEL_2	500	250	—	500	250	—	500	250	—		
t_h	Hold Time										ps	—
	D	300	–275	—	300	–275	—	300	–275	—		
	SEL_1	100	–300	—	100	–300	—	100	–300	—		
	SEL_2	200	–250	—	200	–250	—	100	–250	—		
t_{RR}	Reset Recovery Time	700	600	—	700	600	—	700	600	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_r	Rise/Fall Time	275	475	700	275	475	700	275	475	700	ps	—
t_f	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E256JC	J28-1	Commercial
SY100E256JC	J28-1	Commercial

3-BIT REGISTERED BUS TRANSCEIVER

FEATURES

- 25Ω cutoff bus output
- 50Ω receiver output
- Transmit and receive registers
- 1500ps max. clock to bus
- 1000ps max. clock to Q
- Internal edge slow-down capacitors on bus outputs
- Additional package ground pins
- ESD protection of 2000V
- Fully compatible with industry standard 10KH, 100K ECL levels
- Extended 100E V_{EE} range of –4.2V to –5.46V
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E336

DESCRIPTION

The SY10E336 and SY100E336 offer three bus transceivers with both transmit and receive registers and are designed for use in new, high-performance ECL systems. The bus outputs ($\overline{BUS_0}$ - $\overline{BUS_2}$) are designed to drive a 25Ω bus. The receive outputs (Q_0 – Q_2) are specified for 50Ω. The bus outputs feature a normal logic HIGH level (V_{OH}) and a cutoff LOW level when at a logic LOW. At cutoff, the outputs go to –2.0V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs have edge slow-down capacitors.

The Transmit Enable pins (TEN) determine whether current data is held in the transmit register or new data is loaded from the A/B inputs. A logic LOW on both of the bus enable inputs (BUSEN), when clocked through the register, disables the bus outputs to –2.0V.

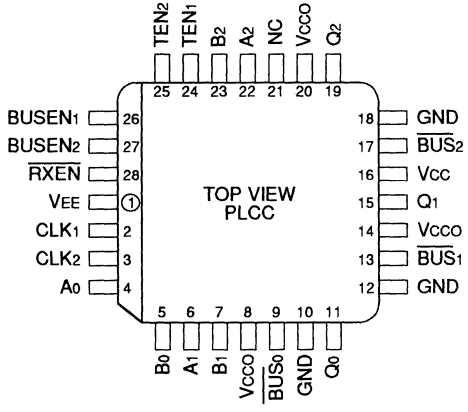
The receiver section clocks bus data into the receive registers after gating with the Receive Enable ($\overline{RXEN}$) input.

All registers are clocked by rising edge of CLK_1 or CLK_2 (or both).

Additional grounding is provided through the ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

4

PIN CONFIGURATION

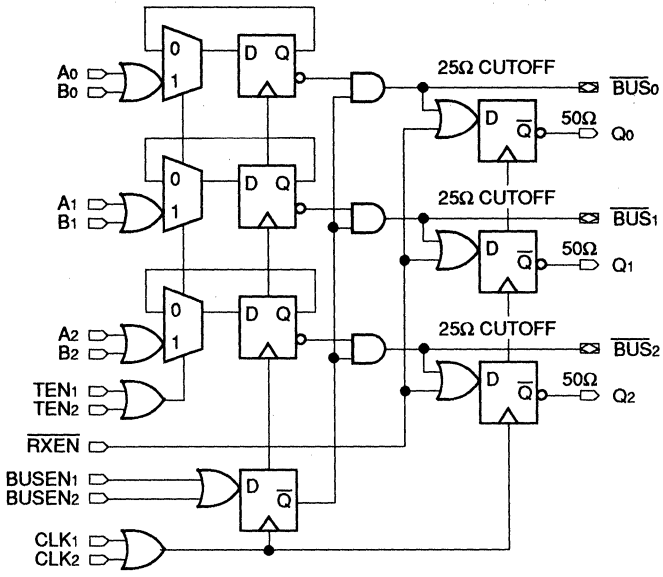


PIN NAMES

Pin	Function
A_0–A_2	Data Inputs A
B_0–B_2	Data Inputs B
$TEN_{1,2}$	Transmit Enable Inputs
$\overline{RXEN}$	Receive Enable Input
$BUSEN_{1,2}$	Bus Enable Inputs
$CLK_{1,2}$	Clock Inputs
$\overline{BUS_0}$–$\overline{BUS_2}$	25Ω Cutoff Bus Outputs
Q_0–Q_2	Receive Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CUT}	Cut-off Output Voltage	–2.10	—	–2.03	–2.10	—	–2.03	–2.10	—	–2.03	V	1
I_{IH}	Input HIGH Current										µA	—
	$\overline{RXEN}$	—	—	225	—	—	225	—	—	225		
	All Other Inputs	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	125	150	—	125	150	—	125	150		
	100E	—	125	150	—	125	150	—	144	173		

NOTE:

1. Measured with V_{TT} = –2.10V.

4

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK to Q	500	700	1000	500	700	1000	500	700	1000		
	CLK to $\overline{BUS}$	825	1250	1800	825	1250	1800	825	1250	1800		
t_s	Set-up Time										ps	—
	BUS, $\overline{RXEN}$	150	–150	—	150	–150	—	150	–150	—		
	BUSEN	100	–200	—	100	–200	—	100	–200	—		
	A, B Data	300	–50	—	300	–50	—	300	–50	—		
	TEN	450	150	—	450	150	—	450	150	—		
t_h	Hold Time										ps	—
	BUS, $\overline{RXEN}$	450	150	—	450	150	—	450	150	—		
	BUSEN	500	200	—	500	200	—	500	200	—		
	A, B Data	350	50	—	350	50	—	350	50	—		
	TEN	200	–150	—	200	–150	—	200	–150	—		
t_{PW}	Minimum Pulse Width, CLK	400	—	—	400	—	—	400	—	—	ps	—
t_r	Rise/Fall Time										ps	—
t_f	20% to 80% (Q_n)	300	450	700	300	450	700	300	450	700		
	20% to 80% (BUS_n Rise)	500	800	1000	500	800	1000	500	800	1000		
	20% to 80% (BUS_n Fall)	300	500	800	300	500	800	300	500	800		

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E336JC	J28-1	Commercial
SY100E336JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

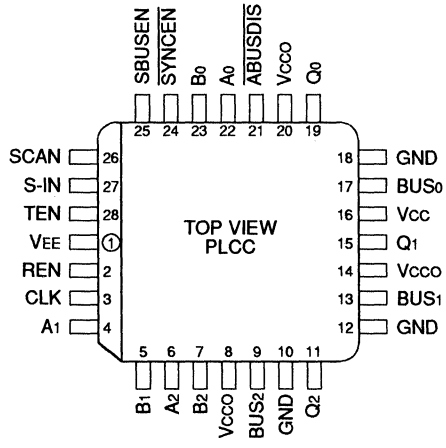
3-BIT SCANNABLE REGISTERED BUS TRANSCEIVER

SY10E337
SY100E337

FEATURES

- 1500ps max. clock to bus (data transmit)
- 1000ps max. clock to Q (data receive)
- 25Ω cutoff bus outputs
- 50Ω receiver outputs
- Scannable implementation of E336
- Synchronous and asynchronous bus enables
- Non-inverting data path
- Bus outputs feature internal edge slow-down capacitors
- Additional package ground pins
- ESD protection of 2000V
- Fully compatible with industry standard 10KH, 100K ECL levels
- Extended 100E V_{EE} range of –4.2V to –5.46V
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E337

PIN CONFIGURATION



DESCRIPTION

The SY10E337 and SY100E337 are 3-bit registered bus transceivers with scan designed for use in new, high-performance ECL systems. The bus outputs (BUS_0–BUS_2) are designed to drive a 25Ω bus; the receive outputs (Q_0–Q_2) are designed for 50Ω. The bus outputs feature a normal logic HIGH level (V_{OH}) and a cutoff LOW level of –2.0V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The LOAD/$\overline{\text{HOLD}}$ function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides, respectively, with a HIGH selecting LOAD. The implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable ($\overline{\text{ABUSDIS}}$) disables the bus for scan mode.

The $\overline{\text{SYNCEN}}$ input allows either synchronousor asynchronous re-enabling after disabling with $\overline{\text{ABUSDIS}}$. An alternative use is asynchronous-only operation with $\overline{\text{ABUSDIS}}$, in which case $\overline{\text{SYNCEN}}$ is tied LOW. $\overline{\text{SYNCEN}}$ is implemented as an overriding SET control to the enable flip-flop.

Scan mode is selected by a logic HIGH at the SCAN input. Scan input data is shifted in through S-IN, and output data appears at the Q_2 output.

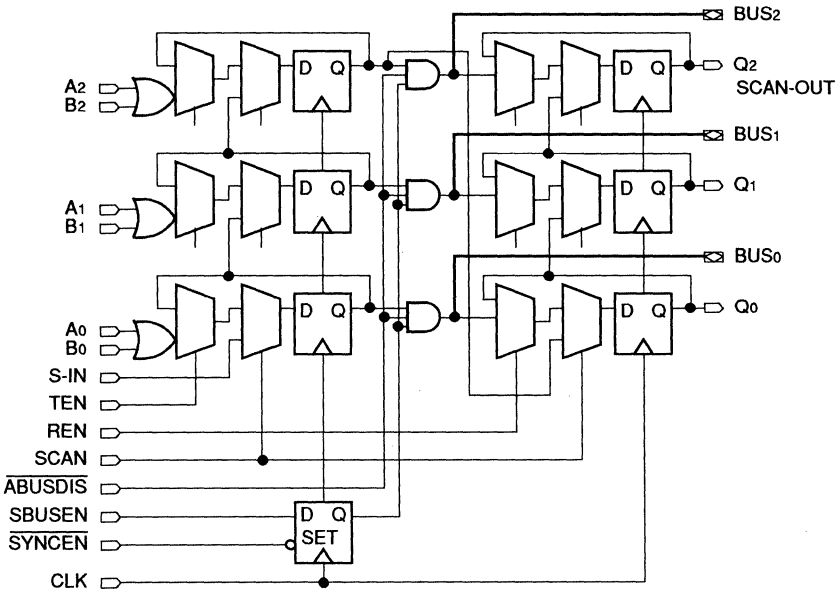
All registers are clocked on the rising edge of CLK. Additional lead-frame grounding is provided through the ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

PIN NAMES

Pin	Function
A_0–A_2	Data Inputs A
B_0–B_2	Data Inputs B
S-IN	Serial (Scan) Data Input
TEN, REN	HOLD/$\overline{\text{LOAD}}$ Controls
SCAN	Scan Control
$\overline{\text{ABUSDIS}}$	Asynchronous Bus Disable
SBUSEN	Synchronous Bus Enable
$\overline{\text{SYNCEN}}$	Synchronous Enable Control
CLK	Clock
BUS_0–BUS_2	25Ω Cutoff BUS Outputs
Q_0–Q_2	Receive Data Outputs (Q_2 serves as SCAN_OUT in scan mode)

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CUT}	Cut-off Output Voltage	–2.10	—	–2.03	–2.10	—	–2.03	–2.10	—	–2.03	V	1
I_{IH}	Input HIGH Current All Other Inputs	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	145	174	—	145	174	—	145	174		
	100E	—	145	174	—	125	174	—	167	200		

NOTE:

1. Applies to BUS outputs only. Measured with V_{TT} = –2.10V.

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK to Q	450	—	1000	450	—	1000	450	—	1000		
	CLK to BUS	800	—	1800	800	—	1800	800	—	1800		
	$\overline{\text{ABUSDIS}}$	500	—	1500	500	—	1500	500	—	1500		
	$\overline{\text{SYNCEN}}$	800	—	1800	800	—	1800	800	—	1800		
t_s	Set-up Time										ps	—
	BUS	350	—	—	350	—	—	350	—	—		
	SBUSEN	100	—	—	100	—	—	100	—	—		
	Data, S-IN	400	—	—	400	—	—	400	—	—		
	TEN, REN, SCAN	550	—	—	550	—	—	550	—	—		
t_h	Hold Time										ps	—
	BUS	350	—	—	350	—	—	350	—	—		
	SBUSEN	500	—	—	500	—	—	500	—	—		
	Data, S-IN	350	—	—	350	—	—	350	—	—		
	TEN, REN, SCAN	200	—	—	200	—	—	200	—	—		
t_{PW}	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	ps	—
t_r t_f	Rise/Fall Time										ps	—
	20% to 80% (Q_n)	300	—	800	300	—	800	300	—	800		
	20% to 80% (BUS_n Rise)	500	—	1000	500	—	1000	500	—	1000		
	20% to 80% (BUS_n Fall)	300	—	800	300	—	800	300	—	800		

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E337JC	J28-1	Commercial
SY100E337JC	J28-1	Commercial

QUAD DIFFERENTIAL AND/NAND

FEATURES

- **Differential D and Q**
- **700ps max. propagation delay**
- **High frequency outputs**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E404**

DESCRIPTION

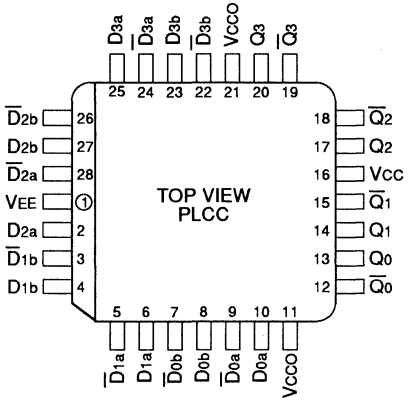
The SY10E404 and SY100E404 are 4-bit differential AND/NAND devices. The differential operation of these devices make them ideal for pulse shaping applications where duty cycle skew is critical. Special design techniques were incorporated to minimize the skew between the upper and lower level gate inputs.

Because a negative 2-input NAND function is equivalent to a 2-input OR function, the differential inputs and outputs of the devices also allow for their use as fully differential 2-input OR/NOR functions.

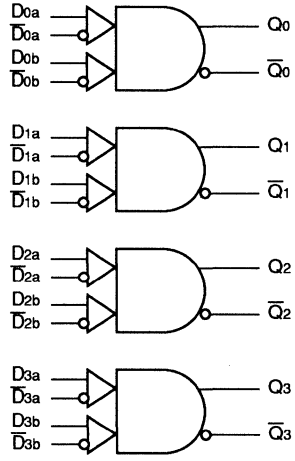
The output RISE/FALL times of these devices are significantly faster than most other standard ECLinPS devices, resulting in an increased bandwidth.

The differential inputs have clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D[0:4], D̄[0:4]	Differential Data Inputs
Q[0:4], Q̄[0:4]	Differential Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

TRUTH TABLE

Da	Db	Q	$\overline{Da}$	$\overline{Db}$	$\overline{Q}$
L	L	L	L	L	L
L	H	L	L	H	H
H	L	L	H	L	H
H	H	H	H	H	H

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	106	127	—	106	127	—	106	127		
	100E	—	106	127	—	106	127	—	122	146		
$V_{PP(DC)}$	Input Sensitivity	50	—	—	50	—	—	50	—	—	mV	1
V_{CMR}	Common Mode Range	–1.5	—	0	–1.5	—	0	–1.5	—	0	V	2

NOTES:

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D_a (Diff)	350	475	650	350	475	650	350	475	650		
	D_a (SE)	300	475	700	300	475	700	300	475	700		
	D_b (Diff)	375	500	675	375	500	675	375	500	675		
	D_b (SE)	325	500	725	325	500	725	325	500	725		
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
$V_{PP(AC)}$	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	2
t_r	Rise/Fall Time	150	—	400	150	—	400	150	—	400	ps	—
t_f	20–80%											

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E404JC	J28-1	Commercial
SY100E404JC	J28-1	Commercial

QUINT DIFFERENTIAL LINE RECEIVER

FEATURES

- **Differential D and Q**
- **V_{BB} output for single-ended use**
- **600ps max. propagation delay**
- **High frequency outputs**
- **2 stages of gain**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E416**

DESCRIPTION

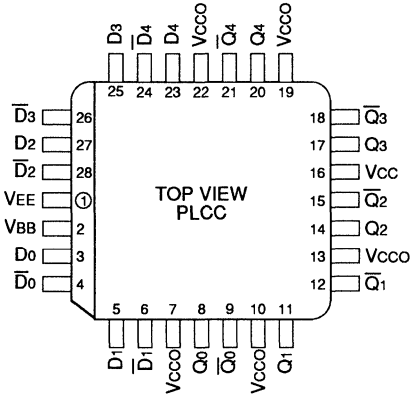
The SY10E416 and SY100E416 are 5-bit differential line receiving devices. The 2.0GHz of bandwidth provided by the high frequency outputs make the devices ideal for buffering of very high speed oscillators.

A V_{BB} pin is available to AC couple an input signal to the devices.

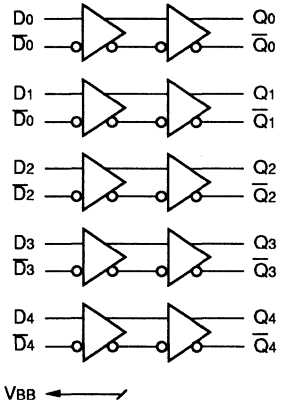
The design incorporates two stages of gain internal to the devices, making them an excellent choice for use in high bandwidth amplifier applications.

4

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D[0:4], $\overline{D}$[0:4]	Differential Data Inputs
Q[0:4], $\overline{Q}$[0:4]	Differential Data Outputs

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Issue Date: February, 1994

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19		
	100E	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	135	162	—	135	162	—	135	162		
	100E	—	135	162	—	135	162	—	155	186		
$V_{PP(DC)}$	Input Sensitivity	50	—	—	50	—	—	50	—	—	mV	1
V_{CMR}	Common Mode Range	−1.5	—	0	−1.5	—	0	−1.5	—	0	V	2

NOTES:

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D (Diff)	250	350	500	250	350	500	250	350	500		
	D (SE)	200	350	550	200	350	550	200	350	550		
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_{SKEW}	Duty Cycle Skew, t_{PLH}–t_{PHL}		±10			±10			±10		ps	2
$V_{PP(AC)}$	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	3
t_r	Rise/Fall Time	100	200	350	100	200	350	100	200	350	ps	—
t_f	20–80%											

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

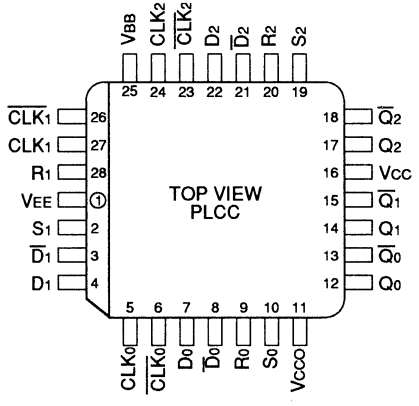
Ordering Code	Package Type	Operating Range
SY10E416JC	J28-1	Commercial
SY100E416JC	J28-1	Commercial

3-BIT DIFFERENTIAL FLIP-FLOP

FEATURES

- **Differential D, clock and Q**
- **V_{BB} output for single-ended use**
- **1100MHz min. toggle frequency**
- **Edge-triggered asynchronous set and reset**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola 10E/100E431**

PIN CONFIGURATION



PIN NAMES

Pin	Function
D[0:2], $\overline{D}$[0:2]	Differential Data Inputs
CLK[0:2], $\overline{CLK}$[0:2]	Differential Clock Inputs
S[0:2]	Edge Triggered Set Inputs
R[0:2]	Edge Triggered Reset Inputs
V_{BB}	V_{BB} Reference Output
Q[0:2], $\overline{Q}$[0:2]	Differential Data Outputs

TRUTH TABLE(1)

D_n	CLK_n	R_n	S_n	Q_n
L	Z	L	L	L
H	Z	L	L	H
X	L	Z	L	L
X	L	L	Z	H

NOTE:

1. Z = LOW-to-HIGH transition.

DESCRIPTION

The SY10E431 and SY100E431 are 3-bit flip-flops with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduces the metastability susceptibility window.

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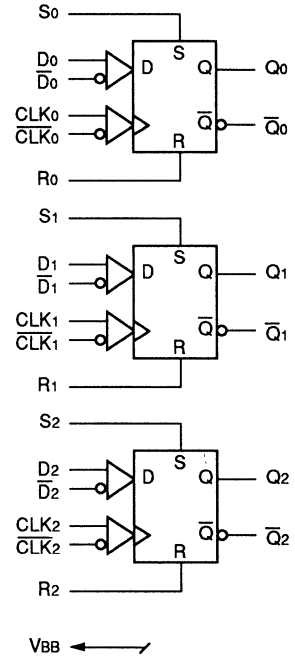
BLOCK DIAGRAM



Rev.: B Amendment: /0
Issue Date: February, 1994

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		
V_{CMR}	Common Mode Range	–1.5	—	0	–1.5	—	0	–1.5	—	0	V	1

NOTES:

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK (Diff)	450	600	750	450	600	750	450	600	750		
	CLK (SE)	400	600	800	400	600	800	400	600	800		
	R	550	725	925	550	725	925	550	725	925		
	S	550	725	925	550	725	925	550	725	925		
t_s	Set-up Time										ps	
	D	200	0	—	200	0	—	200	0	—		
	R	1000	700	—	1000	700	—	1000	700	—		1
	S	1000	700	—	1000	700	—	1000	700	—		1
t_h	Hold Time, D	200	0	—	200	0	—	200	0	—	ps	—
t_{PW}	Minimum Pulse Width, CLK	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	2
$V_{PP(AC)}$	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	3
t_r t_f	Rise/Fall Time 20% to 80%	275	450	650	275	450	650	275	450	650	ps	—

NOTES:

1. These set-up times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Minimum input swing for which AC parameters are guaranteed.

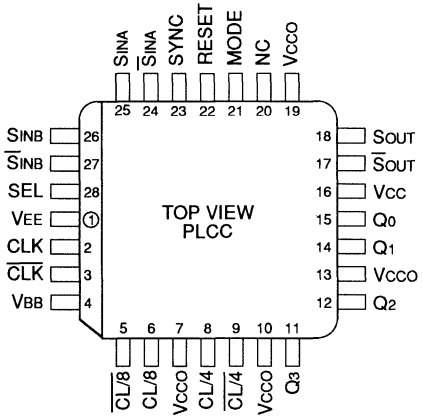
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E431JC	J28-1	Commercial
SY100E431JC	J28-1	Commercial

FEATURES

- **On-chip clock ÷4 and ÷8**
- **2.5Gb/s data rate capability**
- **Differential clock and serial inputs**
- **VBB output for single-ended use**
- **Asynchronous data synchronization**
- **Mode select to expand to 8 bits**
- **Internal 75kΩ input pull-down resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E445**
- **Extended 100E VEE range of –4.2V to –5.46V**

PIN CONFIGURATION



PIN NAMES

Pin	Function
SINA, $\overline{\text{SINA}}$	Differential Serial Data Input A
SINB, $\overline{\text{SINB}}$	Differential Serial Data Input B
SEL	Serial Input Select Pin
SOUT, $\overline{\text{SOUT}}$	Differential Serial Data Output
Q0–Q3	Parallel Data Outputs
CLK, $\overline{\text{CLK}}$	Differential Clock Inputs
CL/4, $\overline{\text{CL/4}}$	Differential ÷4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Differential ÷8 Clock Output
MODE	Conversion Mode 4-bit/8-bit
SYNCH	Conversion Synchronizing Input

DESCRIPTION

The SY10E445 and SY100E445 are integrated 4-bit serial-to-parallel data converters. The devices are designed to operate for NRZ data rates of up to 2.5Gb/s. The chip generates a divide-by-4 and a divide-by-8 clock for both 4-bit conversion and a two-chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q_0, the second to Q_1, etc.

Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel-to-serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse, applied asynchronously for at least two input clock cycles, shifts the start bit for conversion from Q_n to Q_{n-1} by one bit. For each additional shift required, an additional pulse must be applied to the SYNC input. Asserting the SYNC input will force the internal clock dividers to "swallow" a clock pulse, effectively shifting a bit from the Q_n to the Q_{n-1} output (see Timing Diagram B).

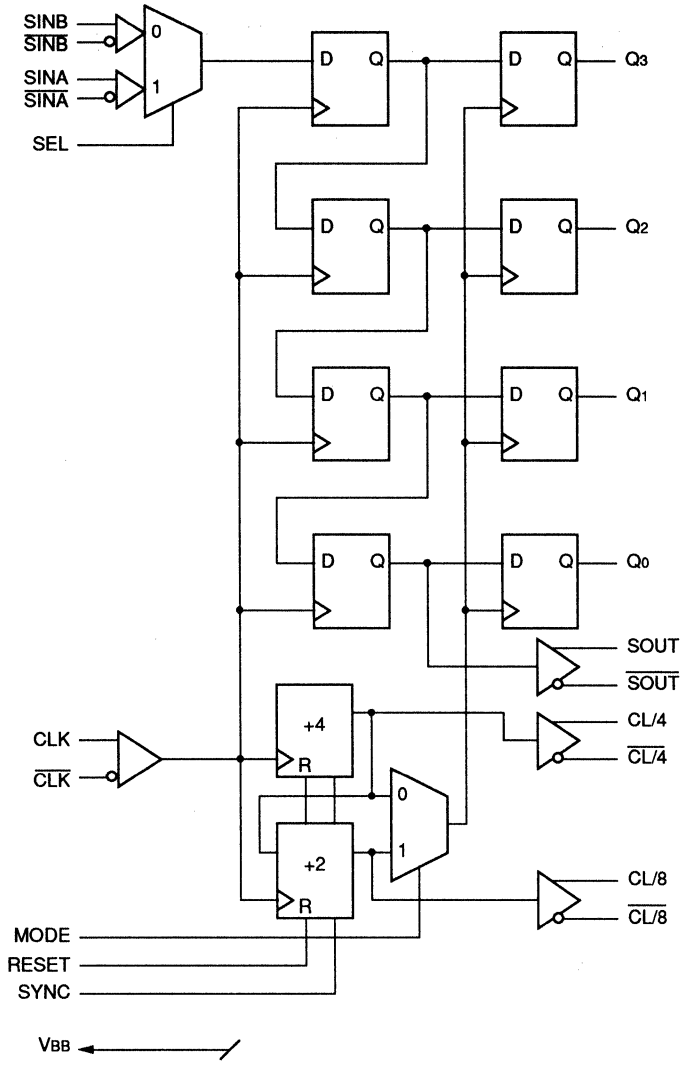
The MODE input is used to select the conversion mode of the device. With the MODE input LOW (or open) the device will function as a 4-bit converter. When the mode input is driven HIGH, the data on the output will change on every eighth clock cycle, thus allowing for an 8-bit conversion scheme using two E445s. When cascaded in an 8-bit conversion scheme, the devices will not operate at the 2.5Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E445.

For lower data rate applications, a VBB reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz, differential input signals are recommended. For single-ended inputs, the VBB pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The VBB provides the switching reference for the input differential amplifier. The VBB can also be used to AC couple an input signal.

4

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLES

Mode	Conversion
L	4-Bit
H	8-Bit

SEL	Serial Input
H	A
L	B

DC CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
V_{OH}	Output HIGH Voltage										V	
	10E (S_{OUT} only)	–1020	—	–790	–980	—	–760	–910	—	–670		1
	100E (S_{OUT} only)	–1025	—	–830	–1025	—	–830	–1025	—	–830		1
V_{BB}	Output Reference Voltage										V	
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{EE}	Power Supply Current										mA	—
	10E	—	154	185	—	154	185	—	154	185		
	100E	—	154	185	—	154	185	—	177	212		

NOTE:

1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

4

DC CHARACTERISTICS

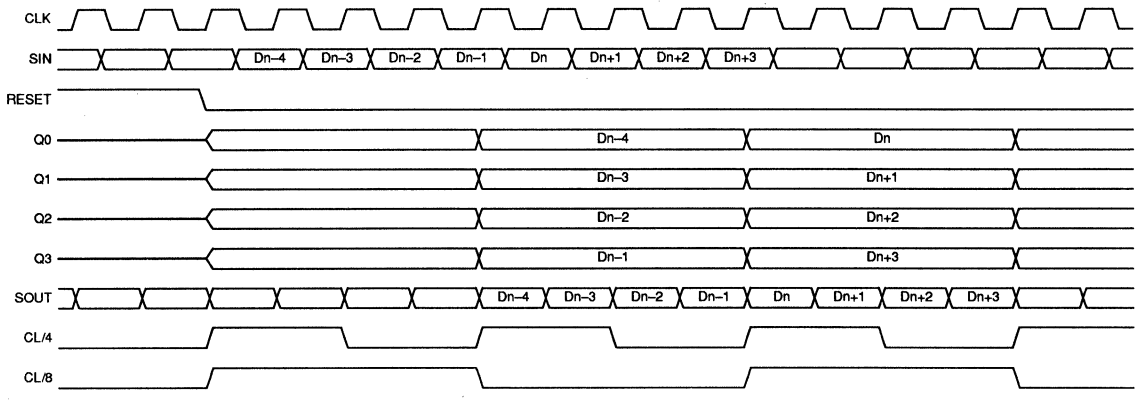
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Conversion Frequency	2.0	—	—	2.0	—	—	2.0	—	—	Gb/s	1
		2.5	—	—	2.5	—	—	2.5	—	—	NRZ	2
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK to Q	1500	1800	2100	1500	1800	2100	1500	1800	2100		
	CLK to S_{OUT}	800	975	1150	800	975	1150	800	975	1150		
	CLK to CL/4	1100	1325	1550	1100	1325	1550	1100	1325	1550		
	CLK to CL/8	1100	1325	1550	1100	1325	1550	1100	1325	1550		
t_S	Set-up Time										ps	—
	SINA, SINB	–100	–250	—	–100	–250	—	–100	–250	—		
	SEL	0	–200	—	0	–200	—	0	–200	—		
t_H	Hold Time, SINA, SINB, SEL	450	300	—	450	300	—	450	300	—	ps	—
t_{RR}	Reset Recovery Time	500	300	—	500	300	—	500	300	—	ps	—
t_{PW}	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	ps	—
	CLK, MR											
t_r	Rise/Fall Times										ps	—
t_f	20% to 80%											
	S_{OUT}	100	225	350	100	225	350	100	225	350		
	Other	200	425	650	200	425	650	200	425	550		

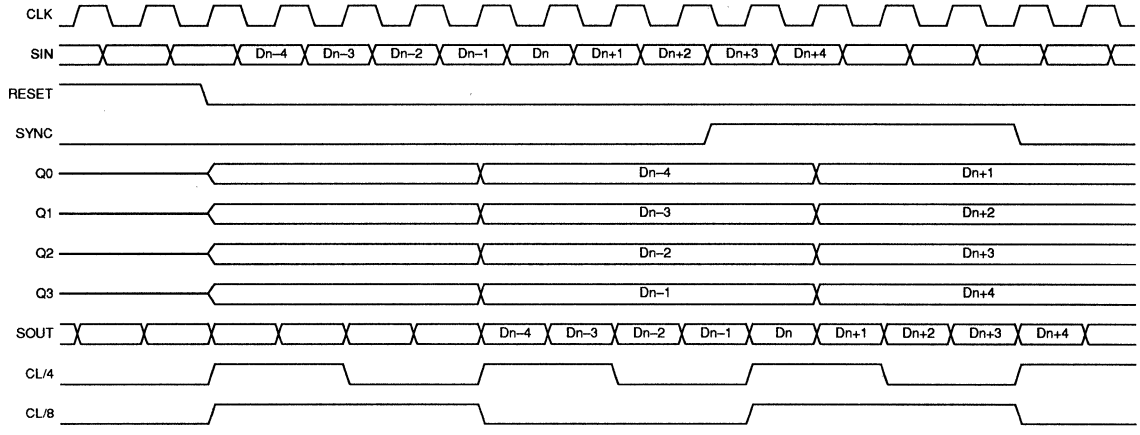
NOTE:

1. Guaranteed for input clock amplitudes of 150mV to 800mV.
2. Guaranteed for input clock amplitudes of 150mV to 400mV.

TIMING DIAGRAMS



Timing Diagram A. 1:4 Serial to Parallel Conversion



Timing Diagram B. 1:4 Serial to Parallel Conversion with SYNC Pulse

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E445JC	J28-1	Commercial
SY100E445JC	J28-1	Commercial

APPLICATIONS INFORMATION

The SY10/100E are integrated 1:4 serial-to-parallel converters. The chips are designed to work with the E446 devices to provide both transmission and receiving of a high-speed serial data path. The E445, under special input conditions, can convert up to a 2.5Gb/s NRZ data stream into 4-bit parallel data. The device also provides a divide-by-four clock output to be used to synchronize the parallel data with the rest of the system.

The E445 features multiplexed dual serial inputs to provide test loop capability when used in conjunction with the E446. Figure 1 illustrates the loop test architecture. The architecture allows for the electrical testing of the link without requiring actual transmission over the serial data path medium. The SINA serial input of the E445 has an extra buffer delay and, thus, should be used as the loop back serial input.

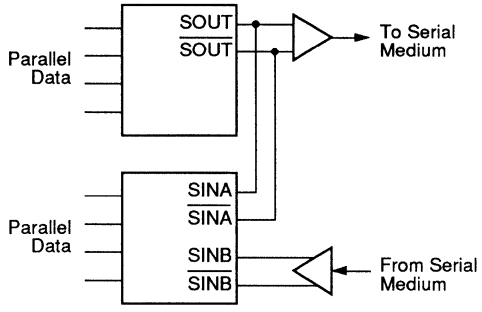


Figure 1. Loop Test Architecture

The E445 features a differential serial output and a divide-by-8 clock output to facilitate the cascading of two devices to build a 1:8 demultiplexer. Figure 2 illustrates the architecture of a 1:8 demultiplexer using two E445s. The timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the higher order device. This feedthrough of the serial inputs bounds the upper end of the frequency of operation. The clock-to-serial output propagation delay, plus the set-up time of the serial input pins, must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, tPD CLK to SOUT = 1150ps or a clock frequency of 950MHz.

The clock frequency is significantly lower than that of a single converter. To increase this frequency, some games can be played with the clock input of the higher order E445. By delaying the clock feeding the second E445 relative to the clock of the first E445, the frequency of operation can be increased. The delay between the two clocks can be increased until the minimum delay of clock-to-serial-out would potentially cause a serial bit to be

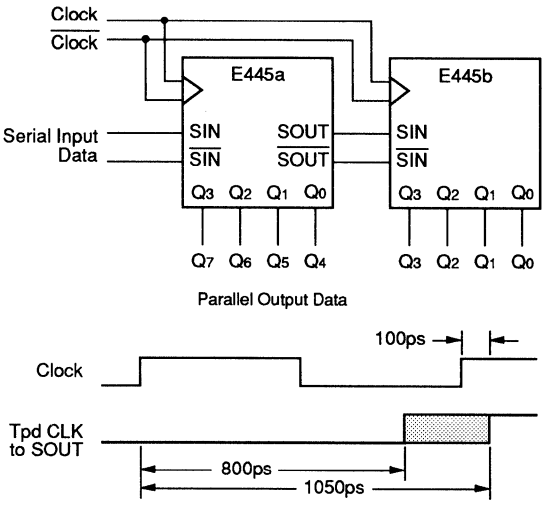


Figure 2. Cascaded 1:8 Converter Architecture

swallowed (Figure 3). With a minimum delay of 800ps on this output, the clock for the lower order E445 cannot be delayed more than 800ps relative to the clock of the first E445 without potentially missing a bit of information. Because the set-up time on the serial input pin is negative, coincident excursions on the data and clock inputs of the E445 will result in correct operation.

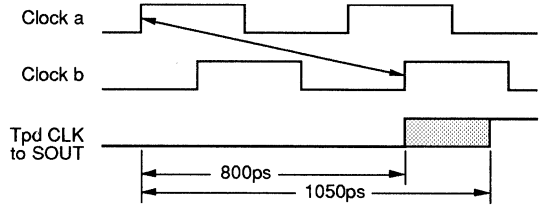


Figure 3. Cascade Frequency Limitation

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E445. By connecting the clock for the second E445 to the complimentary clock input pin, the device will clock a half a clock period after the first E445 (Figure 4). Utilizing this simple technique will raise the potential conversion frequency up to 1.5GHz. The divide-by-eight clock of the second E445 should be used to synchronize the parallel data to the rest of the system as the parallel data of the two E445s will no longer be synchronized. This skew problem between the outputs can be worked around as the parallel information will be static for eight more clock pulses.

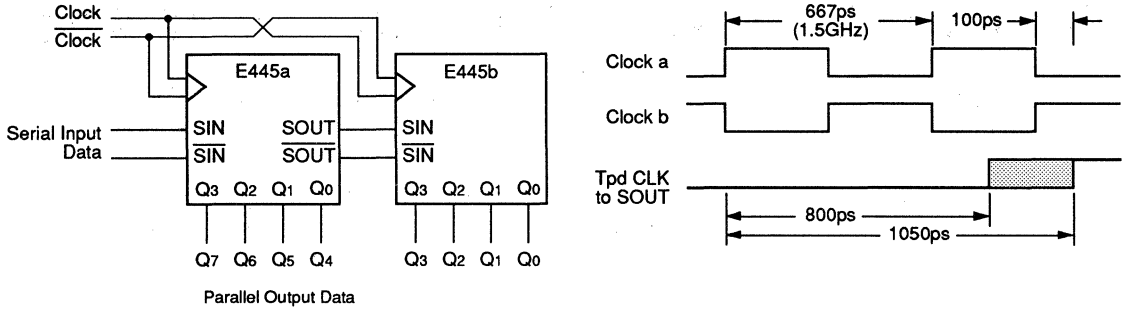
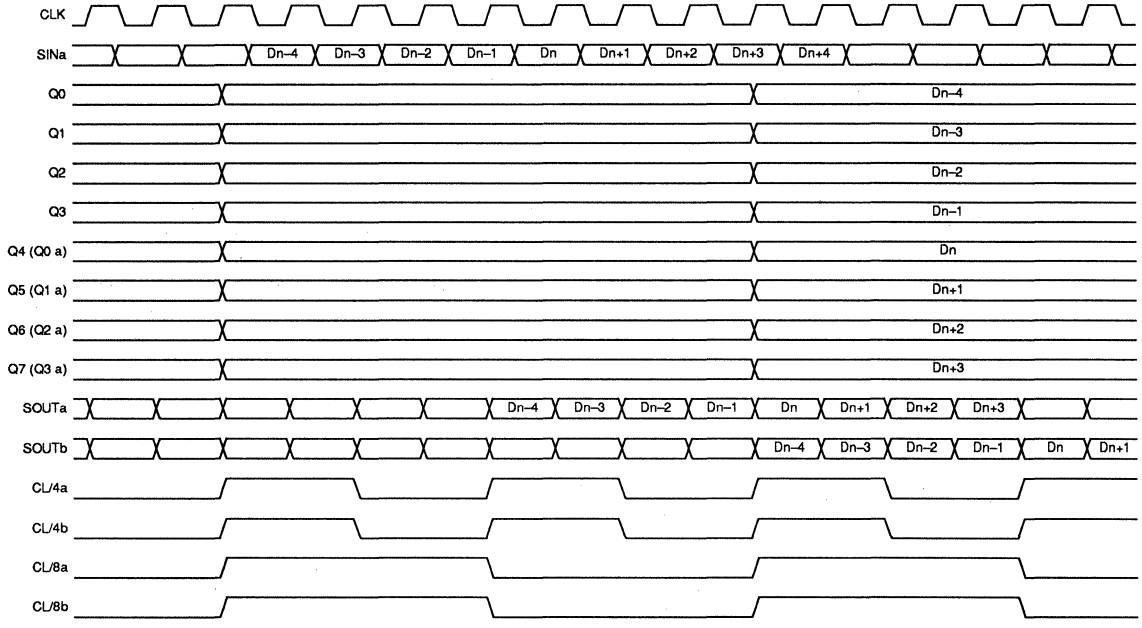


Figure 4. Extended Frequency 1:8 Demultiplexer



Timing Diagram A. 1:8 Serial to Parallel Conversion

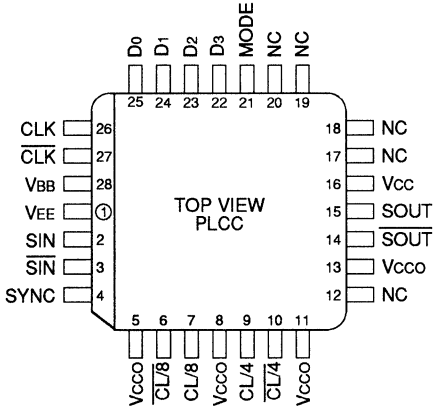
4-BIT PARALLEL-TO-SERIAL CONVERTER

PRELIMINARY
SY10E446
SY100E446

FEATURES

- **On-chip clock ÷4 and ÷8**
- **1.6Gb/s typical data rate capability**
- **Differential clock and serial inputs**
- **VBB output for single-ended use**
- **Asynchronous data synchronization**
- **Mode select to expand to 8 bits**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E446**

PIN CONFIGURATION



PIN NAMES

Pin	Function
SIN, $\overline{SIN}$	Differential Serial Data Input
D0 – D3	Parallel Data Input
SOUT, $\overline{SOUT}$	Differential Serial Data Output
CLK, $\overline{CLK}$	Differential Clock Input
CL/4, $\overline{CL/4}$	Differential 4 Clock Output
CL/8, $\overline{CL/8}$	Differential 8 Clock Output
MODE	Conversion Mode, 4-bit/8-bit
SYNC	Conversion Synchronizing Input

DESCRIPTION

The SY10E446 and SY100E446 are integrated 4-bit parallel-to-serial data converters. These devices are designed to operate for NRZ data rates of up to a minimum of 1.3Gb/s. The chips generate a divide-by-4 and a divide-by-8 clock for both 4-bit conversion and a two-chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8-bit conversion applications.

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and, thus, select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW (or open) the device will function as a 4-bit converter. When the mode input is driven HIGH, the internal load clock will change on every eighth clock cycle, thus allowing for an 8-bit conversion scheme using two E446s. When cascaded in an 8-bit conversion scheme, the devices will not operate at the 1.3Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

For lower data rate applications, a VBB reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz, differential input signals are recommended. For single-ended inputs, the VBB pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The VBB provides the switching reference for the input differential amplifier. The VBB can also be used to AC couple an input signal.

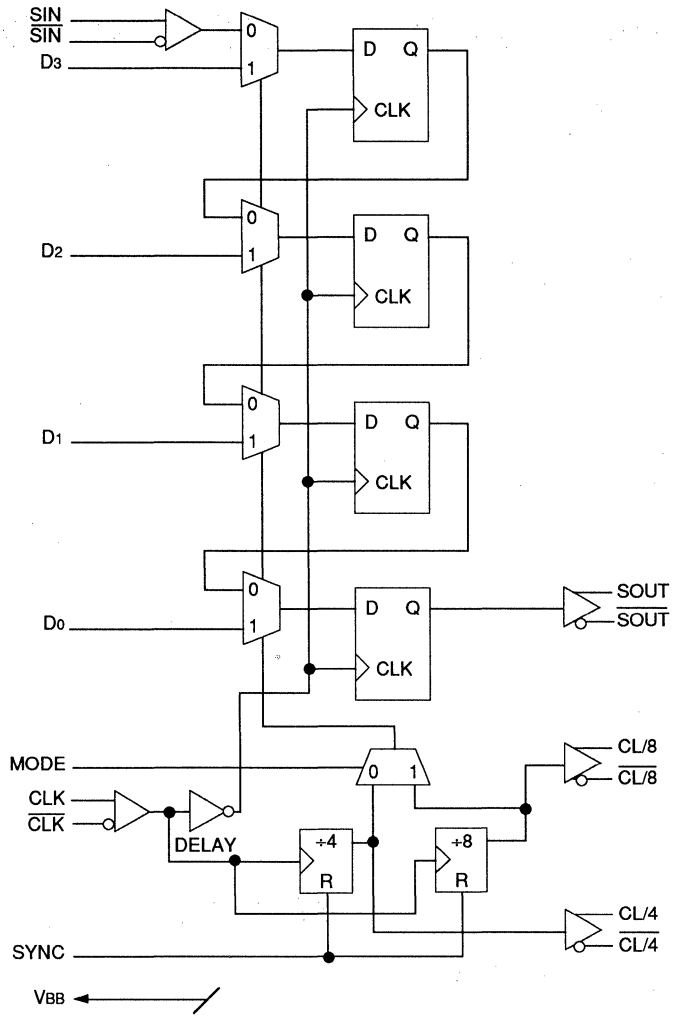
TRUTH TABLE

Mode	Conversion
L	4-Bit
H	8-Bit

4

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
V_{OH}	Output HIGH Voltage										V	1
	10E (SOUT Only)	–1020	—	–790	–980	—	–760	–910	—	–670		
	100E (SOUT Only)	–1025	—	–830	–1025	—	–830	–1025	—	–830		
V_{BB}	Output Reference Voltage										V	—
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{EE}	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		

NOTE:

1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

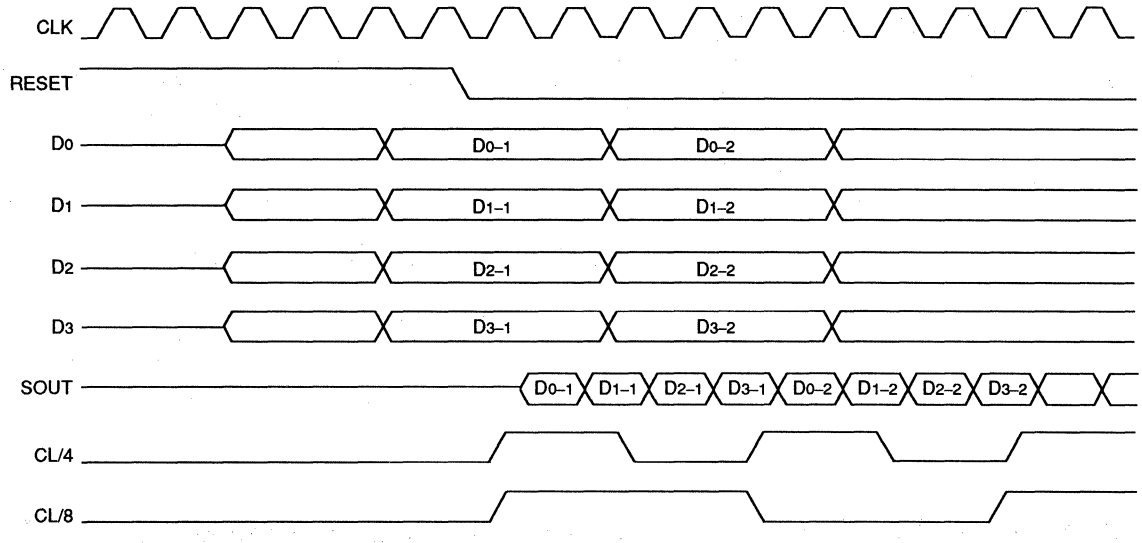
4

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

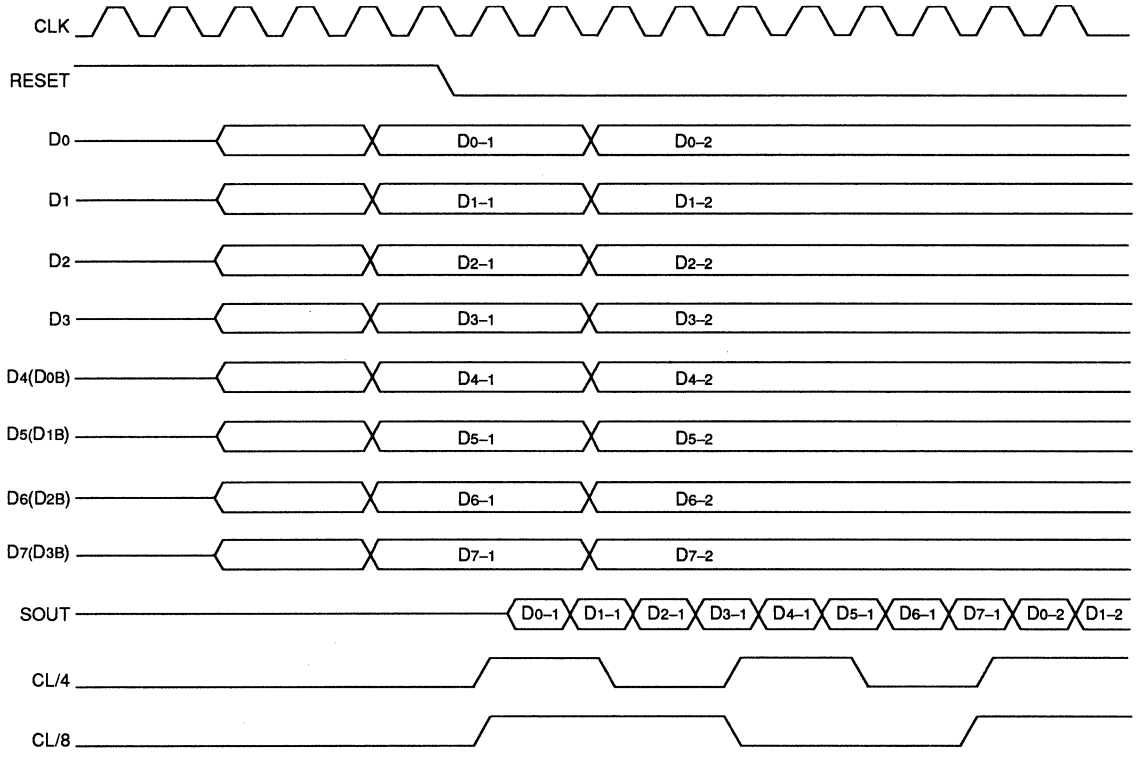
Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Conversion Frequency	1.3	1.6	—	1.3	1.6	—	1.3	1.6	—	Gb/s NRZ	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK to SOUT	1000	1400	1700	1000	1400	1700	1000	1400	1700		
	CLK to CL/4	500	800	1100	500	800	1100	500	800	1100		
	CLK to CL/8	800	1100	1400	800	1100	1400	800	1100	1400		
	SYNC to CL/4, CL/8	500	800	1100	500	800	1100	500	800	1100		
t_s	Set-up Time										ps	—
	SIN	–200	–400	—	–200	–400	—	–200	–400	—		
	D_n	–200	–400	—	–200	–400	—	–200	–400	—		
	Mode	0	–250	—	0	–250	—	0	–250	—		
t_h	Hold Time										ps	—
	SIN	750	550	—	750	550	—	750	550	—		
	D_n	800	600	—	800	600	—	800	600	—		
	Mode	500	300	—	500	300	—	500	300	—		
t_{RR}	Reset Recovery Time	500	200	—	500	200	—	500	200	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_r	Rise/Fall Time										ps	20–80%
t_f	SOUT	100	225	350	100	225	350	100	225	350		
	Other	200	425	650	200	425	650	200	425	650		

TIMING DIAGRAMS



Timing Diagram A. 4:1 Parallel-to-Serial Conversion

TIMING DIAGRAMS (CONTINUED)



Timing Diagram B. 8:1 Parallel-to-Serial Conversion

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E446JC	J28-1	Commercial
SY100E446JC	J28-1	Commercial

APPLICATIONS INFORMATION

The SY10E/100E446 are integrated 4:1 parallel-to-serial converters. The chips are designed to work with the E445 device to provide both transmission and receiving of a high-speed serial data path. The E446 can convert 4 bits of data into a 1.3Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see Timing Diagram A). Note that SOUT is triggered by negative clock edges.

The E446 features a differential serial input and internal divide-by-eight circuitry to facilitate the cascading of two devices to build an 8:1 multiplexer. Figure 1 illustrates the architecture for an 8:1 multiplexer using two E446s (see Timing Diagram B). Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock-to-serial output propagation delay, plus the set-up time of the serial input pins, must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, t_{PD} CLK to SOUT = 1600ps and t_S for SIN = –200ps, yields a minimum period of 1400ps or a clock frequency of 700MHz.

The clock frequency is somewhat lower than that of a single converter. In order to increase this frequency, it is recommended that the clock edge feeding the E446A be delayed with respect to the E446B, as shown in Figure 2.

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E446. By connecting the clock for E446A to the complimentary clock input pin, the device will clock a half a clock period after E446B (Figure 2). Utilizing this simple technique will raise the potential conversion frequency up to the maximum 1.3GHz of a stand-alone E446.

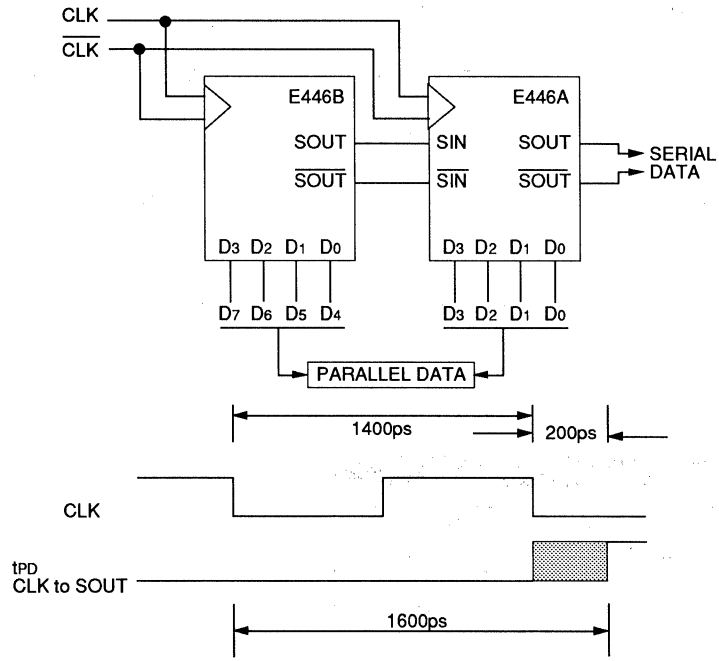


Figure 1. Cascaded 8:1 Converter Architecture

APPLICATIONS INFORMATION (CONTINUED)

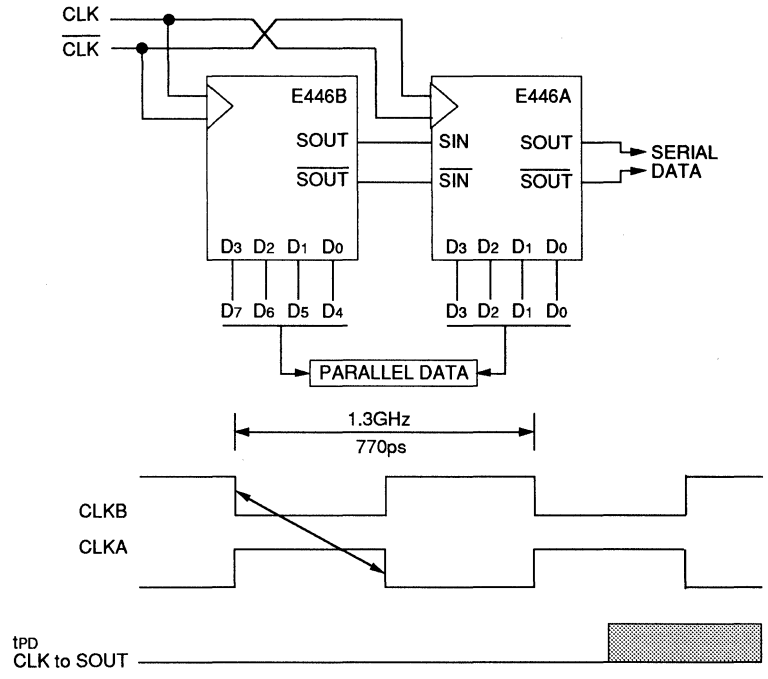


Figure 2. Extended Frequency 8:1 Converter Architecture

SYNERGY SEMICONDUCTOR

6-BIT REGISTER DIFFERENTIAL DATA AND CLOCK

SY10E451
SY100E451

FEATURES

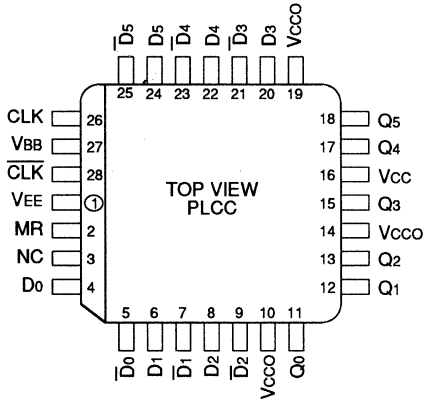
- **1100MHz min. toggle frequency**
- **Differential inputs: data and clock**
- **VBB output for single-ended use**
- **Asynchronous Master Reset**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E451**

DESCRIPTION

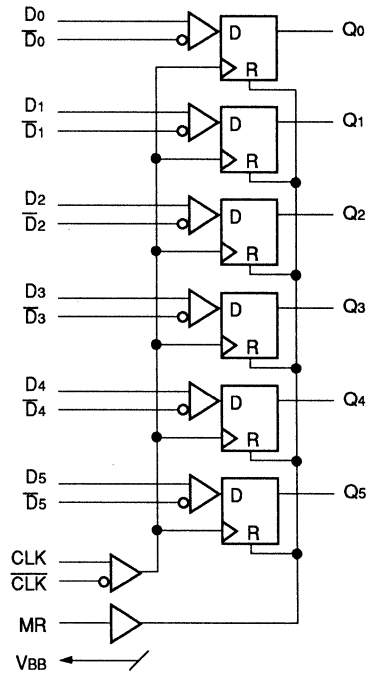
The SY10E451 and SY100E451 offer six D-type flip-flops with single-ended outputs and differential data and clock inputs, designed for use in new, high-performance ECL systems. The registers are triggered by the rising edge of the CLK input.

A logic HIGH on the Master Reset (MR) input resets all outputs to a logic LOW. The VBB output is provided for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01µF capacitor.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0–D5	+ Data Input
D0–D5	– Data Input
CLK	+ Clock Input
CLK	– Clock Input
MR	Master Reset Input
VBB	VBB Output
Q0–Q5	Data Outputs

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Issue Date: February, 1994

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = 25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Ty+p.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19		
	100E	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	84	101	—	84	101	—	84	101		
	100E	—	84	101	—	84	101	—	97	116		
V_{CMR}	Common Mode Range	−2.0	—	−0.4	−2.0	—	−0.4	−2.0	—	−0.4	V	1

NOTE:

1. V_{CMR} is referenced to the most psitive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than $V_{PP(min)}$ and < 1V.

4

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK (Diff)	475	650	800	475	650	800	475	650	800		
	CLK (SE)	425	650	850	425	650	850	425	650	850		
	MR	425	600	850	425	600	850	425	600	850		
t_S	Se-tup Time, D	150	−100	—	150	−100	—	150	−100	—	ps	—
t_H	Hold Time, D	250	100	—	250	100	—	250	100	—	ps	—
V_{PP} (AC)	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	1
t_{RR}	Reset Recovery Time	750	600	—	750	600	—	750	600	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	2
t_r t_f	Rise/Fall Time 20% to 80%	275	450	800	275	450	800	275	450	800	ps	—

NOTES:

1. Minimum input voltage for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E451JC	J28-1	Commercial
SY100E451JC	J28-1	Commercial

5-BIT DIFFERENTIAL REGISTER

FEATURES

- **Differential D, CLK and Q**
- **VBB output for single-ended use**
- **1100MHz min. toggle frequency**
- **Asynchronous Master Reset**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E452**

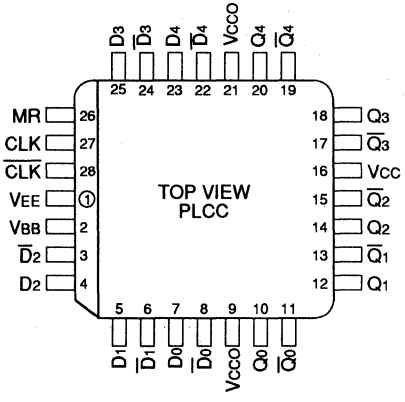
DESCRIPTION

The SY10E452 and SY100E452 are 5-bit differential registers with differential data (inputs and outputs) and clock. The registers are triggered by a positive transition of the positive clock (CLK) input. A high on the Master Reset (MR) asynchronously resets all registers so that the Q outputs go LOW.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the devices. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge-triggered flip-flop nature of the devices, simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state.

The fully differential design of the devices makes them ideal for very high frequency applications where a registered data path is necessary.

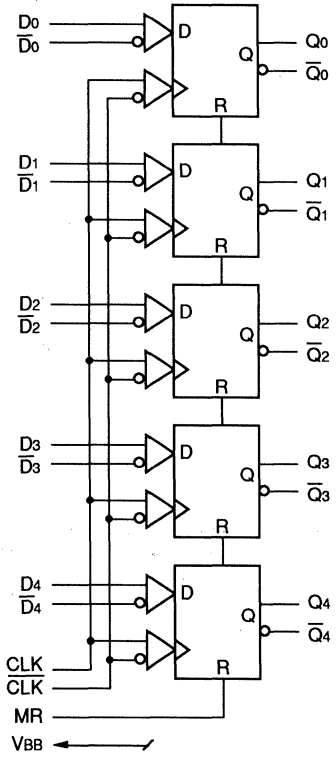
PIN CONFIGURATION



PIN NAMES

Pin	Function
D[0:4], $\overline{D}$[0:4]	Differential Data Inputs
MR	Master Reset Input
CLK, $\overline{CLK}$	Differential Clock Input
VBB	VBB Reference Output
Q[0:4], $\overline{Q}$[0:4]	Differential Data Outputs

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	74	89	—	74	89	—	74	89		
	100E	—	74	89	—	74	89	—	85	102		
V_{CMR}	Common Mode Range	–2.0	—	–0.4	–2.0	—	–0.4	–2.0	—	–0.4	V	1

NOTE:

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

4

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK (Diff)	475	600	800	475	600	800	475	600	800		
	CLK (SE)	425	600	850	425	600	850	425	600	850		
	MR	425	625	850	425	625	850	425	625	850		
t_S	Set-up Time, D	150	–50	—	150	–50	—	150	–50	—	ps	—
t_H	Hold Time, D	200	50	—	200	50	—	200	50	—	ps	—
t_{RR}	Reset Recovery Time	700	450	—	700	450	—	700	450	—	ps	—
t_{PW}	Minimum Pulse Width										ps	—
	CLK	400	—	—	400	—	—	400	—	—		
	MR	400	—	—	400	—	—	400	—	—		
t_{SKEW}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
$V_{PP(AC)}$	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	2
t_r t_f	Rise/Fall Time 20–80%	275	475	675	275	475	675	275	475	675	ps	—

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E452JC	J28-1	Commercial
SY100E452JC	J28-1	Commercial

TRIPLE DIFFERENTIAL 2:1 MULTIPLEXER

FEATURES

- **Differential D and Q**
- **V_{BB} output for single-ended use**
- **700ps max. propagation delay**
- **High frequency outputs**
- **Separate and common select**
- **Extended 100E V_{EE} range of –4.2V to –5.46V**
- **Internal 75KΩ input pulldown resistors**
- **ESD protection of 2000V**

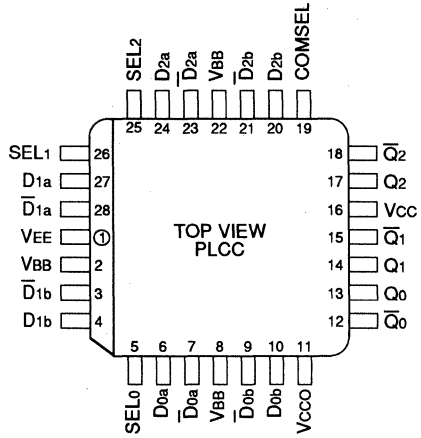
DESCRIPTION

The SY10E457 and SY100E457 are 3-bit differential 2:1 multiplexers. The fully differential data path makes the devices ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided to ease AC coupling input signals.

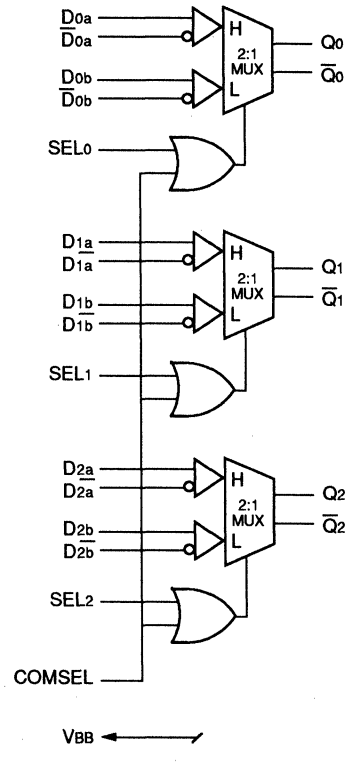
The higher frequency outputs provide the device with a >1.0GHz bandwidth to meet the needs of the most demanding system clock.

Both separate selects and a common select are provided to make the device well suited for both data path and random logic applications.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_n[0:2], $\overline{D}_n$[0:2]	Differential Data Inputs
SEL	Individual Select Input
COMSEL	Common Select Input
V_{BB}	V_{BB} Reference Output
Q[0:2], $\overline{Q}$[0:2]	Differential Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage										V	—
	10E	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19		
	100E	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	92	110	—	92	110	—	92	110		
	100E	—	92	110	—	92	110	—	106	127		
V_{PP} (DC)	Input Sensitivity	50	—	—	50	—	—	50	—	—	mV	1
V_{CMR}	Common Mode Range	−1.5	—	0	−1.5	—	0	−1.5	—	0	V	2

NOTE:

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP} (min.) and <1V.

4

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D (Diff)	375	475	650	375	475	650	375	475	650		
	D	325	475	700	325	475	700	325	475	700		
	SEL	350	500	725	350	500	725	350	500	725		
	COMSEL	375	525	750	375	525	750	375	525	750		
t_{SKEW}	Within-Device Skew	—	40	—	—	40	—	—	40	—	ps	1
t_{SKEW}	Duty Cycle Skew t_{PLH}–t_{PHL}	—	±10	—	—	±10	—	—	±10	—	ps	2
V_{PP} (AC)	Minimum Input Swing	150	—	—	150	—	—	150	—	—	mV	3
t_r	Rise/Fall Time	150	275	450	150	275	450	150	275	450	ps	—
t_f	20–80%											

NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Duty cycle skew guarantee holds only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E457JC	J28-1	Commercial
SY100E457JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

DUAL ANALOG COMPARATOR W/LATCH

ADVANCE INFORMATION
SY10E1651

FEATURES

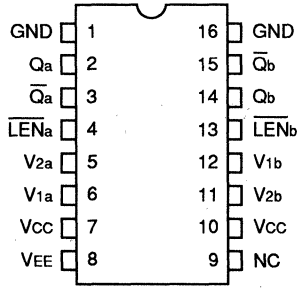
- **Typical 3.0dB bandwidth >1GHz**
- **Typical V to Q propagation delay of 850ps**
- **Typical output rise/fall of 300ps**
- **Common mode range –2.0V to +3.0V**
- **Individual latch enables**
- **Differential outputs**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E1651**

DESCRIPTION

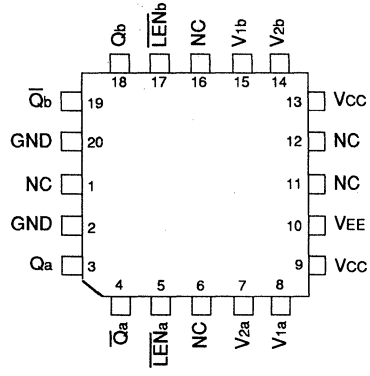
The SY10E1651 is pin-for-pin and functionally compatible with the MC1651 in the MECL III™ family, but is fabricated using Synergy's proprietary ASSET™ bipolar process.

The part has been designed with the goal of minimizing variations in propagation delay versus the amount of input overdrive. The output voltage levels are compatible with 10KH (and 10E) standard logic devices.

PIN CONFIGURATIONS

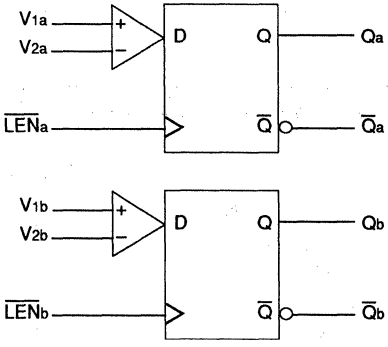


DIP
TOP VIEW



PLCC
TOP VIEW

BLOCK DIAGRAM



VEE = –5.2V
VCC = +5.0V

TRUTH TABLE

$\overline{LEN}$	V1, V2	Q
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

PIN NAMES

Pin	Function
V1, V2	Data Inputs
LEN	Latch Enable Input
Q	Data Outputs

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MECL is a trademark of Motorola Inc.

Rev.: A Amendment: /0
Issue Date: February, 1994

ABSOLUTE MAXIMUM RATING[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SUP}	Total Supply Voltage $\|V_{EE}\| + \|V_{CC}\|$	—	—	12.0	V
V_{PP}	Differential Input Voltage $\|V_1 - V_2\|$	—	—	3.0	V

NOTE:
1. Beyond which device life may be impaired.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –5.2V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1020	—	–840	–980	—	–810	–920	—	–735	mV
V_{OL}	Output LOW Voltage	–1950	—	–1630	–1950	—	–1630	–1950	—	–1600	mV
I_I	Input Current (V_1, V_2)	—	—	65	—	—	65	—	—	65	µA
I_{IH}	Input HIGH Current ($\overline{LEN}$)	—	—	150	—	—	150	—	—	150	
I_{CC}	Positive Supply Current	—	—	50	—	—	50	—	—	50	mA
I_{EE}	Negative Supply Current	—	—	–55	—	—	–55	—	—	–55	
V_{CMR}	Common Mode Range	–2.0	—	3.0	–2.0	—	3.0	–2.0	—	3.0	V

AC ELECTRICAL CHARACTERISTICS

V_{EE} = –5.2V ± 5%; V_{CC} = +5.0V ± 5%

		0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	V to Q	600	850	1150	600	850	1150	600	850	1150	
	$\overline{LEN}$ to Q	500	750	950	500	750	950	500	750	950	
t_r	Rise/Fall Times (20 – 80%)	200	300	700	200	300	700	200	300	700	ps
t_f											

DUAL ANALOG COMPARATOR W/LATCH

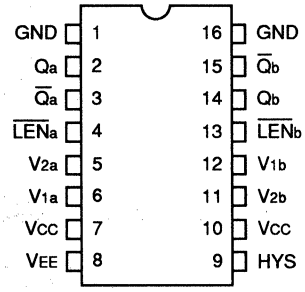
FEATURES

- **Typical 3.0dB bandwidth >1GHz**
- **Typical V to Q propagation delay of 850ps**
- **Typical output rise/fall of 300ps**
- **Common mode range –2.0V to +3.0V**
- **Individual latch enables**
- **Differential outputs**
- **User-controlled input hysterisis**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E1652**

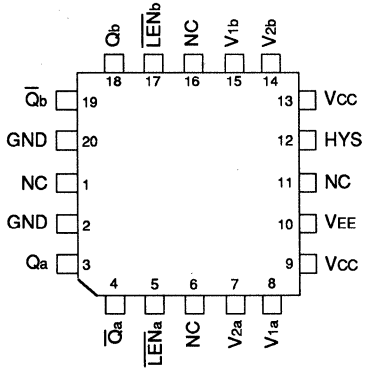
DESCRIPTION

The SY10E1652 is functionally compatible with the SY10E1651 and is fabricated using Synergy's proprietary ASSET™ bipolar process. The hysterisis control pin, HYS, allows the user to define the amount of input hysterisis; whereas, the SY10E1651 has a built-in fixed level of input hysterisis. The device comes in a 10E version only, thus the outputs are only compatible with 10KH logic devices. The device is available in both a 16-pin DIP and a 20-pin PLCC surface mount package.

PIN CONFIGURATIONS



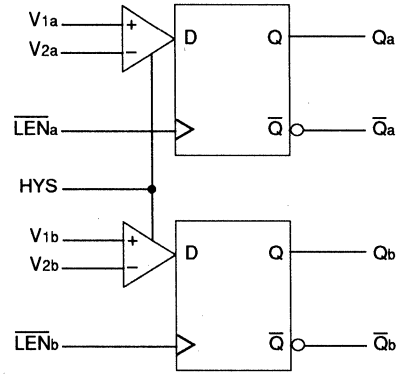
DIP
TOP VIEW



PLCC
TOP VIEW

ASSET is a trademark of Synergy Semiconductor Corporation.

BLOCK DIAGRAM



VEE = –5.2V
VCC = +5.0V

TRUTH TABLE

$\overline{LEN}$	V1, V2	Q
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

PIN NAMES

Pin	Function
V1, V2	Data Inputs
LEN	Latch Enable Inputs
HYS	Hysteresis Control Input
Q	Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

ABSOLUTE MAXIMUM RATING[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SUP}	Total Supply Voltage $\|V_{EE}\| + \|V_{CC}\|$	—	—	12.0	V
V_{PP}	Differential Input Voltage $\|V_1 - V_2\|$	—	—	3.0	V

NOTE:

1. Beyond which device life may be impaired.

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -5.2V \pm 5\%$; $V_{CC} = +5.0V \pm 5\%$

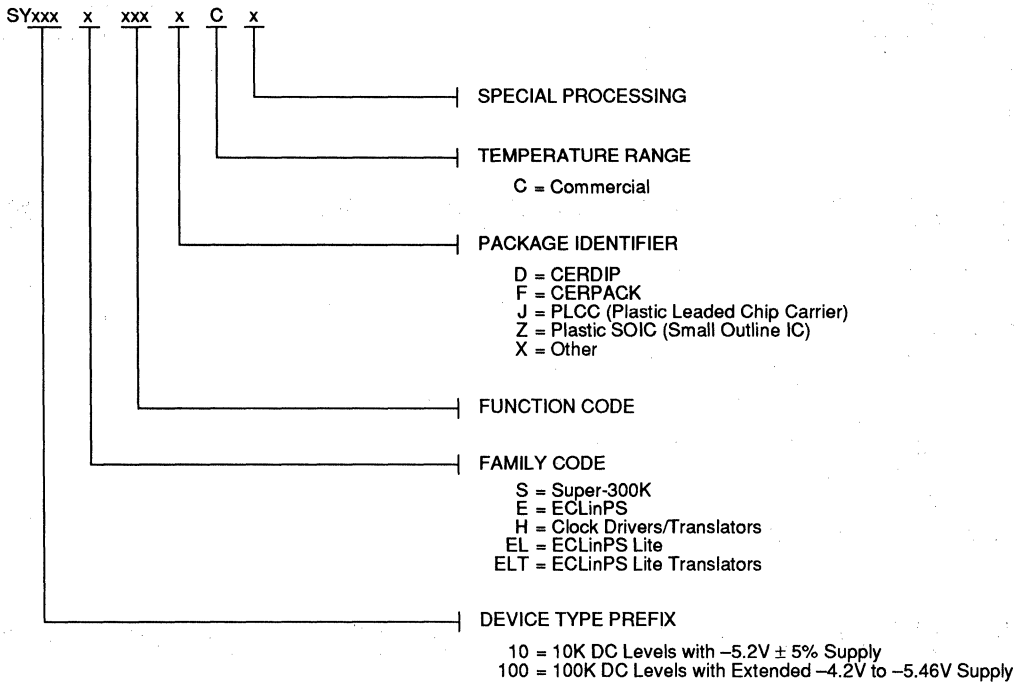
		0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1020	—	–840	–980	—	–810	–920	—	–735	mV
V_{OL}	Output LOW Voltage	–1950	—	–1630	–1950	—	–1630	–1950	—	–1600	mV
I_I	Input Current (V_1, V_2)	—	—	65	—	—	65	—	—	65	µA
I_{IH}	Input HIGH Current ($\overline{LEN}$)	—	—	150	—	—	150	—	—	150	
I_{CC}	Positive Supply Current	—	—	50	—	—	50	—	—	50	mA
I_{EE}	Negative Supply Current	—	—	–55	—	—	–55	—	—	–55	
V_{CMR}	Common Mode Range	–2.0	—	3.0	–2.0	—	3.0	–2.0	—	3.0	V

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -5.2V \pm 5\%$; $V_{CC} = +5.0V \pm 5\%$

		0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	V to Q	600	850	1150	600	850	1150	600	850	1150	
	$\overline{LEN}$ to Q	500	750	950	500	750	950	500	750	950	
t_r	Rise/Fall Times (20 – 80%)	200	300	700	200	300	700	200	300	700	ps
t_f											

LOGIC ORDERING INFORMATION



Rev.: B Amendment: /0
Issue Date: February, 1994

ECLinPS LITE™ LOGIC

PAGE

ECLINPS Lite™ Logic

5

FEATURES

- **275ps package gate delays**
- **2.0GHz+ flip-flop toggle frequencies**
- **Space efficient 8-lead SOIC package**
- **Choice of ECL compatibility: MECL 10H™ (10EL); or ECL 100K (100EL)**
- **Flow-through pinouts**
- **Specified over industrial temperature range: –40°C to +85°C**
- **Extended VEE range for both 10EL and 100EL devices**

NUMERIC INDEX

SY10/100	Function
EL01	4-Input OR/NOR
EL04	2-Input AND/NAND
EL05	2-Input Differential AND/NAND
EL07	2-Input XOR/XNOR
EL11	1:2 Differential Fanout Buffer
EL12	Low Impedance Driver
EL16	Differential Line Receiver
EL31	D Flip-Flop with Set and Reset
EL32	Integrated ÷2 Divider, Differential Input
EL33	Integrated ÷4 Divider, Differential Input
EL35	JK Flip-Flop
EL51	D Flip-Flop with Reset and Differential Clock
EL52	D Flip-Flop with Differential Data and Clock
EL58	2:1 Multiplexer
EL89(1)	Coaxial Cable Driver

NOTE:

1. Available in 10EL version only.

DESCRIPTION

ECLinPS Lite is a family of single, essential logic primitives — gates, muxes, flops, etc. — housed in a space-efficient, cost-effective standard package, the 8-lead SOIC. Packaged gates switch in 250ps typical, with flops toggling at over 2GHz.

ECLinPS Lite, being a single gate family, offers better AC specs and tighter skews than even the ECLinPS™ family. At the same time, the family provides superior isolation over multiple gate logic. Its small package size makes it ideal for pin cards and other applications that require density, but not at the expense of signal integrity.

Synergy's ECLinPS Lite family utilizes the same ASSET™ technology as the ECLinPS family to provide state-of-the-art bipolar process speeds. The small outline SOIC package and special design techniques serve to enhance the level of performance even further. The 8-lead SOIC package shaves over 50% from the propagation delay associated with the ECLinPS family's 28-lead PLCC package. In addition, special design techniques have been applied to decrease output transition times by nearly 50%, resulting in nearly a 100% improvement in bandwidth and toggle frequencies over a standard ECLinPS device.

Like the ECLinPS family, all ECLinPS Lite devices, except the EL89, are offered in 10EL and 100EL versions for compatibility with the two existing ECL standards, ECL 10H and ECL 100K, respectively. As with the ECLinPS family, the AC performance of the two versions of ECLinPS Lite devices are identical, therefore AC performance will not be a factor in choosing an ECL standard.

The VEE power supply range for both ECLinPS Lite versions has been extended beyond the levels defined in the original ECL standard specifications. The lower end of the 100EL VEE limit has been decreased to –5.5V to allow for interfacing with three level series gated 100K arrays. In addition, the upper end of the 10EL VEE limit has been increased to –4.75V to allow for use in PECL designs which use a 5V ± 5% supply. Note the –4.75V VEE for 10EL devices does not always hold for temperatures less than +25°C (see individual data sheets). Therefore, for PECL designs whose environments can fall below +25°C, it is recommended that the 100EL devices be used to allow the designer to choose functions from the entire family.

The transfer curves, switching waveforms and parameter definitions are identical to those of the ECLinPS family. In addition, the application of ECLinPS Lite devices in a system follows the same rules as previous ECL families.

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Rev.: B Amendment: /0
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10EL SERIES DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND[2]

		–40°C		0°C		+25°C		+85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

NOTE:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

100EL SERIES DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND[2]

		–40°C			0°C to +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620		or V_{IL} (Min.)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(Max.)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610		or V_{IL}(Min.)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	—
V_{IL}	Input LOW Voltage	–1810	—	–1475	–1810	—	–1475	mV	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(Max.)

NOTE:

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)		–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)		0 to –6.0	VDC
I_{OUT}	Output Current:	Continuous Surge	50 100	mA
T_A	Operating Temperature Range		–40 to +85	°C
V_{EE}[2]	Operating Range		–5.7 to –4.2	V

NOTES:

1. Absolute maximum rating, beyond which device life may be imparied unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

APPLICATIONS INFORMATION

Introduction

The ECLinPS Lite family of products is very similar in design and performance as the multi-gate ECLinPS family. The following paragraphs will be used to describe behavior that is unique to the ECLinPS Lite family.

Maximum Frequency/Bandwidth

One of the goals of the ECLinPS Lite family was to provide means for using ECL in even higher frequency applications. Much effort was placed in the reduction of the output transition times, as these were the limiting factors of the frequency capability of the original ECLinPS family. With a nearly 50% reduction in output edge rates, the ECLinPS Lite family's frequency capability is nearly twice that of the ECLinPS devices.

The data sheets for the flip-flop devices state maximum toggle frequencies of 2.2GHz. Although impressive, these values tend to underestimate the useful bandwidth of the device. Similarly, the buffer devices have a 3db bandwidth (600mV output swing) of about 1.4GHz; however, the devices can be useful to frequencies well above 2GHz. The ECLinPS Lite device performance can be maximized by taking advantage of the differential I/O functions. From the data sheets for the differential devices, the minimum input swing is 150mV, a value significantly lower than the somewhat arbitrary 600mV output chosen as the f_{MAX} fail criteria. Figure 1 illustrates several ECLinPS Lite devices' output eye voltage versus input frequency. Note for the buffer type devices the outputs produce a 150mV eye pattern for frequencies well over 3GHz.

It may be argued that 150mV input swings leave no noise margins for the design. When analyzed further, this is not the case. For single-ended interconnect, the worst case noise margins are ≈150mV with no common mode noise rejection capabilities. For a 150mV differential input, the same 150mV of noise margin exists; however, in this case, the interface also has common mode noise rejection capability and, thus, may provide a safer environment than a standard single-ended interface.

The purpose of this discussion is to illustrate the potential of using ECLinPS Lite devices at frequencies well above the stated maximum limits. The criteria for establishing the maximum frequency of a device was determined with single-ended interfaces in mind; however, in the 1GHz+ realm of designs, differential interconnect is predominant. For differential interconnect systems, the criteria for f_{MAX} needs to be redefined to better describe the reliable operating frequency range of a device. Under this new set of criteria, the ECLinPS Lite family can be pushed well above 2.5GHz and, thus, provide a cost-effective means for processing very high-speed signals.

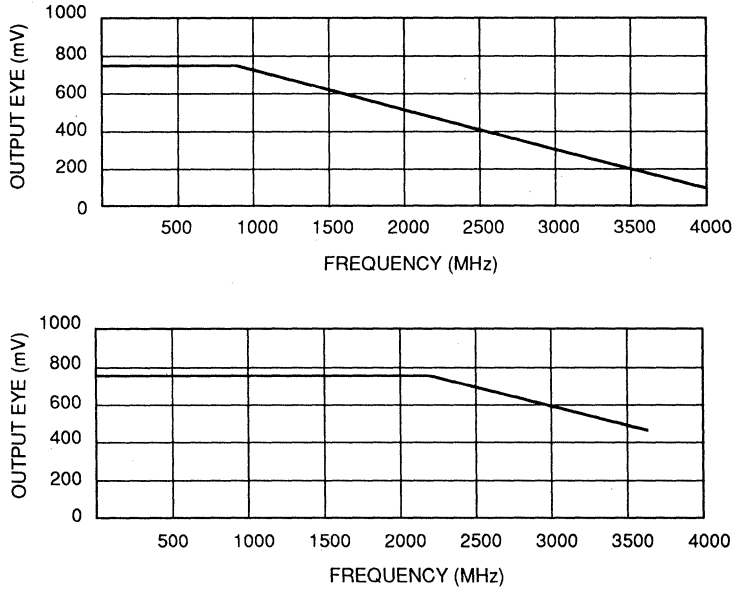


Figure 1. Eye Pattern versus Frequency

Using ECLinPS Lite in PECL Designs

PECL is an acronym for Positive ECL and simply represents using standard ECL devices in a +5V environment. All of the ECLinPS Lite devices, as with the majority of all ECL devices, will operate as specified when positive power supplies are used. The reason for the use of negative power supplies with ECL is due to the fact that the output levels and internal bias levels are VCC rail referenced. Because ground is simpler to keep quiet than a power supply, it was the natural choice for the VCC bias. Because the output levels vary 1:1 with VCC, differences in power supply levels between transmitter and receiver can be problematic. These problems can be eliminated if differential interconnect is used.

With its small size and low power, the ECLinPS Lite family of products will naturally find applications in PECL form in otherwise TTL or CMOS systems. Many of these applications will be in the area of clock distribution. Because minimizing skew is the most important aspect of clock distribution, differential interconnect should be used. This not only minimizes skew but, as previously mentioned, it also eliminates problems due to VCC variation in PECL designs.

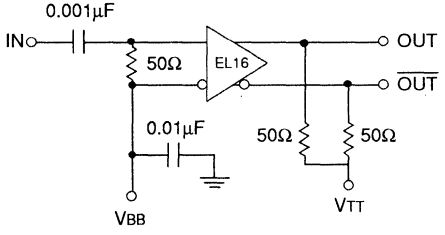


Figure 2. AC Coupling Architecture

An important aspect of using ECLinPS Lite in clock distribution schemes is in the interface to the clock source. By taking advantage of the AC coupling capability of the EL16, ECLinPS Lite products can be interfaced to clock sources which generate other than ECL-compatible outputs. Probably the most cost-efficient and simplest oscillators to choose are sinusoidal oscillators. By using the architecture of Figure 2, a sinusoidal oscillator can be used to drive ECLinPS Lite devices. The only criteria is that the amplitude of the oscillator input not exceed the upper or lower end of the CMR range when centered on the VBB reference. A larger amplitude oscillator output can be used if a lower DC bias is used or if the output is divided down prior to being coupled into the EL16.

Input Clamp Circuitry and CMR Range

To maintain stability during open input situations, all of the differential input devices employ input clamping circuitry. Because all of the inputs of ECLinPS Lite devices have internal input pulldown resistors, when left open, the inputs will pull down to VEE. A clamp voltage will take control of the input buffer when both inputs pull lower than the clamp voltage. This clamp voltage does place a lower bound on the CMR range of a device. In the ECLinPS Lite family, the internal clamp voltage is referenced to the VEE power rail. As a result, if a larger CMR range is necessary, the VEE of a device can be lowered. Each incremental lowering of VEE will increase the CMR range by an equivalent amount.

Package Information

The package chosen for the ECLinPS Lite family is the standard 8-lead SOIC package. The 8-lead SOIC is a plastic surface mount package with gull wing, 50mil pitch leads. Figure 3 illustrates the recommended PCB solder pads for the 8-lead SOIC and refer to Chapter 11 for the various package dimensions.

Because the SOIC is a plastic package, the long term reliability of a device is going to be dependent on the operating junction temperature. As the junction temperature of the device increases, an intermetallic is formed between the gold bond wire and the aluminum bonding pad. This intermetallic eventually causes a void to develop and the affected pin to become an open circuit.

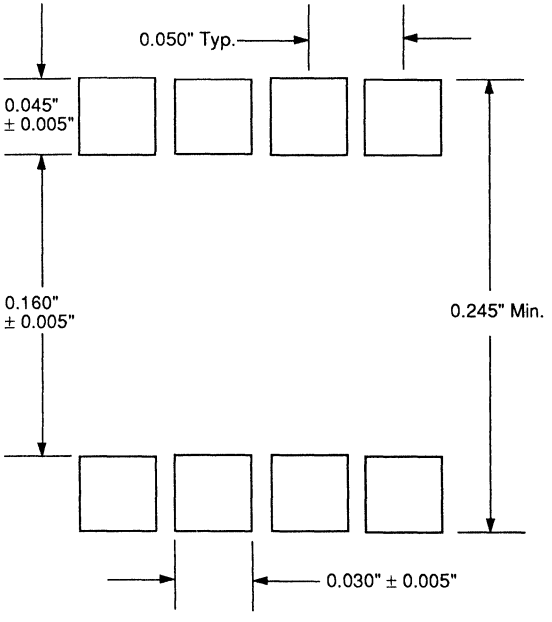


Figure 3. 8-Lead SOIC Solder Pad Dimensions

The 8-lead SOIC exhibits a thermal resistance, as pictured in Figure 4. With this information, as well as the power dissipation of the device in question, the approximate junction temperature and, thus theoretical lifetime, can be estimated. ECLinPS Lite devices are designed with chip power levels that permit acceptable reliability levels, in most systems, under the conventional 500lfpm (2.5m/s) airflow. In fact, for all systems but those that operate at the maximum allowed ambient temperatures, ECLinPS Lite devices will prove reliable with little or no cooling airflow.

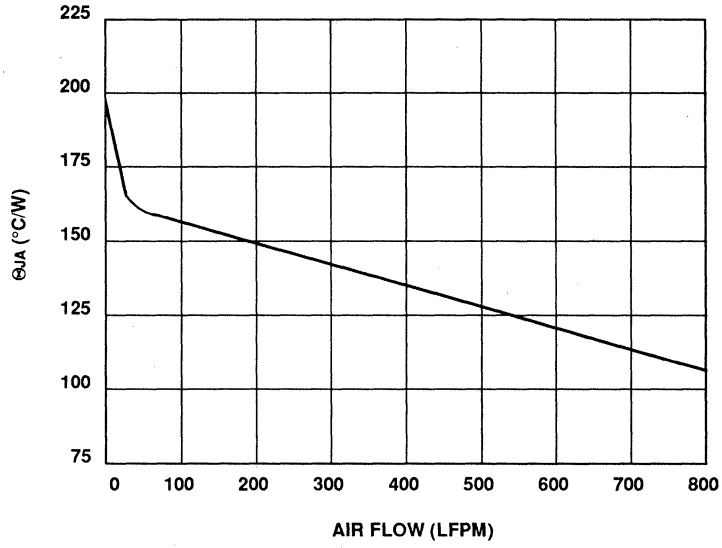


Figure 4. 8-Lead SOIC Thermal Resistance

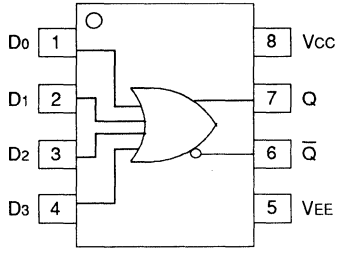
FEATURES

- **230ps propagation delay**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL01 are 4-input OR/NOR gates. These devices are functionally equivalent to the E101 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E101, the EL01 is ideally suited for those applications which require the ultimate in AC performance.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D0–D3	Data Inputs
Q	Data Outputs

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL01ZC	Z8-1	Commercial
SY100EL01ZC	Z8-1	Commercial

5

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	14	—	11	14	17	11	14	17	11	14	17	
	100EL	—	14	—	11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	220	—	120	220	320	130	230	330	150	250	350	ps
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

Rev.: B Amendment: /0
Issue Date: April, 1994

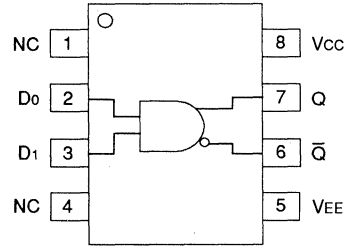
FEATURES

- **240ps propagation delay**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 200V**

DESCRIPTION

The SY10EL/100EL04 are 2-input AND/NAND gates. These devices are functionally equivalent to the E104 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E104, the EL04 is ideally suited for those applications which require the ultimate in AC performance.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D_0, D_1	Data Inputs
Q	Data Outputs

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL04ZC	Z8-1	Commercial
SY100EL04ZC	Z8-1	Commercial

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	−40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	14	—	11	14	17	11	14	17	11	14	17	
	100EL	—	14	—	11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage													V
	10EL	−4.94	−5.2	−5.5	−4.94	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	
	100EL	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	
I_{IH}	Input HIGH Current													µA
	D_0	—	—	250	—	—	250	—	—	250	—	—	250	
	D_1	—	—	150	—	—	150	—	—	150	—	—	150	

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	−40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	235	—	120	235	360	130	240	370	155	265	395	ps
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

Rev.: B Amendment: /0
Issue Date: April, 1994

2-INPUT DIFFERENTIAL AND/NAND

FEATURES

- **275ps propagation delay**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

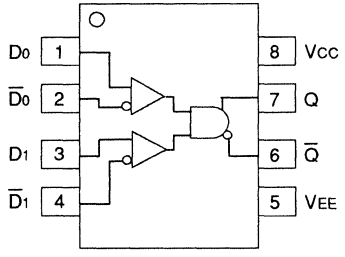
DESCRIPTION

The SY10EL/100EL05 are 2-input differential AND/NAND gates. These devices are functionally equivalent to the E404 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E404, the EL05 is ideally suited for those applications which require the ultimate in AC performance.

Because a negative 2-input NAND is equivalent to a 2-input OR function with inverted inputs, the differential inputs and outputs of the device allows the EL05 to also be used as a 2-input differential OR/NOR gate.

The differential inputs employ clamp circuitry so that, under open conditions (pulled down to V_{EE}), the input to the AND gate will be HIGH. In this way, if one set of inputs is open, the gate will remain active to the other input.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D_0, D_1	Data Inputs
Q	Data Outputs

5

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	18	—	14	18	22	14	18	22	14	18	22	
	100EL	—	18	—	14	18	22	14	18	22	16	21	25	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

Rev.: B Amendment: /0
Issue Date: April, 1994

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	260	—	185	275	390	185	275	390	215	305	420	ps
V_{PP}	Minimum Input Swing(1)	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range(2)	–0.4	—	(2)	–0.4	—	(2)	–0.4	—	(2)	–0.4	—	(2)	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL05ZC	Z8-1	Commercial
SY100EL05ZC	Z8-1	Commercial

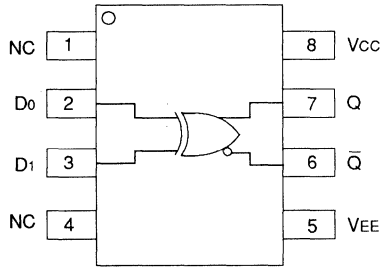
FEATURES

- 260ps propagation delay
- High bandwidth output transitions
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V

DESCRIPTION

The SY10EL/100EL07 are 2-input XOR/XNOR gates. These devices are functionally equivalent to the E107 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E107, the EL07 is ideally suited for those applications which require the ultimate in AC performance.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D_0, D_1	Data Inputs
Q	Data Outputs

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL07ZC	Z8-1	Commercial
SY100EL07ZC	Z8-1	Commercial

5

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{EE}	Power Supply Current													mA
	10EL	—	14	—	11	14	17	11	14	17	11	14	17	
	100EL	—	14	—	11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage													V
	10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current													µA
	D_0	—	—	250	—	—	250	—	—	250	—	—	250	
	D_1	—	—	150	—	—	150	—	—	150	—	—	150	

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	250	—	140	250	385	150	260	395	170	280	415	ps
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

Rev.: B Amendment: /0
Issue Date: April, 1994

FEATURES

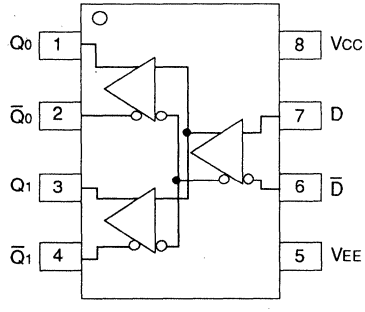
- **265ps propagation delay**
- **5ps skew between outputs**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL11 are 1:2 differential fanout gates. These devices are functionally similar to the E111 devices, with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the EL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the EL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}), the Q outputs will go LOW.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D	Data Inputs
Q_0, Q_1	Data Outputs

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	26	—	21	26	31	21	26	31	21	26	31	
	100EL	—	26	—	21	26	31	21	26	31	24	30	36	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

Rev.: B Amendment: /0
Issue Date: April, 1994

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	260	—	185	260	335	190	265	340	215	290	365	ps
t_{SKEW}	Within-Device Skew[1]	—	5	—	—	5	20	—	5	20	—	5	20	ps
	Duty Cycle Skew[2]	—	5	—	—	5	20	—	5	20	—	5	20	
VPP	Minimum Input Swing[3]	150	—	—	150	—	—	150	—	—	150	—	—	mV
VCMR	Common Mode Range[4]	–0.4	—	(4)	–0.4	—	(4)	–0.4	—	(4)	–0.4	—	(4)	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Within-device skew defined as identical transitions on similar paths through a device.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

5

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL11ZC	Z8-1	Commercial
SY100EL11ZC	Z8-1	Commercial

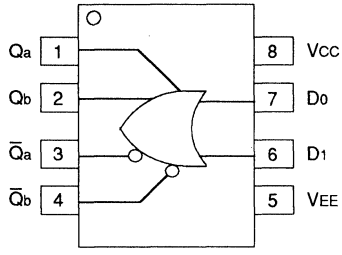
FEATURES

- **290ps propagation delay**
- **Dual outputs for 25Ω drive applications**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL12 are low-impedance drive buffers. With two pairs of OR/NOR outputs, the devices are ideally suited for high drive applications such as memory addressing. These devices are functionally equivalent to the E112 devices, with higher performance capabilities. With propagation delays significantly faster than the E112, the EL12 is ideally suited for those applications which require the ultimate in AC performance.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D_0, D_1	Data Inputs
Q_a, Q_b	Data Outputs

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL12ZC	Z8-1	Commercial
SY100EL12ZC	Z8-1	Commercial

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{EE}	Power Supply Current													mA
	10EL	—	14	—	11	14	17	11	14	17	11	14	17	
	100EL	—	14	—	11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage													V
	10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	280	—	170	280	450	180	290	450	210	320	480	ps
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	350	—	150	350	550	150	350	550	150	350	550	ps

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Issue Date: April, 1994

DIFFERENTIAL RECEIVER

FEATURES

- **250ps propagation delay**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

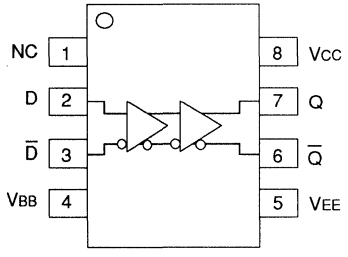
DESCRIPTION

The SY10EL/100EL16 are differential receivers. The devices are functionally equivalent to the E116 devices, with higher performance capabilities. With output transition times significantly faster than the E116, the EL16 is ideally suited for interfacing with high-frequency sources.

The EL16 provides a V_{BB} output for either single-ended use or as a DC bias for AC coupling to the device. The V_{BB} pin should be used only as a bias for the EL16 as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to ground via a 0.01µf capacitor.

Under open input conditions (pulled to V_{EE}), internal input clamps will force the Q output LOW.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D	Data Inputs
Q	Data Outputs
V_{BB}	Reference Voltage Output

5

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	18	—	14	18	22	14	18	22	14	18	22	
	100EL	—	18	—	14	18	22	14	18	22	16	21	26	
V_{BB}	Output Reference Voltage 10EL	–1.43	—	–1.30	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V
	100EL	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

Rev.: B Amendment: /0
Issue Date: April, 1994

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D (Diff)	—	250	—	175	250	325	175	250	325	205	280	355	ps
	D (SE)	—	250	—	125	250	375	125	250	375	155	280	405	
t_{SKEW}	Duty Cycle Skew[1] (Diff)	—	5	—	—	5	20	—	5	20	—	5	20	ps
VPP	Minimum Input Swing[2]	150	—	—	150	—	—	150	—	—	150	—	—	mV
VCMR	Common Mode Range[3]	–0.4	—	(3)	–0.4	—	(3)	–0.4	—	(3)	–0.4	—	(3)	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
2. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

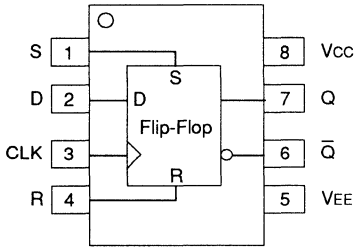
Ordering Code	Package Type	Operating Range
SY10EL16ZC	Z8-1	Commercial
SY100EL16ZC	Z8-1	Commercial

D FLIP-FLOP WITH SET & RESET

FEATURES

- **475ps propagation delay**
- **2.8GHz toggle frequency**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D	Data Inputs
Q	Data Outputs
S	Set
R	Reset
CLK	Clock Input

DESCRIPTION

The SY10EL/100EL31 are D flip-flops with set and reset. The devices are functionally equivalent to the E131 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E131, the EL31 is ideally suited for those applications which require the ultimate in AC performance.

Both the set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

TRUTH TABLE(1)

D	S	R	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	Undef

NOTE:
1. Z = LOW-to-HIGH transition.

5

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{EE}	Power Supply Current													mA
	10EL	—	23	—	18	27	32	18	27	38	18	27	32	
	100EL	—	23	—	18	27	32	18	27	38	21	31	37	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
f_{MAX}	Maximum Toggle Frequency	—	2.5	—	2.2	2.8	—	2.2	2.8	—	2.2	2.8	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK	—	465	—	365	465	580	375	475	590	430	530	645	ps
	S, R	—	455	—	345	455	580	355	465	590	400	510	645	
t_S	Set-up Time	—	0	—	150	0	—	150	0	—	150	0	—	ps
t_H	Hold Time	—	100	—	250	100	—	250	100	—	250	100	—	
t_{RR}	Set/Reset Recovery	400	200	—	400	200	—	400	200	—	400	200	—	ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400	—	—	400	—	—	400	—	—	400	—	—	ps
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL31ZC	Z8-1	Commercial
SY100EL31ZC	Z8-1	Commercial

FEATURES

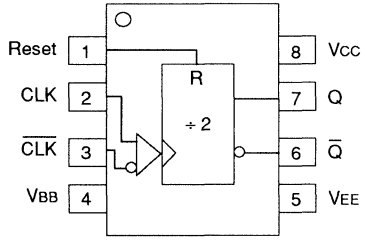
- **510ps propagation delay**
- **3.0GHz toggle frequency**
- **High bandwidth output transistions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL32 are integrated ÷2 dividers. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01µF capacitor. Also note that the VBB is designed to be used as an input bias on the EL32 only; the VBB output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-on, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32s in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
VBB	Reference Voltage Output
Q	Data Outputs

5

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	−40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	25	—	—	25	30	—	25	30	—	25	30	
	100EL	—	25	—	—	25	30	—	25	30	—	29	35	
VBB	Output Reference Voltage 10EL	−1.43	—	−1.30	−1.38	—	−1.27	−1.35	—	−1.25	−1.31	—	−1.19	V
	100EL	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26	−1.38	—	−1.26	
VEE	Power Supply Voltage													V
	10EL	—	−5.2	—	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	
	100EL	—	−4.5	—	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	—	3.0	—	2.6	3.0	—	2.6	3.0	—	2.6	3.0	—	GHz
t_{PLH} t_{PHL}	Prop Delay to Output D Reset to Q	— —	500 540	— —	410 440	500 540	590 640	420 440	510 540	600 640	450 450	540 550	630 650	ps
V_{PP}	Minimum Input Swing[1]	150	—	—	150	—	—	150	—	—	150	—	—	mV
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTE:

1. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL32ZC	Z8-1	Commercial
SY100EL32ZC	Z8-1	Commercial

FEATURES

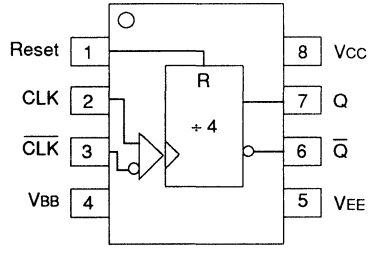
- **650ps propagation delay**
- **4.0GHz toggle frequency**
- **High bandwidth output transistions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL33 are integrated ÷4 dividers. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01µF capacitor. Also note that the VBB is designed to be used as an input bias on the EL33 only; the VBB output has limited current sink and source capability.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset input allows for the synchronization of multiple EL33s in a system.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Clock Inputs
Reset	Asynchronous Reset
VBB	Reference Voltage Output
Q	Data Outputs

5

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	-40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	27	—	—	27	33	—	27	33	—	27	33	
	100EL	—	27	—	—	27	33	—	27	33	—	31	37	
VBB	Output Reference Voltage													V
	10EL	-1.43	—	-1.30	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19	
	100EL	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	
VEE	Power Supply Voltage													V
	10EL	—	-5.2	—	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	
	100EL	—	-4.5	—	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
f_{MAX}	Maximum Toggle Frequency	—	4.2	—	3.8	4.2	—	3.8	4.2	—	3.8	4.2	—	GHz
t_{PLH} t_{PHL}	Prop. Delay to Output D Reset to Q	— —	630 460	— —	540 360	630 460	720 560	550 360	640 460	730 560	590 380	670 480	760 580	ps
VPP	Minimum Input Swing[1]	150	—	—	150	—	—	150	—	—	150	—	—	mV
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTE:

1. Minimum input swing for which AC parameters are guaranteed.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL33ZC	Z8-1	Commercial
SY100EL33ZC	Z8-1	Commercial

FEATURES

- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75KΩ input pull-down resistors
- ESD protection of 2000V

DESCRIPTION

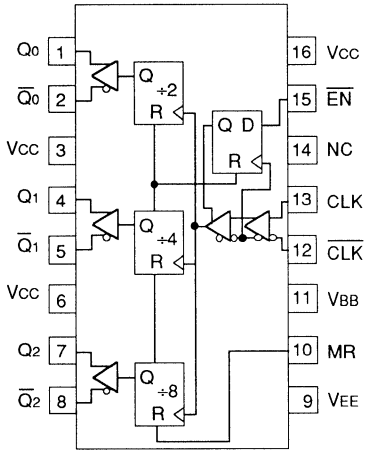
The SY10EL/100EL34 are low skew ÷2, ÷4, ÷8 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The VBB output is designed to act as the switching reference for the input of the EL34 under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34s in a system.

5

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
$\overline{EN}$	Synchronous Enable
MR	Master Reset
VBB	Reference Output
Q0	Differential ÷2 Outputs
Q1	Differential ÷4 Outputs
Q2	Differential ÷8 Outputs

TRUTH TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0–3
X	X	H	Reset Q0–3

NOTE:
Z = LOW-to-HIGH transition
ZZ = HIGH-to-LOW transition

Rev.: B Amendment: /0
Issue Date: April, 1994

AC/DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	65	—	—	65	—	—	65	—	—	65	—	mA
V_{BB}	Output Reference Voltage 10EL 100EL	–1.43 –1.38	— —	–1.30 –1.26	–1.38 –1.38	— —	–1.27 –1.26	–1.35 –1.38	— —	–1.25 –1.26	–1.31 –1.38	— —	–1.19 –1.26	V
I_{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR	— —	1100 800	— —	— —	1100 800	— —	— —	1100 800	— —	— —	1100 800	— —	ps
t_{SKEW}	Within-Device Skew	—	100	—	—	100	—	—	100	—	—	100	—	ps
t_S	Set-up Time $\overline{EN}$	—	150	—	—	150	—	—	150	—	—	150	—	ps
t_H	Hold Time $\overline{EN}$	—	150	—	—	150	—	—	150	—	—	150	—	ps
V_{PP}	Minimum Input Swing	250	—	—	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	Common Mode Range CLK	–2.0	—	–4.0	–2.0	—	–0.4	–2.0	—	–0.4	–2.0	—	–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	—	400	—	—	400	—	—	400	—	—	400	—	ps

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL34ZC	Z16-1	Commercial
SY100EL34ZC	Z16-1	Commercial

JK FLIP-FLOP

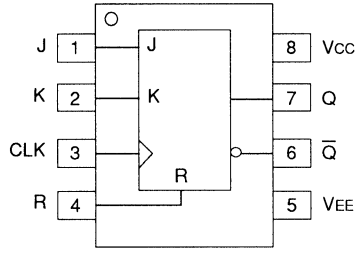
FEATURES

- **525ps propagation delay**
- **2.2GHz toggle frequency**
- **High bandwidth output transistions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL35 are high-speed JK Flip-Flops. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave and, thus, the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

TRUTH TABLE[1]

J	K	R	CLK	Qn+1
L	L	L	Z	Qn
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	$\overline{Qn}$
X	X	H	X	L

NOTE:
1. Z = LOW-to-HIGH transition.

5

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{EE}	Power Supply Current													mA
	10EL	—	27	—	—	27	32	—	27	32	—	27	32	
	100EL	—	27	—	—	27	32	—	27	32	—	32	37	
V_{EE}	Power Supply Voltage													V
	10EL	—	–5.2	—	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	—	–4.5	—	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	—	2.0	—	1.8	2.2	—	1.8	2.2	—	1.8	2.2	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D	— —	515 450	— —	340 275	515 450	690 625	350 275	525 450	700 625	395 350	570 525	745 700	ps
t_S	Set-up Time	—	0	—	150	0	—	150	0	—	150	0	—	ps
t_H	Hold Time	—	100	—	250	100	—	250	100	—	250	100	—	ps
t_{RR}	Reset Recovery	400	200	—	400	200	—	400	200	—	400	200	—	ps
t_{PW}	Minimum Pulse Width CLK, Reset	400	—	—	400	—	—	400	—	—	400	—	—	ps
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL35ZC	Z8-1	Commercial
SY100EL35ZC	Z8-1	Commercial

DIFFERENTIAL CLOCK D FLIP-FLOP

FEATURES

- **475ps propagation delay**
- **2.8GHz toggle frequency**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

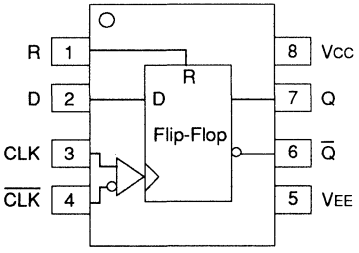
DESCRIPTION

The SY10EL/100EL51 are differential clock D flip-flops with reset. These devices are functionally similar to the E151 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E151, the EL51 is ideally suited for those applications which require the ultimate in AC performance.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input (pulled down to VEE) conditions.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

TRUTH TABLE[1]

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

NOTE:
1. Z = LOW-to-HIGH transition.

PIN NAMES

Pin	Function
R	Reset Input
D	Data Input
CLK	Clock Input
Q	Data Output

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
IEE	Power Supply Current													mA
	10EL	—	24	—	19	24	29	19	24	29	19	24	29	
	100EL	—	24	—	19	24	29	19	24	29	24	30	36	
VEE	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	—	2.8	—	2.2	2.8	—	2.2	2.8	—	2.2	2.8	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	— —	465 455	— —	375 355	465 455	555 555	385 355	475 465	565 565	440 410	530 510	620 620	ps
t_S	Set-up Time	—	0	—	150	0	—	150	0	—	150	0	—	ps
t_H	Hold Time	—	100	—	250	100	—	250	100	—	250	100	—	ps
t_{RR}	Reset Recovery	400	200	—	400	200	—	400	200	—	400	200	—	ps
t_{PW}	Minimum Pulse Width CLK, Reset	400	—	—	400	—	—	400	—	—	400	—	—	ps
V_{PP}	Minimum Input Swing(1)	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range(2)	–0.4	—	(2)	–0.4	—	(2)	–0.4	—	(2)	–0.4	—	(2)	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Minimum input swing for which AC parameters are guaranteed.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

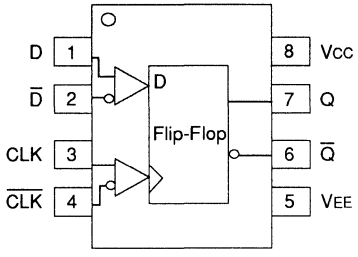
Ordering Code	Package Type	Operating Range
SY10EL51ZC	Z8-1	Commercial
SY100EL51ZC	Z8-1	Commercial

DIFFERENTIAL DATA & CLOCK D FLIP-FLOP

FEATURES

- **365ps propagation delay**
- **2.0GHz toggle frequency**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
D	Data Input
CLK	Clock Input
Q	Data Output

DESCRIPTION

The SY10EL/100EL52 are differential data, differential clock D flip-flops with reset. These devices are functionally equivalent to the E452 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452, the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs also allow the EL52 to be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that, under open input conditions (pulled down to VEE), the outputs of the device will remain stable.

TRUTH TABLE[1]

D	CLK	Q
L	Z	L
H	Z	H

NOTE:
1. Z = LOW-to-HIGH transition.

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DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	-40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current													mA
	10EL	—	21	—	17	21	25	17	21	25	17	21	25	
	100EL	—	21	—	17	21	25	17	21	25	19	24	29	
VEE	Power Supply Voltage													V
	10EL	-4.94	-5.2	-5.5	-4.94	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	
	100EL	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	—	2.5	—	2.2	2.8	—	2.2	2.8	—	2.2	2.8	—	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK	—	335	—	275	365	465	275	365	465	320	410	510	ps
t_S	Set-up Time	—	0	—	125	0	—	125	0	—	125	0	—	ps
t_H	Hold Time	—	50	—	150	50	—	150	50	—	150	50	—	ps
t_{PW}	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	400	—	—	ps
V_{PP}	Minimum Input Swing(1)	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range(2)													V
	D (10EL)	–0.4	—	–1.6	–0.4	—	–1.6	–0.4	—	–1.6	–0.4	—	–1.6	
	D (100EL)	–0.4	—	–1.2	–0.4	—	–1.2	–0.4	—	–1.2	–0.4	—	–1.2	
	CLK (10EL)	–0.6	—	(3)	–0.6	—	(3)	–0.6	—	(3)	–0.6	—	(3)	
	CLK (100EL)	–0.8	—	(3)	–0.8	—	(3)	–0.8	—	(3)	–0.8	—	(3)	
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	225	—	100	225	350	100	225	350	100	225	350	ps

NOTES:

1. Minimum input swing for which AC parameters are guaranteed.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.
3. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL52ZC	Z8-1	Commercial
SY100EL52ZC	Z8-1	Commercial

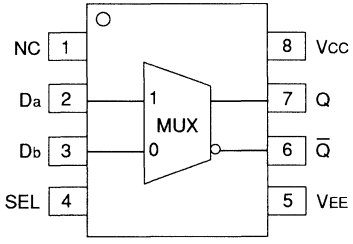
FEATURES

- **230ps propagation delay**
- **High bandwidth output transitions**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

DESCRIPTION

The SY10EL/100EL58 are 2:1 multiplexers. These devices are functionally equivalent to the E158 devices, with higher performance capabilities. With propagation delays and output transition times significantly faster than the E158, the EL58 is ideally suited for those applications which require the ultimate in AC performance.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

TRUTH TABLE

SEL	Data
H	a
L	b

PIN NAMES

Pin	Function
Da, Db	Data Inputs
Q	Data Outputs
SEL	Select Input

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current													mA
	10EL	—	14	—	11	14	17	11	14	17	11	14	17	
	100EL	—	14	—	11	14	17	11	14	17	13	16	19	
V_{EE}	Power Supply Voltage													V
	10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation Delay to	—	220	—	110	220	330	120	230	340	140	250	360	ps
t_{PHL}	Output D	—	250	—	140	250	360	150	260	370	170	280	390	
t_r	Output Rise/Fall Times Q	—	225	—	100	225	350	100	225	350	100	225	350	ps
t_f	(20% to 80%)													

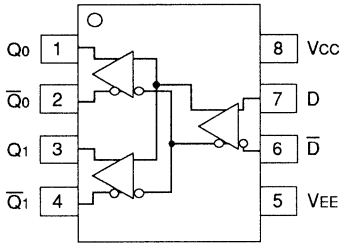
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL58ZC	Z8-1	Commercial
SY100EL58ZC	Z8-1	Commercial

FEATURES

- **375ps propagation delay**
- **1.6V output swings**
- **Internal 75KΩ input pull-down resistors**
- **ESD protection of 2000V**

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

DESCRIPTION

The SY10EL89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in Digital Video Broadcast applications. For this application, since the system is polarity-free, each output of the device can be used as an independent driver. The driver boasts a voltage gain of approximately 40 and produces output swings twice as large as a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6V output swings allow for termination at both ends of the cable while maintaining the required 800mV swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard –2.0V. All of the DC parameters are tested with a 50Ω to –3.0V load. The driver accepts a standard differential ECL input and can run off the Digital Video Broadcast standard –5.0V supply.

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PIN NAMES

Pin	Function
D	Data Inputs
Q_0, Q_1	Data Outputs

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

		–40°C			0°C			+25°C			+85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{EE}	Power Supply Current	18	23	28	18	23	28	18	23	28	18	23	28	mA
V_{OH}	Output HIGH Voltage(1)	–1.23	–1.10	–0.98	–1.17	–1.05	–0.93	–1.13	–1.02	–0.90	–1.06	–0.96	–0.81	V
V_{OL}	Output LOW Voltage(1)	–2.84	–2.72	–2.58	–2.84	–2.70	–2.56	–2.84	–2.70	–2.56	–2.84	–2.67	–2.51	V
V_{EE}	Power Supply Voltage	–4.75	—	–5.5	–4.75	—	–5.5	–4.75	—	–5.5	–4.75	—	–5.5	V
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA

NOTE:

1. V_{OH} and V_{OL} specified for 50Ω to –3.0V load.

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AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	–40°C			0°C			+25°C			+85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D	—	340	—	250	340	430	260	350	440	310	400	490	ps
t_{SKEW}	Within-Device Skew	—	5	20	—	5	20	—	5	20	—	5	20	ps
V_{PP}	Minimum Input Swing(1)	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range(2)	–0.4	—	(2)	–0.4	—	(2)	–0.4	—	(2)	–0.4	—	(2)	V
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	—	330	—	205	330	455	205	330	455	205	330	455	ps

NOTES:

1. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

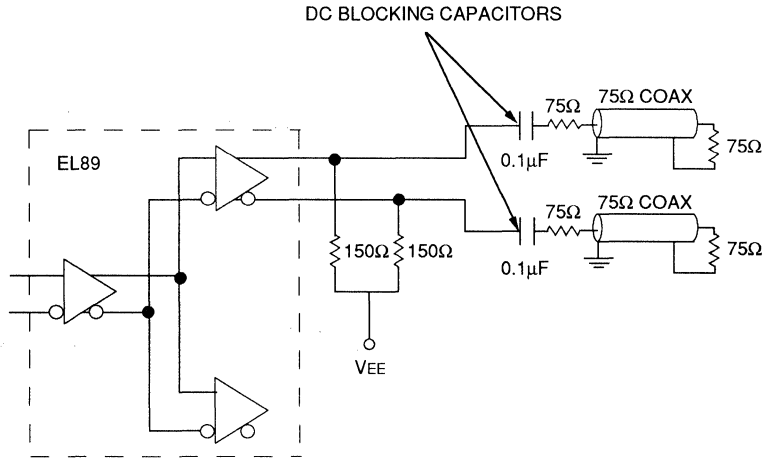


Figure 1. Termination Configuration

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10EL89ZC	Z8-1	Commercial
SY100EL89ZC	Z8-1	Commercial

SYNERGY SEMICONDUCTOR

DUAL TTL-TO-DIFFERENTIAL PECL TRANSLATOR

PRELIMINARY
SY10ELT22
SY100ELT22

FEATURES

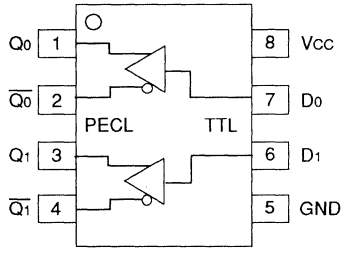
- 300ps typical propagation delay
- <100ps typical output-to-output skew
- ESD protection of 2000V
- Differential PECL outputs
- PNP TTL inputs for minimal loading
- Flow-through pinouts
- Small outline SOIC package

DESCRIPTION

The SY10ELT/100ELT22 are dual TTL-to-differential PECL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT22 makes it ideal for applications which require the tranlation of a clock and a data signal.

The ELT22 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
Q_n	Differential PECL Outputs
D_n	TTL Inputs
V_{CC}	+5.0V Supply
GND	Ground

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ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
TTL Input Voltage[2]	V_I	–0.5 to 6.0	V
TTL Input Current[2]	I_I	–30 to +5.0	mA
ECL Output Current — Continuous — Surge	I_{OUT}	 50 100	mA
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect input.

TRUTH TABLE

D	Q	$\overline{Q}$
H	H	L
L	L	H
Open	H	L

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{CC}	Power Supply Current	—	25	—	25	—	25	mA	—

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output D	100	600	100	600	100	600	ps	50Ω to (V_{CC} – 2.0V)
t_r t_f	Output Rise/Fall Time 20% to 80%	200	500	200	500	200	500	ps	50Ω to (V_{CC} – 2.0V)
t_{skpp}	Part-toPart Skew[1]	—	500	—	500	—	500	ps	50Ω to (V_{CC} – 2.0V)
t_{skwd}	Within-Device Skew[1],[2]	—	200	—	200	—	200	ps	50Ω to (V_{CC} – 2.0V)

NOTE:

1. Guaranteed, but not tested.
2. Same transition @ common Vcc Level.

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	20 100	— —	20 100	— —	20 100	µA	V_{IN} = 2.7V V_{IN} = V_{CC}
I_{IL}	Input LOW Current	—	–0.2	—	–0.2	—	–0.2	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	–1.2	—	–1.2	—	–1.2	V	I_{IN} = –18mA

10EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	3980	4160	4020	4190	4090	4280	mV	—
V_{OL}	Output LOW Voltage	3050	3370	3050	3370	3050	3405	mV	—

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100EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	3975	4120	3975	4120	3975	4120	mV	—
V_{OL}	Output LOW Voltage	3190	3380	3190	3380	3190	3380	mV	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10ELT22ZC	Z8-1	Commercial
SY100ELT22ZC	Z8-1	Commercial

SYNERGY SEMICONDUCTOR

DUAL DIFFERENTIAL PECL-TO-TTL TRANSLATOR

PRELIMINARY
SY10ELT23
SY100ELT23

FEATURES

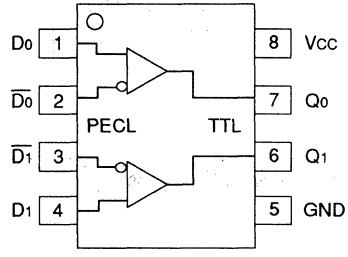
- **2.5ns typical propagation delay**
- **<300ps typical output-to-output skew**
- **ESD protection of 2000V**
- **Differential PECL inputs**
- **24mA TTL outputs**
- **Flow-through pinouts**
- **Small outline SOIC package**

DESCRIPTION

The SY10ELT/100ELT23 are dual differential PECL-to-TTL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
Q_n	TTL Outputs
D_n	Differential PECL Inputs
VCC	+5.0V Supply
GND	Ground

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Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
ECL Input Voltage	V_I	0 to V_{CC} + 0.5	V
Voltage Applied to Output at HIGH State	V_O	–0.5 to 5.5	V
Current Applied to Output at LOW State	I_O	Twice the Rated I_{OL}	mA
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	$\overline{D}$	Q
L	H	L
H	L	H
Open	Open	L

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{CC}	Power Supply Current	—	25	—	25	—	25	mA	—

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D to Output Q	2.0	3.0	2.0	3.0	2.0	3.0	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew[1]	—	1.0	—	1.0	—	1.0	ns	C_L = 50pF
t_{skwd}	Within-Device Skew[1],[2]	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	0.5	1.0	0.5	1.0	0.5	1.0	ns	C_L = 50pF

NOTE:

1. Guaranteed, but not tested.
2. Same transition @ common Vcc Level.

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = −3.0mA I_{OH} = −15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{OUT} = 0V

10EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—		
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	—
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.555		

100EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—		
V_{IH}	Input HIGH Voltage	3.835	4.12	3.835	4.12	3.835	4.12	V	—
V_{IL}	Input LOW Voltage	3.19	3.525	3.19	3.525	3.19	3.525		

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10ELT23ZC	Z8-1	Commercial
SY100ELT23ZC	Z8-1	Commercial

LOGIC ORDERING INFORMATION

SYxxx x xxx x C x

- SPECIAL PROCESSING
- TEMPERATURE RANGE
  - C = Commercial
- PACKAGE IDENTIFIER
  - D = CERDIP
  - F = CERPACK
  - J = PLCC (Plastic Leaded Chip Carrier)
  - Z = Plastic SOIC (Small Outline IC)
  - X = Other
- FUNCTION CODE
- FAMILY CODE
  - S = Super-300K
  - E = ECLinPS
  - H = Clock Drivers/Translators
  - EL = ECLinPS Lite
  - ELT = ECLinPS Lite Translators
- DEVICE TYPE PREFIX
  - 10 = 10K DC Levels with –5.2V ± 5% Supply
  - 100 = 100K DC Levels with Extended –4.2V to –5.46V Supply

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ECLinPS LITE MARKING INFORMATION

X = 100
H = 10

EL ____ Part Number

SY Lot Number

Last Digit of Year

WW

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SUPER – 300K™ LOGIC

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DC characteristics for the 100K parametric limits listed below are guaranteed for the entire *SUPER-300K* family **unless specified on the individual data sheet.**

The specified DC limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

GUARANTEED OPERATING CONDITIONS[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{EE}	Supply Voltage	–4.8	–4.5	–4.2	V
T_A	Operating Temperature	0	25	85	°C

NOTE:

1. Referenced to V_{CC}.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{EE}	V_{EE} Pin Potential to Ground Pin	+0.5 to –7.0	V
V_{IN}	Input Voltage	+0.5 to V_{EE}	V
I_{OUT}	DC Output Current (Output HIGH)	–50	mA
T_C	Temperature Under Bias	–55 to +125	°C
T_j	Junction Temperature	+150	°C
T_{store}	Storage Temperature	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V, Output Load = 50Ω to –2.0V, V_{EE} = –4.5V, T_A = 0°C to 85°C

Symbol	Parameter	V_{EE}	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–4.2V	–1020	—	–870	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
		–4.5V	–1025	–955	–880		
		–5.46V	–1035	—	–880		
V_{OL}	Output LOW Voltage	–4.2V	–1810	—	–1605	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
		–4.5V	–1810	–1705	–1620		
		–5.46V	–1830	—	–1620		
V_{OHC}	Output HIGH Voltage	–4.2V	–1030	—	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
		–4.5V	–1035	—	—		
		–5.46V	–1045	—	—		
V_{OLC}	Output LOW Voltage	–4.2V	—	—	–1595	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
		–4.5V	—	—	–1610		
		–5.46V	—	—	–1610		
V_{IH}	Input HIGH Voltage	–4.2V	–1150	—	–870	mV	Guaranteed Input Voltage HIGH for All Inputs
		–4.5V	–1165	—	–880		
		–5.46V	–1165	—	–880		
V_{IL}	Input LOW Voltage	–4.2V	–1810	—	–1475	mV	Guaranteed Input Voltage LOW for All Inputs
		–4.5V	–1810	—	–1475		
		–5.46V	–1830	—	–1490		
I_{IL}	Input LOW Current	–4.5V	+0.5	—	—	µA	V_{IN} = V_{IL} Min.

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TRIPLE 5-INPUT OR/NOR GATE

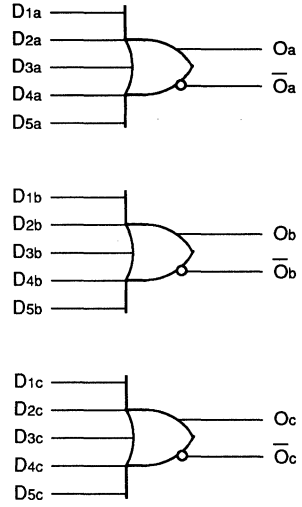
FEATURES

- **Max. propagation delay of 750ps**
- **IEE min. of –25mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **20% faster than National 300K at lower power**
- **Internal 75KΩ input pull-down resistors**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

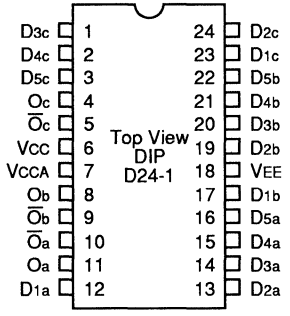
DESCRIPTION

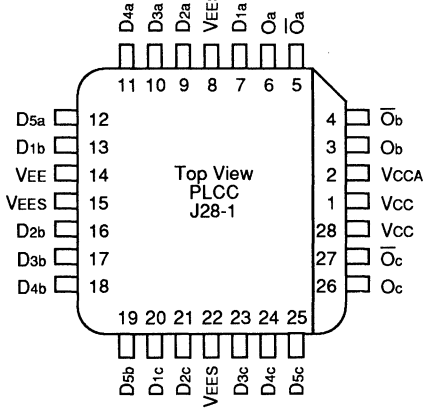
The SY100S301 is an ultra-fast triple 5-input OR/NOR gate designed for use in high-performance ECL systems. The inputs on this device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



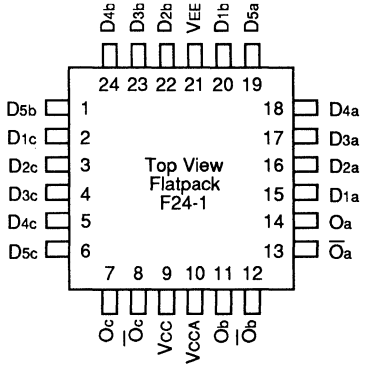
PIN CONFIGURATIONS





PIN NAMES

Pin	Function
Dna, Dnb, Dnc	Data Inputs (n-1...5)
Oa, Ob, Oc	Data Outputs
Oa, Ob, Oc	Complementary Data Outputs



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LOGIC EQUATION

$O_a = D_{1a} + D_{2a} + D_{3a} + D_{4a} + D_{5a}$

$O_b = D_{1b} + D_{2b} + D_{3b} + D_{4a} + D_{5b}$

$O_c = D_{1c} + D_{2c} + D_{3C} + D_{4c} + D_{5c}$

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	200	µA	—
I_{EE}	Power Supply Current	–25	–17	–11	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

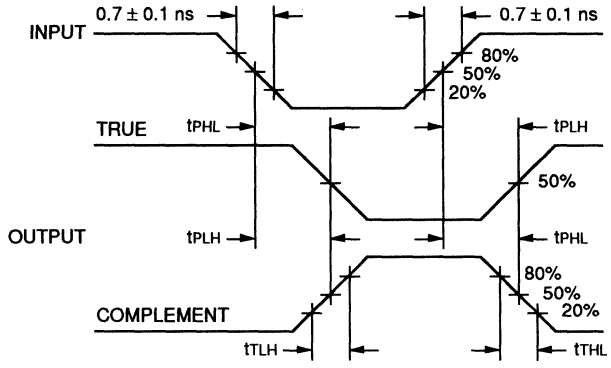
		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	750	300	750	300	750	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S301DC	D24-1	Commercial
SY100S301FC	F24-1	Commercial
SY100S301JC	J28-1	Commercial

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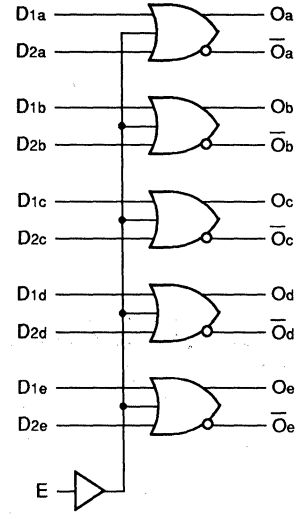
FEATURES

- **Max. propagation delay of 700ps**
- **IEE min. of –45mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  - **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **50% faster than National 300K**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

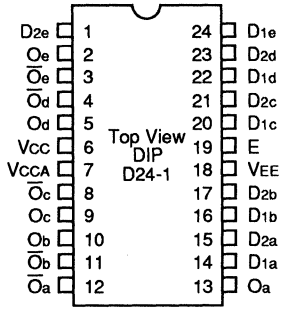
DESCRIPTION

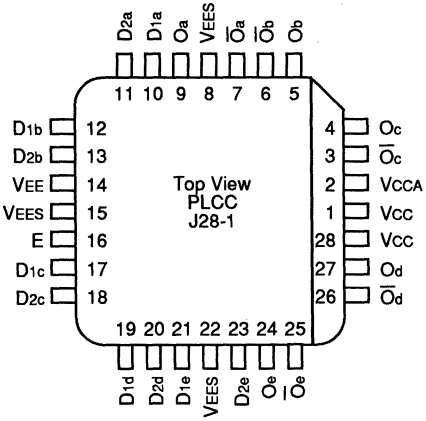
The SY100S302 offers five 2-input OR/NOR gates designed for use in high-performance ECL systems. The five gates are controlled by a common Enable signal. All inputs have 75KΩ pull-down resistors and all outputs are buffered.

BLOCK DIAGRAM



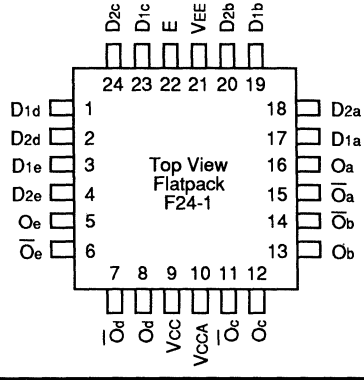
PIN CONFIGURATIONS





PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n-1...5)
E	Enable Input
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs



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TRUTH TABLE[1]

D1X	D2X	E	OX	$\overline{OX}$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

NOTE:
1. H = High Voltage Level
   L = Low Voltage Level

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–45	–28	–21	mA	Inputs Open

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AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	1100	300	1100	300	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	750	300	750	300	750	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	250	950	250	950	250	950	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

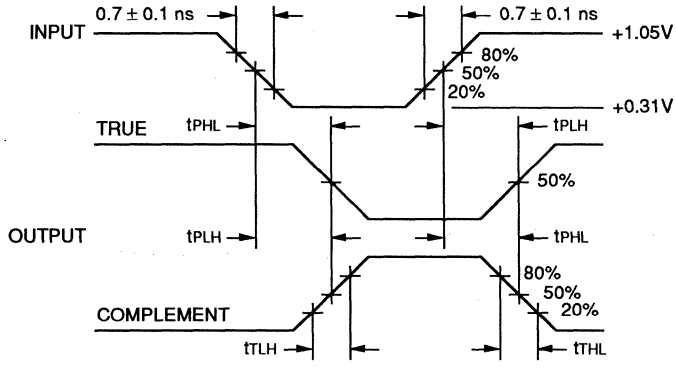
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	250	700	250	700	250	700	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	250	900	250	900	250	900	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S302DC	D24-1	Commercial
SY100S302FC	F24-1	Commercial
SY100S302JC	J28-1	Commercial

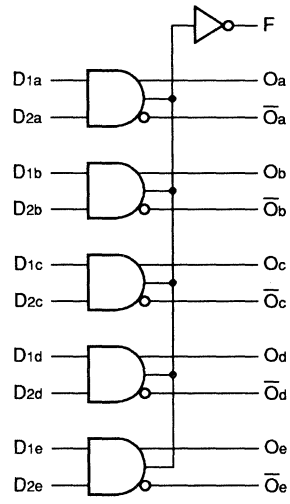
FEATURES

- **Max. propagation delay of 1050ps**
- **IEE min. of –60mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **40% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

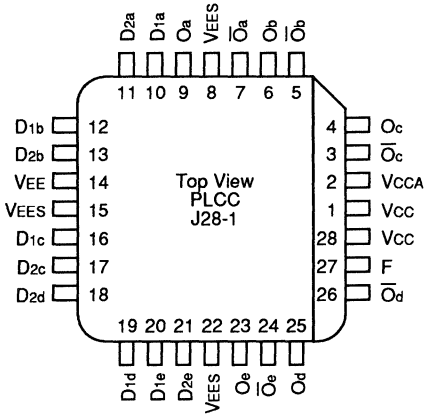
DESCRIPTION

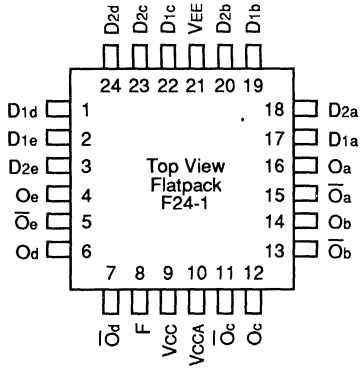
The SY100S304 is an ultra-fast quint AND/NAND gate designed for use in high-performance ECL systems. This device also features a Function (F) output which is the wire-NOR of the AND gate outputs. The inputs on the device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



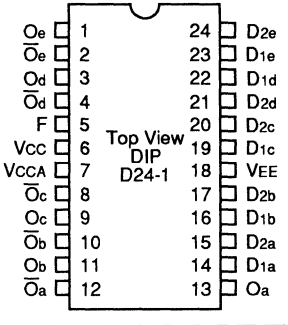
PIN CONFIGURATIONS





PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n = 1...5)
F	Function Output
Oa – Oe	Data Outputs
Ōa – Ōe	Complementary Data Outputs



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DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current D_{2a} — D_{2e} D_{1a} — D_{1e}	 — —	 — —	 250 250	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–60	–40	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_{na} — D_{ne} to O, $\overline{O}$	300	1250	300	1250	300	1250	ps
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1750	600	1750	600	1750	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

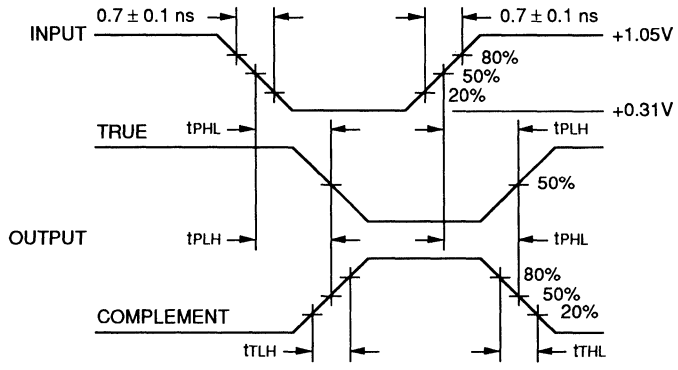
		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_{na} — D_{ne} to O, $\overline{O}$	300	1150	300	1150	300	1150	ps
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1650	600	1650	600	1650	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_{na} — D_{ne} to O, $\overline{O}$	300	1050	300	1050	300	1050	ps
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1550	600	1550	600	1550	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S304DC	D24-1	Commercial
SY100S304FC	F24-1	Commercial
SY100S304JC	J28-1	Commercial

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QUINT EXCLUSIVE OR/NOR GATE

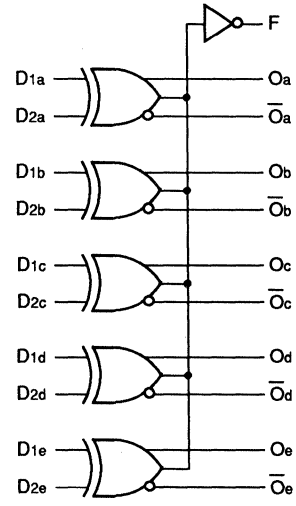
FEATURES

- **Max. propagation delay of 1000ps**
- **IEE min. of –58mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  - **VEE = –4.2V to 5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **50% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

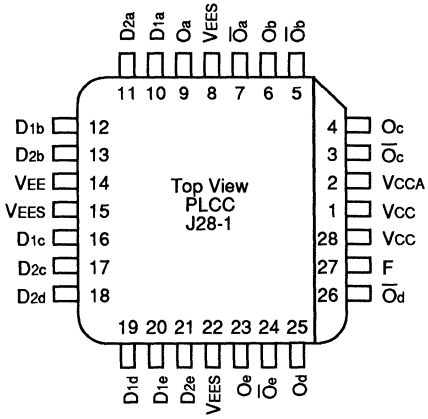
DESCRIPTION

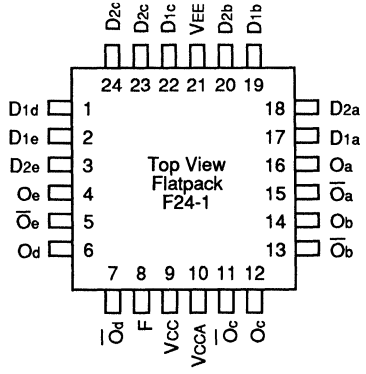
The SY100S307 is an ultra-fast quint exclusive-OR/NOR gate designed for use in high-performance ECL systems. A function output that is the wire-OR result of the exclusive-OR outputs is also available. The inputs on the device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



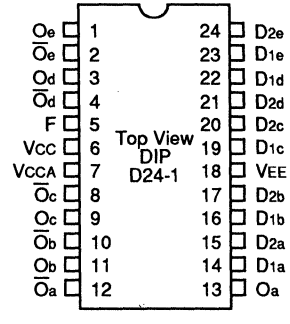
PIN CONFIGURATIONS





PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n = 1...5)
F	Function Output
Oa – Oe	Data Outputs
Oa – Oe	Complementary Data Outputs



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LOGIC EQUATION

$F = (D1a \oplus D2a) + (D1b \oplus D2b) + (D1c \oplus D2c) + (D1d \oplus D2d) + (D1e \oplus D2e)$.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current D2a — D2e D1a — D1e	 — —	 — —	 200 250	µA	$V_{IN} = V_{IH}$ (Max.)
I_{EE}	Power Supply Current	–58	–40	–27	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PH2}	Propagation Delay D2a — D2e to O, $\overline{O}$	200	1200	200	1150	300	1200	ps
t_{PLH} t_{PHL}	Propagation Delay D1a — D1e to O, $\overline{O}$	200	1100	200	1050	200	1100	ps
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1625	300	1625	300	1625	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PH2}	Propagation Delay D2a — D2e to O, $\overline{O}$	200	1100	200	1050	200	1100	ps
t_{PLH} t_{PHL}	Propagation Delay D1a — D1e to O, $\overline{O}$	200	1000	200	950	200	1000	ps
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1525	300	1525	300	1525	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

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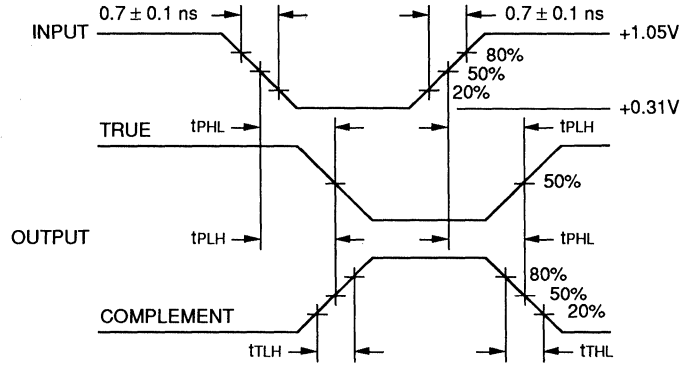
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_{2a} — D_{2e} to O, $\overline{O}$	300	1000	300	1000	300	1000	ps
t_{PLH} t_{PHL}	Propagation Delay D_{1a} — D_{1e} to O, $\overline{O}$	300	900	300	900	300	900	ps
t_{PLH} t_{PHL}	Propagation Delay Data to F	300	1425	300	1425	300	1425	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

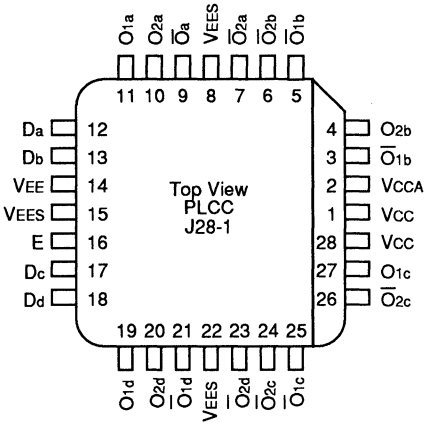
PRODUCT ORDERING CODE

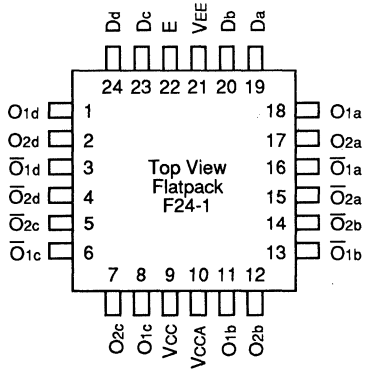
Ordering Code	Package Type	Operating Range
SY100S307DC	D24-1	Commercial
SY100S307FC	F24-1	Commercial
SY100S307JC	J28-1	Commercial

FEATURES

- **Max. propagation delay of 800ps**
- **Enable to Output max. of 950ps**
- **IEE min. of –60mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **50% faster than National 300K**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

PIN CONFIGURATIONS

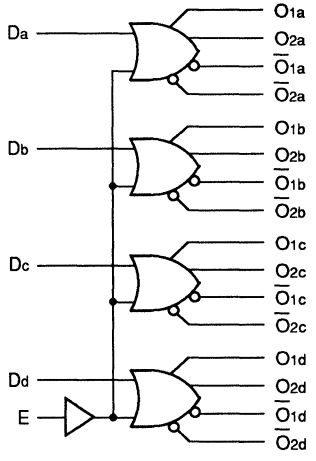




DESCRIPTION

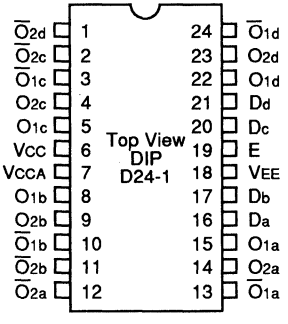
The SY100S313 offers four drivers with two OR and two NOR outputs, designed for use in high-performance ECL systems. The four drivers are controlled by a common Enable signal which is buffered to minimize input loading. If the D inputs are not used, the Enable signal can be used to drive sixteen 50Ω lines. All inputs have 75KΩ pulldown resistors and all outputs are buffered.

BLOCK DIAGRAM



PIN NAMES

Pin	Function
Da – Dd	Data Inputs
E	Enable Input
Ona – Ond	Data Outputs
$\overline{O}$na – $\overline{O}$nd	Complementary Data Outputs



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LOGIC EQUATION

$O = D + E$

$\overline{O} = \overline{D + E}$

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–60	–43	–20	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	200	900	200	900	200	900	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	1100	300	1100	300	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

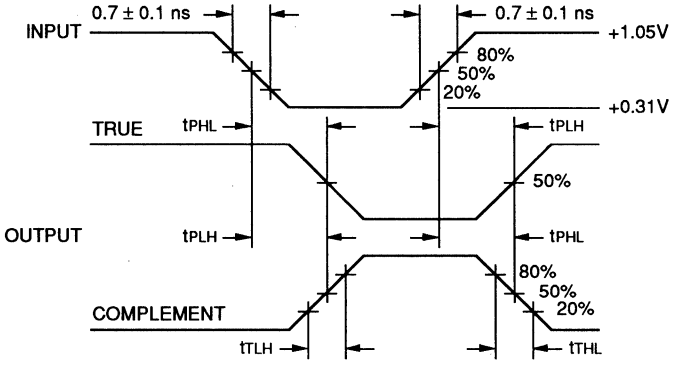
		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	200	850	800	850	200	850	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	1000	300	1000	300	1000	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	200	800	200	800	200	800	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	950	300	950	300	950	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S313DC	D24-1	Commercial
SY100S313FC	F24-1	Commercial
SY100S313JC	J28-1	Commercial

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FEATURES

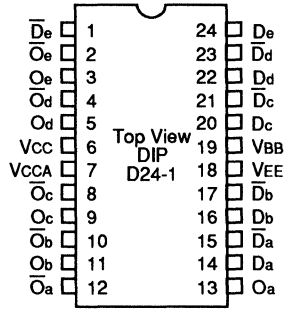
- **Max. propagation delay of 900ps**
- **Differential outputs**
- **IEE min. of –60mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **VBB output for single-ended use**
- **More than twice as fast as National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

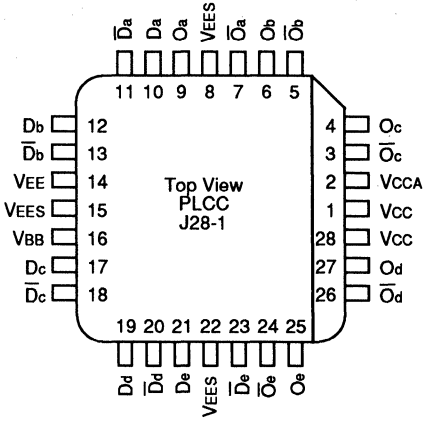
DESCRIPTION

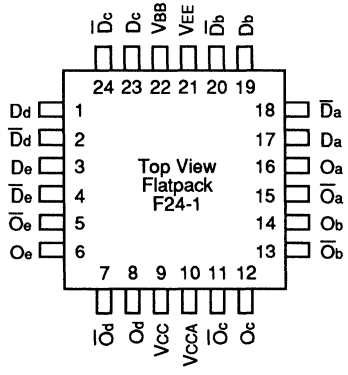
The SY100S314 offers five differential line receivers with emitter follower outputs, designed for use in high-performance ECL systems. For single-ended operation, the VBB reference voltage is available. In the single-ended mode, the apparent input threshold of the true inputs is 30mV higher than the threshold of the complementary inputs.

Common mode rejection of +1.0V is achieved through the use of active current sources. If both the true and complement inputs are at the same potential between VEE and VCC, then the complementary outputs will take on a logic HIGH state. Unlike the other members of the Synergy 300K family, the inputs on this device do not have pull-down resistors.

PIN CONFIGURATIONS







PIN NAMES

Pin	Function
Da – De	Data Inputs
$\overline{Da}$ – $\overline{De}$	Inverting Data Inputs
Oa – Oe	Data Outputs
$\overline{Oa}$ – $\overline{Oe}$	Complementary Data Outputs

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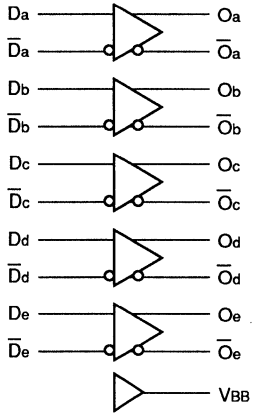
BLOCK DIAGRAM



LOGIC EQUATION

O = D

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible ±V_{CM} with Respect to V_{BB}
I_{IH}	Input HIGH Current	—	—	50	µA	V_{IN} = V_{IH} (Max.), Da - De = V_{BB}, $\overline{Da}$ - $\overline{De}$ = V_{IL} (Min.)
I_{CBO}	Input Leakage Current	–10	—	—	µA	V_{IN} = V_{EE}, Da - De = V_{BB}, $\overline{Da}$ - $\overline{De}$ = V_{IL} (Min.)
I_{EE}	Power Supply Current	–60	–45	–30	mA	Da - De = V_{BB}, $\overline{Da}$ - $\overline{De}$ = V_{IL} (Min.)

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1100	300	1100	300	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

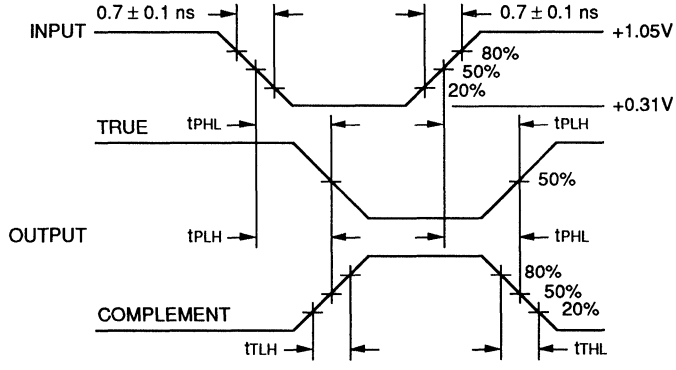
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

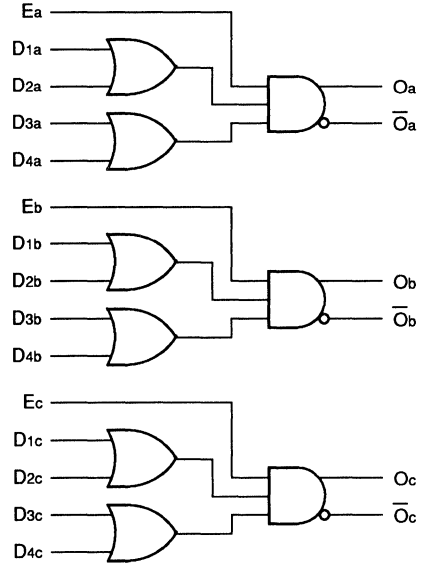
Ordering Code	Package Type	Operating Range
SY100S314DC	D24-1	Commercial
SY100S314FC	F24-1	Commercial
SY100S314JC	J28-1	Commercial

TRIPLE 2-WIDE OA/OAI GATE

FEATURES

- **Max. propagation delay of 900ps**
- **IEE min. of –48mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **Approximately 40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

BLOCK DIAGRAM



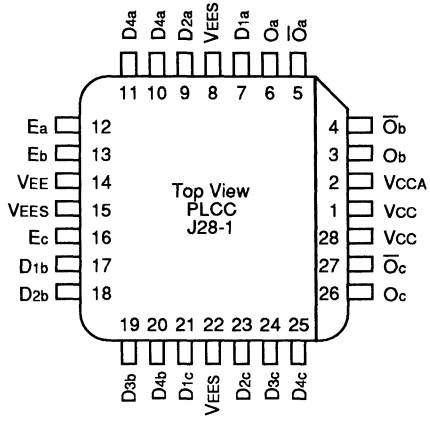
PIN NAMES

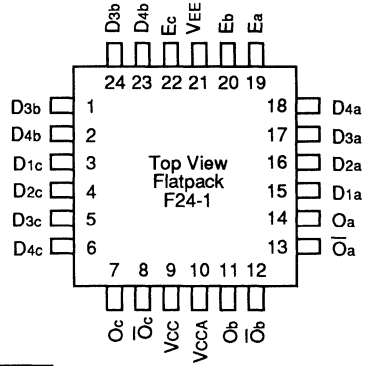
Pin	Function
$D_{na} - D_{nc}$	Data Inputs (n = 1...4)
$E_a - E_c$	Enable Inputs
$O_a - O_c$	Data Outputs
$\overline{O}_a - \overline{O}_c$	Complementary Data Outputs

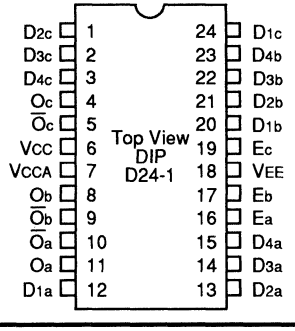
DESCRIPTION

The SY100S317 is a set of ultra-fast, triple 2-wide OR/AND gates designed for use in high-performance ECL systems. This device offers both true and complement outputs. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS







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DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–48	–32	–22	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1100	300	100	300	1100	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	900	300	900	300	900	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

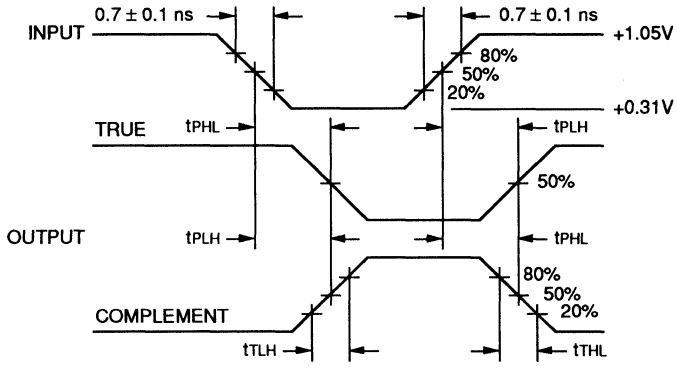
		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	800	300	800	300	800	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	700	300	700	300	700	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S317DC	D24-1	Commercial
SY100S317FC	F24-1	Commercial
SY100S317JC	J28-1	Commercial

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5-WIDE 5, 4, 4, 4, 2 OA/OAI GATE

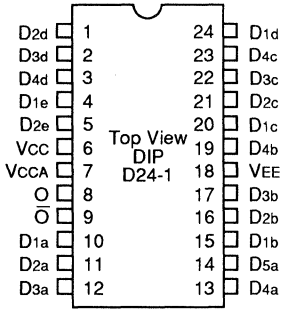
FEATURES

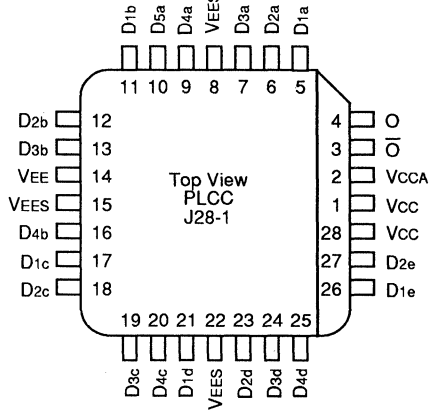
- **Max. propagation delay of 800ps**
- **IEE min. of –55mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **70% faster than National or Signetics**
- **40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

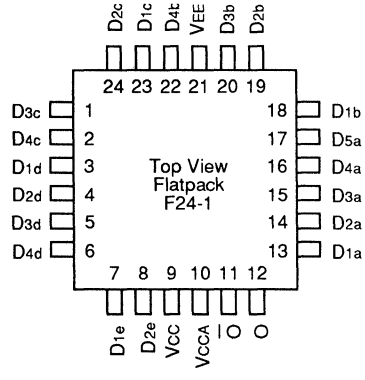
DESCRIPTION

The SY100S318 is an ultra-fast 5-wide 5, 4, 4, 4, 2 OR/AND gate with both true and complementary outputs, designed for use in high-performance ECL systems. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





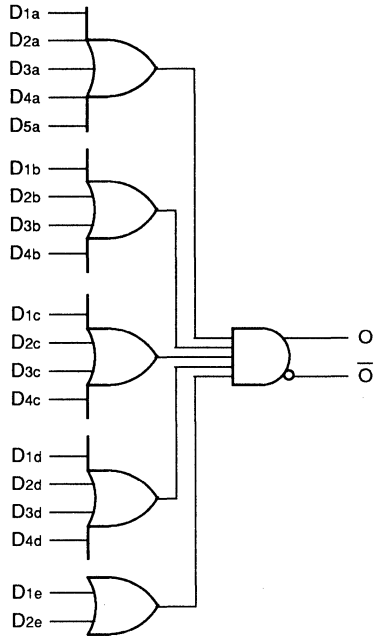


PIN NAMES

Pin	Function
Dna – Dne	Data Inputs (n = 1...5)
O – O̅	Data Outputs

Rev.: B Amendment: /0
Issue Date: April, 1994

BLOCK DIAGRAM



LOGIC EQUATION

O = (D1a + D2a + D3a + D4a + D5a)
(D1b + D2b + D3b + D4b)
(D1c + D2c + D3c + D4c)
(D1d + D2d + D3d + D4d)
(D1e + D2e)

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DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–55	–41	–25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	1000	300	1000	300	1000	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

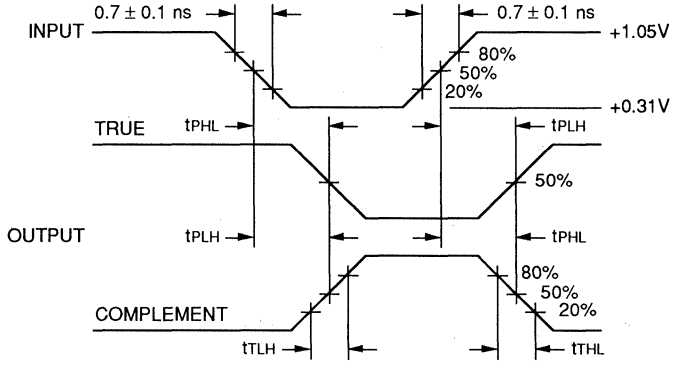
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S318DC	D24-1	Commercial
SY100S318FC	F24-1	Commercial
SY100S318JC	J28-1	Commercial

LOW-POWER 9-BIT INVERTER

SY100S321

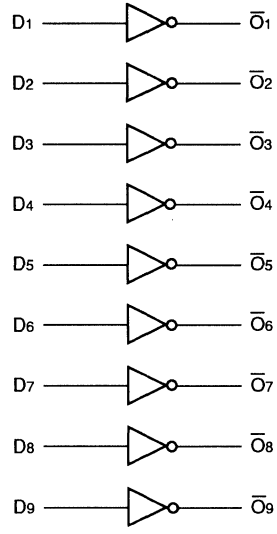
FEATURES

- **Max. propagation delay of 700ps**
- **IEE min. of –55mA**
- **ESD protection of 2000 volts**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **70% faster than National 300K at lower power**
- **Internal 75KΩ input pull-down resistors**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

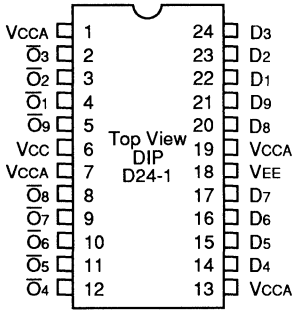
DESCRIPTION

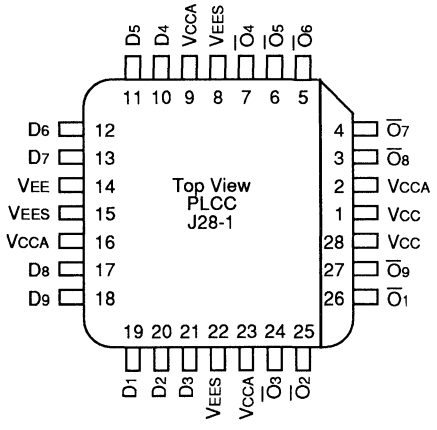
The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

BLOCK DIAGRAM



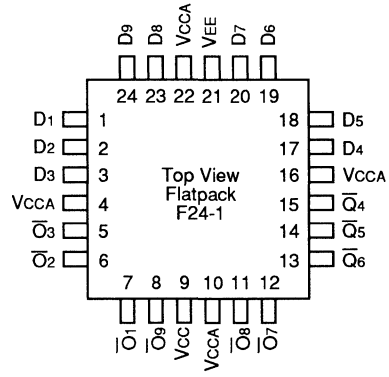
PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D1 – D9	Data Inputs
$\overline{Q}_1$ – $\overline{Q}_9$	Data Outputs



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Rev.: B Amendment: /0
Issue Date: February, 1994

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–55	–41	–25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps	Figures 1 and 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	Figures 1 and 2
t_S, G–G	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	—

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps	Figures 1 and 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	Figures 1 and 2
t_S, G–G	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	—

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	700	300	700	300	700	ps	Figures 1 and 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	Figures 1 and 2
t_S, G–G	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	—

TEST CIRCUITRY(1)

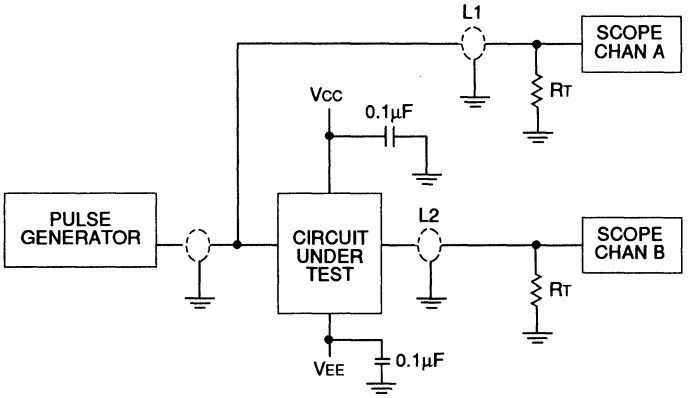

Figure 1. AC Test Circuit

NOTE:

1. V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V.
   L1 and L2 = equal length 50Ω impedance lines.
   R_T = 50Ω terminator internal to scope.
   Decoupling 0.1µF from GND to V_{CC} and V_{EE}.
   All unused outputs are loaded with 50Ω to GND.
   C_L = Fixture and stray capacitance ≤ 3pF.

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SWITCHING WAVEFORMS

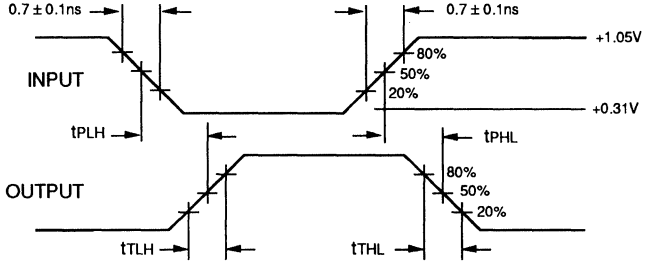


Figure 2. Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S321DC	D24-1	Commercial
SY100S321FC	F24-1	Commercial
SY100S321JC	J28-1	Commercial

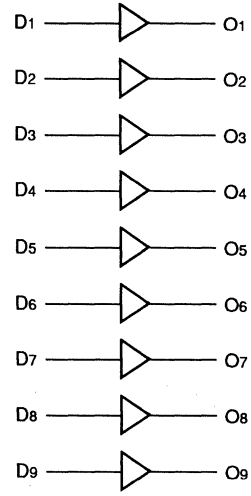
FEATURES

- **Max. propagation delay of 700ps**
- **IEE min. of –55mA**
- **ESD protection of 2000V**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **70% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

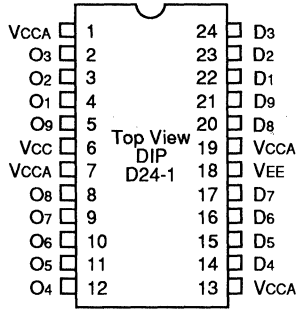
DESCRIPTION

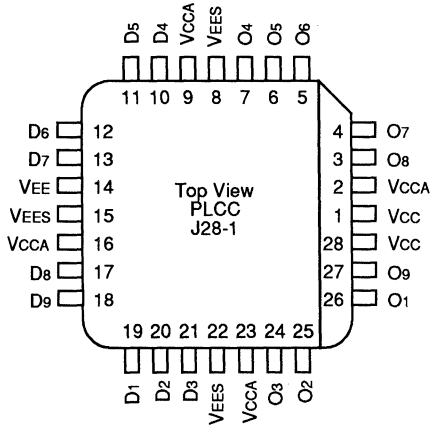
The SY100S322 is an ultra-fast buffer designed for use in high-performance ECL systems. The device provides nine non-inverting buffers with single-ended outputs. The inputs on the device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



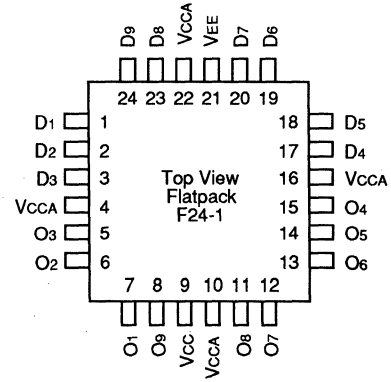
PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D1 – D9	Data Inputs
O1 – O9	Data Outputs



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Issue Date: February, 1994

LOGIC EQUATION

$O_n = D_n$, n = 1 to 9

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–55	–41	–25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	900	300	900	300	900	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	700	300	700	300	700	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

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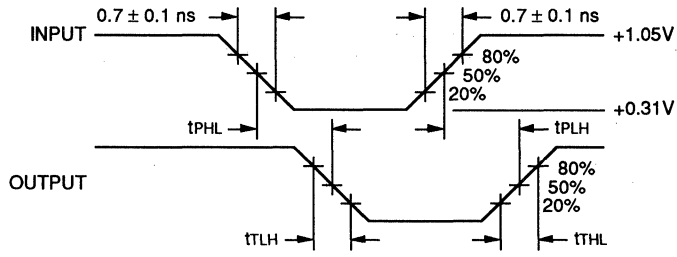
TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S322DC	D24-1	Commercial
SY100S322FC	F24-1	Commercial
SY100S322JC	J28-1	Commercial

LOW POWER HEX TTL-to-ECL TRANSLATOR

SY100S324

FEATURES

- Max. propagation delay of 1.4ns
- IEE min. of –70mA
- ESD protection of 2000V
- Industry standard 100K ECL levels
- Extended supply voltage option:
  — VEE = –4.2V to –5.46V
- Differential outputs
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- Twice as fast as National's 324
- Function and pinout compatible with National and Signetics F100K
- Available in CERDIP, CERPACK and PLCC

DESCRIPTION

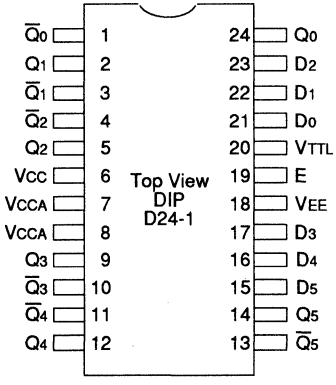
The SY100S324 is a hex translator designed to convert TTL logic levels to 100K ECL levels. The inputs are TTL compatible with differential outputs that can either be used as an inverting/non-inverting translator or as differential line drivers. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all non-inverting outputs LOW.

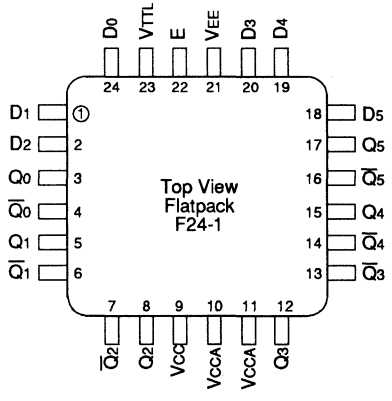
When used in the differential mode, due to its high common mode rejection, it overcomes voltage gradients between the TTL and ECL ground systems. The VEE and VTTL power may be applied in either order.

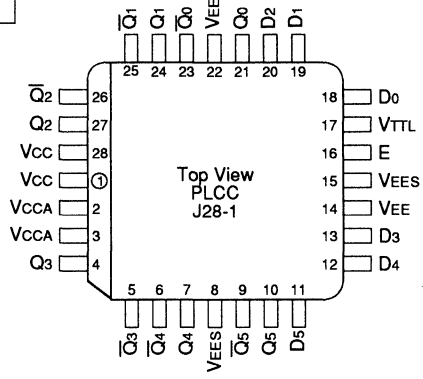
PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
E	Enable Inputs
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

PIN CONFIGURATIONS







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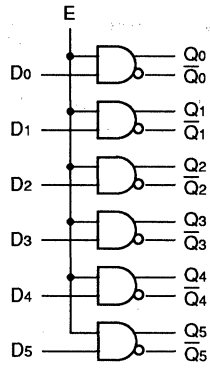
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Sim.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–986	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with 50Ω
V_{OL}	Output LOW Voltage	–1810	–1674	–1620	mV	V_{IN} = V_{IL} (Min.)	
V_{OHC}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage	—	—	–1610	mV	V_{IN} = V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0	—	0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	–1.5	—	—	V	I_{IN} = –10mA	
I_{IH}	Input HIGH Current Data Enable	 — —	 — —	 20 120	µA	 V_{IN} = +2.4V All Other Inputs V_{IN} = GND	
I_{IH}	Input HIGH Current Breakdown Test, All Inputs	—	—	1.0	mA	V_{IN} = +5.5V, V_{TTL} = Max., All Other Inputs V_{IN} = GND	
I_{IL}	Input LOW Current Data Enable	 –1.2 –6.7	 — —	 — —	mA	 V_{IN} = +0.4V All Other Inputs V_{IN} = V_{IH}	
I_{EE}	V_{EE} Power Supply Current	–70	–45	–28	mA	All Inputs V_{IN} = +4.0V	
I_{TTL}	V_{TTL} Power Supply Current	—	25	35	mA	All Inputs V_{IN} = GND	

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	500	950	1500	ps	See Switching Wave Form Figures
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	450	—	1800	ps	

PLCC /FLATPACK

V_{EE} = –4.2V to –5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	400	850	1400	ps	See Switching Wave Form Figures
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	350	—	1700	ps	

SWITCHING WAVEFORM

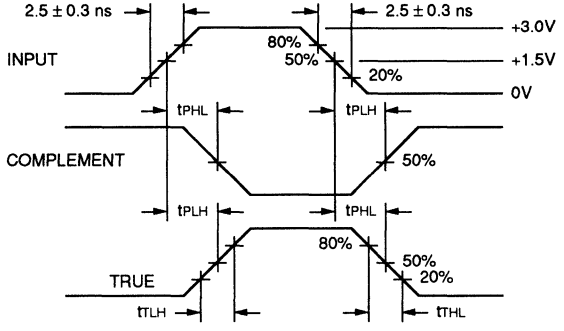


Figure 1. Propagation Delay and Transition Times

TEST CIRCUIT

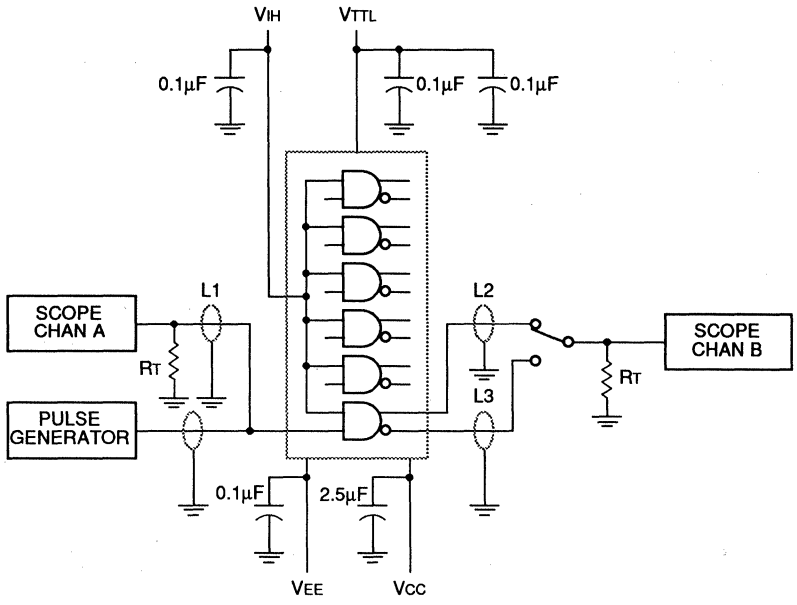


Figure 2. AC Test Circuit

NOTES:

V_{CC}, V_{CCA} = +2V, V_{EE} = –2.5V, V_{TTL} = +7.0V, V_{IH} = +6.0V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S324DC	D24-1	Commercial
SY100S324FC	F24-1	Commercial
SY100S324JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

LOW-POWER HEX ECL-to-TTL TRANSLATOR

SY100S325

FEATURES

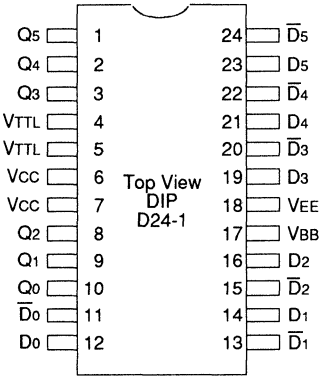
- **Max. propagation delay of 3.7ns**
- **I_{EE} min. of –37mA**
- **ESD protection of 2000V**
- **TTL outputs**
- **Extended supply voltage option:**
  - **V_{EE} = –4.2V to –5.46V**
- **25% faster than National's 325**
- **Differential inputs with built-in offset**
- **Voltage and temperature compensation for improved noise immunity**
- **V_{BB} output for single-ended use**
- **Internal 75KΩ input pull-down resistors**
- **Function and pinout compatible with National and Signetics (F100K)**
- **Available in CERDIP, CERPACK and PLCC**

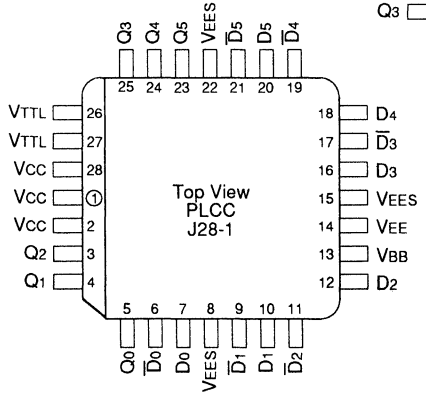
DESCRIPTION

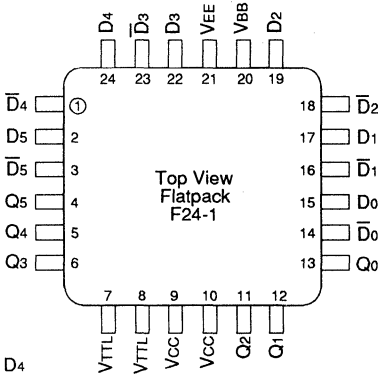
The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 75KΩ pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The V_{TTL} and V_{EE} power may be applied in either order.

PIN CONFIGURATIONS







PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs
Q_0–Q_5	Data Outputs

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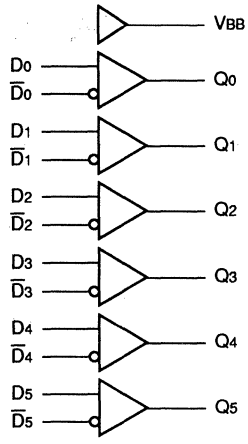
Rev.: B Amendment: /0
Issue Date: April, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	2.5	—	—	V	I_{OH} = –2.0mA	V_{IN} = V_{IH} (Max.)
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 24mA	V_{IN} = V_{IL} (Min.)
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible ±V_{CM} with Respect to V_{BB}	
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.), D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = V_{IL} (Min.)	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IH} (Min.), D_0–D_5 = V_{BB}	
I_{OS}	Output Short Circuit Current	–150	–80	–60	mA	V_{OUT} = GND	
I_{EE}	V_{EE} Power Supply Current	–37	–24	–17	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current	—	42	65	mA	D_0–D_5 = V_{BB}	
V_{BB}	Ouptut Reference Voltage	–1380	–1320	–1260	mV	I_{VBB} = –2.1mA	
V_{IH}	Single-Ended Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to V_{BB})	

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0	2.2	3.0	ns	C_L = 15pF, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0	3.2	3.8	ns	C_L = 50pF, Figure 2

PLCC/FLATPACK

V_{EE} = –4.2V to –5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	2100	2900	ps	C_L = 15pF, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	3100	3700	ps	C_L = 50pF, Figure 2

SWITCHING WAVEFORM

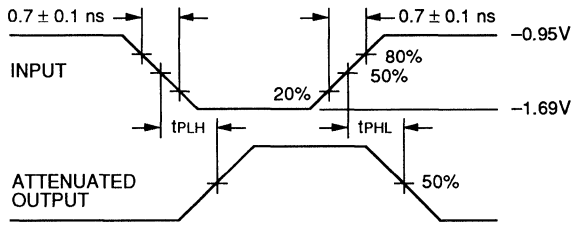


Figure 1. Propagation Delay

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TEST CIRCUITS

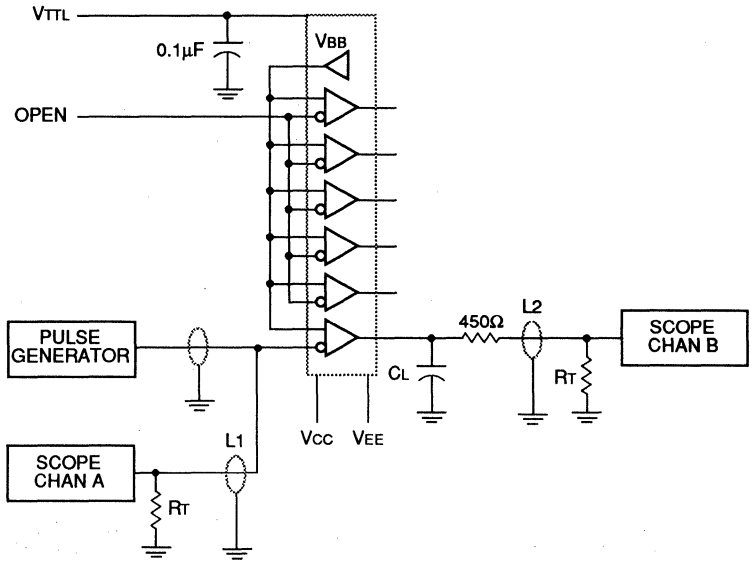


Figure 2. AC Test Circuit for 15pF Loading

NOTES:
V_{CC} = 0V, V_{EE} = –4.5V, V_{TTL} = +5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 3pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S325DC	D24-1	Commercial
SY100S325FC	F24-1	Commercial
SY100S325JC	J28-1	Commercial

LOW-POWER OCTAL ECL/TTL BI-DIRECTIONAL TRANSLATOR WITH LATCH

SYNERGY SEMICONDUCTOR

PRELIMINARY
SY100S328

FEATURES

- **Bi-directional translation**
- **ESD protection of 2000V**
- **Latched outputs**
- **Voltage compensated operating range: –4.2V to –5.7V**
- **Fast TTL outputs**
- **Three-state outputs**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

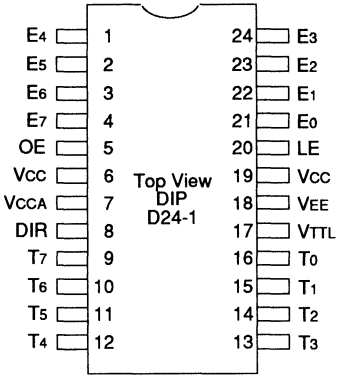
DESCRIPTION

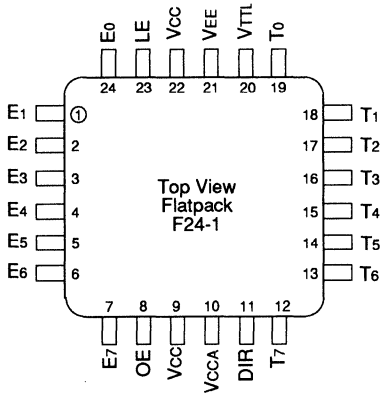
The SY100S328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the SY100S328 transparent.

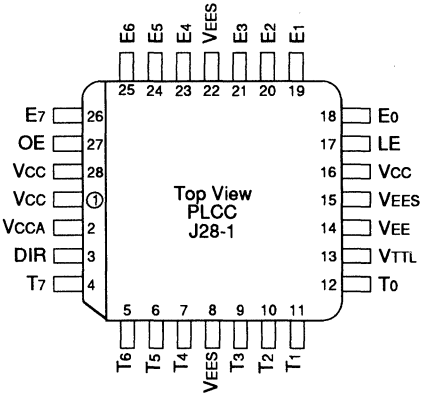
The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The SY100S328 is designed with fast TTL output buffers featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have internal 75KΩ pull-down resistors.

PIN CONFIGURATIONS







PIN NAMES[1]

Pin	Function
E0–E7	ECL Data I/O
T0–T7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

NOTE:

1. All pins function at 100K ECL levels except for T0–T7.

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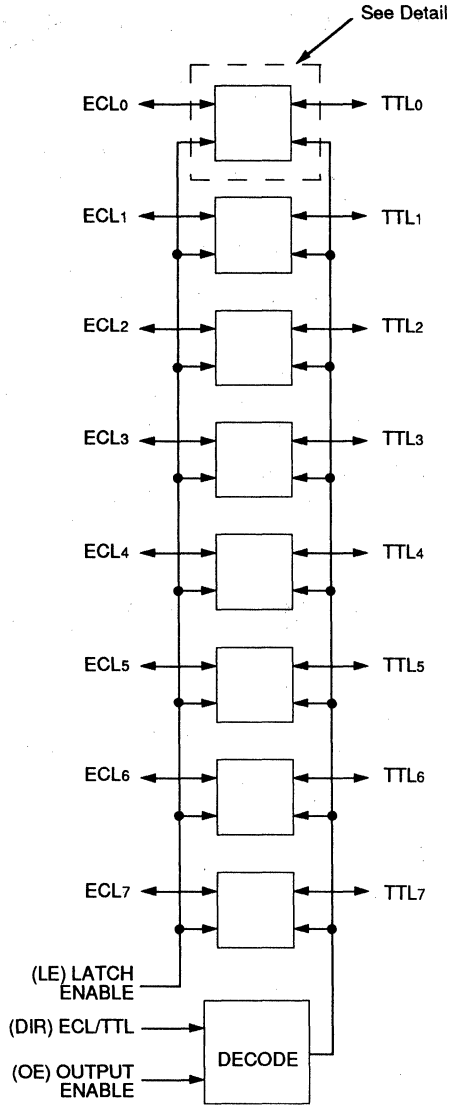
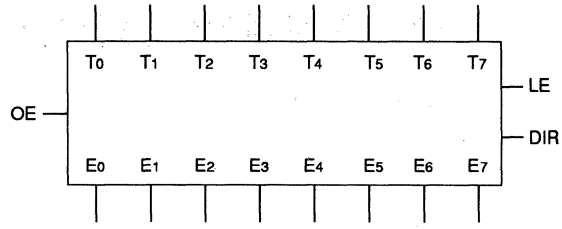
Rev.: B Amendment: /0
Issue Date: February, 1994

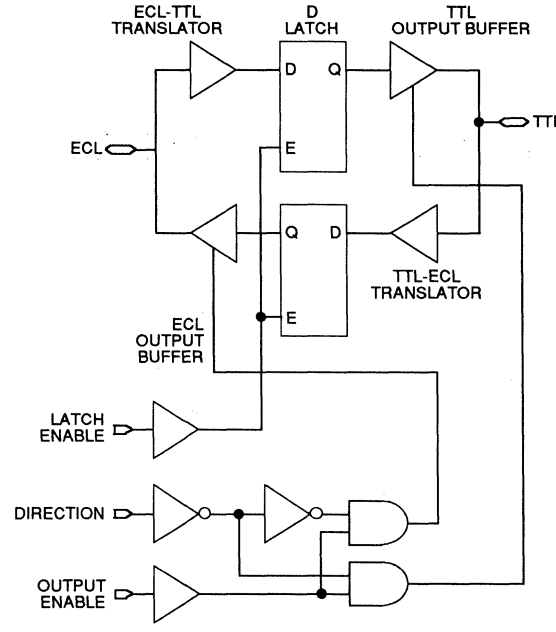
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



DETAIL



NOTE:

1. LE, DIR and OE use ECL logic levels.

TRUTH TABLE[1]

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	—
L	L	H	Input	Z	2, 4
L	H	H	LOW (Cut-Off)	Input	3, 4
H	L	L	L	L	2, 5
H	L	L	H	H	2, 5
H	L	H	X	Latched	2, 4
H	H	L	L	L	3, 5
H	H	L	H	H	3, 5
H	H	H	Latched	X	3, 4

NOTES:
1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = High Impedance.
2. ECL input to TTL output mode.
3. TTL input to ECL output mode.
4. Retains data present before LE is set HIGH.
5. Latch is transparent.

GUARANTEED OPERATING CONDITIONS

Symbol	Rating	Value	Unit
V_{EE}	ECL Supply Voltage	–5.7 to –4.2	V
V_{TTL}	TTL Supply Voltage	+4.5 to +5.5	V
T_C	Case Temperature	0 to +85	°C

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_J	Maximum Junction Temperature Ceramic Plastic	 +175 +150	°C
V_{EE}	V_{EE} Pin Potential to Ground Pin	–7.0 to +0.5	V
V_{TTL}	V_{TTL} Pin Potential to Ground Pin	–0.5 to +6.0	V
—	ECL Input Voltage (DC)	V_{EE} to +0.5	V
—	ECL Output Current (DC Output HIGH)	–50	mA
—	TTL Input Voltage[2]	–0.5 to +6.0	V
—	TTL Input Current[2]	–30 to +5.0	mA
—	Voltage Applied to Output in HIGH State (Three-state Output)	–0.5 to +5.5	V
—	Current Applied to TTL Output in LOW State (Max.)	Twice the Rated I_{OL}	mA

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

TTL-TO-ECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1025	–955	–870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	–1830	–1705	–1620	mV	Loading with 50Ω to –2V
	Cutoff Voltage	—	–2000	–1950	mV	OE or DIR Low, V_{IN} = V_{IH} (Max.) or V_{IL} (Min.), Loading with 50Ω to –2V
V_{OHC}	Output HIGH Voltage Corner Point High	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	–1610	mV	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current	—	—	70	µA	V_{IN} = +2.7V
	Breakdown Test	—	—	1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	–700	—	—	µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{EE}	V_{EE} Supply Current	–159 –169	— —	–75 –75	mA	LE Low, OE and DIR High, Inputs Open V_{EE} = –4.2V to –4.8V V_{EE} = –4.2V to –5.7V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

ECL-TO-TTL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50pF, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9	— —	V	I_{OH} = –3mA, V_{TTL} = 4.75V I_{OH} = –3mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	I_{OL} = 24mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	–1165	—	–870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	–1830	—	–1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	V_{IN} = V_{IL} (Min.)
I_{OZHT}	Three-State Current Output High	—	—	70	µA	V_{OUT} = +2.7V
I_{OZLT}	Three-State Current Output Low	–700	—	—	µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	–150	—	–60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current	—	—	74	mA	V_{TTL} = +5.5V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Tn to En (Transparent)	1.1	3.5	1.1	3.6	1.1	3.8	ns	Figures 1 & 2
tPLH tPHL	LE to En	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1 & 2
tPZH	OE to En (Cutoff to High)	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1 & 2
tPHZ	OE to En (High to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1 & 2
tPHZ	DIR to En (High to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1 & 2
tset	Tn to LE	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
thold	Tn to LE	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
tpw(H)	Pulse Width LE	2.1	—	2.1	—	2.1	—	ns	Figures 1 & 2
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, C_L = 50pF[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	En to Tn (Transparent)	2.3	5.6	2.4	5.6	2.6	5.9	ns	Figures 3 & 4
tPLH tPHL	LE to Tn	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3 & 4
tPZH tPZL	OE to Tn (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	Figures 3 & 4
tPHZ tPLZ	OE to Tn (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	Figures 3 & 4
tPHZ tPLZ	DIR to Tn (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	Figures 3 & 4
tset	En to LE	1.1	—	1.1	—	1.1	—	ns	Figures 3 & 4
thold	En to LE	2.1	—	2.1	—	2.6	—	ns	Figures 3 & 4
tPW (H)	En to LE	4.1	—	4.1	—	4.1	—	ns	Figures 3 & 4

NOTE:

1. The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

PLCC and FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.1	3.3	1.1	3.4	1.1	3.6	ns	Figures 1 & 2
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns	Figures 1 & 2
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.0	1.5	4.2	1.7	4.6	ns	Figures 1 & 2
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	Figures 1 & 2
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	Figures 1 & 2
t_{set}	T_n to LE	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{hold}	T_n to LE	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{pw} (H)	Pulse Width LE	2.0	—	2.0	—	2.0	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	PLCC Only(1)
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	PLCC Only(1)
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	650	—	650	—	650	ps	PLCC Only(1)
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	650	—	650	—	650	ps	PLCC Only(1)

NOTE:

1. Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction — either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) — or in opposite directions, both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} are guaranteed by design.

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

PLCC and FLATPACK

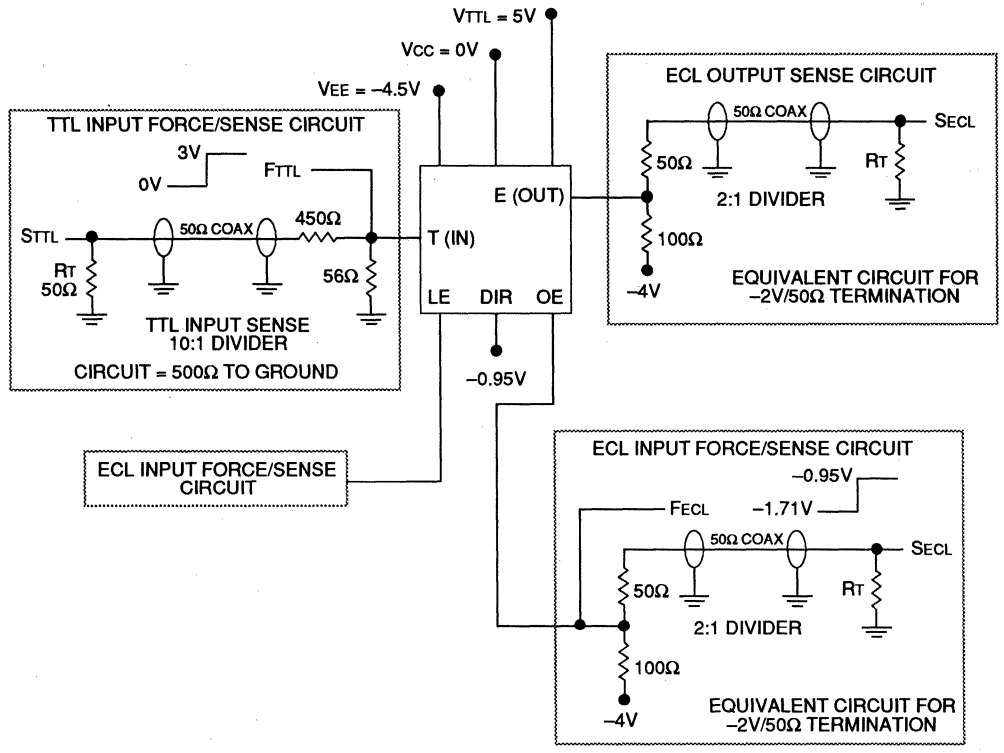
V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50pF

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	En to Tn (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	Figures 3 & 4
t_{PLH} t_{PHL}	LE to Tn	3.1	7.0	3.1	7.0	3.3	7.5	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	Figures 3 & 6
t_{set}	En to LE	1.0	—	1.0	—	1.0	—	ns	Figures 3 & 4
t_{hold}	En to LE	2.0	—	2.0	—	2.5	—	ns	Figures 3 & 4
t_{pw} (H)	Pulse Width LE	4.0	—	4.0	—	4.0	—	ns	Figures 3 & 4
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	600	—	600	—	600	ps	PLCC Only(1)
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	850	—	850	—	850	ps	PLCC Only(1)
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	1350	—	1350	—	1350	ps	PLCC Only(1)
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	950	—	950	—	950	ps	PLCC Only(1)

NOTE:

1. Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction — either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) — or in opposite directions, both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} are guaranteed by design.

TEST CIRCUITRY (TTL-TO-ECL)



NOTES:

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. For ECL input pins, the equivalent force/sense circuitry is optional.

Figure 1. TTL-to-ECL AC Test Circuit

SWITCHING WAVEFORMS (TTL-TO-ECL)

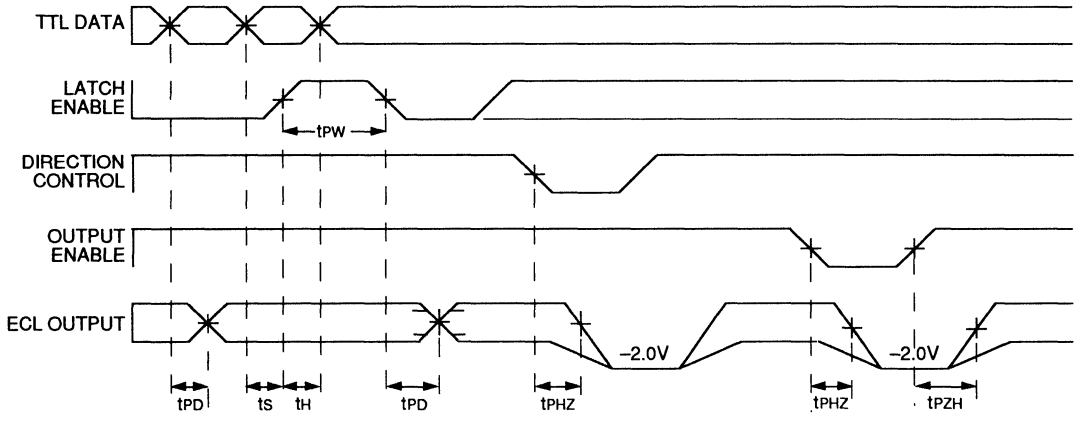


Figure 2. TTL-to-ECL Transition — Propagation Delay and Transition Times

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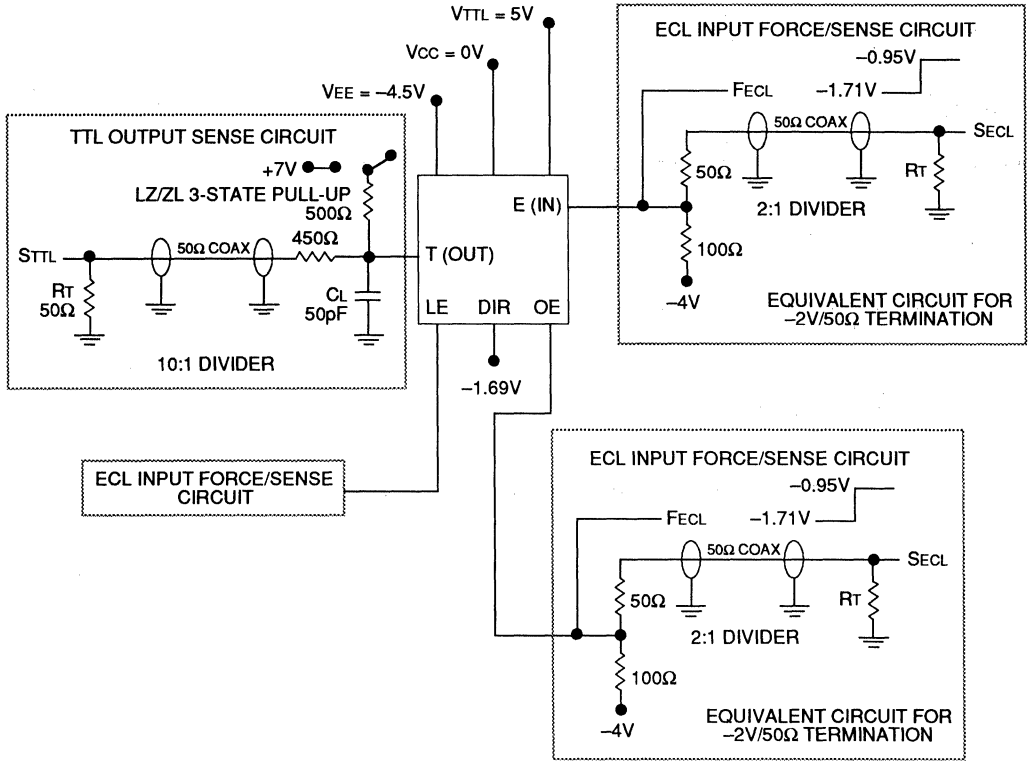
TEST CIRCUITRY (ECL-TO-TTL)

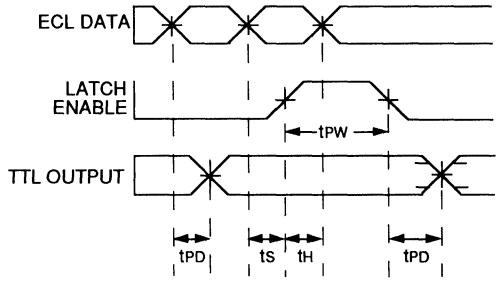


NOTES;

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. The TTL three-state pull-up switch is connected to +7V only for ZL and LZ tests.

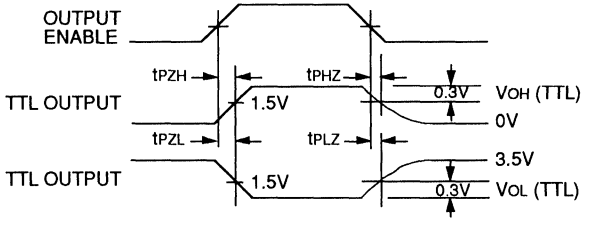
Figure 3. ECL-to-TTL AC Test Circuit

SWITCHING WAVEFORMS (ECL-TO-TTL)



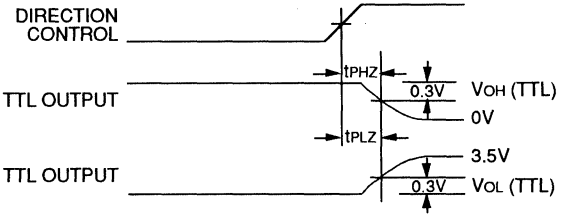
NOTE:
1. DIR is LOW and OE is HIGH.

Figure 4. ECL-to-TTL Transition, Propagation Delay and Transition Times



NOTE:
1. DIR is LOW and LE is HIGH.

Figure 5. ECL-to-TTL Transition, OE to TTL Output Enable and Disable Times



NOTE:
1. OE is HIGH and LE is HIGH.

Figure 6. ECL-to-TTL Transition, DIR to TTL Output Disable Time

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APPLICATIONS

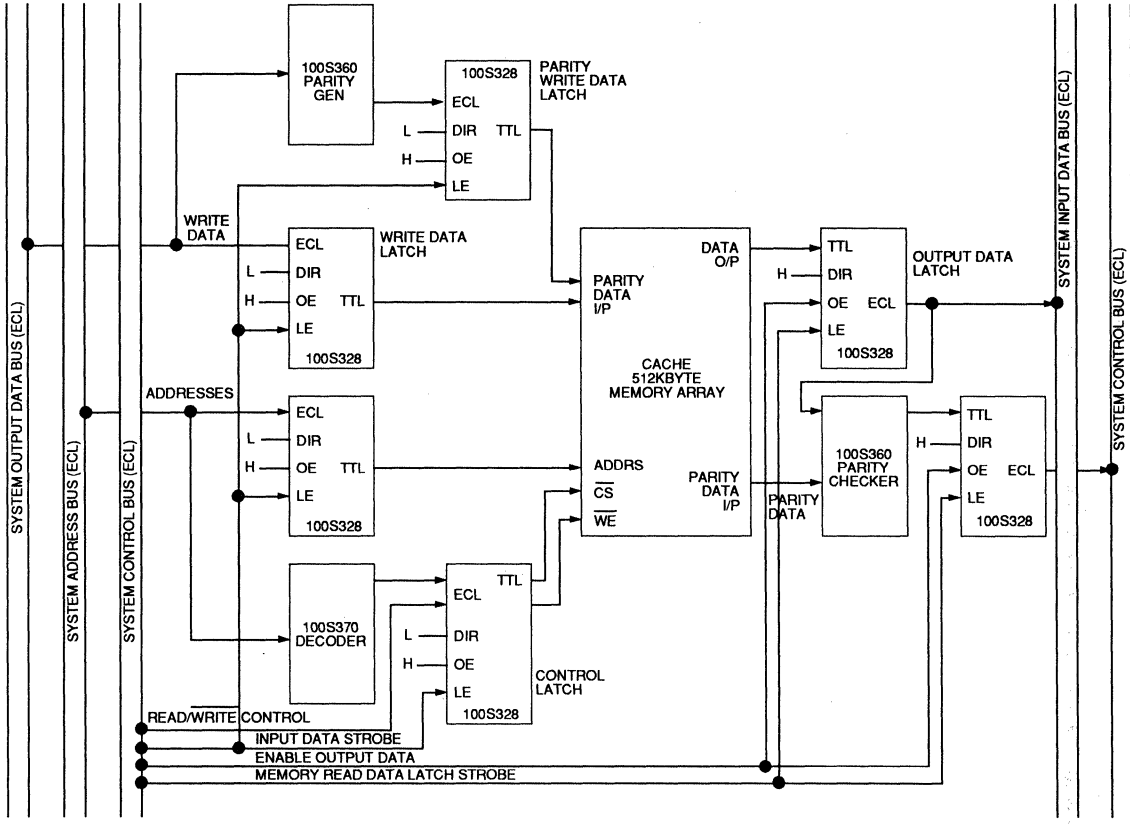


Figure 7. Applications Diagram — MOS/TTL SRAM Interface Using SY100S328 ECL-TTL Latched Translator

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S282DC	D24-1	Commercial
SY100S328FC	F24-1	Commercial
SY100S328JC	J28-1	Commercial

LOW-POWER OCTAL ECL/TTL BI-DIRECTIONAL TRANSLATOR WITH REGISTER

SYNERGY SEMICONDUCTOR

PRELIMINARY
SY100S329

FEATURES

- **Bi-directional translation**
- **ESD protection of 2000V**
- **ECL high impedance outputs**
- **Registered outputs**
- **Voltage compensated operating range: –4.2V to –5.7V**
- **Fast TTL outputs**
- **Three-state outputs**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP and CERPACK**

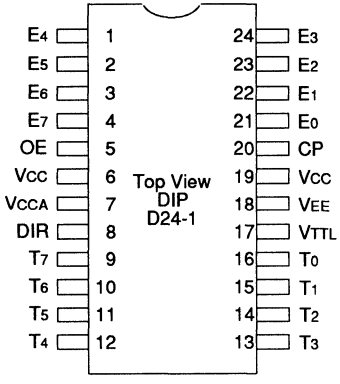
DESCRIPTION

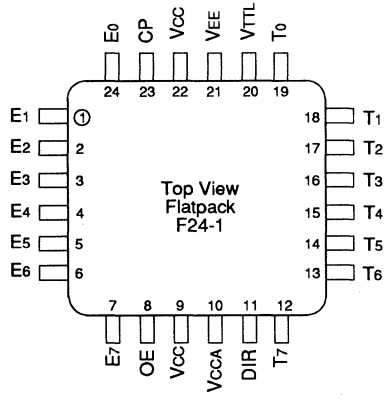
The SY100S329 is an octal registered bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The SY100S329 is designed with fast TTL output buffers featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have internal 75KΩ pull-down resistors.

PIN CONFIGURATIONS





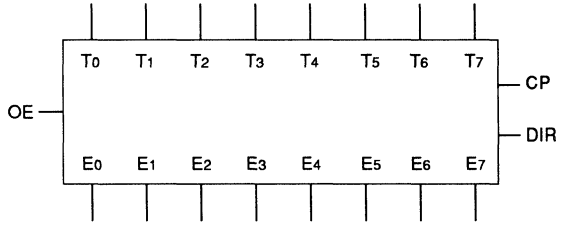
PIN NAMES(1)

Pin	Function
E0–E7	ECL Data I/O
T0–T7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

NOTE:

1. All pins function at 100K ECL levels except for T0–T7.

LOGIC SYMBOL



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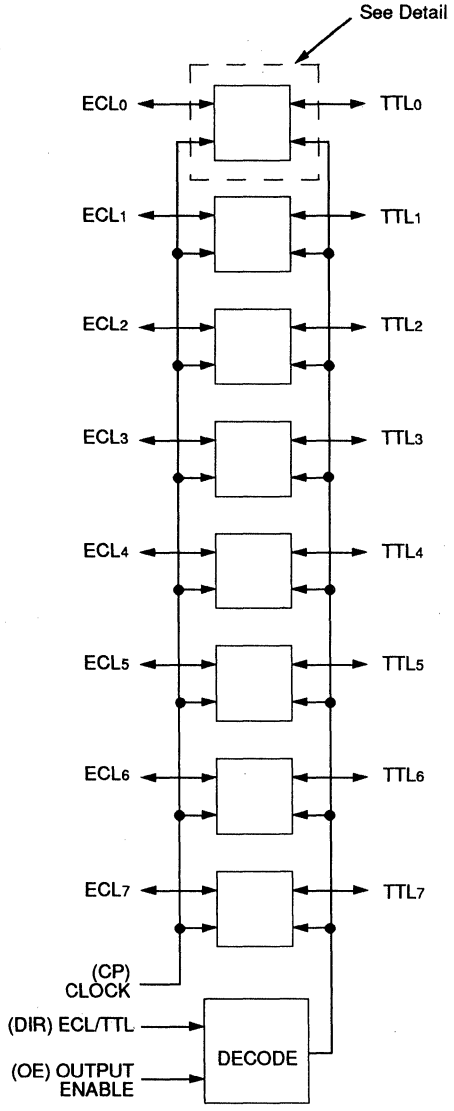
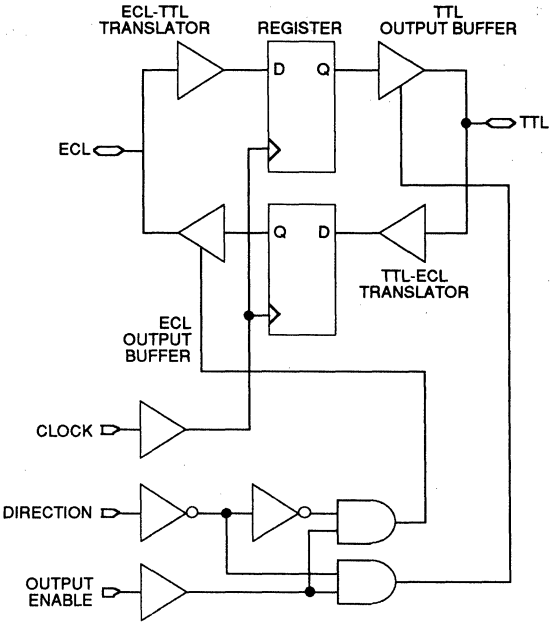
Rev.: B Amendment: /0
Issue Date: February, 1994

FUNCTIONAL BLOCK DIAGRAM



DETAIL



NOTE:

1. CP, DIR and OE use ECL logic levels.

TRUTH TABLE[1]

OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	2, 4
L	H	X	LOW (Cut-Off)	Input	3, 4
H	L	↓	L	L	2
H	L	↓	H	H	2
H	L	L	X	NC	2, 4
H	H	↓	L	L	3
H	H	↓	H	H	3
H	H	L	NC	X	3, 4

NOTES:
1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = High Impedance.
2. ECL input to TTL output mode.
3. TTL input to ECL output mode.
4. Retains data present before CP.

GUARANTEED OPERATING CONDITIONS

Symbol	Rating	Value	Unit
V_{EE}	ECL Supply Voltage	–5.7 to –4.2	V
V_{TTL}	TTL Supply Voltage	+4.5 to +5.5	V
T_C	Case Temperature	0 to +85	°C

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_J	Maximum Junction Temperature Ceramic Plastic	 +175 +150	°C
V_{EE}	V_{EE} Pin Potential to Ground Pin	–7.0 to +0.5	V
V_{TTL}	V_{TTL} Pin Potential to Ground Pin	–0.5 to +6.0	V
—	ECL Input Voltage (DC)	V_{EE} to +0.5	V
—	ECL Output Current (DC Output HIGH)	–50	mA
—	TTL Input Voltage[2]	–0.5 to +6.0	V
—	TTL Input Current[2]	–30 to +5.0	mA
—	Voltage Applied to Output in HIGH State (Three-state Output)	–0.5 to +5.5	V
—	Current Applied to TTL Output in LOW State (Max.)	Twice the Rated I_{OL}	mA

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

TTL-TO-ECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1025	–955	–870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	–1830	–1705	–1620	mV	Loading with 50Ω to –2V
	Cutoff Voltage	—	–2000	–1950	mV	OE or DIR Low, V_{IN} = V_{IH} (Max.) or V_{IL} (Min.), Loading with 50Ω to –2V
V_{OHC}	Output HIGH Voltage Corner Point High	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	–1610	mV	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current	—	—	70	µA	V_{IN} = +2.7V
	Breakdown Test	—	—	1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	–700	—	—	µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{EE}	V_{EE} Supply Current	 –189 –199	 — —	 –94 –94	mA	LE Low, OE and DIR High, Inputs Open V_{EE} = –4.2V to –4.8V V_{EE} = –4.2V to –5.7V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

ECL-TO-TTL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50pF, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9	— —	V	I_{OH} = –3mA, V_{TTL} = 4.75V I_{OH} = –3mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	I_{OL} = 24mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	–1165	—	–870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	–1830	—	–1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	V_{IN} = V_{IL} (Min.)
I_{OZHT}	Three-State Current Output High	—	—	70	µA	V_{OUT} = +2.7V
I_{OZLT}	Three-State Current Output Low	–700	—	—	µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	–150	—	–60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current	—	—	74	mA	V_{TTL} = +5.5V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	350	—	350	—	350	—	MHz	—
t_{PLH} t_{PHL}	CP to En	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1 & 2
t_{PZH}	OE to En (Cutoff to HIGH)	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1 & 2
t_{PHZ}	OE to En (HIGH to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1 & 2
t_{PHZ}	DIR to En (HIGH to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1 & 2
t_{set}	Tn to CP	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
t_{hold}	Tn to CP	1.7	—	1.7	—	1.9	—	ns	Figures 1 & 2
t_{pw}(H)	Pulse Width CP	2.1	—	2.1	—	2.1	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, C_L = 50pF[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	125	—	125	—	125	—	MHz	—
t_{PLH} t_{PHL}	CP to Tn	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	Figures 3 & 6
t_{set}	En to CP	1.1	—	1.1	—	1.1	—	ns	Figures 3 & 4
t_{hold}	En to CP	2.1	—	2.1	—	2.6	—	ns	Figures 3 & 4
t_{PW} (H)	Pulse Width CP	4.1	—	4.1	—	4.1	—	ns	Figures 3 & 4

NOTE:

1. The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	350	—	350	—	350	—	MHz	—
t_{PLH} t_{PHL}	CP to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns	Figures 1 & 2
t_{PZH}	OE to E_n (Cutoff to HIGH)	1.3	4.0	1.5	4.2	1.7	4.6	ns	Figures 1 & 2
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	Figures 1 & 2
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	Figures 1 & 2
t_{set}	T_n to CP	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{hold}	T_n to CP	1.7	—	1.7	—	1.7	—	ns	Figures 1 & 2
t_{pw} (H)	Pulse Width CP	2.0	—	2.0	—	2.0	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	—
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	—
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	650	—	650	—	650	ps	—
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	650	—	650	—	650	ps	—

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50pF

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	125	—	125	—	125	—	MHz	—
t_{PLH} t_{PHL}	CP to Tn	3.1	7.0	3.1	7.0	3.3	7.5	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	Figures 3 & 6
t_{set}	En to CP	1.0	—	1.0	—	1.0	—	ns	Figures 3 & 4
t_{hold}	En to CP	2.0	—	2.0	—	2.5	—	ns	Figures 3 & 4
t_{pw} (H)	Pulse Width CP	4.0	—	4.0	—	4.0	—	ns	Figures 3 & 4
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	600	—	600	—	600	ps	—
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	850	—	850	—	850	ps	—
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	1350	—	1350	—	1350	ps	—
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	950	—	950	—	950	ps	—

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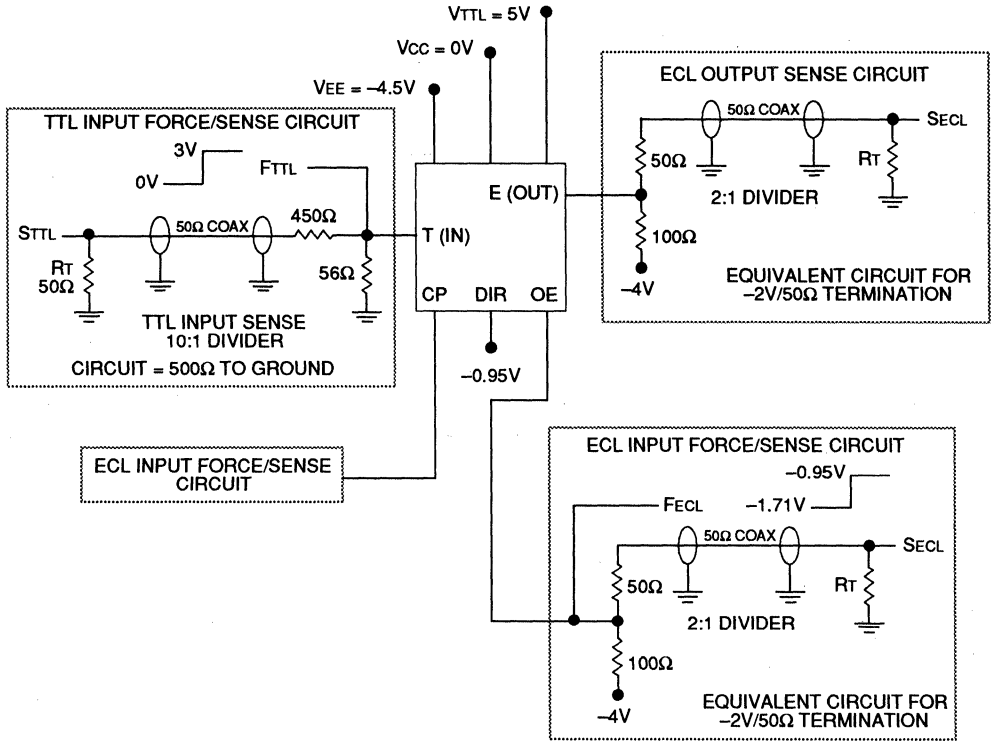
TEST CIRCUITRY (TTL-TO-ECL)



NOTES:

1. Rt = 50Ω termination. When an input or output is being monitored by a scope, Rt is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as Rt.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. VTTL is decoupled to ground with a 0.1μF capacitor, VEE is decoupled to ground with a 0.01μF capacitor and VCC is connected to ground.
4. For ECL input pins, the equivalent force/sense circuitry is optional.

Figure 1. TTL-to-ECL AC Test Circuit

SWITCHING WAVEFORMS (TTL-TO-ECL)

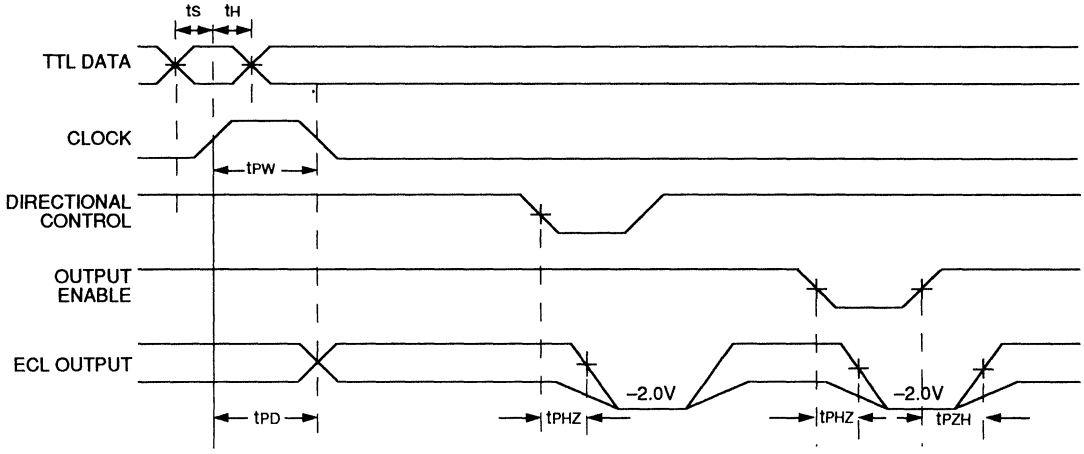
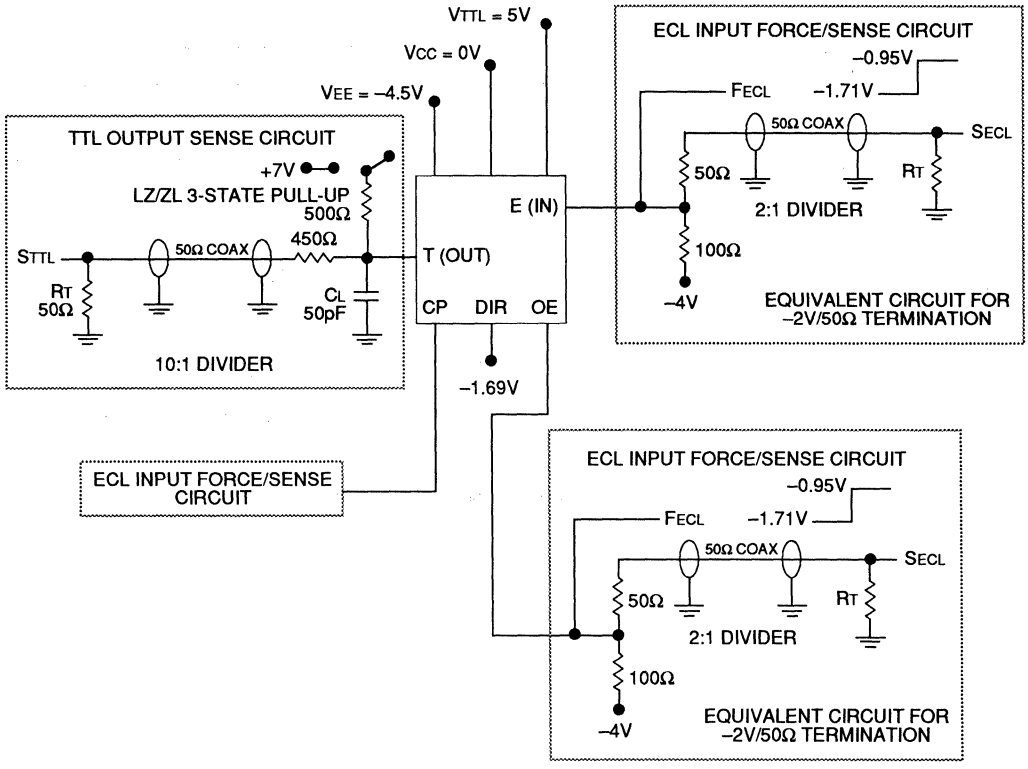


Figure 2. TTL-to-ECL Propagation Delay and Transition Times

6

TEST CIRCUITRY (ECL-TO-TTL)

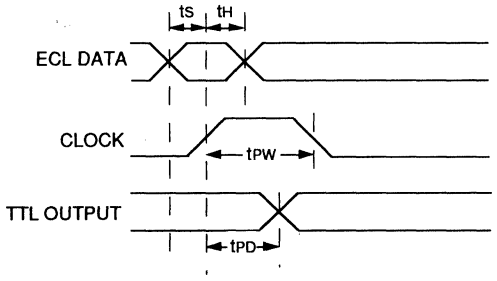


NOTES;

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. The TTL three-state pull-up switch is connected to +7V only for ZL and LZ tests.

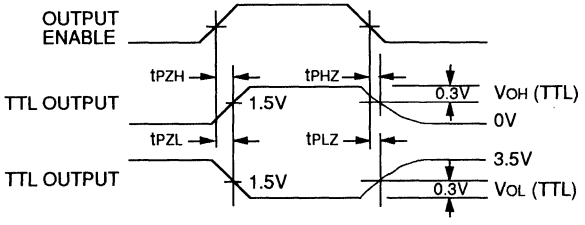
Figure 3. ECL-to-TTL AC Test Circuit

SWITCHING WAVEFORMS (ECL-TO-TTL)



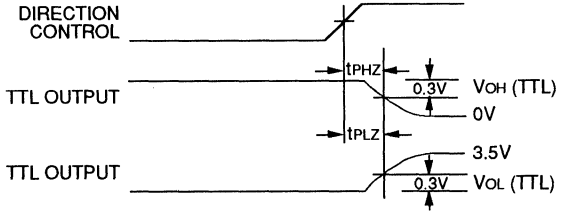
NOTE:
1. DIR is LOW and OE is HIGH.

Figure 4. ECL-to-TTL Transition, Propagation Delay and Transition Times



NOTE:
1. DIR is LOW and LE is HIGH.

Figure 5. ECL-to-TTL Transition, OE to TTL Output Enable and Disable Times



NOTE:
1. OE is HIGH and LE is HIGH.

Figure 6. ECL-to-TTL Transition, DIR to TTL Output Disable Time

PRODUCT ORDERING CODE

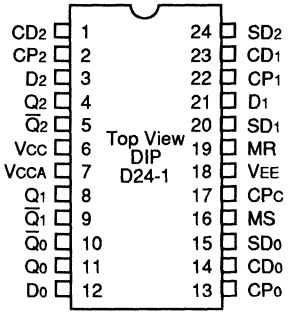
Ordering Code	Package Type	Operating Range
SY100S329DC	D24-1	Commercial
SY100S329FC	F24-1	Commercial

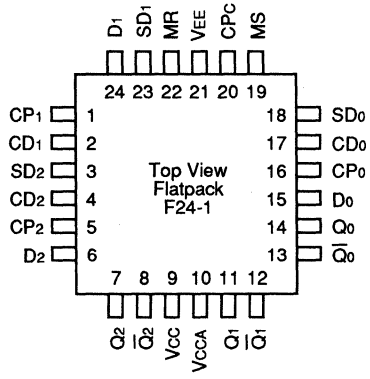
6

FEATURES

- **Max. toggle frequency of 800MHz**
- **Differential outputs**
- **IEE min. of –80mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **150% faster than National or Signetics**
- **40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

PIN CONFIGURATIONS





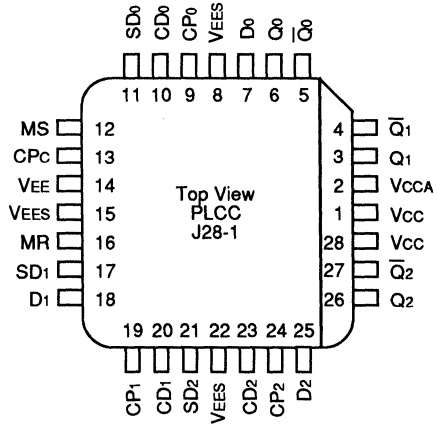
DESCRIPTION

The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CPC), as well as its own clock pulse (CPn). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CPC and CPn are LOW and enters the slave on the rising edge of either CPC or CPn (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SDn) and Direct Clear (CDn) signals. The MR, MS, SDn and DCn signals override the clock signals. The inputs on this device have 75KΩ pull-down resistors.

PIN NAMES

Pin	Function
CP0 – CP2	Individual Clock Inputs
CPC	Common Clock Input
D0 – D2	Data Inputs
CD0 – CD2	Individual Direct Clear Inputs
SDn	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q0 – Q2	Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs



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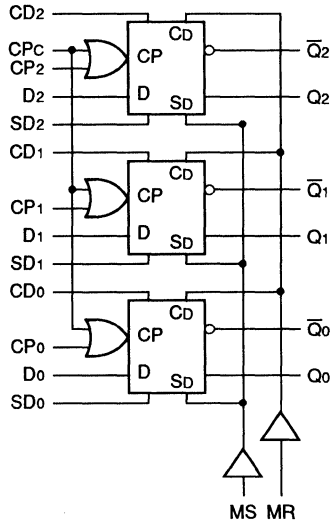
BLOCK DIAGRAM



TRUTH TABLES

Asynchronous Operation[1]

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR DC_n	Q_n (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, ⨍ = Low-to-High Transition

Synchronous Operation[1]

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR DC_n	Q_n
L	⨍	L	L	L	L
H	⨍	L	L	L	H
L	L	⨍	L	L	L
H	L	⨍	L	L	H
X	L	L	L	L	Q_n (t)
X	H	X	L	L	Q_n (t)
X	X	H	L	L	Q_n (t)

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, ⨍ = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–80	–65	–35	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	300	900	300	900	300	900	ps	—
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	900	300	900	300	900	ps	—
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	300	1000	300	1000	300	1000	ps	—
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	1100	300	1100	300	1100	ps	—
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
t_S	Set-up Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 400 500 800	 — — —	 400 500 800	 — — —	 400 500 800	 — — —	ps	—
t_n	Hold Time D_n	300	—	300	—	300	—	ps	—
t_{pw} (H)	Pulse Width HIGH CP_n, CP_C, DC_n SD_n, MR, MS	800	—	800	—	800	—	ps	—

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	300	800	300	800	300	800	ps	—
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	800	300	800	300	800	ps	—
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	300	900	300	900	300	900	ps	—
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	1000	300	1000	300	1000	ps	—
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
t_S	Set-up Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 400 500 800	 — — —	 400 500 800	 — — —	 400 500 800	 — — —	ps	—
t_n	Hold Time D_n	300	—	300	—	300	—	ps	—
t_{pw} (H)	Pulse Width HIGH CP_n, CP_C, DC_n SD_n, MR, MS	800	—	800	—	800	—	ps	—

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay CP_c to Output	300	700	300	700	300	700	ps	—
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	300	700	300	700	300	700	ps	—
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	300	800	300	800	300	800	ps	—
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	900	300	900	300	900	ps	—
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	—
t_S	Set-up Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 400 500 800	 — — —	 400 500 800	 — — —	 400 500 800	 — — —	ps	—
t_n	Hold Time D_n	300	—	300	—	300	—	ps	—
t_{pw} (H)	Pulse Width HIGH CP_n, CP_c, DC_n SD_n, MR, MS	800	—	800	—	800	—	ps	—

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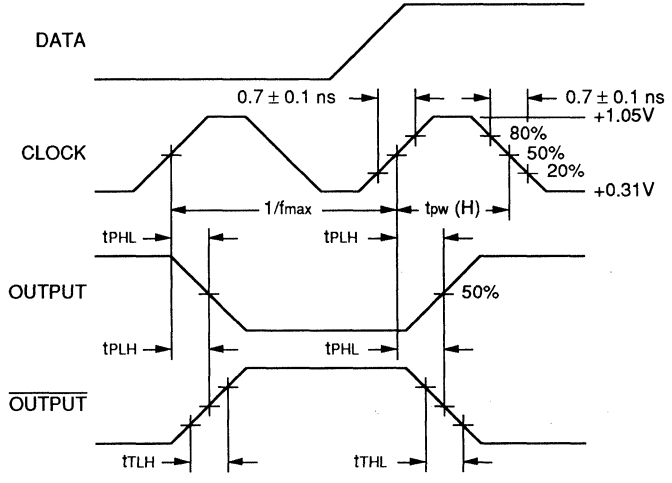
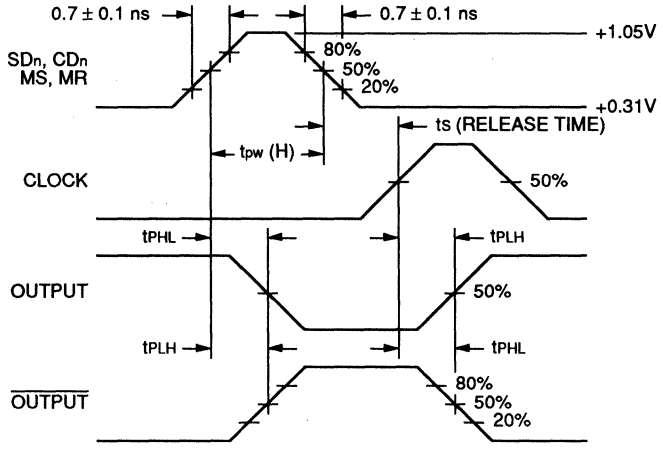
TIMING DIAGRAMS



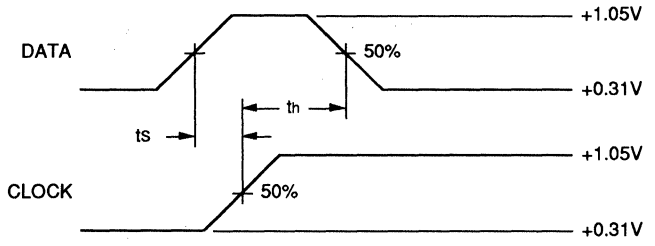
Propagation Delay (Clock) and Transition Times

TIMING DIAGRAMS (CONT'D.)



Propagation Delay (Sets and Resets)

NOTE:
SDn uses complement of DATA and complement of OUTPUT waveforms.



Data Setup and Hold Time

NOTES:
ts is the minimum time before the transition of the clock that information must be present at the data input.
th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S331DC	D24-1	Commercial
SY100S331FC	F24-1	Commercial
SY100S331JC	J28-1	Commercial

4-STAGE COUNTER/ SHIFT REGISTER

FEATURES

- **Max. shift frequency of 700MHz**
- **Clock to Q delay max. of 1100ps**
- **IEE min. of –170mA**
- **ESD protection of 2000V**
- **Internal 75KΩ input pull-down resistors**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **50% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

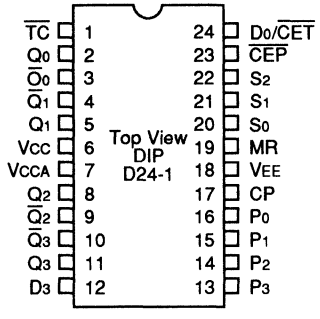
DESCRIPTION

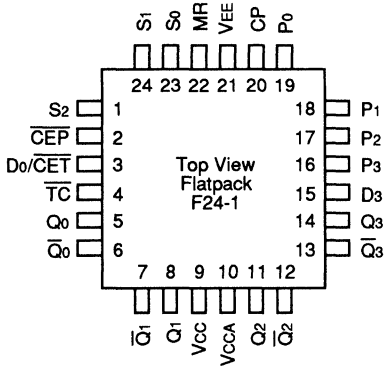
The SY100S336 functions either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register and is designed for use in high-performance ECL systems. Three Select inputs (Sn) are provided for determining the mode of operation. The Function Table lists the available modes of operation. In order to allow cascading for multistage counters, two Count Enable controls ($\overline{CEP}$, $\overline{CET}$) are provided. The $\overline{CET}$ input also functions as the Serial Data input (S_0) for a shift-up operation, while the D_3 input serves as the Serieal Data input for the shift-down operation.

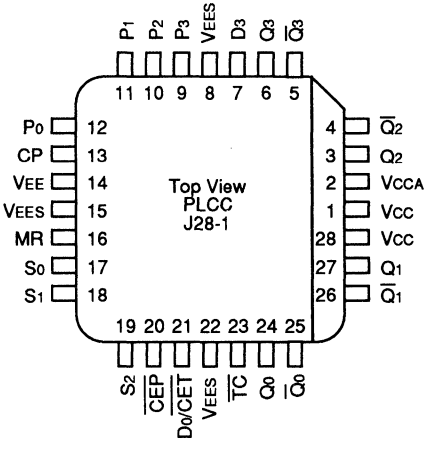
When the device is in the counting mode, the Terminal Count ($\overline{TC}$) goes to a logical LOW when the count reaches 15 for count-up or reaches 0 for count-down. When in the shift mode, the $\overline{TC}$ output simply repeats the Q_3 output.

The flexiblity provided by the $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input allows these signals to be interconnected from one stage to the next higher stage for multistage counting or shift-up operations. The individual Presets (P_n) allow initialization of the counter by entering data in parallel to preset the counter. A logic HIGH on the Master Reset (MR) overrides all other inputs and asynchronously clears the flip-flops. An additional synchronous Clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 75KΩ pull-down resistors.

PIN CONFIGURATIONS







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Rev.: B Amendment: /0
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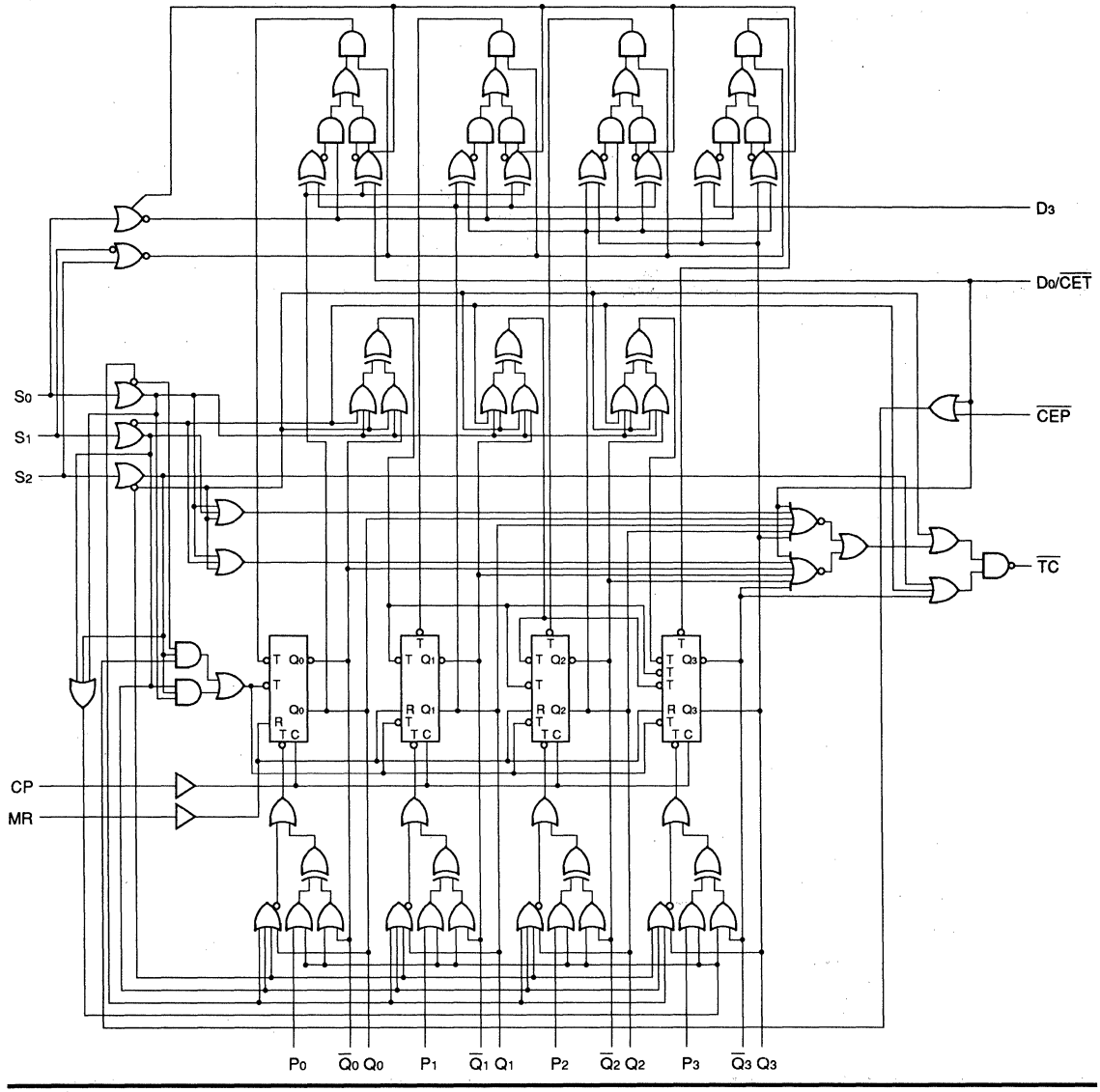
PIN NAMES

Label	Function
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0 — S_2	Select Inputs
MR	Master Reset Input

Label	Function
P_0 – P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0 — Q_3	Data Outputs
$\overline{Q}_0$ — $\overline{Q}_3$	Complementary Data Outputs

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↑	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↑	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	L	H	L	X	X	X	↑	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	X	X	X	↑	D_0	Q_0	Q_1	Q_2	Q_3*	Shift Right
L	H	L	L	L	L	X	↑	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ Not Active
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ Not Active
L	H	L	H	X	X	X	↑	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↑	(Q_{0-3}) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ Not Active
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ Not Active
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   ① = L if $Q_0 - Q_3$ = LLLL
   H if $Q_0 - Q_3 \neq$ LLLL
   ② = L if $Q_0 - Q_3$ = HHHH
   H if $Q_0 - Q_3 \neq$ HHHH
   * Before the clock, $\overline{TC}$ is Q_3; after the clock, $\overline{TC}$ is Q_2

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–170	–145	–90	mA	Inputs Open

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AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	450	1300	450	1300	450	1300	ps
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	2000	600	2000	600	2000	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	500	1500	500	1500	500	1500	ps
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	2000	600	2000	600	2000	ps
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	400	1300	400	1300	400	1300	ps
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1500	2700	1500	2700	1500	2700	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_3	800	—	800	—	800	—	
	P_n	800	—	800	—	800	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	700	—	700	—	700	—	
	S_n	2000	—	2000	—	2000	—	
	MR (Release Time)	900	—	900	—	900	—	
t_h	Hold Time							ps
	D_3	200	—	200	—	200	—	
	P_n	200	—	200	—	200	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	200	—	200	—	200	—	
	S_n	–600	—	–600	—	–600	—	
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q_n}$	450	1200	450	1200	450	1200	ps
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	1900	600	1900	600	1900	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q_n}$	500	1400	500	1400	500	1400	ps
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	1900	600	1900	600	1900	ps
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	400	1200	400	1200	400	1200	ps
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1500	2600	1500	2600	1500	2600	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_3	800	—	800	—	800	—	
	P_n	800	—	800	—	800	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	700	—	700	—	700	—	
	S_n	2000	—	2000	—	2000	—	
	MR (Release Time)	900	—	900	—	900	—	
t_h	Hold Time							ps
	D_3	200	—	200	—	200	—	
	P_n	200	—	200	—	200	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	200	—	200	—	200	—	
	S_n	–600	—	–600	—	–600	—	
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps

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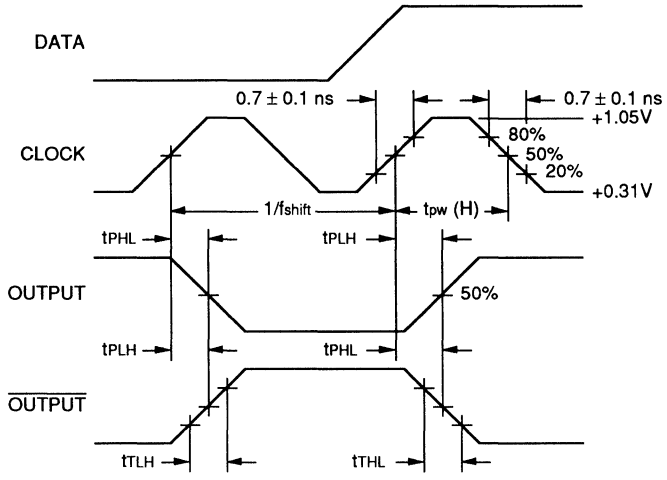
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

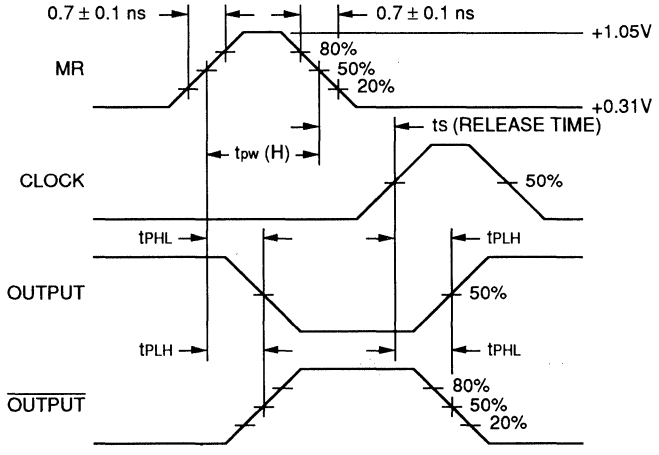
V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q_n}$	450	1100	450	1100	450	1100	ps
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	1800	600	1800	600	1800	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q_n}$	500	1300	500	1300	500	1300	ps
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	1800	600	1800	600	1800	ps
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	400	1100	400	1100	400	1100	ps
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1500	2500	1500	2500	1500	2500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_3	800	—	800	—	800	—	
	P_n	800	—	800	—	800	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	700	—	700	—	700	—	
	S_n	2000	—	2000	—	2000	—	
	MR (Release Time)	900	—	900	—	900	—	
t_h	Hold Time							ps
	D_3	200	—	200	—	200	—	
	P_n	200	—	200	—	200	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	200	—	200	—	200	—	
	S_n	–600	—	–600	—	–600	—	
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps

TIMING DIAGRAMS

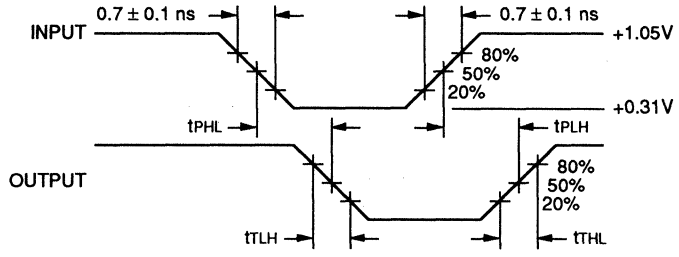


Propagation Delay (Clock) and Transition Times

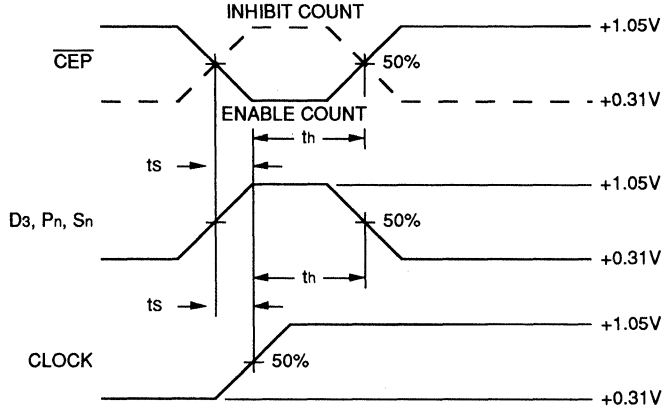


Propagation Delay (Reset)

TIMING DIAGRAMS (CONT'D.)



Propagation Delay (Serial Data, Selects)



Set-up and Hold Time

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

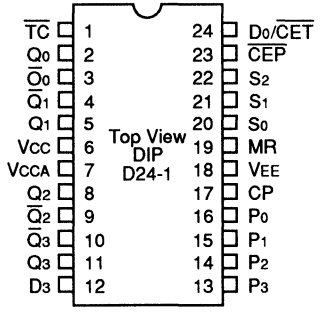
Ordering Code	Package Type	Operating Range
SY100S336DC	D24-1	Commercial
SY100S336FC	F24-1	Commercial
SY100S336JC	J28-1	Commercial

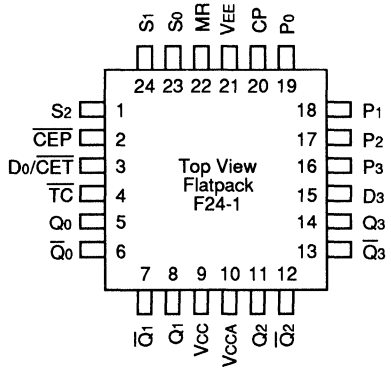
4-STAGE COUNTER/ SHIFT REGISTER

FEATURES

- **Max. shift frequency of 700MHz**
- **Clock to Q delay max. of 1100ps**
- **S_n to $\overline{TC}$ speed improved by 50%**
- **S_n set-up and hold time reduced by more than 50%**
- **I_{EE} min. of –170mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Internal 75KΩ input pull-down resistors**
- **Extended supply voltage option:**
  - **V_{EE} = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **50% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

PIN CONFIGURATIONS





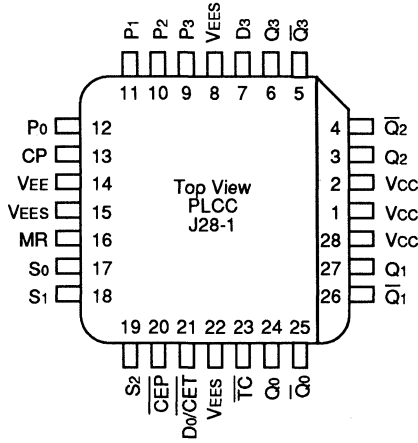
DESCRIPTION

The SY100S336A is functionally the same as the SY100S336, but has S_n to $\overline{TC}$ speed and Sn set-up and hold times significantly improved, allowing for higher clock frequency when used as a cascaded multi-stage counter.

The SY100S336A functions either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register and is designed for use in high-performance ECL systems. Three Select inputs (Sn) are provided for determining the mode of operation. The Function Table lists the available modes of operation. In order to allow cascading for multistage counters, two Count Enable controls ($\overline{CEP}$, $\overline{CET}$) are provided. The $\overline{CET}$ input also functions as the Serial Data input (S_0) for a shift-up operation, while the D_3 input serves as the Serial Data input for the shift-down operation.

When the device is in the counting mode, the Terminal Count ($\overline{TC}$) goes to a logical LOW when the count reaches 15 for count-up or reaches 0 for count-down. When in the shift mode, the $\overline{TC}$ output simply repeats the Q_3 output.

The flexiblity provided by the $\overline{TC}$/Q_3 output and the D_0/$\overline{CET}$ input allows these signals to be interconnected from one stage to the next higher stage for multistage counting or shift-up operations. The individual Presets (P_n) allow initialization of the counter by entering data in parallel to preset the counter. A logic HIGH on the Master Reset (MR) overrides all other inputs and asynchronously clears the flip-flops. An additional synchronous Clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 75KΩ pull-down resistors.



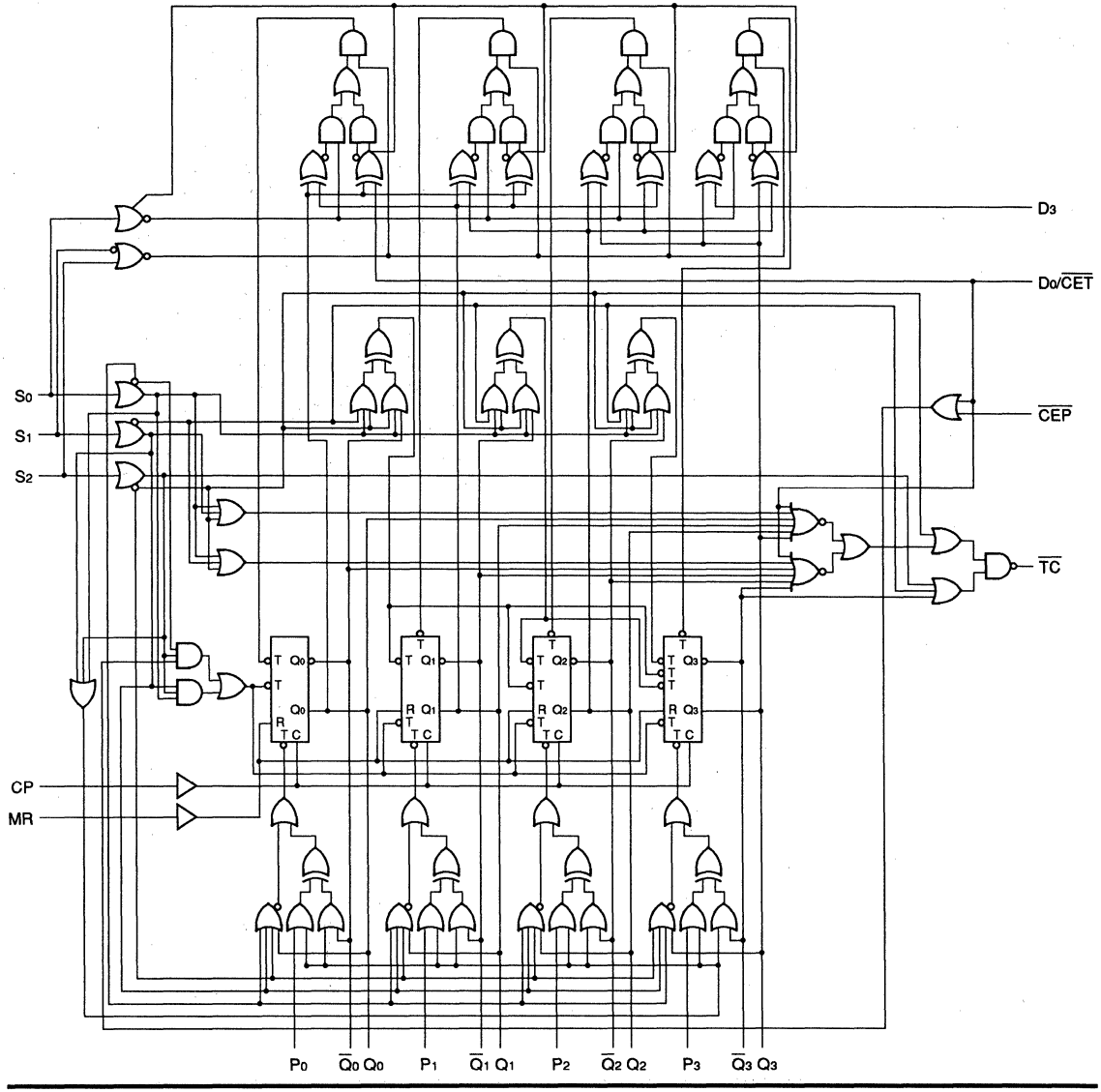
Rev.: B Amendment: /0
Issue Date: February, 1994

PIN NAMES

Label	Function
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0 — S_2	Select Inputs
MR	Master Reset Input

Label	Function
P_0 – P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0 — Q_3	Data Outputs
$\overline{Q}_0$ — $\overline{Q}_3$	Complementary Data Outputs

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↑	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↑	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	L	H	L	X	X	X	↑	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	X	X	X	↑	D_0	Q_0	Q_1	Q_2	Q_3*	Shift Right
L	H	L	L	L	L	X	↑	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ Not Active
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ Not Active
L	H	L	H	X	X	X	↑	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↑	(Q_{0-3}) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ Not Active
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ Not Active
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   ① = L if $Q_0 - Q_3$ = LLLL
   H if $Q_0 - Q_3 \neq$ LLLL
   ② = L if $Q_0 - Q_3$ = HHHH
   H if $Q_0 - Q_3 \neq$ HHHH
   * Before the clock, $\overline{TC}$ is Q_3; after the clock, $\overline{TC}$ is Q_2

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–170	–120	–60	mA	Inputs Open

6

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q_n}$	450	1300	450	1300	450	1300	ps
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	2000	600	2000	600	2000	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q_n}$	500	1500	500	1500	500	1500	ps
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	2000	600	2000	600	2000	ps
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	400	1300	400	1300	400	1300	ps
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	400	1500	400	1500	400	1500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_3	800	—	800	—	800	—	
	P_n	800	—	800	—	800	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	700	—	700	—	700	—	
	S_n	1000	—	1000	—	1000	—	
	MR (Release Time)	900	—	900	—	900	—	
t_h	Hold Time							ps
	D_3	200	—	200	—	200	—	
	P_n	200	—	200	—	200	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	200	—	200	—	200	—	
	S_n	–200	—	–200	—	–200	—	
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q_n}$	450	1200	450	1200	450	1200	ps
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	1900	600	1900	600	1900	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q_n}$	500	1400	500	1400	500	1400	ps
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	1900	600	1900	600	1900	ps
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	400	1200	400	1200	400	1200	ps
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	400	1500	400	1500	400	1500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_3	800	—	800	—	800	—	
	P_n	800	—	800	—	800	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	700	—	700	—	700	—	
	S_n	1000	—	1000	—	1000	—	
	MR (Release Time)	900	—	900	—	900	—	
t_h	Hold Time							ps
	D_3	200	—	200	—	200	—	
	P_n	200	—	200	—	200	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	200	—	200	—	200	—	
	S_n	–200	—	–200	—	–200	—	
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps

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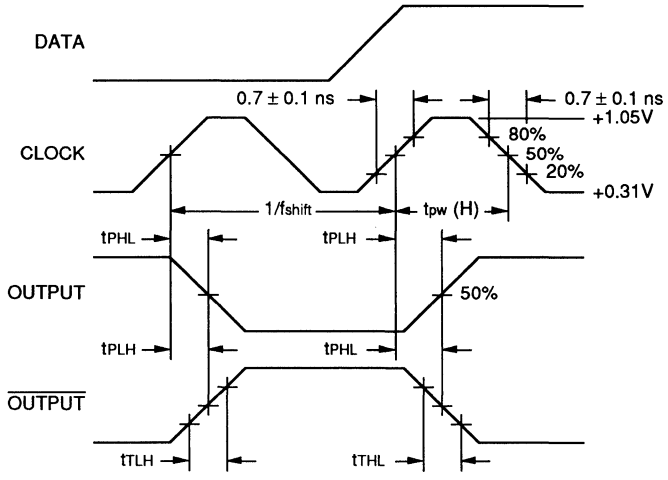
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

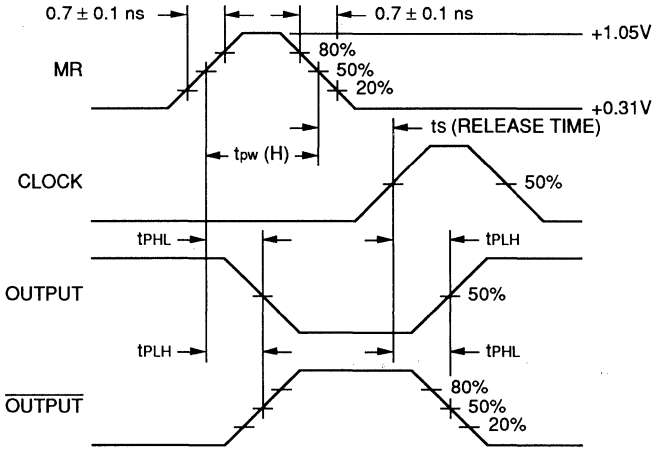
V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q_n}$	450	1100	450	1100	450	1100	ps
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	600	1800	600	1800	600	1800	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q_n}$	500	1300	500	1300	500	1300	ps
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	600	1800	600	1800	600	1800	ps
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	400	1100	400	1100	400	1100	ps
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	400	1500	400	1500	400	1500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_3	800	—	800	—	800	—	
	P_n	800	—	800	—	800	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	700	—	700	—	700	—	
	S_n	1000	—	1000	—	1000	—	
	MR (Release Time)	900	—	900	—	900	—	
t_h	Hold Time							ps
	D_3	200	—	200	—	200	—	
	P_n	200	—	200	—	200	—	
	$D_0/\overline{CET}$, $\overline{CEP}$	200	—	200	—	200	—	
	S_n	–200	—	–200	—	–200	—	
t_{pw} (H)	Pulse Width HIGH, CP, MR	—	800	—	800	—	800	ps

TIMING DIAGRAMS

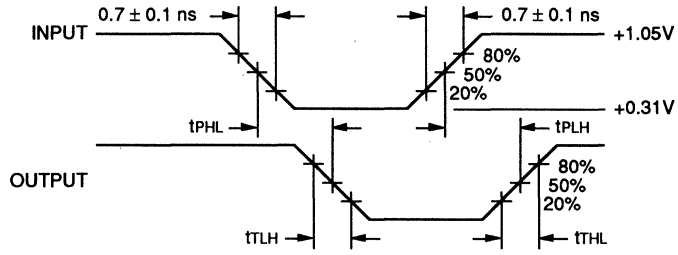


Propagation Delay (Clock) and Transition Times

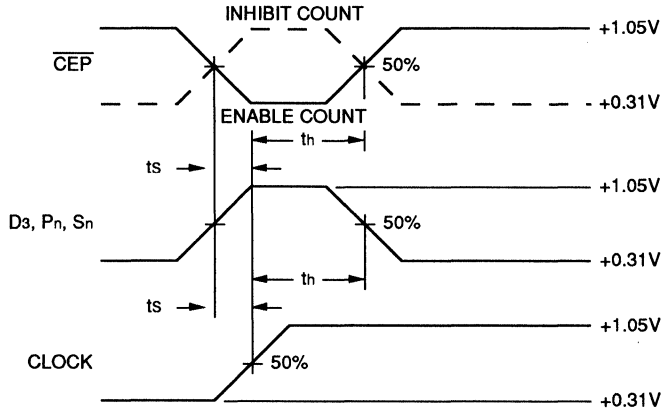


Propagation Delay (Reset)

TIMING DIAGRAMS (CONT'D.)



Propagation Delay (Serial Data, Selects)



Set-up and Hold Time

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S336ADC	D24-1	Commercial
SY100S336AFC	F24-1	Commercial
SY100S336AJC	J28-1	Commercial

FEATURES

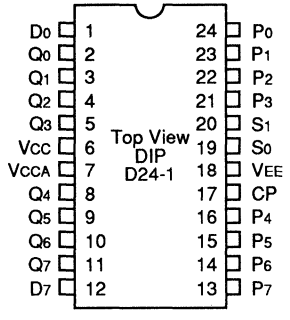
- **Max. shift frequency of 600MHz**
- **Max. Clock to Q delay of 1200ps**
- **IEE min. of –150mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **70% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

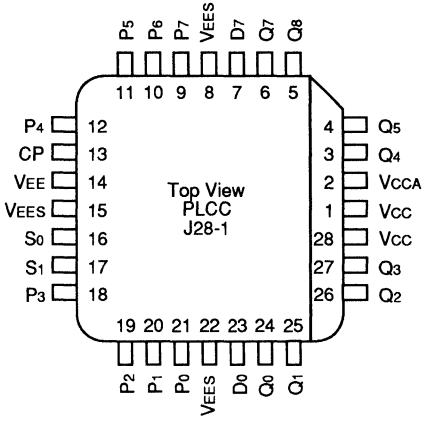
DESCRIPTION

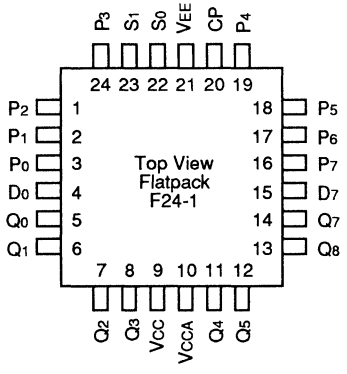
The SY100S341 offer eight D-type, edge-triggered flip-flops with both individual inputs for parallel operation as well as serial inputs for bidirectional shifting, and are designed for use in high-performance ECL systems. Data is clocked into the flip-flops on the rising edge of the clock.

The mode of operation is selected by two Select inputs (S_0, S_1) which determine if the device performs a shift, hold or parallel entry function, as described in the Truth Table. The inputs on these devices have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





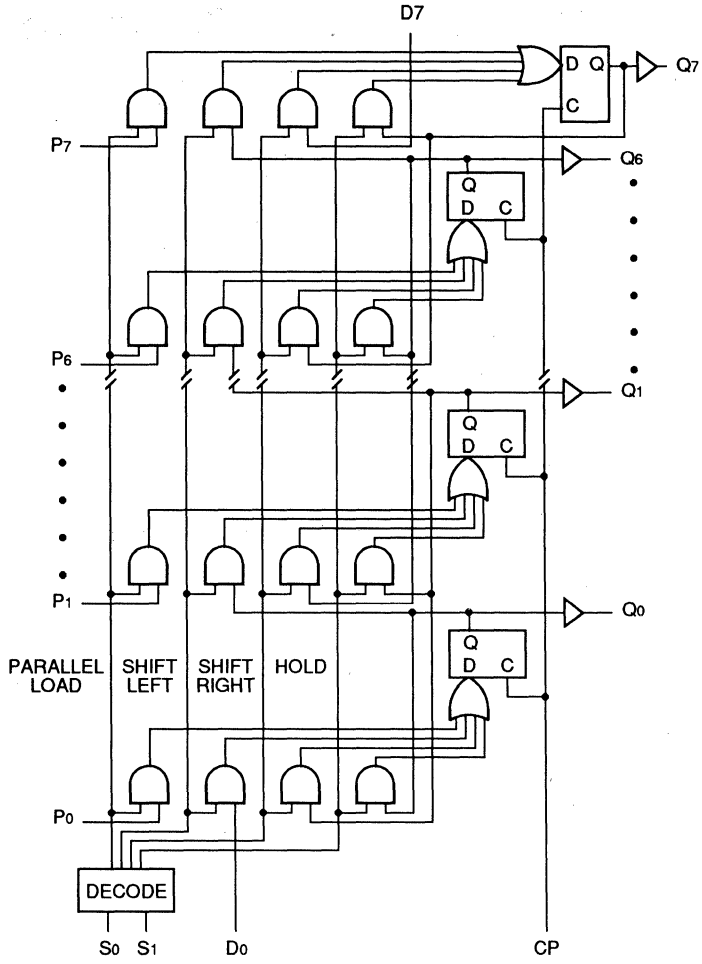


PIN NAMES

Label	Function
CP	Clock Pulse Input
S_0 — S_1	Select Inputs
D_0 — D_7	Serial Inputs
P_0 — P_7	Parallel Inputs
Q_0 — Q_7	Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↗	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↗	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↗	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↗ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–150	–102	–71	mA	Inputs Open

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AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Output	450	1200	450	1200	450	1200	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time							ps
	D_n, P_n	300	—	300	—	300	—	
	S_n	600	—	600	—	600	—	
t_h	Hold Time							ps
	D_n, P_n	300	—	300	—	300	—	
	S_n	0	—	0	—	0	—	
t_{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

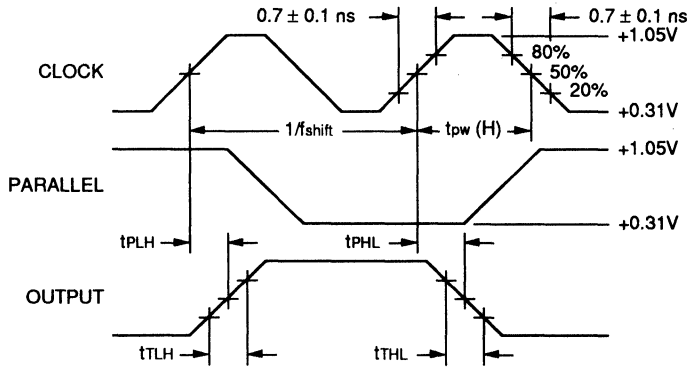
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Output	450	1100	450	1100	450	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_n, P_n S_n	 300 600	 — —	 300 600	 — —	 300 600	 — —	ps
t_h	Hold Time D_n, P_n S_n	 300 0	 — —	 300 0	 — —	 300 0	 — —	ps
t_{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps

PLCC

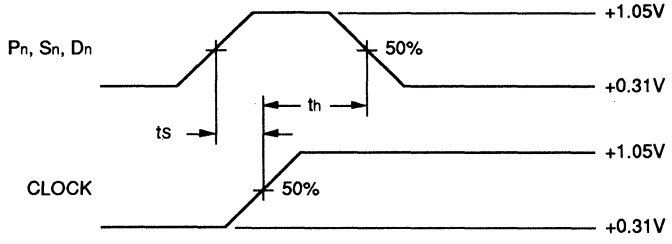
V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{shift}	Shift Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Output	450	1000	450	1000	450	1000	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_n, P_n S_n	 300 600	 — —	 300 600	 — —	 300 600	 — —	ps
t_h	Hold Time D_n, P_n S_n	 300 0	 — —	 300 0	 — —	 300 0	 — —	ps
t_{pw} (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps

TIMING DIAGRAMS



Propagation Delay and Transition Times



Set-up and Hold Times

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S341DC	D24-1	Commercial
SY100S341FC	F24-1	Commercial
SY100S341JC	J28-1	Commercial

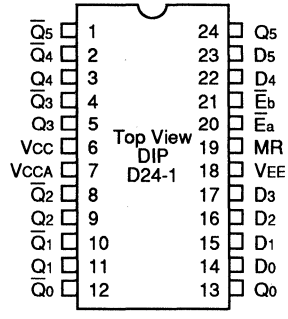
FEATURES

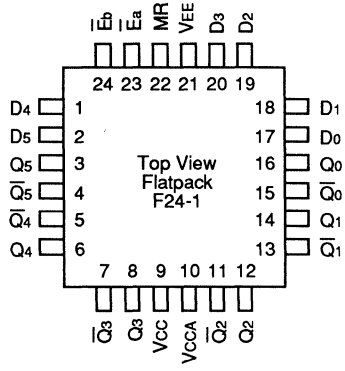
- **Max. transparent propagation delay of 900ps**
- **Min. Master Reset and Enable pulse widths of 100ps**
- **IEE min. of –98mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — VEE = –4.2V to 5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **More than 40% faster than National or Signetics**
- **Approximately 30% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

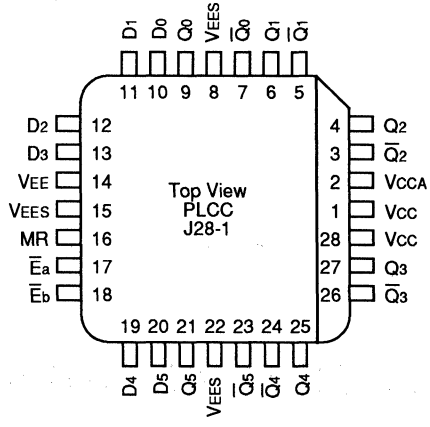
DESCRIPTION

The SY100S350 offers six high-speed D-Latches with both true and complement outputs, and is performance compatible for use with high-performance ECL systems. When both enable signals ($\overline{E}_a$ and $\overline{E}_b$) are at a logic LOW, the latches are transparent and the input signals(D_0–D_5) appear at the outputs (Q_0–Q_5) after a propagation delay. If either or both of the enable signals are at a logic HIGH, then the latches store the last valid data present on its inputs before $\overline{E}_a$ or $\overline{E}_b$ went to a logic HIGH. The Master Reset (MR) overrides all other input signals and takes the outputs to a logic LOW state. All inputs have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





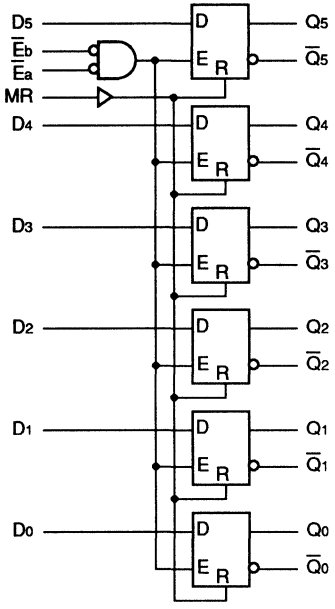


PIN NAMES

Label	Function
D_0 — D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0 — Q_5	Data Outputs
$\overline{Q}_0$ — $\overline{Q}_5$	Complementary Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Each Latch

Inputs				Outputs		
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n	$\overline{Q}_n$	Operating Mode
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched[2]	Latched[2]	
X	H	X	L	Latched[2]	Latched[2]	
X	X	X	H	L	H	Asynchronous

NOTES:

1. H = HIGH State
   L = LOW State
   X = Don't Care
2. Retains data that is present before $\overline{E}$ positive transition.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	MR	—	—	250		
	Dn	—	—	250		
	$\overline{E}_a$, $\overline{E}_b$	—	—	250		
I_{EE}	Power Supply Current	–98	–78	–49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	450	1050	450	1050	450	1050	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	450	1150	450	1150	450	1150	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	450	1250	450	1250	450	1250	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time, D_n to $\overline{E}_n$	600	—	600	—	600	—	ps
t_h	Hold Time, D_n to $\overline{E}_n$	600	—	600	—	600	—	ps
t_r	Release Time, MR to $\overline{E}_n$	1000	—	1000	—	1000	—	ps
t_{PW} (L)	Pulse Width, $\overline{E}_a$, $\overline{E}_b$	1000	—	1000	—	1000	—	ps
t_{PW} (H)	Pulse Width, MR	1100	—	1100	—	1100	—	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	300	1000	300	1000	300	1000	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	300	1100	300	1100	300	1100	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1250	300	1250	300	1250	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps
t_h	Hold Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps
t_r	Release Time, MR to $\overline{E}_n$	1000	—	1000	—	1000	—	ps
t_{PW} (L)	Pulse Width, $\overline{E}_a$, $\overline{E}_b$	1000	—	1000	—	1000	—	ps
t_{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps

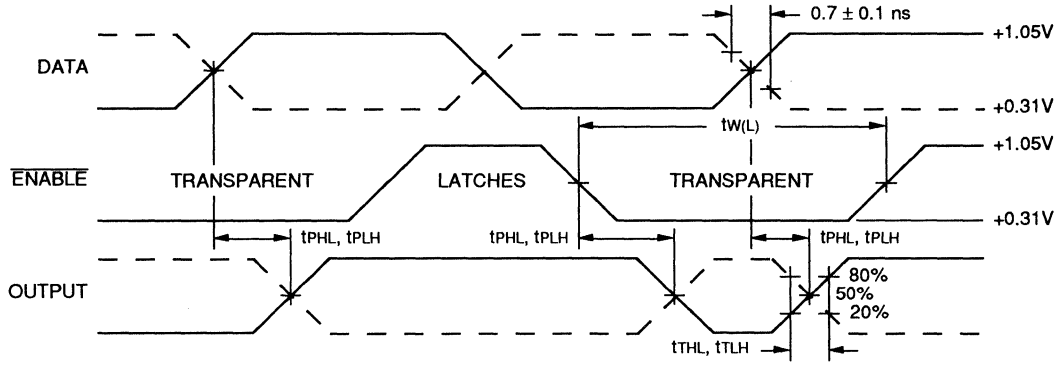
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

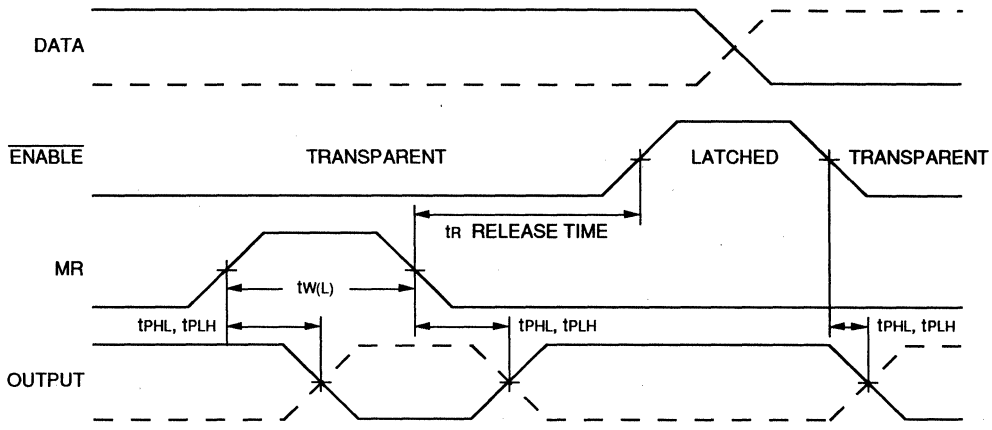
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay D_n to Output	300	900	300	900	300	900	ps
tPLH tPHL	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	300	1000	300	1000	300	1000	ps
tPLH tPHL	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
ts	Set-up Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps
th	Hold Time, D_n to $\overline{E}_n$	500	—	500	—	500	—	ps
tr	Release Time, MR to $\overline{E}_n$	1000	—	1000	—	1000	—	ps
tPW (L)	Pulse Width, $\overline{E}_a$, $\overline{E}_b$	1000	—	1000	—	1000	—	ps
tPW (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps

TIMING DIAGRAMS

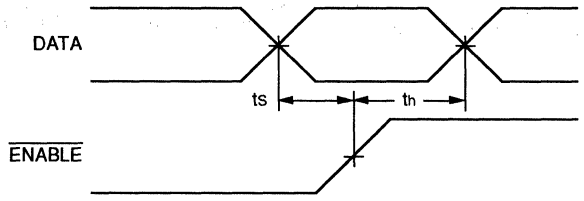


Enable Timing

TIMING DIAGRAMS



Reset Timing



Data Set-up and Hold Times

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S350DC	D24-1	Commercial
SY100S350FC	F24-1	Commercial
SY100S350JC	J28-1	Commercial

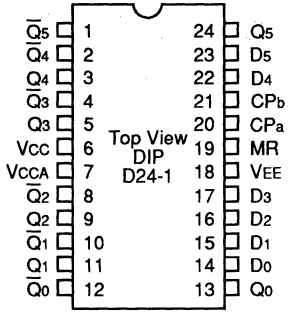
FEATURES

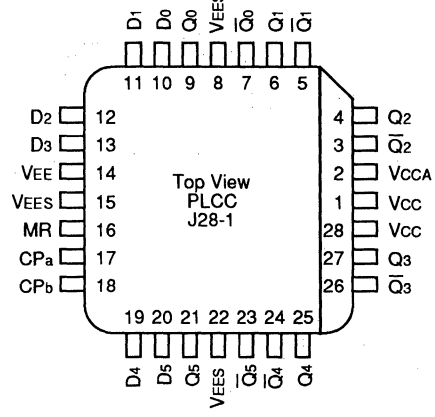
- **Max. toggle frequency of 700MHz**
- **Clock to Q max. of 1200ps**
- **IEE min. of –98mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — VEE = –4.2V to –5.46V
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **50% faster than National 300K**
- **Better than 20% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

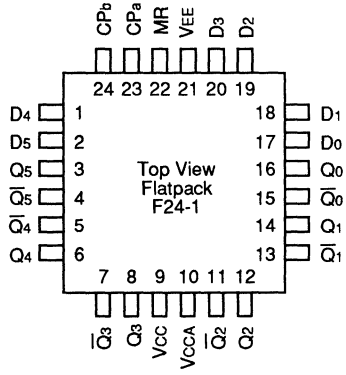
DESCRIPTION

The SY100S351 offers six D-type, edge-triggered, master/slave flip-flops with differential outputs, and is designed for use in high-performance ECL systems. The flip-flops are controlled by the signal from the logical OR operation on a pair of common Clock signals (CPa, CPb). Data enters the master when both CPa and CPb are LOW and transfers to the slave when either CPa or CPb (or both) go to a logic HIGH. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





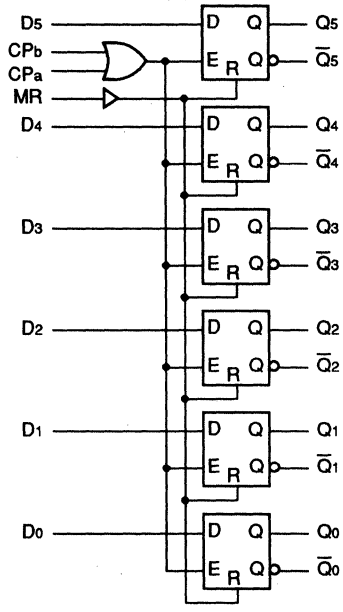


PIN NAMES

Label	Function
D0 — D5	Data Inputs
CPa, CPb	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q0 — Q5	Data Outputs
$\overline{Q0}$ — $\overline{Q5}$	Complementary Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLES

Asynchronous Operation[1]				
Inputs				Outputs
D_n	CP_a	CP_b	MR	Q_n (t+1)
X	X	X	H	L

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   t = Time before CP Positive Transition
   t+1 = Time after CP Positive Transition
   ∫ = LOW-to-HIGH Transition

Synchronous Operation[1]				
Inputs				Outputs
D_n	CP_a	CP_b	MR	Q_n (t+1)
L	∫	L	L	L
H	∫	L	L	H
L	L	∫	L	L
H	L	∫	L	H
X	H	∫	L	Q_n(t)
X	∫	H	L	Q_n(t)
X	L	L	L	Q_n(t)

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current MR D_0 – D_5 CP_a, CP_b	 — — —	 — — —	 270 200 300	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–98	–71	–49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{MAX}	Toggle Frequency	600	—	600	—	600	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	—	1400	—	1400	—	1400	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	—	1400	—	1400	—	1400	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_0–D_5 MR (Release Time)	 500 1000	 — —	 500 1000	 — —	 500 1000	 — —	ps
t_h	Hold Time, D_0–D_5	550	—	550	—	550	—	ps
t_{PW} (H)	Pulse Width HIGH CP_a, CP_b, MR	1000	—	1000	—	1000	—	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{MAX}	Toggle Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	—	1200	—	1200	—	1200	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_0–D_5 MR (Release Time)	 500 1000	 — —	 500 1000	 — —	 500 1000	 — —	ps
t_h	Hold Time, D_0–D_5	550	—	550	—	550	—	ps
t_{PW} (H)	Pulse Width HIGH CP_a, CP_b, MR	1000	—	1000	—	1000	—	ps

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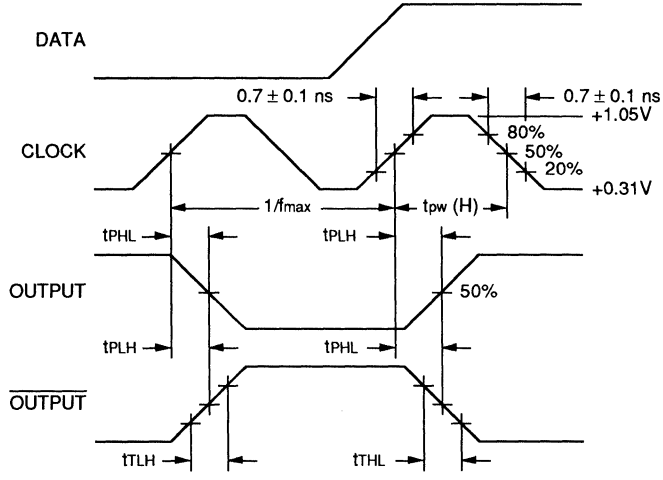
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

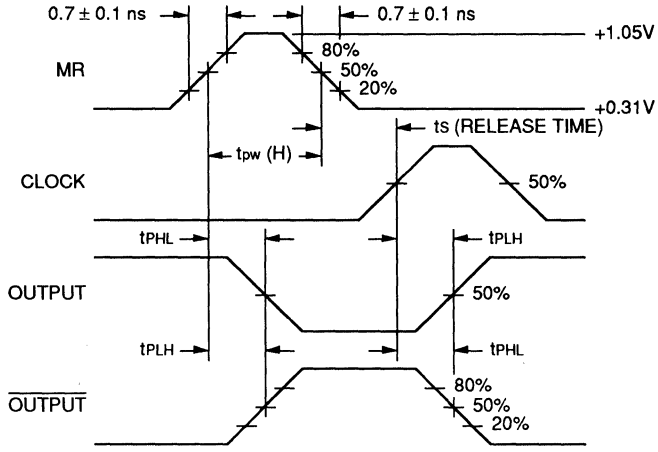
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Toggle Frequency	700	—	700	—	700	—	MHz
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	—	1200	—	1200	—	1200	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_0–D_5 MR (Release Time)	 500 1000	 — —	 500 1000	 — —	 500 1000	 — —	ps
t_h	Hold Time, D_0–D_5	550	—	550	—	550	—	ps
t_{PW} (H)	Pulse Width HIGH CP_a, CP_b, MR	1000	—	1000	—	1000	—	ps

TIMING DIAGRAMS

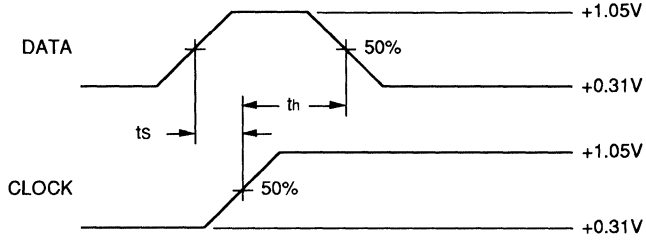


Propagation Delay (Clock) and Transition Times

TIMING DIAGRAMS (CONT'D.)



Propagation Delay (Resets)



Data Se-tup and Hold Time

NOTES:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S351DC	D24-1	Commercial
SY100S351FC	F24-1	Commercial
SY100S351JC	J28-1	Commercial

QUAD MULTIPLEXER/ LATCH

FEATURES

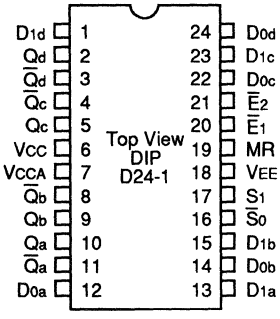
- **Max. propagation delay of 1100ps**
- **Max. enable to output delay of 1400ps**
- **IEE min. of –80mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  - **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **50% faster than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

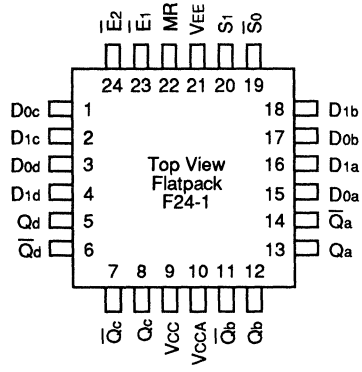
DESCRIPTION

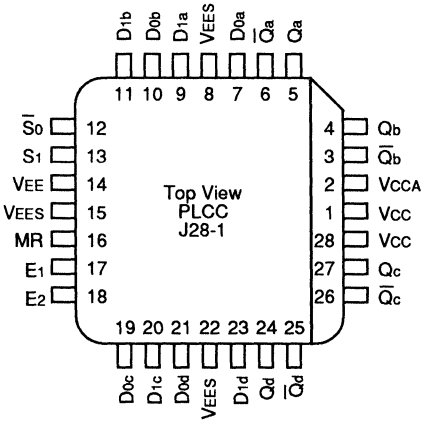
The SY100S355 offers four transparent latches with differential outputs and is designed for use in high-performance ECL systems. The Select inputs ($\overline{S}_0$, S_1) select one of the two sources of input data (D_0 or D_1) to the latch. The Select inputs can also force the outputs to a logic LOW when the latch is in the transparent mode. The latches are in the transparent mode when both Enables ($\overline{E}_1$, $\overline{E}_2$) are at a logic LOW state. In the transparent mode, the Select inputs can pass an input logic HIGH from D_0 or D_1 to the output.

If the Select inputs are tied together, then input data from either D_0 or D_1 is always passed through. A rising edge on either Enable input will latch the outputs with the most recent data at the latch inputs being stored. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





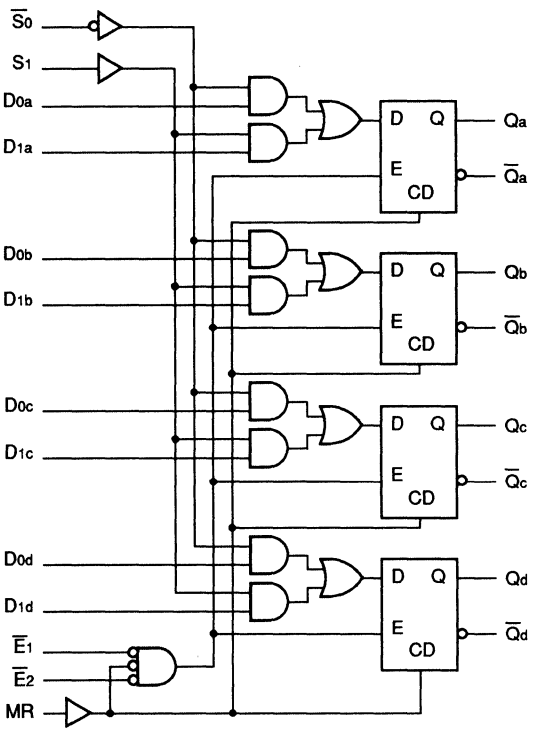


PIN NAMES

Label	Function
$\overline{E}_1 - \overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
$D_{na} - D_{nd}$	Data Inputs
$Q_a - Q_d$	Data Outputs
$\overline{Q}_a - \overline{Q}_d$	Complementary Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs							Outputs	
MR	Ē1	Ē2	S1	S̄o	D1X	D0X	Q̄X	QX
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched	
L	X	H	X	X	X	X	Latched	

NOTE:
1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care

DC ELECTRICAL CHARACTERISTICS

VEE = –4.2V to –5.46V unless otherwise specified; VCC = VCCA = GND, TA = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
IIH	Input HIGH Current				µA	VIN = VIH (Max.)
	S̄o, S1	—	—	220		
	Ē1, Ē2	—	—	350		
	Dna, Dnd	—	—	340		
	MR	—	—	430		
IEE	Power Supply Current	–80	–57	–40	mA	Inputs Open

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AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_{na} – D_{nd} to Output (Transparent Mode)	400	1300	400	1300	400	1300	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	400	1600	400	1600	400	1600	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	300	1200	300	1200	300	1200	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1600	300	1600	300	1600	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_{na} – D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 700 1200 1000	 — — —	 700 1200 1000	 — — —	 700 1200 1000	 — — —	ps
t_h	Hold Time D_{na} – D_{nd} $\overline{S}_0$, S_1	 400 400	 — —	 400 400	 — —	 400 400	 — —	ps
t_{PW} (L)	Pulse Width LOW, $\overline{E}_1$, $\overline{E}_2$	1000	—	1000	—	1000	—	ps
t_{PW} (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_{na} – D_{nd} to Output (Transparent Mode)	300	1200	300	1200	300	1200	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	300	1500	300	1500	300	1500	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	300	1500	300	1500	300	1500	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_{na} – D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 700 1200 1000	 — — —	 700 1200 1000	 — — —	 700 1200 1000	 — — —	ps
t_h	Hold Time D_{na} – D_{nd} $\overline{S}_0$, S_1	 400 400	 — —	 400 400	 — —	 400 400	 — —	ps
t_{PW} (L)	Pulse Width LOW, $\overline{E}_1$, $\overline{E}_2$	1000	—	1000	—	1000	—	ps
t_{PW} (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps

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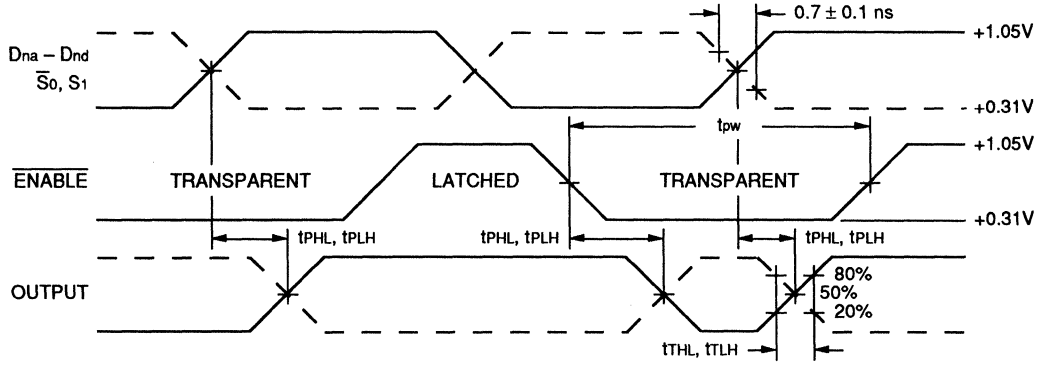
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

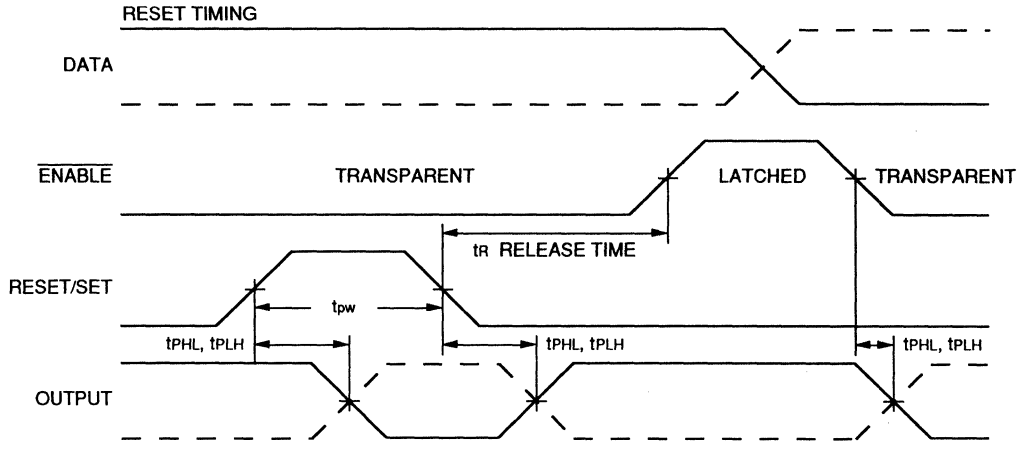
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_{na} – D_{nd} to Output (Transparent Mode)	300	1100	300	1100	300	1100	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	300	1400	300	1400	300	1400	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	300	1400	300	1400	300	1400	ps
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1100	300	1100	300	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps
t_s	Set-up Time D_{na} – D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 700 1200 1000	 — — —	 700 1200 1000	 — — —	 700 1200 1000	 — — —	ps
t_h	Hold Time D_{na} – D_{nd} $\overline{S}_0$, S_1	 300 300	 — —	 300 300	 — —	 300 300	 — —	ps
t_{PW} (L)	Pulse Width LOW, $\overline{E}_1$, $\overline{E}_2$	1000	—	1000	—	1000	—	ps
t_{PW} (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps

TIMING DIAGRAMS

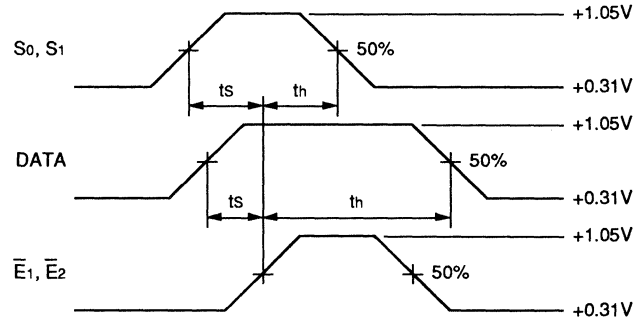


Enable Timing

TIMING DIAGRAMS (CONT'D.)



Reset Timing



Data Set-up and Hold Times

NOTES:

ts is the minimum time before the transition of the clock that information must be present at the data input.

th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S355DC	D24-1	Commercial
SY100S355FC	F24-1	Commercial
SY100S355JC	J28-1	Commercial

DUAL PARITY CHECKER/GENERATOR

FEATURES

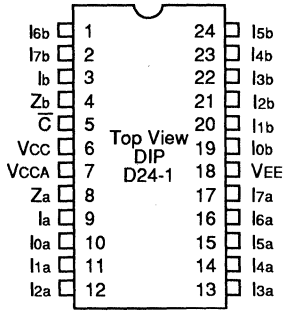
- **Max. propagation delay of 2200ps**
- **IEE min. of –70mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **15% faster than National 300K**
- **Approximately 30% lower power than National 300K**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

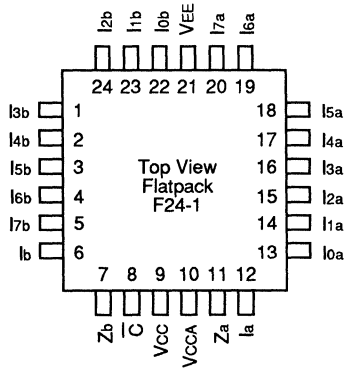
DESCRIPTION

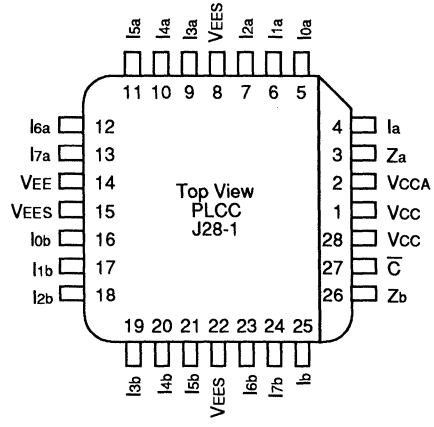
The SY100S360 is a dual parity checker/generator and is designed for use in high-performance ECL systems. The inputs are segmented into two groups of nine inputs each and the parity output is at a logic LOW when an even number of inputs are at a logic HIGH. In each group, one of the nine inputs (Ia, Ib) has a shorter propagation delay and, therefore, is ideal as the expansion input for parity generation of wider data.

A Compare output ($\overline{C}$) is also provided which allows comparison of two 8-bit words. A logic LOW on the $\overline{C}$ output indicates a match. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





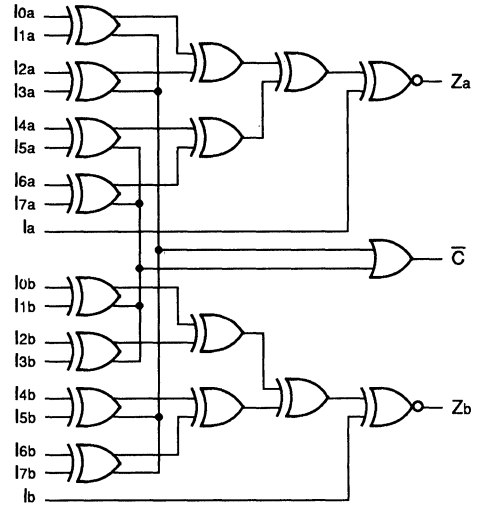


PIN NAMES

Label	Function
Ia, Ib, Ina, Inb	Data Inputs (n = 1...7)
Za – Zb	Parity Odd Outputs
$\overline{C}$	Compare Output

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Sum of High Inputs	Output Z
Even	HIGH
Odd	LOW

NOTE:

1. Comparator Function:
$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) +$
$(I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current Ia, Ib Ina, Inb	 — —	 — —	 300 200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–70	–45	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ina, Inb to Za, Zb	500	2400	500	2400	500	2400	ps
t_{PLH} t_{PHL}	Propagation Delay Ina, Inb to $\overline{C}$	500	1900	500	1900	500	1900	ps
t_{PLH} t_{PHL}	Propagation Delay Ia, Ib to Za, Zb	300	1100	300	1100	300	1100	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

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AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

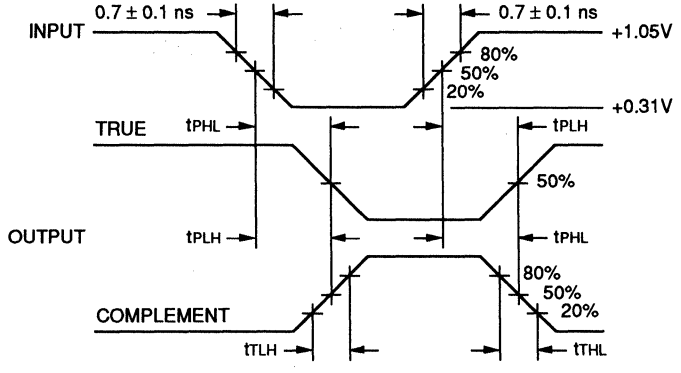
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Ina, Inb to Za, Zb	500	2300	500	2300	500	2300	ps
tPLH tPHL	Propagation Delay Ina, Inb to $\overline{C}$	500	1800	500	1800	500	1800	ps
tPLH tPHL	Propagation Delay Ia, Ib to Za, Zb	300	1000	300	1000	300	1000	ps
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Ina, Inb to Za, Zb	500	2200	500	2200	500	2200	ps
tPLH tPHL	Propagation Delay Ina, Inb to $\overline{C}$	500	1700	500	1700	500	1700	ps
tPLH tPHL	Propagation Delay Ia, Ib to Za, Zb	300	900	300	900	300	900	ps
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S360DC	D24-1	Commercial
SY100S360FC	F24-1	Commercial
SY100S360JC	J28-1	Commercial

DUAL 8-INPUT MULTIPLEXER

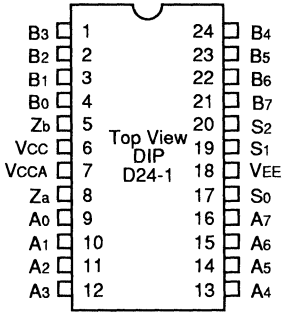
FEATURES

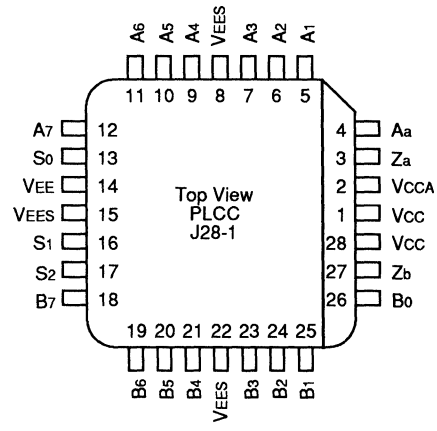
- **Max. propagation delay of 900ps**
- **I_{EE} min. of –92mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **V_{EE} = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **60% faster than National 300K at lower power**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

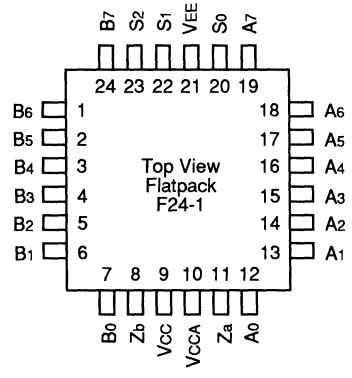
DESCRIPTION

The SY100S363 is a dual 8-input multiplexer designed for use in new, high-performance ECL systems. The three Data Select inputs (S_0, S_1, S_2) determine the bits from each of the inputs (A_n, B_n) that will be passed on through the two outputs. The same bit will be selected from the two groups of 8 inputs. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





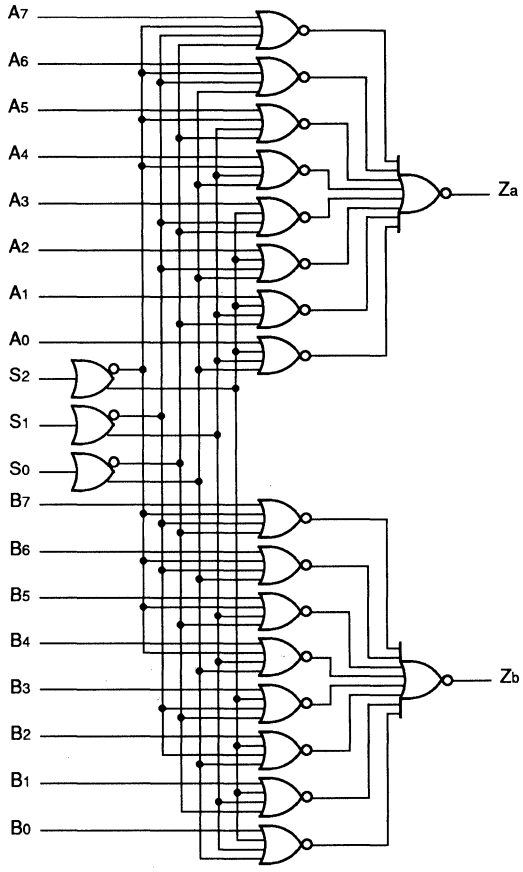


PIN NAMES

Label	Function
$S_0 – S_2$	Data Select Inputs
$A_0 – A_7$	A Data Inputs
$B_0 – B_7$	B Data Inputs
Z_a, Z_b	Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs											Outputs
Select			Data								
S_2	S_1	S_0	A_7/B_7	A_6/B_6	A_5/B_5	A_4/B_4	A_3/B_3	A_2/B_2	A_1/B_1	A_0/B_0	Z_a/Z_b
L	L	L								L	L
L	L	L								H	H
L	L	H							L		L
L	L	H							H		H
L	H	L						L			L
L	H	L						H			H
L	H	H					L				L
L	H	H					H				H
H	L	L				L					L
H	L	L				H					H
H	L	H			L						L
H	L	H			H						H
H	H	L		L							L
H	H	L		H							H
H	H	H	L								L
H	H	H	H								H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Blank = X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	S_n	—	—	200		
	A_n, B_n	—	—	200		
I_{EE}	Power Supply Current	–92	–66	–45	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay A_0 – A_7, B_0 – B_7 to Output	300	1100	300	1100	300	1100	ps
t_{PLH} t_{PHL}	Propagation Delay S_0 – S_2 to Output	400	1500	400	1500	400	1500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay A_0 – A_7, B_0 – B_7 to Output	300	1000	300	1000	300	1000	ps
t_{PLH} t_{PHL}	Propagation Delay S_0 – S_2 to Output	400	1400	400	1400	400	1400	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	1000	300	1000	300	1000	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay A_0 – A_7, B_0 – B_7 to Output	300	900	300	900	300	900	ps
t_{PLH} t_{PHL}	Propagation Delay S_0 – S_2 to Output	400	1300	400	1300	400	1300	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

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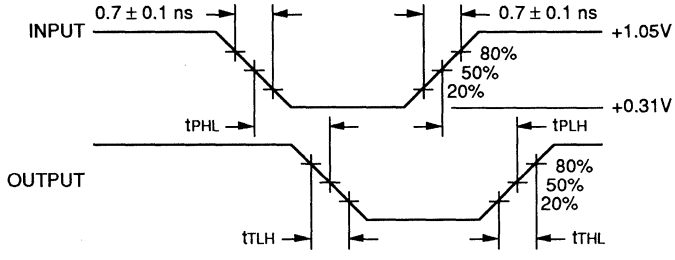
TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S363DC	D24-1	Commercial
SY100S363FC	F24-1	Commercial
SY100S363JC	J28-1	Commercial

16-INPUT MULTIPLEXER

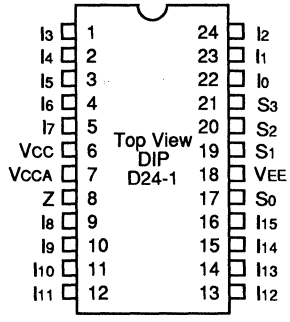
FEATURES

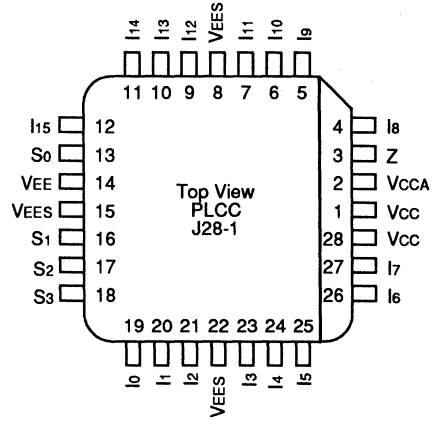
- **Max. propagation delay of 1300ps**
- **IEE min. of –63mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **70% faster than National or Signetics**
- **40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

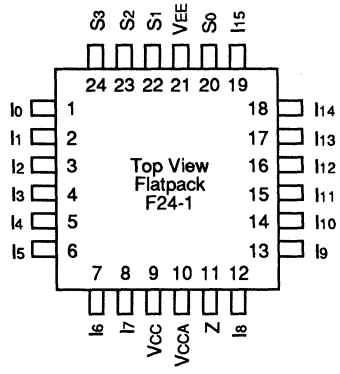
DESCRIPTION

The SY100S364 is a 16-input multiplexer designed for use in high-performance ECL systems. The four Data Select inputs (S_0, S_1, S_2, S_3) determine the bit from the 16 inputs (I_n) that will be passed on to the output as shown in the Truth Table. The output data polarity is the same as the input. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





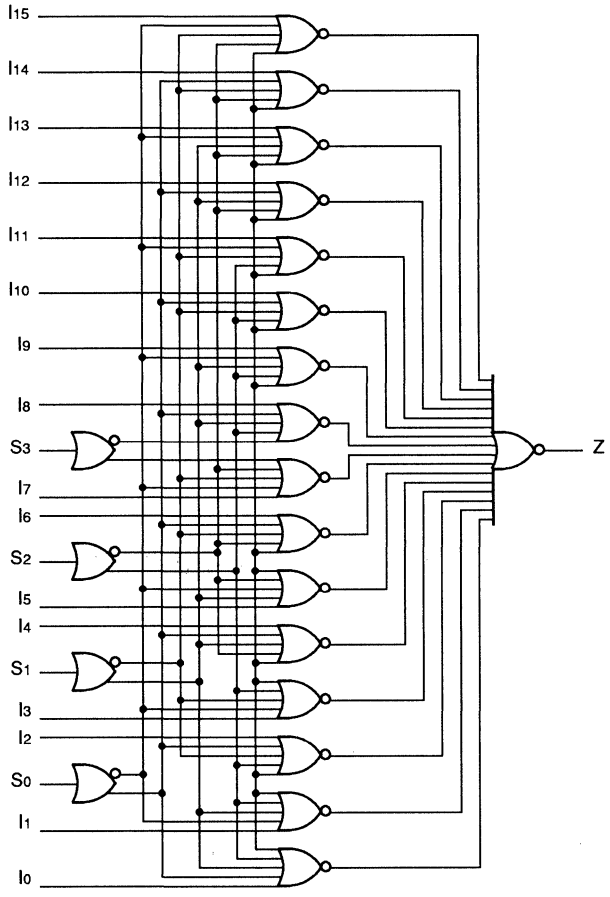


PIN NAMES

Label	Function
$I_0 - I_{15}$	Data Inputs
$S_0 - S_3$	Select Inputs
Z	Data Output

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	I_n	—	—	200		
	S_0, S_1	—	—	200		
	S_2, S_3	—	—	200		
I_{EE}	Power Supply Current	–63	–45	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_0 – I_{15} to Output	400	1500	400	1500	400	1500	ps
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1900	400	1900	400	1900	ps
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	400	1700	400	1700	400	1700	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

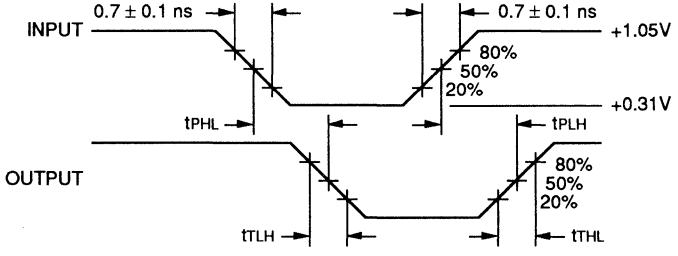
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_0 – I_{15} to Output	400	1400	400	1400	400	1400	ps
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1900	400	1900	400	1900	ps
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	400	1700	400	1700	400	1700	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_0 – I_{15} to Output	400	1300	400	1300	400	1300	ps
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1800	400	1800	400	1800	ps
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	400	1600	400	1600	400	1600	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S364DC	D24-1	Commercial
SY100S364FC	F24-1	Commercial
SY100S364JC	J28-1	Commercial

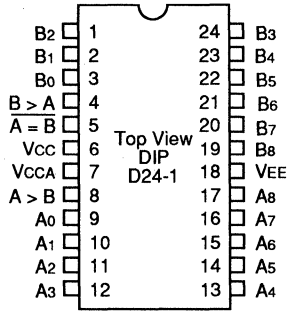
FEATURES

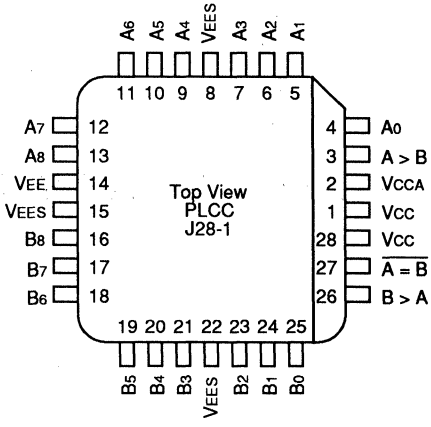
- **Max. propagation delay of 1500ps**
- **IEE min. of –120mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **120% faster than National or Signetics**
- **Approximately 40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

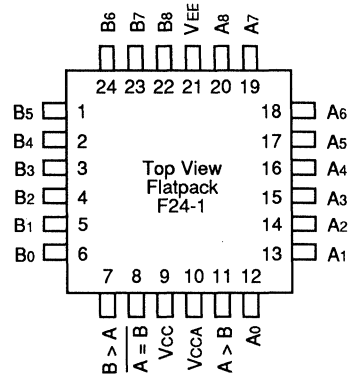
DESCRIPTION

The SY100S366 is an ultra-fast 9-bit magnitude comparator designed for use in high-performance ECL systems. The device compares the arithmetic value of two 9-bit words and indicates whether one word is greater than or equal to the other. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





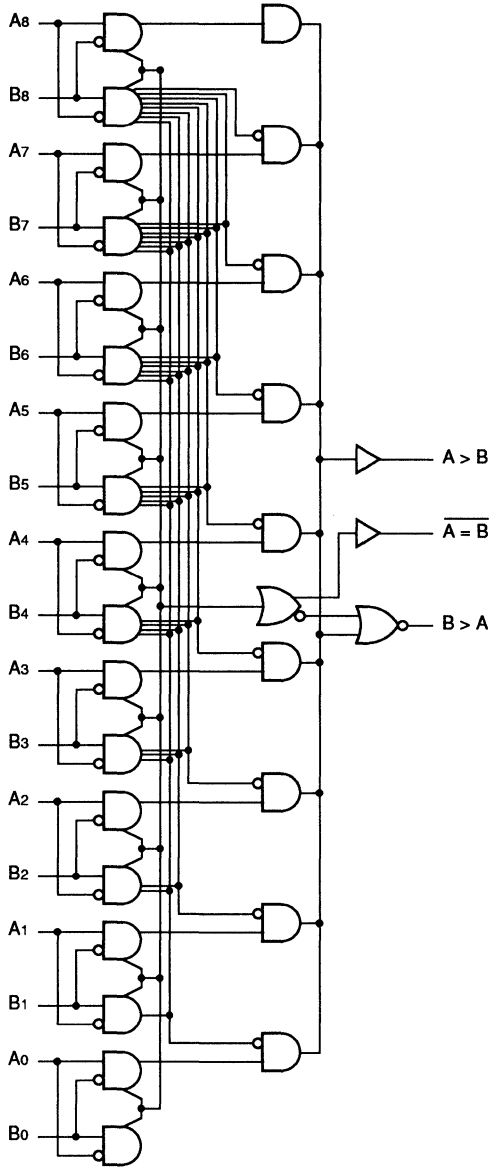


PIN NAMES

Label	Function
$A_0 - A_8$	A Data Inputs
$B_0 - B_8$	B Data Inputs
A > B	A Greater Than B Output
B > A	B Greater Than A Output
$\overline{A = B}$	Complement A Equal to B Output (Active LOW)

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs									Outputs		
A_8B_8	A_7B_7	A_6B_6	A_5B_5	A_4B_4	A_3B_3	A_2B_2	A_1B_1	A_0B_0	A > B	B > A	$\overline{A = B}$
H L									H	L	H
L H									L	H	H
$A_8 = B_8$	H L								H	L	H
$A_8 = B_8$	L H								L	H	H
$A_8 = B_8$	$A_7 = B_7$	H L							H	L	H
$A_8 = B_8$	$A_7 = B_7$	L H							L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	H L						H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	L H						L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	H L					H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	L H					L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	H L				H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	L H				L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	H L			H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	L H			L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	H L		H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	L H		L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	H L	H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	L H	L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	H

NOTE:

1. H = HIGH Voltage Level, L = LOW Voltage Level, Blank = X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	$V_{IN} = V_{IH}$ (Max.)
I_{EE}	Power Supply Current	–120	–86	–60	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; $V_{CC} = V_{CCA}$ = GND, T_A = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1700	400	1700	400	1700	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

AC ELECTRICAL CHARACTERISTICS (CONT'D.)

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

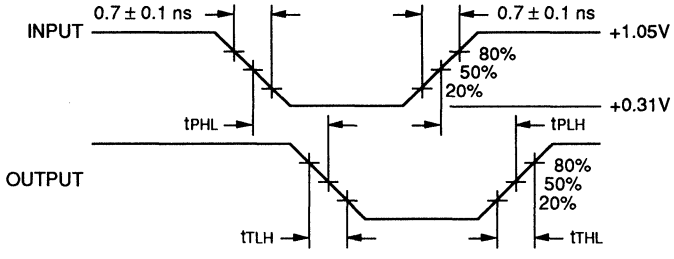
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1600	400	1600	400	1600	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = 85°C		Unit
		Min.	Max.	Min.	Max.	Min.	+Max.	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1500	400	1500	400	1500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S366DC	D24-1	Commercial
SY100S366FC	F24-1	Commercial
SY100S366JC	J28-1	Commercial

UNIVERSAL DEMULTIPLEXER/DECODER

FEATURES

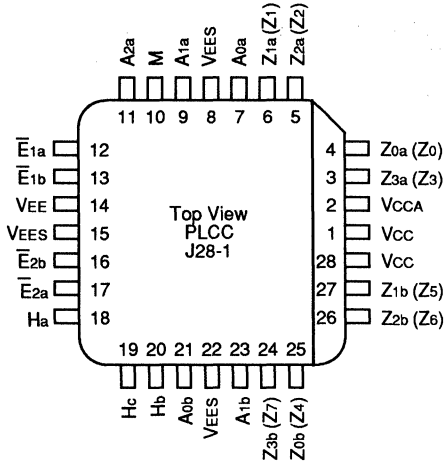
- **Max. propagation delay of 1200ps**
- **IEE min. of –92mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **60% faster than National or Signetics**
- **Approximately 40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

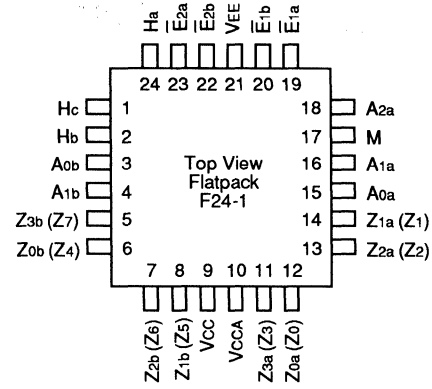
DESCRIPTION

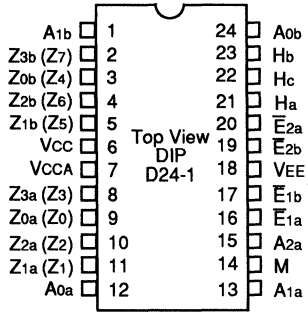
The SY100S370 is a universal demultiplexer/decoder that can be used as either a dual 1-of-4 decoder or as a single 1-of-8 decoder and is designed for use in high-performance ECL systems. The Mode control (M) input determines the function. In the dual 1-of-4 mode, each 4-input group has a pair of active-LOW Enable ($\overline{E}$) inputs. The Enable pins are assigned such that in the single 1-of-8 mode they can be tied together in pairs to result in two active-LOW Enable inputs. $\overline{E}_{1a}$ will be tied to $\overline{E}_{1b}$ and $\overline{E}_{2a}$ to $\overline{E}_{2b}$.

The auxiliary inputs (H_n) are used to determine whether the outputs are active-HIGH or active-LOW. The address inputs for the dual 1-of-4 mode are A_{0a}, A_{1a}, A_{0b}. A_{2a} is unused. In the 1-of-8 mode, the address inputs are A_{0a}, A_{1a}, A_{2a}. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





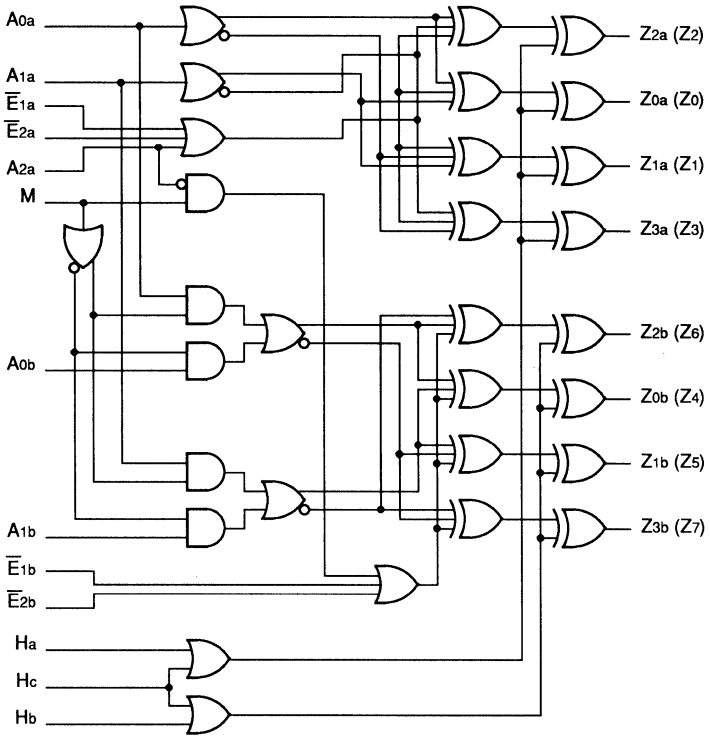


PIN NAMES

Label	Function
Ana, Anb	Address Inputs (n = 0,1,2)
$\overline{E}$na, $\overline{E}$nb	Enable Inputs (n = 1,2)
M	Mode Control Input
Ha	$Z_0 - Z_3$ ($\overline{Z}_{0a} - \overline{Z}_{3a}$) Polarity Select Input
Hb	$Z_4 - Z_7$ ($\overline{Z}_{0b} - \overline{Z}_{3b}$) Polarity Select Input
Hc	Common Polarity Select Input
$Z_0 - Z_7$	Single 1-of-8 Data Outputs
Zna, Znb	Dual 1-of-4 Data Outputs (n = 1...4)

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



6

TRUTH TABLES[1]

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)											
Inputs				Active HIGH Outputs (H_a and H_b Inputs HIGH)				Active LOW Outputs (H_a and H_b Inputs LOW)			
$\overline{E}_{1a}$,$\overline{E}_{1b}$	$\overline{E}_{2a}$,$\overline{E}_{2b}$	A_{1a},A_{1b}	A_{0a},A_{0b}	Z_{0a},Z_{0b}	Z_{1a},Z_{1b}	Z_{2a},Z_{2b}	Z_{3a},Z_{3b}	Z_{0a},Z_{0b}	Z_{1a},Z_{1b}	Z_{2a},Z_{2b}	Z_{3a},Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW)													
Inputs					Active HIGH Outputs* (H_c Input HIGH)								
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   * for H_c = LOW, output states are complemented
   $\overline{E}_1$ = $\overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2$ = $\overline{E}_{2a}$ and $\overline{E}_{2b}$ wired

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	Hc, A0a, A1a, A2a	—	—	310		
	All Others	—	—	250		
I_{EE}	Power Supply Current	–92	–73	–46	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	300	1400	300	1400	300	1400	ps
tPLH tPHL	Propagation Delay A_{na}, A_{nb} to Output	500	1700	500	1700	500	1700	ps
tPLH tPHL	Propagation Delay H_a, H_b, H_c to Output	500	1700	500	1700	500	1700	ps
tPLH tPHL	Propagation Delay M to Output	600	2200	600	2200	600	2200	ps
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

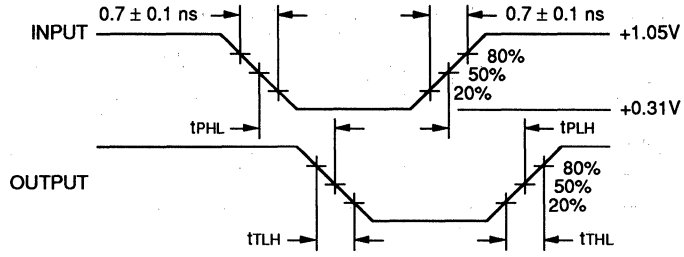
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	300	1300	300	1300	300	1300	ps
tPLH tPHL	Propagation Delay A_{na}, A_{nb} to Output	500	1600	500	1600	500	1600	ps
tPLH tPHL	Propagation Delay H_a, H_b, H_c to Output	500	1600	500	1600	500	1600	ps
tPLH tPHL	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	300	1200	300	1200	300	1200	ps
tPLH tPHL	Propagation Delay A_{na}, A_{nb} to Output	500	1500	500	1500	500	1500	ps
tPLH tPHL	Propagation Delay H_a, H_b, H_c to Output	500	1500	500	1500	500	1500	ps
tPLH tPHL	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S370DC	D24-1	Commercial
SY100S370FC	F24-1	Commercial
SY100S370JC	J28-1	Commercial

TRIPLE 4-INPUT MULTIPLEXER WITH ENABLE

SY100S371

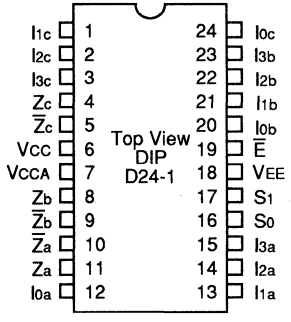
FEATURES

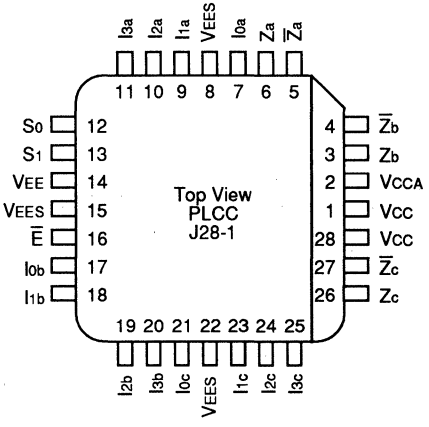
- **Max. propagation delay of 1000ps**
- **IEE min. of –68mA**
- **ESD protection of 2000V**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **40% faster than National or Signetics**
- **40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

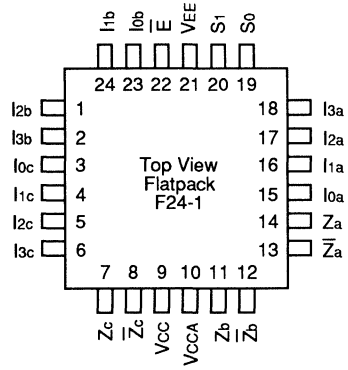
DESCRIPTION

The SY100S371 is an ultra-fast triple 4-input multiplexer with true and complementary outputs designed for use in high-performance ECL systems. The multiplexer is controlled by common select inputs So and S1. A logic HIGH on the Enable ($\overline{E}$) control input takes the outputs to a logic LOW. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS





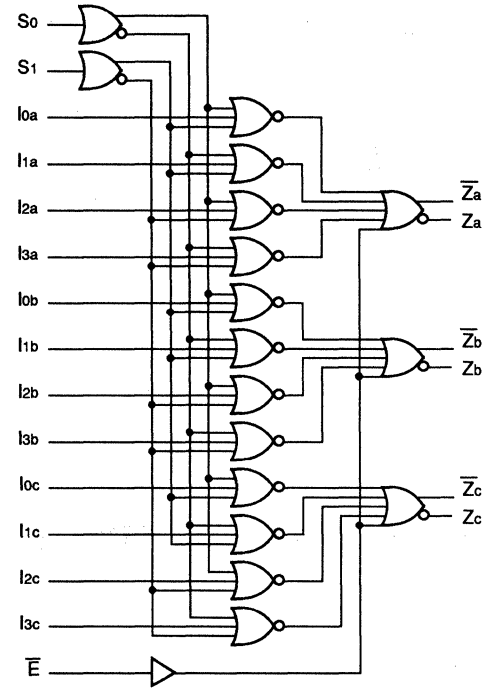


PIN NAMES

Label	Function
I0x – I3x	Data Inputs (x = a, b or c)
So, S1	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Za – Zc	Data Outputs
$\overline{Z}$a – $\overline{Z}$c	Complementary Data Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs			Outputs
$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0X}
L	H	L	I_{1X}
L	L	H	I_{2X}
L	H	H	I_{3X}
H	X	X	L

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	I_{0X} – I_{3X}	—	—	250		
	S_0, S_1, $\overline{E}$	—	—	300		
I_{EE}	Power Supply Current	–68	–48	–34	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_{0X} – I_{3X} to Output	300	1200	300	1200	300	1200	ps
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1600	400	1600	400	1600	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	400	1500	400	1500	400	1500	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

CERPACK

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

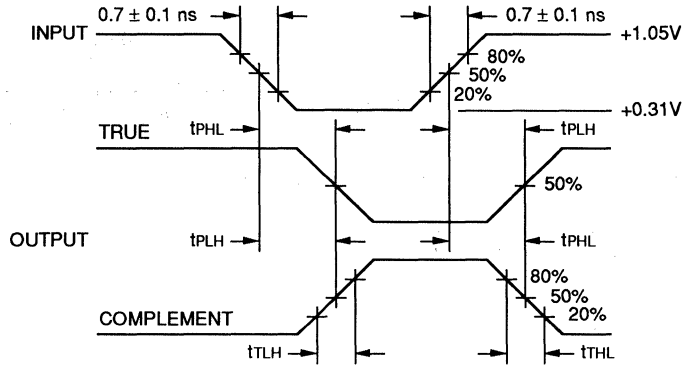
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_{0X} – I_{3X} to Output	300	1100	300	1100	300	1100	ps
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1500	400	1500	400	1500	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	400	1400	400	1400	400	1400	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

PLCC

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND, T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay I_{0X} – I_{3X} to Output	300	1000	300	1000	300	1000	ps
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	400	1400	400	1400	400	1400	ps
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	400	1300	400	1300	400	1300	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S371DC	D24-1	Commercial
SY100S371FC	F24-1	Commercial
SY100S371JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

LOW-POWER HEX PECL-TO-TTL TRANSLATOR

PRELIMINARY
SY100S390

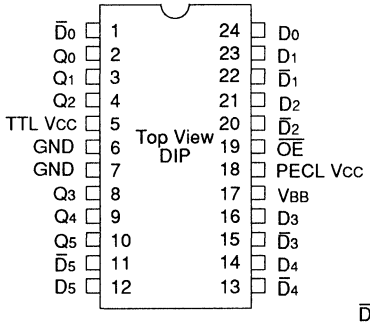
FEATURES

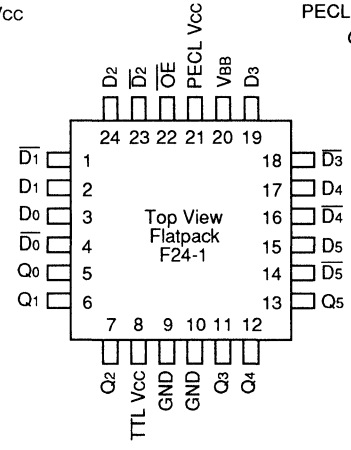
- **Operates from a single +5V supply**
- **Three-state outputs**
- **ESD protection of 2000V**
- **VBB output for single-ended use**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

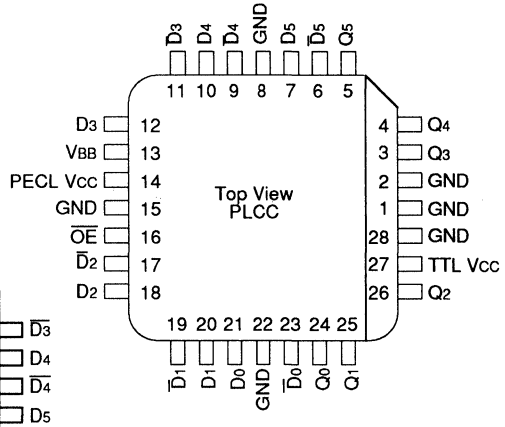
DESCRIPTION

The SY100S390 is a hex PECL-to-TTL translator for converting 100K logic levels to TTL logic levels. Unlike other level translators, the SY100S390 operates using only one +5V supply. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference generator provides VBB for single-ended operation. The standard three-state outputs are enabled by a common active low TTL compatible $\overline{OE}$ input. Partitioned Vccs on chip are brought out on separate power pins, allowing the noisy TTL Vcc power plane to be isolated from the relatively quiet ECL Vcc. The SY100S390 is ideal for applications limited to a single +5V supply, allowing for easy PECL-to-TTL interfacing.

PIN CONFIGURATIONS



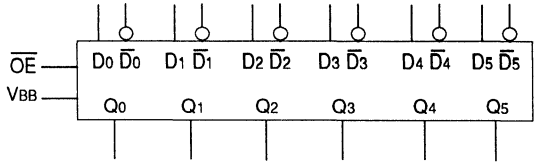




PIN NAMES

Label	Function
D0 — D5	Data Inputs (PECL)
$\overline{D0}$ — $\overline{D5}$	Inverting Data Inputs (PECL)
Q0 — Q5	Data Outputs (TTL)
$\overline{OE}$	Output Enable (TTL)
VBB	Reference Voltage (PECL)

LOGIC SYMBOL



Rev.: B Amendment: /0
Issue Date: April, 1994

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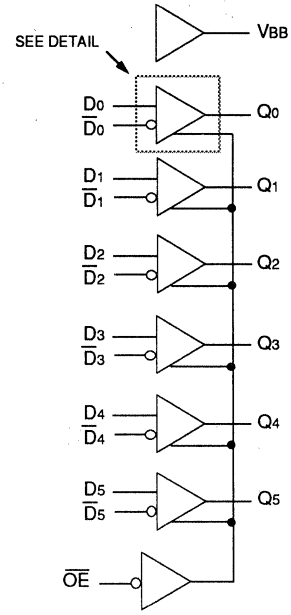
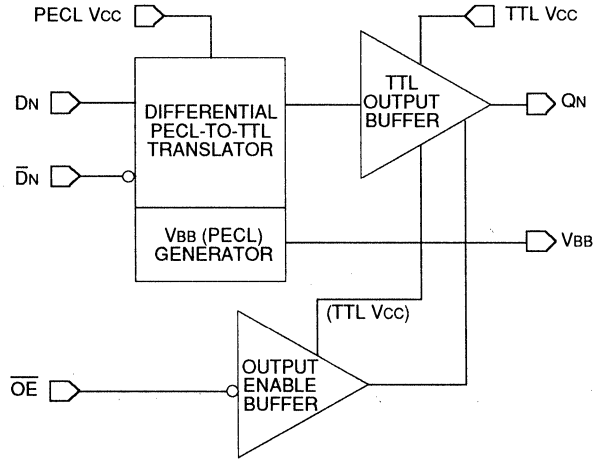
BLOCK DIAGRAM



BLOCK DIAGRAM DETAIL



TRUTH TABLE

Data Inputs (PECL)		Control Input (TTL)	TTL Outputs	Comments
Dn	$\overline{Dn}$	$\overline{OE}$	Qn	
X	X	H	Z	Outputs Disabled
L	H	L	L	Differential Operation
H	L	L	H	Differential Operation
L	L	L	U	Invalid Input States
H	H	L	U	Invalid Input States
Open	Open	L	U	Invalid Input States
L	V_{BB}	L	L	Single Ended Operation
H	V_{BB}	L	H	Single Ended Operation
V_{BB}	L	L	H	Single Ended Operation
V_{BB}	H	L	L	Single Ended Operation
V_{BB}	Open	L	H	Single Ended Operation
Open	V_{BB}	L	L	Single Ended Operation

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   U = Undefined

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operating Temperature	T_A	0 to +85	°C
Supply Voltage	V_{CC}	+4.75 to +5.25	V

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Storage Temperture	T_{STG}	–65 to +150	°C
Max. Junction Temp. Ceramic Plastic	T_J	 +175 +150	 °C °C
V_{CC} Pin Potential to Ground Pin	—	–0.5 to +7.0	V
TTL Input Voltage[2]	—	–0.5 to V_{CC}	V
TTL Input Current[2]	—	–30 to +5.0	mA
V_{BB} Output Current	—	–5.0 to +1.0	mA
PECL Input Potential	—	GND to PECL V_{CC} + 0.5V	—
V_{CC} Differential PECL V_{CC} to TTL V_{CC}	—	–1.0 to +1.0	V
Voltage Applied to Output in High State (with V_{CC} = 0V) Tri-State Output	—	–0.5 to +5.5	V
Current Applied to Output in Low State (max.)	—	Twice the Rated I_{OL}	mA

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

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DC ELECTRICAL CHARACTERISTICS

PECL V_{CC} = +5.0V ± 5%; TTL V_{CC} = +5.0V ± 5%; GND = 0V

Symbol	Parameter		Min.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	Data	PECL V_{CC} – 1.165	PECL V_{CC} – 0.870	V	Guaranteed HIGH Signal for ALL Inputs (with One Input Tied to V_{BB})
		$\overline{OE}$	2.0	—		Guaranteed HIGH Signal (TTL)
V_{IL}	Input LOW Voltage	Data	PECL V_{CC} – 1.830	PECL V_{CC} – 1.475	V	Guaranteed LOW Signal for ALL Inputs (with One Input Tied to V_{BB})
		$\overline{OE}$	—	0.8		Guaranteed LOW Signal (TTL)
V_{BB}	Output Reference Voltage		PECL V_{CC} – 1.38	PECL V_{CC} – 1.26	V	I_{BB} = 0.0mA or –1.0mA
V_{OH}	Output HIGH Voltage (TTL)		2.7	—	V	I_{OH} = –3mA
V_{OL}	Output LOW Voltage (TTL)		—	0.5	V	I_{OL} = 24mA
I_{IH}	Input HIGH Current	Data	—	150	µA	V_{IN} = V_{IH}(Max.), D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = V_{IL}(Min.)
		$\overline{OE}$	—	20		V_{IN} = 2.7V (TTL)
I_{IL}	Input LOW Current	$\overline{OE}$	—	–200	µA	V_{IN} = 0.5V (TTL)
I_{BVI}	Input Breakdown Current	$\overline{OE}$	—	100	µA	V_{IN} = +5.5V, V_{TTL} = +5.25V
I_{CBO}	Input Leakage Current		–10	—	µA	V_{IN} = GND, D_0–D_5 = V_{BB} $\overline{D_0}$–$\overline{D_5}$ = V_{IL}(Min.)
I_{OZH}	Three-State Current Output HIGH		—	50	µA	V_{OUT} = +2.7V
I_{OZL}	Three-State Current Output LOW		—	–50	µA	V_{OUT} = +0.5V
I_{CC}	PECL Supply Current		13	30	mA	—
I_{CCZ}	TTL Supply Current		10	20	mA	Three-State
I_{CCL}	TTL Suply Current LOW		8	17	mA	LOW State
I_{CCH}	TTL Supply Current HIGH		0.4	2.0	mA	HIGH State
I_{OS}	Output Short Circuit Current		–150	–60	mA	V_{OUT} = 0.0V, V_{CC} = +5.25
V_{Diff}	Differential Input Voltage		150	—	mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage		PECL V_{CC} – 2.0	PECL V_{CC} – 0.5	V	—
V_{CD}	Clamp Diode Voltage		—	–1.2	V	I_{IN} = –18mA

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{CC} = +5.0V ± 5%;T_C = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{MAX}	Maximum Clock Frequency	100	—	100	—	100	—	MHz
t_{PLH} t_{PHL}	Propagation Delay[1] Data to Output	3.3	6.4	3.3	6.1	3.3	6.1	ns
t_{PZH} t_{PZL}	Output Enable Time[2]	2.7 2.3	4.8 3.9	2.7 2.3	4.8 3.9	3.0 2.6	5.1 4.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2]	2.3 2.0	4.6 3.6	2.3 2.0	4.6 3.6	2.3 2.0	4.6 3.6	ns

NOTES:

1. Refer to Figure 1.
2. Refer to Figure 2.

CERPACK AND PLCC

V_{CC} = +5.0V ± 5%;T_C = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{MAX}	Maximum Clock Frequency	100	—	100	—	100	—	MHz
t_{PLH} t_{PHL}	Propagation Delay[1] Data to Output	3.3	6.2	3.3	5.9	3.3	5.9	ns
t_{PZH} t_{PZL}	Output Enable Time[2]	2.7 2.3	4.6 3.7	2.7 2.3	4.6 3.7	3.0 2.6	4.9 4.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2]	2.3 2.0	4.4 3.4	2.3 2.0	4.4 3.4	2.3 2.0	4.4 3.4	ns

NOTES:

1. Refer to Figure 1.
2. Refer to Figure 2.

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TIMING WAVEFORMS

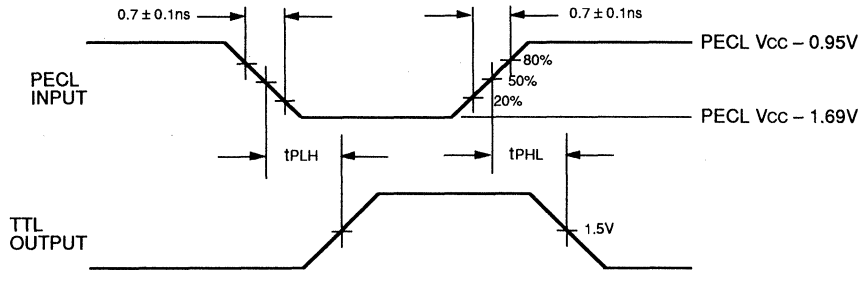


Figure 1. Data-to-Output Propagation Delay

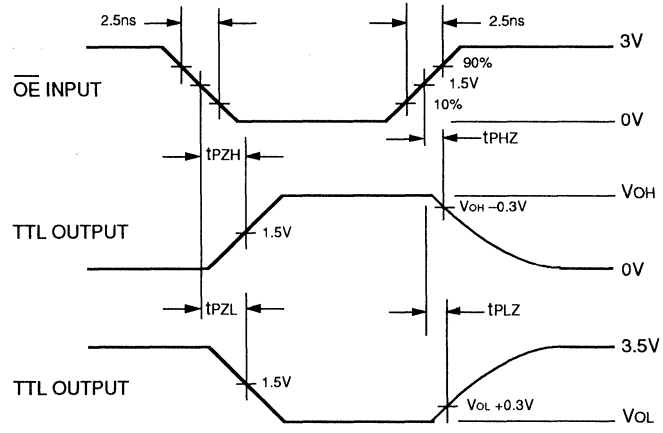
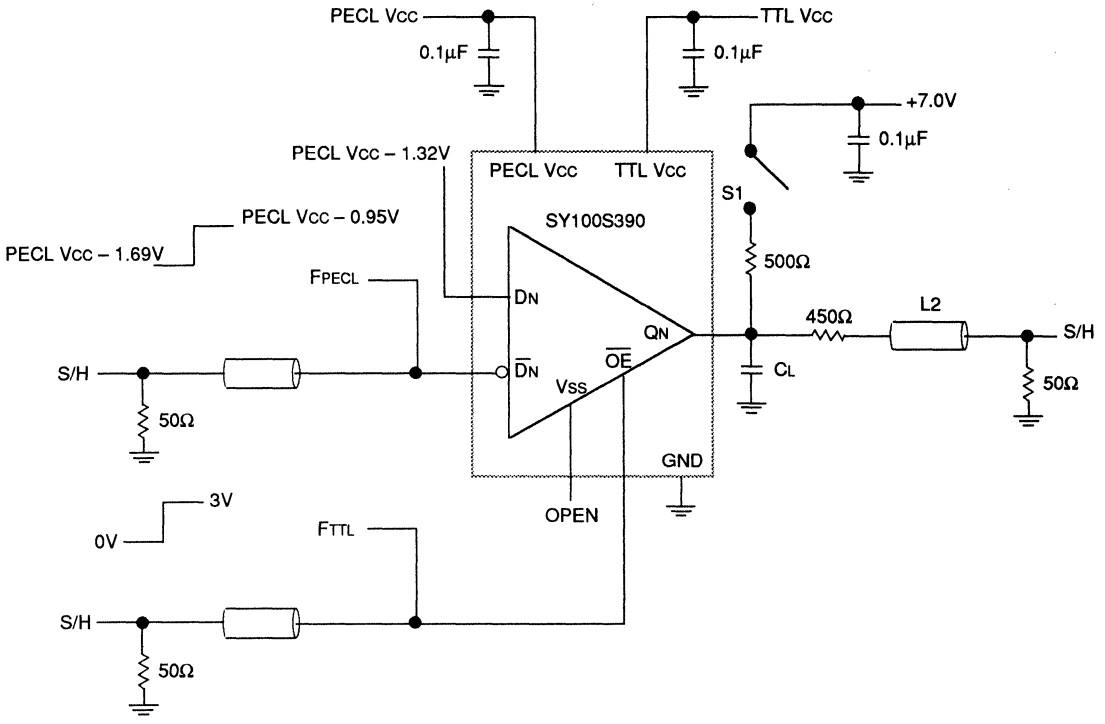


Figure 2. Enable/Disable Propagation Delay

AC TEST CIRCUIT



NOTES:

GND = 0V, PECL Vcc = +5V, TTL Vcc = +5V.
L1 and L2 = equal length 50Ω impedance lines.
50Ω terminators are internal to S/H measurement unit.
Decoupling 0.1µF from GND to PECL Vcc and TTL Vcc.
All unused outputs are loaded with 500Ω to GND.
C_L = Fixture and stray capacitance = 50pF.
Switch S1 is open for t_{PLH}, t_{PHL}, t_{PHZ} and t_{PZH} tests.
Switch S1 is closed only for t_{PLZ} and t_{PZL} tests.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S390DC	D24-1	Commercial
SY100S390FC	F24-1	Commercial
SY100S390JC	J28-1	Commercial

APPLICATION NOTES

1. Device performance will be enhanced by the use of dual VCC power planes, as illustrated in Application Figures 3 and 4. This will minimize the coupling of TTL switching noise into the primary reference to the PECL circuitry and take full advantage of the SY100S390's on-chip VCC partitioning.
2. The device's partitioned VCC may be operated from two 5V ± 5% tolerance supplies provided that they are ramped up/down together so that the maximum differential is 1V. This is to prevent overstress to internal ESD diodes. If the PECL driver to the 'S390 is powered from a separate supply, it must obey this sequence rule also.
3. Glitch-free power up, independent of data input levels, is achieved if TTL logic HIGH is held on the Output Enable pin during ramping up/down of the VCC supply.
4. Undefined output states can occur for some invalid combinations. See Truth Table. This should be avoided to prevent possible oscillation or increased power consumption due to TTL outputs biased into a quasi state with both pull-up and pull-down stages partially on. Three-Stating the outputs will counteract the effects of invalid input states.
5. Pins 8, 15 and 22 on the 28-pin PLCC package are tied to the chip's substrate and are named GNDs. These pins are electrically common to the ground pins 1, 2 and 28. For best thermal performance, tie the GND pins to the circuit ground plane. They may be tied to an electrically isolated thermal dissipation plane or may float.
6. Figure 3 illustrates typical differential input operation.
7. Figure 4 illustrates typical single-ended input operation.

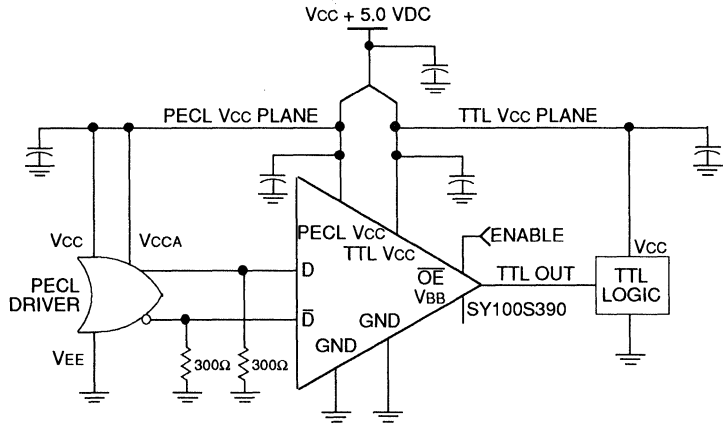


Figure 3.

APPLICATION NOTES (CONT'D.)

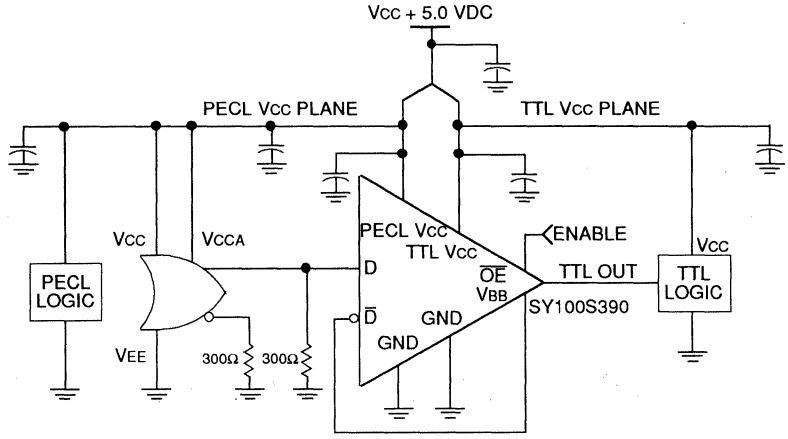


Figure 4.

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SYNERGY SEMICONDUCTOR

LOW-POWER HEX TTL-TO-PECL TRANSLATOR

PRELIMINARY
SY100S391

FEATURES

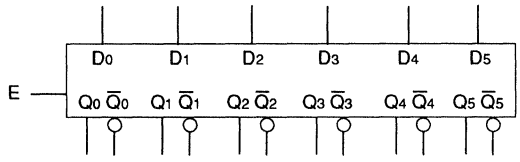
- **Operates from a single +5V supply**
- **Differential PECL outputs**
- **ESD protection of 2000V**
- **Companion chip to SY100S390 PECL-to-TTL translator**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

DESCRIPTION

The SY100S391 is a hex TTL-to-PECL translator for converting TTL logic levels to 100K logic levels. The unique feature of this translator is the ability to do this translation using only one +5V supply. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. A common enable (E), when LOW, holds all inverting outputs HIGH and all non-inverting inputs LOW.

The SY100S391 is ideal for those mixed PECL/TTL applications which only have a +5V supply available. When used in the differential mode, the S391, due to its high common mode rejection, overcomes voltage gradients between the TTL and PECL ground systems.

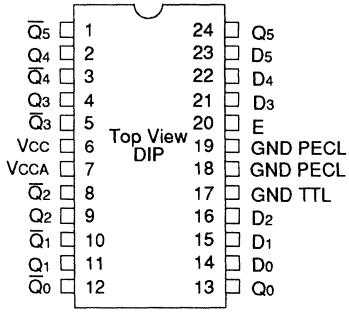
LOGIC SYMBOL

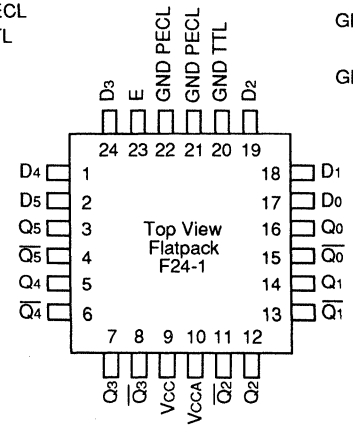


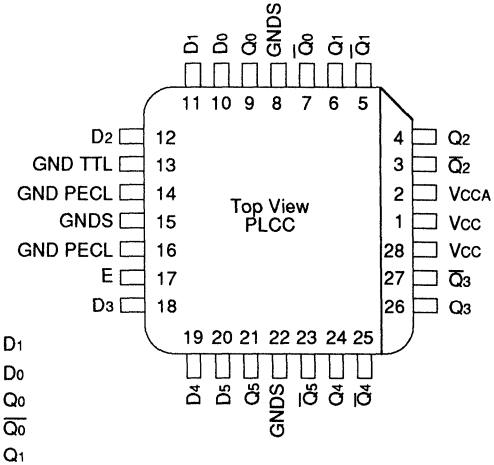
PIN NAMES

Label	Function
D_0 — D_5	Data Inputs (TTL)
Q_0 — Q_5	Data Outputs (PECL)
$\overline{Q}_0$ — $\overline{Q}_5$	Inverting Data Outputs (PECL)
E	Enable Input (TTL)

PIN CONFIGURATIONS







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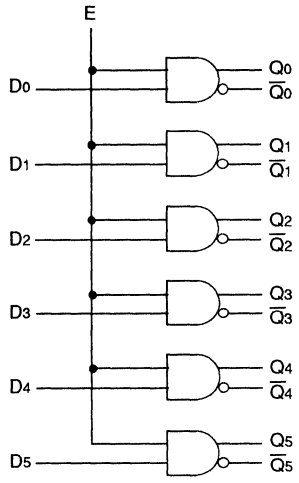
Issue Date: April, 1994

BLOCK DIAGRAM



TRUTH TABLE

Inputs		Outputs	
D_n	E	Q_n	$\overline{Q}_n$
H	H	H	L
L	H	L	H
H	L	L	H
L	L	L	H

NOTE:

1. H = High Voltage Level, L = Low Voltage Level

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operating Temperature	T_A	0 to +85	°C
Supply Voltage	V_{CC}	+4.5 to +5.5	V

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Storage Temperture	T_{STG}	–65 to +150	°C
Max. Junction Temp. Ceramic Plastic	T_J	 +175 +150	 °C °C
V_{CC} Pin Potential to Ground Pin	—	–0.5 to +7.0	V
PECL Output Current (DC Output HIGH)	—	–50	mA
TTL Input Voltage[2]	—	–0.5 to +7.0	V
TTL Input Current[2]	—	–30 to +5.0	mA

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

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TTL-TO-PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5.0V ± 10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC} –1025	V_{CC} –955	V_{CC} –870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620		Loading with 50Ω to V_{CC} –2V
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} –1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to V_{CC} –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	V_{CC} –1610		
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_A Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_A Range
I_{IH}	Input HIGH Current	—	—	10	µA	V_{IN} = +2.7V
	Breakdown Current	—	—	100	µA	V_{IN} = +5.5V, V_{CC} = Max.
I_{IL}	Input LOW Current D_n E	 –0.8 –4.2	—	—	mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{CC}	Vcc Supply Current	32	—	69	mA	Inputs Open

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

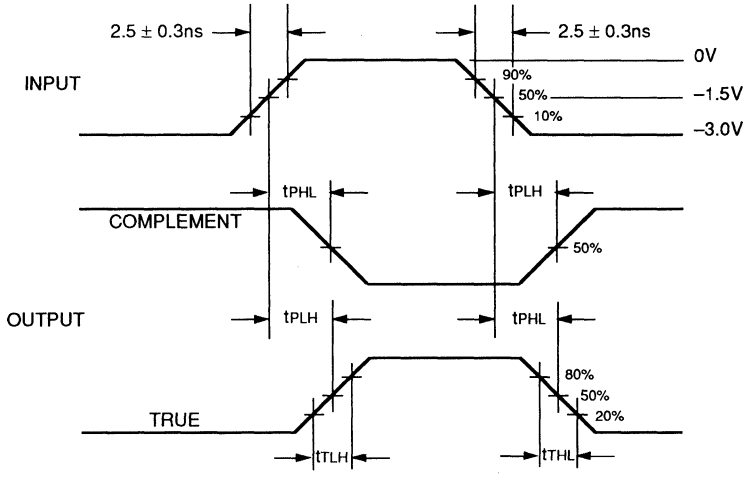
AC ELECTRICAL CHARACTERISTICS

CERDIP, CERPACK AND PLCC

V_{CC} = +5.0V ± 10%;T_C = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = 85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	400	1400	400	1400	400	1400	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	350	1700	350	1700	350	1700	ps

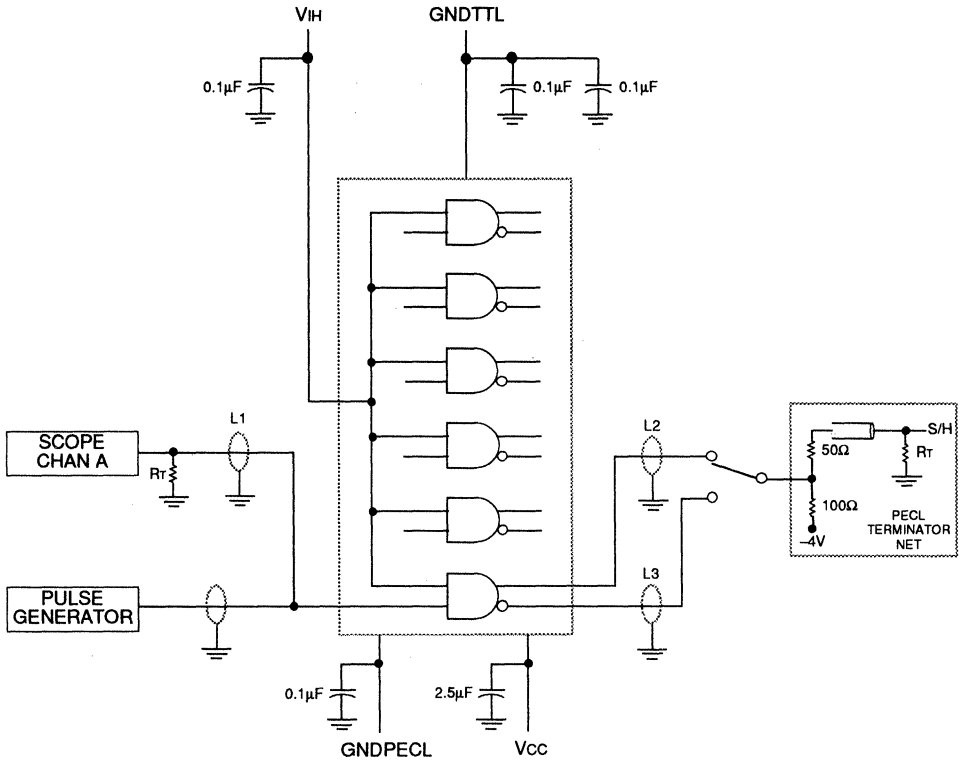
TIMING DIAGRAM



Propagation Delay and Transition Times

6

TEST CIRCUIT



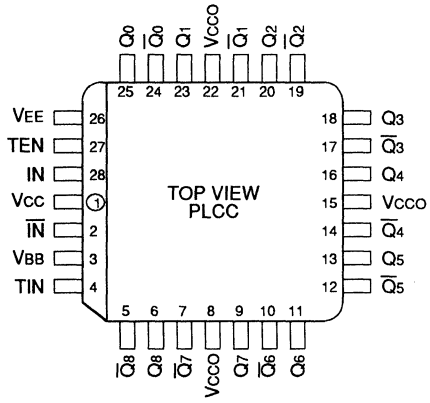
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S391DC	D24-1	Commercial
SY100S391FC	F24-1	Commercial
SY100S391JC	J28-1	Commercial

FEATURES

- PECL version of popular ECLinPS E111
- Low skew
- Guaranteed skew spec
- V_{BB} output
- TTL enable input
- Selectable TTL or PECL clock input
- Single +5V supply
- Differential internal design
- Similar pin configuration to E111
- PECL I/O fully compatible with industry standard
- Internal 75KΩ PECL input pull-down resistors
- ESD protection of 2000V

PIN CONFIGURATION



DESCRIPTION

The SY100S811 is a low skew 1-to-9 PECL differential driver designed for clock distribution in new, high-performance PECL systems. It accepts either a PECL clock input or a TTL input by using the TTL enable pin TEN. When the TTL enable pin is at a TTL logic one level, the TTL input is enabled and the PECL input is disabled. When the enable pin is set to TTL logic zero level, the TTL input is disabled and the PECL input is enabled.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E811 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO} as the pair(s) being used on that side) in order to maintain minimum skew.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of PECL signals to that device only. When using V_{BB} for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01μF capacitor.

PIN NAMES

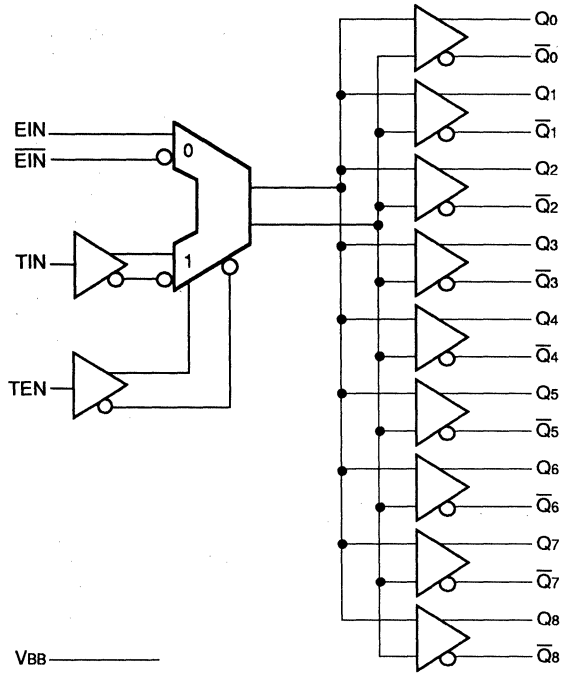
Pin	Function
EIN, $\overline{EIN}$	Differential PECL Input Pair
TIN	TTL Input
TEN	TTL Input Enable
Q0, $\overline{Q0}$ – Q8, $\overline{Q8}$	Differential PECL Outputs
V_{BB}	V_{BB} Output
V_{CC}	PECL V_{CC} (+5.0V)
V_{EE}	PECL Ground (0V)

TRUTH TABLE

TEN	EIN	TIN	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V	$V_{CC} = V_{CCO} = 5.0V$
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.835	—	4.12	3.835	—	4.12	3.835	—	4.12	V	$V_{CC} = V_{CCO} = 5.0V$
V_{IL}	Input LOW Voltage	3.19	—	3.525	3.19	—	3.525	3.19	—	3.525	V	$V_{CC} = V_{CCO} = 5.0V$
I_{CC}	Power Supply Current	—	53	65	—	53	65	—	60	74	mA	All inputs and outputs open

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	—
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	— —	20 100	— —	— —	20 100	— —	— —	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = 5.0V$
I_{IL}	Input LOW Current	—	—	–0.6	—	—	–0.6	—	—	–0.6	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	–1.2	—	—	–1.2	—	—	–1.2	V	$I_{IN} = -18mA$

AC ELECTRICAL CHARACTERISTICS[1–6]

$V_{CC} = V_{CCO} = 5V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output[1] EIN (differential) EIN (single-ended) TIN	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	ps	 2 3
t_{SKEW}	Within-Device Skew	—	25	50	—	25	50	—	25	50	ps	4
V_{PP}	Minimum PECL Input Swing	250	—	—	250	—	—	250	—	—	mV	5
V_{CMR}	PECL Common Mode Range	–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V	6
t_r t_f	Output Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps	—

NOTES:

1. Part-to-part skew is defined as Max. — Min. value at the given temperature.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the S811, as a differential input as low as 50mV will still produce full PECL levels at the output.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

PRODUCT ORDERING CODE

ORDERING CODE	PACKAGE TYPE	OPERATING RANGE
SY100S811JC	J28-1	Commercial

8-INPUT PECL DIFFERENTIAL MULTIPLEXER W/TTL SELECTS

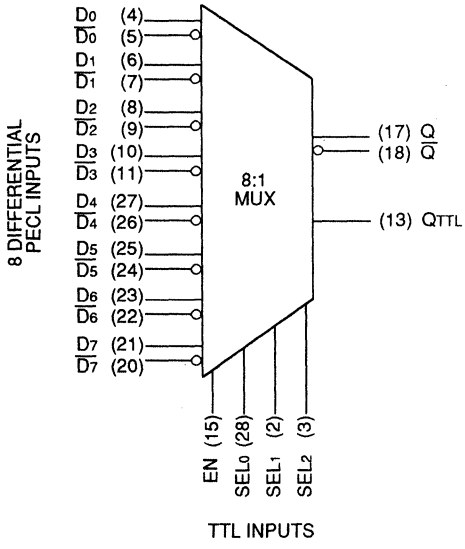
FEATURES

- **Low skew**
- **Differential PECL inputs**
- **Differential cut-off PECL outputs capable of driving 25Ω load for driving data bus**
- **Tri-state TTL output**
- **TTL select and enable input**
- **ESD protection of 2000V**
- **Internal 75KΩ PECL input pull-down resistors**
- **PECL I/O fully compatible with industry standard**

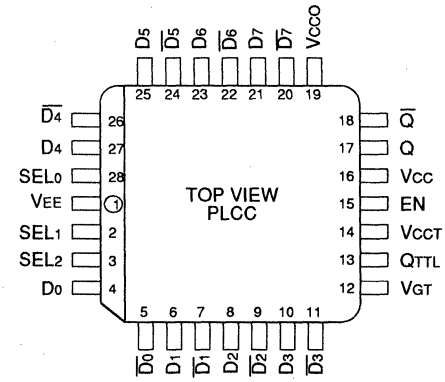
DESCRIPTION

The SY100S863 is a PECL 8:1 multiplexer designed for use in new, high-performance PECL systems. It has differential PECL outputs and a standard TTL output. The TTL select inputs (SEL_0, SEL_1, SEL_2) determine which one of the eight differential PECL data inputs (D_0–D_7) is propagated to the outputs. The enable pin, EN, is provided for expansion. When EN is at a TTL logic one level, both PECL and TTL outputs are enabled. When the enable pin is set to TTL logic zero level, both PECL outputs of the differential pair are in cut-off and the TTL output is in a three-state condition.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0, $\overline{D_0}$ – D_7, $\overline{D_7}$	Differential PECL Input Pairs
Q, $\overline{Q}$	Differential PECL Outputs
Q_{TTL}	TTL Output
EN	Enable Input
$SEL_{0,1,2}$	Select Inputs

TRUTH TABLE

EN	SEL_2	SEL_1	SEL_0	Q	Q_{TTL}
H	L	L	L	D_0	D_0
H	L	L	H	D_1	D_1
H	L	H	L	D_2	D_2
H	L	H	H	D_3	D_3
H	H	L	L	D_4	D_4
H	H	L	H	D_5	D_5
H	H	H	L	D_6	D_6
H	H	H	H	D_7	D_7
L	X	X	X	Z	Z

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Issue Date: April, 1994

PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCT} = 5.0V$; $V_{EE} = V_{GT} = GND$; $T_C = 0°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	3.975	4.045	4.13	V	Loading with 25Ω to 3V
V_{OL}	Output LOW Voltage	3.17	3.295	3.38	V	Loading with 25Ω to 3V
V_{OZ}	Cutoff Voltage	—	3	3.10	V	Loading with 25Ω to 3V
V_{IH}	Input HIGH Voltage	3.835	—	4.13	V	—
V_{IL}	Input LOW Voltage	3.17	—	3.525	V	—
I_{IH}	Input HIGH Current	—	—	350	µA	$V_{IN} = V_{IH}$ (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	$V_{IN} = V_{IL}$ (Min.)
I_{CC}	Vcc Supply Current	—	73	88	mA	—

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCT} = 5.0V \pm 5\%$; $V_{EE} = V_{GT} = GND$; $T_C = 0°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	2.9	—		$I_{OH} = -3mA$
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	$I_{OL} = 24mA$
V_{IH}	Input HIGH Voltage	2.0	—	V_{CC}	V	—
V_{IL}	Input LOW Voltage	0	—	0.8	V	—
I_{IH}	Input HIGH Current	—	—	1.0	mA	$V_{IN} = 2.7V$
I_{IL}	Input LOW Current	–0.7	—	—	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	–1.2	—	—	V	$I_{IN} = -18mA$
I_{OS}	Output Short Circuit Current	–200	—	–60	mA	$V_{OUT} = 0V$, $V_{CCT} = 5.5V$
I_{OZHT}	Tri-state Current Output HIGH	—	—	70	µA	$V_{OUT} = 2.7V$
I_{OZLT}	Tri-state Current Output LOW	–700	—	—	µA	$V_{OUT} = 0.5V$

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PECL AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5V \pm 5\%$; $V_{EE} = V_{GT} = GND$, $T_C = 0°C$ to $+85°C$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay[1]										ps	$R_L = 50\Omega$
t_{PHL}	D to Q	500	—	900	500	—	900	500	—	900		
	SEL_0 to Q	300	—	2000	300	—	2000	300	—	2000		
	SEL_1 to Q	300	—	1750	300	—	1750	300	—	1750		
	SEL_2 to Q	300	—	1500	300	—	1500	300	—	1500		
t_{PZH}	EN to Q (Cutoff to HIGH)	300	—	1750	300	—	1750	300	—	1750	ps	Figures 1 and 2
t_{PHZ}	EN to Q (HIGH to Cutoff)	300	—	1300	300	—	1300	300	—	1300		
t_r	Output Rise/Fall Time	300	400	600	300	400	600	300	400	600	ps	$R_L = 50\Omega$
t_f	20% to 80%											

NOTE:

1. Part-to-part skew is defined as Max. – Min. value at the given temperature.

TTL AC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5V \pm 5\%$; $V_{EE} = V_{GT} = GND$, $T_C = 0°C$ to $+85°C$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay[1]										ns	Figures 3 and 4
t_{PHL}	D to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
	SEL_0 to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
	SEL_1 to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
	SEL_2 to Q_{TTL}	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
t_{PZH}	EN to TTL Output	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	Figures 3 and 4
t_{PZL}	(Enable Time)	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
t_{PHZ}	EN to TTL Output	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	Figures 3 and 4
t_{PLZ}	(Disable Time)	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0		
t_r	Output Rise/Fall Time										ns	$C_L = 25pF$
t_f	0.8V to 2.4V	0.3	—	1.6	0.3	—	1.6	0.3	—	1.6		
	0.8Vto 2.0V	0.3	—	1.2	0.3	—	1.2	0.3	—	1.2		

NOTE:

1. Part-to-part skew is defined as Max. – Min. value at the given temperature.

PECL-TO-PECL TEST CIRCUITRY

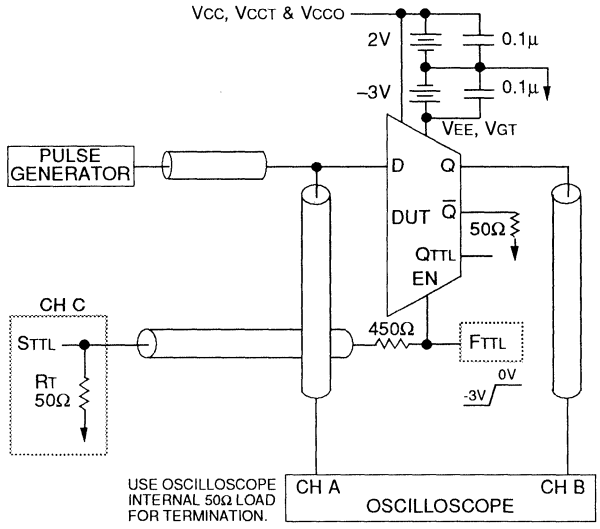

Figure 1. PECL-to-PECL AC Test Circuit

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PECL-TO-PECL SWITCHING WAVEFORMS

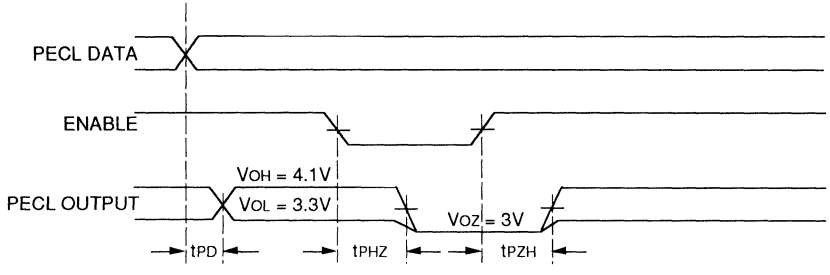


Figure 2. PECL-to-PECL Transition — Propagation Delay and Transition Times

PECL-TO-TTL TEST CIRCUITRY

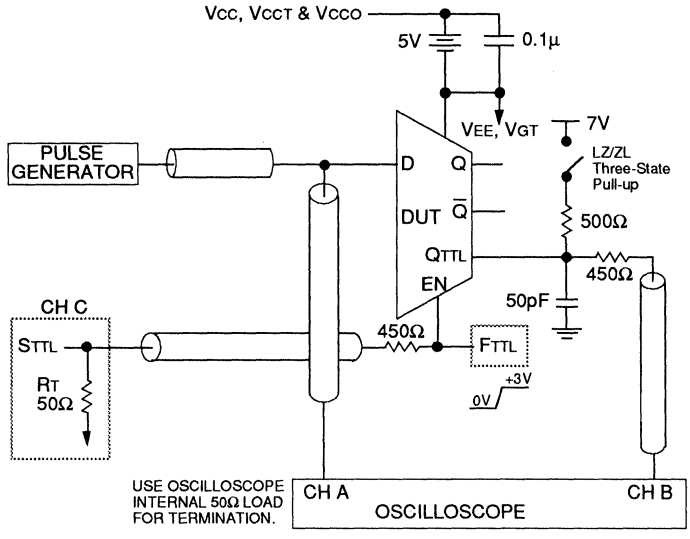


Figure 3. PECL-to-TTL AC Test Circuit

PECL-TO-TTL SWITCHING WAVEFORMS

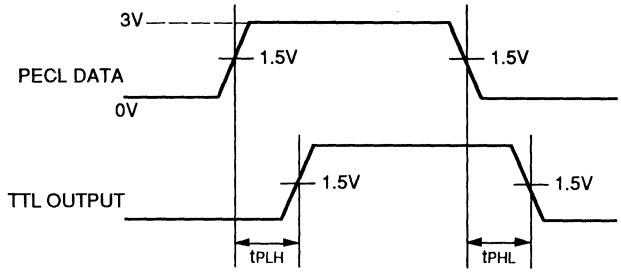


Figure 4a. PECL-to-TTL Transition, Data to TTL Output Delay

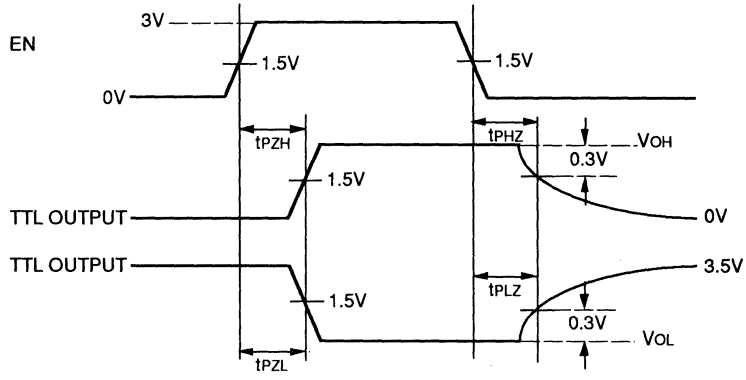


Figure 4b. EN to TTL Output Enable and Disable Times

PRODUCT ORDERING CODE

ORDERING CODE	PACKAGE TYPE	OPERATING RANGE
SY100S863JC	J28-1	Commercial

5-BIT REGISTERED TRANSCEIVER

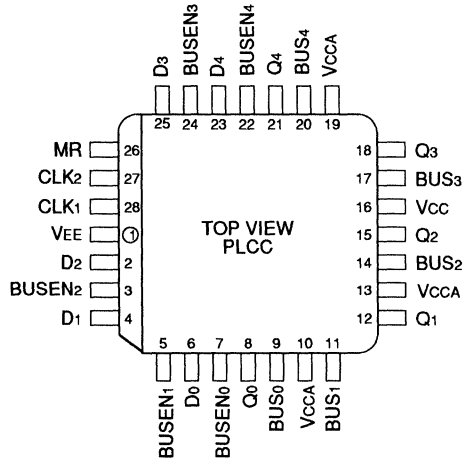
FEATURES

- **25 ohm cut-off bus outputs**
- **50 ohm receiver outputs**
- **Transmit and receive registers with separate clocks**
- **1500ps max. delay from CLK_1 to Bus Outputs (BUS)**
- **1500ps max. delay from CLK_2 to Receiver Outputs (Q)**
- **Individual bus enable pins**
- **Internal 75KΩ input pull-down resistors**
- **Voltage and temperature compensation for improved noise immunity**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option:**
  - **V_{EE} = –4.2V to –5.46V**

DESCRIPTION

The SY100S891 is a 5-bit registered transceiver containing five bus transceivers with both transmit and receive registers. The bus outputs (BUS_0 – BUS_4) are specified for driving a 25 ohm bus and the receive outputs (Q_0 – Q_4) are specified for driving a 50 ohm line. The bus outputs have a normal high level output voltage and a normal low level output voltage when the bus enable ($BUSEN_0$ – $BUSEN_4$) is high. However, the output is switched to a cut-off level when a bus-enable is low. This cut-off level is sufficiently low that a relatively high impedance is presented to the bus in order to minimize reflections. There is one bus-enable for each bus driver; a clock (CLK_1) which is common to all five bus driver registers; and a separate clock (CLK_2) which is common to all five receive registers. Data at the D inputs is clocked to the Bus register by a positive transition of CLK_1 and data on the bus is clocked into the Receiver register by a positive transition of CLK_2. A high on the Master Reset clears all registers.

PIN CONFIGURATION

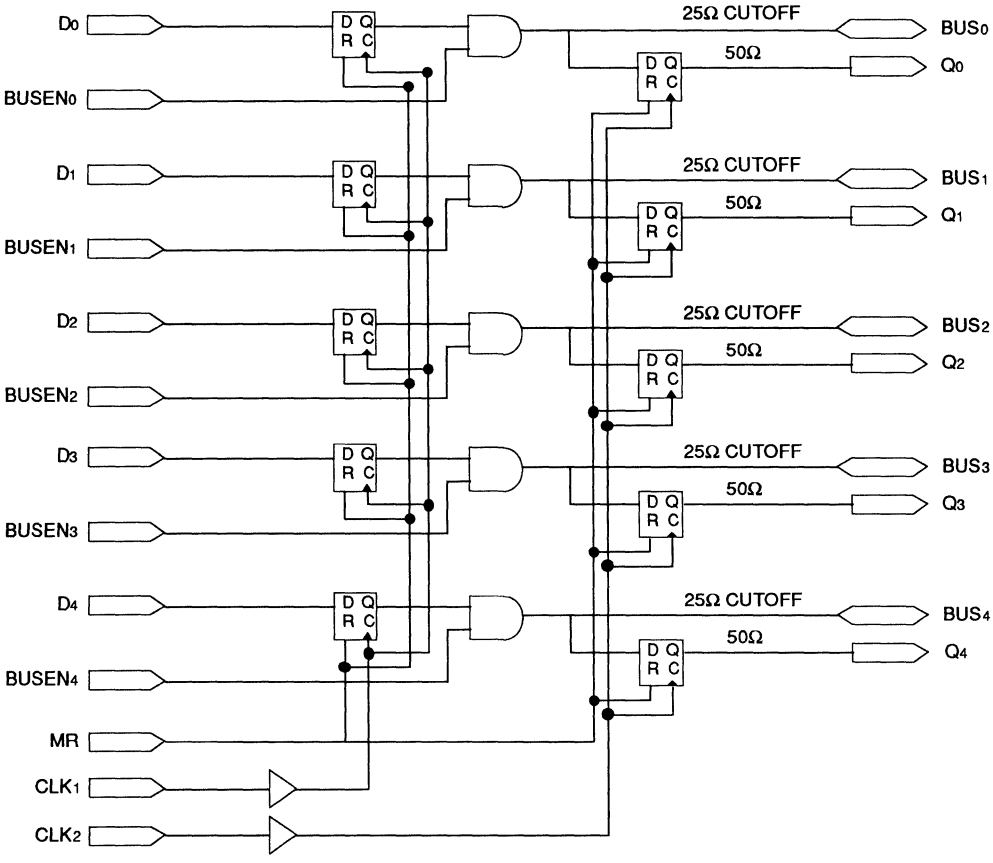


PIN NAMES

Pin	Function
$BUSEN_{0-4}$	Bus Enable Inputs
D_0 – D_4	Data Inputs
CLK_1	Bus Driver Clock Input
CLK_2	Receive Register Clock
MR	Master Reset
Q_0 – Q_4	Bus Receive Outputs
BUS_{0-4}	Bus Outputs

Rev.: B Amendment: /0
Issue Date: February, 1994

BLOCK DIAGRAM



6

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{CUT}	Cut-off Bus Output Voltage	–2200	–2160	–2100	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading with 25Ω to –2.20V
V_{OH}	Output HIGH Voltage Bus	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading with 25Ω to –2.0V
V_{OL}	Output LOW Voltage Bus	–1810	–1705	–1620	mV		
V_{OHA}	Output HIGH Voltage Bus	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.)	
V_{OLA}	Output LOW Voltage Bus	—	—	–1610	mV		
V_{OH}	Output HIGH Voltage Receiver	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading with 50Ω to –2.0V
V_{OL}	Output LOW Voltage Receiver	–1810	–1705	–1620	mV		
V_{OHA}	Output HIGH Voltage Receiver	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.)	
V_{OLA}	Output LOW Voltage Receiver	—	—	–1610	mV		
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IL} (Min.)	
I_{IH}	Input High Current	—	—	150	µA	V_{IN} = V_{IH} (Max.)	
I_{EE}	Power Supply Current	–216	—	—	mA	Inputs Open	
C_{IN}	Input Pin Capacitance	—	4	—	pF	—	
C_{OUT}	Output Pin Capacitance	—	5	—	pF	—	

AC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified; V_{CC} = V_{CCA} = GND; T_A = 0°C to +85°C

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay CLK_1 to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	Loaded with 25Ω to –2.0V
t_{PLH} t_{PHL}	Propagation Delay CLK_2 to Q	500	800	1200	500	800	1200	500	800	1200	ps	Loaded with 50Ω to –2.0V
t_{PLH} t_{PHL}	Propagation Delay BUSEN to Bus	500	800	1200	500	800	1200	500	800	1200	ps	Loaded with 25Ω to –2.0V
t_{PLH} t_{PHL}	Propagation Delay Master Reset to Bus	600	1000	1500	600	1000	1500	600	1000	1500	ps	Loaded with 25Ω to –2.0V
t_{PLH} t_{PHL}	Propagation Delay Master Reset to Q	500	800	1200	500	800	1200	500	800	1200	ps	Loaded with 50Ω to –2.0V
t_s	Set-up Time Bus Wrt CLK_2 D Wrt CLK_1	 — —	 — —	 400 400	 — —	 — —	 400 400	 — —	 — —	 400 400	ps	—
t_{REL}	Master Reset Release Time	—	—	1000	—	—	1000	—	—	1000	ps	—
t_h	Hold Time Bus Wrt CLK_2 D Wrt CLK_1	 — —	 — —	 400 400	 — —	 — —	 400 400	 — —	 — —	 400 400	ps	—
t_r	Output Rise Time Bus Q	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	ps	 25Ω Load 50Ω Load
t_f	Output Fall Time Bus Q	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	 500 300	 — —	 1000 900	ps	 25Ω Load 50Ω Load
t_{SKEW}	Skew (Maximum difference between slowest and fastest path)	—	100	—	—	100	—	—	100	—	ps	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S891JC	J28-1	Commercial

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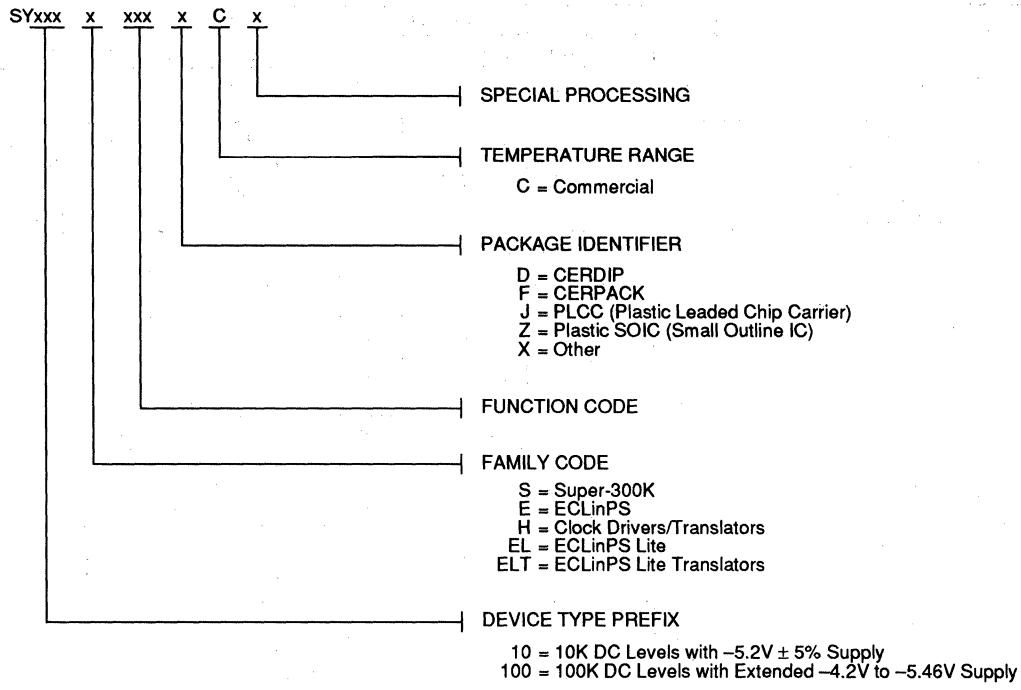
LOGIC ORDERING INFORMATION



Rev.: B Amendment: /0
Issue Date: February, 1994

TRANSLATORS

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DC SPECIFICATIONS 10H AND 100H

10H ECL DC ELECTRICAL

V_{CCT} = 5.0V ± 10%; V_{EE} = −5.2V ± 5%

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	145	—	145	µA	—
I_{IL}	Input LOW Current	—	1.5	—	1.0	—	1.0	mA	—
V_{IH}	Input HIGH Voltage	−1170	−840	−1130	−810	−1070	−735	mV	—
V_{IL}	Input LOW Voltage	−1950	−1480	−1950	−1480	−1950	−1450	mV	—
V_{OH}	Output HIGH Voltage	−1020	−840	−980	−810	−920	−735	mV	50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1950	−1630	−1950	−1630	−1950	−1600	mV	50Ω to −2.0V

100H ECL DC ELECTRICAL

V_{CCT} = 5.0V ± 10%; V_{EE} = −4.5V ± 0.3V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	145	—	145	µA	—
I_{IL}	Input LOW Current	—	1.5	—	1.0	—	1.0	mA	—
V_{IH}	Input HIGH Voltage	−1165	−880	−1165	−880	−1165	−880	mV	—
V_{IL}	Input LOW Voltage	−1810	−1475	−1810	−1475	−1810	−1475	mV	—
V_{OH}	Output HIGH Voltage	−1025	−880	−1025	−880	−1025	−880	mV	50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1620	−1810	−1620	−1810	−1620	mV	50Ω to −2.0V

TTL DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = −5.2V ± 5% (10H Version), V_{EE} = −4.5V ± 0.3V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	20 100	— —	20 100	— —	20 100	µA	V_{IN} = 2.7V V_{IN} = 7.0V
I_{IL}	Input LOW Current	—	−0.6	—	−0.6	—	−0.6	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	−1.2	—	−1.2	—	−1.2	V	I_{IN} = −18mA
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = −3.0mA I_{OH} = −15mA
V_{OL}	Output LOW Voltage	—	0.55	—	0.55	—	0.55	V	I_{OL} = 48mA

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9-BIT TTL–ECL TRANSLATOR

FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- ECL and TTL enable inputs
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- ESD protection of 2000V
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H600

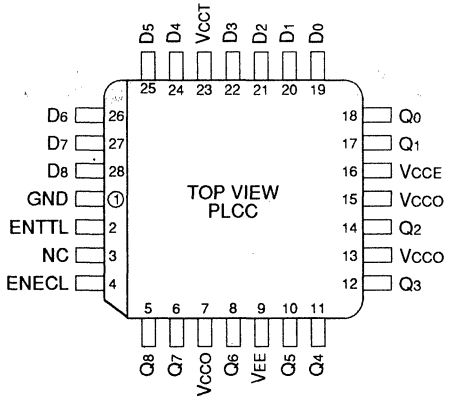
DESCRIPTION

The SY10H600 and SY100H600 are 9-bit, dual supply TTL-to-ECL translators. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

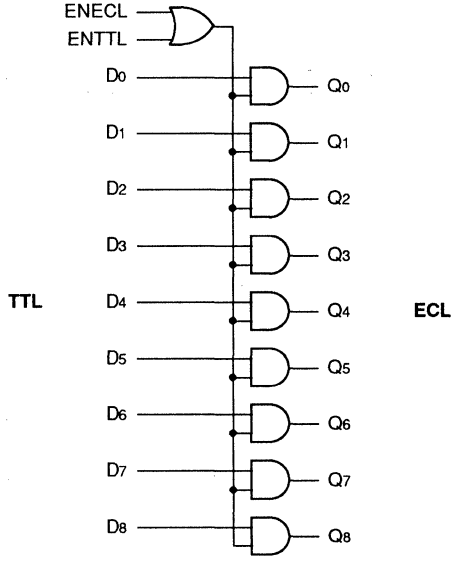
The H600 features both ECL and TTL logic enable controls for maximum flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VCCE	ECL Vcc (0V)
VCCO	ECL Vcc (0V) — Outputs
VCCT	TTL Supply (+5.0V)
VEE	ECL Supply (–5.2/–4.5V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
ENTTL	Enable Control (TTL)

Rev.: B Amendment: /0
Issue Date: April, 1994

TRUTH TABLE

ENECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{EE}	Power Supply Current, ECL							mA	—
	10H	—	125	—	125	—	125		
	100H	—	122	—	123	—	132		
I_{CCH}	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
I_{CCL}		—	50	—	50	—	50		

AC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output							ns	50Ω to –2.0V
t_{PHL}	D	1.4	3.0	1.5	3.2	1.7	3.5		
	ENECL/ENTTL	1.8	3.7	1.9	3.9	2.0	4.1		
t_r	Output Rise/Fall Time	0.5	1.5	0.5	1.5	0.5	1.5	ns	50Ω to –2.0V
t_f	20% to 80%, 80% to 20%								

PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H600JC	J28-1	Commercial
SY100H600JC	J28-1	Commercial

9-BIT ECL-TTL TRANSLATOR

FEATURES

- **9-bit ideal for byte-parity applications**
- **3-state TTL outputs**
- **ESD protection of 2000V**
- **Flow-through configuration**
- **Extra TTL and ECL power pins to minimize switching noise**
- **ECL and TTL 3-state control inputs**
- **4.8ns max. delay into 50pF, 9.6ns into 200pF (all outputs switching)**
- **PNP TTL inputs for low loading**
- **Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)**
- **Fully compatible with Motorola MC10H/100H601**

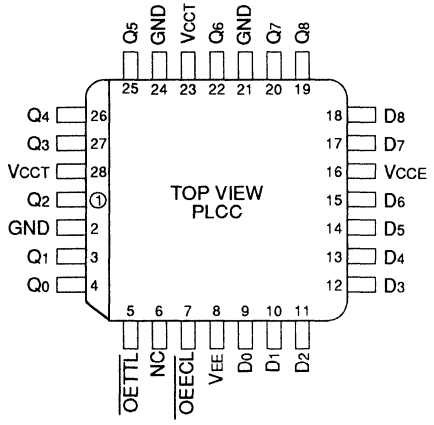
DESCRIPTION

The SY10H601 and SY100H601 are 9-bit, dual supply ECL-to-TTL translators. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

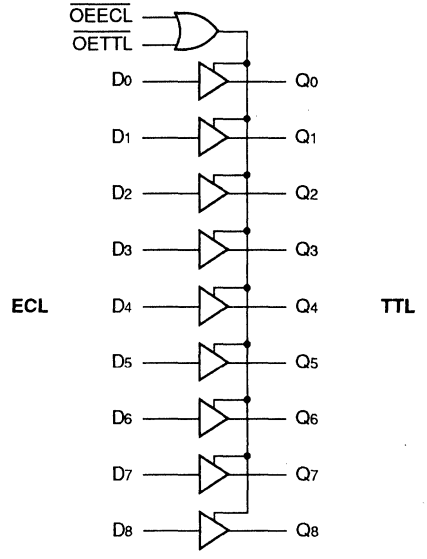
The devices feature a 48mA TTL output stage and AC performance is specified into both a 50pF and 200pF load capacitance. For the 3-state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
V_{CCE}	ECL Vcc (0V)
V_{CCT}	TTL Supply (+5.0V)
V_{EE}	ECL Supply (–5.2/–4.5V)
D_0–D_8	Data Inputs (ECL)
Q_0–Q_8	Data Outputs (TTL)
$\overline{OEECL}$	3-State Control (ECL)
$\overline{OETTL}$	3-State Control (TTL)

Rev.: B Amendment: /0
Issue Date: April, 1994

TRUTH TABLE

$\overline{OEECL}$	$\overline{OETTL}$	D	Q
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{EE}	Power Supply Current, ECL	—	46	—	46	—	50	mA	—
I_{CCH}	Power Supply Current, TTL	—	110	—	110	—	110	mA	—
I_{CCL}		—	110	—	110	—	110		
I_{CCZ}		—	105	—	105	—	105		
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V
I_{OZH}	Output Disable Current HIGH	—	50	—	50	—	50	µA	V_{OUT} = 2.7V
I_{OZL}	Output Disable Current LOW	—	–50	—	–50	—	–50	µA	V_{OUT} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

		T_A = 0°C		T_A = +25°C		T_A = +75°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH}	Propagation Delay to Output	1.7	4.8	1.7	4.8	1.7	4.8	ns	C_L = 50pF
t_{PHL}		3.4	9.6	3.4	9.6	3.4	9.6		C_L = 200pF
t_{PLZ}	Output Disable Time, $\overline{OEECL}$	3.7	6.5	3.7	6.5	3.7	6.5	ns	C_L = 50pF
t_{PHZ}		5.4	13	5.4	13	5.4	13		C_L = 200pF
t_{PLZ}	Output Disable Time, $\overline{OETTL}$	4.3	7.5	4.3	7.5	4.3	7.5	ns	C_L = 50pF
t_{PHZ}		7.0	15	7.0	15	7.0	15		C_L = 200pF
t_{PZL}	Output Enable Time, $\overline{OEECL}$	3.5	6.0	3.5	6.0	3.5	6.0	ns	C_L = 50pF
t_{PZH}		5.0	12	5.0	12	5.0	12		C_L = 200pF
t_{PZL}	Output Enable Time, $\overline{OETTL}$	4.2	7.0	4.2	7.0	4.2	7.0	ns	C_L = 50pF
t_{PZH}		6.0	14	6.0	14	6.0	14		C_L = 200pF
t_r	Output Rise/Fall Time	—	1.2	—	1.2	—	1.2	ns	C_L = 50pF
t_f	1.0V – 2.0V	—	3.0	—	3.0	—	3.0		C_L = 200pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H601JC	J28-1	Commercial
SY100H601JC	J28-1	Commercial

9-BIT LATCH TTL-ECL TRANSLATOR

FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- ESD protection of 2000V
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H602

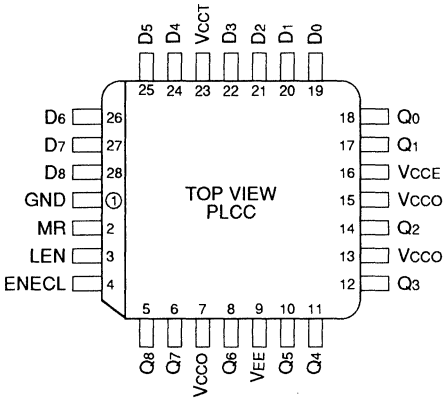
DESCRIPTION

The SY10H602 and SY100H602 are 9-bit, dual supply TTL-to-ECL translators with latches. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

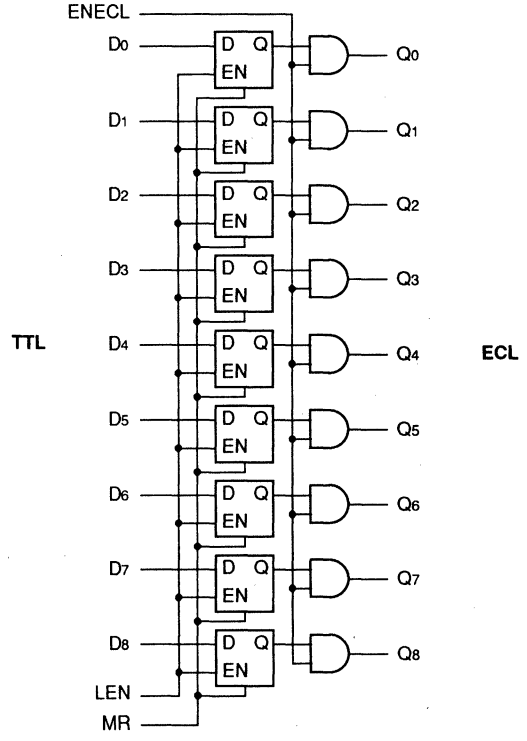
The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VCCE	ECL Vcc (0V)
VCCO	ECL Vcc (0V) — Outputs
VCCT	TTL Supply (+5.0V)
VEE	ECL Supply (–5.2/–4.5V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

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Issue Date: April, 1994

TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q_0
X	X	H	H	L
X	X	X	L	L

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current, ECL							mA	—
	10H	—	125	—	125	—	125		
	100H	—	122	—	123	—	132		
I_{CCH}	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
I_{CCL}		—	50	—	50	—	50		

AC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH}	Propagation Delay to Output							ns	—
t_{PHL}	D	1.4	3.0	1.5	3.2	1.7	3.5		
	LEN	2.0	3.4	2.1	3.5	2.4	3.7		
	MR	2.0	3.4	2.1	3.5	2.5	3.9		
	ENECL	1.6	3.2	1.7	3.3	1.8	3.7		
t_s	Set-up Time, D to LEN	2.0	—	2.0	—	2.0	—	ns	—
t_h	Hold Time, D to LEN	1.0	—	1.0	—	1.0	—	ns	—
$t_{w(L)}$	LEN Pulse Width, LOW	2.0	—	2.0	—	2.0	—	ns	—
t_r	Output Rise/Fall Time	0.5	1.5	0.5	1.5	0.5	1.5	ns	—
t_f	20% to 80%, 80% to 20%								

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H602JC	J28-1	Commercial
SY100H602JC	J28-1	Commercial

9-BIT LATCH ECL-TTL TRANSLATOR

FEATURES

- **9-bit ideal for byte-parity applications**
- **3-state TTL outputs**
- **ESD protection of 2000V**
- **Flow-through configuration**
- **Extra TTL and ECL power/ground pins to minimize switching noise**
- **Dual supply**
- **6.0ns max. delay into 50pF, 12ns into 200pF (all outputs switching)**
- **PNP TTL inputs for low loading**
- **Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)**
- **Fully compatible with Motorola MC10H/100H603**

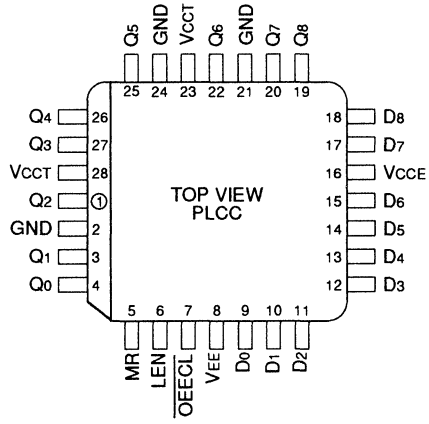
DESCRIPTION

The SY10H603 and SY100H603 are 9-bit, dual supply ECL-to-TTL translators. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

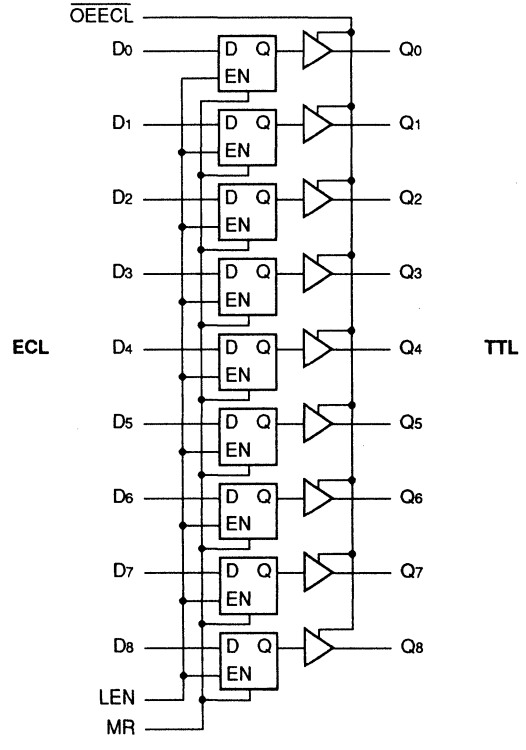
The devices feature a 48mA TTL output stage and AC performance is specified into both a 50pF and 200pF load capacitance. Latching is controlled by Latch Enable (LEN) and Master Reset (MR) resets the latches. A HIGH on $\overline{OEECL}$ sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VCCE	ECL Vcc (0V)
VCCT	TTL Supply (+5.0V)
VEE	ECL Supply (–5.2/–4.5V)
D0–D8	Data Inputs (ECL)
Q0–Q8	Data Outputs (TTL)
$\overline{OEECL}$	3-state Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

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Issue Date: April, 1994

TRUTH TABLE

D	LEN	MR	$\overline{OEECL}$	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q_0
X	X	H	L	L
X	X	X	H	Z

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current, ECL	45	63	45	64	45	68	mA	—
I_{CCH} I_{CCL} I_{CCZ}	Power Supply Current, TTL	80 80 80	110 110 110	80 80 80	110 110 110	80 80 80	110 110 110	mA	—
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V
I_{OZH}	Output Disable Current, HIGH	—	50	—	50	—	50	µA	V_{OUT} = 2.7V
I_{OZL}	Output Disable Current, LOW	—	–50	—	–50	—	–50	µA	V_{OUT} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –5.2V ± 5% (10H Version); V_{EE} = –4.5V ± 0.3V (100H Version)

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.2 6.4	6.0 12	3.2 6.4	6.0 12	3.2 6.4	6.0 12	ns	C_L = 50pF C_L = 200pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns	C_L = 50pF C_L = 200pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns	C_L = 50pF C_L = 200pF
t_s	Set-up Time, D to LEN		1.5	—	1.5	—	1.5	—	ns	—
t_h	Hold Time, D to LEN		0.8	—	0.8	—	0.8	—	ns	—
$t_{w(L)}$	LEN Pulse Width, LOW		2.0	—	2.0	—	2.0	—	ns	—
t_{PLZ} t_{PHZ}	Output Disable Time		2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns	C_L = 50pF C_L = 200pF
t_{PZL} t_{PZH}	Output Enable Time		2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns	C_L = 50pF C_L = 200pF
t_r t_f	Output Rise/Fall Time 1.0V – 2.0V		0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns	C_L = 50pF C_L = 200pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H603JC	J28-1	Commercial
SY100H603JC	J28-1	Commercial

REGISTERED HEX TTL-TO-PECL TRANSLATOR

FEATURES

- **Differential 50Ω ECL outputs**
- **Choice between differential PECL or TTL clock input**
- **Single +5V power supply**
- **VBB output for single-ended use**
- **Multiple power and ground pins to minimize noise**
- **Specified within-device skew**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10H/100H606**

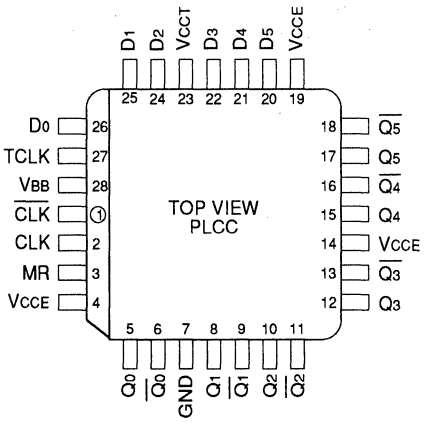
DESCRIPTION

The SY10H606 and SY100H606 are 6-bit, registered, single supply TTL-to-PECL translators. The devices feature differential PECL outputs as well as a choice between either a differential PECL clock input or a TTL clock input. The asynchronous master reset control is a PECL level input.

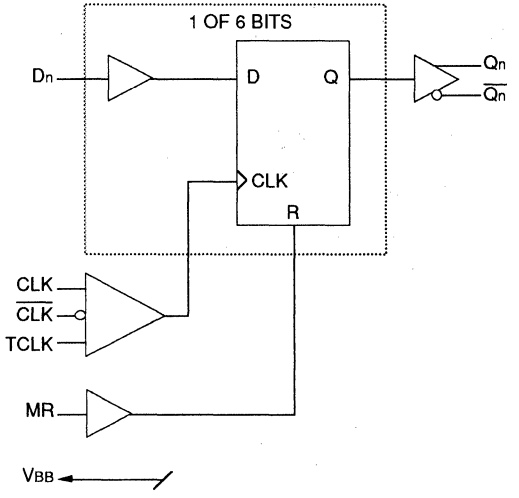
With its differential ECL outputs and TTL inputs, the H606 device is ideally suited for the transmit function of a HPPI bus-type board-to-board interface application. The on-chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with 10KH logic levels, while the 100H device is compatible with 100K logic levels.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

Pin	Function
D0 – D5	TTL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Inputs
TCLK	TTL Clock Input
MR	PECL Master Reset Input
Q0 – Q5	True PECL Outputs
$\overline{Q0}$ – $\overline{Q5}$	Inverted PECL Outputs
VCCE	PECL Vcc
VCCT	TTL Vcc
GND	TTL/PECL Ground

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Rev.: B Amendment: /0
Issue Date: April, 1994

TRUTH TABLE

Dn	MR	TCLK/CLK	Qn + 1
L	L	Z	L
H	L	Z	H
X	H	X	L

NOTE:
1. Z = LOW-to-HIGH transition.

DC ELECTRICAL CHARACTERISTICS

$V_{CCE} = V_{CCT} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A =+ 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{EE}	ECL Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
I_{CCH}	TTL Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
I_{CCL}		—	—	—	—	—	—	—	—	—	mA	—

AC ELECTRICAL CHARACTERISTICS

$V_{CCE} = V_{CCT} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A =+ 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q TCLK to Q MR to Q	 — — —	 — — —	 — — —	 — — —	 2.0 3.0 2.8	 — — —	 — — —	 — — —	 — — —	ns	—
t_{SKEW}	Device Skew Part-to-Part Skew Within-Device Skew	 — —	 — —	 — —	 — —	 1.0 0.35	 — —	 — —	 — —	 — —	ns	—
t_S	Set-up Time	—	—	—	—	0.5	—	—	—	—	ns	—
t_H	Hold Time	—	—	—	—	0.5	—	—	—	—	ns	—
t_{PW}	Minimum Pulse Width CLK, MR	 —	 —	 —	 —	 1.0	 —	 —	 —	 —	ns	—
V_{PP}	Minimum Input Swing	—	—	—	—	150	—	—	—	—	mV	—
t_r t_f	Rise/Fall Times	—	—	—	—	1.0	—	—	—	—	ns	20% — 80%

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H606JC	J28-1	Commercial
SY100H606JC	J28-1	Commercial

REGISTERED HEX PECL-TO-TTL TRANSLATOR

ADVANCE INFORMATION
SY10H607
SY100H607

FEATURES

- **Differential PECL data and clock inputs**
- **48mA sink, 15mA source TTL outputs**
- **Single +5V power supply**
- **Multiple power and ground pins to minimize noise**
- **Specified within-device skew**
- **VBB output for single-ended use**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10H/100H607**

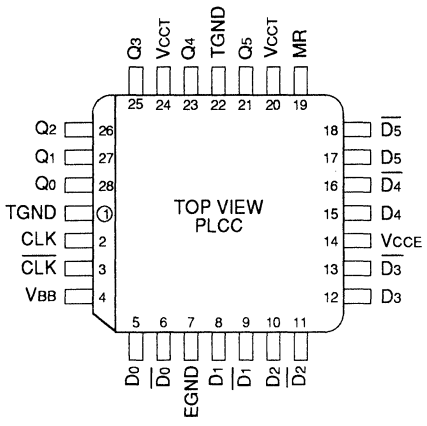
DESCRIPTION

The SY10H607 and SY100H607 are 6-bit, registered, dual supply PECL-to-TTL translators. The devices feature differential PECL inputs for both data and clock. The TTL outputs feature 48mA sink, 15mA source drive capability for driving high fanout loads. The asynchronous master reset control is a PECL level input.

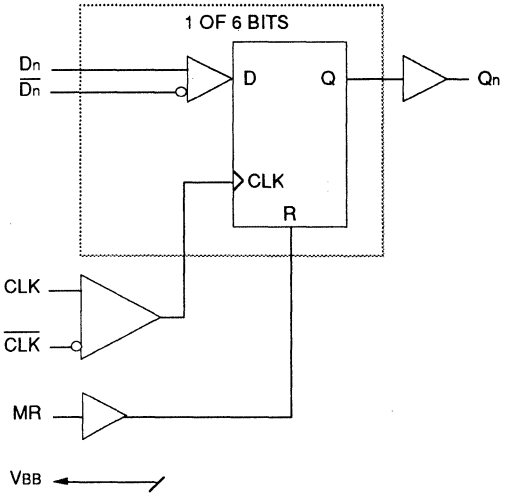
With its differential PECL inputs and TTL outputs, the H607 device is ideally suited for the receive function of a HPPI bus-type board-to-board interface application. The on-chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with 10KH logic levels, while the 100H device is compatible with 100K logic levels.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

Pin	Function
D0 — D5	True PECL Data Inputs
$\overline{D0}$ — $\overline{D5}$	Inverted PECL Data Inputs
CLK, $\overline{CLK}$	Differential PECL Clock Input
MR	PECL Master Reset Input
Q0 — Q5	TTL Outputs
VCCE	PECL Vcc
VCCT	TTL Vcc
TGND	TTL Ground
EGND	PECL Ground

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Rev.: B Amendment: /0
Issue Date: April, 1994

TRUTH TABLE

Dn	MR	TCLK/CLK	Qn + 1
L	L	Z	L
H	L	Z	H
X	H	X	L

NOTE:
1. Z = LOW-to-HIGH transition.

DC ELECTRICAL CHARACTERISTICS

$V_{CCE} = V_{CCT} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	ECL Power Supply Current	—	—	—	—	—	—	mA	—
I_{CCH}	TTL Power Supply Current	—	—	—	—	—	—	mA	—
I_{CCL}		—	—	—	—	—	—	mA	—

AC ELECTRICAL CHARACTERISTICS

$V_{CCE} = V_{CCT} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A =+ 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q MR to Q	 — —	 — —	 — —	 — —	 6.5 6.5	 — —	 — —	 — —	 — —	ns	—
t_{SKEW}	Device Skew Part-to-Part Skew Within-Device Skew	 — —	 — —	 — —	 — —	 2.0 0.7	 — —	 — —	 — —	 — —	ns	—
t_S	Set-up Time	—	—	—	—	0.5	—	—	—	—	ns	—
t_H	Hold Time	—	—	—	—	0.5	—	—	—	—	ns	—
t_{PW}	Minimum Pulse Width CLK, MR	 —	 —	 —	 —	 1.0	 —	 —	 —	 —	ns	—
V_{PP}	Minimum Input Swing	—	—	—	—	150	—	—	—	—	mV	—
t_r t_f	Rise/Fall Times	—	—	—	—	1.2	—	—	—	—	ns	20% — 80%

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H6017C	J28-1	Commercial
SY100H607JC	J28-1	Commercial

SINGLE SUPPLY PECL-TTL 1:9 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H641

FEATURES

- PECL–TTL version of popular ECLInPS E111
- Guaranteed low skew specification
- Latch
- Differential internal design
- V_{BB} output for single-ended operation
- Single +5V supply
- ESD protection of 2000V
- Reset/enable
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H641/100H641

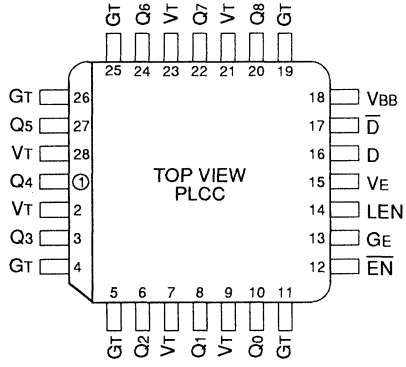
DESCRIPTION

The SY10H641 and SY100H641 are single supply, low skew translating 1:9 clock drivers. Devices in the Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

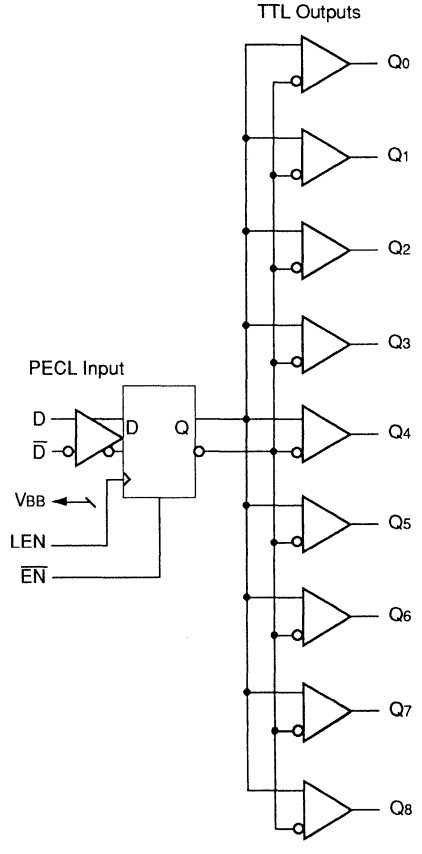
The devices feature a 24mA TTL output stage with AC performance specified into a 50pF load capacitance. A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
VBB	VBB Reference Output (positive ECL)
Q0 - Q8	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)
LEN	Latch Enable Input (positive ECL)

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Rev.: B Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	Vdc
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	Vdc
	V_I (TTL)	–0.5 to +7.0	
Disabled 3-State Output	V_{OUT} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{OUT} (ECL)	50	mAdc
Output Source Current Surge	I_{OUT} (ECL)	100	mAdc
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

NOTE:
1. Do not exceed.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	H	L	Q_0
X	X	H	L

DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	30	—	30	—	30	mA	V_E Pin
I_{CCH}		TTL	—	30	—	30	—	30		Total all V_T pins
I_{CCL}			—	35	—	35	—	35		

AC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_8	5.0	6.0	4.8	5.8	5.3	6.3	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew	Q_0–Q_8	—	1.0	—	1.0	—	1.0	ns	C_L = 50pF
t_{skwd}	Within-Device Skew	Q_0–Q_8	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Output	Q_0–Q_8	4.9	6.9	4.9	6.9	5.0	7.0	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_8	5.0	7.0	4.9	6.9	5.0	7.0	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_8	— —	1.7 1.6	— —	1.7 1.6	— —	1.7 1.6	ns	C_L = 50pF
f_{MAX}	Maximum Input Frequency		135	—	135	—	135	—	MHz	C_L = 50pF
—	Pulse Width		1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time		1.25	—	1.25	—	1.25	—	ns	—
t_{SET}[1]	Set-up		0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—
t_{HOLD}[1]	Hold Time		0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—

NOTE:
1. Guaranteed, but not tested.

VCC AND CLOAD

Ranges to meet duty cycle requirement: 0°C ≤ TA ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
PW1	Ranges of VCC and CL to meet min. pulse width (HIGH or LOW) at fOUT ≤ 40MHz	VCC CL PW	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
PW2	Ranges of VCC and CL to meet min. pulse width (HIGH or LOW) at fOUT ≤ 50MHz	VCC CL PW	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

PIN DESCRIPTION

Pin	Symbol	Description
1	Q4	Signal Output (TTL)
2	VT	TTL VCC (+5.0V)
3	Q3	Signal Output (TTL)
4	GT	TTL Ground (0V)
5	GT	TTL Ground (0V)
6	Q2	Signal Output (TTL)
7	VT	TTL VCC (+5.0V)
8	Q1	Signal Output (TTL)
9	VT	TTL VCC (+5.0V)
10	Q0	Signal Output (TTL)
11	GT	TTL Ground (0V)
12	$\overline{EN}$	Enable Input POS (ECL)
13	GE	ECL Ground (0V)
14	LEN	Latch Enable Input POS (ECL)

Pin	Symbol	Description
15	VE	ECL VCC (+5.0V)
16	D	ECL Signal Input (Non-inverting)
17	$\overline{D}$	ECL Signal Input (Inverting)
18	VBB	VBB Reference Output POS (ECL)
19	GT	TTL Ground (0V)
20	Q8	Signal Output (TTL)
21	VT	TTL VCC (+5.0V)
22	Q7	Signal Output (TTL)
23	VT	TTL VCC (+5.0V)
24	Q6	Signal Output (TTL)
25	GT	TTL Ground (0V)
26	GT	TTL Ground (0V)
27	Q5	Signal Output (TTL)
28	VT	TTL VCC (+5.0V)

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH}(1) V_{IL}(1)	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	V_E = 5.0V

NOTE:

1. V_{IH} and V_{IL} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for V_{CC} = 5.0V.

100H ECL DC ELECTRICAL CHARACTERISTICS

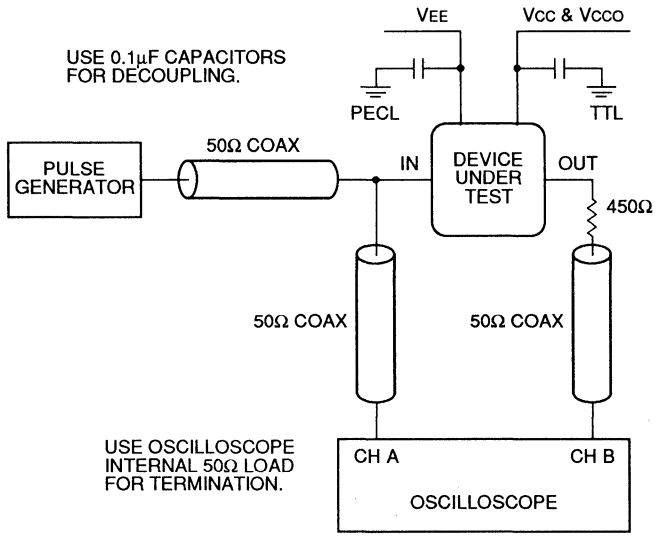
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH}(1) V_{IL}(1)	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	V_E = 5.0V

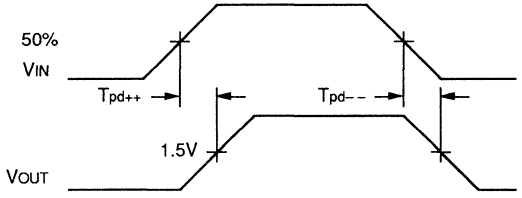
NOTE:

1. V_{IH} and V_{IL} are referenced to V_{CC} and will vary 1:1 with the power supply. The levels shown are for V_{CC} = 5.0V.

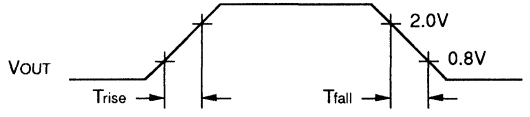
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H641JC	J28-1	Commercial	10KH
SY100H641JC	J28-1	Commercial	100K

FEATURES

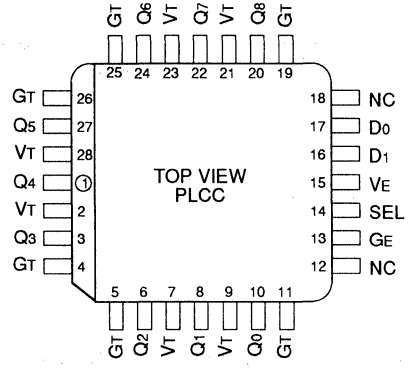
- **Low skew(typically 0.65ns within device)**
- **Guaranteed skew spec 1.25ns part-to-part**
- **Input clock muxing**
- **Differential ECL internal design**
- **Single +5V supply**
- **ESD protection of 2000V**
- **Extra TTL and ECL power/ground pins**
- **Fully compatible with Motorola MC10H645**

DESCRIPTION

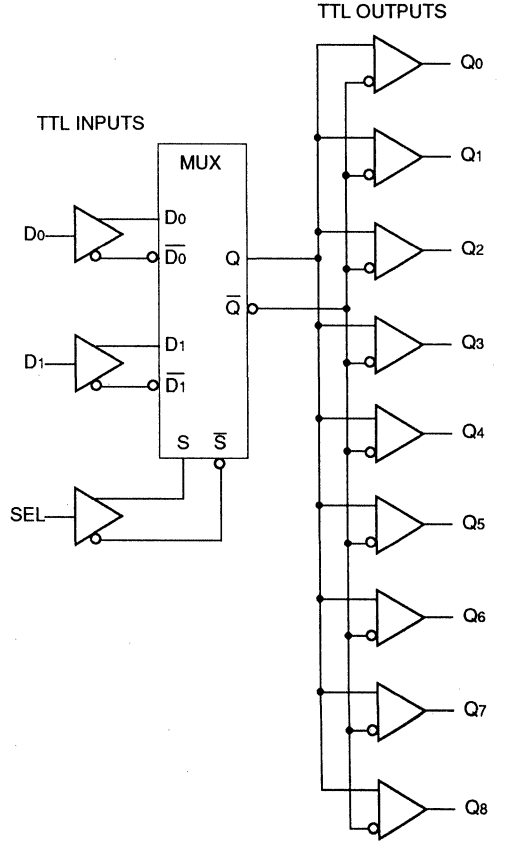
The SY10H645 is a single supply, low skew, TTL I/O 1:9 Clock Driver. Devices in the H600 clock driver family utilize the 28-lead PLCC for optimal power and signal pin placement.

The device features a 24mA TTL output stage with AC performance specified into a 50pF load capacitance. A 2:1 input mux is provided on-chip to allow for distributing both system and diagnostic clock signals or designing clock redundancy into a system. With the SEL input held LOW, the D_0 input will be selected, while the D_1 input is selected when the SEL input is forced HIGH.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
Dn	TTL Signal Input
Q0 - Q8	TTL Signal Outputs
SEL	TTL Mux Select

Rev.: B Amendment:/0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (TTL)	–0.5 to +7.0	V
Disabled 3-State Output	V_{OUT} (TTL)	0.0 to V_T	V
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:
1. Do not exceed.

TRUTH TABLE

D_0	D_1	SEL	Q
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	30	—	30	—	30	mA	V_E Pin
I_{CCH}		TTL	—	30	—	30	—	30		Total all V_T pins
I_{CCL}			—	35	—	35	—	35		
V_{OH}	Output HIGH Voltage		2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage		—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current		–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V

AC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_0 to Output Only	Q_0–Q_8	5.2	6.2	5.2	6.2	5.6	6.6	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew D_0 to Output Only	Q_0–Q_8	—	1.0	—	1.0	—	1.0	ns	—
t_{skwd}[1]	Within-Device Skew D_0 to Output Only	Q_0–Q_8	—	0.65	—	0.65	—	0.65	ns	—
t_{PLH} t_{PHL}	Propagation Delay SEL to Q	Q_0–Q_8	5.2	7.3	5.2	7.2	5.7	7.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 0.8V to 2.0V	Q_0–Q_8	0.5 0.5	1.7 1.6	0.5 0.5	1.7 1.6	0.5 0.5	1.7 1.6	ns	C_L = 50pF
t_S	Set-up Time, SEL to D	—	1.0	—	1.0	—	1.0	—	ns	—

NOTE:
1. Within-device skew defined as identical transitions on similar paths through a device.

7

DUTY CYCLE SPECIFICATIONS

0°C ≤ TA ≤ +85°C. Duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
PW	Range of VCC and CL to meet min.	VCC	4.875	5.0	5.125	V	All Outputs
	pulse width (HIGH or LOW) at	CL	10.0	—	50	pF	
	fOUT ≤ 50MHz	PW	9.0	—	11.0	ns	

PIN DESCRIPTION

Pin	Symbol	Description
1	Q4	Signal Output (TTL)
2	VT	TTL VCC (+5.0V)
3	Q3	Signal Output (TTL)
4	GT	TTL Ground (0V)
5	GT	TTL Ground (0V)
6	Q2	Signal Output (TTL)
7	VT	TTL VCC (+5.0V)
8	Q1	Signal Output (TTL)
9	VT	TTL VCC (+5.0V)
10	Q0	Signal Output (TTL)
11	GT	TTL Ground (0V)
12	NC	No Connection
13	GE	ECL Ground (0V)
14	SEL	Select Input (TTL)

Pin	Symbol	Description
15	VE	ECL VCC (+5.0V)
16	D1	ECL Signal Input (Non-inverting)
17	D0	ECL Signal Input (Inverting)
18	NC	No Connection
19	GT	TTL Ground (0V)
20	Q8	Signal Output (TTL)
21	VT	TTL VCC (+5.0V)
22	Q7	Signal Output (TTL)
23	VT	TTL VCC (+5.0V)
24	Q6	Signal Output (TTL)
25	GT	TTL Ground (0V)
26	GT	TTL Ground (0V)
27	Q5	Signal Output (TTL)
28	VT	TTL VCC (+5.0V)

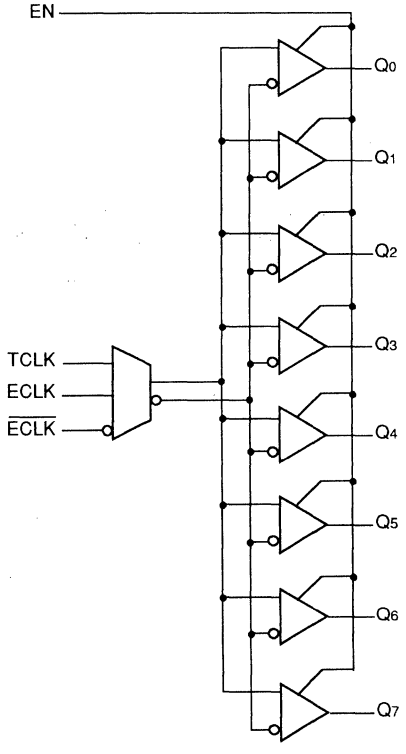
PECL/TTL–TTL 1:8 CLOCK DISTRIBUTION CHIP

ClockWorks™
PRELIMINARY
SY10/100H646

FEATURES

- PECL/TTL–TTL version of popular ECLinPS E111
- Meets specifications required to drive high-performance x86 processors
- Guaranteed low skew specification
- Three-state enable
- Differential internal design
- VBB output for single-ended operation
- Single +5V supply
- ESD protection of 2000V
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: 10H or 100K
- Matched high and low output impedance
- Fully compatible with Motorola MC10/100H646

BLOCK DIAGRAM



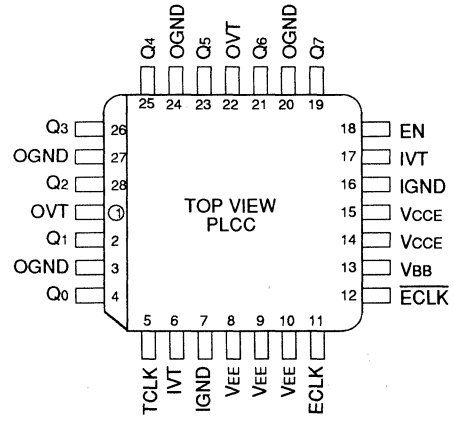
DESCRIPTION

The SY10H646 and SY100H646 are single supply, low skew translating 1:8 clock drivers. Devices in the Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance. The single supply H646 is similar to the H643 which is a dual supply 1:8 version of the same function.

The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

The 10H version is compatible with 10H ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



PIN NAMES

Pin	Function
OGND	TTL Output Ground (0V)
OVT	TTL Output Vcc (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL Vcc (+5.0V)
VEE	ECL VEE (0V)
VCCE	ECL Ground (+5.0V)
ECLK, $\overline{\text{ECLK}}$	Differential Signal Input (PECL)
VBB	VBB Reference Output
Q0–Q7	Signal Outputs (TTL)
EN	Three-State Enable Input (TTL)
LEN	Signal Input (TTL)

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Rev.: B Amendment: /0
Issue Date: April, 1994

DC ELECTRICAL CHARACTERISTICS

$V_T = OVT = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.6	—	2.6	—	2.6	—	V	I_{OH} =24mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	—	—	—	—	—	—	mA	Note 1

NOTE:

1. The outputs must not be shorted to ground, as this will result in permanent damage to the device. The high drive outputs of this device do not include a limiting Ios resistor.

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = OVT = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	225	—	—	175	—	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.83	—	4.16	3.87	—	4.19	3.94	—	4.28	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{IL}	Input LOW Voltage	3.05	—	3.52	3.05	—	3.52	3.05	—	3.555	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{BB}	Output Reference Voltage	3.62	—	3.73	3.65	—	3.75	3.69	—	3.81	V	IVT = IVO = V_{CCE} = 5.0V(1)

NOTE:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = +5.0V.

100K ECL DC ELECTRICAL CHARACTERISTICS

$V_T = OVT = V_{CCE} = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	225	—	—	175	—	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.835	—	4.12	3.835	—	4.12	3.835	—	3.835	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{IL}	Input LOW Voltage	3.19	—	3.525	3.19	—	3.525	3.19	—	3.525	V	IVT = IVO = V_{CCE} = 5.0V(1)
V_{BB}	Output Reference Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V	IVT = IVO = V_{CCE} = 5.0V(1)

NOTE:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CCE} and will vary 1:1 with the power supply. The levels shown are for IVT = IVO = V_{CCE} = +5.0V.

DC ELECTRICAL CHARACTERISTICS

IVT = OVT = VCCE = 5.0V ± 5%

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
ICCL	Power Supply Current	—	—	—	—	166	—	—	—	—	mA	Total all OVT,
ICCH		—	—	—	—	154	—	—	—	—		IVT, and VCCE pins

AC ELECTRICAL CHARACTERISTICS

IVT = OVT = VCCE = 5.0V ± 5%

Symbol	Parameter		TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay to Output	Q0–Q7	—	—	—	—	6.5	—	—	—	—	ns	CL = 50pF
tskpp	Part-to-Part Skew		—	—	1.0	—	—	1.0	—	—	1.0	ns	
tskwd	Within-Device Skew		—	—	0.5	—	—	0.5	—	—	0.5	ns	
tw	Pulse Width Out HIGH or LOW @ fOUT = 50MHz	Q0–Q7	9.0	—	—	9.0	—	—	9.0	—	—	ns	CL = 50pF
tR tF	Output Rise/Fall Time 0.8V to 2.4V 0.8V to 2.0V	Q0–Q7	— —	— —	1.6 1.2	0.7 0.3	— —	1.6 1.2	— —	— —	1.6 1.2	ns	CL = 50pF

NOTE:

The pre-silicon simulation value for typical propagation delay to all outputs is 6.5ns. Final value will be established as the measured statistical mean after characterization of a sufficient number of lots, and thus may not exactly equal the target. The skew specification is an absolute value that measures the worst case tPD difference between any two of the specified outputs.

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TRUTH TABLE

TCLK	ECLK	$\overline{ECLK}$	EN	Q
GND	L	H	H	L
GND	H	L	H	H
H	GND	GND	H	H
L	GND	GND	H	L
X	X	X	L	Z

NOTE:

X = Don't Care
L = Low Voltage Level
H = High Voltage Level
Z = Three-State

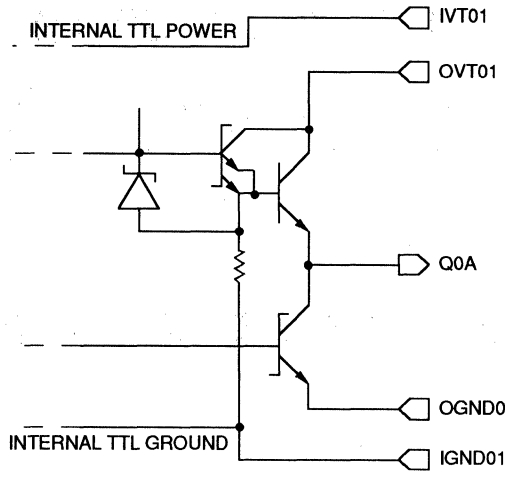


Figure 1. Output Structure

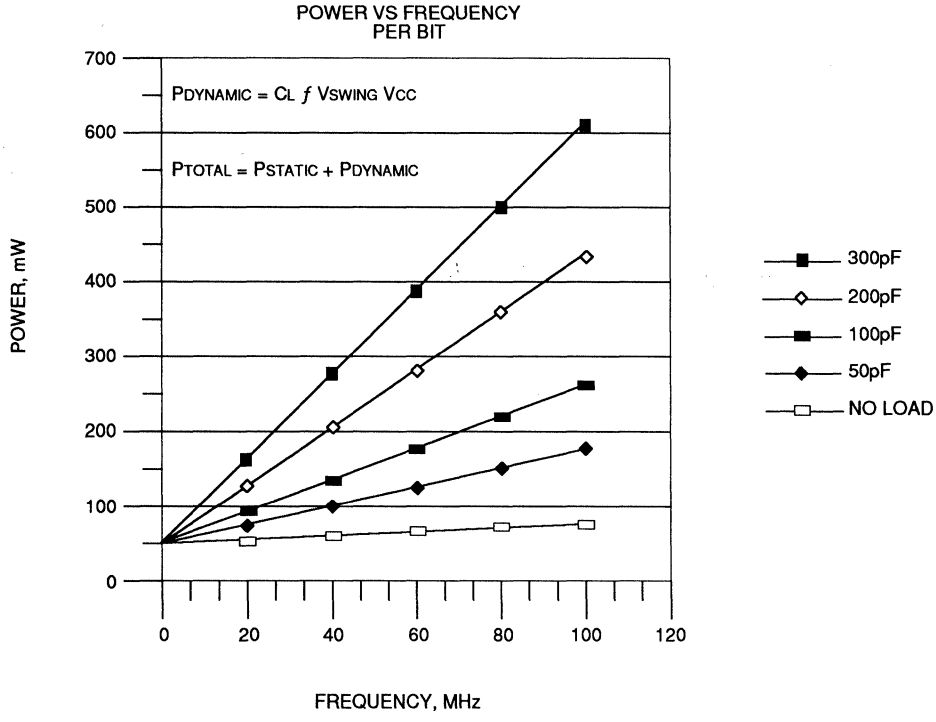


Figure 2. Power Versus Frequency (Typical)

SINGLE SUPPLY PECL-TTL 1:4 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H841

FEATURES

- **Translates positive ECL to TTL (PECL-TTL)**
- **300ps pin-to-pin skew**
- **Guaranteed skew spec**
- **Differential internal design for increased noise immunity and stable threshold inputs**
- **V_{BB} reference output**
- **Single supply**
- **Enable input**
- **Latch enable input**
- **Extra TTL and ECL power/ground pins to reduce cross-talk/noise**
- **High drive capability: 24mA each output**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10K, 100K I/O levels**

DESCRIPTION

The SY10H841 and SY100H841 are single supply, low skew translating 1:4 clock drivers.

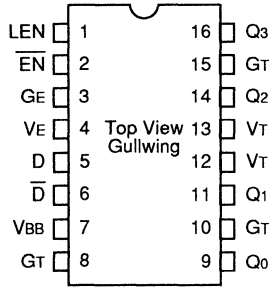
The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

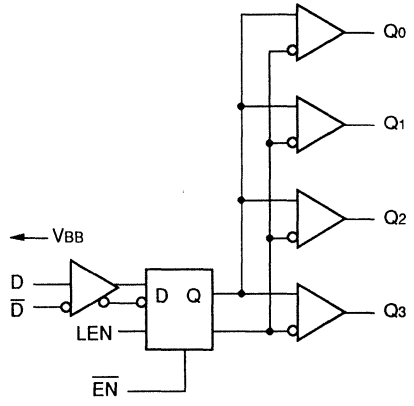
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H841 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
G_T	TTL Ground (0V)
V_T	TTL Vcc (+5.0V)
V_E	ECL Vcc (+5.0V)
G_E	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output (positive ECL)
Q_0 - Q_3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)
LEN	Latch Enable Input

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Rev.: B Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	V
	V_{OUT} (TTL)	0.0 to V_T	
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	$\overline{EN}$	Enable Input Pos (ECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL Vcc (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output Pos (ECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL Vcc (+5.0V)
13	V_T	TTL Vcc (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skwd++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skwd--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF
—	Pulse Width	Q_0–Q_3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q_0–Q_3	1.0	—	1.0	—	1.0	—	ns	—
t_S	Set-up Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—
t_H	Hold Time D, EN	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—

NOTES:

1. Device-to-Device Skew considering the same transitions at common Vcc level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
3. Within-Device Skew considering LOW-to-LOW transitions at common Vcc level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

7

VCC AND CLOAD

Ranges to meet duty cycle requirement: 0°C ≤ T_A ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \leq$ 40MHz	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \leq$ 50MHz	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	$I_{OH} = -3.0mA$ $I_{OH} = -15mA$
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	$I_{OL} = 24mA$
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	$V_{OUT} = 0V$

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

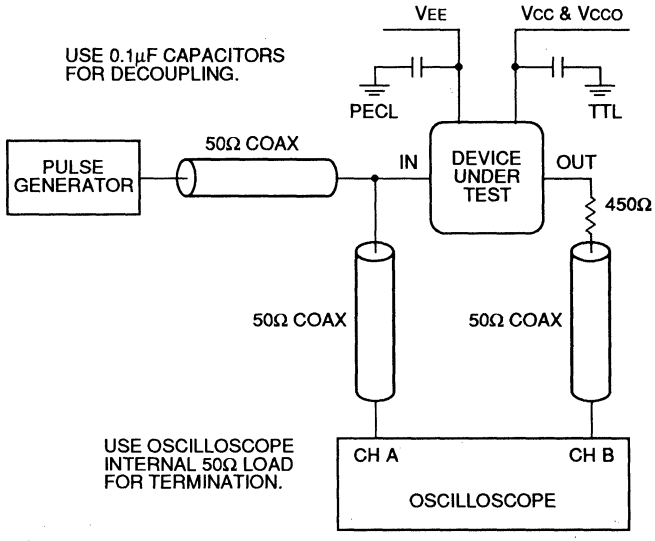
Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	$V_E = 5.0V$
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	$V_E = 5.0V$

100H ECL DC ELECTRICALCHARACTERISTICS

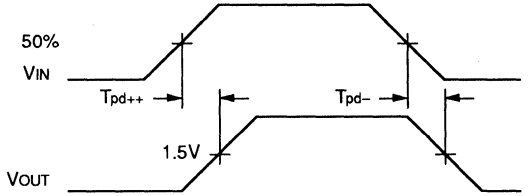
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	$V_E = 5.0V$
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	$V_E = 5.0V$

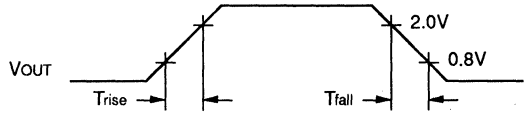
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H841ZC	Z16-1	Commercial	10KH
SY100H841ZC	Z16-1	Commercial	100K

SYNERGY SEMICONDUCTOR

SINGLE SUPPLY PECL-TTL 1:4 CLOCK DRIVER

ClockWorks™
PRELIMINARY
SY10/100H842

FEATURES

- **Translates positive ECL to TTL (PECL-TTL)**
- **300ps pin-to-pin skew**
- **Guaranteed skew spec**
- **Differential internal design for increased noise immunity and stable threshold inputs**
- **V_{BB} reference output**
- **Single supply**
- **Enable input**
- **Extra TTL and ECL power/ground pins to reduce cross-talk/noise**
- **High drive capability: 24mA each output**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10K, 100K I/O levels**

DESCRIPTION

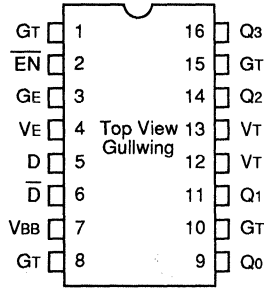
The SY10H842 and SY100H842 are single supply, low skew translating 1:4 clock drivers.

The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

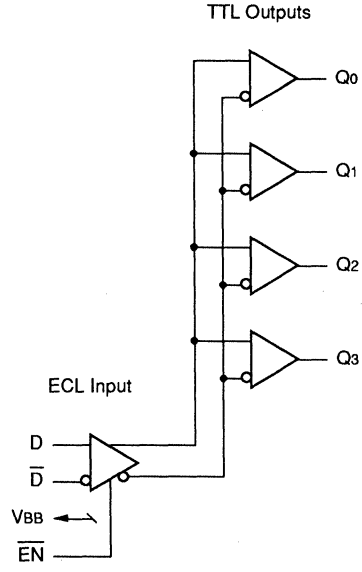
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H842 solves several clock distribution problems such as minimizing skew 300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output (positive ECL)
Q0 - Q3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)

Rev.: B Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	V
	V_{OUT} (TTL)	0.0 to V_T	
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	$\overline{EN}$	Q
L	L	L
H	L	H
X	H	L

PIN DESCRIPTION

Pin	Symbol	Description
1	G_T	TTL Ground (0V)
2	$\overline{EN}$	Enable Input Pos (ECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output Pos (ECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+5.0V)
13	V_T	TTL V_{CC} (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

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DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	35	—	35	—	35	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.5	3.5	2.5	3.5	2.5	3.5	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skwd++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skwd--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay $\overline{EN}$ to Output	Q_0–Q_3	2.5	3.5	2.5	3.5	2.5	3.5	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF

NOTES:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

V_{CC} AND C_{LOAD}

Ranges to meet duty cycle requirement: $0°C \le T_A \le 85°C$. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \le 40MHz$	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at $f_{OUT} \le 50MHz$	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	$I_{OH} = -3.0mA$ $I_{OH} = -15mA$
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	$I_{OL} = 24mA$
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	$V_{OUT} = 0V$

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

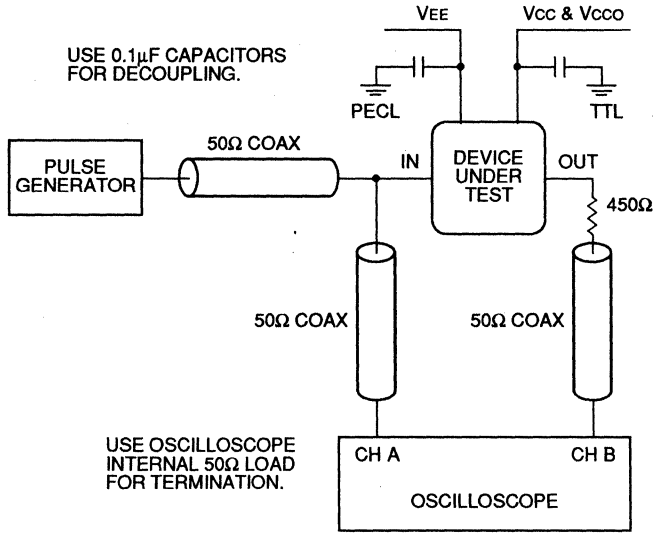
Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	$V_E = 5.0V$
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	$V_E = 5.0V$

100H ECL DC ELECTRICALCHARACTERISTICS

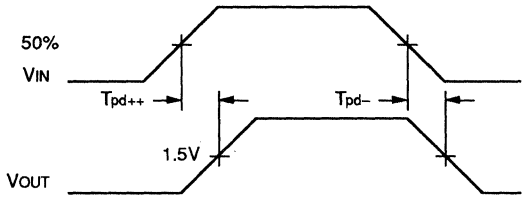
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	$V_E = 5.0V$
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	$V_E = 5.0V$

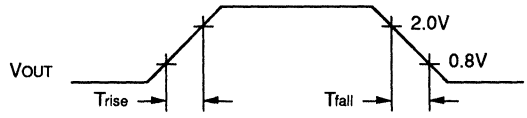
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H842ZC	Z16-1	Commercial	10KH
SY100H842ZC	Z16-1	Commercial	100K

FEATURES

- **Translates positive ECL to TTL (PECL-TTL)**
- **300ps pin-to-pin skew**
- **Guaranteed skew spec**
- **Differential internal design for increased noise immunity and stable threshold inputs**
- **VBB reference output**
- **Single supply**
- **Enable input**
- **Latch enable input**
- **Extra TTL and ECL power/ground pins to reduce cross-talk/noise**
- **High drive capability: 24mA each output**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10K, 100K I/O levels**

DESCRIPTION

The SY10H843 and SY100H843 are single supply, low skew translating 1:4 clock drivers.

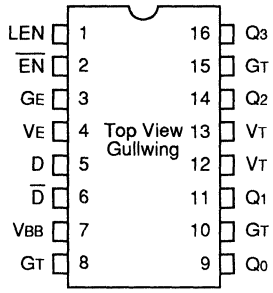
The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs), the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW after completion of the complete HIGH clock cycle. The outputs are kept HIGH by the Disable Timing Synchronizer until the HIGH input clock cycle is complete.

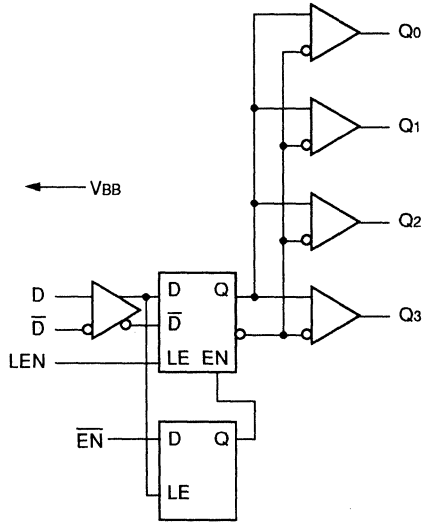
As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H843 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
D, $\overline{D}$	Signal Input (positive ECL)
VBB	VBB Reference Output (positive ECL)
Q0 - Q3	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (positive ECL)
LEN	Latch Enable Input

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Rev.: B Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_E (ECL)	–0.5 to +7.0	V
	V_T (TTL)	–0.5 to +7.0	
Input Voltage	V_I (ECL)	0.0 to V_{EE}	V
	V_{OUT} (TTL)	0.0 to V_T	
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0.0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	LEN	$\overline{EN}$	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	$\overline{EN}$	Enable Input Pos (ECL)
3	G_E	ECL Ground (0V)
4	V_E	ECL V_{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	$\overline{D}$	ECL Signal Input (Inverting)
7	V_{BB}	V_{BB} Reference Output Pos (ECL)
8	G_T	TTL Ground (0V)
9	Q_0	Signal Output (TTL)
10	G_T	TTL Ground (0V)
11	Q_1	Signal Output (TTL)
12	V_T	TTL V_{CC} (+5.0V)
13	V_T	TTL V_{CC} (+5.0V)
14	Q_2	Signal Output (TTL)
15	G_T	TTL Ground (0V)
16	Q_3	Signal Output (TTL)

DC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V_E Pin
I_{CCH}	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V_T pins
I_{CCL}			—	25	—	25	—	25		

AC CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1,4)	Q_0–Q_3	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_{skwd++}	Within-Device Skew(2,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{skwd--}	Within-Device Skew(3,4)	Q_0–Q_3	—	0.3	—	0.3	—	0.3	ns	C_L = 50pF
t_{PLH} t_{PHL}	Propagation Delay LEN to Q	Q_0–Q_3	2.7	3.7	2.7	3.7	2.7	3.7	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	Q_0–Q_3	—	1.5	—	1.5	—	1.5	ns	C_L = 50pF
f_{MAX}	Max. Input Frequency(5)	Q_0–Q_3	160	—	160	—	160	—	MHz	C_L = 50pF
—	Pulse Width	Q_0–Q_3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q_0–Q_3	1.0	—	1.0	—	1.0	—	ns	—
t_S	Set-up Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—
t_H	Hold Time D, $\overline{EN}$	Q_0–Q_3	0.75	—	0.75	—	0.75	—	ns	—

NOTES:

1. Device-to-Device Skew considering the same transitions at common Vcc level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
3. Within-Device Skew considering LOW-to-LOW transitions at common Vcc level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.

V_{CC} AND C_{LOAD}

Ranges to meet duty cycle requirement: 0°C ≤ T_A ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at f_{OUT} ≤ 40MHz	V_{CC} C_L P_W	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P_W	Ranges of V_{CC} and C_L to meet min. pulse width (HIGH or LOW) at f_{OUT} ≤ 50MHz	V_{CC} C_L P_W	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

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TTL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	–200	mA	V_{OUT} = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS

$V_T = V_E = 5.0V \pm 5\%$

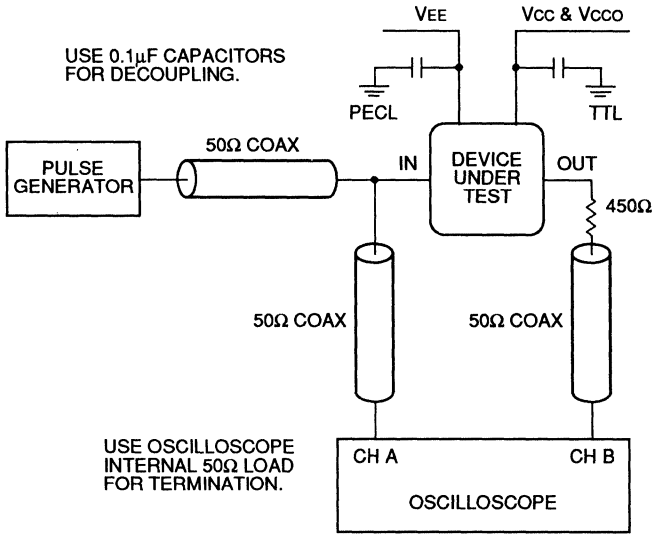
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	V_E = 5.0V

100H ECL DC ELECTRICALCHARACTERISTICS

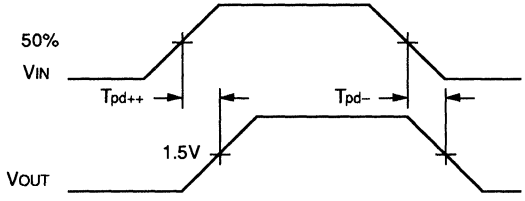
$V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current	— 0.5	225 —	— 0.5	175 —	— 0.5	175 —	µA	—
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	V_E = 5.0V
V_{BB}	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	V_E = 5.0V

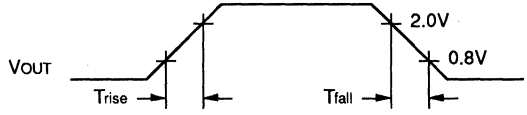
TTL SWITCHING CIRCUIT



ECL/TTL PROPAGATION DELAY — SINGLE ENDED



ECL/TTL WAVEFORMS: RISE AND FALL TIMES



PACKAGE ORDERING CODE

Ordering Code	Package Type	Operating Range	Interface
SY10H843ZC	Z16-1	Commercial	10KH
SY100H843ZC	Z16-1	Commercial	100K

10EL SERIES DC ELECTRICAL CHARACTERISTICS(1)

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND(2)

		–40°C		0°C		+25°C		+85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

NOTE:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

100EL SERIES DC ELECTRICAL CHARACTERISTICS(1)

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND(2)

		–40°C			0°C to +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620		or V_{IL} (Min.)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(Max.)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610		or V_{IL}(Min.)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	—
V_{IL}	Input LOW Voltage	–1810	—	–1475	–1810	—	–1475	mV	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(Max.)

NOTE:

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{OUT}	Output Current: Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}(2)	Operating Range	–5.7 to –4.2	V

NOTES:

1. Absolute maximum rating, beyond which device life may be imparied unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

Rev.: B Amendment: /0
Issue Date: April, 1994

DUAL TTL-TO-DIFFERENTIAL PECL TRANSLATOR

FEATURES

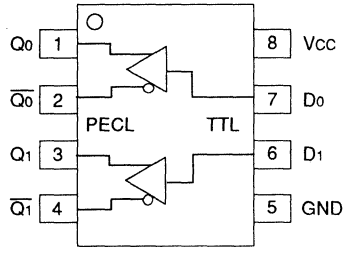
- 300ps typical propagation delay
- <100ps typical output-to-output skew
- ESD protection of 2000V
- Differential PECL outputs
- PNP TTL inputs for minimal loading
- Flow-through pinouts
- Small outline SOIC package

DESCRIPTION

The SY10ELT/100ELT22 are dual TTL-to-differential PECL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT22 makes it ideal for applications which require the tranlation of a clock and a data signal.

The ELT22 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
Q_n	Differential PECL Outputs
D_n	TTL Inputs
V_{CC}	+5.0V Supply
GND	Ground

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Rev.: B Amendment: /0
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ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
TTL Input Voltage[2]	V_I	–0.5 to 6.0	V
TTL Input Current[2]	I_I	–30 to +5.0	mA
ECL Output Current — Continuous — Surge	I_{OUT}	 50 100	mA
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect input.

TRUTH TABLE

D	Q	$\overline{Q}$
H	H	L
L	L	H
Open	H	L

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 5\%$

		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{CC}	Power Supply Current	—	25	—	25	—	25	mA	—

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 5\%$

		$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output D	100	600	100	600	100	600	ps	50Ω to (V_{CC} – 2.0V)
t_r t_f	Output Rise/Fall Time 20% to 80%	200	500	200	500	200	500	ps	50Ω to (V_{CC} – 2.0V)
t_{skpp}	Part-toPart Skew[1]	—	500	—	500	—	500	ps	50Ω to (V_{CC} – 2.0V)
t_{skwd}	Within-Device Skew[1],[2]	—	200	—	200	—	200	ps	50Ω to (V_{CC} – 2.0V)

NOTE:

1. Guaranteed, but not tested.
2. Same transition @ common Vcc Level.

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
V_{IL}	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	20 100	— —	20 100	— —	20 100	µA	V_{IN} = 2.7V V_{IN} = V_{CC}
I_{IL}	Input LOW Current	—	–0.2	—	–0.2	—	–0.2	mA	V_{IN} = 0.5V
V_{IK}	Input Clamp Voltage	—	–1.2	—	–1.2	—	–1.2	V	I_{IN} = –18mA

10EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	3980	4160	4020	4190	4090	4280	mV	—
V_{OL}	Output LOW Voltage	3050	3370	3050	3370	3050	3405	mV	—

100EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	3975	4120	3975	4120	3975	4120	mV	—
V_{OL}	Output LOW Voltage	3190	3380	3190	3380	3190	3380	mV	—

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PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10ELT22ZC	Z8-1	Commercial
SY100ELT22ZC	Z8-1	Commercial

DUAL DIFFERENTIAL PECL-TO-TTL TRANSLATOR

FEATURES

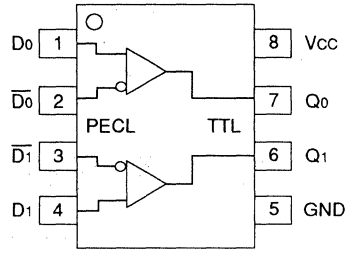
- 2.5ns typical propagation delay
- <300ps typical output-to-output skew
- ESD protection of 2000V
- Differential PECL inputs
- 24mA TTL outputs
- Flow-through pinouts
- Small outline SOIC package

DESCRIPTION

The SY10ELT/100ELT23 are dual differential PECL-to-TTL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
Q_n	TTL Outputs
D_n	Differential PECL Inputs
VCC	+5.0V Supply
GND	Ground

Rev.: B Amendment: /0
Issue Date: April, 1994

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
ECL Input Voltage	V_I	0 to V_{CC} + 0.5	V
Voltage Applied to Output at HIGH State	V_O	–0.5 to 5.5	V
Current Applied to Output at LOW State	I_O	Twice the Rated I_{OL}	mA
Storage Temperature	T_{store}	–65 to +150	°C
Operating Temperature	T_{amb}	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	$\overline{D}$	Q
L	H	L
H	L	H
Open	Open	L

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
I_{CC}	Power Supply Current	—	25	—	25	—	25	mA	—

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D to Output Q	2.0	3.0	2.0	3.0	2.0	3.0	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew[1]	—	1.0	—	1.0	—	1.0	ns	C_L = 50pF
t_{skwd}	Within-Device Skew[1],[2]	—	0.5	—	0.5	—	0.5	ns	C_L = 50pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	0.5	1.0	0.5	1.0	0.5	1.0	ns	C_L = 50pF

NOTE:

1. Guaranteed, but not tested.
2. Same transition @ common Vcc Level.

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TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{OS}	Output Short Circuit Current	–60	–150	–60	–150	–60	–150	mA	V_{OUT} = 0V

10EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—		
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.94	4.28	V	—
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.555		

100EL PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	225	—	175	—	175	µA	—
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—		
V_{IH}	Input HIGH Voltage	3.835	4.12	3.835	4.12	3.835	4.12	V	—
V_{IL}	Input LOW Voltage	3.19	3.525	3.19	3.525	3.19	3.525		

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10ELT23ZC	Z8-1	Commercial
SY100ELT23ZC	Z8-1	Commercial

DC characteristics for the 100K parametric limits listed below are guaranteed for the entire *SUPER-300K* family **unless specified on the individual data sheet.**

The specified DC limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

GUARANTEED OPERATING CONDITIONS(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{EE}	Supply Voltage	–4.8	–4.5	–4.2	V
T_A	Operating Temperature	0	25	85	°C

NOTE:

1. Referenced to Vcc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{EE}	V_{EE} Pin Potential to Ground Pin	+0.5 to –7.0	V
V_{IN}	Input Voltage	+0.5 to V_{EE}	V
I_{OUT}	DC Output Current (Output HIGH)	–50	mA
T_C	Temperature Under Bias	–55 to +125	°C
T_j	Junction Temperature	+150	°C
T_{store}	Storage Temperature	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V, Output Load = 50Ω to –2.0V, V_{EE} = –4.5V, T_A = 0°C to 85°C

Symbol	Parameter	V_{EE}	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–4.2V	–1020	—	–870	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
		–4.5V	–1025	–955	–880		
		–5.46V	–1035	—	–880		
V_{OL}	Output LOW Voltage	–4.2V	–1810	—	–1605	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
		–4.5V	–1810	–1705	–1620		
		–5.46V	–1830	—	–1620		
V_{OHC}	Output HIGH Voltage	–4.2V	–1030	—	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
		–4.5V	–1035	—	—		
		–5.46V	–1045	—	—		
V_{OLC}	Output LOW Voltage	–4.2V	—	—	–1595	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
		–4.5V	—	—	–1610		
		–5.46V	—	—	–1610		
V_{IH}	Input HIGH Voltage	–4.2V	–1150	—	–870	mV	Guaranteed Input Voltage HIGH for All Inputs
		–4.5V	–1165	—	–880		
		–5.46V	–1165	—	–880		
V_{IL}	Input LOW Voltage	–4.2V	–1810	—	–1475	mV	Guaranteed Input Voltage LOW for All Inputs
		–4.5V	–1810	—	–1475		
		–5.46V	–1830	—	–1490		
I_{IL}	Input LOW Current	–4.5V	+0.5	—	—	µA	V_{IN} = V_{IL} Min.

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LOW POWER HEX TTL-to-ECL TRANSLATOR

FEATURES

- Max. propagation delay of 1.4ns
- IEE min. of –70mA
- ESD protection of 2000V
- Industry standard 100K ECL levels
- Extended supply voltage option:
  — VEE = –4.2V to –5.46V
- Differential outputs
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- Twice as fast as National's 324
- Function and pinout compatible with National and Signetics F100K
- Available in CERDIP, CERPACK and PLCC

DESCRIPTION

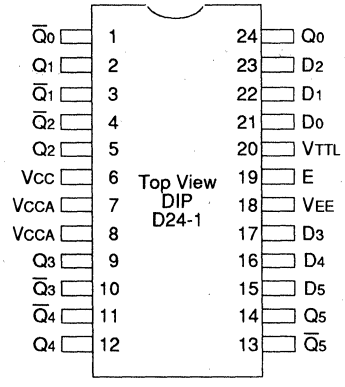
The SY100S324 is a hex translator designed to convert TTL logic levels to 100K ECL levels. The inputs are TTL compatible with differential outputs that can either be used as an inverting/non-inverting translator or as differential line drivers. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all non-inverting outputs LOW.

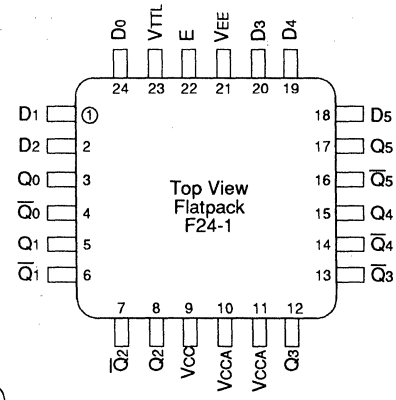
When used in the differential mode, due to its high common mode rejection, it overcomes voltage gradients between the TTL and ECL ground systems. The VEE and VTTL power may be applied in either order.

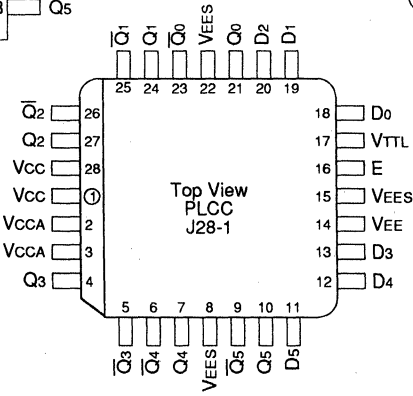
PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
E	Enable Inputs
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

PIN CONFIGURATIONS







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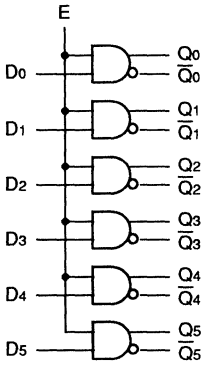
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.46V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Sim.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–986	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with 50Ω
V_{OL}	Output LOW Voltage	–1810	–1674	–1620	mV	V_{IN} = V_{IL} (Min.)	
V_{OHC}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage	—	—	–1610	mV	V_{IN} = V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0	—	0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	–1.5	—	—	V	I_{IN} = –10mA	
I_{IH}	Input HIGH Current Data Enable	 — —	 — —	 20 120	µA	 V_{IN} = +2.4V All Other Inputs V_{IN} = GND	
I_{IH}	Input HIGH Current Breakdown Test, All Inputs	—	—	1.0	mA	V_{IN} = +5.5V, V_{TTL} = Max., All Other Inputs V_{IN} = GND	
I_{IL}	Input LOW Current Data Enable	 –1.2 –6.7	 — —	 — —	mA	 V_{IN} = +0.4V All Other Inputs V_{IN} = V_{IH}	
I_{EE}	V_{EE} Power Supply Current	–70	–45	–28	mA	All Inputs V_{IN} = +4.0V	
I_{TTL}	V_{TTL} Power Supply Current	—	25	35	mA	All Inputs V_{IN} = GND	

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AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = −4.2V to −5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	500	950	1500	ps	See Switching Wave Form Figures
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	450	—	1800	ps	

PLCC /FLATPACK

V_{EE} = −4.2V to −5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	400	850	1400	ps	See Switching Wave Form Figures
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	350	—	1700	ps	

SWITCHING WAVEFORM

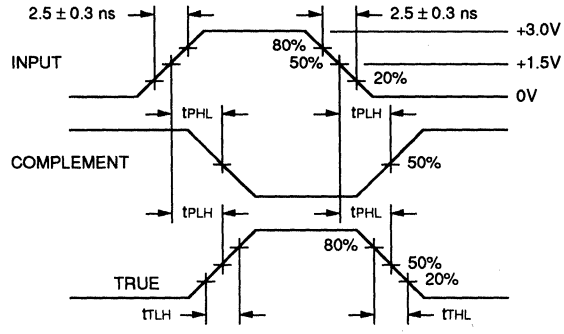

Figure 1. Propagation Delay and Transition Times

TEST CIRCUIT

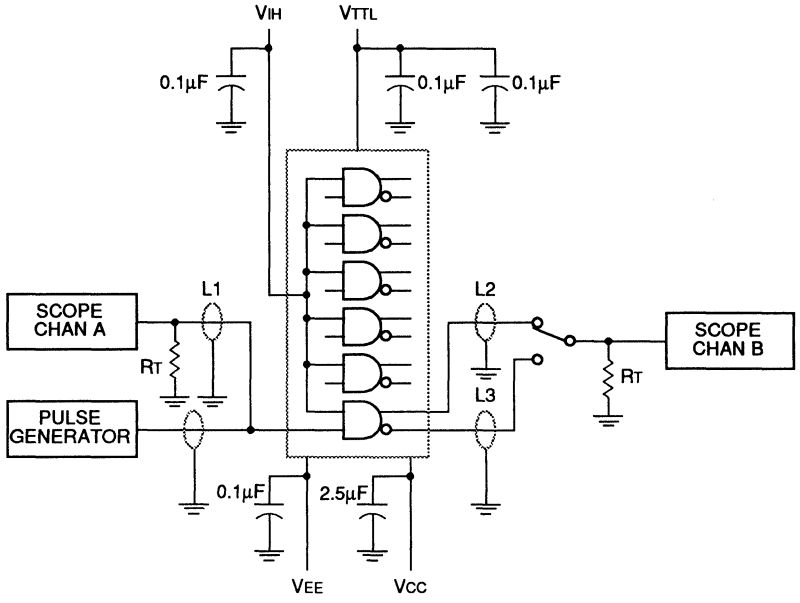

Figure 2. AC Test Circuit

NOTES:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V, V_{TTL} = +7.0V, V_{IH} = +6.0V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3pF

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PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S324DC	D24-1	Commercial
SY100S324FC	F24-1	Commercial
SY100S324JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

LOW-POWER HEX ECL-to-TTL TRANSLATOR

SY100S325

FEATURES

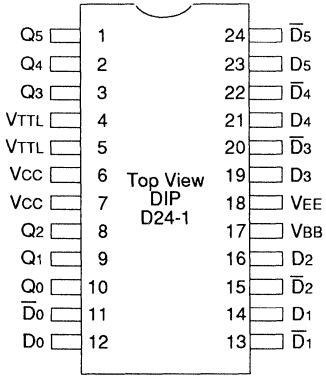
- **Max. propagation delay of 3.7ns**
- **IEE min. of –37mA**
- **ESD protection of 2000V**
- **TTL outputs**
- **Extended supply voltage option:**
  — **VEE = –4.2V to –5.46V**
- **25% faster than National's 325**
- **Differential inputs with built-in offset**
- **Voltage and temperature compensation for improved noise immunity**
- **VBB output for single-ended use**
- **Internal 75KΩ input pull-down resistors**
- **Function and pinout compatible with National and Signetics (F100K)**
- **Available in CERDIP, CERPACK and PLCC**

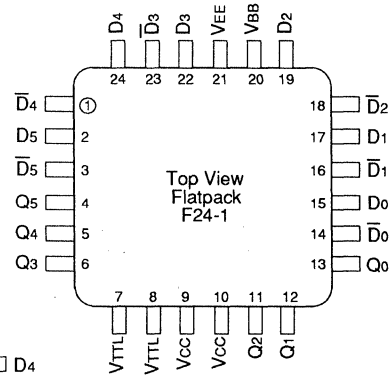
DESCRIPTION

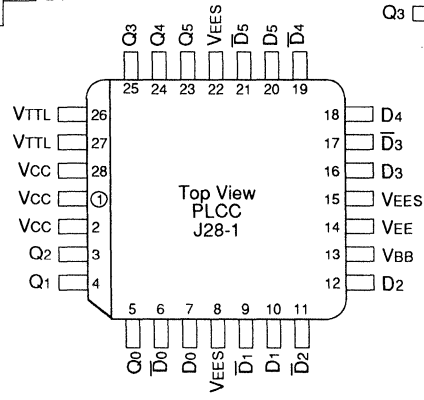
The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 75KΩ pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The VTTL and VEE power may be applied in either order.

PIN CONFIGURATIONS





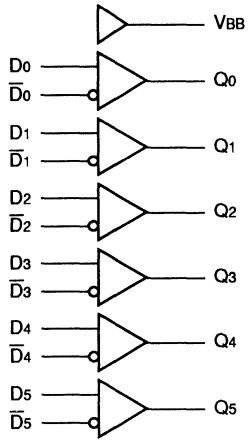


PIN NAMES

Pin	Function
D0–D5	Data Inputs
D̄0–D̄5	Inverting Data Inputs
Q0–Q5	Data Outputs

Rev.: B Amendment: /0
Issue Date: April, 1994

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	2.5	—	—	V	I_{OH} = –2.0mA	V_{IN} = V_{IH} (Max.)
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 24mA	V_{IN} = V_{IL} (Min.)
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible ±V_{CM} with Respect to V_{BB}	
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.), D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = V_{IL} (Min.)	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IH} (Min.), D_0–D_5 = V_{BB}	
I_{OS}	Output Short Circuit Current	–150	–80	–60	mA	V_{OUT} = GND	
I_{EE}	V_{EE} Power Supply Current	–37	–24	–17	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current	—	42	65	mA	D_0–D_5 = V_{BB}	
V_{BB}	Ouptut Reference Voltage	–1380	–1320	–1260	mV	I_{VBB} = –2.1mA	
V_{IH}	Single-Ended Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to V_{BB})	

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AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0	2.2	3.0	ns	C_L = 15pF, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0	3.2	3.8	ns	C_L = 50pF, Figure 2

PLCC/FLATPACK

V_{EE} = –4.2V to –5.6V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	2100	2900	ps	C_L = 15pF, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	3100	3700	ps	C_L = 50pF, Figure 2

SWITCHING WAVEFORM

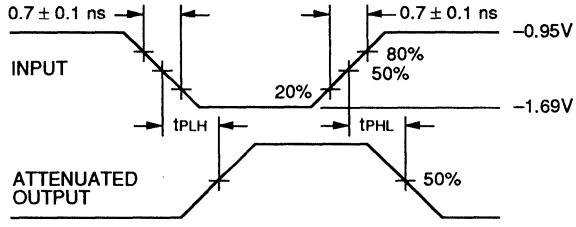


Figure 1. Propagation Delay

TEST CIRCUITS

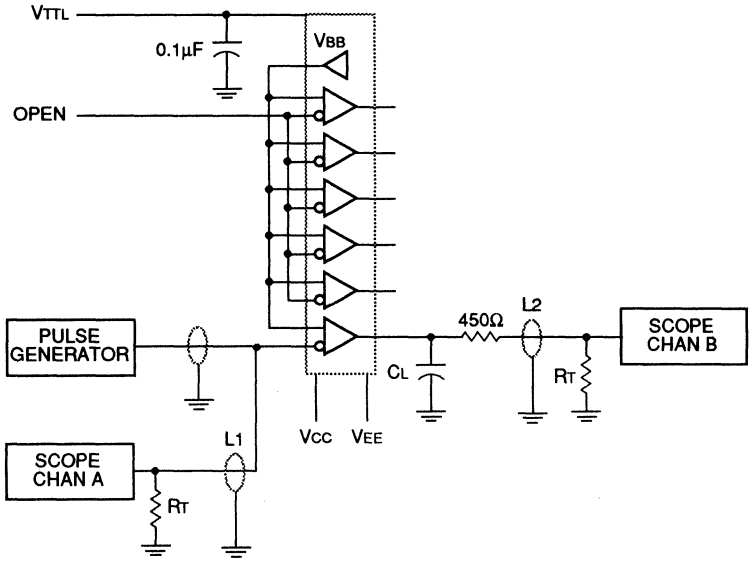


Figure 2. AC Test Circuit for 15pF Loading

NOTES:
V_{CC} = 0V, V_{EE} = –4.5V, V_{TTL} = +5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 3pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S325DC	D24-1	Commercial
SY100S325FC	F24-1	Commercial
SY100S325JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

LOW-POWER OCTAL ECL/TTL BI-DIRECTIONAL TRANSLATOR WITH LATCH

PRELIMINARY
SY100S328

FEATURES

- **Bi-directional translation**
- **ESD protection of 2000V**
- **Latched outputs**
- **Voltage compensated operating range: –4.2V to –5.7V**
- **Fast TTL outputs**
- **Three-state outputs**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

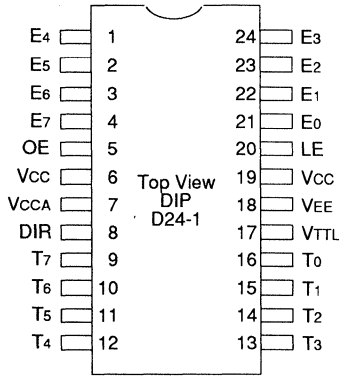
DESCRIPTION

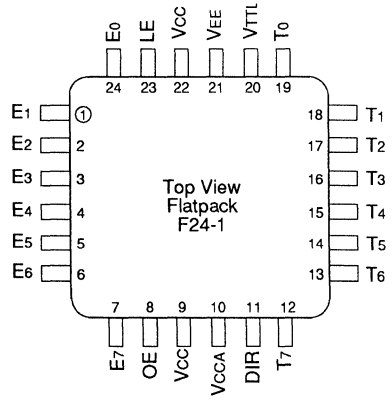
The SY100S328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the SY100S328 transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The SY100S328 is designed with fast TTL output buffers featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have internal 75KΩ pull-down resistors.

PIN CONFIGURATIONS



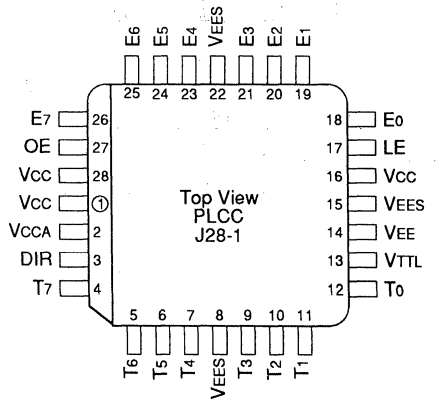


PIN NAMES[1]

Pin	Function
E0–E7	ECL Data I/O
T0–T7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

NOTE:

1. All pins function at 100K ECL levels except for T0–T7.



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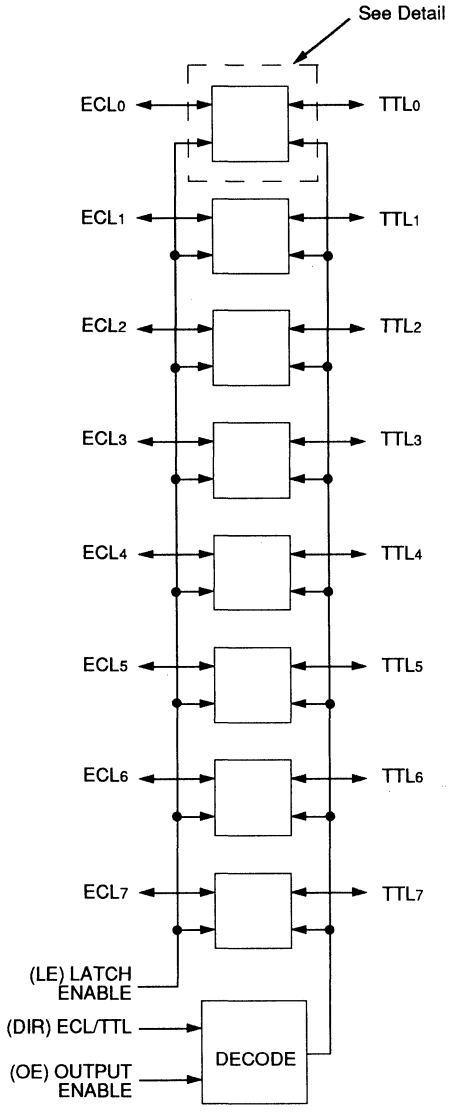
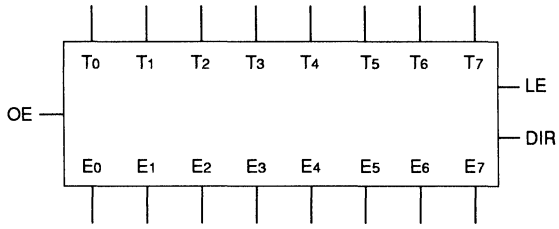
Issue Date: April, 1994

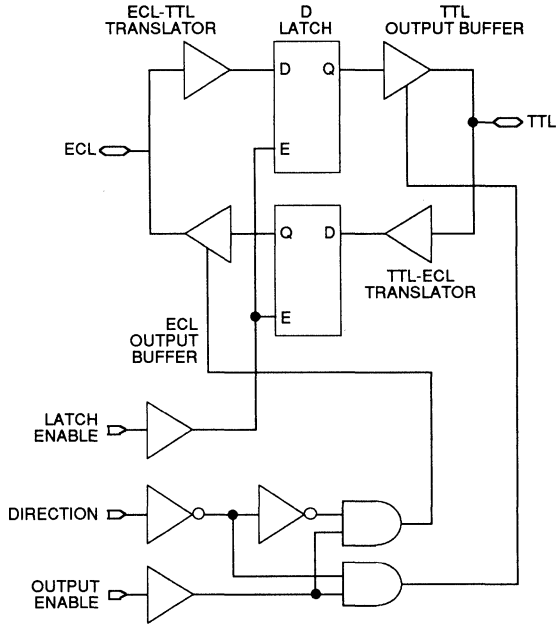
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



DETAIL



NOTE:

1. LE, DIR and OE use ECL logic levels.

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TRUTH TABLE[1]

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	—
L	L	H	Input	Z	2, 4
L	H	H	LOW (Cut-Off)	Input	3, 4
H	L	L	L	L	2, 5
H	L	L	H	H	2, 5
H	L	H	X	Latched	2, 4
H	H	L	L	L	3, 5
H	H	L	H	H	3, 5
H	H	H	Latched	X	3, 4

NOTES:

1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = High Impedance.
2. ECL input to TTL output mode.
3. TTL input to ECL output mode.
4. Retains data present before LE is set HIGH.
5. Latch is transparent.

GUARANTEED OPERATING CONDITIONS

Symbol	Rating	Value	Unit
V_{EE}	ECL Supply Voltage	–5.7 to –4.2	V
V_{TTL}	TTL Supply Voltage	+4.5 to +5.5	V
T_C	Case Temperature	0 to +85	°C

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_J	Maximum Junction Temperature Ceramic Plastic	 +175 +150	°C
V_{EE}	V_{EE} Pin Potential to Ground Pin	–7.0 to +0.5	V
V_{TTL}	V_{TTL} Pin Potential to Ground Pin	–0.5 to +6.0	V
—	ECL Input Voltage (DC)	V_{EE} to +0.5	V
—	ECL Output Current (DC Output HIGH)	–50	mA
—	TTL Input Voltage[2]	–0.5 to +6.0	V
—	TTL Input Current[2]	–30 to +5.0	mA
—	Voltage Applied to Output in HIGH State (Three-state Output)	–0.5 to +5.5	V
—	Current Applied to TTL Output in LOW State (Max.)	Twice the Rated I_{OL}	mA

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

TTL-TO-ECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1025	–955	–870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	–1830	–1705	–1620	mV	Loading with 50Ω to –2V
	Cutoff Voltage	—	–2000	–1950	mV	OE or DIR Low, V_{IN} = V_{IH} (Max.) or V_{IL} (Min.), Loading with 50Ω to –2V
V_{OHC}	Output HIGH Voltage Corner Point High	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	–1610	mV	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current	—	—	70	µA	V_{IN} = +2.7V
	Breakdown Test	—	—	1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	–700	—	—	µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{EE}	V_{EE} Supply Current	 –159 –169	 — —	 –75 –75	mA	LE Low, OE and DIR High, Inputs Open V_{EE} = –4.2V to –4.8V V_{EE} = –4.2V to –5.7V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

ECL-TO-TTL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50pF, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9	— —	V	I_{OH} = –3mA, V_{TTL} = 4.75V I_{OH} = –3mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	I_{OL} = 24mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	–1165	—	–870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	–1830	—	–1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	V_{IN} = V_{IL} (Min.)
I_{OZHT}	Three-State Current Output High	—	—	70	µA	V_{OUT} = +2.7V
I_{OZLT}	Three-State Current Output Low	–700	—	—	µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	–150	—	–60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current	—	—	74	mA	V_{TTL} = +5.5V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Tn to En (Transparent)	1.1	3.5	1.1	3.6	1.1	3.8	ns	Figures 1 & 2
tPLH tPHL	LE to En	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1 & 2
tPZH	OE to En (Cutoff to High)	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1 & 2
tPHZ	OE to En (High to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1 & 2
tPHZ	DIR to En (High to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1 & 2
tset	Tn to LE	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
thold	Tn to LE	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
tpw(H)	Pulse Width LE	2.1	—	2.1	—	2.1	—	ns	Figures 1 & 2
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, C_L = 50pF[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	En to Tn (Transparent)	2.3	5.6	2.4	5.6	2.6	5.9	ns	Figures 3 & 4
tPLH tPHL	LE to Tn	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3 & 4
tPZH tPZL	OE to Tn (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	Figures 3 & 4
tPHZ tPLZ	OE to Tn (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	Figures 3 & 4
tPHZ tPLZ	DIR to Tn (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	Figures 3 & 4
tset	En to LE	1.1	—	1.1	—	1.1	—	ns	Figures 3 & 4
thold	En to LE	2.1	—	2.1	—	2.6	—	ns	Figures 3 & 4
tPW (H)	En to LE	4.1	—	4.1	—	4.1	—	ns	Figures 3 & 4

NOTE:

1. The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

PLCC and FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V

		Tc = 0°C		Tc = +25°C		Tc = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.1	3.3	1.1	3.4	1.1	3.6	ns	Figures 1 & 2
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns	Figures 1 & 2
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.0	1.5	4.2	1.7	4.6	ns	Figures 1 & 2
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	Figures 1 & 2
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	Figures 1 & 2
t_{set}	T_n to LE	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{hold}	T_n to LE	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{pw} (H)	Pulse Width LE	2.0	—	2.0	—	2.0	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	PLCC Only(1)
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	PLCC Only(1)
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	650	—	650	—	650	ps	PLCC Only(1)
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	650	—	650	—	650	ps	PLCC Only(1)

NOTE:

1. Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction — either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) — or in opposite directions, both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} are guaranteed by design.

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ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

PLCC and FLATPACK

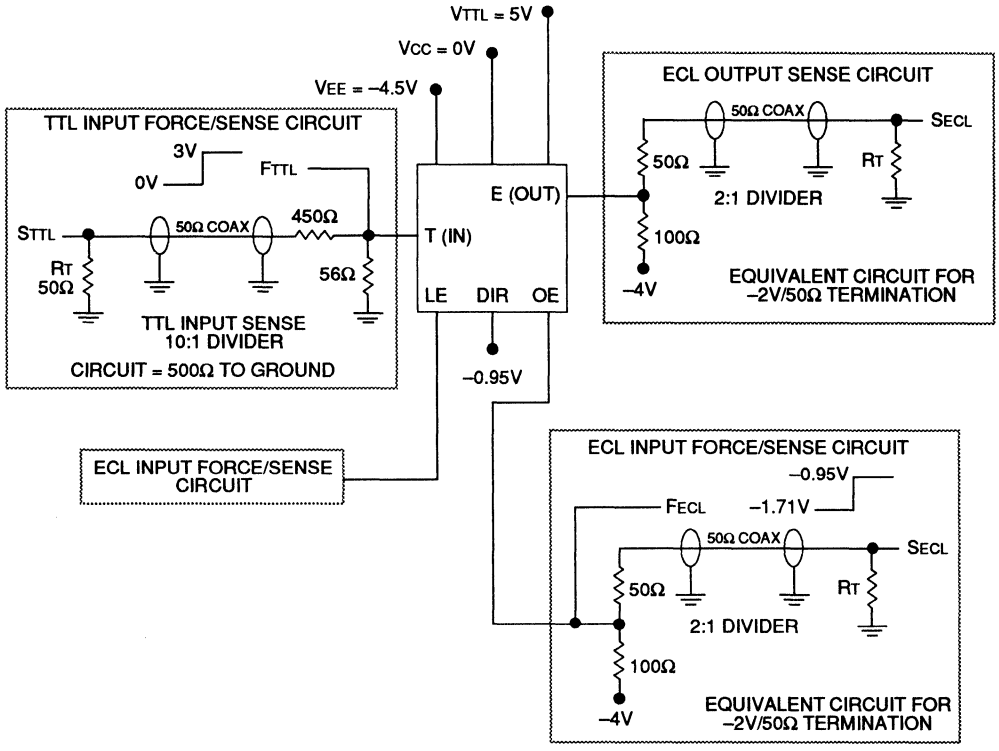
V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50pF

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	Figures 3 & 4
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	7.0	3.3	7.5	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	Figures 3 & 6
t_{set}	E_n to LE	1.0	—	1.0	—	1.0	—	ns	Figures 3 & 4
t_{hold}	E_n to LE	2.0	—	2.0	—	2.5	—	ns	Figures 3 & 4
t_{pw} (H)	Pulse Width LE	4.0	—	4.0	—	4.0	—	ns	Figures 3 & 4
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	600	—	600	—	600	ps	PLCC Only(1)
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	850	—	850	—	850	ps	PLCC Only(1)
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	1350	—	1350	—	1350	ps	PLCC Only(1)
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	950	—	950	—	950	ps	PLCC Only(1)

NOTE:

1. Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction — either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) — or in opposite directions, both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} are guaranteed by design.

TEST CIRCUITRY (TTL-TO-ECL)



NOTES:

1. Rt = 50Ω termination. When an input or output is being monitored by a scope, Rt is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as Rt.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. VTTL is decoupled to ground with a 0.1μF capacitor, VEE is decoupled to ground with a 0.01μF capacitor and VCC is connected to ground.
4. For ECL input pins, the equivalent force/sense circuitry is optional.

Figure 1. TTL-to-ECL AC Test Circuit

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SWITCHING WAVEFORMS (TTL-TO-ECL)

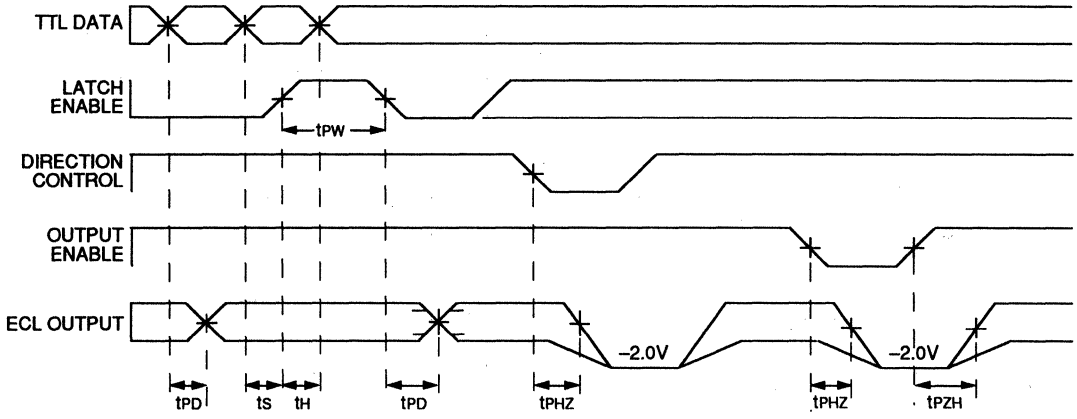
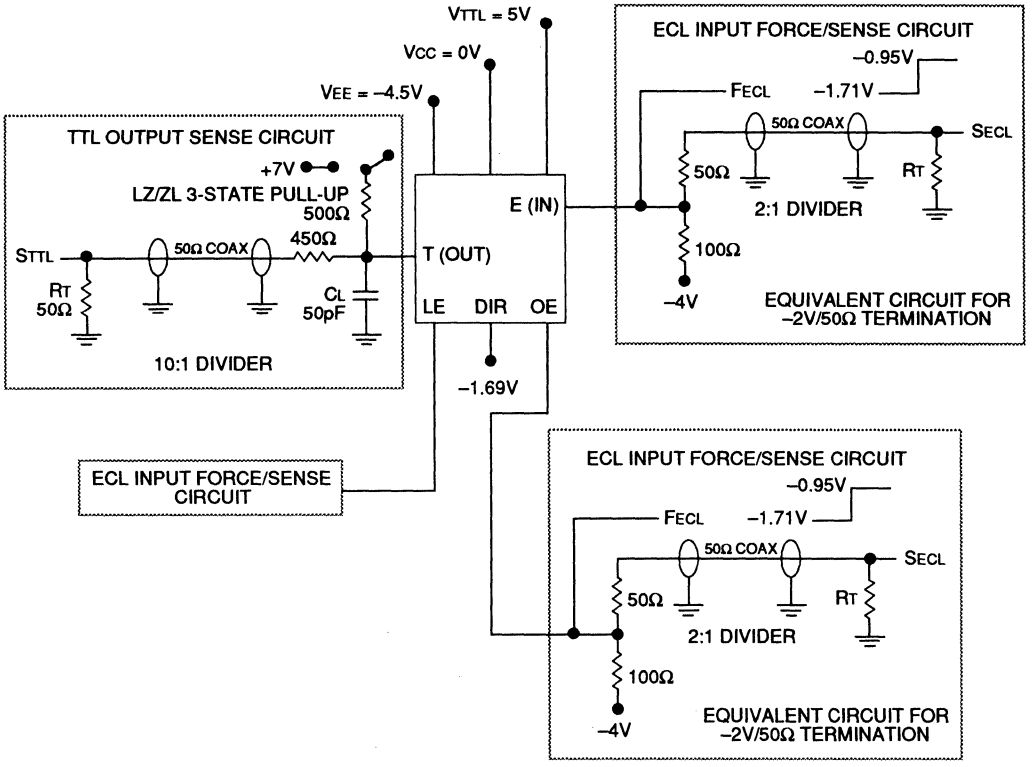


Figure 2. TTL-to-ECL Transition — Propagation Delay and Transition Times

TEST CIRCUITRY (ECL-TO-TTL)



NOTES;

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. The TTL three-state pull-up switch is connected to +7V only for ZL and LZ tests.

Figure 3. ECL-to-TTL AC Test Circuit

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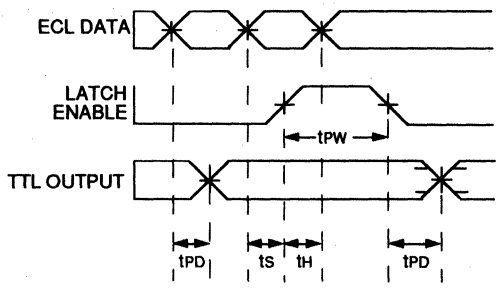
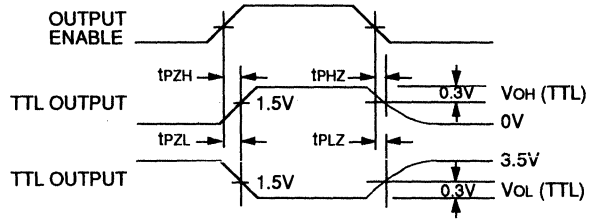
SWITCHING WAVEFORMS (ECL-TO-TTL)



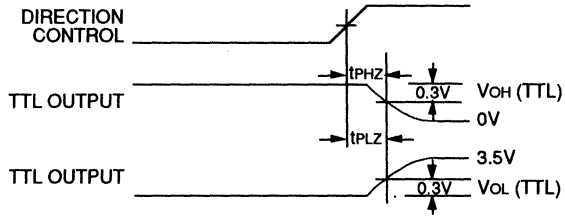
NOTE:
1. DIR is LOW and OE is HIGH.

Figure 4. ECL-to-TTL Transition, Propagation Delay and Transition Times



NOTE:
1. DIR is LOW and LE is HIGH.

Figure 5. ECL-to-TTL Transition, OE to TTL Output Enable and Disable Times



NOTE:
1. OE is HIGH and LE is HIGH.

Figure 6. ECL-to-TTL Transition, DIR to TTL Output Disable Time

APPLICATIONS

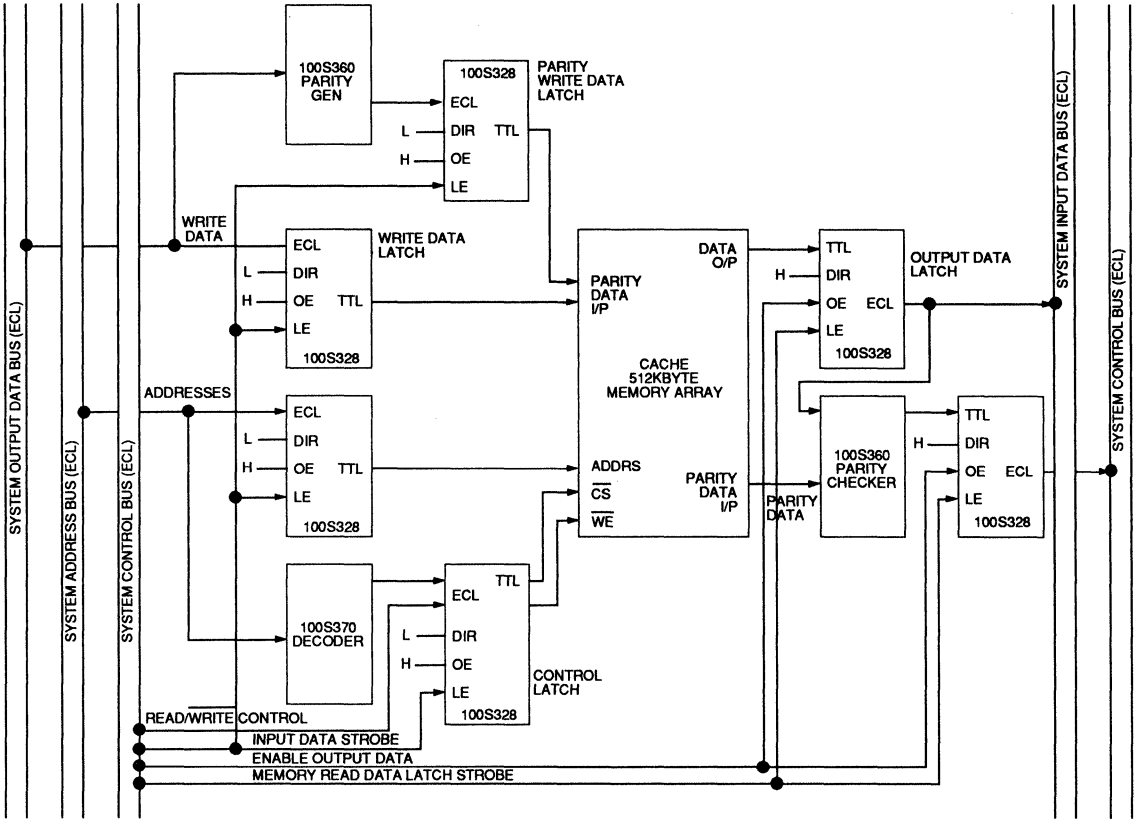


Figure 7. Applications Diagram — MOS/TTL SRAM Interface Using SY100S328 ECL-TTL Latched Translator

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S282DC	D24-1	Commercial
SY100S328FC	F24-1	Commercial
SY100S328JC	J28-1	Commercial

SYNERGY SEMICONDUCTOR

LOW-POWER OCTAL ECL/TTL BI-DIRECTIONAL TRANSLATOR WITH REGISTER

PRELIMINARY
SY100S329

FEATURES

- **Bi-directional translation**
- **ESD protection of 2000V**
- **ECL high impedance outputs**
- **Registered outputs**
- **Voltage compensated operating range: –4.2V to –5.7V**
- **Fast TTL outputs**
- **Three-state outputs**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP and CERPACK**

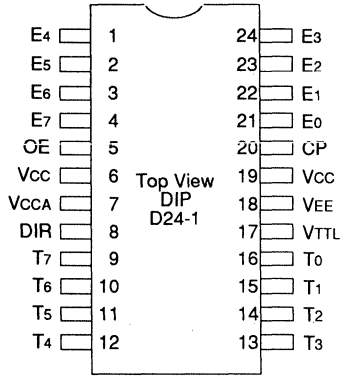
DESCRIPTION

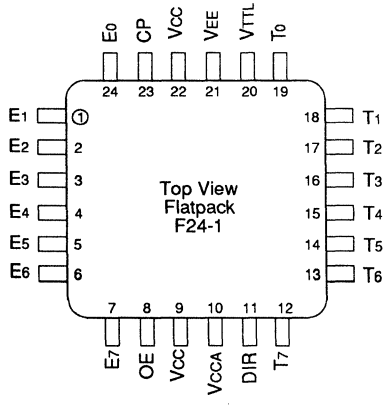
The SY100S329 is an octal registered bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The SY100S329 is designed with fast TTL output buffers featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have internal 75KΩ pull-down resistors.

PIN CONFIGURATIONS





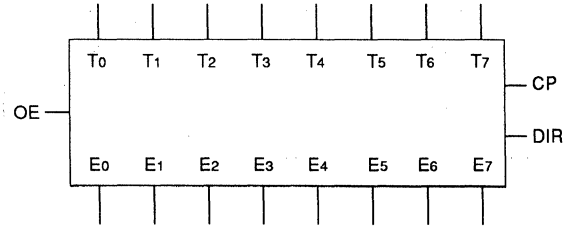
PIN NAMES[1]

Pin	Function
E0–E7	ECL Data I/O
T0–T7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

NOTE:

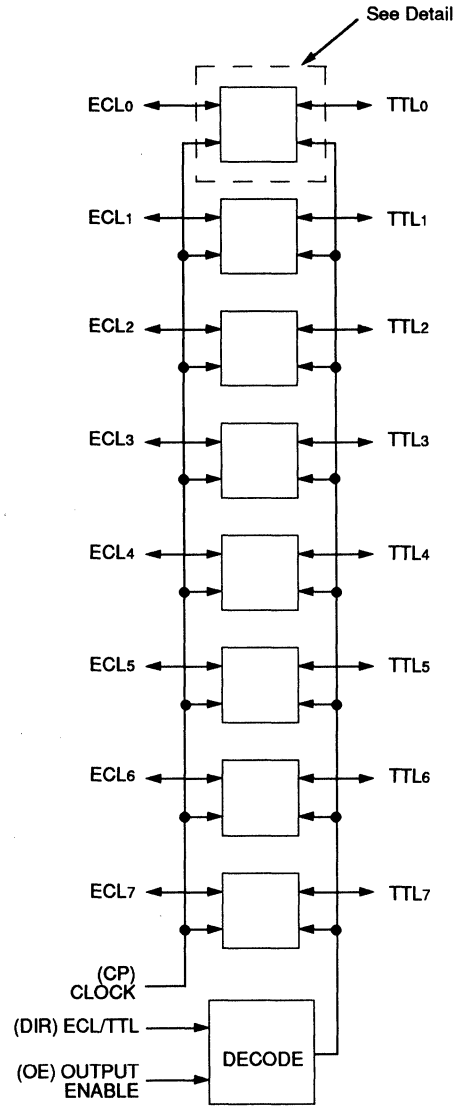
1. All pins function at 100K ECL levels except for T0–T7.

LOGIC SYMBOL

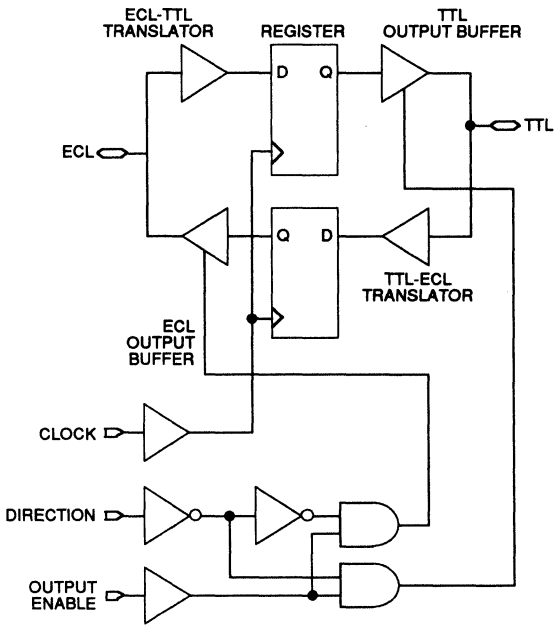


Rev.: B Amendment: /0
Issue Date: April, 1994

FUNCTIONAL BLOCK DIAGRAM



DETAIL



NOTE:

1. CP, DIR and OE use ECL logic levels.

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TRUTH TABLE[1]

OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	2, 4
L	H	X	LOW (Cut-Off)	Input	3, 4
H	L	∫	L	L	2
H	L	∫	H	H	2
H	L	L	X	NC	2, 4
H	H	∫	L	L	3
H	H	∫	H	H	3
H	H	L	NC	X	3, 4

NOTES:
1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = High Impedance.
2. ECL input to TTL output mode.
3. TTL input to ECL output mode.
4. Retains data present before CP.

GUARANTEED OPERATING CONDITIONS

Symbol	Rating	Value	Unit
V_{EE}	ECL Supply Voltage	–5.7 to –4.2	V
V_{TTL}	TTL Supply Voltage	+4.5 to +5.5	V
T_C	Case Temperature	0 to +85	°C

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_J	Maximum Junction Temperature Ceramic Plastic	 +175 +150	°C
V_{EE}	V_{EE} Pin Potential to Ground Pin	–7.0 to +0.5	V
V_{TTL}	V_{TTL} Pin Potential to Ground Pin	–0.5 to +6.0	V
—	ECL Input Voltage (DC)	V_{EE} to +0.5	V
—	ECL Output Current (DC Output HIGH)	–50	mA
—	TTL Input Voltage[2]	–0.5 to +6.0	V
—	TTL Input Current[2]	–30 to +5.0	mA
—	Voltage Applied to Output in HIGH State (Three-state Output)	–0.5 to +5.5	V
—	Current Applied to TTL Output in LOW State (Max.)	Twice the Rated I_{OL}	mA

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

TTL-TO-ECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	–1025	–955	–870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	–1830	–1705	–1620	mV	Loading with 50Ω to –2V
	Cutoff Voltage	—	–2000	–1950	mV	OE or DIR Low, V_{IN} = V_{IH} (Max.) or V_{IL} (Min.), Loading with 50Ω to –2V
V_{OHC}	Output HIGH Voltage Corner Point High	–1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	–1610	mV	
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current	—	—	70	µA	V_{IN} = +2.7V
	Breakdown Test	—	—	1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	–700	—	—	µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{EE}	V_{EE} Supply Current	 –189 –199	 — —	 –94 –94	mA	LE Low, OE and DIR High, Inputs Open V_{EE} = –4.2V to –4.8V V_{EE} = –4.2V to –5.7V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

ECL-TO-TTL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50pF, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9	— —	V	I_{OH} = –3mA, V_{TTL} = 4.75V I_{OH} = –3mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage	—	0.3	0.5	V	I_{OL} = 24mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	–1165	—	–870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	–1830	—	–1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.)
I_{IL}	Input LOW Current	0.50	—	—	µA	V_{IN} = V_{IL} (Min.)
I_{OZHT}	Three-State Current Output High	—	—	70	µA	V_{OUT} = +2.7V
I_{OZLT}	Three-State Current Output Low	–700	—	—	µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	–150	—	–60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current	—	—	74	mA	V_{TTL} = +5.5V

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	350	—	350	—	350	—	MHz	—
t_{PLH} t_{PHL}	CP to En	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1 & 2
t_{PZH}	OE to En (Cutoff to HIGH)	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1 & 2
t_{PHZ}	OE to En (HIGH to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1 & 2
t_{PHZ}	DIR to En (HIGH to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1 & 2
t_{set}	Tn to CP	1.1	—	1.1	—	1.1	—	ns	Figures 1 & 2
t_{hold}	Tn to CP	1.7	—	1.7	—	1.9	—	ns	Figures 1 & 2
t_{pw}(H)	Pulse Width CP	2.1	—	2.1	—	2.1	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2

ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, C_L = 50pF[1]

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	125	—	125	—	125	—	MHz	—
t_{PLH} t_{PHL}	CP to Tn	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	Figures 3 & 6
t_{set}	En to CP	1.1	—	1.1	—	1.1	—	ns	Figures 3 & 4
t_{hold}	En to CP	2.1	—	2.1	—	2.6	—	ns	Figures 3 & 4
t_{PW} (H)	Pulse Width CP	4.1	—	4.1	—	4.1	—	ns	Figures 3 & 4

NOTE:

1. The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

TTL-TO-ECL AC ELECTRICAL CHARACTERISTICS

FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	350	—	350	—	350	—	MHz	—
t_{PLH} t_{PHL}	CP to En	1.7	3.4	1.7	3.5	1.9	3.7	ns	Figures 1 & 2
t_{PZH}	OE to En (Cutoff to HIGH)	1.3	4.0	1.5	4.2	1.7	4.6	ns	Figures 1 & 2
t_{PHZ}	OE to En (HIGH to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	Figures 1 & 2
t_{PHZ}	DIR to En (HIGH to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	Figures 1 & 2
t_{set}	Tn to CP	1.0	—	1.0	—	1.0	—	ns	Figures 1 & 2
t_{hold}	Tn to CP	1.7	—	1.7	—	1.7	—	ns	Figures 1 & 2
t_{pw} (H)	Pulse Width CP	2.0	—	2.0	—	2.0	—	ns	Figures 1 & 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1 & 2
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	—
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	200	—	200	—	200	ps	—
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	650	—	650	—	650	ps	—
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	650	—	650	—	650	ps	—

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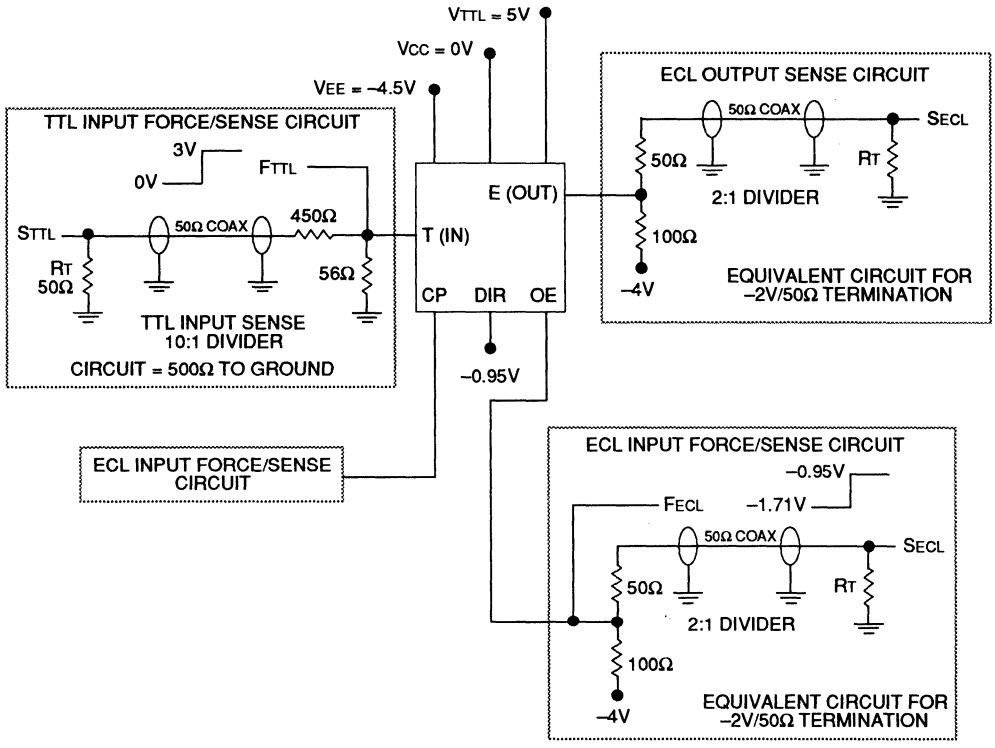
ECL-TO-TTL AC ELECTRICAL CHARACTERISTICS

FLATPACK

V_{EE} = –4.2V to –5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50pF

Symbol	Parameter	Tc = 0°C		Tc = +25°C		Tc = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	Maximum Toggle Frequency	125	—	125	—	125	—	MHz	—
t_{PLH} t_{PHL}	CP to Tn	3.1	7.0	3.1	7.0	3.3	7.5	ns	Figures 3 & 4
t_{PZH} t_{PZL}	OE to Tn (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	OE to Tn (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	Figures 3 & 5
t_{PHZ} t_{PLZ}	DIR to Tn (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	Figures 3 & 6
t_{set}	En to CP	1.0	—	1.0	—	1.0	—	ns	Figures 3 & 4
t_{hold}	En to CP	2.0	—	2.0	—	2.5	—	ns	Figures 3 & 4
t_{pw} (H)	Pulse Width CP	4.0	—	4.0	—	4.0	—	ns	Figures 3 & 4
t_{OSHL}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	600	—	600	—	600	ps	—
t_{OSLH}	Max. Skew Common Edge Output-to-Output Variation Data to Output Path	—	850	—	850	—	850	ps	—
t_{OST}	Max. Skew Opposite Edge Output-to-Output Variation Data to Output Path	—	1350	—	1350	—	1350	ps	—
t_{ps}	Max. Skew Pin (Signal) Transition Variation Data to Output Path	—	950	—	950	—	950	ps	—

TEST CIRCUITRY (TTL-TO-ECL)



NOTES:

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. For ECL input pins, the equivalent force/sense circuitry is optional.

Figure 1. TTL-to-ECL AC Test Circuit

7

SWITCHING WAVEFORMS (TTL-TO-ECL)

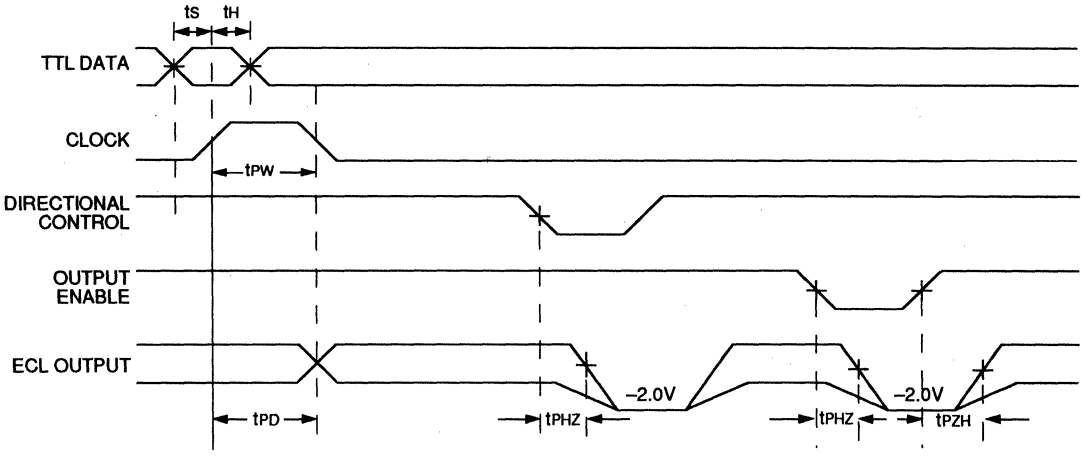
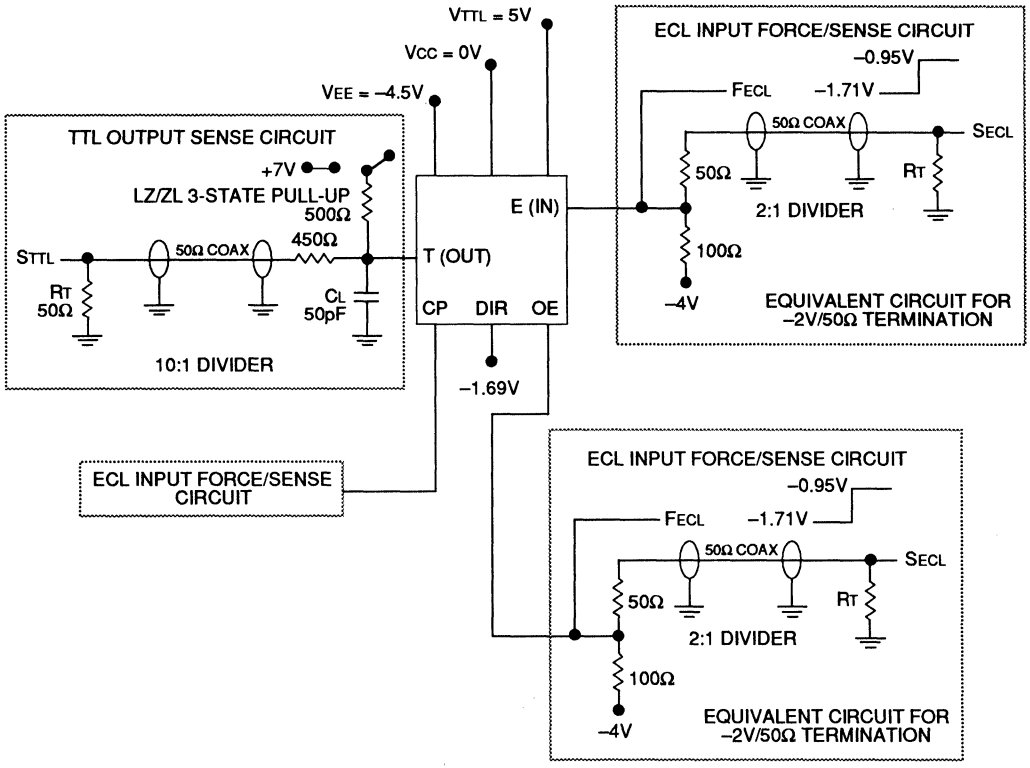


Figure 2. TTL-to-ECL Propagation Delay and Transition Times

TEST CIRCUITRY (ECL-TO-TTL)



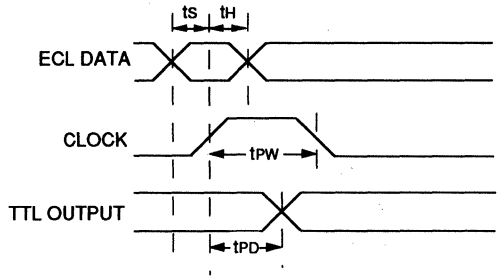
NOTES;

1. R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.
2. TTL and ECL force signals are brought to the DUT via 50Ω coax lines.
3. V_{TTL} is decoupled to ground with a 0.1µF capacitor, V_{EE} is decoupled to ground with a 0.01µF capacitor and V_{CC} is connected to ground.
4. The TTL three-state pull-up switch is connected to +7V only for ZL and LZ tests.

Figure 3. ECL-to-TTL AC Test Circuit

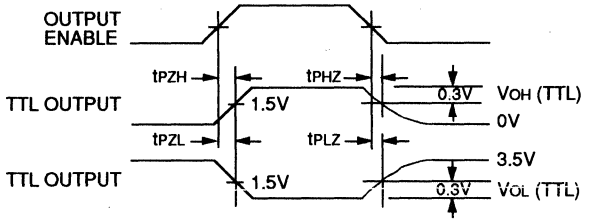
7

SWITCHING WAVEFORMS (ECL-TO-TTL)



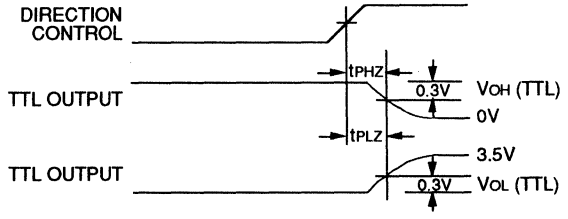
NOTE:
1. DIR is LOW and OE is HIGH.

Figure 4. ECL-to-TTL Transition, Propagation Delay and Transition Times



NOTE:
1. DIR is LOW and LE is HIGH.

Figure 5. ECL-to-TTL Transition, OE to TTL Output Enable and Disable Times



NOTE:
1. OE is HIGH and LE is HIGH.

Figure 6. ECL-to-TTL Transition, DIR to TTL Output Disable Time

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S329DC	D24-1	Commercial
SY100S329FC	F24-1	Commercial

LOW-POWER HEX PECL-TO-TTL TRANSLATOR

PRELIMINARY
SY100S390

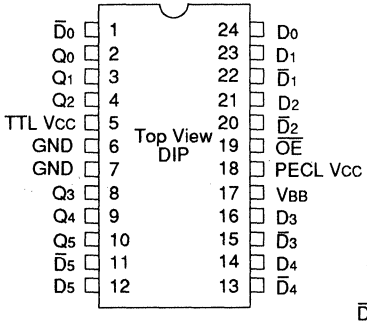
FEATURES

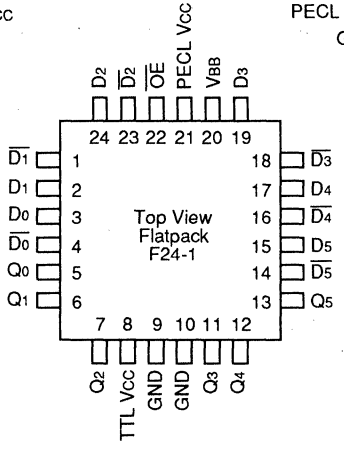
- **Operates from a single +5V supply**
- **Three-state outputs**
- **ESD protection of 2000V**
- **VBB output for single-ended use**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

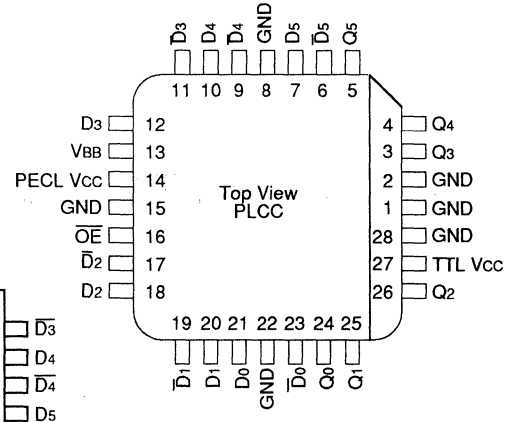
DESCRIPTION

The SY100S390 is a hex PECL-to-TTL translator for converting 100K logic levels to TTL logic levels. Unlike other level translators, the SY100S390 operates using only one +5V supply. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference generator provides VBB for single-ended operation. The standard three-state outputs are enabled by a common active low TTL compatible $\overline{OE}$ input. Partitioned VCCs on chip are brought out on separate power pins, allowing the noisy TTL VCC power plane to be isolated from the relatively quiet ECL VCC. The SY100S390 is ideal for applications limited to a single +5V supply, allowing for easy PECL-to-TTL interfacing.

PIN CONFIGURATIONS



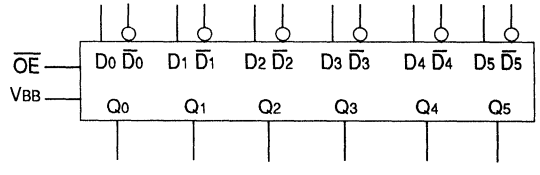




PIN NAMES

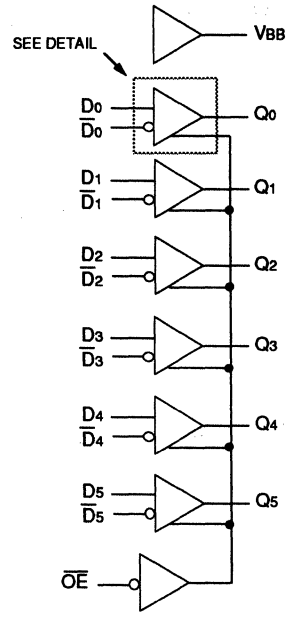
Label	Function
D_0 — D_5	Data Inputs (PECL)
$\overline{D_0}$ — $\overline{D_5}$	Inverting Data Inputs (PECL)
Q_0 — Q_5	Data Outputs (TTL)
$\overline{OE}$	Output Enable (TTL)
VBB	Reference Voltage (PECL)

LOGIC SYMBOL

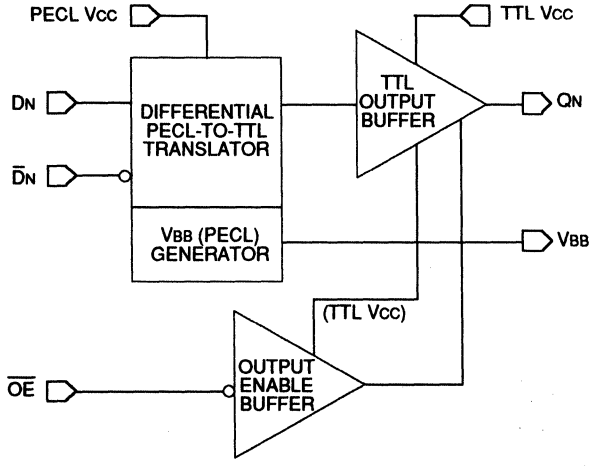


Rev.: B Amendment: /0
Issue Date: April, 1994

BLOCK DIAGRAM



BLOCK DIAGRAM DETAIL



TRUTH TABLE

Data Inputs (PECL)		Control Input (TTL)	TTL Outputs	Comments
Dn	$\overline{Dn}$	$\overline{OE}$	Qn	
X	X	H	Z	Outputs Disabled
L	H	L	L	Differential Operation
H	L	L	H	Differential Operation
L	L	L	U	Invalid Input States
H	H	L	U	Invalid Input States
Open	Open	L	U	Invalid Input States
L	V_{BB}	L	L	Single Ended Operation
H	V_{BB}	L	H	Single Ended Operation
V_{BB}	L	L	H	Single Ended Operation
V_{BB}	H	L	L	Single Ended Operation
V_{BB}	Open	L	H	Single Ended Operation
Open	V_{BB}	L	L	Single Ended Operation

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   U = Undefined

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operating Temperature	T_A	0 to +85	°C
Supply Voltage	V_{CC}	+4.75 to +5.25	V

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Storage Temperture	T_{STG}	–65 to +150	°C
Max. Junction Temp. Ceramic Plastic	T_J	 +175 +150	 °C °C
V_{CC} Pin Potential to Ground Pin	—	–0.5 to +7.0	V
TTL Input Voltage[2]	—	–0.5 to V_{CC}	V
TTL Input Current[2]	—	–30 to +5.0	mA
V_{BB} Output Current	—	–5.0 to +1.0	mA
PECL Input Potential	—	GND to PECL V_{CC} + 0.5V	—
V_{CC} Differential PECL V_{CC} to TTL V_{CC}	—	–1.0 to +1.0	V
Voltage Applied to Output in High State (with V_{CC} = 0V) Three-State Output	—	–0.5 to +5.5	V
Current Applied to Output in Low State (max.)	—	Twice the Rated I_{OL}	mA

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

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DC ELECTRICAL CHARACTERISTICS

PECL V_{CC} = +5.0V ± 5%; TTL V_{CC} = +5.0V ± 5%; GND = 0V

Symbol	Parameter		Min.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	Data	PECL V_{CC} – 1.165	PECL V_{CC} – 0.870	V	Guaranteed HIGH Signal for ALL Inputs (with One Input Tied to V_{BB})
		$\overline{OE}$	2.0	—		Guaranteed HIGH Signal (TTL)
V_{IL}	Input LOW Voltage	Data	PECL V_{CC} – 1.830	PECL V_{CC} – 1.475	V	Guaranteed LOW Signal for ALL Inputs (with One Input Tied to V_{BB})
		$\overline{OE}$	—	0.8		Guaranteed LOW Signal (TTL)
V_{BB}	Output Reference Voltage		PECL V_{CC} – 1.38	PECL V_{CC} – 1.26	V	I_{BB} = 0.0mA or –1.0mA
V_{OH}	Output HIGH Voltage (TTL)		2.7	—	V	I_{OH} = –3mA
V_{OL}	Output LOW Voltage (TTL)		—	0.5	V	I_{OL} = 24mA
I_{IH}	Input HIGH Current	Data	—	150	µA	V_{IN} = V_{IH}(Max.), D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = V_{IL}(Min.)
		$\overline{OE}$	—	20		V_{IN} = 2.7V (TTL)
I_{IL}	Input LOW Current	$\overline{OE}$	—	–200	µA	V_{IN} = 0.5V (TTL)
I_{BVI}	Input Breakdown Current	$\overline{OE}$	—	100	µA	V_{IN} = +5.5V, V_{TTL} = +5.25V
I_{CBO}	Input Leakage Current		–10	—	µA	V_{IN} = GND, D_0–D_5 = V_{BB} $\overline{D_0}$–$\overline{D_5}$ = V_{IL}(Min.)
I_{OZH}	Three-State Current Output HIGH		—	50	µA	V_{OUT} = +2.7V
I_{OZL}	Three-State Current Output LOW		—	–50	µA	V_{OUT} = +0.5V
I_{CC}	PECL Supply Current		13	30	mA	—
I_{CCZ}	TTL Supply Current		10	20	mA	Three-State
I_{CCL}	TTL Suply Current LOW		8	17	mA	LOW State
I_{CCH}	TTL Supply Current HIGH		0.4	2.0	mA	HIGH State
I_{OS}	Output Short Circuit Current		–150	–60	mA	V_{OUT} = 0.0V, V_{CC} = +5.25
V_{Diff}	Differential Input Voltage		150	—	mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage		PECL V_{CC} – 2.0	PECL V_{CC} – 0.5	V	—
V_{CD}	Clamp Diode Voltage		—	–1.2	V	I_{IN} = –18mA

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{CC} = +5.0V ± 5%;T_C = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{MAX}	Maximum Clock Frequency	100	—	100	—	100	—	MHz
t_{PLH} t_{PHL}	Propagation Delay[1] Data to Output	3.3	6.4	3.3	6.1	3.3	6.1	ns
t_{PZH} t_{PZL}	Output Enable Time[2]	2.7 2.3	4.8 3.9	2.7 2.3	4.8 3.9	3.0 2.6	5.1 4.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2]	2.3 2.0	4.6 3.6	2.3 2.0	4.6 3.6	2.3 2.0	4.6 3.6	ns

NOTES:

1. Refer to Figure 1.
2. Refer to Figure 2.

CERPAK AND PLCC

V_{CC} = +5.0V ± 5%;T_C = 0°C to +85°C

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{MAX}	Maximum Clock Frequency	100	—	100	—	100	—	MHz
t_{PLH} t_{PHL}	Propagation Delay[1] Data to Output	3.3	6.2	3.3	5.9	3.3	5.9	ns
t_{PZH} t_{PZL}	Output Enable Time[2]	2.7 2.3	4.6 3.7	2.7 2.3	4.6 3.7	3.0 2.6	4.9 4.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2]	2.3 2.0	4.4 3.4	2.3 2.0	4.4 3.4	2.3 2.0	4.4 3.4	ns

NOTES:

1. Refer to Figure 1.
2. Refer to Figure 2.

7

TIMING WAVEFORMS

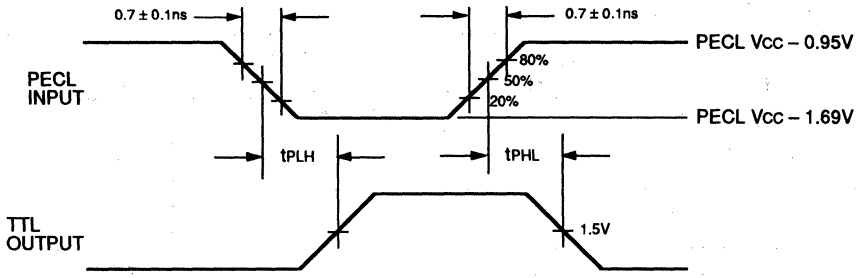


Figure 1. Data-to-Output Propagation Delay

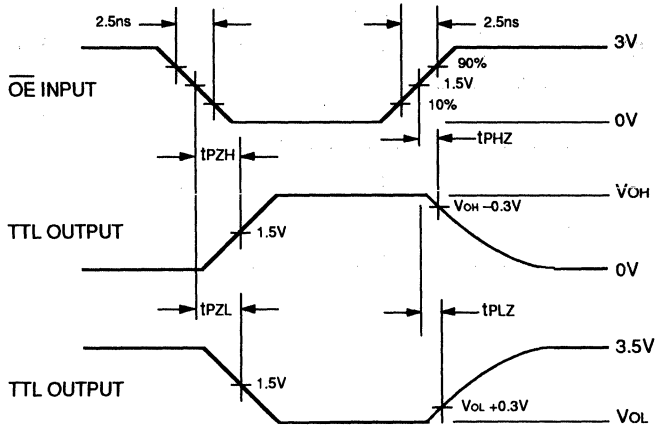
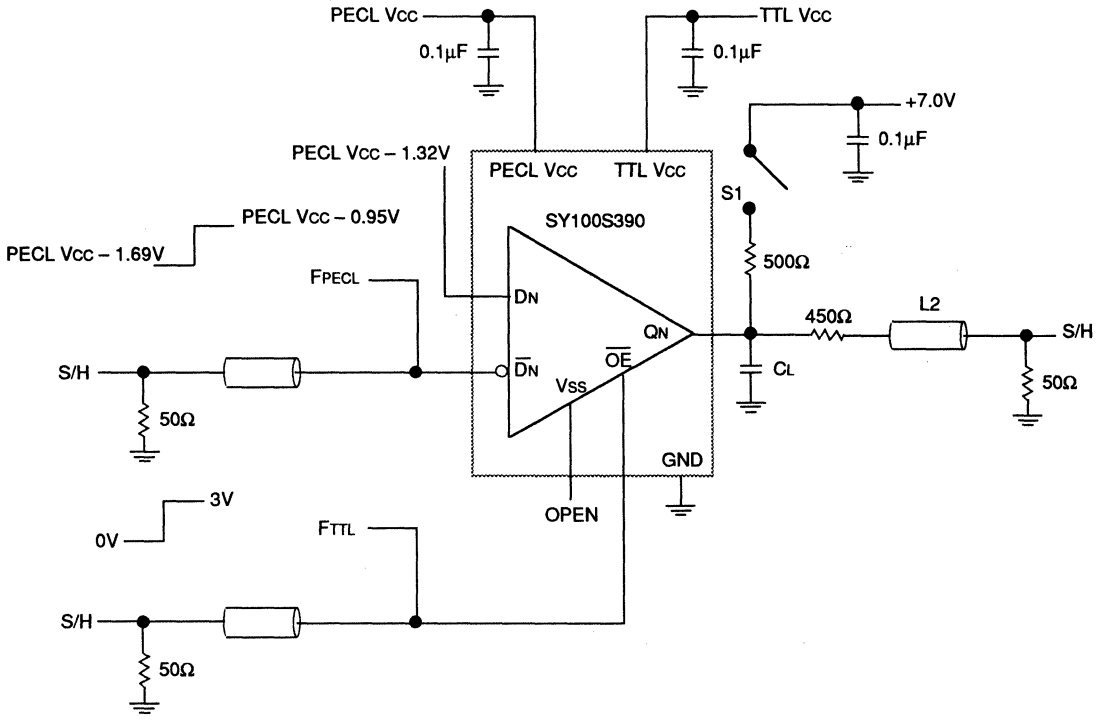


Figure 2. Enable/Disable Propagation Delay

AC TEST CIRCUIT



NOTES:

GND = 0V, PECL Vcc = +5V, TTL Vcc = +5V.
L1 and L2 = equal length 50Ω impedance lines.
50Ω terminators are internal to S/H measurement unit.
Decoupling 0.1µF from GND to PECL VCC and TTL Vcc.
All unused outputs are loaded with 500Ω to GND.
C_L = Fixture and stray capacitance = 50pF.
Switch S1 is open for t_{PLH}, t_{PHL}, t_{PHZ} and t_{PZH} tests.
Switch S1 is closed only for t_{PLZ} and t_{PZL} tests.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S390DC	D24-1	Commercial
SY100S390FC	F24-1	Commercial
SY100S390JC	J28-1	Commercial

APPLICATION NOTES

1. Device performance will be enhanced by the use of dual VCC power planes, as illustrated in Application Figures 3 and 4. This will minimize the coupling of TTL switching noise into the primary reference to the PECL circuitry and take full advantage of the SY100S390's on-chip VCC partitioning.
2. The device's partitioned VCC may be operated from two 5V ± 5% tolerance supplies provided that they are ramped up/down together so that the maximum differential is 1V. This is to prevent overstress to internal ESD diodes. If the PECL driver to the 'S390 is powered from a separate supply, it must obey this sequence rule also.
3. Glitch-free power up, independent of data input levels, is achieved if TTL logic HIGH is held on the Output Enable pin during ramping up/down of the VCC supply.
4. Undefined output states can occur for some invalid combinations. See Truth Table. This should be avoided to prevent possible oscillation or increased power consumption due to TTL outputs biased into a quasi state with both pull-up and pull-down stages partially on. Three-Stating the outputs will counteract the effects of invalid input states.
5. Pins 8, 15 and 22 on the 28-pin PLCC package are tied to the chip's substrate and are named GNDs. These pins are electrically common to the ground pins 1, 2 and 28. For best thermal performance, tie the GND pins to the circuit ground plane. They may be tied to an electrically isolated thermal dissipation plane or may float.
6. Figure 3 illustrates typical differential input operation.
7. Figure 4 illustrates typical single-ended input operation.

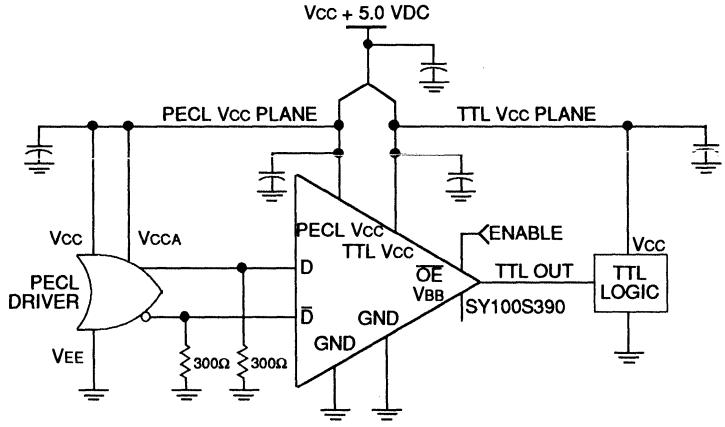


Figure 3.

APPLICATION NOTES (CONT'D.)

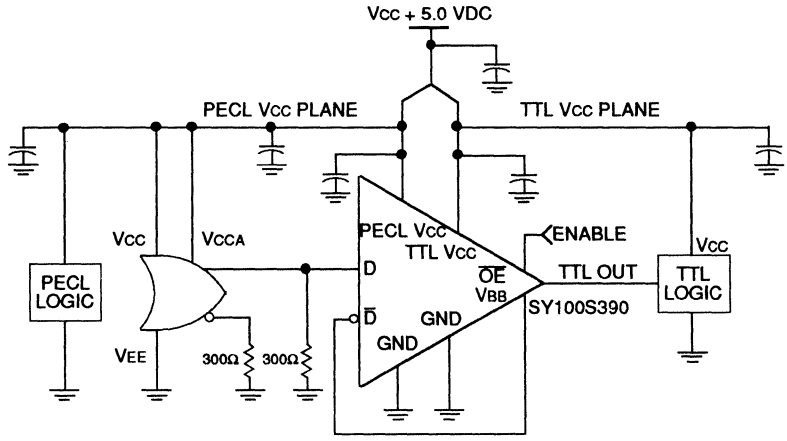


Figure 4.

7

SYNERGY SEMICONDUCTOR

LOW-POWER HEX TTL-TO-PECL TRANSLATOR

PRELIMINARY
SY100S391

FEATURES

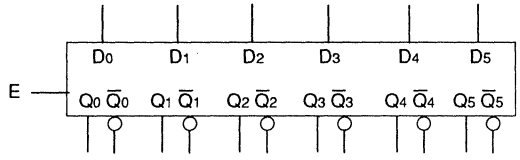
- **Operates from a single +5V supply**
- **Differential PECL outputs**
- **ESD protection of 2000V**
- **Companion chip to SY100S390 PECL-to-TTL translator**
- **Function and pinout compatible with National and Signetics F100K**
- **Available in CERDIP, CERPACK and PLCC**

DESCRIPTION

The SY100S391 is a hex TTL-to-PECL translator for converting TTL logic levels to 100K logic levels. The unique feature of this translator is the ability to do this translation using only one +5V supply. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. A common enable (E), when LOW, holds all inverting outputs HIGH and all non-inverting inputs LOW.

The SY100S391 is ideal for those mixed PECL/TTL applications which only have a +5V supply available. When used in the differential mode, the S391, due to its high common mode rejection, overcomes voltage gradients between the TTL and PECL ground systems.

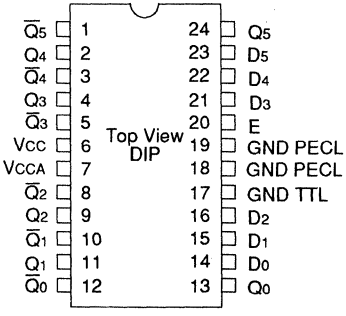
LOGIC SYMBOL

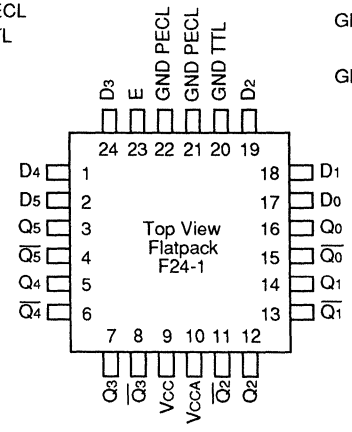


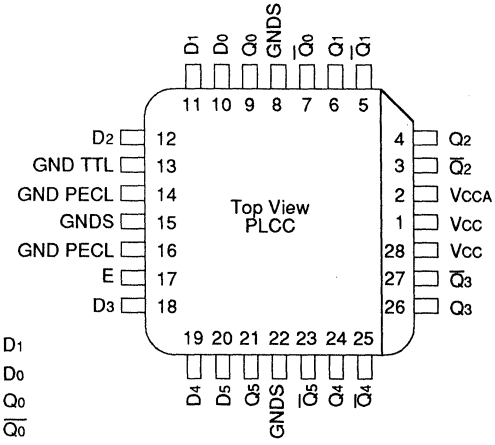
PIN NAMES

Label	Function
D_0 — D_5	Data Inputs (TTL)
Q_0 — Q_5	Data Outputs (PECL)
$\overline{Q}_0$ — $\overline{Q}_5$	Inverting Data Outputs (PECL)
E	Enable Input (TTL)

PIN CONFIGURATIONS

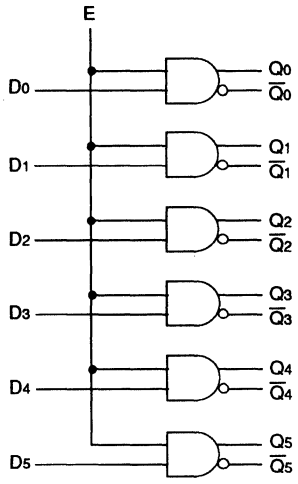






Rev.: B Amendment: /0
Issue Date: April, 1994

BLOCK DIAGRAM



TRUTH TABLE

Inputs		Outputs	
D_n	E	Q_n	$\overline{Q}_n$
H	H	H	L
L	H	L	H
H	L	L	H
L	L	L	H

NOTE:
1. H = High Voltage Level, L = Low Voltage Level

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operating Temperature	T_A	0 to +85	°C
Supply Voltage	V_{CC}	+4.5 to +5.5	V

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Storage Temperture	T_{STG}	–65 to +150	°C
Max. Junction Temp. Ceramic Plastic	T_J	 +175 +150	 °C °C
V_{CC} Pin Potential to Ground Pin	—	–0.5 to +7.0	V
PECL Output Current (DC Output HIGH)	—	–50	mA
TTL Input Voltage[2]	—	–0.5 to +7.0	V
TTL Input Current[2]	—	–30 to +5.0	mA

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is siffucient to protect inputs.

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TTL-TO-PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5.0V ± 10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC} –1025	V_{CC} –955	V_{CC} –870	mV	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)
V_{OL}	Output LOW Voltage	V_{CC} –1890	V_{CC} –1705	V_{CC} –1620		Loading with 50Ω to V_{CC} –2V
V_{OHC}	Output HIGH Voltage Corner Point High	V_{CC} –1035	—	—	mV	V_{IN} = V_{IH} (Min.) or V_{IL} (Max.) Loading with 50Ω to V_{CC} –2V
V_{OLC}	Output LOW Voltage Corner Point Low	—	—	V_{CC} –1610		
V_{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V_{TTL}, V_{EE}, T_A Range
V_{IL}	Input LOW Voltage	0	—	0.8	V	Over V_{TTL}, V_{EE}, T_A Range
I_{IH}	Input HIGH Current	—	—	10	µA	V_{IN} = +2.7V
	Breakdown Current	—	—	100	µA	V_{IN} = +5.5V, V_{CC} = Max.
I_{IL}	Input LOW Current D_n E	 –0.8 –4.2	—	—	mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	–1.2	—	—	V	I_{IN} = –18mA
I_{CC}	V_{CC} Supply Current	32	—	69	mA	Inputs Open

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

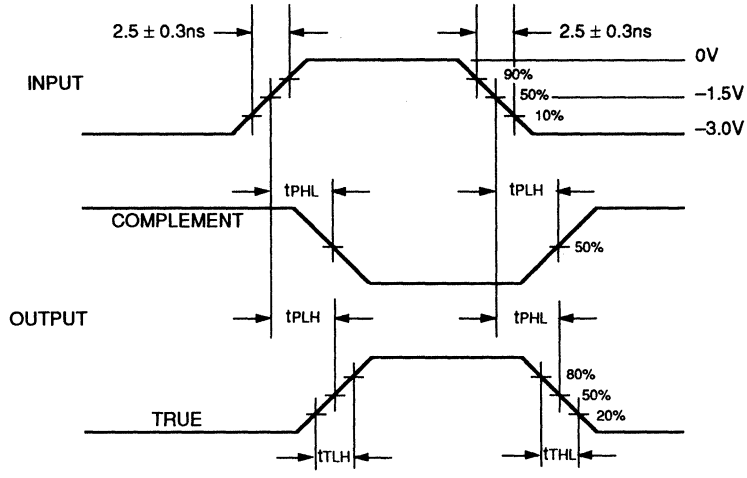
AC ELECTRICAL CHARACTERISTICS

CERDIP, CERPACK AND PLCC

V_{CC} = +5.0V ± 10%;T_C = 0°C to +85°C

		T_A = 0°C		T_A = +25°C		T_A = 85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	400	1400	400	1400	400	1400	ps
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	350	1700	350	1700	350	1700	ps

TIMING DIAGRAM



Propagation Delay and Transition Times

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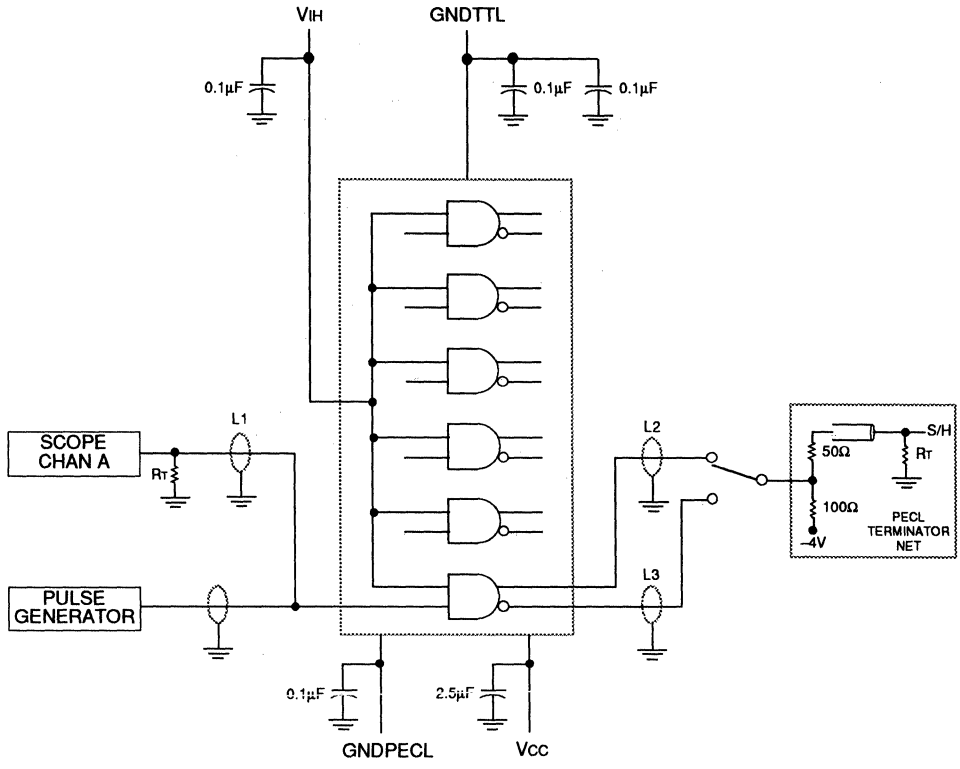
TEST CIRCUIT



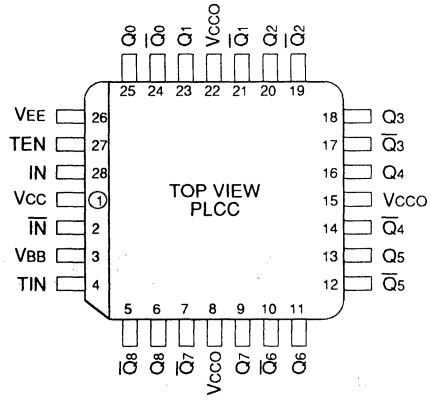
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S391DC	D24-1	Commercial
SY100S391FC	F24-1	Commercial
SY100S391JC	J28-1	Commercial

FEATURES

- PECL version of popular ECLinPS E111
- Low skew
- Guaranteed skew spec
- VBB output
- TTL enable input
- Selectable TTL or PECL clock input
- Single +5V supply
- Differential internal design
- Similar pin configuration to E111
- PECL I/O fully compatible with industry standard
- Internal 75KΩ PECL input pull-down resistors
- ESD protection of 2000V

PIN CONFIGURATION



DESCRIPTION

The SY100S811 is a low skew 1-to-9 PECL differential driver designed for clock distribution in new, high-performance PECL systems. It accepts either a PECL clock input or a TTL input by using the TTL enable pin TEN. When the TTL enable pin is at a TTL logic one level, the TTL input is enabled and the PECL input is disabled. When the enable pin is set to TTL logic zero level, the TTL input is disabled and the PECL input is enabled.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E811 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

The VBB output is intended for use as a reference voltage for single-ended reception of PECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01μF capacitor.

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PIN NAMES

Pin	Function
EIN, $\overline{EIN}$	Differential PECL Input Pair
TIN	TTL Input
TEN	TTL Input Enable
Q0, $\overline{Q0}$ – Q8, $\overline{Q8}$	Differential PECL Outputs
VBB	VBB Output
VCC	PECL VCC (+5.0V)
VEE	PECL Ground (0V)

TRUTH TABLE

TEN	EIN	TIN	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

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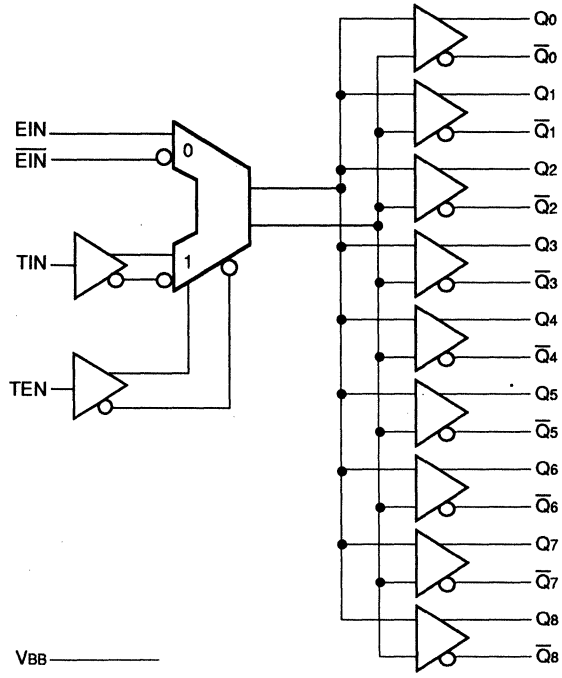
BLOCK DIAGRAM



PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5.0V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{BB}	Output Reference Voltage	3.62	—	3.74	3.62	—	3.74	3.62	—	3.74	V	$V_{CC} = V_{CCO} = 5.0V$
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	µA	—
V_{IH}	Input HIGH Voltage	3.835	—	4.12	3.835	—	4.12	3.835	—	4.12	V	$V_{CC} = V_{CCO} = 5.0V$
V_{IL}	Input LOW Voltage	3.19	—	3.525	3.19	—	3.525	3.19	—	3.525	V	$V_{CC} = V_{CCO} = 5.0V$
I_{CC}	Power Supply Current	—	53	65	—	53	65	—	60	74	mA	All inputs and outputs open

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = 5V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V	—
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V	—
I_{IH}	Input HIGH Current	— —	— —	20 100	— —	— —	20 100	— —	— —	20 100	µA	$V_{IN} = 2.7V$ $V_{IN} = 5.0V$
I_{IL}	Input LOW Current	—	—	–0.6	—	—	–0.6	—	—	–0.6	mA	$V_{IN} = 0.5V$
V_{IK}	Input Clamp Voltage	—	—	–1.2	—	—	–1.2	—	—	–1.2	V	$I_{IN} = -18mA$

AC ELECTRICAL CHARACTERISTICS[1–6]

$V_{CC} = V_{CCO} = 5V \pm 5\%$

Symbol	Parameter	$T_A = 0°C$			$T_A = +25°C$			$T_A = +85°C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output[1] EIN (differential) EIN (single-ended) TIN	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	 430 330 350	 — — —	 630 730 950	ps	 2 3
t_{SKEW}	Within-Device Skew	—	25	50	—	25	50	—	25	50	ps	4
V_{PP}	Minimum PECL Input Swing	250	—	—	250	—	—	250	—	—	mV	5
V_{CMR}	PECL Common Mode Range	–1.6	—	–0.4	–1.6	—	–0.4	–1.6	—	–0.4	V	6
t_r t_f	Output Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps	—

NOTES:

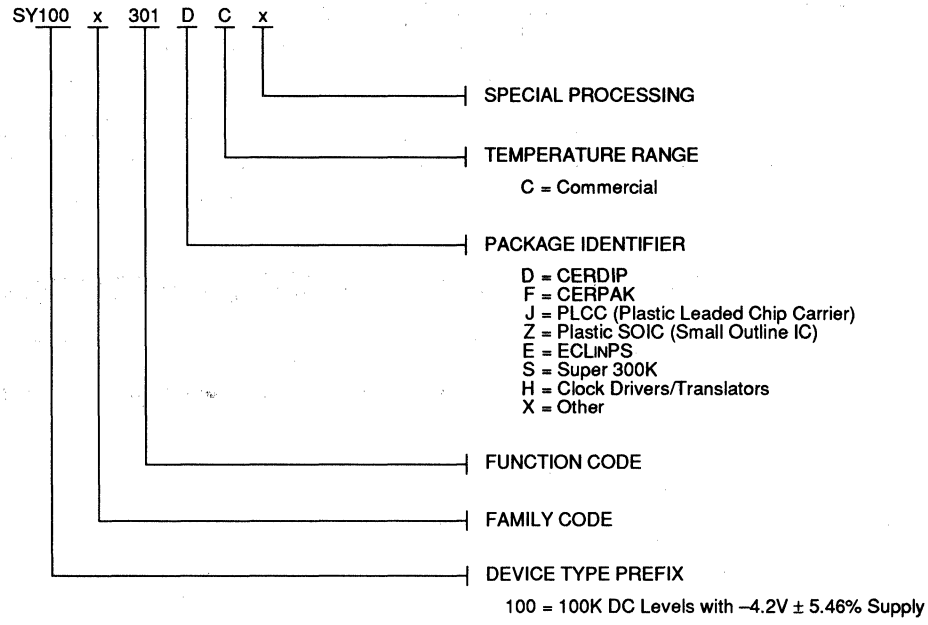
1. Part-to-part skew is defined as Max. — Min. value at the given temperature.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min.) is AC limited for the S811, as a differential input as low as 50mV will still produce full PECL levels at the output.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.).

PRODUCT ORDERING CODE

ORDERING CODE	PACKAGE TYPE	OPERATING RANGE
SY100S811JC	J28-1	Commercial

ORDERING INFORMATION

LOGIC ORDERING INFORMATION



ULTRA-FAST & LOW-POWER RAMs

8

SYNERGY SEMICONDUCTOR

ULTRA-FAST AND LOW-POWER RAMS

8

FEATURES

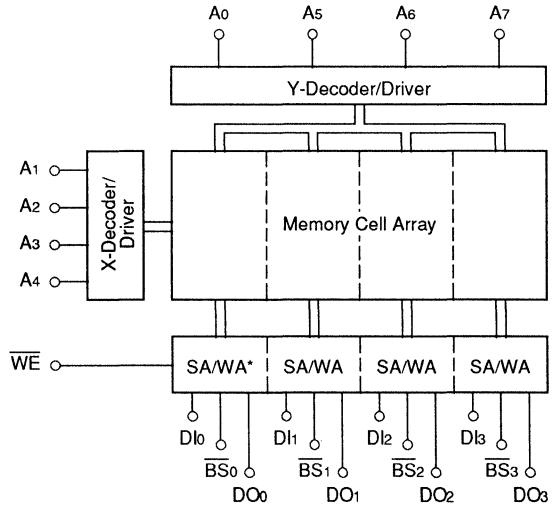
- **Address access time, t_{AA}: 2.5/3/4/5/7ns max.**
- **Block select access time, t_{AB}: 2ns max.**
- **Write pulse width, t_{WW}: 3ns min.**
- **Edge rate, t_r/t_f: 500ps typ.**
- **Power supply current, I_{EE}: –250mA, -200mA for -5/7ns**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Includes popular Block Select function allowing individual read/write control over blocks**
- **Available in hermetic Dip, Flatpack and MLCC**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10/100/101422 are 1024-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 256-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100422 is also supply voltage-compatible with 100K ECL, while the SY101422 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101422 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



* SA = Sense Amplifier
WA = Write Amplifier

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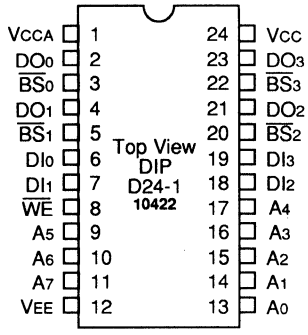
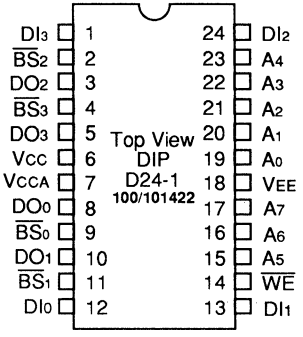
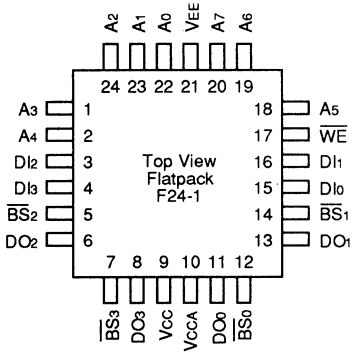
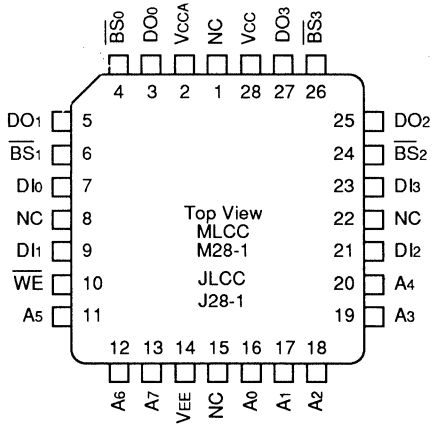
PIN CONFIGURATIONS









PIN NAMES

Label	Function
A_0 - A_7	Address Inputs
$\overline{BS}_0$ - $\overline{BS}_3$	Block Select ($\overline{BS}$)
$\overline{WE}$	Write Enable
DI_0 - DI_3	Data Input (D_{IN})
DO_0 - DO_3	Data Output (D_{OUT})
V_{CC}	GND (0V)
V_{CCA}	Output GND (0V)
V_{EE}	Supply Voltage

TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

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FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101422 are 1024-bit RAMs organized as four 256-by-1-bit blocks with each block having its own Block Select ($\overline{BS}$) control signal that functions essentially like a unique chip select for the Block. The four blocks and Block Selects together make the device a 256 x 4-bit RAM. Memory cell selection is achieved by using the 8 address bits designated as A_0 through A_7. Each of the 2^8 possible input address combinations corresponds to a unique word location in memory. The active low Block Select ($\overline{BS}$) control signals are provided for memory expansion and for independent control of each of the four 256 x 1-bit blocks of memory. The active low Write Enable ($\overline{WE}$) controls the read and write operation on the selected block or blocks. Data resident on the D_{IN} inputs (D_{I0} through D_{I3}) is written into the addressed location only when $\overline{WE}$ and the Block Select ($\overline{BS}$) associated with each of the D_{IN} bits is held LOW. This allows control of the Write operation to any one, two, three or all four of the input data bits. In order to perform a read operation, $\overline{WE}$ is held high, the Block Select ($\overline{BS}$) associated with each of the four output blocks is held low, and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. This allows control of the Read operation to any one, two, three or all four of the output blocks. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

All outputs are forced to a logic LOW level when the RAM is being written into ($\overline{WE}$ = LOW). The output (or outputs) associated with a block (or blocks) of memory can be forced to a logic LOW low level by deselecting that block (or blocks) with its respective Block Select input ($\overline{BS_0}$ – $\overline{BS_3}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage [1]	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	75	°C
Supply Voltage[1]	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		T_C	0	—	85	°C
Supply Voltage[1]	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	85	°C

NOTE:

1. Referenced to V_{CC}.

RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	t_r	—	500	—	ps
Output Fall Time	F	t_f	—	500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	5	—	pF

10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; T_C = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to+ 75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{BS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{BS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply -2.5ns, -3ns, -4ns Current -5ns, -7ns	0°C to +75°C	–250 –200	— —	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) T_C = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{BS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{BS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply -2.5ns, -3ns, -4ns Current -5ns, -7ns	–250 –200	— —	mA	All Inputs and Outputs Open

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SYNERGY SEMICONDUCTOR

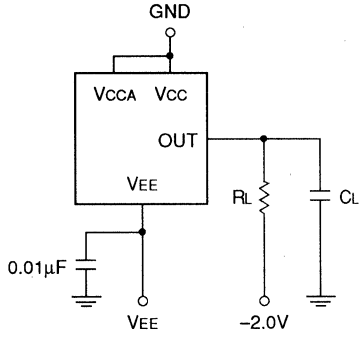
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

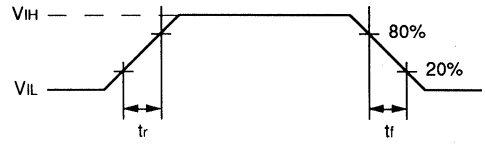
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

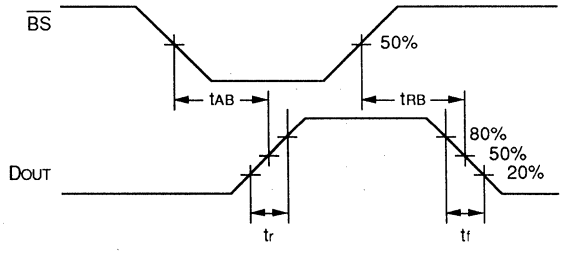
OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

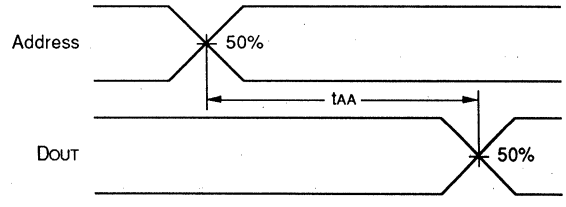
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10422-2.5 SY100422-2.5 SY101422-2.5		SY10422-3 SY100422-3 SY101422-3		SY10422-4 SY100422-4 SY101422-4		SY10422-5 SY100422-5 SY101422-5		SY10422-7 SY100422-7 SY101422-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	TAVQV	Address Access Time	—	2.5	—	3	—	4	—	5	—	7	ns
t_{AB}	TBSLQV	Block Select Access Time	—	2	—	2	—	2	—	3	—	3	ns
t_{RB}	TBSHQL	Block Select Recovery Time	—	2	—	2	—	2	—	3	—	3	ns

READ CYCLE TIMING DIAGRAM

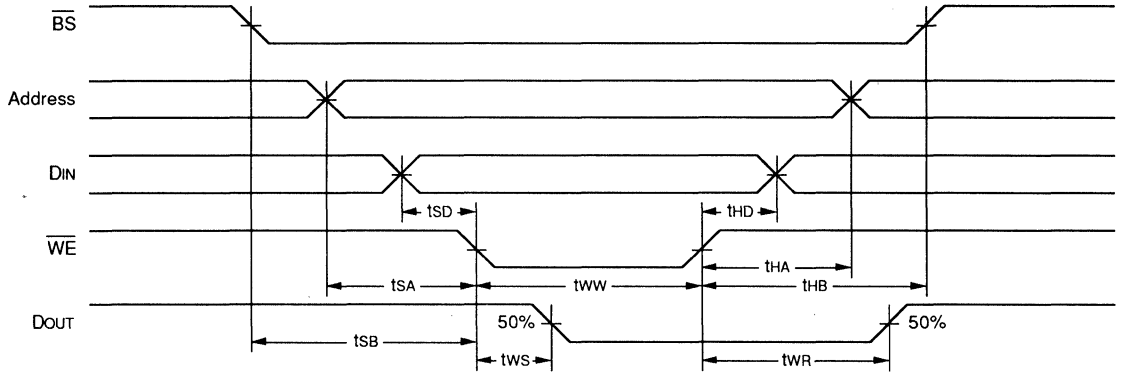




WRITE CYCLE

Symbol		Parameter	SY10422-2.5 SY100422-2.5 SY101422-2.5		SY10422-3 SY100422-3 SY101422-3		SY10422-4 SY100422-4 SY101422-4		SY10422-5 SY100422-5 SY101422-5		SY10422-7 SY100422-7 SY101422-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	3	—	3	—	4	—	3.5	—	5	—	ns
tWS	TWLQL	Write Disable Time	—	2.5	—	3	—	4	—	3.5	—	4	ns
tWR	TWHQV	Write Recovery Time	—	2.5	—	3	—	4	—	3.5	—	4	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	1	—	0.5	—	1	—	ns
tSB	TBSLWL	Block Select Set-up Time	0	—	0	—	0	—	0.5	—	1	—	ns
tSD	TDVWL	Data Set-up Time	0	—	0	—	0	—	0.5	—	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns
tHB	TWHBSX	Block Select Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



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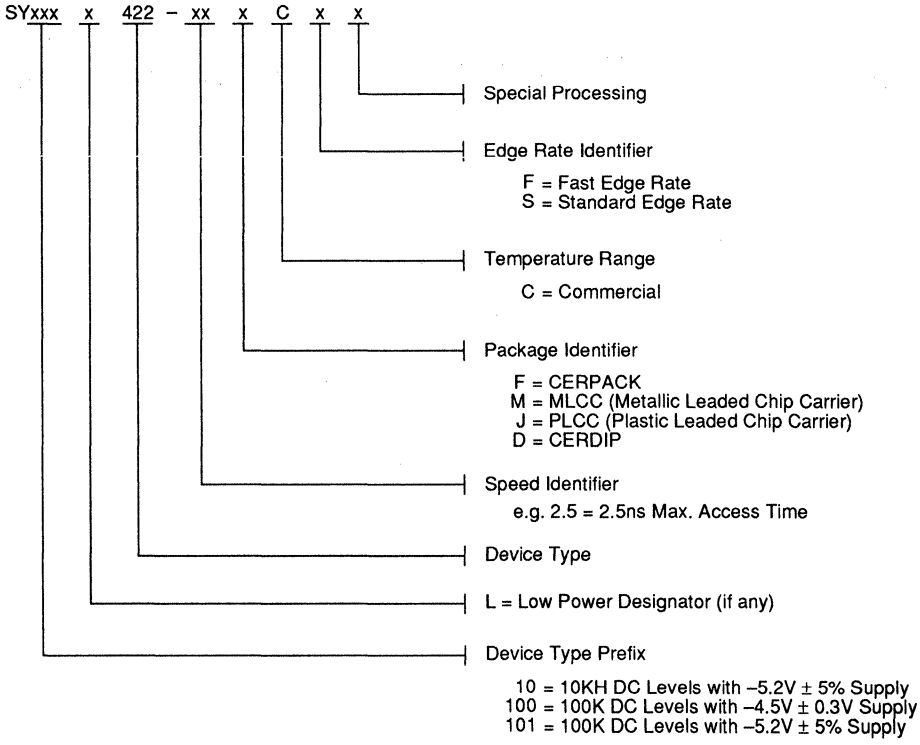
PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
2.5	SY10/100/101422-2.5FCF	Fast	F24-1	Commercial
	SY10/100/101422-2.5MCF	Fast	M28-1	Commercial
3	SY10/100/101422-3FCF	Fast	F24-1	Commercial
	SY10/100/101422-3MCF	Fast	M28-1	Commercial
4	SY10/100/101422-4FCF	Fast	F24-1	Commercial
	SY10/100/101422-4MCF	Fast	M28-1	Commercial
5	SY10/100/101422-5FCS	Standard	F24-1	Commercial
	SY10/100/101422-5JCS	Standard	J28-1	Commercial
	SY10/100/101422-5DCS	Standard	D28-1	Commercia
7	SY10/100/101422-7FCS	Standard	F24-1	Commercial
	SY10/100/101422-7JCS	Standard	J28-1	Commercial
	SY10/100/101422-7DCS	Standard	D28-1	Commercial



1K x 4 ECL RAM

FEATURES

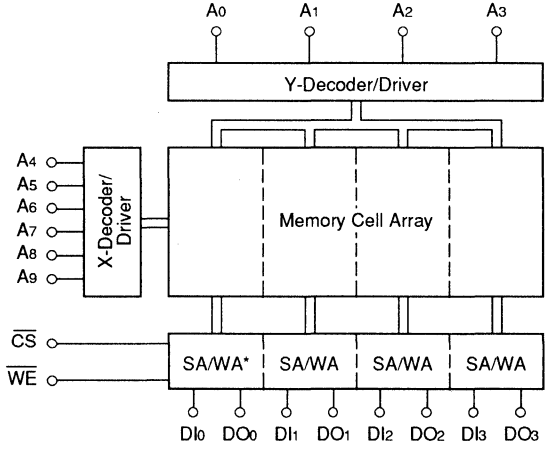
- **Address access time, t_{AA}: 2.5/3/4/5/7ns max.**
- **Chip select access time, t_{AC}: 2ns max.**
- **Write pulse width, t_{WW}: 3ns min.**
- **Edge rate, t_r/t_f: 500ps typ.**
- **Power supply current, I_{EE}: –300mA, -220mA for -5/7ns**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic Dip, Flatpack and MLCC**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10/100/101474 are 4096-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 1024-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100474 is also supply voltage-compatible with 100K ECL, while the SY101474 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101474 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



* SA = Sense Amplifier
WA = Write Amplifier

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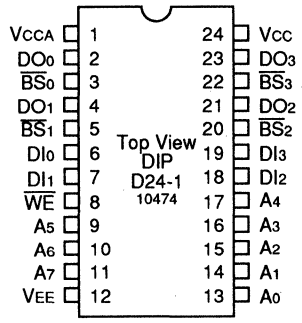
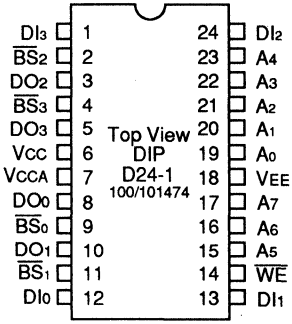
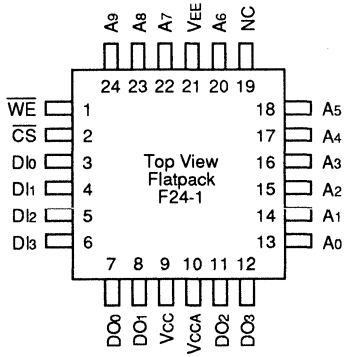
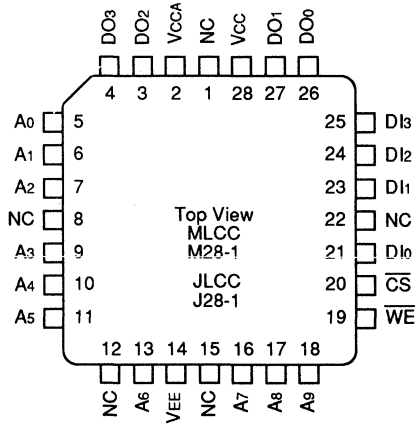
Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS









PIN NAMES

Label	Function
A0 - A9	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DI0 - DI3	Data Input (DIN)
DO0 - DO3	Data Output (DOUT)
VCC	GND (0V)
VCCA	Output GND (0V)
VEE	Supply Voltage
NC	No Connect

TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101474 are 4096-bit RAMs organized as 1024-words-by-4-bits. Memory cell selection is achieved by using the 10 address bits designated as A_0 through A_9. Each of the 2^{10} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the D_{IN} inputs (D_{I0} through D_{I3}) is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	75	°C
Supply Voltage(1)	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		T_C	0	—	85	°C
Supply Voltage(1)	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	85	°C

NOTE:

1. Referenced to V_{CC}.

RISE AND FALL TIME

Parameter	Code(1)	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
Output Fall Time	F	tf	—	500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	5	—	pF

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10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply -2.5ns, -3ns, -4ns Current -5ns, -7ns	0°C to +75°C	–300 –220	— —	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s

V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply -2.5ns, -3ns, -4ns Current -5ns, -7ns	–300 –220	— —	mA	All Inputs and Outputs Open

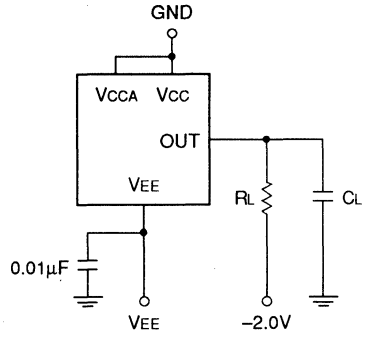
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

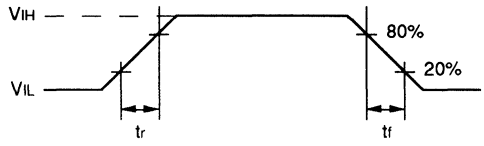
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10474-2.5 SY100474-2.5 SY101474-2.5		SY10474-3 SY100474-3 SY101474-3		SY10474-4 SY100474-4 SY101474-4		SY10474-5 SY100474-5 SY101474-5		SY10474-7 SY100474-7 SY101474-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tAA	TAVQV	Address Access Time	—	2.5	—	3	—	4	—	5	—	7	ns
tAC	TSLQV	Chip Select Access Time	—	2	—	2	—	2	—	3	—	3	ns
tRC	TSHQL	Chip Select Recovery Time	—	2	—	2	—	2	—	3	—	3	ns

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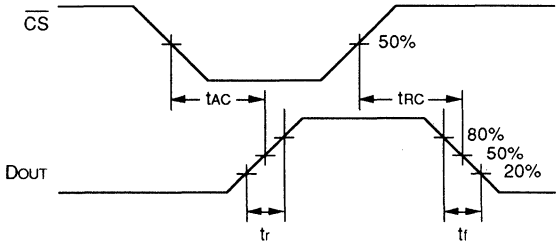
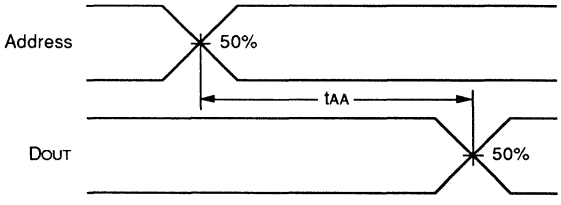
READ CYCLE TIMING DIAGRAM

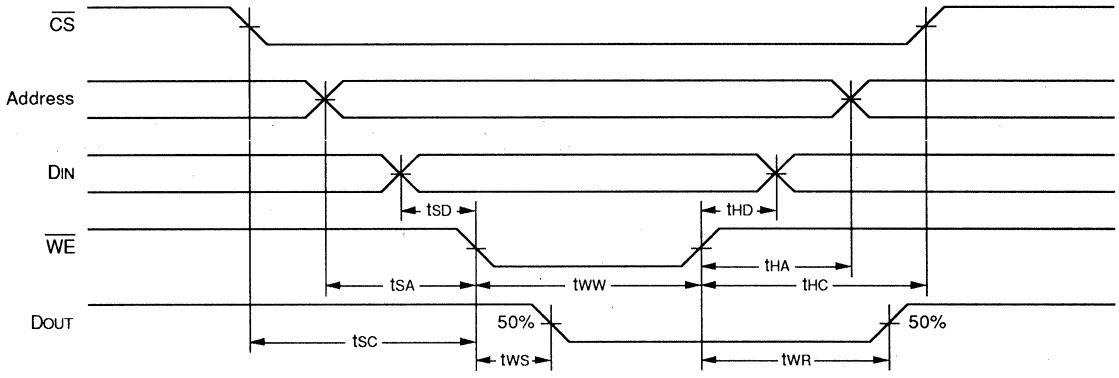




WRITE CYCLE

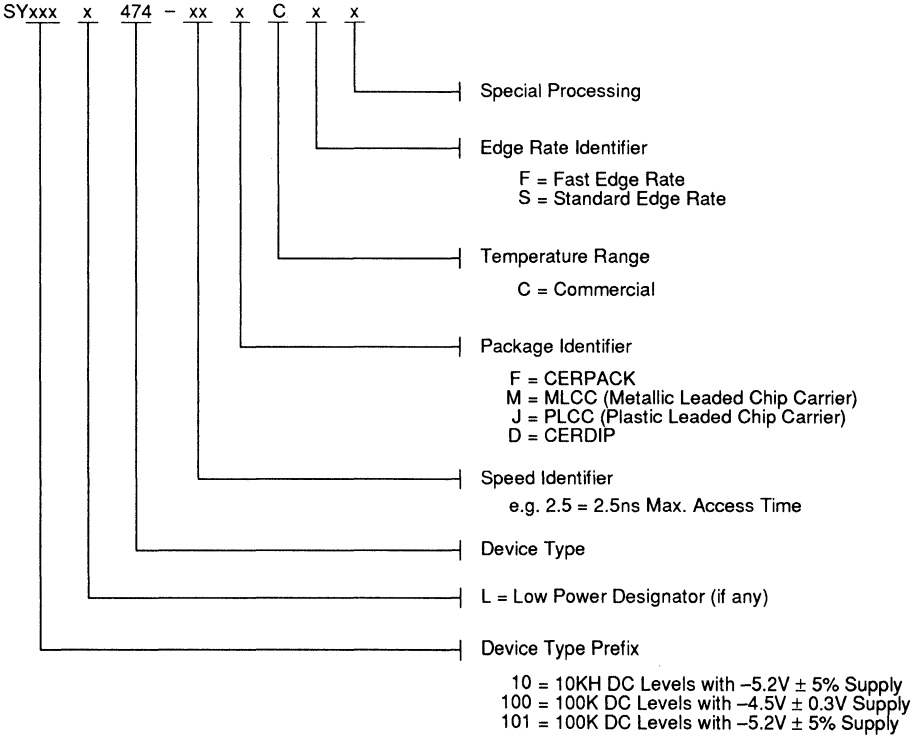
Symbol		Parameter	SY10474-2.5 SY100474-2.5 SY101474-2.5		SY10474-3 SY100474-3 SY101474-3		SY10474-4 SY100474-4 SY101474-4		SY10474-5 SY100474-5 SY101474-5		SY10474-7 SY100474-7 SY101474-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	3	—	3	—	4	—	3.5	—	5	—	ns
tWS	TWLQL	Write Disable Time	—	2.5	—	3	—	4	—	3.5	—	4	ns
tWR	TWHQV	Write Recovery Time	—	2.5	—	3	—	4	—	3.5	—	4	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	1	—	0.5	—	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	0	—	0	—	0	—	0.5	—	1	—	ns
tSD	TDVWL	Data Set-up Time	0	—	0	—	0	—	0.5	—	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	1	—	1.0	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
2.5	SY10/100/101474-2.5FCF	Fast	F24-1	Commercial
	SY10/100/101474-2.5MCF	Fast	M28-1	Commercial
3	SY10/100/101474-3FCF	Fast	F24-1	Commercial
	SY10/100/101474-3MCF	Fast	M28-1	Commercial
4	SY10/100/101474-4FCF	Fast	F24-1	Commercial
	SY10/100/101474-4MCF	Fast	M28-1	Commercial
5	SY10/100/101474-5FCS	Standard	F24-1	Commercial
	SY10/100/101474-5JCS	Standard	J28-1	Commercial
	SY10/100/101474-5DCS	Standard	D28-1	Commercial
7	SY10/100/101474-7FCS	Standard	F24-1	Commercial
	SY10/100/101474-7JCS	Standard	J28-1	Commercial
	SY10/100/101474-7DCS	Standard	D28-1	Commercial



8

FEATURES

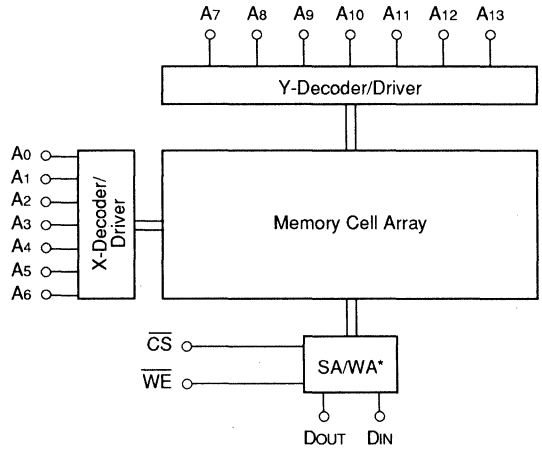
- **Address access time, t_{AA}: 6/8/10ns max.**
- **Chip select access time, t_{AC}: 3ns max.**
- **Edge rate, t_r/t_f: 500ps (typ.)**
- **Write recovery times under 5ns**
- **Power supply current, I_{EE}: –260mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic DIP**
- **ESD Protection of 2000V**

DESCRIPTION

The Synergy SY10/100/101480 are 16384-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 16384-words-by-1-bit and meet the standard 10K/100K family signal levels. The SY100480 is also supply voltage-compatible with 100K ECL, while the SY101480 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101480 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

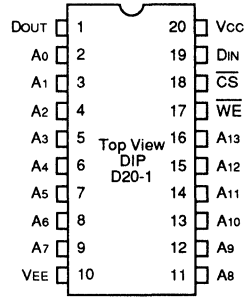
BLOCK DIAGRAM



* SA = Sense Amplifier
WA = Write Amplifier

Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS



PIN NAMES

Label	Function
A0 - A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DIN	Data Input
DOUT	Data Output
VCC	GND (0V)
VEE	Supply Voltage

TRUTH TABLE

Input				
$\overline{CS}$	$\overline{WE}$	DIN	Output	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101480 are 16384-bit RAMs organized as 16384-words-by-1-bit. Memory cell selection is achieved by using the 14 address bits designated as A0 through A13. Each of the 2^{14} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the DIN input is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to DOUT to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The output is brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

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ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
VEE Pin Potential to VCC Pin	VEE	+0.5 to –7.0	V
Input Voltage	VIN	+0.5 to –2.0	V
DC Output Current (Output High)	IOUT	–30	mA
Temperature Under Bias	TC	–55 to +125	°C
Storage Temperature	Tstore	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage[1]	10K	VEE	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	75	°C
Supply Voltage[1]	100K	VEE	–4.8	–4.5	–4.2	V
Case Temperature		TC	0	—	85	°C
Supply Voltage[1]	101K	VEE	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	85	°C

NOTE:

1. Referenced to VCC.

RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
Output Fall Time	F	tf	—	500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	CIN	—	4	—	pF
Output Pin Capacitance	COUT	—	5	—	pF

10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current –6, –8ns –10ns	0°C to +75°C	 –260 –220	 — —	mA	All Inputs and Outputs Open

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100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = −4.5V (100K) T_C = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = −5.2V (101K) Output Load = 50Ω to −2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	−1025	−880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	−1810	−1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	−1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	−1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	−1165	−880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	−1810	−1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	−2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	−2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current −6, −8ns −10ns	 −260 −220	 — —	mA	All Inputs and Outputs Open

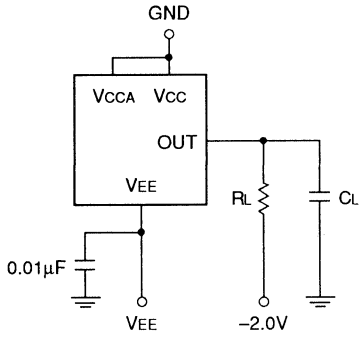
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

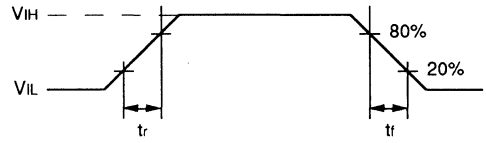
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10480-6 SY100480-6 SY101480-6		SY10480-8 SY100480-8 SY101480-8		SY10480-10 SY100480-10 SY101480-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	TAVQV	Address Access Time	—	6	—	8	—	10	ns
t_{AC}	TSLQV	Chip Select Access Time	—	3	—	3	—	3	ns
t_{RC}	TSHQL	Chip Select Recovery Time	—	3	—	3	—	3	ns

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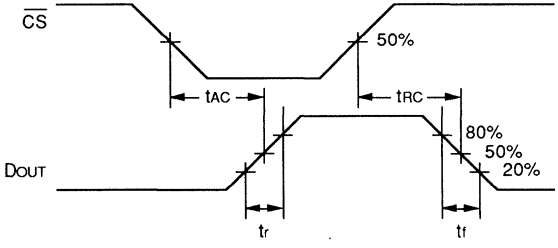
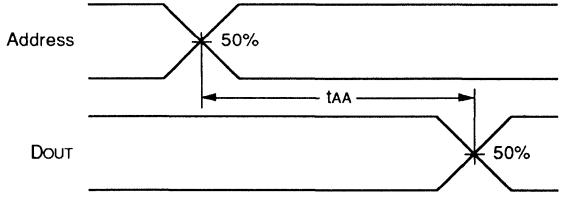
READ CYCLE TIMING DIAGRAM

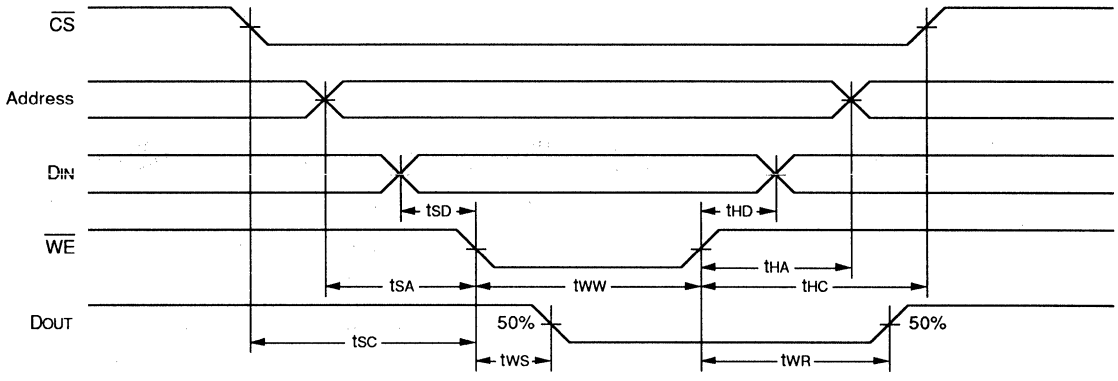




WRITE CYCLE

Symbol		Parameter	SY10480-6 SY100480-6 SY101480-6		SY10480-8 SY100480-8 SY101480-8		SY10480-10 SY100480-10 SY101480-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	6	—	8	—	10	—	ns
tWS	TWLQL	Write Disable Time	—	3	—	4	—	5	ns
tWR	TWHQV	Write Recovery Time	—	5	—	5	—	5	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	1	—	1	—	1	—	ns
tSD	TDVWL	Data Set-up Time	1	—	1	—	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
6	SY10480-6DCF	Fast	D20-1	Commercial
6	SY100480-6DCF	Fast	D20-1	Commercial
6	SY101480-6DCF	Fast	D20-1	Commercial
8	SY10480-8DCF SY10480-8DCS	Fast Standard	D20-1	Commercial
8	SY100480-8DCF SY100480-8DCS	Fast Standard	D20-1	Commercial

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
8	SY101480-8DCF SY101480-8DCS	Fast Standard	D20-1	Commercial
10	SY10480-10DCS	Standard	D20-1	Commercial
10	SY100480-10DCS	Standard	D20-1	Commercial
10	SY101480-10DCS	Standard	D20-1	Commercial

SYxxx x 480 – xx x C x x

- Special Processing
- Edge Rate Identifier
  - F = Fast Edge Rate
  - S = Standard Edge Rate
- Temperature Range
  - C = Commercial
- Package Identifier
  - D = CERDIP
- Speed Identifier
  - e.g. 6 = 6ns Max. Access Time
- Device Type
- L = Low Power Designator (if any)
- Device Type Prefix
  - 10 = 10KH DC Levels with –5.2V ± 5% Supply
  - 100 = 100K DC Levels with –4.5V ± 0.3V Supply
  - 101 = 100K DC Levels with –5.2V ± 5% Supply

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FEATURES

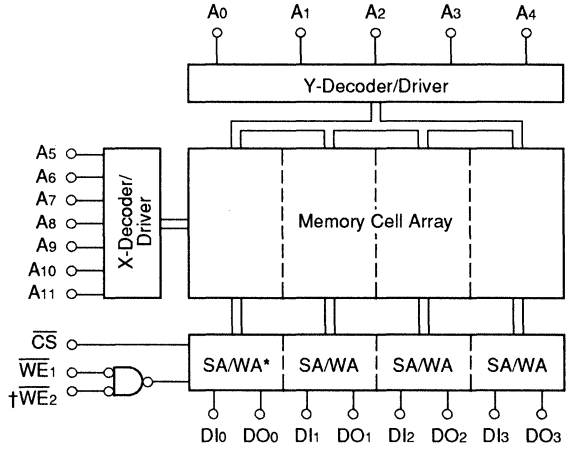
- **Address access time, t_{AA}: 4/5/6ns max.**
- **Chip select access time, t_{AC}: 3ns max.**
- **Edge rate, t_r/t_f: 500ps (typ.)**
- **Write recovery times under 5ns**
- **Power supply current, I_{EE}: –350mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic DIP, Flatpack, MLCC and ceramic SOIC**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10/100/101484 are 16384-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 4096-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100484 is also supply voltage-compatible with 100K ECL, while the SY101484 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101484 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

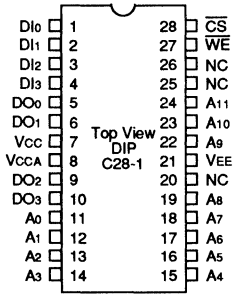
BLOCK DIAGRAM

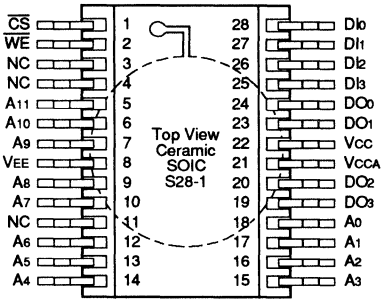


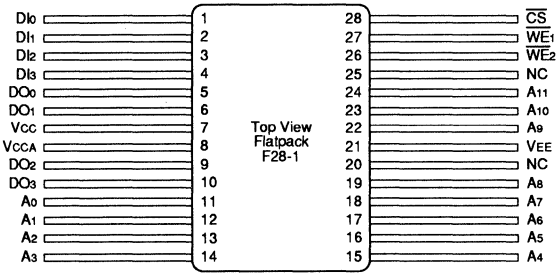
* SA = Sense Amplifier
WA = Write Amplifier
† $\overline{WE_2}$ is available on CERPACK only.

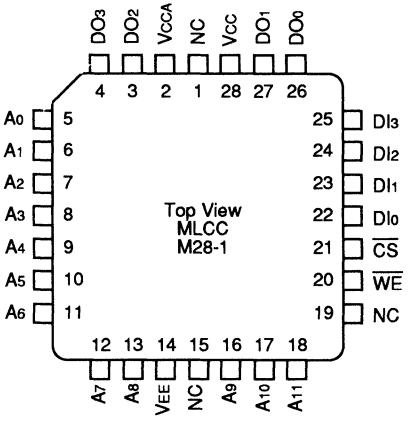
Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS









PIN NAMES

Label	Function
A0 - A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DI0 - DI3	Data Input (DIN)
DO0 - DO3	Data Output (DOUT)
VCC	GND (0V)
VCCA	Output GND (0V)
VEE	Supply Voltage
NC	No Connect

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TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}_{1,2}$	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101484 are 16384-bit RAMs organized as 4096-words-by-4-bits. Memory cell selection is achieved by using the 12 address bits designated as A_0 through A_{11}. Each of the 2^{12} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the DIN inputs (D_{I0} through D_{I3}) is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to DOUT (D_{O0} through D_{O3}) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	VIN	+0.5 to –2.0	V
DC Output Current (Output High)	IOUT	–30	mA
Temperature Under Bias	TC	–55 to +125	°C
Storage Temperature	Tstore	–65 to +150	°C

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage(1)	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	75	°C
Supply Voltage(1)	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		TC	0	—	85	°C
Supply Voltage(1)	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	85	°C

NOTE:
1. Referenced to V_{CC}.

RISE AND FALL TIME

Parameter	Code(1)	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
Output Fall Time	F	tf	—	500	—	ps

NOTE:
1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	CIN	—	4	—	pF
Output Pin Capacitance	COUT	—	5	—	pF

10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	0°C to +75°C	–350	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s

V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	–350	—	mA	All Inputs and Outputs Open

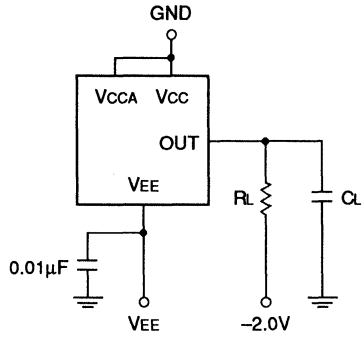
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

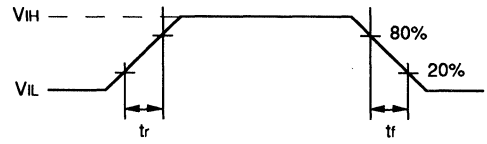
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to –2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	–0.933V –0.90V –0.863V	–1.733V –1.70V –1.663V
100/101K	0°C to +85°C	–0.90V	–1.70V

Loading Condition



Input Pulse



tr = tf = 1.0ns typ.

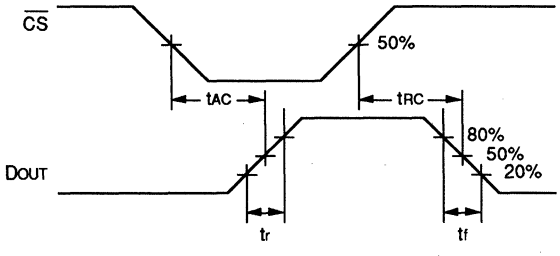
OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to –2V.)

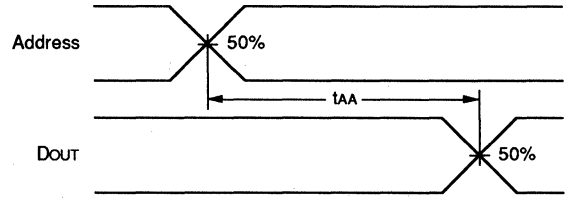
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10484-4 SY100484-4 SY101484-4		SY10484-5 SY100484-5 SY101484-5		SY10484-6 SY100484-6 SY101484-6		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	TAVQV	Address Access Time	—	4	—	5	—	6	ns
t_{AC}	TSLQV	Chip Select Access Time	—	3	—	3	—	3	ns
t_{RC}	TSHQL	Chip Select Recovery Time	—	3	—	3	—	3	ns

READ CYCLE TIMING DIAGRAM

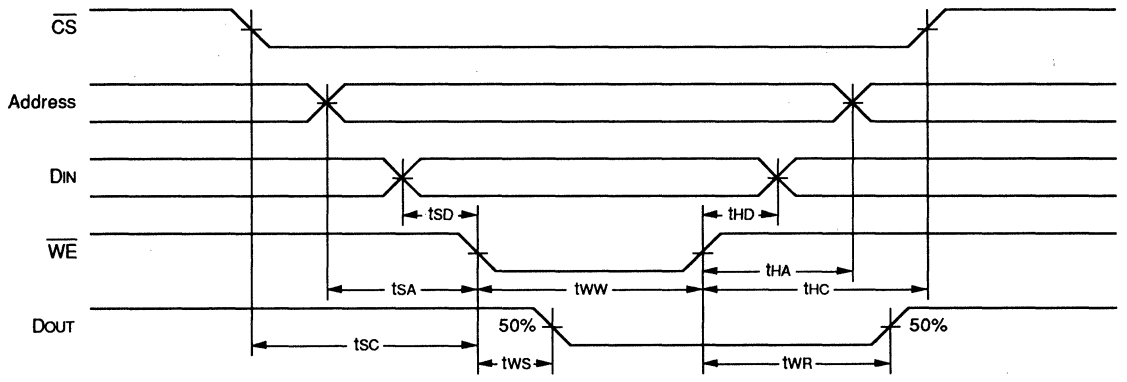




WRITE CYCLE

Symbol		Parameter	SY10484-4 SY100484-4 SY101484-4		SY10484-5 SY100484-5 SY101484-5		SY10484-6 SY100484-6 SY101484-6		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	4	—	5	—	6	—	ns
tWS	TWLQL	Write Disable Time	—	3	—	3	—	3	ns
tWR	TWHQV	Write Recovery Time	—	4	—	5	—	5	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	1	—	1	—	1	—	ns
tSD	TDVWL	Data Set-up Time	1	—	1	—	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



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PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
4	SY10484-4FCF	Fast	F28-1	Commercial
	SY10484-4SCF	Fast	S28-1	Commercial
	SY10484-4MCF	Fast	M28-1	Commercial
4	SY100484-4FCF	Fast	F28-1	Commercial
	SY100484-4SCF	Fast	S28-1	Commercial
	SY100484-MCF	Fast	M28-1	Commercial
4	SY101484-4FCF	Fast	F28-1	Commercial
	SY101484-4SCF	Fast	S28-1	Commercial
	SY101484-4MCF	Fast	M28-1	Commercial
5	SY10484-5CCF	Fast	C28-1	Commercial
	SY10484-5FCF	Fast	F28-1	Commercial
	SY10484-5SCF	Fast	S28-1	Commercial
	SY10484-5MCF	Fast	M28-1	Commercial
5	SY100484-5CCF	Fast	C28-1	Commercial
	SY100484-5FCF	Fast	F28-1	Commercial
	SY100484-5SCF	Fast	S28-1	Commercial
	SY100484-5MCF	Fast	M28-1	Commercial
5	SY101484-5CCF	Fast	C28-1	Commercial
	SY101484-5FCF	Fast	F28-1	Commercial
	SY101484-5SCF	Fast	S28-1	Commercial
	SY101484-5MCF	Fast	M28-1	Commercial
6	SY10484-6CCF	Fast	C28-1	Commercial
	SY10484-6FCF	Fast	F28-1	Commercial
	SY10484-6SCF	Fast	S28-1	Commercial
	SY10484-6MCF	Fast	M28-1	Commercial
6	SY100484-6CCF	Fast	C28-1	Commercial
	SY100484-6FCF	Fast	F28-1	Commercial
	SY100484-6SCF	Fast	S28-1	Commercial
	SY100484-6MCF	Fast	M28-1	Commercial
6	SY101484-6CCF	Fast	C28-1	Commercial
	SY101484-6FCF	Fast	F28-1	Commercial
	SY101484-6SCF	Fast	S28-1	Commercial
	SY101484-6MCF	Fast	M28-1	Commercial

SYxxx x 484 – xx x C x x

- Special Processing
- Edge Rate Identifier
  - F = Fast Edge Rate
  - S = Standard Edge Rate
- Temperature Range
  - C = Commercial
- Package Identifier
  - C = Ceramic Sidebraze DIP
  - F = CERPACK
  - M = MLCC (Metallic Leaded Chip Carrier)
  - S = Ceramic Gullwing SOIC
- Speed Identifier
  - e.g. 4 = 4ns Max. Access Time
- Device Type
- L = Low Power Designator (if any)
- Device Type Prefix
  - 10 = 10KH DC Levels with –5.2V ± 5% Supply
  - 100 = 100K DC Levels with –4.5V ± 0.3V Supply
  - 101 = 100K DC Levels with –5.2V ± 5% Supply

FEATURES

- **Extremely fast access times: t_{CHCH} = 5/6ns (max.)**
- **Extended supply voltage option: — V_{EE} = –5.2V**
- **Completely self-timed read and write cycle**
- **On-chip input and output registers**
- **Power supply current, I_{EE}: –400mA (-5), –350mA (-6)**
- **On-chip parity checking — with odd address parity mode pin**
- **Clock enable input simplifies pipeline control**
- **Scan diagnostics supported by on-chip scan registers**
- **High speed ceramic flatpack**
- **I/O compatible with 100K standard**
- **Built with advanced ASSET™ I technology**
- **ESD protection of 2000V**

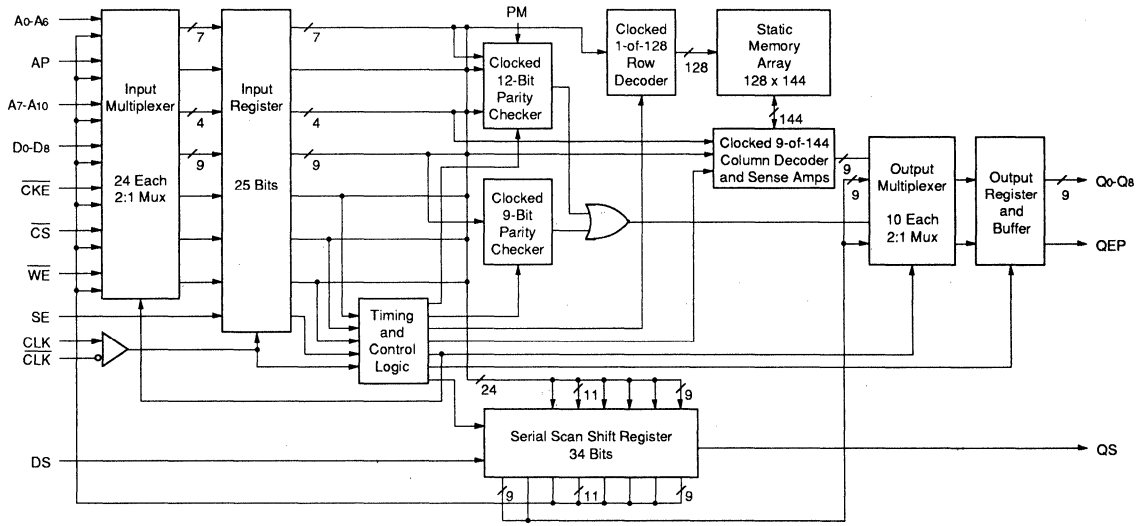
GENERAL DESCRIPTION

The SY101492 is an extremely high-performance 2K x 9 SRAM. It is the first of a family of similar 9-bit wide SRAMs designed specifically for very high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs and address translation lookaside buffers. The SY101492 offers several features which are very desirable in such applications.

The 101492 employs proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

FUNCTIONAL BLOCK DIAGRAM

Complete Functional Diagram



Rev.: B Amendment: /0
Issue Date: April, 1994

FUNCTIONAL DESCRIPTION

Advanced Self-timed Architecture

This advanced self-timed RAM simplifies the system design of extremely fast memory arrays by minimizing the impact of timing skews on the cycle time of the memory array. All input signals (address, data and control signals) are registered on-chip by a transition of the clock. By registering all inputs with minimal set-up and hold times (set-up + hold = 2ns) the troublesome skews inherent with traditional static RAM timing requirements are significantly reduced. With skew problems minimized, very short cycle times become practical. Output registers (self-timed on-chip) hold output data valid for an extended portion of the cycle, easing system read timing requirements.

Hidden Write Cycle Mode

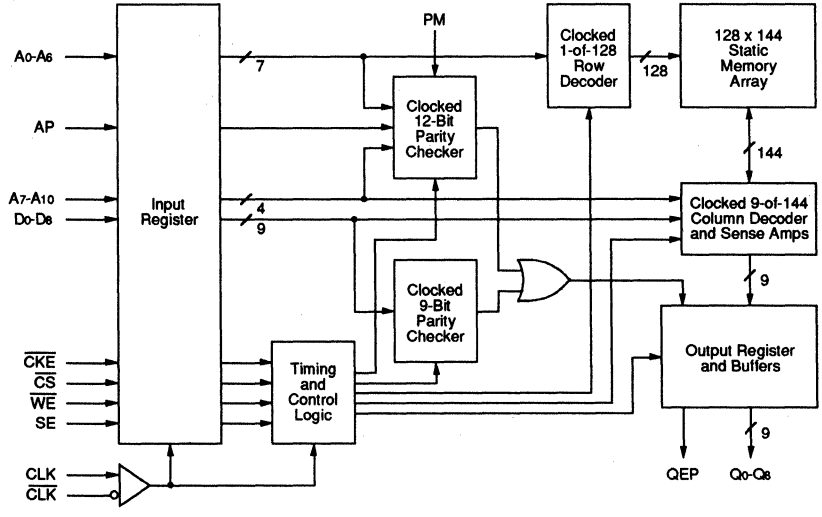
The hidden write cycle timing allows relaxed data bus timing. This will often ease system set-up and hold requirements for the data output bus. Hidden write timing is essentially a technique for interleaving reads and writes. This advanced self-timed SRAM supports hidden write timing more conveniently in the system than first generation self-timed SRAMs due to the unique control signal functions defined for write enable ($\overline{WE}$) and chip select ($\overline{CS}$). By keeping the output register active (with the last read data) during a write cycle, this device greatly simplifies the timing of interleaved memory architectures. This mode may be very useful in cache and register file applications, where multiple sources and/or destinations may be interleaved within each machine cycle.

Parity Checking

The device also offers several convenient features which may be useful in specific applications. One such feature is the on-chip parity checking function. For systems where parity checking is desirable, this device will check for odd parity on the 9-bit data input field and will check for either even or odd parity (depending on the polarity of the parity mode pin — PM) on the 11-bit address field combined with the address parity input. Odd parity is met when the number of highs in the field is odd. Address parity checking can be conveniently disabled if desired, allowing data field only parity checking. If either the data or address demonstrates a parity error, then the parity error output flag is set. The polarity of the error output flag facilitates emitter dot ORing several error outputs for minimal delay. The parity checking feature is benign in the sense that, if parity checking is not desired, the output can simply be ignored without detrimental effects to normal operation.

FUNCTIONAL BLOCK DIAGRAM

Scan Functions Excluded



FUNCTIONAL DESCRIPTION (Cont'd)

Serial Scan Diagnostics Registers

Another convenient feature provided on-chip is the scan diagnostics register. For system designs where scan diagnostics are included, this device allows observing the state of the input registers (scan out) and forcing the state of the input and output registers (scan in). For writable control store applications the control store can be loaded via the serial channel (scan in), simplifying circuit board layout by eliminating the wide parallel data input bus structure. For systems where scan diagnostics are not desired, the scan enable input can simply be left open allowing the on-chip pulldown device to disable scan functions and provide normal SRAM functionality.

Pipeline Control

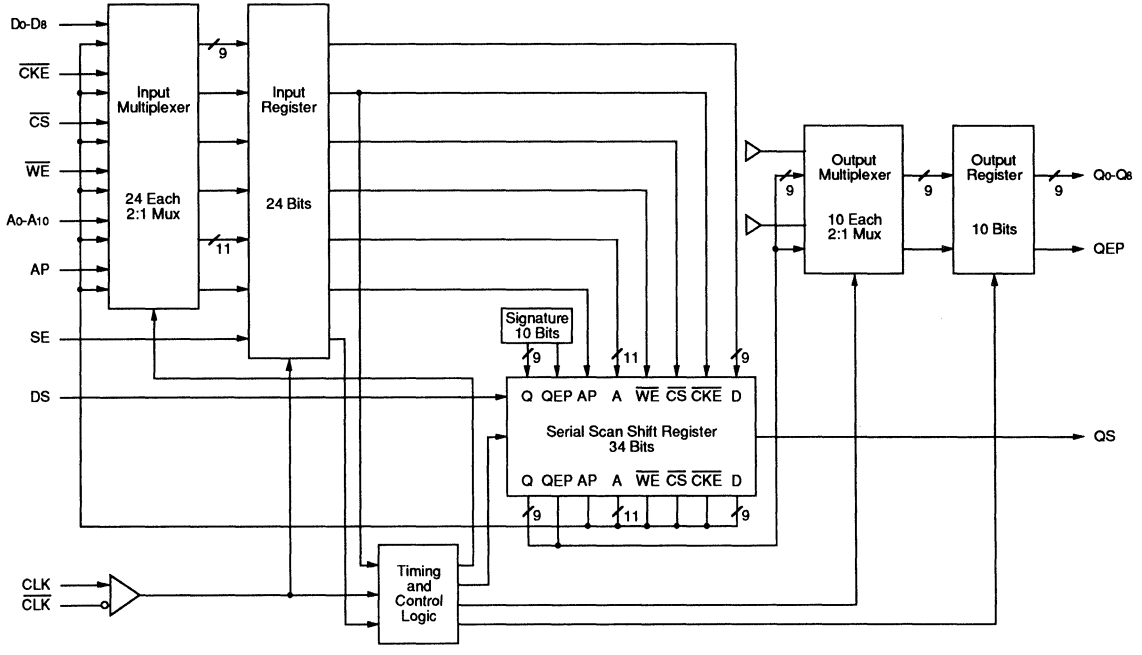
Yet a third convenient feature is the clock enable input. This control simplifies starting and stopping pipeline operations in pipelined systems. It reduces, and may eliminate, the need to gate the clock signal external to the RAM. This feature is also benign since the on-chip pulldown device will ensure normal operation if the clock enable is not used.

100K Compatible I/O

The device is I/O compatible with standard temperature compensated 100K ECL logic, allowing trouble free interfacing in high-performance ECL systems.

FUNCTIONAL BLOCK DIAGRAM

Scan Functions Only



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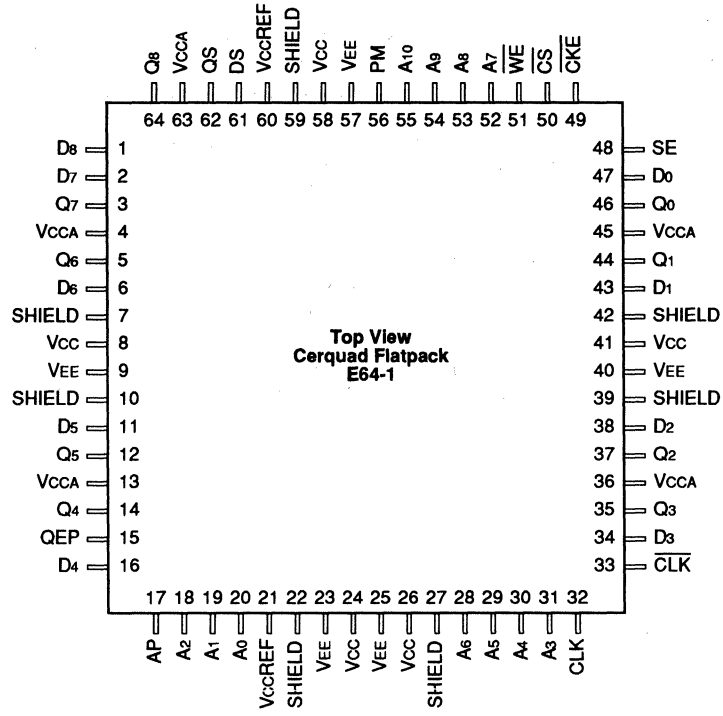
PIN CONFIGURATION



NOTES:
Pin 26 is reserved for (A11).
Pin 57 is reserved for (A12).

PIN DESCRIPTION

Inputs

All input signals are registered by the rising edge of the clock and the falling edge of the clock bar. Address, data in and control lines are all registered in exactly the same manner, and are all specified for exactly the same input set-up and hold requirements.

A_0-A_{10} **Address Inputs:** Used to select the memory location for storing or retrieving data.

AP **Address Parity Input:** Should be set/reset to ensure parity when combined with A_0-A_{10}. May also be tied to V_{EE} to disable parity checking of the address field. An internal pulldown is included to disable address parity checking when this input is not connected.

D_0-D_8 **Data Inputs:** During a write operation the data inputs are stored in the specified address location.

$\overline{CKE}$ **Clock Enable Input:** When active (low), this input allows the device to function normally with each rising edge of the clock. When inactive, this input will force the device to do nothing on each rising clock edge, thereby providing a convenient means for controlling the clock input to the device. Although this input functions as if it gates the clock on an off, this input actually is registered by the clock exactly as all other inputs and, as such, has the same input set-up and hold requirements as all other inputs. A natural assumption is that gating off the clock with the clock enable control will reduce the device power consumption substantially; but this assumption is, in fact, false. The state of the clock enable pin has very little effect on power consumption. An internal pulldown device is included to permit normal operation even when not connected.

$\overline{CS}$ **Chip Select Input:** Can be used to inhibit a write operation or to force the device outputs to a deselected (low) state when not writing. When active (low), each rising clock edge allows a write or read operation to occur. When inactive, a write operation is precluded. When inactive, and when Write Enable is also inactive, a deselect read operation will force the outputs to the inactive (low) state. An internal pulldown device is included to permit normal operation even when not connected.

$\overline{WE}$ **Write Enable Input:** When active (low), each rising clock edge allows a write operation to occur, but when active, the write function has no effect on the state of the data output pins. When inactive, each rising clock edge allows either a read operation or a deselect read operation to occur.

PM **Parity Mode Input:** When tied to V_{EE}, device will check for Odd parity on the address field. When tied to V_{CC}, device will check for Even parity on the address field.

CLK **Differential Clock Input:** The "true" side of the differential clock input.

$\overline{CLK}$ **Differential Clock Input:** The "complement" side of the differential clock input.

SE **Scan Enable Input:** Enables the serial scan diagnostics mode. With Scan Enable active (high), the contents of the scan shift register is shifted one position on each rising clock edge. The bit shifted out will appear on the QS pin and the bit shifted in will come from the DS pin. Information serially scanned into the device can be loaded into either the input register or the output register. An internal pulldown device is included to permit normal operation even when not connected.

DS **Serial Data Input:** When in scan diagnostics mode, this input allows serial shifting external data into the scan shift register.

Outputs

QS **Serial Data Output:** When in scan diagnostics mode, this output allows reading internal data directly from the scan shift register. In normal mode, QS will output the same logic level as the last registered value of D_8.

Q_0-Q_8 **Data Outputs:** These represent the contents of the addressed memory location during a read cycle. The outputs will not change unless another read cycle occurs, or unless the outputs are forced inactive (low) by a deselect read operation.

QEP **Parity Error Output:** Normally low, it goes high when the registered inputs have a parity error. For a read cycle, it indicates the address input has a parity error, since data input parity is only checked during write cycles. The parity error output delay approximates access time, appearing close to the time the data word appears in a read cycle. The parity error output signal will remain active (high) for a duration of the one cycle time, after which it may change back to inactive (low) if the next set of inputs contains no parity errors.

Power Supplies

V_{EE}	Negative Supply
V_{CC}	Positive Supply (Ground)
V_{CCREF}	Positive Supply (Ground)
V_{CCA}	Positive Supply (Ground) for output buffers only

Shield

Used to shield the input pins that are adjacent to V_{CC} and V_{EE} power pins from mutually coupled inductive noise. These pins should be connected to a DC power level or left floating, dependent on board layout convenience. Note that the pin marked PM is actually a shield pin but must be connected to the appropriate level to facilitate parity.

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TRUTH TABLES

Recall that all inputs are registered by a rising clock edge. The following truth tables illustrate device operation if the inputs shown are registered; the outputs shown will appear at access time.

Normal Operations[1]

Normal operations are defined by SE = LOW for prior and current cycle.

Inputs								Outputs		
$\overline{CKE}$	$\overline{CS}$	$\overline{WE}$	A	AP	PM	D	Data Parity	Q	QEP	Type of Operation
No Operation										
H	X	X	X	X	X	X	(X)	NC	NC	No Operation
Read										
L	L	H	V	O	VEE	X	(X)	V	L	Read
L	L	H	V	E	VCC	X	(X)	V	L	Read
L	H	H	X	X	X	X	(X)	L	L	Deselect
L	L	H	V	E	VEE	X	(X)	V	H	Read, A Parity Error
L	L	H	V	O	VCC	X	(X)	V	H	Read, A Parity Error
L	L	H	X	VEE	X	X	(X)	V	NC	Read, A Parity Disabled
Write										
L	L	L	V	O	VEE	V	(O)	NC	L	Write
L	L	L	V	E	VCC	V	(O)	NC	L	Write
L	H	L	X	X	X	X	(X)	NC	L	Write Inhibit
L	L	L	V	E	VEE	V	(O)	NC	H	Write, A Parity Error
L	L	L	V	O	VCC	V	(O)	NC	H	Write, A Parity Error
L	L	L	V	O	VEE	V	(E)	NC	H	Write, D Parity Error
L	L	L	V	E	VCC	V	(E)	NC	H	Write, D Parity Error

NOTE:

1. Special Characters: O = Odd, E = Even, NC = No Change, X = Don't Care, V = Valid

Scan Mode Operation[1]

Scan operation depends on current and prior states of SE (as registered by the rising edge of the clock), and on the state of the $\overline{CKE}$ bit after scan is completed (as scanned in serially):

Inputs				Outputs			
Prior SE	Current SE	Scanned $\overline{CKE}$	DS	QS	Q	QEP	Type of Operation
L	L	X	X	D8	X	X	Normal operation
L	H	X	V	D7	NC	NC	Enter scan mode and do first shift
H	H	X	V	V	NC	NC	Serial shift on each clock
H	L	L	X	V	V/NC	V/NC	Exit scan mode; do last shift and then execute instruction scanned into input register; if read or deselected, Q and QEP will update, else no change
H	L	H	V	V	V	V	Exit scan mode; do last shift and then copy scan register into Q and QEP; do not execute input instruction

NOTE:

1. Special Characters: O = Odd, E = Even, NC = No Change, X = Don't Care, V = Valid

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature	T_C	0	—	+85	°C

NOTE:

1. Referenced to V_{CC}.

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	3	—	pF
Output Pin Capacitance	C_{OUT}	—	3	—	pF

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V, V_{CCA} = 0V, V_{EE} = –5.2V, T_C = 0°C to +85°C, Airflow > 2.5m/s, Output Load = 50Ω to –2.0V

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Operating Current (–5)	T_{CHCH} = 5ns	I_{EEO}	–500	—	—	mA
Operating Current (–6)	T_{CHCH} = 6ns	I_{EEO}	–450	—	—	mA
Input LOW Current	—	I_{IL}	–50	—	+170	µA
Input HIGH Current	—	I_{IH}	—	—	+220	µA
Output HIGH Voltage	50Ω to –2V	V_{OH}	–1025	—	–880	mV
Output LOW Voltage	50Ω to –2V	V_{OL}	–1810	—	–1620	mV
Output HIGH Corner V	50Ω to –2V	V_{OHC}	–1025	—	—	mV
Output LOW Corner V	50Ω to –2V	V_{OLC}	—	—	–1620	mV
Input HIGH Voltage	—	V_{IH}	–1165	—	–880	mV
Input LOW Voltage	—	V_{IL}	–1810	—	–1475	mV

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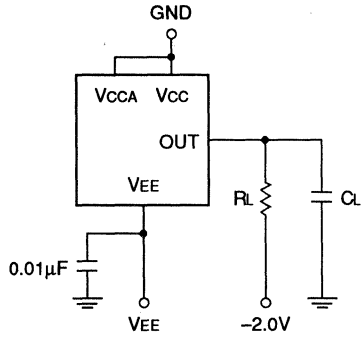
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

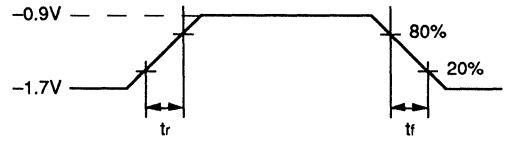
$V_{CC} = V_{CCA} = 0V$
$V_{EE} = -5.2V \pm 5\%$
Airflow > 2.5m/s

Output Load = 50Ω to −2.0V
T_C = 0°C to +85°C

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Description

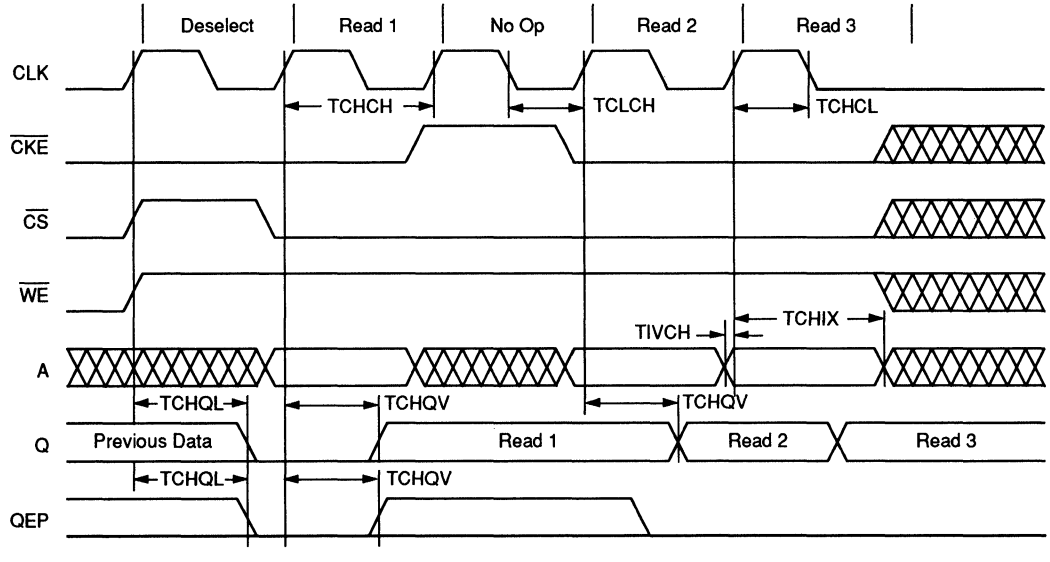
A read cycle is performed when the following conditions are present at the time the clock rising edge registers the inputs: $\overline{CKE}$ = Low, $\overline{CS}$ = Low, $\overline{WE}$ = High, SE = Low and was low for the previous cycle also. At access time the outputs become valid, making a single glitch-free transition from the previous state to the new state. A deselect read cycle is very similar to a read cycle except that $\overline{CS}$ = High and the outputs all go inactive (low) at access time. The minimum read cycle time realized in an application is largely a function of the system skews between inputs, and of set-up and hold requirements of the device to which the RAM provides data. If the address field and address parity bit combine to parity, then the parity error output will not assert, remaining low. The parity error output timing closely approximates access time and meets the same specifications.

AC CHARACTERISTICS (READ CYCLE)(1)

Symbol	Parameter	SY101492-5		SY101492-6		Unit
		Min.	Max.	Min.	Max.	
TCHCH	Cycle Time	5	—	6	—	ns
TCHQV	Access Time(2)	2.5	5	2.5	6	ns
TCHQL	Disable Time	2.5	5	2.5	6	ns
TIVCH	Input Set-up Time	0.5	—	0.5	—	ns
TCHIX	Input Hold Time	2	—	2	—	ns
TCHCL	Clock High Pulse Width	1.5	—	1.5	—	ns
TCLCH	Clock Low Pulse Width	1.5	—	1.5	—	ns
TCHQEPV	Parity Access(2)	2.5	5	2.5	6	ns

NOTES:

1. All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.
2. Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



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WRITE CYCLE

Description

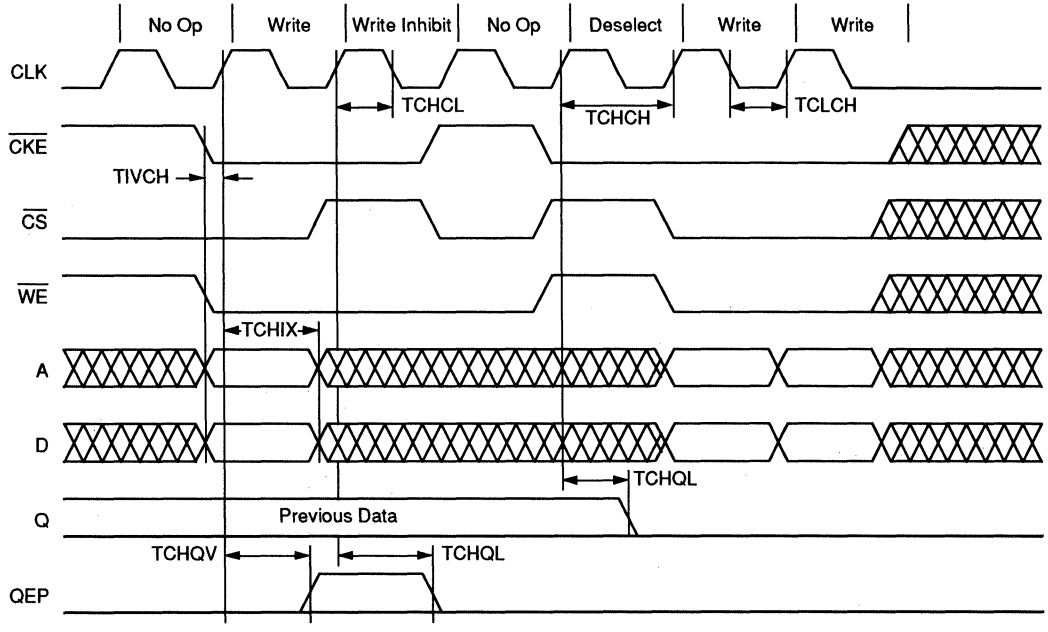
A write cycle is performed when the following conditions are present at the time the clock rising edge registers the inputs: $\overline{CKE}$ = Low, $\overline{CS}$ = Low, $\overline{WE}$ = Low, SE = Low and was low for the previous cycle also. The minimum write cycle time realized in an application is largely a function of the system skews on the inputs. Notice that a write cycle will not cause a change in any output except the parity error output; data outputs remain unchanged in any case. During writes, parity is checked on both the address field (combined with the address parity input) and the data field. The parity error output will not assert if both fields show parity. The parity error output timing closely approximates access time and meets the same access time specifications.

AC CHARACTERISTICS (WRITE CYCLE)[1]

Symbol	Parameter	SY101492-5		SY101492-6		Unit
		Min.	Max.	Min.	Max.	
TCHCH	Cycle Time	5	—	6	—	ns
TIVCH	Input Set-up Time	0.5	—	0.5	—	ns
TCHIX	Input Hold Time	2	—	2	—	ns
TCHCL	Clock High Pulse Width	1.5	—	1.5	—	ns
TCLCH	Clock Low Pulse Width	1.5	—	1.5	—	ns
TCHQV	Parity Access Time[2]	2.5	5	2.5	6	ns
TCHQL	Disable Time	2.5	5	2.5	6	ns

NOTES:

1. All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.
2. Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

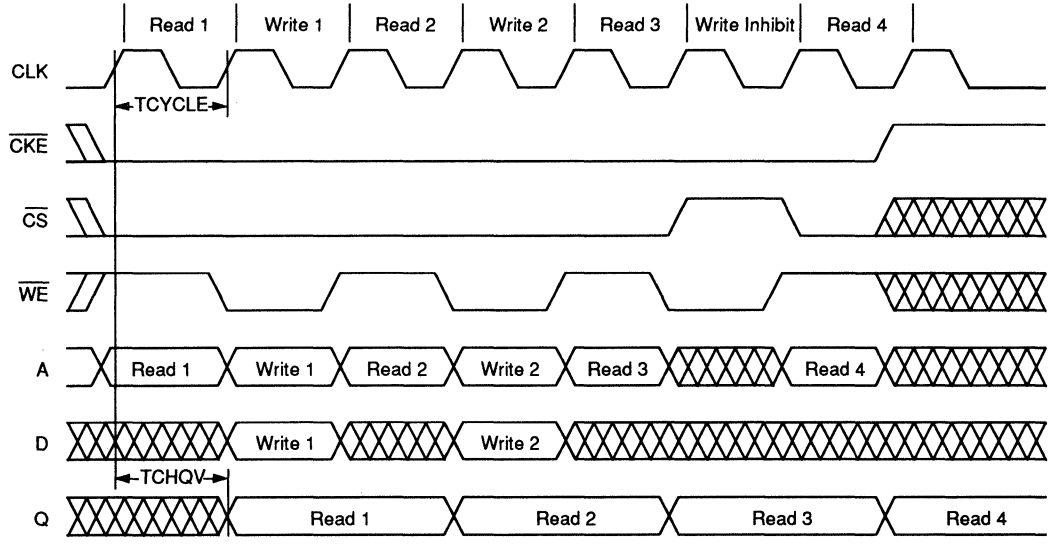


HIDDEN WRITE CYCLE

The hidden write cycle allows the SRAM to be operated at twice the bandwidth of the data output bus. With relaxed data bus timing (relative to the SRAM address and control input timing), system constraints of set-up and hold times may be much more easily met. Hidden write is a technique for interleaving read and write cycles in such a way that the write cycle timing has no effect on the data output bus (read timing). To allow hidden write operation, the definition of the functions performed by chip select ($\overline{CS}$) and write enable ($\overline{WE}$) are subtly but importantly different than implemented on common SRAMs.

With hidden write timing there are no unusual restrictions. Consecutive read and write cycles may be at different or at the same address location. If a read is not desired at any given moment, a read deselect or a no op may be executed instead. Similarly, if a write is unnecessary, a write inhibit or no op may be substituted.

Hidden write can provide throughput enhancement in certain cases. If, for example, the RAM is utilized as a register file and provides data to a pipelined ALU implemented in a gate array. If the ALU data input register requires 3ns set-up and 3ns hold, the total data input window required is 4ns wide. The SRAM maximum access is 7ns and the minimum access time is 2.5ns; the difference is the guaranteed data output valid window. In this example, the SRAM must be operated at greater than 9ns cycle time to allow room for data and clock skews. Depending on system details, a 10 or 11ns cycle could be practical. In contrast, using hidden write timing, the memory could be run at 7ns cycles with the data output bus cycle times of 14ns, easing the ALU set-up and hold times while allowing a store and a fetch every 14ns.



SCAN MODE

Description

The scan mode allows serial input and output for diagnostics or for loading RAM (e.g., in a writable control store application). In overview:

1. The first clock cycle with scan active (SE = High) causes the device to enter scan mode and serially shift.

2. Succeeding clock cycles with scan active cause serial shifting, and

3. The first clock cycle with scan inactive (SE = Low) causes the device to shift and then execute (conditionally) either the scanned-in instruction or to force the outputs to a scanned-in test vector (see truth table).

Several devices can be linked serially in a scan chain. A detailed description follows:

1. Scan bits are transferred from the input register to the scan serial register at the end of every regular read or write cycle. The device also transfers a fixed scan signature into the remaining bits of the serial scan register in preparation to also shift this data out (the remaining bits are those bits of the serial shift register which correspond with the output register).

2. On the first and each succeeding clock rising edge with scan active (SE = High), the device will shift the serial shift register one bit.

   A. The state of DS is shifted into the chain.

   B. The last bit of the chain is shifted out on QS.

   C. The other outputs remain unchanged. The rest of the RAM executes a no operation. It will not write regardless of the state of the bit in the WE location of the input register.

   D. Any number of shifts can occur in scan mode; two to infinite shifts are possible.

3. The first rising clock edge with scan inactive (SE = Low) causes the device to shift the scan chain and exit scan mode and to conditionally either:

   A. Execute the scanned-in instruction (e.g., read, write, deselect) with normal timing response (access, cycle) only if the scanned-in bit in the $\overline{CKE}$ location of the input register is active ($\overline{CKE}$ = Low). The output may be affected, according to the instruction executed. The contents of the scan register bits corresponding to the output register are ignored.

   Or:

   B. Transfer the contents of the scan register into the output buffer and ignore the contents of the input register only if the scanned in bit in the $\overline{CKE}$ location of the input register is inactive ($\overline{CKE}$ = High).

4. The second and succeeding clock cycles after scan is inactive (SE = Low) are defined as normal mode operations and do not cause any scan functions.

The scan sequence is:

Input DS

to Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7, Q_8, QEP,

to AP, A_2, A_1, A_0, A_6, A_5, A_4, A_3, A_{10}, A_9, A_8, A_7,

to $\overline{WE}$, $\overline{CS}$, $\overline{CKE}$,

to D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8,

to QS Output

The scan logic is designed to output a sequence of bits recognizable as a scan signature, intended as an aid in fault detection in those cases where the fault causes a malfunction in the serial scan chain. This bit sequence can be easily recognized by the scan diagnostics processor as it is shifted out, providing a reasonably sure method of determining where and/or if the serial scan chain is defective. The scan signature bit sequence corresponds to the outputs:

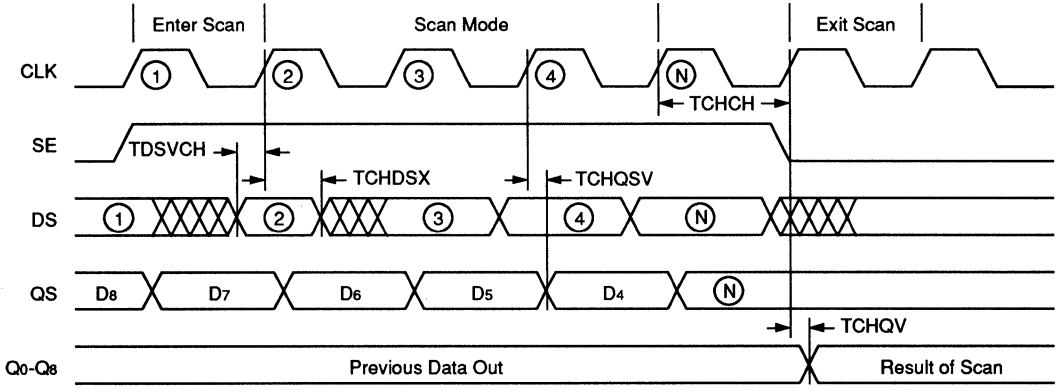
Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	QEP
H	L	L	H	L	H	L	H	H	L

AC CHARACTERISTICS (SCAN MODE)[1]

Symbol	Parameter	SY101492-5		SY101492-6		Unit
		Min.	Max.	Min.	Max.	
TCHCH	Serial Scan Mode Cycle Time	5	—	6	—	ns
TDSVCH	Serial Data Set-up Time	0.5	—	0.5	—	ns
TCHDSX	Serial Data Hold Time	2	—	2	—	ns
TCHQSV	Serial Output Delay Time[2]	2.5	5	2.5	6	ns

NOTES:

1. All maximum timing specs are referenced to the latter of CLK and $\overline{CLK}$, whichever occurs later. All minimum timing specs are referenced to the earlier of CLK and $\overline{CLK}$. CLK and $\overline{CLK}$ must cross each other between 10% and 90% of AC input levels.
2. Maximum access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.



RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
Output Fall Time	F	tf	—	500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

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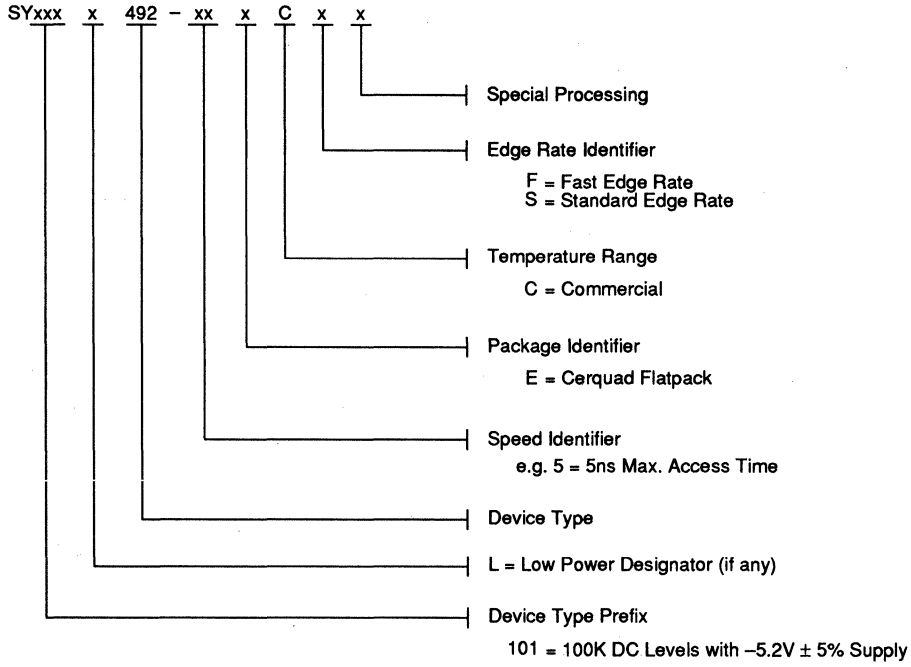
PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
5	SY101492-5ECF	Fast	E64-1	Commercial
6	SY101492-6ECF	Fast	E64-1	Commercial



FEATURES

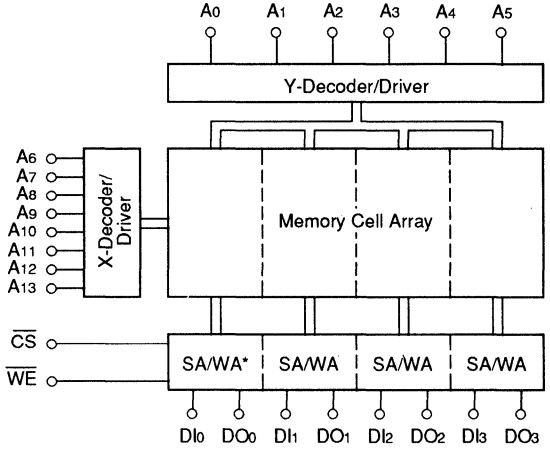
- **Address access time, t_{AA}: 6/7ns max.**
- **Chip select access time, t_{AC}: 3ns max.**
- **Edge rate, t_r/t_f: 500ps (typ.)**
- **Write recovery times under 5ns**
- **Power supply current, I_{EE}: –395mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Improved noise margins with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic DIP and Flatpack**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10/100/101494 are 65536-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 16384-words-by-4-bits and meet the standard 10K/100K family I/O signal levels. All devices feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101494 employ proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM

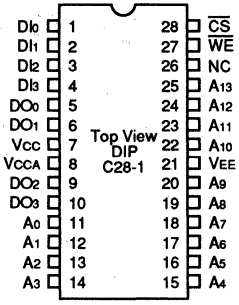


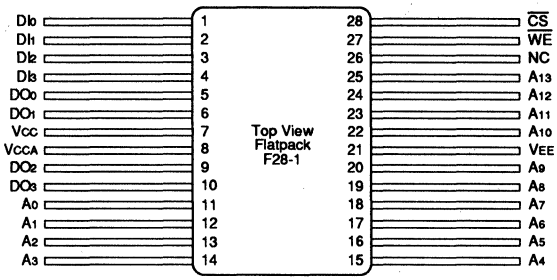
* SA = Sense Amplifier
WA = Write Amplifier

ASSET is a trademark of Synergy Semiconductor Corporation.

Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS





PIN NAMES

Label	Function
A_0 - A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DI_0 - DI_3	Data Input (D_{IN})
DO_0 - DO_3	Data Output (D_{OUT})
V_{CC}	GND (0V)
V_{CCA}	Output GND (0V)
V_{EE}	Supply Voltage
NC	No Connect

TRUTH TABLE

Input				
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101494 are 65536-bit RAMs organized as 16384-words-by-4-bits. Memory cell selection is achieved by using the 14 address bits designated as A_0 through A_{13}. Each of the 2^{14} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the D_{IN} inputs (DI_0 through DI_3) is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
VEE Pin Potential to VCC Pin	VEE	+0.5 to –7.0	V
Input Voltage	VIN	+0.5 to –2.0	V
DC Output Current (Output High)	IOUT	–30	mA
Temperature Under Bias	TC	–55 to +125	°C
Storage Temperature	Tstore	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage[1]	10K	VEE	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	75	°C
Supply Voltage[1]	100K	VEE	–4.8	–4.5	–4.2	V
Case Temperature		TC	0	—	85	°C
Supply Voltage[1]	101K	VEE	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	85	°C

NOTE:

1. Referenced to VCC.

RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
Output Fall Time	F	tf	—	500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	CIN	—	4	—	pF
Output Pin Capacitance	COUT	—	5	—	pF

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10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	0°C to +75°C	–395	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	–395	—	mA	All Inputs and Outputs Open

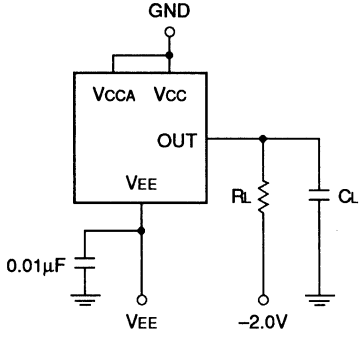
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

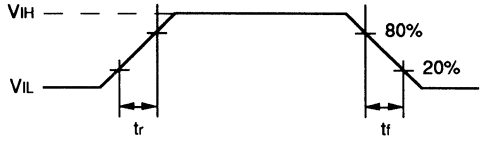
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C	−0.933V	−1.733V
	+25°C	−0.90V	−1.70V
	+75°C	−0.863V	−1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



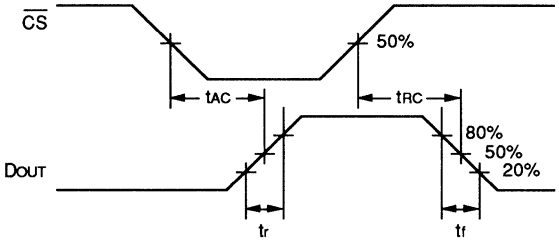
tr = tf = 1.0ns typ.
OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

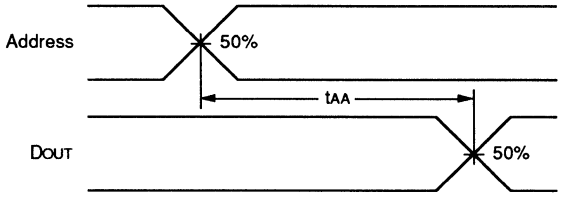
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10494-6 SY100494-6 SY101494-6		SY10494-7 SY100494-7 SY101494-7		Unit
			Min.	Max.	Min.	Max.	
t_{AA}	TAVQV	Address Access Time	—	6	—	7	ns
t_{AC}	TSLQV	Chip Select Access Time	—	3	—	3	ns
t_{RC}	TSHQL	Chip Select Recovery Time	—	3	—	3	ns

READ CYCLE TIMING DIAGRAM





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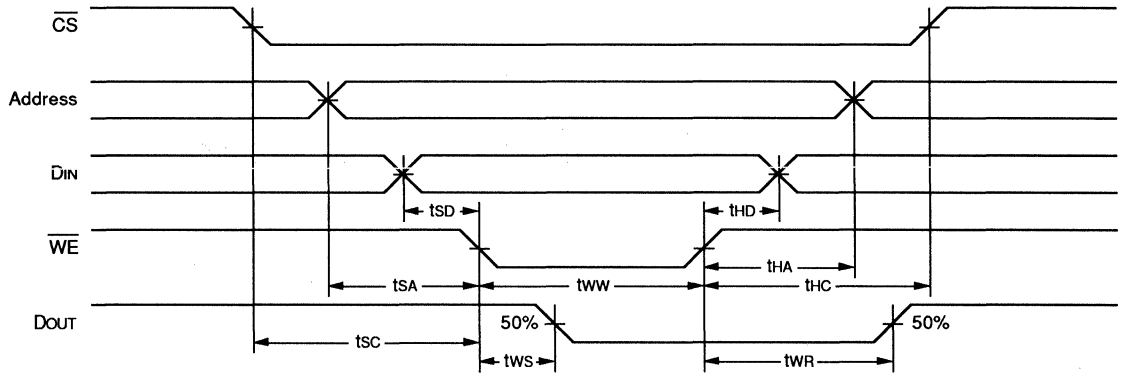
WRITE CYCLE

Symbol		Parameter	SY10494-6 SY100494-6 SY101494-6		SY10494-7 SY100494-7 SY101494-7		Unit
			Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	5	—	6	—	ns
tWS	TWLQL	Write Disable Time	—	3	—	3	ns
tWR	TWHQV	Write Recovery Time	—	5	—	5	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	1	—	1	—	ns
tSD	TDVWL	Data Set-up Time	1	—	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
6	SY10494-6CCF	Fast	C28-1	Commercial
	SY10494-6FCF	Fast	F28-1	Commercial
6	SY100494-6CCF	Fast	C28-1	Commercial
	SY100494-6FCF	Fast	F28-1	Commercial
6	SY101494-6CCF	Fast	C28-1	Commercial
	SY101494-6FCF	Fast	F28-1	Commercial

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
7	SY10494-7CCF	Fast	C28-1	Commercial
	SY10494-7FCF	Fast	F28-1	Commercial
7	SY100494-7CCF	Fast	C28-1	Commercial
	SY100494-7FCF	Fast	F28-1	Commercial
7	SY101494-7CCF	Fast	C28-1	Commercial
	SY101494-7FCF	Fast	F28-1	Commercial

SYxxx x 494 – xx x C x x

- Special Processing
- Edge Rate Identifier
  - F = Fast Edge Rate
  - S = Standard Edge Rate
- Temperature Range
  - C = Commercial
- Package Identifier
  - C = Ceramic Sidebraze DIP
  - F = CERPACK
- Speed Identifier
  - e.g. 6 = 6ns Max. Access Time
- Device Type
- L = Low Power Designator (if any)
- Device Type Prefix
  - 10 = 10KH DC Levels with –5.2V ± 5% Supply
  - 100 = 100K DC Levels with –4.5V ± 0.3V Supply
  - 101 = 100K DC Levels with –5.2V ± 5% Supply

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SYNERGY SEMICONDUCTOR

LOW-POWER 256 x 4 ECL RAM

SY10L422-5/7
SY100L422-5/7
SY101L422-5/7

FEATURES

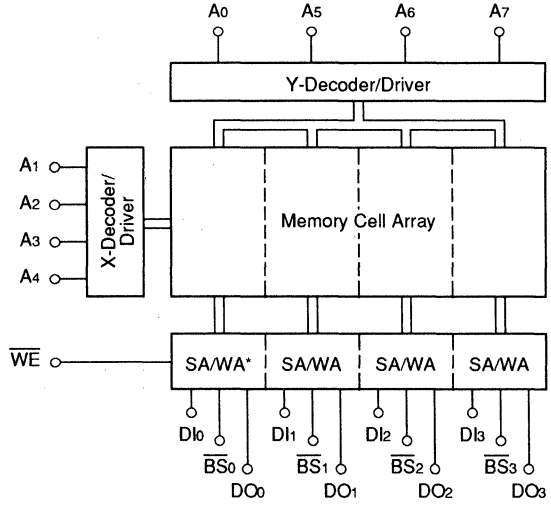
- **Address access time, t_{AA}: 5/7ns max.**
- **Block select access time, t_{AB}: 3ns max.**
- **Write pulse width, t_{WW}: 3.5/5ns min.**
- **Write recovery times under 5ns**
- **Low power supply current, I_{EE}: –150mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Includes popular Block Select function allowing individual read/write control over blocks**
- **Available in DIP, PLCC and ceramic Flatpack**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10L/100L/101L422 are 1024-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 256-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100L422 is also supply voltage-compatible with 100K ECL, while the SY101L422 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10L/100L/101L422 employs proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

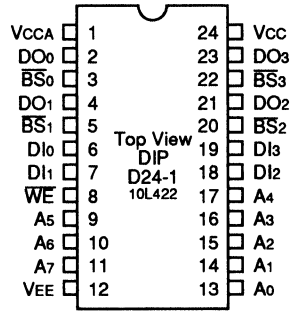
BLOCK DIAGRAM

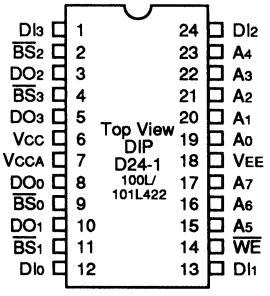


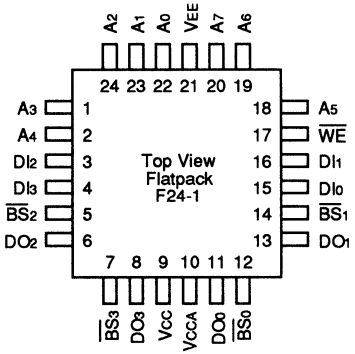
* SA = Sense Amplifier
WA = Write Amplifier

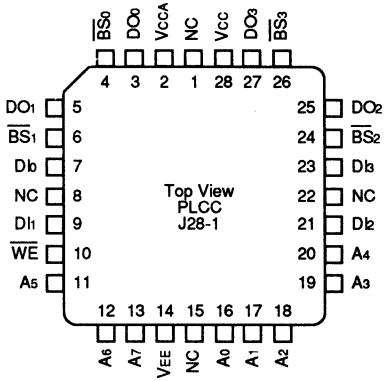
Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS









PIN NAMES

Label	Function
A_0 - A_7	Address Inputs
$\overline{BS}_0$ - $\overline{BS}_3$	Block Select ($\overline{BS}$)
$\overline{WE}$	Write Enable
DI_0 - DI_3	Data Input (D_{IN})
DO_0 - DO_3	Data Output (D_{OUT})
V_{CC}	GND (0V)
V_{CCA}	Output GND (0V)
V_{EE}	Supply Voltage
NC	No Connect

TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

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FUNCTIONAL DESCRIPTION

The Synergy SY10L/100L/101L422 are 1024-bit RAM organized as four 256-by-1-bit blocks with each block having its own Block Select ($\overline{BS}$) control signal that functions essentially like a unique chip select for the Block. The four blocks and Block Selects together make the device a 256 x 4-bit RAM. Memory cell selection is achieved by using the 8 address bits designated as A_0 through A_7. Each of the 2^8 possible input address combinations corresponds to a unique word location in memory. The active low Block Select ($\overline{BS}$) control signals are provided for memory expansion and for independent control of each of the four 256 x 1-bit blocks of memory. The active low Write Enable ($\overline{WE}$) controls the read and write operation on the selected block or blocks. Data resident on the D_{IN} inputs (DI_0 through DI_3) is written into the addressed location only when $\overline{WE}$ and the Block Select ($\overline{BS}$) associated with each of the D_{IN} bits is held LOW. This allows control of the Write operation to any one, two, three or all four of the input data bits. In order to perform a read operation, $\overline{WE}$ is held high, the Block Select ($\overline{BS}$) associated with each of the four output blocks is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. This allows control of the Read operation to any one, two, three or all four of the output blocks. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

All outputs are forced to a logic LOW level when the RAM is being written into ($\overline{WE}$ = LOW). The output (or outputs) associated with a block (or blocks) of memory can be forced to a logic LOW low level by deselecting that block (or blocks) with its respective Block Select input ($\overline{BS_0}$ – $\overline{BS_3}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	75	°C
Supply Voltage(1)	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		T_C	0	—	85	°C
Supply Voltage(1)	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	85	°C

NOTE:

1. Referenced to V_{CC}.

RISE AND FALL TIME

Parameter	Code(1)	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	S	t_r	—	1500	—	ps
Output Fall Time	S	t_f	—	1500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	5	—	pF

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10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to+ 75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{BS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{BS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	0°C to +75°C	–150	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{BS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{BS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	–150	—	mA	All Inputs and Outputs Open

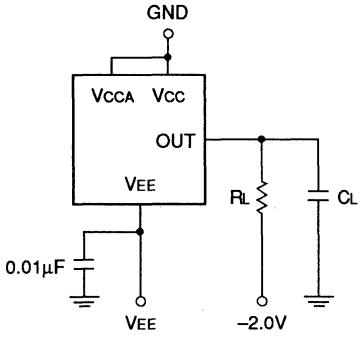
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

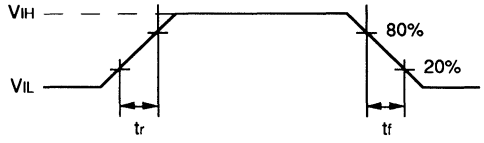
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10L422-5 SY100L422-5 SY101L422-5		SY10L422-7 SY100L422-7 SY101L422-7		Unit
			Min.	Max.	Min.	Max.	
t_{AA}	TAVQV	Address AccessTime	—	5	—	7	ns
t_{AB}	TBSLQV	Block Select AccessTime	—	3	—	3	ns
t_{RB}	TBSHQL	Block Select Recovery Time	—	3	—	3	ns

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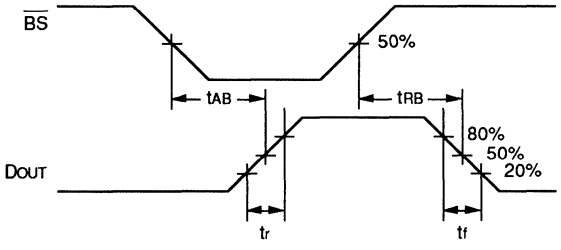
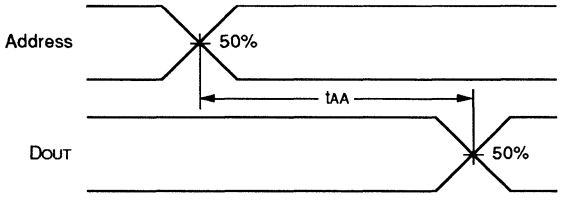
READ CYCLE TIMING DIAGRAM

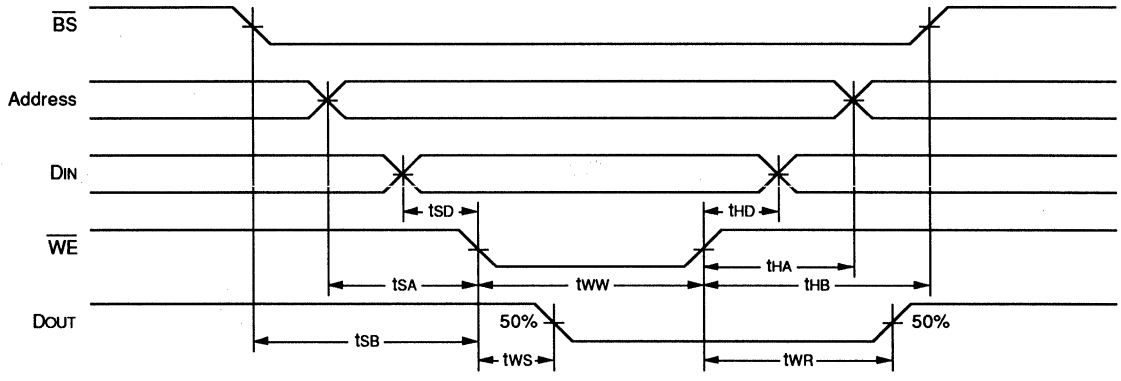




WRITE CYCLE

Symbol		Parameter	SY10L422-5 SY100L422-5 SY101L422-5		SY10L422-7 SY100L422-7 SY101L422-7		Unit
			Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	3.5	—	5	—	ns
tWS	TWLQL	Write Disable Time	—	3.5	—	4	ns
tWR	TWHQV	Write Recovery Time	—	3.5	—	4	ns
tSA	TAVWL	Address Set-up Time	0.5	—	1	—	ns
tSB	TBSLWL	Block Select Set-up Time	0.5	—	1	—	ns
tSD	TDVWL	Data Set-up Time	0.5	—	1	—	ns
tHA	TWHAX	Address Hold Time	1.0	—	1	—	ns
tHB	TWHBSX	Block Select Hold Time	1.0	—	1	—	ns
tHD	TWHDX	Data Hold Time	1.0	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM

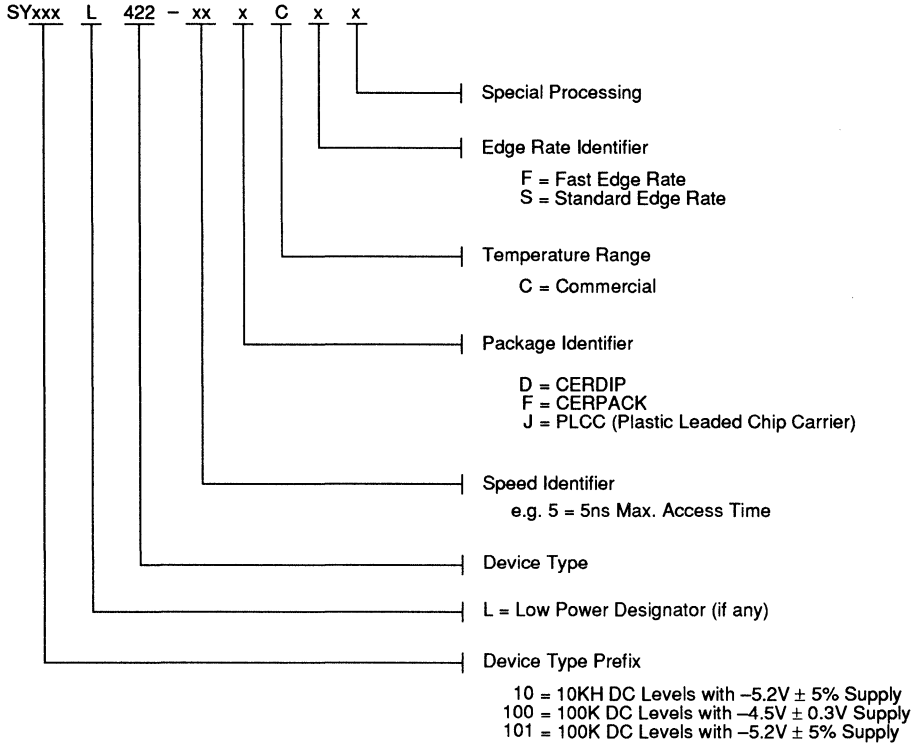


PRODUCT ORDERING CODE

Speed (ns)	Ordering Code[1]	Edge Rate	Package Type	Operating Range
5	SY10L/100L/101L422-5DCS	Standard	D24-1	Commercial
	SY10L/100L/101L422-5FCS	Standard	F24-1	Commercial
	SY10L/100L/101L422-5JCS	Standard	J28-1	Commercial
7	SY10L/100L/101L422-7DCS	Standard	D24-1	Commercial
	SY10L/100L/101L422-7FCS	Standard	F24-1	Commercial
	SY10L/100L/101L422-7JCS	Standard	J28-1	Commercial

NOTE:

1. Device marking will not include "SY" prefix.



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SYNERGY SEMICONDUCTOR

LOW-POWER 1K x 4 ECL RAM

SY10L474-5/7
SY100L474-5/7
SY101L474-5/7

FEATURES

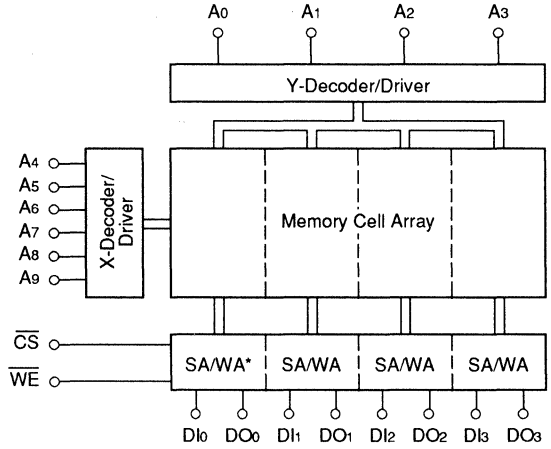
- **Address access time, t_{AA}: 5/7ns max.**
- **Chip select access time, t_{AC}: 3ns max.**
- **Write pulse width, t_{WW}: 5ns min.**
- **Write recovery times under 5ns**
- **Low power supply current, I_{EE}: –180mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in DIP, PLCC and ceramic Flatpack**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10L/100L/101L474 are 4096-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 1024-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100L474 is also supply voltage-compatible with 100K ECL, while the SY101L474 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10L/100L/101L474 employs proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

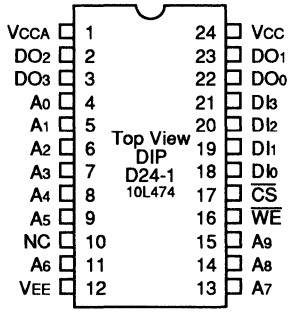
BLOCK DIAGRAM

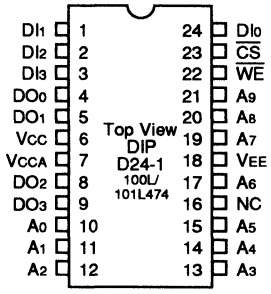


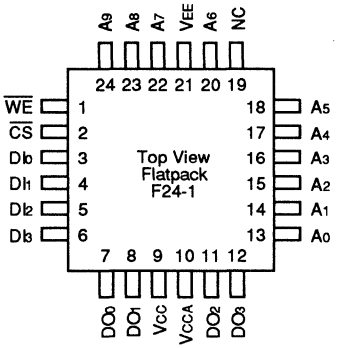
* SA = Sense Amplifier
WA = Write Amplifier

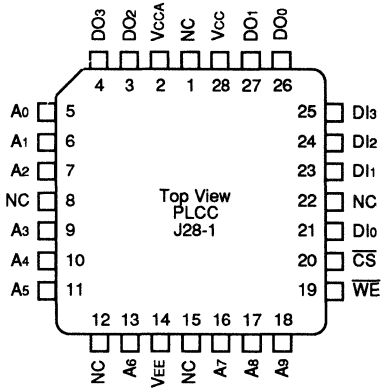
Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS









PIN NAMES

Label	Function
A0 - A9	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DI0 - DI3	Data Input (DIN)
DO0 - DO3	Data Output (DOUT)
VCC	GND (0V)
VCCA	Output GND (0V)
VEE	Supply Voltage
NC	No Connect

TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

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FUNCTIONAL DESCRIPTION

The Synergy SY10L/100L/101L474 are 4096-bit RAMs organized as 1024-words-by-4-bits. Memory cell selection is achieved by using the 10 address bits designated as A_0 through A_9. Each of the 2^{10} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the D_{IN} inputs (DI_0 through DI_3) is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
VEE Pin Potential to VCC Pin	VEE	+0.5 to –7.0	V
Input Voltage	VIN	+0.5 to VEE	V
DC Output Current (Output High)	IOUT	–30	mA
Temperature Under Bias	TC	–55 to +125	°C
Storage Temperature	Tstore	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage [1]	10K	VEE	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	75	°C
Supply Voltage[1]	100K	VEE	–4.8	–4.5	–4.2	V
Case Temperature		TC	0	—	85	°C
Supply Voltage[1]	101K	VEE	–5.46	–5.2	–4.94	V
Case Temperature		TC	0	—	85	°C

NOTE:

1. Referenced to VCC.

RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	S	tr	—	1500	—	ps
Output Fall Time	S	tf	—	1500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	CIN	—	4	—	pF
Output Pin Capacitance	COUT	—	5	—	pF

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10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	0°C to +75°C	–180	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	–180	—	mA	All Inputs and Outputs Open

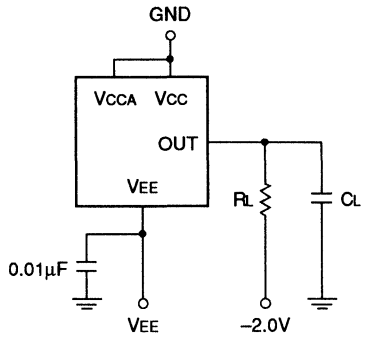
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

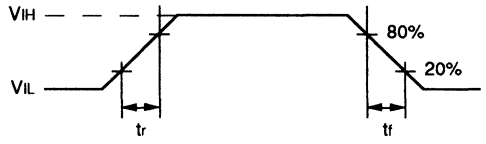
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

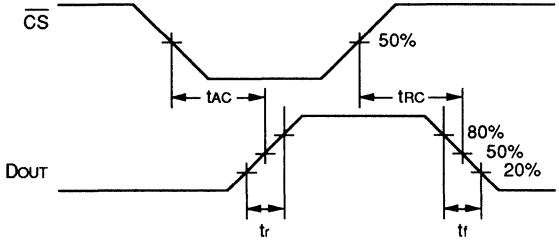
OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

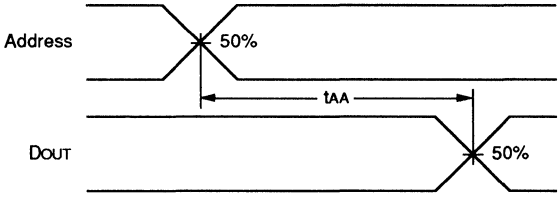
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10L474-5 SY100L474-5 SY101L474-5 Min.	SY10L474-5 SY100L474-5 SY101L474-5 Max.	SY10L474-7 SY100L474-7 SY101L474-7 Min.	SY10L474-7 SY100L474-7 SY101L474-7 Max.	Unit
t_{AA}	TAVQV	Address AccessTime	—	5	—	7	ns
t_{AC}	TSLQV	Chip Select AccessTime	—	3	—	3	ns
t_{RC}	TSHQL	Chip Select Recovery Time	—	3	—	3	ns

READ CYCLE TIMING DIAGRAM





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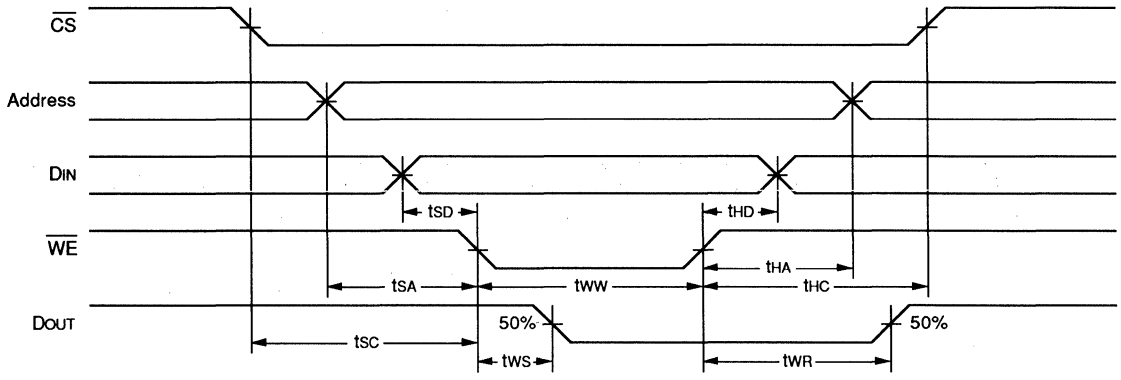
WRITE CYCLE

Symbol		Parameter	SY10L474-5 SY100L474-5 SY101L474-5		SY10L474-7 SY100L474-7 SY101L474-7		Unit
			Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	5	—	5	—	ns
tWS	TWLQL	Write Disable Time	—	3	—	4	ns
tWR	TWHQV	Write Recovery Time	—	5	—	5	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	0	—	0	—	ns
tSD	TDVWL	Data Set-up Time	0	—	0	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM

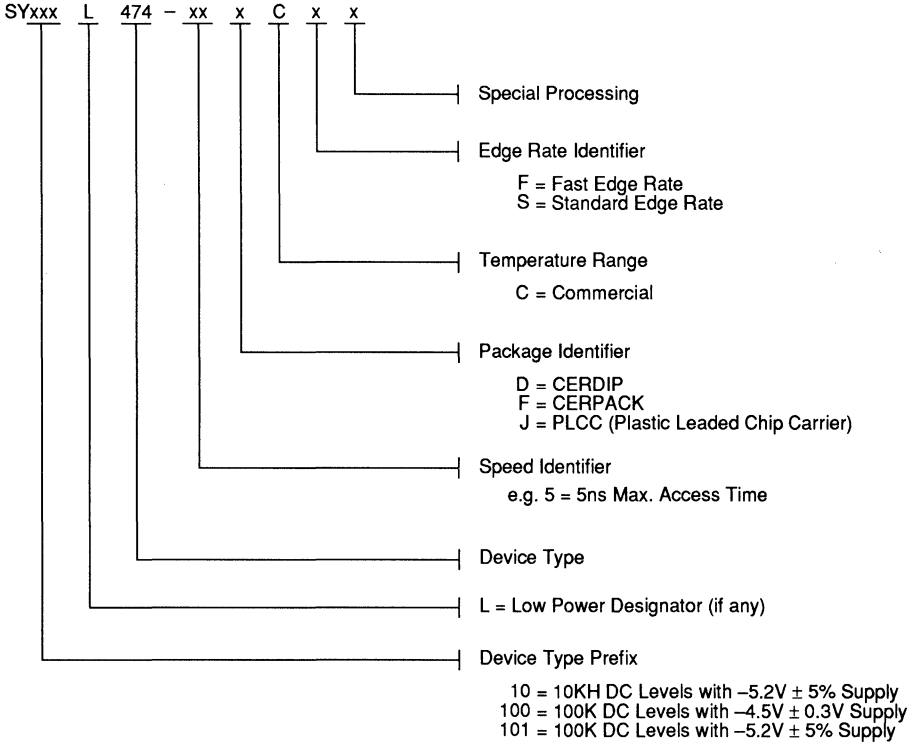


PRODUCT ORDERING CODE

Speed (ns)	Ordering Code[1]	Edge Rate	Package Type	Operating Range
5	SY10L/100L/101L474-5DCS	Standard	D24-1	Commercial
	SY10L/100L/101L474-5FCS	Standard	F24-1	Commercial
	SY10L/100L/101L474-5JCS	Standard	J28-1	Commercial
7	SY10L/100L/101L474-7DCS	Standard	D24-1	Commercial
	SY10L/100L/101L474-7FCS	Standard	F24-1	Commercial
	SY10L/100L/101L474-7JCS	Standard	J28-1	Commercial

NOTE:

1. Device marking will not include "SY" prefix.



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FEATURES

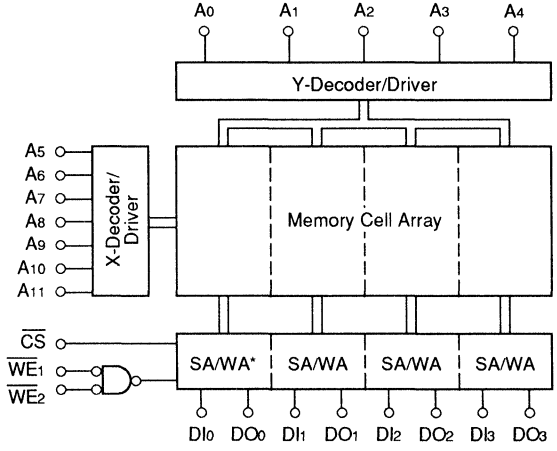
- **Address access time, t_{AA}: 7/8/10ns max.**
- **Chip select access time, t_{AC}: 3ns max.**
- **Write recovery times under 5ns**
- **Low power supply current, I_{EE}: –220mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic DIP, SOJ and ceramic Flatpack**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10L/100L/101L484 are 16384-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 4096-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100L484 is also supply voltage-compatible with 100K ECL, while the SY101L484 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10L/100L/101L484 employs proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

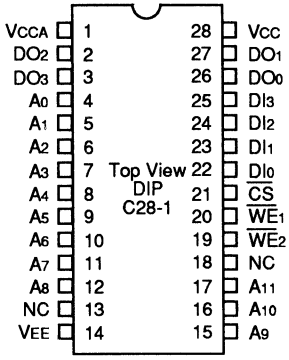
BLOCK DIAGRAM

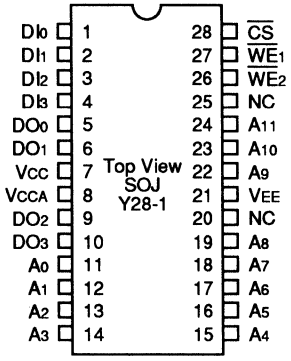


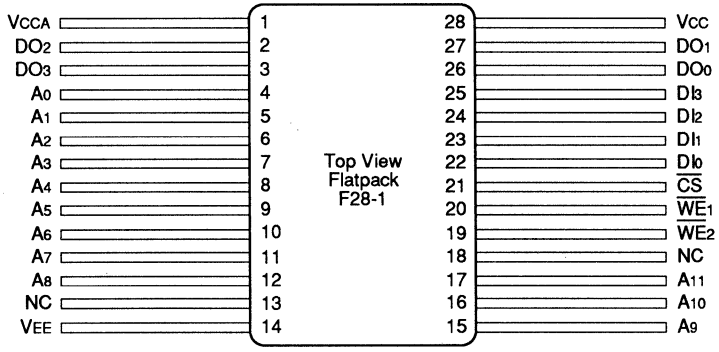
* SA = Sense Amplifier
WA = Write Amplifier

Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS







PIN NAMES

Label	Function
A_0 - A_{11}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE_1}$, $\overline{WE_2}$	Write Enable ($\overline{WE}$)
DI_0 - DI_3	Data Input (D_{IN})
DO_0 - DO_3	Data Output (D_{OUT})
V_{CC}	GND (0V)
V_{CCA}	Output GND (0V)
V_{EE}	Supply Voltage
NC	No Connect

TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE_{1,2}}$	D_{IN}		
H	X	X	L	Disabled
L	L*	H	L	Write "H"
L	L*	L	L	Write "L"
L	H*	X	D_{OUT}	Read

NOTE:

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
*L = Both $\overline{WE_1}$ and $\overline{WE_2}$ are Low
*H = Either $\overline{WE_1}$ or $\overline{WE_2}$ is High

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FUNCTIONAL DESCRIPTION

The Synergy SY10L/100L/101L484 is a 16,384-bit RAM organized as 4,096-words-by-4-bits. Memory cell selection is achieved by using the 12 address bits designated as A_0 through A_{11}. Each of the 2^{12} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The two active low Write Enable signals ($\overline{WE_1}$/$\overline{WE_2}$) control the read and write operation. Data resident on the D_{IN} inputs (D_{I0} through D_{I3}) is written into the addressed location only when $\overline{WE_1}$, $\overline{WE_2}$ and $\overline{CS}$ are held low. In order to perform a read operation, either $\overline{WE_1}$ or $\overline{WE_2}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (D_{O0} through D_{O3}) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE_1}$ = $\overline{WE_2}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage[1]	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	75	°C
Supply Voltage[1]	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		T_C	0	—	85	°C
Supply Voltage[1]	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	85	°C

NOTE:

1. Referenced to V_{CC}.

RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	S	t_r	—	1500	—	ps
Output Fall Time	S	t_f	—	1500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	5	—	pF

10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = −5.2V; Airflow > 2.5m/s; Output Load = 50Ω to −2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	−1020 −980 −920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	−1645 −1630 −1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	−2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	−2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	0°C to +75°C	−220	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = −4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = −5.2V (101K) Output Load = 50Ω to −2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	−1025	−880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	−1810	−1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	−1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	−1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	−1165	−880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	−1810	−1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	−2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	−2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	−220	—	mA	All Inputs and Outputs Open

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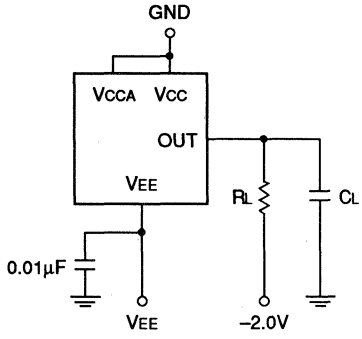
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

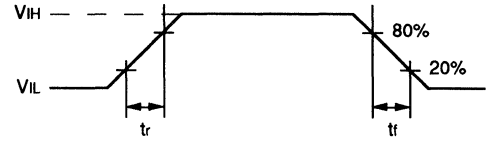
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



tr = tf = 1.0ns typ.

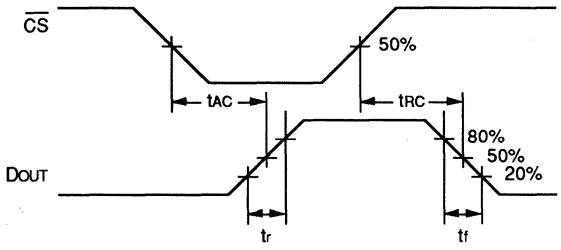
OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

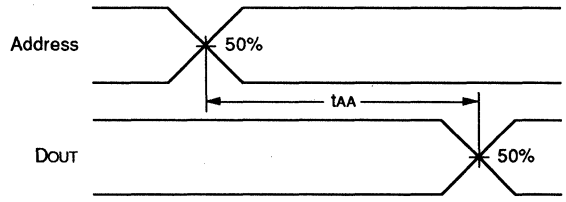
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10L484-7 SY100L484-7 SY101L484-7		SY10L484-8 SY100L484-8 SY101L484-8		SY10L484-10 SY100L484-10 SY101L484-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	TAVQV	Address AccessTime	—	7	—	8	—	10	ns
t_{AC}	TSLQV	Chip Select AccessTime	—	3	—	3	—	3	ns
t_{RC}	TSHQL	Chip Select Recovery Time	—	3	—	3	—	3	ns

READ CYCLE TIMING DIAGRAM

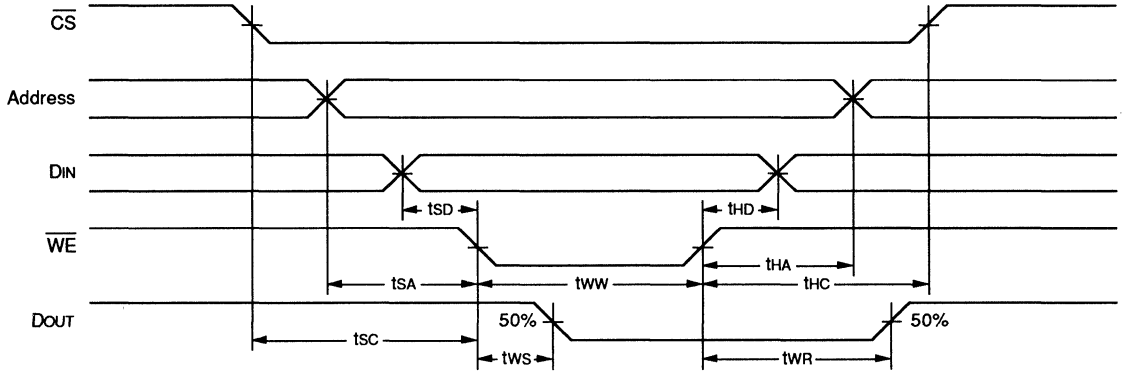




WRITE CYCLE

Symbol		Parameter	SY10L484-7 SY100L484-7 SY101L484-7		SY10L484-8 SY100L484-8 SY101L484-8		SY10L484-10 SY100L484-10 SY101L484-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tWW	TWLWH	Write Pulse Width	5	—	6	—	8	—	ns
tWS	TWLQL	Write Disable Time	—	5	—	5	—	5	ns
tWR	TWHQV	Write Recovery Time	—	5	—	5	—	5	ns
tSA	TAVWL	Address Set-up Time	1	—	1	—	1	—	ns
tSC	TSLWL	Chip Select Set-up TiLe	0	—	0	—	0	—	ns
tSD	TDVWL	Data Set-up Time	0	—	0	—	0	—	ns
tHA	TWHAX	Address Hold Time	1	—	1	—	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	1	—	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	1	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



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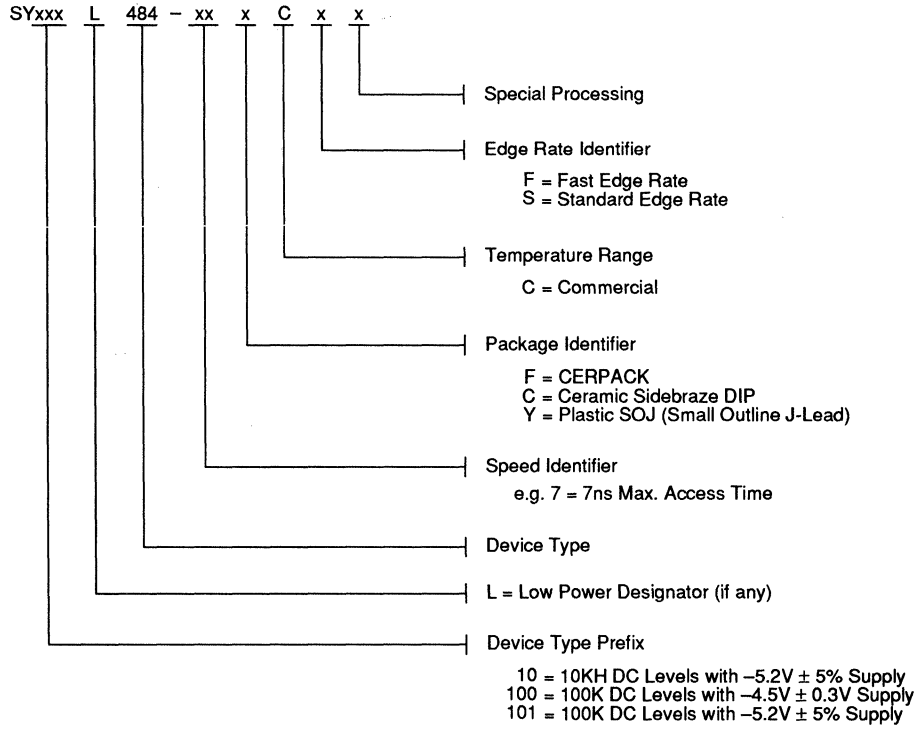
PRODUCT ORDERING CODE

Speed (ns)	Ordering Code[1]	Edge Rate	Package Type	Operating Range
7	SY10L/100L/101L484-7CCS	Standard	C28-1	Commercial
	SY10L/100L/101L484-7FCS	Standard	F28-1	Commercial
	SY10L/100L/101L484-7YCS	Standard	Y28-1	Commercial
8	SY10L/100L/101L484-8CCS	Standard	C28-1	Commercial
	SY10L/100L/101L484-8FCS	Standard	F28-1	Commercial
	SY10L/100L/101L484-8YCS	Standard	Y28-1	Commercial
10	SY10L/100L/101L484-10CCS	Standard	C28-1	Commercial
	SY10L/100L/101L484-10FCS	Standard	F28-1	Commercial
	SY10L/100L/101L484-10YCS	Standard	Y28-1	Commercial

NOTE:

1. Device marking will not include "SY" prefix.



LOW-POWER 16K x 4 ECL RAM

SY10L494-10
SY100L494-10
SY101L494-10

FEATURES

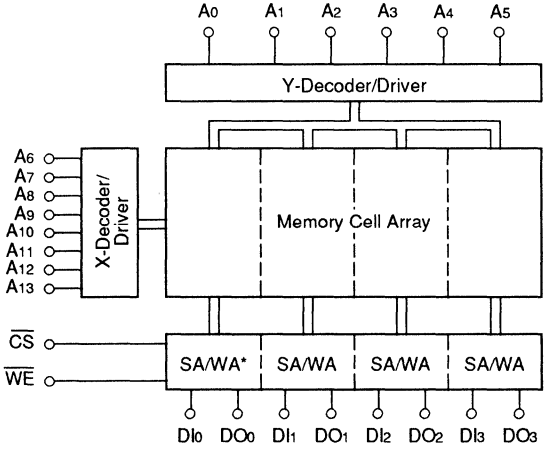
- **Address access time, t_{AA}: 10ns max.**
- **Chip select access time, t_{AC}: 3ns max.**
- **Write recovery times under 5ns**
- **Low power supply current, I_{EE}: –220mA**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ I technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Improved noise margins with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Available in hermetic DIP, SOJ and ceramic Flatpack**
- **ESD protection of 2000V**

DESCRIPTION

The Synergy SY10L/100L/101L494 are 65536-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 16384-words-by-4-bits and meet the standard 10K/100K family I/O signal levels. All devices feature on-chip voltage and temperature compensation for improved noise margin.

The SY10L/100L/101L494 employs proprietary circuit design techniques and Synergy's proprietary ASSET I advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET I uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



* SA = Sense Amplifier
WA = Write Amplifier

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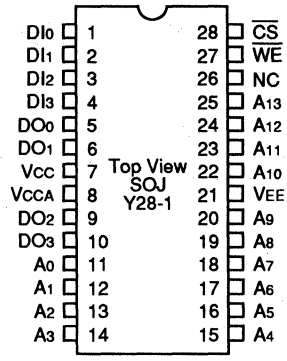
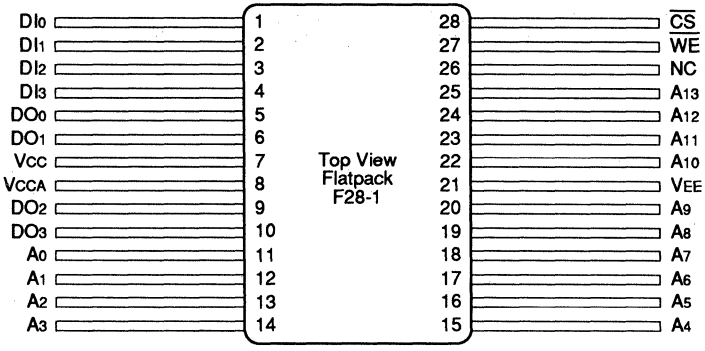
Rev.: B Amendment: /0
Issue Date: April, 1994

PIN CONFIGURATIONS





PIN NAMES

Label	Function
A_0 - A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
DI_0 - DI_3	Data Input (D_{IN})
DO_0 - DO_3	Data Output (D_{OUT})
V_{CC}	GND (0V)
V_{CCA}	Output GND (0V)
V_{EE}	Supply Voltage
NC	No Connect

TRUTH TABLE

Input				
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10L/100L/101L494 are 65,536-bit RAMs organized as 16,384-words-by-4-bits. Memory cell selection is achieved by using the 14 address bits designated as A_0 through A_{13}. Each of the 2^{14} possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ($\overline{CS}$) is provided for memory expansion. The active low Write Enable ($\overline{WE}$) controls the read and write operation. Data resident on the D_{IN} inputs (DI_0 through DI_3) is written into the addressed location only when $\overline{WE}$ and $\overline{CS}$ are held low. In order to perform a read operation, $\overline{WE}$ is held high, $\overline{CS}$ is held low and the non-inverted output data at the addressed location is transferred to D_{OUT} (DO_0 through DO_3) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ($\overline{WE}$ = LOW) or when the device is deselected via the active low chip select pin ($\overline{CS}$ = HIGH).

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to V_{CC} Pin	V_{EE}	+0.5 to –7.0	V
Input Voltage	V_{IN}	+0.5 to –2.0	V
DC Output Current (Output High)	I_{OUT}	–30	mA
Temperature Under Bias	T_C	–55 to +125	°C
Storage Temperature	T_{store}	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

GUARANTEED OPERATING CONDITIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage[1]	10K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	75	°C
Supply Voltage[1]	100K	V_{EE}	–4.8	–4.5	–4.2	V
Case Temperature		T_C	0	—	85	°C
Supply Voltage[1]	101K	V_{EE}	–5.46	–5.2	–4.94	V
Case Temperature		T_C	0	—	85	°C

NOTE:

1. Referenced to Vcc.

RISE AND FALL TIME

Parameter	Code[1]	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	S	t_r	—	1500	—	ps
Output Fall Time	S	t_f	—	1500	—	ps

NOTE:

1. F = Fast Edge Rate
   S = Standard Edge Rate

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	5	—	pF

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10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; Tc = 0°C to +75°C; V_{EE} = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	0°C +25°C +75°C	–1000 –960 –900	–840 –810 –720	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1665 –1650 –1625	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	0°C +25°C +75°C	–1020 –980 –920	— — —	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	0°C +25°C +75°C	— — —	–1645 –1630 –1605	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	0°C +25°C +75°C	–1145 –1105 –1045	–840 –810 –720	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	0°C +25°C +75°C	–1870 –1850 –1830	–1490 –1475 –1450	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0°C to +75°C	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	0°C to +75°C	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	0°C to +75°C	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	0°C to +75°C	–220	—	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V V_{EE} = –4.5V (100K) Tc = 0°C to +85°C Airflow > 2.5m/s
V_{CC} = 0V V_{EE} = –5.2V (101K) Output Load = 50Ω to –2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output High Voltage	–1025	–880	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OL}	Output Low Voltage	–1810	–1620	mV	V_{IN} = V_{IH} Max. or V_{IL} Min.
V_{OHC}	Output High Voltage	–1035	—	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{OLC}	Output Low Voltage	—	–1610	mV	V_{IN} = V_{IH} Min. or V_{IL} Max.
V_{IH}	Input High Voltage	–1165	–880	mV	Guaranteed Input Voltage High for All Inputs
V_{IL}	Input Low Voltage	–1810	–1475	mV	Guaranteed Input Voltage Low for All Inputs
I_{IH}	Input High Current	0.0	20	µA	V_{IN} = V_{IH} Max.
I_{IL}	Input Low Current	–2	2	µA	V_{IN} = V_{IL} Min.
I_{IL}	$\overline{CS}$ Input Low Current	30	170	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{CS}$ Input High Current	40	220	µA	V_{IN} = V_{IH} Max.
I_{IL}	$\overline{WE}$ Input Low Current	–2	35	µA	V_{IN} = V_{IL} Min.
I_{IH}	$\overline{WE}$ Input High Current	0.0	60	µA	V_{IN} = V_{IH} Max.
I_{EE}	Power Supply Current	–220	—	mA	All Inputs and Outputs Open

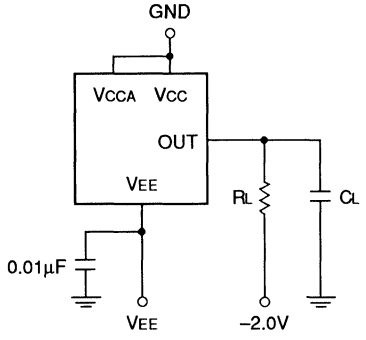
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

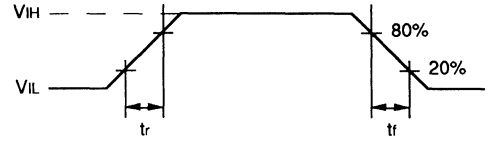
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to −2.0V
$V_{EE} = -5.2V \pm 5\%$(10K) T_C = 0°C to +75°C (10K)
$V_{EE} = -4.5V \pm 0.3V$(100K) T_C = 0°C to +85°C (100K/101K)
$V_{EE} = -5.2V \pm 5\%$(101K) Airflow > 2.5m/s

	T_C	V_{IH}	V_{IL}
10K	0°C +25°C +75°C	−0.933V −0.90V −0.863V	−1.733V −1.70V −1.663V
100/101K	0°C to +85°C	−0.90V	−1.70V

Loading Condition



Input Pulse



$t_r = t_f$ = 1.0ns typ.

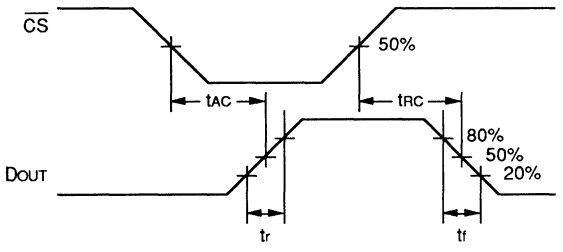
OUTPUT LOAD: R_L = 50Ω
C_L = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to −2V.)

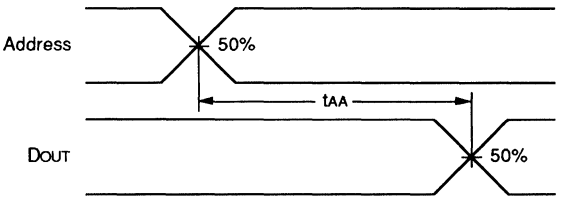
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol		Parameter	SY10L494-10 SY100L494-10 SY101L494-10 Min.	Max.	Unit
t_{AA}	TAVQV	Address AccessTime	—	10	ns
t_{AC}	TSLQV	Chip Select AccessTime	—	3	ns
t_{RC}	TSHQL	Chip Select Recovery Time	—	3	ns

READ CYCLE TIMING DIAGRAM

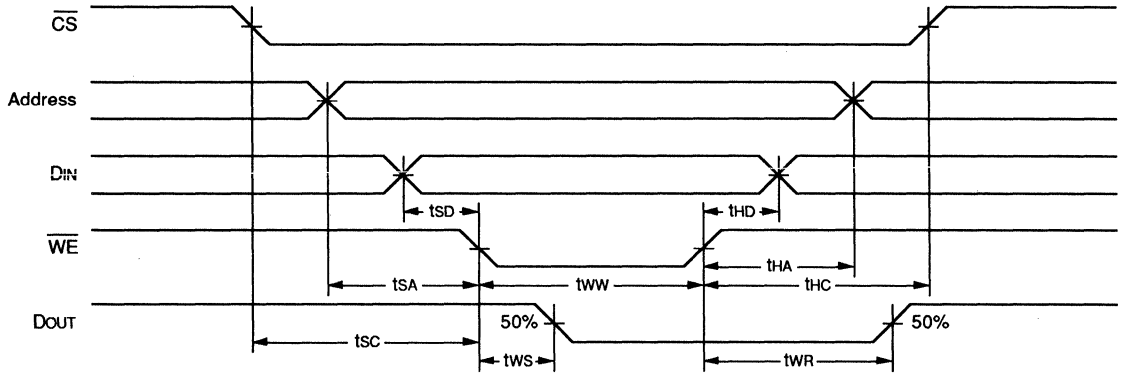




WRITE CYCLE

Symbol		Parameter	SY10L494-10 SY100L494-10 SY101L494-10		Unit
			Min.	Max.	
tWW	TWLWH	Write Pulse Width	8	—	ns
tWS	TWLQL	Write Disable Time	—	3	ns
tWR	TWHQV	Write Recovery Time	—	5	ns
tSA	TAVWL	Address Set-up Time	1	—	ns
tSC	TSLWL	Chip Select Set-up Time	1	—	ns
tSD	TDVWL	Data Set-up Time	1	—	ns
tHA	TWHAX	Address Hold Time	1	—	ns
tHC	TWHSX	Chip Select Hold Time	1	—	ns
tHD	TWHDX	Data Hold Time	1	—	ns

WRITE CYCLE TIMING DIAGRAM

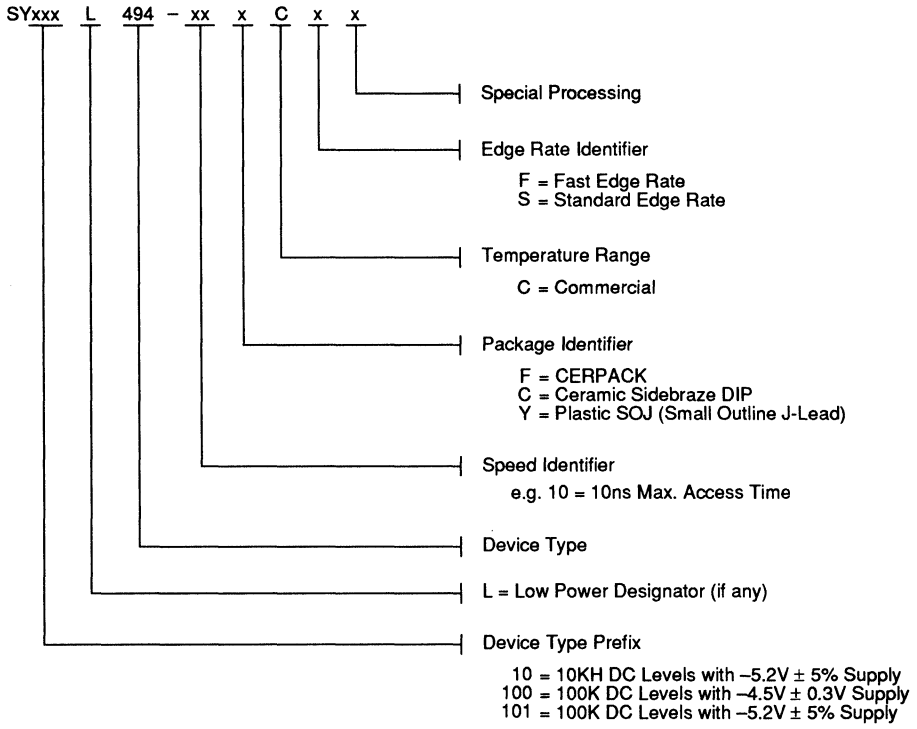


PRODUCT ORDERING CODE

Speed (ns)	Ordering Code[1]	Edge Rate	Package Type	Operating Range
10	SY10L/100L/101L494-10CCS	Standard	C28-1	Commercial
	SY10L/100L/101L494-10FCS	Standard	F28-1	Commercial
	SY10L/100L/101L494-10YCS	Standard	Y28-1	Commercial

NOTE:

1. Device marking will not include "SY" prefix.



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SYNERGY SEMICONDUCTOR

TTL BICMOS STATIC RAM 64K (16K X 4-BIT)

PRELIMINARY
SY61B98-7
SY61B98-10
SY61B98-12

FEATURES

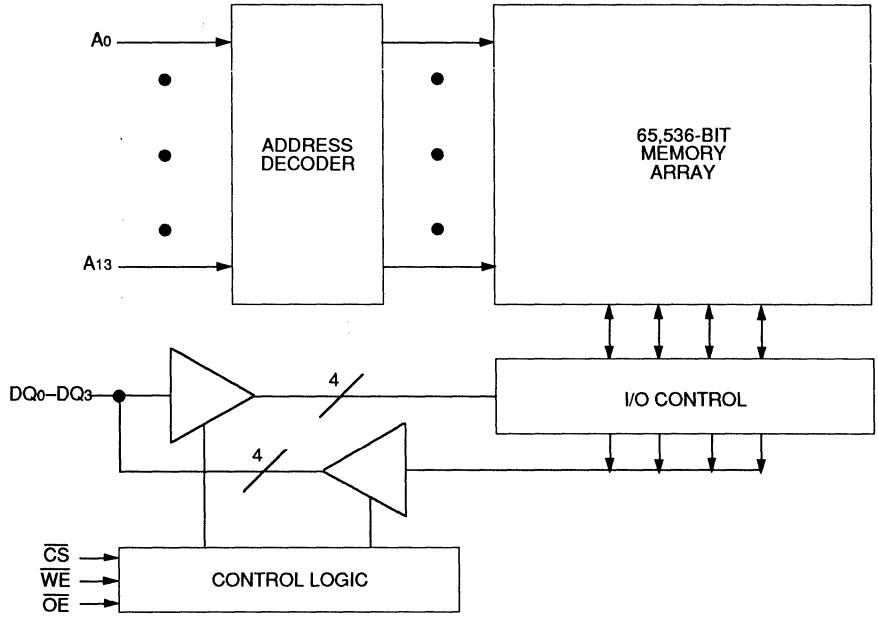
- **Address access time, t_{AA}: 7/10/12ns max.**
- **Chip select access time, t_{ACS}: 4/6/7ns max.**
- **Popular 16K x 4 with common I/O organization**
- **Power supply current, I_{CC}: 200mA max.**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ BiCMOS technology**
- **Fully TTL compatible I/O and power supply levels**
- **Available in 24-pin, 300-mil plastic SOJ**

DESCRIPTION

The Synergy SY61B98 is a 65,536-bit Static Random Access Memory (SRAM), designed with advanced BiCMOS circuitry. The device is organized as 16,384-words-by-4-bits with common I/O and meets standard TTL signal levels operating from a +5.0V ±10% power supply.

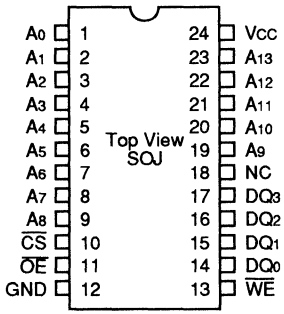
The SY61B98 employs proprietary circuit design techniques and Synergy's proprietary ASSET BiCMOS technology to achieve extremely fast access times and write pulse widths. ASSET BiCMOS uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET BiCMOS, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



Rev.: A Amendment: /0
Issue Date: February, 1994

PIN CONFIGURATION



PIN NAMES

Label	Function
$A_0 - A_{13}$	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$DQ_0 - DQ_3$	Data Input/Output
V_{CC}	Positive Power Supply Terminal
GND	Negative Power Supply Terminal

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Terminal Voltage with Respect to GND	V_{TERM}(2)	–0.5 to +7.0	°C
Temperature Under Bias	T_{BIAS}	–55 to +125	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_T	1.25	W
DC Output Current	I_{OUT}	50	mA

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. V_{IN} pins must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DQ	Function
H	X	X	High Z	Deselect Chip
L	L	H	$DATA_{OUT}$	Read Cycle
L	X	L	$DATA_{IN}$	Write Cycle
L	H	H	High Z	Outputs Disabled

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Case Temperature	T_C	0	—	+75	°C

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Parameter(1)	Symbol	Condition	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is guaranteed by device characterization, but is not production tested.

8

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%; T_C = 0°C to +75°C, Airflow > 2.5m/s

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	V_{CC} = V_{CC} (Min.), I_{OH} = –4.0mA
V_{OL}	Output LOW Voltage	—	0.5	V	V_{CC} = V_{CC} (Min.), I_{OL} = 10.0mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V	Guaranteed Input Voltage HIGH for All Inputs(1)
V_{IL}	Input LOW Voltage	–0.5	0.8	V	Guaranteed Input Voltage LOW for All Inputs(1)
I_{IH}	Input HIGH Current	—	10	µA	V_{IN} = V_{CC}
I_{IL}	Input LOW Current	–10	—	µA	V_{IN} = GND
I_{CEX}	Output Leakage Current	–10	10	µA	V_{OUT} = GND and V_{OUT} = V_{CC}
I_{CC} (Static)	Power Supply Current	—	TBD	mA	V_{CC} = V_{CC} (Max.), All Inputs and Outputs Open
I_{CC} (Dynamic)	SY61B98-7 SY61B98-10 SY61B98-12	— — —	200 180 160	mA mA mA	V_{CC} = V_{CC} (Max.), $\overline{CS} \le V_{IL}$ (Max.), All Address Inputs Cycling at f_{MAX}(2)

NOTES:

1. V_{IL} (Max.) and V_{IH} (Min.) are absolute voltages with respect to device ground and include all voltage transients due to system/tester noise.
2. f_{MAX} = 1/t_{RC}.

AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

Input Pulse Levels	0.0V to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

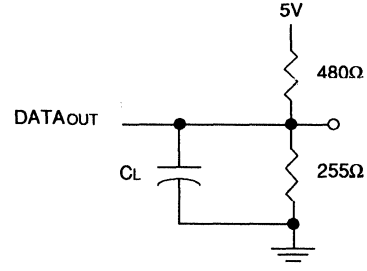


Figure 1. AC Test Load

C_L = 5pF (for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, and t_{OW})
C_L = 30pF (for all active output AC measurements)
Capacitance value includes all stray capacitance of scope and fixture.

READ CYCLE

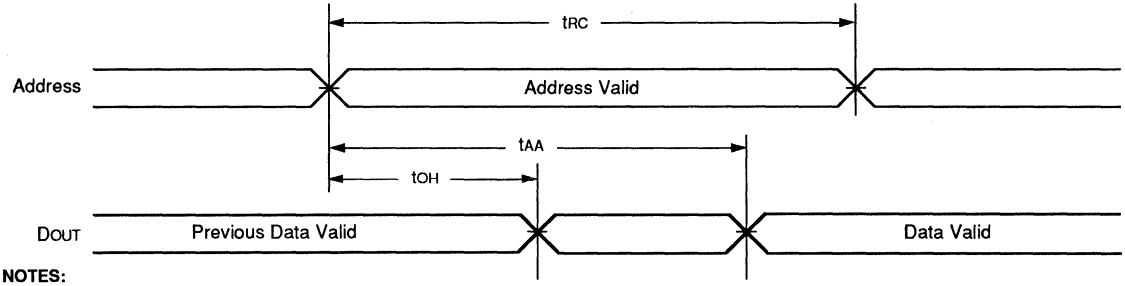
Symbol		Parameter	SY61B98-7		SY61B98-10		SY61B98-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tRC	TAVAX	Read Cycle Time	7	—	10	—	12	—	ns
tAA	TAVQV	Address Access Time	—	7	—	10	—	12	ns
tACS	TSLQV	Chip Select Access Time	—	4	—	6	—	7	ns
tCLZ	TSLQX	Chip Select to Output Active	1	—	1	—	1	—	ns
tCHZ(1)	TSHQZ	Chip Deselect to Output High-Z	—	4	—	6	—	7	ns
tOE	TGLQV	Output Enable to Output Valid	—	4	—	5	—	6	ns
tOLZ	TGLQX	Output Enable to Output Active	1	—	1	—	1	—	ns
tOHZ(1)	TGHQZ	Output Disable to Output High-Z	—	3	—	3	—	3	ns
tOH	TAXQX	Output Hold from Address Change	3	—	3	—	3	—	ns

NOTE:

1. These parameters are guaranteed by device characterization and are not 100% tested in production.

READ CYCLE TIMING DIAGRAMS

ADDRESS ACCESS CYCLE



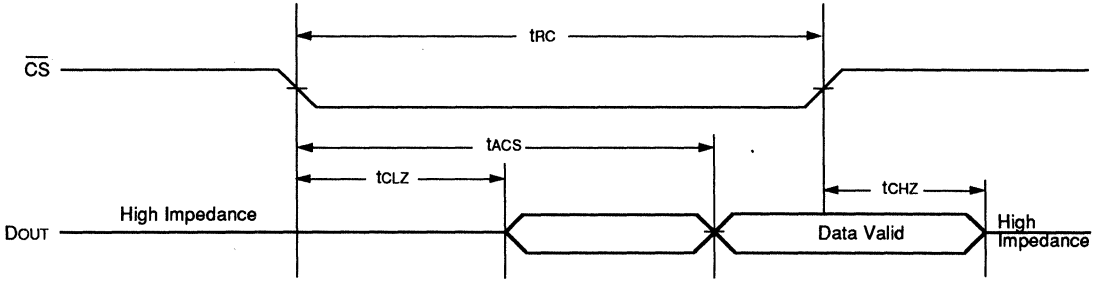
NOTES:

1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. The device is continually selected, where $\overline{CS}$ = $\overline{OE}$ = VIL.

8

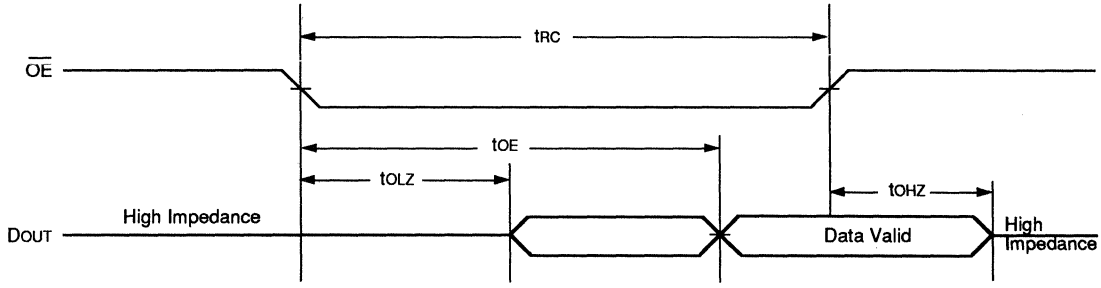
READ CYCLE TIMING DIAGRAMS (CONTINUED)

CHIP SELECT ACCESS CYCLE



NOTES:
1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. Address valid prior to or coincident with the HIGH-to-LOW transition of $\overline{CS}$.
3. $\overline{OE}$ = VIL.

OUTPUT ENABLE ACCESS CYCLE



NOTES:
1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. Address valid prior to or coincident with the HIGH-to-LOW transition of $\overline{OE}$.
3. $\overline{CS}$ = VIL.

WRITE CYCLE

Symbol		Parameter	SY61B98-7		SY61B98-10		SY61B98-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	TAVAX	Write Cycle Time	7	—	10	—	12	—	ns
t_{WP}	TWLWH	Write Pulse Width	4	—	6	—	8	—	ns
t_{WHZ}(2)	TWLQZ	Write Disable Time	—	3	—	3	—	4	ns
t_{OW}	TWHQV	Output Active From End of Write Time	—	3	—	3	—	3	ns
t_{AS}	TAVWL	Address Set-up Time	0	—	0	—	0	—	ns
t_{CW}	TSLWH	Chip Select Set-up Time to Write Terminate	4	—	6	—	8	—	ns
t_{DW}	TDVWH	Data Set-up Time to Write Terminate	4	—	5	—	6	—	ns
t_{WR}	TWHAX	Write Recovery Time/Address Hold Time	0	—	0	—	0	—	ns
t_{HC}	TWHSX	Chip Select Hold Time	0	—	0	—	0	—	ns
t_{DH}	TWHDX	Data Hold Time	0	—	0	—	0	—	ns
t_{AW}	TAVWH	Address Valid to Write Terminate	8	—	8	—	8	—	ns

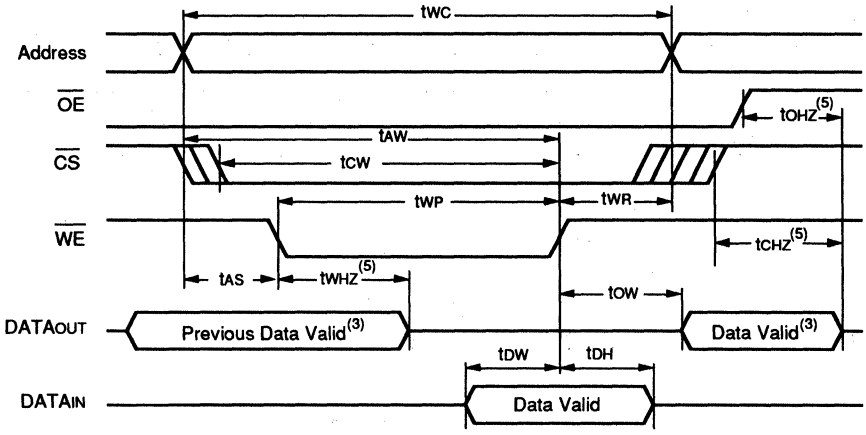
NOTE:

1. $\overline{CS}$ or $\overline{WE}$ must be HIGH during an address transition.
2. This parameter is guaranteed by device characterization and is not 100% tested in production.

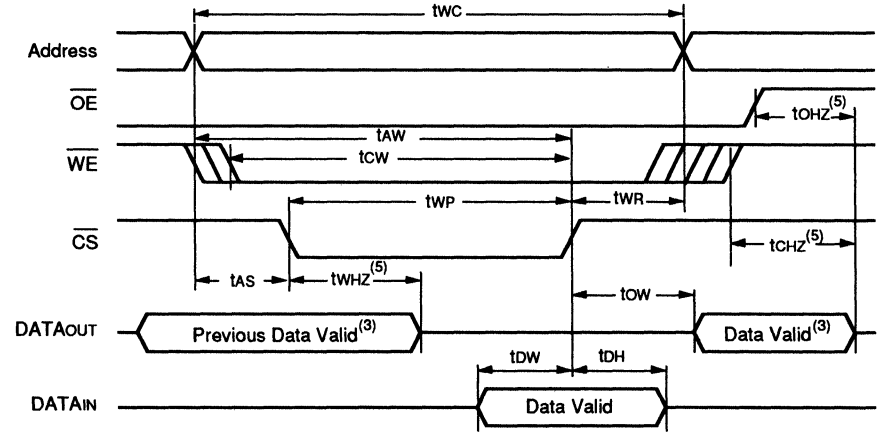
8

WRITE CYCLE TIMING DIAGRAMS

WE CONTROLLED



CS CONTROLLED

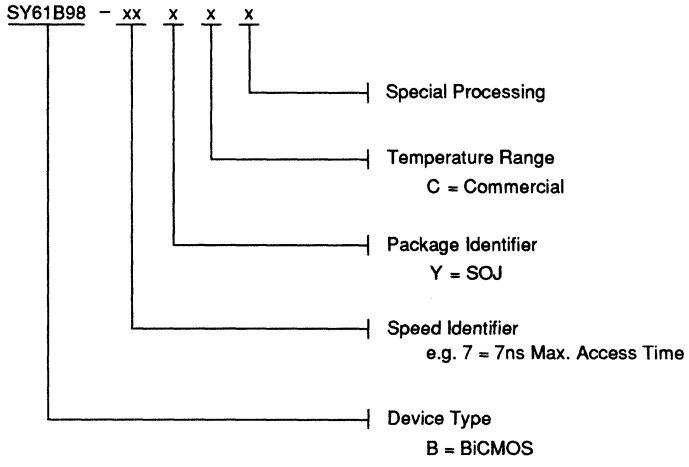


NOTES:

1. A write occurs during the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, the DQ pins are in the output state and input signals must not be applied.
4. If $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ HIGH transition, the outputs remain in the high-impedance state. Likewise, if $\overline{CS}$ HIGH transition occurs simultaneously with or before $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. The transition is measured ±200mV from previous steady state.
6. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.

PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Package Type	Operating Range
7	SY61B98-7YC	Y24-1	Commercial
10	SY61B98-10YC	Y24-1	Commercial
12	SY61B98-12YC	Y24-1	Commercial



8

SYNERGY SEMICONDUCTOR

TTL BICMOS STATIC RAM 64K (16K X 4-BIT)

PRELIMINARY
SY71B88-7
SY71B88-10
SY71B88-12

FEATURES

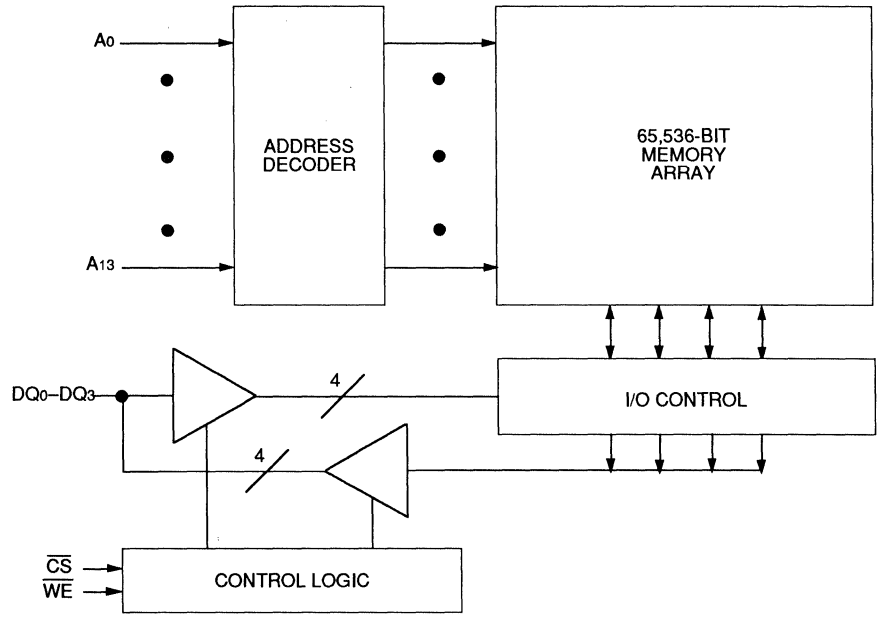
- **Address access time, t_{AA}: 7/10/12ns max.**
- **Chip select access time, t_{ACS}: 4/6/7ns max.**
- **Popular 16K x 4 with common I/O organization**
- **Power supply current, I_{CC}: 200mA max.**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ BiCMOS technology**
- **Fully TTL compatible I/O and power supply levels**
- **Available in 24-pin, 300-mil plastic SOJ**

DESCRIPTION

The Synergy SY71B88 is a 65,536-bit Static Random Access Memory (SRAM), designed with advanced BiCMOS circuitry. The device is organized as 16,384-words-by-4-bits with common I/O and meets standard TTL signal levels operating from a +5.0V ±10% power supply.

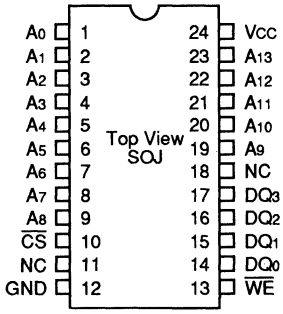
The SY71B88 employs proprietary circuit design techniques and Synergy's proprietary ASSET BiCMOS technology to achieve extremely fast access times and write pulse widths. ASSET BiCMOS uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET BiCMOS, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



Rev.: A Amendment: /0
Issue Date: February, 1994

PIN CONFIGURATION



PIN NAMES

Label	Function
$A_0 - A_{13}$	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$DQ_0 - DQ_3$	Data Input/Output
V_{CC}	Positive Power Supply Terminal
GND	Negative Power Supply Terminal

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Terminal Voltage with Respect to GND	V_{TERM}(2)	–0.5 to +7.0	°C
Temperature Under Bias	T_{BIAS}	–55 to +125	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_T	1.25	W
DC Output Current	I_{OUT}	50	mA

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. V_{IN} pins must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DQ	Function
H	X	High Z	Deselect Chip
L	H	$DATA_{OUT}$	Read Cycle
L	L	$DATA_{IN}$	Write Cycle

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Case Temperature	T_C	0	—	+75	°C

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Parameter(1)	Symbol	Condition	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is guaranteed by device characterization, but is not production tested.

8

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%; T_C = 0°C to +75°C, Airflow > 2.5m/s

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	V_{CC} = V_{CC} (Min.), I_{OH} = –4.0mA
V_{OL}	Output LOW Voltage	—	0.5	V	V_{CC} = V_{CC} (Min.), I_{OL} = 10.0mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V	Guaranteed Input Voltage HIGH for All Inputs(1)
V_{IL}	Input LOW Voltage	–0.5	0.8	V	Guaranteed Input Voltage LOW for All Inputs(1)
I_{IH}	Input HIGH Current	—	10	µA	V_{IN} = V_{CC}
I_{IL}	Input LOW Current	–10	—	µA	V_{IN} = GND
I_{CEX}	Output Leakage Current	–10	10	µA	V_{OUT} = GND and V_{OUT} = V_{CC}
I_{CC} (Static)	Power Supply Current	—	TBD	mA	V_{CC} = V_{CC} (Max.), All Inputs and Outputs Open
I_{CC} (Dynamic)	SY71B88-7 SY71B88-10 SY71B88-12	— — —	200 180 160	mA mA mA	V_{CC} = V_{CC} (Max.), $\overline{CS} \le V_{IL}$ (Max.), All Address Inputs Cycling at f_{MAX}(2)

NOTES:

1. V_{IL} (Max.) and V_{IH} (Min.) are absolute voltages with respect to device ground and include all voltage transients due to system/tester noise.
2. f_{MAX} = 1/t_{RC}.

AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

Input Pulse Levels	0.0V to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

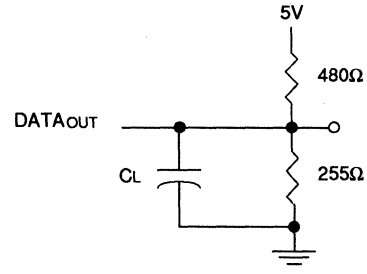


Figure 1. AC Test Load

C_L = 5pF (for t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{OW})
C_L = 30pF (for all active output AC measurements)
Capacitance value includes all stray capacitance of scope and fixture.

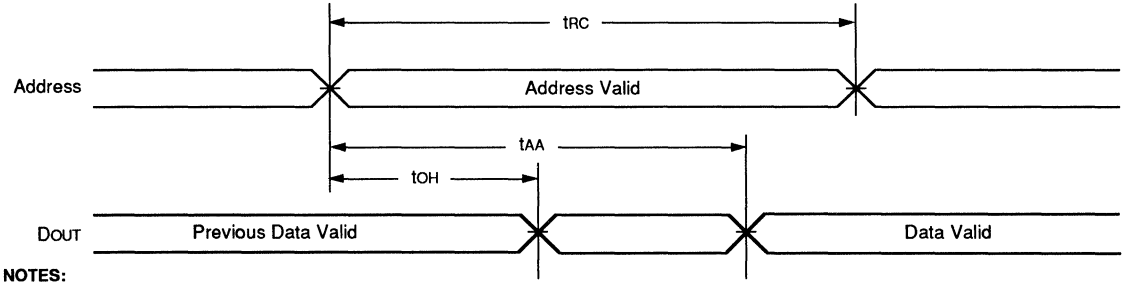
READ CYCLE

Symbol		Parameter	SY71B88-7		SY71B88-10		SY71B88-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tRC	TAVAX	Read Cycle Time	7	—	10	—	12	—	ns
tAA	TAVQV	Address Access Time	—	7	—	10	—	12	ns
tACS	TSLQV	Chip Select Access Time	—	4	—	6	—	7	ns
tCLZ	TSLQX	Chip Select to Output Active	1	—	1	—	1	—	ns
tCHZ(1)	TSHQZ	Chip Deselect to Output High-Z	—	4	—	6	—	7	ns
tOH	TAXQX	Output Hold from Address Change	3	—	3	—	3	—	ns

NOTE:
1. This parameter is guaranteed by device characterization and is not 100% tested in production.

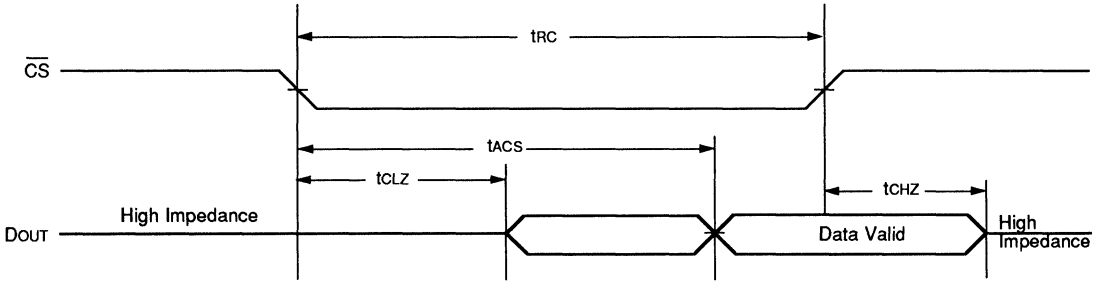
READ CYCLE TIMING DIAGRAMS

ADDRESS ACCESS CYCLE



NOTES:
1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. The device is continually selected, where $\overline{CS}$ = VIL.

CHIP SELECT ACCESS CYCLE



NOTES:
1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. Address valid prior to or coincident with the HIGH-to-LOW transition of $\overline{CS}$.

8

WRITE CYCLE

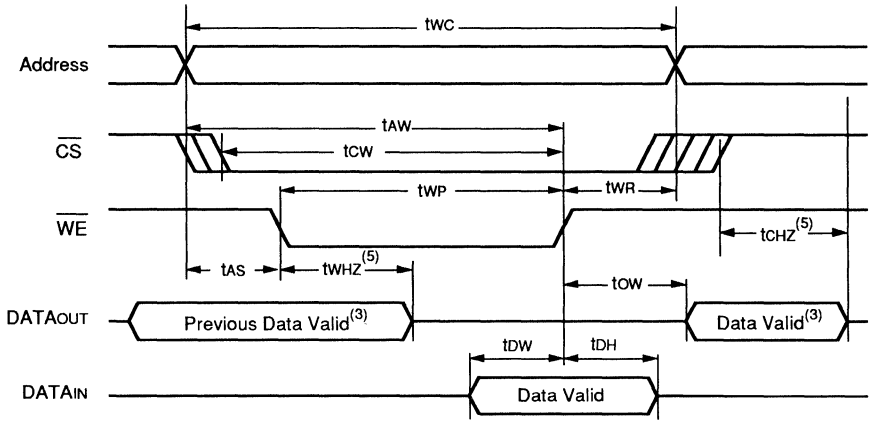
Symbol		Parameter	SY71B88-7		SY71B88-10		SY71B88-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	TAVAX	Write Cycle Time	7	—	10	—	12	—	ns
t_{WP}	TWLWH	Write Pulse Width	4	—	6	—	8	—	ns
t_{WHZ}(2)	TWLQZ	Write Disable Time	—	3	—	3	—	4	ns
t_{OW}	TWHQV	Output Active From End of Write Time	—	3	—	3	—	3	ns
t_{AS}	TAVWL	Address Set-up Time	0	—	0	—	0	—	ns
t_{CW}	TSLWH	Chip Select Set-up Time to Write Terminate	4	—	6	—	8	—	ns
t_{DW}	TDVWH	Data Set-up Time to Write Terminate	4	—	5	—	6	—	ns
t_{WR}	TWHAX	Write Recovery Time/Address Hold Time	0	—	0	—	0	—	ns
t_{HC}	TWHSX	Chip Select Hold Time	0	—	0	—	0	—	ns
t_{DH}	TWHDX	Data Hold Time	0	—	0	—	0	—	ns
t_{AW}	TAVWH	Address Valid to Write Terminate	8	—	8	—	8	—	ns

NOTE:

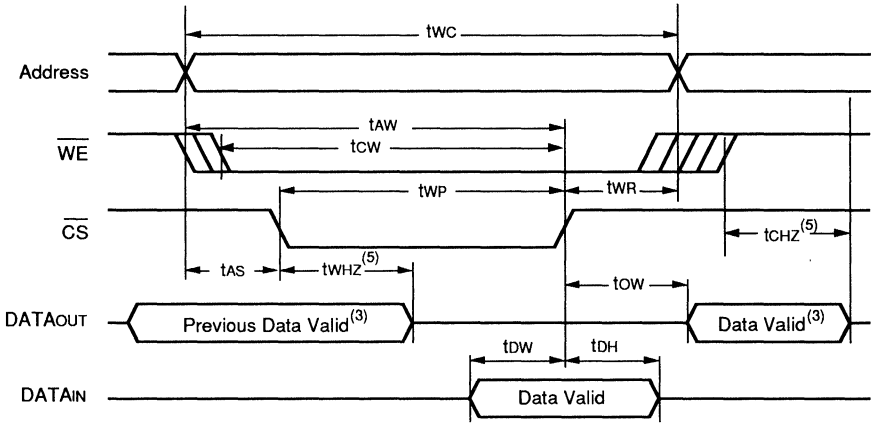
1. $\overline{CS}$ or $\overline{WE}$ must be HIGH during an address transition.
2. This parameter is guaranteed by device characterization and is not 100% tested in production.

WRITE CYCLE TIMING DIAGRAMS

$\overline{WE}$ CONTROLLED



$\overline{CS}$ CONTROLLED



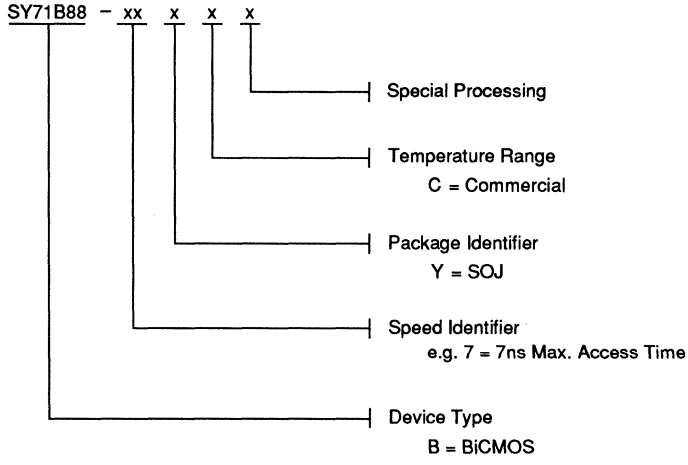
NOTES:

1. A write occurs during the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, the DQ pins are in the output state and input signals must not be applied.
4. If $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ HIGH transition, the outputs remain in the high-impedance state. Likewise, if $\overline{CS}$ HIGH transition occurs simultaneously with or before $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. The transition is measured ±200mV from previous steady state.

8

PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Package Type	Operating Range
7	SY71B88-7YC	Y24-1	Commercial
10	SY71B88-10YC	Y24-1	Commercial
12	SY71B88-12YC	Y24-1	Commercial



SYNERGY SEMICONDUCTOR

TTL BICMOS STATIC RAM 64K (16K X 4-BIT)

PRELIMINARY
SY71B98-7
SY71B98-10
SY71B98-12

FEATURES

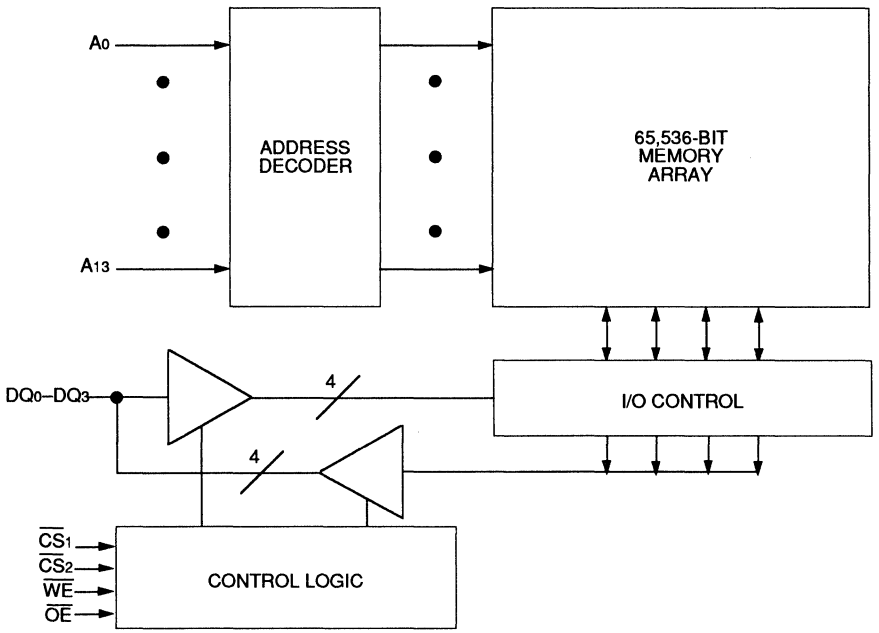
- **Address access time, t_{AA}: 7/10/12ns max.**
- **Chip select access time, t_{ACS}: 4/6/7ns max.**
- **Popular 16K x 4 with common I/O organization**
- **Power supply current, I_{CC}: 200mA max.**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ BiCMOS technology**
- **Fully TTL compatible I/O and power supply levels**
- **Available in 24-pin, 300-mil plastic SOJ**

DESCRIPTION

The Synergy SY71B98 is a 65,536-bit Static Random Access Memory (SRAM), designed with advanced BiCMOS circuitry. The device is organized as 16,384-words-by-4-bits with common I/O and meets standard TTL signal levels operating from a +5.0V ±10% power supply.

The SY71B98 employs proprietary circuit design techniques and Synergy's proprietary ASSET BiCMOS technology to achieve extremely fast access times and write pulse widths. ASSET BiCMOS uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET BiCMOS, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



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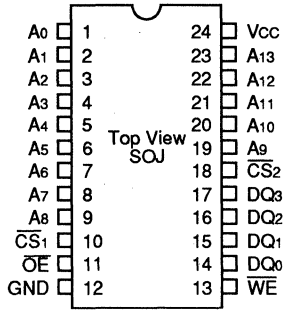
Rev.: A Amendment: /0
Issue Date: February, 1994

PIN CONFIGURATION



PIN NAMES

Label	Function
$A_0 - A_{13}$	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$, $\overline{CS_2}$	Chip Select Inputs
$\overline{OE}$	Output Enable Input
$DQ_0 - DQ_3$	Data Input/Output
V_{CC}	Positive Power Supply Terminal
GND	Negative Power Supply Terminal

ABSOLUTE MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Terminal Voltage with Respect to GND	V_{TERM}(2)	–0.5 to +7.0	°C
Temperature Under Bias	T_{BIAS}	–55 to +125	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_T	1.25	W
DC Output Current	I_{OUT}	50	mA

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. V_{IN} pins must not exceed V_{CC} + 0.5V.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Parameter(1)	Symbol	Condition	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is guaranteed by device characterization, but is not production tested.

TRUTH TABLE(1)

$\overline{CS_1}$	$\overline{CS_2}$	$\overline{OE}$	$\overline{WE}$	DQ	Function
X	H	X	X	High Z	Deselect Chip
H	X	X	X	High Z	Deselect Chip
L	L	L	H	$DATA_{OUT}$	Read Cycle
L	L	X	L	$DATA_{IN}$	Write Cycle
L	L	H	H	High Z	Outputs Disabled

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Case Temperature	T_C	0	—	+75	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5.0V ± 10%; T_C = 0°C to +75°C, Airflow > 2.5m/s

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	V_{CC} = V_{CC} (Min.), I_{OH} = –4.0mA
V_{OL}	Output LOW Voltage	—	0.5	V	V_{CC} = V_{CC} (Min.), I_{OL} = 10.0mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC} + 0.5	V	Guaranteed Input Voltage HIGH for All Inputs(1)
V_{IL}	Input LOW Voltage	–0.5	0.8	V	Guaranteed Input Voltage LOW for All Inputs(1)
I_{IH}	Input HIGH Current	—	10	µA	V_{IN} = V_{CC}
I_{IL}	Input LOW Current	–10	—	µA	V_{IN} = GND
I_{CEX}	Output Leakage Current	–10	10	µA	V_{OUT} = GND and V_{OUT} = V_{CC}
I_{CC} (Static)	Power Supply Current	—	TBD	mA	V_{CC} = V_{CC} (Max.), All Inputs and Outputs Open
I_{CC} (Dynamic)	SY71B98-7	—	200	mA	V_{CC} = V_{CC} (Max.),
	SY71B98-10	—	180	mA	$\overline{CS} \le V_{IL}$ (Max.),
	SY71B98-12	—	160	mA	All Address Inputs Cycling at f_{MAX}(2)

NOTES:

1. V_{IL} (Max.) and V_{IH} (Min.) are absolute voltages with respect to device ground and include all voltage transients due to system/tester noise.
2. f_{MAX} = 1/t_{RC}.

AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

Input Pulse Levels	0.0V to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

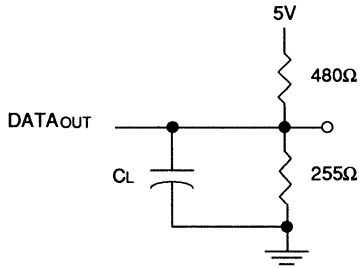


Figure 1. AC Test Load

C_L = 5pF (for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, and t_{OW})
C_L = 30pF (for all active output AC measurements)
Capacitance value includes all stray capacitance of scope and fixture.

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READ CYCLE

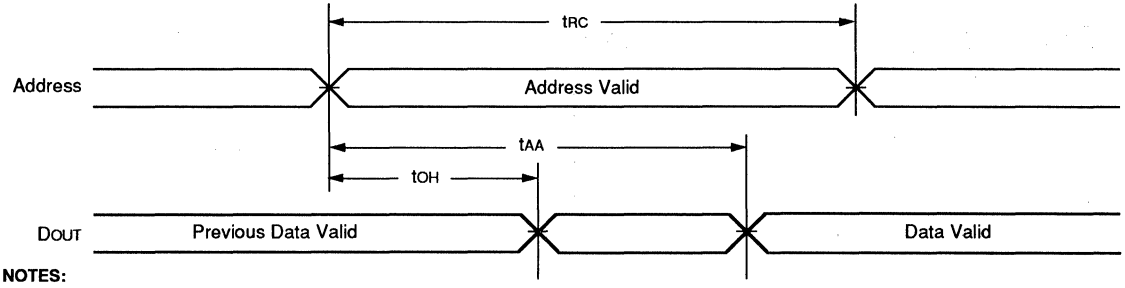
Symbol		Parameter	SY71B98-7		SY71B98-10		SY71B98-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	TAVAX	Read Cycle Time	7	—	10	—	12	—	ns
t_{AA}	TAVQV	Address Access Time	—	7	—	10	—	12	ns
t_{ACS}	TSLQV	Chip Select Access Time	—	4	—	6	—	7	ns
t_{CLZ}	TSLQX	Chip Select to Output Active	1	—	1	—	1	—	ns
t_{CHZ}(1)	TSHQZ	Chip Deselect to Output High-Z	—	4	—	6	—	7	ns
t_{OE}	TGLQV	Output Enable to Output Valid	—	4	—	5	—	6	ns
t_{OLZ}	TGLQX	Output Enable to Output Active	1	—	1	—	1	—	ns
t_{OHZ}(1)	TGHQZ	Output Disable to Output High-Z	—	3	—	3	—	3	ns
t_{OH}	TAXQX	Output Hold from Address Change	3	—	3	—	3	—	ns

NOTE:

1. These parameters are guaranteed by device characterization and are not 100% tested in production.

READ CYCLE TIMING DIAGRAMS

ADDRESS ACCESS CYCLE

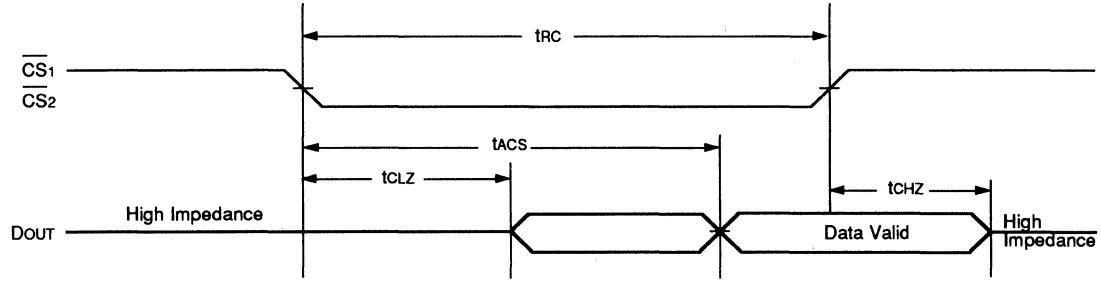


NOTES:

1. $\overline{WE}$ must be HIGH for ≥ t_{WR} prior to start of read cycle.
2. The device is continually selected, where $\overline{CS_1}$ = $\overline{CS_2}$ = $\overline{OE}$ = V_{IL}.

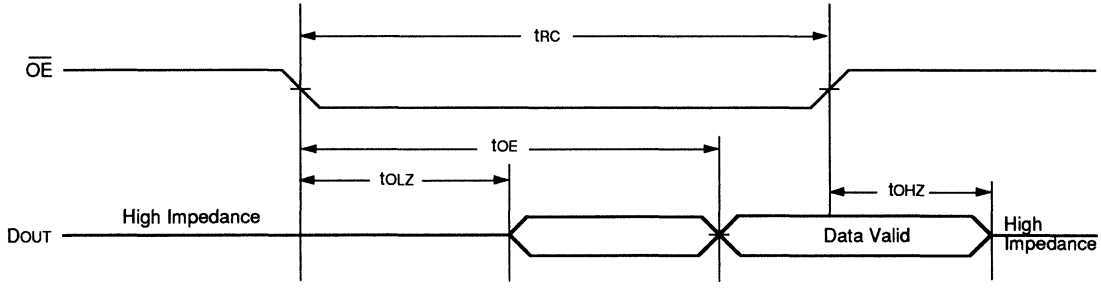
READ CYCLE TIMING DIAGRAMS (CONTINUED)

CHIP SELECT ACCESS CYCLE



NOTES:
1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. Address valid prior to or coincident with the HIGH-to-LOW transition of $\overline{CS_1}$, $\overline{CS_2}$.
3. $\overline{OE}$ = VIL.

OUTPUT ENABLE ACCESS CYCLE



NOTES:
1. $\overline{WE}$ must be HIGH for ≥ tWR prior to start of read cycle.
2. Address valid prior to or coincident with the HIGH-to-LOW transition of $\overline{OE}$.
3. $\overline{CS_1}$ and $\overline{CS_2}$ = VIL.

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WRITE CYCLE

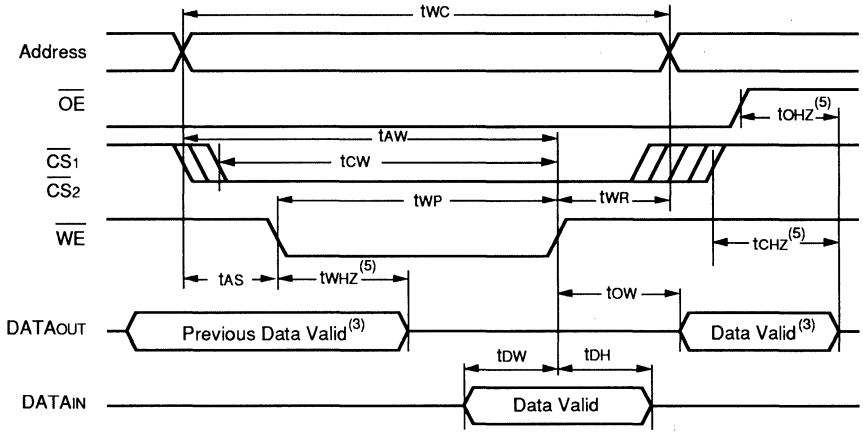
Symbol		Parameter	SY71B98-7		SY71B98-10		SY71B98-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	TAVAX	Write Cycle Time	7	—	10	—	12	—	ns
t_{WP}	TWLWH	Write Pulse Width	4	—	6	—	8	—	ns
t_{WHZ}(2)	TWLQZ	Write Disable Time	—	3	—	3	—	4	ns
t_{OW}	TWHQV	Output Active From End of Write Time	—	3	—	3	—	3	ns
t_{AS}	TAVWL	Address Set-up Time	0	—	0	—	0	—	ns
t_{CW}	TSLWH	Chip Select Set-up Time to Write Terminate	4	—	6	—	8	—	ns
t_{DW}	TDVWH	Data Set-up Time to Write Terminate	4	—	5	—	6	—	ns
t_{WR}	TWHAX	Write Recovery Time/Address Hold Time	0	—	0	—	0	—	ns
t_{HC}	TWHSX	Chip Select Hold Time	0	—	0	—	0	—	ns
t_{DH}	TWHDX	Data Hold Time	0	—	0	—	0	—	ns
t_{AW}	TAVWH	Address Valid to Write Terminate	8	—	8	—	8	—	ns

NOTE:

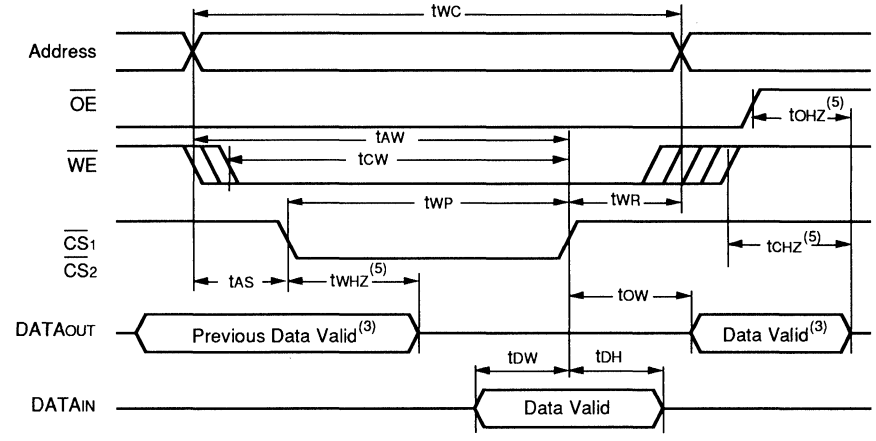
1. $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ must be HIGH during an address transition.
2. This parameter is guaranteed by device characterization and is not 100% tested in production.

WRITE CYCLE TIMING DIAGRAMS

$\overline{WE}$ CONTROLLED



$\overline{CS}$ CONTROLLED

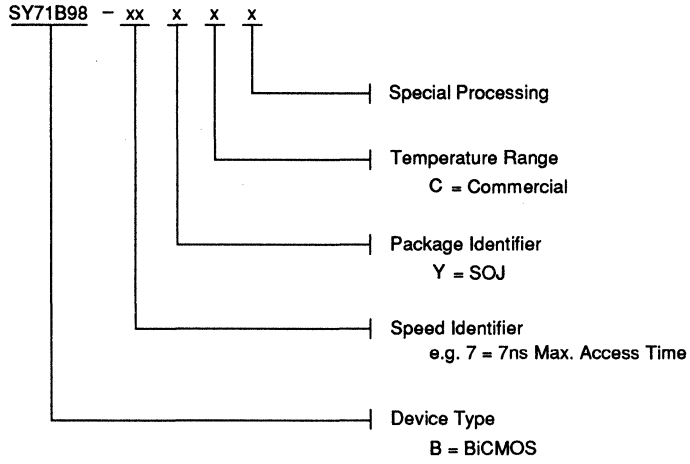


NOTES:

1. A write occurs during the overlap of $\overline{CS}_1$ and $\overline{CS}_2$ LOW and $\overline{WE}$ LOW.
2. t_{WR} is measured from the earlier of $\overline{CS}_1$ and $\overline{CS}_2$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, the DQ pins are in the output state and input signals must not be applied.
4. If $\overline{CS}_1$ and $\overline{CS}_2$ LOW transition occurs simultaneously with or after the $\overline{WE}$ HIGH transition, the outputs remain in the high-impedance state. Likewise, if $\overline{CS}_1$ and $\overline{CS}_2$ HIGH transition occurs simultaneously with or before $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. The transition is measured ±200mV from previous steady state.
6. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a $\overline{CS}_1$ and $\overline{CS}_2$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.

PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Package Type	Operating Range
7	SY71B98-7YC	Y24-1	Commercial
10	SY71B98-10YC	Y24-1	Commercial
12	SY71B98-12YC	Y24-1	Commercial



9

SYNERGY SEMICONDUCTOR

ULTRA-HIGH-SPEED 1K x 24 FIFO

ADVANCE INFORMATION
SY69164

FEATURES

- System clock speeds to 200MHz
- User-selectable bandwidth — one read or write operation each clock cycle
- 24-bit wide data path for efficient transfers
- Sequential read and write, READ DATA VALID flag
- EMPTY, FULL and HALF-FULL status flags
- Simple initialization via $\overline{\text{RESET}}$ input
- Compatible with 10KH ECL logic
- Improved noise margins via on-chip voltage and temperature compensation; designed for alpha-particle immunity
- Available in thermally-enhanced 208-pin PQFP or 207-pin PPGA
- Power dissipation = 16 watts (typ.)

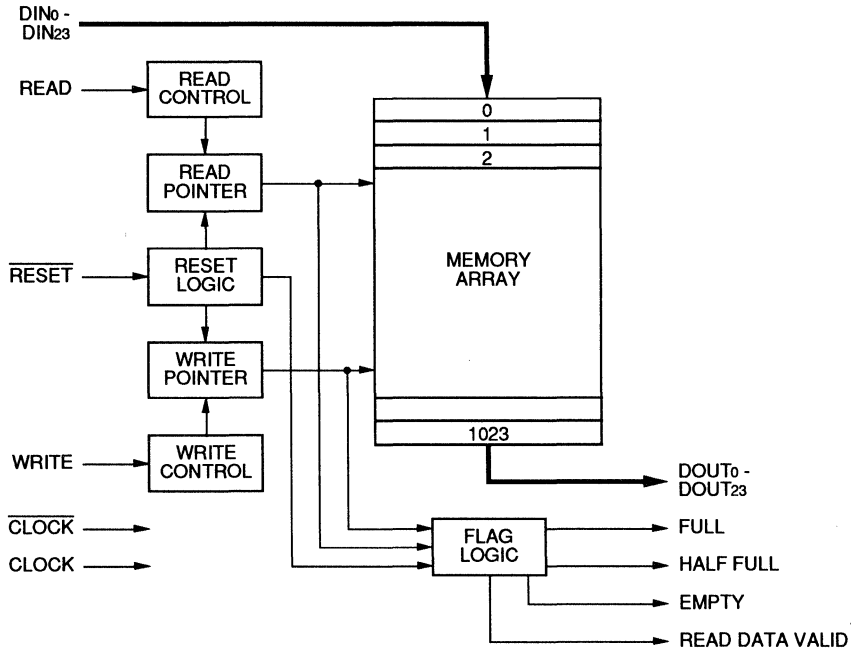
DESCRIPTION

The Synergy SY69164 is an ultra-high-speed 1K-word-by-24-bit First-In/First-Out (FIFO) memory, fabricated in Synergy's proprietary ASSET™ I bipolar process.

With a differential clock applied to the FIFO, data is written into or read out of the memory under control of the WRITE or READ pin, respectively. All address vectors are generated internally. FULL, HALF-FULL and EMPTY flags are provided to help prevent overflow/underflow. The asynchronous RESET pin initializes the device and resets both write and read pointers to zero. Output data integrity can be assured by use of the READ DATA VALID output flag. All inputs and outputs are single-ended ECL.

Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but allow device operation at reduced power levels with virtually no soft error sensitivity. Outstanding reliability is achieved in volume production.

BLOCK DIAGRAM



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Issue Date: February, 1994

SYNERGY SEMICONDUCTOR

ULTRA-HIGH-SPEED 3K x 8 FIFO

ADVANCE INFORMATION
SY69165

FEATURES

- **System clock speeds to 600MHz**
- **User-selectable bandwidth — one read or write operation each clock cycle**
- **Pipelined architecture — highest performance with minimum latency**
- **Sequential read and write, READ DATA VALID flag**
- **EMPTY, FULL and HALF-FULL status flags**
- **Simple initialization via $\overline{\text{RESET}}$ input**
- **Compatible with 10KH ECL logic**
- **Improved noise margins via on-chip voltage and temperature compensation; designed for alpha-particle immunity**
- **Available in thermally-enhanced 208-pin PQFP or 207-pin PPGA**
- **Power dissipation = 16 watts (typ.)**

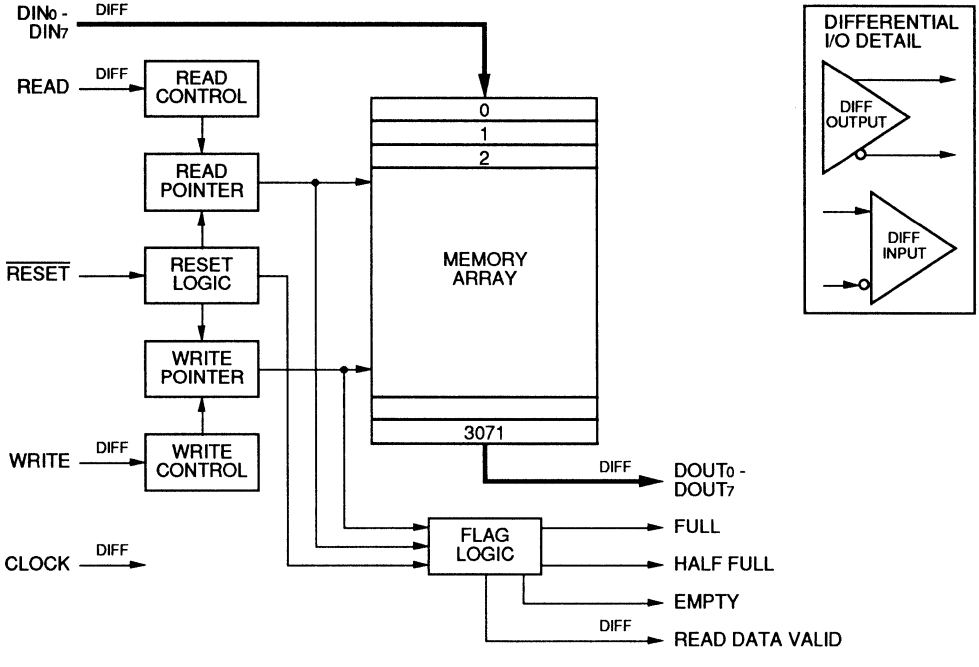
DESCRIPTION

The Synergy SY69165 is an ultra-high-speed 3K-word-by-8-bit First-In/First-Out (FIFO) memory, fabricated in Synergy's proprietary ASSET™ I bipolar process.

With a differential clock (up to 600MHz) applied to the FIFO, data is written into or read out of the memory under control of the WRITE or READ pin, respectively. All address vectors are generated internally. FULL, HALF-FULL and EMPTY flags are provided to help prevent overflow/underflow. The asynchronous RESET pin initializes the device and resets both write and read pointers to zero. Output data integrity can be assured by use of the READ DATA VALID output flag. High-speed inputs and outputs are differential ECL; lower-speed signals are single-ended.

Synergy's circuit design techniques, coupled with ASSET I, result not only in ultra-fast performance, but allow device operation at reduced power levels with virtually no soft error sensitivity. Outstanding reliability is achieved in volume production.

BLOCK DIAGRAM



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Rev.: B Amendment: /0
Issue Date: February, 1994

SYNERGY SEMICONDUCTOR

ULTRA-HIGH-SPEED 64-WORD x 18-BIT FIFO

PRELIMINARY
SY69167
SY69267

FEATURES

- System clock speeds to 200MHz
- User-selectable bandwidth — one read or one write operation each clock cycle
- Selectable OVERFLOW and UNDERFLOW interrupts
- EMPTY, HALF-FULL and FULL status flag outputs
- Simple initialization via $\overline{\text{RESET}}$ input
- Compatible with ECL logic standards: SY69167 for 10KH designs, or SY69267 for 100K designs
- Improved noise margins via on-chip voltage and temperature compensation; designed for alpha-particle immunity
- Available in thermally-enhanced 64-pin Quad Flatpack (QFP)
- Power dissipation only 4 watts (typ.)

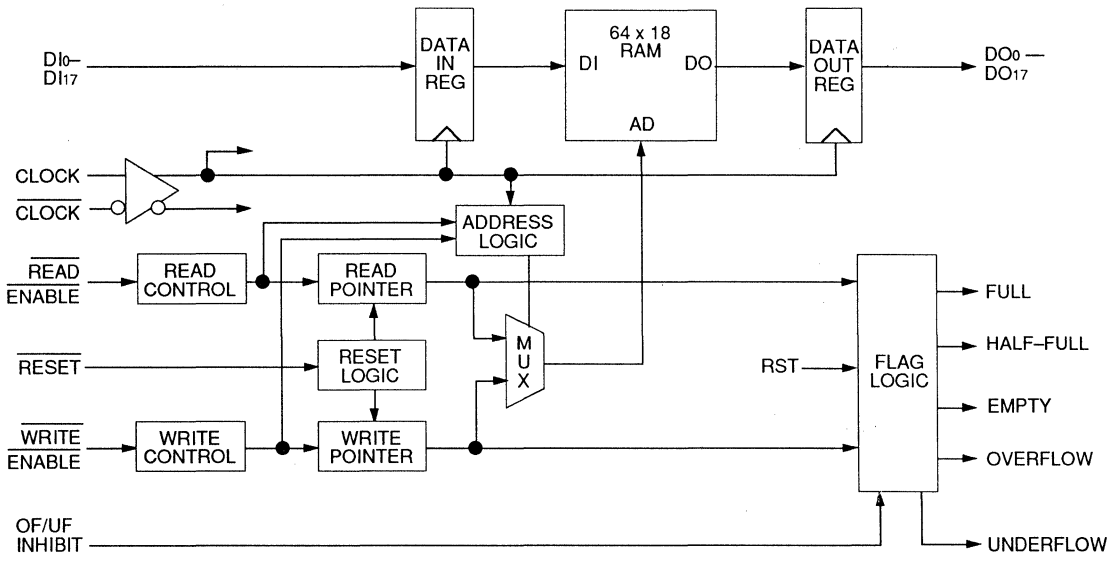
DESCRIPTION

Synergy's SY69167 and SY69267 are ultra-high-speed 64-word-by-18-bit First-In/First-Out (FIFO) static memories. Both are fabricated in Synergy's proprietary ASSET™ I bipolar process.

With a system clock up to 200MHz applied to the FIFO, data is written into or read out of the memory under control of the WRITE ENABLE or READ ENABLE input, respectively; one write **or** one read operation per clock cycle. All address vectors are generated internally. FULL, HALF-FULL and EMPTY status flags, plus selectable OVERFLOW and UNDERFLOW interrupt outputs are provided. The RESET input initializes the device and resets both read and write pointers to zero. All inputs and outputs (except the differential CLOCK inputs) are single-ended ECL (SY69167 for 10KH, SY69267 for 100K)

Synergy's circuit design techniques, coupled with ASSET technology, result not only in ultra-fast performance, but allow device operation at reduced power levels with virtually no soft error sensitivity. Outstanding reliability is achieved in volume production.

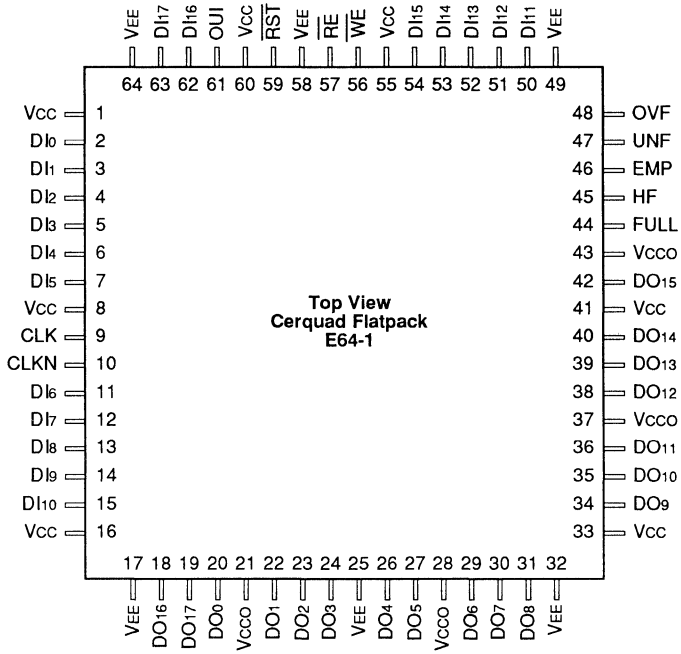
BLOCK DIAGRAM



ASSET is a trademark of Synergy Semiconductor Corporation.

Rev.: B Amendment: /0
Issue Date: February, 1994

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The Synergy SY69167/267 synchronous FIFOs are ultra-high-performance, wide-word First-In/First-Out buffers. The single-clock synchronous design yields a 400MByte/sec. bandwidth which is easily usable without the complicated timing constraints of lower-performance CMOS FIFOs. The design is a single-stage pipeline with all control and data signals registered on the rising edge of the clock so that only set-up and hold, with respect to the clock, need to be observed. The FIFO's 18-bit width allows two parity-checked bytes per device for reduced board area.

All input signals are sampled on the rising edge of the clock. The corresponding activity is initiated during the next clock period. All output signals are driven by registers which are also clocked on the rising edge.

INPUT SIGNALS

RESET — Reset of the device occurs whenever this input is pulled low. Reset consists of setting the read and write pointers to zero and clearing the condition flags (except for EMPTY). The EMPTY flag is set high on reset.

WRITE ENABLE ($\overline{WE}$) — Initiates a write into the FIFO during the next clock period. The data written is the data present on the Data Input (DI) lines concurrent with the asserted $\overline{WE}$ input. $\overline{WE}$ may be asserted continuously and the corresponding data during each clock period will be written into the FIFO. If the FIFO is full, further writes can be inhibited by asserting the OVERFLOW/UNDERFLOW INHIBIT (OUI) input. If OUI is not asserted, then writes can

continue even when the FIFO is full. In this case, the write pointer will wrap-around.

READ ENABLE ($\overline{RE}$) — Initiates a read of the FIFO during the next clock period (providing the $\overline{WE}$ is not asserted during the same clock period). The data from the FIFO is registered and appears on the Data Out (DO) pins during the second clock period after the corresponding $\overline{RE}$. The data will be valid until the next entry is read. $\overline{RE}$ may be asserted continuously to read out successive FIFO entries; however, note that reads have lower priority than writes and will be blocked whenever $\overline{WE}$ is asserted during the same clock period. [This condition may be detected by forming a "Data Out Valid" signal from the ANDing of one-clock-period-delayed versions of the $\overline{RE}$ and $\overline{WE}$ signals, as in Figure 1.]

If the FIFO is empty, reads can be inhibited by asserting the OUI input. If overflow and underflow are not inhibited, then reads will continue even when the FIFO is empty. In this case, the read pointer will wrap-around.

CLOCK — The differential clock controls all registers in the device. All registers are clocked on the falling edge of CLOCK. The clock frequency may be up to 200MHz (there is no minimum clock frequency).

DATA IN (DI_0–DI_{17}) — The 18 bits of input data are registered on each falling edge of the clock.

OVERFLOW/UNDERFLOW INHIBIT (OUI) — This input controls read and write pointer updates when the FIFO is full or empty. If inhibited, then no writes will be performed when the FIFO is full and no reads will be performed when the FIFO is empty.

OUTPUT SIGNALS

DATA OUTPUT (DO_0–DO_{17}) — The 18 bits of output data are driven by the FIFO output register. This register is clocked on each falling edge of the clock.

FULL — This flag is set high whenever the cumulative number of writes is greater than the cumulative number of reads by 64. The flag will be reset by the next read operation.

HALF-FULL — This flag is set high when the read pointer is 32 or more entries behind the write pointer (e.g., reading out word 15, writing into word 47).

EMPTY — This flag is set high when the last location written has been read. The flag will be reset by the next write operation. Reset will set the empty flag high.

OVERFLOW — This flag is set high when the FIFO is full and another write occurs. This flag is enabled only when OUI is not asserted.

UNDERFLOW/OE — This flag is set high when the FIFO is empty and another read occurs. This flag is enabled only when OUI is not asserted.

If OVER/UNDERFLOW INHIBIT is a low, then the UNDERFLOW/OE pin becomes an input pin to enable DATA OUTPUTS. In this case, a high on the UNDERFLOW/OE pin will enable all DATA OUTPUTS and a low will disable DATA OUTPUTS. This allows the DATA OUTPUTS to be bused with other chips.

If OVER/UNDERFLOW INHIBIT is a high, then the DATA OUTPUTS are enabled.

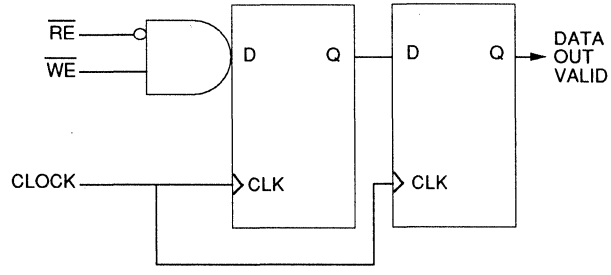


Figure 1.

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	–8 to 0	V_{dc}
Input Voltage (V_{CC} = 0V)	V_I	0 to V_{EE}	V_{dc}
Output Current Continuous Surge	I_{OUT}	 50 100	mA
OperatingTemperature Range 10KH Series 100K Series	T_A	 0 to +75 0 to +85	°C
Operating Range[2]	V_{EE}	–5.7 to –4.2	V

NOTES:

1. Beyond which device life may be impaired.
2. Parametric values specified at::
   10KH series: –4.94V to –5.46V
   100K series: –4.2V to –4.8V

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	SY69167		SY69267		Unit
		Min.	Max.	Min.	Max.	
t_{CLKL}	Input Clock Low	2.5	—	2.5	—	ns
t_{CLKP}	Input Clock Period	5	—	5	—	ns
t_{SU}	Input Set-up Time	1.3	—	1.3	—	ns
t_{WP}	Write Enable Pulse Width	1	—	1	—	ns
t_H	Input Hold Time	0.1	—	0.1	—	ns
t_{DO}	Data Output Access Time	t_{CLKP}	t_{CLKP}+1.7	t_{CLKP}	t_{CLKP}+1.7	ns

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = Max.		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IH}	Input HIGH Current		—	150	—	150	—	150	µA
I_{EE}	Power Supply Current	69167	—	—	—	975	—	—	mA
		69267	—	—	—	975	—	—	

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10KH DC ELECTRICAL CHARACTERISTICS

V_{EE} = –5.2V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = Max.		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	–1020	–840	–980	–810	–920	–735	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1630	–1950	–1630	–1950	–1600	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1070	–735	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.3	—	0.3	—	µA

NOTE:

1. 10KH series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts.

100K DC ELECTRICAL CHARACTERISTICS

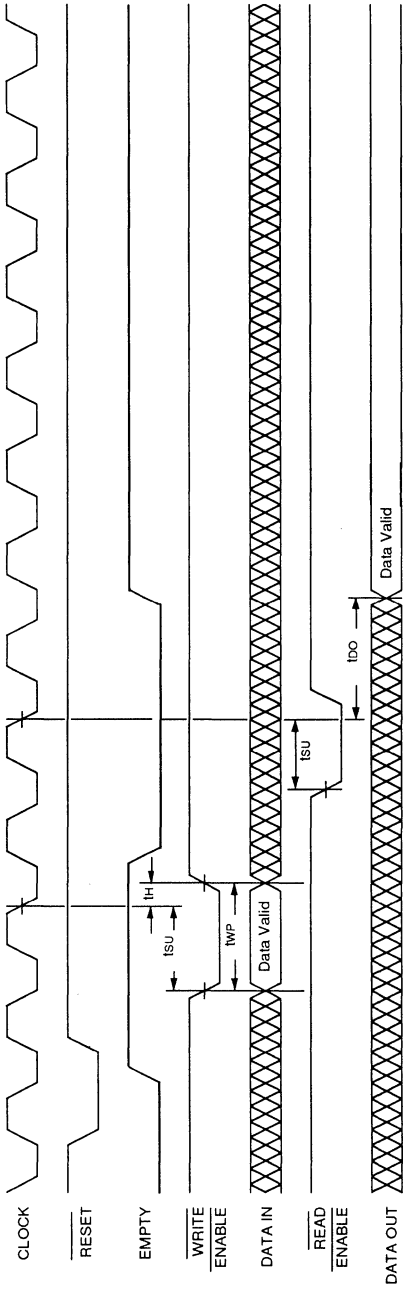
V_{EE} = –4.5V ± 5%; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL} (Min.)	50Ω to –2.0V
V_{OHA}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	
V_{OLA}	Output LOW Voltage	—	—	–1610	mV	or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IL} (Min.)	

NOTE:

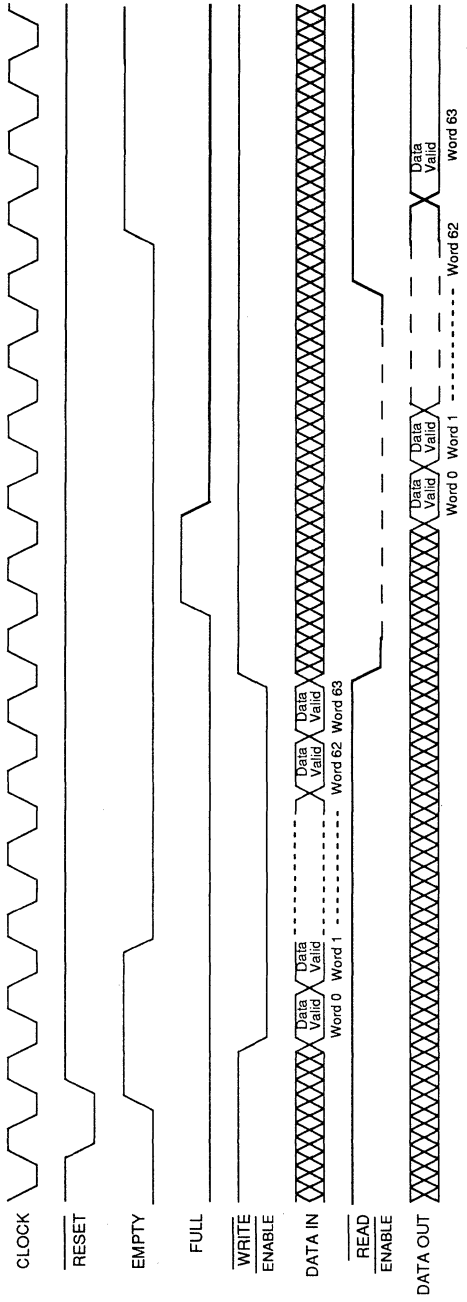
1. 100K series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts.

TIMING DIAGRAMS



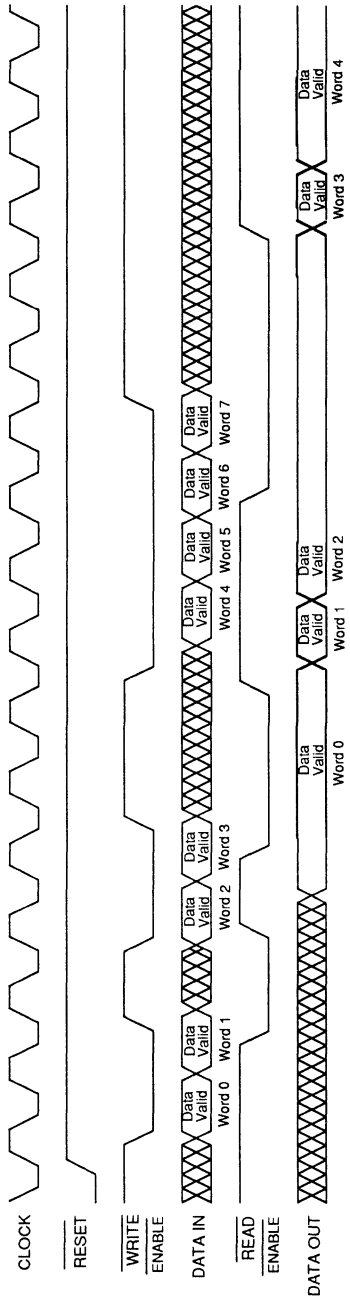
Basic Operation: Reset followed by a single write and a single read (note FULL and EMPTY flags).

TIMING DIAGRAMS (CONTINUED)



Burst Operation: Reset, Write until full, then Read until empty.

TIMING DIAGRAMS (CONTINUED)



Interlaced Operation: Reset, asynchronous writing and reading of single and multiple words (note that Write operations take priority over Read operations).

SYNERGY SEMICONDUCTOR

ULTRA-HIGH-SPEED 64-WORD x 18-BIT FIFO

PRELIMINARY
SY69168
SY69268

FEATURES

- 10ns read and/or write cycle
- System clock speeds to 100MHz
- Selectable OVERFLOW and UNDERFLOW interrupts
- EMPTY, FULL and HALF-FULL status flag outputs
- Simple initialization via $\overline{\text{RESET}}$ input
- Compatible with ECL logic standards: SY69168 for 10KH designs or SY69268 for 100K designs
- Improved noise margins via on-chip voltage and temperature compensation; designed for alpha-particle immunity
- Retransmit of data
- Independent output enable
- Available in thermally-enhanced 64-pin Quad Flatpack (QFP)
- Power dissipation only 4 watts (typ.)

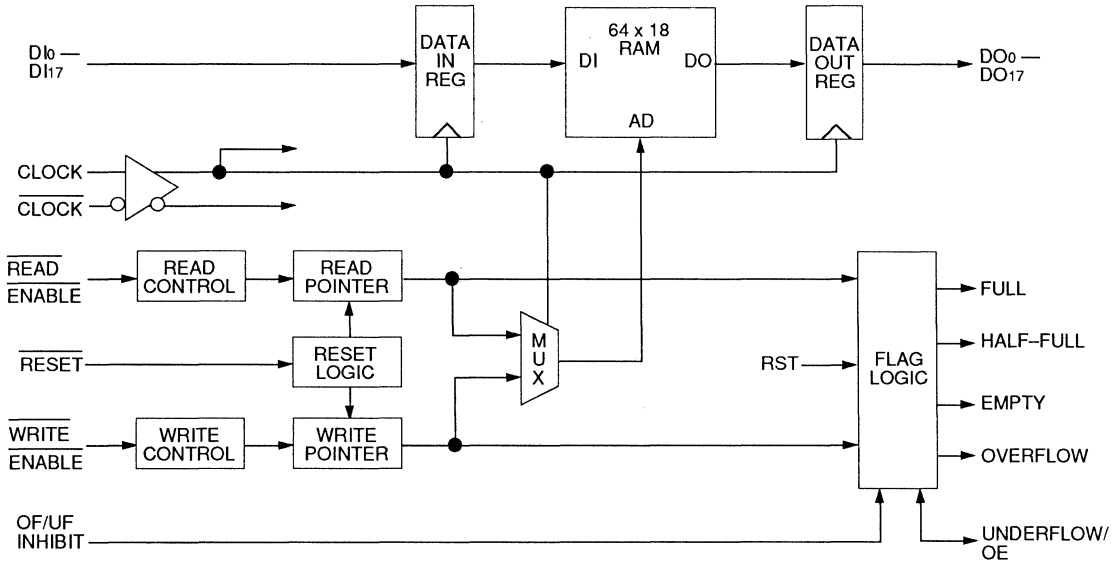
DESCRIPTION

Synergy's SY69168 and SY69268 are ultra-high-speed 64-word-by-18-bit First-In/First-Out (FIFO) static memories. Both are fabricated in Synergy's proprietary ASSET™ bipolar process.

With a system clock up to 100MHz applied to the FIFO, data is written into or read out of the memory under control of the WRITE ENABLE or READ ENABLE input, respectively; one read and/or one write operation per clock cycle. All address vectors are generated internally. FULL, HALF-FULL and EMPTY status flags, plus selectable OVERFLOW and UNDERFLOW interrupt outputs are provided. The RESET input initializes the device and resets both read and write pointers to zero. All inputs and outputs (except the differential CLOCK inputs) are single-ended ECL (SY69168 for 10KH, SY69268 for 100K).

Synergy's circuit design techniques, coupled with ASSET technology, result in not only ultra-fast performance, but allow device operation at reduced power levels, with virtually no soft error sensitivity. Outstanding reliability is achieved in volume production.

BLOCK DIAGRAM



ASSET is a trademark of Synergy Semiconductor Corporation.

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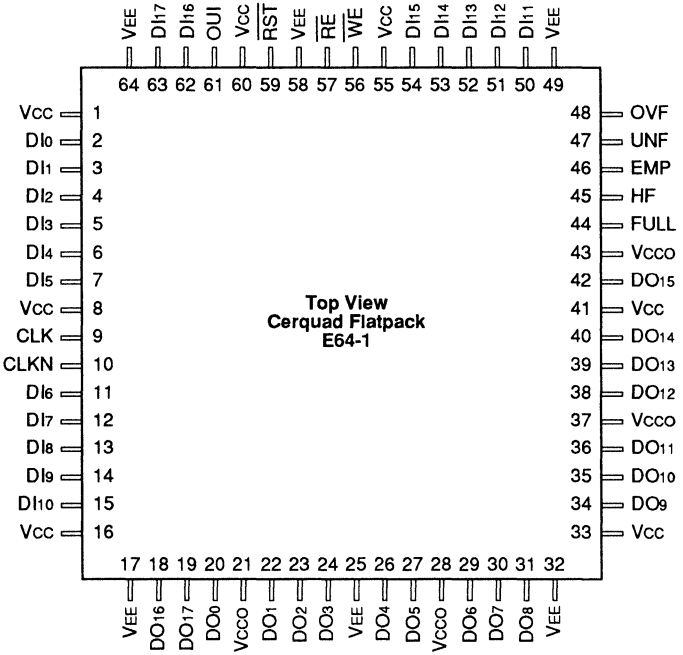
PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The Synergy SY69168/268 synchronous FIFOs are ultra-high-performance, wide-word First-In/First-Out buffers. The single-clock synchronous design yields a 200MByte/sec. bandwidth which is easily usable without the complicated timing constraints of lower-performance CMOS FIFOs. The design is a single-stage pipeline with all control and data signals registered on the falling edge of the clock so that only set-up and hold, with respect to the clock, need to be observed. The FIFO's 18-bit width allows two parity-checked bytes per device for reduced board area.

All input signals are sampled on the falling edge of the clock. The corresponding activity is initiated during the next clock period; one clock period equals one FIFO cycle. If a write operation is requested, it occurs during the first half (clock low) of the cycle; if a read operation is requested, it occurs during the second half (clock high) of the cycle. All output signals are driven by registers which are also clocked on the falling edge.

INPUT SIGNALS

RESET — Reset of the device occurs whenever this input is pulled low. Reset consists of setting the read and write pointers to zero and clearing the condition flags (except for EMPTY). The EMPTY flag is set high on reset.

Reset will set both write and read pointers to zero if READ ENABLE is high during the same clock period. Reset will set only the read pointer to zero if READ ENABLE is low at the same clock period. This independent reset of the read pointer allows retransmit of the FIFO data.

WRITE ENABLE ($\overline{WE}$) — Initiates a write into the FIFO during the next clock period. The data written is the data present on the Data Input (DI) lines concurrent with the asserted $\overline{WE}$ input. $\overline{WE}$ may be asserted continuously and the corresponding data during each clock period will be written into the FIFO. If the FIFO is full, further writes can be inhibited by asserting the OVERFLOW/UNDERFLOW

INHIBIT (OUI) input. If OUI is not asserted, then writes can continue even when the FIFO is full. In this case, the write pointer will wrap-around.

READ ENABLE ($\overline{RE}$) — Initiates a read of the FIFO during the next clock period. The data from the FIFO is registered and appears on the Data Out (DO) pins one clock period after the corresponding $\overline{RE}$. The data will be valid until the next entry is read. $\overline{RE}$ may be asserted continuously to read out successive FIFO entries.

If the FIFO is empty, reads can be inhibited by asserting the OUI input.. If overflow and underflow are not inhibited, then reads will continue even when the FIFO is empty. In this case, the read pointer will wrap-around.

CLOCK — The differential clock controls all registers in the device. All registers are clocked on the falling edge of CLOCK. The clock frequency may be up to 100MHz (there is no minimum clock frequency).

DATA-IN (DI_0–DI_{17}) — The 18 bits of input data are registered on each falling edge of the clock.

ABSOLUTE MAXIMUM RATINGS[1]

Rating	Symbol	Value	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	–8 to 0	Vdc
Input Voltage (V_{CC} = 0V)	V_I	0 to V_{EE}	Vdc
Output Current Continuous Surge	I_{OUT}	 50 100	mA
OperatingTemperature Range 10KH Series 100K Series	T_A	 0 to +75 0 to +85	°C
Operating Range[2]	V_{EE}	–5.7 to –4.2	V

NOTES:

1. Beyond which device life may be impaired.
2. Parametric values specified at::
   10KH series: –4.94V to –5.46V
   100K series: –4.2V to –4.8V

OVERFLOW/UNDERFLOW INHIBIT (OUI) — This input controls read and write pointer updates when the FIFO is full or empty. If inhibited, then no writes will be performed when the FIFO is full, and no reads will be performed when the FIFO is empty.

OUTPUT SIGNALS

DATA OUTPUT (DO_0–DO_{17}) — The 18 bits of output data are driven by the FIFO output register. This register is clocked on each falling edge of the clock.

FULL — This flag is set high whenever the cumulative number of writes is greater than the cumulative number of reads by 64. The flag will be reset by the next read operation.

HALF-FULL — This flag is set high when the read pointer is 32 or more entries behind the write pointer (e.g., reading out word 15, writing into word 47).

EMPTY — This flag is set high when the last location written has been read. The flag will be reset by the next write operation. Reset will set the empty flag high.

OVERFLOW — This flag is set high when the FIFO is full and another write occurs. This flag is enabled only when OUI is not asserted.

UNDERFLOW/OE — This flag is set high when the FIFO is empty and another read occurs. This flag is enabled only when OUI is not asserted.

If OVER/UNDERFLOW INHIBIT is a low, then the UNDERFLOW/OE pin becomes an input pin to enable DATA OUTPUTS. In this case, a high on the UNDERFLOW/OE pin will enable all DATA OUTPUTS and a low will disable DATA OUTPUTS. This allows the DATA OUTPUTS to be bused with other chips.

If OVER/UNDERFLOW INHIBIT is a high, then the DATA OUTPUTS are enabled.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	SY69168		SY69268		Unit
		Min.	Max.	Min.	Max.	
t_{CLKL}	Input Clock Low	5	—	5	—	ns
t_{CLKP}	Input Clock Period	10	—	10	—	ns
t_{SU}	Input Set-up Time	1.3	—	1.3	—	ns
t_{WP}	Write Enable Pulse Width	1	—	1	—	ns
t_H	Input Hold Time	0.1	—	0.1	—	ns
t_{DO}	Data Output Access Time	t_{CLKP}	t_{CLKP}+1.7	t_{CLKP}	t_{CLKP}+1.7	ns

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = Max.		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IH}	Input HIGH Current		—	150	—	150	—	150	µA
I_{EE}	Power Supply Current	69168	—	—	—	975	—	—	mA
		69268	—	—	—	975	—	—	

10KH DC ELECTRICAL CHARACTERISTICS

V_{EE} = –5.2V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = Max.		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	–1020	–840	–980	–810	–920	–735	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1630	–1950	–1630	–1950	–1600	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–840	–1130	–810	–1070	–735	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.3	—	0.3	—	µA

NOTE:

1. 10KH series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts.

100K DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.5V ± 5%; V_{CC} = V_{CCO} = GND; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	–1025	–955	–880	mV	V_{IN} = V_{IH} (Max.)	Loading with
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL} (Min.)	50Ω to –2.0V
V_{OHA}	Output HIGH Voltage	–1035	—	—	mV	V_{IN} = V_{IH} (Min.)	
V_{OLA}	Output LOW Voltage	—	—	–1610	mV	or V_{IL} (Max.)	
V_{IH}	Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IL} (Min.)	

NOTE:

1. 100K series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts.

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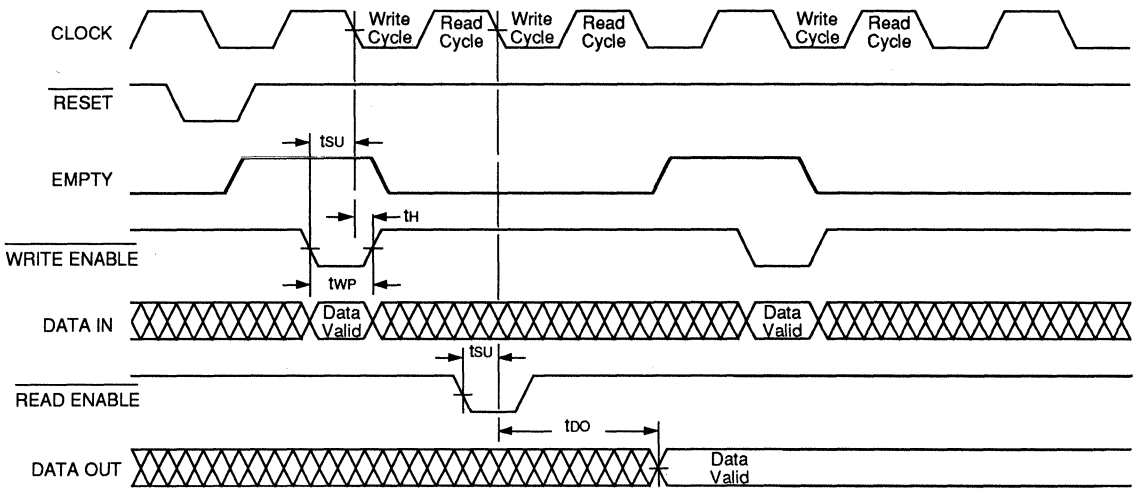
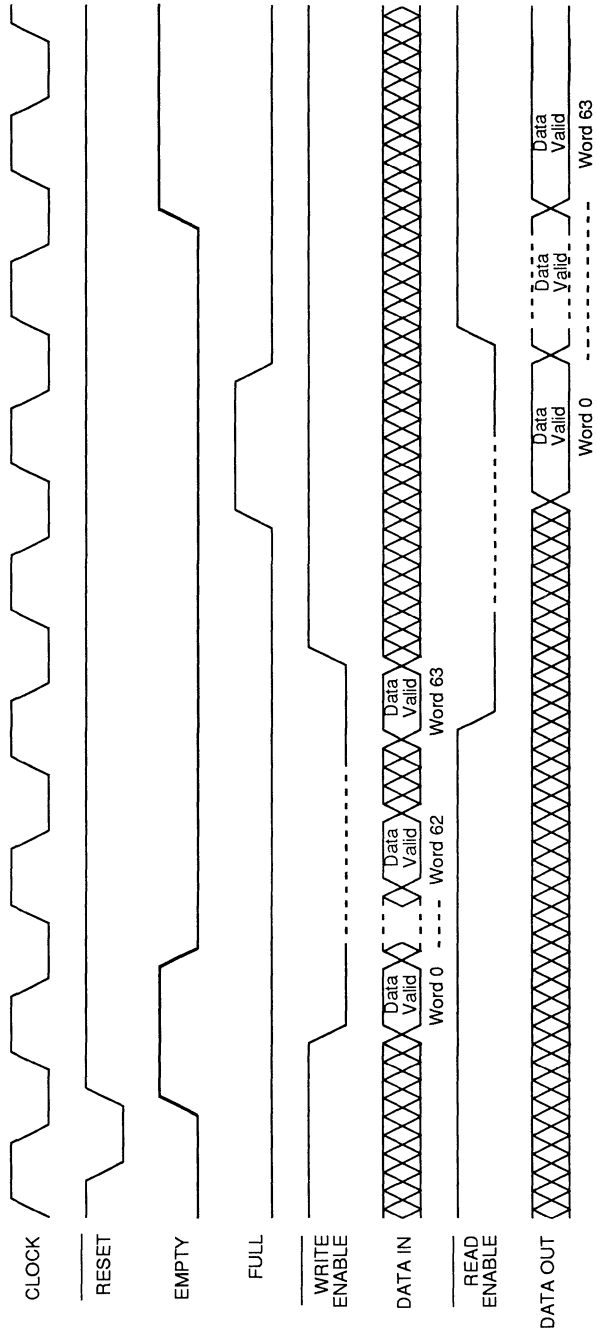
TIMING DIAGRAMS



Basic Operation: Reset followed by a single write and a single read (note FULL and EMPTY flags).

TIMING DIAGRAMS (CONTINUED)



Burst Operation: Reset, Write until full, then Read until empty.

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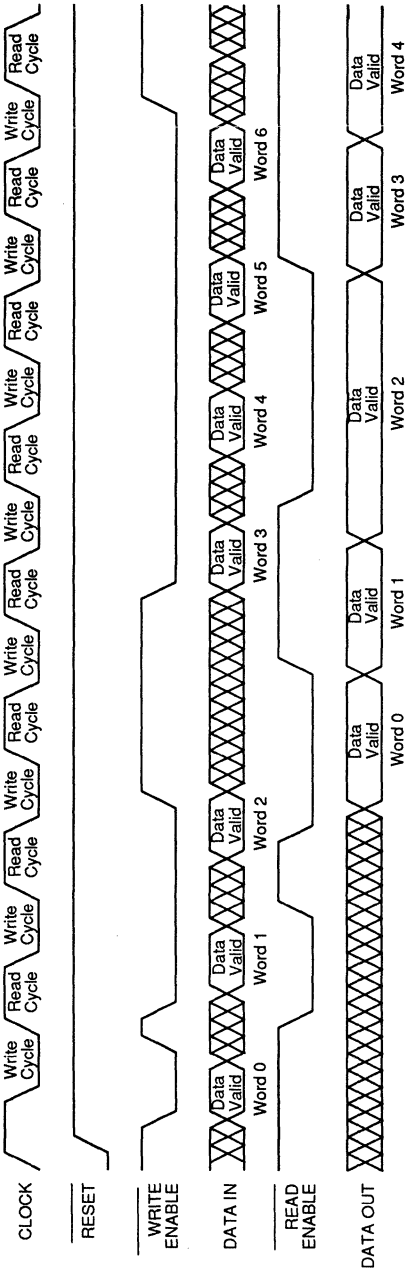
TIMING DIAGRAMS (CONTINUED)



Interlaced Operation: Reset, asynchronous writing and reading of single and multiple words (note that Write operations take priority over Read operations).

SYNERGY SEMICONDUCTOR

ULTRA-HIGH-SPEED 2K x 12 PROGRAMMABLE DELAY LINE

ADVANCE INFORMATION
SY69170

FEATURES

- **Ultra-fast — shift rates to 200MHz**
- **System clock speeds to 600MHz**
- **User-programmable delay — 2- to 2048-bit total delay with 2-bit resolution**
- **Separate controls for LOAD and RUN gives greatest flexibility**
- **Simple initialization via $\overline{\text{RESET}}$ input**
- **Compatible with 10KH ECL logic**
- **Improved noise margins via on-chip voltage and temperature compensation; designed for alpha-particle immunity**
- **Available in thermally-enhanced 208-pin PQFP or 207-pin PPGA**
- **Power dissipation = 16 watts (typ.)**

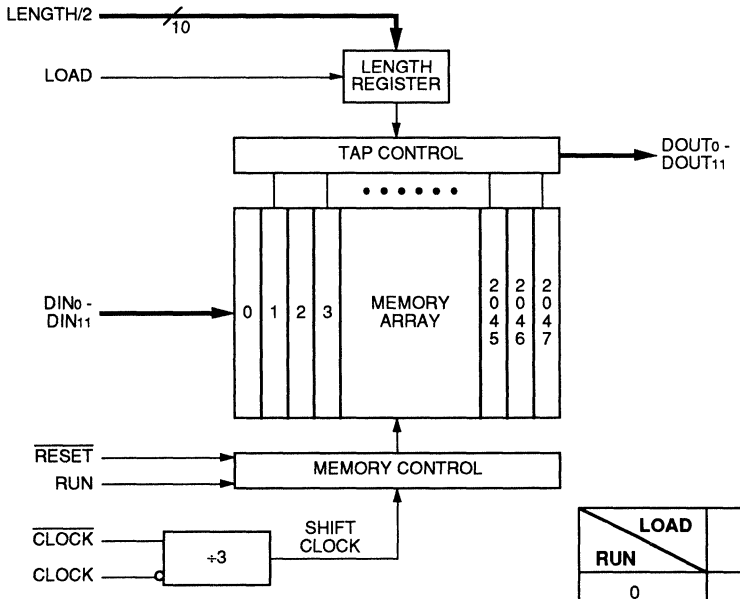
DESCRIPTION

The Synergy SY69170 is a 12-bit wide ultra-high-speed delay line fabricated in Synergy's proprietary ASSET™ I bipolar process. The line length may be user-programmed in 2-bit steps from 2 to 2048 bits.

The internal shift clock is derived from the CLOCK input (up to 600MHz, differential) and is one-third the frequency of CLOCK. Data is written into word 0 and read out of the word location specified by the Length Register on each internal clock cycle. A 10-bit Tap Length value (value = length/2) is clocked into the Length Register under control of the LOAD pin when shift is disabled. Normal shift operation occurs with RUN asserted and LOAD negated. The asynchronous RESET pin initializes the device at power- on. All inputs and outputs (except CLOCK) are single-ended ECL.

Synergy's circuit design techniques coupled with ASSET I result in ultra-fast performance, reduced power dissipation, and virtual insensitivity to soft errors. Outstanding reliability is achieved in volume production.

BLOCK DIAGRAM



RUN \ LOAD	0	1
0	X	LOAD TAP
1	SHIFT	X

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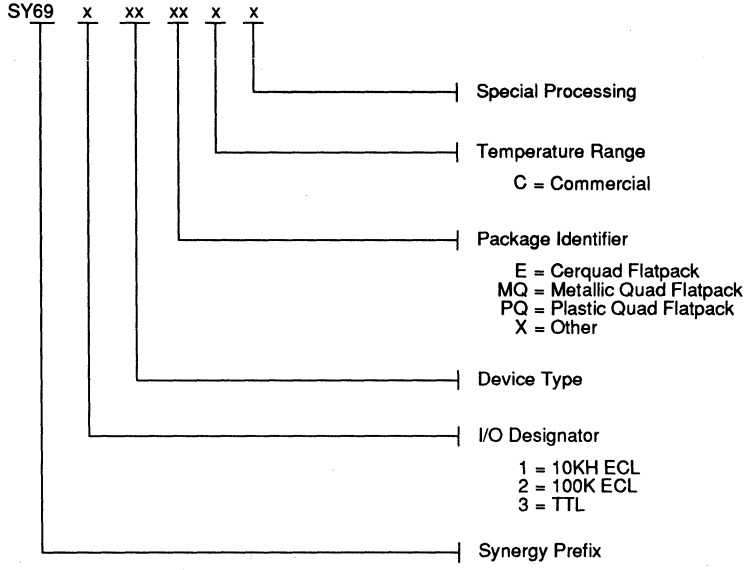
FIFO ORDERING INFORMATION



QUALITY & RELIABILITY

Synergy Semiconductor has adopted the following statement as the Mission of the Company:

To Create and Supply the Highest Performance Microelectronics Solutions, with a Total Commitment to Customer Satisfaction.

Synergy has made the decision to use the ISO 9000 as the method to meet this mission statement. Therefore, Synergy is actively working toward ISO 9001 compliance to certify the Quality Assurance and Operating Systems of the Company. Synergy Semiconductor is also utilizing the principles of Total Quality Management (TQM) throughout the Company, to ensure that all employees are involved with the process of continuous improvement through a systematic methodology of problem identification, definition, cause analysis, solution implementation and control.

Synergy's Quality System begins with the Quality Manual. This manual is written to conform to the requirements of ISO 9001 and it specifies the requirements of all operations that affect the quality of the Synergy product. It is the responsibility of the management of Synergy Semiconductor to ensure that the requirements of the Quality Systems are understood, implemented, and maintained as required by this Quality Manual. The scope of this requirement includes purchase order review, the control of the designs of the Synergy products, control of all documents that relate to the product quality, the purchased material supplies and services, product identification and traceability, process controls, inspection and testing and the maintenance of the test equipment, proper control of rejected product, corrective actions, handling, storage, packaging and delivery of the Synergy product, the maintenance of the quality records, the requirements for quality audits, the training of the Synergy personnel and, finally, the use of statistical techniques to measure the quality of the Synergy processes and products.

Synergy has combined the principles of continuous improvement with ISO 9001, because we believe that nothing that we do is "good enough". We will always strive to improve, but in a controlled manner.

Because this data book is not a controlled document, and statements and specifications in it may change from time to time as we strive for improvement, Synergy may not be held entirely liable for the contents of this book. Please contact Synergy Sales and Marketing, or an authorized sales representative of Synergy, for the latest product information.

The quality goals of Synergy are to deliver the highest quality products and services to our customers and maintain the cost of quality at its minimum value through methods which prevent the manufacture of defective units by continually striving to reduce device-to-device variability through the use of statistical process control (SPC) techniques. SPC is augmented with many traditional control systems. The quality systems, as outlined herein, are implemented to satisfy Synergy's and our customers' quality requirements.

The Quality Assurance Organization has the responsibility to represent our customers' quality goals within the Synergy environment and to verify that the intent of this program is carried out in its entirety. Verification shall be accomplished by meeting with and providing information to our customers, suppliers and Synergy management; by teaching statistical control and data analysis techniques; by auditing products, processes and systems; and by following up to ensure that corrective action is being implemented as necessary.

Product Testing Summary

Through wafer fabrication, all Synergy material is continuously monitored for conformance to requirements. Any wafer that would be a reliability hazard or expected to not yield good dice, is stopped and assigned to engineering analysis.

After polysilicon (poly2) is activated, a complete electrical Parametric Test is performed. Similarly, complete electrical Parametric Tests are also done after Metal 1 and Metal 2. Again, any wafer that would be a reliability hazard or expected to not yield good dice, is stopped and assigned to engineering analysis.

Synergy has developed the ability to perform AC wafer parametric testing at both hot and cold temperatures, if required, for die shipments or economic reasons such as assembly in an expensive package.

Post assembly, all products go through a test flow whose objective is to guarantee, as a minimum, the specification of the data sheet. Customer special requirements are reviewed by Synergy product engineering staff and included in the test programs and/or customized test flows.

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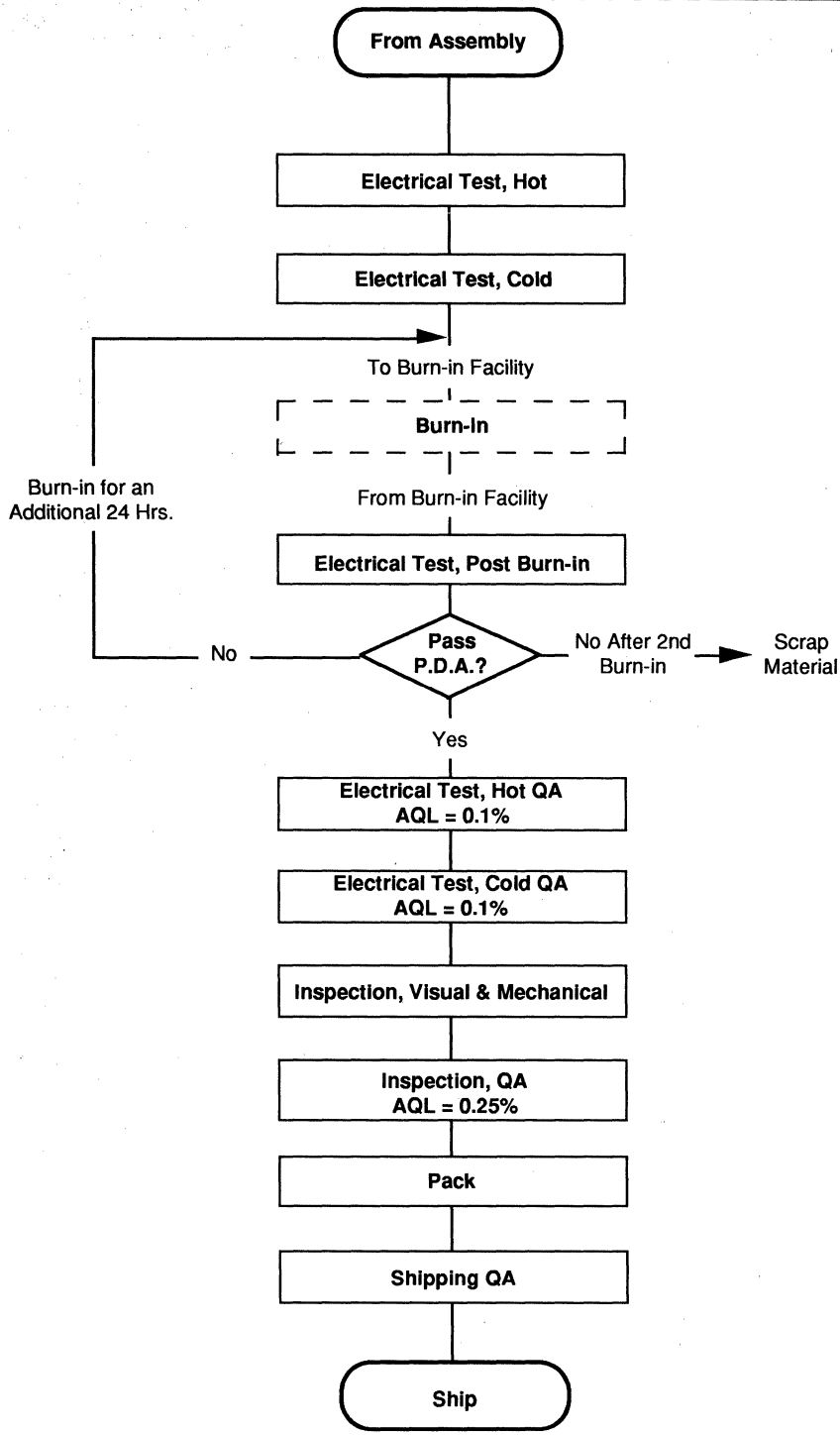
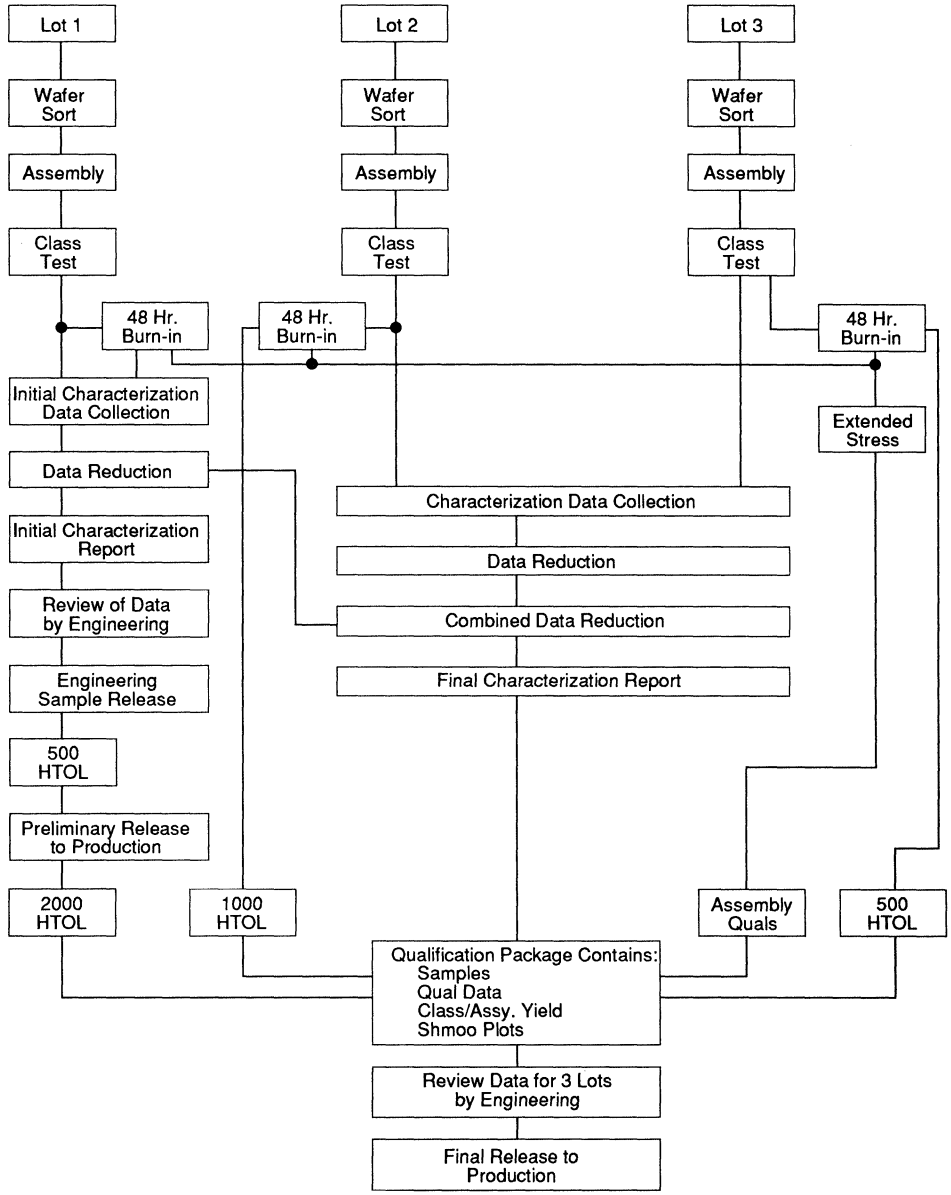

From Assembly
Electrical Test, Hot
Electrical Test, Cold
To Burn-in Facility
Burn-In
Burn-in for an Additional 24 Hrs.
From Burn-in Facility
Electrical Test, Post Burn-in
Pass P.D.A.?
No
No After 2nd Burn-in
Scrap Material
Yes
Electrical Test, Hot QA AQL = 0.1%
Electrical Test, Cold QA AQL = 0.1%
Inspection, Visual & Mechanical
Inspection, QA AQL = 0.25%
Pack
Shipping QA
Ship

Qualification Procedures

New products, packages and processes are qualified per procedures as stringent or beyond MIL-STD-883C. We also use JEDEC, ASTM and other standard test methods for non-normalized evaluations such as 85/85, ESD or ALPHA tests on RAMs.

A) Product Qualification Flow Chart
(Generic Product on Existing Technology)



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B) Package Qualification Test Conditions

Test	MIL-STD-883 Method	Test Conditions	Test Duration	End Point	Minimum Sample Size
High Temp. Storage	1008	+175°C (C,D,P) +150°C (M)	1000 Hrs.	E	45
Temperature Cycle	1010	–65°C to +150°C (C,D,M,P)	1000 Cycles	E,V (P) E,V,H (C,M,D)	45
Thermal Shock	1011	–55°C to +125°C (C,D,M,P)	100 Cycles	E,V (P) E,V,H (C,M,D)	45
Autoclave	N/A	+121°C, 2 Atm, 100% RH (M,P)	96 Hrs.	E,V	22
Humidity/HAST	N/A	+131°C, 85% RH, Biased (P)	50 Hrs.	E,V	22
Salt Atmosphere	1009	+35°C (C,D)	24 Hrs.	V	22
Solvents/Flux	2015	Chemicals (C,D,M,P)		V	11
Mechanical Shock	2002	1500G Peak (C,D)	6 Orient.	E,H	22
Variable Vibration	2007	20G Peak (C,D)	3 Orient.	E,H	22
Centrifuge	2001	30,000G (C,D)	Y1 Orient.	E,H	22
Die Adherence	2019	Die Shear (C,D,M,P)		To Destruction	5
Wire Bond	2011	Wire Pull (C,D,M,P)		To Destruction	100
Cavity Moisture	1018	+100°C Bake (C,D)	1 Cycle	ppm Water	3
Seal Integrity	2024	Lid Torque (D)		To Destruction	11
Lead Strength	2004 B2	Bend Fatigue (C,D,M,P)		To Destruction	11
Solderability	2003	+150°C +100°C Steam (C,D,M,P)	80 Hrs. 4 Hrs.	V V	11

C = Solder-sealed Ceramic, D = Glass-sealed Ceramic, P = Plastic, E = Electrical Test, H = Hermeticity Test, V = Visual Inspection

Even though the present process is state-of-the-art, both from a performance and a reliability point of view, we continuously feed back new information into the process.

Reliability failure rate is extremely low, rendering quantification very costly. However, because Synergy continuously refines the understanding of its process, it is expected to have better and better reliability as process improvements are tested and implemented per our rigorous change procedure system. A special focus is directed to failure analysis. Even though the number of failures are limited, a point is made to feed back into the process improvement program all failure analysis from any life test or customer return. The table that follows summarizes the minimum testing requirements. Also, each change is reviewed by a committee of Quality, Reliability and Process specialists that will add any test or evaluation that is viewed as necessary.

C) Process Qualification Procedures

Test Item	Test Conditions	Sample Size	Package Change	Die or Wafer Change	Assembly Change
High Temperature Storage Life	1000 hrs. @ T_A = +175°C MIL-STD-883, Method 1008	45 units/lot 1 to 3 lots	O	O	O
High Temperature and Humidity Bias Life (HAST)	50 hrs. @ T_A = +131°C, RH = 85%, V_{EE} specified per device type (plastic only)	22 units/lot 1 to 3 lots	O	O	O
Pressure Cooker	96 hrs. @ T_A = +121°C, RH = 100% (plastic only)	22 units/lot 1 to 3 lots	O	O	O
Thermal Environmental	Solder Heat @T_A = +220°C, 30 sec., 250 cycles @ –65°C to +150°C and 100 shocks @ –55°C to +125°C	45 units/lot 1 to 3 lots	O	X	O
Mechanical Environmental	20G, 10 to 2000Hz; 1500G, 0.5ms; 30000G, 1 min. (ceramic only)	22 units/lot 1 to 3 lots	O	X	O
Lead Fatigue	90 degree bends, 3 bends MIL-STD-883, Method 2004 B2	11 units/lot 1 to 3 lots	X	N/A	X
Solderability	+230°C, 5 sec., Rosin Base Flux MIL-STD-883, Method 2003	11 units/lot 1 to 3 lots	X	N/A	X
Long Term Temperature Cycle	1000 cycles @ –65°C to +150°C MIL-STD-883, Method 1010C	45 units/lot 1 to 3 lots	O	O	O

O = Performed, X = Performed, if necessary.

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Product Reliability

Design for Reliability

Our Technology and Design Rules are crafted by our resident device scientists who use very conservative rules. Typically, we look for the toughest industry standards such as 20 FITs or better. We have measured 10 FITs with a very conservatively estimated 0.5ev activation energy.

ASSET I designs include conservative device design rules. This allows us to be very successful in "shrinking" our designs. Without reaching the limit of our technology, we have, with our initial shrink, substantially improved speed performance. The interconnect is also designed conservatively with:

1.9E5 A/cm^2 for Metal 1 and
1.0E5 A/cm^2 for Metal 2,

giving good resistance to electromigration.

All minimum dimensional design rules are checked on a computer. Other design rules are checked manually. We use Cadence Physical Design Verification (PDV) software running on Sun 4 SPARCstations.

Accelerated Testing

Accelerated testing is done through:

1) HTOL, where forcing a junction temperature of +125°C to +175°C and using a conservative activation energy of 0.50ev, gives us an acceleration of between 20X and 80X.
2) Electromigration, where we use both a temperature of +150°C to +200°C and a current density of 2E6 to 5E6A/cm^2. This gives us a very aggressive acceleration, in the range of 1 hour equivalent to 1 year, which allows us to have a good estimation of the electromigration wearout of our metalization system. For electromigration, we use the Black model with the equation coefficients of Ea = 0.50ev and n = 2.0.
3) Elimination of early failures for infant mortality through burn-in. RAMs are burned-in 100% and logic is sampled to a 0.5% LTPD. Burn-in is 48 hours at a maximum junction temperature of +125°C to +175°C.
4) Alpha particle testing using 1µCi Radium 226 (Ra^{226}) with alpha flux density of 3.85 E8 alphas/cm^2/hr and 1µCi Thorium 228 (Th^{228}) with a flux density of 2.76E8 alphas/cm^2/hr. For an application density of 5.0E-2 alpha/cm^2/hr we have demonstrated a FIT soft error failure rate of much less than 200 FITs.

Wafer Process Control and Reliability

1) Wafer process control and reliability differs from wafer level parametric testing. It is a key part of our wafer level monitor program. As an example, we monitor metal width by a minimum and wide line double Kelvin measurement. This monitor has no impact on yield, but is key to the current density through a minimum line, therefore to the electromigration wearout performance.
2) Wafer process control and reliability uses several methods such as:
   - Construction analysis (cross section, with visual and SEM analysis using optical and/or microscope). Visual inspection is performed at different steps of the process.
   - SPC in-line monitors for thin film thicknesses and Sheet Rho, CDs, particle counts, etc.
   - Topside integrity
   - Parameter trend analysis of over 150 electrical parameters

In-Process

Product reliability is monitored throughout the manufacturing process using:

- Statistical Process Control (SPC) monitors for thin film thicknesses and Sheet Rho, CDs, particle counts, etc.
- Visual inspection with optical microscopes and SEMs for non-destructive and destructive analysis including cross sections.
- Specifications covering process flow, travelers through each manufacturing operation and operation procedures.
- Extensive electrical measurements (over 500 different parameters measured on every wafer after Metal 2, sampled after poly and Metal 1) and graphs of key monitors.
- Topside integrity.

End Product

The "end product" is checked extensively in wafer form with test programs that include speed measurements. After assembly in a package, parts are tested over temperature to the full data sheet specification. Then they **all** go through a 48-hour burn-in program (100% for RAMs and to a 0.5% LTPD for logic).

In addition, random samples from the standard production go through our Reliability Program:

- HTOL up to 10,000 hours
- Pressure pot up to 168 hours
- 85/85 up to 1,000 hours
- Package qualifications and monitor
- Electromigration end of life evaluation

Reliability Characterization

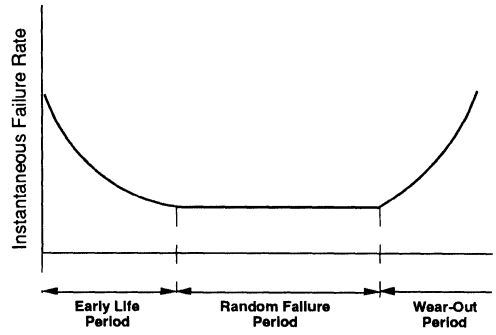
In its life time, a product typically goes through three phases of failure rate:

A) Early Life Period: when the failure rate decreases with time as the infant mortality is being weeded out.

B) Random Failure Period: when the failure rate stabilizes to a constant failure rate.

C) Wear-Out Failure Period: when the failure rate increases with time and graphs as a straight line on a log normal probability curve.

Distribution of Component Failure



Long Term Reliability Program

The long term reliability of our product is checked extensively in its packaged form, after all electrical and burn-in operations are completed. Random samples from our standard production go through Synergy's Long Term Reliability Program:

— High Temperature Operating Life (HTOL) with samples from each product family are pulled every quarter and tested up to a minimum of 2,000 hours. Some are periodically tested to End of Life (or 10,000 hours)

— Pressure pot up to 168 hours

— 85/85 up to 1,000 hours

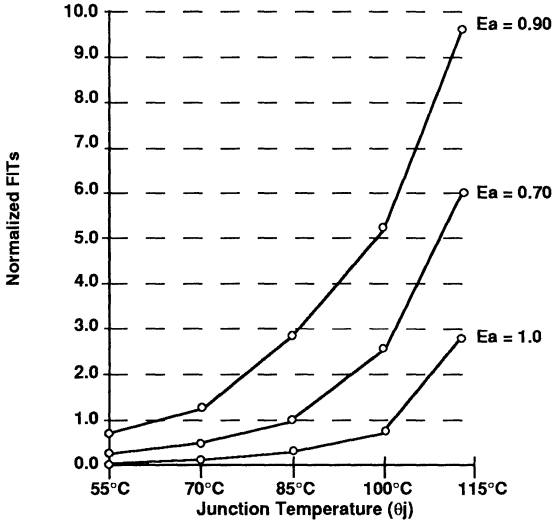
— Package qualification and monitor

— Electromigration end of life evaluation

A quarterly report is published for customer information. Such reports include projected "FIT" rate performances:

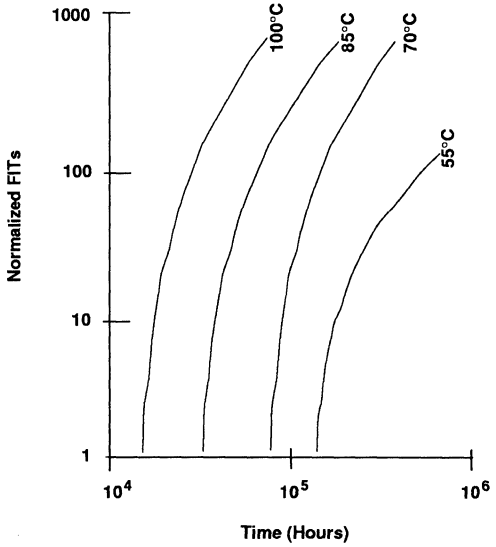
1 FIT = 1 Failure in 10^9 Devices * Hours

HTOL FIT Rate as a Function of Activation Energy & Temperature



These curves correspond to the "RANDOM FAILURE PERIOD" where there is a constant FIT rate. Through failure analysis, a dominant Activation Energy can be defined for a given product, therefore a FIT rate for a defined User Junction Temperature.

End of Life Electromigration Projection



These curves correspond to the "WEAR-OUT FAILURE PERIOD" where the FIT rate increases with time. A single metal line current density equivalence can be defined for a given product, therefore a FIT rate as a function of time for a defined User Junction Temperature.

10

Customer Returns

Customer returns are treated with high priority. Synergy's policy specifies that the customer will receive a verbal answer within 5 working days, followed by a written report within 2 weeks after we have received the return. Routinely, all customer returns are retested per the Final Test testing procedure. Any additional evaluation is under the control of the failure analysis engineer.

SYNERGY SEMICONDUCTOR

PACKAGING INDEX

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PACKAGE INFORMATION

ASSEMBLY

Synergy offers four microelectronic package technologies: (1) transfer molded epoxy resin, with and without embedded copper heat spreaders; (2) stamped, anodized aluminum cap and base with an epoxy preform applied to the sealing surfaces; (3) glass sealed ceramic; and (4) solder sealed laminated ceramic packages. Packages with a variety of lead counts and outlines (package families) are manufactured in each package technology to industry accepted dimensional standards such as JEDEC (Joint Electron Device Engineering Council). Depending on the package family, lead counts vary from 8 (SOIC) to 304 (PQFP with embedded heat spreader) leads. Packages are assembled by Synergy-qualified and controlled subcontractors which are located both domestically and abroad.

PACKAGE FAMILIES

Synergy's package families are offered for both through-hole and surface-mount applications. The through-hole class consists of Dual In-line Packages (DIPs) ranging from 20 to 28 leads. In addition, Synergy provides an assorted range of Ceramic Pin Grid Arrays as required for its Semicustom ASIC product with lead counts up to 259 leads. Synergy's through-hole offerings are summarized in Table 1.

The surface-mount class consists of Small Outline Integrated Circuits (SOICs), Plastic Leaded Chip Carriers (PLCCs), Small Outline packages (SOJs), ceramic dual packages (FPs), ceramic quad packages (CPKs), Metal Quad packages (MQUADs), and Plastic Quad Flatpacks with and without heat spreaders (PQUADs). Synergy's surface-mount offerings are summarized in Table 2.

Lead Count	Ceramic S/B DIP	CERDIP	Plastic DIP	Plastic Pin Grid Array	Ceramic Pin Grid Array
20		X			
24		X			
28	X		X		
259					X

Table 1. Synergy Through-Hole Packages

Lead Count	Quad Cerpack	Dual Cerpack	Plastic Leaded Chip Carrier	Ceramic Leaded Chip Carrier	Metallic Leaded Chip Carrier	Leadless Chip Carrier	Plastic Small Outline J-Leaded	Ceramic SOIC	Plastic SOIC	Metal Quad Flatpack	Plastic Quad w/Heat Spreader
8									X		
16							X		X		
20		X							X		
24	X										
28		X	X	X	X	X	X	X			
44			X								
64	X										
68			X								
80										X	
84			X								
128										X	
160										X	X
208										X	X
240										X	
304										X	X

Table 2. Synergy Surface-Mount Packages

In summary, the package types listed in both Tables 1 and 2 are currently available package types in production. Synergy, however, continues to investigate, tool, prototype, qualify and introduce other package types into production as required by its customer demands.

PACKAGE TECHNOLOGIES

Different package families may use essentially the same package materials, technology and assembly procedures. For example, the materials and assembly processes are quite similar between the plastic PDIP, SOIC, PQFP and PLCC families or between the Cerpack and Cerdip families. Therefore, the assembly flows can be simply summarized for each of the three main package technologies, as shown in Table 3.

Process Step	Glass-Sealed Ceramic	Solder-Sealed Ceramic	Molded Plastic	Metal Quad
Die Prep	Wafer Saw D.I. Wash	Wafer Saw D.I.Wash	Wafer Saw D.I. Wash	Wafer Saw D.I. Wash
2nd Optical	50X Die Visual Gate	50X Die Visual Gate	50X Die Visual Gate	50X Die Visual Gate
Die Atttach	Gold Eutectic Jumper Chips	Gold Eutectic	Silver Epoxy Cu Leadframe	Silver Epoxy Cu Leadframe
Wire Bond	Ultrasonic Aluminum Wire	Ultrasonic Aluminum Wire	Thermosonic Gold Wire	Ultrasonic Aluminum Wire
3rd Optical	30X Internal Visual Gate	30X Internal Visual Gate	30X Internal Visual Gate	30X Internal Visual Gate
Seal	Glass 10 min. @ +430°C	Au-Sn Solder 15 min. @ +320°C	Epoxy 6 hrs. @ +175°C	Epoxy 6 hrs. @ +175°C
Mark	Epoxy Ink	Epoxy Ink	Epoxy Ink	Epoxy Ink
Lead Finish	Tin Plate	Gold Plate (As Received)	Solder Plate Deflash	Solder Plate
Hermeticity	Fine Leak Gross Leak (NID)	Gross Leak (Bubble Test Only)	Not Applicable	Gross Leak (Bubble Test Only)
Trim/Form	Singulate Leads Form Leads	Singulate Leads Form Leads	Singulate Leads Form Leads	Singulate Leads Form Leads
4th Optical	3X External Visual Gate	3X External Visual Gate	3X External Visual Gate	3X External Visual Gate
Pack	Antistatic Tube Carriers	Antistatic Tube Carriers	Antistatic Tube Carriers	Antistatic Tube

Table 3. Synergy Commercial Assembly Flows

ASSEMBLY SITES

Synergy maintains one domestic subcontractor: Indy Electronics, Inc., in Manteca, California. Indy is tuilized primarily for the assembly of MQUADs.

Amkor Electronics, Inc. provides Synergy's high volume production assembly in either its Korean (Anam Industrial Co., Ltd., AICL) facilities or its Philippines (Amkor/Anam Pilipinas Inc., AAPI) facility, depending on the package family. Amkor is a leader in quality high volume assembly production and the world's largest assembly subcontractor. All Amkor facilities are certified to ISO9002 (a series of manufacturing standards set by the International Standards Organization which defines what a quality system should do). Amkor has a well established Statistical Process Control (SPC) program to ensure high quality assembly. Communications between Synergy and all Amkor assembly sites are on a real-time basis through computer networking with CAMSTAR software on AS400 systems. In addition to tracking of Work-In-Process (WIP), Synergy also receives assembly yield and quality reports on a weekly and monthly basis. The philosophies and methodologies of Continuous Improvement (CI) are constantly being implemented at Amkor; there is a heavy emphasis on training.

PACKAGE RELIABILITY

Package failure mechanisms can originate from errors in die design, integrated circuit wafer processing, package materials, or package assembly processing. Improper handling of the assembled device is a common cause of IC failures. Furthermore, a package failure mechanism may be determined by the environment to which the package is subjected. Environmental stresses, such as temperature, humidity, mechanical force, electrical stress, or combinations of these, can promote circuit failures.

Synergy conducts package environmental and high temperature operating life integrity tests for two reasons:

1. To qualify new packages, assembly facilities, major assembly process changes, and major package materials changes. In addition, major wafer process changes, as well as external wafer foundries, are qualified in the same manner. This assures that the new capability meets Synergy's required integrated circuit quality standards.
2. To serve as a routine production monitor of all assembly facilities to detect any long term shifts in package quality and reliability performance.

The particular series of stress tests chosen to qualify a new package depends on the particular package technology and the specific failure mechanism of interest. The ceramic packages are assembled in such a manner that their cases are impervious to moisture. Thus, they are considered to be hermetic. In general, each of the assembly technologies have certain attributable unique failure mechanisms. In order to root out failure mechanism causes, Table 4 shows which environmental and mechanical tests are appropriate for each of the four package technologies.

Test	MIL-STD-883 Method	Test Conditions	Test Duration	End Point	Minimum Sample Size
High Temp. Storage	1008	+175°C (C,D,P) +150°C (M)	1000 Hrs.	E	45
Temperature Cycle	1010	–65°C to +150°C (C,D,M,P)	1000 Cycles	E,V (P) E,V,H (C,M,D)	45
Thermal Shock	1011	–55°C to +125°C (C,D,M,P)	100 Cycles	E,V (P) E,V,H (C,M,D)	45
Autoclave	N/A	+121°C, 2 Atm, 100% RH (M,P)	96 Hrs.	E,V	22
Humidity/HAST	N/A	+131°C, 85% RH, Biased (P)	50 Hrs.	E,V	22
Salt Atmosphere	1009	+35°C (C,D)	24 Hrs.	V	22
Solvents/Flux	2015	Chemicals (C,D,M,P)		V	11
Mechanical Shock	2002	1500G Peak (C,D)	6 Orient.	E,H	22
Variable Vibration	2007	20G Peak (C,D)	3 Orient.	E,H	22
Centrifuge	2001	30,000G (C,D)	Y1 Orient.	E,H	22
Die Adherence	2019	Die Shear (C,D,M,P)		To Destruction	5
Wire Bond	2011	Wire Pull (C,D,M,P)		To Destruction	100
Cavity Moisture	1018	+100°C Bake (C,D)	1 Cycle	ppm Water	3
Seal Integrity	2024	Lid Torque (D)		To Destruction	11
Lead Strength	2004 B2	Bend Fatigue (C,D,M,P)		To Destruction	11
Solderability	2003	+150°C +100°C Steam (C,D,M,P)	80 Hrs. 4 Hrs.	V V	11

C = Solder-sealed Ceramic, D = Glass-sealed Ceramic, P = Plastic, E = Electrical Test, H = Hermeticity Test, V = Visual Inspection

Table 4. Package Qualification Test Conditions

Note that not all of the tests listed in Table 4 are necessary for a new package or an assembly process change. It is only necessary to focus on a weakness likely to be introduced by the change. Table 5 summarizes the tests required for various types of materials/process changes.

Test Item	Test Conditions	Sample Size	Package Change	Die or Wafer Change	Assembly Change
High Temperature Storage Life	1000 hrs. @ T_A = +175°C MIL-STD-883, Method 1008	45 units/lot 1 to 3 lots	O	O	O
High Temperature and Humidity Bias Life (HAST)	50 hrs. @ T_A = +131°C, RH = 85%, V_{EE} specified per device type (plastic only)	22 units/lot 1 to 3 lots	O	O	O
Pressure Cooker	96 hrs. @ T_A = +121°C, RH = 100% (plastic only)	22 units/lot 1 to 3 lots	O	O	O
Thermal Environmental	Solder Heat @T_A =+ 220°C, 90 sec., 250 cycles @ –65°C to +150°C and 100 shocks @ –55°C to +125°C	45 units/lot 1 to 3 lots	O	X	O
Mechanical Environmental	20G, 10 to 2000Hz; 1500G, 0.5ms; 30000G, 1 min. (ceramic only)	22 units/lot 1 to 3 lots	O	X	O
Lead Fatigue	90 degree bends, 3 bends MIL-STD-883, Method 2004 B2	11 units/lot 1 to 3 lots	X	N/A	X
Solderability	+230°C, 5 sec., Rosin Base Flux MIL-STD-883, Method 2003	11 units/lot 1 to 3 lots	X	N/A	X
Long Term Temperature Cycle	1000 cycles @ –65°C to +150°C MIL-STD-883, Method 1010C	45 units/lot 1 to 3 lots	O	O	O

O = Performed, X = Performed, if necessary.

Table 5. Materials/Process Changes Requiring Qualification

THERMAL RESISTANCE

Semiconductor integrated circuits dissipate heat while operating; typically, the faster the operating frequency, the more heat is dissipated by the device. This temperature increase on the junction of the die is a direct function of: (1) the amount of power dissipated in the circuit, and (2) on the net thermal resistance between the heat source and a reference point such as the surrounding ambient of still air at +25°C. It has been established (literature) that the long-term reliability of a semiconductor component is a direct function of the die junction temperature at which it is operated. It is, therefore, necessary to consider the thermal resistance of the IC package before mounting on to a board.

The thermal resistance of a package is a measure of the package's ability to transfer heat from the die to the surrounding environment. The basic formula for converting power dissipation to estimated junction temperature can be mathematically described as follows:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D (\theta_{JA}) \quad (2)$$

where:

T_J = device junction temperature
T_A = ambient temperature (still air)
P_D = calculated device power dissipation in watts
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient

Only two terms on the right side of the equation can be varied by the user — the ambient temperature and the device case-ambient thermal resistance. Under recommended use, the V_{EE} supply and loading

dictate a fixed power dissipation. The θ_{CA} term is affected by the system air flow and the package mounting technique. On the other hand, the θ_{JC} term is essentially independent of air flow and the external mounting technique. It is a function of the package material thermal conductivities, die bonding method and die area.

There are additional factors which affect the thermal resistance of any particular package type such as:

a. Die Size has a large effect with smaller die sizes resulting in higher thermal resistance if other package parameters remain unchanged.
b. Die Attach methods and materials can have large effects on thermal resistance if there is excessive voiding. Device reliability and mechanical stress are also affected.
c. Leadframe material plays a major role, particularly for plastic packages. Copper (with its superior conductive properties over A42) leadframes greatly improve thermal resistance performance. The larger the die attach pad, the lower the thermal resistance value.
d. Package Body Material can also have a large affect on thermal resistance, however, selection of a particular package type is dictated by reliability, manufacturing, cost, etc.
e. Embedded Heat Spreaders play a major role in the reduction of thermal resistance.

Typical (average) values of junction-to-ambient operating temperature values are listed for various packages in Table 6.

No. Leads	Body Style	Body Material	Leadframe Material	Body Width	Die Bond	Avg. Die Area (Sq. Mils)	Avg. PAD Area (Sq. Mils)	Avg. θ_{JA} (°C/W)
8	SOIC	Epoxy	Cu	0.150"	Epoxy	8,000	15,000	150
16	SOIC	Epoxy	Cu	0.300"	Epoxy	8,100	22,500	95
20	SOIC	Epoxy	Cu	0.300"	Epoxy	8,100	22,500	85
24	Cerdip	Alumina	A42	0.300"	Eutectic	16,000	38,800	65
24	Cerdip	Alumina	A42	0.400"	Eutectic	11,200	38,800	65
28	PLCC	Epoxy	Cu	0.450"	Epoxy	16,000	40,000	60
28	Sidebraze	Alumina	A42	0.400"	Eutectic	56,500	98,800	50
28	MQUAD	Aluminum	Cu	0.450"	Epoxy	16,000	40,000	50
44	PLCC	Epoxy	Cu	0.450"	Epoxy	16,000	40,000	50
160	PQUAD	Epoxy w/H/S*	Cu	28mm	Epoxy	160,000	377,000	17
208	MQUAD	Aluminum	Cu	28mm	Epoxy	160,000	223,000	19

***NOTE:**
Heatspreader size is 22mm square.

Table 6. Thermal Resistance Values at Still Air

As already mentioned, junction-ambient thermal resistance, θ_{JA}, of a particular package is a function of die size, materials, package geometry, power dissipation, etc. The way that an IC package is mounted and positioned relative to the direction and magnitude of forced air cooling within the operating system has a major effect on thermal resistance. Figure 1 shows the typical decrease in θ_{JA} as air flow is increased from Still Air to 1,000 linear feet per minute (lfm) over low lead count (<44) packages soldered to a printed circuit board. Packages are often mounted in an inverted position such that the case surface in contact with the die is exposed to the greatest amount of air flow to achieve the lowest operating junction temperature. In general, θ_{JA} and θ_{JC} decrease with an increase in die size, power dissipation and package size. Thermal resistance will also decrease with the use of lower conductivity package materials.

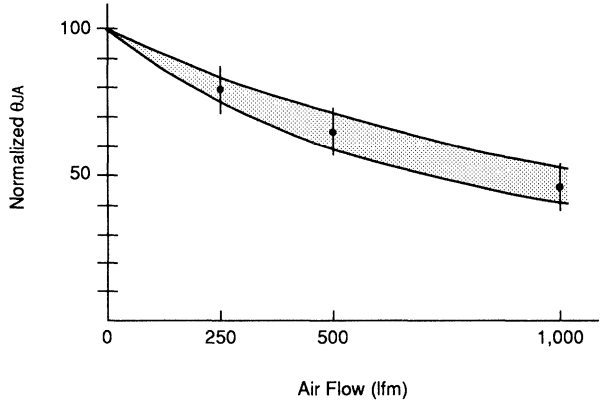


Figure 1. Effect of Air Flow on Thermal Resistance

External heat sinks applied to the IC package also have a major impact in lowering thermal resistance by increasing the heat flow to the ambient environment, particularly in high pincount devices. Heat sink performance will vary by size, material, design, system air flow, positioning, etc. Figure 2 shows the effect of heat sinks on a 208-MQUAD and a 160-PQFP with an embedded heat spreader.

208 MQUAD and 160 PQII Thermal Resistance

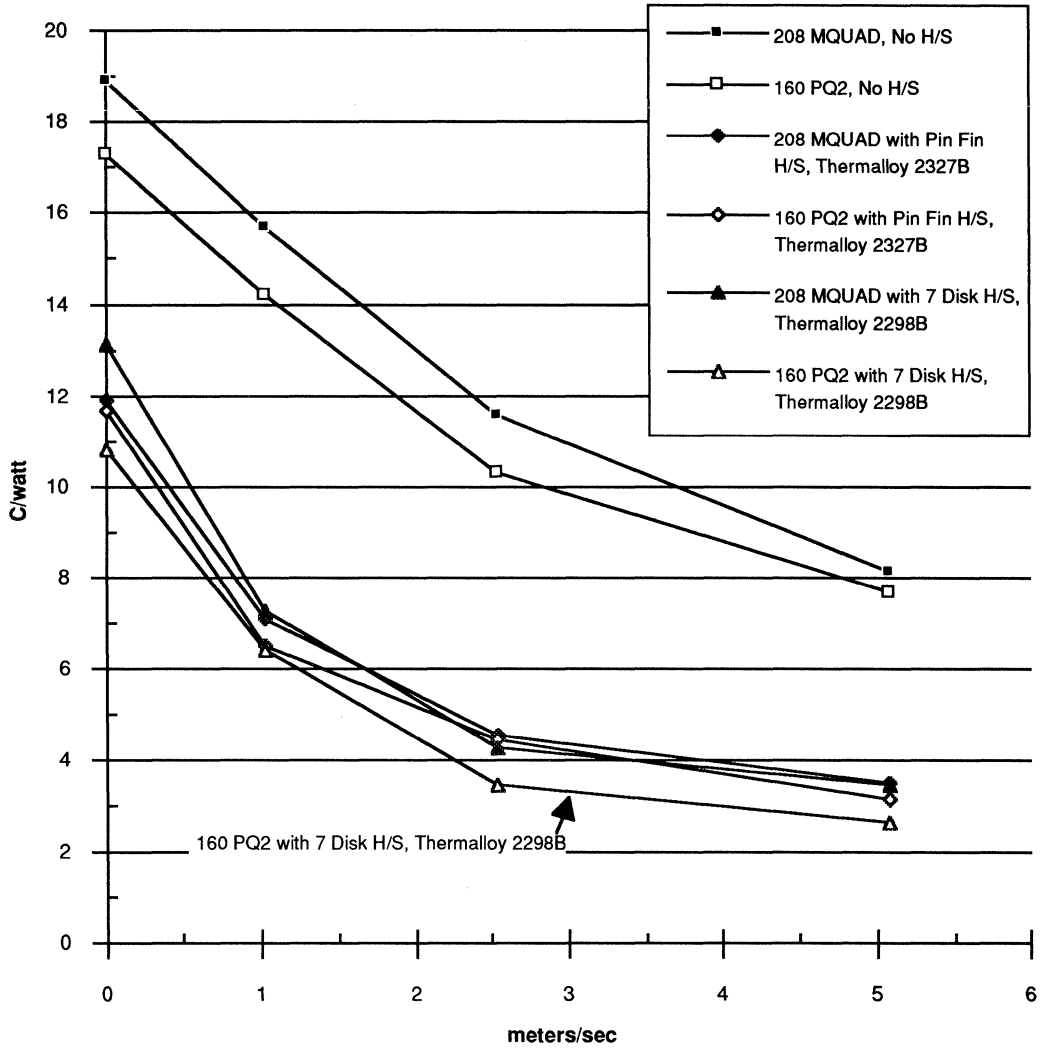
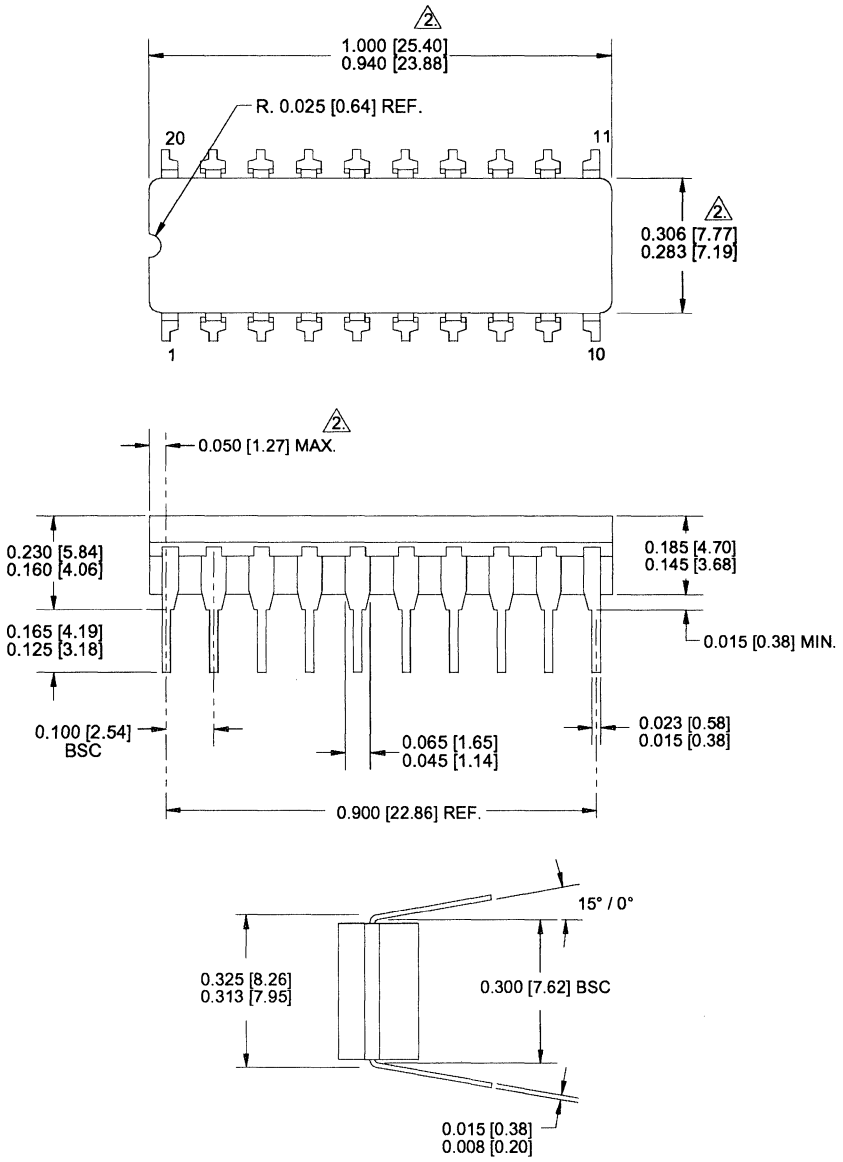


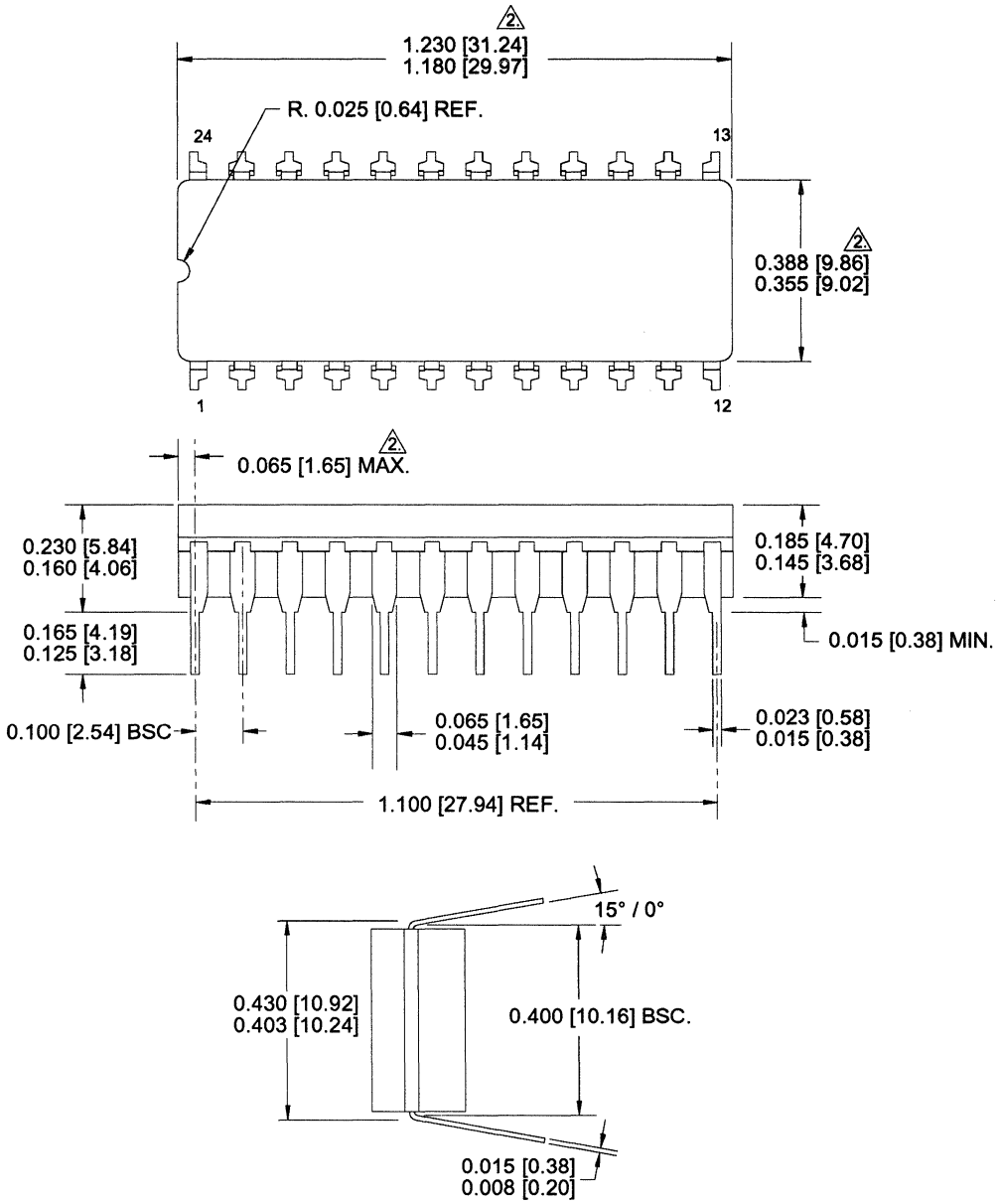
Table 5. Materials/Process Changes Requiring Qualification

20 LEAD CERDIP (D20-1)



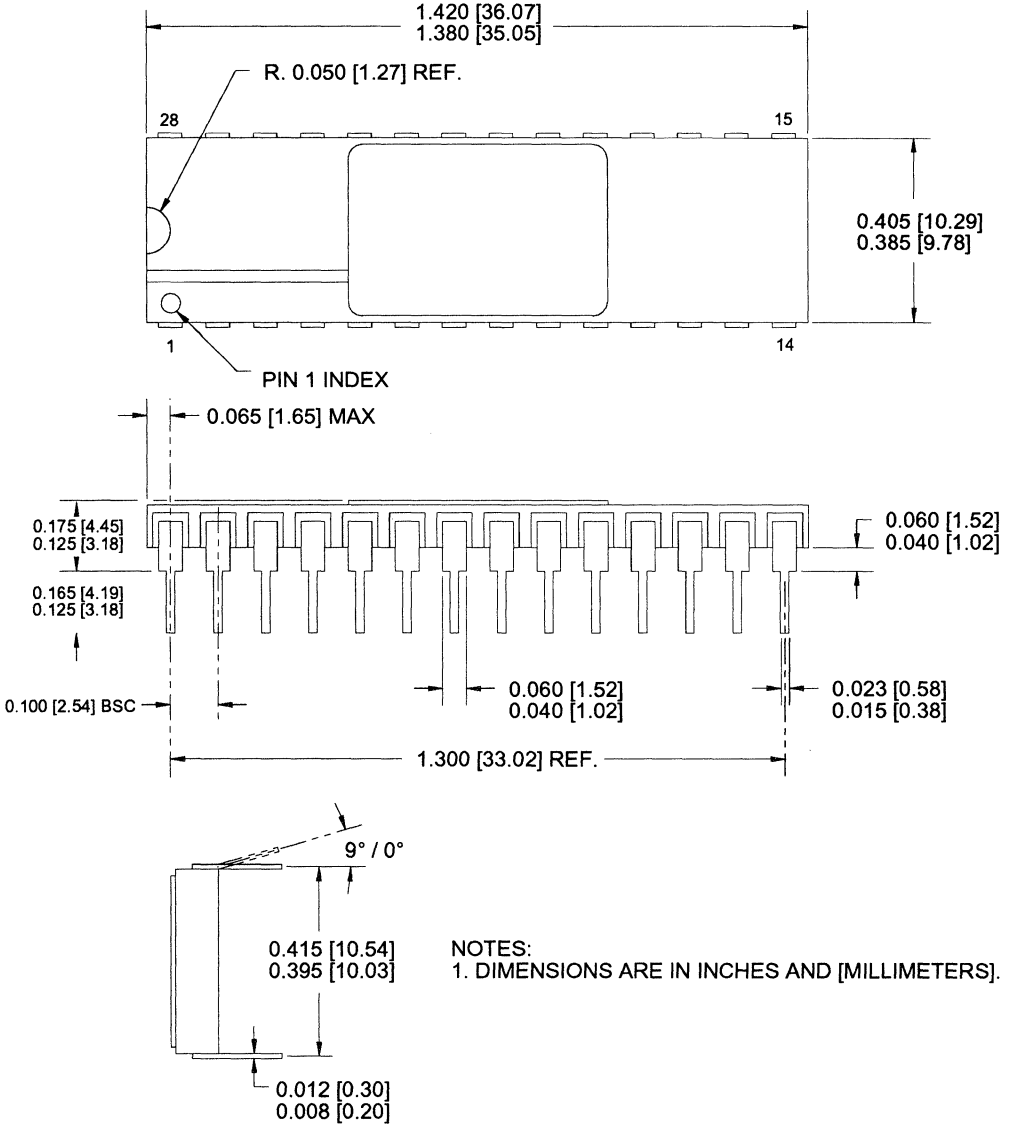
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

24 LEAD CERDIP (D24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

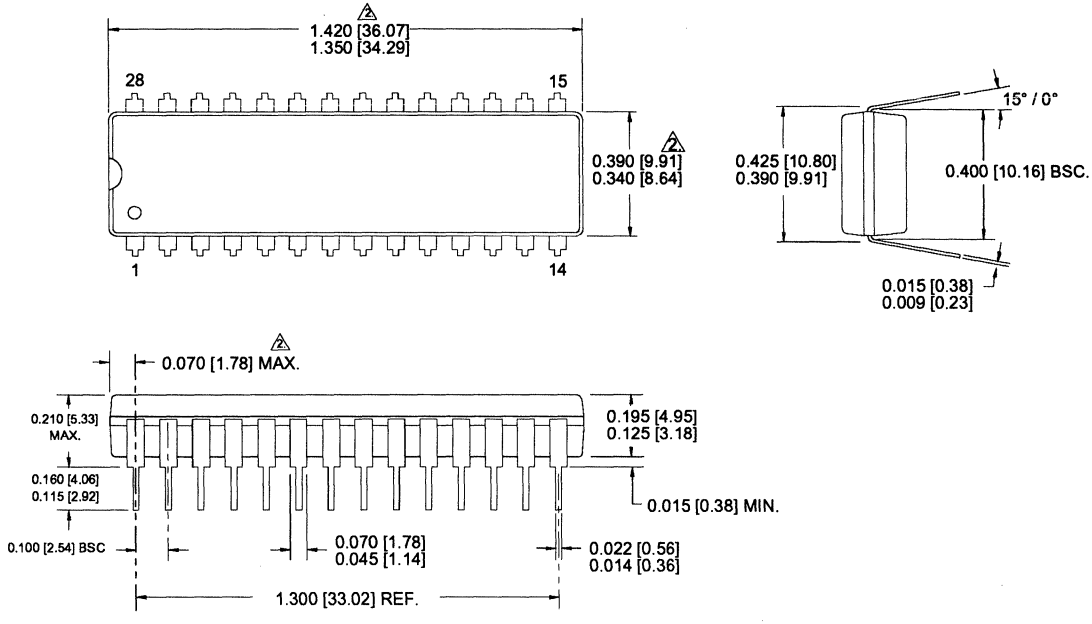
28 LEAD CERAMIC SIDEBRAZE (C28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

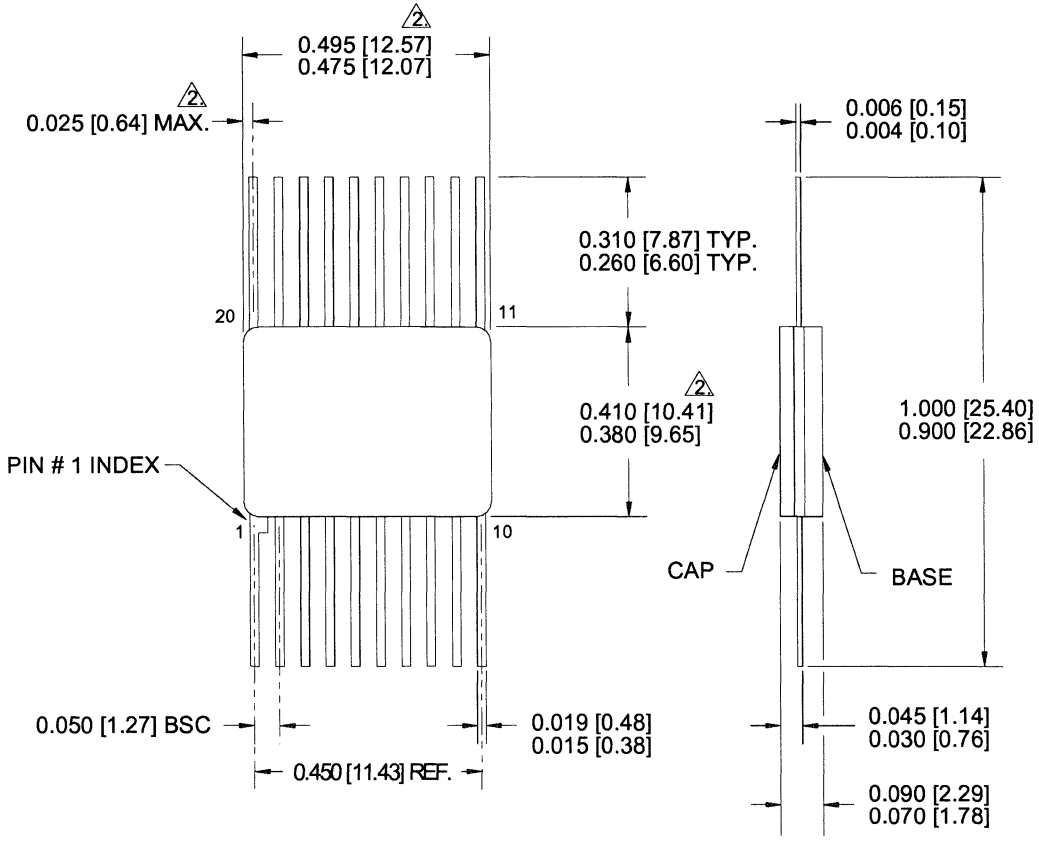
11

28 LEAD PLASTIC DIP (P28-1)



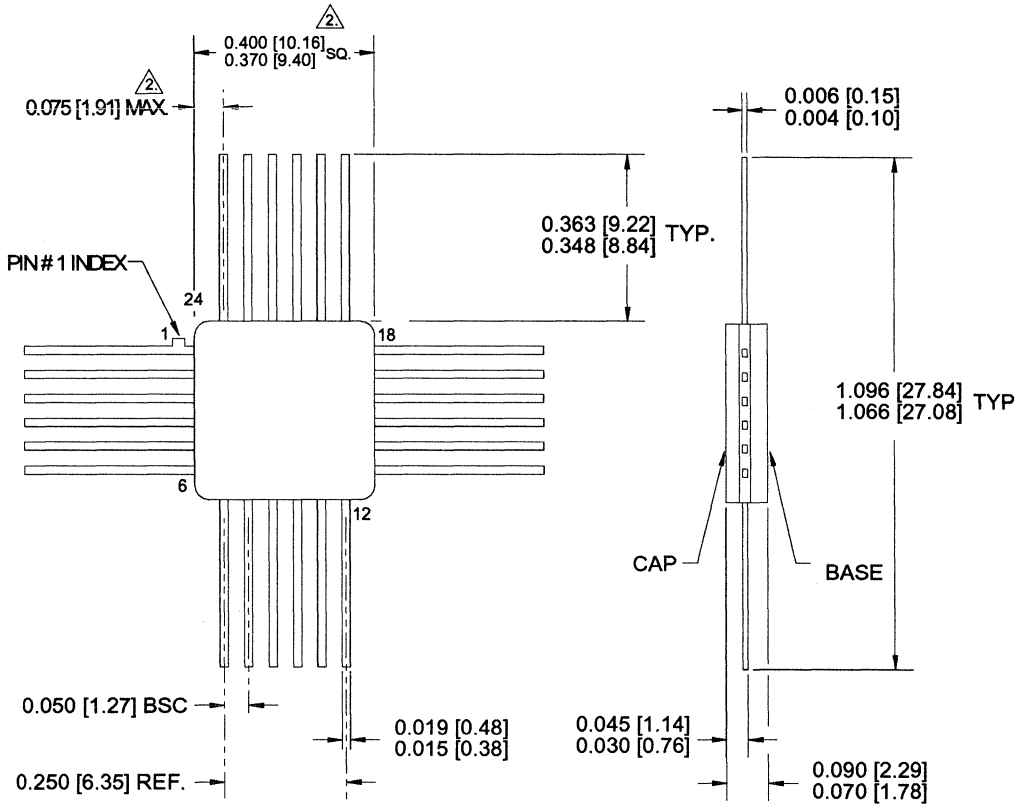
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS .010 [0.25] PER SIDE.

20 LEAD CERAMIC FLATPACK (F20-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

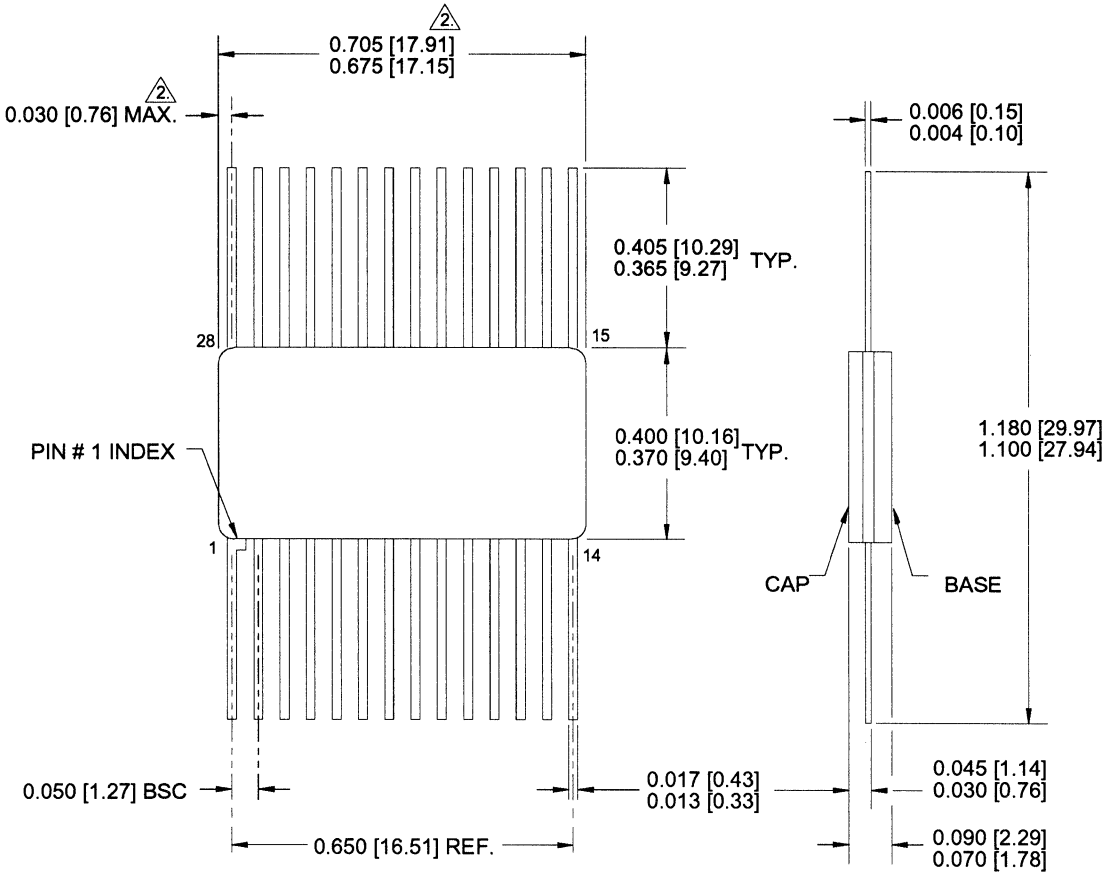
24 LEAD CERAMIC FLATPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

28 LEAD CERAMIC FLATPACK (F28-1)

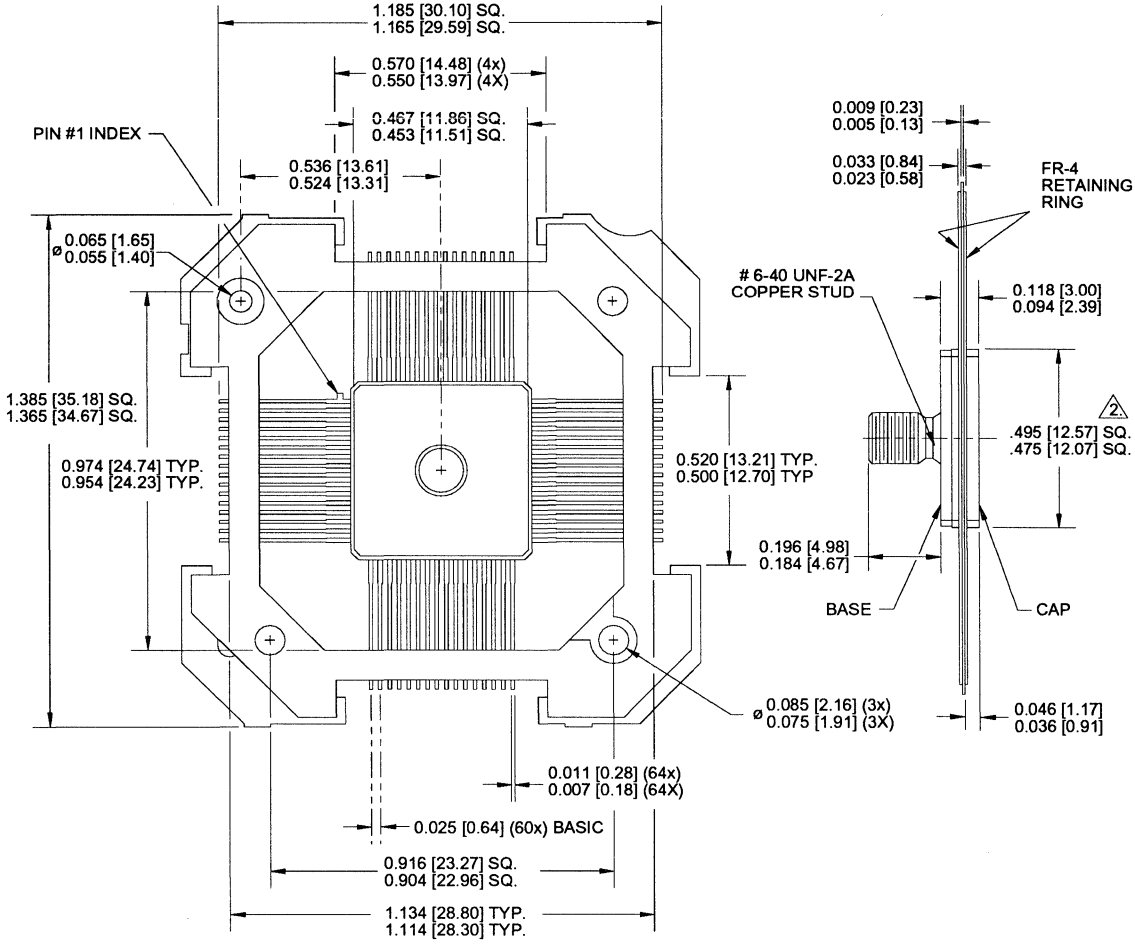


NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2 THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

11

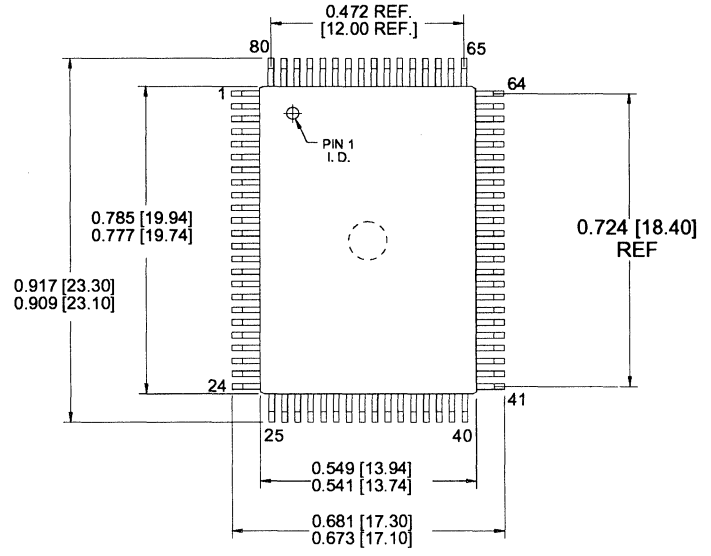
64 LEAD CERQUAD FLATPACK (E64-1)

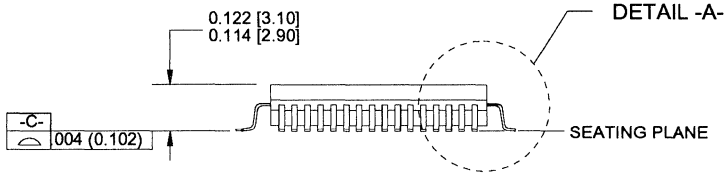


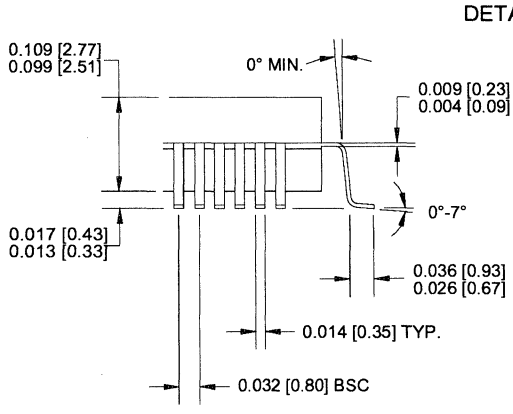
NOTES:
1. DIMENSIONS ARE IN INCHES[MILLIMETERS]

2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.

80 METAL QUAD FLATPACK (Q80-1)

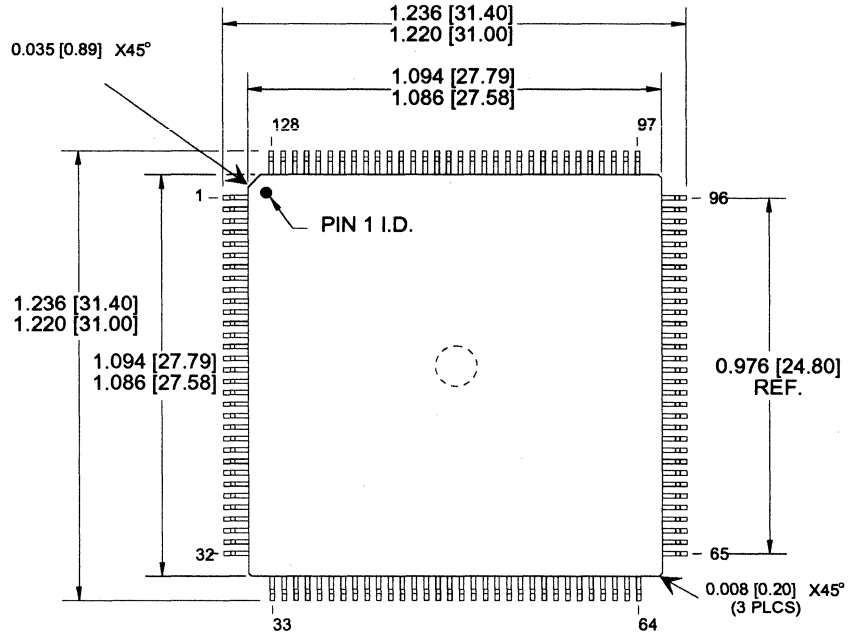




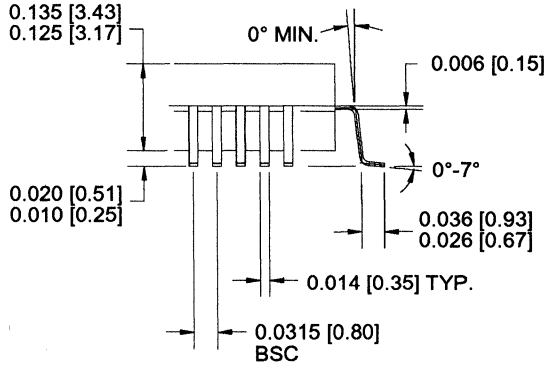


NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].
3. TOP VIEW, CAVITY DOWN

128 METAL QUAD FLATPACK (Q128-1)

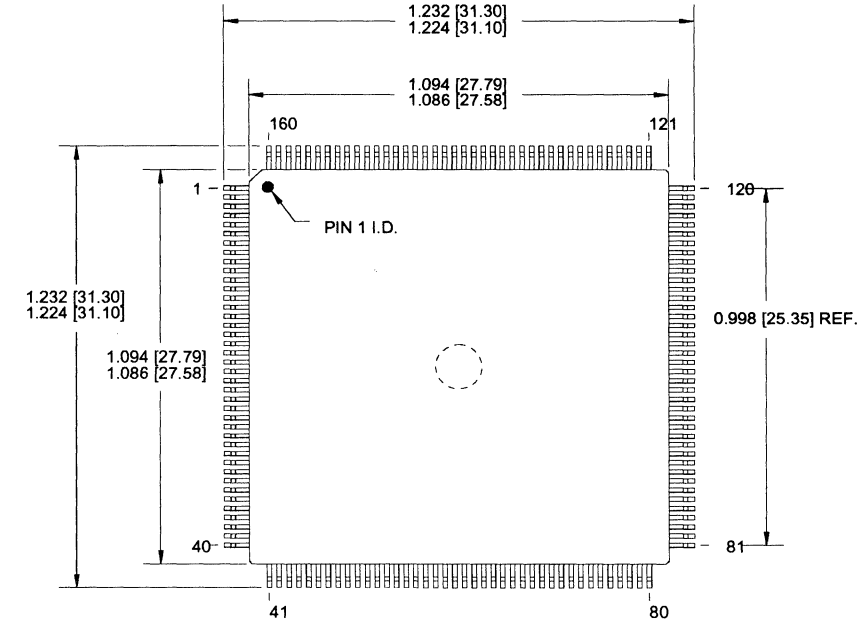


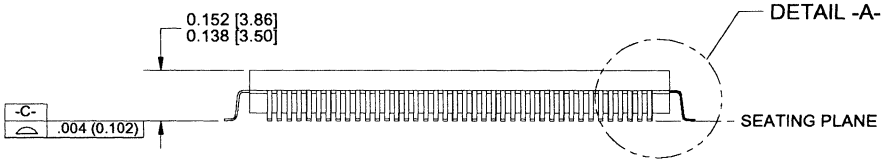
DETAIL -A-



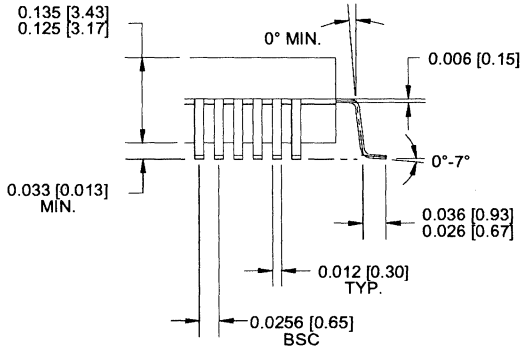
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS]
2. CONTROLLING DIMENSION: [MILLIMETERS].

160 METAL QUAD FLATPACK (Q160-1)





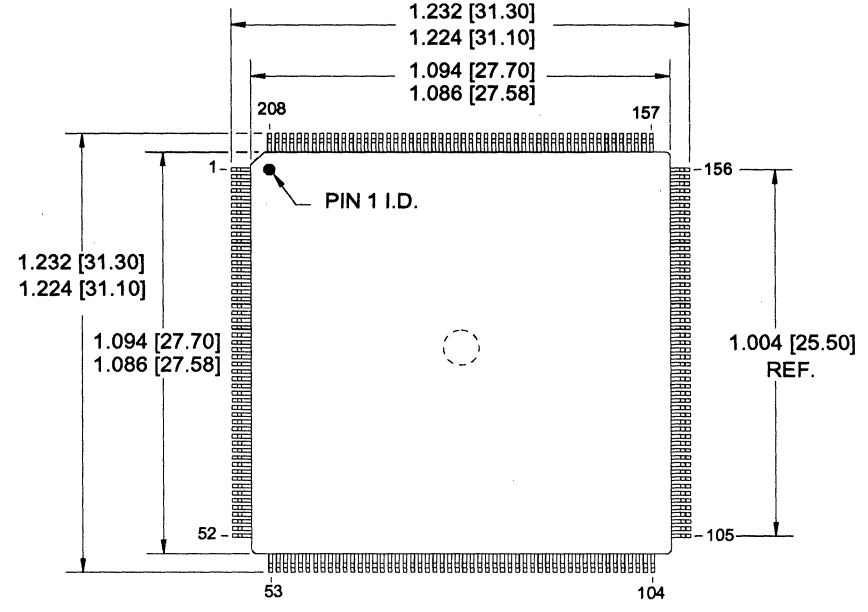
DETAIL -A-

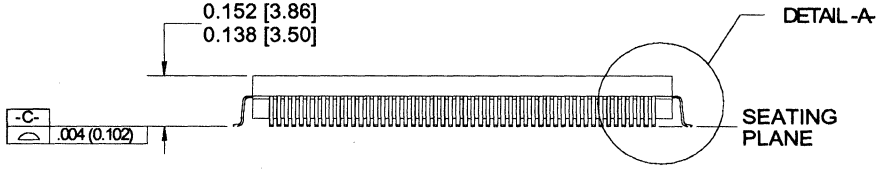


NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].

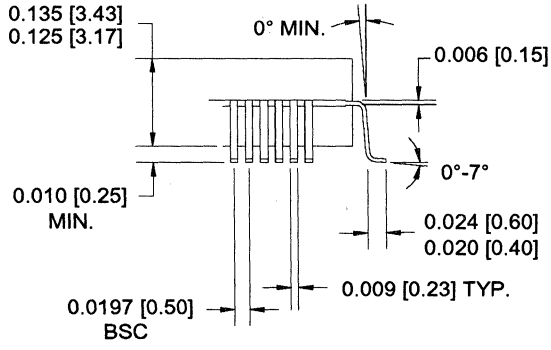
11

208 LEAD METAL QUAD FLATPACK (Q208-1)





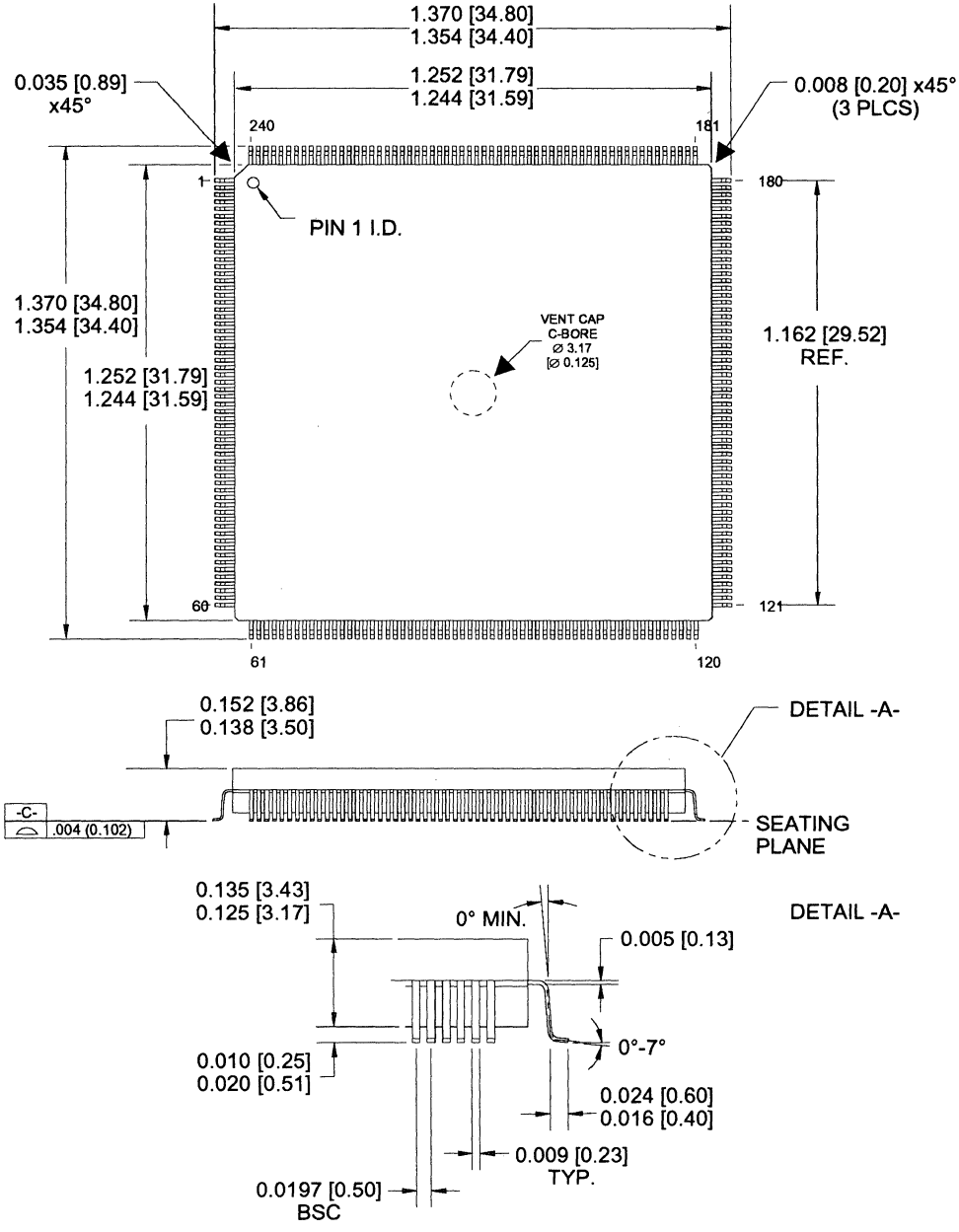
DETAIL -A-



NOTES:

1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].

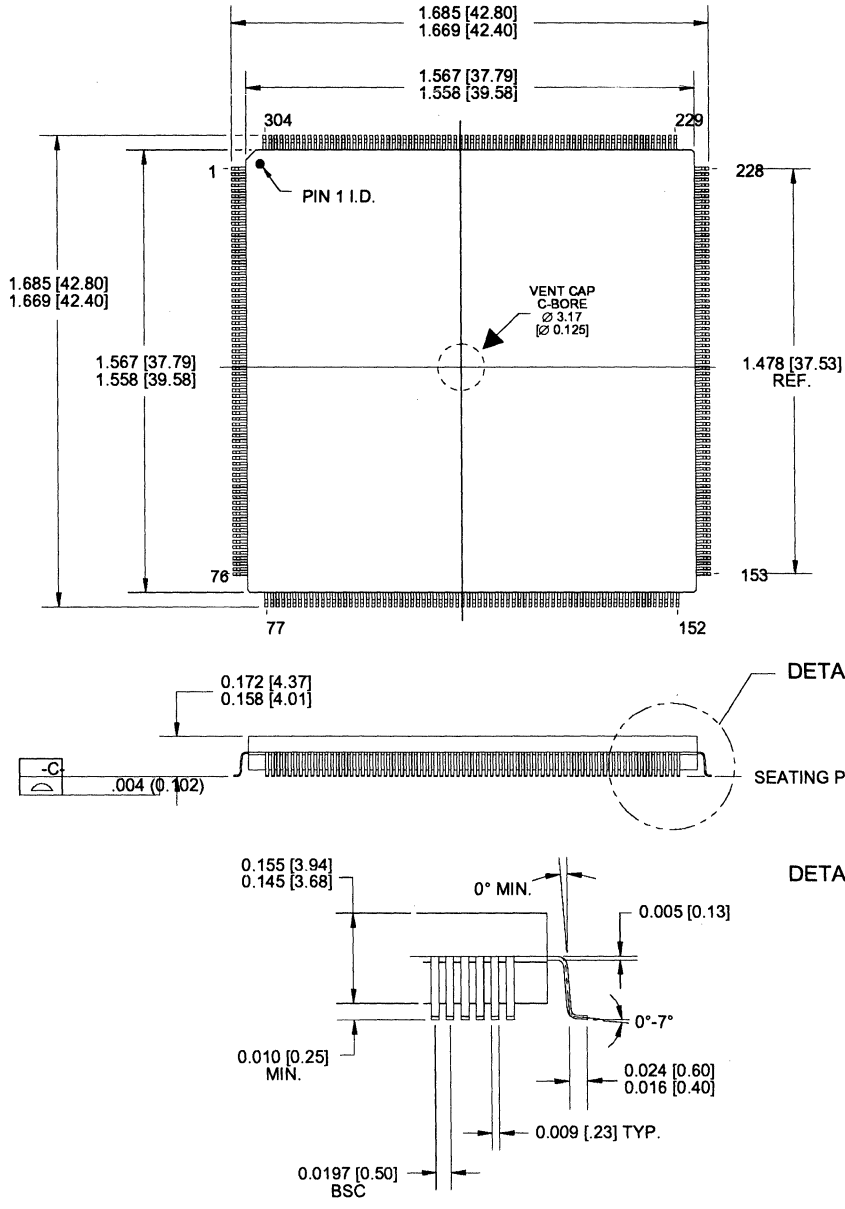
240 LEAD METAL QUAD FLATPACK (Q240-1)



NOTES:
1. CONTROLLING DIMENSION: [MILLIMETERS].
2. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

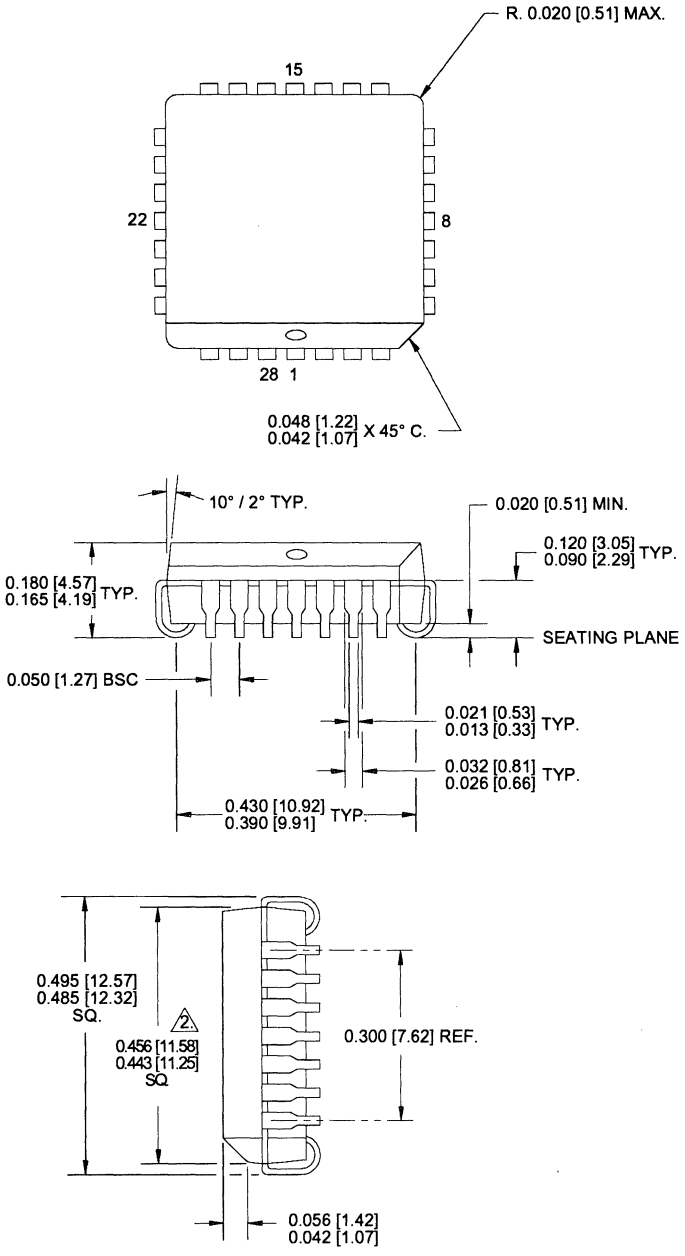
11

304 LEAD METAL QUAD FLATPACK (Q304-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].

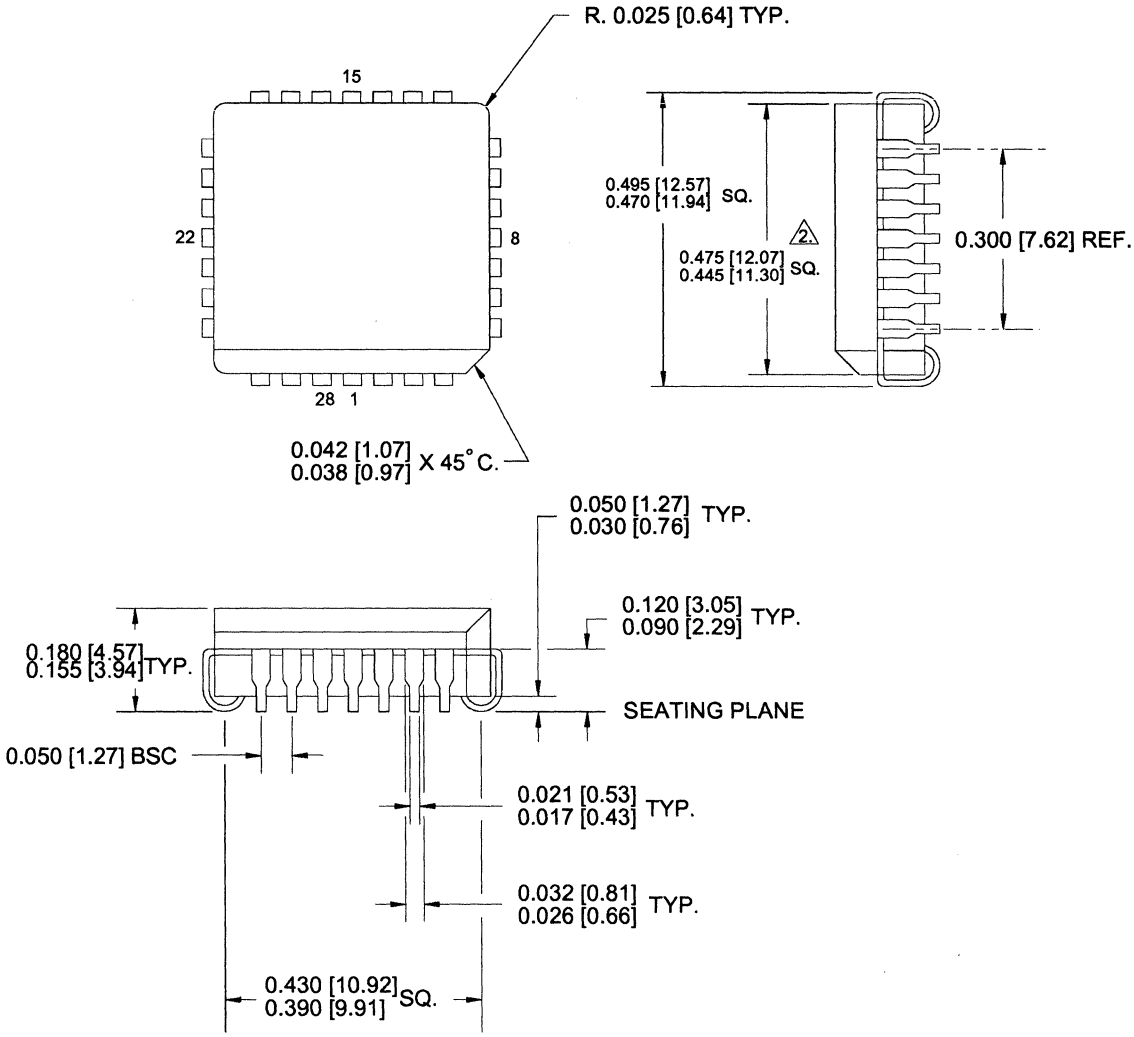
28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH PROTRUSION OF 0.010 [0.25] INCH MAX. PER SIDE.

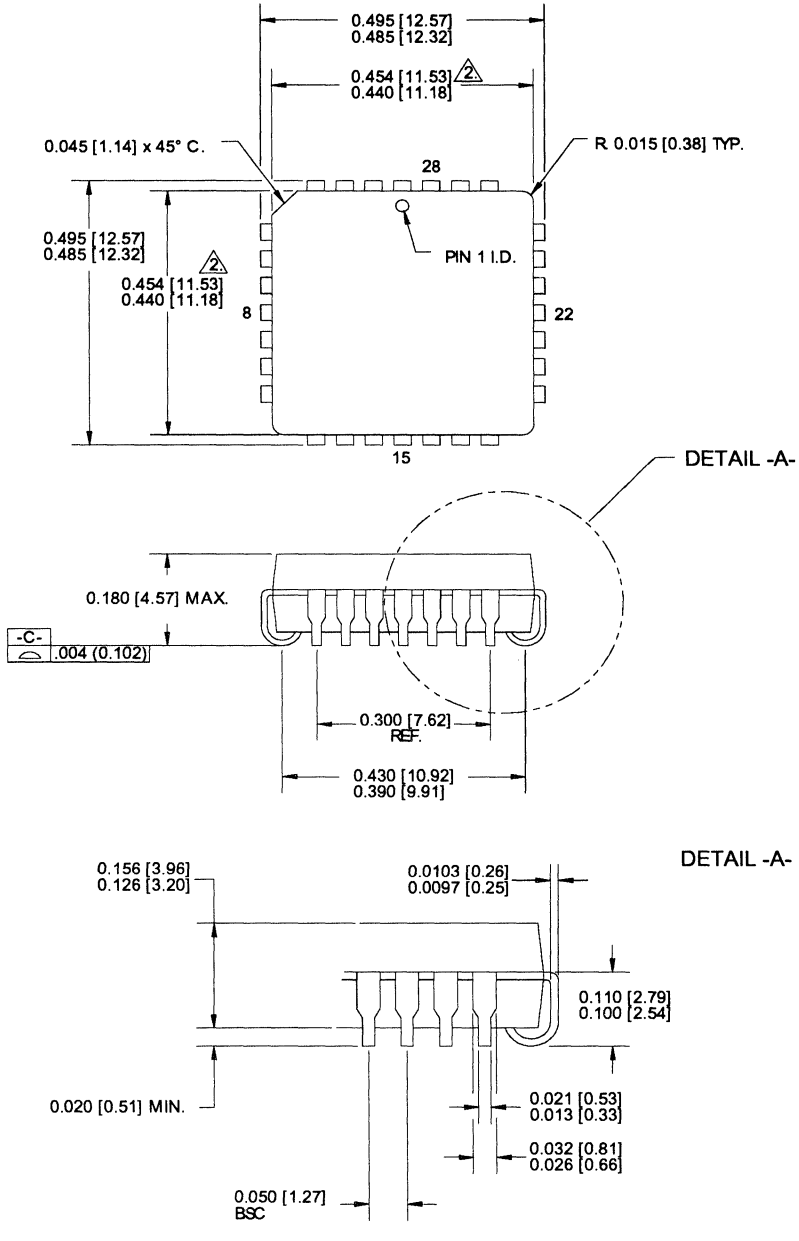
11

28 LEAD CERAMIC LEADED CHIP CARRIER (H28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION INCLUDES CAP TO BASE ALIGNMENT TOLERANCE.

28 LEAD METALLIC LEADED CHIP CARRIER (M28-1)

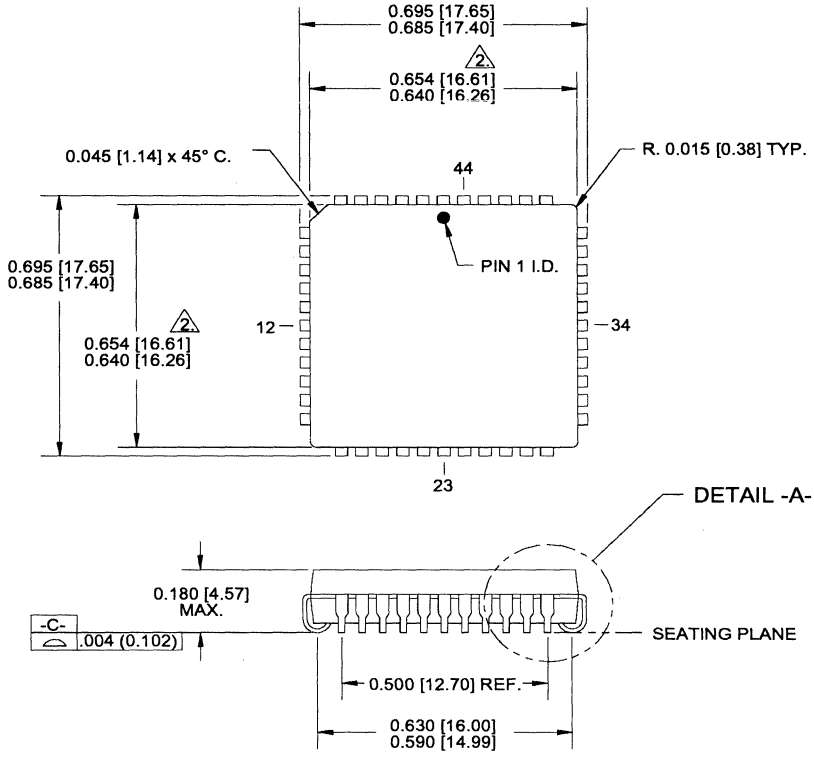


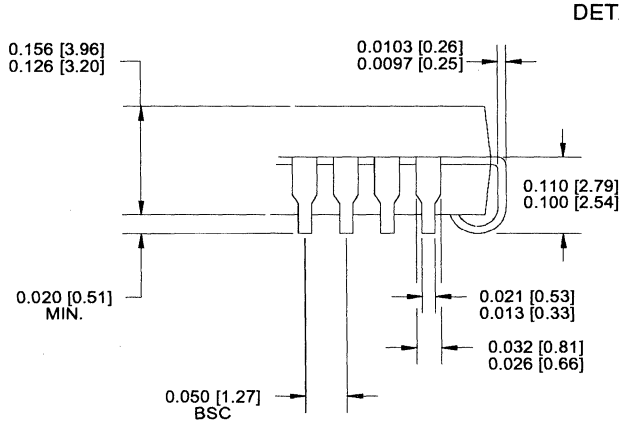
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2 THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS 0.010 [0.25] PER SIDE.

11

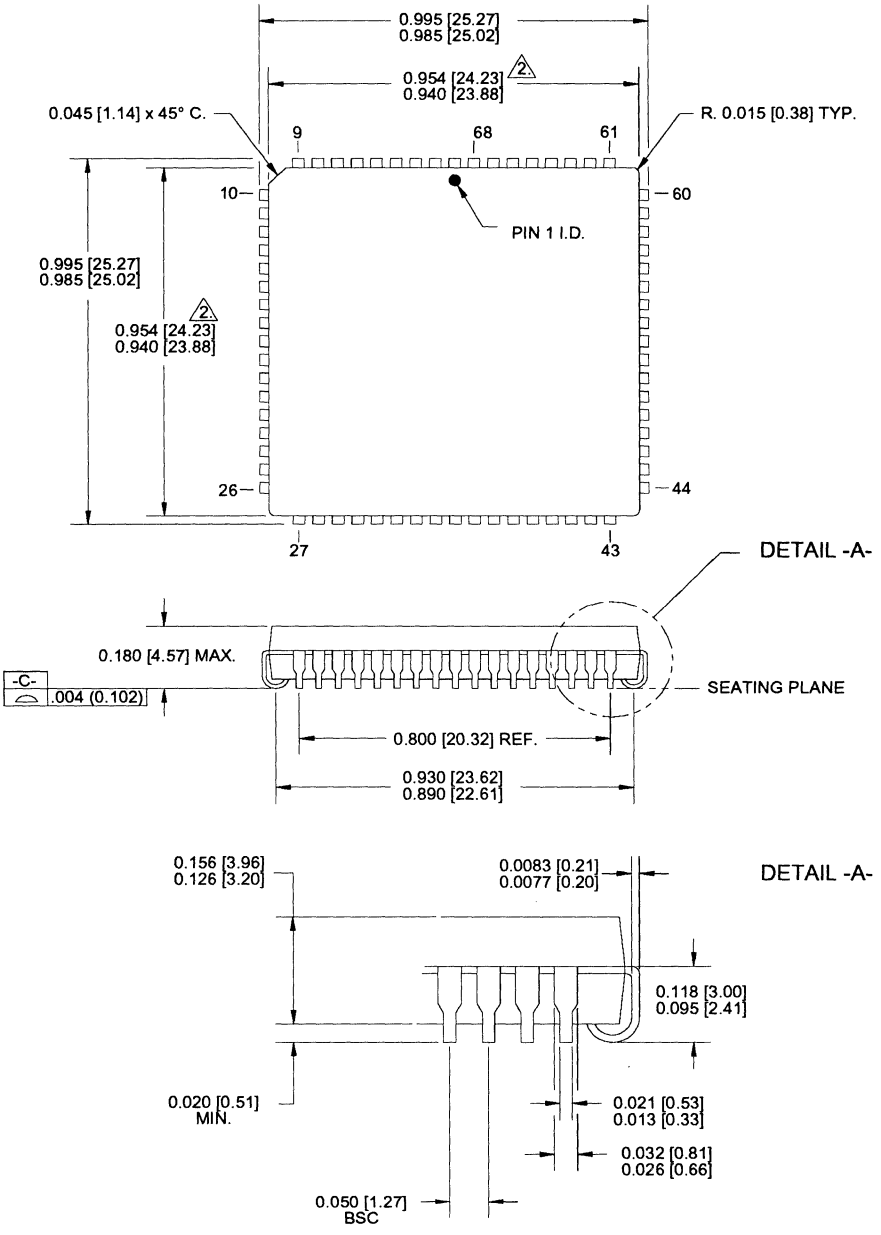
44 LEAD PLASTIC LEADED CHIP CARRIER (J44-1)





NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS 0.010 [0.25] PER SIDE.

68 LEAD PLASTIC LEADED CHIP CARRIER (J68-1)

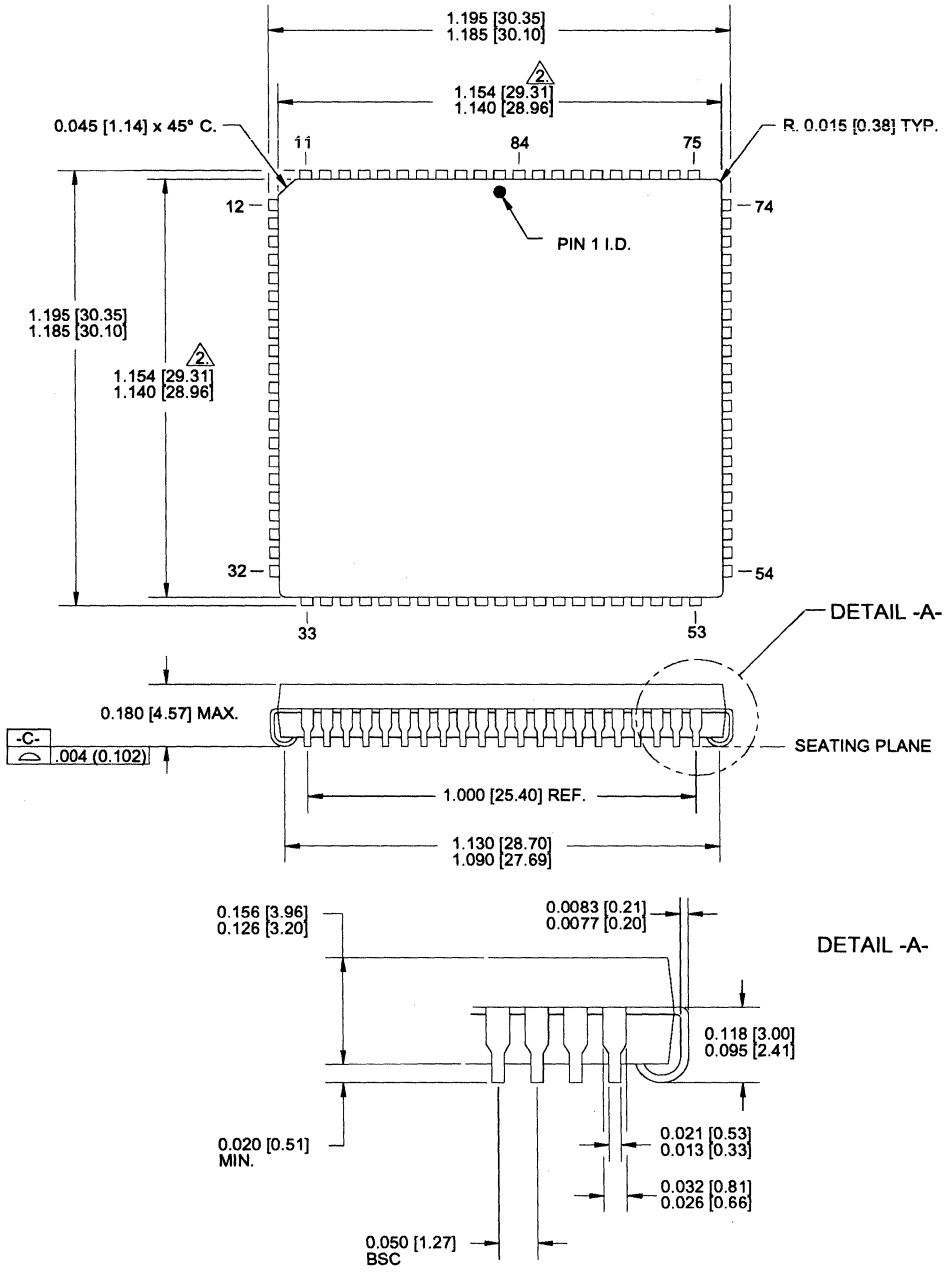


NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2 THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS .010 [0.25] PER SIDE.

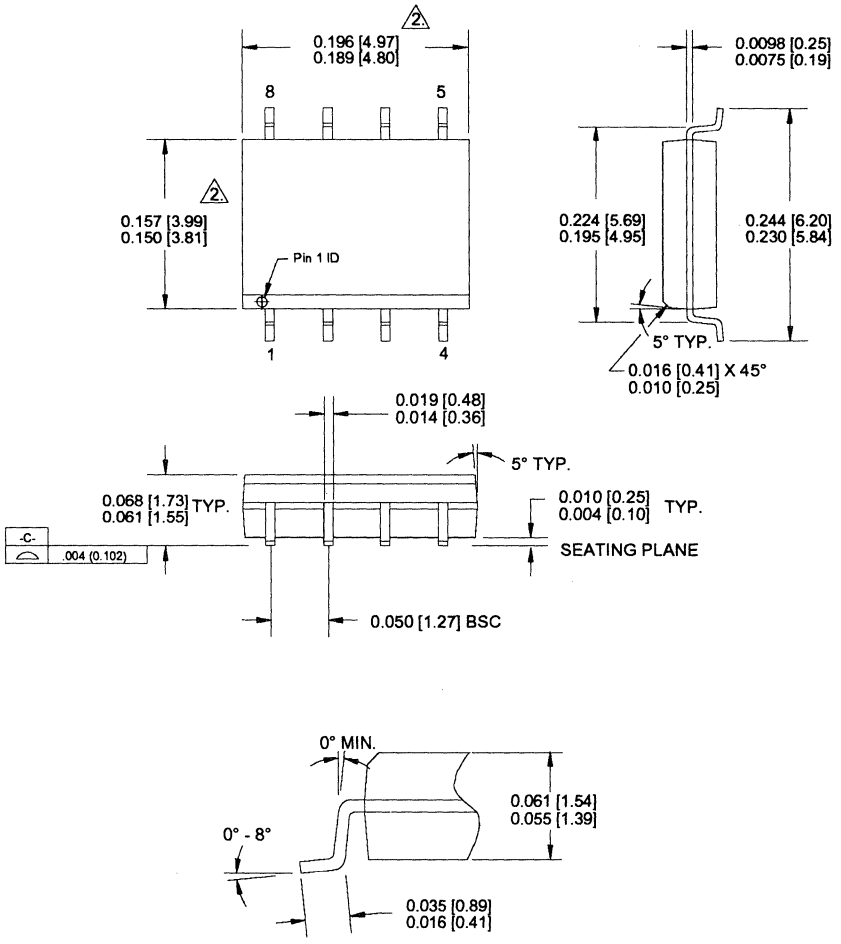
11

84 LEAD PLASTIC LEADED CHIP CARRIER (J84-1)



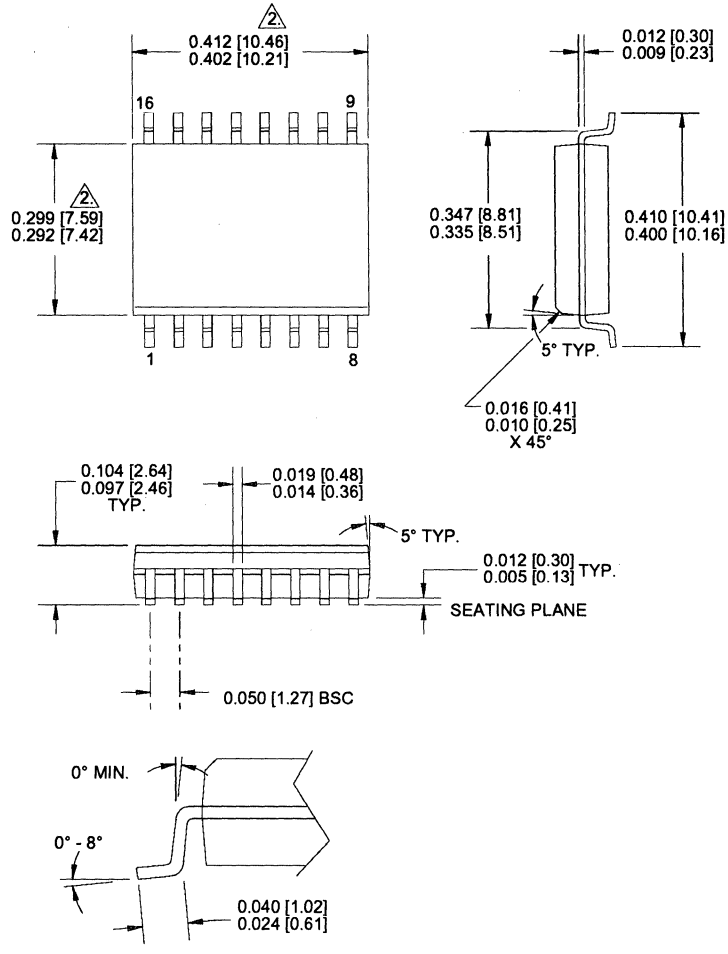
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH

8 LEAD PLASTIC SOIC (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS 0.010 [0.25] PER SIDE.

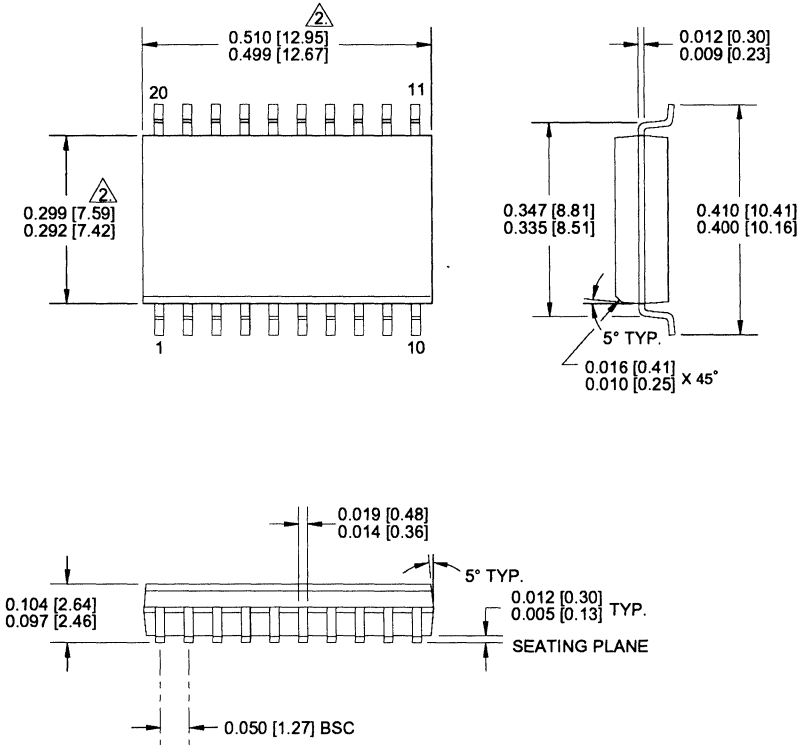
16 LEAD PLASTIC SOIC (Z16-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2 THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS 0.010 [0.25] PER SIDE.

20 LEAD PLASTIC SOIC (Z20-1)

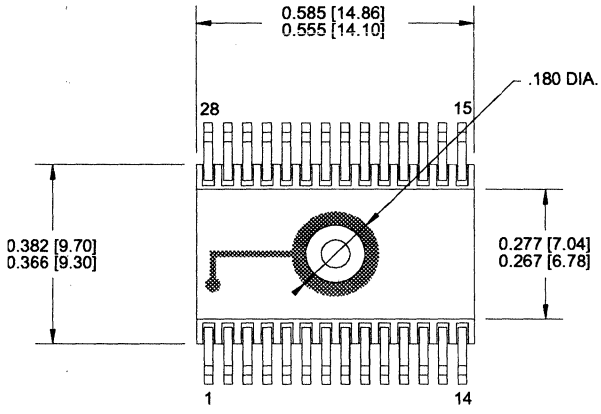


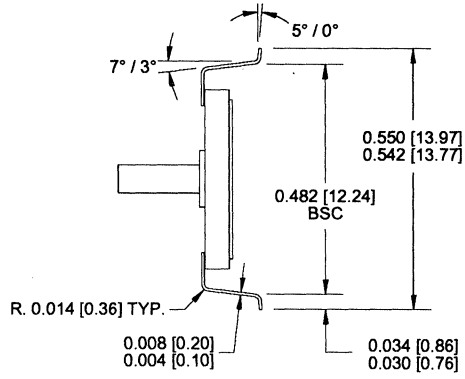
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

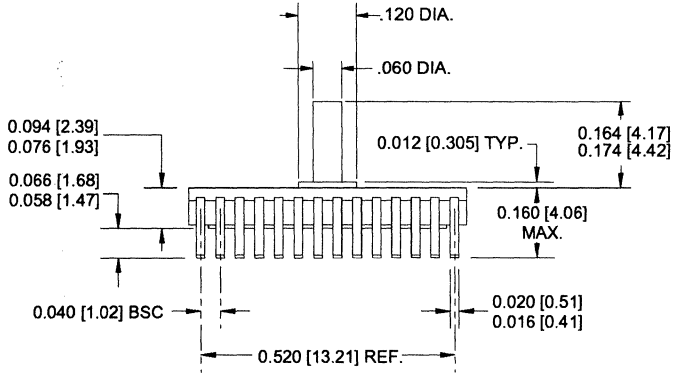
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS 0.010 [0.25] PER SIDE.

11

28 LEAD CERAMIC SOIC WITH HEAT SINK STUD (S28-1)

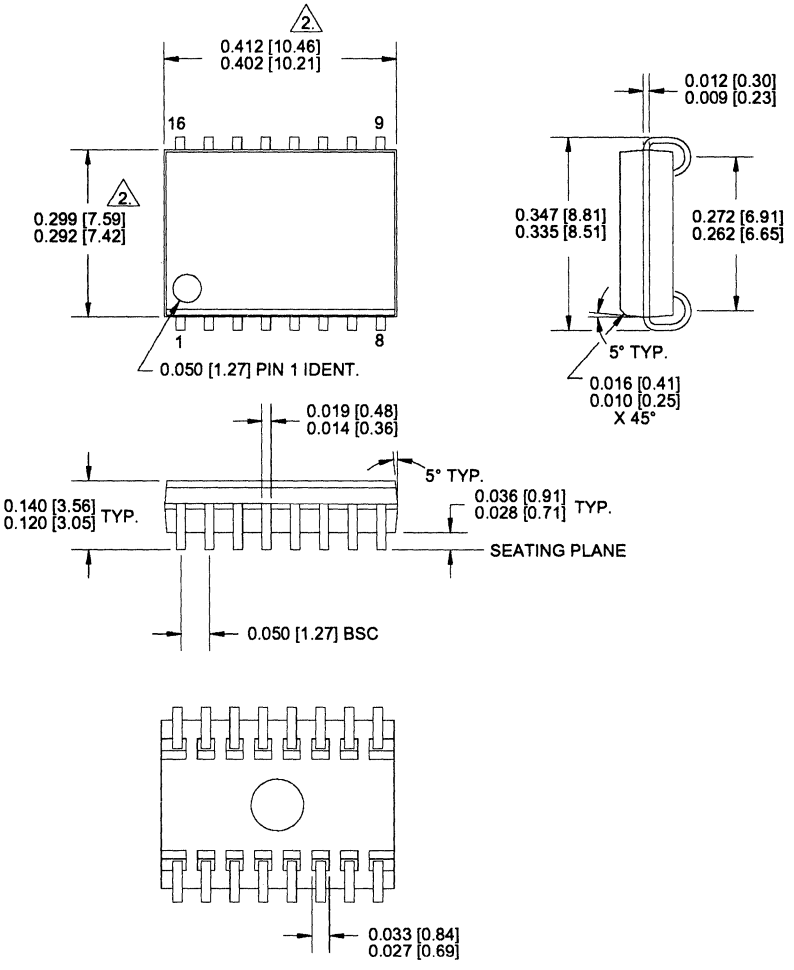






NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. HEATSINK IS ELECTRICALLY INSULATED FROM THE INTEGRATED CIRCUIT.

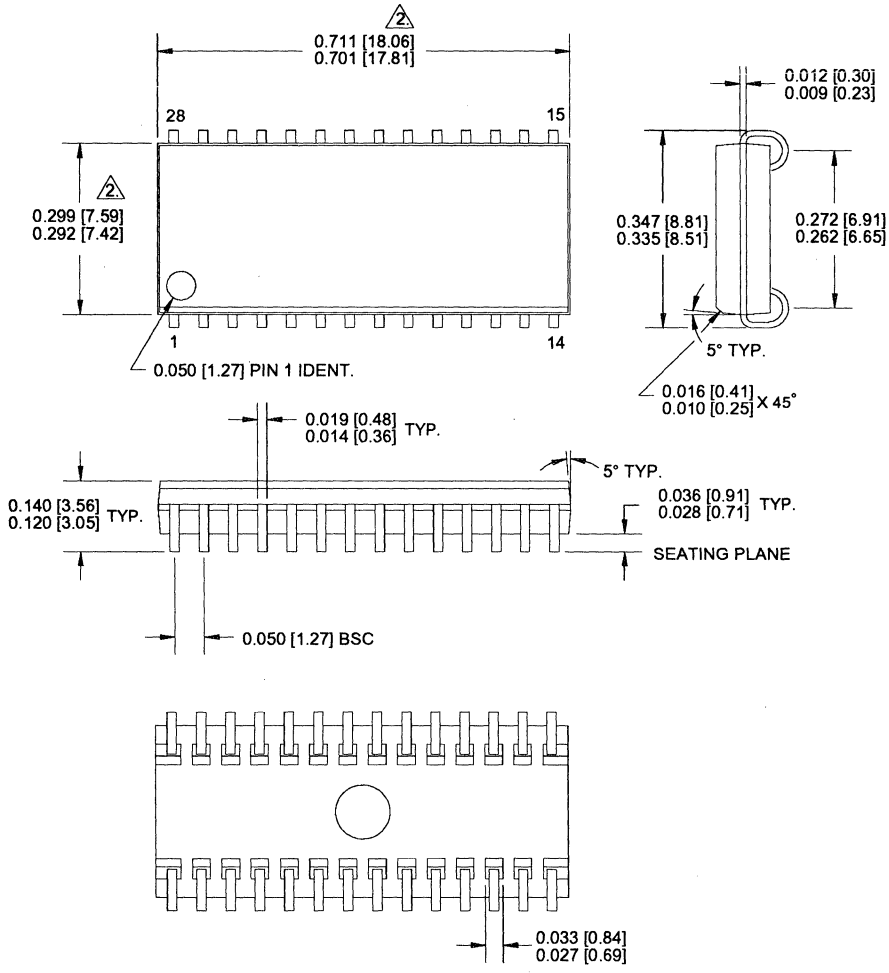
16 LEAD PLASTIC SOJ (Y16-1)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS .010 [0.25] PER SIDE.

11

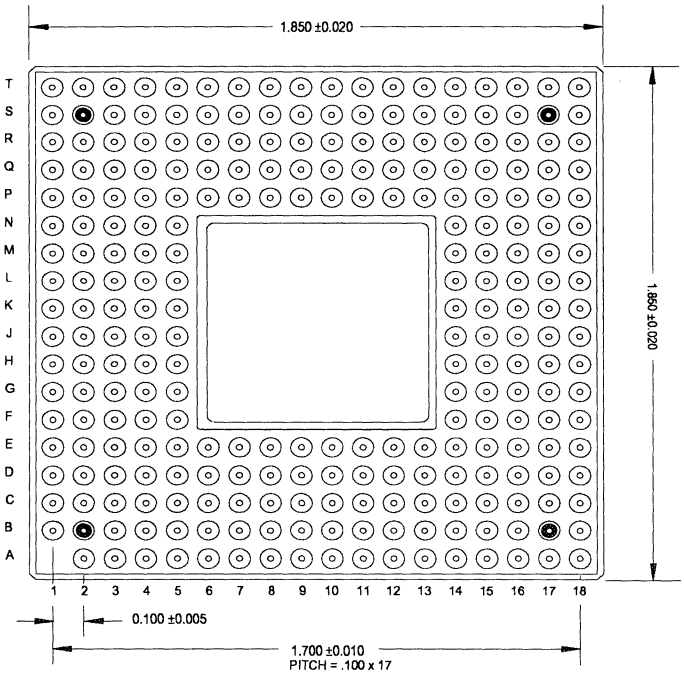
28 LEAD PLASTIC SOJ (Y28-1)

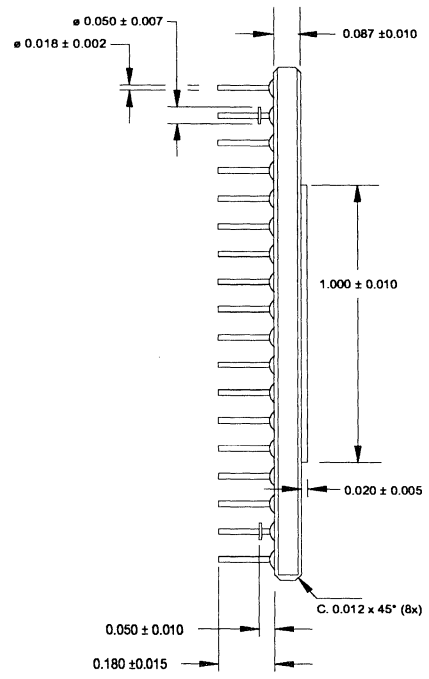


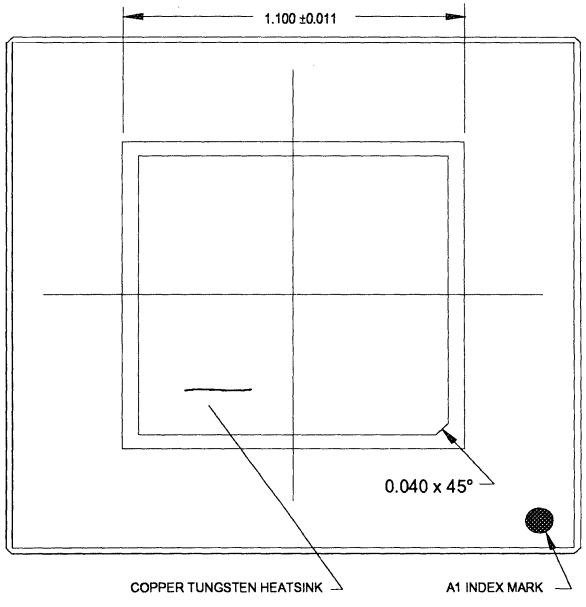
NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS .010 [0.25] PER SIDE.

259 LEAD CERAMIC PIN GRID ARRAY (G259-1)



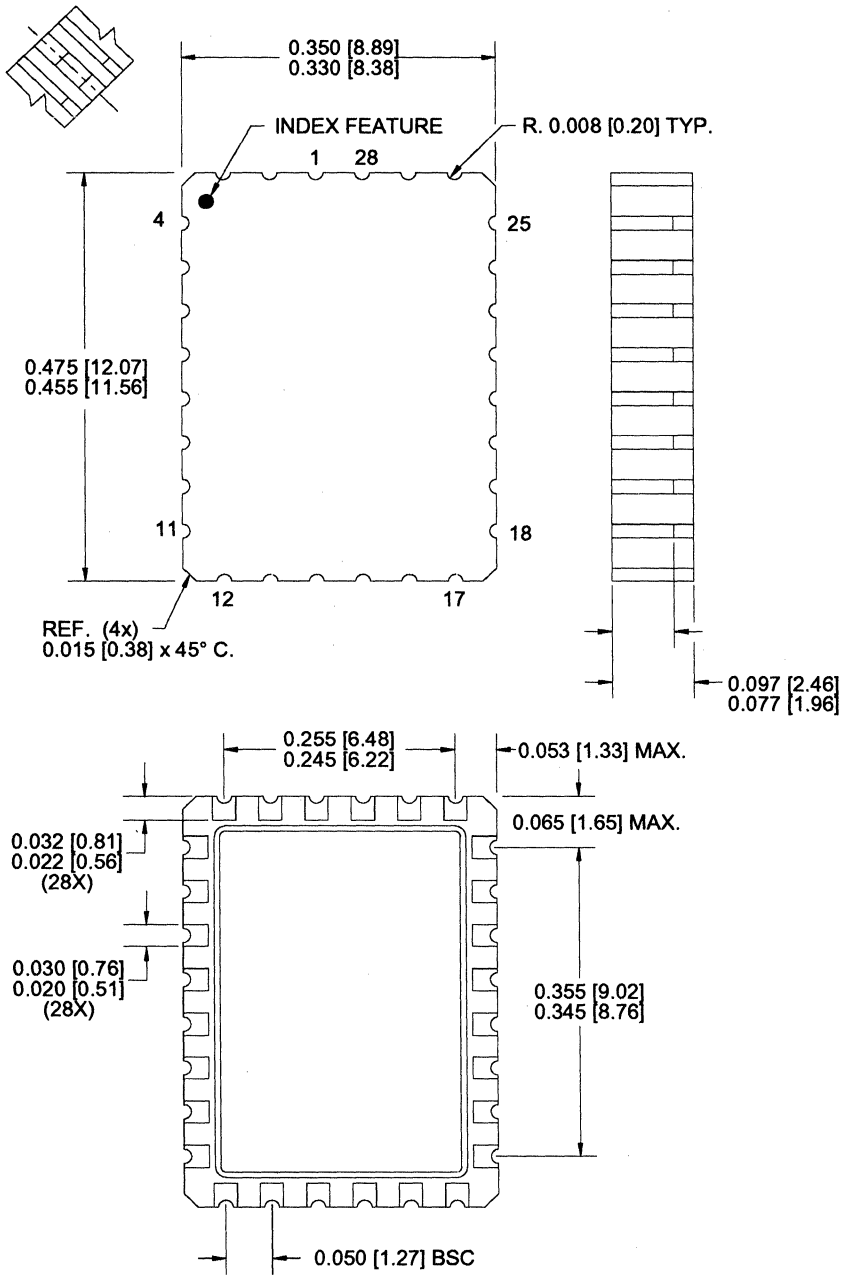




NOTES:
1.0 Heat sink and pins, and package lid are gold plated.

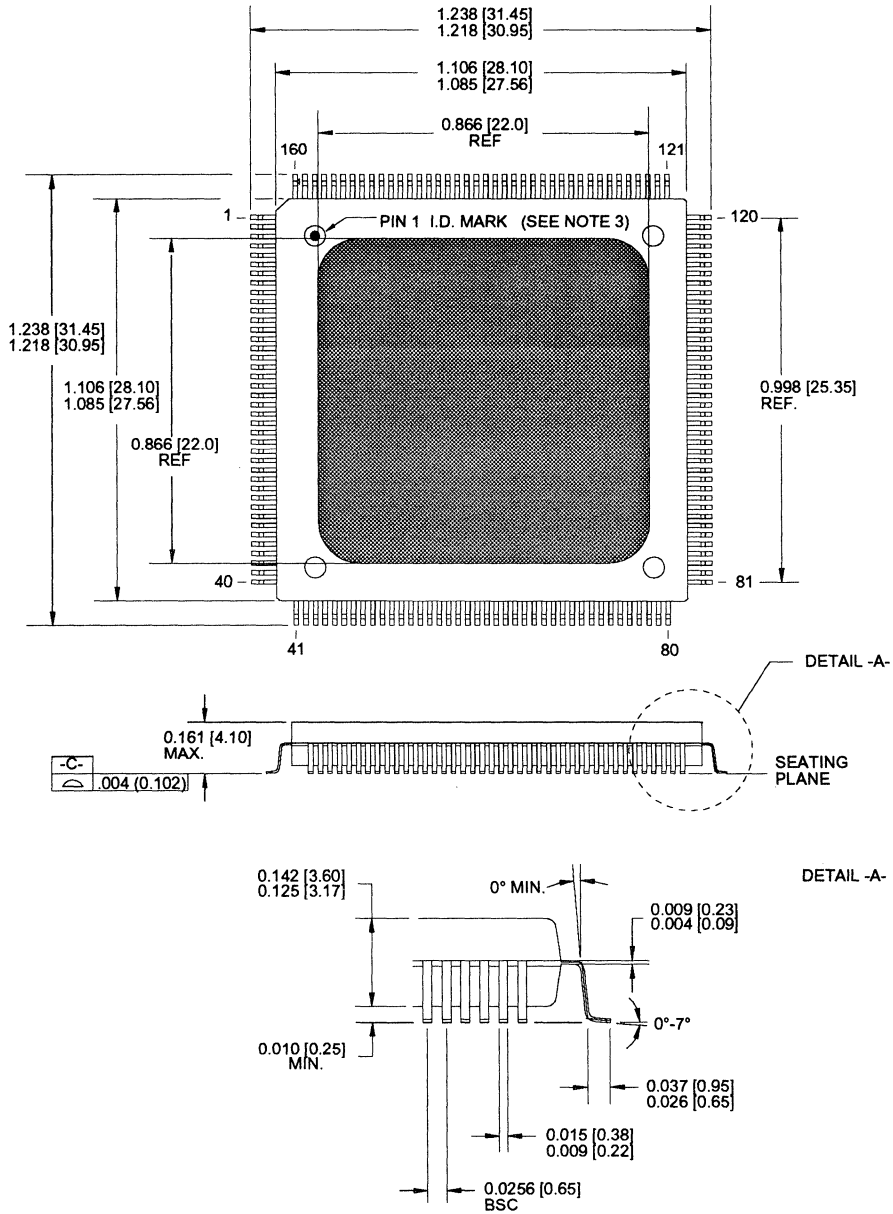
11

28 LEADLESS CHIP CARRIER (L28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES [MILLIMETERS].

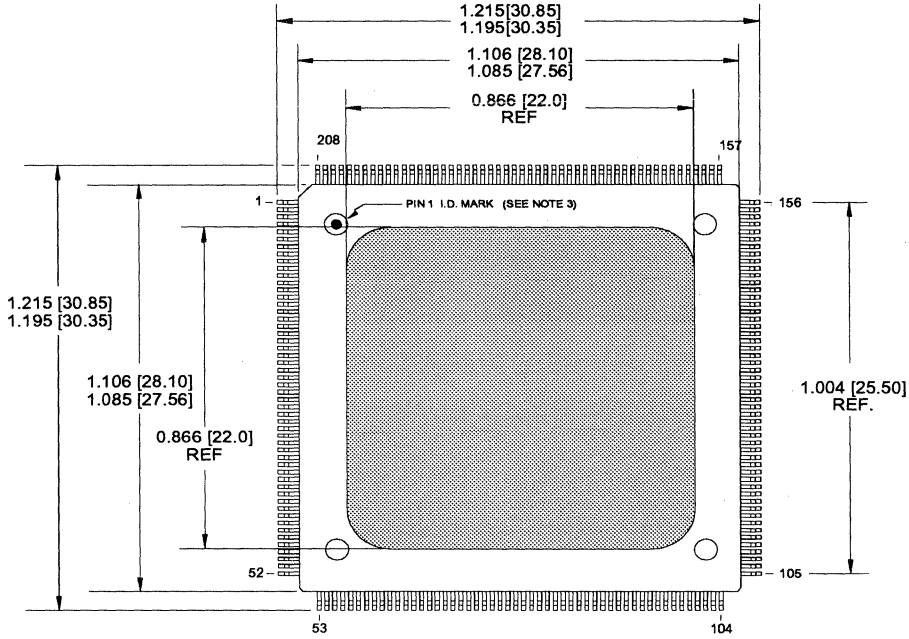
160 PLASTIC QUAD FLATPACK WITH HEATSPREADER (R160-1)



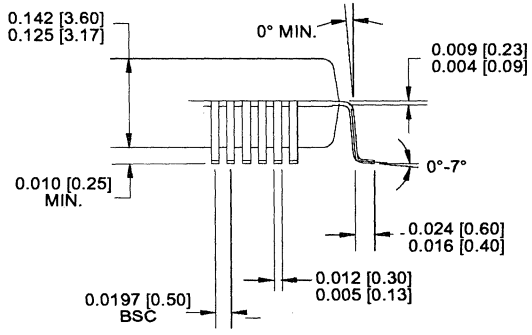
NOTES:
1. DIMENSIONS ARE IN INCHES ND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].
3. THE PIN 1 ID MARK IS ROUNDED AT THE BOTTOM.
   THE REMAINING MARKS ARE FLAT AT THE BOTTOM.

11

208 PLASTIC QUAD FLATPACK WITH HEATSPREADER (R208-1)

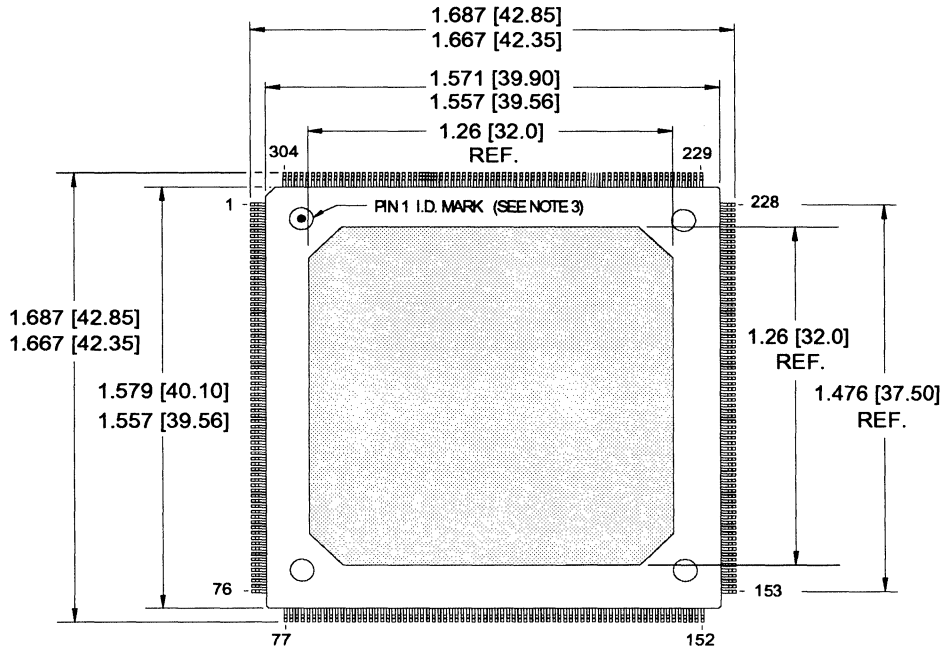


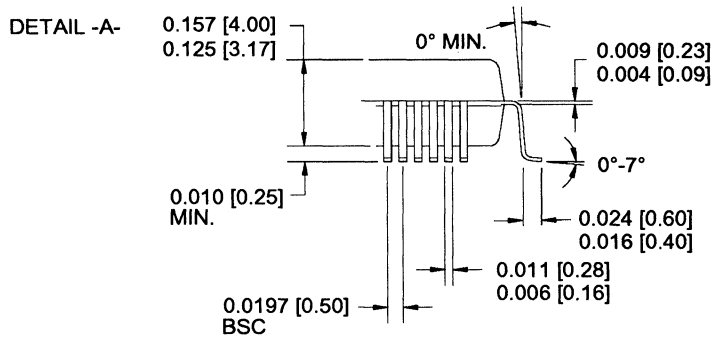
DETAIL -A-



NOTES:
1. CONTROLLING DIMENSION: [MILLIMETERS].
2. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
3. THE PIN 1 ID MARK IS ROUNDED AT THE BOTTOM.
   THE REMAINING MARKS ARE FLAT AT THE BOTTOM.

304 PLASTIC QUAD FLATPACK WITH HEATSPREADER (R304-1)





NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].
3. THE PIN 1 ID MARK IS ROUNDED AT THE BOTTOM.
   THE REMAINING MARKS ARE FLAT AT THE BOTTOM.

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