DATEL®
INNOVATION and EXCELLENCE

PC-430

Very High Speed ISA A/D-DSP Coprocessor Board

FEATURES

- **Up to 10 MHz A/D sample rate**
- **Choice of 12, 14, or 16-bit A/D resolution**
- **Up to 8 Mb dual-ported RAM**
- **Analog pretrigger ring buffer**
- **8k x 32 expansion RAM**
- **Programmable interrupt to PC/AT host**
- **2-16 Channel simultaneous sampling eliminates phase skew**
- **On-board 320C30 40 MHz digital signal processor**
- **On-board DSP library - FFT's, filters, matrix math, floating point, etc.**
- **Fast, simple, powerful command executive. No local programming required.**
- **Windows® compatible**

NEW
Now with LabVIEW® VI's

Advanced performance from the PC-430's on-board Digital Signal Processor (DSP) offers a broad range of high-speed waveform analysis and recording applications. The PC-430 will acquire up to sixteen analog input channels, digitize and store them in local memory while DSP math processing and data transfer are done concurrently. The system is intended for preprocessing "seamless" A/D data streams to mass storage.

The PC-430 is ideal for non-stop, continuous Fast Fourier Transform (FFT) processing, communications receiver signal collection to disk, or simultaneous graphics display of spectral data. Application areas include signal recovery from noisy channels, harmonic distortion analyzers, and vibration/ resonance filtering systems. For use with ultrasonic, sonar, or acoustic signals, the interrupt-driven, simultaneous block transfers of data ensure no information loss. Other uses include high-speed mapping and imaging, satellite channels, astrophysics, seismology, biomedical signals, array processing, control systems, simulators, engine analyzers, aerodynamics, and vehicle systems.

Several different "pluggable" analog options offer up to 16 input channels in single-ended or differential configurations, multiple input ranges, sampling rates to 10 MHz, 12/14/16-bit A/D resolutions, and various simultaneous sampling configurations (1 A/D per channel) up to 16 channels. The simultaneous feature is intended for parallel sampling applications that cannot tolerate phase skew introduced by the A/D system.

A/D triggering uses a programmable timer-counter section which controls the interval between A/D conversions and the interval between multi-sample A/D scans. The number of samples can be counted for repeating array sampling. The timer-counter uses an on-board crystal oscillator or an

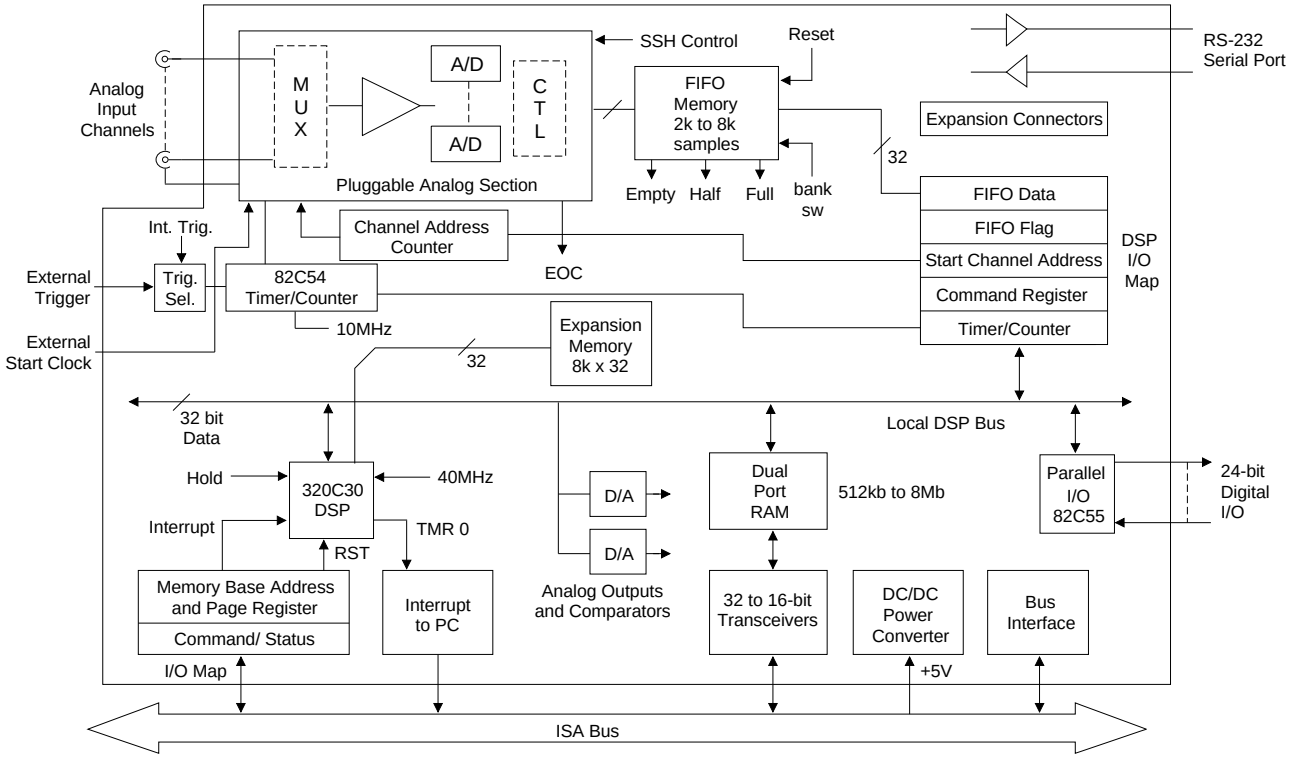

Figure 1. Functional Block Diagram

external timebase for precision phase-tracking. The digital output of the A/D passes directly to a first-in, first-out (FIFO) memory. The FIFO acts to decouple the precision timing of the A/D section with the block transfers governed by the DSP. Additional internal DSP timers are also used.

A/D FIFO data may be sent to dual port random access memory (DPR) shared with the host PC/AT bus. The DPR is organized as 128k by 32 bits up to 2M x 32. Typically, a swapped dual buffer method is used so that samples are not lost during other processing. Local hardware registers control all A/D, FIFO, and trigger activity.

Single cycle fetch and execution, parallel instructions, zero-overhead of looping instructions, software variable wait states, block repeat and a 64-word internal instruction cache memory are some of the advanced high speed features of the Texas Instrument 320C30 DSP. The DSP uses 32-bit local data paths for very high speed. Data passed to the host PC/AT bus uses 32-to-16 bit transceivers to the DPR. Simultaneous access attempts to the DPR by both the PC/AT host and the DSP are resolved by high speed arbitration logic. The DSP also has a separate 8k by 32-bit local expansion memory for the stack or temporary data. The architecture of the DSP allows simultaneous processing of two tables from two sections of memory.

The PC-430 appears as both I/O and memory addresses to the host PC/AT. At power up, the PC-430 is disconnected from host memory and must be enabled through the I/O registers. The DPR may be addressed up to 16 Mb.

After loading in the Executive from disk to the DPR, the DSP is transitioned from reset to run using an I/O control bit. The board may be reset at any time using this technique. The comprehensive Executive software package offers fast A/D sample collection and DSP math without writing any local programs. A simple, powerful, high speed command list is used to access the local DSP library.

Host PC to PC-430 Interface

The DPR can be accessed from the PC through two user-selectable methods, both of which map the DPR into the PC's memory. The first method locates a movable 1 MB window of DPR into the PC's extended memory above the 1 MB address. The host PC must have at least 1 MB of free extended memory below the PC's 16 MB address. Since the host PC memory is usually contiguous, this means the PC cannot have more than 15 MB of memory using this first method. Also, the CPU must be in protected mode to access this PC-430 extended memory. PC-430 software uses XMS drivers for this purpose.

The second method is new to the enhanced PC-430. This method maps a 64 kB DPR relocatable window into the PC's memory anywhere below the 16 MB address. Usually in this "paged" mode, the 64 kB block will be located below 1 MB where the CPU can access it in real mode. DPR blocks longer than 64 kB are accessed by a sliding window technique controlled by an I/O mapped paging register. Either access method works with DOS or Windows and both have speed and software trade-offs.

Memory Organization

At power up, the entire PC-430 DSP memory is empty (there is no local non-volatile memory). All executable code is downloaded from the host PC disk into the PC-430's Dual Port RAM (DPR). Typically, this download is from a TI COFF object file. The host PC does not require any extended memory to be installed for the PC-430 but any existing PC extended memory may be used to collect PC-430 data blocks.

PC-430 SOFTWARE

The following are some methods to control the PC-430:

- Use the PC-430 DATEL Executive software
- Modify the Executive by adding your own code.
- Develop your application from scratch using the TI compiler.
- PC-430LV "bridge" drivers to National Instruments LabVIEW.

PC-430EXEC - Executive, Commander, and Scheduler

DATEL's Executive software offers an easy way to control the PC-430 which retains the full power of the DSP. The Executive consists of two portions - a host side menu-driven user interface (the Commander) and a local downloaded DSP executable code (the Scheduler). The Commander is provided either in an MS-DOS graphics version or compatible to Microsoft Windows. When the Commander is invoked, it performs a DPR memory test, loads the scheduler into the DPR and waits for user-directed control of the PC-430.

The Executive can perform three tasks simultaneously at high speed without losing data:

- Fast "seamless" non-stop A/D data collection to local DSP memory.
- Concurrent DSP math processing of data blocks.
- Simultaneous upload of processed data blocks to the PC host.

The Commander is primarily a high speed data acquisition recorder plus user interface. The PC-430 generated data can be sent to host PC memory or disk. The saved disk files can then be displayed and processed by any graphics system such as a spreadsheet which accepts binary or floating point files. Commander operation may be batched to interleave external functions between data saves.

The scheduler is a binary COFF file (SKED.OUT) which consists of local DSP boot code, vectors, local interrupt service routines (ISR's), the full DSP library, software control/status blocks and the Application Function Block (AFB) processor.

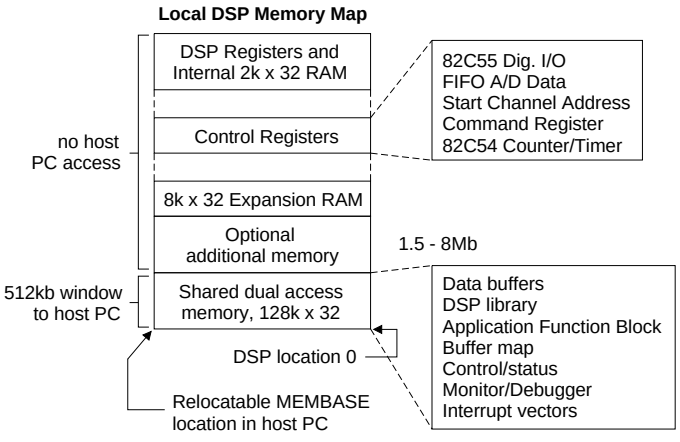

Figure 2. Local DSP Map

FUNCTIONAL SPECIFICATIONS

(Typical at +25 °C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	PC-430B	PC-430D	PC-430E	PC-430F
Number of Channels	4 (single A/D)	1 (single A/D)	16SE/8D [Note 8] (single A/D)	2 Simultaneous (two A/D's)
Input Configuration (non-isolated) [Note 19]	Single Ended	Differential	SE or Diff.	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1) [Notes 1 & 16]	0 to +10 V ±10 V ±5 V	±5 V	0 to +10 V ±10 V ±5 V	0 to +10 V ±5 V
Input Overvoltage (no damage, power on)	±15 V	±15 V	±15 V	±15 V
Overvoltage Recovery Time, maximum	2 µs	2 µs	2 µs	2 µs
Common Mode Voltage Range, maximum	—	±1 V	±10 V	—
Input Impedance [Notes 6 &10]	10 MΩ	2 KΩ	100 MΩ	1 KΩ
SAMPLE/HOLD				
Acquisition Time	750 ns	50 ns	750 ns	165 ns
Aperture Delay	20 ns	10 ns	20 ns	20 ns
Aperture Delay Uncertainty	±100 ps	±7 ps	±40 ps	±40 ps
A/D CONVERTER				
Resolution	14 bits	12 bits	12 bits	12 bits
Conversion Period	1.6 µs	200 ns	500 ns	400 ns [Note 12]
SYSTEM DC CHARACTERISTICS [Note 7]				
Integral Non-linearity (LSB of FSR)	±1.5	±2	±1	±1
Differential Non-linearity (LSB of FSR)	±1	±1	±0.75	±1
Full Scale Temperature Coefficient (LSB per °C)	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.3	±0.3	±0.1	±0.1
SYSTEM DYNAMIC PERFORMANCE [Note 2]				
Throughput to FIFO (single channel, gain = 1)	500 kHz	5 MHz	2 MHz	2 MHz
Throughput to FIFO (multiple channels, gain = 1)	330 kHz	[Note 15]	500 kHz [Note 4]	2 MHz/chan. (2 chans.)
Total Harmonic Distortion [Note 3]	–75 dB	–68 dB	–72 dB	–70 dB

The PC-430J in short-cycled addressing is recommended in place of the PC-430A. Model PC-430E can substitute for the PC-430C.

ANALOG INPUTS	
Programmable Gains	See Note 1
Common Mode Rejection (DC - 60 Hz)	-80 dB (g = 100) (430E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software

Please read all notes carefully.

A/D CONVERTER	
Output Coding	Positive-true, right justified, straight bin. (unipolar) or right-justified 2's complement (bipolar) with sign extension thru bit 15
Trigger Sources (Software selectable)	1. Local Pacer frame clock 2. External TTL frame clock 3. Analog threshold comp.
A/D Sample Clock (software selectable)	1. Internal programmable 82C54 timer 2. Ext. TTL input, active low

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	PC-430G	PC-430H	PC-430J	PC-430K
Number of Channels	2 Simultaneous (two A/D's)	1 (single A/D)	8 Simultaneous A/D's [Note 8]	2 Simultaneous (two A/D's)
Input Configuration (non-isolated) [Note 19]	Single Ended	Differential	Single Ended	Limited Differential
Full Scale Input Ranges (user-selectable) (gain = 1) [Notes 1 & 16]	±5 V or 0 to +10 V (separate models)	±5 V	±5 V, ±10 V [Note 13]	0 to +10 V, ±5 V (separate models)
Input Overvoltage (no damage, power on)	±15 V	±15 V	±15 V	±15 V
Overvoltage Recovery Time, maximum	2 µs	1 µs	3 µs	—
Common Mode Voltage Range, maximum	—	±1 V	—	±1 V
Input Impedance [Notes 6 &10]	1 MΩ	2 KΩ	8 KΩ (bipolar)	1 KΩ
SAMPLE/HOLD				
Acquisition Time	350 ns [Note 11]	35 ns	400 ns	50 ns
Aperture Delay	20 ns	±10 ns	—	10 ns
Aperture Delay Uncertainty	±70 ps	3 ps rms	—	±7 ps
A/D CONVERTER				
Resolution	14 bits	12 bits	12 bits	12 bits
Conversion Period	500 ns [Note 12]	100 ns	2 µs [Note 12]	200 ns [Note 12]
SYSTEM DC CHARACTERISTICS [Note 7]				
Integral Non-linearity (LSB of FSR)	±1.5	±1.5	±1	±2
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1
Full Scale Temperature Coefficient (LSB per °C)	±0.3	±1	[Note 13]	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.3	±1	[Note 13]	±0.3
SYSTEM DYNAMIC PERFORMANCE [Note 2]				
Throughput to FIFO (single channel, gain = 1)	1 MHz	10 MHz	400 KHz	5 MHz
Throughput to FIFO (multiple channels, gain = 1)	1 MHz/chan. (2 chans.)	[Note 15]	250 KHz/chan.**	5 MHz/ch.
Total Harmonic Distortion [Note 3]	–80 dB	–65 dB	–75 dB	–68 dB

**A 380 KHz per channel option is available on special order.

NOTES

1. Resistor-programmed gain from x1 to x100 is available on PC-430E with increased settling delay at higher gain.

2. Total throughput for single A/D modules includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. THD test conditions are:
   A. Input freq. 500 KHz (430F), 50 KHz (430J,L,M), 2 MHz (430H), 200 KHz (430B,E,G), 1 MHz (430D,K,N,P)
   B. Generator/filter THD is -90 dB minimum.
   C. THD computed by FFT to 5th harmonic.
   $$THD = 20\left(\log 10\ \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin}\right)$$
   D. Inputs are half full scale less 0.5 dB. No channel advance.
   E. A/D sample rate = 500 kHz (430B,E,G), 4 MHz (430D,K), 2 MHz (430F), 10 MHz (430H), 250 kHz (430J), 190 kHz (430L,M), 2.5 MHz (430P)

4. The rates shown for sequential sampling with single A/D modules are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PCI-430E were scanned, the maximum sample rate on any one channel would be 2 µs x 4 channels = 8 µs (125 KHz per channel).

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	PC-430L	PC-430M	PC-430N	PC-430P
Number of Channels	16 Simultaneous A/D's [Note 8]	4 Simultaneous A/D's	2 Simultaneous A/D's	4 Simultaneous A/D's
Input Configuration (non-isolated) [Note 19]	Single Ended	Single Ended	Single Ended	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1) [Notes 1 & 16]	±5 V, ±10 V, (user selectable) [Note 13]	±10 V	±2.5 V	±2.5 V or 0 to +5 V (user selectable)
Input Overvoltage (no damage, power on)	±15 V	±12 V	±15 V	±7 V
Overvoltage Recovery Time, maximum	—	—	—	—
Common Mode Voltage Range, maximum	—	—	—	—
Input Impedance [Notes 6 &10]	8 KΩ	10 MΩ	10 MΩ or 50 Ω	1000 Ω
SAMPLE/HOLD				
Acquisition Time	400 ns	—	35 ns	—
Aperture Delay	—	—	±10 ns	—
Aperture Delay Uncertainty	—	—	5 ps	—
A/D CONVERTER				
Resolution	12 bits	16 bits	14 bits	14 bits
Conversion Period	2 µs [Note 12]	5 µs [Note 12]	200 ns [Note 12]	400 ns [Note 12]
SYSTEM DC CHARACTERISTICS [Note 7]				
Integral Non-linearity (LSB of FSR)	±2	±4	±1	±3
Differential Non-linearity (LSB of FSR)	±1	±3	±1	±1.5
Full Scale Temperature Coefficient (LSB per °C)	[Note 13]	±1	±0.5	±0.5
Zero or Offset Temperature Coefficient (LSB per °C)	[Note 13]	±1	±0.5	±0.5
SYSTEM DYNAMIC PERFORMANCE [Note 2]				
Throughput to FIFO (single channel, gain = 1)	400 kHz	200 KHz	5 MHz	3 MHz* min. [Note 9]
Throughput to FIFO (multiple channels, gain = 1)	190 kHz/chan.	200 KHz/chan.	5 MHz/chan.	2.5 MHz/chan.
Total Harmonic Distortion [Note 3]	-75 dB	-83 dB	-75 dB	-75 dB

* The sample rate to published specifications is 3 MHz. The A/D is functional to 5 MHz. Valid data output per channel is delayed by 4 samples after the start of the sample clock. Please make note of this for products such as the PC-414P, PC-430P, and DVME-614P which use non-continuous A/D sampling. Data output is pipelined meaning that the first four samples per channel should be discarded. For all 4 channels, discard 16 samples. The design is intended for semi-continuous sampling of wideband signals and is less suitable for low speed data acquisition. Approximately 5 dB SFDR improvement can be achieved by directly connecting an external A/D sample clock. Contact DATEL for details.

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.

6. The input impedance of 10 MΩ minimum avoids attenuation errors from external input source resistance. For many applications, an in-line coaxial 50 Ω shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors.

7. Allow 20 minutes warmup time to rated specifications for models PC-430B,G,M,N.

8. A 25-pin DB-25S connector is used for the PC-430E, J, and L.

9. The sample rate to published specifications is 3 MHz. The A/D is functional to 5 MHz. Data output is delayed by 4 sample clocks. Data output is pipelined meaning that the first four samples should be discarded. The design is intended for semi-continuous sampling of wideband signals. Approximately 5 dB SFDR improvement can be achieved by directly connecting an external A/D sample clock. Contact DATEL for details.

10. Input impedance is shown with power on. Impedance with power off is 1.5 KΩ or less.

11. PC-430G acquisition time is 350 ns to ±0.01% of FSR.

12. All channels in simultaneous sampling.

SPECIFICATIONS, CONTINUED

(Typical @ +25°C, dynamic conditions, unless noted)

TRIGGER CONTROL	
Programmable Timer Counter Type	82C54 (DSP waits required)
Functions	1. EOC sample counter. 2. A/D start rate (16 bit divisor) 3. SSH sample counter (430A)
Pacer Sample Counter	3 to 65,535 samples.
Clock Source	
Internal	10 MHz crystal clock
External	TTL input, direct to A/D
Analog Trigger	Uses comparator and on-board D/A channel. [Note 5]
Pretrigger	Sample down counter is delayed until an external trigger. Pretrigger samples are stored in a ring buffer.
ISA BUS INTERFACE	
Architecture	I/O and memory mapped, for IBM-PC/AT, and compatibles.
I/O Mapping	Three 16-bit I/O registers. Decodes I/O address lines A9 - A2.
Data Transfer	Memory block transfer, real or protected mode.
Data Bus	16 bits
Number of Interrupts	1 interrupt, software selectable on levels 9, 10, 11, or 15.
Bus Interrupt Sources	DSP interrupt request to PC.
LOCAL MICROCOMPUTER	
CPU Type	TI TMS 320C30
Local Data Bus	32 bits
CPU Clock Speed	40 MHz
Local DMA Controller	Internal to 320C30 CPU
Primary Memory (Dual access to PC/AT)	128k x 32 static RAM, expandable to 2048k x 32 total (8 Mb).
Expansion Memory	8k x 32 static RAM
Internal DSP Memory	Two 1k x 32
Dual Port Access	Hold mode by control bit or from PC/AT dynamic hold per each access.
CPU Test Port	Supports TI XDS1000 Extended Development System
Local Interrupts to DSP	Int 0-3 from PC host request, A/D FIFO or acquire flags or optional external interrupt.
DSP Wait States	Software programmable up to 7 waits via DSP register.
Digital I/O Port	24 lines, programmable In or Out, TTL levels, 82C55

MISCELLANEOUS	
Analog Input Connectors	Four miniature threaded coaxial, type SMA, mounted on rear slot. DB-25 for PC-430E,J, & L.
Trigger Connector (all models except E, J, & L)	5th SMA for external TTL trigger.
D/A Analog Outputs	2 channels, ±5V or ±10V output ranges, 12 bit resolution, 5µs settling. May be used to select analog trigger level.
A/D FIFO Memory	2048 or 8192 A/D samples, programmable 16 or 32 bits wide.
Memory Expansion Port	Dual-row header connector for 320C30 memory (unbuffered).
Serial Port and External Trigger/Pacer Clock (dual row header)	Two serial channels, compatible to 320C30 serial ports. Both scan (Trigger) and A/D sample clocks are accepted at connector.
RS-232-C Serial Port	3 header pins. Uses software UART.
Operating Temp. Range	0 to +60°C
Storage Temp. Range	-25 to +85°C
Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet. Forced cooling is recommended.
Power Required	+5V DC 3.5 Amps max.
Outline Dimensions	4.5 x 13.2 inches

13. PC-430J and L bipolar input is user-selectable ±5 V or ±10 V per channel (default). Total full scale error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±2 LSB maximum. Monotonicity: no missing codes over temperature range.

14. Avoid mixing external triggers which are a close submultiple of the internal A/D start clock to prevent lost samples.

15. Models PC-430D and H use a single channel 12-bit A/D converter with ±5 V inputs. An external A/D clock is required above 4 MHz and the 82C54 timer must be bypassed. 10 MHz sampling may continue until the FIFO memory is full.

16. Input polarity: Some models are fixed as bipolar only whereas others are user-selectable unipolar or bipolar. Still others require separate model numbers.

17. Models F, G, J, K, L, M, N, and P use one A/D converter per channel.

18. The customer must use shielded cables to insure EMC compliance.

19. A/D-per-channel boards (models F, G, J, K, L, M, N, P) may be operated in "software differential" mode. Two A/D's are applied to the high and low legs of a single differential input channel. The two data values are then algebraically subtracted, either on the fly in real time or after all samples have been stored. Channel capacity in "software differential" is one-half the number of single-ended channels.

    This technique offers excellent bandwidth, high common mode rejection and optional mix of single-ended and differential channels.

Application Function Blocks (AFB)

The Executive optimizes three competing objectives:

- Easy to use
- Fast
- Powerful (access to a full DSP software library)

A high speed command list is used to achieve these mutually exclusive goals. The AFB is a short list of commands which call local PC-430 DSP library functions previously downloaded by the Commander to the DPR and reside in the scheduler. No local programming is needed.

Similar to a spreadsheet macro or DOS batch file but much faster, the user writes the AFB file with any text editor and the Commander converts it on the PC side to an internal binary form. The Commander then downloads the converted AFB file to the DPR for execution.

The AFB is powerful because of full access to the DSP library and because repeating functions may be looped. These loops in turn may be nested. Loops can run with a loop count or "forever". Unlike a slow ASCII interpreter, the AFB system runs at nearly the full speed of the 320C30 DSP with minimal overhead. Besides the large DSP library, the user may write additional AFB functions in "C" or TI assembly and integrate them with the schedular.

AFB Library Functions

Over 60 functions are included in the Executive AFB library. These are fully described in the PC-430 User's Manual (included with the board). The functions become resident when the scheduler is downloaded. Fully commented source code to these functions is found in the PC-430SRC and PC-430WINS packages. Most functions are written in a mix of high performance "C" and 320C30 Assembly language. Users may modify the functions or add their own functions and rebuild the system.

The functions are grouped in five major categories:

- A/D Scan and Timer/Counter Routines
- DSP Array Math Routines
- Array Conversion Routines
- Single Variable Transcendentals
- Buffer Management

FIFO Data Format

A/D data is delivered as a stream from the FIFO memory. For multichannel inputs, this means that data is multiplexed. For example, for 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, . . . Some applications may need this data de-multiplexed by software so that each channel's data is placed in its own separate buffer.

Table 1. PC-430 I/O Registers

I/O Address	Direction	Function
I/O BASE + 0	Write Read	PC Command Register PC Status Register
I/O BASE + 2	Write Read	Memory Base Address Not Used
I/O BASE + 4	Write	Page Address Register

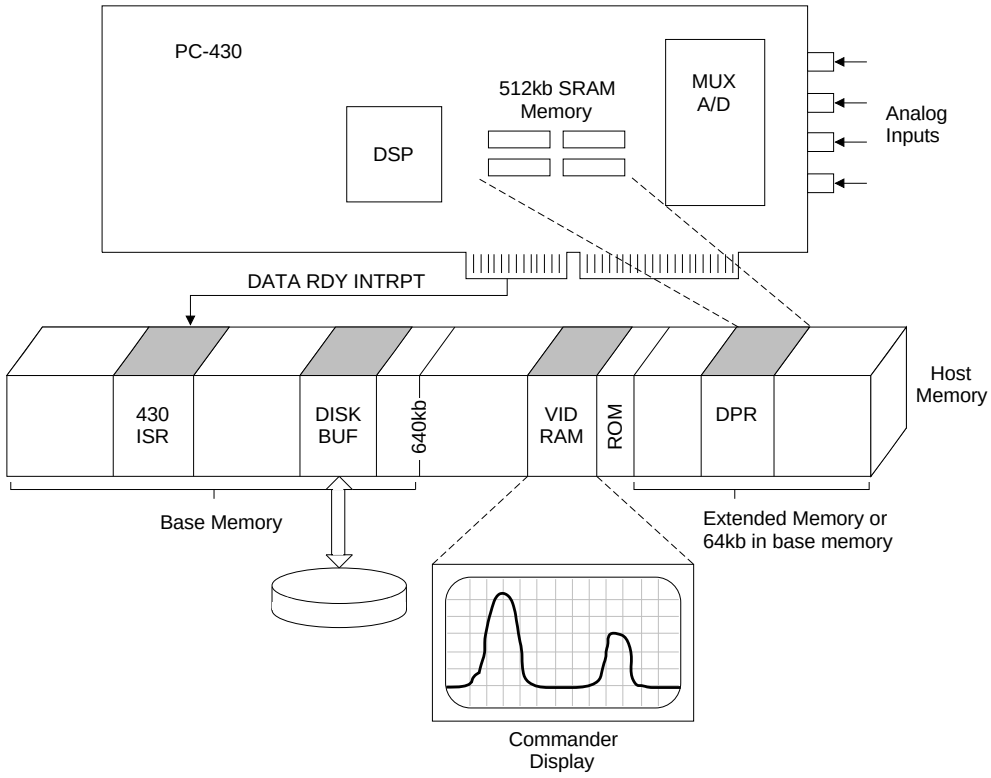

Figure 3. Array Preprocessing

ORDERING INFORMATION

Hardware:

PC-430

Input Channels, A/D Resolution

B = 4SE chans., 14 bits
D = 1D chan., 12 bits
E = 16SE/8D chans., 12 bits
F = 2SE simul. chans., 12 bits
G = 2SE simul. chans., 14 bits
H = 1D chan., 12 bits
J = 8SE simul. chans., 12 bits
K = 2SE simul. chans., 12 bits
L = 16SE simul. chans., 12 bits
M = 4SE simul. chans., 16 bits
N = 2SE simul. chans., 14 bits
P = 4SE simul. chans., 14 bits

A/D FIFO Size

1 = 2k samples
2 = 8k samples

A/D Polarity

A = Bipolar or selectable
B = Unipolar
For models with user-selectable polarity use the "A" designator. CAUTION: Read the input range specifications carefully.

Total On-Board Memory*

1 = 512 kilobytes
2 = 2 megabytes
3 = 8 megabytes

Memory options are surface mounted. Once selected, they cannot be changed.
*Not including 8k x 32 expansion memory, installed on all models.

Example: PC-430G2A 14 bits, 8k FIFO, bipolar input, 512 kB memory.

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. The warranty period is one year.

61-7342340 SMA to BNC cable, one required per channel, one meter.

Software:

PC-430EXEC	Executive, Commander, and Scheduler executables only for MS-DOS. 3.5 inch 1.4 Mb disks.
PC-430SRC	Full source code to PC-430EXEC. Requires Microsoft and TI "C". Includes MS-DOS Window Boss library.
PC-430WIN	Microsoft Windows 95 version of PC-430EXEC. Executables only.
PC-430WINS	Full source code to PC-430WIN. Requires Microsoft Visual BASIC, Borland C++, MASM, and TI "C".
PC-430LV, LVS	Bridge driver to National Instruments' LabVIEW®. See PC-430LV data sheet.
UM-CMDRSRC	Commander software manual (included with Commander).