ALS/AS Logic Data Book

1986

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Advanced Low-Power Schottky Advanced Schottky





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INTRODUCTION

The ALS/AS Logic Data Book presents pertinent technical information on Texas Instruments advanced families of TTL integrated circuits, Advanced Low-Power Schottky[†] (ALS), and Advanced Schottky[†] (AS). TI's ALS or AS functions provide the system design engineer with management tools to optimize system performance. Aggressive design goals can be achieved by utilizing ALS in noncritical paths and high-performance AS in speed critical paths.

The use of pin-for-pin compatible devices with the most popular LSTTL and STTL functions, existing TTL-based systems may be easily upgraded to ALS/AS to reduce system power requirements, enhance system performance, and improve overall system reliability. New system designs can capitalize on both the improved efficiency of the pin-compatible devices and the higher densities of the MSI/LSI series of devices unique to the ALS/AS family.

ALS and AS devices utilize an advanced wafer fabrication process that includes walled emitters, ion-implanted transistors, oxide isolations, and composed masks. This process is coupled with circuit design techniques to implement the following:

- improve input threshold and noise margins
- improve line driving and receiving
- maintain or increase drive capability
- tolerate ± 10% supply voltage swings
- take advantage of new packaging
 - 24-pin 300-mil DIP
 - plastic "Small Outline"
- specify ac parameters over the full operating temperature range

The ALS/AS family will grow to well over 400 devices through the end of 1986. Included among the new functions are:

- the fastest stand-alone 32-bit error detection and correction circuit (EDAC)
- high-performance 16 × 4 and 16 × 5 "zero-fall-through" FIFO (first in, first out) memory devices with 24-nanosecond fall through
- edge-triggered octal, 9-bit, and 10-bit read-back latches
- high-speed and low-power bus-transceivers with internal registers
- many additional pin-compatible ALS and AS devices

Also included in this book are several linear interface circuits that utilize the Advanced Low-Power Schottky[†] technology to provide a new linear interface family of devices with improved speed-power characteristics. The leadership functions are as follows:

- IBM 360/370 I/O Line Drivers
- IEEE-488 (GPIB) Octal Bus Transceivers
- RS-422-A Quad Line Drivers
- RS-422-A, RS-423-A, and RS-485 Quad Line Receivers

This data book provides a functional index of all bipolar digital, as well as, selected linear interface device types available or under development. Package dimensions given in the Mechanical Data section of this book are in metric measurement (and parenthetically in inches), which should simplify board layout for designers involved in metric conversion and new designs. The General Information section includes an explanation of the function tables, parameter measurement information, thermal information, D flip-flop and latch signal conventions, and typical characteristics related to the products listed in this volume.

Complete technical data for any Texas Instruments semiconductor/component product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to:

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We sincerely believe that you will find the new ALS/AS Logic Data Book a meaningfull addition to your technical library.

[†]Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I - OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

ICC Supply current

The current into* the V_{CC} supply terminal of an integrated circuit.

ICCH Supply current, outputs high

The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

ICCL Supply current, outputs low

The current into* the VCC supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input.

I_|L Low-level input current

The current into* an input when a low-level voltage is applied to that input.

IOH High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

IOL Low-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

IOS Short-circuit output current

The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

IOZH Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied

The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

^{*}Current out of a terminal is given as a negative value.



IOZL Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied

The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

VIH High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

VIK Input clamp voltage

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

VIL Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

VOH High-level output voltage

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

VOL Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

ta Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

tdis Disable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state. NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

ten Enable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., \dot{G}). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs will change only if they are responding to data that would cause the output to go low so $t_{en} = t_{PHL}$.

^{*}Current out of a terminal is given as a negative value.



GLOSSARY TTL SYMBOLS. TERMS. AND DEFINITIONS

th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

- NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
 - The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

tpd Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{nd} = t_{PH} or t_{Pl} H).

tphL Propagation delay time, high-to-low-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

tpHZ Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

tpLH Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

tpLZ Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

tpzH Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

tpzL Enable time (of a three-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} Sense recovery time

The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

- NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
 - The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

tw Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.



PART II - CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

PART III - STRESS

Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



The following symbols are used in function tables on TI data sheets:

Н high level (steady state) low level (steady state) = ϯ transition from low to high level transition from high to low level = value/level or resulting value/level is routed to indicated destination value/level is re-entered Х irrelevant (any input, including transitions) z off (high-impedance) state of a 3-state-output the level of steady-state inputs at inputs A through H respectively a..h Q_0 level of Q before the indicated steady-state input conditions were established Qη complement of Qn or level of \overline{\Omega} before the indicated steady-state input conditions were established level of Q before the most recent active transition indicated by \(\psi\$ or \(\extstyle \) Q_n one high-level pulse one low-level pulse TOGGLE each output changes to the complement of its previous level on each active transition indicated by

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, \bigcap or \bigcap , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FU	NCT	'ION	TA	BL	E

	INPUTS										OUTPUTS			
01.545	МО	DE	01.004	SEF	RIAL	ı	PARA	LLEL	-	_		ο-		
CLEAR	S1	SO	CLOCK	LEFT	RIGHT	Α	В	С	D	QA	σВ	σc	σD	
L	×	X	×	Х	х	х	х	Х	×	L	L·	L	L	
Н	×	X	L	х	X	х	X	X	X	Q _{A0}	α_{B0}	α_{C0}	Q_{D0}	
Н	н	Н	t	х	×	а	b	С	d	а	b	С	d	
н	L	Н	1	х	н	x	Х	X	X	Н	Q_{An}	Q_{Bn}	Q_{Cn}	
н	L	Н	1	х	L	х	X	X	X	L	Q_{An}	α_{Bn}	α_{Cn}	
н	н	L	1	н	X	x	Х	Х	×	QBn	Q_{Cn}	α_{Dn}	Н	
н	н	L	1	L	×	x	×	Х	X	QΒn	α_{Cn}	α_{Dn}	L	
н	L	L	×	×	×	х	×	X	X	Q _{A0}	σ_{B0}	σ^{C0}	$\dot{\sigma}_{D0}$	

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A , data entered at B will be at Q_B , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_D is now at Q_D , the previous levels of Q_D and Q_D are now at Q_D and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

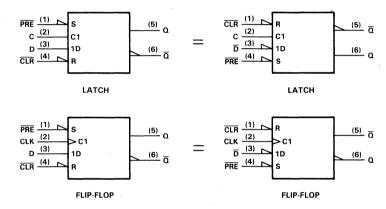
The truth table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called $\overline{\Omega}$ and those producing complementary data are called $\overline{\Omega}$. An input that causes a Ω output to go high or a $\overline{\Omega}$ output to go low is called Preset (PRE). An input that causes a $\overline{\Omega}$ output to go high or a Ω output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.

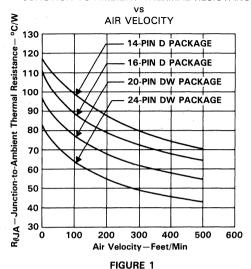


The figures show that when Q and \overline{Q} exchange names, the Preset and Clear pins also exchange names. The polarity indicators (\triangleright) on \overline{PRE} and \overline{CLR} remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the Advanced Low-Power Schottky (ALS) and Advanced Schottky (AS) families. In general, junction temperature for any device can be calculated using Equation 1.

JUNCTION-TO-AMBIENT THERMAL RESISTANCE



$$T_J = R_{\theta JA} (V_{CC} \cdot I_{CC} + N \cdot I_{OL} \cdot V_{OL}) + T_A$$

(1)

where

T_J = virtual junction temperature

 $R_{\theta}JA$ = thermal resistance, junction to ambient air

VCC = supply voltage (5 V for typical, 5.5 V for maximum)

ICC = supply current

N = the number of outputs

IOL = the low-level output current

VOL = the low-level output voltage

 T_A = the ambient air temperature

Typical junction temperature can be calculated using Equation 1 directly with typical values of I_{CC} taken from the data sheets and $V_{CC}=5$ volts. To calculate maximum junction temperature, it is necessary to take into account the spread of I_{CC} values for a population. Due to different specification practices that have been followed, it is sometimes useful to use slightly different calculation procedures for the ALS and AS families.

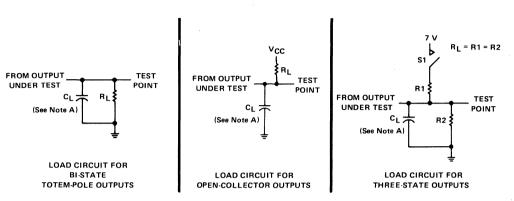
Maximum junction temperature for all 54ALS, 54AS, and some 74ALS parts can be calculated using Equation 1 with I_{CC} being the maximum value specified on the data sheet and V_{CC} = 5.5 volts. In fact, I_{CC} for Series 54 devices at the temperature extremes of $-55\,^{\circ}$ C to $125\,^{\circ}$ C will be higher than for a Series 74 device at the temperature extremes of $0\,^{\circ}$ C to $70\,^{\circ}$ C. This is reflected in the limits specified for some 74ALS devices, which are less than those specified for 54ALS devices. The AS family and most ALS family data sheets give a single maximum value for I_{CC}. If that value is used to calculate maximum junction temperature for series 74 devices, an unrealistically high value will result. Instead, Equation 2 can be used. This uses the factor 1.31 to scale the typical value of I_{CC} up to a practical maximum value for process variations and thermal effects.

Thus, for 74AS and 74ALS devices if a lowered maximum ICC has not been specified:

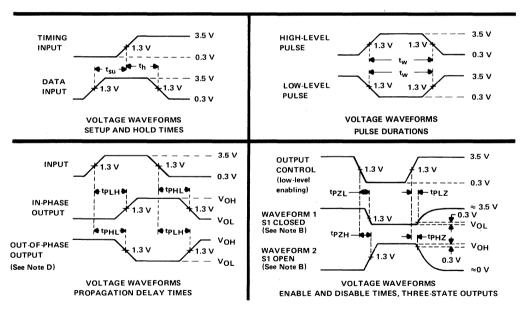
$$T_{J}max = R_{\theta JA} (5.5 \cdot 1.31 \cdot I_{CCtyp} + N \cdot I_{OL} \cdot V_{OL}) + T_{A}$$

(2)

SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTE A: C₁ includes probe and jig capacitance.



NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_{\Gamma}=t_{\Gamma}=2$ ns, duty cycle = 50%.
- D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- E. The outputs are measured one at a time with one input transition per measurement.

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	STD TTL	ALS	AS	н	L	LS	s	VOLUME	
Hex 2-Input Gates	'804		А	В					3	
	′04	•			•	•	•	•	2	
Hex Inverters			Α	•					3	
	1004		•	•					,	
	'00	•			•	•	•	•	2	
Quadruple 2-Input Gates			Α	•					- 3	
	1000		Α	Α					,	
	'10	•			•	•	•	•	2	
Triple 3-Input Gates	10		Α	•					3	
	1010		Α						3	
	'20	•			•	•	•	•	2	
Dual 4-Input Gates	20		Α	•					3	
	1020		Α						3	
8-Input Gates	,30	•			•	•	•	•	2	
o-input dates	30		Α	•					3	
13-Input Gates	133							٠	2	
13-input Gates	133		•						3	
Dual 2-Input Gates	'8003		•			_		l	,	

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

			TE	CHN	COLOC	Ϋ́			
DESCRIPTION	TYPE	STD TTL	ALS	AS	н	L	LS	s	VOLUME
	'05	•			•		•	•	2
Hex Inverters	05		Α	T					3
	1005		•						,
	'01	•			•		•		2
	01		•						3
Quadruple 2-Input Gates	'03	•				•	•	•	2
	03		В						3
	1003		Α						,
Table Oliver A Control	'12	•					•		2
Triple 3-Input Gates	12		Α						3
Direct A leaves Coster	'22	•			•		•	•	2
Dual 4-Input Gates	1 22		В						3

POSITIVE-AND GATES

	1		TEC	HNOL	.OG\	′		
DESCRIPTION	TYPE	STD	ALS	AS	н	LS	s	VOLUME
Hex 2-Input Gates	'808		Α	В				3
	'08	•				•	•	2
Quadruple 2-Input Gates	708		•	•				3
	1008		Α	•] 3
	'11				•	•	•	2
Triple 3-Input Gates	1 ''		Α	•				3
	1011		A	T				3
D. J. A.L Cours	'21				•	•		2
Dual 4-Input Gates	21		•	•				3

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	STD	ALS	AS	н	LS	s	VOLUME
Quadruple 2-Input Gates	'09	•				•	•	2
Quadruple 2-liiput Gates	1 03		•					3
Trials 2 Issue Cons	′15				•	•	•	2
Triple 3-Input Gates	15		Α					3

POSITIVE-OR GATES

			TECH				
DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	s	VOLUME
Hex 2-Input Gates	'832		Α	В			3
	'32	•			•	•	2
Quadruple 2-Input Gates	32		•	•			2
	1032		Α	•			,

POSITIVE-NOR GATES

DESCRIPTION	TYPE	STD	ALS	AS	L	LS	s	VOLUME
Hex 2-Input Gates	'805		Α	В				3
	′02	•			٠	•	•	2
Quadruple 2-Input Gates		1 02		•	•			
[1002	1	Α					3
Triple 3-Input Gates	'27	•				•		2
Triple 3-lilput Gates	21		•	•				3
Dual 4-Input Gates with Strobe	'25	•						2
Dual 5-Input Gates	′260						•	1 -

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	s	VOLUME
11	'14	•			•		
Hex Inverters	'19				•		1
Octal Inverters	'619				•		
Dord Aller A Braille - MAND	′13	•			•		1
Dual 4-Input Positive-NAND	′18				•		2
Triple 4-Input Positive-NAND	'618				•		
0 1 1 01 10 11 11 11 11 11	'24				•		
Quadruple 2-Input Positive-NAND	′132	•			•	•	

CURRENT-SENSING GATES

DESCRIPTION	T1/DE	TECHNOLOGY		VOLUME	
DESCRIPTION	TYPE	ALS	AS	LS	VOLUME
Hex	′63			•	2

DELAY ELEMENTS

DESCRIPTION		TECH	INOL	VOLUME	
DESCRIPTION	TYP	ALS	AS	LS	VOLUME
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31			•	2

- Denotes available technology.
- A Denotes "A" suffix version available in the technology indicated.
- B Denotes "B" suffix version available in the technology indicated.



GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND OR INVEST CATE

			T	ECHN	OLO	GY			
DESCRIPTION	TYPE	STD	ALS	AS	н	L	LS	s	VOLUME
2-Wide 4-Input	'55				•	•	•		
4-Wide, 4-2-3-2 Input	′64					T		•	
4-Wide 2-2-3-2 Input	′54				•	П			,
4-Wide 2-Input	'54	•					Г		1 -
4-Wide 2-3-3-2 Input	'54						•		1
Dual 2-Wide 2-Input	'51	•			•	•	•	•	1

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

		T	ECHNO	LOGY	,	
DESCRIPTION	TYPE	STD TTL	ALS	AS	s	VOLUME
4-Wide 4-2-3-2 Input	'65				•	2

EXPANDABLE GATES

		TECHNOLO						}	
DESCRIPTION	TYPE	STD	ALS	AS	н	L	LS	VOLUME	
Dual 4-Input Positive-NOR with Strobe	'23	•					Г		
4-Wide AND-OR	'52				•			,	
4-Wide AND-OR-INVERT	'53	•			•			2	
2-Wide AND-OR-INVERT	'55				•	•	•	1	
Dual 2-Wide AND-OR-INVERT	'50	•		7	•	Г	T	1	

EXPANDERS

		T				
DESCRIPTION	TYPE	STD	ALS	AS	н	VOLUME
Dual 4-Input	'60	•			•	
Triple 3-Input	'61				•	2
3-2-2-3 Input AND-OR	'62				•	l

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

		I	TECH	NOL	OGY		
DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	s	VOLUME
	'07	•					2
	'17	•					1
Hex	'35		•				3
	1035		•				3
	′06	•					2
Hex Inverter	′16	•					
	1005		•				3
	′26	•			•		2
/	′38	•			•	•	
Quad 2-Input Positive-NAND	36		Α				3
	. '39	•					2
	1003		Α				3
Quad 2-Input Positive-NOR	'33	•			•		2
Quad 2-input i daitive-NON	- 33		Α				3

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

			TECHI	NOLO	GY		
DESCRIPTION	TYPE	STD	ALS	AS	LS	s	VOLUME
Noninverting	'757			•			
Octal Buffers/Drivers	'760			•			
Inverting Octal	'756			•			
Buffers/Drivers	'763		•	•			3
Inverting and Non-Inverting Octal Buffers/Drivers	'762		•	•			,
Non-Inverting Quad Transceivers	'759			•			
Inverting Quad Transceivers	'758		•	•			

A Denotes "A" suffix version available in the technology indicated.



Denotes available technology.

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

			TECH	OLC	GY	,	
DESCRIPTION	TYPE	STD	ALS	AS	LS	s	VOLUME
Noninverting 10-Bit Buffers/Drivers	'29827		•				
Inverting 10-Bit Buffers/Drivers	'29828		•				
Noninverting 10-Bit Transceivers	'29861		•				LSI
Inverting 10-Bit Transceivers	129862		•				LSI
Noninverting 9-Bit Transceivers	129863		•				
Inverting 9-Bit Transceivers	129864		•				
	'241				•	•	2
	241		Α	•			3
	244				•	•	2
	244		Α	•			3
	'465				•		2
Noninverting	405		Α				3
Octal Buffers/Drivers	'467				•		2
	467		Α				3
	'541				•		2
	541		•				
	'1244 ⁴		Α				3
	'231		•	•			1
					•		2
	'240		A	•			3
					•	1	2
Inverting Octal	'466		Α			1	3
Buffers/Drivers					•		2
	'468		Α	-		T	3
						1	2
	'540		•		†	1	3
	'1240¶		•				
Inverting and Noninverting		_		1	† —	T	3
Octal Buffers/Drivers	'230			•	1		
	1			\vdash	•	T	2
Octal Transceivers	'245		A	•	 	†	
	1245		A	\vdash	t	T	3
Noninverting	'365	A			Α	T	2
Hex Buffers/Drivers	'367	A	1		А	Т	2
Inverting	'366	A	†		А	T	2
Hex Buffers/Drivers	'368	A	†	T	A	T	2
	125	•	1	t	A	t^{-}	
Quad Buffers/Drivers	126			+	A	t-	1
with Independent	'425		t	\vdash	+	1	2
Output Controls	'426	•	-	1	 	+-	1
Noninverting	+	Ť	+	+-	•	+	
Quad Transceivers	1243	\vdash	A	•	 	+	3
***************************************	+	+	+	Ė		t^-	2
Inverting	'242	-	A	•	Ť	t	
Quad Transceivers	11242	+	-	Ť	+	+	3
Quad Transceivers with Storage	226	+-	Ť	+	-		
12 Input NAND Gate	1134	+-	+	+	+	+	2

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	STD	ALS	AS	s	VOLUME
Hex 2-Input Positive-NAND	'804		Α	В		
Hex 2-Input Positive NOR	'805		Α	В		3
Hex 2-Input Positive-AND	.808		Α	В] '
Hex 2-Input Positive-OR	'832		Α	В		1
Quad 2-Input Positive-NOR	128	•				1
Oual 4-Input Positive-NAND	1140				•	1 -

- Denotes available technology.
- Denotes very low power.
- A Denotes "A" suffix version available in the technology indicated.
- B Denotes "B" suffix version available in the technology indicated.



BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

	T	T	TECH	INOL	OGY	,		
DESCRIPTION	TYPE	STD	ALS	AS	н	LS	s	VOLUME
Hex 2-Input Positive-NAND	'804		A	В				
Hex 2-Input Positive-NOR	'805		Α	В				1
Hex 2-Input Positive-AND	'808		Α	В				1
Hex 2-Input Positive-OR	'832		A	В				3
Hex Inverter	1004		•	•				1
Hex Buffer	'34		•	•				1
нех витег	11034		•	Α				
	'37	•				•	•	2
Quad 2-Input Positive-NAND	3/		Α					3
	1000		Α	•				1 3
	'28	•				•		2
Quad 2-Input Positive-NOR	20		Α					
	1002		Α		Г			
	1036			Α	Г		Г	
Quad 2-Input Positive-AND	1008		Α	•				3
Quad 2-Input Positive-OR	1032		Α	•				1
Triple 3-Input Positive-NAND	1010		Α					1
Triple 3-Input Positive-AND	1011 .		Α					1
	'40	•			•	•	•	2
Dual 4-Input Positive-NAND	140		Α		T			
	1020		A					3
Line Driver/Memory Driver with Series Damping Resistor	'436						•	2
Line Driver/Memory Driver	'437	-	 	 	H	-	•	1

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

	TYPE]	TE	CHNC	LOG	Y	
DESCRIPTION	OF OUTPUT	TYPE	ALS	AS	LS	s	VOLUME
Quad with Bit Direction	3-State	'446		T	•		
Controls	3-State	'449			•		1
	ос	'440			•	Г	1
	ос	'441		T	•		
	3-State	'442			•		2
Quad Tridirection	3-State	'443		1	•		1
	3-State	'444		1	•		1
	ос	'448			•	Г	1
4-Bit with Storage	3-State	'226				•	1

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	STD	ALS	AS	LS	s	VOLUME
	'2620			•			
Inverting Outputs, 3-State	'2640			•			١ ,
T 0 2 C	'2623			•] 3
True Outputs, 3-State	'2645			•			l

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/OUTPUT RESISTORS

				Y				
DESCRIPTION		TYPE	STD TTL	ALS	AS	LS	s	VOLUME
Input Resistors	Inverting Outputs	'746		•				
input nesistors	Noninverting Outputs	'747		•				3
0	Inverting Outputs	'2540		•				3
Output Resistors Noninverting Out		′2541		•				

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OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

		TYPE	Γ	TEC	HNOL	OGY	
DESCRIPTION		OF	TYPE	_			
		OUTPUT	1	ALS	AS	LS	VOLUME
	T	2 54-4-	1245	Α	•		3
		3-State	'245			•	2
		ос	'621	Α	•		3
	l	00	021			•	2
	Low	3-State	'623	Α	٠		3
12 mA/24 mA/48 mA/64 mA	Power	3-State	023			•	2
Sink, True Outputs	rowei	OC, 3-State	'639	А	•		3
Sink, Tibe Outputs	į	OC, 3-State	039			•	2
		3-State	652	•	•		3 & LSI
		3-State	002			•	2
		OC, 3-State	'654	A			3
		UC, 3-State				•	2
		3-State	'620	Α	٠		3
		5 Giole				•	2
		ос	-622	Α	•		3
		00	022			•	2
12 mA/24 mA/48 mA/64 mA	Low	OC, 3-State	'638	Α	•		3
Sink, Inverting Outputs	Power	OC. 3-State	036			•	2
		0.00	'651	•	•		3 & LSI
		3-State				•	2
		00.00	'653	•			3
		OC, 3-State	'653			•	2
				A	•		
	Low	oc	'641			•	2
12 mA/24 mA/48 mA/64 mA	Power			Α	•		3
Sink, True Outputs		3-State	'645			•	2
	Very Low					_	
	Power	3-State	1645	Α		ì	3
				A	•		
	Low	3-State	'640				2
12 mA/24 mA/48 mA/64 mA	Power			А	•		3
Sink, Inverting Outputs		oc	'642			•	2
	Very Low	<u> </u>	1				
	Power	3-State	1640	Α			3
				A	•		
12 mA/24 mA/48 mA/64 mA		3-State	643				
Sink, True and	Low					•	2
Inverting Outputs	Power	ос	644	A	•		3
		ļ				•	2
Registered with Multiplex		3-State	646	•	•		3 & LSI
12 mA/24 mA/48 mA/64 mA					L	•	2
True Outputs		ос	'647	•			3
		1				•	2
Registered with Multiplexed		3-State	648	•	•		3 & LSI
12 mA/24 mA/48 mA/64 mA				L		•	2
Inverting Outputs		ос	'649	•			3 & LSI
g corpore						•	2
Universal Transceiver/			'877		•		
Port Controllers		3-State	1852		•		3 & LSI
, or commonera		L	'856		•		L



FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

			TI	CHNC	LOG	Y			
DESCRIPTION	TYPE	STD TTL	ALS	AS	н	L	LS	s	VOLUME
	′73	•		<u> </u>	•	•	Α		
	′76						Α		
•	′78				•	•	Α		
	103			1	•				2
	106			Т	•				'
	107	•					Α		l 1
Dual J-K Edge-Triggered	108				•				1
	109	•		1			A		
	109		А	•					3
	'112						Α	•	2
	1112		Α						3
							A	•	2
	1113		A						3
				1			Α	•	2
	1114		Α						3
	'70	•							
Single J-K Edge-Triggered	'101			1	•				
	1102				•				
	'73	•			•	•		_	
	'76	•			•				
Dual Pulse-Triggered	'78			 	•	•			
	107	•							
	771				•	•			2
	'72	•			•	•			
Single Pulse-Triggered	1104	•						_	
	1105	•		†	\vdash				
Dual J-K with Data Lockout	1111	•							
Single J-K with Data Lockout	1110	•							
Dual D-Type	'74	•	A		•	•	Α	٠	3

QUAD AND HEX FLIP-FLOPS

				I	TECH	VOLC	GY		
DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	STD	ALS	AS	LS	s	VOLUME
			174	•			•	•	2
	6	Q	174		•	•			3
	L	1	'378				•		
D Type			1171				•		2
	١.	a, ā		•			•	•	1
	4	u, u	175		•	Α			3
			'379				•		
	Τ.	_	'276	•				Г	2
J-K	4	Q	'376	•					ĺ

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

					TECH	NOLO	GY		
DESCRIPTION	NO. OF BITS	ОИТРИТ	TYPE	STD TTL	ALS	AS	LS	s	VOLUME
		3-State	1374		•	•		Г	3
True Data	Octal	3-State	3/4				•	•	2
		3-State	1574		В	•			3
		2-State	'273		•	-	•	-	2
True Data with Clear	Octal	3-State	1575		•	•			
		3-State	'874		•	•			3
		3-State	'878		•	•			
True with Enable	Octal	2-State	'377				•		2
	i	3-State	'534		•	•			
Inverting	Octal	3-State	1564		Α				
		3-State	'576		Α	•			3
Inverting with Clear	Octal	3-State	'577		Α	•] 3
inverting with Clear	Octai	3-State	'879		Α	•			
Inverting with Preset	Octal	3-State	'876		Α	•			
True	Octal	3-State	'825			•			
Inverting	Octal	3-State	'826			•			ļ
True	9-Bit	3-State	'823			•]
Inverting	9-Bit	3-State	'824			•			
True	10-Bit	3-State	'821			•			
Inverting	10-Bit	3-State	'822			•			3 & LSI
True	Octal	3-State	'29825		A	•			J & L31
Inverting	Octal	3-State	'29826		A	•			ĺ
True	9-Bit	3-State	29823		A	•			l
Inverting	9-Bit	3-State	29824		•	•			
True	10-Bit	3-State	'29821		•	•			
Inverting	10-Bit	3-State	'29822		A	•			1

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LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	STD	ALS	AS	L	LS	VOLUME
Dual 2-Bit	2-State	'75	•			•	•	
	2-State	'77	•			•	•	2
Transparent	2-State	'375		-			•	1 2
S-R	2-State	'279	•				Α	1

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

			TECHI	,			
DESCRIPTION .	TYPE	STD	ALS	AS	LS	L	VOLUME
	'122	• `			•	•	
Single	'130	•					
	'422	T			•		2
Dual	'123	•			•	•	Ì
Duai	'423				•]

OCTAL, 9-BIT, AND 10-BIT READ-BACK LATCHES

			TECHNOLOGY					
DESCRIPTION	NO. OF BITS	TYPE	STD TTL	ALS	AS	LS	s	VOLUME
Edge-Triggered Inverting and Noninverting	Octal	1996		•				
	Octal	1990		•]
Transparent True	9-Bit	'992		•]
	10-Bit	'994		•				
	Octal	1991		•				3 & LSI
Transparent Noninverting	9-Bit	'992		•				3 & L31
	10-Bit	1994		•				
Transparent with Clear True Outputs	Octal	'666		•				
Transparent with Clear Inverting Outputs	Octal	'667		•				

OCTAL, 9-BIT, AND 10-BIT LATCHES

	-				TECH	NOLO	GY			
DESCRIPTION	NO. OF BITS	ОИТРИТ	TYPE	STD TTL	ALS	AS	LS	s	VOLUME	
			'268					•		
_		3-State	'373				•	•	2	
Transparent	Octal				•	•			3	
		3-State	'573		•	•			}	
Dual 4-Bit		2-State	1100	•					2	
	Octal	2-State	′116	•] ^	
Transparent		3-State	'873		В	•				
		3-State	'533		•	•				
Inverting Transparent	Octal	3-State	'563		Α				3	
	1	3-State	'580		Α	•] '	
Dual 4-Bit Inverting Transparent	Octal	3-State	'880		А	•				
		3-State	'604				•			
-Input Multiplexed Octal	0	ос	'605				•		1	
2-input Multiplexed	Octal	Octal	3-State	'606				•		2
		ОС	'607				•		1	
Addressable	Octal	2-State	'259	•	•		•		3	
Multi-Mode Buffered	Octal	3-State	'412	-		\vdash		•	2	
True	Octal	3-State	'845		•	•				
Inverting	Octal	3-State	'846		•			$\overline{}$	1	
True	9-Bit	3-State	'843		•	•			3 & LSI	
Inverting	9-Bit	3-State	'844		•	•			3 & LSI	
True	10-Bit	3-State	'841		•	•				
Inverting	10-Bit	3-State	'842		•	•				
True	Octal	3-State	'29845		•	•				
Inverting	Octal	3-State	'29846		•	•			ĺ	
True	9-Bit	3-State	'29843		•	•			3	
Inverting	9-Bit	3-State	'29844		. •	•] 3	
True	10-Bit	3:State	'29841		•	•				
Inverting	10-Bit	3-State	129842		•	•			1	

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

		1						
DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	s	L	VOLUME
Single	'121	•					•	
Dual	'221	•			•			

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REGISTERS

SHIFT REGISTERS

	NO.	Ī	мо	DES	-	T	Γ	TE	CHNC	LOG	Υ		
DESCRIPTION	OF	S.B	_	LOAD	НОГР	TYPE	STD	ALS	AS	Γ.	LS	s	
	BITS	ò	S.L	é	오		TTL	ALS	AS	L	LS	S	VOLUME
Sign-Protected		Х		Х	х	'322					А		
		Х	Х	Х	х	198	•						2
Parallel-In		×	×	x	×	'299					•	•	
Parallel-Out	8	Ĺ	Ľ	L	Ĺ	235		•	•	Ĺ			3
		×	×	x	×	'323					•		2
Bidirectional		L^	<u> </u>	l^	_	323		•	•				3
Bioliectional	4	×	×	×	×	1194	•				Α	•	2
	1 *	1	^	^	^	194			•				3
Parallel-In,		×	×	x	x	1671						1	
Parallel-Out,	4	Ĺ	L^	L^	_	6/1			L		Ŀ	L	
Registered	4	×	х	×	x	1672		1	1		•		2
Outputs	<u> </u>	-	├-	<u> </u>	<u>_</u>				_		├	-	ļ
	8	×	1	X	×	1199	•		├		-	<u> </u>	
	5	×	<u> </u>	X		'96	•			•	•		
		×		×		195	A			•	В	_	2
			1_	┞_	<u></u>				A	L		—	3
Parallel-In,		X	<u> </u>	х	<u></u>	.99	L	ļ		•	<u> </u>	L	
Parallel-Out	ŀ	X	_	х	Х	1178	•					_	2
	4	X	L	X	Х	1179	•					_	
		×		x		195	•				А	•	2
	ļ	Ĺ		l^		100			A				3
	1	Х		х		'295					В		2
		Х		х		1395					Α		2
Serial-In	16	х	Γ	х	х	'673					•		2
Parallel-Out	8	x				164	•			•	•		l - '
raranei-Out	8	l ^				164		•					3
	16	Х	Г	х	х	'674					•	Г	
	ļ	T.,		1			•				A		2
Parallel-In,		×		X	×	1165							3
Serial-Out	8	Г	\vdash				•	 -			A		2
		×		×	х	1166		_	_	_		_	3
Serial-In.	8	×	\vdash	\vdash	_	'91	A	 - -	_	•	•	1	
Serial-Out	4	×	Н	×	_	194			_	 -		_	2

SHIFT REGISTERS WITH LATCHES

	NO.		T	TEC	HNOL	OGY					
DESCRIPTION	OF BITS	OUTPUTS	TYPE	ALS	AS	LS	VOLUME				
Parallel-in, Parallel-Out	4	3-State	'671			•					
with Output Latches	"	3-State	'672			•					
	16	2-State	'673			•					
Serial-In, Parallel-Out	8	Buffered	'594			•					
with Output Latches		3-State	1595			•					
		۰	۰	٥		ОС	1596			•	2
										ОС	'599
Parallel-In, Serial-Out,	8	2-State	'597			•					
with Input Latches	l °	3-State	'5ъ9			•					
Parallel I/O Ports with											
Input Latches, Multiplexed	8	3-State	'598			•					
Serial Inputs	i		1								

SIGN-PROTECTED REGISTERS

		NO.		мо	DES	3		TEC	HNOL	OGY	
	DESCRIPTION	OF BITS	S-R	S-L	LOAD	ногр	TYPE	ALS	AS	LS	VOLUME
1	Sign-Protected Register	8	Īχ		X	х	'322			Α	2

REGISTER FILES

			Т	ECHNO	DLOGY	1	
DESCRIPTION	ОИТРИТ	TYPE	STD TTL	ALS	AS	LS	VOLUME
8 Words × 2 Bits	3-State	172	•				
4.14.	OC	170	•			•	2
4 Words × 4 Bits	3-State	'670				•	
D -1 10 W -1 - 1 B	3-State	'870			•		0.0.10
Dual 16 Words x 4 Bits	3-State	'871			•		3 & LSI
64 Words × 40 Bits	3-State	'8834			A		LSI

OTHER REGISTERS

	T		TEC	HNOL	.og	/		
DESCRIPTION	TYPE	STD TTL	ALS	AS	L	LS	s	VOLUME
	.98				•			2
Quadruple Multiplexers	'298	•		•		•		3
with Storage	'398				•			
	'399				•			2
8-Bit Universal Shift Registers	'299		•	•		•	•	3
Quadruple Bus-Buffer Registers	173	•				А		2
Octal Storage Register	'396					•		1
Dual-Rank 8-Bit	'963		A					
Shift Registers	1964		•					3 & LSI
8-Bit Diagnostics/	'29818		•					
Pipeline Registers	'819		A					1

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COUNTERS

SYNCHRONOUS COUNTERS - POSITIVE-EDGE TRIGGERED

	PARALLEL			TECH	NOL	OGY			T
DESCRIPTION	LOAD	TYPE	STD TTL	ALS	AS	L	LS	s	VOLUME
	Sync	160	•				·A		2
	Sylic	100		В	•				3
	Sync	162	•				Α	•	2
Decade	Sync	102		В	•				3
Decade	Sync	'560		Α					3
	Sync	'668					•		
	Sync	'690					•		2
	Sync	'692					•		1 '
	Sync	1168					В	•	1
	Sync	108		В	•				3
		190	•				•		. 2
	Async	190		•					3
Decade Up/Down	Async	1192	•			•	•		2
	Async	192		•					3
	Sync	'568		Α] 3
	Sync	'696					•		
	Sync	'698					•		1
Decade Rate 1	Async	167							2
Multipler, N10	Set-to-9	167	•						
		161	•				Α		
	Sync	161		В	•				. 3
		163	•				Α	•	2
4 Die Die ee	Sync	163		В	•				3
4-Bit Binary	Sync	'561		Α					3
	Sync	'669					•		
	Sync	'691					•		
	Sync	'693					•		2
							В	•	
	Sync	1169		В	•				3
		(101	•				•		2
4 Die Dinner	Async	1191		•					3
4-Bit Binary		(100	•			•	•		2
Up/Down	Async	193		•					_
	Sync	'569		Α					3
	Sync	'697			_		•		
	Sync	'699					•		_
6-Bit Binary 1 Rate Multipler, N2		'97	•						2
	Async CLR	'867			•	-		-	
8-Bit Up/Down	Sync CLR	'869		-	•			-	3 & LSI
	J SYNG CEN	009						Ц	

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) - NEGATIVE-EDGE TRIGGERED

	PARALLEL			TECH	NOL	OGY			
DESCRIPTION	LOAD	TYPE	STD TTL	ALS	AS	L	LS	s	VOLUME
	Set-to-9	'90	Α			•	•		
		'68					•		1
Decade	Yes	176	•		I			Г] .
	Yes	1196	•				•	•	
	Set-to-9	'290	•				•		i
	None	'93	Α			•	•]
		′69					•		2
4-Bit Binary	Yes	177	•						1 ′
	Yes	'197	•				•	•	l
	None	′293	•				•		1
Divide-by-12	None	'92	Α				•		1
Dual Decade	None	'390	•				•		1
Duar Decade	Set-to-9	'490	•				•		1
Dual 4-Bit Binary	None	'393	•				•		

8-BIT BINARY COUNTERS WITH REGISTERS

	TYPE		TECH	INOL		
DESCRIPTION	OF OUTPUT	TYPE	ALS	AS	LS	VOLUME
Parallel Register	3-State	'590			•	
Outputs	oc	'591	<u> </u>		•	1 .
Parallel Register Inputs	2-State	'592			•	2
Parallel I/O	3-State	'593			•	1

FREQUENCY DIVIDERS, RATE MULTIPLIERS

		TECHNOLOGY						
DESCRIPTION	TYPE	STD TTL	ALS	AS	LS	VOLUME		
50-to-1 Frequency Divider	156		T		•			
60-to-1 Frequency Divider	'57				•	1 .		
60-Bit Binary Rate Multiplier	'97	•	1			2		
Decade Rate Multiplier	167	•	1		1	1		

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DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

	TYPE			TE	CHNC	LOG	Y		
DESCRIPTION	OF	TYPE	STD	ALS	AS	L	LS	s	VOLUME
	ОИТРИТ		TTL	ALS	AS	١.	LS	S	
	2-State	150	•						2
101	3-State	'250			•				
16-to-1	3-State	'850			•				3 & LSI
	3-State	'851			•				1
Dual 8-to-1	-3-State	'351	•						
	2-State	151	A				•	•	2
	2-State	1151		•	•				3
	2-State	152	Α				•		_
	0.0	1054	•				•	•	2
8-to-1	3-State	'251		•	•				3
	3-State	'354					•		
	2-State	'355					•		
	3-State	'356					•	Г	2
	ос	'357					•		
			•			•	•	•	
	2-State	153		•	•				3
							•	•	2
	3-State	′253		•	•				3
Dual 4-to-1							•		2
	2-State	′352		•	•				3
	3-State				_		•		2
		'353		•	Α				3
	3-State	'604					•		
	ос	'605					•		
Octal 2-to-1 with Storage	3-State	'606					•		2
	oc	'607					•		
	2-State	'98				•			
			•				•		2
Quad 2-to-1 with Storage	2-State	'298			•	_			3
	2-State	'398					•		
	2-State	'399					•		2
			•			•	•	•	
	2-State	1157		•	•				3
					_		•	•	2
	2-State	1158		•	•				3
Quad 2-to-1							В	•	2
	3-State	'257		A	•				3
							В	•	2
	3-State	'258		A	•	_	Ť	1	3
6-to-1 Universal Multiplexer	3-State	'857		•	•				3

DECODERS/DEMULTIPLEXERS

	TYPE			TE	CHNC	LOC	Y		
DESCRIPTION	OF OUTPUT	TYPE	STD TTL	ALS	AS	L	LS	s	VOLUME
4-to-16	3-State	1154	•			•			
4-10-10	ОС	1159	•						
4-to-10 BCD-to-Decimal	2-State	'42	Α			•	•		1
4-to-10 Excess 3-to- Decimal	2-State	'43	Α			•			2
4-to-10 Excess 3-Gray- to-Decimal	2-State	'44	А			•			
3-to-8 with Address		131		•	Α				3
Latches	2-State	137		•	•				
			L	L	L		•		2
	2-State	1138		•	•		l		3
3-to-8	2-31816	130					•	•	. 2
	2-State	139		•	•				3
	2-State	139					Α	•	
Dual 2-to-4	2-State	1155	•				Α		2
	ОС	1156	•				•		1

CODE CONVERTERS

		TECHNO	LOGY	
DESCRIPTION	TYPE	STD	s	VOLUME
6-Line-BCD to 6-Line Binary, or 4-Line to 4-Line BCD 9's/BCD 10's Converters	184	•		2
6-Bit-Binary to 6-Bit BCD Converters	'185	Α		1
BCD-to-Binary Converters	'484		Α	
Binary-to-BCD Converters	'485		Α	7 4

PRIORITY ENCODERS/REGISTERS

		Т	ECHN	OLOG	Y	
DESCRIPTIÓN	TYPE	STD	ALS	AS	LS	VOLUME
Full BCD	'147	•			•	
Cascadable Octal	1148	•			•	1 .
Cascadable Octal with 3-State Outputs	'348				•	2
4-Bit Cascadable with Registers	'278	•				1

SHIFTERS

				TECHNOLOGY					
DESCRIPTION	OUTPUT	TYPE	STD TTL	ALS	AS	L	LS	s	VOLUME
4-Bit Shifter	3-State	'350						•	2
Parallel 16-Bit Multi-Mode Barrel Shifter	3-State	'897			•				LSI
32-Bit Barrel Shifter	3-State	'8838			•				

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DISPLAY DECODERS/DRIVERS, MEMODRY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

	OFF-STATE			TECHI	NOLO	GY		
DESCRIPTION	OUTPUT	TYPE	STD		AS		LS	VOLUME
	VOLTAGE	1	TTL	ALS	AS	L	LS	ļ
	30 V	'45	•					
DOD to Destroit	60 V	1141	•					
BCD-to-Decimal	15 V	1145	•				•	1
	7 V	'445					•	1
	30 V	'46	Α			•		
	15 V	'47	Α			•	•	Ì
	5.5 V	'48	•				•	1 .
	5.5 V	'49	•				•	2
000 0 0	30 V	'246	•					i
BCD-to-Seven-Segment	15 V	'247	•				•	1
	7 V	'347					•	1
	7 V	'447					•	1
	5.5 V	'248	•				•	1
	5.5 V	'249	•				•	1

MEMORY/MICROPROCESSOR CONTROLLERS

	DECODINE		TYPE	TE	CHN	LOG	Υ	VOLUME
	DESCRIPTION		ITPE	ALS	AS	LS	s	VOLUME
System Cont	trollers (Universal	or for '888)	'890		•			LSI
	Transparent,	4K, 16K	'600			Α		
Memory	Burst Modes	64K	'601			Α		
Refresh Controllers Cycle Steal,		4K, 16K	'602			А		2
Controllers	Burst Modes	64K	'603			Α		1
Memory Cyc	le Controller		'608			•		1
	M M		'612			•		
Memory Mag	ppers	ОС	'613			•		
Memory May	ppers	3-State	'610			•		LSI
with Output	Latches	ос	'611			•		
Multi-Mode I	Latches (8080A A	Applications)	'412				•	2
		16K, 64K,	2967	A				
Durania Ma			′2968	•				LSI
Dynamic Me	ynamic Memory Controllers	16K, 64K	'6301	•				LSI
		256K, 1 MEG	'6302	A				

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

		TECH			
DESCRIPTION	TYPE	STD	ALS	AS	VOLUME
BCD Counter/4-Bit Latch/BCD-to-Decimal Decoder/Driver	142	•			
BCD Counter/4-Bit				-	
Latch/BCD-to-Seven-Segment	143				2
Decoder/LED Driver	140				-
BCD Counter/4-Bit				ļ	
Latch/BCD-to-Seven-Segment Decoder/Lamp Driver	1144	•			

CLOCK GENERATOR CIRCUITS

		Ĺ	TECH	NOL	OGY		
DESCRIPTION	TYPE	STD	ALS	AS	LS	s	VOLUME
Quadruple Complementary-Output Logic Elements	'265	•					
Dual Pulse Synchronizers/Drivers	'120	•					1
C	'320				•] ,
Crystal-Controlled Oscillators	'321				•	T	1 2
Digital Phase-Lock Loop	'297				•		1
Programmable Frequency	'292				•		1
Dividers/Digital Timers	'294				•		1
Dual VCO	124	T		Г			2

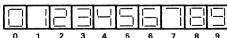
VOLTAGE-CONTROLLED OSCILLATORS

		DESCRI	TION				TECHNO	LOGY	
No. VCOs	COMP'L	ENABLE	RANGE INPUT	Rext	f _{max} MHz	TYPE	LS	s	VOLUME
Single	Yes	Yes	Yes	No	20	1624	•		
Single	Yes	Yes	Yes	Yes	20	'628	•		
Dual	No	Yes	Yes	No	60	1124		•	2
Dual	Yes	Yes	No	No	20	1626	•		2
Dual	No	No	No	No	20	'627	•		
Dual	No	Yes	Yes	No	20	'629	•		

RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '143, '144



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COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

	DE	SCRIPT	TION									
P = Q	P>Q	P <q< th=""><th>ОИТРИТ</th><th>OUTPUT ENABLE</th><th>TYPE</th><th>STD</th><th>ALS</th><th>AS</th><th>L</th><th>LS</th><th>s</th><th>VOLUME</th></q<>	ОИТРИТ	OUTPUT ENABLE	TYPE	STD	ALS	AS	L	LS	s	VOLUME
Yes	Yes	No	2-State	No	'85	•			•	•	•	2

8-BIT COMPARATORS

			DE	SCRIP	TION				TEC	HNOL	OGY	
INPUTS	P=Q	P=Q	P>Q	P>Q	P <q< th=""><th>оитрит</th><th>OUTPUT ENABLE</th><th>TYPE</th><th>ALS</th><th>AS</th><th>LS</th><th>VOLUME</th></q<>	оитрит	OUTPUT ENABLE	TYPE	ALS	AS	LS	VOLUME
	Yes	No	No	No	No	ос	Yes	'518	•			
20-kΩ	No	Yes	No	No	No	2-S	Yes	'520	•			3
Pull-Up	No	Yes	No	No	No	ос	Yes	1522	•			
ruii-Op	No	Yes	No	Yes	No	2·S	No	'682		•	2	
	No	Yes	No	Yes	No	ос	No	'683			•	2
	Yes	No	No	No	No	ос	Yes	1519	•			3
	No	Yes	No	No	No	2-S	Yes	1521	•			3
	No	Yes	No	Yes	No	2-S	No	'684			•	
	No	Yes	No	Yes	No	ос	No	1685			•	
Standard	No	Yes	No	Yes	No	2-S	Yes	'686			•	. 2
Standard	No	Yes	No	Yes	No	ос	Yes	'687			•	
	No	Yes	No	No	No	2-S	Yes	'688	•			3
											٠	2
	No	Yes	No	No	No	ос	Yes	689	•			3
											•	2
Latched P Logic & Arith	No	No	Yes	No	Yes	2-S	Yes	'885		•		3 & LSI
Latched P&Q Logic & Arith	Yes	No	Yes	No	Yes	Latched	Yes	'866		•		3

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT	LATCHED	TYPE	TECHNOLOGY		
DESCRIPTION	ENABLE	OUTPUT	1176	ALS	AS	VOLUME
10.00 1.00	Yes		'677	•		
16-Bit to 4-Bit		Yes	'678	•		1 .
10 Division 4 Div	Yes		'679	•		3
12-Bit to 4-Bit		Yes	'680	•		1

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

		NO.		Т	ECHNO	OLOG	Υ			
DESCRIPTION		OF BITS	TYPE	STD TTL	ALS	AS	LS	s	VOLUME	
		8	1180	•					2	
Odd/Even Parity Generators/Checkers		9	'280		•	•	•	•	3 & LSI	
		9	'286			•			3 & LSI	
	3-State	8	'636				•		2	
	ос	8	'637				•			
	3-State	16	'616		•				3 & LSI	
	oc	16	'617		A				3 & L31	
Parallel Error	3-State	16	'630				•		2	
Detection/Correction	ОС	16	'631				•			
Circuits	3-State	16	'8400		A				LSI	
	3-State	32	'632		Α	•				
	oc	32	'633		A	•			3 & LSI	
	3-State	32	'634		•	•] 3 01 L31	
	ОС	32	'635		A	•				

FUSE-PROGRAMMABLE COMPARATORS

			TECHN				
DESCRIPTION	TYPE	STD	ALS	AS	LS	s	VOLUME
16-Bit Identity Comparator	'526		•				
12-Bit identity Comparator	'528		•				3
8-Bit Identity Comparator	'527						3
and 4-Bit Comparator	527		1				

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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

						TECHNOLOGY						
DESCRIPTION	TYPE	STD	ALS	AS	н	LS	s	VOLUME				
1-Bit Gated	'80	•			Г							
2-Bit	'82	•			Г							
4-Bit	'83	Α				Α		2				
4-DII	'283	•	1			•	•	1				
Dual 1-Bit Carry-Save	1183				•	•						

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

				TECH	VOLC	GY		
DESCRIPTION		TYPE	STD TTL	ALS	AS	LS	s	VOLUME
4-Bit Parallel Binary Accumulators		'281					•	
4-Bit Parallel Binary	Accumulators	'681				•		2
		181	•			•	•	1
		181			Α			3 & LSI
4-Bit Arithmetic Logic Units/ Function Generators		-11181			•			3 & L31
		1004				Α		2
		'381					•	2
		'881			Α			3 & LSI
4-Bit Arithmetic Log with Ripple Carry	gic Unit	'382				•		2
		44.00	•				•	2
Look-Ahead Carry	16-Bit	1182						
Generators		'282			A			3
	32-Bit	'882			Α			3 & LSI
Quad Serial Adder/S	Subtractor	'385				•		2

MULTIPLIERS

DESCRIPTION							
DESCRIPTION	TYPE	STD	ALS	AS	LS	s	VOLUME
2-Bit-by-4-Bit Parallel Binary Multipliers	'261			Г	•	Г	
	'284	•					
4-Bit-by-4-Bit Parallel Binary Multipliers	'285	•				1	2
25-MHz 6-Bit Binary Rate Multipliers	'97	•					
25-MHz Decade Rate Multipliers	1167	•		,			
8-Bit × 1-Bit 2's Complement Multipliers	'384				•	Г	

OTHER ARITHMETIC OPERATORS

			TE	CHNC	LOG	Υ			
DESCRIPTION	TYPE	STD TTL	ALS	AS	н	L	LS	s	VOLUME
Quad 2-Input Exclusive-OR	′86	•				•	Α	•	2
Gates with Totem-Pole	.00		•						3
Outputs	'386						Α		
Quad 2-Input Exclusive-OR									2
Gates with Open-Collector	1136				<u> </u>			_	
Outputs	l		•						3
Quad 2-Input Exclusive-	'266						•		2
NOR Gates	'810		•	A					3
Quad 2-Input Exclusive-NOR					1				
Gates with Open-Collector	'811		•			f		i	3
Outputs	1			l					
Quad Exclusive OR/NOR	135								
Gates	135			1	1	1		•	2
4-Bit True/Complement	'87			Г		Г			′
Element	87			L	Ľ	L	L	<u> </u>	

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

	CASCADABLE			TECH	NOLO	GY	
DESCRIPTION	TO N-BITS	TYPE	ALS	AS	LS	s	VOLUME
	No	'887		•		-	
8-Bit Slice	Yes	'888		•			LSI
	Yes	'895		•		Г	

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INTERFACE ALS CIRCUITS

All type numbers on this page refer to devices in the SN55ALS and SN75ALS families.

IBM 360/370 I/O LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Quadruple Line Driver	′126	•	ALS/AS
Quadruple Line Driver	1130	•	ALS/AS

IEEE-488 (GPIB) INTERFACE BUS TRANSCEIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
	1160	A	
	1161	A	
Octal Transceiver	1162	A	ALS/AS
Octal Transceiver	'163	A	ALS/AS
	1164	A	
	1165	A	

RS-422-A, RS-423-A, AND RS-485 LINE RECEIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Quad Differential with 3-State Outputs	193	•	ALS/AS
Quad Differential with 3-State Outputs (TTL Comp.)	195	•	ALS/AS

RS-422-A LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY ALS	VOLUME
Quad Differential	1192	•	ALS/AS
Quad Differential with 3-State Outputs	194	•	ALS/AS

- Denotes available technology.
- ▲ Denotes planned new products.



MEMORIES

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROMs) STANDARD PROMs

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	s	VOLUME
	TBP28S166	2048W × 8B	3-State	•	
	TBP38S165	2048W × 8B	3-State	•	
	TBP38S166	2048W × 8B	3-State	•	
16K-Bit Arrays	TBP38SA165	2048W × 8B	ос	•	
	TBP38SA166	2048W × 8B	oc	•	
	TBP34S162	4096W × 4B	3-State	•	
	TBP34SA162 .	4096W × 4B	oc .	▲	
	TBP24S81	2048W × 4B	3-State	•	
	TBP24SA81	2048W × 4B	oc		
	TBP28S85A	1024W × 8B	3-State		
	TBP28S86A	1024W × 8B	3-State	•	
8K-Bit Arrays	TBP28SA86A	1024W × 8B	ос	•	
	TBP38S85	1024W × 8B	3-State		
	TBP38S86	1024W × 8B	3-State		
	TBP38SA85	1024W × 8B	oc		
	TBP38SA86	1024W × 8B	oc		4
	TBP24S41	1024W × 4B	3-State	•	
	TBP24SA41	1024W × 4B	oc	•	
4K-Bit Arrays	TBP28S42	512W × 8B	3-State	•	
4K-Bit Arrays	TBP28SA42	512W × 8B	oc	•	
	TBP28S46	512W × 8B	3-State	•	
	TBP28SA46	512W × 8B	oc	•	
2K-Bit Arrays	TBP38S22	256W × 8B	3-State	•	,
ZK-Bit Allays	TBP38SA22	256W × 8B	oc	•	
	TBP24S10	256W × 4B	3-State	•	
1K-Bit Arrays	TBP24SA10	256W × 4B	oc	•	
IN-DIL Allays	TBP34S10	256W × 4B	3-State	•	
	TBP34SA10	256W × 4B	oc	•	
	TBP18S030	32W × 8B	3-State	•	
256-Bit Arrays	TBP18SA030	32W × 8B	oc	•	
230-Dit Alldys	TBP38S030	32W × 8B	3-State	•	
	TBP38SA030	32W × 8B	ос	•	

LOW-POWER PROMs

. DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	s	VOLUME
	TBP28L166	2048W × 8B	3-State	•	
16K-Bit Arrays	TBP38L165	2048W × 8B	3-State	•	
TOK-DIT Arrays	TBP38L166	2048W × 8B	3-State	•	
	TBP34L162	4096W × 4B.	3-State	A	
OK Die A	TBP28L85A	1024W × 8B	3-State	•	
	TBP28L86A	1024W × 8B	3-State	•	
8K-Bit Arrays	TBP38L85 .	1024W × 8B	3-State	A	
	TBP38L86	1024W × 8B	3-State	•	4
AK Dis A	TBP28L42	512W × 8B	3-State	•	
4K-Bit Arrays	TBP28L46	512W × 8B	3-State	•	
	TBP28L22	256W × 8B	3-State	•	
2K-Bit Arrays	TBP28LA22	256W × 8B	oc	•	
	TBP38L22	256W × 8B	3-State	•	
1K-Bit Arrays	TBP34L10	256W × 4B	3-State	•	
256-Bit Arrays	TBP38L030	32W × 8B	3-State	•	

REGISTERED PROMs

DESCRIPTION	ТҮРЕ	ORGANIZATION	TYPE	s	VOLUME
	TBP34R162	4096W × 4B	3-State	•	
16K-Blt Arrays	TBP34SR165	4096W × 4B	3-State	•	4
	TBP38R165	2048W × 8B	3-State	•	

RANDOM-ACCESS READ-WRITE MEMORIES (RAMs)

		TYPE			TECHI	NOLO	GY			
DESCRIPTION	ORGANIZATION	OF OUTPUT	TYPE	STD TTL	ALS	AS	LS	s	VOLUME	
250 04 4	256 × 1	3-State	'201					•		
256-Bit Arrays		ос	'301					•].	
64-Bit Arrays		ос	'89	•	-					
		3-State	1189				А	В	4	
	16 × 4	3-State	'219				Α			
		OC	'289				Α	В		
		ос	'319				Α		1	
16-Bit Multiple-Port Register File	8 × 2	3-State	'172	•						
		oc .	'170	•			•		2	
16-Bit Register File	4 × 4	3-State	'670				•	T	1	
Dual 64-Bit			'870			•				
Register Files	16 × 4	3-State	'871			•			3	

FIRST-IN FIRST-OUT MEMORIES (FIFOs)

	TYPE		TECHNOLOGY			Υ		
DESCRIPTION	OF OUTPUT	TYPE	ALS	AS	LS	s	VOLUME	
	3-State	222			•			
16 × 4	3-State	224			•		1	
	3-State	227			•		LSI	
	- 3-State	228			•			
	3-State	232	Α				3 & LSI	
***************************************	3-State	225			•	•	LSI	
16 × 5	3-State	229	Α					
	- 3-State	233	Α				3 & LSI	

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PROGRAMMABLE LOGIC ARRAYS

PROGRAMMABLE LOGIC ARRAYS

		JIMIN	ABLE LOGI	C Anna 13			
DESCRIPTION	INPUTS		OUTPUTS	TYPE	ALS	NO. OF	VOLUME
		NO.	TYPE	NO		PINS	
		8	Active-Low	'PAL16L8A	•		
High-Performance PAL*	16	4		'PAL16R4A	•	20	
riigii r ciromianee r AE		6	Registered	'PAL16R6A	•		
		8		'PAL16R8A	•		
		8	Active-Low	'PAL16L8A-2	•		
Half-Power PAL*	16	4		'PAL16R4A-2	•	20	
Half-Power PAL	16	-6	Registered	'PAL16R6A-2	•	20	i
		8		'PAL16R8A-2	•		
		8	Active-Low	'PAL20L8A	•		
		4		'PAL20R4A	•		
High-Performance PAL*	20	6	Registered	'PAL20R6A	•	24	
		8	1	'PAL20R8A			
		8	Active-Low	PAL20LBA-2	•		
		4	ACTIVE-LOW	'PAL20R4A-2	÷	-	
Half-Power PAL	20	6	Desistant	'PAL2OR6A-2		24	
		8	Registered	h	÷		
				'PAL20R8A-2	-		
		8	Active-Low	TIBPAL16L8-12	•		
Impact PAL*	16	4		'TIBPAL16R4-12	•	20	
		6	Registered	'TIBPAL16R6-12	•		
		8		'TIBPAL16R8-12	•		
		8	Active-Low	'TIBPAL16L8-15	•		
Impact PAL*	16	4		TIBPAL16R4-15	•	20	
Impact PAL	10	6	Registered	'TIBPAL16R6-15	•	20	
		8		'TIBPAL16R8-15	•		
		8	Active-Low	'TIBPAL20L8-15	•	•	
		4		'TIBPAL20R4-15	•		
Impact PAL*	20	6	Registered	'TIBPAL20R6-15	•	24	
		8	1 "	'TIBPAL2OR8-15	•		
		10	Active-Low	'TIBPAL20L10-20			
		4	ACTIVE LOW	TIBPAL20X4-20			
Exclusive-OR PAL*	20	8	Registered	TIBPAL20X8-20	-	24	4
		10	negistered				4
				TIBPAL20X10-20			
		8	Active-Low	TIBPAL20L10-35			
Exclusive-OR PAL*	20	4		TIBPAL20X4-35	•	24	
		8	Registered	'TIBPAL20X8-35	•		
		10		TIBPAL20X10-35	•		
		8	Active-Low	'TIBPALR19L8-25	•		
Registered-Input PAL*	19	4		TIBPALR19R4-25	•	24	
negistereo-input r.A.c.	13	6	Registered	TIBPALR19R6-25	•	24	
		8		'TIBPALR19R8-25	•		
		8	Active-Low	TIBPALR19L8-40	•		
		4		'TIBPALR19R4-40	•		
Registered-Input PAL*	19	6	Registered	'TIBPALR19R6-40	•	24	
		8	1 "	TIBPALR19R8-40	•		
		8	Active-Low	TIBPALT19L8-25			
		4	ACTIVE-EUW	'TIBPALT1984-25	•		
Latched-Input PAL*	19	- 6	Pagistors		\cdot	24	
			Registered	TIBPALT19R6-25			
		8		TIBPALT19R8-25	•		
		8	Active-Low	TIBPALT19L8-40	•		
Latched-Input PAL*	19	4		TIBPALT19R4-40	•	24	
		6	Registered	'TIBPALT19R6-40	•		
		8		TIBPALT19R8-40	•		
Field-Programmable	14	6	3-State	TIFPLA839	•	24	
14 × 32 × 6 Logic Arrays	14		oc	TIFPLA840	•	24	

^{*} PAL is a registered trademark of Monolithic Memories Incorporated.

Denotes available technology.



General Information

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SN54ALSOOA, SN54ASOO, SN74ALSOOA, SN74ASOO QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

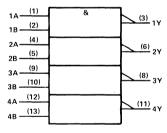
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS00A and SN74AS00 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	INP	JTS	OUTPUT
Г	Α	В	Y
Γ	Н	Н	L
ļ	L	Χ	н
	Х	L	Н

logic symbol†



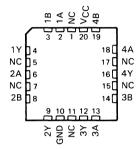
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

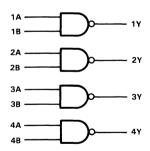
SN54ALS00A, SN54AS00 . . . J PACKAGE SN74ALS00A, SN74AS00 . . . D OR N PACKAGE (TOP VIEW)

1A 🗌	1	U14 VCC
1B 🗌	2	13 4B
1 Y 🗌	3	12 🗌 4A
2A 🗌	4	11 🔲 4Y
2B 🗌	5	10 🔲 3B
2Y 🗌	6	9∏ 3A
GND [7	8 🗌 3Y

SN54ALS00A, SN54AS00, . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



recommended operating conditions

		SN	SN54ALS00A			SN74ALS00A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Іон	High-level output current			-0.4			-0.4	mA	
lOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMP.	TIONO	SI	154ALS	AOO	SN74ALS00A			LINUT
PARAMETER	TEST COND	TEST CONDITIONS			MAX	MIN	TYP [†]	MAX	UNIT
· V _{IK}	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		Vcc-	- 2		V
V	$V_{CC} = 4.5 V$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V,	I _{OL} = 8 mA				0.35		0.5]
lį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_1 = 2.7 \text{ V}$			20			20	μΑ
lir	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	· mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.5	0.85		0.5	0.85	mA
CCL	V _{CC} = 5.5 V,	V _I = 4.5 V		1.5	3		1.5	3	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX				
	1 1		'ALSOOA	SN54	SN54ALS00A		SN74ALS00A		
			TYP	MIN	MAX	MIN	MAX		
tPLH	A or B	Υ	7	3	16	3	11		
tPHL	A or B	Y	5	2	13	2	8	ns	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ASOO, SN74ASOO QUADRUPLE 2-INPUT POSITIVE-NAND GATES

absolute maximum ratings over opera	ting free-air	temperature rang	je (unless otherw	ise noted)
Supply voltage, VCC				7 V
Input voltage				7 V
Operating free-air temperature range	: SN54ASOC)		55°C to 125°C
	SN74ASOC)		. 0°C to 70°C
Storage temperature range			0	65°C to 150°C

recommended operating conditions

,		S	SN54AS00		SI	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 2			- 2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN54AS00			SI			
PARAMETER			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
VOH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -	2		Vcc-	2		V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
l _l	$V_{CC} = 5.5 V,$	V _j = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
tj <u>L</u>	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
ССН	$V_{CC} = 5.5 V,$	V _I = 0 V		2	3.2		2	3.2	mA
Icci	V _{CC} = 5.5 V,	$V_1 = 4.5 \text{ V}$		10.8	17.4		10.8	17.4	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ p}$ $R_L = 50 \Omega$ $T_A = MIN$	F,	ν,	UNIT
	(1147-01)	(001/01/	SN54	4AS00	SN7	4AS00]
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	Υ	1	5	1	4.5	ns
tPHL	A or B	Y	1	5	1	4	1115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALSO1, SN74ALSO1 QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

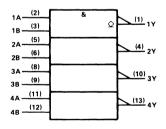
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y=\overline{A}\cdot\overline{B}$ or $Y=\overline{A}+\overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALSO1 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALSO1 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

ſ	INP	UTS	OUTPUT
	Α	В	Y
	н н		L
1	L	Х	н
1	Х	L	н

logic symbol†



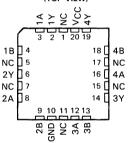
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

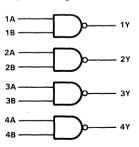
SN54ALS01 . . . J PACKAGE SN74ALS01 . . . D OR N PACKAGE (TOP VIEW)

1Y [1	U 14	□vcc
1A [2	13] 4Y
1B []3	12] 4B
2Y [4	11] 4A
2A [5	10] 3Y
2B [_ 6	9] 3B
GND [7	8] 3A

SN54ALS01 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





Supply voltage, VCC
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54ALS01
SN74ALS01
Storage temperature range

recommended operating conditions

			SN54ALS01			SN74ALS01			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	٧	
Voн	High-level output voltage			5.5			5.5	٧	
lOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS01			SI	UNIT		
PARAMETER	TEST C	ONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
ViK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			- 1.5	٧
Іон	$V_{CC} = 4.5 V$	V _{OH} = 5.5 V			0.1			0.1	mA
V	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 8 mA					0.35	0.5	\ \
I _I	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ήн	$V_{CC} = 5.5 V$,	V ₁ = 2.7 V			20			20	μΑ
Iμ	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
Іссн	$V_{CC} = 5.5 V$,	V _I = 0 V		0.43	0.85		0.43	0.85	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		1.62	3		1.62	3	mA

 $^{^{\}dagger}AII$ typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 2 k T _A = MI	Ω,	V,	UNIT
			SN54ALS01		SN74ALS01		
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	23	66	23	54	ns
t _{PHL}	A or B	Y	8	39	8	28	ns



SN54ALSO2, SN54ASO2, SN74ALSO2, SN74ASO2 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

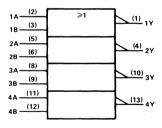
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS02 and SN54AS02 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS02 and SN74AS02 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

INI	PUTS	OUTPUT
Α	В	Υ
Н	X	L
Х	Н	L
L	L	Н

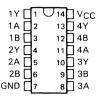
logic symbol†



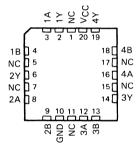
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

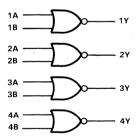
SN54ALS02, SN54AS02 . . . J PACKAGE SN74ALS02, SN74AS02 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS02, SN54AS02 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





Supply voltage, VCC	7 V
Operating free-air temperature range: SN54ALS02	-55°C to 125°C
SN74ALS02	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		S	SN54ALS02			SN74ALS02		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон	High-level output current			-0.4			-0.4	mA
loL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	TEST CONDITIONS		N54ALS	02	SI	174ALS	02	UNIT
T ANAMETER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
VoH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -2			V
VOL	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5	V
l _i	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
¹ ІН	$V_{CC} = 5.5 \text{ V},$	$V_1 = 2.7 \text{ V}$			20			20	μΑ
İIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		- 112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.86	2.2		0.86	2.2	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		2.16	4		2.16	4	mΑ

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 1)

			V _{CC} = 5 V,		V _{CC} = 4.5	V to 5.5 \	1,	
			$C_L = 50 pF$,	1	$C_L = 50 pt$	F,		Ì
PARAMETER	FROM	TO	$R_L = 500 \Omega$,	R _L =		= 500 Ω,		
PANAMETER	(INPUT)	(OUTPUT)	T _A = 25°C		$T_A = MIN$	to MAX		UNIT
	1 1		'ALS02	SN54	SN54ALS02		ALS02	
	_		TYP	MIN	MAX	MIN	MAX	,
^t PLH	A or B	Υ	7 -	1	18	3	12	ns
tPHL ·	A or B	V	F	1	11	2	10] "'3



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ASO2, SN74ASO2 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

absolute maximum ratings over operati	ing free-air temperature range (unless othe	erwise noted)
, , , ,	SN54AS02	
Storage temperature range		-65°C to 150°C

recommended operating conditions

		S	SN54AS02			SN74AS02		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			- 2			- 2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	. 0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TECT COND	ITIONIC	S	N54AS	02	S	02	UNIT	
PARAMETER	TEST COND	ITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
V _{IK}	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
VoH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	Vcc-	2		V _{CC} -2	!		V
V _{OL}	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
l _l	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
ήL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.5	Ī		-0.5	mA
10 [‡]	$V_{CC} = 5.5 V,$	V _O ≈ 2.25 V	- 30		-112	- 30		-112	mA
Iссн	$V_{CC} = 5.5 V,$	V ₁ = 0 V		3.7	5.9	1.	3.7	5.9	mA
^I CCL	$V_{CC} = 5.5 \text{ V},$	V _I = 4.5 V		12.5	20.1		12.5	20.1	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ C}_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$		<i>'.</i>	UNIT	
			SN54	AS02	SN74	IAS02	
			MIN	MAX	MIN	MAX	
^t PLH	A or B	Y	1	5	1	4.5	
^t PHL	A or B	Y	1	5	1	4.5	ns

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS03B, SN74ALS03B QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

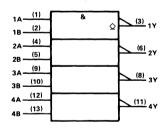
These devices contain four independent 2-input NAND buffers. They perform the Boolean functions $Y=\overline{A} * \overline{B}$ or $Y=\overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS03B is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS03B is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	INPL	ITS	OUTPUT
1	١	В	Υ
F	1	Н	L
L		Х	Н
>	(L	н

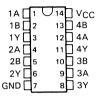
logic symbol†



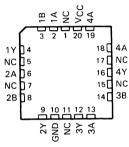
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

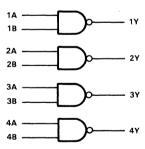
SN54ALS03B . . . J PACKAGE SN74ALS03B . . . D OR N PACKAGE (TOP VIEW)



SN54ALS03B . . . FK PACKAGE



NC-No internal connection





Supply voltage, VCC	· 	V
Input voltage		V
Off-state output voltage		V
Operating free-air temperature range:	SN54ALS03B55°C to 125°	С
	SN74ALS03B	С
Storage temperature range	65°C to 150°	С

recommended operating conditions

	,		SN54ALS03B			SN74ALS03B			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Vон	High-level output voltage			5.5			5.5	٧	
lOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETED	PARAMETER TEST CONDITIONS		SI	SN54ALS03B			SN74ALS03B		
PARAMETER	IESI CI	פאטו ווטאכ	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			- 1.5	V
- Гон	$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V			0.1			0.1	mA
Va.	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	1 _{OL} = 8 mA					0.35	0.5	ľ
7	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
^I ссн	V _{CC} = 5.5 V,	V ₁ = 0 V		0.43	0.85		0.43	0.85	mA
^I CCL	$V_{CC} = 5.5 V$,	V _I = 4.5 V		1.62	3		1.62	4	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 2 \text{ k}\Omega,$ $T_{A} = 25 \text{ °C}$		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 2 \text{ k}\Omega$, $T_A = \text{MIN}$	=,		UNIT
			'ALS03B	SN544	ALS03B	SN74	ALS03B	
1			TYP	MIN	MAX	MIN	MAX	
tPLH .	A or B	Y	35	20	59	20	50	nc
^t PHL	A or B	Y	8	3	23	3	13	ns



SN54ALS04B, SN54AS04, SN74ALS04B, SN74AS04 HEX INVERTERS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

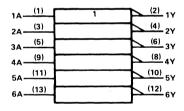
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS04B and SN54AS04 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS04B and SN74AS04 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each inverter)

INPUT	OUTPUT
Α	Y
Н	L
L	н

logic symbol[†]



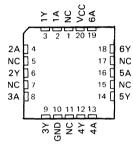
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

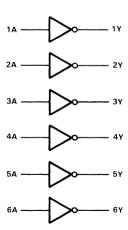
SN54ALS04B, SN54AS04 . . . J PACKAGE SN74ALS04B, SN74AS04 . . . D OR N PACKAGE (TOP VIEW)

1A 🛮 1	U 14	∐vcc
		6A
2A ☐ 3 2Y ☐ 4	12	∐6Y □5A
3AH	10	H ₅ Y
3Y 🗍 6		54A
GND 7	8	□4Y

SN54ALS04B, SN54AS04 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





Supply voltage, VCC	
Input voltage	7 V
Operating free-air temperature range	: SN54ALS04B 55 °C to 125 °C
, ,	SN74ALS04B
Storage temperature range	−65 °C to 150 °C

recommended operating conditions

		SI	SN54ALS04B		SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	ONIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
V _{IH}	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.7			0.8	V
Іон	High-level output current			-0.4			-0.4	mA
lor	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COND	TEST CONDITIONS M		54ALS)4B	SN	74ALS	04B	UNIT
PARAMETER	TEST CONDI			TYP†	MAX	MIN	TYP†	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	!		V
V	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	v
VOL	$V_{CC} = 4.5 V,$	IOL = 8 mA					0.35	0.5	\ \ \
1 ₁	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ίн	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
10‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.65	1.1		0.65	1.1	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		2.9	4.2		2.9	4.2	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω T_A = MIN to MAX			
			SN54	SN54ALS04B SN74ALS04B			
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Υ	3	14	3	11	ns
tPHL	Α	Υ .	2	12	2	8	ns



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IQS.

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise n	oted)
Supply voltage, VCC		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54AS0455°C	to 125°C
	SN74AS04	C to 70°C
Storage temperature range	_65°C	to 150°C

recommended operating conditions

		S	SN54AS04			SN74AS04			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			. 2			V	
VIL	Low-level input voltage			0.8			0.8	V	
lон	High-level output current			- 2			2	mA	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	-55		. 125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COND	TEST CONDITIONS		N54AS	04	S	UNIT		
PARAMETER	TEST COND	IIIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	ONL
Vik	$V_{CC} = 4.5 V,$	lj = −18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	lOH = −2 mA	Vcc-2	2		Vcc-	2		V
VOL	$V_{CC} = 4.5 V,$	IOL = 20 mA		0.35	0.5		0.35	0.5	V
l ₁	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
ИL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		3	4.8		3	4.8	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		14	26.3		14	26.3	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MI	Ο Ω,	V,	UNIT
			SN54	AS04	SN74	AS04	
			MIN	MAX	MIN	MAX	
tPLH	Α	Υ	1	6	1	5	ns
^t PHL	Α	Y	1	4.5	1	4	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS05A, SN74ALS05A HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher VOH levels.

The SN54ALS05A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS05A is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

logic symbol †

1A (1)	1 🛇	(2) 1Y
2A (3)		(4) 2Y
3A (5)		(6) 3Y
4A (9)		(8) 4Y
5A (11)		(10) 5Y
6A (13)		(12) 6Y

 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

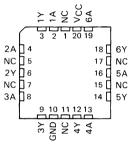
Pin numbers shown are for D, J, and N packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

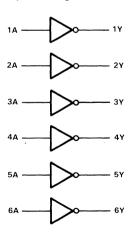
SN54ALS05A . . . J PACKAGE SN74ALS05A . . . D OR N PACKAGE (TOP VIEW)

1A 11 714 VCC 1Y **□**2 13 A 2A ∏3 12 T 6Y 2 Y 11 7 5A Π_4 3A П 10 □ 5Y 3Y П6 9 □ 4A GND 17

SN54ALS05A . . . FK PACKAGE



NC - No internal connection



recommended operating conditions

		SN	SN54ALS05A			SN74ALS05A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V _{IH}	High-level input voltage	. 2	· · · · · · · · · · · · · · · · · · ·		2			V	
V _{IL}	Low-level input voltage			0.7			0.8	٧	
Vон	High-level output voltage			5.5			5.5	V	
lor	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	SN54ALS05A			SN74ALS05A		
PARAMETER	IESI C	CNOTIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
ЮН	$V_{CC} = 4.5 V$	V _{OH} = 5.5 V			0.1			0.1	mA
	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	IOL = 8 mA					0.35	0.5	\ \ \
lį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ин	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
ΊL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			~0.1			-0.1	mA
Іссн	$V_{CC} = 5.5 V$,	V ₁ = 0 V		0.65	1.1		0.65	1.1	mA
^I CCL	$V_{CC} = 5.5 V$,	$V_{ } = 4.5 \text{ V}$		2.9	4.2		2.9	4.2	mA

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ ALSO5A	C _L R _L T _A	$V_{CC} = 4.5 \text{ V}$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to I}$ $SN54ALS05A$		ALS05A	UNIT
	1		TYP	MIN	MAX	MIN	MAX	
^t PLH	А	Y	45	23	84	23	54	ns
^t PHL	Α	Y	9	4	24	4	14	ns



SN54ALSO8, SN54ASO8, SN74ALSO8, SN74ASO8 QUADRUPLE 2-INPUT POSITIVE-AND GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

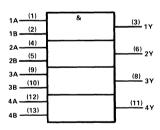
The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS08 and SN74AS08 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE

(each gate)

ſ	INP	JTS	OUTPUT
	Α	В	Y
Γ	Н	Н	Н
l	L	X	L
ı	X	L	L

logic symbol†



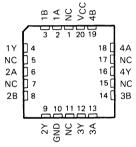
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

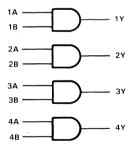
SN54ALS08, SN54AS08 . . . J PACKAGE SN74ALS08, SN74AS08 . . . D OR N PACKAGE (TOP VIEW)

1 A 🔲	1 U	14	Vcc
1B 🗌	2	13	4B
1Y 🔲	3	12	4A
2A 🗌	4	11	4Y
2B 🗌	5	10	3В
2Y 🗌	6	9	ЗА
GND 🗌	7	_8	3Y

SN54ALS08, SN54AS08 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



Supply voltage, VCC		
Input voltage		7 V
Operating free-air temperature range:	SN54ALS08	
	SN74ALS08	
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SI	SN54ALS08			SN74ALS08		
	·	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	mA
ЮН	High-level output current			-0.4			-0.4	mA
lOL	Lowlevel output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	N54ALS	08	Sf	V74ALS	80	UNIT
PANAIVIETEN	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _j = -18 mA			- 1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2					V
VOL	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5	ľ
lη	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ŀН	$V_{CC} = 5.5 V,$	V _I ≈ 2.7 V			20			20	μΑ
ΗL	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$	l .		-0.1			-0.1	mA
lo [‡]	$V_{CC} = .5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
ICCH	$V_{CC} = 5.5 V,$	V _I = 4.5 V		1.3	2.4		1.3	2.4	mA
ICCL	$V_{CC} = 5.5 V,$	$V_I = 0 V^*$		2.2	4		2.2	4	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		$C_L = 50 p$ $R_L = 500$	· ·			
			'ALS08	SN54ALS08 SN74ALS08		ALS08		
			TYP	MIN	MAX	MIN	MAX	١
^t PLH	A or B	Y	8	4	18	4	14	ns
^t PHL	A or B	Y	6.5	3	15	3	10	ns



[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ASO8, SN74ASO8 QUADRUPLE 2-INPUT POSITIVE AND GATES

${\bf absolute} \ \ {\bf maximum} \ \ {\bf ratings} \ \ {\bf over} \ \ {\bf operating} \ \ {\bf free-air} \ \ {\bf temperature} \ \ {\bf range} \ \ ({\bf unless} \ \ {\bf otherwise} \ \ {\bf noted})$

Supply voltage, VCC	7 V
Input voltage	
Operating free-air temperature range: SN54AS	08
SN74AS	08
Storage temperature range	-65°C to 150°C

recommended operating conditions

		s	SN54AS08			SN74AS08			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	mA	
Іон	High-level output current			-2			- 2	mA	
loL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	SN54AS08		SN74ASC	8	UNIT
PARAMETER	TEST CONDITIONS	MIN TYP† M	AX I	MIN TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$	-	1.2		-1.2	V
V _{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -2 \text{ mA}$	V _{CC} -2	\	/ _{CC} - 2		V
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 20 \text{ mA}$	0.35	0.5	0.35	0.5	V
l _l	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$		0.1		0.1	mA
lН	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$		20		20	μΑ
ηΓ	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$		0.5		-0.5	mA
10 [‡]	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$	- 30 - 1	12 -	- 30	-112	mA
Іссн	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 4.5 \text{ V}$	5.8	9.3	5.8	9.3	mA
ICCL	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0 \text{ V}$	14.9	24	14.9	24	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 50 \Omega,$ $T_A = \text{MIN to MAX}$ SN54AS08 SN74AS08				
			MIN	MAX	MIN	MAX		
^t PLH	A or B	Y	1	6.5	1	5.5	ns	
t _{PHL}	A or B	Y	1	6.5	1	5.5	ns	

[‡] The output conditions hav been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS09, SN74ALS09 QUADRUPLE 2 INPUT POSITIVE AND GATES WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

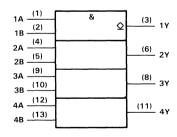
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher VOH levels.

The SN54ALS09 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS09 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Н
L	X	L
Х	L	l L

logic symbol†



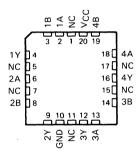
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

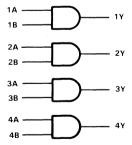
SN54ALS09 . . . J PACKAGE SN74ALS09 . . . D OR N PACKAGE (TOP VIEW)

1A [1	U 14	□ vcc
1B [2	13	☐ 4B
1 Y 🗌	3	12] 4A
2A 🗌	4	11	☐ 4Y
2B 🗌	5	10] 3B
2Y 🗀	6	9] 3A
BND [7	8] 3Y

SN54ALS09 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



SN54ALS09, SN74ALS09 QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 	7 V
Input voltage		 	7 V
Off-state output voltage		 	7 V
Operating free-air temperature range:	SN54ALS09	 	-55°C to 125°C
	SN74ALS09	 	0°C to 70°C
Storage temperature range		 	-65°C to 150°C

recommended operating conditions

			SN54ALS09			SI	UNIT		
		M	IN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4	.5	. 5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2		:	V
VIL	Low-level input voltage				0.7			0.8	V
VoH	High-level output voltage				5.5	,		5.5	V
lOL	Low-level output current				4			8	mA
TA	Operating free-air temperature		55.		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST COL	IDITIONO	S	N54ALS	09	SI	N74ALS	09	
PARAMETER	TEST COM	IDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_1 = -18 \text{ mA}$			- 1.5			- 1.5	V
loн	$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V			0.1			0.1	mA
VOL	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 8 \text{ mA}$,	0.35	0.5	1
lj lj	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
l _{IH}	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IJL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			- 0.1	mA
Iссн	$V_{CC} = 5.5 V$,	V _I = 4.5 V		1.35	2.4		1.35	2.4	mA
¹ CCL	$V_{CC} = 5.5 V$,	V _I = 0 V		2.2	4		2.2	4	mA

[.] † All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$\begin{array}{c} \text{V}_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, \\ \text{C}_L = 50 \text{ pF}, \\ \text{R}_L = 2 \text{ k}\Omega, \\ \text{T}_A = \text{MIN to MAX} \\ \\ \hline \text{SN54ALS09} & \text{SN74ALS09} \\ \hline \text{MIN} & \text{MAX} & \text{MIN} & \text{MAX} \end{array}$		ALS09	UNIT
			IVIIIV	WAX	MIIN	WAX	
^t PLH	A or B	Υ	20	69	23	54	ns
^t PHL	A or B	Υ	5	23	5	15	ns



SN54ALS10A, SN54AS10, SN74ALS10A, SN74AS10 TRIPLE 3-INPUT POSITIVE-NAND GATES

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

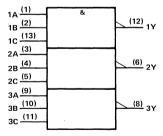
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS10A and SN54AS10 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS10A and SN74AS10 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	NPUTS	3	OUTPUT
Α	В	С	Y
Н	Н	I	L
L	Χ	Х	н
Χ	L	Х	Н
Х	Χ	L	н

logic symbol †



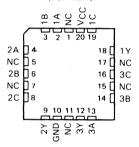
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

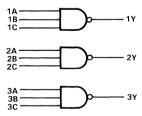
SN54ALS10A, SN54AS10 . . . J PACKAGE SN74ALS10A, SN74AS10 . . . D OR N PACKAGE (TOP VIEW)

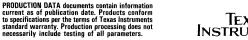
1 4 1	_	11.	h
1 A 🗌	1	O 14	□ v _{cc}
1B [2	13	1C
2A[3	12	1Y
2B 🗀	4	11	ЗС
2C[5	10	3в
2Y [6	9	∃за
GND[7	8]3Y

SN54ALS10A, SN54AS10 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54ALS10A
SN74ALS10A0°C to 70°C
Storage temperature range -65 °C to 150 °C

recommended operating conditions

		SN54ALS10A			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	CIVIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	٧
ЮН	High-level output current			-0.4			-0.4	mA
loL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	SN54ALS10A			SN74ALS10A		
PARAMETER			MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	VCC-2	2		Vcc-2	2		٧
V	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	IOL = 8 mA					0.35	0.5) v
lj .	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ίн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
Iссн	V _{CC} = 5.5 V,	V _I = 0 V		0.32	0.6		0.32	0.6	mA
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		1.2	2.2		1.2	2.2	mA

PARAMETER	FROM (INPUT)	TO (OUTPUT)				UNIT	
			MIN	MAX	MIN	MAX	1
tPLH	Any	Y	2	16	2	11	ns
tPHL	Any	Y	2	12	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{CS} .

SN54AS10, SN74AS10 TRIPLE 3-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage
Operating free-air temperature range: SN54AS10
SN74AS10
Storage temperature range -65 °C to 150 °C

recommended operating conditions

		S	SN54AS10			SN74AS10		
		MIN	MIN NOM MAX		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-2			-2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	TIONS	S	N54AS	10	S	UNIT		
PARAMETER	TEST CONDI	IIIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNII
VIK	V _{CC} = 4.5 V,	l _l = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	Vcc-2	2		VCC-2	2		V
VOL	V _{CC} = 4.5 V,	IOL = 20 mA		0.35	0.5		0.35	0.5	V
lį	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ήн	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 \text{ V}$			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.5			-0.5	mA
I _O ‡	V _{CC} = 5.5 V,	$V_0 = 2.25 V$	-30		-112	- 30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		1.5	2.4		1.5	2.4	mA
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		8.1	13		8.1	13	mA

PARAMETER	FROM (INPUT)	TO (OUTPUT)		UNIT			
			SN54AS10		SN74AS10		
			MIN	MAX	MIN	MAX]
t _{PLH}	Any	Υ	1	5	1	4.5	ns
^t PHL	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

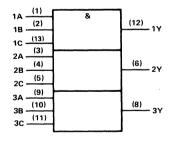
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + C}$ in positive logic.

The SN54ALS11A and SN54AS11 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74ALS11A and SN74AS11 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	NPUT	OUTPUT	
Α	В	С	Υ
Н	Н	Н	Н
L.	X	Х	L
Х	L	Х	L
Х	Х	L	L

logic symbol†

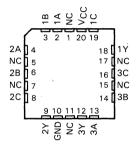


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

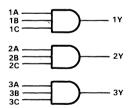
SN54ALS11A, SN54AS11 . . . J PACKAGE SN74ALS11A, SN74AS11 . . . D OR N PACKAGE (TOP VIEW)

1A[1	U 14	□∨cc
1B 🛚	2	13]1C
2A[3	12] 1Y
2B 🗌	4	11	Эзс
2C[5	10] 3B
2Y [6	9]3A
GND[7	8] 3Y

SN54ALS11A, SN54AS11 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection





Pin numbers shown are for D, J, and N packages.

Supply voltage, VCC		 	<u>.</u> 7 V
Input voltage		 	7 V
Operating free-air temperature range: SN	54ALS11A	 	– 55 °C to 125 °C
SN	74ALS11A	 	0 °C to 70 °C
Storage temperature range		 	65 °C to 150 °C

recommended operating conditions

		SI	SN54ALS11A			SN74ALS11A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	. 5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			-0.4			-0.4	mA	
lOL	Low-level output current			4			- 8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COND	TEST CONDITIONS		SN54ALS11A			SN74ALS11A		
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA		,	-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -0.4 mA	V _{CC} -2			V _{CC} -2			V
V	V _{CC} = 4.5 V,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
Vol	V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	
Ŋ	$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA
ин	V _{CC} = 5.5 V,	V ₁ = 2.7 V			20			20	μА
ΊL	V _{CC} = 5.5 V,	V ₁ = 0.4 V			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	- 30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		1	1.8		1	1.8	mA
¹ CCL	$V_{CC} = 5.5 V,$	V _I = 0 V		1.6	3		1.6	3	mA

PARAMETER	PARAMETER FROM (INPUT)			UNIT			
			SN54	ALS11A	SN744	LS11A	
			MIN	MAX	MIN	MAX	1
tPLH	Any	Y	2	17	2	13	ns
tPHL	Any	Y	2	14	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Supply voltage, V _{CC}	
Input voltage	
Operating free-air temperature range: SN54AS11	
SN74AS11	
Storage temperature range	- 65 °C to 150 °C

recommended operating conditions

		S	SN54AS11			SN74AS11			
1		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
ІОН	High-level output current			- 2			-2	mA	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		S	SN54AS11			SN74AS11		
			MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	l _j = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -2 mA	V _{CC} -2			V _{CC} -2			V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
lį	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΉΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
η <u>ι</u>	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
lo‡	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		4.3	7		4.3	7	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 0 V	,	11.2	18		11.2	18	mA

PARAMETER	FROM (INPUT)	TO (OUTPUT)		UNIT			
			SN54AS11		SN74AS11]
			MIN	MAX	MIN	MAX	
tPLH	Any	Y	1	6.5	1	6	ns
tPHL	Any	Y	1	6.5	1	5.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS12A, SN74ALS12A TRIPLE 3 INPUT POSITIVE NAND GATES WITH OPEN COLLECTOR OUTPUTS

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

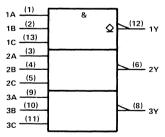
These devices contain three independent 3-input NAND gates with open-collector outputs. These gates perform the Boolean functions $Y=\overline{A\cdot B\cdot C}$ or $Y=\overline{A+B+C}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher VOH levels.

The SN54ALS12A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS12A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

ı	NPUTS	3	OUTPUT
Α	В	С	Y
Н	Н	Н	L
L	Χ	X	н
x	L	Х	Н
х	Χ	L	н

logic symbol[†]

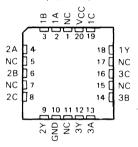


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

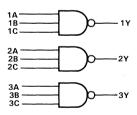
SN54ALS12A . . . J PACKAGE SN74ALS12A . . . D OR N PACKAGE (TOP VIEW)

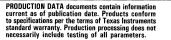


SN54ALS12A . . . FK PACKAGE (TOP VIEW)



NC No internal connection







Pin numbers shown are for D, J, and N packages.

 Off-state output voltage
 7 V

 Operating free-air temperature range:
 SN54ALS12A
 -55 °C to 125 °C

 SN74ALS12A
 0 °C to 70 °C

 Storage temperature range
 -65 °C to 150 °C

recommended operating conditions

1		SN	SN54ALS12A			SN74ALS12A		
1		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧ -
VIH	High-level input voltage	2			2		***************************************	V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	PARAMETER TEST CONDITIONS	ONDITIONS	SN	54ALS1	2A	SN	2A	UNIT	
PARAMETER	, IESI C	UNDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNII
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.5			-1.5	V
ЮН	$V_{CC} = 4.5 V$,	V _{OH} ≈ 5.5 V			0.1			0.1	mA
	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	v
VOL	$V_{CC} = 4.5 V$,	IOL = 8 mA					0.35	0.5	0.5
Ιι	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V$,	$V_{ } = 2.7 V$			20			20	μΑ
կլ I	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.32	0.6		0.32	0.6	mA
ICCL	$V_{CC} = 5.5 V$,	V _I = 4.5 V		1.2	2.2		1.2	2.2	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25 ^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	то (оитрит)		UNIT			
			SN544	SN54ALS12A		SN74ALS12A	
			MIN	MAX	MIN	MAX	
^t PLH	Any	Y	23	59	23	54	ns
^t PHL	Any	Y	5	26	5	18	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS15A, SN74ALS15A TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

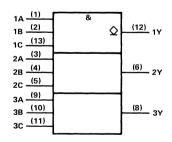
These devices contain three independent 3-input AND gates with open-collector outputs. These gates perform the Boolean functions $Y=A \cdot B \cdot C$ or $Y=\overline{A+B+C}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS15A is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS15A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

1	NPUTS	3	OUTPUT
Α	В	С	Y
Н	Н	Н	H
L	X	Х	L
Х	L	Х	L
Х	Χ	L	L

logic symbol†



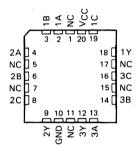
 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

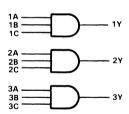
SN54ALS15A . . . J PACKAGE SN74ALS15A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS15A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection



SN54ALS15A, SN74ALS15A TRIPLE 3-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted	
Supply voltage, VCC	7 V
Input voltage	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54ALS15A	-55°C to 125°C
SN74ALS15A	
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN	SN54ALS15A			SN74ALS15A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.7			0.8	٧	
VOH	High-level output voltage			5.5			5.5	٧	
ō	Low-level output current			. 4			8	mA	
TA	Operating free-air temperature	- 55		125	0		- 70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		S	SN54ALS15A			SN74ALS15A		
PARAMETER			MIN	TYP†	MAX	MIN	TYPt	MAX	UNIT
ViK	$V_{CC} = 4.5 V$	I _I = -18 mA			-1.5			-1.5	V
ЮН	$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V			0.1			0.1	mA
	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	v
VOL	$V_{CC} = 4.5 V$	I _{OL} = 8 mA					0.35	0.5	٧
Ц	$V_{CC} = 5.5 V$	V _I = 7 V	,		0.1			0.1	mA
ін і	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
ІССН	$V_{CC} = 5.5 V,$	V _I = 4.5 V		1	1.8		1	1.8	mA
ICCL	$V_{CC} = 5.5 V$,	V _I = 0 V		1.66	3		1.66	3	mA

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_{L} = 50 \text{ pF}$ $R_{L} = 2 \text{ k}\Omega$ $T_{A} = \text{MIN to MAX}$ $SN54ALS15A \qquad SN74ALS15A$			UNIT	
		<u> </u>	MIN	MAX	MIN	MAX	
^t PLH	Any	Y	20	59	20	45	ns
^t PHL	Any	Y	6	25	6	20	ns



SN54ALS20A, SN54AS20, SN74ALS20A, SN74AS20 DUAL 4-INPUT POSITIVE-NAND GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

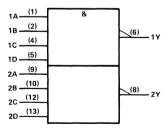
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A + \overline{B} + \overline{C} + \overline{D}}$ in positive logic.

The SN54ALS20A and SN54AS20 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS20A and SN74AS20 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	INP	UTS		OUTPUT
Α	В	С	D	Y
Н	Н	Н	Н	L
L	X	X	Х	н
Х	L	Х	Х	н
Х	X	L	X	н
Х	Х	X	L	н

logic symbol†



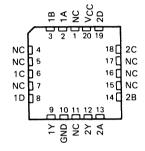
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

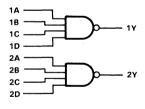
SN54ALS20A, SN54AS20 . . . J PACKAGE SN74ALS20A, SN74AS20 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS20A, SN54AS20 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





recommended operating conditions

		SN54ALS20A			SN	OA	UNIT	
]		 MIN	NOM	MAX	MIN	NOM	MAX	ONIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	٧
Іон	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETER	TEST SOND	TIONO	SN	54ALS2	20A	SN	74ALS2	20A	UNIT
PARAMETER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	V _{CC} = 4.5 V,	l ₁ = -18 mA			- 1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		V _{CC} -2			V
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5	V
l l	$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1			0.1	mA
IH	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
liL	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.1			-0.1	mA
lo [‡]	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		0.22	0.4		0.22	0.4	mA
ICCL	V _{CC} = 5.5 V,	V ₁ = 4.5 V	I	0.81	1.5		0.81	1.5	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}.$ $C_L = 50 \text{ pF}.$ $R_L = 500 \Omega.$ $T_A = 25 ^{\circ}\text{C}$ 'ALS20A	SN54/	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = MIN$ ALS20A	to MAX	ALS20A	UNIT
			TYP	MIN	MAX	MIN	MAX	
t _{PLH}	Any	Y	7	1	18	3	11	
tPHL	Any	Y	6	1	15	3	10	ns



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

 Operating free-air temperature range:
 SN54AS20
 -55 °C to 125 °C

 SN74AS20
 0 °C to 70 °C

 Storage temperature range
 -65 °C to 150 °C

recommended operating conditions

		s	N54AS2	20	S	N74AS2	20	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			.2			V
VIL	Low-level input voltage			0,8			0.8	٧
ЮН	High-level output current			- 2			-2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETED	TECT COMP.	TIONS	S	N54AS2	20	SN74AS20			UNIT
PARAMETER	TEST COND	TIONS	MIN TYP [†] MAX			MIN	TYP [†]	MAX	UNIT
V _{IK}	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2	2		V _{CC} - 2			V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
lį	$V_{CC} = 5.5 V$	V _I = 7 V			0.1			0.1	mA
ин .	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.5			-0.5	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Iссн	$V_{CC} = 5.5 V$,	V _I = 0 V		1	1.6		1	1.6	mA
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		5.4	8.7		5.4	8.7	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$V_{CC} = 4.5$ $C_L = 50 \text{ p}$ $R_L = 500 $ $T_A = MIN$ $AS20$ MAX	F, Ω, to MAX	AS20	UNIT
[†] PLH	Any	Υ	1	5.5	1	5	200
t _{PHL}	Any	Υ	1	5	1	4.5	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS21A, SN54AS21, SN74ALS21A, SN74AS21 **DUAL 4-INPUT POSITIVE-AND GATES**

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

logic symbol†

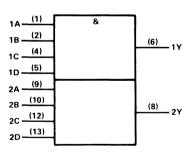
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A + B + C + D}$ in positive logic.

The SN54ALS21A and SN54AS21 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS21A and SN74AS21 are characterized for operation from 0°C to 70°C.

	INP		OUTPUT	
Α	В	С	D	Y
Н	H	Н	Н	Н
L	Χ	X	Х	Ł
Х	L	X	Χ	L
Х	X	L	Х	L
Х	Х	X	L	L

FUNCTION TABLE (each gate)

logic diagram (positive logic)

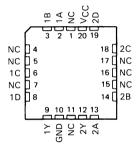


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

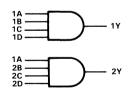
Pin numbers shown are for D, J, and N packages.

SN54ALS21A, SN54AS21 . . . J PACKAGE SN74ALS21A, SN74AS21 . . . D OR N PACKAGE (TOP VIEW) 1A 🗆 1 U14 VCC 1B ∏2 13 2D ис Пз 12 🗆 2C 1C Π 4 11 NC 1D | 5 10 T 2B 1Y ∏6 9∏2A GND [8 7 2Y

SN54ALS21A, SN54AS21 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





recommended operating conditions

		·sn	154ALS2	1A	SN	SN74ALS21A		LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	TIONS	SN	54ALS	21A	SN	74ALS	21A	UNIT
PANAMETER	TEST CONDITIONS		MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			٧
V	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	IOL = 8 mA					0.35	0.5	\ \
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
ΊL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
lo‡	V _{CC} = 5.5 V,	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
Iссн	$V_{CC} = 5.5 V,$	V _I = 4.5 V		0.85	1.4		0.85	1.4	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 0 V		1.4	2.3		1.4	2.3	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	$V_{CC} = 5V,$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}C$ 'ALS21A TYP	!	V _{CC} = 4.5 C _L = 50 pl R _L = 500 s T _A = MIN ALS21A MAX	=, ∩, to MAX	ALS21A	UNIT
^t PLH	Any	V	8.3	4	18	4	15	ns
t _{PHL}] ^''y	'	6.5	2	12	2	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS21, SN74AS21 **DUAL 4-INPUT POSITIVE AND GATES**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS21	I − 55 °C to 125 °C
SN74AS21	I
Storage temperature range	-65°C to 150°C

recommended operating conditions

		S	N54AS2	21	s	SN74AS21		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcс	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
loн	High-level output current			- 2			- 2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		S	SN54AS21			N74AS	21	UNIT		
PARAMETER	TEST COND	ITIONS	MIN	TYPt	MAX	MIN	TYP†	MAX	GNII		
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	V		
VoH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			٧		
VoL	V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V		
l _i	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA		
IH.	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ		
IL.	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA		
IO‡	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		-112	mA		
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		2.9	4.6		2.9	4.6	mA		
^I CCL	V _{CC} = 5.5 V,	V _I = 0 V		7.4	12		7.4	12	mA		

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$			
			SN54	SN54AS21 SN74AS21		AS21	
			MIN	MAX	MIN	MAX	
tPLH	Any	Y	1	6.5	1	6	ns
t _{PHL}	Any	Y	1	6.5	1	6	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output, Ios.

SN54ALS22B, SN74ALS22B DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

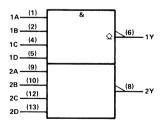
These devices contain two independent 4-input NAND gates. They perform the Boolean functions Y = $\overline{A \cdot B \cdot C \cdot D}$ or Y = $\overline{A + B + C + D}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher VOH levels.

The SN54ALS22B is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS22B is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	INP	UTS		OUTPUT
Α	В	С	D	Υ
Н	Н	Н	Н	L
L	X	X	X	Н
х	L	X	X	Н
х	Χ	L	X	Н
Х	Χ	X	L	Н

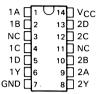
logic symbol†



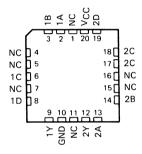
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

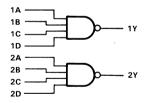
SN54ALS22B . . . J PACKAGE SN74ALS22B . . . D OR N PACKAGE (TOP VIEW)

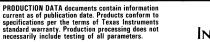


SN54ALS22B . . . FK PACKAGE (TOP VIEW)



NC-No internal connection







SN54ALS22B, SN74ALS22B DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 7 V
Input voltage		
Off-state output voltage		 7 V
Operating free-air temperature range:		
	SN74ALS22B	 0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SN	154ALS2	22B	SN	SN74ALS22B		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage	T		0.7			0.8	V
Voн	High-level output voltage	T		5.5			5.5	V
loL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TECT OF	TEST CONDITIONS		V54ALS	22B	SN	174ALS2	22B	UNIT
PARAMETER	TEST CC	PINDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
V _{IK}	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			-1.5	V
ЮН	$V_{CC} = 4.5 V$	V _{OH} = 5.5 V			0.1			0.1	mA
VOL	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	v
VOL.	$V_{CC} = 4.5 V$,	IOL = 8 mA					0.35	0.5	
lį .	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
Іссн	$V_{CC} = 5.5 V$,	V _I = 0 V		0.22	0.4		0.22	0.4	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		0.8	1.5		0.8	1.5	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_{L} = 50 \text{ pF}$, $R_{L} = 2 \text{ k}\Omega$, $T_{A} = 25 ^{\circ}\text{C}$		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 2 \text{ k}\Omega$, $T_A = \text{MIN}$	F,	·,	UNIT
,			'ALS22B SN54ALS22B		ALS22B	SN74	ALS22B	
			TYP	MIN	MAX	MIN	MAX	
^t PLH	Any	Y	35	23	65	23	45	
^t PHL	Any	Y	8	4	32 4 1		18	ns



SN54ALS27, SN54AS27, SN74ALS27, SN74AS27 TRIPLE 3 INPUT POSITIVE NOR CATES

1A Π 1

2A ∏3

1B 🗌

SN54ALS27, SN54AS27 . . . J PACKAGE

SN74ALS27, SN74AS27 . . . D OR N PACKAGE

(TOP VIEW)

14 VCC

13 1 C

12 1Y

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers. and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A + B + C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54ALS27 and SN54AS27 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS27 and SN74AS27 are characterized for operation from 0 °C to 70°C.

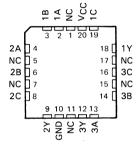
FUNCTION TABLE (each gate)

1	NPUTS	3	OUTPUT
Α	В	С	Υ
Н	Х	Х	L
Х	Н	Х	L
Х	X	Н	L
L	L	L	н

2C ∏5

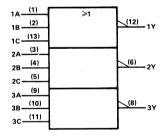
28 □4 11 T3C 10 T 3B 2Y 🗆 6 9 3A GND □7 ٦зү

SN54ALS27, SN54AS27 . . . FK PACKAGE (TOP VIEW)



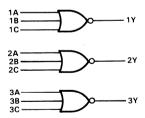
NC - No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984, and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	 	7 V
Input voltage		
Operating free-air temperature range: SN54ALS27	 	– 55 °C to 125 °C
SN74ALS27	 	0 °C to 70 °C
Storage temperature range	 	-65 °C to 150 °C

recommended operating conditions

		SI	V54ALS	27	SI	174ALS	27	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	٧.
IOH	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	SN54ALS27			174ALS	27	UNIT
PARAMETER	1EST CONDI	ITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	l _l = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -0.4 mA	V _{CC} -2			V _{CC} -2			V
14	V _{CC} = 4.5 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	v
VOL	V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5)
l _l	V _{CC} = 5.5 V,	V _I = 7 V		,	0.1			0.1	mA
lін	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 \text{ V}$			20			20	μΑ
I _{IL}	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.97	1.8		0.97	1.8	mA
ICCL .	$V_{CC} = 5.5 V$	V _I = 4.5 V		2	4		2	4	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MII	Ω,	V,	UNIT
			SN54ALS27 SN74ALS27		ALS27		
			MIN	MAX	MIN	MAX	
tPLH	Any	Y	4	26	4	15	ns
tPHL	Any	Y	1	11	3	9	ns



[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{CS}.

SN54AS27, SN74AS27 TRIPLE 3-INPUT POSITIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Operating free-air temperature range: SN54AS27 – 55 °C to 125 °C

recommended operating conditions

		S	N54AS	27	SN74AS27			LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 2			- 2	mA
^I OL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		S	SN54AS27			SN74AS27			
PARAMETER	TEST COND	HIONS	MiN	TYP†	MAX	MIN	TYP†	MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V	
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V	
V _{OL}	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V	
l _I	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ	
ΙιL	$V_{CC} = 5.5 V$	$V_{ } = 0.4 V$			-0.5			-0.5	mA	
lo‡	$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	-30		-112	-30		-112	mA	
IССН	$V_{CC} = 5.5 V,$	V _I = 0 V		4	6.4		4	6.4	mA	
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		10.6	. 17.1		10.6	17.1	mA	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = Mir	Ω,	V,	UNIT	
			SN54	SN54AS27 SN74AS27		AS27	27	
			MIN	MAX	WIN	MAX		
^t PLH	Any	Y	1	6.5	1	5.5	ns	
^t PHL	Any	Y	1	5	1	4.5	ns	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

SN54ALS28A, SN74ALS28A QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

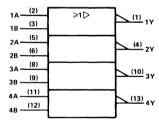
These devices contain four independent 2-input NOR buffer gates. They perform the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS28A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS28A is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

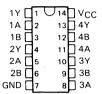
Γ	INP	UTS	OUTPUT
Γ	Α	В	Y
Γ	Н	Х	L
l	X	Н	L
	L	L	н

logic symbol†

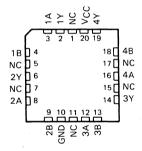


 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

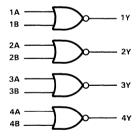
SN54ALS28A . . . J PACKAGE SN74ALS28A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS28A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



Pin numbers shown are for D, J, and N packages.

SN54ALS28A, SN74ALS28A QUADRUPLE 2-INPUT POSITIVE NOR BUFFERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS28A	55°C to 125°C
SN74ALS28A	0°C to 70°C
Storage temperature range	65°C to 150°C

recommended operating conditions

		SN	54ALS2	8A	SN	74ALS2	8A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			-2.6	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA45750	TF0T 00ND	7.01.0	SN	54ALS2	8A	SN74ALS28A			UNIT
PARAMETER	TEST COND	ITIONS	MIN	TYP [†]	MAX	MIN	TYP	MAX	UNIT
V _{IK}	VCC = 4.5 V,	I _I = -18 mA			-1.5			-1.5	٧
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	', I _{OH} = -0.4 mA	Vcc	- 2		V _{CC}	- 2		
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 \text{ V},$	IOH = -2.6 mA				2.4	3.3		
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA		-			0.35	0.5	V
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
IH	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 \text{ V}$			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			- 0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	- 30		- 112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		1.7	2.8		1.7	2.8	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		5.6	9		5.6	9	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V,$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$		$V_{CC} = 4.5$ $C_{L} = 50 \text{ pl}$ $R_{L} = 500 \text{ s}$ $T_{A} = \text{MIN}$	=, n,	<i>I</i> ,	UNIT
				TYP	MIN	MAX	MIN	MAX	
TYP MIN MAX MIN MAX	tPLH	A or B	Y	4	1	16	2	8	
tpj H A or B Y 4 1 16 2 8	^t PHL	A or B	Y	4	1	10	2	7	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30 8-INPUT POSITIVE-NAND GATES

MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

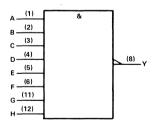
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54ALS30A and SN54AS30 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS30A and SN74AS30 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	н

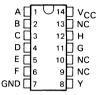
logic symbol†



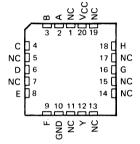
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

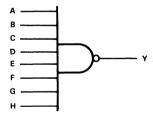
SN54ALS30A, SN54AS30 . . . J PACKAGE SN74ALS30A, SN74AS30 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS30A, SN54AS30 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		
Input voltage		
	: SN54ALS30A	
	SN74ALS30A	0 °C to 70 °C
Ctorogo tomporatura rango		-65°C to 150°C

recommended operating conditions

		SN	154ALS3	BOA	SN	74ALS3	30A	
1		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
loL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	SN54ALS30A			SN74ALS30A		
PARAMETER			MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
	V _{CC} = 4.5 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	v
VOT.	V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	5 V
lj .	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ	V _{CC} = 5.5 V,	$V_{ } = 2.7 \text{ V}$			20	-		20	μΑ
ΊL	$V_{CC} = 5.5 V,$	$V_{ } = 0.4 \text{ V}$			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.22	0.36		0.22	0.36	mA
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		0.54	0.9		0.54	0.9	mA

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 R _L = 500 T _A = MI	Ω, I to MAX		UNIT
			SN54/	SN54ALS30A SN74ALS3		SN74ALS30A	
			MIN	MAX	MIN	MAX	
tPLH	Any	Υ Υ	3	15	3	10	ns
tPHL	Any	Y	3	15	3	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54AS30
SN74AS30
Storage temperature range -65 °C to 150 °C

recommended operating conditions

		S	SN54AS30			SN74AS30			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage			0.8			0.8	V	
ЮН	High-level output current			- 2			- 2	mA	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS30			SI	N74AS	30	UNIT
PARAMETER	TEST CONDI	HIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNII
VIK	V _{CC} = 4.5 V,	I _l = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}	$V_{CC} = 4.5 V,$	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V
lj	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IL	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$,		-0.5			-0.5	mA
10‡	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		0.9	1.5		0.9	1.5	mA
CCL	$V_{CC} = 5.5 \text{ V},$	V ₁ = 4.5 V		3	4.9		3	4.9	mA

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MI	Ω,	V,	UNIT
	*		SN54AS30 SN74AS30			AS30	
			MIN	MAX	MIN	MAX	
^t PLH	Any	Y	1	5.5	1	5	ns
tPHL t	Any	Y	1	5	1	4.5	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$. ‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS32, SN54AS32, SN74ALS32, SN74AS32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

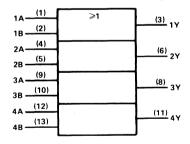
These devices contain four independent 2-input OR gates. They perform the Boolean functions Y = A + B or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS32 and SN74AS32 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

INPL	JTS	OUTPUT
Α	В	Υ
Н	Х	Н
×	Н	н
L	L	L

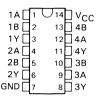
logic symbol†



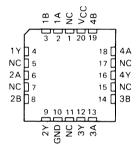
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

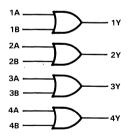
SN54ALS32, SN54AS32 . . . J PACKAGE SN74ALS32, SN74AS32 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS32, SN54AS32 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS32 -55°C to 125°C SN74ALS32 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		S	SN54ALS32			SN74ALS32			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	. 2			2			V	
VIL	Low-level input voltage			0.7			0.8	mA	
ЮН	High-level output current			-0.4			-0.4	mA	
lOL	Lowlevel output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	154ALS	32	SN	UNIT		
PARAMETER			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V$,	l _j =18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			٧
V	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 8 \text{ mA}$					0.35	0.5	V
l _l	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IΙL	$V_{CC} = 5.5 V$	$V_I = 0.4 V$			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
Іссн	$V_{CC} = 5.5 V$,	V _I = 4.5 V		1.9	4		1.9	4	mA
^I CCL	$V_{CC} = 5.5 V$,	V _I = 0 V		2.6	4.9		2.6	4.9	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$ 'ALS32	SN54	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = \text{MIN}$ ALS32	=, ⊋, to MAX	ALS32	UNIT
		1	TYP	MIN	MAX	MIN	MAX]
^t PLH	A or B	Y	8.8	3	18	3	14	ns
^t PHL	A or B	Υ ,	6.8	3	16	3	12	ns



[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS32, SN74AS32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

absolute maximum	ratings ove	r operating	tree-air	temperature	range	(unless	otherwise no	ted)

Supply voltage, VCC		 	7 V
Input voltage		 	7 V
Operating free-air temperature range:	SN54AS32	 	-55°C to 125°C
	SN74AS32	 	0°C to 70°C
Storage temperature range			65 9C to 150 9C

recommended operating conditions

		 SN54AS32			s	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	mA
Іон	High-level output current			- 2			- 2	mA
lOL	Lowlevel output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		[′] 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS32		S	UNIT			
PARAMETER			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	V _{CC} = 4.5 V,	l _l = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -2 mA	V _{CC} -2			V _{CC} -2			V
VOL	V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
11	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
ΙΙL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
1 ₀ ‡	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
1ссн	V _{CC} = 5.5 V,	V _I = 4.5 V		7.3	12		7.3	12	mA
ICCL	V _{CC} = 5.5 V,	V _I = 0 V		16.5	26.6		16.5	26.6	mA

 $^{^{\}dagger}$ All typical values are at VCC $\,=\,5$ V, TA $\,=\,25\,^{\circ}\text{C}.$

FROM	TO (OUTPUT)		$C_L = 50 \text{ pl}$ $R_L = 50 \Omega$	F,	<i>'</i> ,	UNIT
(1141 017	(001101)	SN54AS32 SN74AS32			AS32	1
		MIN	MAX	MIN	MAX	1
A or B	Y	1	7.5	1	5.8	ns
A or B	Y	1	6.5	1	5.8	ns
	(INPUT) A or B	(INPUT) (OUTPUT) A or B Y	(INPUT) (OUTPUT) SN54 MIN A or B Y 1	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

^{*} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS33A, SN74ALS33A QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

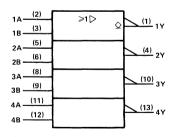
These devices contain four independent 2-input NOR buffer gates with open-collector outputs. Open-collector outputs require resistive pull-up to perform logically but can deliver higher VOH levels and are commonly used in wired-AND applications. These devices perform the Boolean functions Y = A + B or Y = A + B in positive logic.

The SN54ALS33A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS33A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INP	JTS	OUTPUT
Α	В	Υ
Н	Х	L
×	н	L
L	L	н

logic symbol†



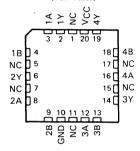
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

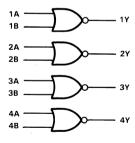
SN54ALS33A . . . J PACKAGE SN74ALS33A . . . D OR N PACKAGE (TOP VIEW)

1 Y 🛚	1	V14 Vcc
1A 🗌	2	13 4Y
1B 🗌	3	12 🗍 4B
2Y 🗌	4	11 🗀 4A
2A 🗌	5	10 🗍 3Y
2B 🗌	6	9 🗍 3B
GND [7	8 🗍 3A

SN54ALS33A . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection



SN54ALS33A, SN74ALS33A QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 	7 V
Input voltage		 	7 V
Off-state output voltage		 	7 V
Operating free-air temperature range:	SN54ALS33A	 	. −55 °C to 125 °C
	SN74ALS33A	 	0°C to 70°C
Storage temperature range			-65°C to 150°C

recommended operating conditions

		SN	SN54ALS33A			SN74ALS33A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Voн	High-level output voltage			5.5		_	5.5	V	
loL	Low-level output current			12			24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	DNDITIONS	SN!	54ALS3	ЗА	SN	74ALS3	ЗА	UNIT
PANAIVIETEN	1251 CC	TEST CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.5			-1.5	V
loн	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V	1		0.1			0.1	mA
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
\ VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	ľ
11	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
IH	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IΙL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1		_	-0.1	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		1.7	2.8		1.7	2.8	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		5.6	9		5.6	9	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L T _A	$C_L = 50 \text{ pF}, \qquad C_L = R_L = 680 \Omega, \qquad R_L = T_A = 25 ^{\circ} C \qquad T_A = 7 ^{\circ} ALS33A \qquad SN54ALS33$				F, Ω, to MAX	V, ALS33A MAX	UNIT
			IVIIIV	117	IVIAA	IVIIIV	IVIAA	IVIIIV	IVIAA	
tPLH	A or B	Y		18	24	10	59	10	33	ns
tPHL	A or B	Υ		7	10	2	18	2	12	115



SN54ALS34, SN54AS34, SN74ALS34, SN74AS34 HEX NONINVERTERS

D2261, DECEMBER 1983-REVISED MAY 1986

- Noninverters
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

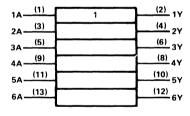
These devices contain six independent noninverters. They perform the Boolean function Y = A.

The SN54ALS34 and SN54AS34 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS34 and SN74AS34 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each buffer)

INPUT	OUTPUT
Α	Υ
Н	н
L	L

logic symbol †



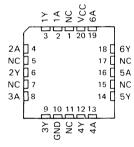
 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

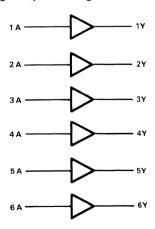
SN54ALS34, SN54AS34 . . . J PACKAGE SN74ALS34, SN74AS34 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS34, SN54AS34 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		
Operating free-air temperature range:		
	SN74ALS34	0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SI	SN54ALS34			SN74ALS34			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcс	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
٧ _{IL}	Low-level input voltage			0.7			0.8	V	
юн	High-level output current			-0.4			-0.4	mA	
lor	Low-level output current			4			8	_ mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SI	154ALS	34	SN74ALS34			LIBUT
PARAMETER			MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.2			- 1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
.,	$V_{CC} = 4.5 \text{ V},$	IOL = 4 mA		0.25	0.4		0.25	0.4	.,
VOL	V _{CC} = 4.5 V,	IOL = 8 mA					0.35	0.5	V
l _l	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V ₁ = 2.7 V			20			20	μΑ
ИL	V _{CC} = 5.5 V,	$V_1 = 0.4 V$			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	-30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		3.1	5		3.1	5	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 0 V		5	8		5	8	mA

[†]All typical values are at $V_{CC} = 25$ °C.

switching characteristics (see Note 1)

•	-	-						
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$ 'ALS34	-	$V_{CC} = 4.5$ $C_{L} = 50 \text{ pF}$ $R_{L} = 500 \Omega$ $T_{A} = MIN \Omega$ ALS34	:, ⊋, to MAX	V, ALS34	UNIT
			TYP	MIN	MAX	MIN	MAX	1
^t PLH	А		9.4	4	18	4	15	
^t PHL .	. ^	1	5	1	12	1	10	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted),

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS34	55°C to 125°C
SN74AS34	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54AS34			SN74AS34				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2		,,,,,,	2			V	
VIL	Low-level input voltage			0.8			0.8	V	
loн	High-level output current			- 2			- 2	mA	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS34		SN74AS34			UNIT	
PARAMETER			MIN	TYPt	MAX	MIN	TYP†	MAX	ONIT
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$l_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			V
V _{OL}	$V_{CC} = 4.5 V$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
lį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
liH .	$V_{CC} = 5.5 V$,	V ₁ = 2.7 V			20			20	μΑ
ήL	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.1			-0.1	mA
I _O ‡	$V_{CC} = 5.5 V$	$V_0 = 2.25 \text{ V}$	-30	-	-112	- 30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 4.5 V		7.4	12		7.4	12	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 0 V		21.3	34.6		21.3	34.6	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		UNIT			
			SN54AS34 SN74AS3		/4AS34		
			MIN	MAX	MIN	MAX	
^t PLH		.,	1	6.5	1	5.5	ns
t _{PHL}	Α	Υ	1	7	1	6	

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS

SN54ALS35A, SN74ALS35A HEX NONINVERTERS WITH OPEN COLLECTOR OUTPUTS

D2661, DECEMBER 1983-REVISED MAY 1986

- Noninverters with Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent noninverters. They perform the Boolean functions Y=A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS35A is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS35A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each buffer)

	INPUT	OUTPUT
1	Α	Υ
Ī	Н	Н
١	L	L

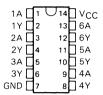
logic symbol[†]

1A (1)	DΦ	(2) 1Y
2A (3)		(4) 2Y
3A (5)		(6) 3Y
4A (9)		(8) 4Y
5A (11)		(10) 5Y
6A (13)		(12) 6Y

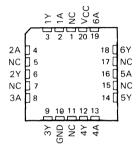
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J and N packages.

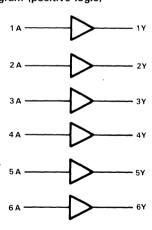
SN54ALS35A . . . J PACKAGE SN74ALS35A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS35A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection





SN54ALS35A, SN74ALS35A HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 7 V
Input voltage		 7 V
Off-state output voltage		 7 V
Operating free-air temperature range:	SN54ALS35A	 -55°C to 125°C
	SN74ALS35A	 0°C to 70°C
Storage temperature range		 -65°C to 150°C

recommended operating conditions

		SN	SN54ALS35A		SN74ALS35A			UNIT
	A	MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	٧
VOH	High-level output voltage			5.5			5.5	V
lor	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TECT OF	TEST CONDITIONS		54ALS	85A	SN74ALS35A			UNIT
PARAMETER	TEST COMBITIONS		MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	l _l = -18 mA			- 1.2			-1.2	V
IOH	$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V			0.1			0.1	mA
V	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	IQL = 8 mA					0.35	0.5	· ·
Ŋ	$V_{CC} = 5.5 V$	V ₁ = 7 V			0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 V$	V _I = 2.7 V			20			20	μА
lic i	$V_{CC} = 5.5 V$	V _I = 0.4 V			-0.1			-0.1	mA
^I ССН	$V_{CC} = 5.5 V$	V _I = 4.5 V		2.7	4.7		2.7	4.7	mA
^I CCL	$V_{CC} = 5.5 V$,	$V_I = 0 V$		4.1	6.3		4.1	6.3	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V.}$ $C_{L} = 50 \text{ pF.}$ $R_{L} = 2 \text{ k}\Omega.$ $T_{A} = 25 \text{ °C}$ $ALS35A$ TYP		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 2 \text{ k}\Omega$ $T_A = \text{MIN}$ $ALS35A$ MAX	to MAX	NLS35A MAX	UNIT
^t PLH	A		34	20	60	20	50	ns
, tphl]^	<u>'</u>	9	2	17	2	14	ns



SN54ALS37A, SN74ALS37A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

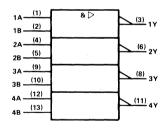
These devices contain four independent 2-input NAND buffer gates. They perform the Boolean functions $Y=\overline{A \cdot B}$ or $Y=\overline{A}+\overline{B}$ in positive logic.

The SN54ALS37A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS37A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
L	X	н
×	L	н

logic symbol†



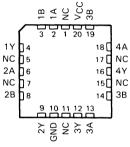
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS37A . . . J PACKAGE SN74ALS37A . . . D OR N PACKAGE (TOP VIEW)

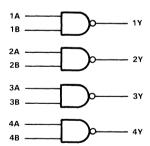


SN54ALS37A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic diagram (positive logic)





SN54ALS37A, SN74ALS37A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

absolute maximum	ratings over	operating	free-air	temperature	range	(unless	otherwise noted)
aboolate maximum	Tuttings over	operating	noc un	temperature	unge	(united)	other wise noteur

	7 V	
Input voltage		/
	SN54ALS37A55 °C to 125 °C	
	SN74ALS37A)
Storage temperature range	-65°C to 150°C	•

recommended operating conditions

	,	SN54ALS37A				SN74ALS37A			
		 MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			. V	
VIL	Low-level input voltage			0.7			0.8	V	
Іон	High-level output current			- 1			-2.6	mA	
lOL	Low-level output current			12			24	mΑ	
TA	Operating free-air temperature	- 55		125	0		70	°Ç	

electrical characteristics over recommended operating-free-air temperature range (unless otherwise

DADAMETED	TEST COMP	TIONO	SN	54ALS	37A	SN	74ALS	37A	
PARAMETER	TEST CONDI	TEST CONDITIONS		TYP	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -:	2		V _{CC} -2			
∨он	$V_{CC} = 4.5 V,$	IOH = -1 mA	. 2.4	3.3] v
,	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2]
VoL	$V_{CC} = 4.5 V,$	IOL = 12 mA	,	0.25	0.4		0.25	0.4	v
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5]
łį	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1	}		0.1	mA
lΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
¹ ССН	$V_{CC} = 5.5 V,$	V ₁ = 0 V		0.86	1.6		0.86	1.6	mA
¹ CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		4.8	7.8		4.8	7.8	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = \text{MIN}$	=, ⊋,	; v ,	UNIT
	1	i	'ALS37A	SN54/	ALS37A	SN7	4ALS37A	
			TYP	MIN	MAX	MIN	MAX	
tpLH `	A or B	Y	4	2	17	2	8	no
^t PHL	A or B	Y	5	2	10	2	7	ns



^{*} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS38A, SN74ALS38A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

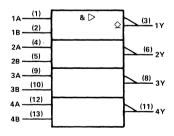
These devices contain four independent 2-input NAND buffer gates with open-collector outputs. These NAND buffers perform the Boolean functions $Y=\overline{A\cdot B}$ or $Y=\overline{A}+\overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher VOH levels.

The SN54ALS38A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS38A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
Н	Н	L
L	Х	Н
X	L	Н

logic symbol†



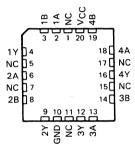
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS38A . . . J PACKAGE SN74ALS38A . . . D OR N PACKAGE (TOP VIEW)

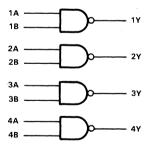
1A 🛮 1	U14□ Vcc
1B 🛮 2	13 4B
1Y 🛮 3	12 🗀 4A
2A 🛮 4	11 🛮 4Y
2B 🗌 5	10 🗍 3B
2Y 🛮 6	9 🗍 3A
GND 7	8∐ 3Y

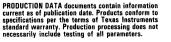
SN54ALS38A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic diagram (positive logic)







SN54ALS38A, SN74ALS38A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage		7 V
Operating free-air temperature range	SN54ALS38A 55 °C to	125°C
	SN74ALS38A	to 70°C
Storage temperature range	_ 65°C +c	15000

recommended operating conditions

		SN	54ALS3	8A	SN	74ALS3	8A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			· V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
^I OL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETED	TEST CO	DAIDITIONS	SN	154ALS	38A	SN	74ALS3	88A	LIBUT
PARAMETER	IESI CI	ONDITIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.5			-1.5	V
loн	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL}	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	v
lj .	$V_{CC} = 5.5 V$,	V ₁ = 7 V	- I		0.1			0.1	mA
ин	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.1			-0.1	mA
Іссн	$V_{CC} = 5.5 V$,	V _I = 0 V		0.86	1.6		0.86	1.6	mA
lccr	$V_{CC} = 5.5 V$,	V _I = 4.5 V		4.8	7.8		4.8	7.8	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 680 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$		$V_{CC} = 4.5$ $C_L = 50 \text{ ps}$ $R_L = 680 \text{ s}$ $T_A = MIN$	F, Ω, to MAX		UNIT
],			'ALS38A	SN54/	ALS38A	SN74/	ALS38A	
			TYP	MIN	MAX	MIN	MAX	
tPLH	A or B	Y	18	10	59	10	33	ns
^t PHL	A or B	Y	7	2	18	2	12	115



SN54ALS40A, SN74ALS40A DUAL 4-INPUT POSITIVE-NAND BUFFERS

D2661, APRIL 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

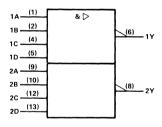
These devices contain two independent 4-input NAND buffer gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS40A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS40A is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

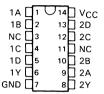
	INP	UTS		OUTPUT
Α	В	С	D	Υ
Н	Н	Н	Н	L
L	Х	Χ	Χ	н
X	L	X	Χ	Н
X	X	L	Х	н
Х	Х	X	L	Н

logic symbol†

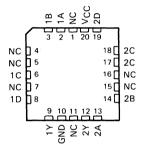


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS40A . . . J PACKAGE SN74ALS40A . . . D OR N PACKAGE (TOP VIEW)

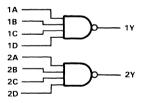


SN54ALS40A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

SN54ALS40A, SN74ALS40A DUAL 4-INPUT POSITIVE-NAND BUFFERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
Operating free-air temperature range: SN54ALS40A	-55 °C to 125 °C
SN74ALS40A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN	54ALS4	IOA	SN	174ALS4	ΙOΑ	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			-2.6	mA
IOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETED	TEST SOND	TIONO	SN	154ALS4	10A	SN	74ALS4	AO	
PARAMETER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		V _{CC} -2	2		
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					\ \
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		Ì
Vol	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5	l ,
4	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V ₁ = 2.7 V			20			20	μΑ
1 _{IL}	$V_{CC} = 5.5 V,$	$V_1 = 0.4 \ V$			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_{O} = 2.25 \text{ V}$	- 30		-112	-30		-112	mA
¹ ссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.43	0.8		0.43	0.8	mA
¹ CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		2.4	3.9		2.4	3.9	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX			UNIT	
1	1		'ALS40A	SN54A	LS40A	SN74/	ALS40A	
	<u> </u>		TYP	MIN	MAX	MIN	MAX	1
t _{PLH}	Any	Υ	5	2	10	2	8	ns
^t PHL	Any	Y	5	2	10	2	7	1115



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS74A, SN54AS74, SN74ALS74A, SN74AS74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, APRIL 1982 - REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C _L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

description

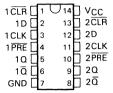
These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS74A and SN74AS74 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

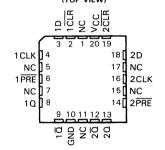
FUNCTION TABLE

	INPUTS			OUTPUTS		
PRESET	CLEAR	CLOCK	D	a	ā	
L	Н	X	X	Н	٦	
[н	L	X	X	L	н	
L	L	X	×	Н*	Н*	
Н	Н	†	н	н	L	
н	Н	†	L	L	н	
Н	Н	L	Х	σ^{o}	\overline{Q}_{o}	

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level. SN54ALS74A, SN54AS74 . . . J PACKAGE SN74ALS74A, SN74AS74 . . . D OR N PACKAGE (TOP VIEW)

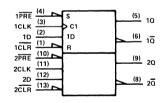


SN54ALS74A, SN54AS74 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54ALS74A, SN54AS7455°C to 125°C
SN74ALS74A, SN74AS740°C to 70°C
Storage temperature range65°C to 150°C

conform truments does not eters.

SN54ALS74A, SN74ALS74A DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

recommended operating conditions

			SI	154ALS	74A	S	V74ALS	74A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				-0.4			-0.4	mA
loL	Low-level output current				4			8	mA
fclock	Clock frequency		0		30	0		34	MHz
		PRE or CLR low	15			15			
t _w	Pulse duration	CLK high	17.5			14.5			ns
		CLK low	17.5			14.5			
	Setup time	Data	16			15			
t _{su}	before CLK↑	PRE or CLR inactive	10			10			ns
th	Hold time, data after CLK↑		2			0			, ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CONDITIO	NC	Si	N54ALS	74A	s	N74ALS	74A	UNIT
r	ANAMETEN	TEST CONDITIO	INO	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I ₁ = -18 mA			- 1.5			-1.5	V
Voн		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		V
Vol		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5	V
1.	CLK or D	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	
l)	PRE or CLR	VCC = 5.5 V,	V = / V			0.2			0.2	mA
l	CLK or D	Vcc = 5.5 V,	V _I = 2.7 V			20			20	^
ΊН	PRE or CLR	vCC = 5.5 v,	V = 2.7 V			40			40	μΑ
1	CLK or D	V E E V	V _I = 0.4 V			-0.2			-0.2	
ΙL	PRE or CLR	$V_{CC} = 5.5 V$,	v ₁ = 0.4 V			-0.4			-0.4	mA
10 [‡]		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		-112	mA
lcc		$V_{CC} = 5.5 V,$	See Note 1		2.4	4		2.4	4	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MI	pF,) Ω,	5 V,	UNIT
[SN54	SN54ALS74A		4ALS74A]
			MIN	MAX	MIN	MAX	
f _{max}			30		34		MHz
^t PLH	PRE or CLR	Q or Q	3	18	3	13	
^t PHL	FRE OF CER	d br d	5	17	5	15	ns
^t Pl.H	CLK	Q or Q	5	23	5	16	
^t PHL	CLIX	4,014	5	20	5	18	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CC} is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

SN54AS74, SN74AS74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

recommended operating conditions

			SI	V54AS7	4	SN	74AS74		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8		,	0.8	V
Іон	High-level output current				-2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		90	0		105	MHz
		PRE or CLR low	4			4			
tw	Pulse duration	CLK high	4			4			ns
		CLK low	5.5			5.5			
	Setup time	Data	4.5			4.5			
t _{su}	before CLK↑	PRE or CLR inactive	2			2			ns
th	Hold time, data after CLK↑		0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAG	A METER	TEGT O	ONDITIONS	SN5	4AS74		SI	N74AS7	4	UNIT
PAR	RAMETER	IESI C	UNDITIONS	MIN T	'YP† N	1AX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 V$,	l _l = -18 mA			1.2			- 1.2	V
Vон		$V_{CC} = 4.5 \text{ V to } 5.9$	$5 \text{ V}, \text{ I}_{OH} = -2 \text{ mA}$	V _{CC} -2			Vcc-	2		٧
VOL		$V_{CC} = 4.5 V$,	$I_{OL} = 20 \text{ mA}$	(0.25	0.5		0.25	0.5	V
11		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
1	CLK or D	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μА
۱чн	PRE or CLR	VCC = 5.5 V,	V - 2.7 V			40			40	μ_
1	CLK or D	V _{CC} = 5.5 V,	V _I = 0.4 V		_	0.5			-0.5	mA
ΊL	PRE or CLR	ACC = 2.2 A	V = 0.4 V		_	1.8			- 1.8	IIIA
l _{lo} ‡		$V_{CC} = 5.5 V$,	V _O = 2.25 V	-30	_	112	- 30		-112	mA
Icc		V _{CC} = 5.5 V	See Note 1		10.5	16		10.5	16	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54	AS74	SN744	\S74	
			MIN	MAX	MIN	MAX	
f _{max}			90		105		MHz
^t PLH	PRE or CLR	Q or $\overline{\mathbb{Q}}$	3	8.5	3	7.5	
^t PHL	PRE OF CLR	u or u	3.5	11.5	3.5	10.5	ns
^t PLH	01.14	Q or Q	3.5	9	3.5	8	
tpHI	CLK	l a or a	4.5	10.5	4.5	9	ns



^{*}TO output conditions have been chosen to produce a current that closely approximates one half of the true short-current output current, IOS. NOTE 1: ICC is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

SN54ALS86, SN74ALS86, SN54AS86, SN74AS86 OUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS86, SN54AS86 . . . J PACKAGE SN74ALS86, SN74AS86 . . . D OR N PACKAGE (TOP VIEW)

1A	1	U ₁₄	□vcc
1B	2	13	П _{4В}
1 Y 🗌	3	12	5 4A
2A 🗌	4	11	☐ 4Y
2B 🗌	5	10	3B
2 Y 🗌	6	9] ЗА
GND [7	8] 3Y

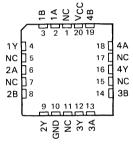
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y=A \oplus B=\overline{A}B+A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

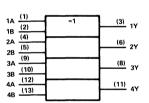
The SN54ALS86 and SN54AS86 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS86 and SN74AS86 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS86, SN54AS86 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol[†]



FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
L	L	L
L	Н	н
Н	L	Н
Н	н	L

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

These are five equivalent Exclusive-OR symbols valid for an 'ALS86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	
Input voltage	
Operating free-air temperature range: SN54ALS86	55 °C to 125 °C
SN74ALS86	
Storage temperature range	

recommended operating conditions

		SI	V54ALS	86	SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		S	SN54ALS86			SN74ALS86			
PARAMETER	IESI C	UNDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$\dot{V}_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V	
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	Vcc-	2		V _{CC} -	2		٧	
Vai	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V	
VOL	$V_{CC} = 4.5 V$,	IOL = 8 mA					0.35	0.5	ľ	
l _j	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA	
lін	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ	
ΊL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA	
lo [‡]	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA	
lcc	$V_{CC} = 5.5 V$,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5 \text{ V to } 5.5 \text{ V},$ $C_L=50 \text{ pF},$ $R_L=500 \Omega,$ $T_A=\text{MIN to MAX}$					
			SN54ALS86		SN74			
			MIN	MAX	MIN	MAX		
t _{PLH}	A or B	V	3	22	3	17		
tPHL:	(other input low)	T	2	14	2	12	ns	
^t PLH	A or B	V	3	22	3	17	p.o.	
[†] PĤL	(other input high)	' ·	2	12	2	10	ns	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

PRODUCT PREVIEW

SN54AS86, SN74AS86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
	86
SN74AS	86 0°C to 70°C
Storage temperature range	

recommended operating conditions

		S	SN54AS86			SN74AS86		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 2			- 2	mA
IOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TF0T 00M	DITIONS	SN54AS86		SI	174AS8	6	
PARAMETER	TEST CON	IDITIONS	MIN T	YP [†] MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}	$V_{CC} = 4.5 V,$	I _I = -18 mA		- 1.2			- 1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	V, I _{OH} = -2 mA	V _{CC} -2		V _{CC} -:	2		V
V _{OL}	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA	0	.35 0.5		0.35	0.5	V
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V		0.1			0.1	mA
ήн	$V_{CC} = 5.5 V,$	V _I = 2.7 V		20)		20	μΑ
hL	$V_{CC} = 5.5 V,$	V _I = 0.4 V		- 0.1			- 0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30	- 112	- 30		-112	mA
ССН	$V_{CC} = 5.5 V,$	V _I = 0 V		18		18		mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		15		15		mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.9 C _L = 50 p R _L = 500 T _A = MIN	Ω,	UNIT
	.		SN54AS86	SN74AS86	1
1			MIN TYP† MAX	MIN TYP† MAX	
tPLH	A or B		3.6	3.6	ns
t _{PHL}	(other input low)	1	3.5	3.5] ""
t _{PLH}	A or B	V	3.6	3.6	
tPHL	(other input high)	Ť	3.5	3.5	ns

 $^{^{\}dagger}$ All typical valves are at VCC $\,=\,5$ V, TA $\,=\,25\,^{o}\text{C}.$

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Inc.

SN54AS95, SN74AS95 4-RIT PARALLEL-ACCESS SHIFT REGISTER

D2661, DECEMBER 1983-REVISED MAY 1986

9 CLK 1

CLK 2

- Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- Right or Left Shifts
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These four-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load Shift right (the direction Q_A toward Q_D) Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the Clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of Clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of Clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Qp to input C, etc.); and serial data is entered at input D. The clock input may be applied commonly to Clock 1 and Clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low. However, conditions described in the last three lines of the function table will also ensure that the register contents are protected.

The SN54AS95 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS95 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

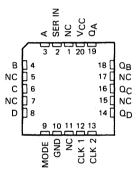
SN54AS95 ... J PACKAGE
SN74AS95 ... D OR N PACKAGE
(TOP VIEW)

SER IN 1 1 14 VCC
A 2 13 QA
B 3 12 QB
C 4 11 QC
D 5 10 QD

SN54AS95 . . . FK PACKAGE
(TOP VIEW)

MODE | 6

GND I



NC-No internal connection

-	UN	CH	UN	IAB	LE

			INPUTS						OUTP	UTS	
MODE	CLO	CKS	SERIAL		PARA	LLEL		QA	αв	αc	a_{D}
CONTROL	2 (L)	1 (R)	JENIAL	Α	В	С	D	Ч	чΒ	40	~D
Н	Н	Х	Х	Х	Х	X	Χ	QAO	σ_{BO}	σ^{CO}	σ^{D0}
Н	↓	x	Х	а	b	С	d	а	b	С	d
н	↓	x	Х	Q_B^{\dagger}	σ_{C_1}	a_D^{\dagger}	d	Q _{Bn}	α_{Cn}	α_{Dn}	d.
L	L	н	Х	×	Х	Х	Х	QAO	σ_{BO}	σ_{CO}	σ_{D0}
L	×	. 1	Н	X	Χ	Χ	Х	Н	q_{An}	Q_{Bn}	q_{Cn}
L	x	↓ .	L	Х	Х	X	Х	L		QBn	α_{Cn}
1	L	L	Х	X	Х	Χ	Х	QAO	Q_{BO}	σ_{CO}	σ_{D0}
1	L	L	Х	x	Х	Χ	X	QAO	Q_{BO}	α_{CO}	Q_{DO}
1	L	н	X	Х	X	Χ	X	QAO	Q_{BO}	σ_{C0}	σ_{D0}
1	н	L	Х	Х	X	X	Х	Q _{AO}	α_{B0}	a_{CO}	σ_{D0}
1	Н	н	Х	Х	Х	X	Х	Q _{A0}	σ_{B0}	σC0	σ_{D0}

†Shifting left requires external connection of QB to A, QC to B, and QD to C. Serial data is entered at input D.

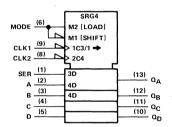
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions). $\downarrow = transition from high to low level, \uparrow = transition from low to high level.$

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

 Q_{AO} , Q_{BO} , Q_{CO} , Q_{DO} = the level of Q_{A} , Q_{B} , Q_{C} , or Q_{D} , respectively, before the indicated steady-state input conditions were established.

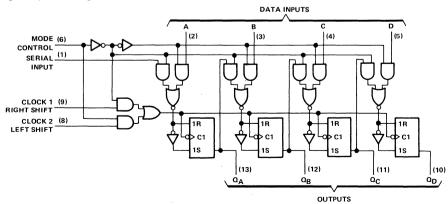
 Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent \downarrow transition of the clock.

logic symbol†



 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)





SN54AS95, SN74AS95 **4-BIT PARALLEL-ACCESS SHIFT REGISTER**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Operating free-air temperature range: SN54AS95 -55°C to 125°C SN74AS95 0°C to 70°C

Storage temperature range -65°C to 150°C

recommended operating conditions

			S	N54AS	95	SN74AS85			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency	0	-	80	0		100	MHz	
tw	Pulse duration, CLK high or low		6.5			5			ns
t _{su}	Setup time, data before CLK	(↓	2.5			2			ns
	Hold time after CLK I	Data	2.5			2.5			
th		CLK 1 to Mode	3.5		,	3			ns
	(see Figure 1)	CLK 2 to Mode	1			0			1
	Clock enable time	CLK 1	13			12			
t _{en}	(see Figure 1)	CLK 2	13			12			ns
	Clock inhibit time	CLK 1	3			2.5			
^t in	(see Figure 1)	CLK 2	1			0			ns
TA	Operating free-air temperatu	re	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA	METER	TEST CONDI	FIONO	S	N54AS	95	S	N74ASS)5	
PARAMETER		TEST CONDI	IIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V
Voн		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	- 2		V
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	٧
l ₁		$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1			0.1	mA
ΉΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
Lie	Mode	V _{CC} = 5.5 V,	V _{II} = 0.4 V			-1			- 1	mA
IIL.	All other	VCC = 3.5 V,	VIL = 0.4 V			-0.5			-0.5	IIIA_
lo‡		V _{CC} = 5.5 V,	$V_0 = 2.35 V$	- 30		-112	- 30		-112	mA
¹ ССН		V _{CC} = 5.5 V			21	34		21	34	mA
^I CCL	1	V _{CC} = 5.5 V			26	39		26	39	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristice (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4$ $C_L = 50$ $R_L = 500$ $T_A = Min$	Ω,	V ,	UNIT
	1	SN54AS95 SN7		SN74	74AS95		
			MIN	MAX	MIN	MAX	1
fmax			80		100		MHz
^t PLH	CLK	0	2	11	2	10	ns
^t PHL		ď	2	10.5	2	9.5	1 "5

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

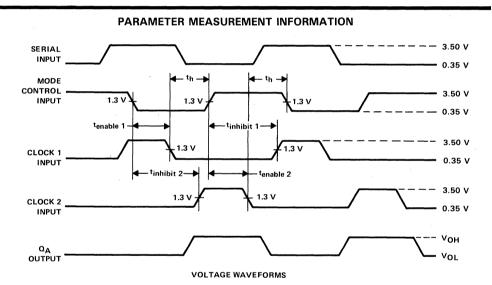


FIGURE 1-CLOCK ENABLE, INHIBIT, AND HOLD TIMES

SN54ALS109A, SN54AS109, SN74ALS109A, SN74AS109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, APRIL 1982 - REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109A	50 MHz	6 mW
'AS109	129 MHz	29 mW

description

These devices contain two independent J- \overline{K} positive-edgetriggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and \overline{K} input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and \overline{K} inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding \overline{K} and trying J high. They also can perform as D-type flip-flops if J and \overline{K} are tied together.

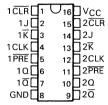
The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS109A and SN74AS109 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

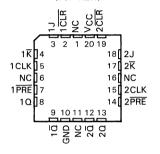
	INPUTS					
PRESET	CLEAR	CLOCK	J	ĸ	Q	ā
L	Н	X	X	Х	Н	L
н	L	Х	X	X	L	н
L	L	X	Х	х	Н*	Н*
н	н	1	L	L	L	Н
н	Н	1	Н	L	TOG	GLE
н	Н	1	L	Н	a_0	\overline{a}_0
н	н	†	Н	н	Н	L
Н	Н	L	х	х	a_0	$\bar{\alpha}_0$

^{*} The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{|L} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS109A, SN54AS109 . . . J PACKAGE SN74ALS109A, SN74AS109 . . . D OR N PACKAGE (TOP VIEW)

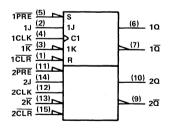


SN54ALS109A, SN54AS109 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	/ V
Input voltage	7 V
Operating free-air temperature range: SN54ALS109A, SN54AS109	-55°C to 125°C
SN74ALS109A, SN74AS109	0°C to 70°C
Storage temperature range	-65°C to 150°C

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54ALS109A, SN74ALS109A DUAL J.K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

recommended operating conditions

			SN	154ALS	109A	SN	74ALS1	09A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				-0.4			-0.4	mA
lOL	Low-level output current				4			8	mA
fclock	Clock frequency		0		30	0		34	MHz
		PRE or CLR low	15			15			
tw	Pulse duration	CLK high	16.5			14.5			ns
		CLK low	16.5			14.5	-		1
	Setup time	Data	15			15			
t _{su}	before CLK↑	PRE or CLR inactive	10			10			ns
th	Hold time, data after CLK†		0			. 0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

_		TEAT COMPLETO		SN	54ALS	109A	SN	74ALS	109A	
	ARAMETER	TEST CONDITION	NS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.5			-1.5	V
Vон		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		V _{CC} -	2		V
Vai		$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 V$,	IOL = 8 mA					0.35	0.5	ľ
	CLK, J, or K	.,	., 7.,			0.1			0.1	
l)	PRE or CLR	$V_{CC} = 5.5 V$	$V_1 = 7 V$			0.2			0.2	mA
	CLK, J, or K	V	V 27V			20			20	
ΉΗ	PRE or CLR	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			40			40	μΑ
	CLK, J or K	V	$V_{I} = 0.4 \text{ V}$			-0.2			-0.2	
ήL	PRE or CLR	$V_{CC} = 5.5 V$,	VI = 0.4 V			-0.4			-0.4	mA
10 [‡]		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	-30		-112	mA
¹ CC		$V_{CC} = 5.5 V,$	See Note 1		2.4	4		2.4	4	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.$ $C_L = 50$ $R_L = 500$ $T_A = Min$	pF, Ω,	ο V ,	UNIT
		• •	SN54/	ALS109A	SN74	ALS109A	
			MIN	MAX	MIN	MAX	
f _{max}			30		34		MHz
tPLH	PRE or CLR	Q or Q	3	17	3	13	ns
tPHL	PRE OF CER	4 01 4	5	17	5	15	115
tPLH	CLK	Q or Q	5	21	5	16	ns
tPHL	CLN	2014	5	20	5	18	115



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

SN54AS109, SN74AS109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

recommended operating conditions

			SI	N54AS1	09	SN	74AS10	9	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		. 2			2			V
VIL	Low-level input voltage				0.8			0.8	V
Iон	High-level output current				- 2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		90	0		105	MHz
		PRE or CLR low	4			4		_	
tw	Pulse duration	CLK high	4			4			ns
		CLK low	5.5			5.5			1
	Setup time	Data	5.5			5.5			ns
t _{su}	before CLK↑	PRE or CLR inactive	2			2			iis
th	Hold time, data after CLK↑		0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TF0T (CAIDITIONS	SI	N54AS1	09	SI	N74AS1	09	
PAI	RAMETER	1EST C	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			- 1.2	٧
Vон		$V_{CC} = 4.5 \text{ V to 5}.$	5 V, I _{OH} = -2 mA	V _{CC} -	2		Vcc-	2		V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I _I		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
1	CLK, J or K	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	
ΙΗ	PRE or CLR	ACC = 2.2 A	V = 2.7 V			40			40	μΑ
1.	CLK, J or K	V 55V	V 0.4.V			-0.5			0.5	^
ΙL	PRE or CLR	$V_{CC} = 5.5 V$	V _I = 0.4 V			- 1.8			- 1.8	mA
10 [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
lcc		$V_{CC} = 5.5 V,$	See Note 1		11.5	17		11.5	17	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4$. $C_L = 50$ $R_L = 500$ $T_A = MIN$	pF, Ω, I to MAX		UNIT
1			SN54	AS109	SN74	AS109	
			MIN	MAX	MIN	MAX	
f _{max}			90		105		MHz
^t PLH	PRE or CLR	Q or $\overline{\mathbf{Q}}$	3	9	3	8	
tPHL	PRE OF CER	4 61 4	3.5	11.5	3.5	10.5	ns
tPLH	CLK	Q or Q	3.5	10	3.5	9	ns
tPHL	CLK	4014	4.5	10.5	4.5	9	IIIS



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios. NOTE 1: ICC is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

SN54ALS112A. SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2661, APRIL 1982-REVISED MAY 1986

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS112A	50 MHz	6 mW

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

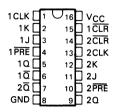
The SN54ALS112A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS112A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

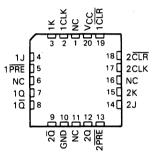
		NPUTS			OUT	PUTS
PRE	CLR	CLK	J	K	a	ā
L	Н	X	X	X	Н	٦
Н	L	X	X	X	L	н
L	L	X	X	X	H [†]	H [†]
Н	Н	1	L	L	00	\overline{a}_0
ĺН	Н	1	Н	L	Н	L
Н	Н	1	L	Н	L	н
Н	Н	Ţ	н	Н	TOG	GLE
Н	Н	Н	Χ_	Х	QΟ	\overline{a}_0

[†]The output levels in this configuration are not guaranteed to meet the minimum levels for VOH. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS112A . . . J PACKAGE SN74ALS112A . . . D OR N PACKAGE (TOP VIEW)

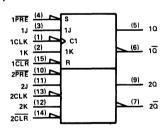


SN54ALS112A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol‡

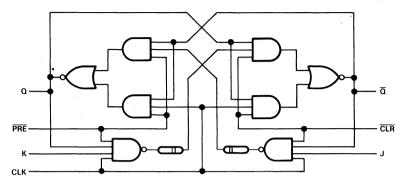


[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS112A, SN74ALS112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS	3112A – 55°C to 125°C
SN74ALS	6112A
Storage temperature range	-65°C to 150°C

recommended operating conditions

	,		SN	54ALS1	12A	SN:	74ALS1	12A	
		•	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	3	2			2			V
VIL	Low-level input voltage	!		***************************************	0.7			0.8	V
lOH.	High-level output curre	nt			-0.4			-0.4	mA
lOL	Low-level output currer	nt			4			8	mA
f _{clock}	Clock frequency		0		25	,0		30	MHz
		PRE or CLR low	15			10			
t_{W}	Pulse duration	CLK high	20			16.5			ns
		CLK low	20			16.5			
	Setup time	Data	25			22			
t _{su}	before CLK↓	PRE or CLR inactive	22			20			ns
th	Hold time, data after C	LK↓	0			0			ns
TA	Operating free-air temp	erature	- 55		125	0		70	°C



SN54ALS112A, SN74ALS112A DUAL J.K NEGATIVE EDGE TRIGGERED FLIP FLOPS WITH CLEAR AND PRESET

electrical characteristice over recommended operating free-air temperature range (unless otherwise noted)

	40445750	TEAT CONDITIO		SN	54ALS1	12A	SNZ	4ALS1	12A	
۲	ARAMETER	TEST CONDITIO	JNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.5			- 1.5	V
Vон		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -2			V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 V$	IOL = 8 mA					0.35	0.5	v
	J, K, or CLK	V 55.V	., .,			0.1			0.1	
41	PRE or CLR	$V_{CC} = 5.5 V$,	V _I = 7 V			0.2			0.2	mA
1	J, K, or CLK	V	V. 27V			20			20	
ΉΗ	PRE or CLR	$V_{CC} = 5.5 V$,	V _I = 2.7 V			40			40	μΑ
l	J, K, or CLK	V	V: 0.4.V			-0.2			-0.2	^
ηL	PRE or CLR	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.4			-0.4	mA
10‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
Icc		V _{CC} = 5.5 V,	See Note 1		2.5	4.5		2.5	4.5	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	ТО (О U ТРUT)		V _{CC} = 4.5 C _L = 50 pF R _L = 500 Ω T _A = MIN t	, o MAX		UNIT
			SN54A	LS112A	SN74AL	LS112A	
			MIN	MAX	MIN	MAX	
f _{max}			25		30		MHz
tPLH	PRE or CLR	Q or $\overline{\mathbb{Q}}$. 3	26	3	15	
^t PHL	- FRE OF CER	2 07 0	4	23	4	18	ns
^t PLH	CLK	Q or $\overline{\Omega}$	3	23	3	15	no.
tPHL		2014	5	24	5	19	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios. NOTE 1: ICC is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

SN54ALS113A, SN74ALS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2261, APRIL 1982-REVISED MAY 1986

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS113A	40 MHz ($C_L = 15 pF$)	6 mW

description

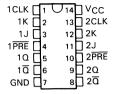
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS113A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74ALS113A is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

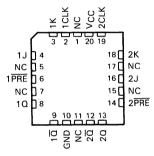
FUNCTION TABLE

	INPUTS								
PRE	PRE CLK J K				ā				
L	×	Х	Х	Н	L				
н	1	L	L.	a_0	\bar{a}_0				
н	1	н	L	н	L				
н	1	L	Н	L	н				
н	1	н	Н	TOG	GLE				
н	Н	×	×	00	\bar{a}_0				

SN54ALS113A . . . J PACKAGE SN74ALS113A . . . D OR N PACKAGE (TOP VIEW)

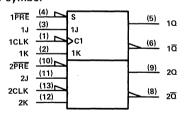


SN54ALS113A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

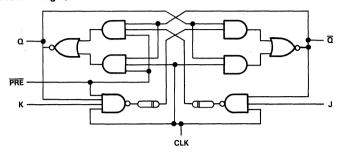
logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS113A	-55°C to 125°C
SN74ALS113A	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			S	N54ALS	113A	SN	74ALS1	13A	LIAUT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input volta	ge	2			2			V	
V _{IL}	Low-level input voltage	Low-level input voltage			0.7			0.8	V	
IOH	High-level output curi	High-level output current			-0.4			-0.4	mA	
lOL	Low-level output current				4			8	mA	
fclock	Clock frequency		0		25	0		30	MHz	
	Pulse duration	PRE low	20			10			ns	
t _w		CLK high	20			16.5				
		CLK low	20			16.5				
	Setup time	Data	25			22			ns	
^t su	before CLK↓	PRE inactive	25			20			118	
th	Hold time, data after CLK↓		0			0			ns	
TA	Operating free-air ten	perature	- 55		125	٥		70	°C	

SN54ALS113A, SN74ALS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

electrical characteristics over recommended operating free-air temperature range (unless otherwise

		TEAT COUR	TIONS.	SN	54ALS1	13A	SN74ALS113A			UNIT
PA	RAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			- 1.5			-1.5	V
Voн		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$I_{OH} = 0.4 \text{ mA}$	V _{CC} -2			Vcc-	2		V
Vol		$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
• OL		$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5	· ·
1.	J, K, or CLK	Vac = 5.5.V V	V _I = 7 V			0.1			0.1	mA
lj	$\frac{V_{CC}}{PRE}$ $V_{CC} = 5.5 \text{ V},$	vCC = 5.5 v,	V = 7 V			0.2			0.2	IIIA
l	J, K, or CLK	Vac - 5.5.V	V _I = 2.7 V			- 20			20	μΑ
ΊΗ	PRE	$V_{CC} = 5.5 V,$	V - 2.7 V			40			40	μΑ
1	J, K, or CLK	$V_{CC} = 5.5 V_{r}$	V _I = 0.4 V			-0.2			-0.2	mA
IIL	PRE	vCC = 5.5 v,	VI = 0.4 V			-0.4			-0.4	IIIA
10‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Icc		$V_{CC} = 5.5 V,$	See Note 1		2.5	4.5		2.5	4.5	mA

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = MIN$	F, Ω,	V,	UNIT
			SN54AL	.S113A	SN74	SN74ALS113A	
			MIN	MAX	MIN	MAX	
fmax			25		30		MHz
t _{PLH}	PRE	Q or $\overline{\mathbb{Q}}$	3	23	3	14	
tPHL	FNE	2012	4	26	4	16	ns
t _{PLH}	CLK	Q or $\overline{\Omega}$	3 ·	22	3	15	
^t PHL	CLK d or d	5	23	5	19	ns	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

SN54ALS114A, SN74ALS114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET. COMMON CLEAR. AND COMMON CLOCK

D2661, DECEMBER 1982-REVISED MAY 1986

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Typical Maximum Clock Frequency
 . . . 40 MHz
- Typical Power Dissipation per Flip-Flop . . . 6 mW
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS114A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS114A is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE

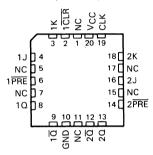
		OUTPUTS				
PRE	CLR	CLK	J	K	Q	ā
L	Н	X	Х	Х	Н	L
Н	L	X	X	X	L	Н
L	L	X	X	X	H*	H*
н	Н	1 .	L	L	a_0	\overline{a}_{O}
н	Н	1	н	L	Н	L
Н	Н	1	L	Н	L	Н
н	Н	1	Н	Н	TOG	GLE
Н	Н	Н	X	X	σo	₫o

^{*} The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54ALS114A . . . J PACKAGE SN74ALS114A . . . D OR N PACKAGE (TOP VIEW)

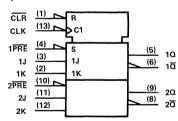
CLR	10	14	□vcc
1K 🛚	2	13	CLK
1J 🛚	3	12] 2K
1PRE	4	11] 2J
10 🗌	5	10	2PRE
10 □	6	9] 2Q
GND 🗌	7	8	20

SN54ALS114A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol†



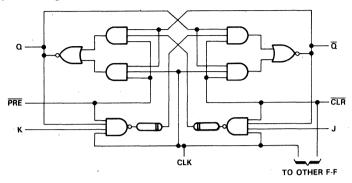
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for D. J. and N packages.



SN54ALS114A, SN74ALS114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	7 V
Operating free-air temperature range:	SN54ALS114A
	SN74ALS114A 0 °C to 70 °C
Storage temperature range	65°C to 150°C

recommended operating conditions

			SN	54ALS1	14A	SN	SN74ALS114A			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	High-level input voltage				2	-		V	
VIL	Low-level input voltage				0.7			0.8	V	
ЮН	High-level output current	High-level output current			-0.4			0.4	mA	
loL	Low-level output current				4			8	mA	
fclock	Clock frequency		0		25	0		30	MHz	
		PRE or CLR low	20			10				
t _w	Pulse duration	CLK high	20			16.5			ns	
		CLK low	20			16.5				
	Setup time	Data	25			22				
t _{su}	before CLK↓	PRE or CLR inactive	25			20	***************************************	-0.4	ns	
th	Hold time, data after CLK		0			0			ns	
TA	Operating free-air tempera	ture	- 55		125	0		70	°C	

SN54ALS114A, SN74ALS114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

_	ARAMETER	TEST CONDITIONS		SN	SN54ALS114A			SN74ALS114A		
	ANAIVIETEN			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.5			- 1.5	V
Vон		$V_{CC} = 4.5 \text{ V to 5}.$	5 V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	. ,		V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4				V
L VOL		$V_{CC} = 4.5 V,$	IOL = 8 mA					0.35	0.5	\
l ₁	J, K, or CLK	Vcc = 5.5 V,	V _I = 7 V			0.1			0.1	mA
"	PRE or CLR	· (C = 0.0 v,	., ., .			0.2			0.2	} '''`
ΉΗ	J, K, or CLK	V _{CC} = 5.5 V,	$C = 5.5 \text{ V}, \qquad V_1 = 2.7 \text{ V}$			20			20	μА
'IH	PRE or CLR	VCC = 5.5 V,	V - 2.7 V			40			40	μΑ
IIL	J, K, or CLK	Vcc = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
11	PRE or CLR	VCC = 5.5 V,	VCC = 5.5 V, V = 0.4 V			-0.4			-0.4	IIIA
lo‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
Icc		$V_{CC} = 5.5 V,$	See Note 1		2.5	4.5		2.5	4.5	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ p}$ $R_L = 500$ $T_A = MIN$	F, Ω,	v .	UNIT
			SN54ALS114A		SN74ALS114A		
			MIN	MAX	MIN	MAX	
f _{max}			25		30		MHz
^t PLH	PRE or CLR	Q or $\overline{\mathbb{Q}}$	3	29	3	15	ns
^t PHL	THE OF CER	4 6/ 4	4	30	4	18.	115
^t PLH	CLK	Q or $\overline{\mathbf{Q}}$	3	28	3	15	ns
^t PHL		1 2514	5	31	5	19	115

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los. NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

SN54ALS131, SN54AS131A, SN74ALS131, SN74AS131A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS REGISTERS

D2661, APRIL 1982-REVISED MAY 1986

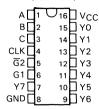
- Combines Decoder and 3-Bit Address Register
- Incorporates 2 Enable Inputs to Simplify Cascading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

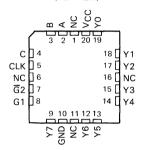
The 'ALS131 and 'AS131A are three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock input (CLK) goes from low to high, the 'ALS131 and 'AS131A act as decoders/demultiplexers and the address present at the select inputs (A. B, and C) is stored in the registers. Further address changes are ignored until the next rising transition of CLK. The output enable controls, G1 and $\overline{G}2$, control the state of the outputs independently of the select or CLK inputs. All of the outputs are high unless G1 is high and G2 is low. The 'ALS131 and 'ALS131A are ideally suited for implementing alitch-free decoders in strobed (stored-address) applications in busoriented systems.

The SN54ALS131 and SN54AS131A are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS131 and SN74AS131A are characterized for operation from 0 °C to 70 °C.

SN54ALS131, SN54AS131A . . . J PACKAGE SN74ALS131, SN74AS131A . . . D OR N PACKAGE (TOP VIEW)

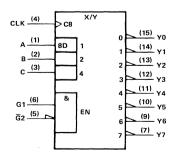


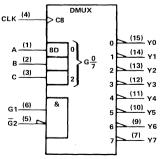
SN54ALS131, SN54AS131A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbols † (alternatives)

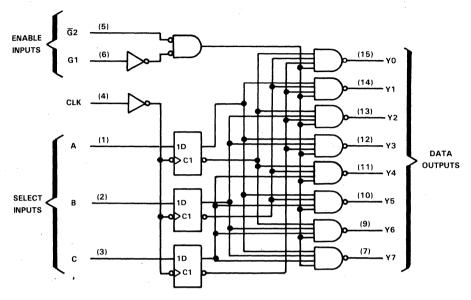




[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.



logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

		INPL	JTS										
CLK	EN/	ABLE	S	ELEC	T				OUT	PUTS	.		
	G1	Ğ2	С	В	Α	YO	Y1	Y2	Υ3	Y4	Y5	Υ6	Y7
Х	Х	Н	Х	X	X	Н	Н	Н	Н	Н	Н	Н	Н
X	L	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
1	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
1	н	L	L	. F	Н	Н	L	Н	Н	Н	Н	Н	Н
1	н	L	L	Н	L	н	Н	L	Н	Н	Н	Н	Н
1	н	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	Н
1	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
1	н	L	н	L	н	Н	Н	Н	Н	Н	L	Н	Н
1	Н	L	Н	Н	L	н	Н	Н	Н	Н	Н	L	Н
1	Н	L	Н	Н	Н	н	Н	Н	Н	Н	Н	Н	L
L,						OUTPUTS CORRESPONDING							3
or	Н	L	x	X	Χ	TO STORED ADDRESS, L;							
Н							ALL	отн	ERS,	Н			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	
Operating free-air temperature range:	SN54ALS131, SN54AS131A55°C to 125°C
	SN74ALS131, SN74AS131A 0°C to 70°C
Storage temperature	−65°C to 150°C



SN54ALS131, SN74ALS131 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS REGISTERS

recommended operating conditions

			S	N54ALS	131	SN	74ALS1	31	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
v_{IH}	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
Іон	High-level output current				-0.4			-0.4	mA
lOL	Low-level output current				4			8	mA
^f clock	Clock frequency		0		40	0		50	MHz
•	Pulse duration	CLK high	12.5			10			
t _w	ruise duration	CLK low	12.5			10			ns
t _{su}	Setup time at A, B, and C before	e CLK†	15			10			ns
th	Hold time at A, B, and C after C	LK ↑	0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETIONS	SN54ALS131	SN74ALS131	UNIT
PARAMETER	TEST CONDITIONS	MIN TYP† MAX	MIN TYP† MAX	ONIT
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$	-1.5	-1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2	V _{CC} -2	V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 4 \text{ mA}$	0.25 0.4	0.25 0.4	
VOL	V _{CC} = 4.5 V, I _{OL} = 8 mA		0.35 0.5	\ \ \
11	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$	0.1	0.1	mA
ήн	$V_{CC} = 5.5 \text{ V}, \qquad V_{i} = 2.7 \text{ V}$	20	20	μΑ
I _{IL}	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$	-0.1	-0.1	mA
10 [‡]	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$	-30 -112	-30 -112	mA
lcc	V _{CC} = 5.5 V	5 11	5 11	mA

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$V_{CC} = 4$ $C_L = 50$ $R_L = 500$ $T_A = MIN$ ALS131 MAX	pF,) Ω, N to MAX	5 V, ALS131 MAX	UNIT
f _{max}			40		50		MHz
tPLH	CLK	V	8	28	8	25	ns
tPHL	CLK	,	7	24	7	20	115
tPLH	C1		7	24	7	20	ns
tPHL	G1	, , , , , , , , , , , , , , , , , , , ,	6	20	6	17	113
tPLH	G2	Y	5	18	5	15	ns
tPHL	GZ	'	. 5	18	5	15	113

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

recommended operating conditions

			SN	54AS13	31A	SN7	4AS13	1A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V.
V _{IL}	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				- 2			-2	mA
IOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		90	0		100	MHz
	Pulse duration	CLK high	5.5			5			ns
tw	ruise duration	CLK low	5.5			5			115
t _{su}	Setup time at A, B, and C before	ore CLK1	3.5			3.5			ns
th	Hold time at A, B, and C after	CLK↑	1			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	 s	N54AS	131A	SI	174AS1	31A	UNIT
PANAMETEN	TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2		٧
V _{OL}	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V
4	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$			20			20	μΑ
ΊL	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$			-0.5			-0.5	mA
lo [‡]	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
¹ ссн	V _{CC} = 5.5 V		15	29		15	29	mA
ICCL	$V_{CC} = 5.5 V$		16	30		16	30	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SNEA	$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = \text{MIN t}$ $AS131A$, , o MAX	/, AS131A	UNIT
		•	MIN	MAX	MIN	MAX	
f _{max}			90		100		MHz
^t PLH	CLK	Y	2	15	2	14.5	
^t PHL	CLK	ľ	2	10	2	9.5	ns
^t PLH	G1	Y	2	10.5	2	10	
^t PHL	<u> </u>	<u>'</u>	2	. 9	2	9	ns
tPLH	G2	v .	2	7.5	2	7	ns
^t PHL		<u> </u>	2	8.5	2	8.5	115



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS133, SN74ALS133 13-INPUT POSITIVE-NAND GATES

D2661, APRIL 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain a single 13-input NAND gate. They perform the Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

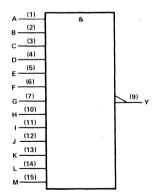
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54ALS133 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS133 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

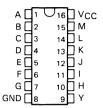
INPUTS A THRU M	OUTPUT
INTOTS A TIMO W	Υ
All inputs H	٦
One or more inputs L	н

logic symbol†

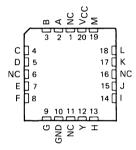


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS133 . . . J PACKAGE SN74ALS133 . . . D OR N PACKAGE (TOP VIEW)

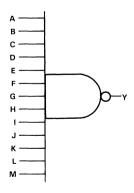


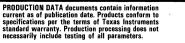
SN54ALS133 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic diagram (positive logic)







Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) SN74ALS133 0 °C to 70 °C

recommended operating conditions

		SN	54ALS1	133	SN	74ALS1	133	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон .	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	TEST CONDITIONS			133	SN	74ALS	133	UNIT
PARAMETER	TEST CONDI	ITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} - 2			V
V _{OL}	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	IOL = 8 mA					0.35	0.5	l
ή	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
ΙΙL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1			-0.1	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
ıссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.24	0.34		0.24	0.34	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		0.56	0.8		0.56	0.8	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$		<i>'.</i>	UNIT		
			'ALS133	SN54/	ALS133	SN74#	ALS133	l
			TYP	MIN	MAX	MIN	MAX	
t _{PLH}	Any	Y	8	1	16	3	11	ns
tPHL	Any	Υ	17	5	47	5	25	ns



[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS136, SN54AS136, SN74ALS136, SN74AS136 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

D2837, MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS136, SN54AS136 . . . J PACKAGE SN74ALS136, SN74AS136 . . . D OR N PACKAGE (TOP VIEW)

1A 🛮	1	U 14	□vcc
18□	2	13	☐ 4B
1 Y 🗌	3	12] 4A
2A 🗌	4	11] 4Y
2B 🗌	5	10] 3B
2Y 🗌	6	9] 3A
$NP\square$	٦,	0	1 3 V

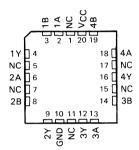
description

These devices contain four independent Exclusive-OR gates with open-collector outputs. They perform the Boolean functions $Y = A \bigoplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS136 and SN54AS136 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS136 and SN74AS136 are characterized for operation from 0 °C to 70 °C.

SN54ALS136, SN54AS136 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol[†]

1A (1)	=1 Q	(3) 1Y
1B (4)	~	,,,
1A (2) 1B (4) 2A (5)		(6) 2Y
(9)		(8)
3A (10) 3B (12)		
4A (12) 4B (13)		(11) 4Y
40	r I	

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
L	L	L
L	Н	н
Н	L	н
Н	Н	L

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

exclusive-OR logic

An Exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

These are five equivalent Exclusive-OR symbols valid for an 'ALS136 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

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SN54ALS136, SN74ALS136 QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Off-state output voltage		7 V
Operating free-air temperature range:	SN54ALS136	-55°C to 125°C
	SN74ALS136	0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SI	SN54ALS136			SN74ALS136			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Vон	High-level output voltage			5.5			5.5	V	
lOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TFOT (SN	154ALS1	136	SN				
	1651 (CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			-1.5	V
Т ОН	$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V			0.1			0.1	mA
V	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL -	V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	ľ
lj .	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IIL III	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
lcc	$V_{CC} = 5.5 V,$	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 R _L = 2 k	-	V,	UNIT
	1	i		SN54ALS136		SN74ALS136	
			MIN	MAX	MIN	MAX	
tPLH .	A or B	V	20	55	20	50	ns
^t PHL	(other input low)	1	3	18	3	15	115
^t PLH	A or B	· ·	20	55	20	50	ns
tPHL	(other input high)	· .	3	15	3	12	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



PRODUCT PREVIEW

SN54AS136, SN74AS136 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		7 V
Off-state output voltage		7 V
Operating free-air temperature range:	SN54AS136	-55°C to 125°C
	SN74AS136	0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SI	SN54AS136			SN74AS136			
		MIN	MIN NOM MAX MIN N		NOM	MAX	UNIT		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
Voн	High-level output voltage			5.5			5.5	V	
IOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT OF	TEST CONDITIONS			SN74AS86			UNIT
PARAMETER	IESI CO	MIN TYP†	MAX	MIN	TYP^{\dagger}	MAX	UNII	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA		- 1.5			-1.5	V
Юн	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V		2			2	mA
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA	0.35	0.5		0.35	0.5	V
l _l	V _{CC} = 5.5 V,	V _I = 7 V		0.1			0.1	mA
ŀн	$V_{CC} = 5.5 V,$	$V_1 = 2.7 \text{ V}$		20			20	μΑ
l _I L	$V_{CC} = 5.5 V,$	V ₁ = 0.4 V		-01			-0.1	mA
Іссн	$V_{CC} = 5.5 V$		18			18		mA
ICCL	V _{CC} = 5.5 V		15			15		mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$\begin{array}{l} V_{CC} = 4.8 \\ C_L = 50 \text{ p} \\ R_L = 2 \text{ k} \Omega \\ T_A = \text{MIN} \end{array}$	UNIT			
			SN54AS136	SN74AS136			
			MIN TYP† MAX	MIN TYP† MAX			
^t PLH	A or B	V	10.5	10.5	ns		
^t PHL	(other input low)	'	4.3	4.3] ""		
^t PLH	A or B		10.5	10.5			
^t PHL	(other input high)	ther input high)		4.3	ns		

 $^{^{\}dagger}$ All typical valves are at VCC = 5 V, TA = 25 °C.



SN54ALS137, SN54AS137, SN74ALS137, SN74AS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

D2661, APRIL 1982-REVISED MAY 1986.

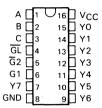
- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Output Enables to Simplify Cascading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

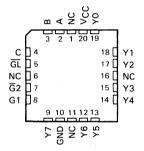
The 'ALS137 and 'AS137 are three-line to eightline decoder/demultiplexer with latches on the three address inputs. When the latch-enable input (GL) is low, the 'ALS137 and 'AS137 acts as a decoder/demultiplexer. When GL goes from low to high, the address present at the select inputs (A. B. and C) is stored in the latches. Further address changes are ignored as long as GL remains high. The output enable controls, G1 and $\overline{G}2$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G}2$ is high. The 'ALS137 and 'AS137 are ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54ALS137 and SN54AS137 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS137 and SN74AS137 are characterized for operation from 0 °C to 70 °C.

SN54ALS137, SN54AS137 . . . J PACKAGE SN74ALS137, SN74AS137 . . . D OR N PACKAGE (TOP VIEW)

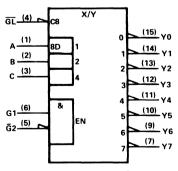


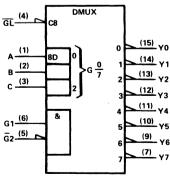
SN54ALS137, SN54AS137 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

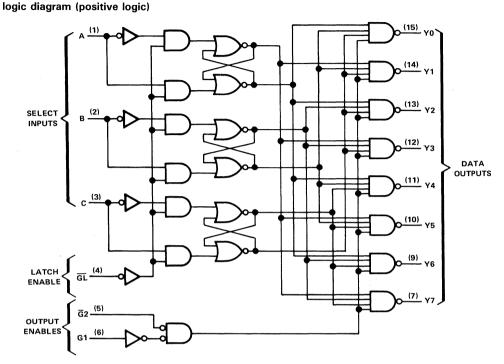
logic symbols (alternatives)†





[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.





Pin numbers shown are for D, J, and N packages.

FUNCTION TABLE

	INPUTS								UTI				
ENABLE			SE	LE	СТ				,011	-01			
GL	G1	G2	С	В	Α	YO	Υ1	Y2	Υ3	Ý4	Y5	Y6	Y7
Х	Х	Н	х	Х	Х	Н	Н	Н	Н	Н	Н	Н	н
х	L	х	×	Х	Х	н	Н	Н	Н	Н	Н	Н	н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	н	н	L	Н	Н	Н	Н	H	н
Ł	Н	L	L	н	L	н	Н	L	H	Н	Н	Н	н
L	Н	L	L	Н	Н	н	Н	Н	L	Н	Н	Н	н
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	I
L	Н	L	н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	Н	L	н	Н	L	н	Н	Н	Н	Н	Н	L	Η:
L	Н	L	н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
Н	ы	L	V		_	Out	put	corre	espoi	ndin	g to	store	d
Ľ	H L X X X address, L; all others, H												

SN54ALS137, SN54AS137, SN74ALS137, SN74AS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54ALS137, SN54AS137 55 °C to 125 °C
SN74ALS137, SN74AS1370°C to 70°C
Storage temperature

recommended operating conditions

		S	N54ALS	137	SN	74ALS1	37	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	CIVIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
IOL	Low-level output current		-	4			8	mA
t _w	Pulse duration, GL low	15			10			ns
t _{su}	Setup time at A, B, and C before GL1	15			10			ns
th	Hold time at A, B, and C after GL1	5			5			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETIONS		SI	SN54ALS137			SN74ALS137			
PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	1	
VIK	$V_{CC} = 4.5 \text{ V}, \text{II}$	= -18 mA			- 1.5			- 1.5	V	
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{C}$	H = -0.4 mA	V _{CC} -	2		Vcc-	2		V	
Vai	$V_{CC} = 4.5 \text{ V},$ IC	L = 4 mA		0.25	0.4		0.25	0.4	V	
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{C}$	L = 8 mA					0.35	0.5	ľ	
l($V_{CC} = 5.5 \text{ V}, \qquad V$	= 7 V			0.1			0.1	mA	
ЧН	$V_{CC} = 5.5 \text{ V}, V_{CC}$	= 2.7 V			20			20	μΑ	
ИL	$V_{CC} = 5.5 \text{ V}, \qquad \text{V}$	= 0.4 V			-0.1			-0.1	mA	
10 [‡]	$V_{CC} = 5.5 \text{ V}, V_{CC}$	O = 2.25 V	- 30		-112	- 30		-112	mA	
Icc	V _{CC} = 5.5 V			5	11		5	11	mA	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$C_L = 50$ $R_L = 500$ $T_A = MII$	Ω, N to MAX		UNIT
			SN54	ALS137	SN74/	ALS137	1
			MIN	MAX	MIN	MAX	
t _{PLH}	A, B, C	A. B. C		25	5	20	
t _{PHL}	Α, Β, C	'	6	25	6	20	ns
. tplh	G2	Υ	4	15	4	12	
^t PHL	G2	'	5	18	5	15	ns
t _{PLH}	G1	Y	5	21	5	17	
^t PHL] "		5	19	5	15	ns
t _{PLH}	tpi H	Y	7	27	7	22	
^t PHL	GL GL	'	7	25	7	20	ns



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

recommended operating conditions

			N54AS	137	S	N74AS1	37	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2.			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			- 2			- 2	mA
lOL	Low-level output current			20			20	mA
t _w	Pulse duration, GL low	5			4.5			ns
t _{su}	Setup times at A, B, and C before \overline{GL} 1	4.5			4			ns
th	Hold time at A, B, and C after GL1	1			1			ns
TA	Operating free-air temperature	- 55		125	0		70	°C ,

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEAT COMPLETOR		8	N54AS	137	SN	UNIT		
PARAMETER	TEST CONDITION	MIN	TYP	MAX	MIN	TYP [†]	MAX	UNII	
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18^{\circ} \text{mA}$			-1.2	-		-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2	!		Vcc -	- 2		V
VOL	$V_{CC} = 4.5 V$,	IOL = 20 mA		0.35	0.5		0.35	0.5	V
1	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
¹ıн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 1		*.	- 1	mA
1 ₀ ‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
^I cc	$V_{CC} = 5.5 V$			15	24		15	24	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	PARAMETER FROM TO (INPUT) (OUTPUT)		C F	$C_{CC} = 4.5$ $C_{L} = 50 \text{ pf}$ $C_{L} = 500 \text{ s}$ $C_{L} = 500 \text{ s}$:, ⊋, to MAX	V, AS137	UNIT
			MIN	MAX	MIN	MAX	
tPLH			2	14	2	12.5	
tPHL	A, B, C	Υ	2	14	2	12.5	ns
. tplH	G ₂	Υ	. 2	9	2	8	
^t PHL	1 62	ř	2	9	2	8.5	ns
^t PLH	G1	Υ	2	11	2	10	ns
^t PHL		•	2	10	2	9	'''
tpLH	GL .	Υ	2	14.5	3	13.5	200
tpHL		·	2	15	3	14	ns



[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS138, SN54AS138, SN74ALS138, SN74AS138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

D2661, APRIL 1982-REVISED MAY 1986

- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

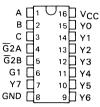
description

The 'ALS138 and 'AS138 circuits are designed to be used in high-performance memorydecoding or data-routing applications requiring very short propagation delay times. In highperformance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

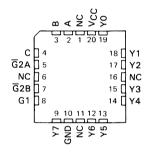
The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54ALS138 and SN54AS138 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS138 and SN74AS138 characterized for operation from 0°C to 70°C.

SN54ALS138, SN54AS138 . . . J PACKAGE SN74ALS138, SN74AS138 . . . D OR N PACKAGE (TOP VIEW)

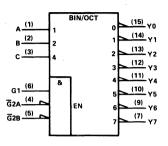


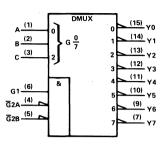
SN54ALS138, SN54AS138 . . . FK PACKAGE (TOP VIEW)



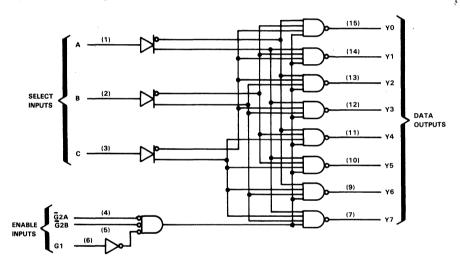
NC-No internal connection

logic symbols (alternatives)†





logic diagram (positive logic)



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

SN54ALS138, SN54AS138, SN74ALS138, SN74AS138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

FUNCTION TABLE

	ENABL INPUTS			SELECT INPUTS			OUTPUTS						
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	X	X	Н	Н	Н	Н	Н	Н	Н	Н
Х	Χ	Н	×	X	X	Н	Н	Н	Н	Н	Н	Н	Н
L	Х	Χ	×	X	X	н	Н	Н	Н	Н	Н	Н	Н
Н	L	L.	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
Н	L	L	L	Н	L	н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	L	Н	L	Н	н	Н	Н	Н	Н	L	Н	Н
Н	L	L	Н	Н	L	н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Н	Н	Н	н	Н	Н	Н	Н	Н	Н	L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, vCC	
Input voltage	7 V
Operating free-air temperature range; SN54ALS138, SN54AS138	-55°C to 125°C
SN74ALS138, SN74AS138	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		Si	154ALS	138	SN	74ALS1	38	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONI
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ПОН	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLETIONS		SN54ALS138			S	LIAUT		
PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{ } = -18 \text{ mA}$				- 1.5			- 1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$		vcc-	2	1	v _{cc} -	2		٧
Voi	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 4 \text{ mA}$			0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 8 \text{ mA}$						0.35	0.5]
l _l	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$				0.1			0.1	mA
ЧН	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$				20			20	μΑ
l _{IL}	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$				-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$		- 30		- 112	- 30		-112	mA
¹ CC	V _{CC} = 5.5 V			5	10		5	10	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS138, SN74ALS138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MIR	Ω,	V,	UNIT
	'		SN54	ALS138	SN74/	ALS138	
			MIN	MAX	MIN	MAX	
^t PLH	A, B, C	Any Y	2	28	6	22	
t _{PHL}	1 4, 5, 6	Ally 1	6	22	. 6	18	ns
tPLH	Enable	Any Y	2	22	4	17	
^t PHL	Enable	Ally 1	· 4	21	- 5	17	ns

SN54AS138, SN74AS138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

		Si	N54AS1	38	SN74AS138		UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ПОН	High-level output current			- 2			- 2	mA
IOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	ER TEST CONDITIONS		8	N54AS	138	S	N74AS	138	LINUT
PARAMETER			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	t _I = -18 mA			-1.2			- 1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -	2	*	Vcc-	2		V
V _{OL}	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
11	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1			0.1	mA
IН	V _{CC} = 5.5 V,	$V_{ } = 2.7 \text{ V}$			20			20	μΑ
HL	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.5			-0.5	mA
10‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
¹ ссн	V _{CC} = 5.5 V			12	17.5		12	17.5	mA
^I CCL	V _{CC} = 5,5 V			14	20		14	20	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _I	V_{CC} 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX			UNIT
			SN54A	S138	SN744	\S138	1
			MIN	MAX	MIN	MAX	
^t PLH	A B C	A, B, C Any Y	2	11	2	10	
[†] PHL	A, B, C		2	11	2	9.5	ns
^t PLH	G1	Any Y	2	11.5	2	10	ns
[†] PHL]	Ally	2	11	2	10	'''5
^t PLH	G2	Any Y	2	9	2	7.5	
^t PHL] 32	Any i	2	10	2	8.5	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS139, SN54AS139, SN74ALS139, SN74AS139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

D2661, APRIL 1982-REVISED MAY 1986

- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

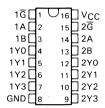
description

The 'ALS139 and 'AS139 circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

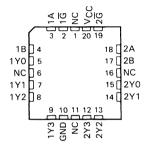
The 'ALS139 and 'AS139 are comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

The SN54ALS139 and SN54AS139 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS139 and SN74AS139 are characterized for operation from 0°C to 70°C.

SN54ALS139, SN54AS139 . . . J PACKAGE SN74ALS139, SN74AS139 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS139, SN54AS139 . . . FK PACKAGE (TOP VIEW)



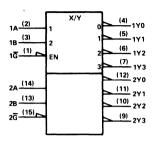
NC-No internal connection

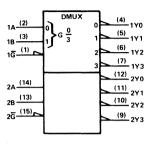
FUNCTION TABLE

INPUTS				OUTPUTS					
BLE SE	SELECT				,011	-014			
В		Α	Γ	YO	Y1	Y2	Υ3		
×		Х	Ι	Н	Н	Н	Н		
L		L	l	L	Н	Н	Н		
L		H		Н	L	Н	Н		
Н	١	L	l	Н	Н	L	Н		
Н	ı	Н		Н	Н	Н	L		
X L L		X		H L H	H H L	H H L			

SN54ALS139, SN54AS139, SN74ALS139, SN74AS139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

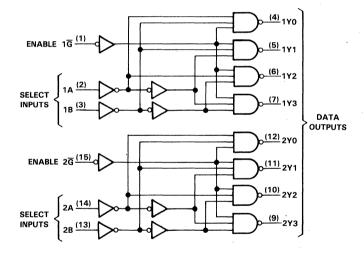
logic symbols[†] (alternatives)





 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pins numbers shown are for D, J, and N packages.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	7 V
Input voltage	
Operating free-air temperature range:	SN54ALS139, SN54AS13955 °C to 125 °C
	SN74ALS139, SN74AS139 0°C to 70°C
Storage temperature range	-65°C to 150°C



SN54ALS139, SN74ALS139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

		SN	SN54ALS139		SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	ONII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VII	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	SN54ALS139			SN74ALS139		
PANAIVIETEN			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	Iį = -18 mA			-1.2			-1.2	V
V _{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -:	2		V _{CC} -2	2		V
VOL	$V_{CC} = 4.5 \text{ V},$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
\ VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	7 °
lj	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 V$			20			20	μΑ
IΙL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
lcc	V _{CC} = 5.5 V			8	13		8	13	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$ 'ALS139	SN54	$V_{CC} = 4.5$ $C_{L} = 50 \text{ pl}$ $R_{L} = 500 \text{ s}$ $T_{A} = \text{MIN}$ ALS139	=, ∩, to MAX	V,	UNIT
			TYP	MIN	MAX	MIN	MAX	1
t _{PLH}	A or B		9	3	17	3	14	
^t PHL	AOIB	'	9	3	17	3	14	ns
[†] PLH	G	V	9	3	. 17	3	14	ns
^t PHL		'	9	3	18	3	15] ''5

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

recommended operating conditions

		SN54AS139			SI	UNIT		
	·	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VII	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 2			- 2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	SN54AS139			SN74AS139			
PARAMETER			MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	٧	
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -2 \text{ mA}$	V _{CC} -2	2		Vcc-	2		V	
VoL	$V_{CC} = 4.5 V$,	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V	
lį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA	
ήн	$V_{CC} = 5.5 V$,	$V_{i} = 2.7 V$			20	1		20	μΑ	
lιΓ	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.5			-0.5	mΑ	
10 [‡]	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA	
^I cc	V _{CC} = 5.5 V			13			13		mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L}1 = 50 \Omega,$ $T_{A} = \text{MIN to MAX}$					
	((331, 31,	SN54AS139	SN74AS139]			
			MIN TYP [†] MAX	MIN TYP† MAX				
t _{PLH}	A or B	V	5.5	5.5	1			
tPHL	AUID	T	6	6	ns			
tPLH	G	V	5.5	5.5				
^t PHL	9	•	5	5	ns			

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS151, SN54AS151, SN74ALS151, SN74AS151 1 OF 8 DATA SELECTORS/MULTIPLEXERS

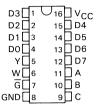
D2661, APRIL 1982-REVISED MAY 1986

 8-Line to 1-Line Multiplexers Can Perform As:

> Boolean Function Generators Parallel-to-Serial Converters Data Source Selectors

- Input Clamping Diodes Simplify System Design
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS151, SN54AS151 . . . J PACKAGE SN74ALS151, SN74AS151 . . . D OR N PACKAGE (TOP VIEW)

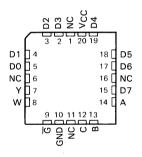


description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input $\overline{(G)}$ must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54ALS151 and SN54AS151 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS151 and SN74AS151 are characterized for operation from 0 °C to 70 °C.

SN54ALS151, SN54AS151 . . . FK PACKAGE (TOP VIEW)



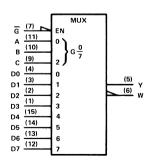
NC-No internal connection

FUNCTION TABLE

		INP	UTS	оит	PUTS
:	SELECT	г	STROBE	v	w
С	В	Α	G	_ '	
Х	Х	Х	Н	L	Н
L	L	L	L	DO	DO
L	L	Н	L	D1	D1
L	н	L	L	D2	D2
L	Н	н	L	D3	D3
Н	L	L	L	D4	D4
н	L	Н	L	D5	D5
Н	Н	L	L	D6	D6
Н	Н	Н	L	D7	D7

 $H = high\ level,\ L = low\ level,\ X = irrelevant$ DO, D1 . . . D7 = the level of the D respective input

logic symbol[†]



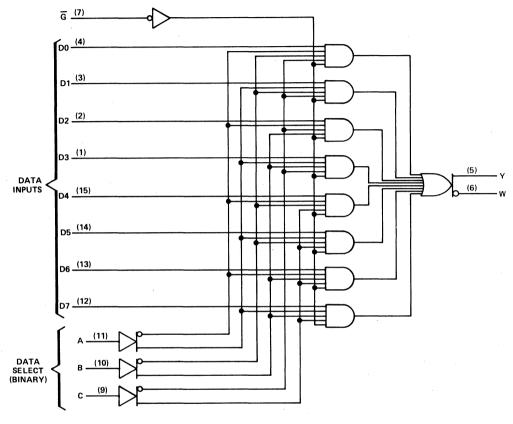
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



SN54ALS151, SN54AS151, SN74ALS151, SN74AS151 1 OF 8 DATA SELECTORS/MULTIPLEXERS

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS151, SN54AS151	55 °C to 125 °C
SN74ALS151, SN74AS151	0 °C to 70 °C
Storage temperature range	65 °C to 150°C

SN54ALS151, SN74ALS151 1 OF 8 DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

		SI	SN54ALS151		SN74ALS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
v_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			- 2.6	mA
loL	Low-level output current			12			24	mA
TΑ	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DARAMETER	TEST COMPLETIONS	SN54ALS151	SN74ALS1	51	UNIT
PARAMETER	TEST CONDITIONS	MIN TYP† MAX	MIN TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{\parallel} = -18 \text{ mA}$	- 1.5		-1.5	٧
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	V _{CC} -2		
Voн	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -1 \text{ mA}$	2.4 3.3			V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -2.6 \text{ mA}$		2.4 3.2		
V	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 12 \text{ mA}$	0.25 0.4	0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 24 \text{ mA}$		0.35	0.5	V
l _l	$V_{CC} = 5.5 \text{ V}, V_{I} = 7 \text{ V}$. 0.1		0.1	mA
ЧH	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$	20		20	μΑ
ΙΙL	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$	-0.1		-0.1	mA
lo‡	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$	-30 -112	- 30	- 112	mA
Icc	$V_{CC} = 5.5 \text{ V}, \qquad \text{Inputs at } 4.5 \text{ V}$	7.5 12	7.5	12	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $\boxed{\text{SN54ALS151}} \qquad \text{SN74ALS151}$				
			MIN	MAX 21	MIN	MAX	-	
tPLH tPLH	A, B, or C	Y	4		4	18	ns	
t _{PHL}			. 8	35	8	24	<u> </u>	
^t PLH	A, B, or C	l w	7	36	7	24	ns	
t _{PHL}		· · ·	7	26	7	23	'''	
tPLH	A D	Υ	3	14	3	10		
tPHL	Any D	Y	5	21	5	15	ns	
tPLH	Any D	w	3	23	3	15		
^t PHL	Ally D	**	4	20	4	15	ns	
[‡] PLH	G	Y	4	21	4	18	ns	
tPHL	١	1	4	25	4	19] "18	
tPLH	ਫ	w	5	27	5	19		
tpHL		\	5	26	5	23	ns	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

recommended operating conditions

		SN54AS151			S	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			- 12			- 15	mA
lOL	Low-level output current			-32			48	mA
TA	Operating free-air temperature	- 55		125	. 0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEGT CONDIT	IONIC	SI	154AS1	51	SN	74AS15	51	UNIT	
	PARAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	v _{cc} -	2		Vcc-	2			
Vон		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2.4	3.2					\ \ \	
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2.4	3.3			
Vai		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.5				_ v	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5		
1.	A, B, or C	V _{CC} = 5.5 V,	V _I = 7 V			0.2			0.2	mA	
=	All others	VCC = 5.5 V,	V = 7 V			0.1			0.1] ""	
1	A, B, or C	VCC = 5.5 V,	V _I = 2.7 V			40			40		
ΉΗ	All others	VCC = 5.5 V,	V = 2.7 V			20			20	μΑ	
1	A, B, or C	VCC = 5.5 V,	V _I = 0.4 V			- 1			- 1	mA	
ηL	All others	VCC = 5.5 V,	V = 0.4 V			-0.5			-0.5	l IIIA	
lo‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	-30		112	mA	
Icc		$V_{CC} = 5.5 \text{ V},$			18.6	30		18.6	30	mA	

 $^{^{\}dagger}AII$ typical values are at $V_{\mbox{\footnotesize CC}}~=~5$ V, $T_{\mbox{\footnotesize A}}~=~25\,^{o}C.$

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ R_L = 500 \ \Omega, \\ T_A = \text{MIN to MAX} \\ \hline \text{SN54AS151} & \text{SN74AS151} \\ \end{array}$					
			MIN	MAX	MIN	MAX	ļ		
tPLH	A, B, or C	. Y	4.5	16	4.5	14.5	ns		
^t PHL	., .,	•	4.5	16	4.5	15			
^t PLH	A P or C	w	4	14.5	4	12	ns		
^t PHL	A, B, or C	**	4	14.5	4	12] '''		
tPLH	A D	Y	3	11.5	3	10.5			
tPHL	Any D	Ť	3	12	3	11	ns		
tPLH		w	2	8	2	6.5			
tPHL	Any D	l vv	1	5.5	1	4.5	ns		
tPLH	G	Y	4.5	16	4.5	14			
tPHL	G	'	3	12.5	3	11	ns		
tPLH	G	W	1.5	7	1.5	6			
tPHL	U	, vv	3	11	3	10	ns		



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS153, SN54AS153, SN74ALS153, SN74AS153 DUAL 1 OF 4 DATA SELECTORS/MULTIPLEXERS

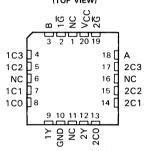
D2661, APRIL 1982-REVISED MAY 1986

- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- 'ALS253 and 'AS253 Are 3-State Versions of These Parts
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS153, SN54AS153 . . . J PACKAGE SN74ALS153, SN74AS153 . . . D OR N PACKAGE (TOP VIEW)

1G 1 16 Vc	·c
B	i
1C3 🛛 3 14 🗒 A	
1C2 4 13 2C	
1C1 5 12 2C	2
1C0 6 11 2C	: 1
1Y 🔲 7 10 🔲 2C	C
GND 🛛 8 9 🗍 2Y	•

SN54ALS153, SN54AS153 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

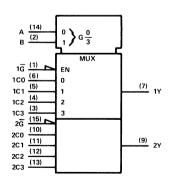
The SN54ALS153 and SN54AS153 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74ALS153 and SN74AS153 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

FUNCTION TABLE

	SELECT INPUTS		DATA	NPUTS	3	STROBE	ОUТРUТ	
В	Α	CO	C1	C2	С3	G	Υ	
×	×	×	X	X	X	Н	L	
L	L	L	X	X	×	L	L	
L	L	н	X	X	×	L	н	
L	н	×	L	X	×	L	L	
L	н	×	Н	X	×	L	н	
н	L	x	X	L	· x	L	L	
н	L	x	X	Н	×	L	н	
Н	Н	×	X	X	L	L	L	
н	н	x	X	Х	н	L	н	

Select inputs A and B are common to both sections.

logic symbol[†]

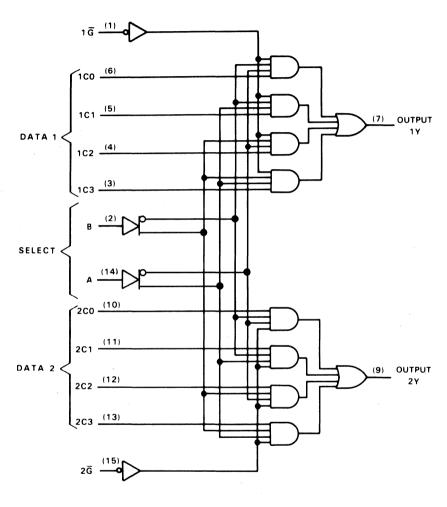


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



logic diagram (positive logic)



Pin numbers shown are D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	
Operating free-air temperature range:	SN54ALS153, SN54AS153 55 °C to 125 °C
	SN74ALS153, SN74AS153
Storage temperature range	



SN54ALS153, SN74ALS153 **DUAL 1 OF 4 DATA SELECTORS/MULTIPLEXERS**

recommended operating conditions

		SI	SN54ALS153			SN74ALS153			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			- 1			-2.6	mA	
lOL	Low-level output current			12			24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	154ALS	153	SN			
PARAMETER	I IEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		
Voн	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V _{OL}	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL.	V _{CC} = 4.5 V	I _{OL} = 24 mA					0.35	0.5	1 _
lj .	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lіН	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
ΙΙL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
IO‡	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
lcc	$V_{CC} = 5.5 V,$	All inputs at 4.5 V		7.5	14		7.5	14	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM TO (OUTPUT)			UNIT			
			SN54ALS153 SN74ALS153		ALS153		
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	Y	5	29	5	21	
^t PHL	A 01 B		5	27	5	21	ns
^t PLH	Data (Any C)	V	3	15	3	10	
tPHL	Data (Ally C)	T	2	18	4	15	ns
^t PLH	G	V	5	27	5	18	
tPHL	ď	*	3	22	5	18	ns

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

recommended operating conditions

	'	SN54AS163			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	Civil
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
ViL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 12			– 15	mA
loL	Low-level output current			32			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST COM	DITIONS	SI	V54AS1	53	SN	74AS15	53	LINUT	
	PARAMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	I _j = -18 mA			-1.2			-1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA ,	Vcc-	2		Vcc-	2			
∨он	$V_{CC} = 4.5 V$		IOH = -12 mA	2.4	3.2					7 v [
		V _{CC} = 4.5 V,	IOH = -15 mA				2.4	3.3		1	
Vai		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.5				V	
VOL		V _{CC} = 4.5 V	I _{OL} = 48 mA					0.35	0.5	1	
1.	А, В	V _{CC} = 5.5 V,	V _I = 7 V			0.2			0.2	mA	
11	All others	1 vCC = 5.5 v,				0.1			0.1] IIIA	
	А, В	V _{CC} = 5.5 V,	V _I = 2.7 V			40			40	μΑ	
ΉΗ	All others	VCC = 5.5 V,	V = 2.7 V			20			20] μΑ	
1	A, B	V _{CC} = 5.5 V,	V _I = 0.4 V			- 1			1	mA	
ηL	All others	vCC = 5.5 v,	V = 0.4 V		-0.5				-0.5] '''^	
lo‡		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA	
laa		V 5 5 V	Outputs high		16	26		16	26		
Icc		$V_{CC} = 5.5 V$	Outputs low		21	33		21	33	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MI	pF,) Ω,		UNIT
			SN54AS153 SN74AS153			1	
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	Y	3	14	3	12.5	ns
[†] PḤL	A 01 B		3	12.5	3	11	1 115
^t PLH	Data (Any C)		2	8	2	7	
t _{PHL}	Data (Ally C)	'	2	8.5	2	8	ns
tPLH	G		3	13	3	11.5	ns
^t PHL	d d	1	2	10	2	9] "



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN74ALS156 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN-COLLECTOR OUTPUTS

D2930, JUNE 1986

Applications:

Dual 2-Line to 4-Line Decoder
Dual 1-Line to 4-Line Demultiplexer
3-Line to 8-Line Decoder
1-Line to 8-Line Demultiplexer

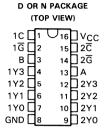
 Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words

description

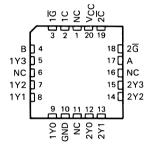
The 'ALS156 circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit enabling or disabling each of the 4-bit sections as desired.

Data applied to input 1C is inverted at its outputs and data applied at input $2\overline{C}$ is not inverted through its outputs. The inverter following the 1C data input permits use of the 'ALS156 as a 3-line to 8-line demultiplexer without external gating. All inputs are clamped with high-performance Schottky diodes to suppress line ringing and simplify system design.

The SN74ALS156 is characterized for operation from 0° C to 70° C.

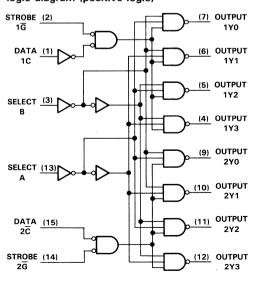


FN PACKAGE (TOP VIEW)



NC-No internal connection

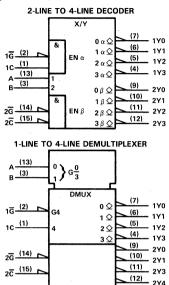
logic diagram (positive logic)





SN74ALS156 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN-COLLECTOR OUTPUTS

logic symbols† (alternatives)



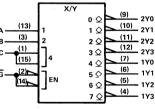
FUNCTION TABLE

2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER

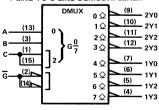
	11	NPUTS		OUTPUTS				
SEL	ECT	STROBE	DATA					
В	Α	1G	1C	1Y0	1Y1	1Y2	1Y3	
X	Х	Н	Х	Н	Н	Н	Н	
L	L	L	н	Ł	н	H ×	Н	
L	Н	L	Н	н	L	Н	Н	
Н	L	L	н	Н	Н	L	Н	
н	Н	L	н	н	. н	Н	L.	
×	Х	×	L	Н	Н	Н	Н	

	11	NPUTS		OUTPUTS				
SEL	ECT	STROBE	DATA	0011015				
В	Α	2G	2C	2Y0	2Y1	2Y2	2Y3	
Х	Х	Η ′	Х	Η	Н	Н	Н	
L	L	L	L	L	н	Н	Н	
L	Н	L	L	Н	L	н	н	
Н	L	L	L	Н	н	L	Н	
Н	Н	L	L	Н	Н	Н	L	
x	X	×	н	Н	Н	Н	Н	

3-LINE TO 8-LINE DECODER



1-LINE TO 8-LINE DEMULTIPLEXER



FUNCTION TABLE 3-LINE TO 8-LINE DECODER OR

1-LINE TO 8-LINE DEMULTIPLEXER

	11	IPUTS					OUT	PUTS			
,	SELECT	Г	STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C‡	В	Α	Ч	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
-L	L	H	L	н	L	Н	Н	Н	Н	Н	Н
L	/ H	L	L	н	Н	L	Н	Н	Н	Н	Н
L	Н	Н	L	н	Н	Н	L	Н	Н	Н	Н
Н	L	L,	L	н	Н	Н	Н	L	Н	Н	Н
Н	L	Н	L	н	Н	Н	Н	Н	L	Н	Н
Н	Н	L	L	Н	Н	Н	Н	Н	Н	L	Н
Н	Н	Н	L	н	Н	Н	Н	Н	Н	Н	L

 $^{^{\}ddagger}$ C = inputs 1C and $2\overline{C}$ connected together

Pin numbers shown on logic symbols are for D and N packages only.



 $[\]S \overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together

[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALS156 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
Vон	High-level output voltage			5.5	V
lOL	Low-level output current			8	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	MIN TYP	† MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA		-1.5	V
V	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA	0.2	5 0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA	0.3	5 0.5	7 °
Г ОН	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V		0.1	mA
11	$V_{CC} = 5.5 V,$	V _I = 7 V		0.1	mA
IH	$V_{CC} = 5.5 V,$	V _I = 2.7 V		20	μΑ
lir.	$V_{CC} = 5.5 V,$	V _I = 0.4 V		-0.1	μΑ
ICCL	V _{CC} = 5.5 V			5 9	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics[‡]

PARAMETER	FROM	то	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 0 ^{\circ}\text{C to } 70 ^{\circ}\text{C}$		UNIT															
			TYP	MIN	MAX																
^t PLH	А, В	1Y, 2Y	30	13	55	ns															
^t PHL	7 4, 5	11, 21	12	6	25] "15															
t _{PLH}	1C	1Y	38	18	50																
^t PHL	7 '		1.1		1.1	11	• 1	• •	1.1	, ,	1.4	1 7	11	1 1	I Y	1 Y	1 Y	ΙΥ	12	6	23
^t PLH	1 <u>G</u>	1Y	24	13	38																
t _{PHL}	7 '6 1	1 1	13	6	22	ns															
^t PLH	2 0 , 2 0	2Y	24	13	38																
^t PHL		∠ T	13	6	22	ns															

[‡]For load circuits and voltage waveforms see Section 1.

SN54ALS157, SN54ALS158, SN54AS157, SN54AS158 SN74ALS157, SN74ALS158, SN74AS157, SN74AS158 QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS

D2661, APRIL 1982-REVISED MAY 1986

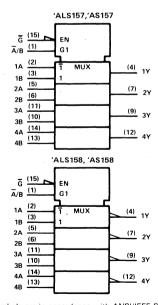
- **Buffered Inputs and Outputs**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input (\overline{G}) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'ALS157 and 'AS157 present true data whereas the 'ALS158 and 'AS158 present inverted data to minimize propagation delay time.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbols†

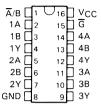


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

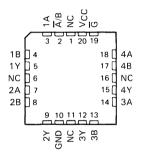
Pin numbers shown are for D. J. and N packages.

PRODUCTION DATA documents contain information current as of publication date Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . D OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)

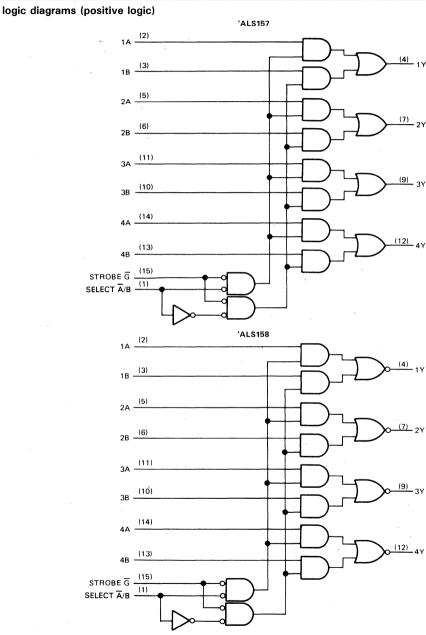


NC-No internal connection

FUNCTION TABLE

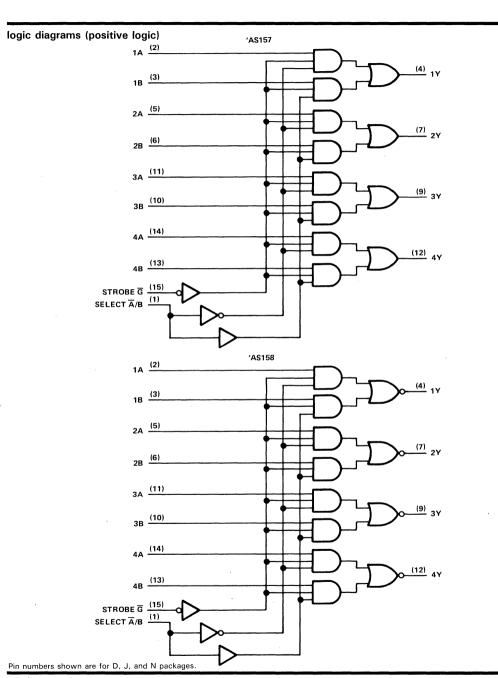
,	INPUTS	OUTPUT Y			
STROBE	SELECT	D.A	ΛTA	'ALS157	'ALS158
G	A/B	A	В	'AS157	'AS158
Н	Х	Х	Х	L	Н
L	L	L	Х	L	н
L	Ł	Н	Х	Н	L
L	н	×	L	L	Н
L	Н	×	Н	Н	L





Pin numbers shown are for D, J, and N packages.







SN54ALS157, SN54ALS158, SN74ALS157, SN74ALS158 QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

			SN54ALS157 SN74ALS157 SN54ALS158 SN74ALS158 MIN NOM MAX MIN NOM MAX					UNIT
		MIN						
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ТОН	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54A SN54A		SN74ALS SN74ALS		UNIT
			MIN TYP	† MAX	MIN TYP	MAX	1
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA		-1.2		-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2		V _{CC} -2		V
Vol	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA	0.2	5 0.4	0.25	0.4	
VOL	V _{CC} = 4.5 V,	I _{OL} = 8 mA			0.35	0.5	7 °
II.	$V_{CC} = 5.5 V,$	V ₁ = 7 V		0.1		0.1	mA
lін	V _{CC} = 5.5 V,	V _I = 2.7 V		20		20	μΑ
[‡] IL	$V_{CC} = 5.5 V,$	V _I = 0.4 V		-0.1		-0.1	mA
lo‡	V _{CC} = 5.5 V,	V _O = 2.25 V	-30	- 112	- 30	-112	mA
'ALS157	V E E V	See Note 1		6 11	6	11	
CC ALS158	$V_{CC} = 5.5 V,$	See Note 1		5 10	5	10	mA

 $^{^{\}dagger}$ All typical values ae at V_{CC} = 5 V, T_A = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}. NOTE 1: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

SN54ALS157, SN54ALS158, SN74ALS157, SN74ALS158 QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS

'ALS157 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V,$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω T_A = MIN to MAX				UNIT
			'ALS157	SN54ALS157		SN74ALS157]
	İ		TYP	MIN	MAX	MIN	MAX	1
[†] PLH	A or B	V	9	4	17	4	14	
[†] PHL	7 A OF B	Ť	6	2	15	2	12	ns
^t PLH	Ā/B	V	15	7	28	7	24	
†PHL	7 4/6	, r	9	4	16	4	13	ns
^t PLH	G	V	14	7	25	7	20	
[†] PHL	7 "	Y	10	4	18	4	13	ns

'ALS158 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V,$ $C_{L} = 50 pF,$ $R_{L} = 500 \Omega,$ $T_{A} = 25 °C$	C _L	V_{CC} = 4.5 V to 5.5 C_L = 50 pF, R_L = 500 Ω T_A = MIN to MAX			UNIT	
			'ALS158	SN54	ALS158	SN74	ALS158		
			TYP	MIN	MAX	MIN	MAX	1	
^t PLH	A or B	Υ	9	4	18	4	15		
^t PHL	7 7 01 5	Y		5	2	12	2	8	ns
^t PLH	Ā/B	Υ	13	5	22	5	18		
^t PHL	A/B		13	5	22	5	18	ns	
tPLH	G	ν'	13	5	22	5	18	ns	
tPHL	J	τ	- 13	5	22	5	18	115	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN54AS157, SN54AS158, SN74AS157, SN74AS158 QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54AS157, SN54AS158 55 °C to 125 °C
	SN74AS157, SN74AS158 0°C to 70°C
Storago tomporaturo rango	-65°C to 150°C

recommended operating conditions

		1	SN54AS157 SN54AS158				SN74AS157 SN74AS158			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
VIH	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.8			0.8	V		
ЮН	High-level output current			- 2			- 2	mA		
lOL	Low-level output current			20			20	mA		
TA	Operating free-air temperature	- 55		125	0		70	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDITIONS			SN54AS157 SN54AS158			SN74AS157 SN74AS158			
				MIN	TYP†	MAX	MIN	TYP [†]	MAX	1	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V	
Vон		V _{CC} = 4.5 V to 5.5 V	V , $I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2		V	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V	
	Ā/B	V 55.V	7.1/			0.2			0.2		
Ц	A, B, or G	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
	Ā/B	.,				40			40		
ΉΗ	A, B, or \overline{G}	$V_{CC} = 5.5 \text{ V},$	$V_I = 2.7 V$			20			20	μΑ	
	Ā/B	.,				- 1			- 1		
կլ	A, B or \overline{G}	$V_{CC} = 5.5 \text{ V},$	$V_1 = 0.4 V$			-0.5			-0.5	mA	
10 [‡]		$V_{CC} = 5.5 V$,	V _O = 2.25 V	-30		-112	-30		-112	mA	
laa	'AS157	V _{CC} = 5.5 V			17.5	28		17.5	28	mA	
ICC	'AS158	ΛCC = 2.2 Λ			15.6	22.5		15.6	22.5] 'MA	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, IOS.

SN54AS157, SN54AS158, SN74AS157, SN74AS158 QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS

'AS157 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
}			SN54	AS157	SN74	AS157	1
			MIN	MAX	MIN	MAX	
t _{PLH}	A or B	~	1	7.5	1	6	
[†] PHL	A 01 B	·	1	6.5	1	5.5	ns
^t PLH	A/B	V	2	12	2	11	ns
^t PHL	Α/Β	' ' '	2	12	2	10	1115
^t PLH	G	V	2	12.5	2	10.5	ns
^t PHL	9	'	2	8.5	2	7.5	1115

'AS158 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)			$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX					
j			SN544	S158	SN74	AS158			
			MIN	MAX	MIN	MAX	ļ		
^t PLH	A or B	· · ·	1	6	1	5			
^t PHL	1 4016	r	1	5.5	1	4.5	ns		
^t PLH	Ā/B	V	2	11	2	9.5	ns		
. ^t PHL	7/5	'	2	11.5	2	10.5	115		
^t PLH	G	Υ	2	8	2	6.5	ns		
^t PHL		'	2	11.5	2	10	115		

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS160B THRU SN54ALS163B, SN54AS160 THRU SN54AS163 SN74ALS160B THRU SN74ALS163B. SN74AS160 THRU SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

D2661, APRIL 1982-REVISED MAY 1986

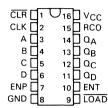
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

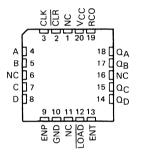
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160B, 'ALS162B, 'AS160, and 'AS162 are decade counters, and the 'ALS161B, 'ALS163B, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, they may be preset to any number between 0 and 9, or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . D OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

The clear function for the 'ALS160B, 'ALS161B, 'AS160, and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'ALS162B, 'ALS163B, 'AS162, and 'AS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both countenable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with QA high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

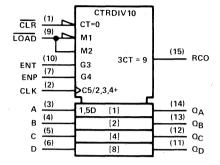
These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or IOAD) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS160B through SN54ALS163B and SN54AS160 through SN54AS163 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS160B through SN74ALS163B and SN74AS160 through SN74AS163 are characterized for operation from 0°C to 70°C.

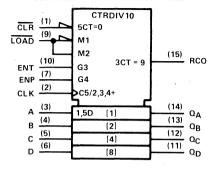


logic symbols†

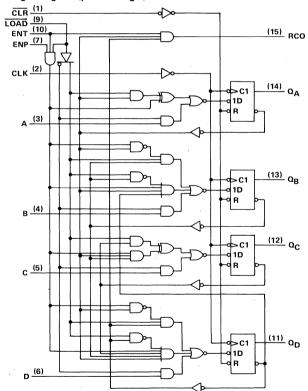
'ALS160B AND 'AS160 DECADE COUNTERS WITH DIRECT CLEAR



'ALS162B AND 'AS162 DECADE COUNTERS WITH SYNCHRONOUS CLEAR



'ALS160B and 'AS160 logic diagram (positive logic)

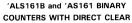


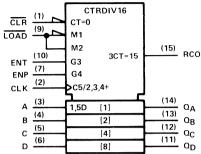
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

^{&#}x27;ALS162B and 'AS162 decade counters are similar; however the clear is synchronous as shown for the 'ALS163B and 'AS163 binary counters.

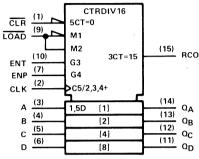


logic symbols†

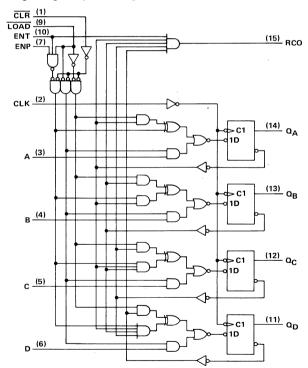




'ALS163B AND 'AS163 BINARY COUNTERS WITH SYNCHRONOUS CLEAR



'ALS163B and 'AS163 logic diagram (positive logic)



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

^{&#}x27;ALS161B and 'AS161 synchronous binary counters are similar; however the clear is asynchronous as shown for the 'ALS160B and 'AS160 decade counters.

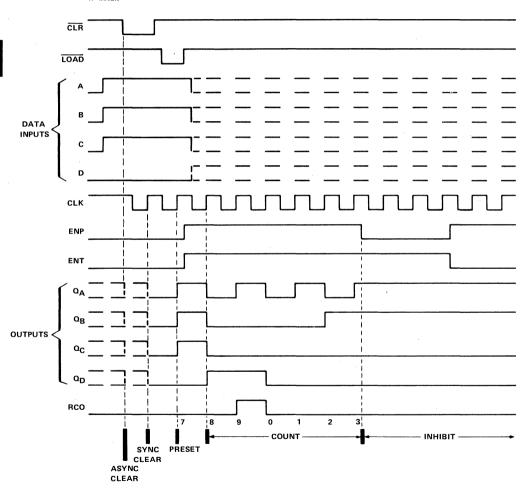


typical clear, preset, count, and inhibit sequences

'ALS160B, 'AS160, 'ALS162B, 'AS162

Illustrated below is the following sequence:

- Clear outputs to zero ('ALS160B and 'AS160 are asynchronous; 'ALS162B and 'AS162 are synchronous)
- 2. Preset to BCD seven
- 3. Count to eight, nine, zero, one, two, and three
- 4. Inhibit



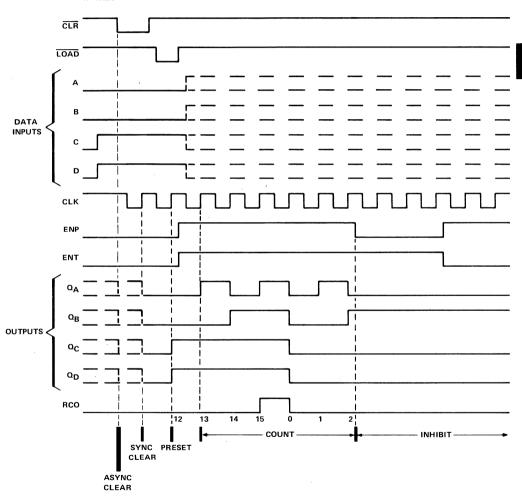


typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, 'AS163

Illustrated below is the following sequence:

- 1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous)
- 2. Preset to binary twelve
- 3. Count to thirteen, fourteen, fifteen, zero, one, and two
- 4. Inhibit



SN54ALS160B THRU SN54ALS163B SN74ALS160B THRU SN74ALS163B SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operat	ting free-air temperature range (unless otherwise noted)
Supply voltage, VCC	
Input voltage	
Operating free-air temperature range	: SN54ALS160B thru SN54ALS163B55°C to 125°C
	SN74ALS160B thru SN74ALS163B 0 °C to 70 °C
Storage temperature range	65°C to 150°C

recommended operating conditions

					54ALS1 THRU 54ALS1			174ALS THRU 174ALS		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input	voltage		2			2			V
VIL	Low-level input	voltage				0.7			0.8	V
ІОН	High-level outpu	t current				-0.4			-0.4	mA
lOL	Low-level outpu	t current				4			8	mA
f _{clock}	Clock frequency			0		22	0		40	MHz
	Pulse duration	CLK high or low		20			12.5			
tw	ruise duration	'ALS160B, 'ALS161B	CLR low	20			15			ns
		A, B, C, D		20			15			
		LOAD		20			15			
			'ALS160B, 'ALS161B	25			15			
	Setup time	ENP, ENT	'ALS162B, 'ALS163B	20			15			
t _{su}	before CLK↑	'ALS160B, 'ALS161B	CLR inactive	10			10			ns
		/ALC100D /ALC100D	CLR low	20			15			
		'ALS162B, 'ALS163B	CLR high (inactive)	10			10		-	
th	Hold time, all sy	nchronous inputs after (CLK1	0			0	W. C.		ns
TA	Operating free-a	ir temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54ALS160B THRU SN54ALS163B			SN74ALS160B THRU SN74ALS163B		
			MIN	TYP [†]	MAX	MIN	TYP	MAX	}
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -	2		V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = 4.5 V,	IOL = 8 mA					0.35	0.5	1
l _I	$V_{CC} = 5.5 V,$	V _I = 7 V		-	0.1			0.1	mA
lін	$V_{CC} = 5.5 V$,	V ₁ = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2			-0.2	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		-112	mA
lcc	V _{CC} = 5.5 V			12	21		12	21	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS160B THRU SN54ALS163B SN74ALS160B THRU SN74ALS163B SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

'ALS160B, 'ALS161B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				
			SN54A	SN54ALS160B SN54ALS161B		SN74ALS160B SN74ALS161B		
•			MIN	MAX	MIN	MAX		
f _{max}			22		40		MHz	
^t PLH	CLK	RCO	5	34	5	20	ns	
tPHL) OLK	1100	5	27	5	20	113	
tPLH	CLK	Any Q	4	19	4	15	ns	
^t PHL	CLK	Ally Q	6	25	6	20	115	
tPLH	ENT	DCO	3	18	3	13		
^t PHL	[[14]	RCO	3	17	3	13	ns	
^t PHL	CLR	Any Q	8	27	8	24	ns	
[†] PHL	CLR	RCO	11	32	11	23	ns	

'ALS162B, 'ALS163B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		$V_{CC} = 4$ $C_L = 50$ $R_L = 500$ $T_A = MII$ $LS162B$ $LS163B$ MAX	Ω, N to MAX SN74A	LS162B LS163B	UNIT
f _{max}			35		40		MHz
tPLH	CLK	RCO	5	25	5	20	
^t PHL	CLK	RCO	5	25	5	20	ns
^t PLH	CLK	Anu 0	4	18	4	15	
^t PHL	CLN	Any Q	6	25	6	20	ns
^t PLH	ENT	RCO	3	16	3	13	
t _{PHL}	l ENT.	NCO NCO	3	16	3	13	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS160 THRU SN54AS163 SN74AS160 THRU SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC			7 V
Input voltage			7 V
Operating free-air temperature range:	SN54AS160 thru SN54A	\S163	. -55°C to 125°C
	SN74AS160 thru SN74A	AS163	0°C to 70°C
Storage temperature range			65°C to 150°C

recommended operating conditions

				SI	N54AS1	60	SN	174AS1	60	
					THRU			THRU		
				SI	N54AS1	63	SN	174AS1	63	UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
٧cc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input	voltage		2			2			V
ا_\	Low-level input	voltage				0.8			0.8	V
ПОН	High-level outpu	t current				-2			-2	mA
loL	Low-level outpu	t current				20			20	mA
fclock	Clock frequency			0		65	0		75	MHz
	Pulse duration	CLK high or low	The state of the s	7.7			6.7			
t _W	ruise duration	'AS160, 'AS161 CLF	low	10			8			ns
		A, B, C, D		10			8			
		LOAD		10			8			
	Setup time	ENP, ENT		10			8			
t _{su}	before CLK↑	'AS160, 'AS161 CLF	inactive	10			8			ns
		440400 440400	CLR low	14			12			
		'AS162, 'AS163	CLR high (inactive)	10			9			
th	Hold time, all sy	nchronous inputs after	CLK↑	2			0			ns
TA	Operating free-a	ir temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS SN54AS160 THRU SN54AS163 MIN TYP [†] MAX MI			174AS1 THRU 174AS1	63	UNIT					
				MIN	TYP [↑]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.2			1.2	V
∨он		$V_{CC} = 4.5 \text{ V to } 5.5$	$5 V$, $I_{OH} = -2 mA$	vcc-	2		vcc-	2		V
VOL		$V_{CC} = 4.5 V$	$I_{OL} = 20 \text{ mA}$		0.25	0.5		0.25	0.5	V
	LOAD					0.3			0.3	
l _l	ENT	$V_{CC} = 5.5 V$	$V_1 = 7 V_1$			0.2			0.2	mA
	All other					0.1			0.1	
	LOAD					60			60	
ΊΗ	ENT	$V_{CC} = 5.5 V$	$V_1 = 2.7 V$			40			40	μΑ
	All other					20			20	
	LOAD					-1.5			-1.5	
IIL.	ENT	$V_{CC} = 5.5 V$,	$V_1 = 0.4 \ V$			- 1			- 1	mA
	All other	T				-0.5			-0.5	
10.‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
Icc		V _{CC} = 5.5 V			35	53		35	53	mA

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54AS160 THRU SN54AS163 SN74AS160 THRU SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

'AS160, 'AS161 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		$R_{L} = 500 \Omega,$ $T_{A} = MIN \text{ to MAX}$ $SN54AS160$ $SN74AS160$		οF, Ω, I to MAX SN74AS160	
			MIN	MAX	MIN	MAX	
f _{max}			65		75		MHz
^t PHL		RCO	2	14	2	12.5	
^t PLH	CLK	RCO (with LOAD high)	1	8.5	1	8	ns
^t PLH		RCO (with LOAD low)	3	17.5	3	16.5	
^t PLH	CLK	Any Q	1	7.5	1	7	
^t PHL	CLK	Ally d	2	14	2	13	ns
^t PLH	ENT	RCO	1.5	10	1.5	9	ns
^t PHL	LIVI	NCO NCO	1	9.5	1	8.5	115
^t PHL	CLR	Any Q	2	14	2	13	ns
^t PHL	CLR	RCO	2	14	2	12.5	ns

'AS162, 'AS163 switching characteristics (see Note 1)

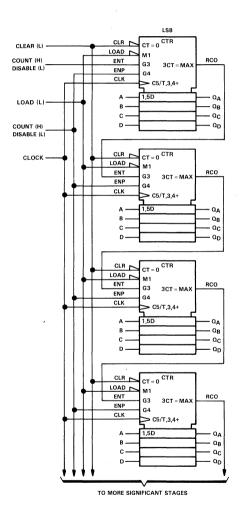
PARAMETER	FROM (INPUT)	TO (OUTPUT)		$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pf,} \\ R_L = 500 \Omega, \\ T_A = \text{MIN to MAX} \\ \hline \text{SN54AS162} & \text{SN74AS162} \\ \hline \text{SN54AS163} & \text{SN74AS163} \\ \hline \text{MIN} & \text{MAX} & \text{MIN} & \text{M} \end{array}$		NS162	UNIT
fmax			65		75	***	MHz
^t PHL		RCO	2	14	2	12.5	
tPLH	CLK	RCO (with LOAD high)	1	8.5	1	8	ns
tPLH		RCO (with LOAD low)	3	17.5	3	16.5	
tPLH	CLK	Any Q	1	7.5	1	7	
^t PHL	CLK	Ally d	2	14	2	13	ns
^t PLH	ENT	RCO	1.5	10	1.5	9	ns
t _{PHL}	CIVI		1	9.5	1	8.5	113

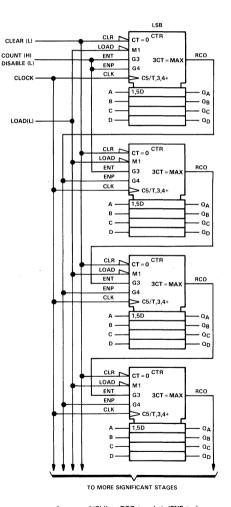
NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The 'ALS160B, 'AS160, 'ALS162B, and 'AS162 will count in BCD and the 'ALS161B, 'AS161, 'ALS163B, and 'AS163 will count in binary. When additional stages are added, the f_{MAX} decreases in Figure 1, but remains unchanged in Figure 2.





 $f_{MAX} = 1/(CLK \text{ to RCO } t_{PLH}) + (ENT \text{ to RCO } t_{PLH}) (N-2) + (ENT \text{ } t_{su})$

 $f_{MAX} = 1/CLK \text{ to RCO } t_{PLH}) + (ENP t_{su})$

FIGURE 1

FIGURE 2



- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- **Direct Clear**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flipflop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54ALS164 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS164 is characterized for operation from 0 °C to 70 °C.

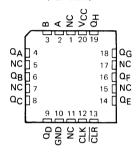
SN54ALS164 . . . J PACKAGE SN74ALS164 . . . D OR N PACKAGE

(TOP VIEW)

	_		
Α		U 14[]	VCC
В	2	13	QΗ
QΑ	□ 3	12	Q_G
QΒ	4	11	Q_{F}
σc	□ 5	10	Œ
σD	□6	9	CLR
ND	□ 7	8	CLK

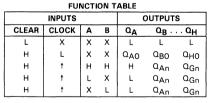
SN54ALS164 . . . FK PACKAGE (TOP VIEW)

G



NC-No Internal connection

logic symbol †



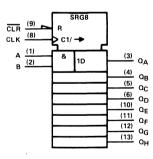
H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

† = transition from low to high level.

 Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_{A} , Q_{B} , or Q_{H} , respectively, before the indicated steady-state input conditions were established.

 Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most-recent † transition of the clock; indicates a one-bit shift.



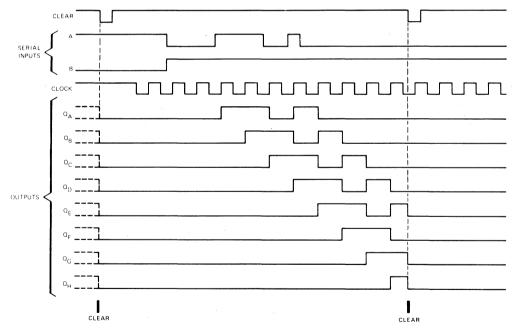
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J and N packages.

CLEAR (9) CLOCK (8) SERIAL A (11) INPUTS A (21) OUTPUT O

Pin numbers shown are for D, J, and N packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 	7 V
Input voltage			
Operating free-air temperature range:	SN54ALS164	 	$-55^{\rm o}\text{C}$ to $125^{\rm o}\text{C}$
Storage temperature range		 	-65 °C to 150 °C



SN54ALS164, SN74ALS164 8-BIT-PARALLEL-OUT SERIAL SHIFT REGISTERS

recommended operating conditions

				SN54ALS	164	S	N74ALS	164	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5 5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
loн	High-level output current				-0.4			-0.4	mA
· loL	Low-level output current				4			8	mA
fclock	Clock frequency								MHz
		CLR low							
tw	Pulse duration	CLK high							ns
		CLK low							
	Setup time	SH/LD							
t _{su}		Data							ns
	before CLK1	CLR inactive							
th	Hold time, data after CLK1	***************************************	()		0			ns
TA	Operating free-air temperature)	- 58	i	125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		S	SN54ALS164			SN74ALS164		
PANAMETER	1531 66	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 \text{ V},$	I ₁ = -18 mA			-1.5			-1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	Vcc-	2		Vcc-	2		V
VoL	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	v
VOL [$V_{CC} = 4.5 V$,	I _{OL} = 8 mA					0.35	0.5	1 °
Ц	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lіН	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
· IIL	$V_{CC} = 5.5 V,$	V ₁ = 0.4 V			- 0.1			-0.1	mA
lO‡	$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
Icc	V _{CC} = 5.5 V	See Note 1		10			10		mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	C _L = 50 R _L = 50	$V_{CC}=4.5~V$ to $5.5~V$, $C_L=50~pF$, $R_L=500~\Omega$, $T_A=MIN$ to MAX					
			SN54ALS164	SN74ALS164	İ				
			MIN TYP† MAX	MIN TYP† MAX					
f _{max}			60	60	MHz				
tPHL	CLR	Any Q	12	12	ns				
[‡] PLH	CLK	Any Q	10	10	200				
tPHL] CLK	Ally Q	11	11	ns				

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

Additional information on these products can be obtained from the factory as it becomes available.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

NOTE 1: With 4.5 Volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS165, SN74ALS165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

D2661, JUNE 1982-REVISED MAY 1986

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'ALS165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output $\overline{\mathrm{O}}_{H}$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/LD input. The 'ALS165 also features a clock inhibit function and a complemented serial output $\overline{\mathrm{O}}_{H}$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/ $\overline{\text{LD}}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/ $\overline{\text{LD}}$ is held high. The parallel inputs to the register are enabled while SH/ $\overline{\text{LD}}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

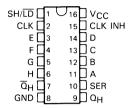
The SN54ALS165 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS165 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

FUNCTION TABLE

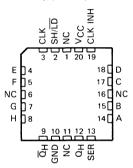
	INPUTS						
SH/LD	CLK	CLK	FUNCTION				
L	X	X	PARALLEL LOAD				
Н	Н	X	NO CHANGE				
Н	X	Н	NO CHANGE				
Н	L	†	SHIFT				
Н	1	L	SHIFT				

SHIFT—content of each internal register shifts toward serial output $Q_{\mbox{\scriptsize H}}$. Data at serial input is shifted into first register.

SN54ALS165 . . . J PACKAGE SN74ALS165 . . . D OR N PACKAGE (TOP VIEW)

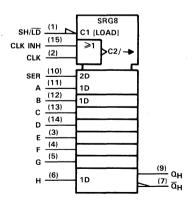


SN54ALS165 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

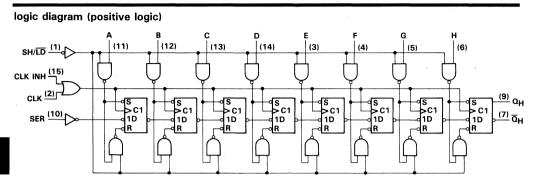
logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

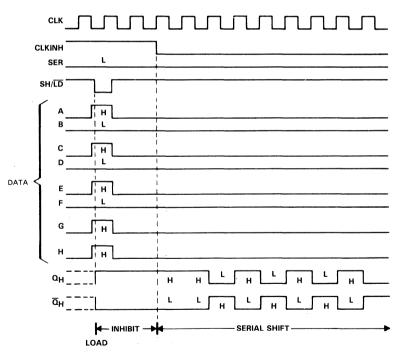
Pin numbers are for D, J, and N packages.

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Pin numbers are for D, J, and N packages.

typical shift, load, and inhibit sequences



SN54ALS165, SN74ALS165 PARALLEL LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operati	ing nee-an temperature range tuniess other	si wise noteu,
Supply voltage, VCC		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54ALS165	-55°C to 125°C
	SN74ALS166	0°C to 70°C

recommended operating conditions

Storage temperature range

				SN	54ALS1	65	SN	74ALS1	65	UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage			4.5	5	55	4.5	5	5.5	V
V _{IH}	High-level input voltage			2			2			V
VIL	Low-level input voltage				0.7			0.8	V	
ГОН	High-level output current					-0.4			-0.4	mA
lOL	Low-level output current					4			8	mA
fclock	Clock frequency									MHz
		CLR low								
t _w	Pulse duration	CLK high								ns
		CLK low	,							
		SH/LD								
t _{su}	Setup time before CLK1	Data								ns
		CLR inactive								
th	Hold time, data after CLK↑									ns
TA	Operating free-air temperat	ıre		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	154ALS	165	SN	UNIT		
PANAIVIETEN	1251 CO	TEST CONDITIONS				MIN	TYP [†]	MAX	UNII
VIK	VCC = 4.5 V,	I _I = -18 mA			- 1.5			-1.5	V
Voн	VCC = 4.5 V to 5.5	V, I _{OH} = -0.4 mA	V _{CC} -	2		V _{CC} -2	2		V
V	VCC = 4.5 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	1 '
Ч	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ЧН	VCC = 5.5 V,	V ₁ = 2.7 V			20			20	μΑ
IL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
10‡	VCC = 5.5 V,	V _O = 2.25 V	- 30		- 112	- 30		-112	mA
¹ CC	V _{CC} = 5.5 V	See Note 1		16			16		mA

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{\circ}C.$



[†] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, IOS. NOTE 1: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to the SH/LD input, ICC is measured first with the parallel inputs at $4.5\ V$, then with the parallel inputs grounded.

SN54ALS165, SN74ALS165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R _L T _F	UNIT					
			SN54ALS165 SN74ALS165						
			MIN TYP†	MAX	MIN	TYP [†]	MAX]	
f _{max}			25		25			MHz	
tPLH	cu/ <u>ID</u>	SH/LD Any				21	_	ns	
^t PHL	311/120	Ally	26		26]	
tPLH	CLK	Any	14	14			ns		
tPHL	CLK	Ally	16	16			16		
tPLH	Н	0	13		13			ns	
tPHL	п	QΗ	24	24		24		1 115	
tPLH	Н	ΩH	19		19			ns	
[†] PHL	, ,	ФН	17			17		1115	

 † All typical values are at VCC = 5 V, TA = 25 °C. NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.



- **Direct Overriding Clear**
- Parallel to Serial Conversion
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

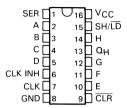
description

The 'ALS166 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

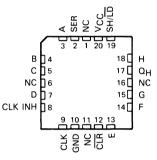
These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flipflops to zero.

The SN54ALS166 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS166 is characterized for operation from 0°C to 70°C.

SN54ALS166 . . . J PACKAGE SN74ALS166 . . . D OR N PACKAGE (TOP VIEW)

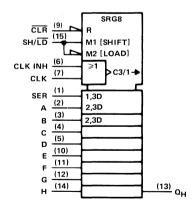


SN54ALS166 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol†



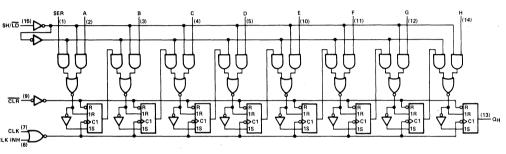
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for D, J, and N packages.

FUNCTION TABLE

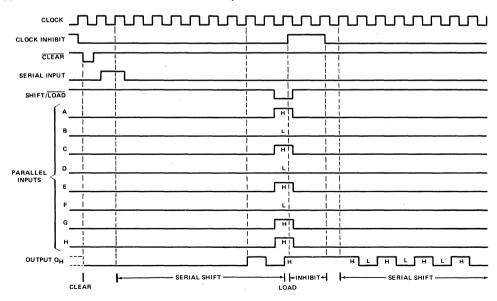
		IN	PUTS			INTE	RNAL	ОИТРИТ	
CLEAR	SHIFT/	CLOCK	CLOCK	SERIAL	PARALLEL	OUT	PUTS		
CLEAR	LOAD	INHIBIT	CLUCK	SERIAL	A H	QA	QΒ	αн	
L	X	X	×	Х	×	L	L	L	
н	×	L	L	×	×	Q _{A0}	σ_{B0}	Q _{H0}	
н	L	L	1	×	ah	а	b .	h	
н.	н	L	†	н	×	н	q_{An}	a_{Gn}	
н	. н	L	1	L	×	L	\mathbf{Q}_{An}	Q_{Gn}	
н	×	н	1	х	×	Q _{A0}	Q_{B0}	Q _{H0}	

logic diagram (positive logic)



Pin numbers are for D, J, and N packages.

typical clear, shift, load, inhibit, and shift sequences



SN54ALS166, SN74ALS166 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operat	ing free-air	temperature	range (unless	otherwise noted)
Supply voltage, VCC				7 V
Input voltage				7 V
Operating free-air temperature range:	SN54ALS1	66		55°C to 125°C
	SN74ALS1	66		0°C to 70°C
Storage temperature range				65°C to 150°C

recommended operating conditions

			s	N54ALS	166	SN	74ALS1	66	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vсс	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	9	2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ГОН	High-level output curre	nt			-0.4			-0.4	mA
loL	Low-level output currer	nt			4			8	mA
fclock	Clock frequency								MHz
		CLR low							
tw	Pulse duration	CLK high							ns
		CLK low							
	Setup time	SH/LD							
t _{su}	before CLK1	Data							ns
	before CLK	CLR inactive							1
th	Hold time, data after C	LK†							ns
TA	Operating free-air temp	erature	- 55		125	0		70	°C

SN54ALS166, SN74ALS166 PARALLEL LOAD 8-BIT SHIFT REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AL	S166	SN74ALS166			UNIT
FANAIVIETEN	TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ m}$	A		- 1.5			- 1.5	V
∨он	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4$	4 mA V _{CC}	- 2		Vcc-	2		V
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 4 \text{ mA}$	١	0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 8 \text{ m/s}$	\				0.35	0.5	·
l _l	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$			0.1			0.1	mA
ЧH	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$			20			20	μΑ
IIL	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25$	V -30		-112	- 30		-112	mA
¹ CC	V _{CC} = 5.5 V See Note 1		16			16		mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)						UNIT	
			SN54ALS166 SN74/					66	l
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
f _{max}				60			60		MHz
tPHL	CLR	QH		10			10		ns
^t PLH	CLK	QΗ		12			12		ns
tPHL		<u>ч</u> н		13			13		115

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

NCTE 2: Load circuit and voltage waveforms are shown in Section 1.

Additional information on these products can be obtained from the factory as it becomes available.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: With 4.5 volts applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0 to 4.5 volts.

SN54ALS168B, SN54ALS169B, SN54AS168, SN54AS169 SN74ALS168B, SN74ALS169B, SN74AS168, SN74AS169 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

MARCH 1984 - REVISED MAY 1986

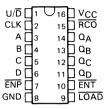
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- **Fully Independent Clock Circuit**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

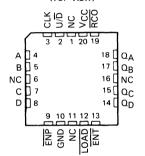
These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'ALS168B and 'AS168 are decade counters and the 'ALS169B and 'AS169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the countenable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . D OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)



NC -- No internal connection

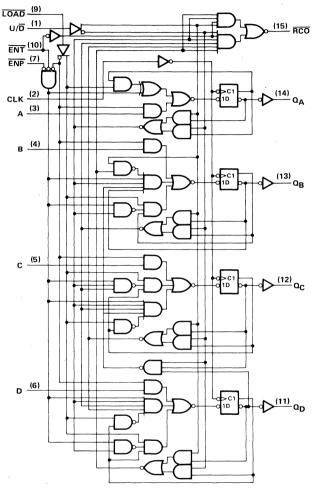
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{\text{ENP}}$ and $\overline{\text{ENT}}$) must be low to count. The direction of the count is determined by the level of the U/ $\overline{\text{D}}$ input. When U/\overline{D} is high, the counter counts up; when low, it counts down. Input \overline{ENT} is fed forward to enable the carry output. The riple carry output (RCO) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at ENP or ENT are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, LOAD, U/D) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

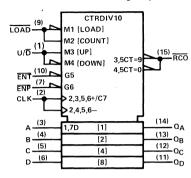
The SN54ALS168B, SN54AS168, SN54ALS169B, and SN54AS169 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS168B, SN74AS168, SN74ALS169B, and SN74AS169 are characterized for operation from 0°C to 70°C.



'ALS168B, 'AS168 logic diagram (positive logic)

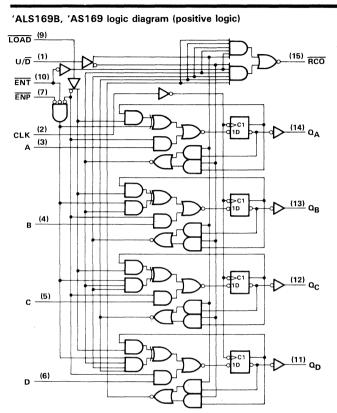


'ALS168B, 'AS168 logic symbol[†]

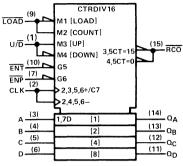


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

SN54ALS169B, SN54AS169, SN74ALS169B, SN74AS169 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS



'ALS169B, 'AS169 logic symbol[†]



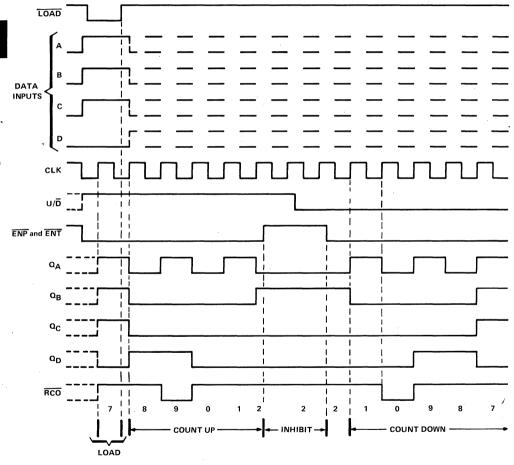
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

SN54ALS168B, SN54AS168, SN74ALS168B, SN74AS168 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS

'ALS168B, 'AS168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

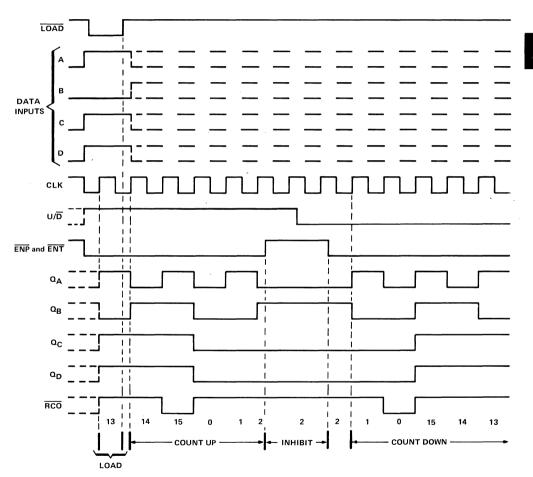
- 1. Load (preset) to BCD seven
- 2. Count up to eight, nine (maximum), zero, one, and two
- 3 Inhihi
- 4. Count down to one, zero (minimum), nine, eight, and seven



'ALS169B, 'AS169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

- 1. Load (preset) to binary thirteen
- 2. Count up to fourteen, fifteen (maximum), zero, one, and two
- 3. Inhibi
- 4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen





SN54ALS168B, SN54ALS169B, SN74ALS168B, SN74ALS169B SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54ALS168B, SN54ALS169B
	SN74ALS168B, SN74ALS169B 0 °C to 70 °C
Storage temperature range	

recommended operating conditions

								174ALS168B 174ALS169B		
			MIN	NOM	MAX	MIN	NOM	MAX	1	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
ViH	High-level input voltage		2			2			V	
VIL	Low-level input voltage				0.7			0.8	V	
ЮН	High-level output current				-0.4			-0.4	mA	
lOL	Low-level output current				4			8	mA	
fclock	Clock frequency		0		22	0		40	MHz	
tw	Pulse duration	CLK high or low	14			12.5			ns	
		A, B, C, or D	20			15				
	C-+ +! h - f CLKA	ENP or ENT	25			15				
t _{su}	Setup time before CLK†	LOAD	20			15			ns	
		U/D	28			15			1	
th	Hold time, data after CLK†		0			0			ns	
TA	Operating free-air temperature		- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B		
			MIN	TYP [†]	MAX	MIN	TYP	MAX]
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		v _{cc} -	2		V
V _{OL}	V _{CC} = 4.5 V,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
	$V_{CC} = 4.5 \text{ V},$	IOL = 8 mA					0.35	0.5	ľ
11	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
liH	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μA
1 _{IL}	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2			-0.2	mA
10‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		- 112	- 30		112	mA
¹ CC	V _{CC} = 5.5 V			15	25		15	25	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS168B, SN54ALS169B, SN74ALS168B, SN74ALS169B SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

'ALS168B, 'ALS169B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	SN54A	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $RL = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54ALS168B$ $SN74ALS168B$			
			SN54A	SN54ALS169B		SN74ALS169B	
			MIN	MAX	MIN	MAX	1
fmax			22		40		MHz
tPLH	CLK	RCO	3	25	3	20	ns
^t PHL			6	25	6	20	
^t PLH	CLK	Any Q	2	20	2	15	⊸l ns
^t PHL			5	23	5	20	
^t PLH	ENT	RCO	2	16	2	13	⊸l ns
^t PHL			3	24	3	16	
^t PLH	U/D	RCO	5	22	5	19	ns
[†] PHL			5	22	5	19	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS168, SN54AS169, SN74AS168, SN74AS169 SYNCHRONOUS 4 BIT UP/DOWN DECADE AND BINARY COUNTERS

recommended operating conditions

				N54AS1 N54AS1		1	N74AS1 N74AS1		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage		4.5	- 5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
Іон	High-level output current				- 2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		65	0		75	MHz
t _W	Pulse duration	CLK high or low	7.7			6.7			ns
		A, B, C, or D	10			8			
	Catalan time a bafalla CLKA	ENP or ENT	10			8			
t _{su}	Setup time before CLK↑	LOAD	10			8			ns
		U/D	10			8			1
th	Hold time, data after CLK↑		2			0			ns
ŤA	Operating free-air temperat	ure	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			SN54AS168 SN54AS169			SN74AS168 SN74AS169			
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V	
VOF	4	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2		V	
VOL	•	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.25	0.5		0.25	0.5	V	
lı	LOAD, ENT, U/D	V _{CC} = 5.5 V,	V _I = 7 V			0.2			0.2	mA	
'1	All others	VCC = 5.5 V,	VI = 7 V			0.1			0.1	IIIA	
1	LOAD, ENT, U/D	V F F V	V _I = 2.7 V			40			40	_	
ΊΗ	All others	$V_{CC} = 5.5 V$,	V = 2.7 V			20			20	μΑ	
1	LOAD, ENT, U/D	V 55.V	V 0.4 V			- 1			- 1	^	
i JIË	All others,	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.5			-0.5	· mA	
lo‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		- 112	-30		-112	mA	
lcc		$V_{CC} = 5.5 \text{ V}$			41	63		41	63	mA	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS168, SN54AS169, SN74AS168, SN74AS169 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

'AS168, 'AS169 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 RL = 500 T _A = MI	Ω,	∀ ,	UNIT
•	,	(3331,		SN54AS168 SN54AS169		4AS168 4AS169	
			MIN	MAX	MIN	MAX	1
f _{max}			65		75		MHz
^t PLH	CLK	RCO	3	17.5	3	16.5	
^t PHL] CLK	(LOAD high or low)	2	14	2	13	ns
^t PLH	CLK	Any Q	1	7.5	1	7	
^t PHL	CLK	Ally G	2	14	2	13	ns
^t PLH	ENT	RCO	1.5	10	1.5	9	
[†] PHL		1100	1.5	10	1.5	9	ns
[†] PLH	Ú/ D	RCO	2	14	2	12	nc nc
t _{PHL}	7 0/6	NCO NCO	2	14.5	2	13	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS174, SN54ALS175, SN54AS174, SN54AS175A SN74ALS174, SN74ALS175, SN74AS174, SN74AS175A HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

D2661, APRIL 1982 - REVISED MAY 1986

- 'ALS174 and 'AS174 Contain Six Flip-Flops with Single-Rail Outputs
- 'ALS175 and 'AS175A Contain Four Flip-Flops with Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include: Buffer/Storage Registers Shift Registers
 Pattern Generators
- Fully Buffered Outputs for Maximum Isolation from External Disturbances ('AS only)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and the 'ALS175 and 'AS175A feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

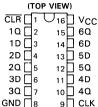
The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175A are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175A are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (EACH FLIP-FLOP)

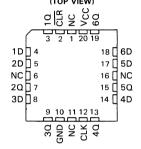
	NPUTS	OUT	PUTS	
CLR	CLK	Q	Ō١	
L	Х	Х	L	Н
Н	†	Н	н	L
Н	1	L	L	Н
Н	L	X	a_0	\bar{a}_0

[†]'ALS175 and 'AS175A only

SN54ALS174, SN54AS174 . . . J PACKAGE SN74ALS174, SN74AS174 . . . D OR N PACKAGE



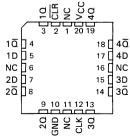
SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175A . . . J PACKAGE SN74ALS175, SN74AS175A . . . D OR N PACKAGE (TOP VIEW)

CLR [1 2	U ₁₆ V _C	
10 [3	14 🗍 40	ī
1D [4	13 🗍 4 D	
2D [5	12 3D	
20 [6	11 🗍 30	
20 [7	10 🗌 30	!
GND [8	9 CL	K

SN54ALS175, SN54AS175A . . . FK PACKAGE (TOP VIEW)

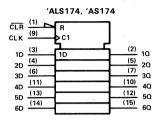


NC - No internal connection.



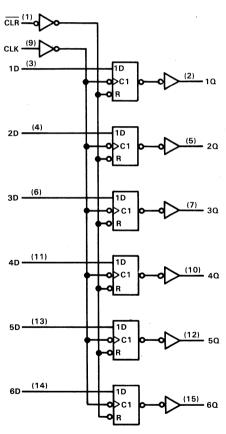
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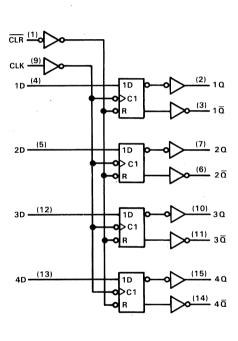
logic symbols[†]



'ALS175, 'AS175A CLR (1) > C1 (2) 1D (4) 10 (3) 10 1D (7) 2D (5) 20 (6) 2Q (10) 30 (11) ЗQ (15) 4D (13) 4Q (14)

logic diagrams (positive logic)





 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.



SN54ALS174, SN54ALS175, SN74ALS174, SN74ALS175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, V_{CC} 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS174, SN54ALS175 -55°C to 125°C SN74ALS174, SN74ALS175 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

				N54ALS			74ALS1 74ALS1		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX]
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V.
ЮН	High-level output current				-0.4			-0.4	mA
loL	Low-level output current				4			8	mA
fclock	Clock frequency		0		40	0		50	MHz
		CLR low	15		-	10			
t _w	Pulse duration	CLK high	12.5	,		10			ns
		CLK low	12.5			10]
	Setup time	Data	15			10			
t _{su}	before CLK↑	CLR inactive	8			6			ns
th	Hold time, data after CLK↑	•	0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		-	SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175		
				MIN	TYP [†]	MAX	MIN	TYP†	MAX	1
VIK		$V_{CC} = 4.5 V$,	$I_{\parallel} = -18 \text{ mA}$			-1.5			- 1.5	V
Voн		$V_{CC} = 4.5 \text{ V to}$	5.5 V I _{OH} = -0.4 mA	V _{CC} -	2		Vcc-	2		V
Vol		$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 \text{ V}$	IOL = 8 mA					0.35	0.5	1
lj		$V_{CC} = 5.5 V$,	V ₁ = 7 V	/		0.1			0.1	mA
۱н		$V_{CC} = 5.5 V$,	$V_{\parallel} = 2.7 \text{ V}$			20			20	μΑ
IL		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	- 30		-112	mA
	'ALS174	V 5 5 V	See Note 1		11	19		11	19	I
lcc	'ALS175	$V_{CC} = 5.5 V,$	See Note 1		8	14		9	14	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.



[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with D inputs and CLR grounded, and CLK at 4.5 V.

SN54ALS174, SN54ALS175, SN74ALS174, SN74ALS175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.$ $C_{L} = 50$ $R_{L} = 500$ $T_{A} = MIN$ ALS174	pF, Ω I to MAX SN74	ALS174 ALS175	UNIT
			MIN	MAX	MIN	MAX	
f _{max}			40		50		MHz
^t PLH	CLR	Any Q ('ALS175)	5	20	5	18	
t _{PHL}	CLIT	Any Q	8	30	8	23	ns
^t PLH	CLK	. Any Q	3	20	3	15	
tPHL	CLK	(or Q, 'ALS175)	5	24	5	17	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN54AS174, SN54AS175A, SN74AS174, SN74AS175A HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54AS174, SN54AS175A 55 °C to 125 °C
	SN74AS174, SN74AS175A 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

				i	SN54AS SN54AS		_	N74AS1 N74AS1		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
Іон	High-level output current					- 2			- 2	mA
lOL	Low-level output current					20			20	mA
fclock	Clock frequency			0		100	0		100	MHz
		CLR low		5.5			5			
	D. I d	CLK high		4			4			
t _w	Pulse duration	CLK I	'AS174	6		***************************************	6			ns
		CLK low	'AS175A	5			5			1
	0	Б.	'AS174	4			4			
t _{su}	Setup time	Data	'AS175A	3			3			ns
	before CLK↑	CLR inactive	9 .	6			6			1
th	Hold time, data after CLK↑			1			1			ns
TA	Operating free-air temperature			- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	PARAMETER TEST CONDITIONS		1	SN54AS		SI SN	UNIT		
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK	$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	V
VOH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	v _{cc} -	2		v _{cc} -	- 2		V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
Iį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
¹iн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.5			-0.5	mA
10 [‡]	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.25 \text{ V}$	- 30		-112	30		- 112	mA
'AS174	V E E V	See Note 1		30	45		30	45	mA
ICC AS175	$V_{CC} = 5.5 V,$	See Note 1		22.5	34		22.5	34	I '''A

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with D inputs and CLR grounded, and CLK at 4.5 V.

SN54AS174, SN54AS175A, SN74AS174, SN74AS175A HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

'AS174 switching characteristics (see Note 2)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5$ V to 5.5 V $C_L=50$ pF, $R_L=500$ Ω $T_A=MIN$ to MAX				
ı		(INFOT)	(001701)	SN5	4AS174	SN	174AS174	
L				MIN	MAX	MIN	MAX	
	f _{max}			100		100		MHz
	^t PHL	CLR	Any Q	5	15	5	14	ns
	tPLH	CLK	Any Q	3.5	9.5	3.5	8	
l	^t PHL	CLK	Ally Q	4.5	11.5	4.5	10	ns

'AS175A switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)				UNIT		
			SN54	AS175A	SN74/]		
			MIN	MAX	MIN	MAX	1	
f _{max}			100		100		MHz	
^t PLH	CLR	Any Q or $\overline{\mathbb{Q}}$	4	10	4	9		
^t PHL	CLN	Ally G of G	4.5	15	4.5	13	ns	
^t PLH	CLK	Any Q or Q	4	8.5	4	7.5		
^t PHL	CLK	Ally Q of Q	4	11	4	10	ns	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

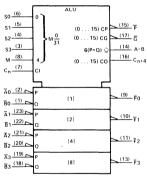
D2661, DECEMBER 1982-REVISED MAY 1986

- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil Packages. The 'AS881A is Offered in 300-mil Packages. Both Devices are Available in Both Plastic and Ceramic Chip Carriers.
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:

Addition
Subtraction
Shift Operand A One Position
Magnitude Comparison
Plus Twelve Other Arithmetic Operations

- Logic Function Modes
 Exclusive-OR
 Comparator
 AND, NAND, OR, NOR
 'AS881A Provides Status Register Checks
 Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

logic symbol†



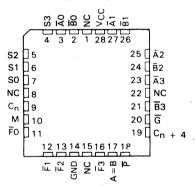
 $^\dagger This$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, JW, NT, and NW packages.

SN54AS181A . . . JT OR JW PACKAGE SN54AS881A . . . JT PACKAGE SN74AS181A . . . DW, NT OR NW PACKAGE SN74AS881A . . . DW OR NT PACKAGE (TOP VIEW)

Во□	1	\bigcup_{24}	□vcc
Ā0 [2	23	∏Ā1
S3 🗌	3	22	∏Ē1
S2 [4	21	∏Ā2
S1 [5	20	∏Ē2
so 🗌	6	19	
C _n [7	18	B3
М [8	17	□Ē
FO [9	16	$\Box C_{n+4}$
F1 [10	15	Ρ̈́
F2 [11	14	$\Box A = B$
GND [12	13	

SN54AS181A, SN54AS881A . . . FK PACKAGE SN74AS181A, SN74AS881A . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

TYPICAL ADDITION TIMES (CL = 15 pF, RL = 280 Ω , TA = 25°C)

NUMBER	A	DDITION TIMES		PACK	AGE COUNT	CARRY METHOD		
OF	USING 'AS881A	881A USING 'AS181A USING 'S1		ARITHMETIC	LOOK-AHEAD	BETWEEN		
BITS	AND'AS882 AND 'AS882 AND '		AND 'S182	LOGIC UNITS	CARRY GENERATORS	S ALUs		
1 to 4	5 ns	5 ns	11 ns	. 1		NONE		
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE		
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD		
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD		

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (SO, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input ($C_{\rm n}$) and a ripple-carry output ($C_{\rm n}+4$) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	Ã0	ВO	Ā1	B1	Ã2	Ē2	Ā3	B3	ĒΟ	F1	F2	F3	Cn	C _{n+4}	P	Ğ
Active-high data (Table 2)	A0	во	Α1	B1	A2	B2	А3	В3	F0	F1	F2	F3	Ĉ'n	Cn+4	Х	Υ

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'AS181A and 'AS881A can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with $C_{n}=H$ when performing this comparison. The A=B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

٢	INDUT	OUTPUT Cn+4	ACTIVE-LOW DATA	ACTIVE-HIGH DATA
L	INFO I Cn	OUTFUT Cn+4	(FIGURE 1)	(FIGURE 2)
Γ	Н	Н	A ≽ B	A ≤ B
ĺ	н	L	A < B	A > B
	L	• н	A > B	A < B
1	L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.



description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the \overline{P} , \overline{G} , and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode the 'AS881A provides the user with a status check on the input words A and B, and the outut word F. While in the logic mode the \overline{P} , \overline{G} , and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{P} = FO + F1 + F2 + F3$$

 $\overline{G} = H$
 $C_{n+4} = PC_n$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

S0 = S3 = H, S1 = S2 = L, and M = H

		DATA	INPUTS		0	UTF	PUTS
Cn		DATA	INPUIS		Ğ	P	C _{n+4}
Н	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	Ā3 = B 3	Н	L	Н
L	$\overline{A}0 = \overline{B}0$	$\overline{A}1 = \overline{B}1$	$\overline{A}2 = \overline{B}2$	$\overline{A}3 = \overline{B}3$	н	L	L
×	Ã0≠B0	Х	Х	X	Н	Н	L
×	×	Ā1≠B1	Х	X	Н	Н	L
×	×	Х	Ā2≠B2	X	н	Н	L
X	×	×	X	Ā3≠B3	н	н	L

S0 = S1 = S3 = L, S2 = H, and M = H

•		DATA	INDUITO		(OUT	PUTS				
Cn		DATA INPUTS									
Н	\overline{A} 0 or \overline{B} 0 = L	$\overline{A}1 \text{ or } \overline{B}1 = L$	$\overline{A}2$ or $\overline{B}2 = L$	$\overline{A}3$ or $\overline{B}3 = L$	Н	L	Н				
L	$\overline{A}0 \text{ or } \overline{B}0 = L$	$\overline{A}1$ or $\overline{B}1 = L$	$\overline{A}2$ or $\overline{B}2 = L$	$\overline{A}3$ or $\overline{B}3 = L$	н	L	L				
х	$\overline{A}0 = \overline{B}0 = H$	×	x	×	н	Н	L				
Х	x	$\overline{A}1 = \overline{B}1 = H$	x	x	н	Н	L				
х	, x	×	$\overline{A}2 = \overline{B}2 = H$	×	н.	Н	L				
Х	×	×	×	$\overline{A}3 = \overline{B}3 = H$	н	Н	L				

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits \overline{F} i. By monitoring the \overline{P} and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an A = B status while the exclusive-OR($\widehat{+}$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs (Āi, Bi) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words, which is available on the totem-pole P output, is particularly useful when cascading 'AS881s. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode (\bar{P} and \bar{G}). Thus the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs (Ai, Bi) being high, it is necessary to set the control lines (S3,S2,S1,S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\vec{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	so	М	$\overline{P} = F0 + F1 + F2 + F3$
L	Н	L	L	Н	Ā0B0 + Ā1B1 + Ā2B2 + Ā3B3
Н	L	L	Н	Н	(AO BO) + (A1 B1) + (A2 B2) + (A3 B3)

signal designations

In both Figures 1 and 2, the polarity indicators (\(\sigma\)) indicate that the associated input or output is activelow with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the activehigh data given in Table 2. The 'AS181A and 'AS881A together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.



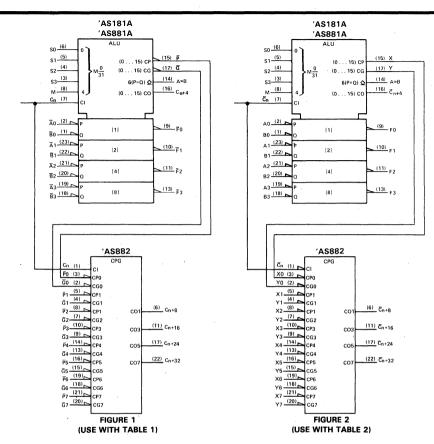


TABLE 1

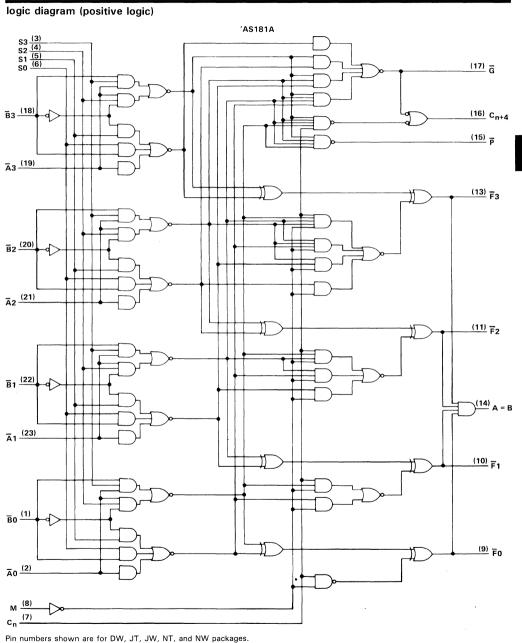
	ELEC				ACTIVE-LOW [DATA
51	ELE	3110	יוי	M = H	M = L; ARITHME	TIC OPERATIONS
62	S2	C1	en.	LOGIC	Cn = L	C _n = H
53	32	31	30	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F = Ā	F = A MINUS 1	F = A
L	L	L	н	F ≈ AB	F = AB MINUS 1	F = AB
L	L	Н	L	F = A + B	F = AB MINUS 1	F = AB
L	L	Н	н	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	Н	L	Ł	$F = \overline{A + B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
L	н	L	н	F = B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
L	н	н	L	F = A	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	Н	Н	F = A + B .	F = A + B	F = (A + B) PLUS 1
Н	L	L	L	F = ĀB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
Н	L	L	н	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
н	L	н	L	F≃B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
н	L	н	н	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	н	L	L	F = 0	F = A PLUS A †	F = A PLUS A PLUS 1
н	н	L	н	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
н	н	Н	L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	н	н	н	F = A.	F = A	F = A PLUS 1

[†]Each bit is shifted to the next more significant position.

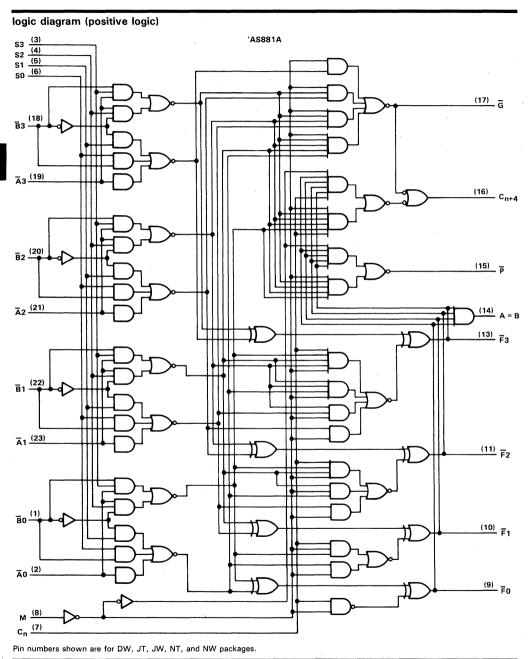
TABLE 2

٠.					ACTIVE-HIGH [DATA
St	LEC	,110	PIN .	M≃H	M = L; ARITHME	TIC OPERATIONS
				LOGIC	C̄n = H	Č _n = L
53	S2	51	SO	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F=Ā	F = A	F = A PLUS 1
L	L	L	н	F = A + B	F = A + B	F = (A + B) PLUS 1
L	L	н	L	F = ĀB	F = A + B	F = (A + B) PLUS 1
L	L	н	н	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	Н	L	L	F = AB	F = A PLUS AB	F = A PLUS AB PLUS 1
L	н	L	н	F=B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS
L	н	н	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	н	н	н	F = AB	F = AB MINUS 1	F = AB
н	L	L	L	F = A + B	F = A PLUS AB	F = A PLUS AB PLUS 1
н	L	L	н	F = A + B	F = A PLUS B	F = A PLUS B PLUS 1
н	L	н	L	F=B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS
н	L	н	н	F = AB	F = AB MINUS 1	F = AB
н	н	L	L	F = 1	F = A PLUS A †	F = A PLUS A PLUS 1
н	н	L	н	F = A + B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
н	н	н	L	F = A + B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
н	н	н	н	F = A	F = A MINUS 1	F = A











absolute	maximum ratings over operating free-air temperature range (unless otherwise noted)
Supp	ply voltage, VCC
Inpu	t voltage
Off-	state output voltage (A = B output only)
Ope	rating free-air temperature range: SN54AS181A, SN54AS881A55°C to 125°C
	SN74AS181A, SN74AS881A 0 °C to 70 °C
Stor	age temperature range65°C to 150°C

recommended operating conditions

		•		N54AS	•	5	SN74AS'		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0.8			0.8	V
Voн	High-level output voltage	A = B output only			5.5			5.5	V
ЮН	High-level output current	All outputs except A = B and G			- 2			– 2	mA
		Ğ			-3			-3	mA
loL	Low-level output current	All outputs except G			20			20	mA
		G			48			48	mA
TA	Operating free-air temperatu	Operating free-air temperature				0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

i .	PARAMETER	TEST CONDI	TIONE		SN54AS		S	UNIT		
L'	ANAIVIETEN	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	V
Voн	Any output except A = B	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	v _{cc} -	2		v _{CC} -	2		٧
	Ġ	$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		٧
ІОН	A = B	$V_{CC} = 4.5 V$,	$V_{OH} = 5.5 V$			0.1			0.1	mA
VOL	Any output except G	V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	٧
	G	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.4	0.5		0.4	0.5	V
	M input					0.1			0.1	
1.	Any A or B input	V _{CC} = 5.5 V,	14. 7.14			0.3			0.3	
14	Any S input	vCC = 5.5 v,	V = 7 V			0.4			0.4	mA
	Carry input					0.6			0.6	1
	M input					20			20	
1	Any A or B input	V 55V	1/2 2 7 1/			60			60	1 .
ЧΗ	Any S input	$V_{CC} = 5.5 V$,	V = 2.7 V			80			80	μΑ
	Carry input					120			120	1
	M input					- 2			- 2	
1	Any A or B input	V	V 04.V			- 6			6	1.
ηL	Any S input	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-8			- 8	mA
	Carry input					-12			- 12	1
	All outputs except			- 30	- 45	- 112	- 30	- 45	- 112	
lo‡	$A = B$ and \overline{G}	$V_{CC} = 5.5 V$	$V_0 = 2.25 \text{ V}$		73		"	73	2	mA
	G				- 165			-165		1
laa		V _{CC} = 5.5 V	'AS181A		135	200		135	200	
ICC		νCC = 5.5 Λ	'AS881A		135	. 210		135	210	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

^{*}The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, IOS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 5 \text{ V},$ $C_L = 15 \text{ pF},$ $R_L = 500 \Omega$ $(280 \Omega \text{ for } I)$ $T_A = 25 ^{\circ}\text{C}$ $AS = 181 \text{ AS } 181 \text{ AS } 881 \text{ MIN TYP}^{\dagger}$	A A	C R T SN5-	L = 5(L = 5(<u>A = M</u> 4AS1 4AS8		5 pF f 80 Ω f IAX SN7 SN7	or A = for A = 4AS1 4AS8	B),	UNIT
^t pd	Cn	C _{n+4}		5		2	7	11	2	7	9	ns
^t pd	Any Ā or B	C _{n+4}	M = 0 V, S1 = S2 = 0 V, $S0 = \text{S3} = 4.5 \text{ V} (\overline{\text{SUM}} \text{ mode})$	6		2	8	14	2	8	12	ns
^t pd	Any Ā or B	C _{n + 4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	7		2	8	20	2	8	16	ns
t _{pd}	Cn	Any F	M = 0 V (SUM or DIFF mode)	5		3	. 6	11	3	6	9	ns
^t pd	Any A or B	Ğ	M = 0 V, S1 = S2 = 0 V, $S0 = S3 = 4.5 \text{ V} (\overline{SUM} \text{ mode})$	4		2	5	9	2	5	7	ns
^t pd	Any Ā or B	Ğ	M = 0 V, S0 = S3 = 0 V, $\text{S1} = \text{S2} = 4.5 \text{ V} (\overline{\text{DIFF}} \text{ mode})$	5		2	6	12	2	6	9	ns
^t pd	Any A or B	P	M=0 V, S1=S2=0 V, S0=S3=4.5 V (SUM mode)	5		2	6	11	2	6	8	ns
^t pd	Any Ā or B	P	M = 0 V, S0 = S3 = 0 V, $\text{S1} = \text{S2} = 4.5 \text{ V} (\overline{\text{DIFF}} \text{ mode})$	5		2	6	13	2	6	10	ns
^t pd	Āi or Bi	Fi	M = 0 V, S1 = S2 = 0 V, $\text{S0} = \text{S3} = 4.5 \text{ V} (\overline{\text{SUM}} \text{ mode})$	5		2	5	11	2	5	8	ns
^t pd	Āior Bi	Fi	M = 0 V, S0 = S1 = 0 V, S1 = S2 = 4.5 V (DIFF mode)	5		2	6	12	2	6	10	ns
^t pd	Āior Bi	Fi	M = 4.5 V (LOGIC mode)	6		2	6	16	2	6	11	ns
` ^t pd	Any Ā or B	A = B	M = 0 V, S0 = S3 = 0 V, $\text{S1} = \text{S2} = 4.5 \text{ V} (\overline{\text{DIFF}} \text{ mode})$	12		4	14	26	4	14	21	ns

additional 'AS881A switching characteristics involving status checks (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC}=5~V,$ $C_L=15~pF,$ $R_L=500~\Omega,$ $T_A=25~^{\circ}C$ $^{\prime}AS881A$ MIN TYP † MAX	SNS	C _L = ! R _L = ! T _A = !	= 4.5 V 50 pF, 500 Ω, MIN to 381A MAX	MAX SN:	74AS	881A MAX	UNIT
^t pd	Any Ā or B	Ē	$C_n = 4.5V$, $M = 4.5V$, S0 = S3 = 4.5V, $S1 = S2 = 0V$, Equality $(\vec{A}i = \vec{B}i \text{ or } \vec{A}i \neq \vec{B}i)$	8	2	10	19	2	10	15	ns
^t pd	Any Ā or B	C _{n+4}	$C_n = 4.5 \text{ V}, M = 4.5 \text{ V},$ S0 = S3 = 4.5 V, S1 = S2 = 0 V, Equality $(\overline{A}i = \overline{B}i \text{ or } \overline{A}i \neq \overline{B}i)$	10	2	12	24	2	12	18	ns
^t pd	Any Ā or B	P P	$C_n = 4.5 \text{ V}, M = 4.5 \text{ V},$ S2 = 4.5 V, S0 = S1 = S3 = 0 V, $(\overline{A}i = \overline{B}i = H \text{ or } \overline{A}i \text{ or } \overline{B}i = L)$	8	2	10	19	2	10	15	ns
[†] pd	Any Ā or B	C _{n+4}	$C_n = 4.5 \text{ V}, M = 4.5 \text{ V},$ S2 = 4.5 V, S0 = S1 = S3 = 0 V, $(\overline{A}i = \overline{B}i = H \text{ or } \overline{A}i \text{ or } \overline{B}i = L)$	f 1	2	13	25	2	13	19	ns

 $t_{pd} = t_{PHL} \text{ or } t_{PLH}$ TAll typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \, ^{\circ}\text{C}$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER		R INPUT IE BIT	OTHER DAT	TA INPUTS	OUTPUT	OUTPUT
TANAMETER	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	(SEE NOTE 1)
tPLH tPHL	Āi	- Bi	None	Remaining \overline{A} and $\overline{\overline{B}}$	C _n	Fi	In-Phase
tPLH tPHL	Bi	Āi	None	Remaining Ā and B	C _n	Fi	In-Phase
t _{PLH}	Āi	Bi	None	None	Remaining Ā and B, C _n	P	In-Phase
t _{PLH}	Bi	Āi	None	None	Remaining Ā and Ē, C _n	P	In-Phase
tPLH tPHL	Āi	None	Bi	Remaining B	Remaining Ā, C _n	G	In-Phase
tPLH tPHL	Bi	None	Āi	Remaining B	Remaining Ā, C _n	G.	In-Phase
t _{PLH}	Cn	None	None	All Ā	AII B	Any F or C _{n+4}	In-Phase
t _{PLH}	Āi	None	Bi	Remaining B	Remaining Ā, C _n	C _{n+4}	Out-of-Phase
t _{PLH}	Bi	None	Āi	Remaining B	Remaining Ā, C _n	C _{n+4}	Out-of-Phase

DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER		INPUT	OTHER DAT	TA INPUTS	OUTPUT	OUTPUT	
PANAIVIETEN	TEST	APPLY	APPLY	APPLY	APPLY	TEST	(SEE NOTE 1)	
	1531	4.5 V	GND	4.5 V	GND	1231	(SEE NOTE 1)	
t _{PLH}	Āi	None	Ēi	Remaining	Remaining	Fi	In-Phase	
tPHL.	~'	None	ы	Ā	B, C _n		III-i ilase	
^t PLH	Bi	Āi	None	Remaining	Remaining	Ēi	Out-of-Phase	
tPHL	Di	~ 1	None	Ā	B, C _n	• • • • • • • • • • • • • • • • • • • •	Out-or-mase	
^t PLH	Āi	None		None	Remaining	Ē	In-Phase	
tPHL	A	None	D)	None	A and B, C _n	r	III-Filase	
^t PLH	- Bi	Āi	None	None	Remaining	P	Out-of-Phase	
t _{PHL}	Di.	~'	None	None	A and B, C _n	'	Out of Filase	
^t PLH	Āi	Ri	None	None	Remaining	G	In-Phase	
^t PHL	/ (,	140110	110110	\overline{A} and \overline{B} , C_n		minasc	
^t PLH	Bi	None	Āi	None	Remaining	G	Out-of-Phase	
^t PHL		None		None	\overline{A} and \overline{B} , C_n	J	Out-or-i nase	
^t PLH	Āi	None	- Bi	Remaining	remaining	A = B	In-Phase	
^t PHL		110110	J.	Ā	₿, С _п	A = 0	III T TIGGE	
^t PLH	Bi	Āi	None	Remaining	Remaining	A = B	Out-of-Phase	
tPHL t		,	110.10	Ā.	В, С _п			
^t PLH	Cn	None	None	All	None	Cn + 4_	In-Phase	
^t PHL	911	110110	140110	\overline{A} and $\overline{\overline{B}}$		or any F	Wi i iidoo	
^t PLH	Āi	Bi	None	None	Remaining	Cn+4	Out-of-Phase	
^t PHL	, ((J.		,,,,,,,	. Ā, Ē, C _n	V₁1+4	00.0.111096	
^t PLH	Bi	None	Āi	None	Remaining	C _{n+4}	In-Phase	
t _{PHL}			- "		Ā, B, C _n	911+4	Music	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



D2661, DECEMBER 1985-REVISED MAY 1986

- Package Options Include Compact 300-mil or Standard 600-mil DIPs and Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:

Addition

Subtraction

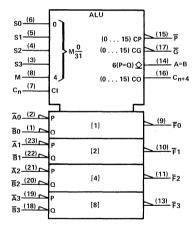
Shift Operand A One Position

Magnitude Comparison

Plus Twelve Other Arithmetic Operations

- Logic Function Modes Exclusive-OR Comparator AND, NAND, OR, NOR
- Dependable Texas Instruments Quality and Reliability

logic symbol†



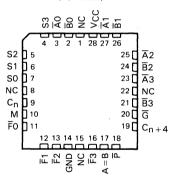
 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J, JT, N, and NT packages.

SN54AS181B . . . JT OR JW PACKAGE SN74AS181B . . . N OR NT PACKAGE (TOP VIEW)

Bo [1 U 2	24 23	VCC A1
S3 [3	22	Ē1 ĀΩ
S2 [4	21	Ā2
S1 🖺	5	20	B2
so 🖺	6	19	<u>A</u> 3
C _n	7	18	B3
М	8	17	G
Fo [9	16	C_{n+4}
F1 [10	15	P
F2 [11	14	A = B
GND □	12	13	F3

SN54AS181B . . . FK PACKAGE SN74AS181B . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

TYPICAL ADDITION TIMES (CL = 15 pF, RL = 280 Ω , TA = 25 °C)

NUMBER		ADDITION TIMES		PACK	AGE COUNT	CARRY METHOD
OF	USING 'AS181B	USING 'AS881B	USING 'S181	ARITHMETIC	LOOK-AHEAD	BETWEEN
BITS	AND'AS882	AND 'AS882	AND 'S182	LOGIC UNITS	CARRY GENERATORS	ALUs
1 to 4	5 ns	5 ns	11 ns	1		NONE
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

Texas Instruments

description

The 'AS181B arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, \overline{G} and \overline{P} , for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	ĀO	Вo	Ā1	B̄1	Ā2	B2	Ā3	B3	FΟ	F1	F2	F3	Cn	C _{n+4}	P	G
Active-high data (Table 2)	A0	во	Α1	В1	A2	B2	А3	В3	FO	F1	F2	F3	Ōn	\overline{C}_{n+4}	Х	Υ

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

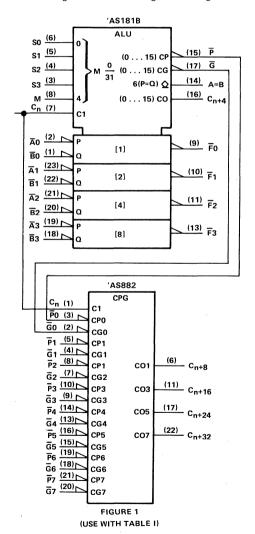
The 'AS181B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT Cn	OUTPUT Cn+4	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
Н	Н	A≥B	A≤B
н	L	A < B	A > B
L	н	A>B	A < B
L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

signal designations

In both Figures 1 and 2, the polarity indicators () indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181B together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.



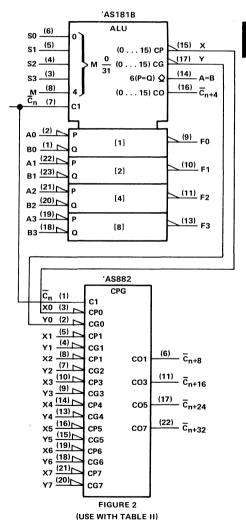


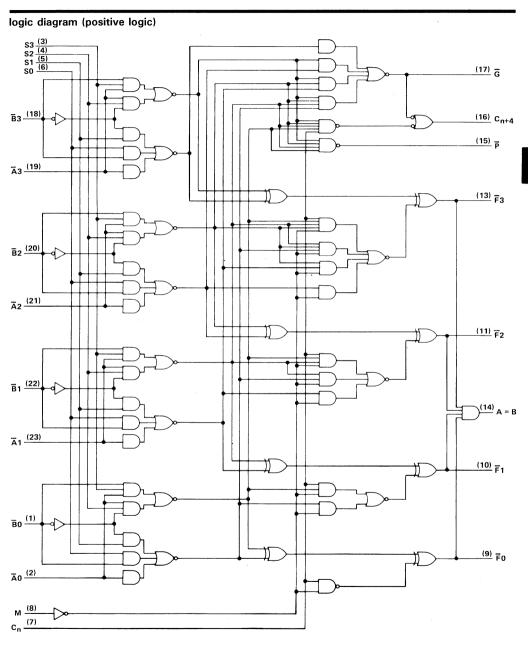
TABLE I

	SELE	CTIC	. B.I		ACTIVE-LOW DATA	
	SELE	CHO	714	M = H	M = L; ARITH	METIC OPERATIONS
62	S2	61	60	LOGIC	C _n = L	C _n = H
33	32	31	30	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	Н	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	Н	L	$F = \overline{A} + B$	F = AB MINUS 1	$F = A\overline{B}$
L	L	Н	Н	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	Н	L	L	$F = \overline{A + B}$	$F = A PLUS (A + \overline{B})$	F = A PLUS (A + B) PLUS 1
L	Н	L	Н	F = B	$F = AB PLUS (A + \overline{B})$	F = AB PLUS (A + B) PLUS 1
L	Н	Н	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	Н	Н	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B}) PLUS 1$
Н	L	L	L	F = ĀB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
н	L	L	Н	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
Н	L	Н	L	F = B	$F = A\overline{B} PLUS (A + B)$	F = AB PLUS (A + B) PLUS 1
Н	L	Н	Н	F = A + B	F = (A + B)	F = (A + B) PLUS 1
Н	Н	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
Н	н	L	н	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	Н	Н	L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	Н	Н	Н	F = A	F = A	F = A PLUS 1

TABLE II

	OF! F	0710			ACTIVE-HIGH DATA	\				
	SELE	CHC	PIN	M = H	M = L; ARITH	METIC OPERATIONS				
62	S2	61	60	LOGIC	C _n = H	C _n = L				
33	32	31	30	FUNCTIONS	(no carry)	(with carry)				
Ł	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1				
L	L.	L	Н	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1				
L	L	Н	L	F = AB	$F = A + \overline{B}$	$F \approx (A + \overline{B}) \text{ PLUS 1}$				
L	L	Н	Н	F = 0	F = MINUS 1 (2's COMP)	F ≈ ZERO				
L	Н	L	L	$F = \overline{AB}$	F = A PLUS AB	F = A PLUS AB PLUS 1				
L	Н	L	Н	. F = B	$F = (A + B) PLUS A\overline{B}$	F ≈ (A + B) PLUS AB PLUS 1				
L	Н	Н	L	F = A ⊕ B	F = A MINUS B MINUS 1	F ≈ A MINUS B				
L	Н	Н	Н	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$				
Н	L	L	L	$F = \widetilde{A} + B$	F = A PLUS AB	F ≈ A PLUS AB PLUS 1				
Н	L	L	Н	$F = \overline{A \oplus B}$	F = A PLUS B	F ≈ A PLUS B PLUS 1				
Н	L	Н	L	F = B	$F = (A + \overline{B}) PLUS AB$	F ≈ (A + B) PLUS AB PLUS 1				
Н	L	Н	Н	F = AB	F = AB MINUS 1	F = AB				
Н	Н	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1				
Н	Н	L	Н	$F = A + \overline{B}$	F = (A + B) PLUS A	A ≈ (A + B) PLUS A PLUS 1				
Н	Н	Н	L	F = A + B	$F = (A + \overline{B}) PLUS A$	$F \approx (A + \overline{B}) \text{ PLUS A PLUS 1}$				
н	н	Н	Н	F = A	F = A MINUS 1	F ≈ A				

^{*}Each bit is shifted to the next more significant position.



Pin numbers shown are for J, JT, N, and NT packages.



absolute maximum ratings over operating free-air temperature range (unless other	wise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Off-state output voltage (A = B output only)	7 V
Operating free-air temperature range: SN54AS181B	-55°C to 125°C
SN74AS181B	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN54AS181B			SN	74AS18	31B	UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT		
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
VIH	High-level input voltage		2			2			V -		
VIL	Low-level input voltage				0.8			0.8	V		
Voн	High-level output voltage	A = B output only			5.5			5.5	V		
Іон	High-level output current	All outputs except A = B and G			-2			- 2	mA		
		G			-3			-3	mA		
lOL	Low-level output current	All outputs except G			20			20	mA		
		G			48			48	mA		
TA	Operating free-air temperature		- 55		125	0		- 70	· °C		



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEAT AGUADIT	-1010	SN	154AS1	31B	SN	74AS18	31B	LINUT	
	PARAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	V	
Voн	Any output except A = B	V _{CC} = 4.5 V to 5.5 V	, I _{OH} = -2 mA	VCC - 2	2		V _{CC} -	- 2		٧	
	G	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V	
ТОН	A = B	$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V			0.1			0.1	mA	
VOL	Any output except \overline{G}	V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	V	
	G	$V_{CC} = 4.5 V$,	$I_{OL} = 48 \text{ mA}$		0.4	0.5		0.4	0.5	V	
	M input					0.1			0.1		
l ₁	Any A or B input	$V_{CC} = 5.5 V,$	V 7 V			0.3			0.3	mA	
"	Any S input		V - / V			0.4			0.4		
	Carry input					0.6			0.6	1	
	M input		V _I = 2.7 V			20			20	20	
1	Any A or B input	$V_{CC} = 5.5 \text{ V},$				60			60	μA	
ΙΗ	Any S input	νCC = 3.5 ν,				80			80		
	Carry input					120			120	1	
	M input					-0.5			-0.5		
1.	Any A or B input	V 55V	0.4.1/			- 1.5			- 1.5	1.1	
IL.	Any S input	$V_{CC} = 5.5 V,$	V = 0.4 V			- 2			- 2	mA	
	Carry input			-3		-3	1				
lo‡	All outputs except $A = B$ and \overline{G}	V _{CC} = 5.5 V,	Vo = 2.25 V	- 30	-45	-112	-30	-45	-112	mA	
	G		0	- 30		- 125	-30		- 125	1	
Icc		V _{CC} = 5.5 V			74	117		74	117	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54	$V_{CC} = 4.5$ $C_{L} = 50 \text{ pF}$ $R_{L} = 500 \text{ G}$ $T_{A} = \text{MIN} \text{ a}$ AS181B	;, }, to MAX	V, AS181B	UNIT	
		*		MIN	MAX	MIN	MAX		
tPLH	_			3	9	3	8.5		
t _{PHL}	C _n	C _{n + 4}		2	7	2	6.5	ns	
tPLH	Any	C _{n+4}	M = 0 V, S1 = S2 = 0 V,	3.5	13	5	12		
tPHL	Ā or ₿	^C n+4	S0 = S3 = 4.5 V (SUM mode)	3.5	12.5	5	12	ns	
tPLH	Any	6	M = 0 V, S0 = S3 = 0 V,	5	14.5	5	13		
t _{PHL}	Ā or ₿	C _{n+4}	S1 = S2 = 4.5 V (DIFF mode)	5	13.5	5	12.5	ns	
tPLH	_	Any F	M = 0 V (SUM or DIFF mode)	3	10.5	3	9	no	
^t PHL	Cn	Aily F	W = 0 V (SOW OF DIFF Hode)	3	8	3	7.5	ns	
tPLH	Any	G	M = 0 V, S1 = S2 = 0 V,	3	8.5	3	8		
t _{PHL}	Ā or B̄	G	S0 = S3 = 4.5 V (SUM mode)	2	7	2	6	ns	
tPLH	Any	G	M = 0 V, S0 = S3 = 0 V,	3	10.5	3	9.5	ns	
tPHL	Ā or ₿	G	S1 = S2 = 4.5 V (DIFF mode)	2	9	2	7	113	
tPLH	Any	P	M = 0 V, S1 = S2 = 0 V,	3	8.5	3	7.5	ns	
tPHL	A or B		S0 = S3 = 4.5 V (SUM mode)	2	7.5	2	6	115	
tPLH	Any	Ē	M = 0 V, S0 = S3 = 0 V,	3	10.5	3	9	ns	
tPHL	ĀorB		S1 = S2 = 4.5 V (DIFF mode)	3	8.5	3	8	115	
tPLH	Ai or	Fi	M = 0 V, S1 = S2 = 0 V,	3	11	3	9.5	ns	
t _{PHL}	Bi	F1	S0 = S3 = 4.5 V (SUM mode)	3	9	3	7.5	115	
tPLH	Ai or	ξi	M = 0 V, S0 = S3 = 0 V,	3	12	3	10.5	ns	
tPHL	Bi	F1	S1 = S2 = 4.5 V (DIFF mode)	3	11	3	9.5	115	
tPLH	Any	Any ₹	M = 0 V, S1 = S2 = 0 V,	3	13.5	3	12	ns	
t _{PHL}	Ā or B̄	Ony I	S0 = S3 = 4.5 V (SUM mode)	3	13	3	11.5	113	
tPLH	Any	Anv F	M = 0 V, S0 = S3 = 0 V,	3	16	3	14.5	ns	
t _{PHL}	A or B	City I	S1 = S2 = 4.5 V (DIFF mode)	3	13	3	12.5	113	
tPLH	Ai or Bi	Fi	M = 4.5 V (LOGIC mode)	3	12.5	3	11	ns	
^t PHL	7.1 51 51	,,	,===,	3	10	3	9.5	115	
t _{PLH}	Any	A = B	M = 0 V, S0 = S3 = 0 V,	4	19	4	17	ns	
^t PHL	A or B	^ - 5	\$1 = \$2 = 4.5 V (DIFF mode)	5	18.5	5	15	113	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT	OTHER INPUT SAME BIT		OTHER DAT	A INPUTS	OUTPUT	OUTPUT WAVEFORM	
PANAIVIETEN	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	(SEE NOTE 1)	
tPLH tPHL	Āi	Bi	None	Remaining A and B	Cn	Fi	In-Phase	
tPLH tPHL	Bi	Āi	None	Remaining Ā and B	C _n	Fi	In-Phase	
tPLH tPHL	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase	
tPLH tPHL	Bi	Āi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase	
t _{PLH}	Āi	None	Bi .	Remaining B	Remaining Ā, C _n	G	In-Phase	
tPLH tPHL	Bi	None	Āi	Remaining B	Remaining Ā, C _n	IG	In-Phase	
^t PLH ^t PHL	C _n	None	None	All Ā	All B	Any F or C _{n+4}	In-Phase	
tPLH tPHL	Āi	None	Bi	Remaining B	Remaining Ā, C _n	C _{n+4}	Out-of-Phase	
t _{PLH}	Bi	None	Āi	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT	INPUT SAME		OTHER DAT	A INPUTS	OUTPUT	OUTPUT WAVEFORM	
PANAIVIETEN	TEST	APPLY	APPLY	APPLY	APPLY	TEST	(SEE NOTE 1)	
		4.5 V	GND	4.5 V	GND			
^t PLH	Āi	None	Bi	Remaining	Remaining	Fi	In-Phase	
^t PHL				Ā	B, C _n			
tPLH	- Bi	Āi	None	Remaining	Remaining	Fi	Out-of-Phase	
tPHL	Di		None	Ā	B, Cn		Out-or-mase	
tPLH	Āi	None	Bi	None	Remaining	P	In-Phase	
t _{PHL}	Ai	None Bi		None	A and B, Cn	r	III-I IIase	
tPLH	Bi	Āi	None	None	Remaining	P	Out-of-Phase	
tPHL	Ві	AI	None	None	\overline{A} and \overline{B} , C_n	P	Out-of-Phase	
^t PLH	Āi	Bi	None	None	Remaining	G	In-Phase	
t _{PHL}	. AI	DI	None	None	\overline{A} and \overline{B} , C_n	u	in-Friase	
tPLH	Bi	None	Āi	None	Remaining	G	Out-of-Phase	
t _{PHL}	ы	None	Α'	None	\overline{A} and \overline{B} , C_n	G	Out-or-rhase	
^t PLH	Āi	None	Bi	Remaining	Remaining	A = B	In-Phase	
^t PHL	Α,	None	Di	Ā	B, C _n	A - B	m-i nase	
tPLH	Bi	Āi	None	Remaining	Remaining	A = B	Out-of-Phase	
t _{PHL}	ы	^'	None	Ā	B, C _n	А-Б	Out-or-mase	
t _{PLH}	Cn	None	None	All	None	C _{n+4}	In-Phase	
tPHL	∨n	None	None	A and B	None	or any F	III-FIIdSe	
tPLH	Āi	Bi	None	None	Remaining	C .	Out-of-Phase	
tPHL	Α,	101	None	None	Ā, B, C _n	C _{n+4}	Out-or-Phase	
t _{PLH}	Bi	None	Āi	None	Remaining	C	In-Phase	
^t PHL		None		None	Ā, B, C _n	C _{n+4}	III-F Hase	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER INPUT SAME BIT		OTHER	DATA INPUTS	OUTPUT	OUTPUT WAVEFORM
PANAMETER	TEST	APPLY 4.5 V	APPLY APPLY GND 4.5 V	APPLY GND	TEST	(SEE NOTE 1)	
tPLH	Āi	Bi	None	None	Remaining	Fi	Out-of-Phase
^t PHL					\overline{A} and \overline{B} , C_n		
tPLH	Bi	Āi	None	None	Remaining	Fi	Out-of-Phase
tPHL]]	1,45116	1,500	A and B, C _n		Out-01-Filase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE

FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT	OTHER INPUT SAME BIT		OTHER DAT	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
PARAMETER	TEST	APPLY	APPLY	APPLY	APPLY	TEST	(SEE NOTE 1)	
	1631	4.5 V	GND	4.5 V	GND	1201	(GEE NOTE 1)	
tPLH	Āi	Ēi	None	Remaining	None	P	Out-of-Phase	
tPHL .	Ai	ы	None	Ā and B̄, C _n	None		Out-of-Friase	
t _{PLH}	Bi	Bi Ai None	None	Remaining	None	P	Out-of-Phase	
tPHL	ы	A'	A and B, Cn		None		Out-or-Filase	
tPLH	Āi	None	Bi	Remaining	None	P	In-Phase	
tPHL	Ai	None	Ы	\overline{A} and \overline{B} , C_n	None	1 '	in-i ilase	
tPLH	Bi	None	Āi	Remaining	None	Ē	In-Phase	
t _{PHL}	ы	None		\overline{A} and \overline{B} , C_n	None	'	III T TIUSE	
tPLH	Āi	Bi	None	Remaining	None	Cn+4	In-Phase	
tPHL	A	B1	None	A and B, Cn	None	On+4	III-I IIdae	
tPLH	Bi	Āi	None	Remaining	None	Cn+4	In-Phase	
tPHL	ы		None	\overline{A} and \overline{B} , C_n	140116	On+4	III-Filase	
tPLH	Āi	None	Bi	Remaining	None	C _{n+4}	Out-of-Phase	
tPHL	AI	None	Ы	A and B, C _n	140116	On+4	Out of Thase	
tPLH	Bi	None	Āi	Remaining	None	Cn+4	Out-of-Phase	
tPHL	OI .	None		\overline{A} and \overline{B} , C_n	,,,,,,,,		Out-oi-Filase	

INPUT PAIRS HIGH/NOT HIGH TEST TABLE

FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

PARAMETER	INPUT	OTHER INPUT SAME BIT		OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND	TEST	(SEE NOTE 1)
tPLH tPHL	Āi	Bi	None	Remaining Ā, C _n	Remaining	P	In-Phase
tPLH tPHL	Bi	Āi	None	Remaining B , C n •	Remaining Ā	Ē	In-Phase
tPLH tPHL	Āi	Bi	None	Remaining Ā, C _n	Remaining B	Cn+4	Out-of-Phase
tPLH tPHL	Bi	Āi	None	Remaining B, C _n	Remaining Ā	C _{n+4}	Out-of-Phase

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



PRODUCT **PREVIEW**

SN54AS182, SN74AS182 LOOK-AHEAD CARRY GENERATOR

D2661, DECEMBER 1983-REVISED MAY 1986

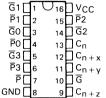
- High-Speed Replacement for the 'S182
- Offers Carry Functions in a Compatible Form for Direct Connections to the ALU
- Cascadable to Perform Look-Ahead Across n-Bit Adders
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

PIN DESIGNATIONS

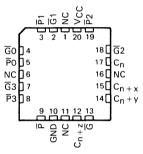
ALTERNATIVE	DESIGNATIONS [†]	FUNCTION		
Ğ0, Ğ1, Ğ2, Ğ3	G0, G1, G2, G3	Carry Generate Inputs		
PO, P1, P2, P3	P0, P1, P2, P3	Carry Propagate Inputs		
Cn	<u></u>	Carry Input		
C_{n+x} , C_{n+y} ,	\overline{C}_{n+x} , \overline{C}_{n+y} ,	Carry Outputs		
C_{n+z}	\overline{C}_{n+z}	Curry Gutputs		
G	Y	Carry Generate Output		
P X		Carry Propagate Output		
	VCC	. Supply Voltage		
	GND	Ground		

[†] Interpretations are illustrated in connection with the Function Tables for the 'AS181B and 'AS881A.

SN54AS182 . . . J PACKAGE SN74AS182 . . . D OR N PACKAGE (TOP VIEW)



SN54AS182 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

description

The 'AS182 look-ahead carry generators are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders.

This generator, when used in conjunction with the 'AS181B or 'AS881A Arithmetic Logic Unit ALU, provides high-speed carry look-ahead capability for any word length. The 'AS182 generates the look-ahead (anticipated carry) across a group of four ALUs. In addition, other carry look-ahead circuits may be employed to anticipate carry-across sections of four look-ahead packages up to n-bits. The method of cascading 'AS182 circuits to perform multilevel look-ahead is illustrated under the typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connections to the ALU. Reinterpretations of carry functions as explained on the 'AS181B and 'AS881A data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'AS182 are:

$$\begin{array}{lll} C_{n+x} = G0 + P0 \ C_n & \overline{C}_{n+x} = \overline{Y0 \ (x0 + C_n)} \\ C_{n+y} = G1 + P1 \ G0 + P1 \ P0 \ C_n & \overline{C}_{n+x} = \overline{Y1 \ [x1 + Y0 \ (x0 + C_n)]} \\ C_{n+z} = G2 + P2 \ G1 + P2 \ P1 \ G0 + P2 \ P1 \ P0 \ C_n & \overline{C}_{n+z} = \overline{Y2 \ (x2 + Y1 \ [x1 + Y0 \ (x0 + C_n)]} \\ \overline{G} = G3 + \overline{P3} \ G2 + \overline{P3} \ P2 \ G1 + \overline{P3} \ P2 \ P1 \ \overline{G0} & Y = Y3 \ (x3 + Y2) \ (x3 + X2 + Y1) \ (x3 + X2 + X1 + Y0) \\ \overline{F} = \overline{P3} \ \overline{P2} \ P1 \ \overline{P0} & X = X3 + X2 + X1 + X0 \end{array}$$

SN54AS182, SN74AS182 LOOK-AHEAD CARRY GENERATOR

FUNCTION TABLE FOR G OUTPUT INPUTS OUTPUT G3 Ğ0 P1 G2 Ğ1 P3 P2 G x L X х Х Х L х L Х Х Х Х Ĺ L Х х Х Х L L L Х Х L L L L L All other combinations

		OUTPU	
NPUT	S		OUTPU
P2	P1	ĒΩ	P

Ē3

All other

combinations

FC	FOR C _{n + x} OUTPUT								
	NPUT	OUTPUT							
Ğ0	P0	C _{n+x}							
L	Х	Х	Н						
Х	L	Н	н						
	all othe nbinati	L							

FUNCTION TABLE

FUNCTION TABLE Cn + y OUTPUT

			OUTPUT		
Ğ1	Ğ0	P1	P0	Cn	C _{n+y}
L	Х	Х	Х	Х	Н
Х	L	L	Χ	Х	н
Х	X	L	L	Н	н
	C	i -			

FUNCTION TABLE FOR Cn + 2 OUTPUT

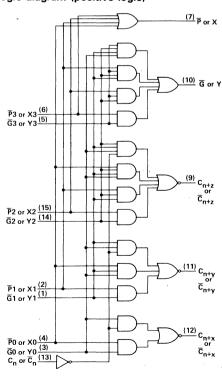
н

INPUTS							OUTPUT		
Ğ2	G1	Ğ0	P2	P1	P0	Cn	C _{n+z}		
L	Х	Х	Х	Х	Х	X	Н		
X	L	X	L	X	Х	Х	н		
Χ	Х	L	L	L	X	Х	н		
Χ	Χ	Х	L	L	L	н	н		
All other combinations							L		

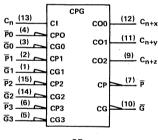
H = high-level, L = low level, X = irrelevant.

Any inputs not shown in a given table are irrelevant with respect

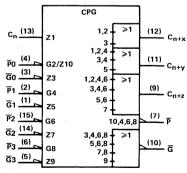
logic diagram (positive logic)



logic symbols†



OR



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for D, J, and N packages.



SN54AS182, SN74AS182 LOOK-AHEAD CARRY GENERATOR

absolute maximum ratings over operating free-air tempera	ture range (unles:	otherwise noted)
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Supply voltage, VCC	
Input voltage	7 V
Operating free-air temperature range	: SN54AS18255°C to 125°C
	SN74AS182
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SI	SN54AS182			SN74AS182		
-		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8		-	0.8	V
Іон	High-level output current			- 2			- 2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54AS182			SN74AS182			
					TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			- 1.2	V	
Vон		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$		V _{CC} -			V _{CC} -2			V	
VOL	`	$V_{CC} = 4.5 V$,	$l_{OL} = 20 \text{ mA}$		0.3	0.5		0.3	0.5	V	
	C _n	V _{CC} = 5.5 V,				0.1			0.1	mA	
	<u>P</u> 3					0.2			0.2		
1,	₽2		V _I = 7.0 V			0.3	<u></u>		0.3		
'	₱0, ₱1, ₲3		.,			0.4			0.4		
	Ğ0, Ğ2					0.7			0.7		
	G1					0.8			0.8		
	Cn	V _{CC} = 5.5 V,	V ₁ = 2.7 V			0.02			0.02	mA	
	₽3					0.04			0.04		
ηн	P2					0.06			0.06		
'IH	P0, P1, G3					0.08			0.08		
	<u>G</u> 0, <u>G</u> 2					0.14			0.14		
	G1					0.16			0.16		
	Cn		V ₁ = 0.4 V			-0.5			-0.5	mA	
	P3	V _{CC} = 5.5 V,				- 1			- 1		
	<u>₽</u> 2					- 1.5			- 1.5		
ΊL	Po, P1, G3					- 2			- 2		
	Ğ0, Ğ2					-3.5			-3.5	l	
	G1					- 4			-4		
lo [‡]		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA	
Іссн		V _{CC} = 5.5 V			17		17		mA		
^I CCL				23			23			A	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, IOS.



switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	V _{CC} = 4.5 C _L = 50 p R _L = 500 T _A = MIN	UNIT	
1			SN54AS182	SN74AS182	
			MIN TYP [†] MAX	MIN TYP [†] MAX	1
^t PLH	Cn	C _{n+x} , C _{n+y} C _{n+z}	5	5	- ns
^t PHL	∨n	C _{n+z}	5	5	
^t PLH	Any ₱ or ₲	C _{n+x} , C _{n+y}	5	5	ns
t _{PHL}	Any i oi d	C _{n+z}	5	5	
^t PLH	Any ₱ or ₲	G	6	6	ns ns
^t PHL	Any i oi d	9	5	5	
tPLH	Any ₱	Ē	5	5	
^t PHL	Auy I	<u> </u>	5	5	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

'AS181B, 'AS881A

Cn G P Cn G

NOTE: Remaining inputs and outputs of 'AS181B or 'AS881A are not shown.

FIGURE 1. THE 'AS182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT

SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

D2661, DECEMBER 1982-REVISED MAY 1986

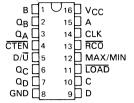
- Single Down/Up Count Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable with Load Control
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

descriptions

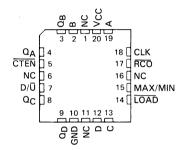
The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{\text{CTEN}}$) is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/\overline{U}) input. When D/\overline{U} is low, the counter counts up and when D/\overline{U} is high, it counts down

SN54ALS190, SN54ALS191 . . . J PACKAGE SN74ALS190, SN74ALS191 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS190, SN54ALS191 . . . FK PACKAGE
(TOP VIEW)



NC - no internal connection.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{\text{CTEN}}$ and $\overline{\text{D/U}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

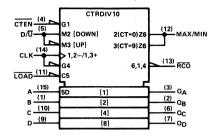
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/Ū, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

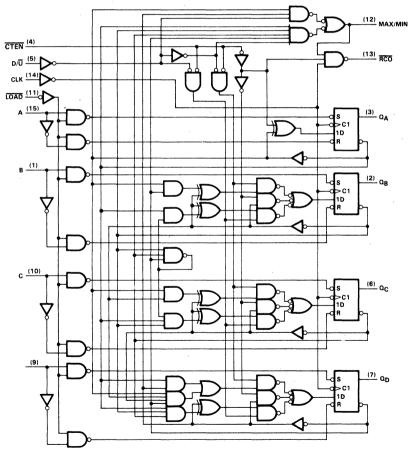
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS190 and SN54ALS191 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74ALS190 and SN74ALS191 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

'ALS190 logic symbol[†]



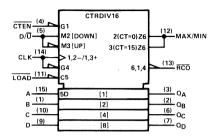
'ALS190 logic diagram (positive logic)



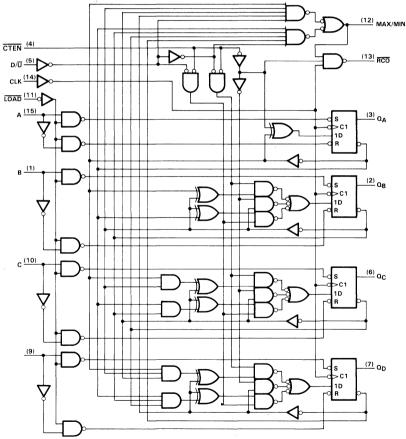
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.



'ALS191 logic symbol[†]



'ALS191 logic diagram (positive logic)



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.



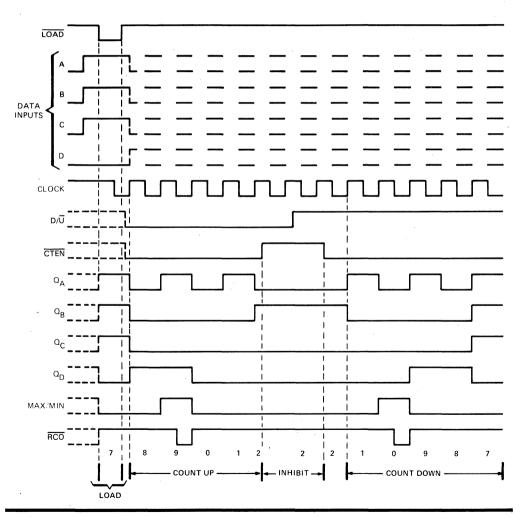
ALS and AS Circuits

typical load, count, and inhibit sequences

'ALS190

Illustrated below is the following sequence:

- 1. Load (preset) to BCD seven.
- 2. Count up to eight, nine (maximum), zero, one, and two.
- 4. Count down to one, zero (minimum), nine, eight, and seven.



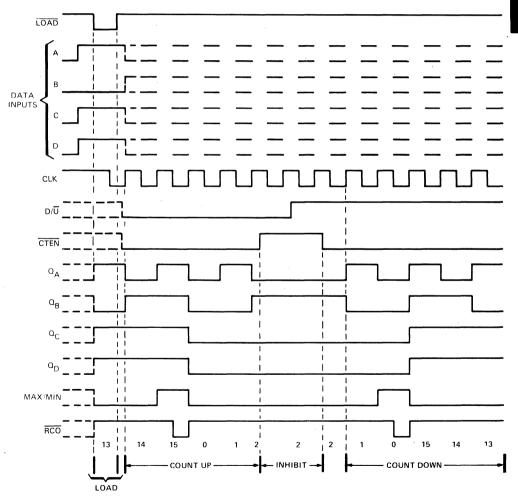


typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

- 1. Load (preset) to binary thirteen.
- 2. Count up to fourteen, fifteen (maximum), zero, one, and two.
- 3. Inhibit.
- 4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	
Operating free-air temperature range:	SN54ALS190, SN54ALS19155 °C to 125 °C
	SN74ALS190, SN74ALS191 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	,				N54ALS N54ALS		1	74ALS1 74ALS1		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	ge		2			2			V
VIL	Low-level input voltag	je				0.7			0.8	V
ЮН						-0.4			-0.4	mA
lOL	Low-level output current					4			8	mA
£	Clock frequency	'ALS190		0		20	0		25	MHz
†clock	Clock frequency	'ALS191		0		20	0		30	IVIIIZ
		CLK high or low	'ALS190	25			20			
t _W	Pulse duration	CER High or low	'ALS191	20			16.5			ns
		LOAD low		25			20			
		Data before LOAD1		25			20			
١.	Setup time	CTEN before CLK1		45			20			ns
t _{su}	Setup time	D/U before CLK1		45			20			115
	•	LOAD inactive before	CLK1	20			20			
		Data after LOAD1		5			5			
th	Hold time	CTEN after CLK1		0			0			ns
		D/U after CLK1		0			0			
TA				- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST COMPLETE	TEST CONDITIONS		SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191		
PARAMETER	TEST CONDITIO	ons	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			-1.5	V
VoH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -0.4 mA	Vcc-	2		Vcc-	2		V
Va	$V_{CC} = 4.5 V,$	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V}$	IOL = 8 mA					0.35	0.5	ľ
I _I	V _{CC} = 5:5 V,	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
CTEN or CLK	Vcc = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	A
IIL All others	VCC = 5.5 V,	V = 0.4 V			-0.1			-0.1	mA
lo [‡]	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
Icc	V _{CC} = 5.5 V,	All inputs at 0 V		12	22		12	22	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS190, SN54ALS191, SN74ALS190, SN74ALS191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	(OUTPUT) T _A = MIN to MAX SN54ALS190 SN74A SN54ALS191 SN74A				UNIT
	'ALS190		MIN	MAX	MIN	MAX	
f _{max}	'ALS191		20		25 30		MHz
tPLH			7	37	8	30	
tPHL	LOAD	Any Q	8	34	8	30	ns
t _{PLH}	A, B, C, D	1	4	25	4	21	
tPHL	A, B, C, D	Any Q	4	25	4	21	ns
^t PLH	CLK	RCO	5	24	5	20	ns
^t PHL	OLK	1100	5	25	5	20	113
^t PLH	CLK	Any Q	3	26	3	. 18	ns
^t PHL	our.	/, C	3	22	3	18	110
^t PLH	CLK	MAX/MIN	8	37	8	31	ns
^t PHL			8	34	8	31	1.0
^t PLH	D/Ū	RCO	12	45	15	37	ns
^t PHL		1	10	36	10	28	
^t PLH	D/Ū	MAX/MIN	8	35	8	25	ns
^t PHL	3,0	III JUNIO	8	30	8	25	
^t PLH	CTEN	RCO	4	21	4	18	ns
^t PHL		1.00	4	23	4	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

D2661, DECEMBER 1982-REVISED MAY 1986

- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

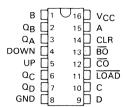
description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

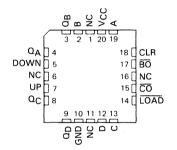
The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

SN54ALS192, SN54AS193 . . . J PACKAGE SN74ALS192, SN74ALS193 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS192, SN54ALS193 . . . FK PACKAGE (TOP VIEW)



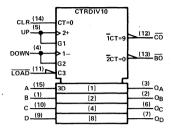
NC - no internal connection.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

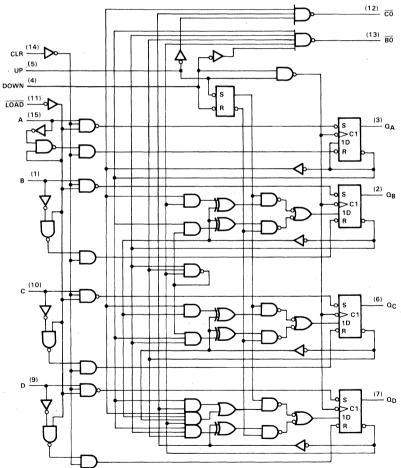
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (\overline{CO}) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS192 and SN54ALS193 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74ALS192 and SN74ALS193 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

'ALS192 logic symbol[†]



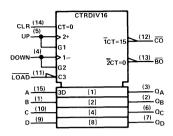
'ALS192 logic diagram (positive logic)



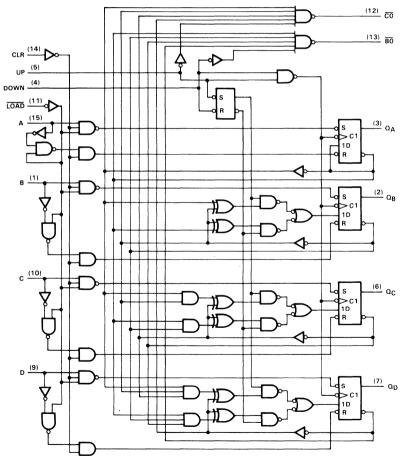
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.



'ALS193 logic symbol†



'ALS193 logic diagrams (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

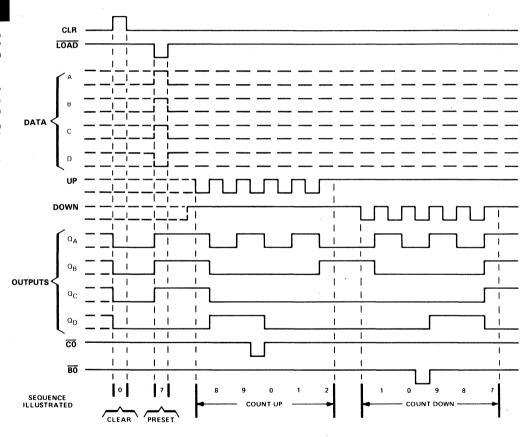


typical clear, load, and count sequence

'ALS192

Illustrated below is the following sequence:

- 1. Clear outputs to zero.
- 2. Load (preset) to BCD seven.
- 3. Count up to eight, nine, carry, zero, one, and two.
- 4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

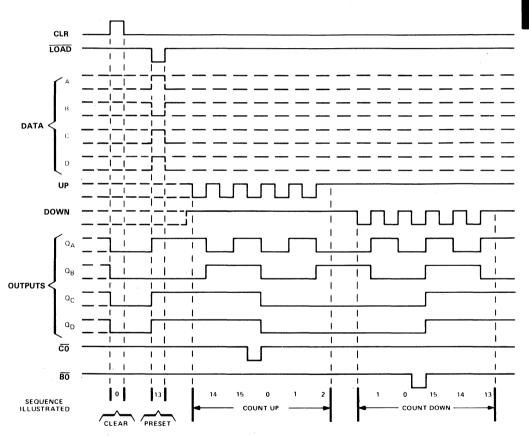


typical clear, load, and count sequences

'ALS193

Illustrated below is the following sequence:

- 1. Clear outputs to zero.
- 2. Load (preset) to binary thirteen.
- 3. Count up to fourteen, fifteen, carry, zero, one, and two.
- 4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.



SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		
Input voltage		
Operating free-air temperature range:	SN54ALS192, SN54ALS193	– 55 °C to 125 °C
	SN74ALS192, SN74ALS193	0°C to 70°C
Ctorogo tompovotivo vones		05.00 + 450.00

recommended operating conditions

					N54ALS N54ALS		1	74ALS1 74ALS1		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input vo	Itage		2			2			٧
VIL	Low-level input vol	Itage				0.7			0.8	٧
ЮН	High-level output current					-0.4			-0.4	mA
lOL	Low-level output current					4			8	mA
4	Clock frequency	'ALS192		0		20	0		25	MHz
†clock	Clock frequency	'ALS193		0		20	0		30	IVITIZ
		CLR high	10			10			ns	
	Pulse duration	LOAD low		25			20			_ ""
tw	ruise duration	UP or DOWN high or low	'ALS192	25			20			ns
		OF OF DOWN High of low	'ALS193	30			16.5			1115
		Data before LOAD1		25	1		20			
t _{su}	Setup time	CLR inactive before UP1 or I	OOWN1	20	Ī		20			ns
		LOAD inactive before UP1 or	DOWNI	. 20			20			115
	,	Data after LOAD1		5			5			
t _h	Hold time	UP high after DOWN1		0			0			ns
		DOWN high after UP1		0			0]
TA	Operating free-air t	perating free-air temperature				125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS		SN54ALS192 SN54ALS193			SN SN			
PARAMETER	TEST CONDITION		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}	$V_{CC} = 4.5 V,$	l ₁ = -18 mA			- 1.5			- 1.5	V
V _{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		V
Va	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VoL	V _{CC} = 4.5 V	I _{OL} = 8 mA					0.35	0.5	
1	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
IH	$V_{CC} = 5.5 V,$	V _I = 2.7 V	T		20			20	μΑ
UP, DOWN	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
I _{IL} All others	VCC = 5.5 V,	V = 0.4 V			-0.1			-0.1	IIIA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	- 30		-112	mA
Icc	$V_{CC} = 5.5 V$,	See Note 1		12	22		12	22	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5 V.



SN54ALS192, SN54ALS193, SN74ALS192, SN74ALS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

switching characteristics (see Note 2)

PARAMETER	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $\text{SN54ALS192} \qquad \text{SN74ALS192}$					
			1	ALS193	SN74			
			MIN	MAX	MIN	MAX		
	'Α	LS192	20		25		MHz	
fmax	Α΄	LS193	25		30		IVITIZ	
^t PLH	Up	со	3	20	4	16	ns	
^t PHL	7 00		3	21	5	18	113	
^t PLH	Down	во	4	20	4	16	ns	
^t PHL	Down	1	5	22	5	18	,,,,	
^t PLH	Up or Down	Any Q	4	27	4	19	ns	
^t PHL	Op or Down	Ally G	4	23	4	17	113	
^t PLH	LOAD	Any Q	8	38	8	30	ns	
^t PHL	LOAD	Ally C	8	37	8	. 28	,,,,	
^t PHL	CLR	Any Q	5	20	5	17	ns	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



SN54AS194, SN74AS194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

D2661 DECEMBER 1983-REVISED MAY 1986

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data Latching Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These bidirectional shift registers feature parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

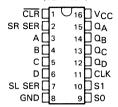
Inhibit clock (temporary data latch/do nothing) Shift-right (in the direction Q_A toward Q_D) Shift-left (in the direction Q_D toward Q_A) Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

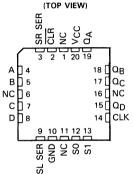
Shift-right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When SO is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

The SN54AS194 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74AS194 is characterized for operation from 0 $^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54AS194 . . . J PACKAGE SN74AS194 . . . D OR N PACKAGE (TOP VIEW)



SN54AS194 . . . FK PACKAGE



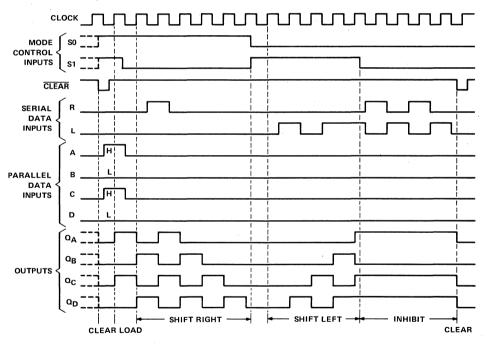
NC-No internal connection

					FUNCTIO	N T	ABLE							
				INPUT	S						OUT	PUTS		
CLEAR	МС	DE/	01 001	SEI	RIAL		PARA	LLEI	_		_	_	_	l
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	Α	В	С	D	QA	αВ	σ_{C}	σ_{D}	l
L	×	×	×	Х	Х	х	Х	Х	X	L	L	L	L	
н	×	X	L	×	х	x	Х	Х	Х	Q _{A0}	α_{B0}	σ_{CO}	σ_{D0}	
н	н	Н	1	х	X	а	b	С	d	а	b	С	d	l
н	L	Н	↑,	x	H.	х	X	Х	X	н	\mathbf{Q}_{An}	Q_{Bn}	Q_{Cn}	
н	L	Н	Ť	X	L	x	Х	Х	Х	L	Q_{An}	Q_{Bn}	\mathtt{Q}_{Cn}	
н	Н	L	1	н	X	х	Х	Х	Х	QBn	Q_{Cn}	\mathtt{Q}_{Dn}	Н	
н	Н	L	1	L	Х	x	Х	Х	Х	QBn	α_{Cn}	α_{Dn}	L	l
н	L	L	×	х	Х	х	X	Х	X	Q _{A0}	σ_{B0}	σ_{CO}	σ_{D0}	l

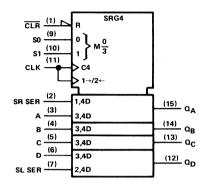
- H = high level (steady state)
- L = low level (steady state)
 X = irrelevant (any input, including tran-
- sitions)

 ↑ = transition from low to high level
- a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
- Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
- $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Cn}$ respectively, before the most-recent \uparrow transition of the clock.

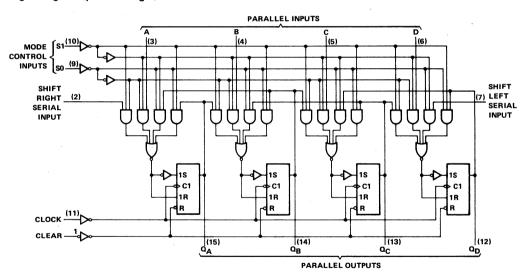
typical clear, load, right-shift, inhibit, and clear sequences



logic symbol†



logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54AS194 -55°C to 125°C SN74AS194 .0°C to 150°C Storage temperature range -65°C to 150°C

recommended operating conditions

			SI	154AS1	94	SI	174AS1	94	LINUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage		1		0.8			0.8	V
ЮН	High-level output current			- 2			- 2	mA	
lOL	Low-level output current				20			20	mA
f _{clock}	Clock frequency		0		75	0		80	MHz
		CLR	4			4			
t_{W}	Pulse duration	CLK high	4			2			ns
		CLK low	6			6			
+	Set-up time before CLK↑	Select	9			8			
t _{su}	Set-up time before CERT	Data	3.5			3			ns
twr	Recovery time	CLR	6			6			ns
^t h	Hold time, data after CLK↑		0.5			0			ns
TA	Operating free-air temperature				125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

ARAMETER	TECT CONDITIO	NAIC	SI	SN54AS194			SN74AS194			
ANAMETER	TEST CONDITIO	JNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -	2		Vcc-	2		V	
	$V_{CC} = 4.5 V$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V	
Data, CLK, CLR	V	1/. 7.1/			0.1			0.1		
Mode, SL, SR	νCC = 5.5 v,	V ₁ = 7 V			0.2			0.2	mA	
Data, CLK, CLR	V F F V	V. 27.V			20			20		
Mode, SL,SR	νCC = 9.9 v,	V = 2.7 V			40			40	μΑ	
Data, CLK, CLR	V				-0.5			-0.5		
Mode, SL, SR	vcc = 5.5 v,	V ₁ = 0.4 V			- 1			- 1	mA	
	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	-30		-112	mA	
	Voc = 5.5.V	Outputs high		30	49		30	43	^	
	νCC = 5.5 V,	Outputs low		38	60		38	53	mA.	
	Data, CLK, ČLR Mode, SL, SR Data, CLK, ČLR Mode, SL,SR Data, CLK, ČLR	V _{CC} = 4.5 V, V _{CC} = 4.5 V to 5.5 V, V _{CC} = 4.5 V, V _{CC} = 4.5 V, V _{CC} = 4.5 V, V _{CC} = 5.5 V,	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	MIN VCC = 4.5 V,	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	VCC = 4.5 V,	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	VCC = 4.5 V,	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS194, SN74AS194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	C _I R: T,	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to MAX}$ $SN54AS194 = SN74AS194$				
			MIN	MAX	MIN	MAX	1	
f _{max}			75		80		MHz	
^t PLH	CLK	Any Q	2.5	8	3	7	ns	
^t PHL	- CLN	Ally C	2.5	8	3	7	. 113	
^t PHL	CLR	Any Q	3.5	13	4	12	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



- Parallel-to-Serial, Serial-to-Parallel Conversions
- Parallel Synchronous Loading
- J and K Inputs to First Stage
- Right-Shift Only with Complementary Outputs on Last Stage
- **Direct Overriding Clear**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

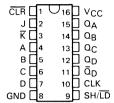
Parallel (broadside) load Shift (in the direction QA toward QD)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading serial data flow is inhibited.

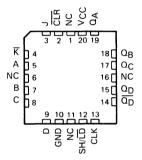
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

The SN54AS195 is characterized for operation over the full military range of -55 °C to 125 °C. The SN74AS195 is characterized for operation from 0°C to 70°C.

SN54AS195 . . . J PACKAGE SN74AS195 . . . D OR N PACKAGE (TOP VIEW)

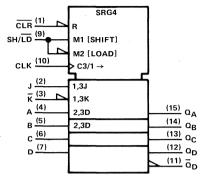


SN54AS195 . . . FK PACKAGE (TOP VIEW)



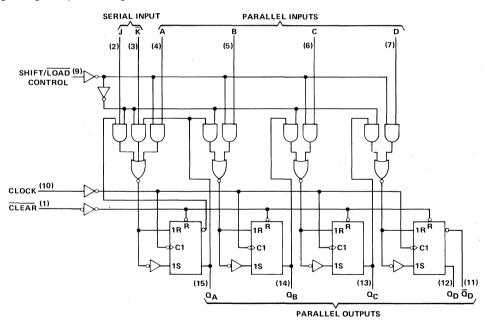
NC-No internal connection

logic symbol†



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

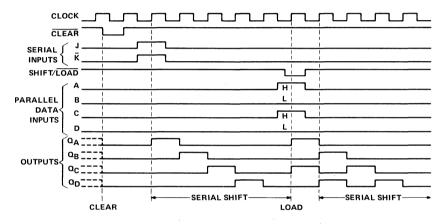


SN54AS195, SN74AS195 **4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

FUNCTION TABLE

		INPUTS							OUTPUTS						
CLEAR	SHIFT/LOAD	СГОСК	SEF	RIAL	P	AR/	ALLI	EL	<u> </u>		0-	Ω-	\overline{a}_{D}		
CLEAR	SHIFT/LUAD	CLOCK	J	K	Α	В	С	D	QA	αв	σc	αD	αр		
L	X	Х	X	Х	X	Х	Х	X	L	L	L	L	Н		
н	L	↑	×	Х	a	b	С	d	а	b	С	d	d		
Н	н	L	×	X	×	Х	Х	Х	QAO	α_{BO}	σ^{CO}	σ_{DO}	\overline{a}_{DO}		
Н	н	· 1	L	Н	×	Х	Х	Х	QAO	Q_{AO}	α_{Bn}	Q_{Cn}	\overline{a}_{Cn}		
Н	н	 	L	L	X	Х	Х	Х	L	Q_{An}	a_{Bn}	α_{Cn}	\overline{a}_{Cn}		
н	н	1	Н	Н	X	Х	Х	X	Н	Q_{An}	a_{Bn}	q_{Cn}	\overline{a}_{Cn}		
Н	н	1	. н	Н	X	Х	Х	X	α _{An}	Q_{An}	α_{Bn}	a_{Cn}	$\overline{\alpha}_{Cn}$		

typical clear, shift, and load sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54AS195 -55°C to 125°C SN74AS195 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

			Si	N54AS1	95	SI	N74AS1	95	
,			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input volt	age	2			2			V
VIL	Low-level input volta	age		·	0.8			0.8	V
ІОН	High-level output cu	rrent			- 2			-2	mA
lOL	Low-level output cu	rent			20			20	mA
fclock	Clock frequency		0		60	0		70	MHz
	Pulse duration	CLK high	4			4			
tw	ruise duration	CLR low	4			4			ns
		Data before CLK↑	4			3.5			
t _{su}	Setup time	SH/LD before CLK↑	9			8			ns .
		CLR high before CLK1	6.5			6			
	Hold time	Data after CLK↑	1			0.5			
^t h	riola time	SH/LD after CLK↑	0			0			ns
TA	Operating free-air te	mperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

20	DAMETER	TEST COMPLE	IONO	SI	V54AS1	95	SN	174AS1	95	LIBUT
PA	RAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
Voн		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -	2		V _{CC} -2			V
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	٧
1.	SH/LD	V 55.V				0.2			0.2	
11	All others	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
	SH/LD					40			40	
ΊΗ	All others	$V_{CC} = 5.5 V$	$V_I = 2.7 V$			20			20	μA
	SH/LD	V	V 0.4.V			- 1			- 1	4
ήL	All others	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.5			-0.5	mA
1o [‡]		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Іссн		V _{CC} = 5.5 V			32	51		32	51	mA
ICCL		V _{CC} = 5.5 V	· · · · · · · · · · · · · · · · · · ·		36	57		36	57	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS195, SN74AS195 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX					
			SN54	AS195	SN74	AS195			
		1	MIN	MAX	MIN	MAX]		
f _{max}			60		70		MHz		
^t PLH	CLK	Any Q	3	10	3	8.5			
tPHL	CLK	Ally C	2.5	11.5	2.5	10.5	ns		
^t PLH	CLR	ā₀	4	9.5	4	8	ns		
^t PHL	- CLN	Q _A thru Q _D	5	13	5	11.5] ''s		

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.



SN54ALS229A, SN74ALS229A 16 × 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

D2876, MARCH 1986-REVISED MAY 1986

- Independent Asychronous Inputs and Outputs
- 16 Words by 5 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

description

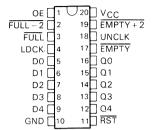
These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

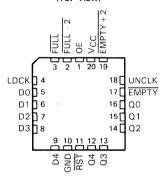
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the FULL, EMPTY, FULL -2, and EMPTY +2 output flags. The FULL output will be low whenever the memory is full, and high whenever not full. The FULL -2 output will be low whenever the memory contains 14 data words. The EMPTY output will be low whenever the memory is empty, and high whenever it is not empty. The EMPTY +2 output will be low whenever 2 words remain in memory.

SN54ALS229A . . . J PACKAGE SN74ALS229A . . . DW OR N PACKAGE (TOP VIEW)

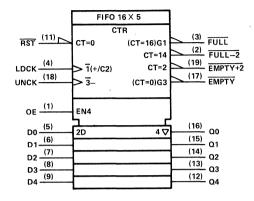


SN54ALS229A . . . FK PACKAGE SN74ALS229A . . . FN PACKAGE (TOP VIEW)

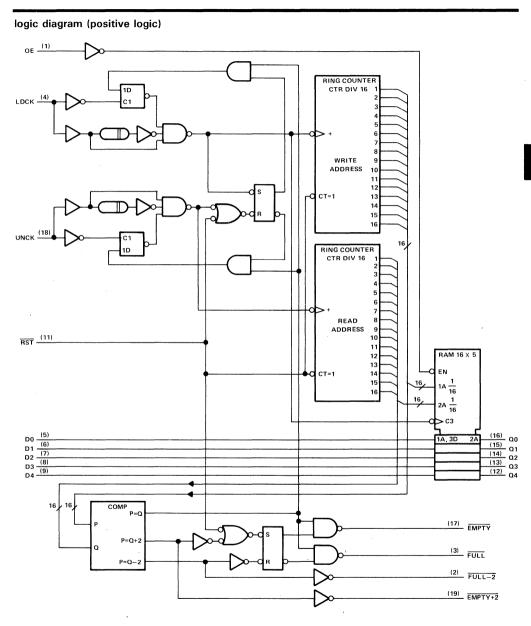


A low level on the reset input (\overline{RST}) resets the internal stack control pointers and also sets \overline{EMPTY} low and sets \overline{FULL} , $\overline{FULL}-2$, and $\overline{EMPTY}+2$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a \overline{RST} pulse or from an empty condition, will cause \overline{EMPTY} to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

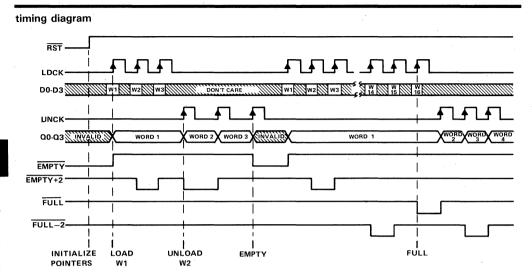
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	٧
Input voltage	
Voltage applied to a disabled 3-state output	V
Operating free-air temperature range: SN54ALS229A55°C to 125°	°C
SN74ALS229A 0 °C to 70 °C	°C
Storage temperature range	эC

recommended operating conditions

				SN	54ALS	229A	SN	174ALS	229A	UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage	t voltage				0.8			0.8	V
lou	High-level output current		Q outputs			-1.0			- 1.6	mA
ЮН	nign-lever output current		Status flags			-0.4			-0.4	1 mA
1	Low-level output current		Q outputs			12			24	
lOL	Low-level output current		Status flags			4			8	mA.
	Clark for any		LDCK	0		25	. 0		30	
fclock	Clock frequency		UNCK	0		25	0		30	MHz
			RST low	20			15			
			LDCK low	15			10			
tw	Pulse duration		LDCK high	25			20			ns
			UNCK low	15		***************************************	10			1
		•	UNCK high	25			20			1
	Catalan	Data before LC	OCK↑	10			10			
tsu	Setup time	RST (inactive)	before LDCK↑	5			5			ns
th	Hold time	Data after LDC	CK†	5			5			ns
TA	Operating free-air temperature			-55		125	0		70	°C



SN54ALS229A, SN74ALS229A 16 × 5 ASYNCHRONOUS FIRST IN FIRST OUT MEMORIES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TECT OF	ONDITIONS	SN5	4ALS	229A	SN	74ALS	229A	
P.	AKAIVIETEK	1551 (1	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	$I_{\rm J}=-18~{\rm mA}$			-1.2			-1.2	V
	Status flags	$V_{CC} = 4.5 \text{ V to 5}$	$.5 \text{ V, I}_{OH} = -0.4 \text{ mA}$	Vcc-	2		Vcc-	- 2		
V _{OH}	Q outputs	$V_{CC} = 4.5 V$,	I _{OH} = -1 mA	2.4	3.3] _v
VOH	Q outputs	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		1 °
	Q outputs	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	Q outputs	$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5] _v
VOL	Status flags	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	1 °
1	Status Hags	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	V _O = 0.4 V			-20			- 20	μΑ
l _l		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ЧH		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
ΊL		$V_{CC} = 5.5 V$,	$V_{ } = 0.4 V$			-0.2			-0.2	mA
lo‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	- 30		-112	mA
Icc		$V_{CC} = 5.5 V$			95	150		95	140	mA

switching characteristics (see Note 1)

			-	C = 5			$V_{CC} = 4.5$	V to 5.5	٧,	
			CL	= 50 p	ρF,		$C_L = 50 pF$			
	FROM	то	$R1 = 500 \Omega,$							
PARAMETER	(INPUT)	(OUTPUT)	R2	= 500	Ω,			UNIT		
	(1141 01)	(001101)	TA	= 25°	С					
	:		. 1	LS229	A	SN54	ALS229A	SN74	ALS229A	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
·	LDCK					25		30		MHz
fmax	UNCK					25		30		IVITIZ
^t pd	LDCK↑	Any Q		24	47	7	54	7	50	ns
t _{pd}	UNCK↑	Any Q		19	29	9	35	9	33	ns
^t PLH	LDCK↑	EMPTY		18	26	9	32	9	30	ns
^t PHL	UNCK↑	EMPTY		18	25	9	32	9	29	ns
t _{PHL}	RST↓	EMPTY		15	21	6	26	6	24	ns
t _{pd}	LDCK↑	EMPTY + 2		23	33	10	40	10	38	ns
t _{pd}	UNCK↑	EMPTY + 2		20	29	9	38	9	35	ns
^t PLH	RST↓	EMPTY + 2		20	28	9	35	9	33	ns
t _{pd}	LDCK↑	FULL – 2		23	33	10	40	10	38	ns
t _{pd}	UNCK↑	FULL – 2		20	29	9	38	9	35	ns
tPLH	RST↓	FULL – 2		20	28	9	35	9	33	ns
^t PHL	LDCK↑	FULL		21	28	10	35	10	33	ns
^t PLH	UNCK↑	FULL		17	23	8	29	8	27	ns
^t PLH	RST↓	FULL		18	27	8	33	8	31	ns
t _{en}	OE↑	Q		8	13	1	16	2	15	ns
t _{dis}	OE↑	Q		8	14	. 2	20	2	17	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS230, SN54ALS231, SN54AS230, SN54AS231 SN74ALS230, SN74ALS231, SN74AS230, SN74AS231 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 'ALS230 and 'AS230 have True and Complementary Outputs
- 'ALS231 and 'AS231 have Complementary G and G Inputs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High Capacitive Drive Capability
- Current Sinking Capability Up to 64 mA
- Dependable Texas Instruments Quality and Reliability

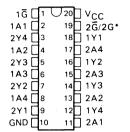
description

These octal buffers and line drivers are designed specifically to improve the performance of threestate memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G (active-low output control) inputs, and complementary G and \overline{G} inputs.

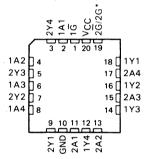
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum IOI is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)

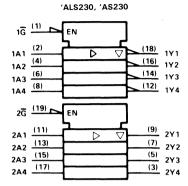


SN54ALS', SN54AS', ... FK PACKAGE (TOP VIEW)



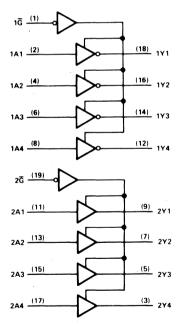
*2G for 'AS230 or 2G for 'ALS231, 'AS231

logic symbols†

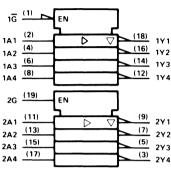


logic diagrams (positive logic)

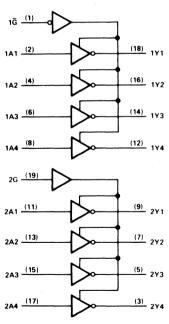
'ALS230, 'AS230



'ALS231, 'AS231



'ALS231, 'AS231



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

SN54ALS230, SN74ALS230 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operat	ting free-air temperature range (unless othe	rwise noted)
Supply voltage, VCC		7 V
Input voltage		7 V
Voltage applied to a disabled 3-state	output	5.5 V

recommended operating conditions

		SN	154ALS2	230	SN	74ALS2	230	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	OWIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 12			- 15	mA
lai	Low-level output current			12			24	mA
IOL	Low-level output current						48 [†]	IIIA
TA	Operating free-air temperature	- 55		125	0		70	°C

[†]The 48 mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA	NACTED	TEST CO	NDITIONS	SN	54ALS2	30	SN	74ALS2	230	UNIT
PARA	AMETER	1651 60	NUTTONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNII
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
VoH		$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
VOH		$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2						•
		$V_{CC} = 4.5 V$,	I _{OH} = -15 mA				2			
		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5	V
1		V _{CC} = 4.75 V, I _{OL}	= 48 mA (-1 versions)					0.35	0.5	
lozh		$V_{CC} = 5.5 V,$	V _O = 2.7 V			20			20	μΑ
IOZL		$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μΑ
l ₁		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ЧН		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	- μΑ
ΊL		$V_{CC} = 5.5 V$,	V _I = 0.4 V			- 0.1			-0.1	mA
IO [§]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		-112	mA
			Outputs high		7			7		
lcc l	'ALS230	$V_{CC} = 5.5 V$,	Outputs low		15			15		mA
			Outputs disabled		12			12		

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

'ALS230 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _L R1 R2 T _A	= 50 p = 500 = 500 = 25° LS230	F, Ω, Ω, C	C _L R1 R2 T _A	$C = 4.5^{\circ}$ = 50 pF, = 500 Ω , = 500 Ω , = MIN to	,	UNIT
^t PLH	А	Υ		5					ns
^t PHL				5					
^t PZH	G	V		9					 ns
tPZL				10					113
t _{PHZ}	G	V	5					ns	
tPLZ		1		6					HIS

SN54ALS231, SN74ALS231 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operat	ting free-air temperature range (unless oth	erwise noted)
Supply voltage, VCC		7 V
Input voltage		7 V
Voltage applied to a disabled 3-state	output	5.5 V
Operating free-air temperature range:	: SN54ALS231	55°C to 125°C
-	SN74ALS231	0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SN	SN54ALS231		SN	231	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	ONIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.7			0.8	V
ПОН	High-level output current			- 12			- 15	mA
1	Low level autout aument			12			24	mA
IOL	Low-level output current						48 [†]	IIIA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}$ The 48 mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETER	TEST CO	NDITIONS	SN	54ALS	231	SN	74ALS2	231	UNIT
PARA	AIVIETER	1251 00	MUITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
VoH		$V_{CC} = 4.5 V$,	I _{OH} = -3 mA	2.4	3.2		2.4	3.2		v
VOH		$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2						•
		$V_{CC} = 4.5 V$,	I _{OH} = -15 mA			•	2			
		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	V
		$V_{CC} = 4.75 \text{ V, } I_{OL}$	= 48 mA (-1 versions)					0.35	0.5	
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
IOZL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
lj		$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA
ήн		$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
IIL		$V_{CC} = 5.5 V$,	V _I = 0.4 V			- 0.1			-0.1	mA
IO [§]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	- 30		- 112	mA
			Outputs high		7	11		7	11	
ICC	'ALS231	$V_{CC} = 5.5 V$,	Outputs low		15	22		15	22	mA
			Outputs disabled		12	19		12	19	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

⁵The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS231, SN74ALS231 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

'ALS231 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS231	C _L R1 R2 T _A	C = 4.5 V tc = 50 pF, = 500 Ω, = 500 Ω, = MIN to M ALS231 MAX 12 11 17 21 12 18 18 22 12	MAX	MAX SN74ALS231 MIN MAX		
		•	TYP	MIN				1	
tpLH	^	Υ	5	2	12	2	9		
tPHL	A	. '	5	2	11	2	9	ns	
^t PZH	1 G	Y	9	4	17	4	14	ns	
tPZL	. 10		10	5	21	5	18		
tPHZ	1 G	Υ	5	2	12	2	10		
tPLZ	10	'	6	3	18	.3	12	ns	
^t PZH	2G	Υ	11	5	18	5	16	20	
tPZL	20	Y	12	5	22	5	19	ns .	
[†] PHZ	2G	Υ	6	2	12	2	10		
[†] PLZ	20	1	7	3	19	3	13	ns	

SN54AS230, SN54AS231, SN74AS230, SN74AS231 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, V _{CC}
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54AS230, SN54AS231 55°C to 125°C
SN74AS230, SN74AS231 0 °C to 70 °C

recommended operating conditions

			N54AS2 N54AS2		SN74AS230 SN74AS231			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			-12			- 15	mA
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		AMETER TEST CONDITIONS		1	N54AS2 N54AS2		SN74AS230 SN74AS231			UNIT
	PANAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V, I _{OH} = -2 mA	Vcc-	2		Vcc-	2		
۷он		$V_{CC} = 4.5 V,$	I _{OH} = -3 mA	2.4	3.4		2.4	3.4		v
VOH		$V_{CC} = 4.5 V,$	I _{OH} = -12 mA	2.4] '
	1	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2.4			1
		V _{CC} = 4.5 V,	I _{OL} = 48 mA	1	0.27	0.55				V
VOL		V _{CC} = 4.5 V	I _{OL} = 64 mA					0.31	0.55	1 °
lozh		V _{CC} = 5.5 V,	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL		V _{CC} = 5.5 V,	$V_0 = 0.4 \text{ V}$			- 50			- 50	μΑ
IJ		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΙΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
1	'AS230 2A	V _{CC} = 5.5 V,	V _I = 0.4 V			1			-1	mA
ΙΙL	All others	vCC = 5.5 v,	V ₁ = 0.4 V			-0.5			-0.5	l IIIA
10 [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	-50		- 150	- 50		- 150	mA
			Outputs high		16	25		16	25	
	'AS230	$V_{CC} = 5.5 V$	Outputs low		55	87		55	87	mA
1			Outputs disabled		29	46		29	46]
lcc :			Outputs high		12	18		12	18	
	'AS231	$V_{CC} = 5.5 V$	Outputs low		52	82		52	82	mA
			Outputs disabled	1	25	39		25	39	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS230, SN54AS231, SN74AS230, SN74AS231 OCTAL BUFFERS AND LINE DRIVERS WITH 3 STATE OUTPUTS

'AS230 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	·	V _{CC} = 4 C _L = 50 R1 = 500 R2 = 500 T _A = MII	Ω, Ο Ω,	, ν,	UNIT	
				AS230		AS230		
			MIN	MAX	MIN	MAX		
^t PLH	1A	1Ÿ	2.5	7	2.5	6.5	ns	
tPHL	16	''	2	6	2	5.7		
tPLH	24	2Y	2.5	9	2.5	6.2	ns	
tPHL	2A	21	2	7	2	6.2		
tPZH			2	7	2	6.4		
tPZL	1 G	1Y	2	9	2	8.5		
tPHZ	10	1 1	2	5.5	2	5	ns	
^t PLZ			2	12.5	2	9.5		
^t PZH			2	10	2	9		
tPZL	2 G	2Y	2	8	2	7.5		
tPHZ	20	21	2	6.5	2	6	ns	
tPLZ			2	10.5	2	9		

'AS231 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		$V_{CC} = 4.5 \text{ V to } 5$ $C_L = 50 \text{ pF,}$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS231$		٧,	UNIT	
,			SN5	4AS231	SN7	4AS231		
			MIN	MAX	MIN	MAX		
t _{PLH}	Α	Υ	2	7	2	6.5		
tPHL	Α	· '	2	6	2	5.7	ns	
tPZH			2	7	2	6.4		
tPZL	G	Y	2	9	2	8.5	ns	
tPHZ	G	'	2	5.5	2	5		
^t PLZ			. 2	12.5	2	9.5	1	
tPZH			3	7	3	6		
tPZL	G	Y	3	10	3	9	1	
^t PHZ	G	, , , , , , , , , , , , , , , , , , ,	3	6.5	3	6	ns	
tPLZ			3	13.5	3	7	1	

SN54ALS232A, SN74ALS232A 16 × ASYNCHRONOUS FIRST IN FIRST OUT MEMORIES

D2876, OCTOBER 1985 - REVISED MAY 1986

- Independent Asynchronous Inputs and Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 16 Words by 4 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

description

These 64-bit memories use Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 4 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

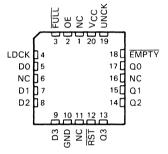
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

SN54ALS232A . . . J PACKAGE SN74ALS232A . . . D OR N PACKAGE (TOP VIEW)

> OE TI VIG VCC FULL 2 15 UNCK LDCK ∏3 14 EMPTY DO 14 00 ٦ 13 D1 [5 ٦ و ١ 12 D2 🛮 6 11 D Q2 D3 Π_7 10 D Q3 RST GND ∏8 a

SN54ALS232A . . . FK PACKAGE SN74ALS232A . . . FN PACKAGE

(TOP VIEW)



NC-No internal connection.

Status of the FIFO memory is monitored by the FULL and EMPTY output flags. The FULL output will be low when the memory is full, and high when the memory is not full. The EMPTY output will be low when the memory is empty, and high when it is not empty.

A low level on the reset input (\overline{RST}) resets the internal stack control pointers and also sets \overline{EMPTY} low and sets \overline{FULL} high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a \overline{RST} pulse or from an empty condition, will cause \overline{EMPTY} to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the \overline{FULL} or \overline{EMPTY} output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

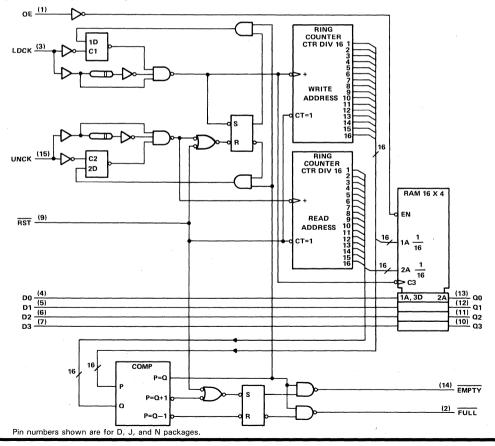
logic symbol† FIFO 16X4 CTR (9) (3) (2) FULL LDCK -> ī(+/C2) (CT = 16)G1UNCK (15) (14) EMPTY > 3-(CT = 0)G3OE __(1) EN4 (<u>13)</u> Q0 (4) 2D 4 V (5) (12) Q1 (<u>11)</u> Q2 (6) D2

(7) D3

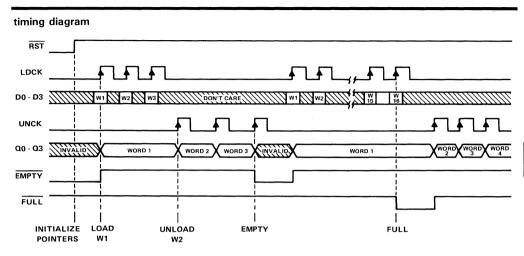
†This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

(10)_ Q3

logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Subbly voltage, ACC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS232A55°C to 125°C
SN74ALS232A 0°C to 70°C
Storage temperature range65 °C to 150 °C

recommended operating conditions

			SN	54ALS2	232A	SN	74ALS2	232A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	٧
	High-level output current	Q outputs			- 1			-1.6	
ЮН	n mgm 16461 Gatput Current	FULL, EMPTY			-0.4			-0.4	mA
IOL Low-level output current	Q outputs			12			24	mA	
	FULL, EMPTY			4			8	l mA	
	Clock frequency	LDCK	0		25	0		30	MHz
†clock		UNCK	0		25	0		30	
		RST low	20			15			
		LDCK low	15			10			
tw	Pulse duration	LDCK high	25			20			ns
		UNCK low	15			10			
		UNCK high	25			20			
	Setup time	Data before LDCK↑	10			10			
t _{su}		RST (inactive) before LDCK↑	5			5			ns
th	Hold time	Data after LDCK↑	5			5			ns
TA	Operating free-air temperature		- 55		125	0		70	°C



SN54ALS232A, SN74ALS232A 16 × 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	INDITIONS	SN	54ALS2	32A	SN	UNIT		
	ranalvie i en	1251 00	NUTTIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			- 1.2			-1.2	V
	FULL, EMPTY	$V_{CC} = 4.5 \text{ V to 5}.$	5 V, I _{OH} = -0.4 mA	Vcc-2	2		V _{CC} -	2	,	
Voн	0	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3] v
	Q outputs	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -2.6 mA				2.4	3.2]
	Q outputs	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
	Q outputs	$V_{CC} = 4.5 \text{ V},$	1 _{OL} = 24 mA					0.35	0.5]
VOL	FULL, EMPTY	$V_{CC} = 4.5 \text{ V},$	I _{OH} = 4 mA		0.25	0.4		0.25	0.4	7 °
	FULL, EIVIFT	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5]
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 20			- 20	μΑ
l _l		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lн		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ.
I _I L		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2			-0.2	mA
10 [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Icc		V _{CC} = 5.5 V			75	125		75	125	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$					UNIT		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	LDCK			40		25		30		MHz
IIIdx	UNCK			40		25		30		
^t pd	LDCK↑	Any Q	ĺ	30	40	4	50	4	46	ns
^t pd	UNCK†	Any Q		20	27	7	35	7	31	ns
tPLH	LDCK↑	EMPTY		17	23	8	29	8	26	ns
^t PHL	UNCK↑	EMPTY		19	24	10	36	10	29	ns
^t PHL	RST↓	EMPTY		13	18	5	23	5	20	ns
^t PHL	LDCK↑	FULL		21	26	10	35	10	31	ns
t _{PLH}	UNCKT	FULL		17	23	8	28	8	25	ns
^t PLH	RST↓	FULL "		18	24	8	31	8	28	ns
t _{en}	OE↑	Q		7	12	1	16	1	14	ns
^t dis	OE↓	Q		10	16	2	23	2	21	ns



 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS233A, SN74ALS233A \times 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

D2876, JANUARY 1986 - REVISED MAY 1986

- Independent Asynchronous Inputs and Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 16 Words by 5 Bits Each
- Data Rates from 0 to 30 MHz
- Fall-Through Time . . . 24 ns Typ
- 3-State Outputs

description

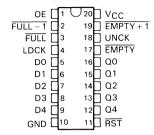
These 80-bit memories utilize Advanced Low-Power Schottky technology and feature high speed and fast fall-through times. They are organized as 16 words by 5 bits each.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

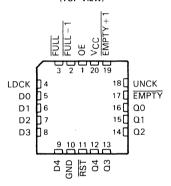
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals will have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the \overline{FULL} , \overline{EMPTY} , $\overline{FULL}-1$, and $\overline{EMPTY}+1$ output flags. The FULL output will be low whenever the memory is full, and high whenever not full. The $\overline{FULL}-1$ output will be low whenever the memory contains 15 data words. The \overline{EMPTY} output will be low whenever the memory is empty, and high whenever it is not empty. The $\overline{EMPTY}+1$ output will be low whenever one word remains in memory.

SN54ALS233A J PACKAGE SN74ALS233A DW OR N PACKAGE (TOP VIEW)



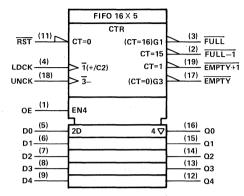
SN54ALS233A . . . FK PACKAGE SN74ALS233A . . . FN PACKAGE (TOP VIEW)



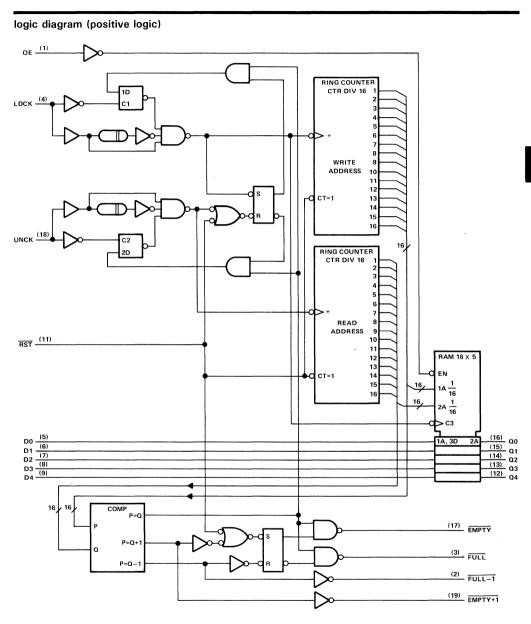
A low level on the reset input (\overline{RST}) resets the internal stack control pointers and also sets \overline{EMPTY} low and sets \overline{FULL} , $\overline{FULL}-1$, and $\overline{EMPTY}+1$ high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a \overline{RST} pulse or from an empty condition, will cause \overline{EMPTY} to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.



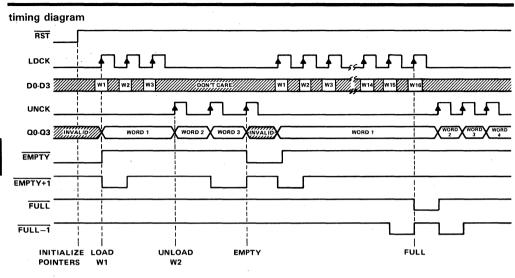
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.



Pin numbers are for D, J, and N packages.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS23	3A 55°C to 125°C
SN74ALS23	BA
Storage temperature range	-65°C to 150°C

$\begin{array}{c} \text{SN54ALS233A, SN74ALS233A} \\ \text{16} \times \text{5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES} \end{array}$

recommended operating conditions

			SN	54ALS2	33A	SN	74ALS2	33A	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
lovi	High-level output current	Q outputs			- 1			-1.6	mA
Іон	riigii-ievei oatpat caireit	Status flags			-0.4			-0.4	mA
1	Low-level output current	Q outputs			12			24	mA
lOL	Low-level output current	Status flags			4			8	1 mA
f	Clask fraguency	LDCK	0		25	0		30	MHz
¹clock	Clock frequency	UNCK	0		25	0		30	IVITIZ
		RST low	20			15			
		LDCK low	15			10			
t _w	Pulse duration	LDCK high	25			20			ns
		UNCK low	15			10			
		UNCK high	25			20			
	C-turn time-	Data before LDCK↑	10			10			
t _{su}	Setup time	RST inactive before LDCK↑	5			5			ns
th	Hold time	Data after LDCK↑	. 5			5			ns
TA	Operating free-air temperature	•	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CO	MIDITIONE	SN	54ALS2	233A	SN	UNIT		
「	ANAIVIETEN	lesi co	TEST CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			-1.2	٧
	Status flags	$V_{CC} = 4.5 \text{ V to 5.5}$	$5 \text{ V}, \text{ I}_{OH} = -0.4 \text{ mA}$	Vcc-	2		V _{CC} -	- 2		
∨он	Q outputs	V _{CC} = 4.5 V,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	Q outputs	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	Q outputs	$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL	Q outputs	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	v
\ VOL	Status flags	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	·
	Status Hays	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20		•	- 20	μΑ
Ч		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ		V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ΊL		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
lo [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	- 30		-112	mA
Icc		V _{CC} = 5.5 V			88	143		88	133	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS233A, SN74ALS233A 16×5 Asynchronous first in first-out memories

switching characteristics (see Note 1)

İ	1		1 -	C = p			$V_{CC} = 4.5$		٧,	
			1 -	= 50			C _L = 50 pl			
PARAMETER	FROM	то		= 500			R1 = 500			UNIT
	(INPUT)	(OUTPUT)	1	= 500			R2 = 500			
			TA	= 25	°C		$T_A = -MI$	N to MAX	(1
			'Δ	LS233.	A	SN54	ALS233A	SN74	ALS233A	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	LDCK			40		25		30		MHz
'max	UNCK			40		25		30		IVIIIZ
^t pd	LDCK↑	Any Q		24	44	7	52	7	. 48	ns
^t pd	UNCK↑	Any Q		19	29	9	35	9	33	ns
^t PLH	LDCK↑	EMPTY		18	25	9	30	9	28	ns
^t PHL	UNCK↑	EMPTY		18	25	9	33	10	30	ns
^t PHL	RST↓	EMPTY		13	19	6	24	6	22	ns
t _{pd}	LDCK↑	EMPTY + 1		22	31	10	40	10	37	ns
^t pd	UNCKT	EMPTY + 1		22	31	9	40	10	37	ns
^t PLH	RST↓	EMPTY + 1		19	27	8	32	8	31	ns
^t pd	LDCK↑	FULL – 1		23	32	11	38	12	36	ns
t _{pd}	UNCK↑	FULL – 1		23	32	11	39	12	36	ns
^t PLH	RST↓	FULL – 1		20	28	10	. 34	11	32	ns
^t PHL	LDCK↑	FULL		21	28	10	35	12	33	ns
^t PLH	UNCK↑	FULL		· 17	24	8	29	9	27	ns
^t PLH	RST↓	FULL		18	27	8	32	9	30	ns
t _{en}	OE↑	a		8	13	1	16	2	15	ns
^t dis	OE↑	Q		8	12	2	20	2	17	ns

SN54ALS240A, SN54ALS241A, SN54AS240, SN54AS241 SN74ALS240A, SN74ALS241A, SN74AS240, SN74AS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

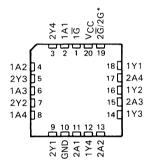
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW or N PACKAGE (TOP VIEW)

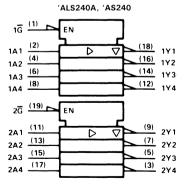
1Ğ[1	J 20]vcc
1A1[]2	19] 2 <u>G</u> /2G*
2Y4 []3	18]1Y1
1A2[4	17]2A4
2Y3 [5	16] 1Y2
1A3[_ 6	15]2A3
2Y2[٦7	14] 1Y3
1A4 []8	13]2A2
2Y1 [9	12] 1Y4
GND [10	11]2A1

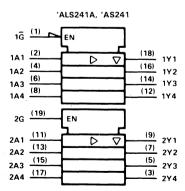
SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)



*2G for 'ALS240A, 'AS240 or 2G for 'ALS241A, 'AS241

logic symbols†



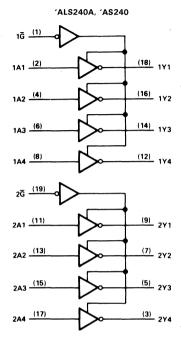


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers are for DW, J, and N packages.

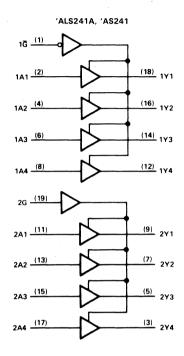


SN54ALS240A, SN54ALS241A, SN54AS240, SN54AS241 SN74ALS240A, SN74ALS241A, SN74AS240, SN74AS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic diagrams (positive logic)



Pin numbers are for DW, J, and N packages.



SN54ALS240A, SN54ALS241A, SN74ALS240A, SN74ALS241A OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS240A, SN54ALS241A 55 °C to 125 °C
SN74ALS240A, SN74ALS241A 0°C to 70°C
Storage temperature range

recommended operating conditions

			54ALS2 54ALS2			74ALS2		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 12			- 15	mA
la.	Low-level output current			12			24	
lor	Low-level output current						48 [†]	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^\}dagger$ The 48 mA limit applies only to the -1 versions and only if the V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CO	ONDITIONS	_	N54ALS N54ALS			N74ALS N74ALS		UNIT
				MIN	TYP [‡]	MAX	MIN	TYP‡	MAX	
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -	- 2		V _{CC} -	2		
V _{OH}		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2] ,
VOH		$V_{CC} = 4.5 \text{ V},$	I _{OH} = . – 12 mA	2						1 '
		$V_{CC} = 4.5 V$	I _{OH} = -15 mA				2]
		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	V
		$V_{CC} = 4.75 \text{ V},$	I _{OL} = 48 mA (-1 versions)					0.00	0.5	
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			-20	μΑ
- II		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μА
HL		$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.1			-0.1	mA
lo§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		-112	mA .
			Outputs high		4	11		4	11	
l	'ALS240A		Outputs low		13	23		13	23	
Icc		Vcc = 5.5 V	Outputs disabled		14	25		14	25	mA
1.00		1 *((= 3.3 *	Outputs high		9	17		9	15] '''
	'ALS241A		Outputs low		15	28		15	26]
			Outputs disabled		17	32		17	30	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25 °C.



[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS240A, SN54ALS241A, SN74ALS240A, SN74ALS241A OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

'ALS240A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$ 'ALS240A	SN54A MIN	$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500 \text{ S}$ $R2 = 500 \text{ S}$ $T_A = MIN$ MAX	-, Ω, Ω, to MAX	V, ALS240A MAX	UNIT
tPLH	Α	Υ	6	2	22	2	9	ns
^t PHL	^	l ' l	5	2	11	2	9	113
tPZH	G	Y	9	4	34	5	13	
t _{PZL}		1 ' 1	10	5	26	5	18	ns
t _{PHZ}	G	v	6.	1	15	2	10	ne
[†] PLZ	0		7	3	24	3	12	ns

'ALS241A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_{L} = 50 \text{ p}$ $R1 = 500$ $T_{A} = MIN$	F. Ω,	/,	UNIT
			SN54A	LS241A	SN74A	LS241A	
			MIN	MAX	MIN	MAX	
tPLH	A	Y	3	31	3	11	ns
^t PHL	1 ^	1	1	14	3	. 10	1115
^t PZH	1 G	Y	5	33	7	21	ns
^t PZL] ''	1	7	27	7	21	115
^t PHZ	1 G	· ·	2	13	2	10	ns
^t PLZ] '9		2	32	3	15	""
^t PZH	2G	Y	7	38	7	21	ns
^t PZL	26	1	7	. 30	7	21	115
tPHZ	2G		2	17	2	10	ns
^t PLZ]2G	. '	3	35	3	15	115

SN54AS240, SN54AS241, SN74AS240, SN74AS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

 Input voltage
 7 V

 Voltage applied to a disabled 3-state output
 5.5 V

Storage temperature range -65 °C to 150 °C

recommended operating conditions

		SN54AS240 SN54AS241			SN74AS240 SN74AS241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX]
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIΗ	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			- 12			- 15	mA
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

. 1	PARAMETER	TEST COM	NDITIONS		154AS2 154AS2		l	74AS24 74AS24		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V , $I_{OH} = -2 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
VoH		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V , $I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V
VOH		$V_{CC} = 4.5 V,$	Q.,,	2.4]
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$				2.4			
VOL		$V_{CC} = 4.5 V$			0.27	0.55				V
VOL		$V_{CC} = 4.75 \text{ V},$	I _{OL} = 64 mA					0.31	0.55	1 °
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
IOZL		$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 50			- 50	μΑ
Ц	•	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
ΊL	'AS241A inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			- 1			- 1	mA
	All others	ν _{CC} = 3.5 ν,	V = 0.4 V			-0.5			-0.5	111/4
lo‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 150	- 50		-150	mA
			Outputs high		11	17		11	17	
	'AS240		Outputs low		51	75		51	75	
lcc		V _{CC} = 5.5 V	Outputs disabled		24	38		24	38	mA
100		VCC = 5.5 V	Outputs high		22	35		22	35] '''^
	'AS241	l —	Outputs low		61	90		61	90]
			Outputs disabled		35	56	,	35	56]

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_{\Delta} = 25 ^{\circ}\text{C}$.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS240, SN54AS241, SN74AS240, SN74AS241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

'AS240 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R1 = 500 \text{ s}$ $R2 = 500 \text{ s}$ $T_A = MIN$	=, Ω, Ω,	v, '	UNIT
			SN54	4 S240	SN74	}	
			MIN	MAX	MIN	MAX	
tPLH	Α	V	2	, 7	2	6.5	ns
^t PHL		<u>'</u>	2	6	2	5.7	113
t _{PZH}	1 G	v	2	7	2	6.4	ns
tPZL ·	10	'	2	9.5	2	9	1 113
^t PHZ	G	Y	2	5.5	2	5	ns
tPLZ		' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	2	12.5	2	9.5	1

'AS241 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} V_{CC} = 4.5 \ V \ to \ 5.5 \ V, \\ C_{L} = 50 \ pF, \\ R1 = 500 \ \Omega, \\ R2 = 500 \ \Omega, \\ T_{A} = MIN \ to \ MAX \\ \hline \frac{NN54AS241}{MIN} \qquad \frac{NN74AS241}{MAX} \\ \hline \frac{MIN}{2} \qquad \qquad 9 \qquad 2 \qquad 6.2 \\ \hline \begin{array}{c} 6.2 \\ 6.2 \\ \hline \end{array}$		F, Ω, Ω, to MAX SN74AS241		UNIT	
tPLH	A	Y		9	2	6.2		
tPHL	1		2	7	2	6.2	ns	
^t PZH	1 <u>G</u>	Υ,	2	10	2	9	ns	
^t PZL	1 19	٠, .	2	8	2	7.5	113	
^t PHZ	1G	Υ	2	6.5	2	6	ns	
tPLZ	1 '9	'	2	10.5	2	9	,3	
^t PZH	2G	Υ	2	11	3	10.5	ns	
^t PZL	20	'	3	9.5	3	8.5	,,,3	
^t PHZ	2G	Υ	3	7	3	7	ns	
tPLZ	23	'	3	12	3	12	3	



SN54ALS242B, SN54ALS243A, SN54AS242, SN54AS243 SN74ALS242B, SN74ALS243A, SN74AS242, SN74AS243 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- 2-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

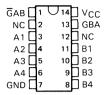
These quadruple bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{G}AB$). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the quadruple bus transceivers the capability to store data by simultaneous enabling of GBA and $\overline{G}AB$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will retain their states. The 4-bit codes appearing on the two sets of buses will be complimentary for the 'ALS242 and 'AS242 or identical for the 'ALS243 and 'AS243.

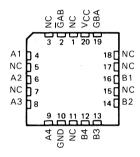
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum IQL is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74' family is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54' . . . J PACKAGE SN74' . . . D OR N PACKAGE (TOP VIEW)



SN54' . . . FK PACKAGE (TOP VIEW)



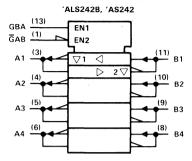
NC-No internal connection

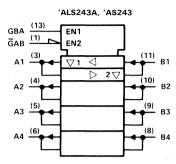
FUNCTION TABLE

INP	UTS	'ALS242B	'ALS243A
GAB	GBA	'AS242	'AS243
L	L	Ā to B	A to B
Н	Н	B̄ to A	B to A
Н	L	Isolation	Isolation
1	ы	Latch A and B	Latch A and B
_	•••	$(A = \overline{B})$	(A = B)

SN54ALS242B, SN54ALS243A SN74ALS242B, SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

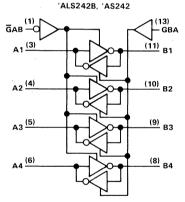
logic symbols†

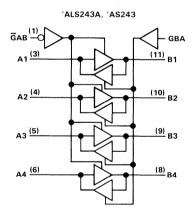




[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagrams (positive logic)





Pin numbers are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage: All inputs	
I/O ports	
Operating free-air temperature range: SN54ALS242B, SN54ALS243A 55 °C to 125 °C	
SN74ALS242B, SN74ALS243A0°C to 70°C	
Storage temperature range	



SN54ALS242B, SN54ALS243A SN74ALS242B. SN74ALS243A QUADRUPLE BUS TRANSCEIVERS WITH 3 STATE OUTPUTS

recommended operating conditions

		1	SN54ALS242B SN54ALS243A			SN74ALS242B SN74ALS243A		
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-12			– 15	mA
loi	Low-level output current			12			24	mA
IOL	Low-level output current						48 [†]	11114
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^\}dagger$ The 48-mA limit applies only to the -1 versions, and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		ARAMETER TEST CONDITIONS		i	54ALS2 54ALS2		l	4ALS24 4ALS24		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			~ 1.2			-1.2	٧
		$V_{CC} = 4.5 \text{ V to } 5.5$	V, I _{OH} = -0.4 mA	V _{CC} -	2		V _{CC} -	2		
VOF		$V_{CC} = 4.5 V$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
VOF	1	$V_{CC} = 4.5 V$,	I _{OH} = -12 mA	2						\ \ \
		$V_{CC} = 4.5 V$,	I _{OH} = -15 mA				2			
		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	-	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	V
		$V_{CC} = 4.75 V$,	I _{OL} = 48 mA (-1 versions)					0.35	0.5	
11	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
'1	A or B ports	$V_{CC} = 5.5 V$,	$V_1 = 5.5 V$			0.1			0.1	'''A
۱н	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μА
ΉΗ	A or B ports‡	VCC = 5.5 V,	V - 2.7 V			20			20	μ.
	Control inputs	V 55.V				-0.1			-0.1	
IL	A or B ports‡	$V_{CC} = 5.5 V,$	VI = 0.4 V			-0.1			-0.1	mA
lo§		V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-	-112	- 30		-112	mA
			Outputs high		10	20		10	16	
	'ALS242B		Outputs low		14	26		14	- 21	
lac		V _{CC} = 5.5 V	Outputs disabled		12	24		12	19	
ICC		ACC = 2.2 A	Oututs high		15	30		15	. 25	mA
	'ALS243A		Outputs low		20	35		20	30	
			Outputs disabled		- 21	37		21	32	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

⁵ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

'ALS242B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$ 'ALS242B	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to LS242B	MAX	LS242B	UNIT
,			TYP	MIN	MAX	MIN	MAX	l
t _{PLH}	A or B	B or A	5	2	15	2	11	ns
t _{PHL}	7 ~ 01 6	BUIA	5	2	14	2	10] '''
[†] PZH	GAB	В	10	4	22	4	18	ns
^t PZL	7 5/20 1	В	11	7	25	7	21	113
tPHZ	GAB	В	6	2	16	2	14	ns
t _{PLZ}	T GAB	Ь	5	2	18	2	12	115
^t PZH	GBA	A	10	4	22	4	18	ns
tPZL	7 664	A	11	7	25	7	21	115
^t PHZ	GBA	Λ	6	2	16	2	14	ns
^t PLZ		A .	5	2	18	2	12	113

'ALS243A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$C_L = 50$ $R1 = 500$ $R2 = 500$	Ο Ω,	V,	UNIT
			SN54.	ALS243A	SN74A	LS243A	1
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	B or A	4	15	4	11	ns
^t PHL	A OF B	B 01 A	4	15	4	11	lis
^t PZH	БАВ	В	7	25	7	20	ns
tPZL	GAB	P .	. 7	25	7	20	7 '''
t _{PHZ}	GAB	В	2	16	2	14	ns
^t PLZ	JAB JAB		3	27	3	22	1115
^t PZH	GBA	А	7	25	7	20	ns
^t PZL] GDA		7	25	7	20	115
^t PHZ	GBA	А	2	16	2	14	ns
^t PLZ	J GDA		3	27	3	22] '''

SN54AS242, SN54AS243 SN74AS242, SN74AS243 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum	ratings over operating	ig tree-air to	emperature r	ange (uniess otr	nerwise notea)
Supply voltage,	Vcc				7 V
Input voltage:	All inputs				7 V
	I/O ports				5.5 V
Operating free-a	ir temperature range:	SN54AS242	, SN54AS243		55°C to 125°C
		SN74AS242	, SN74AS243		0°C to 70°C
Storage tempera	ature range				65°C to 150°C

recommended operating conditions

		i i	SN54AS242 SN54AS243			SN74AS242 SN74AS243		
	· ·	MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
ViH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 12			- 15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETED	TEGT CONDU	riono	1	N54AS2 N54AS2			174AS2		LINUT
P	ARAMETER	TEST CONDI	IIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_1 = -18 \text{ mA}$			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	1 _{OH} = -2 mA	Vcc-	2		V _{CC} -	2		
Vон		$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4]
VOH		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2.4] `
		$V_{CC} = 4.5 V$,	$I_{OH} = -15 \text{ mA}$				2.4			
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 48 \text{ mA}$			0.55	1]
*OL		V _{CC} = 4.5 V,	$I_{OL} = 64 \text{ mA}$						0.55	<u>l</u>
I _I	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
"	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1] '''
ΉΗ	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μА
чн	A or B ports‡	ν _{CC} = 5.5 ν ,	V - 2.7 V			70			70	μΑ
	Control inputs					-0.5			-0.5	
	'AS242					- 0.5			-0.5	1
IIL	A or B ports [‡]	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			0.5			0.5	mA
	'AS243				,	- 1			- 1	
	A or B ports [‡]					_ '			'	ļ
IO§		$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 50		- 150	- 50		- 150	mA
			Outputs high		18	28		18	28	
	'AS242		Outputs low		38	60		38	60]
loc		V _{CC} = 5.5 V	Outputs disabled		25	39		25	39	m _A
ICC	'AS243	VCC - 5.5 V	Outputs high		28	44		28	44] '''^
			Outputs low		47	74		47	74	
			Outputs disabled		35	56		35	56]

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \, ^{\circ}\text{C}$.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS242 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to } MAX$ $SN54AS242 = SN74AS242$				$\begin{array}{c} \text{C}_L = 50 \text{ pF,} \\ \text{TO} \\ \text{R1} = 500 \ \Omega, \\ \text{(OUTPUT)} \\ \text{R2} = 500 \ \Omega, \\ \text{T}_A = \text{MIN to MAX} \end{array}$		$\begin{array}{cccc} & & & & & & & \\ C_L & = 50 \text{ pF}, & & & \\ R1 & = 500 \Omega, & & & \\ (OUTPUT) & & & R2 & = 500 \Omega, \\ & & & T_A & = \text{MIN to MAX} \end{array}$			UNIT
			MIN SN54	MAX	MIN	MAX	-					
tPLH			2	7	2	6.5						
tPHL	A or B B or A	B or A	2	6	2	5.7	ns					
^t PZH	<u>G</u> AB	В	2	9	2	5.5						
tPZL	GAB	В	2	8.5	2	7.5	ns					
tPHZ	GAB	В	2	7	2	6.5	ne					
tPLZ	GAB	ь	2	12.5	2	9.5	ns ns					
tPZH	GBA	А	3	7	3	6	ne					
tPZL	GBA .	A	3	9	3	8	ns					
tPHZ	CDA	Α	3	8.5	3	. 6	ns					
tPLZ	GBA		3	13.5	3	10.5	1 ""					

'AS243 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОUТРИТ)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to } MAX$			UNIT	
		· ·	SN54	AS243	SN74A	S243	
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	B or A	3	9	3	7.5	
tpHL	A 01 B	or B	3	8	3	6.5	ns
^t PZH	GAB B	R	2	10	2	9	ns
^t PZL		2	9	2	7.5] '''	
^t PHZ	ĞАВ	В	2	7	2	6.5	ns
tpLZ	UAD		2	11	2	9] "
^t PZH	GBA	А	3	11.	3	10.5	ns
tPZL	GDA		3	9.5	3	8.5] '''
^t PHZ	GBA	А	3	7.5	3	7	ns
tPLZ	GDA .	i A	3	14	3	11	1 ns

SN54ALS244A, SN54AS244, SN74ALS244A, SN74AS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

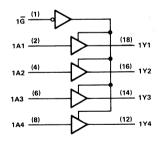
description

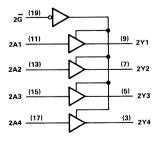
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240A, 'ALS241A, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{\underline{G}}$ (active-low output control) inputs, and complementary \underline{G} and $\overline{\underline{G}}$ inputs.

The -1 version of the SN74ALS244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS244A.

The SN54ALS244A and SN54AS244 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS244A and SN74AS244 are characterized for operation from 0 °C to 70 °C.

logic diagram (positive logic)





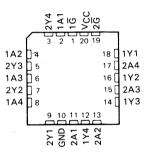
PRODUCTION DATA documents contain information

roubot from PATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

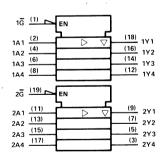
SN54ALS244A, SN54AS244 . . . J PACKAGE SN74ALS244A, SN74AS244 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS244A, SN54AS244 . . . FK PACKAGE (TOP VIEW)



logic symbol[†]



 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Pin numbers shown are for DW, J, and N packages.

SN54ALS244A, SN74ALS244A OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
Voltage applied to a disabled 3-state	output
Operating free-air temperature range	: SN54ALS244A
	SN74ALS244A
Storage temperature range	65°C to 150°C

recommended operating conditions

		SN54ALS244A			SN	UNIT		
	,	MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-12			- 15	mA
lOL	Low-level output current			12			24	mA
'OL	Low-level output current						48 [†]	IIIA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^\}dagger The$ extended limits apply only if VCC is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMP	TEST CONDITIONS		54ALS2	44A	SNZ	4ALS2	14A	
PARAMETER	IEST COND	ITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			-1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2		Vcc-	2.			
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -3 mA	2.4	3.2		2.4	3.2		l _v
VOH	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2						ľ
	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2			
	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 24 mA					0.05	0.5	V
	$I_{OL} = 48 \text{ mA for} - 1 \text{ ve}$	rsion)					0.35	0.5	
IOZH	$V_{CC} = 5.5 V,$	V _O = 2.7 V			20.			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 20			- 20	μΑ
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 \text{ V}$			20			20	μA
ήL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1			-0.1	mA
IO§	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
		Outputs high		9	15		9	15	
^I cc	$V_{CC} = 5.5 V$	Outputs low		15	- 24		15	24	mA
		Outputs disabled		17	27		17	27	

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}, T_{A} = 25 ^{\circ}\text{C}.$



The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS244A, SN74ALS244A OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to MAX}$			UNIT	
1			SN54ALS244A SN74ALS244A			ALS244A	1
			MIN	MAX	MIN	MAX	
tPLH	Α	Y	1	18	3	10	
tPHL	^	, , , , , , , , , , , , , , , , , , ,	3	13	3	10	ns
tPZH	G	Y	1	29	7	20	ns
tPZL	9	1	1	27	7	20	115
tPHZ	G	Y	2	12	2	10	ns
tPLZ	, , , , , , , , , , , , , , , , , , ,	•	1	21	3	13	113



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	`
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54A	S244
SN74A	.S244 0 °C to 70 °C
Storage temperature range	- 65 °C to 150 °C

recommended operating conditions

		SN54AS244			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
Іон	High-level output current			-12			- 15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAN	IETED	TEGT OF	MDITIONE	S	N54AS2	244	S	N74AS	244	UNIT
PARAMETER		IESI CC	TEST CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNI
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
		V _{CC} = 4.5 V to 5.5	4.5 V to 5.5 V, I _{OH} = -2 mA		2		v _{cc} -	2		
V		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -3 mA	2.4	3.4		2.4	3.4] ,
Vон		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2.4						7 °
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2.4			1
.,		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA	T		0.55				I v
v_{OL}		$V_{CC} = 4.5 \text{ V}$	I _{OL} = 64 mA						0.55	7 °
lozh		$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μA
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50			- 50	μA
lj.		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μA
1	G					-0.5			-0.5	Ι.
ΙL	Α	$V_{CC} = 5.5 \text{ V},$	$V_I = 0.4 V$			- 1			-1	mA
IO‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-50		- 150	- 50		- 150	mA
			Outputs high		22	34		22	34	
Icc -		V _{CC} = 5.5 V	Outputs low		60	90		60	90	mA
			Outputs disabled	1	34	54		34	54	7

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{o}C.$



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS244, SN74AS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$\begin{array}{c} \text{V}_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, \\ \text{C}_L = 50 \text{ pF}, \\ \text{R1} = 500 \Omega, \\ \text{R2} = 500 \Omega, \\ \text{T}_{A} = \text{MIN to MAX} \end{array}$			UNIT
,		1	SN54	AS244	SN74/].	
			MIN	MAX	MIN	MAX	1
^t PLH	Α	V	2	9	2	6.2	ns
^t PHL	A	1	2	7	2	6.2] "
^t PZH	G		2	10	2	9	ns
^t PZL	ď	'	2	8	2	7.5] ''5
t _{PHZ}	G		2	6.5	2	6	ns
^t PLZ	3	'	2	10.5	2	9	115

SN54ALS245A, SN54AS245, SN74ALS245A, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

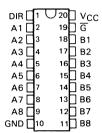
These octal bus transceivers are designed for asynchronous twoway communication between data buses The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\vec{G}) can be used to disable the device so that the buses are effectively isolated.

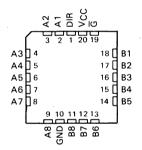
The –1 version of the SN74ALS245A is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no –1 version of the SN54ALS245A.

The SN54ALS245A and SN54AS245 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS245A and SN74AS245 are characterized for operation from 0 °C to 70 °C.

SN54ALS245A, SN54AS245 . . . J PACKAGE SN74ALS245A, SN74AS245 . . . DW OR N PACKAGE (TOP VIEW)



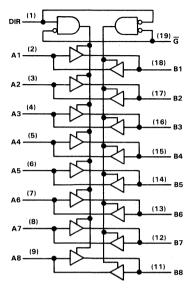
SN54ALS245A, SN54AS245 . . . FK PACKAGE



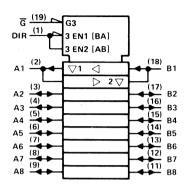
FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	н	A data to B bus
н	×	Isolation

logic diagram (positive logic)



logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC .					 	 7 V
Input voltage: All input	s				 	 7 V
I/O ports	3				 	 5.5 V
Operating free-air temp	perature range:	SN54	ALS245A		 	 55°C to 125°C
		SN74	ALS245A	٠	 	 0°C to 70°C
Storage temperature ra	ange					-65°C to 150°C

recommended operating conditions

		SN54ALS245A			SN74ALS245A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
lOH	High-level output current			-12			- 15	mA
1	I am land antend annual			12			24	mA
lOL	Low-level output current						48 [‡]	IIIA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}ddagger}$ The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS245A-1 only.



SN54ALS245A, SN74ALS245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST COMPLITIONS			SN54ALS245A			SN74ALS245A			
PA	RAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V	
		$V_{CC} = 4.5 \text{ V to } 5.5$	V_{r} I _{OH} = -0.4 mA	vcc-	- 2		Vcc-	2			
\/-··		$V_{CC} = 4.5 V,$	IOH = -3 mA	2.4	3.2		2.4	3.2		- v	
Voн		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2							
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2			1	
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4		
		$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	V	
		$(I_{OL} = 48 \text{ mA for} - 1 \text{ versions})$						0.35	0.5		
1.	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
"	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA	
	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	_	
l 'IH	A or B ports [‡]					20			20	μΑ	
	Control inputs	., 55.,				-0.1			-0.1	mA	
1 ₁ - 1 ₁ - 1 ₀ §	A or B ports [‡]	$V_{CC} = 5.5 V$,	$V_{\parallel} = 0.4 \text{ V}$			-0.1			-0.1	1 '''A	
IO§		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA	
		V _{CC} = 5.5 V	Outputs high		30	48		30	45		
Icc			Outputs low		36	60		36	55	mA	
			Outputs disabled		38	63		38	58	1	

 $^{^{\}dagger}AII$ typical values are at V_{CC} =5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		UNIT			
			SN54ALS245A		SN74ALS245A]
			MIN	MAX	MIN	MAX	
^t PLH	A or B	B or A	1	19	3	10	
t _{PHL}	AOIB		1	14	3	10	ns
^t PZH	G	A or B	2	30	5	20	ns
tPZL			2	29	5	20] "
^t PHZ	G	A or B	2	14	2	10	ns
tpLZ			2	30	4	15	115

For I/O ports, the parameters |_{HA} and |_L include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS245, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3 STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, V _{CC}
Input voltage: All inputs
I/O ports
Operating free-air temperature range: SN54AS245
SN74AS245
Storage temperature range65°C to 150°C

recommended operating conditions

		SI	SN54AS245		SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	OWIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2		-	V
V _{IL}	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 12			- 15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TECT CO.	NOTIONS		SN54AS	245	S	N74AS	245	UNIT	
		TEST CO	TEST CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNII	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5$	5 V, I _{OH} = -2 mA	Vcc-	2		v _{cc} -	2			
V		$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V	
Voн		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2						1 °	
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2			1	
Vol		$V_{CC} = 4.5 V$,	I _{OL} = 48 mA		0.3	0.55				v	
VOL		-	$V_{CC} = 4.5 V,$	I _{OL} = 64 mA					0.35	0.55]
lj.	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
'1	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1] '''^	
les s	Control inputs	Vcc = 5.5 V,	V _I = 2.4 V			50			20		
ήн	A or B ports [‡]	νCC = 5.5 v,	V = 2.4 V			70			70	μΑ	
lu.	Control inputs	Vcc = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA	
IIL	A or B ports [‡]	vCC = 5.5 v,	V = 0.4 V			-0.75			-0.75] IIIA	
IO§		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 50		- 150	- 50		- 150	mA	
			Outputs high		62	. 97		62	97		
Icc		$V_{CC} = 5.5 V$	Outputs low		95	143		95	143	m·A	
			Outputs disabled		79	123		79	123	1	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



 $^{^{\}ddagger}$ For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54AS245, SN74AS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		$V_{CC} = 4.$ $C_L = 50$ $R1 = 500$ $R2 = 500$ $T_A = MIN$	pF,) Ω,) Ω,	5 V,	UNIT
,			SN54	AS245	SN74	AS245	1
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	B or A	2	9.5	2	7.5	
^t PHL	7 701 5	B 01 A	2	9	2	7	ns
^t PZH	G	A or B	2	11	2	9	
tPZL]	G A or B		10.5	2	8.5	ns
^t PHZ	G	A or B	2	7.5	2	5.5	ns
[†] PLZ	,	20	2	12	2	9.5	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS250 1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983-REVISED JANUARY 1986

- 4-Line to 1-Line Multiplexer that can Select 1 and 16 Data Inputs
- Applications:

Boolean Function Generator Parallel-to-Serial Converter **Data Source Selector**

- **Buffered 3-State Bus Driver Inputs Permit** Multiplexing from N Lines to One Line
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

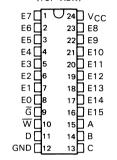
The 'AS250 provides full binary decoding to select one of sixteen data sources with an inverting W output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered enable output (G) may be used for n-line-to-one-line cascading. Taking the G high will place the output in a high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

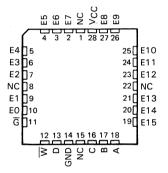
The enable (\overline{G}) does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

The SN74AS250 is characterized for operation from 0°C to 70°C.

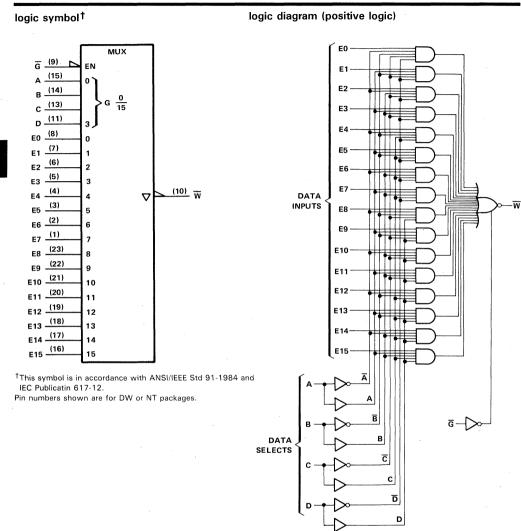
SN74AS250 . . . DW OR NT PACKAGE (TOP VIEW)



SN74AS250 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection



SN74AS250 1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

		II	IPUT			OUTPUT
G	Α	В	С	D	Ei	w
L	L	L	L	L	EO	EO
L	Н	L	L	L	E1	E1
L	L	Н	L	L	E2	E2
L	н	Н	L	L	E3	E3
L	L	L	Н	L	E4	E4
L	н	L	Н	L	E5	E5
L	L	Н	Н	L	E6	E6
L	н	Н	Н	L	E7	E7
L	L	L	L	н	E8	E8
L	н	L	L	Н	E9	E9 ·
L	L	Н	L	н	E10	E10
L	Н	Н	L	Н	E11	E11
L	L	L	Н	н	E12	E12
L	н	L	Н	Н	E13	E13
L	L	Н	Н	Н	E14	E14
L	н	Н	Н	Н	E15	E15
Н	Х	. X	Х	Х	Х	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range	°C to 70°C
Storage temperature range 65°	C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
loн	High-level output current			- 15	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C

SN74AS250 1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	ITIONS	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	$I_I = -18 \text{ mA}$			- 1.2	>
V _{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, I _{OH} = -2 mA	V _{CC} -2			V
VOH	$V_{CC} = 4.5 V$	$I_{OH} = -15 \text{ mA}$	2.4	3.3		•
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.35	0.5	V
^I OZH	V _{CC} = 5.5 V,	$V_0 = 2.7 V$			50	μΑ
lOZL .	V _{CC} = 5.5 V,	V _O = 0.4 V			- 50	μΑ
I _I	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
IIH	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
I _{IL}	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5	mA
lo [‡]	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	mA
		Outputs high		26	42	
Icc	V _{CC} = 5.5 V	Outputs low		31	50	mA
		Outputs disabled		30	48	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	((((((((((0°C	UNIT
			MIN TYP [†]	MAX	
^t PLH	DATA	DATA W		8	ns
^t PHL	- J	**	2	6	113
tPLH	SELECT	- - - - - - - - - -	4	13	no
^t PHL	- SELECT	vv .	4	10	ns
^t PZH		$\overline{\mathbf{w}}$	2	7	
^t PZL		VV	4	20	ns
^t PHZ	- G	$\overline{\mathbb{W}}$	2	6	no
tPLZ		٠, .	2	6	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS251, SN54AS251, SN74ALS251, SN74AS251 1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Three-State Versions of 'ALS151 and 'AS151
- Three-State Outputs Interface Directly with System Bus
- Performs Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

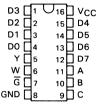
description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

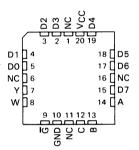
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the signal enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe (\overline{G}) . The outputs are disabled when \overline{G} is high.

The SN54ALS251 and SN54AS251 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS251 and SN74AS251 are characterized for operation from 0 °C to 70 °C.

SN54ALS251, SN54AS251 . . . J PACKAGE SN74ALS251, SN74AS251 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS251, SN54AS251 . . . FK PACKAGE (TOP VIEW)



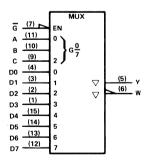
NC - No internal connection.

FUNCTION TABLE

	IN	PUT	S	OUT	PUTS
S	ELEC	Γ	STROBE	Y	w
С	В	Α	Ğ	•	W
х	Χæ	Х	н	Z	Z
L	L	L	L	D0	D0
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	н	Н	L	D3	D3
н	L	L	L	D4	D4
н	L	Н	L	D5	D5
н	н	L	L	D6	D6
н	н	н	L	D7	D7

D0, D1 . . . D7 = the level of the respective D input

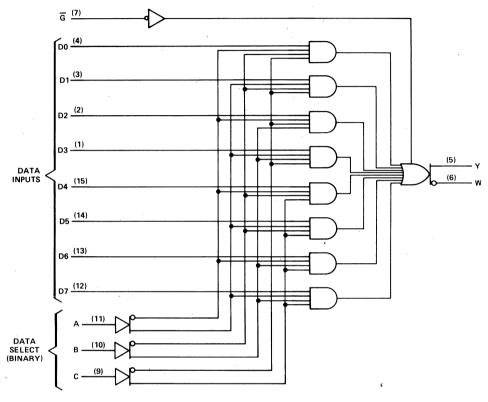
logic symbol[†]



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS251, SN54AS251 55 °C to 125 °C
SN74ALS251, SN74AS251
Storage temperature range



SN54ALS251, SN74ALS251 1-0F-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SI	SN54ALS251		SN74ALS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	. 2			2			V
V_{1L}	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			-2.6	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDIT	TIONO	S	N54ALS	251	S	N74ALS	3251	UNIT
	PARAIVIETER	TEST CONDIT	TIONS	MIN	TYP [†]	MAX	MIN	TYP†	MAX	UNII
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	v _{cc} -	2		v _{cc} -	2		
۷он		$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3				_	V
		V _{CC} = 4.5 V,	I _{OH} = -2.6 mA				2.4	3.2		1
\/a.		V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	1 °
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
lozL		V _{CC} = 5.5 V,	V _I = 0.4 V			- 20			- 20	μΑ
11		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
ΊΗ		V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IIL		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
lo‡		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
	Enabled	$V_{CC} = 5.5 V,$	Inputs at Gnd.		7	10		7	10	^
ICC	Disabled	V _{CC} = 5.5 V,	Inputs at 4.5 V		9.4	14		9.4	14	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS251, SN74ALS251 1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 R1 = 500 R2 = 500 T _A = MII	Ω, ΩΩ, N to MAX		UNIT
				IALS251		ALS251	
			MIN	MAX	MIN	MAX	
tPLH	A, B or C	Y	1	21	5	18	ns.
^t PHL	1 4, 5 01 0	'	8	34	8	24	113
^t PLH	A, B or C	w	8	38	8	24	
tPHL	7, 50, 6	, , , , , , , , , , , , , , , , , , , ,	7	26	7	23	ns
tPLH	Any D	Υ	2	15	2	10	ns
^t PHL	1 4119 5	'	3	23	3	15	115
t _{PLH}	Any D	· w	3	25	3	15	ns
t _{PHL}	1 Ally D		3	20	3	15	115
^t PZH	G	Υ	3	21	3	15	ns
tPZL	1	' .	3	19	3	15	1115
tPZH	G	w	3	21	3	4 5	
^t PZL	1	\'	3	19	3	15	ns
^t PHZ	G	Y	2	12	2	10	200
tPLZ	1 "		1	18	1	10	ns
tPHZ	G	w	2	12	2	10	
tPLZ] "	l vv	1	18	1	10	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS251, SN74AS251 1-OF-8 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SI	V54AS2	51	SN	74AS25	1	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	٧
Іон	High-level output current			-12			- 15	mA
loL	Low-level output current			32			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST CONDI	FIONC	S	N54AS	251	S	N74AS2	251	LIBUT
	PARAMETER	TEST CONDI	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
۷ _{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -	2		vcc-	2		
۷он		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2.4	3.2					٧
		$V_{CC} = 4.5 V,$	I _{OH} = -15 mA				2.4	3.3		
./		$V_{CC} = 4.5 V,$	I _{OL} = 32 mA	-	0.25	0.5				V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5	1 °
OZF		V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μΑ
OZL		V _{CC} = 5.5 V,	V _I = 0.4 V			- 50			- 50	μΑ
	A, B, C	V _{CC} = 5.5 V,	V _I = 7 V			0.2			0.2	mA
I	All other	VCC = 5.5 V,	V = / V			0.1			0.1	11114
	A, B, C	Vcc = 5.5 V,	V _I = 2.7 V			40		-	40	
IH	All other	VCC = 5.5 V,	V = 2.7 V			20			20	μΑ
	A, B, C	V E E V	V _I = 0.4 V		-0.6			-0.6		mA
IL	All other	$V_{CC} = 5.5 V$,	V = 0.4 V		-0.3			-0.3] "''A
o [‡]		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	- 30		-112	mA
СС		$V_{CC} = 5.5 V$,			28			28		mA

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 R1 = 50 R2 = 50	Ο Ω,	UNIT
			MIN TYP† MAX	MIN TYP† MAX	1
tPLH	A D	~	5	5	1
[†] PHL	A, B,or C	Y	5	5	ns
t _{PLH}	A, B, or C	w	4.5	4.5	ns
[†] PHL	A, B, 01 C		4.5	4.5	115
^t PLH	Any D	Υ	3	3	ns
t _{PHL}	Ally D	'	4	4	113
^t PLH	Any D	w	3	3	ns
t _{PHL}	,, 2		2.5	2.5	
^t PZH	G	Y	5	5	ns
^t PZL			6	6	1110
tPZH	G	W	5	5	ns
[†] PZL	0		6	6	
^t PHZ	G	Y	3	3	ns
^t PLZ	9		4	4	.,,,
[†] PHZ	G	w	3	3	ns
tPLZ		· · ·	4	4	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

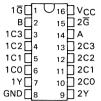
Additional information on these products can be obtained from the factory as it becomes available.

SN54ALS253, SN54AS253, SN74ALS253, SN74AS253 **DUAL 1-0F-4 DATA SELECTORS/MULTIPLEXERS** WITH 3-STATE OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Three-State Versions of 'ALS153 and 'AS153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS253, SN54AS253 . . . J PACKAGE SN74ALS253, SN74AS253 . . . D OR N PACKAGE (TOP VIEW)



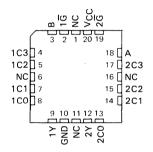
description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe (G). The output is disabled when its strope is high.

The SN54ALS253 and SN54AS253 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS253 and SN74AS253 are characterized for operation from 0 °C to 70 °C.

SN54ALS253, SN54AS253 . . . FK PACKAGE (TOP VIEW)



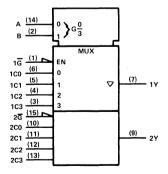
NC-No internal connection

FUNCTION TABLE

	ECT PUTS		DATA	INPUTS		OUTPUT CONTROL	ОИТРИТ
В	Α	CO	C1	C2	СЗ	G	Y
Х	X	X	×	X	Х	Н	Z
L	L	L	×	X	X	L	L
L	L	н	×	×	X	L	н
L	н	×	L	×	X	L	L
L	Н	×	Н	×	Х	L	н
Н	L	×	×	L	Х	L	L
н	L	×	×	н	X	L	н
Н	н	×	X	X	L	L	L
н	н	x	X	×	Н	L	ĺн

Address inputs A and B are common to both sections.

logic symbol[†]



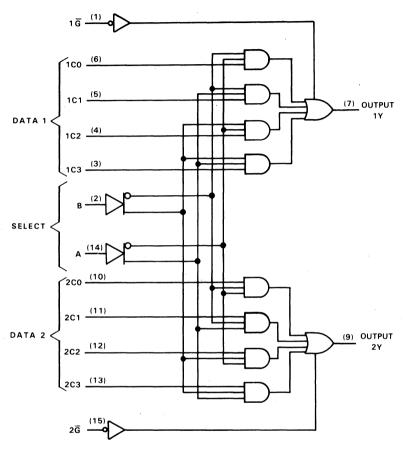
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



SN54ALS253, SN54AS253, SN74ALS253, SN74AS253 DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	
Voltage applied to a disabled 3-state output	
Operating free-air temperature range: SN54ALS253, SN54AS253	, – 55 °C to 125 °C
SN74ALS253, SN74AS253	0 °C to 70 °C
Storage temperature range	65 °C to 150 °C



SN54ALS253, SN74ALS253 DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SI	154ALS	253	SN	74ALS2	53	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	. 2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITI	ONC	SI	V54ALS	253	SN	74ALS2	53	LIBUT
PARAMETER	TEST CONDITION	UNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
Vik	$V_{CC} = 4.5 V,$	i _l = -18 mA			-1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	Vcc-	2		vcc-	2		
∨он	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					v
	$V_{CC} = 4.5 V,$	IOH = -2.6 mA				2.4	3.2		
Voi	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	1 °
^I OZH	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL	$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
tį	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 V$			20			20	μΑ
ΙΙL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
Io‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		-112	mA
loo	V _{CC} = 5.5 V	Outputs enabled		6.5	12		6.5	12	mA
lcc	VCC = 5.5 V	Outputs disabled		7.5	14		7.5	14] ""A

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to MAX}$				UNIT
			SN54	ALS253	SN74/	ALS253]
			MIN	MAX	MIN	MAX	
^t PLH	A or B	Any Y	5	30	5	21	ns
^t PHL	7016	Ally	5	27	5	21	115
[‡] PLH	Data (Any C)	Any Y	2	15	2	10	
^t PHL	Data (Ally C)	Ally 1	3	18	3	14	ns
^t PZH	G	Any Y	3	20	3	14	
tPZL	J	Ally 1	2	19	4	16	ns
tPHZ	G	Any Y	2	12	2	10	
^t PLZ		Any t	2	18	2	14	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS253, SN74AS253 **DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS** WITH 3-STATE OUTPUTS

recommended operating conditions

		S	N54AS2	253	S	N74AS2	253	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	. V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			- 12			- 15	mA
loL	Low-level output current			32			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEGT COM	DITIONO	SI	N54AS2	53	SN	74AS25	53	
PAR	AMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -2 mA	Vcc-	2		Vcc-	2		
۷он		V _{CC} = 4.5 V,	I _{OH} = -12 mA	2.4	3.2					1 v
		V _{CC} = 4.5 V,	I _{OH} = -15 mA				2.4	3.2		1
V		V _{CC} = 4.5 V,	I _{OL} = 32 mA		0.25	0.5				V
VOL		V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5	1 °
lozh		V _{CC} = 5.5 V,	$V_0 = 2.7 V$			50			50	μΑ
OZL		V _{CC} = 5.5 V,	$V_0 = 0.4 \text{ V}$			- 50			- 50	μΑ
II.	А, В	V _{CC} = 5.5 V,	V _I = 7 V			0.2			0.2	mA
. "	All others	VCC = 5.5 V,	VI - 7 V			0.1			0.1] ""A
	A, B	V _{CC} = 5.5 V,	V _I = 2.7 V			40			40	μΑ
ΉΗ	All others	VCC = 5.5 V,	V - 2.7 V			20			20	μΑ
l _{IL}	A, B	V _{CC} = 5.5 V,	V _I = 0.4 V			- 1			- 1	mA
'IL	All others	VCC = 5.5 V,	V) = 0.4 V			-0.5			-0.5	'''
10‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	- 30		-112	mA
			Outputs high		18	29		18	29	
Icc		$V_{CC} = 5.5 V$	Outputs low		20	32		20	32	mA
			Outputs disabled		21	33		21	33	1

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} \text{V}_{CC} = 4.5 \text{ V to } 5.5 \text{ V},\\ \text{C}_L = 50 \text{ pF},\\ \text{R1} = 500 \ \Omega,\\ \text{R2} = 500 \ \Omega,\\ \text{T}_A = \text{MIN to MAX} \end{array}$			UNIT	
ĺ			SN54	AS253	SN74	AS253	1 1
,			MIN	MAX	MIN	MAX	
^t PLH	A or B	Y	4	14.5	4	13.5	ns
^t PHL	A 01 B	'	4	. 12	4	11.5	""
^t PLH	Data (Any C)	Υ	3	8.5	3	7.5	ns
^t PHL	Data (Ally C)	'	3	8.5	3	8	113
^t PZH	G	Any Y	4	13	4	12.5	ns
tPZL		Ally 1	4	12	4	11.5	118
^t PHZ	G	Any Y	2	6.5	2	6	ns
tPLZ		Any 1	2	8	2	7	113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS257, SN54ALS258, SN54AS257, SN54AS258 SN74ALS257, SN74ALS258, SN74AS257, SN74AS258

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

 Three-State Outputs Interface Directly with System Bus

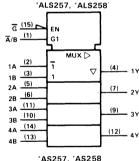
- Provides Bus Interface from Multiple Sources in High-Performance Systems
- Package Options include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

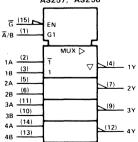
description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin (\overline{G}) is at a high-logic level.

The SN54' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

logic symbol†





[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

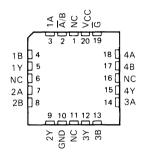
Pin numbers shown are for D, J, and N packages.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . D OR N PACKAGE (TOP VIEW)

D2661, APRIL 1982-REVISED MAY 1986

A/B 1 1 16 VCC 1A 2 15 G 1B 3 14 4A 1Y 4 13 4B 2A 5 12 4Y

SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)



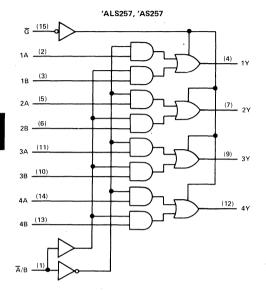
FUNCTION TABLE

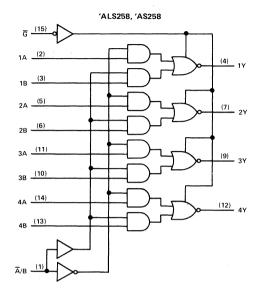
	INPUTS		OUTPUT Y						
OUTPUT	SELECT	DATA		DATA		ECT DAT		'ALS257	'ALS258
G	Ā/B	Α	В	'AS257	'AS258				
Н	×	Х	Х	Z	Z				
L	L	L	Х	L.	н				
L	L	н	Х	н	L				
L	н	×	L	L	н				
L	Н	×	Н	Н	L				



SN54ALS257, SN54ALS258, SN54AS257, SN54AS258 SN74ALS257, SN74ALS258, SN74AS257, SN74AS258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

logic diagram (positive logic)





Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7	V
Input voltage	7	V
Voltage applied to a disabled 3-state output	5.5	i۷
Operating free-air temperature range: SN54ALS', SN54AS'	-55°C to 125	٥С
SN74ALS', SN74AS'	0°C to 70	°C
Storage temperature range	65°C to 150	00

SN54ALS257, SN54ALS258, SN74ALS257, SN74ALS258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

		ı	SN54ALS257 SN54ALS258		SN74ALS257 SN74ALS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	1
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			- 1			-2.6	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CONDITI	TEST CONDITIONS		N54ALS N54ALS		ĺ	74ALS2 74ALS2		UNIT
	ANAIVIETEN	TEST CONDITI	ONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2 V _{CC} - 2						
Voн		V _{CC} = 4.5 V,	I _{OH} = -1 mA	2.4	3.3					\ \
		$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL		V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	1
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
1		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IL		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		-112	mA
			Outputs high		3	6		3	6	
}	'ALS257	V _{CC} = 5.5 V	Outputs low		8	12		8	12	1 1
1			Outputs disabled		9	14		9	14	mA
Icc			Outputs high		2.5	4		2.5	4] '''A
	'ALS258	$V_{CC} = 5.5 V$	Outputs low		7	11		7	11]
			Outputs disabled		8	13		8	13	1

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS257, SN54ALS258, SN74ALS257, SN74ALS258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

'ALS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54ALS257$ $SN74ALS257$			UNIT ,	
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	Any Y	2	12	. 2	10	ns
t _{PHL}	AUIB	Ally 1	2	14	2	12	1 "
tPLH	Ā/B	Any Y	7	21	7	18	ns
^t PHL	A/B	Any i	6.	25	6	22] ''` }
^t PZH	G	Any Y	4	20	4	16	
^t PZL	G	Ally 1	5	22	5	18	ns
^t PHZ	G	Any Y	2	12	2	10	ns
^t PLZ	J	Ally I	4	35	4	15	'''

'ALS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	T _A = MIN to MAX		ν,	UNIT	
			SN54	ALS258	SN74/	ALS258	7
			MIN	MAX	MIN	MAX	1
^t PLH	A or B	Any Y	1 .	12	2	8	ns
t _{PHL}	7015	7.,,,,	2	9	2	7	7 '''
tPLH	Ā/B	Any Y	5	28	8	20	ns
^t PHL	7/8	Ally I	8	25	5	25] '''
^t PZH	G	Any Y	5	20	5	18	ns
^t PZL	3	Any i	5	21	- 5	18	7 '''
^t PHZ	G	Any Y	2	12	2	10	ns
^t PLZ		Ally	5	37	5	18	7 ′′°

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS257, SN54AS258, SN74AS257, SN74AS258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54AS257 SN54AS258		SN74AS257 SN74AS258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	, 4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 12			- 15	mA
lOL	Low-level output current			32			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CONDITION	ONIC		N54AS2 N54AS2		_	174AS25 174AS25		UNIT
Г	ANAIVIETEN	TEST CONDITIO	JNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONII
V _{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
∨он		$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2.4	3.3					\ \
		$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2.4	3.2		
VoL		$V_{CC} = 4.5 V,$	$I_{OL} = 32 \text{ mA}$		0.25	0.5				v
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5	ľ
lozh		V _{CC} = 5.5 V,	$V_0 = 2.7 V$			50			50	μΑ
lozL		V _{CC} = 5.5 V,	V _O = 0.4 V			- 50			- 50	μΑ
1.	A, B or G	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lj	Ā/B	VCC = 5.5 V,	VI - 7 V			0.2			0.2	11124
1	A, B, or \overline{G}	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μА
ΉΗ	Ā/B	7 VCC = 5.5 V,	V - 2.7 V			40			40	μΑ
П	A, B, or \overline{G}	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.5			-0.5	mA
ЧL	Ā/B	7 VCC = 5.5 V,	V = 0.4 V			– 1			- 1	IIIA
lo [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA
			Outputs high		12.1	19.7		12.1	19.7	
	'AS257	V _{CC} = 5.5 V	Outputs low		19	30.6		19	30.6	1
1			Outputs disabled		19.7	31.9		19.7	31.9	mA
Icc			Outputs high		8.4	13.5		8.4	13.5] '''A
	'AS258	$V_{CC} = 5.5 V$	Outputs low		15.2	24.6		15.2	24.6	I
	1		Outputs disabled		15.5	25.2	l	15.5	25.2	1

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54AS257, SN54AS258, SN74AS257, SN74AS258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

'AS257 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R1=500$ Ω , $R2=500$ Ω , $T_A=MIN$ to MAX			UNIT		
	•		SN54	AS257	SN74	IAS257		
			MIN	MAX	MIN	MAX		
t _{PLH}	A or B	Any Y	1	6.5	1	5.5		
t _{PHL}	AUID	Ally I	1	7	1	6	ns	
tPLH	Ā/B	Any Y	2	12	2	11	ns	
tPHL	A/B	Ally 1	2	10.5	2	10	115	
^t PZH	G	Any Y	2	8.5	2	7.5	ns	
^t PZL	G	Ally 1	2	10.5	2	9.5	115	
^t PHZ	G	Any Y	1.5	8	1.5	6.5	ne	
^t PLZ	3	Olly 1	2	8	2	7	ns	

'AS258 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 C _L = 50 R1 = 50 R2 = 50 T _A = MI		pF,) Ω,) Ω, l to MAX		UNIT
			MIN	MAX	MIN	MAX	1
t _{PLH}	A or B	Any Y	1	5.5	1	5	
^t PHL	AOIB	Any t	1	5	1	4	ns
tPLH	Ā/B	Any Y	2	11	2	9.5	ns
^t PHL	A/B	Ally I	2	11	2	10	115
^t PZH	Ğ	Any Y	2	8.5	2	. 8	ns
^t PZL	, 0	Ally 1	2	11	2	10	113
^t PHZ	G	Any Y	1.5	7	1.5	6	ns
^t PLZ	J	Carry 1	2	8.5	2	6.5	'''

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

SN54ALS259, SN74ALS259 8-BIT ADDRESSABLE LATCHES

D2661, DECEMBER 1982-REVISED MAY 1986

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

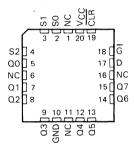
Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (G) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable G should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode. the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54ALS259 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS259 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS259 . . . J PACKAGE SN74ALS259 . . . D OR N PACKAGE

(-	го	P VIEW	<i>l</i>)
so 🗆	1	U ₁₆	□vcc
S1 🗌	2	15	CLR
S2 🗌	3	14	□ē
α ο [4	13	D
Q1 🗌	5	12	<u>0</u> 7
Q2 🗌	6	11	□ 06
0 3 [7	10	Q5
GND [8	9	Q4

SN54ALS259 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

FUNCTION TABLE

CL	PUTS	G	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
Н	1	L	D	Q _{iO}	Addressable Latch
н	l F	۲	Q_{iO}	Q_{iO}	Memory
L	. 1	L	D	L	8-Line Demultiplexer
L	. ł	Н	L	L	Clear

D = the level at the data input.

 $Q_{\hat{i}\hat{O}} \equiv$ the level of $Q_{\hat{i}}$ (i = Q, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

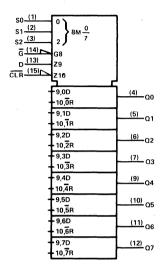
SELE	CT INF	LATCH	
S2	S1	S0	ADDRESSED
L	L	L	0
L	L	Н	1
L	Н	L	2
L	Н	Н	3
Н	L	L	4
Н	L	Н	5
) н	Н	L	6
Н	Н	Н	7

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SN54ALS259, SN74ALS259 8-BIT ADDRESSABLE LATCHES

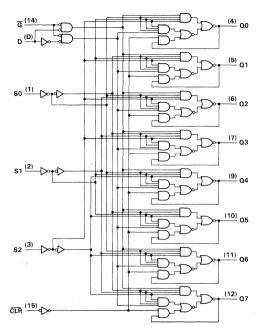
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range	: SN54ALS25955°C to 125°C
	SN74ALS259 0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

			SI	SN54ALS259		SI	V74ALS	259		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	- 5	5.5	V		
VIH	High-level input	voltage	2			2			V	
VIL	Low-level input	voltage			0.7			0.8	V	
ЮН	High-level outpu			-0.4			-0.4	mA		
loL	Low-level outpu			4			. 8	mA		
+	Pulse duration	G low	20			15				
t _W	ruise duration	CLR low	10			10			ns	
	Setup time	Data before G↑				15				
t _{su}	Setup time	Address before G↑	20			15			ns	
+.	Hold time	Data after G↑	0			0			no	
th	h Hold tillle	Address after G↑	0			0			ns	
TA	Operating free-air temperature				125	0		70	°C	



electrical characteristics over recommended operating free-air temperature range (unless otherwise

DADAMETER	TEGT COND	TIONS	SN	154ALS2	59	SN74ALS259			
PARAMETER	TEST COND	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 \text{ V},$	$I_I = -18 \text{ mA}$			- 1.5			- 1.5	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	Ì
1	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
lIL .	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
lcc	V _{CC} = 5.5 V			14	22		14	22	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \, ^{\circ}\text{C}$.

'ALS259 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = 25 ^{\circ}\text{C}$ $ALS259$ TYP		$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = MIN \text{ to}$ $ALS259$ MAX	MAX	ALS259 MAX	UNIT
tou	Clear	Any Q	8	2	15	2	12	ns
t _{PHL}	Clear	Ally Q						115
^t PLH	Data	Any Q	10	4	22	4	19	ns
tPHL	Data	Ally Q	8	2	15	2	12	113
^t PLH	Address	Anu 0	15	4	26	4	22	ns
^t PHL	Address	Any Q	8	2	15	2	12	115
t _{PLH}	Enable	Any Q	13	4	22	4	20	ns
^t PHL	Linable	Ally C	8	2	16	2	13] ''5

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

- Performs Look-Ahead Carry Across n-Bit Counters
- Accommodates Active-High or Active-Low Carry
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Improves Cascaded Counters System Performance
- Dependable Texas Instruments Quality and Reliability

description

This look-ahead generator was designed specifically to perform a carry-anticipate across any number of n-bit counters, thus increasing system clock frequency. A carry enable CE, and carry outputs RCOA and RCOB are provided for n-bit cascading.

The counter can be used with either active-high-carry or active-low-carry counters. For active-high-carry counters, CE is active high, the A set of inputs and output RCOA are used, and the B set of inputs are connected to a low logic level. For active-low-carry counters, CE is active low, the B set of inputs and output RCOB are used, and the A set of inputs are connected to a high logic level. See Figures 1 and 2 for typical applications.

The SN54AS264 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74AS264 is characterized for operation in the temperature range of $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

positive logic equations

ACTIVE-HIGH-CARRY COUNTERS (CE is high, all B inputs are low)

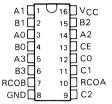
C0 = A0 $C1 = A0 \cdot A1$

 $C2 = A0 \cdot A1 \cdot A2$

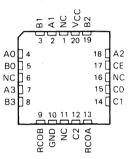
 $RCOA = A0 \cdot A1 \cdot A2 \cdot A3$

RCOB is high

SN54AS264 . . . J PACKAGE SN74AS264 . . . D OR N PACKAGE (TOP VIEW)



SN54AS264 . . . FK PACKAGE
(TOP VIEW)



NC -- No internal connection

ACTIVE-LOW-CARRY COUNTERS

(CE is low, all A inputs are high)

 $C0 = \overline{\overline{B0}}$ $C1 = \overline{\overline{B0} \cdot \overline{B1}}$ $C2 = \overline{\overline{B0} \cdot \overline{B1} \cdot \overline{B2}}$

 $RCOA = \overline{B1} \cdot \overline{B2} \cdot \overline{B3}$

 $\mathsf{RCOB} = \overline{\overline{\mathsf{B0}} \cdot \overline{\mathsf{B1}} \cdot \overline{\mathsf{B2}} \cdot \overline{\mathsf{B3}}}$

FUNCTION TABLE FOR CO OUTPUT

	INPUT	OUTPUT	
A0	во	CE	C0
Н	Н	X	Н
Н	X	Н	Н
L	Х	X	L
Х	L	L	L

FUNCTION TABLE FOR C1 OUTPUT

		OUTPUT			
A1	Α0	В1	во	CE	C1
Н	X	Н	Х	Х	Н
. н	Н	X	Н	X	н
Н	Н	Х	Х	Н	Н
L	X	Х	Х	Х	L
X	L	L	Х	Х	L
X	Х	L	L	L	L

FUNCTION TABLE FOR C2 OUTPUT

	INPUTS							
A2	A1	A0	B2	B1	ВО	CE	C2	
Н	Х	Х	Н	Х	Х	Х	Н	
Н	Н	Х	X	Н	X	Х	н	
Н	Н	Н	X	X	Н	Х	н	
Н	Н	Н	X	X	Х	Н	Н	
L	Х	Х	Х	Х	Х	Х	L	
X	L	X	L	X	Х	Χ	L	
x	X	L	L	L	Х	Χ	L	
X	Х	Х	L	L	L	L	L	

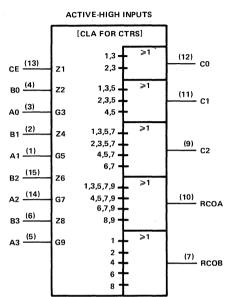
FUNCTION TABLE FOR RCOA OUTPUT

			INF	UTS				OUTPUT
А3	A2	A1	A0	В3	B2	B1	CE	RCOA
Н	Х	Х	Х	Н	Х	Х	Х	Н
Н	Н	X	Χ	Х	Н	Х	Χ	Н
Н	H	Н	X	Х	Х	Н	Х	Н
Н	Н	Н	Н	X	X	Х	Н	Н
L	X	X	Χ	Х	Х	Х	Х	Г
Х	L	X	X	Ł	X	X	Х	L
Х	Х	L	X	L	L	X	Х	L
Х	X	X	L	L	L	L	Х	L
Х	Х	X	X	L	L	L	L	L

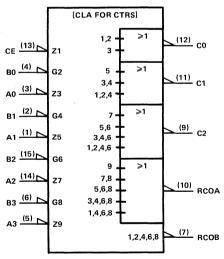
FUNCTION TABLE FOR RCOB OUTPUT

		OUTPUT			
В3	B2	В1	во	CE	RCOB
Н	Х	Х	Х	Х	Н
X	Н	X	X	X	Н
X	X	Н	X	X	Н
X	X	X	Н	Х	н
Х	Х	Х	Χ	Н	н
L	L	L	L	L	L

logic symbols†



ACTIVE-LOW INPUTS

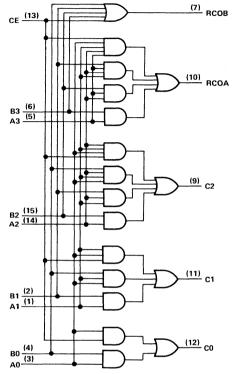


 $^{^{\}dagger}$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over free-air temperature (unless otherwise noted)

Supply voltage, VCC		
Input voltage		
Operating free-air temperature range:	SN54AS26455°C to 125°C	
	SN74AS264 0 °C to 70 °C	
Storage temperature range	65°C to 150°C	

recommended operating conditions

		S	SN54AS264			SN74AS264		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
¹ ОН	High-level output current			- 2			-2	mA
OL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-eir temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SI	SN54AS264			SN74AS264			
"	ANAIVIETEN	IEST COND	1231 CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	I _I = -18 mA	T		-1.2			-1.2	٧	
Vон		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	Vcc-	2		V _{CC} -	2		٧	
VOL		V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	٧	
	CE					500			500		
	A0, A2	•				700			700		
1	A1	V _{CC} = 5.5 V,	V 7 V			800			800		
lų .	A3, B0, B1	ν(C = 5.5 v,	V - / V	L		400			400	μΑ	
1	B2					300			300		
	B3					200			200		
	CE	V _{CC} = 5.5 V,	V _I = 2.7 V			100			100		
1	A0, A2					140			140	μΑ	
ин	A1					160			160		
'IH	A3, B0, B1	VCC = 5.5 V,				80			80] #	
1	B2					60			60]	
Į	B3				٠.	40			40		
	CE					- 2.5			- 2.5		
1	A0					-3.5			-3.5		
կլ	A1, A2	V _{CC} = 5.5 V,				-4			-4	mA	
''L	A3, B0, B1	VCC = 3.5 V,	V = 0.4 V	}		-2			-2	A	
	B2					- 1			- 1		
L	B3					- 1.5			- 1.5		
10 [‡]		V _{CC} = 5.5 V	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA	
ІССН		V _{CC} = 5.5 V			26			26		mΑ	
ICCL		ACC = 2.2 A			28			28		IIIA	

 $^{^{\}dagger}_{\perp}All$ typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 50 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS264$ $SN74AS264$							
			SN54AS264			S				
			MIN	TYP	MAX	MIN	TYP [†]	MAX	1	
t _{PLH}	CE	C0, C1, C2		6			6			
t _{PHL}		CO, C1, C2	5			5			ns	
tPLH	An or Bn	C0, C1, C2		- 5			5			
^t PHL	An or Bn	CO, C1, C2	5		5			ns		
^t PLH	An, Bn, or CE	RCOA	5			5			ns	
tPHL	All, Bil, Or CE	- NCOA	5			5				
tPLH	Bn or CE	RCOB	5			5				
[†] PHL	BITOFCE	NCOB	5			5			ns	

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{o}C.$



[‡]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS264, SN74AS264 LOOK-AHEAD CARRY GENERATORS FOR COUNTERS

TYPICAL APPLICATION INFORMATION

The circuit shown in Figure 1 illustrates how the 'AS264 can implement look-ahead carry for the activehigh-carry 'AS163, while Figure 2 shows the look-ahead carry for the active-low-carry 'AS169.

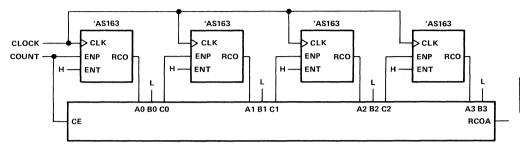


FIGURE 1-ACTIVE-HIGH-CARRY

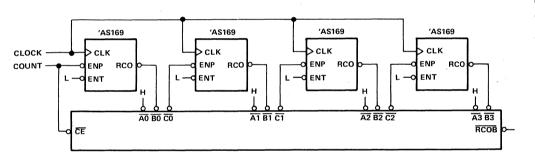


FIGURE 2-ACTIVE-LOW-CARRY

SN54ALS273, SN74ALS273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

D2661, APRIL 1982-REVISED MAY 1986

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-FLop
- Applications Include:

Buffer/Storage Registers Shift Registers Pattern Generators

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS273 is characterized for operation from 0 °C to 70 °C.

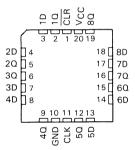
FUNCTION TABLE (EACH FLIP-FLOP)

(EACH FLIFTLOF)								
IN	OUTPUT							
CLEAR	CLOCK	D	Q					
L	X	Х	L					
Н	1	н	н					
н	1	L	L					
н	L	х	σ^0					

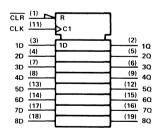
SN54ALS273 . . . J PACKAGE SN74ALS273 . . . DW OR N PACKAGE (TOP VIEW)

CLR [1	U20∏ V _{CC}
10 [2	19 🗌 8Q
1D [3	18 🗌 8D
2D [4	17 7D
20 [5	16 7Q
30 [6	15 🗌 6Q
3D [7	14 🗌 6 D
4D [8	13 🗍 5 D
40 [9	12 5Q
GND [10	11 CLK

SN54ALS273 . . . FK PACKAGE (TOP VIEW)



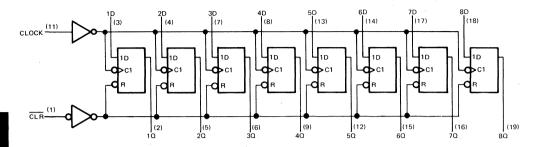
logic symbol[†]



 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	
Operating free-air temperature range:	SN54ALS273
	SN74ALS273
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

			SI	N54ALS	273	SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	,	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input volta	ge	2			2			V
VIL	Low-level input voltag	ge			0.7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
loL	Low-level output current				12			24	mA
fclock	Clock frequency		0		30	0		35	MHz
		CLR low	10			10			
t _w	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			1
	Setup time	Data	10			10			
t _{su}	before CLK1	Clear inactive state	15			15			ns
th	Hold time, data after CLK1		0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	SN54ALS273			SN74ALS273			
FARAMETER	TEST CONDIT	10145	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			- 1.5	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		v _{cc} -	2			
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -1 mA	2.4	3.3] v	
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2]	
VoL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V	
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 24 \text{ mA}$					0.35	0.5]	
l _l	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1			0.1	mA	
IH	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ	
կլ	$V_{CC} = 5.5 V,$	$V_i = 0.4 V$			-0.2			-0.2	mA	
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA	
Іссн	V _{CC} = 5.5 V			11	20		11	20	A	
ICCL	$V_{CC} = 5.5 V$			19	29		19	29	mA	

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$V_{CC}=4.5~V$ to $5.5~V$, $C_L=50~pF$, $R_L=500~\Omega$, $T_A=MIN$ to MAX					
		1	SN54	SN54ALS273		SN74ALS273		
		1	MIN	MAX	MIN	MAX		
fmax			30		35		MHz	
tPHL	CLR	Any Q	4	24	4	18	ns	
^t PLH	CLK	CLK Any Q	2	20	2	12		
tPHL		l Ally G	3	17	3	15	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS280, SN54AS280, SN74ALS280, SN74AS280 9-RIT PARITY GENERATORS/CHECKERS

D2661, DECEMBER 1982 - REVISED MAY 1986

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

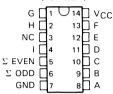
These universal, monolithic, nine-bit parity generators/checkers utilize Advanced Schottky high-performance circuitry and feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'ALS280 and 'AS280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'ALS280 and 'AS280 to be substituted for the '180 in existing designs to produce an identical function even if the devices are mixed with existing '180's.

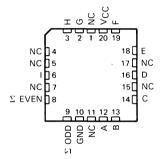
All 'AS280 inputs are buffered to lower the drive requirements.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS280, SN54AS280 . . . J PACKAGE SN74ALS280, SN74AS280 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS280, SN54AS280 . . . FK PACKAGE (TOP VIEW)

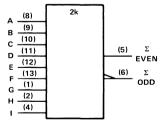


NC-No internal connection

FUNCTION TABLE

NUMBER OF INPUTS A	OUTPUTS				
THRU I THAT ARE HIGH	Σ EVEN	Σ ODD			
0,2,4,6,8	н	L			
1,3,5,7,9	L	Н			

logic symbol †

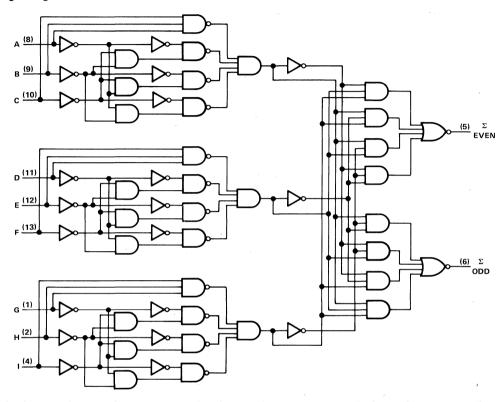


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	 	7 V
Input voltage	 	7 V
Operating free-air temperature range: SN54ALS280	 -55 °C to 12	5°C
SN74ALS280	 0°C to 7	0°C
Storage temperature range	 -65°C to 15	0°C

recommended operating conditions

		s	SN54ALS280			SN74ALS280		
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.7			0.8	٧
ТОН	High-level output current			- 1			-2.6	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT COMPLICATO	SN54ALS280	SN74ALS280	
PARAMETER	TEST CONDITIONS	MIN TYP† MAX	MIN TYP† MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$	-1.2	-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2	V _{CC} - 2	
Voн	$V_{CC} = 4.5 \text{ V}, \qquad I_{QH} = -1 \text{ mA}$	2.4 3.3		V
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -2.6 \text{ mA}$		2.4 3.2	
VOL	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 12 \text{ mA}$	0.25 0.4	0.25 0.4	V
VOL.	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 24 \text{ mA}$		0.35 0.5	·
11	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$	0.1	0.1	mA
ЧН	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$	20	20	μΑ
IJL	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$	-0.1	-0.1	mA
10‡	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$	-30 -112	-30 -112	mA
^I cc	$V_{CC} = 5.5 V$	10 16	10 16	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

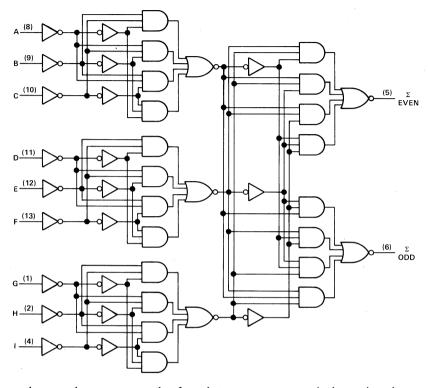
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$ 'ALS280	C _L R _L T _A	CC = 4.5 V = 50 pF, = 500 Ω , Δ = MIN to	MAX	ALS280	UNIT
			TYP	MIN	MAX	MIN	MAX	1
^t PLH	Any	ny Σ Even	12	3	24	3	20	200
[†] PHL	7 4114 1	2 Even	12	3	24	3	20	ns
^t PLH	Anv	Σ Odd	12	3	24	3	20	ns
^t PHL	Ally	2 Odd	13	4	26	4	22] "'5

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7	٧
Input voltage	7	٧
Operating free-air temperature range: SN54AS28055°C to 12	.5°	С
SN74AS280 0 °C to 7	0 °	С
Storage temperature range = 65 °C to 15	o o	0

recommended operating conditions

		S	SN54AS280			SN74AS280			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
ЮН	High-level output current			- 2			- 2	mA	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT COMPLTIONS		SI	SN54AS280			SN74AS280		
PARAMETER	IEST CONL	TEST CONDITIONS			MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	lOH = −2 mA	V _{CC} -	2		Vcc-	2		V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
liL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
ГО [‡]	. V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
^I CC	V _{CC} = 5.5 V			25	40		25	35	mA

switching characteristics (see Note 1)

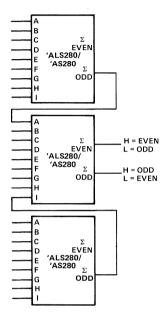
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C	CC = 4.5 \ L = 50 pF, L = 500 Ω, A = MIN to		V.	UNIT
		•	SN54AS280		SN74AS280		
			MIN	MAX	MIN	MAX]
tPLH	Any	Σ Even	3	13	3	12	ns
t _{PHL}	1 4119	2 Even	3	12.5	3	11	115
tPLHi	Any	Σ Odd	3	13	3	12	ns
^t PHL] Ally	2 300	3	12.5	3	11.5	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

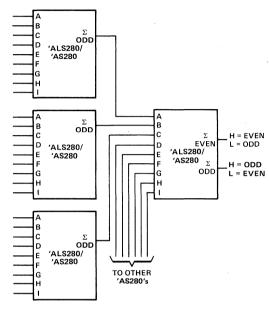
 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TYPICAL APPLICATION DATA

25-LINE PARITY/GENERATOR CHECKER



81-LINE PARITY/GENERATOR CHECKER



Three 'ALS280/'AS280 can be used to implement a 25-line parity generator/checker.

As an alternative, the Σ ODD outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

Longer word lengths can be implemented by cascading 'ALS280/'AS280. As shown here, parity can be generated for word lengths up to 81 bits.



SN54AS282, SN74AS282 LOOK-AHEAD CARRY GENERATOR WITH SELECTABLE CARRY INPUTS

D2811, DECEMBER 1983-REVISED MAY 1986

- Selectable Carry Inputs Version of the Popular 'S182 Allows Double Precision Carry
- Offers Carry Functions in a Compatible Form for Direct Connection to the ALU
- Cascadable to Perform Look-Ahead Across n-Bit Adders
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

PIN DESIGNATIONS

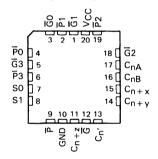
1.11 525161.51.1101.15							
ALTERNATIVE	DESIGNATIONS †	FUNCTION					
GO, G1, G2, G3	G0, G1, G2, G3	Carry Generate Inputs					
P0, P1, P2, P3	P0, P1, P2, P3	Carry Propagate Inputs					
C _{nA} , C _{nB}	$\overline{C}_{nA}, \overline{C}_{nB}$	Carry Inputs					
C _n '	<u>C</u> n′	Selected Carry					
C _{n+x} , C _{n+y} , C _{n+z}	$\overline{C}_{n+x}, \overline{C}_{n+y}, \overline{C}_{n+z}$	Carry Outputs					
G	Υ	Carry Generate Outputs					
P	V	Carry Propagate					
Р	X	Outputs					
S0	, S1	Carry Select Inputs					
V	СС	Supply Voltage					
G	ND	Ground					

 $^{^\}dagger$ Interpretations are illustrated in connection with the Function Tables for the 'AS181A and 'AS881A.

SN54AS282 . . . J PACKAGE SN74AS282 . . . DW OR N PACKAGE (TOP VIEW)

Ğ1 [Ti	U20	П	Vcc
P1 [72	19	Ħ	P2
Ğ٥ []3	18	5	G2
Po []₄	17		C_{nA}
Ğ3 [5	16		C_{nB}
P3] 6	15		C_{n+x}
S0 [7	14		C_{n+y}
S1 []8	13		$C_{n'}$
ΡĮ] 9	12		<u>G</u>
GND (]10) 11		C_{n+z}

SN54AS282 . . . FK PACKAGE



description

The 'AS282 look-ahead carry generator is capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. The 'AS282 is functionally the same as the SN54AS182/SN74AS182 except that the carry input (C_n) is selected from C_nA , C_nB , and their complements \overline{C}_nA and \overline{C}_nB . The logic equations are written in terms of the selected carry C_n . This signal is also available as an output at C_n '.

When used in conjunction with the 'AS181A, 'AS881A, or 'AS888 arithmetic logic unit (ALU), this generator provides high-speed carry look-ahead capability for any word length. The 'AS282 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry across sections of four look-ahead circuits may be employed to anticipated carry across sections of four look-ahead packages up to n-bits. The method of cascading 'AS282 circuits to perform multi-level look-ahead is illustrated under typical application data.

logic equations

$$C_{n+x} = G0 + P0 C_n$$

$$C_{n+y} = G1 + P1 G0 + P1 P0 C_n$$

$$C_{n+z} = G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 C_n$$

$$\overline{G} = \overline{G3 + P3 \ G2 + P3 \ P2 \ G1 + P3 \ P2 \ P1 \ G0}$$

$$\overline{P} = \overline{P3} \ P2 \ P1 \ P0$$

$$\begin{array}{l} \overline{C}_{n+x} = \overline{Y0 \ (X0+C_n)} \\ \overline{C}_{n+y} = \overline{Y1 \ [X1+Y0 \ (X0+C_n)]} \\ \text{or} \\ \overline{C}_{n+z} = \overline{Y2 \ (X2+Y1 \ [X1+Y0 \ (X0+C_n)])} \\ Y = Y3 \ (X3+Y2) \ (X3+X2+Y1) \ (X3+X2+X1+Y0) \\ X = X3+X2+X1+X0 \end{array}$$



FUNCTION TABLE FOR G OUTPUT

	INPUTS								
Ğ3	Ğ2	G1	Ğ0	P3	P2	P1	G		
L	Х	X	. X	Х	Х	Х	L		
Х	L	Х	Х	L	Х	Х	L		
Х	Х	L	Х	L	L	Х	L		
Х	X	Х	L	L	L	L	L		
	Al	lother	comb	ination	s		н		

FUNCTION TABLE FOR P OUTPUT

	INPUTS			OUTPUT
P3	P2	P		
L	L	L	L	L
	All o	other nations	3	н

FUNCTION TABLE FOR Cn' OUTPUT

INF	PUTS	OUTPUT			
S1	S0	C _n ′			
L	L	C _{nA}			
L	Н	Ō _{nA}			
Н	L	C _{nB}			
Н	н	ŌnB			

FUNCTION TABLE

FOR Cn+x OUTPUT

INPUTS			OUTPUT			
ĞΟ	P0	Cn′	Cn+x			
L	Х	Х	Н			
X	L	Н	н			
1	All othe mbinati		.L			

FUNCTION TABLE Cn + v OUTPUT

ſ		OUTPUT			
Ğ1	INPUTS G1 G0 P1 P0 C _n				1
31	- GU	г	FU	C _n ′	C _{n+y}
L	Х	Χ	Х	Х	н
X	L	L	Χ	X	н
х	Х	L	L	Н	н
	All other				
	C	ombina	ations		-

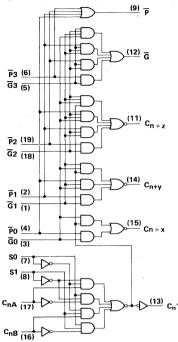
FUNCTION TABLE FOR Cn+z OUTPUT

			INPU	TS			OUTPUT
Ğ2	G1	Ğ0	P2	P1	P0	C _n ′	C _{n+z}
L	Х	X	Х	Х	X	X	Н
Х	L	Χ	L	Х	Χ	×	н
х	Х	L	L	L	Х	×	н
X	Х	X	L	L	L	Н	н
		All oth	er con	nbinati	ons		L

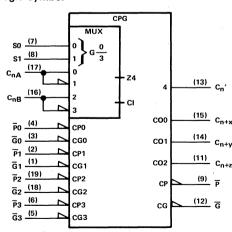
H = high-level, L = low level, X = irrelevant.

Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



logic symbol[†]



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



SN54AS282, SN74AS282 LOOK-AHEAD CARRY GENERATOR WITH SELECTABLE CARRY INPUTS

absolute maximum ratings over operating free-air temperature range (unless other	wise noted)
Supply voltage, VCC	
Operating free-air temperature range: SN54AS282	-55°C to 125°C
Storage temperature range	

recommended operating conditions

		SI	SN54AS282			SN74AS282			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
IOH	High-level output current			- 2			-2	mA	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SI	N54AS2	82	SI	V74AS2	82	
		IEST CON	IDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
Voн		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -2 \text{ mA}$	V _{CC} -	2		V _{CC} -	2		V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	C _{nA} , C _{nB}					200			200	
	S0, S1, P3					200			200	
1,	P2) F.F.V	14. 7.14			300			300	_
l)	P0, P1, G3	$V_{CC} = 5.5 V,$	V = 7 V			400			400	μΑ
	<u>G</u> 0, <u>G</u> 2					700			700	
	G1					800			800	
	C _{nA} , C _{hB}					40			40	
	S0, S1, P3					40			40	
١.	P2		V 0 7 V			60			60	
ΉΗ	₱0, ₱1, ₲3	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			80			80	μΑ
	<u>G</u> 0, <u>G</u> 2					140			140	
	Ğ1					160			160	
	C _{nA} , C _{nB}					- 1			- 1	
	S0, S1, P3					- 1			- 1	
1	<u>P</u> 2	V	.,			- 1.5			-1.5	
կլ Մ	PO, P1, G3	$V_{CC} = 5.5 V,$	V ₁ = 0.4 V			- 2			- 2	mA
	<u>G</u> 0, <u>G</u> 2					-3.5			-3.5	
	G1				-4			- 4		
lo [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Іссн		V _{CC} = 5.5 V			22		T	22		mA
ICCL		νCC = 2.5 Λ			26			26		mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.



[‡]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, los.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 p R _L = 500 T _A = MIN SN54AS282		
			MIN TYP [†] MAX	MIN TYP [†] MAX	
tPLH .	S0, S1,	C _n ′	6	6	ns
^t PHL	C _{nA} , or C _{nB}	On.	6	6	
tPLH	S0, S1,	C _{n+x} , C _{n+y} ,	6	6	ns
^t PHL	C _{nA} , or C _{nB}	C _{n+z}	. 6	6] '''
^t PLH	PorG	C _{n+x} , C _{n+y} ,	5	5	ns
^t PHL	7 '" 1	C _{n+z}	5	5	
^t PLH	P or G		6	6	ins
tPHL	7 ' "	3	5	5	ins
tPLH	P	P	5	5	
tPHL		1 -	5	5	ns

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

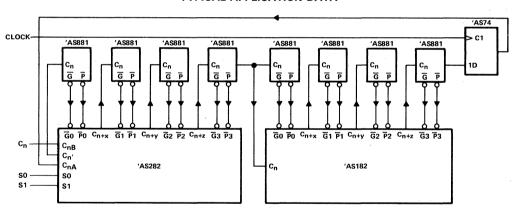


FIGURE 1-32-BIT LOOK-AHEAD CARRY WITH DOUBLE-PRECISION CARRY IN 'AS282 AND 'AS182

SN54AS286, SN74AS286 9-BIT PARITY GENERATORS/CHECKER WITH BUS DRIVER PARITY I/O PORT

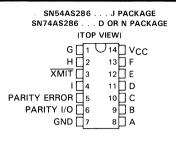
D2809, DECEMBER 1983 - REVISED MAY 1986

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port
- Glitch-Free Bus During Power Up/Down
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

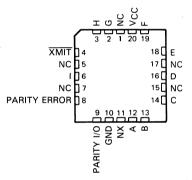
description

The SN54AS286 and SN74AS286 universal nine-bit parity generators/checkers feature a local output for parity checking and a 48-milliampere bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The XMIT control input is implemented specifically to accommodate cascading. When XMIT is low the parity tree is disabled and PE will remain at a high logic level regardless of the input levels. When XMIT is high the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.



SN54AS286 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

The SN54AS286 is characterized for operation over the full military range of -55 °C to 125 °C. The SN74AS286 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	XMIT	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	1	Н	Н
1, 3, 5, 7, 9	ı	L	Н
0, 2, 4, 6, 8	h	h	Н
0, 2, 4, 0, 8	h	1	L
1, 3, 5, 7, 9	h	h	Ĺ
1, 3, 5, 7, 9	h	1	н

h - high input level

(6) PARITY

PARITY

ERROR

I — low input level L — low output level

H - high output level

logic symbol†

N2

2,1

A (8) B (10)

C (10)

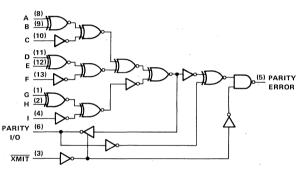
(12)

(13)

G (1)

(4)

logic diagram (positive logic)



 $^\dagger This$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range

Supply voltage, VCC	
Input voltage	[.]
Voltage applied to a disabled 3-state	output
Operating free-air temperature range	SN54AS286
	SN74AS286
Storage temperature	65°C to 140°C

recommended operating conditions

			Si	SN54AS286			SN74AS286			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	•	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage		2			2			V	
VIL	Low-level input voltage				0.8			0.8	V	
Jan	I Pate to the state of the stat	Parity error			- 2			- 2	mA	
Іон	High-level output current	Parity I/O			- 12			- 15		
la.	Low-level output current	Parity error			20			20	A	
lor	Low-level output current	Parity I/O			32			48	mA	
TA	Operating free-air temperature		- 55		125	0		70	°C	



electrical characteristics over recommended free-air temperature range (unless otherwise noted)

	ADAMETED	TEST OF	NUTIONS	SI	154AS2	86	SI	UNIT		
_ P	ARAMETER	1651 00	NDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2			- 1.2	V
	All outputs	$V_{CC} = 4.5 \text{ V to 5}.$	$5 \text{ V}, \text{ I}_{OH} = -2 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
VOH		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	2.9		2.4	3		l _v
VOH	Parity I/O	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2.4						•
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$				2.4			
	Parity error	$V_{CC} = 4.5 V$,	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	
VOL	Parity I/O	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA			0.5				V
	ranty 1/O	$V_{CC} = 4.5 V$,	$I_{OL} = 48 \text{ mA}$						0.5	
1.	Parity I/O	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	mA
l)	All other inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	'''A
1	Parity I/O [‡]	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			50			50	μΑ
ΙΉ	All other inputs	ACC = 2.2 A'	V - 2.7 V			20			20	μΑ
1	Parity I/O [‡]	$V_{CC} = 5.5 V_{c}$	V _I = 0.4 V			0.5			-0.5	mA
ll.	All other inputs	VCC = 5.5 V,	Vj = 0.4 V			0.5			-0.5	IIIA
lo§		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA
laa	Transmit	V _{CC} = 5.5 V			30	43		30	43	mA
'cc	Receive	ACC - 9.9 A	v		35	50		35	50	IIIA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R1=500$ Ω, $R2=500$ Ω, $T_A=MIN$ to MAX				UNIT
	}		SN54	SN54AS286 SN74AS2			
			MIN ,	MAX	MIN	MAX	1
^t PLH	Any A thru I	Parity I/O	3	17	3	15	ns
^t PHL	Ally A tillu I	Tanty 1/O	3	15	3	14	l iis
[†] PLH	- Any A thru I	Parity error	3	20	3	16.5	
^t PHL	Ally A tillu I	ranty entor	3	18	3	16.5	ns
^t PLH	Parity I/O	Parity error	3	10	3	9	
^t PHL	ranty 1/O	ranty entit	3	10	3	9	ns
^t PZH			3	14	3	13	
t _{PZL}	XMIT	Parity I/O	3	17	3	16]
^t PHZ		Parity I/O	3	13	3	11.5	ns
^t PLZ			3	11	3	10]

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

 $^{^{\}uparrow}All$ typical values are at VCC = 5 V, TA = 25 °C. $^{\ddagger}For$ I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

TYPICAL APPLICATION DATA

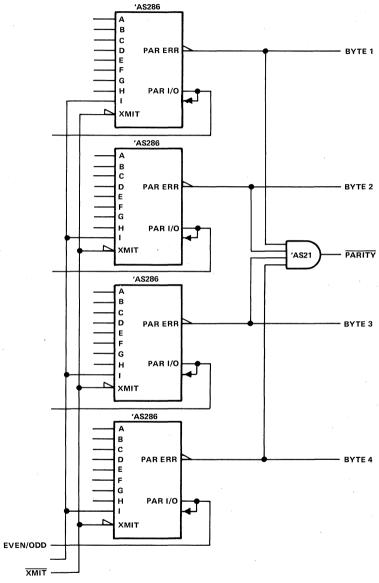


FIGURE 1. 32-BIT PARITY GENERATOR/CHECKER

Figure 1 shows a 32-bit parity generator/checker with output polarity-switching, parity error detection, and parity on every byte.



TYPICAL APPLICATION DATA

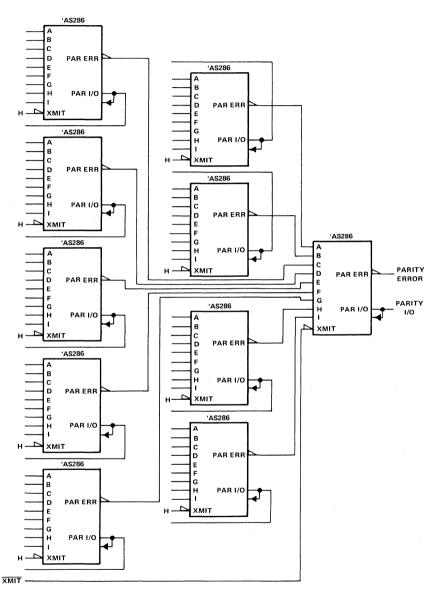


FIGURE 2. 90-BIT PARITY GENERATOR/CHECKER WITH PARITY ERROR DETECTION

In Figure 2, a 90-bit parity generator/checker with the XMIT on the last stage is available for use with parity detection.



SN54AS298, SN74AS298 OUADRUPLE 2-INPUT MULTIPLEXER WITH STORAGE

D2661, DECEMBER 1983-REVISED MAY 1986

 Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

Applications:

Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

Implements Separate Registers Capable of Parallel Exchange of Contents, yet Retains External Load Capability

Has Universal-Type Register for Implementing Various Shift Patterns, including Compound Left-Right Capability

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

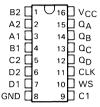
description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54AS157/SN74AS157 and SN54AS175/SN74AS175) in a single 16-pin package.

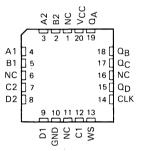
When the word-select (WS) input is low, Word 1 (A1, B1, C1, D1 is applied to the flip-flops. A high input to the word-select (WS) will cause the selection of Word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

The SN54AS298 is characterized for operation over the full military range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS298 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

SN54AS298 . . . J PACKAGE SN74AS298 . . . D OR N PACKAGE (TOP VIEW)



SN54AS298 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

	1011011011111111												
INP	JTS	OUTPUTS											
WORD SELECT	сьоск	QΑ	αв	σc	α_{D}								
L	1	a1	b1	c1	d1								
н	1	a2	b2	c2	d2								
×	Н	QAO	Q_{BO}	σ_{CO}	σ^{D0}								

H = high level (steady state)

L = low level (steady state)

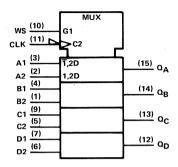
X = irrelevant (any input, including transitions)

↓ = transition from high to low level

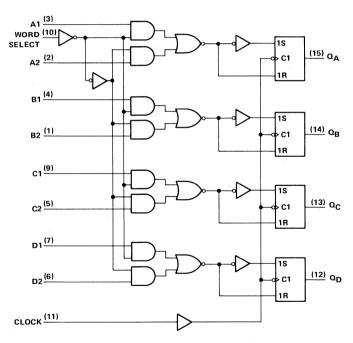
a1, a2, etc. = the level of steady-state input at A1, A2, etc. $Q_{A0}, \ Q_{B0}, \ \text{etc.} = \text{the level of } Q_A, \ Q_B, \ \text{etc. entered on the most-recent} \ \downarrow \ \text{transition of the clock input.}$



logic symbol[†]



logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.



SN54AS298, SN74AS298 QUADRUPLE 2-INPUT MULTIPLEXER WITH STORAGE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	/
Input voltage	/
Operating free-air temperature range: SN54AS298	2
SN74AS298	С
Storage temperature range -65°C to 150°C	_

recommended operating conditions

			SI	154AS2	98	SI	N74AS2	98	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	CIVIT
Vcc	Supply voltage		4.5	5	5.5	4.5	, 5	5.5	V
ViH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				-2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		100	0		100	MHz
t _w	Pulse duration, CLK high or low		5			5			ns
	Setup time before CLK ↓	Data	4.5			4.5			ns
t _{su}	Setup time before CLK ¥	Word Select	13			13			115
	Hold time after CLK ↓	Data	3.5			3.5			ns
th	Hold time after CLK +	Word Select	1			1			115
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Ĺ.,		TF0T 0	ONDITIONO	SN	54AS29	98	SN	74AS29	8	UNIT
PAI	RAMETER	IESI C	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1			- 1	V
Vон		$V_{CC} = 4.5 \text{ V to } 5.5$	V, I _{OH} = -2 mA	V _{CC} -	2		V _{CC} -	2		\ \
VoL		$V_{CC} = 4.5 V,$	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V
l _l		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ЧН	WS	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			40			40	μА
ΙΉ	All other	VCC = 3.5 V,	V = 2.7 V			20			20	μ
l	WS	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.75			-0.75	mA
ΊL	All other	ν()(= 5.5 v,	V = 0.4 V			-0.5			-0.5	1111/2
lo‡		$V_{CC} = 5.5 V$,	$V_O = 2.25 V$	-30		-112	-30		-112	mA
Іссн		$V_{CC} = 5.5 V$			21	33		21	33	mA
ICCL		V _{CC} = 5.5 V			22	36		22	36	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characterisitcs (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$					
			SN54	SN54AS298 SN74AS298					
			MIN .	MAX	MIN	MAX			
f _{max}			100	13.4	100		MHz		
^t PLH	CLK	Q	2	16	2	9	ns		
· ^t PHL	CLK		1	12	1	11			

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

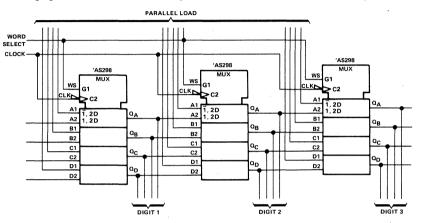


[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TYPICAL APPLICATION DATA

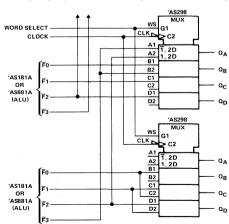
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the 'AS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.



SN54ALS299, SN54ALS323, SN54AS299, SN54AS323 SN74ALS299, SN74ALS323, SN74AS299, SN74AS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- Multiplexed I/O Ports Provides Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS299 and AS299 Have Direct Overriding Clear
- 'ALS323 and AS323 Have Synchronous Clear
- Application:

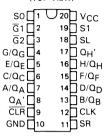
Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

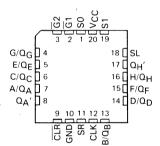
description

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously on 'ALS299, 'AS299 and synchronously on 'ALS323, 'AS323 when $\overline{\text{CLR}}$ is low. Taking either of the output controls, $\overline{\text{G1}}$ or $\overline{\text{G2}}$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

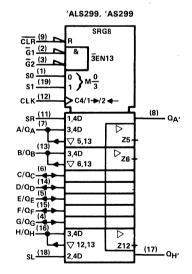
The SN54' family is characterized for operation over the full military range of $-55\,^{\circ}$ C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

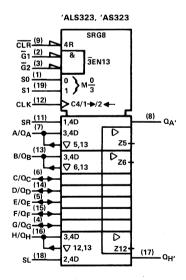
FUNCTION TABLE

				INP	UTS						I/	O POR	TS				ООТ	PUTS
MODE	CLR	S1	so	CON		CLK	SL	SR	A/Q _A	B/QB	C/QC	D/QD	E/QE	F/Q _F	G/QG	H/Q _H	Q _A ′	QH'
				Ğ1	Ğ2												İ	
Clear	L	Х	L	L	L	Х	Х	Х	L	L	L	L	L	L	L	L	L	L
('ALS299)	L	L	Х	L	L	х	х	Χ	L	L	L	L	L	L	L	L	L	L
('AS299)	L	Н	Н	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	. L	L
Clear	L	X	L	L	L	1	Х	Х	L	L	L	L	L	L	L	L	L	L
('ALS323)	L	1 L	X	L	L	1	Х	Х	L	L	L	L	L	L	L	L	L	L
('AS323)	L	Н	н	Х	Х	1	Х	Х	X	Х	Х	Х	Х	Х	Х	X	L	L
Hold	Н	L	L	L	L	Х	Х	Х	QAO	σ_{BO}	σco	σ_{D0}	σ_{EO}	Q_{F0}	a_{G0}	σ _{H0}	QAO	σH0
Hold	Ŧ	Х	Х	L	Ľ	L	Х	Х	QAO	σ_{BO}	σ^{CO}	σ_{DO}	σ_{EO}	Q_{FO}	q_{G0}	σ_{HO}	QAO	σ_{HO}
Shift Right	Н	L	Н	L	L	1	Х	Н	Н	Q_{An}	α_{Bn}	QCn	Q_{Dn}	QEn	Q_{Fn}	Q_{Gn}	Н	QGn
Simil Hight	Н	L	Н	L	L	1	X	L	, L	Q_{An}	Q_{Bn}	α_{Cn}	Q_{Dn}	α_{En}	Q_{Fn}	Q_{Gn}	L	α_{Gn}
Shift Left	Н	Н	L	L	L	1	Н	Х	QBn	QCn	Q_{Dn}	QEn	QFn	QGn	QHn	Н	Ω _{Bn}	Н
Jimit Leit	Н	Н	L	L	L	1	L	Х		α_{Cn}		α_{En}	Q_{Fn}	α_{Gn}	σ_{Hn}	L	QBn	L
Load	Н	Н	Н	Х	Х	1	Х	Х	а	b	С	d	е	f	g	h	а	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbols†

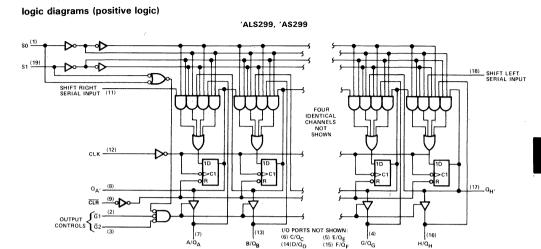


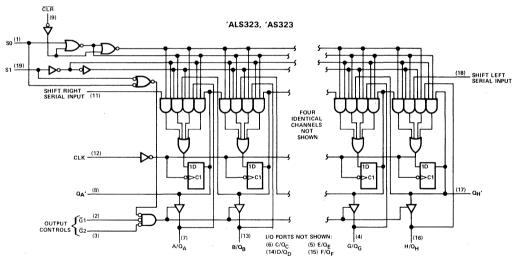


 $^{^{\}dagger}$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



SN54ALS299, SN54ALS323, SN54AS299, SN54AS323 SN74ALS299, SN74ALS323, SN74AS299, SN74AS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS





Pin numbers shown are for DW, J, and N packages.

solute maximum ratings over operating	i free-air temperature range (uniess otherwise noteu)
Supply voltage, VCC	
Input voltage: All inputs	
I/O ports	5.5 V
Operating free-air temperature range:	SN54ALS', SN54AS'
	SN74ALS', SN74AS'
Storage temperature range	65°C to 150°C



SN54ALS299, SN54ALS323, SN74ALS299, SN74ALS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

recommended operating conditions

				SN	154ALS2	299	SN	74ALS2	299	
				SN	154ALS3	323	SN	74ALS	323	UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage						2			V
VIL	Low-level input voltage					0.7			0.8	V
la	High-level output current	QA' or QH'				-0.4			-0.4	mA
Іон	mign-level output current	Q _A thru Q _H	·			- 1			-2.6	"IIA
la.	Low-level output current	QA' or QH'				4			8	mA
lOL	Low-level output current	Q _A thru Q _H		.		12			24	l ma
fclock	Clock frequency (at 50%	duty cycle)		0		17	0		30	MHz
	Pulse duration	CLK high or lov	v	22			16.5			
tw	ruise duration	CLR low ('ALS:	299)	12			10			ns
		Select		25			20			
		Serial or	High level	18			16			
	Setup time before CLK↑	Parallel data	Low level	15			6			
^t su	Setup time before CLK	CLR inactive ('/	ALS299)	15			15			ns
		CLR active ('AL	.S323)	25			20			
		CLR inactive ('/	ALS323)	18			16			İ
+.	Hold time after CLK↑	Select	,	0			0			
th .	moid time after CLK1	Serial or paralle	erial or parallel data				0			nş
TA	Operating free-air tempera	ture		- 55		125	0		70°	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				1	N54AL			N74ALS		
PAI	RAMETER	TEST CONDITI	ONS	MIN	ΤΥΡ [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.5			- 1.5	٧
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$l_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		
∨он	Q _A thru Q _H	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	Lay und all	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	Q _A , or Q _H ,	$V_{CC} = 4.5 \text{ V},$	IOL = 4 mA		0.25	0.4		0.25	0.4	
VOL	QA' OI QH'	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 8 \text{ mA}$					0.35	0.5	l _v
VOL	Q _A thru Q _H	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	·
	Lag tilla QH	$V_{CC} = 4.5 \text{ V},$	IOL = 24 mA					0.35	0.5	
łı	A thru H	$V_{CC} = 5.5 \text{ V},$	V _I = 5.5 V			0.1			0.1	mA
1	Any other	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	IIIA
ЧH [‡]		$V_{CC} = 5.5 V$	V _I = 2.7 V			20			20	μΑ
I _{IL} ‡	S0, S1, SR, SL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
I III.	All others	ACC = 9.9 A	V = 0.4 V			-0.1			-0.1	IIIA
1 - 5	QA', QH'	V _{CC} = 5.5 V,	Vo = 2.25 V	-15		- 70	- 15		- 70	mA
lO§	Q _A thru Q _H	ACC = 2.2 A	VO = 2.25 V	-30		-112	-30		-112] "'A
		,	Outputs high		15	28		15	28	
Icc		$V_{CC} = 5.5 V$	Outputs low		22	38		22	38	mA
-			Outputs disabled		23	40		23	40	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



[‡]For I/O ports (QA through QH), the parameters IIH and IIL include the off-state output current.

SN54ALS299, SN54ALS323, SN74ALS299, SN74ALS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	SN54A	V _{CC} = 4.5 C _L = 50 pF R1 = 500 S R2 = 500 S T _A = MIN to SN54ALS299 SN54ALS323		ALS299 ALS323	UNIT
4				MAX	MIN 30	MAX	MHz
fmax			17			10	IVITIZ
[†] PLH	CLK	QA thru QH	2	19	4	13	
^t PHL			4	25	7	19	ns
[‡] PLH		QA' or QH'	2	21	5	15	
^t PHL		QA O QH	4	22	8	18	
•	CLR	QA thru QH	6	29	6	22	
^t PHL	('ALS299 only)	Q _A ' or Q _H '	6	29	6	22	ns
[‡] PZH	Ğ1, Ğ2	Q _A thru Q _H	5	22	6	16	
[†] PZL	G1, G2	QA tiliu QH	6	26	8	22	ns
^t PZH	S0, S1	0. 450	5	21	7	17	
^t PZL	30, 31	Q _A thru Q _H	6	26	8	22	ns
^t PHZ	Ğ1, Ğ2	Q _A thru Q _H	1	15	1	8	
^t PLZ	G1, G2	α _A thru α _H	5	38	5	15	ns
^t PHZ	S0, S1	O . thru Ou	1	16	1	12	no
[†] PLZ	30, 31	QA thru QH	8	34	8	25	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

recommended operating conditions

					SN54AS SN54AS		1	N74AS2 N74AS3		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			٧
VIL	Low-level input voltage					0.8			0.8	V
lou	High-level output current	QA' or QH'				-2			-2	mA
Іон	riigii-ievei output current	Q _A thru Q _H				- 12			- 15	IIIA
lai	Low-level output current	Q _A ' or Q _H '				20			20	mA
lOL	Low-level output current	Q _A thru Q _H				32			48	mA
fclock	Clock frequency (at 50% duty	y cycle)								MHz
	Pulse duration	CLK high or low								no
t _w	ruise duration	CLR low ('AS299	9)							ns
		Select								
'		Serial or	High level							
١.	Setup time before CLK↑	Parallel data	Low level							ns
tsu	Setup time before CER	CLR inactive ('AS	S299)							115
1		CLR active ('AS3	323)							
		CLR inactive ('AS	6323)							
	Hold time after CLK↑	Select								no
th	Hold tille after CENT	Serial or parallel	data							ns
TA	Operating free-air temperature			-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETER	TEGT COMPLET	IONO.	1	SN54AS SN54AS		SN74AS299 SN74AS323			UNIT
PAH	AMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
-	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	I _{OH} = -2 mA	V _{CC} -	2		Vcc-	2		
Vон	Q _A thru Q _H	$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V
	QA tilla QH	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2.4	3.2		1
	QA' or QH'	$V_{CC} = 4.5 V$	$I_{OL} = 20 \text{ mA}$	ŀ	0.25	0.5		0.25	0.5	
VOL	Q _A thru Q _H	$V_{CC} = 4.5 V$	I _{OL} = 32 mA		0.25	0.5				V
	QA tint QH	$V_{CC} = 4.5 V$	I _{OL} = 48 mA					0.35	0.5	
IĮ	A thru H	$V_{CC} = 5.5 V$,	$V_{ } = 5.5 \text{ V}$							mA
ı,	Any other	$V_{CC} = 5.5 V$	V _I = 7 V	T] ""^
liH‡		$V_{CC} = 5.5 V$,	V _I = 2.7 V							μΑ
ا _{ال} ‡		$V_{CC} = 5.5 V$,	$V_{\parallel} = 0.4 \text{ V}$							mA
IO§		$V_{CC} = 5.5 V$,	V _O = 2.25 V	-30		-112	-30		-112	mA
			Outputs high							
^I CC		$V_{CC} = 5.5 V$	Outputs low							mΑ
			Outputs disabled		95			95		1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



 $^{^{\}ddagger}$ For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS299, SN54AS323, SN74AS299, SN74AS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 R1 = 50 R2 = 50 T _A = M	10 Ω, 10 Ω, IN to MAX	UNIT
			SN54AS299 SN54AS323	SN74AS299 SN74AS323	
			MIN TYP† MAX	MIN TYP† MAX	
fmax					MHz
tPLH	CLK	Q _A thru Q _H	10	10	
^t PHL	CER	QA UNU QH	10	10	ns
^t PLH	CLK	$\Omega_{ extsf{A}}'$ or $\Omega_{ extsf{H}}'$	10	10	
^t PHL	02.1		10	10	
tPHL	CLR	Q _A thru Q _H	12	12	ns
THE	02.1	Q _A ' or Q _H '	12	12	
^t PZH	Ğ1, Ğ2	QA thru QH	10	10	ns
^t PZL	G1, G2	ФД 11110 ФН	10	10	1.0
^t PZH	S0, S1	Q _A thru Q _H	10	10	ns
^t PZL	55, 51	α _A and α _B	10	10	3
^t PHZ	Ğ1, Ğ2	Q _A thru Q _H	7	7	ns
^t PLZ	31, 32	OA UIIU OH	7	7] ""
^t PHZ	S0, S1	Q _A thru Q _H	7	7	ns
^t PLZ	23, 81	GA SIIIU GH	7	7	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

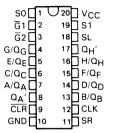
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS323, SN54AS323 SN74ALS323, SN74AS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

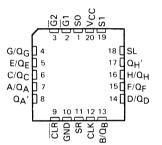
D2661, DECEMBER 1982-REVISED MAY 1986

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- Operates with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- 'ALS323 and 'AS323 Have Synchronous Clear
- Application:
 - Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)



For complete information on the SN54ALS323, SN54AS323, SN74ALS323, SN74AS323, see page 2-343.

SN54ALS352, SN54AS352, SN74ALS352, SN74AS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

D2661, APRIL 1982-REVISED MAY 1986

- Inverting Versions of 'ALS153 and 'AS153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Typical 'ALS352 Power per Multiplexer . . . 16 mW
- Typical 'AS352 Average Propagation Delay Times Data Input to Output . . . 2.7 ns Strobe Input to Output . . . 4.5 ns Select Input to Output . . . 4.5 ns
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs (G) are provided for each of the two four-line sections.

The SN54ALS352 and SN54AS352 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS352 and SN74AS352 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

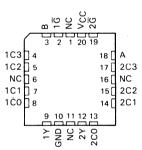
SEL	ECT) A T A	NPUTS		CTROPE	ОПТРОТ
INP	UTS		JA 1 A 1	INFOI	•		001701
В	Α	CO	C1	C2	С3	Ğ	Υ
X	×	×	X	X	×	н	н
L	L	L	X	X	×	L	н
L	L	н	X	×	×	L	L
L	н	×	L	X	×	L	Н
L	н	x	н	X	×	L	L
н	L	×	Х	L	X	L	н
н	L	×	X	н	×	L	L
н	н	×	X	X	L	L	н
н	н	x	Х	×	н	L	L

Select inputs A and B are common to both sections.

SN54ALS352, SN54AS352 . . . J PACKAGE SN74ALS352, SN74AS352 . . . D OR N PACKAGE (TOP VIEW)

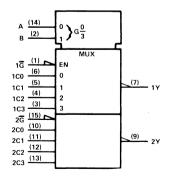
1Ğ[1	U ₁₆	□vcc
В[2	15] 2G
1C3[3	14] A
1C2[4	13] 2C3
1C1[5	12	2C2
1C0[6	11] 2C1
1 Y [7	10] 2C0
GND	18	9	2Y

SN54ALS352, SN54AS352 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol[†]

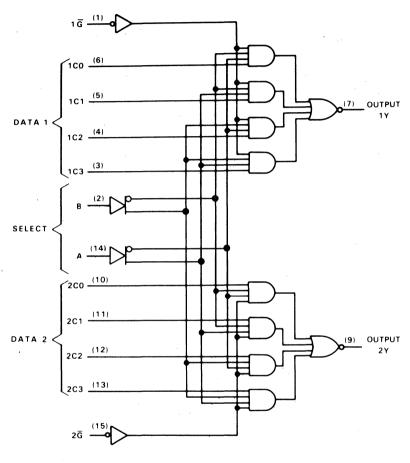


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

Pin numbers shown are for D, J, and N packages.



logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	
Input voltage	
Operating free-air temperature range: SN54ALS352, SN54AS352 55 °C to 125 °C	
SN74ALS352, SN74AS352	
Storage temperature range65 °C to 150 °C	



SN54ALS352, SN74ALS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

		 SI	154ALS	SN54ALS352			SN74ALS352			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.7			0.8	V		
Іон	High-level output current			- 1			-2.6	mA		
lOL	Low-level output current			12			24	mA		
TA	Operating free-air temperature	- 55		125	0		70	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT CONDITI	ONG	SI	N54ALS	352	SN	UNIT		
PARAMETER	TEST CONDITIONS			TYP	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		v _{cc} -	2		
∨oH [$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V/~:	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	ľ
Ч	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ЧΗ	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IL	V _{CC} = 5.5 V,	V _I = 0.4 V	1		-0.1			- O. 1	mA
10 [‡]	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
Icc	V _{CC} = 5.5 V,	See Note 1		6.5	10		6.5	10	mA

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{o}C.$

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	ТО (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MII	Ω,	ν,	UNIT
	}		SN54	ALS352	SN74	ALS352	1
	1		MIN	MAX	MIN	MAX	1
tPLH	A or B	Υ	5	32	5	24	
tPHL	7 4016	, 'T	5	24	5	21	ns
tPLH	Data (Any C)	Y	3	24	3	18	ns
tPHL	Data (Ally C)	· '	2	15	2	13	115
^t PLH	G	Y	4	26	4	18	ns
^t PHL	7 '	İ '	4	24	4	20	115

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CC} is measured with data and select inputs at 4.5 V, and G inputs grounded.

SN54AS352, SN74AS352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

recommended operating conditions

		SI	V54AS3	52	SN	74AS35	2	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONII
Vcc	Supply voltage	4.5	- 5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			- 12			- 15	mA `
lOL	Low-level output current			32			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEAT 00N	DITIONS	SI	V54AS3	52	SN	74AS3	52	UNIT
PARAMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	5 V, I _{OH} = -2 mA	V _{CC} -	2		Vcc-	2		
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2.4	3.2					7 v
	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2.4	3.3		
	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.5				V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5	7 °
, A, B	V _{CC} = 5.5 V,	V _I = 7 V .			0.2			0.2	mA
All others	vCC = 5.5 v,	V = / V			0.1			0.1] ""
, A, B	V _{CC} = 5.5 V,	V _I = 2.7 V			40			40	
IIH All others	VCC = 5.5 V,	VI = 2.7 V			20			20	μΑ
, A, B	V 5.5.V	V _I = 0.4 V			-1			- 1	mA
IIL All others	$V_{CC} = 5.5 V$,	V = 0.4 V			-0.5			-0.5	T MA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	- 30		-112	mA
	V 55V	Outputs high		15.5	25		15.5	25	A
lcc	$V_{CC} = 5.5 V$	Outputs low		17.5	28		17.5	28	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		V _{CC} = 4 C _L = 50 R _L = 500 T _A = MII	Ω,	V,	UNIT
			SN54	AS352	SN74/	AS352	1
			MIN	MAX	MIN	MAX	1
t _{PLH}	A or B	or B Y	4	12.5	4	11	ns
^t PHL	AUIB		4	14	4	13	115
^t PLH	Data (Any C)	V	2	7.5	2	6.5	ns
tPHL	Data (Ally C)	¥.	2	7	2	6] '''
^t PLH	G	· ·	3	8	3	7	ns
^t PHL		'	4	13.5	4	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



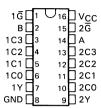
[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS353, SN54AS353A, SN74ALS353, SN74AS353A DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Inverting Versions of 'ALS253 and 'AS253
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Typical 'ALS353 Power per Multiplexer . . . 20 mW
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS353, SN54AS353A . . . J PACKAGE SN74ALS353, SN74AS353A . . . D OR N PACKAGE (TOP VIEW)



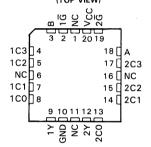
description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs (\overline{G}) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe $(\overline{\bf G})$. The output is disabled when its strobe is high.

The SN54ALS353 and SN54AS353A are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS353 and SN74AS353A are characterized for operation from 0 °C to 70 °C.

SN54ALS353, SN54AS353A . . . FK PACKAGE



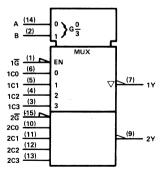
NC-No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS			OUTPUT CONTROL	ОИТРИТ	
В	A	CO	C1	C2	C3	G	Y
X	Х	×	X	X	Х	Н	Z
L	L	L	X	X	Х	L	н
L	L	H	X	X	Х	' L.	L
L	н	×	L	X	Х	L	н
L	н	×	н	X	X	L	L
Н	L	×	×	L	Х	L	Н
Н	L	×	×	н	Х	L	L
Н	Н	х	×	×	L	L	н
Н	Н	Х	×	×	Н	L	L

Select inputs A and B are common to both sections.

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

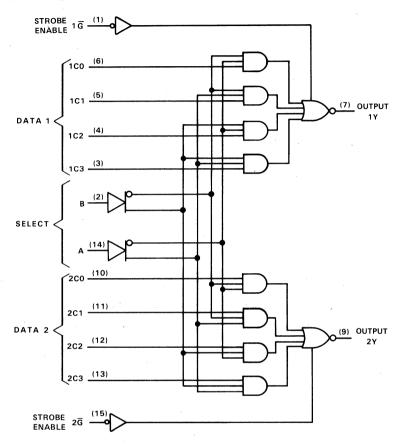
Pin numbers shown are for D, J, and N packages.





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logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	V
Input voltage	٧
Voltage applied to a disabled 3-state output	٧
Operating free-air temperature range: SN54ALS353, SN54AS353A	,C
SN74ALS353, SN74AS353A	,C
Storage temperature range – 65 °C to 150 °C	,C

SN54ALS353, SN74ALS353 **DUAL 1-0F-4 DATA SELECTORS/MULTIPLEXERS** WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54ALS353			SN74ALS353		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон	High-level output current			- 1			-2.6	mA
¹ OL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAR	AMETER		TEST CONDITIONS		SI	V54ALS	353	SN	UNIT			
PAN	AIVIETER		IESI COND	IIIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}		$V_{CC} = 4.5$	V ,	$I_1 = -18 \text{ mA}$				- 1.5			-1.5	٧
		$V_{CC} = 4.5$	√ to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$		v _{cc} -	2		vcc-	2		
Voн		$V_{CC} = 4.5$	V,	$I_{OH} = -1 \text{ mA}$		2.4	3.3] v
		$V_{CC} = 4.5$	V ,	$I_{OH} = -2.6 \text{ mA}$					2.4	3.2		
V _{OL}		$V_{CC} = 4.5$	V ,	$I_{OL} = 12 \text{ mA}$			0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5$	/ ,	I _{OL} = 24 mA						0.35	0.5	
lozh		V _{CC} = 5.5 \	√,	$V_0 = 2.7 V$				20			20	μΑ
lozL		$V_{CC} = 5.5$	√,	$V_0 = 0.4 V$,				- 20			- 20	μΑ
lį		$V_{CC} = 5.5$	√ ,	V _I = 7 V				0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5$	V,	$V_I = 2.7 V$				20			20	μΑ
կլ		$V_{CC} = 5.5$	V,	$V_1 = 0.4 V$				-0.1			-0.1	mA
lo‡		V _{CC} = 5.5	√,	V _O = 2.25 V		- 30		-112	- 30		-112	mA
di di	isabled	Vac - 5 5 V	,	All inputs, at 4.5 V			8	,13		8	13	^
ICC e	nabled	V _{CC} = 5.5 \	٧.	All inputs at Gnd			7	12		7	12	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	$B2 = 500 \Omega$						
			SN54	ALS353	SN74]		
			MIN	MAX	MIN	MAX		
tPLH	A or B	Y	5	32	5	24		
t _{PHL}	AOLP	,	5	24	5	21	ns	
t _{PLH}	Data (Any C)	Y	4	24	4	18		
t _{PHL}	Data (Any C)	'	3	15	3	13	ns	
^t PZH	G	Y	3	18	3	13		
^t PZL		1	3	20	2	16	ns	
^t PHZ	<u>G</u>	Y	2	12	2	10	ns	
^t PLZ		'	2	22	2	14] ''5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS353A, SN74AS353A DUAL 1-OF-4 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN	SN54AS353A SN74AS353A					
	· .	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
٧ _{IH}	High-level input voltage	. 2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
ГОН	High-level output current			- 12			- 15	mA
loL	Low-level output current			32			48	mA
T_A	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-	A D A A4ETED	TEOT O	ONDITIONS	SN	54AS3	53A	SN	74AS3	53A	
Ρ,	ARAMETER	IESI C	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.2			-1.2	٧
		$V_{CC} = 4.5 \text{ V to } 5.5$	$5 \text{ V}, \text{ I}_{OH} = -2 \text{ mA}$	V _{CC} -	2		V _{CC} -	2		
Vон		$V_{CC} = 4.5 V$,	I _{OH} = -12 mA	2.4	3.2					V
		$V_{CC} = 4.5 V$,	I _{OH} = -15 mA				2.4	3.3		
Va		$V_{CC} = 4.5 V$,	I _{OL} = 32 mA		0.25	0.5				V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 48 mA					0.35	0.5	\
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			50			50	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$,			- 50			- 50	μΑ
1.	A, B	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.2			0.2	mA
iţ.	All others		S = 5.5 V, VI = 7 V			0.1			0.1	1 '''
1	А, В	VCC = 5.5 V,	V _I = 2.7 V			40			40	μА
ΊΗ	All others	VCC = 5.5 V,	V - 2.7 V			20			20	μΑ
l	A, B	V _{CC} = 5.5 V,	V _I = 0.4 V			- 1			- 1	mA
ΊL	All others	VCC = 5.5 V,	V) - 0.4 V			-0.5			-0.5	1 '''^
10‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
			Outputs high		15	24		15	24	
ICC		$V_{CC} = 5.5 \text{ V}$	Outputs low		19	31		19	31	mA
			Outputs disabled		18	30		18	30	1

 $^{^{\}dagger}$ All typical values are at $^{\lor}$ CC = 5 V, T_A = 25 $^{\circ}$ C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS353A = SN74AS353A$			
			MIN	MAX	MIN	MAX	
^t PLH	A or B	Y	3	10	3	. 9	ns
^t PHL	7010	'	4	14	4	12	115
^t PLH	Data (Any C)	γ .	3	8.5	3	7.5	ns
^t PHL	Data (Ally C)	!	2	6.5	2	6	113
^t PZH	Strobe	Y	3	8.5	3	7.5	ns
^t PZL	Strobe	1	4	13.5	4	12.5] ''5
^t PHZ	Strobe	V	2	6.5	2	5.5	ns
tPLZ	Stione	'	3	9	3	7.5] '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS373, SN54AS373, SN74ALS373, SN74AS373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data
 Lines
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

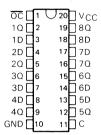
The eight latches of the 'ALS373 and 'AS373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input (\overline{OC}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

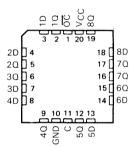
The output control \overline{OC} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS373 and SN54AS373 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS373 and SN74AS373 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS373, SN54AS373 . . . J PACKAGE SN74ALS373, SN74AS373 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS373, SN54AS373 . . . FK PACKAGE (TOP VIEW)



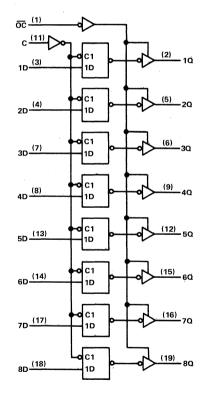
FUNCTION TABLE (EACH LATCH)

<u> </u>			
	INPUTS		OUTPUT
ŌĊ	ENABLE C	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	α ₀
Н	X	Х	Z

logic symbol†

C (11) 1D (3) 2D (4) 3D (7) 4D (8) 5D (13) 6D (14) 7D (17)	EN C1	(2) 10 (5) 20 (6) 30 (9) 40 (12) 50 (15) 60 (16) 70
7D (17) 8D (18)		(16) (19) 80

logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



SN54ALS373, SN54AS373, SN74ALS373, SN74AS373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over tree-all	r temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state	output
Operating free-air temperature range:	SN54ALS373, SN54AS373 55 °C to 125 °C
	SN74ALS373, SN74AS373
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SM	154ALS	373) SN	174ALS	373	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	Civii
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2	-		2			V
VIL	Low-level input voltage			0.7			0.8	V
ТОН	High-level output current			- 1			- 2.6	mA
lor	Low-level output current			12			24	mA
t _W	Pulse duration, enable C high	10			10			ns
t _{su}	Setup time, data before enable C↓	10			10			ns
th	Hold time, data after enable C↓	7			7			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

DADAMETED	TEST CONDITIONS		SI	154ALS	373	SN	UNIT		
PARAMETER	TEST CC	MULLIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	JUNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	Vcc	2		Vcc	2		
Voн	$V_{CC} = 4.5 V$,	I _{OH} = -1 mA	2.4	3.3					\
	V _{CC} = 4.5 V,	I _{OH} = -2.6 mA				2.4	. 3.2		1
Vai	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V	I _{OL} = 24 mA					0.35	0.5	
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V			20			- 20	μΑ
^I OZL	V _{CC} = 5.5 V,	V _I = 0.4 V			- 20			- 20	μΑ
lj	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lН	$V_{CC} = 5.5 V$,	V _I ≈ 2.7 V			20			20	μΑ
Iμ	V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.1			- 0.1	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		- 112	- 30		- 112	mA
		Outputs high		9	16		9	16	
1cc	$V_{CC} = 5.5 V$	Outputs low		16	25		16	25	mA
		Outputs disabled		17	27		17	27	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS373, SN74ALS373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R1 = 500 \text{ s}$ $R2 = 500 \text{ s}$ $T_A = MIN$	=, Ω, Ω,	V.	UNIT
			SN54ALS373		SN74		
			MIN	MAX	MIN	MAX	
tPLH	D	Q	2	17	2	12	ns
tPHL	D	ŭ.	1	. 19	4	16	IIS
^t PLH	С	Any Q	6	29	6	22	20
tPHL	C	Ally G	1	27	7	23	ns
^t PZH	ōc	Any Q	3	33	6	18	
^t PZL		Ally U	3	24	5	20	ns
^t PHZ	oc	Any Q	2	24	2	10	
^t PLZ		Any Q	2	16	2	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS373, SN74AS373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SN	154AS3	73	SN	74AS3	173	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			- 12			- 15	mA
loL	Low-level output current			32			48	mA
t _w	Pulse duration, enable C high	5.5			4.5			ns
t _{su}	Setup time, data before enable C↓	2			2			ns
th	Hold time, data after enable C↓	3			3			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

DADAMETER	TEAT COME	UTIONS	SI	154AS3	73	SN	74AS37	73	
PARAMETER	TEST COND	OTTIONS	MIN	TYP [†]	MAX	MIN	TYP	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	vcc -	2		Vcc-	2		
V _{OH}	V _{CC} = 4.5 V,	I _{OH} = -12 mA	2.4	3.2					V
	V _{CC} = 4.5 V,	$I_{OH} = -15 \text{ mA}$				2.4	3.3		
V	V _{CC} = 4.5 V,	I _{OL} = 32 mA		0.27	0.5				V
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.32	0.5	
lozh	V _{CC} = 5.5 V,	$V_0 = 2.7 V$			50			50	μΑ
^I OZL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 50			- 50	μΑ
Ч	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mΑ
ΉΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IIL	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.02	-0.5		-0.02	- 0.5	mΑ
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		- 112	mA
		Outputs high		55	90		55	90	
lcc l	$V_{CC} = 5.5 V$	Outputs low		55	85		55	85	mA
		Outputs disabled		65	100		65	100	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54AS373, SN74AS373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		(OUTPUT) $R2 = 500 \Omega,$					
			MIN	MAX	MIN	MAX		
tPLH	6		3	8	3.5	6		
t _{PHL}	D	,	3	7	3.5	6	ns	
tPLH .	С	Any Q	6.5	14	6.5	11.5		
tPHL	C . ,	Any d	5 -	8	5	7.5	ns	
^t PZH	o c	Any 0	2	7.5	2	6.5	no	
[†] PZL	UC .	Any Q	4.5	10.5	4.5	9.5	ns	
[†] PHZ	ōc	Any Q	3	7.∙5	3	6.5	ns	
[†] PLZ		Any u	3	8	3	7]. '''	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS374, SN54AS374, SN74ALS374, SN74AS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 REVISED MAY 1986

- D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ALS374 and 'AS374 are edgetriggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

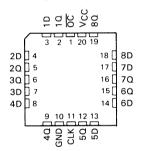
The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374 and SN54AS374 are characterized for operation over the full military temperature range of – 55 °C to 125 °C. The SN74ALS374 and SN74AS374 are characterized for operation from 0 °C to 70 °C.

SN54ALS374, SN54AS374 . . . J PACKAGE SN74ALS374, SN74AS374 . . . DW OR N PACKAGE (TOP VIEW)

ōc ☐	1	U20		۷cc
10 🏻	2	19		80
1D 🛛	3	18	р	8D
2D 🗌	4	17		7D
20 🗌	5	16	р	7Q
30 🗌	6	15		60
3D 🗌	7	14		6D
4D 🗌	8	13		5D
40 [9	12		5Q
GND 🗖	l۱c) 11	П	CLK

SN54ALS374, SN54AS374 . . . FK PACKAGE (TOP VIEW)

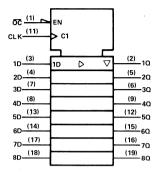


FUNCTION TABLE (EACH FLIP-FLOP)

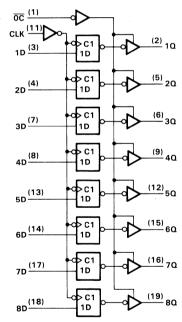
	NPUTS		OUTPUT
δĊ	CLK	D	Q
L	1	Н	Н
L	†	L	L
L	L	Х	ο ₀
Н	×	Х	Z



logic symbol[†]



logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS374, SN54AS374
SN74ALS374, SN74AS374
Storage temperature range



SN54ALS374, SN74ALS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

			S	N54ALS	374	SI	N74ALS	374	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
IOH	high-level output current				- 1			-2.6	mA
lOL	Low-level output current				12			24	mA
fclock	Clock frequency		0		30	0		35	MHz
	Pulse duration	CLK high	16.5			14			ns
t _W	ruise duration	CLK low	16.5			14			1 115
t _{su}	Setup time, data before CLK1		10			10			ns
th	Hold time, data after CLK1		4			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

PARAMETER	TEST CONDITIONS		SI	V54ALS	374	SN	LINUT		
PANAIVIETEN	IESI C	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.9$	$5 \text{ V}, \text{ I}_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		vcc-	2		
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL _	$V_{CC} = 4.5 \text{ V}$	1 _{OL} = 24 mA					0.35	0.5	V
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL	$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μΑ
11	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
liΗ 🧲	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
lıL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.2			-0.2	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
		Outputs high		11	19		11	19	
lcc .	$V_{CC} = 5.5 V$	Outputs low		19	28		19	28	mA
		Outputs disabled		20	31		20	31	

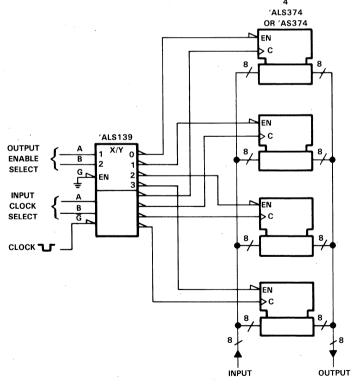
 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching charac	cteristics (see Note 1)						
				V _{CC} = 4.5 \	√ to 5.5 V	,	
			-	$C_L = 50 pF$,			
PARAMETER	FROM	то		$R1 = 500 \Omega$			UNIT
PARAMETER	(INPUT)	(OUTPUT)		$R2 = 500 \Omega$			UNIT
			_ i	$T_A = MIN to$	MAX		
			SN54	1ALS374	SN74	ALS374	
			MIN	MAX	MIN	MAX	
f _{max}			30		35		MHz
t _{PLH}	CLK	Q	3	21	3	12	ns
^t PHL	l CLK		5	19	5	16	115
^t PZH	ŌC	Q	5	27	5	. 17	ns
tPZL	1		6	23	7.	18	113
^t PHZ	ōc	Q	2	12	2	10	ns
tPLZ]	1	3	33	3	18	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

EXPANDABLE 4-WORD BY 8-BIT GENERAL REGISTER FILE





SN54AS374, SN74AS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

			-	S	N54AS	374	S	N74AS	374	UNIT
			Γ	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.7			0.8	V
loн	High-level output current					-12			-15	mA
lOL	Low-level output current					32			48	mA
fclock	Clock frequency			0		100	0		125	MHz
+	Pulse duration	CLK high		5.5	5		4			ns
t _w	ruise duration	CLK low		5			3			115
+	Setup time data			3			2			ns
t _{su}	before CLK1			3			-			ns
^t h	Hold time, data after CLK1			3			2			ns
TA	Operating free-air temperature			- 55		125	0		70	°C

DADAMETED	TEGT (CONDITIONS	SI	N54AS3	74	SN	74AS37	14	LIBUT
PARAMETER	lesi c	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to 5}.$	5 V, $I_{OH} = -2 \text{ mA}$	V _{CC} -	2		V _{CC} -	2		
Voн	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2.4	3.2			-		V
	$V_{CC} = 4.5 V,$	$l_{OH} = -15 \text{ mA}$				2.4	3.3		
Va	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.29	0.5				V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA					0.34	0.5	v
lozh	$V_{CC} = 5.5 V$,	V _O = 2.7 V			50			50	μΑ
lozL	$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 50			- 50	μΑ
l _l	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
OC, CLK	\/ F.F.\/	V 0.4 V			-0.5			-0.5	
IL Data	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			- 3			- 2	mA
lo [‡]	$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	- 30		-112	mA
		Outputs high		77	120		77	120	
Icc	$V_{CC} = 5.5 V$	Outputs low		84	128		84	128	mA
		Outputs disabled		84	128		84	128	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

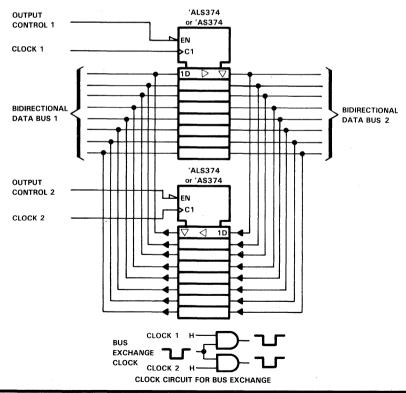
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching charac	cteristics (see Note 1)								
				V _{CC} = 4.5 V to 5.5 V,					
	*		-	$C_L = 50 pF,$					
PARAMETER	FROM	то	1	$R1 = 500 \Omega$			UNIT		
PANAIVIETEN	(INPUT)	(OUTPUT)	Į.	$R2 = 500 \Omega$			UNIT		
				TA = MIN to	MAX				
			SN54	4AS374	SN74	AS374	1		
			MIN	MAX	MIN	MAX			
fmax			100		125		MHz		
^t PLH	CLK	Q	3	11	3	8	ns		
tPHL	CER		4	11.5	4	9	1 115		
^t PZH	ōc	Q	2	7	2	6	ns		
^t PZL		4	3	11	. 3	10	1 115		
tPHZ	ōc	à	2	7	2	6	ns		
^t PLZ	1		2	7	2	6	1 ''5		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

BIDIRECTIONAL BUS DRIVER





SN54ALS465A THRU SN54ALS468A, SN74ALS465A THRU SN74ALS468A OCTAL BUFFERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 - REVISED MAY 1986

- Mechanically and Functionally Interchangeable with DM71/81LS97 and DM71/81LS98
- P-N-P Inputs Reduce Bus Loading
- 3-State Outputs Rated at IOL of 12 mA and 24 mA for SN54ALS' and SN74ALS', Respectively
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DEVICE	DATA PATH
'ALS465A	True
'ALS466A	Inverting
'ALS467A	True
'ALS468A	Inverting

description

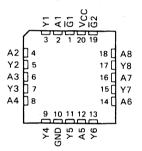
These octal buffers utilize the latest advanced low-power Schottky technology. The 'ALS465A and 'ALS466A have a two-input active-low AND enable gate controlling all eight data buffers. The 'ALS467A and 'ALS468A have two separate active-low enable inputs each controlling four data buffers. In each case, a high level on any \overline{G} places the affected outputs at high impedance.

The SN54ALS465A, SN54ALS466A, SN54ALS467A, and SN54ALS468A are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS465A, SN74ALS466A, SN74ALS467A, and SN74ALS468A are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

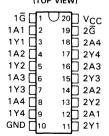
SN54ALS465A, SN54ALS466A . . . J PACKAGE SN74ALS465A, SN74ALS466A . . . DW OR N PACKAGE (TOP VIEW)



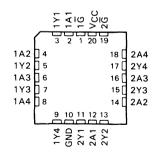
SN54ALS465A, SN54ALS466A . . . FK PACKAGE
(TOP VIEW)



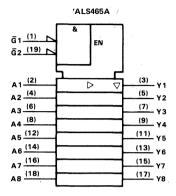
SN54ALS467A, SN54ALS468A . . . J PACKAGE SN74ALS467A, SN74ALS468A . . . DW OR N PACKAGE (TOP VIEW)

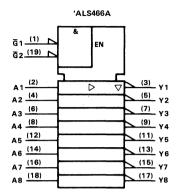


SN54ALS467A, SN54ALS468A . . . FK PACKAGE (TOP VIEW)

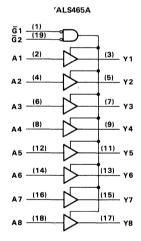


logic symbols†





logic diagrams (positive logic)



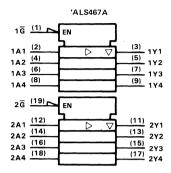
	'Δ	LS466A		
Ğ1. Ğ2.	(1)	D		
A 1	(2)		(3)	Y 1
A2 ·	(4)		(5)	Y2
АЗ -	(6)		(7)	Y3
A4	(8)	S	(9)	Y4
A5	(12)	S	(11)	Y5
A6	(14)		(13)	Y 6
A7	(16)	S	(15)	Y 7
A8	(18)	S	(17)	Y8

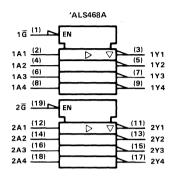
 $^{^\}dagger These$ symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



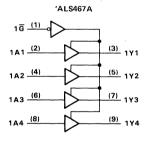
SN54ALS465A THRU SN54ALS468A, SN74ALS465A THRU SN74ALS468A OCTAL BUFFERS WITH 3-STATE OUTPUTS

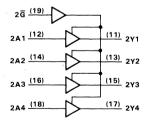
logic symbols†

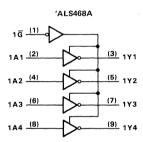


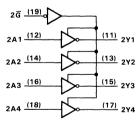


logic diagrams (positive logic)









[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



SN54ALS465A THRU SN54ALS468A, SN74ALS465A THRU SN74ALS468A OCTAL BUFFERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operati	ng free-air temperatu	ire range (unless otherwise note	d)
Supply voltage, VCC			7 V
Input voltage			7 V
Voltage applied to a disabled 3-state	output		5.5 V
Operating free-air temperature range:	SN54ALS465A THRU	SN54ALS468A	-55°C to 125°C
	SN74ALS465A THRU	SN74ALS468A	0°C to 70°C

Storage temperature range recommended operating conditions

		SN54ALS465A THRU SN54ALS468A		THRU THRU				UNIT
	· ·	MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VιΗ	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
loн	High-level output current			-12			- 15	mA
loi	Low-level output current			12			24	mA
IOL	Low-level output current						48†	IIIA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}\text{The}$ extended limit applies only if $V_{\mbox{\footnotesize{CC}}}$ is maintained between 4.75 V and 5.25 V.

The 48 mA limit applies for SN74ALS465A-1, SN74ALS466A-1, SN74ALS467A-1, and SN74ALS468A-1 only.

PARAMETER		TEST CONDITIONS		s	N54ALS THRU N54ALS	J 468A	SN	174ALS4 THRU 174ALS4	168A	UNIT
				MIN	TYP [‡]		MIN	TYPI	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$		<u> </u>		- 1.5			- 1.5	V
			V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -			V _{CC} -			ļ
Vон	<u> </u>	$V_{CC} = 4.5 \text{ V},$		2.4	3.2		2.4	3.2		l v
- 011	·	$V_{CC} = 4.5 \text{ V},$		2						1
			$I_{OH} = -15 \text{ mA}$				2			<u> </u>
VoL		$V_{CC} = 4.5 V,$	<u> </u>		0.25	0.4		0.25	0.4	l
		$V_{CC} = 4.5 V,$		١ .			ļ	0.35	0.5	V
		(I _{OL} = 48 mA for -1 versions)								
lozh		$V_{CC} = 5.5 V$,				20			20	μΑ
lozL		$V_{CC} = 5.5 V$,		<u> </u>		- 20			- 20	μΑ
lı		$V_{CC} = 5.5 V$,	V _I = 7 V	<u> </u>		0.1	<u> </u>		0.1	mA
ΊΗ		$V_{CC} = 5.5 V$	V _I = 2.7 V	<u> </u>		20			20	μΑ
ΙΙL		$V_{CC} = 5.5 V,$	$V_{\parallel} = 0.4 V$	<u> </u>		-0.1			-0.1	mA
10 [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
	'ALS465A		Outputs high		11	21		11	16	1
	'ALS467A	$V_{CC} = 5.5 V$	Outputs low		19	33		19	28	mA
1cc	ALSTOTA		Outputs disabled		23	38		23	33	
	'ALS466A		Outputs high		7	15		7	10	
	ALS468A	Vcc = 55 V	Outputs low		16	29		16	24	mA
	AL5400A		Outputs disabled		19	32		19	27	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54ALS465A THRU SN54ALS468A, SN74ALS465A THRU SN74ALS468A OCTAL BUFFERS WITH 3-STATE OUTPUTS

'ALS465A, 'ALS467A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				
			ı	SN54ALS465A SN54ALS467A		1		
			SN54			SN74ALS467A		
			MIN	MAX	MIN	MAX		
^t PLH	Α	Υ	2	16	2	13		
^t PHL		'	4	15	4	12	ns	
^t PZH	G	Any Y	4	27	4	23		
t _{PZL}	· ·	Ally 1	5	30	5	25	ns	
^t PHZ	G	Any Y	2	12	2	10	ns	
tPLZ	J	Ally 1	3	21	3	18	115	

'ALS466A, 'ALS468A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$			
			SN54ALS466A SN54ALS468A		SN74ALS466A SN74ALS468A		
			MIN	MAX	MIN	MAX	
^t PLH	A	Y	3	14	3	12	
^t PHL	^	^ 2		11	2	9	ns
^t PZH	G	Any Y	4	21	4	16	
^t PZL	3	Any t	7	25	7	23	ns
^t PHZ	G	Any Y	2	12	2	10	
tPLZ		Ally 1	2	20	2	17	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522 8-BIT IDENTITY COMPARATORS

D2661, JUNE 1982-REVISED MAY 1986

- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- 'ALS518, 'ALS520, and 'ALS522 Have 20-kΩ Pull-up Resistors on Q Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

Ì	INPUT	OUTPUT FUNCTION					
TYPE	PULL-UP	AND					
	RESISTOR	CONFIGURATION					
'ALS518	Yes	P = Q open-collector					
'ALS519	No	P = Q open-collector					
'ALS520	Yes	P=Q totem-pole					
'ALS521†	No	$\overline{P} = \overline{Q}$ totem-pole					
'ALS522	Yes	$\overline{P} = \overline{Q}$ open-collector					

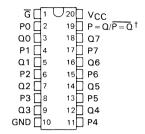
1'ALS521 is identical to 'ALS688

description

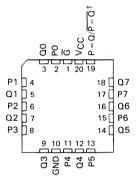
These identity comparators perform comparisons on two eightbit binary or BCD words. The 'ALS518 and 'ALS519 provide P=Q outputs, while the 'ALS520, 'ALS521, and 'ALS522 provide $\overline{P=Q}$ outputs. The 'ALS518, 'ALS519, and 'ALS522 have open-collector outputs. The 'ALS518, 'ALS520, and 'ALS522 feature 20-k Ω pull-up termination resistors on the Q inputs for analog or switch data.

The SN54ALS518 through SN54ALS522 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS518 through SN74ALS522 are characterized for operation from 0 °C to 70 °C.

SN54ALS' . . . J PACKAGE SN74ALS' . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS' . . . FK PACKAGE (TOP VIEW)



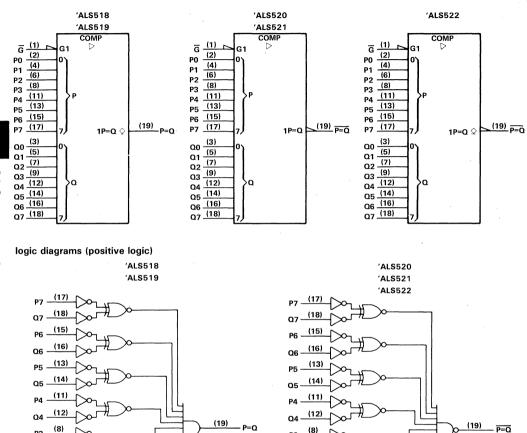
[†] P=Q for 'ALS518 and 'ALS519, and $\overline{P}=\overline{Q}$ for 'ALS520, 'ALS521, and 'ALS522.

FUNCTION TABLE

INP	UTS	OUTPUTS			
DATA P, Q	ENABLE G	P = Q	$\overline{P} = \overline{Q}$		
P=Q	L	H	L		
P>Q	L	L	Н		
,P <q< td=""><td>L</td><td>L</td><td>Н</td></q<>	L	L	Н		
Х	Н	L	• н		

logic symbols†

SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522 **8-BIT IDENTITY COMPARATORS**



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



(9)

(6) (7)

(4)

(5)

(2) (3)

00 G (1)

Р3

03

Q2 (4)

QO

(5)

(2)

SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522 **8-BIT IDENTITY COMPARATORS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage: Q inputs of 'ALS518	, 'ALS522
All other inputs	
Off-state output voltage	
Operating free-air temperature range	: SN54ALS518, SN54ALS519, SN54ALS522 55 °C to 125 °C
	SN74ALS518, SN74ALS519, SN74ALS522 0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SI	SN54ALS518			SN74ALS518		
		SI	SN54ALS519		SN74ALS519			UNIT
		SI	N54ALS	522	SN	74ALS5	22	
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
ViH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Vон	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

PARAMETER		TEST CONDITIONS		SN SN	54ALS5 54ALS5 54ALS5	i19 i22	SN74ALS518 SN74ALS519 SN74ALS522			UNIT	
Vest		V _{CC} = 4.5 V,	I _I = -18 mA	MIN	IYP	- 1.5	MIN	TYP [†]	- 1.5	V	
VIK				 							
ЮН		$V_{CC} = 5.5 \text{ V},$	V _{OH} = 5.5 V			0.1	İ		0.1	mA	
VOL		$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V	
\ VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA	T				0.35	0.5	ľ	
łı	'ALS518, 'ALS522 Q inputs	$V_{CC} = 5.5 V$,	$V_{I} = 5.5 V$			0.1			0.1	mA	
"	All other inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	IIIA	
ΙΗ	'ALS518, 'ALS522 Q inputs	$V_{CC} = 5.5 V$,	V _I = 2.7 V			-0.2			-0.2	mA	
"IH	All other inputs	VCC = 5.5 V,	V - 2.7 V			20			20	μΑ	
1	'ALS518, 'ALS522 Q inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.6	1		-0.6	mA	
11L	All other inputs	vCC = 5.5 v,	V = 0.4 V			-0.1			-0.1	l IIIA	
	'ALS518				11	17		11	17		
1cc	'ALS519	$V_{CC} = 5.5 V$,	See Note 1		11	17		11	17	mA	
	'ALS522	}			11	17		11	17	1	

 $^{^{\}dagger}$ All typical values are at V $_{CC}~=~5$ V, T $_{A}~=~25\,^{\circ}C$. NOTE 1: I $_{CC}$ is measured with \overline{G} grounded, P and Q at 4.5 V.



SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522 8-BIT IDENTITY COMPARATORS

'ALS518, 'ALS519 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L T _A SN54A	C = 4.5 V to = 50 pF, = 680 Ω, = MIN to MA LS518 LS519	AX SN74	ALS518 ALS519 MAX	UNIT
tPLH	P or Q	P=Q	15	37	15	33	ns
tPHL	1 01 4	1 – 4	3	18	3	15	1.5
tPLH	G	P=Q	15	37	15	33	ns
tPHL	ď	1 – 4	3	18	3	15	

'ALS522 switching characteristics (see Note 1)

	mig characteriotics (cos	•							
			V _C	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$					
			CL	= 50 pF,					
	FROM	то	RL	= 680 Ω,					
PARAMETER	(INPUT)	(OUTPUT)	TA	= MIN to MA	AX		UNIT		
			SN54/	SN54ALS522		ALS522			
	·		MIN	MAX	MIN	MAX			
tPLH	P or Q	P=Q	10	30	10	25	ns		
t _{PHL}	Poru	P=U	5	25	5	23	lis		
· tPLH	G	<u>P=Ω</u>	8	30	8	25	ns		
tPHL	G	1 - 4	8	30	8	23	''		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522 **8-BIT IDENTITY COMPARATORS**

absolute maximum ratings over operati	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	
Input voltage: Q inputs of 'ALS520	
All other inputs	,
Operating free-air temperature range:	SN54ALS520, SN54ALS52155°C to 125°C
	SN74ALS520, SN74ALS521
Storage temperature range	

recommended operating conditions

		SI	SN54ALS520			SN74ALS520		
		SI	SN54ALS521			SN74ALS521		
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон -	High-level output current			- 1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

	ADAMETED	TEST CONF	UTIONS		N54ALS N54ALS			74ALS5		UNIT
-	ARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX]
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			-1.5	V
		$V_{CC} = 4.5 \text{ V to 5}.$	5 V, IOH = -0.4 mA	Vcc-	2		vcc-	2		
Vон		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -1 mA	2.4	3.3					V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		1 .
V/01		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
V_{OL}	•	$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5]
1.	'ALS520 Q inputs	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	mA
Ц	All other inputs	V _{CC} = 5.5 V	V _I = 7 V			0.1			0.1	mA
1	'ALS520 Q inputs	Vcc = 5.5 V,	V1 = 2.7 V			-0.2			-0.2	mA
ΉΗ	All other inputs	VCC = 5.5 V,	V = 2.7 V			20			20	μΑ
l	'ALS520 Q inputs	VCC = 5.5 V,	V _I = 0.4 V			-0.6			-0.6	
IIL.	All other inputs	VCC = 5.5 V,	V) - 0.4 V			-0.1			-0.1	mA
10 [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
loo	'ALS520	V _{CC} = 5.5 V,	See Note 1		12	19		12	19	^
1CC	'ALS521	νCC = 5.5 V,	See Note 1		12	19		12	19	mA

 $^{^{\}dagger}All$ typical values are at VCC = 5 V, TA = 25 °C.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with $\overline{\mathbf{G}}$ grounded and P and Q inputs at 4.5 V.

SN54ALS518 THRU SN54ALS522, SN74ALS518 THRU SN74ALS522 8-BIT IDENTITY COMPARATORS

'ALS520, 'ALS521 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)				UNIT		
^t PLH	P or Q	P=Q	3	19	3	12		
t _{PHL}	FORQ	r=u	3	25	5	20	ns	
tPLH	G	P=Q	2 .	18	2	12		
tPHL		, r=u	5	23	5	22	ns	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

SN54ALS526, SN54ALS527, SN54ALS528 SN74ALS526, SN74ALS527, SN74ALS528 FUSE-PROGRAMMABLE IDENTITY COMPARATORS

D2826 JUNE 1984 - REVISED MAY 1986

- Can Be Programmed and Verified on Most Incoming Test Equipment
- Reduces Board and Package Size for Similar Fixed Comparator Functions
- High-Speed Address Recognition
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

Programming Capabilities

'ALS526 - Fuse Programmable 16-Bit

Identity Comparator

'ALS527 - Fuse Programmable 8-Bit

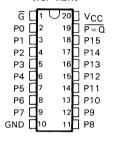
Identity Comparator and 4-Bit

Comparator

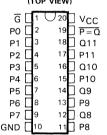
'ALS528 - Fuse Programmable 12-Bit

Identity Comparator

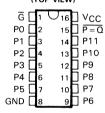
SN54ALS526 . . . J PACKAGE SN74ALS526 . . . DW OR N PACKAGE (TOP VIEW)



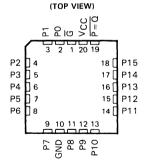
SN54ALS527 . . . J PACKAGE SN74ALS527 . . . DW OR N PACKAGE (TOP VIEW)



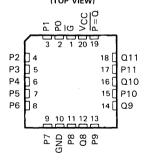
SN54ALS528 . . . J PACKAGE SN54ALS528 . . . DW OR N PACKAGE (TOP VIEW)



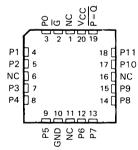
SN54ALS526 . . . FK PACKAGE



SN54ALS527 . . . FK PACKAGE (TOP VIEW)



SN54ALS528 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

description

The 'ALS526 and 'ALS528 are fuse-programmable identity comparators designed for easy programming in fixed-comparator applications. The 'ALS526 compares a 16-bit data word against a preprogrammed 16-bit data word while the 'ALS528 compares a 12-bit data word against a preprogrammed 12-bit data word. The $\overline{P} = \overline{Q}$ output will go low when the applied data word (P inputs) matches the preprogrammed data word (Q represents the preprogrammed data word). Programming is easily accomplished on the bench or with conventional automatic test equipment. Special equipment such as PROM-programmers are not reauired.

The 'ALS527 is a combination of an 8-bit fuse-programmable comparator and a conventional 4-bit comparator. For the $\overline{P=Q}$ output to go low, the applied data word P0 through P7 must match the preprogrammed data word Q0 through Q7, and the applied data word P8 through P11 must match the applied data word Q8 through Q11.

The SN54ALS526, SN54ALS527, and SN54ALS528 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS526, SN74ALS527, and SN74ALS528 are characterized for operation from 0°C to 70°C.

programming procedure

Before any fuses are blown, the inputs will recognize a low logic level. Therefore, only the bits that are to recognize a high logic level require programming. A fuse is blown by applying 12 volts (VIHH) to the desired P input and also to the \overline{G} input. This permanently programs the pin to recognize a high. Only one input pin should be programmed at a time.

- Take \overline{G} to V_{IL} and apply V_{IH} to all P inputs[†]. Step 1.
- Take desired P input to VIHH, output will be low if the fuse is intact. Step 2.
- Step 3. Pulse G to VIHH. After G has returned to VIL, the output will be high indicating that the fuse is blown.
- Step 4. Take P input back to VIH. Repeat steps 2 through 4 to program additional inputs.

verification procedure

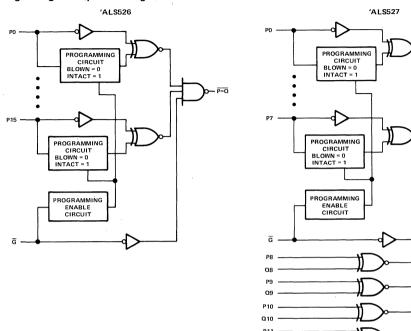
These devices can be checked to determine which fuses if any are blown. Figure 1 shows how verification can be accomplished during programming.

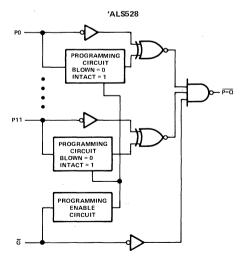
- Step 1. Take \overline{G} and all P inputs[†] to V_{IL}. If the output is low, all fuses are intact.
- Take all P inputs to VIH. The output should be high except when all fuses are blown. If all fuses Step 2. are blown then the output will be low.
- Take test input to VIHH, leaving other inputs at VIH. If the output goes low, the fuse is intact. Step 3. If the output goes high, the fuse is blown.
- Take test input back to VIH. Repeat steps 3 and 4 to test additional inputs.



[†]For the 'ALS527, P8 through P11 inputs must match the Q8 through Q11 inputs.

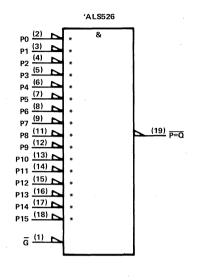
logic diagrams (positive logic)

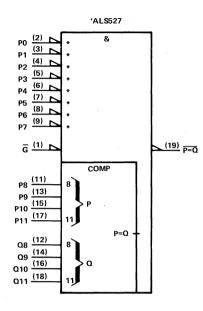


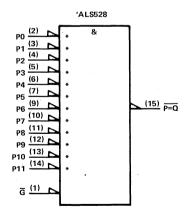




logic symbols†







[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

^{*}These inputs can be programmed to be active high. The asterisk is not a part of the symbol. For a correct symbol for the programmed device, delete the polarity symbol (

) at any input whose programming fuse has been blown.



Pin numbers shown are for DW, J, and N packages.

SN54ALS526, SN54ALS527, SN54ALS528 SN74ALS526, SN74ALS527, SN74ALS528 FUSE-PROGRAMMABLE IDENTITY COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7	7 V
Input voltage (see Note 1)	5.5	iν
Operating free-air temperature range: SN54ALS'	125	°C
SN74ALS' 0°CC t	o 70	°C
Storage temperature range65°C to	150	°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		s	SN54ALS'			SN74ALS'			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2		5.5	2		5.5	V	
VIL	Low-level input voltage			0.7			0.8	V	
Іон	High-level output current			- 1			- 2.6	mA	
lOL	Low-level output current			12			24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

2424	ACTED	TEST CONDU	TIONO	S	N54ALS	,	S	N74ALS	S'	UNIT
PARA	METER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		V _{CC} -	2		
∨он		$V_{CC} = 4.5 V,$	$I_{OH} = -1 \text{ mA}$	2.4	3					٧
į		$V_{CC} = 4.5 V,$	$l_{OH} = -2.6 \text{ mA}$				2.4	2.9		
VOL		$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.36	0.5	•
Ų		$V_{CC} = 5.5 V,$	$V_1 = 5.5 \text{ V}$			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
ΙL		VCC = 5.5, V,	V _{IL} = 0.4 V			-0.2			-0.2	mA
lo [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-130	- 30		- 130	mA
	'ALS526				16	27		16	27	
Icc	'ALS527	$V_{CC} = 5.5 \text{ V}$, All inputs	at 4.5 V		15	24		` 15	24	mA
	'AL\$528				13	21		13	21	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX				
			SN54	ALS'	SN74ALS'		
			MIN	MAX	MIN	MAX	
tpLH	P or Q	<u>P</u> =Q \	3	18	3	15	
tPHL	Poru	P≡u	2	15	2	12	ns
tPLH	ĪG	<u>P=Q</u>	2	18	2	15	
tpHL	G	r=u	2	15	2	12	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

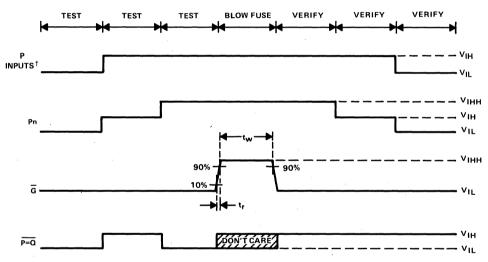


[‡]The output conditions have been chosen to produce a current that closely approximtes one half of the true short-circuit output current, I_{OS}.

SN54ALS526, SN54ALS527, SN54ALS528 SN74ALS526, SN74ALS527, SN74ALS528 FUSE-PROGRAMMABLE IDENTITY COMPARATORS

programming parameters

	PARAMETER		MIN	MAX	UNIT
VIH	High-level input voltage		2	5.5	V
VIL	Low-level input voltage			0.8	V
VIHH	Program-pulse input voltage		11.5	12.5	V
Vcc	Supply voltage		6.5	7.5	V
1	Program-pulse input current	Pn (G low)		10	mA
Iнн	Program-pulse input current	G		1.24	IIIA
		'ALS526		31	
Ісснн	Supply current with VIHH applied	'ALS527		29	mA
		'ALS528		26	
t _W	Pulse duration, program		10	50	μs
t _r	Rise time, program voltage			10	μS



Illustrated above is the following sequence:

NOTES: A. It is desired to program a particular input to recognize a high level input. With \overline{G} low and all P inputs † at V_{IL} , the output is low if no fuses are blown.

- B. With \overline{G} low all P inputs † at V_{IH} , the output is high unless all fuses are blown. C. The desired input is taken to V_{IHH} , the output goes low if the fuse is intact.
- D. G is pulsed to V_{IHH} blowing the desired fuse.
- E. After \overline{G} is low output will be high indicating that the fuse is blown.
- F. The programmed input returns to V_{IH}, the output is high unless all fuses have been blown.
 - G. All P inputs † are taken to V_{IL}, the output is high if a fuse has been blown.

 † For the 'ALS527, P8 through P11 inputs must match the Q8 through Q11 inputs.

FIGURE 1. PROGRAMMING WAVEFORMS



SN54ALS533, SN54AS533, SN74ALS533, SN74AS533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, APRIL 1982 - REVISED MAY 1986

- 8-Latches In a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

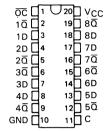
The eight latches of the 'ALS533 and 'AS533 are transparent D-type latches. While the enable (C) is high, the $\overline{\mathbb{Q}}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{\mathbb{Q}}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ALS533 and 'AS533 are functionally equivalent to the 'ALS373 and 'AS373 except for having inverted outputs.

A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

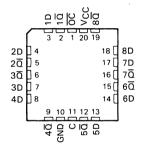
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS533 and SN54AS533 are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN74ALS533 and SN74AS533 are characterized for operation from 0 °C to 70 °C.

SN54ALS533, SN54AS533 . . . J PACKAGE SN74ALS533, SN74AS533 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS533, SN54AS533 . . . FK PACKAGE (TOP VIEW)



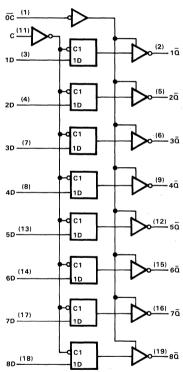
FUNCTION TABLE (EACH LATCH)

	INPUTS		OUTPUT
ŌĊ	ENABLE C	D	ā
L	Н	Н	L
L	Н	L	н
L	L	X	\bar{a}_0
Н	×	X	z

logic symbol[†]

80	OC (1) C (11) C (11) 10 (3) 20 (4) 30 (7) 40 (8) 50 (13) 60 (14) 70 (17)	EN C1 1 1D D	> \(\nabla \)	(2) (5) (6) (9) (12) (15) (16) (19)	20 30 40 50 60 70
				(19)	8₫

logic diagram (positive logic)



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS533, SN54AS53355 °C to 125 °C
SN74ALS533, SN74AS5330°C to 70°C
Storage temperature range



SN54ALS533, SN74ALS533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		5	SN54ALS533		SN74ALS533			
		MIN	NOM	MAX	MIN	NOM	MAX	רואט
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ГОН	High-level output current			- 1			-2.6	mA
lOL	Low-level output current			12			24	mA
t _w	Pulse duration, enable C high	15			15			ns
t _{su}	Setup time, data before enable C↓	15			15			ns
th	Hold time, data after enable C↓	7			7			ns
TA	Operating free-air temperature	- 55		125	0		70	00

PARAMETER	TEST CONDITIONS		SI	SN54ALS533			SN74ALS533		
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.5			-1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$		V _{CC} -	V _{CC} -2		V _{CC} -2			
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
Vai	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V_r$	IOL = 24 mA					0.35	0.5	V
lozн	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozl	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			- 20			- 20	μΑ
lı	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lН	$V_{CC} = 5.5 V$,	$V_i = 2.7 V$			20			20	μΑ
1/L	$V_{CC} = 5.5 V$,	$V_J = 0.4 V$			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		-112	mA
¹ CC		Outputs high		10	17		10	17	
	$V_{CC} = 5.5 V$	Outputs low		17	26		17	26	mA
		Outputs disabled		18.5	28		18.5	28	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 $^{\circ}$ C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$V_{CC}=4.5$ V to 5.5 V $C_L=50$ pF, R1 = 500 Ω , R2 = 500 Ω , $T_A=MIN$ to MAX				UNIT
			SN54.	ALS533	SN74	ALS533	
			MIN	MAX	MIN ·	MAX	
t _{PLH}	D	ā	4	24	4	19	ns
tPHL	В	<u> </u>	4	14	4	13	113
tPLH	С	Any Q	5	28	5	23	ns
tPHL	C	Ally Q	4	21	· 4	18	115
tPZH	oc	Any Q	4	19	4 .	17	ns
tPZL	96	Ally Q	4	20	4	· 18	115
[†] PHZ	ŌC	Any Q	2	12	2	10	ns
[†] PLZ	<u> </u>	Ally Q	3	22	3	16	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1

SN54AS533, SN74AS533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		S	N54AS5	,33	SI	N74AS5	,33	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-12			- 15	mA
loL	Low-level output current			32		-	48	mA
t _W	Pulse duration, enable C high	3			2			ns
t _{su}	Setup time, data before enable C↓	2			2			ns
th	Hold time, data after enable C↓	3		7	3			ns
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT O	CANDITIONS	SI	V54AS5	33	SN	74AS53	33	
PARAMETER	TEST C	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to 5.1}$	$5 \text{ V}, \text{ I}_{OH} = -2 \text{ mA}$	V _{CC} -	2		Vcc-	2		
Voн	$V_{CC} = 4.5 V$,	I _{OH} = -12 mA	2.4	3.2					V
	$V_{CC} = 4.5 V$,	$I_{OH} = -15 \text{ mA}$				2.4	3.3		}
Vo.	$V_{CC} = 4.5 V$,	I _{OL} = 32 mA		0.29	0.5				V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.34	0.5	ľ
lozh	$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ
IOZL	$V_{CC} = 5.5 V$,	V ₁ = 0.4 V			- 50			- 50	μΑ
lį .	$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA
ΉΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μА
1fL	$V_{CC} = 5.5 V$,	V _I = 0.5 V		-0.02	-0.5		-0.02	-0.5	mA
10 [‡]	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		-112	mA
		Outputs high		62	100		62	100	
'cc	$V_{CC} = 5.5 V$	Outputs low		64	100		64	100	mA
1		Outputs disabled		71	110		71	110	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)		V _{CC} = 4 C _L = 50 R1 = 500 R2 = 500 T _A = MII	pF,) Ω,) Ω, N to MAX		UNIT
				IAS533		AS533	
			MIN	MAX	MIN	MAX	
tPLH .	D	ā	4	10	4	7.5	ns
^t PHL	١	<u> </u>	4	8	4	7	113
^t PLH	С	Any Q	5	11	5	9	
^t PHL	C	Ally G	4.5	8.5	4.5	8	ns
^t PZH ·	ōc	Any Q	2	7.5	2	6.5	
tPZL	00	Ally C	4.5	10.5	4.5	9.5	ns
^t PHZ	ōc	Any Q	3	7.5	3	6.5	ns
^t PLZ		Ally d	3	8	3	7	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS534, SN54AS534, SN74ALS534, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 - REVISED MAY 1986

- 3-State Bus-Driving Inverting Outputs
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

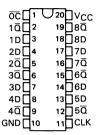
The eight flip-flops of the 'ALS534 and 'AS534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{\Omega}$ outputs will be set to the complement of the logic states that were set up at the D inputs. The 'ALS534 and 'AS534 are functionally equivalent to the 'ALS374 and 'AS374 except for having inverted outputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

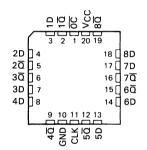
The output control does not affect the internal operatin of the flipflops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534 and SN54AS534 are characterized for operation over the full military temperature range of -55 $^{\circ}$ C to 125 $^{\circ}$ C. The SN74ALS534 and SN74AS534 are characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

SN54ALS534, SN54AS534 . . . J PACKAGE SN74ALS534, SN74AS534 . . . DW OR N PACKAGE (TOP VIEW)



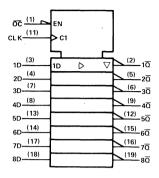
SN54ALS534, SN54AS534 . . . FK PACKAGE (TOP VIEW)



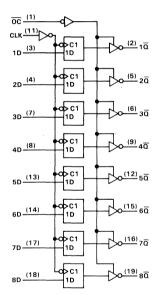
FUNCTION TABLE (EACH FLIP-FLOP)

	NPUTS	3	OUTPUT
ŌC	CLK	D	ā
L	†	Н	L
L	†	L	н
L	L	Х	\bar{a}_0
н	X	Х	z

logic symbol†



logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, Vcc		7 V
	output	
Operating free-air temperature ran	e: SN54ALS534, SN54AS534	to 125 °C
Sporating not in temperature	SN74ALS534, SN74AS534	
Storage temperature range		to 150 °C



SN54ALS534, SN74ALS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

				SN	54ALS5	34	SN	74ALS5	34	UNIT
			N	ΛIN	NOM	MAX	MIN	NOM	MAX	1 01111
VCC	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltag	9		2			2			V
VIL	Low-level input voltage)				0.7			0.8	V
Іон	High-level output curre	nt				- 1			- 2.6	mA
lOL	Low-level output curre	nt				12			24	mA
fclock	Clock frequency			0		30	0		35	MHz
+	Pulse duration	CLK high	16	6.5	***************************************		14			
t _w	ruise duration	CLK low	16	6.5			14			ns
t _{su}	Setup time, data befor	e CLK1		10			10			ns
th	Hold time, data after C	LK1		0			0			ns
TA	Operating free-air temperature		-	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMPLET	ONO	SI	154ALS	534	SN	74ALS5	34	
PARAMETER	TEST CONDITI	ONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			-1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		vcc-	2		
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
V _{OL}	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	\ \
lozh	V _{CC} = 5.5 V,	V ₀ = 2.7 V			20			20	μΑ
lozL	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			- 20			- 20	μΑ
I _I	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
liн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
CLK, OC	V 5.5.V	V 04V			-0.1			-0.1	^
lir D	$V_{CC} = 5.5 \text{ V},$	$V_I = 0.4 V$			-0.2			-0.2	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
		Outputs high		11	19		11	19	
cc	$V_{CC} = 5.5 V$	Outputs low		19	28		19	28	mA
	<u> </u>	Outputs disabled	1	10	31		20	31	1

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.$ $C_L = 50$ $R1 = 500$ $R2 = 500$ $T_A = MIN$	pF,) Ω,) Ω,		UNIT
			SN54	ALS534	SN74	ALS534	
			MIN	MAX	MIN	MAX	
f _{max}			30		35		MHz
t _{PLH}	CLK	Any $\overline{\overline{Q}}$	3	15	3	12	ns
tPHL	CLK	Any Q	5	18	5	16	115
^t PZH	ōc	Any Q	5	19	5	17	ns
tPZL		Ally Q	7	20	7	18] '''
t _{PHZ}	ōc	Any Q	2	12	2	10	ns
†PLZ_		Ally Q	2	16	2	14] '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS534, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

				SN	154AS5	34	SI	N74AS5	34	UNIT
			N	/IN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltag	e		2			2			V
VIL	Low-level input voltage	9				0.8			0.8	V
ЮН	High-level output curre	nt				- 12			- 15	mA
lOL	Low-level output curre	nt				32			48	mA
f _{clock}	Clock frequency			0		100	0		125	MHz
	Pulse duration	CLK high		5.5			4			
t _w	ruise duration	CLK low		5			3			ns
t _{su}	Setup time, data befor	e CLK↑		3			2			ns
th	Hold time, data after (CLK ↑		3			2			ns
TA	Operating free-air temp	perature		55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT	CONDITIONS	SI	V54AS5	34	SN	74AS53	34	UNIT
PARAMETER	TEST	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to 5}.$	5 V, $I_{OH} = -2 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
V _{OH}	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V
	$V_{CC} = 4.5 V,$	I _{OH} = -15 mA				2.4	3.3		1
	$V_{CC} = 4.5 V,$	I _{OL} = 32 mA		0.29	0.5				V
V _{OL}	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.34	0.5	ľ
lozh	$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ
lozL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 50			- 50	μΑ
I	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lн	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
OC, CLK	V 55.V				-0.5			-0.5	mA
IIL D	$V_{CC} = 5.5 \text{ V},$	$V_I = 0.4 V$			-3		***************************************	- 2	'''A
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
		Outputs high		77	120		77	120	
ICC mA	$V_{CC} = 5.5 V$	Outputs low		84	128		84	128	mA
		Outputs disabled		84	128		84	128	1

 $^{^{\}dagger}AII$ typical values are at VCC $\,=\,5$ V, $T_{\mbox{\scriptsize A}}\,=\,25\,^{o}\mbox{\scriptsize C}.$

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS534, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	FROM TO		$V_{CC} = 4$ $C_L = 50$ $R1 = 500$ $R2 = 500$ $T_A = Mir$	pF, Ο Ω, Ο Ω,		UNIT
			SN54	AS534	SN74	AS534	
			MIN	MAX	MIN	MAX	
f _{max}			100		125		MHz
t _{PLH}	CLK	Any Q	3	11	3	8	ns
^t PHL	CLK	Ally G	4	11.5	4	9	115
t _{PZH}	<u>oc</u>	Any Q	2	7	2	6	ns
tPZL	OC	Ally G	3	11	3	10	1 115
tPHZ	<u>oc</u>	Any Q	2	7	2	6	ns
tPLZ	00	Ally u	2	7	2	6	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS540, SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 - REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240/SN74ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

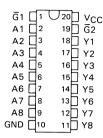
The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS540 provides inverted data and the 'ALS541 provides true data at the outputs.

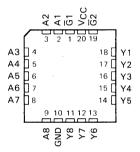
The -1 versions of the SN74ALS540 and SN74ALS541 parts are identical to the standard versions except that the recommended maximum I_{QL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS540 and SN54ALS541.

The SN54ALS540 and SN54ALS541 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0°C to 70°C.

SN54ALS540, SN54ALS541 . . . J PACKAGE SN74ALS540, SN74ALS541 . . . DW OR N PACKAGE (TOP VIEW)

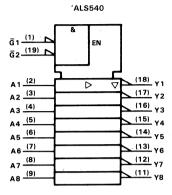


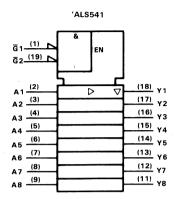
SN54ALS540, SN54ALS541 . . . FK PACKAGE (TOP VIEW)



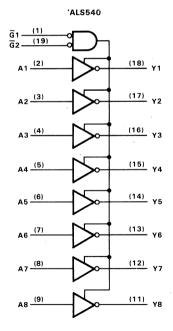


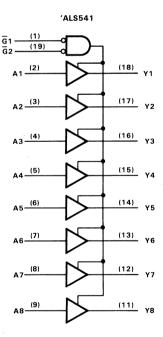
logic symbols[†]





logic diagrams (positive logic)





[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



SN54ALS540, SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS540, SN54ALS541
SN74ALS540, SN74ALS541
Storage temperature range65 °C to 150 °C

recommended operating conditions

		1	SN54ALS540 SN54ALS541			SN74ALS540 SN74ALS541		
		MIN	NOM	MAX	MIN	NOM	MAX	1
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 12			- 15	mA
1	Low-level output current			12			24	mA
lOL	Low-level output current						48 [†]	l IIIA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}$ The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS			N54ALS N54ALS		SN74ALS540 SN74ALS541			UNIT
	PARAMETER	TEST C	UNDITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNII
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		Vcc-	2		
Vон		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -3 mA	mA 2.4 3.2 2.4		3.2		l _v		
VOH		$V_{CC} = 4.5 \text{ V},$	t _{OH} = -12 mA	2						1 °
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2			
V _{OL}		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA¶					0.35	0.5	
lozh		$V_{CC} = 5.5 V,$	V _O = 2.7 V			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
Ч		$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
lн		$V_{CC} = 5.5 V$,	$V_{\parallel} = 2.7 V$			20			20	μΑ
l _{IL}		$V_{CC} = 5.5 \text{ V},$	$V_{\parallel} = 0.4 V$			-0.1			-0.1	mA
lo§		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30	,	- 112	mA
			Outputs high		5	10		5	10	
	'ALS540	$V_{CC} = 5.5 V$	Outputs low		13	22		13	22	mA
			Outputs disabled		11	19		11	19	
lcc			Outputs high		6	14		6	14	
	'ALS541	$V_{CC} = 5.5 V$	Outputs low		15	25		15	25	mA
			Outputs disabled		13.5	22		13.5	22	1

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



The 48 mA limit applies for the SN74ALS540-1 and SN74ALS541-1 only.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IQS. I I_{OL} = 48 mA for -1 versions.

SN54ALS540, SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

'ALS540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX				
			'ALS540	SN54ALS540		SN74ALS540]
			TYP	MIN	MAX	MIN	MAX	
t _{PLH}	Α	. v	7.5	2	14	2	12	
t _{PHL}		· •	5.6	2	11	2	9	ns
^t PZH	G	Y	9	5	18	5	15	
tPZL	, a	1 -	12.5	8	24	8	20	ns
tPHZ	Ğ		4	1	12	1	10	ns
^t PLZ	ū	'	7	2	14	2	12	115

'ALS541 switching characteristics (see Note 1)

PARAMETER	FROM TO (OUTPUT)		$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$	VC CL R1 R2	UNIT			
			'ALS541	SN54A	LS541	SN74ALS541]
			TYP	MIN	MAX	MIN	MAX	
[†] PLH	- A	V	8.7	4	. 17	4	14	
^t PHL	7 ^	Y .	7	2	12	2	10	ns
^t PZH	G		9	5	18	5	15	
t _{PZL}	7 '	T	12.5	8	24	8	20	ns
^t PHZ	- G	V	4	1	12	1	10	
tPLZ] '	r	7	2	14	2	12	ns

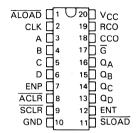
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS560A, SN54ALS561A, SN74ALS560A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- Carry Output for n-Bit Cascading
- Buffer-Type Outputs Drive Bus Lines Directly
- Choice of Asynchronous or Synchronous Load or Clear
- Internal Look-Ahead for Fast Cascading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS560A, SN54ALS561A . . . J PACKAGE SN74ALS560A, SN74ALS561A . . . DW OR N PACKAGE (TOP VIEW)

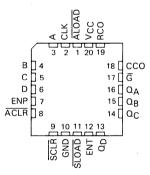


description

The 'ALS560A decade counters and 'ALS561A binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear (\$\overline{ACLR}\$) or Synchronous Clear (\$\overline{SCLR}\$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to Asynchronous Load (\$\overline{ALOAD}\$) or by the combination of a low level at Synchronous Load (\$\overline{SLOAD}\$) and a positive-going clock transition. The counting function is enabled only when Enable P (ENP), Enable T (ENT), \$\overline{ACLR}\$, \$\overline{ALOAD}\$, \$\overline{SCLR}\$, and \$\overline{SLOAD}\$ are all high.

SN54ALS560A, SN54ALS561A . . . FK PACKAGE (TOP VIEW)



A high level at the Output Enable (\overline{G}) forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of \overline{G} . ENT is fed forward to enable the Ripple Carry Output (RCO) to produce a high-level pulse while the count is maximum (9 or 15). The Clocked Carry Output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (both ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very-high-speed counting, RCO should be used for cascading since CCO does not become active until the clock returns to the low level.

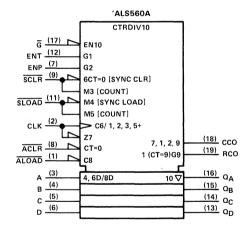
The SN54ALS560A and SN54ALS561A are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $\,^{\circ}$ C. The SN74ALS560A and SN74ALS561A are characterized for operation from 0 $\,^{\circ}$ C to 70 $\,^{\circ}$ C.

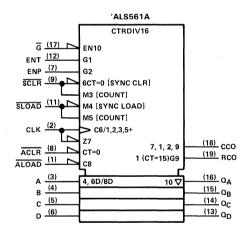
SN54ALS560A, SN54ALS561A, SN74ALS560A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

			OPERATION					
G	ACLR	ALOAD	SCLR	SLOAD	ENT	ENP	CLK	OPERATION
Н	X	X	Х	X	Х	Х	Х	Q Outputs Disabled
L	L	X	χX	X	X	X	X	Asynchronous Clear
L	Н	L	X	· X	X	X	Х	Asynchronous Load
L	н	Н	L	X	X	X	1	Synchronous Clear
L	Н	Н	Н	L	X	X	1	Synchronous Load
L	Н	Н	н	Н	н	н	1	Count
L	• н	н	н	н	L	X	X	Inhibit Counting
L	н	Н	Н	Н	X	L	X	Inhibit Counting

logic symbols†

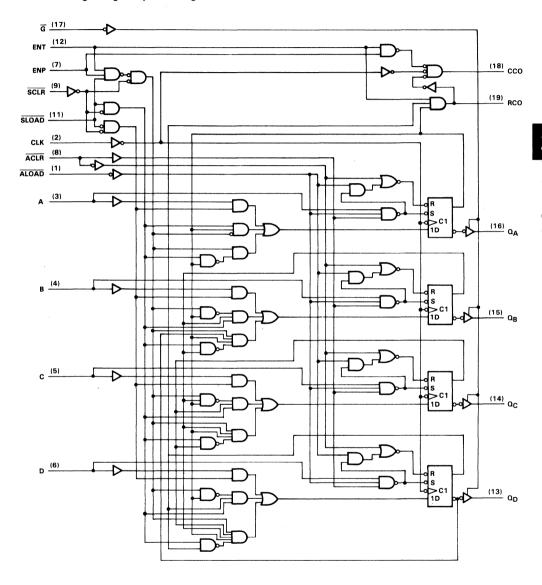




[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D. J. and N packages.



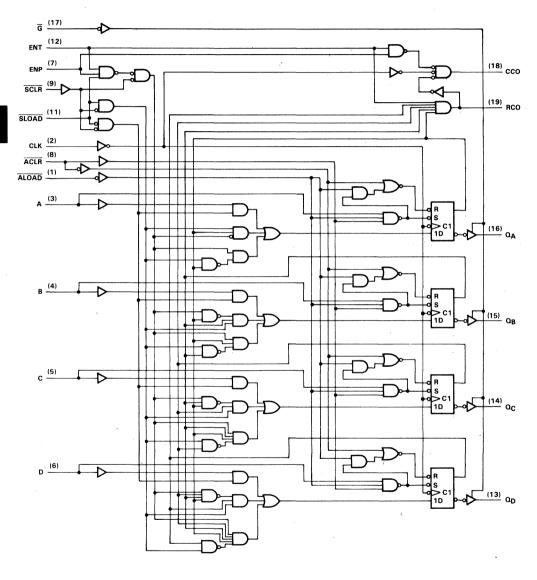
'ALS560A logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.



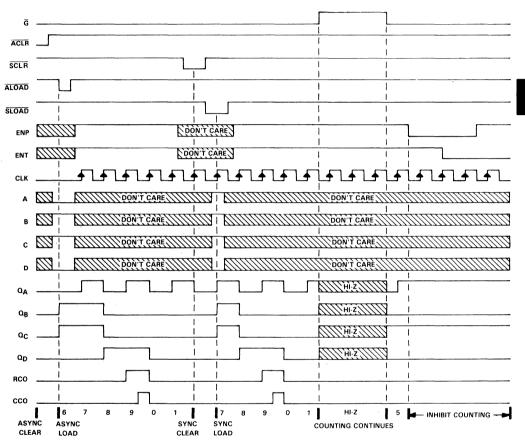
'ALS561A logic diagram (positive logic)



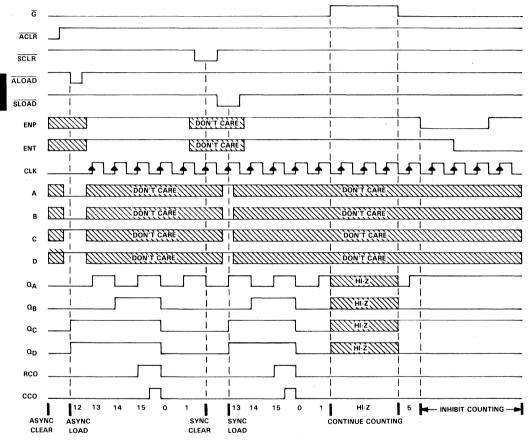
Pin numbers shown are for D, J, and N packages.



'ALS560A typical load, count, and inhibit sequences



'ALS561A typical load, count, and inhibit sequences



SN54ALS560A, SN54ALS561A, SN74ALS560A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54ALS560A, SN54ALS561A 55 °C to 125 °C
	SN74ALS560A, SN74ALS561A 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

				1	54ALS5 54ALS5			74ALS5		UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.7			0.8	V
	TR. L. L. L. L. L. L. L. L. L. L. L. L. L.	Q outputs	Q outputs			- 1			-2.6	mA
ЮН	High-level output current	CCO and R	CO			-0.4			-0.4	1117
1	Q outputs				12			24	mΑ	
lOL	Low-level output current	CCO and R	CCO and RCO			4			8	1117
	Clock frequency 'ALS560A			0		18	0		20	мн
fclock	Clock frequency	'ALS561A				25	0		30	IVIII
	Pulse duration	ACLR or Al	OAD low	20			15			
		'ALS560A	CLK high	27.5			25			
t_{W}		ALSSOUA	CLK low	27.5			25			ns
	(A) \$561	'ALS561A	CLK high	20			16.5			
		ALSSETA	CLK low	20			16.5			
		ENP, ENT	High	25			20			
		EINF, EINT	Low	25			20			
		Data at A,	B, C, D	25			20			
	Setup time before CLK†	SCLR	Low	21			15			ns
^t su	Setup time before CEK	JOER	High (inactive)	35			30			''3
		SLOAD	Low	20			15			
		SLOAD	High (inactive)	35			30			1
		ACLR or ALOAD inactive		10			10			
th	Hold time after CLK1 for dat	a, ENP, ENT, So	0			0			ns	
TA	Operating free-air temperatu	ire		- 55		125	0		70	°C

SN54ALS560A, SN54ALS561A, SN74ALS560A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SI	V54ALS	560A	SN	74ALS5	60A	
P/	ARAMETER	TEST CONDITION	ONS	SI	V54ALS	561A	SN	74ALS5	61A	UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		V _{CC} -	2		
VOH	Q outputs	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					V
	Q outputs	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	Q outputs	$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL	Q outputs	$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	_
VOL	CCO and RCO	$V_{CC} = 4.5 V$,	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	Ť
	CCO and neo	$V_{CC} = 4.5 V,$	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
^l ozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μΑ
I.	ENT and ENP	$V_{CC} = 5.5 V,$	V _I = 7 V			0.2			0.2	mA
h ·	Other inputs	VCC = 5.5 V,	V1 - 7 V			0.1			0.1] ""^
l	ENT and ENP	V _{CC} = 5.5 V,	V _I = 2.7 V			40			40	μΑ
ii.	Other inputs	VCC = 5.5 V,	V - 2.7 V			20			20	μΑ.
I _L		$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.2			-0.2	mA
lo [‡]	CCO and RCO	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 15		- 70	- 15		- 70	mA
10.	Q	vCC = 9.9 v,	ν ₀ = 2.25 ν	- 30		-112	- 30		-112	IIIA
			Outputs high		17	27		17	27	
ICC .	$V_{CC} = 5.5 V$	Outputs low		21	33		21	33	mA	
			Outputs disabled		22	36		22	36	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 o C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS560A, SN54ALS561A, SN74ALS560A, SN74ALS561A SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_A = \text{MIN to MAX} \\ \\ \hline SN54ALS560A \\ SN54ALS561A \\ \\ \hline \end{array}$					
	·/ A1	25604	MIN 18	MAX	MIN 20	MAX		
f _{max}	'ALS560A 'ALS561A		25		30		MHz	
tPLH		T	4	15	4	12		
tPHL	CLK Any Q	5	21	5	18	ns		
tPLH			9	35	9	29		
tPHL	CLK	RCO	8	29	8	24	ns	
tPLH			8	31	8	26	ļ	
tPHL	CLK	CCO	5	20	5	16	ns	
tPLH	ĀLOAD		10	38	10	35		
tPHL		Any Q	7	27	7	23	ns	
t _{PLH}			15	50	15	40		
†PHL	ALOAD	RCO	12	35	12	30	ns	
[†] PLH			25	65	25	55		
†PHL	ALOAD	CCO	12	42	12	33	ns	
^t PLH	A, B, C,		8	35	8	30		
^t PHL	or D	Any Q	7	27	7	22	ns	
^t PLH		500	5	20	5	16		
[†] PHL	ENT	RCO	4	18	4	14	ns	
[†] PLH	ENIT	000	12	35	12	32		
tPHL	ENT	cco	4	15	4	12	ns	
t _{PLH}	END	cco	5	22	5	18		
^t PHL	ENP	((0)	4	14	4	12	ns	
[†] PHL	ACLR	Any Q	7	28	7	22	ns	
^t PZH	G	Any Q	5	24	5	19	no	
[†] PZL		Any U	8	28	8	23	_ ne	
tPHZ	Ē	5	. 2	12	2	10	nc	
[†] PLZ	1 6	Any Q	4	20	4	15	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS563A, SN74ALS563A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus Structured Pinout
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

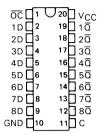
The eight latches are transparent D-type latches. When the enable (C) is high the \overline{Q} outputs will follow the complements of data (D) inputs. When the enable is taken low the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

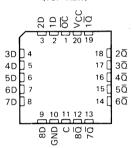
The output control (\overline{OC}) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS563A is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS563A is characterized for operation from 0 °C to 70 °C.

SN54ALS563A . . . J PACKAGE SN74ALS563A . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS563A . . . FK PACKAGE (TOP VIEW)

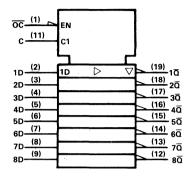


FUNCTION TABLE

1	NPUT	3	OUTPUT				
E	NABL	ā					
ОC	С	D	۱ "				
L	Н	Н	L				
L	Н	L	н				
L	L	X	σ_0				
Н	X	Х	z				

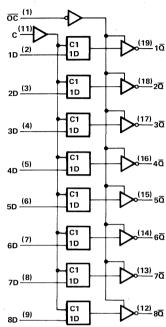


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC			 	7 V
Input voltage				
Voltage applied to a dis	abled 3-state outpu	ıt	 	5.5 V
Operating free-air tempe	erature range: SN5	4ALS563A	 	-55°C to 125°C
	SN7	4ALS563A	 	0°C to 70°C
Storage temperature rar	nge		 	-65°C to 150°C

recommended operating conditions

9		SN	SN54ALS563A			SN74ALS563A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			- 1			-2.6	mA	
lOL	Low-level output current			12			24	mA	
t _w	Pulse duration, enable C high	15			15			ns	
t _{su}	Setup time, data before enable C1	10			10			ns	
th	Hold time, data after enable C↓	10			10			ns	
TA	Operating free-air temperature	- 55		125	0		70	°C	



SN54ALS563A, SN74ALS563A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted

PARAMETER	TEST CO	SN	54ALS56	63A	SN	74ALS56	3A	UNIT	
PARAMETER	1231 CO	NUTTONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	OWII
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
Voн	$V_{CC} = 4.5 V$,	$I_{OL} = -1 \text{ mA}$	2.4	3.3					\ \
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		1
Voi	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	1
IOZH	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
IOZL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20			-20	μΑ
l)	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
IIH	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
Iμ	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			- 0.1	mA
10 [‡]	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		- 112	30		- 112	mA
		Outputs high		10	17		10	17	
^I cc	$V_{CC} = 5.5 V$	Outputs low		16	26		16	26	mA
		Outputs disabled		17	29		17	29	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$ $ALS563A$ TYP	$\begin{array}{c} V_{CC} = 4.5 \text{ V} \\ C_L = 50 \text{ pF}, \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_A = \text{MIN to} \\ \text{SN54ALS563A} \\ \text{MIN} \qquad \text{MAX} \end{array}$		мах	ALS563A MAX	UNIT
tpLH	D	ā	10	3	21	3	18	ns
^t PHL] [8	3	15	3	14	115
tPLH	С	ā	8	8	29	8	22	ns
tPHL	1 ~	<u> </u>	14	8	22	8	21	115
tPZH	ос	Īa	8	4	21	4	18	ne
^t PZL		u	10	4	21	4	18	ns
^t PHZ	ос	ō	5	2	12	2	10	ns
[†] PLZ		9	7	3	18	3	15	113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los-

SN54ALS564A, SN74ALS564A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 - REVISED MAY 1986

- 3-State Buffer-Type Inverting Outputs Drive **Bus-Lines Directly**
- **Rus-Structured Pinout**
- **Buffered Control Inputs**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature inverting three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS564A is characterized for operation over the full military temperature range of -55 °C to 125°C. The SN74ALS564A is characterized for operation from 0°C to 70°C.

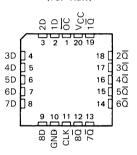
FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
ŌĊ	CLK	D	₫
L	1	Н	L
L	1	L	H
L	L	X	\overline{a}_0
Н	Х	Х	Z

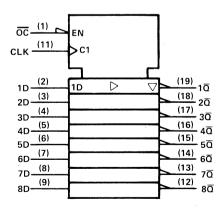
SN54ALS564A . . . J PACKAGE SN74ALS564A . . . DW OR N PACKAGE (TOP VIEW)

oc □	1	U 20	Vcc
1D [2	19	1 <u>0</u>
2D 🗌	3	18	$2\overline{Q}$
3D 🗌	4	17	3 <u>0</u>
4D 🗌	5	16	4 <u>0</u>
5D 🗌	6	15	5 <u>0</u>
6D [7	14	6 <u>0</u>
7D 🗌	8	13	7 <u>0</u>
8D 🗌	9	12	8 <u>0</u>
GND [10	11	CLK

SN54ALS564A . . . FK PACKAGE (TOP VIEW)



logic symbol†

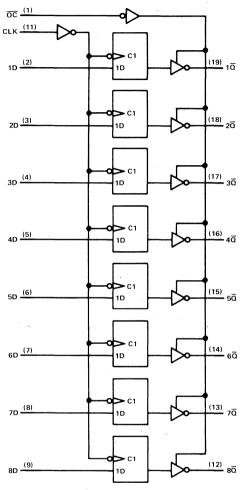


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.



logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS564A
SN74ALS564A 0 °C to 70 °C
Storage temperature range – 65 °C to 150 °C



SN54ALS564A, SN74ALS564A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

				SN	54ALS5	64A	SN	74ALS5	64A	UNIT	
			1	MIN	NOM	MAX	MIN	NOM	MAX	ONII	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage			2			2			٧	
VIL	Low-level input voltage				0.7			0.8	V		
ЮН	High-level output current					1			-2.6	mA	
loL	Low-level output current					12			24	mA	
fclock	Clock frequency			0		25	0		30	MHz	
	Pulse duration	CLK high		16.5			14				
t _w	r dise duration	CLK low		16.5			14			ns	
t _{su}	Setup time, data before CLK1		15.			15			ns		
th	Hold time, data after CLK1			4			0			ns	
ТА	Operating free-air temper	erature		- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	54ALS	64A	SN	74ALS	64A	UNIT
PANAMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc	2		Vcc	2		
∨он	V _{CC} = 4.5 V,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					\ \
	V _{CC} = 4.5 V,	I _{OH} . = -2.6 mA				2.4	3.2		1
V	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	1 °
lozh	V _{CC} = 5.5 V,	V _{O.} ≠ 2.7 V			20			20	μΑ
^I OZL	V _{CC} = 5.5 V,	V _O = 0.4 V			- 20			- 20	μΑ
l _l	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
IIH	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.2			-0.2	mA
lo‡	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
		Outputs high		10	18		10	18	,
^I cc	$V_{CC} = 5.5 V$	Outputs low		15	24		15	24	mΑ
		Outputs disabled		16	30		16	30	1

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{\circ}C_{\cdot}$

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS564A, SN74ALS564A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ} C$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to MAX}$				UNIT
			'ALS564A	SN54ALS564A		SN74ALS564A		
			TYP	MIN	MAX	MIN	MAX	
f _{max}			50	25		30		MHz
tPLH	CLK	Any $\overline{\overline{Q}}$	9	4	15	4	14	ns
^t PHL	CLK	Ally Q	9	4	15	4	14	115
^t PZH	ōc	Any Q	11	4	21	4	18	ns
tpZL	OC	Ally Q	11	4	21	4	18	lis
t _{PHZ}	- <u>oc</u>	Any Q	6	2	12	2	10	no.
tPLZ	00	Ally U	. 8	3	17	3	15	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS568A, SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

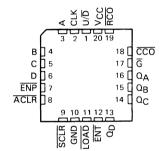
D2661, APRIL 1982-REVISED MAY 1986

- 3-State Q Outputs Drive Bus Lines Directly
- Counter Operation Independent of 3-State Output
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Also Provided
- Fully Cascadable
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS568A, SN54ALS569A . . . J PACKAGE SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE (TOP VIEW)

U/D 🗆	1	U20		Vcc
CLK 🗌	2	19		RCO
A 🗌	3	18		CCO
В[4	17		Ğ
c[5	16		Q_A
D□	6	15		σ_{B}
ENP [7	14		σ_{C}
ACLR [8	13		σ_{D}
SCLR	9	12		ENT
GND□	10	11	П	LOAD

SN54ALS568A, SN54ALS569A . . . FK PACKAGE (TOP VIEW)



description

The 'ALS568A decade counters and 'ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either Asynchronous Clear (\overline{ACLR}) or Synchronous Clear (\overline{SCLR}) . Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding Load (\overline{LOAD}) low during a positive-going clock transition. The counting function is enabled only when Enable P (\overline{ENP}) and Enable T (\overline{ENT}) are low and \overline{ACLR} , \overline{SCLR} , and \overline{LOAD} are high. The Up/Down (U/\overline{D}) input controls the direction of the count. These counters count up when U/\overline{D} is high and count down when U/\overline{D} is low.

A high level at the Output Enable (\overline{G}) forces the Ω outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of of \overline{G} . \overline{ENT} is fed forward to enable the Ripple Carry Output (\overline{RCO}) to produce a low-level pulse while the count is zero (all Ω outputs low) when counting down or maximum (9 or 15) when counting up. The Clocked Carry Output (\overline{CCO}) produces a low level pulse for a duration equal to that of the low level of the clock when \overline{RCO} is low and the counter is enabled (both \overline{ENP} and \overline{ENT} are low); otherwise, \overline{CCO} is high. \overline{CCO} does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting \overline{RCO} or \overline{CCO} of the first counter to \overline{ENT} of the next counter. However, for very-high-speed counting, \overline{RCO} should be used for cascading since \overline{CCO} does not become active until the clock returns to the low level.

The SN54ALS568A and SN54ALS569A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS568A and SN74ALS569A are characterized for operation from 0°C to 70°C.

SN54ALS568A, SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

FI	IN	CT	JOI.	N	TA	RI	F

			OPERATION					
Ğ	ACLR	SCLR	LOAD	ENT	ENP	U/D	CLK	OPERATION
Н	Х	X	X	Х	Х	X	X	Q Outputs Disabled
Ł	L	X	X	X	X	X	X	Asynchronous Clear
L	Н	L	X	X	X	X	†	Synchronous Clear
L	Н	H	L	X	X	X	†	Load
L	н	н	Н	L	L	н	, †	Count Up
L	H	Н	Н	L	L	Ĺ	†	Count Down
L	Н	Н	Н	н	X	X	X	Inhibit Count
L	Н	Н	н	Х	Н	Х	×	Inhibit Count

logic symbols†

ENP (7)

SCLR (9)

LOAD (11)

G8

5CT=0

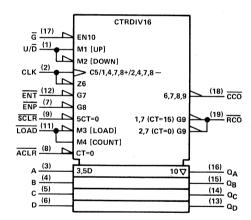
CTRDIV10 G (17) EN10 U/D (1) M1 [UP] M2 [DOWN] CLK (2) **>** C5/1,4,7,8+/2,4,7,8 -ENT (12) G7

'ALS568A

(1<u>8)</u> CCO 6,7,8,9 (19) RCO 1,7 (CT=9) G9 2.7 (CT=0) G9 M3 [LOAD]

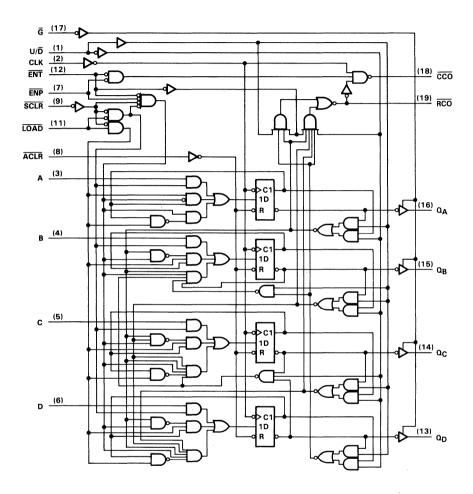
M4 [COUNT] ACLR (8) CT=0 A (3) (16) 10 ▽ ·QΑ 3,5D B (4) (15) αB c (5) (14) α_{C} (13) (6) QD

'ALS569A



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

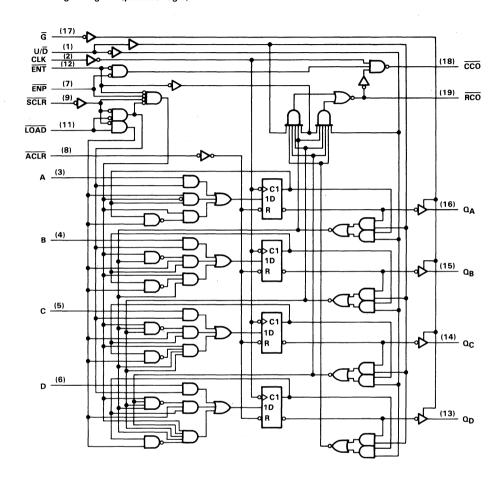
'ALS568A logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

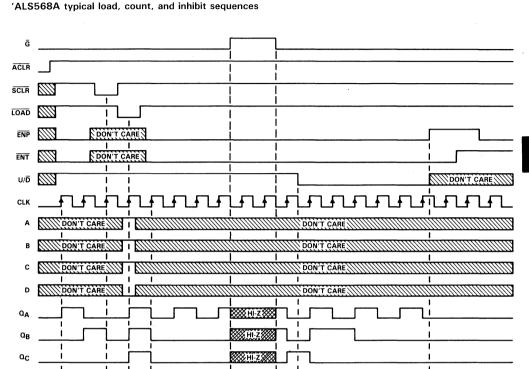


'ALS569A logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.





3

COUNT DOWN

Q_D
RCO

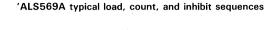
ASYNC CLEAR COUNT

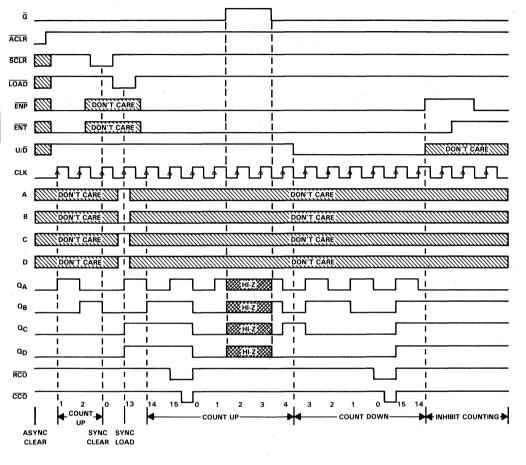
SYNC SYNC

CLEAR LOAD



INHIBIT COUNTING





SN54ALS568A, SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS568A, SN54ALS569A
SN74ALS568A, SN74ALS569A
Storage temperature range – 65 °C to 150 °C

recommended operating conditions

					54ALS5			174ALS!		
				MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltge					0.7			0.8	С
1	High-level output current	Q outputs				- 1			-2.6	mA
Іон	High-level output current	CCO and R	CO			-0.4			-0.4	mA
1	Low-level output current	Q outputs				12			24	^
lOL	Low-level output current	CCO and R	CO			4			8	mA
4	Clock frequency	'ALS568A		0		18	0		20	MHz
fclock	Clock frequency	'ALS569A		0		22	0		30	IVIMZ
	Pulse duration	ALCR or LC	DAD low	20			15			
		'ALS568A	CLK high	27.5			25			ns
t_{W}			CLK low	27.5			25			
t _w		'ALS569A	CLK high	20			16.5			
			CLK low	20			16.5			
		Data at A,	B, C, D	25			20			
		ENP, ENT	High	35			30			1
		EINF, EINT	Low	25			20			
		SCLR	Low	20			15			
t _{su}	Setup time before CLK ↑	SCLN	High (inactive)	35			30			ns
		LOAD	Low	20			15			
		LOAD	High (inactive)	35			30			
		U/D		35			30			
		ACLR inact	ive	10			10			
th	Hold time after CLK↑ for any	input		0			0			ns
TA	Operating free-air temperatu	re		- 55		125	0		70	°C



SN54ALS568A, SN54ALS569A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETER	TEST CONDITIO	INC	1	N54ALS			74ALS5		UNIT
'A"	AWIETEN	TEST CONDITIO	, N.S		TYP [†]	MAX	MIN	TYP [†]	MAX	ONIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			-1.5	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V, I _{OH} = -0.4 mA	Vcc-	2		Vcc-	2		
Vou	V _{OH} Q outputs	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3	***************************************				V
VOH		$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		i
	Q outputs	$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL	a outputs	$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	_v
VOL.	CCO and RCO	$V_{CC} = 4.5 V$,	$I_{OH} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
	000 4114 1100	$V_{CC} = 4.5 V$,	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μA
l _l		$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
ΙΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
կլ		$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.2			-0.2	mA
lo‡	CCO and RCO	V _{CC} = 5.5 V,	V _O = 2.25 V	- 15		- 70	- 15		– 70	mA
	Q outputs	V((= 0.5 V)	VU = 2:23 V	- 30		-112	- 30		- 112] ""A
			Outputs high		16	26		16	26	6
lcc		$V_{CC} = 5.5 V$	Outputs low		20	32		20	32	mA
			Outputs disabled		20	32		20	32	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS568A, SN54ALS569A, SN74ALS568A, SN74ALS569A SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	SN54A SN54A	$\begin{array}{c} V_{CC} = 4.5 \text{ N} \\ C_{L} = 50 \text{ pF,} \\ R1 = 500 \Omega \\ R2 = 500 \Omega \\ \hline T_{A} = \text{MIN to} \\ \text{SN54ALS568A} \\ \text{SN54ALS569A} \\ \hline \text{MIN} \qquad \text{MAX} \\ \end{array}$		o MAX SN74ALS568A SN74ALS569A	
	'ΔΙ S	 568A	18	IVIAA	MIN 20	MAX	
f _{max}		569A	22		30		MHz
tPLH			4	21	4	13	
t _{PHL}	CLK	Any Q	7	19	7	16	ns
^t PLH	CLK	RCO 12		37	12	28	
[†] PHL	CLK	l RCO	10	28	10	19	ns
^t PLH	CLK	cco	5	17	5	13	ns
^t PHL	CLK	660	6	30	6	25	113
^t PLH	U/D	RCO	9	31	9	23	ns
^t PHL	0,5	nco	9	33	9	19] "
^t PLH	ENT	RCO	6	21	6	15	ns
^t PHL		1100	4	20	4	13	110
^t PLH	ENT	cco	5	18	5	13	ns
^t PHL	EIV1		9	32	9	23	110
^t PLH	ENP	cco	4	18	4	12	ns
^t PHL			5	18	5	14	l lis
^t PHL	ACLR	Any Q	9	25	9	20	ns
^t PZH	G	Any Q	6	23	6	18	ns
tPZL	-	, =	6	29	6	24	
^t PHZ	G	Any Q	1	12	1	10	ns
^t PLZ		1, 2	3	29	3	13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS573B, SN54ALS580A, SN54AS573, SN54AS580 SN74ALS573B, SN74ALS580A, SN74AS573, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- **Bus-Structured Pinout**
- Choice of True or Inverting Logic 'ALS573B, 'AS573 True Outputs 'ALS580A. 'AS580 **Inverting Outputs**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

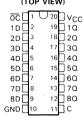
The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q or \overline{Q}) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a highimpedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

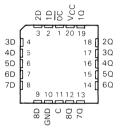
The output control (OC) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

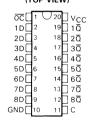
SN54ALS573B, SN54AS573 . . . J PACKAGE SN74ALS573B, SN74AS573 . . . DW OR N PACKAGE (TOP VIEW)



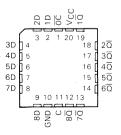
SN54ALS573B, SN54AS573 . . . FK PACKAGE (TOP VIEW)



SN54ALS580A, SN54AS580 . . . J PACKAGE SN74ALS580A, SN74AS580 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS580A, SN54AS580 . . . FK PACKAGE (TOP VIEW)





FUNCTION TABLES

'ALS573B, 'AS573 (EACH LATCH)

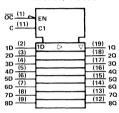
IN	PUTS	3	ОИТРИТ
ΕN	IABL		
оc	С	D	a
L	Н	Н	Н
L	Н	L	L
L	L	X	σO
Н	X	Х	Z

'ALS580A, 'AS580 (EACH LATCH)

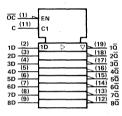
INI	PUTS		ОИТРИТ
EN	ABLE	<u>α</u>	
<u>oc</u>	С	D	u
L	Н	Н	L
L	Н	L	Н
L	L	Х	\overline{a}_0
Н	Х	Х	Z

logic symbols†

'ALS573B, 'AS573



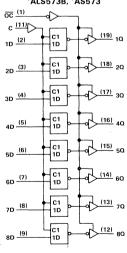
'ALS580A, 'AS580



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'ALS573B, 'AS573



OC (1) ENABLE C (11) (<u>19)</u> 1Q C1 1D 1D (2) ~<u>(18)</u> 2Q C1 2D (3) 1D (<u>17)</u> 3Q C1 3D (4) (16) 4Q 4D (5) (15) 5Q 5D (6) 10 (14) 6Q 6D (7) 10 <u>(13)</u> 7Q C1 7D (8) 10

1D

8D (9)

(12) 8Q

'ALS580A, 'AS580

Pin numbers shown are for DW, J, and N packages.

SN54ALS573B, SN54ALS580A, SN74ALS573B, SN74ALS580A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	. 7	V
Input voltage	. 7	V
Voltage applied to a disabled 3-state output	5.5	V
Operating free-air temperature range; SN54ALS573B, SN54ALS580A55°C to 1	125	٥С
SN74ALS573B, SN74ALS580A 0°C to	70	°C
Storage temperature range – 65 °C to 1	150	°C

recommended operating conditions

		*	SN	54ALS5	73B	SI	ļ.		
1			SN54ALS580A			SN74ALS580A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	. 5	5.5	V
V _{IH}	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Іон	High-level output current			- 1			-2.6	mA	
lOL	Low-level output current				12			-24	mA
	Pulse duration, enable C high	'ALS573B	10			10			
t _w	Fulse duration, enable C high	'ALS580A	15			15			ns
t _{su}	Setup time, data before enable C↓		10			10			ns
+.	Hold time, data after enable C↓	'ALS573B	7			7			200
th	noid time, data after enable C1	'ALS580A	10			10			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	TEST CONDITIONS		I54ALS I54ALS!			74ALS5 74ALS5		UNIT	
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	x	
V_{IK}		$V_{CC} = 4.5 V,$	$I_1 = -18 \text{ mA}$	1		- 1.2			-1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		Vcc-	2			
νон		$V_{CC} = 4.5 V,$	$I_{OH} = -1 \text{ mA}$	2.4	3.3] v		
		$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2]	
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V	
		$V_{CC} = 4.5 V,$	$I_{OL} = 24 \text{ mA}$					0.35	0.5] _ `	
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ	
lozL		V _{CC} = 5.5 V,	$V_0 = 0.4 V$			- 20			- 20	μΑ	
11		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
ΊΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ	
ΊL		$V_{CC} = 5.5 V,$	$V_l = 0.4 V$			-0.1			-0.1	mA	
10 [‡]		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA	
			Outputs high		10	17		10	17		
	'ALS573B		Outputs low		15	24		15	24]	
		V _{CC} = 5.5 V	Outputs disabled		16	27		16	27	mA	
cc	'ALS580A	VCC = 5.5 V	Outputs high		10	17		10	17	I IIIA	
		,	Outputs low		16	26		16	26	1	
			Outputs disabled		17	29		17	29]	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54ALS573B, SN54ALS580A, SN74ALS573B, SN74ALS580A OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

'ALS573B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$ 'ALS573B TYP		$V_{CC} = 4.5$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega$ $T_A = MIN \text{ to}$ $ALS573B$ MAX	MAX	V, ALS573B MAX	UNIT
^t PLH	D	Q	7	2	15	2	14	
^t PHL	1 "	u	7	2	15	2	14	ns
tPLH .	С	Q	12	8	25	8	20	20
^t PHL		u u	12	8	20	8	. 19	ns
tPZH	ōc	Ω	9	4	21	4	18	
tPZL	00	. u	11	4	21	4	18	ns
^t PHZ	ōc	Q	5	2	12	2	10	ns
^t PLZ			7	3	18	3	15	115

'ALS580A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$ 'ALS580A TYP	C R R T	CC = 4.5 L = 50 pF, 1 = 500 Ω 2 = 500 Ω A = MIN to LS580A	, , o MAX	US580A MAX	UNIT
^t PLH	D	ā	10	3	21	3	18	ns
tPHL temperature] "	Q.	8	3	15	3	14] "15
t _{PLH}	С	ā	8	8	29	8	22	
^t PHL] [u	14	8	22	8	21	ns
^t PZH	ōc	ā	8	4	21	4	18	
^t PZL] "	ū.	10	4	21	4	18	ns
^t PHZ	ōc	ā	5	2	12	2	10	ns
tPLZ		ū	7	3	18	3	15] "15

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS573, SN54AS580, SN74AS573, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	' V
Input voltage	' V
Voltage applied to a disabled 3-state output	V
Operating free-air temperature range: SN54AS573, SN54AS580	٥C
SN74AS573, SN74AS580 0°C to 70	°C
Storage temperature range65°C to 150	٥C

recommended operating conditions

			SN	154AS57	'3	SN	74AS57	'3	
			SN	SN54AS580			74AS58	30	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				-12			-15	mA
lOL	Low-level output current				32			- 48	mA
	Bules duration analys C high	'AS573	5.5			4.5			
t _w	Pulse duration, enable C high	'AS580	3			2			ns
t _{su}	Setup time, data before enable C↓		2			2			ns
th	Hold time, data after enable C↓		3			3			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIO	TEST CONDITIONS			73 80	SN74AS573 SN74AS580			UNIT	
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
v_{iK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2			
۷он		$V_{CC} = 4.5 V,$	I _{OH} = -12 mA	2.4	3.2] v	
		V _{CC} = 4.5 V,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.3			
V _{OL}		V _{CC} = 4.5 V,	I _{OL} = 32 mA		0.28	0.5				V	
		$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.33	0.5	1 °	
lozh		$V_{CC} = 5.5 V,$	V _O = 2.7 V			50			50	μΑ	
lozL		V _{CC} = 5.5 V,	$V_0 = 0.4 V$,			- 50			- 50	μΑ	
Ч		V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA	
ΊΗ		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ	
ΙΙL		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA	
lo‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	-30		-112	mA	
			Outputs high		56	93		56	93		
	'AS573	1	Outputs low		55	90		55	90		
		V F F V	Outputs disabled		65	106		65	106	mA	
lcc		V _{CC} = 5.5 V	Outputs high		62	100		62	100		
	'AS580	'AS580			65	106		65	106	7	
			Outputs disabled		71	115		71	115		

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS573, SN54AS580, SN74AS573, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

'AS573 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX SN54AS573 SN74AS573			UNIT	
			MIN	MAX	MIN	MAX	
tPLH			3	9	3	6	
tPHL	D	Q	3	7	3	6	ns
tPLH	0		6	14	6	11.5	
tPHL	С	Q	4	9	4	7.5	ns
tPZH	ŌC	Q	2	8	2	6.5	
t _{PZL}	00.		4	11	4	9.5	ns
t _{PHZ}	ōc	Q	2	8	2	6.5	ns
[†] PLZ	36	1	2	8	2	7	1115

'AS580 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS580 = SN74AS580$				
			SN54	AS580	SN74			
			MIN	MAX	MIN	MAX	}	
^t PLH	D	ū	3	10	3	7.5		
^t PHL	j	ų d	3	7.5	3	7	ns	
tPLH	C	ā	5	12	5	9		
tPHL	· ·	4	4	8.5	4	8	ns	
^t PZH	ŌC	ā	2	7.5	2	6.5		
^t PZL			4	10.5	4	9.5	ns	
t _{PHZ}	ŌĊ	ā	2	7.5	2	6.5	ns.	
tPLZ		<u> </u>	2	8	2	7	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS574A, SN54ALS575A, SN54AS574, SN54AS575 SN74ALS574A, SN74ALS575A, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, JUNE 1982 - REVISED MAY 1986

- 3-State Buffer-Type Noninverting Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- 'ALS575A and 'AS575 Have Synchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. The 'ALS575A and 'AS575 $\underline{\text{may}}$ be synchronously cleared by taking the $\overline{\text{CLR}}$ input low.

The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS' and SN74AS' devices are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLES

'ALS574A, 'AS574 (EACH FLIP-FLOP)

11	NPUT	S	OUTPUT
0C	CLK	D	Q
L	1	Н	Н
L	†	L	L
L	L	Х	a_0
н	Х	Χ	Z

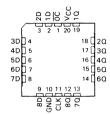
'ALS575A, 'AS575 (EACH FLIP-FLOP)

	INP	UTS		OUTPUT
ŌĊ	CLR	CLK	D	a
L	L	1	Х	L
L	Н	1	Н	н
L	Н	†	L	L
L	Н	L	Х	a_0
н	X	X	Х	z

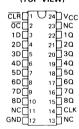
SN54ALS574A, SN54AS574 . . . J PACKAGE SN74ALS574A, SN74AS574 . . . DW OR N PACKAGE (TOP VIEW)



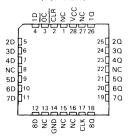
SN54ALS574A, SN54AS574 . . . FK PACKAGE



SN54ALS575A, SN54AS575...JT PACKAGE SN74ALS575A, SN74AS575...DW OR NT PACKAGE (TOP VIEW)



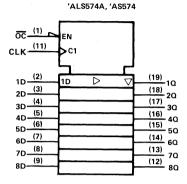
SN54ALS575A, SN54AS575 . . . FK PACKAGE SN74ALS575A, SN74AS575 . . . FN PACKAGE



NC-No internal connection



logic symbols†

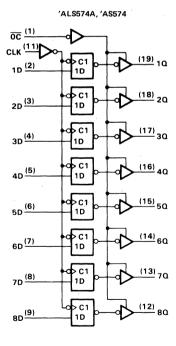


'ALS575A, 'AS575

OC (2) CLK (14) CLR (1)	EN > C1 1R	
1D (3) 2D (4) 3D (5) 4D (6) 5D (7) 6D (8) 7D (10)	1D D 🗸	(22) 10 (21) 20 (20) 30 (19) 40 (18) 50 (17) 60 (16) 70 (15) 80

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



Pin numbers shown are for DW, J, and N packages.

'ALS575A, 'AS575 OC (2) CLK (14) CLR (1) (22) 10 C1 1D (3) (21) 20 2D (4) (<u>20)</u> 3Q 3D (5) 1 D (1<u>9)</u> 40 4D (6) 1D (1<u>8)</u> 5Q > C 1 5D (7) (<u>17)</u> 60 6D (8) (1<u>6)</u> 70 C1 7D (9) 1D (15) 8Q > C1 8D (10) 1D

Pin numbers shown are for DW, JT, and NT packages.



SN54ALS574A, SN54ALS575A, SN74ALS574A, SN74ALS575A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54ALS574A, SN54ALS575A 55°C to 125°C
SN74ALS574A, SN74ALS575A 0°C to 70°C
Storage temperature range 65 °C to 150 °C

recommended operating conditions

			SN54ALS57 SN54ALS57							
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	. 5.5	V	
VIH	High-level input voltage					2			V	
VIL	Low-level input voltage				0.7			0.8	V	
loн	High-level output current			- 1			- 2.6	mA		
lOL	Low-level output current				12			24	mA	
f	Clock frequency	'ALS574A	0		28	0		35	MHz	
^f clock		'ALS575A	0		25	0		30		
	Pulse duration	'ALS574A CLK high or low	16.5			14				
t _w	ruise duration	'ALS575A CLK high or low	20			16.5			ns	
•	Setup time	Data	15			15				
t _{su}	before CLK↑	'ALS575A CLR	15			15			ns	
+.	Hold time	Data	4			0				
th	after CLK!	'ALS575A CLR	Ω			0			ns	
TA	Operating free-air temperat	ure	55		125	0		70	°C	

SN54ALS574A, SN54ALS575A, SN74ALS574A, SN74ALS575A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				SI	N54ALS	574A	SN	174ALS	574A	
PAR	AMETER	TEST CONDITION	ONS	SI	N54ALS	575A	SN	174ALS!	575A	UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	1
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -	2		V _{CC} -	2		
∨он	,	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4 3.3] v		
		$V_{CC} = 4.5 V$,	I _{OH} = -2.6 mA				2.4	3.2		1
Vai		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 V$	IOL = 24 mA					0.35	0.5]
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μA
lozu		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20			- 20	μΑ
Ιį		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ЧН		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL		$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.2			-0.2	mA
10‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
			Outputs high		11	18		11	18	
	'ALS574A		Outputs low		17	27		17	27]
laa		V _{CC} = 5.5 V	Outputs disabled		17	28		17	28	mA
Icc		VCC = 5.5 V	Outputs high		10	17		10	17	
	'ALS575A		Outputs low		15	24		15	24]
			Outputs disabled		16	30		16	30	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

'ALS574A switching characteristics (see Note 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C,$	VC CL R1 R2 TA	UNIT			
			'ALS574A TYP	SN54A	LS574A MAX	SN74A MIN	LS574A MAX	
		·			WIAA		WAA	
f _{max}			50	28		35		MHz
^t PLH	CLK	Q	8	4	22	4	14	ns
^t PHL	CER	. 4	. 8	4	17	4	14	113
^t PZH	<u>oc</u>	Q	9	4	21	4	18	ns
tpZL		ų ,	12	4	26	4	18	1 '18
t _{PHZ}	ŌC	Q	5	2	16	2	· 10	ns
tPLZ		ď	5	2	25	2	12	1 '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS575A, SN74ALS575A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS575A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R R: T,	CC = 50 L = 50 1 = 50 2 = 50 A = 25	pF, O Ω, O Ω, i°C	C _L R1 R2 T _A	CC = 4.5 V = 50 pF, = 500 Ω , $CC = 500 \Omega$	MAX		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	ALS575A MAX	1	
fmax			40	50		25		30		MHz	
tpLH	CLK	Q		8	11	4	15	4	14		
^t PHL	CLK			9	11.5	4	15	4	14	ns	
^t PZH	oc	α		11	14	4	21	4	18		
[†] PZL	00	u u		12	15	4	21	4	18	ns	
^t PHZ	oc	Q		6	8	2	12	2	10	ns	
[†] PLZ		<u> </u>		. 8	11	3	15	3	13	115	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS574, SN54AS575, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

				1 -	N54AS5 N54AS5			74AS57 74AS57	-	UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	ONIT
Vсс	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
ГОН	High-level output current					- 12			- 15	mA
lOL	Low-level output current					32			48	mA
f _{clock}	Clock frequency		,	0		100	0		125	MHz
	Pulse duration	CLK high		5			4			ns
t _w	Pulse duration	CLK low		4			2			115
	Setup time	Data		3			2			ns
tsu	before CLK↑	'AS575	CLR high or low	6.5			5.5] '''
	Hold time	Data		3			2			
th	after CLK↑	'AS575	CLR	0			0			ns
TA	Operating free-air temperatu	ire .		-55		125	0		70	°C



SN54AS574, SN54AS575, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise

PAR	AMETER	TEST CONDITION	IS	ł	SN54AS			N74AS N74AS		UNIT
			•	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
v_{IK}		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			- 1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -	2		Vcc -	2		
۷он		$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2.4	3.2					\ \
		$V_{CC} = 4.5 V,$	IOH = -15 mA		-		2.4	3.3		1
Va		$V_{CC} = 4.5 V,$	I _{OL} = 32 mA		0.29	0.5				V
VOL		$V_{CC} = 4.5 \text{ V},$	IOL = 48 mA					0.34	0.5]
lozh		$V_{CC} = 5.5 V$,	V _O = 2.7 V			50			50	μΑ
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50			- 50	μΑ
_		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΉΗ		V _{CC} = 5.5 V,	V ₁ = 2.7 V			20			20	μΑ
	OC, CLK, CLR	V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.5			-0.5	mA
,,,,	D	VCC = 5.5 V,	V - 0.4 V			- 3			- 2	IIIA
10 [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		- 112	mA
			Outputs high		73	116		73	116	
	'AS574		Outputs low		85	134		85	134	
1		V: F.F.V	Outputs disabled		84	134		84	134	mA
lcc		V _{CC} = 5.5 V	Outputs high		78	126		78	126	1
	'AS575		Outputs low		89	142		89	142	1
			Outputs disabled		88	142		88	142	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (очтрит)		UNIT			
			i	AS574 AS575	F	1AS574 1AS575	
			MIN	MAX	MIN	MAX	İ
f _{max}			100		125		MHz
^t PLH	CLK	Any Q	3	11	3	8	ns
[†] PHL	CER	Any G	4	11	4	9	1115
^t PZH	oc	Any Q	2	7	2	6	ns
tPZL		Ally Q	3	11	3	10	1 '''
[†] PHZ	ōc	Any Q	2	7	2	6	ns
^t PLZ		Ally Q	2	7	2	6	1115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS576A, SN54ALS577A, SN54AS576, SN54AS577 SN74ALS576A, SN74ALS577A, SN74AS576, SN74AS577 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 - REVISED MAY 1986

- 3-State Buffer-Type Inverting Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- 'ALS577A and 'AS577 Have Synchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

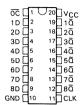
These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

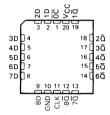
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C .

SN54ALS576A, SN54AS576 . . . J PACKAGE SN74ALS576A, SN74AS576 . . . DW OR N PACKAGE (TOP VIEW)



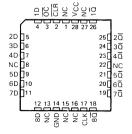
SN54ALS576A, SN54AS576 . . . FK PACKAGE (TOP VIEW)



SN54ALS577A, SN54AS577 . . . JT PACKAGE SN74ALS577A, SN74AS577 . . . DW OR NT PACKAGE (TOP VIEW)



SN54ALS577A, SN54AS577 . . . FK PACKAGE SN74ALS577A, SN74AS577 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection



FUNCTION TABLES

ALS576A, AS576 (Each Flip-Flop)

OUTPUT INPUTS ōς CLK D ā L н L L L н L āο L х

х

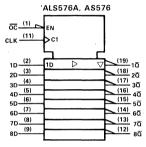
z

х

ALS577A, AS577 (Each Flip-Flop)

	INP	UTS		OUTPUT
ОC	CLR	CLK	D	ā
L	L	†	Х	Н
L	Н	†	Н	L
L	Н	†	L	Н
L	н	L	Х	ā _o z
н	X	×	Х	Z

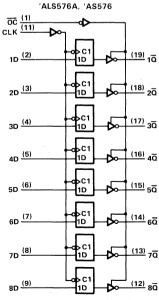
logic symbols†



'ALS577A, 'AS577 <u>oc</u> <u>(2)</u> ► CLK (1) CLR 1 R (<u>22)</u> 1Q 1D 1D-(<u>21)</u> 2Q (4) 2D-(5) (20) 3D-- 3Q (6) (19) 4Q 4D-(7) (18) 5Q 5D: 6D_(8) (<u>17)</u> 6Q (16) 7Q (9) 7D-(<u>15)</u> 8Ō (10) 8D-

logic diagrams (positive logic)

Н



Pin numbers shown are for DW, J, and N packages.

'ALS577A, 'AS577 OC (2) CLK (14) CLR (1) (22) 1Q 1D (3) 1D (21) 2Q 2D (4) 1D (<u>20)</u> 3Q 3D (5) (19) 4Q 4D (6) 1D (18) 5Q 5D (7) 1D (17) 6Q (<u>16)</u> 70 (15) 8Q 8D (10)

Pin numbers shown are for DW, JT and NT packages.



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS576A, SN54ALS577A, SN74ALS576A, SN74ALS577A OCTAL D.TYPE EDGE TRIGGERED FLIP FLOPS WITH 3 STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 7 V
Input voltage		 7 V
Voltage applied to a disabled 3-state or	utput	 5.5 V
Operating free-air temperature range:	SN54ALS', SN54AS'	 55 °C to 125 °C
	SN74ALS', SN74AS'	 0 °C to 70 °C
Storage temperature range		- 65 °C to 150 °C

recommended operating conditions

			1	54ALS5		ł	74ALS57		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX] """
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	9	2			2			V
VIL	Low-level input voltage	:			0.7			0.8	V
loн	High-level output curre	nt			- 1			-2.6	mA
lOL	Low-level output current				12			24	mA
f	Clock frequency	'ALS576A	0		25	0		30	MHz
fclock	Clock frequency	'ALS577A	0		25	0		30	IVITIZ
	Pulse duration	CLK high or low 'ALS576A	20			16.5			
tw	ruise duration	CLK high or low 'ALS577A	20			16.5			ns
	Setup time	Data	15			15			
t _{su}	before CLK1	CLR ('ALS577A)	15			15			ns
+.	Hold time	Data	4			0			
th	after CLK1	CLR ('ALS577A)	4			0			ns
TA	Operating free-air temp	erature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS		54ALS5			SN74ALS576A SN74ALS577A		
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	1
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.2			1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.9$	$5 \text{ V}, \text{ I}_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc	2		
∨он	$V_{CC} = 4.5 V$,	IOH = -1 mA	2.4	3.3					\ \
	$V_{CC} = 4.5 V,$	I _{OH} = -2.6 mA				2.4	3.2		1
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	1 °
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
^l ozL	$V_{CC} = 5.5 V_{c}$	V _O = 0.4 V			- 20			- 20	μΑ
l _l	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
IH	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IIL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
10 [‡]	$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA
		Outputs high		10	18		10	18	
¹ cc	$V_{CC} = 5.5 V$	Outputs low		15	24		15	24	mA
		Outputs disabled		16	30		16	30	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS576A, SN54ALS577A, SN74ALS576A, SN74ALS577A OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS576A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} \text{V}_{\text{CC}} = 5 \text{ V,} \\ \text{C}_{\text{L}} = 50 \text{ pF,} \\ \text{R1} = 500 \Omega, \\ \text{R2} = 500 \Omega, \\ \text{T}_{\text{A}} = 25 ^{\circ}\text{C} \\ \text{'ALS576A} \\ \end{array}$	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω, = 500 Ω, = MIN to LS576A	, MAX	LS576A MAX	UNIT
f _{max}		<u> </u>	50	25		30		MHz
^t PLH	CLK	Any Q	9	4	15	4	14	
tPHL	CLK	Any U	9	4	15	4	14	ns
^t PZH	ОC	Any Q	11	4	21	4	18	
^t PZL	00	Any u	11	4	21	4	18	ns
^t PHZ	ŌC	Any Q 'ALS576	6	2	12	2	10	ns
^t PLZ		Any Q	8	3	17	3	15	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

'ALS577A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	= 500 = 500 = 500 = 25° ALS577	pF, ∫Ω, ∫Ω, ≧C	CL R1 R2 T _A SN54A	$CC = 4.5$ \\ = 50 pF, \\ = 500 \Omega\$.\\ = 500 \Omega\$.\\ = MIN to \\ LS577A \\ MAX	MAX SN74A	LS577A	UNIT
		l	MIN	TYP	MAX	MIN	WAX	MIN	MAX	2011
†max			40	50		25		30		MHz
t _{PLH}	CLK	Any Q		9	11	4	15	4	14	ns
tPHL t	OER	Ally C		9	11.5	4	15	4	14	3
^t PZH	oc	Any Q		11	15	4	21	4	18	no
^t PZL		Any C		11	15	4	21	4	18	ns
tPHZ -	ōc	Any Q 'ALS577		6	8	2	12	2	10	ns
[†] PLZ		Any $\overline{\Omega}$		8	12	3	17	3	15	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS576, SN54AS577, SN74AS576, SN74AS577 OCTAL D-TYPE EDGE-TRIGGERED FLOP-FLOPS WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54	AS576		SN7	4AS57	6	
			SN54	AS577		SN7	4AS57	7	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	ONII
Vсс	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				- 12			- 15	mA
lOL	Low-level output current				32			48	mA
fclock	Clock frequency		0		100	0		125	MHz
	Pulse duration	CLK high	5			4			ns
t _w	ruise duration	CLK low	4			2			1115
	Setup time	Data	3			2			ns
t _{su}	before CLK1	CLR ('AS577)	6.5			5.5			ns
	Hold time	Data	3			2			
^t h	after CLK1	CLR ('AS577)	0			0			ns
ТД	Operating free-air tempera	ture	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAN	METER	TEST CO	ONDITIONS		N54AS5 N54AS5		1	74AS57 74AS57	-	UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc -	2		
V_{OH}		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2.4	3.2		ļ			\ \
		V _{CC} = 4.5 V,	I _{OH} = -15 mA				2.4	3.3		1
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.29	0.5				V
VOL		V _{CC} = 4.5 V						0.33	0.5	1 °
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μΑ
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50			- 50	μΑ
lj		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	-	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
lu.	D	V _{CC} = 5.5 V,	V _I = 0.4 V			- 3			- 2	mA
ll III	All other	VCC = 5.5 V,	V = 0.4 V			- 0.5			- 0.5	1
lo‡		$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 30		- 112	- 30		- 112	mA
			Outputs high		77	125		77	125	
	'AS576		Outputs low		84	135		84	135	
loo		V _{CC} = 5.5 V	Outputs disabled		84	135		84	135	mA
ICC		VCC - 5.5 V	Outputs high		78	126		78	126] ''''
	'AS577		Outputs low		76	123		76	123	
		Outputs low Outputs disabled		88	142		88	142	1	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54AS576, SN54AS577, SN74AS576, SN74AS577 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				UNIT
			MIN	MAX	MIN	MAX	1
f _{max}			100		125		MHz
t _{PLH}	CLK	Any Q	3	11	3	8	ns
tPHL tPHL	CLK	Aily G	4	11	4	9] '''
^t PZH	oc	Any Q	2	7	2	6	ns
^t PZL] 00	Any Q	3	11	3	10	115
^t PHZ	ōc	Any Q	2	7	2	6	ns
t _{PLZ}		Any d	2	7	2	6	1

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS580, SN54AS580, SN74ALS580, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic

'ALS573, 'AS573 'ALS580, 'AS580 True Outputs Inverting Outputs

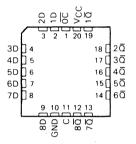
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

For complete information on the SN54ALS580, SN54AS580, SN74ALS580 and SN74AS580, see page 2-435.

SN54ALS580, SN54AS580 . . . J PACKAGE SN74ALS580, SN74AS580 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS580, SN54AS580 . . . FK PACKAGE
(TOP VIEW)



SN74ALS614, SN74ALS615 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

DW OR NT PACKAGE

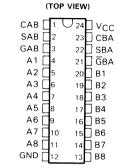
D2915, JANUARY 1986

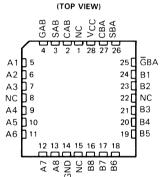
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths 'ALS614 . . . Inverting logic 'ALS615 . . . True logic
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether realtime or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and realtime data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time





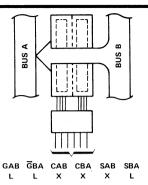
FN PACKAGE

NC-No internal connection

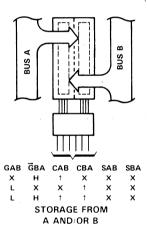
transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}BA$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

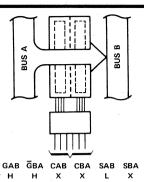
The -1 versions of the SN74ALS614 and SN74ALS615 are identical to the standard versions except that the recommended maximum I_{QL} is increased to 48 milliamperes.

The SN74ALS614 and SN74ALS615 are characterized for operation from 0°C to 70°C.

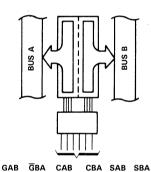


REAL-TIME TRANSFER BUS B TO BUS A





REAL-TIME TRANSFER BUS A TO BUS B



Horl Horl H

TRANSFER STORED DATA TO A AND/OR B

SN74ALS614, SN74ALS615 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

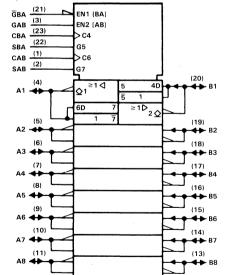
FUNCTION TABLE

		INPL	JTS			DATA	A I/O	OPERATION O	OR FUNCTION	
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	SN74ALS614	SN74ALS615	
L	Н	H or L	H or L	Х	Х	lan	Input	Isolation	Isolation	
L	Н	1	1	Х	X	Input	mput	Store A and B Data	Store A and B Data	
X	Н	1	H or L	Х	X	Input	Unspecified [†]	Store A, Hold B	Store A, Hold B	
Н	Н	1	1	Χ‡	X	Input	Output	Store A in both registers	Store A in both registers	
L	Х	HorL	1	Х	X	Unspecified †	Input	Hold A, Store B	Hold A, Store B	
L	L	1	1	Х	X [‡]	Output	Input	Store B in both registers	Store B in both registers	
L	L	X	X	Х	L	0		Real-Time B Data to A Bus	Real-Time B Data to A bus	
L	L	X	H or L	Χ	Н	Output	Input	Stored B Data to A Bus	Stored B data to A Bus	
Н	Н	X	Х	L	X	1	0	Real-Time A Data to B Bus	Real-Time A Data to B Bus	
Н	Н	HorL	Х	Ξ	Х	Input	Output	Stored A Data to B Bus	Stored A Data to B Bus	
Н		اعدا	H or L	Н	Н	0	0	Stored A Data to B Bus and	Stored A Data to B Bus and	
	L	n or L	n or L	П	п	Output	Output	Stored \overline{B} Data to A Bus	Stored B Data to A Bus	

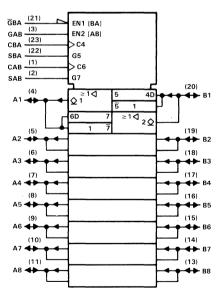
[†]The data output functions may be enabled or disabled by various signals at the GAB or $\overline{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols†

SN74ALS614



SN74ALS615



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW and NT packages.

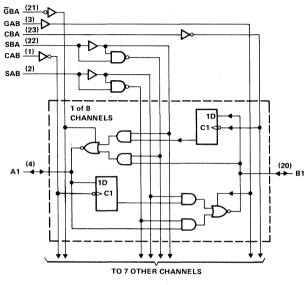


[‡] Select control = L: clocks can occur simultaneously.

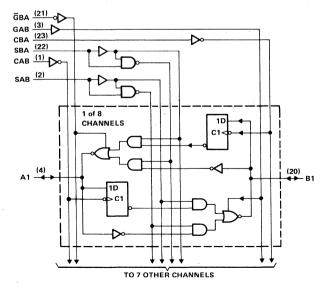
Select control = H: clocks must be staggered in order to load both registers.

logic diagrams (positive logic)

SN74ALS614



SN74ALS615



Pin numbers shown are for DW and NT packages.



SN74ALS614, SN74ALS615 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage: All inputs
Operating free-air temperature range
Storage temperature range – 65 °C to 150 °C

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
Vон	High-level output voltage				5.5	V
IOI Low-level output current					24	mA
IOL	Low-level output current				48 [†]	I IIIA
١.	Pulse duration	CBA or CAB high	16.5			
tw	ruise duration	CBA or CAB low	16.5			ns
t _{su}	Setup time before CAB† or CBA†	A or B	10			ns
th	Hold time after CAB↑ or CBA↑	A or B	0			ns
TA	Operating free-air temperature		0		70	°C

[†]The extended condition applies if Vcc is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS614-1 and SN74ALS615-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CONDITI	ONS	MIN	TYP‡	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	_I = -18 mA			-1.2	V	
loн		$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V			0.1	mA	
		$V_{CC} = 4.5 \text{ V},$ 1	OL = 12 mA		0.25	0.4		
V _{OL}		$V_{CC} = 4.75 \text{ V},$ I $I_{OL} = 48 \text{ mA for -1 v}$	0.		0.35	0.5	\ 	
	Control inputs	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA	
lj.	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1] ""A	
1	Control inputs	V 55V				20	_	
ΉΗ	A or B ports§	$V_{CC} = 5.5 V,$	V = 2.7 V			20	μΑ	
l	Control inputs	$V_{CC} = 5.5 \text{ V},$	V 0.4.V			-0.2	mA	
ΙĮĽ	A or B ports§	vCC = 9.5 v,	$V_1 = 0.4 \text{ V}$			-0.2] ""A	
	'ALS614		Outputs high		52	60	- A	
ذه ا	AL3014	$V_{CC} = 5.5 \text{ V}$	Outputs low		57	70	mA	
ICC	'ALS615	vCC = 9.5 v	Output high			60	mA	
	MLSOIS	Ī	Output low		48	72] '''A	



 $^{^\}ddagger$ All typical values are at VCC = 5 V, TA = 25 °C. § For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN74ALS614, SN74ALS615 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

SN74ALS614 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C F	CC = 5 L = 50 L = 680 A = 25°	pF,) Ω,	V _{CC} = 4. C _L = 50 R _L = 680 T _A = 0°C	UNIT		
			MIN	TYP	MAX	MIN	MAX	7	
^t PLH	CBA or CAB	A or B		37	52	20	64	T	
tPHL	CBA OF CAB	AOIB		14	19	6	20	ns	
^t PLH	A or B	B or A		31	42	14	51	ns	
^t PHL	AOIB			6	10	2	12		
tPLH .	SBA or SAB [†]	A or B		35	47	19	58	ns	
tPHL	(with A or B high)	Aorb		12	20	5	22		
t _{PLH}	SBA or SAB [†]	A or B		35	47	19	58	ns	
t _{PHL}	(with A or B low)	A or B		12	20	5	22		
t _{PLH}	GBA or GAB	A or B		16	22	9	27	T	
t _{PHL}	GDA OI GAB	AUIB		12	18	6	22	ns	

SN74ALS615 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C F	CC = 5 CL = 50 CL = 680 A = 25	pF,) Ω,	V _{CC} = 4.9 C _L = 50 p R _L = 680 T _A = 0°C	UNIT		
			MIN	TYP	MAX	MIN	MAX	7	
^t PLH	CBA or CAB	A or B		33	50	19	64	T	
^t PHL	CDA OF CAB	AOIB		14	-20	6	22	ns	
^t PLH	A or B	B or A		28	44	12	56	ns	
^t PHL	AUIB	BOFA		11	17	4	20		
^t PLH	SBA or SAB [†]	A or B		35	50	19	62		
^t PHL	(with A or B high)	AOIB		15	22	5	25	ns	
^t PLH	SBA or SAB [†]	A or B		35	50	19	62	ns	
^t PHL	(with A or B low)	A or B		15	22	5	25		
^t PLH	GBA or GAB	A or B		17	23	6	27		
^t PHL	GDA OF GAB	A OF B		14	20	6	24	ns	

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2840, APRIL 1984-REVISED MAY 1986

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT
'ALS616	3-State
'ALS617	Open-Collector

description

The 'ALS616 and 'ALS617 are 16-bit parallel error detection and correction circuits in 40-pin, 600-mil packages. The EDACs use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During memory read cycles, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

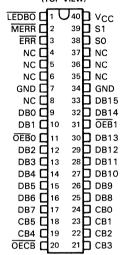
Single-bit errors in the 16-bit data word are flagged and corrected. Single-bit errors in the 6-bit check word are flagged, but the data word will remain unaltered. The 6-bit error syndrome code will pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 22-bit word from memory. The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

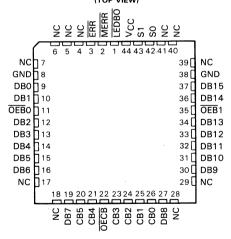
Read-modify-write (byte-control) operations can be performed with the 'ALS616 and 'ALS617 EDACs by using output latch enable, LEDBO, and individual OEBO and OEB1 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

SN54ALS616, SN54ALS617 . . . JD PACKAGE SN74ALS616, SN74ALS617 . . . JD OR N PACKAGE (TOP VIEW)



SN74ALS616, SN74ALS617 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

The SN54ALS616 and SN54ALS617 are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C. The SN74ALS616 and SN74ALS617 are characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.



SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1 S0	DATA I/O	DB CONTROL OEBO & OEB1	DB OUTPUT LATCH	CHECK I/O	CB CONTROL OECB	ERROF ERR	R FLAGS MERR
Write	Generate check word	LL	Input	н	X	Output check bits [†]	L	Н	Н

[†]See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB5) are generated internally in the EDAC by six 8-input parity generators using the 16-bit data word as defined in Table 2. These six check bits are stored in memory along with the original 16-bit data word. This 22-bit word will later be used in the memory read cycle for error detection and correction.

TABLE 2. PARITY ALGORITHM

CHECK WORD							16-B	IT DA	DATA WORD							
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
. CBO			X		Х	Х	Х			Х			Х		Х	Х
CB1		Χ		Х		Х	X	Х				Χ		Χ		Χ
CB2	×			X	X			X	Χ		X			Х	X	
CB3	×	Х	X				X	Х			Х	X	Х			
CB4	×	Х	Χ	Х	X	Χ			X	X						
CB5									Χ	X	Х	X	Х	Х	Х	Х

The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 6-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on MERR and a low on ERR, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both ERR and MERR, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBI	R OF ERRORS	ERROF	RFLAGS	DATA CORRECTION
16-BIT DATA WORD	6-BIT CHECK WORD	ERR	MERR	DATA CONNECTION
0	0	Н	Н	Not applicable
1	0	L	Н	Correction .
0	1	L	Н	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L.	Interrupt



SN54ALS616, SN54ALS617, SN74ALS616, SN74ALS617 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CON S1	TROL SO	DATA I/O	DB CONTROL OEB0 & OEB1	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS ERR MERR
Read	Read & flag	Н	L	Input	н	Х	Input	Н	Enabled [†]
Read	Latch input data & check bits	н	Н	Latched input data	н	L	Latched input check word	Н	Enabled [†]
Read	Output corrected data and syndrome bits	#	н	Output corrected data word	L	×	Output syndrome bits [‡]	L	Enabled [†]

[†]See Table 3 for error description.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to the internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all highs will be detected.

As the corrected word is made available on the data I/O port (DBO thru DB15), the check word I/O port (CBO thru CB5) presents a 6-bit syndrome error code. This syndrome code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

[‡]See Table 5 for error location.

TABLE 5. SYNDROME DECODING

SY	ND	s	ERROR				
5	4	3	2	1	0		
L	L	L	L	L	L	2-bit	
L	L	L	L	L	Н	unc	
L	L	L	L	Н	Ĺ	unc	
L	L	L	L	Н	Н	2-bit	
L	L	L	Н	L	L	unc	
L	L	L	Н	L	Н	2-bit	
L	L	L	Н	Н	L	2-bit	
L	L	L	Н	Н	Н	unc	
L	L	Н	L	L	L	unc	
L	L	Н	L	L	Н	2-bit	
L	L	Н	L	Н	L	2-bit	
L	L	Н	L	Н	Н	DB7	
L	L	Н	Н	L	L	2-bit	
L	L	Н	Н	L	Н	unc	
L	L	Н	Н	Н	L	DB6	
L	L	Н	Н	Н	Н	2-bit	

SYNDROME BITS						ERROR	
5	4	3	2	1	0		
L	Н	L	Ŀ	L	L	unc	
L	Н	L	L	L	Н	2-bit	
L	Н	L	L	Н	L	2-bit	
L	Н	L	Ĺ	Н	Н	DB5	
L	Н	L	Н	L	L	2-bit	
L	Н	L	Н	L	Н	DB4	
L	Н	L	Н	Н	L	DB3	
L	Н	L	Н	Ĥ	Н	2-bit	
L	Н	Н	L	L	L	2-bit	
L	Н	Н	L	L	Н	DB2	
L	Н	Н	L	Н	L	DB1	
L	Н	Н	L	Н	Н	2-bit	
L	Н	Н	Н	L	L	DB0	
L	Н	Н	Н	L	н	2-bit	
L	Н	Н	Н	Н	L	2-bit	
L	Н	Н	Н	Н	н	CB5	

SY	ND	ROI	ΝE	ВІТ	S	ERROR		
5	4	3	2	1	0	ERRUR		
Н	L	L	L	L	L	unc		
Н	L	L	L	L	Н	2-bit		
Н	L	L	L	Н	L	2-bit		
Н	L	L	L	Н	Н	DB15		
Н	L	L	Н	L	L	2-bit		
Н	L	Ł	Н	L	Н	DB14		
Н	L	L	Н	Н	L	DB13		
Н	L	L	Н	Н	Н	2-bit		
Н	L.	Н	L	L	L	2-bit		
Н	L	Н	L	L	Н	DB12		
Н	L	Н	L	Н	L	DB11		
Н	L	Н	Ļ	Н	Н	2-bit		
Н	L	Н	Н	L	L	DB10		
Н	L	Н	Н	L	Н	2-bit		
Н	L	Н	Н	Н	L	2-bit		
Н	L	Н	Н	Н	Н	CB4		

SY	ND	OR	VΙΕ	BIT	s	
5	4	0	ERROR			
Н	Н	L	L	L	L	2-bit
Н	Н	L	L	L	Н	DB8
Н	Н	L	L	Н	L	unc
Н	Н	L	L	Н	Н	2-bit
Н	Н	L	Н	L	L	DB9
Н	Н	L	Ĥ	L	Н	2-bit
Н	Н	L	Н	Н	L	2-bit
Н	Н	L	Н	Н	Н	СВЗ
Н	Н	Н	L	L	L	unc
Н	Н	Н	L	L	Н	2-bit
Н	Н	Н	L	Н	L	2-bit
Н	Н	Н	L	Н	Н	CB2
Н	Н	Н	Н	L	L	2-bit
Н	Н	Н	Н	L	Н	CB1
Н	Н	Н	Н	Н	L	СВО
Н	Н	Н	Н	Н	Н	none

CB X = error in check bit X

DB Y = error in data bit Y

2-bit = double-bit error

unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS616 and 'ALS617 devices are capable of byte-write operations. The 22-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB}}0$ or $\overline{\text{OEB}}1$ controls. $\overline{\text{OEB}}0$ controls DB0-DB7 (byte 0), $\overline{\text{OEB}}1$ controls DB8-DB15 (byte 1).

Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CON S1	TROL SO	BYTEn [†]	ŌEBn†	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL	ERROR FLAG
Read	Read & Flag	Н	L	Input	Н	X	Input	Н	Enabled
Read	Latch input data & check bits	н	Н	Latched Input data	н	L	Latched input check word	н	Enabled
Read	Latch corrected data word into output latch	н	н	Latched output data word	Н	Н	Hi-Z Output Syndrome bits	H L	Enabled
Modify/ write	Modify appropriate byte or bytes & generate new check word	· Ł	L	Input modified BYTEO Output unchanged BYTEO	H	Н	Output check word	L	нн

[†]OEBO controls DBO-DB7 (BYTE0), OEB1 controls DB8-DB15 (BYTE1)

diagnostic operations

The 'ALS616 and 'ALS617 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the ERR flag should be low. If a diagnostic data word with two errors in any bit location is applied, the MERR flag should be low. After the checkword is latched into the input latch, it can be verified by taking OECB low. This outputs the latched checkword. The diagnostic data word can be latched into the output data latch and verified via the $\overline{\text{LEDBO}}$ control pin. By changing from the diagnostic mode (S1 = L, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

TABLE 7. DIAGNOSTIC FUNCTION

EDAC FUNCTION		TROL S0	DATA I/O	DB BYTE CONTROL OEBn	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS ERR MERR
Read & flag	н	L	Input correct data word	Н	×	Input correct check bits	Н	н н
Latch input check word while data input latch remains transparent	L	н	Input diagnostic data word [†]	н	Ľ	Latched input check bits	Н	Enabled
Latch diagnostic data word into output latch	L	н	Input diagnostic data word [†]	Н	. н	Output latched check bits Hi-Z	L	Enabled
Latch diagnostic data word into input latch	Н	н	Latched input diagnostic data word	Н	Н	Output syndrome bits Hi-Z	L — H — –	Enabled
Output diagnostic data word & syndrome bits	Н	Н	Output diagnostic data word	L	н	Output syndrome bits Hi-Z	L — — — — —	Enabled
Output corrected diagnostic data word & output syndrome bits	н	Н	Output corrected diagnostic data word	L	· L	Output syndrome bits Hi-Z	L — — — —	Enabled

[†]Diagnostic data is a data word with an error in one bit location except when testing the MERR error flag. In this case, the diagnostic data word will contain errors in two bit locations.



logic diagram (positive logic) DECODER SYNDROME X/Y GENERATOR 0 S0 3 2 3 CHECK-BIT 6 2 GENERATOR LATCHES C1 CB0-CB5 -1D MUX [6 X-OR BUFFERS **ERROR** DETECTOR OECB **LATCHES** C1 ERROR ERR ΕN 16 DB0-DB7 1D **MÚLTI-ERROR** MERR DB8-DB15 -4-1D 16 BUFFERS BIT-IN-ERROR ERROR DECODER CORRECTOR OEB0 LATCHES ΕN 16 16 OEB1 16 C1 [16 X-OR]

LEDBO -

^{*&#}x27;ALS616 has 3-state (\bigcirc) check-bit and data outputs.

^{&#}x27;ALS617 has open-collector(\(\Omega\)) check-bit and data outputs.

recommended operating conditions

				SN	I54ALS I54ALS	617	SN	74ALS6 74ALS6	17	UNIT
				MIN		MAX	MIN	NOM		
	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage			-		0.7	ļ		0.8	V
vон	High-level output voltage	DB or CB	'ALS617	+		5.5			5.5	
ЮН	High-level output current	ERR or MERR		<u> </u>		-0.4			-0.4	mA
		DB or CB	'ALS616	ļ		-1			-2.6	
loL	Low-level output current	ERR or MERF				4			8	mA
·OL	2011 lovor output current	DB or CB				12			24	
t_W	Pulse duration	LEDBO low		45			25			ns
		(1) Data an (S1 = H)	d check word before S01	15			12			
		(2) S0 high	before LEDBO↑ (S1 = H) †	45			45			
		(3) LEDBO high before the earlier of SO↓ or S1↓†					0			
			high before S1↑ (S0 = H)	1.0			0			1
tsu	Setup time		tic data word before S11	╁┷			·			ns
		(S0 = H)		28			12			
		1	tic check word before the . S1↓ or S0↑	15			12			
			stic data word before $(S1 = L \text{ and } S0 = H)^{\dagger}$	35			20			
		(8) Read-m	ode, S0 low and S1 high	35			30			
	. *	(9) Data an (S1 = H)	d check word after SO↑	20			15			
		(10) Data we	ord after S1↑ (S0 = H)	20			15			1
th	Hold time	(11) Check v S1↓ or	word after the later of SO1	20			15			ns
			stic data word after (S1 = L, S0 = H) [‡]	0			0	***************************************		
t _{corr}	Correction time (see Figure	L		70			65			ns
TC	Operating case temperature			- 55		125				°C
TA	Operating free-air temperatu	ire		1			0		70	°C

[†]These times ensure that corrected data is saved in the output data latch.



[‡]These times ensure that the diagnostic data word is saved in the output data latch.

SN54ALS616, SN74ALS616 16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

'ALS616 electrical characteristics over recommended operating temperature range (unless otherwise noted)

	ADAMETED	TF0T 001	UDITIONS		N54AL	S 6 16	s	N74ALS	616	UNIT
P.	ARAMETER	TEST CO	ADITIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	ONLI
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.5			- 1.5	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		
Voн	DB or CB	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -1 mA	2.4	3.3					V
	DB OF CB	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	ERR or MERR	$V_{CC} = 4.5 V$,	IOH = 4 mA		Q.25	0.4		0.25	0.4	
V	ERR OF WERK	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	V
VOF	DB or CB	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	DB OF CB	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	
1.	SO or S1	$V_{CC} = 5.5 V$,	V ₁ = 7 V	T		0.1			0.1	mA
ŧ _l	DB or CB	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	IIIA
1	S0 or S1	VCC = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ΉΗ	DB or CB [‡]	vCC = 5.5 v,	V = 2.7 V			20			20	μΑ
	S0 or S1	V 55V	V _I = 0.4 V			-0.4			-0.4	^
l IIL	DB or CB‡	$V_{CC} = 5.5 V,$	v _j = 0.4 v			-0.1			-0.1	mA
lo§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
1cc		V _{CC} = 5.5 V	See Note 1		110	190		110	170	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

'ALS616 switching characteristics, $V_{CC} = 4.5 \text{ V}$ to 5.5 V, $C_L = 50 \text{ pF}$, $T_C = -55 ^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$ for SN54ALS616, $T_A = 0$ °C to 70°C for SN74ALS616

PARAMETER	FROM	то	TEST CONDITIONS	SN54A	LS616	SN74	ALS616	UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	MAX	MIN	MAX	ONL
	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	10	43	10	40	ns
^t pd	DB	ERR	S1 = L, S0 = H, $R_L = 500 \Omega$	10	43	10	40	115
	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	15	65	15	55	ns
^t pd	DB	MERR	S1 = L, S0 = H, $R_L = 500 \Omega$	15	65	15	55	115
t _{pd}	S0↓ and S1↓	СВ	R1 = R2 = 500 Ω	10	60	10	49	ns
t _{pd}	DB	СВ	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	49	ns
t _{pd}	LEDBO↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t _{pd}	S1↑	СВ	S0 = H, R1 = R2 = 500 Ω	10	50	10	50	ns
t _{en}	OECB↓	СВ	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
^t dis	OECB↑	СВ	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t _{en}	OEBO and OEB1↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns
t _{dis}	OEB0 and OEB1↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	30	2	27	ns

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with SO and S1 at 4.5 V and all CB and DB pins grounded.

'ALS617 electrical characteristics over recommended operating temperature range (unless otherwise noted)

	ARAMETER	TEST CON	DITIONS	SN	54ALS	317	SN	74ALS6	17	UNIT
· -	ANAMETEN	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
Vон	ERR or MERR	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			VCC-2			٧
Іон	DB or CB	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1			0.1	mA
	ERR or MERR	$V_{CC} = 4.5 \text{ V},$	IOH = 4 mA		0.25	0.4		0.25	0.4	
VOL	ETTIT OF WILLIAM	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 8 \text{ mA}$					0.35	0.5	V
VOL	DB or CB	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	· ·
	DB of CB	V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	
1.	S0 or S1	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
4	DB or CB	$V_{CC} = 5.5 \text{ V},$	V _I = 5.5 V			0.1			0.1	IIIA
1	S0 or S1	Vcc = 5.5 V,	V _I = 2.7 V			20			20	^
Ιн	DB or CB [‡]	VCC = 5.5 V,	V = 2.7 V			20			20	μΑ
1	S0 or S1	Vcc = 5.5 V,	V _I = 0.4 V			-0.4			-0.4	mA
IL	DB or CB [‡]	vCC = 5.5 v,	V = 0.4 V			-0.1			-0.1	mA
IO§	ERR or MERR	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Icc		V _{CC} = 5.5 V	See Note 1		110			110		mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

'ALS617 switching characteristics, $V_{CC} = 4.5 \text{ V}$ to 5.5 V, $C_L = 50 \text{ pF}$, $T_C = -55 ^{\circ}\text{C}$ to $125 ^{\circ}\text{C}$ for SN54ALS617, $T_A = 0$ °C to 70 °C for SN74ALS617

PARAMETER	FROM	TO	TEST CONDITIONS	SN54ALS617	SN74ALS617	
PARAIVIETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN TYP† MAX	MIN TYPT MAX	UNIT
	DB and CB	ERR	S1 = H, S0 = L, R_L = 500 Ω	26	26	
t _{pd}	DB	ĒRR	S1 = L, S0 = H, $R_L = 500 \Omega$	26	26	ns
t	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	40	40	ns
^t pd	DB and CB	IVILITI	S1 = L, S0 = H, R_L = 500 Ω	40	40	115
t _{pd}	S0↓ and S1↓	СВ	$R_L = 680 \Omega$	40	40	ns
t _{pd}	DB	СВ	S1 = L, S0 = L, $R_L = 680 \Omega$	40	40	ns
t _{pd}	LEDBO↓	DB	S1 = X, S0 = H, $R_L = 680 \Omega$	26	26	ns
t _{pd}	S1↑	СВ	S0 = H, $R_L = 680 \Omega$	40	40	ns
tPLH	OECB↑	СВ	S1 = X, S0 = H, R_L = 680 Ω	24	24	ns
tPHL	OECB↓	СВ	S1 = X, S0 = H, R _L = 680 Ω	24	24	ns
tPLH	OEB0 and OEB1↑	DB	S1 = X, S0 = H, R _L = 680 Ω	24	24	ns
tPHL	OEB0 and OEB1↓	DB	S1 = X, S0 = H, R _L = 680 Ω	24	24	ns

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

Additional information on these products can be obtained from the factory as it becomes available.

[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with SO and S1 at 4.5 V and all CB and DB pins grounded.

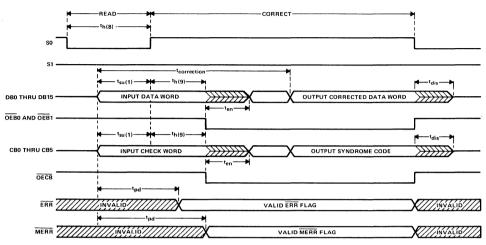


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

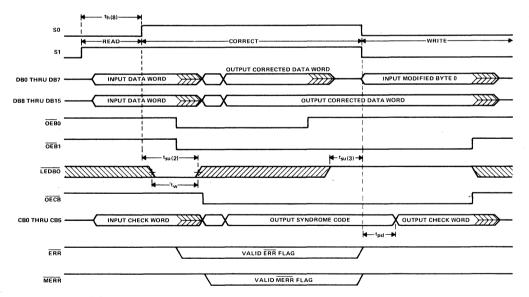


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

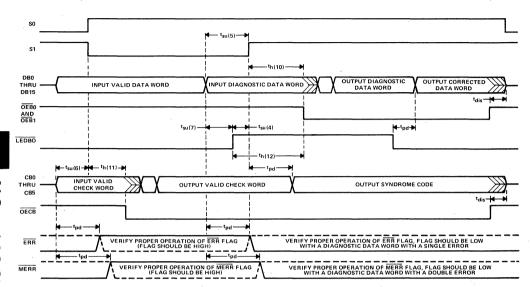


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

SN54ALS620A THRU SN54ALS623A, SN54AS620 THRU SN54AS623 SN74ALS620A THRU SN74ALS623A, SN74AS620 THRU SN74AS623 OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1982 - REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Local Bus-Latch Capability
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS620A, 'AS620	3-State	Inverting
'ALS621A, 'AS621	Open-Collector	True
'ALS622A, 'AS622	Open-Collector	Inverting
'ALS623A, 'AS623	3-State	True

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the octal bus transceivers the capability to store data by

simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS621A, 'AS621 and 'ALS623A, 'AS623 or complementary for the 'ALS620A, 'AS620 and 'ALS622A. 'AS622.

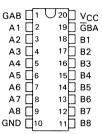
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

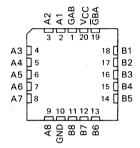
FUNCTION TABLE

ENABLE	INPUTS	OPERA	ATION
ĞВА	GAB	'ALS620A, 'ALS622A 'AS620, 'AS622	'ALS621A, 'ALS623A 'AS621, 'AS623
L	L	B data to A bus	B data to A bus
Н	Н	A data to B bus	A data to B bus
Н	L	Isolation	Isolation
L	Н	B data to A bus, A data to B bus	B data to A bus, A data to B bus

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)

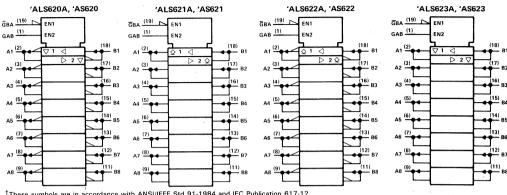


PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



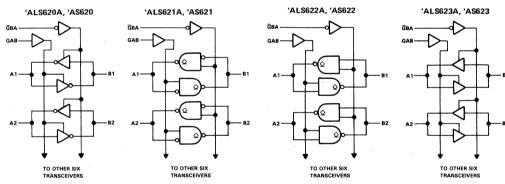
SN54ALS620A THRU SN54ALS623A, SN54AS620 THRU SN54AS623 SN74ALS620A THRU SN74ALS623A, SN74AS620 THRU SN74AS623 OCTAL BUS TRANSCEIVERS

logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

logic diagrams (positive logic)



SN54ALS620A, SN54ALS623A, SN74ALS620A, SN74ALS623A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage: All inputs		7 V
I/O ports		5.5 V
Operating free-air temperature range:	SN54ALS620A, SN54ALS623A	55°C to 125°C
	SN74ALS620A, SN74ALS623A	
Storage temperature range		-65° C to 150° C

recommended operating conditions

			SN54ALS620A SN54ALS623A				SN74ALS620A SN74ALS623A		
		MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.7			0.8	٧	
ЮН	High-level output current			-12			- 15	mA	
lo:	Lava laval autorit autorit			12			24	^	
lOL	Low-level output current						48†	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

 $^{^{\}dagger}\text{The}$ extended limits apply only if $V_{\mbox{\footnotesize{CC}}}$ is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS620A-1 and SN74ALS623A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	PARAMETER	TEST COND	ITIONS		4ALS6		SN74ALS620A SN74ALS623A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	1
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{j} = -18 \text{ mA}$				-1.5			-1.5	٧	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
V		$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
Vон		V _{CC} = 4.5 V,	I _{OH} = -12 mA	2						v
		V _{CC} = 4.5 V,	I _{OH} = -15 mA				2			
		V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL		V _{CC} = 4.5 V,	1 _{OL} = 24 mA					0.05	۰.	V
		(I _{OL} = 48 mA for -1 ver					0.35	0.5		
1.	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	0.1 mA
Ч	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	
l	Control inputs	V _{CC} = 5.5 V,	V 2.7.V			20			20	
ΙН	A or B ports§	VCC = 5.5 V,	$V_1 = 2.7 V$			20			20	μА
1	Control inputs	V 5 5 V	V _I = 0.4 V			-0.1			-0.1	
llL	A or B ports§	$V_{CC} = 5.5 V,$	V = 0.4 V			-0.1			-0.1	m/
Ιο¶		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	- 30		-112	m/
			Outputs high		24	39		24	34	
	'ALS620A	V _{CC} = 5.5 V	Outputs low		31	49		31	44	
lcc			Outputs disabled		33	52		33	47	m/
iCC			Outputs high		32	48		32	43] ""
	'ALS623A	ļ	Outputs low		39	55		39	50]
		1	Outputs disabled		42	60		42	42 55	

 \ddagger All typical values are at VCC = 5 V, TA = 25 °C §For I/O ports, the parameters $I_{|H}$ and $I_{|L}$ include the off-state output current.



The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios.

SN54ALS620A, SN54ALS623A, SN74ALS620A, SN74ALS623A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

'ALS620A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ŤО (О UТР ИТ)	$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_A = \text{MIN to MAX} \\ \text{SN54ALS620A} & \text{SN74ALS620A} \end{array}$			UNIT	
			MIN	MAX	MIN	MAX	
^t PLH	^	В	2	12	2	10	
^t PHL	Α	В .	2	12	2	10	ns
^t PLH	В	Α	2	12	2	10	ns
^t PHL		^	2	12	2	10	118
^t PZH	Ğва	Α	3 .	23	3	17	ns
tPZL	GUA	^	5	31	5	25	113
^t PHZ	G ва	А	2	14	2	12	ns
^t PLZ	GBA		3	22	3	18	113
^t PZH	GAB	В	3	23	3	18	ns
tPZL	CAB		5	31	5	25	113
tPHZ	GAB	В	2	14	2	12	ns
^t PLZ	GAB		3	22	3	18	113

'ALS623A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R1=500$ Ω , $R2=500$ Ω , $T_A=MIN$ to MAX		,	UNIT	
			SN54A MIN	LS623A		LS623A	
+	-		2	MAX 15	MIN 2	MAX	
tPLH	A .	В	3	13	3	13	ns
†PHL	 		2		2		
tPLH .	В	Α		15		13	ns
^t PHL			3	13	3	11	
^t PZH	Gва	Α Α	5	25	5	22	ns
^t PZL	7 004	^	5	25	5	22] "15
[†] PHZ	Бва		2	19	2	16	
[†] PLZ	GBA	А	2	23	2	19	ns
^t PZH	CAR		5	25	5	22	
tPZL	GAB	В	5	25	5	22	ns
[†] PHZ	CAR		2	19	2	16	
^t PLZ	GAB	В	2	23	2	19	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS621A, SN54ALS622A, SN74ALS621A, SN74ALS622A OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	
Input voltage: All inputs and I/O ports	
Operating free-air temperature range: SN54ALS621A, SN54ALS622A	
SN74ALS621A, SN74ALS622A 0°C to 70°C	
Storage temperature range65°C to 150°C	

recommended operating conditions

						SN74ALS621A SN74ALS622A			
		MIN	NOM	MAX	MIN	NOM	MAX	1	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Voн	High-level output voltage			5.5			5.5	V	
lou	1 1			12			24		
lOL	Low-level output current						48†	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

[†]The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS621A-1 and SN74ALS622A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		PARAMETER TEST CONDITIONS			SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A		
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
VIK		$V_{CC} = 4.5 V,$	I ₁ = -18 mA			-1.5			-1.5	٧
ЮН		$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V			0.1			0.1	mA
		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V_{OL}		$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	V
		(I _{OL} = 48 mA fo	r -1 versions)					0.35	0.5	
1.	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
t _i	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	
l	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μА
ΉΗ	A or B ports§	vCC = 5.5 v,	V = 2.7 V			20			20	μΑ
1	Control inputs	V E E V	V _I = 0.4 V			-0.1			-0.1	mA
ΊL	A or B ports§	$V_{CC} = 5.5 V,$	V = 0.4 V			-0.1			-0.1	IIIA
	'ALS621A	V00 - 5 5 V	Outputs high		29	45		29	40	
1	ALSOZ IA	$V_{CC} = 5.5 V$	Outputs low		35	53		35	48	mA
Icc	'ALS622A	V 55V	Outputs high		11	20		11	15	l IIIA
	ALSOZZA	$V_{CC} = 5.5 V$	Outputs low		20	33		20	28	

‡All typical values are at V $_{CC}=5$ V, T $_{A}=25\,^{\circ}\text{C}.$ §For I/O ports, the parameters I $_{IH}$ and I $_{IL}$ include the off-state output current.



SN54ALS621A, SN54ALS622A, SN74ALS621A, SN74ALS622A OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

'ALS621A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 680 \Omega$ $T_A = MIN \text{ to}$	•		UNIT	
			SN544	LS621A	SN74ALS621A			
	<u> </u>		MIN	MAX	MIN	MAX		
tPLH	Α	В	10	45	10	33	ns	
tPHL	^	ь	5	24	5	20	115	
^t PLH	В	Α	10	45	10	33	ns	
^t PHL	6	A	5	24	5	20	115	
^t PLH	GBA	Α	10	47	10	39	ns	
^t PHL	GDA		12	40	12	35	115	
tPLH	GAB	В	10	47	10	39	ns	
tPHL	GAB	ь	12	40	12	35	115	

'ALS622A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ N}$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega,$ $T_A = MIN \text{ to}$			UNIT
	•	Ì	SN54ALS622A SN74	SN74A	LS622A	1	
			MIN	MAX	MIN	MAX	
^t PLH	Α	В	8	42	8	35	
tPHL	A	•	5	23	5	19	ns
tPLH	В	А	8	42	8	35	ns
^t PHL	В		. 5	23	5	19	115
^t PLH	Ğва	Α	8	45	8	38	
^t PHL	GDA	^	10	40	10	35	, ns.
^t PLH	GAB	В	8	45	8	38	ns
^t PHL	GAB	"	10	40	10	35	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS620, SN54AS623, SN74AS620, SN74AS623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage: All inputs
I/O ports
Operating free-air temperature range: SN54AS620, SN54AS623
SN74AS620, SN74AS623
Storage temperature range

recommended operating conditions

			N54AS6 N54AS6		sı sı	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX]
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-12			- 15	mA
IOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER	TEST COND	ITIONS		154AS6 154AS6	-	1	74AS6 174AS6		UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	1
VIK		V _{CC} = 4.5 V,	i _l = -18 mA			-1.2			-1.2	٧
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2		_	V _{CC} -2			
V		$V_{CC} = 4.5 V,$	$l_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
VOH		$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2] *
		$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2			
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.30	0.55				V
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 64 \text{ mA}$					0.35	0.55	
ı.	Control inputs	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
lj	A or B ports	$V_{CC} = 5.5 V,$	$V_I = 5.5 V$			0.1			0.1	IIIA
1	Control inputs	$V_{CC} = 5.5 V_{c}$	$V_1 = 2.7 \text{ V}$			20			20	μΑ
۱н	A or B ports‡	VCC = 5.5 V,	V - 2.7 V			70			70	μΑ
	Control inputs	$V_{CC} = 5.5 V_{c}$	$V_1 = 0.4 \text{ V}$			-0.5			-0.5	mA
¹ IL	A or B ports‡	VCC = 5.5 V,	· · · · · · · · · · · · · · · · · · ·			-0.75			-0.75	IIIA
IO§		$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 50		- 150	- 50		-150	mA
			Outputs high		35	57		35	57	1
	'AS620	$V_{CC} = 5.5 V$	Outputs low		74	122		74	122]
lcc	с —		Outputs disabled		48	77		48	77	mA
			Outputs high		57	93		57	93	
	'AS623	$V_{CC} = 5.5 V$	Outputs low		116	189		116	189	
			Outputs disabled		71	116		71	116	1

 $^{^{\}dagger}AII$ typical values are at VCC2 = 5 V, T_A = 25 °C.



[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

'AS620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R1 = 500 R2 = 500 T _A = MI	0Ω, 0Ω,	v,	UNIT
			SN54	AS620		AS620	
			MIN	MAX	MIN	MAX	
tPLH	Α	В	1	8	1	7	
^t PHL		В	2	7	2	6	ns
^t PLH	В	Α	1	8	1	7	
^t PHL	D	^	2	7	2	6	ns
^t PZH	GBA	Α	2	8.5	2	8	
tPZL	GDA	^	2	10	2	9	ns
^t PHZ	ĞВА	Α	1	7.5	1	6	
tPLZ	GBA .	A	2	15	2	12	ns
^t PZH	GAB	В	2	9	2	8	
tPZL	GAB	В	2	10.5	2	9	ns
^t PHZ	GAB	В	1	6.5	1	6	
tPLZ	GAB	В	2	16	2	13	ns

'AS623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS623$ $SN74AS623$									
1			MIN	AS623 MAX	MIN	MAX							
tPLH			1	10	1	9							
tPHL	Α Α	В	1	9	1	8	ns						
t _{PLH}			1	10	1	9							
tPHL t	В .	Α	1	9.5	1	8.5	ns						
tPZH	5		2	11.5	2	11							
tPZL	ĞВА	Α	2	11	2	10	ns						
[†] PHZ	ĞВА		1	8.5	1	7.5							
[†] PLZ	GBA .	· A	1	13.5	1	11.5	ns						
^t PZH	GAB	В	2	13	2	11.5							
^t PZL	1 GAB	В	2	12	2	11	ns						
tPHZ	GAB	В -	1	8	1	7							
^t PLZ	T GAB		1	10.5	1	9	ns						

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS621, SN54AS622, SN74AS621, SN74AS622 OCTAL BUS TRANSCEIVERS WTIH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
	ts
Operating free-air temperature rang	e: SN54AS621, SN54AS622
	SN74AS621, SN74AS622
Storage temperature range	- 65 °C to 150 °C

recommended operating conditions

			N54AS6 N54AS6			174AS6 174AS6		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5.	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Voн	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER	TEST CO	ONDITIONS		N54AS6 N54AS6		18 18	UNIT		
				MIN	TYP†	MAX	MIN	TYP†	MAX	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
ЮН		$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1			0.1	mA
		$V_{CC} = 4.5 V$,	I _{OL} = 48 mA		0.30	0.5				V
v_{OL}		$V_{CC} = 4.5 V$,	I _{OL} = 64 mA					0.35	0.5	\ \
	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lį	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	mA
,	Control inputs	V- 55V	., 27,4			20			20	
ΉН	A or B ports‡	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			70			70	μΑ
	Control inputs	V 5.5.V	V 0 4 V			-0.5			-0.5	
ΗL	A or B ports‡	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.75			-0.75	mA
	(40004	V _{CC} = 5.5 V	Outputs high		48	79		48	79	
	'AS621	VCC - 3.5 V	Outputs low		116	189		116	189	
ICC		V _{CC} = 5.5 V	Outputs high	24 39 2	24	39	mA			
	'AS622	vCC = 5.5 v	Outputs low		63	103		63	103	

[†]All typical values are at VCC = 5 V, TA = 25 °C ‡For I/O ports, the parameters $l_{|H}$ and $l_{|L}$ include the off-state output current.

SN54AS621, SN54AS622, SN74AS621, SN74AS622 OCTAL BUS TRANSCEIVERS WTIH OPEN-COLLECTOR OUTPUTS

'AS621 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		$V_{CC} = 4.5$ $C_L = 50 \text{ pi}$ $R_L = 500$ $T_A = MIN$	F, Ω,	<i>.</i>	UNIT
			SN54	AS621	SN74	AS621	
			MIN	MAX	MIN	MAX	
^t PLH	А	В	5	28.5	5	24	ns
^t PHL	^	B	1	8.5	1	7.5	115
^t PLH	В	Α	5	23	5	21	ns
^t PHL		. ^	1	8.5	1	7.5	115
tPLH	ĒΡΛ	Α	5	24	5	21	· nc
[‡] PHL	GBA	Α	1	10	1	9	ns
^t PLH	GAR	В	5	26	5	22	ns
^t PHL	B GBA GAB		1	11	1	10	115

'AS622 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX								
			SN54	AS622	SN74	4S622	1				
			MIN	MAX	MIN	MAX	1				
^t PLH	A	D	5	28.5	5	24.5					
tPHL	1 ^ 1	В	1	8.5	1	8	ns				
^t PLH	В	1 8.5 1 5 30 5									
[†] PHL	†	. А	1	8.5	1	8	ns				
^t PLH	ĞВА	Α	5	26	5	22					
^t PHL	1 GBA	Α .	1	11.5	1	10	ns				
tPLH	GAB	В	5	26	5	23					
^t PHL	1 GAB	В	1	11.5	1	10.5	ns				

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 - REVISED MAY 1986

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'ALS632A and 'ALS633
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
ALS632A	52-pin	yes	3-State
'ALS633	52-pin	yes	Open-Collector
ALS634	48-pin	no	3-State
'ALS635	48-pin	no	Open-Collector

description

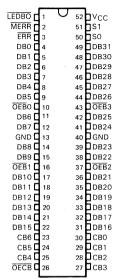
The 'ALS632A and 'ALS633 through 'ALS635 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('ALS632A and 'ALS633) or 48-pin ('ALS634 and 'ALS635) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

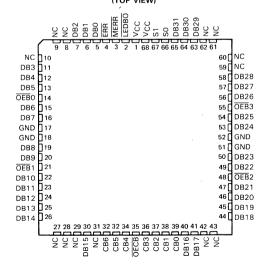
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'ALS632A, 'ALS633 . . . JD PACKAGE (TOP VIEW)



'ALS632A, 'ALS633 . . . FN PACKAGE (TOP VIEW)

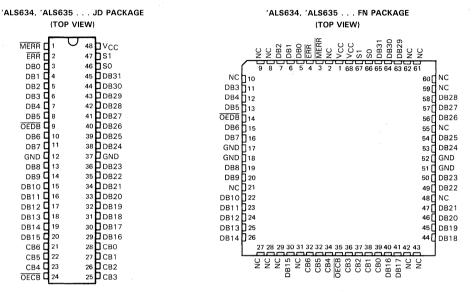


NC-No internal connection



Read-modify-write (byte-control) operations can be performed with the 'ALS632A and 'ALS633 EDACs by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEBO}}$ thru $\overline{\text{OEB}}$ 3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.



NC-No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CON S1	TROL SO	DATA I/O	DB CONTROL OEBn OR OEDB	DB OUTPUT LATCH ('ALS632A, 'ALS633) LEDBO	CHECK I/O	CB CONTROL OECB	ERROR ERR	FLAGS MERR
Write	Generate check word	L	L	Input	Н	×	Output check bits1	L	н	н

[†]See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.



TABLE 2. PARITY ALGORITHM

CHECK WORD													32	-BIT	DA	TΑ	wo	RD														
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	Х		Х	Х		Х					Х		Х	Х	Х			Х	-		Х		Х	Х	Х	Х		Х				Х
CB1				Х		Х		Х		Х		Х		Χ	Х	Х				Х		Х		Х		Χ		Χ		Х	Х	Χ
CB2	Х		Х			Х	Х		Х			Х	Х			Х	Х		Х			Х	Х		Х			Χ	Х			Х
CB3			Х	Х	Х				Х	Χ	Х				Х	Х			Х	Х	Х				Х	Χ	Х				Х	Х
CB4	Х	Х							Х	Х	Х	Х	Х	Х			Х	Х							Х	Χ	Х	Χ	Х	Χ		
CB5	Х	Х	Х	Х	Х	Х	Х	Х									Х	Х	Х	Х	X	Х	Х	Х								
CB6	х	Х	X	Х	Х	Х	Х	Х																	Х	Х	Х	Χ	Χ	Х	Χ	Х

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on MERR and a low on ERR, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both ERR and MERR, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBE	R OF ERRORS	ERROF	FLAGS	DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	ERR	MERR	DATA CORRECTION
0	0	Н	Н	Not applicable
1	0	L	Н	Correction
0	1	L	Н	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag (ERR) will be set low while the dual error flag (MERR) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.



TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CON' S1	TROL SO	DATA I/O	DB CONTROL OEBn OR OEDB	DB OUTPUT LATCH ('ALS632A, 'ALS633) LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS ERR MERR
Read	Read & flag	Н	L	Input	Н	Х	Input	Н	Enabled†
	Latch input			Latched			Latched		
Read	data & check	Н	Н	input	Н	L,	input	н	Enabled†
	bits			data			check word		
	Output			Output			Output		
Read	corrected data	Н	Н	corrected	L	Х	syndrome	L	Enabled† *
	& syndrome bits			data word			bits‡		

[†]See Table 3 for error description.

As the corrected word is made available on the data I/O port (DBO thru DB31), the check word I/O port (CBO thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

[‡]See Table 5 for error location.

TABLE 5. SYNDROME DECODING

SYNDROME BITS	ERROR	SYN	IDRO	ME	BITS	ERROR	Г	SY	ND	RO	VΙΕ	BIT	s	ERROR		SYN	IDF	RON	ΛE	віт	s	ERROR
6 5 4 3 2 1 0	ERRUR	6 5	4 3	2	1 0	ERNOR	6	5	4	3	2	1	0	ENNUN	6	5	4	3	2	1	0	ENNUN
LLLLLL	unc	LH	LL	L	LL	2-bit	F	l L	L	L	L	L	L	2-bit	Н	Н	L	L	L	L	L	unc
LLLLLLLH	2-bit	LH	LL	L	LH	unc	+	l L	L	L	L	L	Н	unc	Н	Н	L	L	L	L	Н	2-bit
LLLLLHL	2-bit	LH	L L	L	H L	DB7	+	l L	L	L	L	Н	L	unc	Н	Н	L	L	L	Н	L	2-bit
LLLLLHH	unc	LH	L L	L	н н	2-bit		l L	L	L	L	Н	Н	2-bit	Н	Н	L	L	L	Н	Н	DB23
LLLLHLL	2-bit	LH	L L	Н	LL	DB6	F	I L	L	L	Н	L	L	unc	Н	Н	L	L	Н	L	L	2-bit
LLLLHLH	unc	LH	L L	Н	L H	2-bit		l L	L	L	Н	L	Н	2-bit	Н	Н	L	L	Н	L	Н	DB22
LLLLHHL	unc	LH	L L	Н	H L	2-bit	F	l L	L	L	Н	Н	L	2-bit	Н	Н	L	L	Н	Н	L	DB21
LLLLHHH	2-bit	LH	LL	Н	н н	DB5		L	L	L	Н	Н	Н	unc	Н	Н	L	L	Н	Н	Н	2-bit
LLLHLL	2-bit	LH	L H	L	LL	DB4	F	l L	L	Н	L	L	L	unc	Н	Н	L	Н	L	L	L	2-bit
LLLHLLH	unc	LH	L H	L	LH	2-bit	+	ł L	L	Н	L	L	Н	2-bit	Н	Н	L	Н	Ł	L	Н	DB20
LLLHLHL	DB31	LH	L H	L	H L	2-bit		ł L	L	Н	L	Н	L	2-bit	Н	Н	L	Н	L	Н	L	DB19
LLLHLHH	2-bit	LH	L H	L	н н	DB3	+	ł L	L	Н	L	Н	Н	DB15	Н	Н	L	Н	L	Н	Н	2-bit
LLLHHLL	unc	LH	L H	Н	L L	2-bit	F	l L	L	Н	Н	L	L	2-bit	Н	Н	L	Н	Н	L	L	DB18
LLLHHLH	2-bit	LH	L H	Н	LH	DB2	⊦	ł L	L	Н	Н	L	Н	unc	Н	Н	L	Н	Н	L	Н	2-bit
LLLHHHL	2-bit	L H	L H	Н	H L	unc		l L	L	Н	Н	Н	L	DB14	Н	Н	L	Н	Н	Н	L	2-bit
LLLHHHH	DB30	LH	L H	Н	н н	2-bit		l L	L	Н	Н	Н	Н	2-bit	Н	Н	L	Н	Н	Н	Н	CB4
LLHLLLL	2-bit	LH	H L	L	LL	DB0	F	1 L	Н	L	L	L	L	unc	Н	Н	Н	L	L	L	L	2-bit
LLHLLLH	unc	LH	H L	L	LH	2-bit		1 L	Н	L	L	L	Н	2-bit	Н	Н	Н	L	L	L	Н	DB16
LLHLLHL	DB29	LH	H L	L	H L	2-bit	1	l L	Н	L	L	Н	L	2-bit	Н	Н	Н	L	L	Н	L	unc
LLHLLHH	2-bit	LH	H L	L	н н	unc	+	ł L	Н	L	L	Н	Н	DB13	Н	Н	Н	L	L	Н	Н	2-bit
LLHLHLL	DB28	LH	H L	Н	LL	2-bit	F	ł L	Н	L	Н	L	L	2-bit	Н	Н	Н	L	Н	L	L	DB17
LLHLHLH	2-bit	LH	H L	Н	LH	DB1	+	ł L	Н	L	Н	L	Н	DB12	Н	Н	Н	L	Н	L	Н	2-bit
LLHLHHL	2-bit	LH	H L	Н	H L	unc	+	1 L	Н	L	Н	н	L	DB11	Н	Н	Н	L	Н	Н	L	2-bit
LLHLHHH	DB27	LH	H L	Н	н н	2-bit	⊦	ł L	Н	L	Н	Н	Н	2-bit	Н	Н	Н	L	Н	Н	Н	CB3
LLHHLLL	DB26	LH	н н	L	LL	2-bit	F	1 L	Н	Н	L	L	L	2-bit	Н	Н	Н	Н	L	L	L	unc
LLHHLLH	2-bit	LH	н н	L	L H	unc	+	1 L	Н	Н	L	L	Н	DB10	Н	Н	Н	Н	L	L	Н	2-bit
LLHHLHL	2-bit	LH	н н	L	H L	unc	+	ł L	Н	Н	L	Н	L	DB9 /	Н	Н	Н	Н	L	Н	L	2-bit
LLHHLHH	DB25	LH	н н	L	н н	2-bit	+	ł L	Н	Н	L	Н	Н	2-bit	Н	Н	Н	Н	L	Н	Н	CB2
LLHHHLL	2-bit	LH	н н	Н	LL	unc	F	1 L	Н	Н	Н	L	L	DB8	Н	Н	Н	Н	Н	L	Ļ	2-bit
LLHHHLH	DB24	LH	н н	Н	LH	2-bit	+	ł L	Н	Н	Н	L	Н	2-bit	Н	Н	Н	Н	Н	L	Н	CB1
LLHHHHL	unc	LH	н н	Н	H L	2-bit	+	l L	Н	Н	Н	Н	L	2-bit	Н	Н	Н	Н	Н	Н	L	СВО
LLHHHHH	2-bit	LH	н н	Н	н н	СВ6	+	l L	Н	Н	Н	Н	Н	CB5	Н	Н	Н	Н	Н	Н	Н	none

CB X= error in check bit X DB Y= error in data bit Y 2-bit = double-bit error

unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'ALS632A and 'ALS633 devices are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking LEDBO from a low to a high.

Byte control can now be employed on the data word through the OEBO through OEB3 controls. OEBO controls DB0-DB7 (byte 0), OEB1 controls DB8-DB15 (byte 1), OEB2 controls DB16-DB23 (byte 2), and OEB3 controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and SO low. Table 6 lists the read-modify-write functions.



TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION		TROL SO	BYTEn†	ŌEBn†	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL	ERROR FLAG
Read	Read & Flag	Н	L	Input	Н.	×	Input	Н	Enabled
Read	Latch input data & check bits	Н	Н	Latched Input data	Н	L	Latched input check word	Н	Enabled
Read	Latch corrected data word into output latch	н	н	Latched output data word	Н	Н	Hi-Z Output Syndrome bits	L L	Enabled
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTEO Output unchanged BYTEO	H L	н	Output check word	L	н н

[†] OEBO controls DB0-DB7 (BYTE0), OEB1 controls DB8-DB15 (BYTE1), OEB3 controls DB16-DB23 (BYTE2), OEB3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632A and 'ALS633 thru 'ALS635 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the \overline{ERR} flag should be low. If a diagnostic data word with two errors in any bit location is applied, the \overline{MERR} flag should be low. After the checkword is latched into the input latch, it can be verified by taking \overline{OECB} low. This outputs the latched checkword. With the 'ALS632A and 'ALS633, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'ALS634 and 'ALS635 do not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('ALS632A and 'ALS633) and Table 8 ('ALS634 and 'ALS635) list the diagnostic functions.

TABLE 7. 'ALS632A, 'ALS633 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CON S1	TROL S0	DATA I/O	DB BYTE CONTROL OEBn	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS ERR MERR
Read & flag	Н	L	Input correct data word	Н	×	Input correct check bits	Н	н н
Latch input check word while data input latch remains transparent	L	Н	Input diagnostic data word [†]	Н	L	Latched input check bits	I	Enabled
Latch diagnostic data word into output latch	L	Н	Input diagnostic data word [†]	Н	н	Output latched check bits Hi-Z	L H	Enabled
Latch diagnostic data word into input latch	н	Н	Latched input diagnostic data word	н	Н	Output syndrome bits Hi-Z	L 	Enabled
Output diagnostic data word & syndrome bits	н	Н	Output diagnostic data word	L	н	Output syndrome bits Hi-Z	L H	Enabled
Output corrected diagnostic data word & output syndrome bits	н	Н	Output corrected diagnostic data word	L	L	Output syndrome bits Hi-Z		Enabled

[†]Diagnostic data is a data word with an error in one bit location except when testing the MERR error flag. In this case, the diagnostic data word will contain errors in two bit locations.

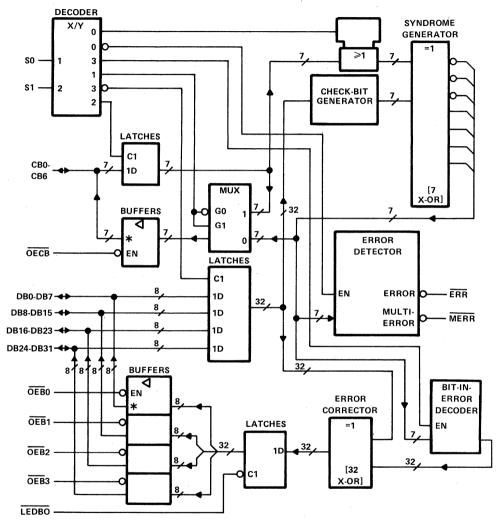
TABLE 8. 'ALS634, 'ALS635 DIAGNOSTIC FUNCTION

EDAC FUNCTION	CON	rrol	DATA I/O	DB CONTROL	CHECK I/O	CB CONTROL	ERRO	R FLAGS		
EDAC FUNCTION	S1	S0	DATA I/O	OEDB	CHECK I/O	OECB	ERR	MERR		
Read & flag	Н	L	Input correct data word	н	Input correct check bits	Н	Н	Н		
Latch input check bits while data input latch remains transparent	L	н	Input diagnostic data word [†]	Н	Latched input check bits	Н	En	abled		
Output input check bits	L	н	Input diagnostic data word [†]	Н	Output input check bits	L	En	abled		
Latch diagnostic data into input latch	н	н	Latched input diagnostic data word	Н	Output syndrome bits Hi-Z	L H	En	abled		
Output corrected diagnostic data word	Н	н	Output corrected diagnostic data word	Output L syndrome bits Hi-Z H		agnostic L		L H	En	abled

[†]Diagnostic data is a data word with an error in one bit location except when testing the MERR error flag. In this case, the diagnostic data word will contain errors in two bit locations.



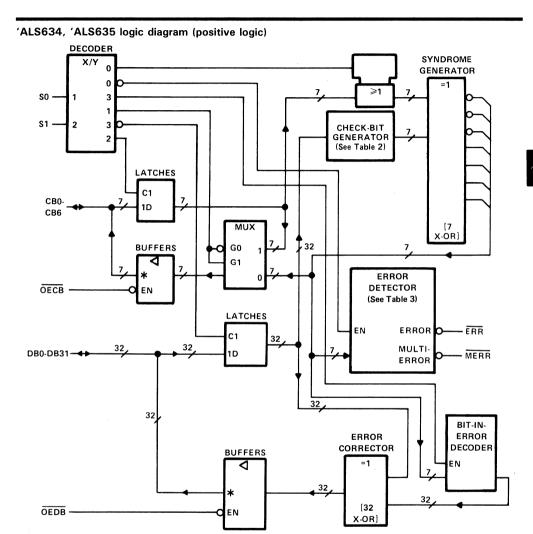
'ALS632A, 'ALS633 logic diagram (positive logic)



^{*&#}x27;ALS632A has 3-state (\(\nabla\)) check-bit and data outputs.

^{&#}x27;ALS633 has open-collector (A) check-bit and data outputs.

SN54ALS634, SN54ALS635, SN74ALS634, SN74ALS635 32 BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS



^{*&#}x27;ALS634 has 3-state (\(\nabla\)) check-bit and data outputs. 'ALS635 has open-collector ((2)) check-bit and data outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage: CB and DB
All others
Operating free-air temperature range:
SN74ALS632A, SN74ALS633 thru SN74ALS635 0°C to 70°C
Operating case temperature range:
SN54ALS632A, SN54ALS633 thru SN54ALS635
Storage temperature range -65 °C to 150 °C

recommended operating conditions

			SN	154ALS 154ALS THRU 154ALS NOM	633	SN	74ALS6 74ALS6 THRU 74ALS6 NOM	633	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	· 5	5.5	٠V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.6			0.8	V
		ERR or MERR			-0.4			-0.4	
ЮН	High-level output current	DB or CB 'ALS632A, 'ALS634			- 1			-2.6	mA
	1 - 1 - 1 - 1 - 1 - 1	ERR or MERR			4			8	mA
JOL	Low-level output current	DB or CB			12			24	mA
tw	Pulse duration	LEDBO low	45			25			ns
		(1) Data and check word before S0↑ (S1 = H)	15			10			
		(2) S0 high before LEDBO↑ (S1 = H) †	45			45			
		(3) LEDBO high before the earlier of SO↓ or S1↓ [†]	0			0			
		(4) LEDBO high before S11 (S0 = H)	0			0			
t _{su}	Setup time	(5) Diagnostic data word before S1↑ (S0 = H)	28			10			ns
		(6) Diagnostic check word before the later of S1↓ or S0↑	15			10			
		(7) Diagnostic data word before LEDBO↑ (S1 = L and S0 = H) [‡]	35			20			
		(8) Read-mode, SO low and S1 high	35			30			
		(9) Data and check word after S0↑ (S1 = H)	20			15			
		(10) Data word after S11 (S0 = H)	20			15			1
t _h	Hold time	(11) Check word after the later of S1↓ or S0↑	20			15			ns
		(12) Diagnostic data word after LEDBO↑ (S1 = L, S0 = H)‡	0			0			
t _{corr}	Correction time (see Figure 1)	65		58			ns	
TC	Operating case temperature		- 55		125		20 30 15 15 15		°C
TA	Operating free-air temperatur	е				0		70	°C

[†]These times ensure that corrected data is saved in the output data latch.

[‡]These times ensure that the diagnostic data word is saved in the output data latch.



SN54ALS632A, SN54ALS634, SN74ALS632A, SN74ALS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH 3-STATE OUTPUTS

'ALS632A, 'ALS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDI	TIONS	1	N54ALS N54ALS			174ALS6 N74ALS		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			-1.5	٧
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	vcc-	2		V _{CC} -	2		
∨он	DB or CB	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					V
	DB OI CB	$V_{CC} = 4.5 V$,	IOH = -2.6 mA				2.4	3.2		
	ERR or MERR	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	
\ \/	ENN OF WIENN	$V_{CC} = 4.5 \text{ V},$	IOL = 8 mA					0.35	0.5	V
VOL	DB or CB	V _{CC} = 4.5 V,	I _{OL} = 12 mA	T	0.25	0.4		0.25	0.4	\ \ \
	DB of CB	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	
1.	S0 or S1	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
11	All others	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	IIIA
	S0 or S1		V _I = 2.7 V			20			20	
ΊΗ	All others [‡]	$V_{CC} = 5.5 V$,	V = 2.7 V		-	20			20	μΑ
	S0 or S1					-0.4			-0.4	mA
l L	All others [‡]	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.1			-0.1	l mA
IO§		$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 30		-112	- 30		-112	mΑ
ICC		V _{CC} = 5.5 V,	See Note 1		150	250		150	250	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

'ALS632A switching characteristics, $V_{CC} = 4.5 \text{ V}$ to 5.5 V, $C_L = 50 \text{ pF}$, $T_{C} = -55 \,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$ for SN54ALS632A, $T_A = 0$ °C to 70 °C for SN74ALS632A

PARAMETER	FROM	то	TEST CONDITIONS	SN54A	ALS632A	SN74A	LS632A	LINUT
FARAMETER	(INPUT)	(OUTPUT)	1EST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
+ .	DB and CB	ERR	S1 = H, S0 = L, $R_L = 500 \Omega$	10	50	10	40	
^t pd	DB	ERR	S1 = L, S0 = H, $R_L = 500 \Omega$	10	43	10	40	ns
	DB and CB	MERR	S1 = H, S0 = L, R _L = 500 Ω	15	67	15	55	
^t pd	DB	MERR	S1 = L, S0 = H, R _L = 500 Ω	15	67	15	55	ns
^t pd	S0↓ and S1↓	СВ	R1 = R2 = 500 Ω	10	60	10	48	ns
^t PLH	S0↓ and S1↓	ERR	$R_L = 500 \Omega$	5	30	5	25	ns
^t pd	DB	СВ	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
^t pd	LEDBO↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
^t pd	S1†	СВ	S0 = H, R1 = R2 = 500 Ω	10	. 60	10	50	ns
t _{en}	OECB↓	СВ	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns
^t dis	OECB↑	СВ	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns
t _{en}	OEBO thru OEB3↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns
^t dis	OEBO thru OEB3↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	2	40	2	25	ns

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

SN54ALS634, SN74ALS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH 3-STATE OUTPUTS

'ALS634 switching characteristics, VCC = 4.5 V to 5.5 V, CL = 50 pF, TC = -55 °C to 125 °C for SN54ALS634, TA = 0 °C to 70 °C for SN74ALS634

PARAMETER	FROM	TO	TEST CONDITIONS	SN54	ALS634	SN74#	LS634	UNIT
PANAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
+ .	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	10	43	10	40	ns
^t pd	DB and CB	Lim	S1 = L, S0 = H, $R_L = 500 \Omega$	10	43	10	40	1115
t	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	15	67	15	55	ns
^t pd	DB and CB	·	S1 = L, S0 = H, $R_L = 500 \Omega$	15	67	15	55	1 115
^t pd	S0↓ and S1↓	СВ	R1 = R2 = 500 Ω	10	60	10	48	ns
^t PLH	S0↓ and S1↓	ERR	$R_L = 500 \Omega$	5	30	5	25	ns
^t pd	DB	СВ	S1 = L, S0 = L, R1 = R2 = 500 Ω	10	60	10	48	ns
^t pd	S1↑	СВ	S0 = H, R1 = R2 = 500 Ω	7	35	7	30	ns
t _{en}	OECB↓	СВ	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns
^t dis	OECB↑	СВ	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns
t _{en}	OEDB↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	30	ns
^t dis	OEDB↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	2	30	2	25	ns

PRODUCT PREVIEW

SN54ALS633, SN74ALS633 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH OPEN-COLLECTOR OUTPUTS

'ALS633 electrical characteristics over recommended operating temperature range (unless otherwise noted)

	ARAMETER	TEST CONDIT	TONE	SN54		33	SN	74ALS6	33	UNIT
,	ANAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
V _{IK}		$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			- 1.5			- 1.5	V
VoH	ERR or MERR	V _{CC} = 4.5 V to 5.5	V , $I_{OH} = -0.4 \text{ mA}$	Vcc-	2		V _{CC} -2	?		V
ІОН	DB or CB	$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V			0.1			0.1	mA
	ERR or MERR	$V_{CC} = 4.5 \text{ V},$	IOL = 4 mA		0.25	0.4		0.25	0.4	
VOL	ETTIT OF WILTHIT	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	V
VOL	DB or CB	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	ľ
	DB OF CB	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	
li .	S0 or S1	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
"	All others	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	IIIA
I _{IH}	S0 or S1	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
Hוי	All others [‡]	VCC = 3.5 V,	V - 2.7 V			20			20	μΑ
1 _{IL}	S0 or S1	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.4			-0.4	mA
11L	All others [‡]	ν _{CC} = 3.5 ν,	V - 0.4 V			-0.1			-0.1	IIIA
l _O §	ERR or MERR	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	-30		-112	mA
lcc		$V_{CC} = 5.5 \text{ V},$	See Note 1		150	250		150	250	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

'ALS633 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55 °C to 125 °C for SN54ALS633, T_A = 0 °C to 70 °C for SN74ALS633

PARAMETER	FROM	то	TEST CONDITIONS	SN54ALS633		SN74ALS633		UNIT	
PANAIVIE I EK	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNII	
+ .	DB and CB	ERR	S1 = H, S0 = L, R _L = 500 Ω	10	43	10	40	ns	
^t pd	DB	ERR	S1 = L, S0 = H, $R_L = 500 \Omega$	10	43	10	40	115	
+ .	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	15	67	15	55	ns	
^t pd	DB and CB		S1 = L, S0 = H, R _L = 500 Ω	15	67	15	55		
t _{pd}	S0↓ and S1↓	СВ	R _L = 680 Ω	10	75	10	60	ns	
^t PLH	S0↓ and S1↓	ERR	R _L = 500 Ω	5	30	5	25	ns	
^t pd	DB	СВ	S1 = L, S0 = L, $R_L = 680 \Omega$	10	70	10	60	ns	
t _{pd}	<u>LEDBO</u> ↓	DB	S1 = X, S0 = H, $R_L = 680 \Omega$	15	70	15	50	ns	
t _{pd}	S1↑	CB	S0 = H, R _L = 680 Ω	10	60	10	45	ns	
^t PLH	ŌECB↑	СВ	S1 = X, S0 = H, R _L = 680 Ω	2	35	2	30	ns	
^t PHL	OECB↓	СВ	S1 = X, S0 = H, $R_L = 680 \Omega$	2	35	2	30	ns	
^t PLH	OEBO thru OEB3↑	DB	S1 = X, S0 = H, $R_L = 680 \Omega$	2	35	2	30	ns	
^t PHL	OEBO thru OEB3↓	DB	S1 = X, S0 = H, $R_L = 680 \Omega$	2	35	2	30	ns	

 $^{^{\}ddagger} For I/O$ ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with SO and S1 at 4.5 V and all CB and DB pins grounded.

SN54ALS635, SN74ALS635 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH OPEN-COLLECTOR OUTPUTS

'ALS635 electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN	SN54ALS635			SN74ALS635		
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.5			- 1.5	V
Vон	ERR or MERR	$V_{CC} = 4.5 \text{ V to } 5.5$	5 V, I _{OH} = -0.4 mA	V _{CC} -	2		V _{CC} -2	2		V
IОН	DB or CB	$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V			0.1			0.1	mA
V _{OL} -	ERR or MERR	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	· V
	ENN OF WIENN	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA					0.35	0.5	
	DB or CB	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
		$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
l)	S0 or S1	$V_{CC} = 5.5 V$,	V _I = 7 V							mA
''	All others	$V_{CC} = 5.5 V$,	V _I = 5.5 V							IIIA
ΉΗ	S0 or S1	$V_{CC} = 5.5 V_{r}$	V _I = 2.7 V							μА
'IH	All others [‡]	ν _{CC} = 3.3 ν,	V == 2.7 V							μ^
1	S0 or S1	V _{CC} = 5.5 V,	V _I = 0.4 V							mA
'IL	All others [‡]									IIIA
IO§	ERR or MERR	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
¹ CC		$V_{CC} = 5.5 V$,	See Note 1		150			150		mA

 $^{^{\}dagger}\,AII$ typical values are at VCC = 5 V, TA = 25 °C.

'ALS635 switching characteristics, V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_C = -55 °C to 125 °C for SN54ALS635, T_A = 0 °C to 70 °C for SN74ALS635

PARAMETER	FROM	TO	TECT CONDITIONS	SN54ALS635	SN74ALS635	LINUT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN TYP [†] MAX	MIN TYP [†] MAX	UNIT
	DB and CB	ERR	S1 = H, S0 = L, $R_L = 500 \Omega$	26	26	ns
^t pd	DB	ERR	S1 = L, S0 = H, R _L = 500 Ω	26	26	115
.	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	40	40	ns
^{-t} pd	DB and CB		S1 = L, S0 = H, $R_L = 500 \Omega$	40	40	
t _{pd}	S0↓ and S1↓	СВ	R _L = 680 Ω	40	40	ns
^t PLH	S0↓ and S1↓	ERR	R _L = 500 Ω	14	14	ns
^t pd	DB	СВ	S1 = L, S0 = L, $R_L = 680 \Omega$	40	40	ns
t _{pd}	S1↑	DB	S0 = H, R _L = 680 Ω	40	40	ns
t _{PLH}	OECB↑	СВ	S1 = X, S0 = H, R _L = 680 Ω	24	24	ns
^t PHL	OECB↓	СВ	S1 = X, S0 = H, R _L = 680 Ω	24	24	ns
^t PLH	OEDB↑	DB	S1 = X, S0 = H, $R_L = 680 \Omega$	24	24	ns
^t PHL	<u>OEDB</u> ↓	DB	S1 = X, S0 = H, $R_L = 680 \Omega$	24	24	ns

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.



For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with SO and S1 at 4.5 V and all CB and DB pins grounded.

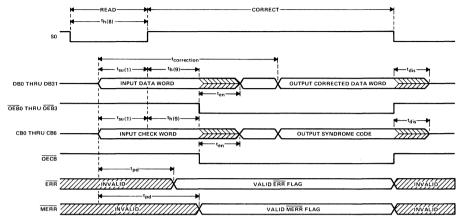


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

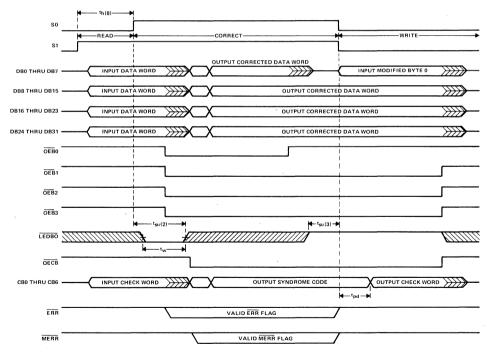


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS



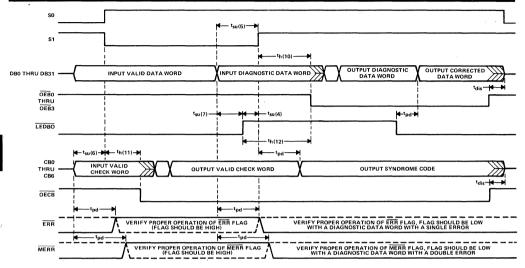


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

SN54AS632, SN54AS634 SN74AS632, SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2661, JANUARY 1986

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Built-In Diagnostic Capability
- Fast Write and Read Cycle Processing Times
- Byte-Write Capability . . . 'AS632
- Dependable Texas Instruments Quality and Reliability

DEVICE	PACKAGE	BYTE-WRITE	OUTPUT
'AS632	52-pin	yes	3-State
'AS634	48-pin	no	3-State

description

The 'AS632 and 'AS634 devices are 32-bit parallel error detection and correction circuits (EDACs) in 52-pin ('AS632) or 48-pin ('AS634) 600-mil packages. The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

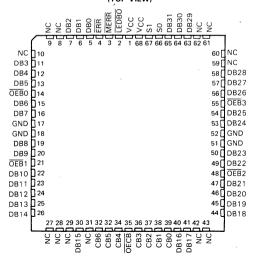
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

'AS632 . . . JD PACKAGE (TOP VIEW)

LEDBO [1	U	52	Ь∨сс
MERR	2		51	1 S1
ERR C	3		50	∃ so
DB0	4		49	DB31
DB1	5		48	D DB30
DB2	6		47	DB29
DB3	7		46	DB28
DB4 🗖	8		45	DB27
DB5	9		44	□ DB26
OEBO 🗖	10		43	OEB3
DB6	11		42	DB25
DB7	12		41	DB24
GND 🗆	13		40	GND
DB8	14		39	□ DB23
DB9	15		38	DB22
OEB1	16			OEB2
DB10 🗖	17		36	DB21
DB11 🗖	18		35	DB20
DB12 🔲	19		34	DB19
DB13 🗖	20		33	DB18
DB14 🔲	21		32	DB17
DB15	22		31	□DB16
СВ6	23		30	СВО
СВ5	24		29	СВ1
СВ4	25		28	СВ2
OECB 📮	26		27	П СВЗ

'AS632 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection



Read-modify-write (byte-control) operations can be performed with the 'AS632 EDAC by using output latch enable, LEDBO, and the individual OEBO thru OEB3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

'AS634 JD PACKAGE 'AS634 FN PACK (TOP VIEW) (TOP VIEW)	(AGE
NERR	50 NC NC Sec DB26 DB26 Sec DB27 Sec DB2
DB13	46 DB20
DB15	45 🛭 DB19 44 🗓 DB18
CB6 21 28 CB0 27 28 29 30 31 32 32 34 35 36 37 37 37 CB1 CB4 22 27 CB1 CB4 23 26 CB2 CB2 CB2 CB2 CB3 CB3 CB3 CB4 C	

NC-No internal connection

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE		CON S1	CONTROL S1 S0	DATA I/O	DB CONTROL OEBn OR OEDB	DB OUTPUT LATCH ('AS632) LEDBO	CHECK I/O	CB CONTROL OECB	ERROR ERR	FLAGS MERR
Write	Generate check word	L	L	Input	Н	· x	Output check bits†	L	н	н

[†]See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction.



SN54AS632, SN54AS634 SN74AS632, SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 2. PARITY ALGORITHM

CHECK WORD													32	-BIT	DA	TA	wc	RD														
ВІТ	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	Х		Х	Х		Х					Х		Х	X	Х			Х			X		Х	Х	Х	Х		Х				×
CB1				Х		Х		Х		Х		Χ		Х	Х	Х				Χ		Х		Х		Х		Х		Х	Х	Х
CB2	X		Х			Х	Х		Х			Х	Х			Х	Х		Х			Х	Х		Х			Х	Х			Х
CB3			Χ	Х	Х				Х	Х	Х				Х	Х			Х	Х	Х				х	х	х				Х	Х
CB4	Х	Х							Х	Х	Х	Χ	Х	Х			Х	Х							Х	Х	Х	Х	Х	Х		
CB5	Х	Х	Χ	Х	Х	Х	Х	Х									Х	Х	Х	Х	Х	X	X	Х								
CB6	x	Х	Х	Х	Х	Х	Х	Х																	Х	Х	Х	Χ	X	Х	Х	Х

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on MERR and a low on ERR, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both ERR and MERR, which is the interrupt indication for the CPU.

TABLE 3. ERROR FUNCTION

TOTAL NUMBE	R OF ERRORS	ERROP	FLAGS	DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	ERR	MERR	DATA CORRECTION
0	0	Н	Н	Not applicable
1	0	L	Н	Correction
0	1	L	Н	Correction
1	1	L	L	Interrupt
· 2	0	L	L	Interrupt
О	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag (ERR) will be set low while the dual error flag (MERR) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.



ALS and AS Circuits

32 BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CON'	TROL SO	DATA I/O	DB CONTROL OEBn OR OEDB	DB OUTPUT LATCH ('AS632) LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS ERR MERR
Read	Read & flag	Н	L	Input	Н	X	Input	Н	Enabled†
	Latch input			Latched			Latched		
Read	data & check	Н	Н	input	н	L	input	н	Enabled†
	bits			data			check word		1
	Output			Output			Output		
Read	corrected data	н	Н	corrected	L	X	syndrome	L	Enabled†
	& syndrome bits			data word			bits‡		

[†]See Table 3 for error description.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CBO thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

[‡]See Table 5 for error location.

SN54AS632, SN54AS634 SN74AS632. SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 5. SYNDROME DECODING

SYNDROME BITS		SYNDROME BITS	FDDGD	SYNDROME BITS	FRROR	SYNDROME BITS	EDDOD
6 5 4 3 2 1 0	ERROR	6 5 4 3 2 1 0	ERROR	6 5 4 3 2 1 0	ERROR	6 5 4 3 2 1 0	ERROR
LLLLLL	unc	LHLLLL	2-bit	HLLLLLL	2-bit	HHLLLLL	unc
LLLLLLH	2-bit	LHLLLLH	unc	HLLLLLH	unc	HHLLLLH	2-bit
LLLLLHL	2-bit	LHLLLHL	DB7	HLLLLHL	unc	HHLLLHL	2-bit
LLLLLHH	unc	LHLLLHH	2-bit	HLLLLHH	2-bit	HHLLLHH	DB23
LLLLHLL	2-bit	LHLLHLL	DB6	HLLLHLL	unc	HHLLHLL	2-bit
LLLLHLH	unc	LHLLHLH	2-bit	HLLLHLH	2-bit	H H L L H L H	DB22
LLLLHHL	unc	LHLLHHL	2-bit	HLLLHHL	2-bit	HHLLHHL	DB21
LLLLHHH	2-bit	L H L L H H H	DB5	HLLLHHH	unc	нн	2-bit
LLLHLLL	2-bit	LHLHLLL	DB4	HLLHLLL	unc	HHLHLLL	2-bit
LLLHLLH	unc	LHLHLLH	2-bit	H L L H L L H	2-bit	HHLHLLH	DB20
LLLHLHL	DB31	LHLHLHL	2-bit	HLLHLHL	2-bit	H H L H L H L	DB19
LLLHLHH	2-bit	LHLHLHH	DB3	нььньнн	DB15	HHLHLHH	2-bit
LLLHHLL	unc	LHLHHLL	2-bit	HLLHHLL	2-bit	HHLHHLL	DB18
LLLHHLH	2-bit	LHLHHLH	DB2	нссннсн	unc	HHLHHLH	2-bit
LLLHHHL	2-bit	L H L H H H L	unc	нггнннг	DB14	H H L H H H L	2-bit
LLLHHHH	DB30	LHLHHHH	2-bit	нггнннн	2-bit	ннгнннн	CB4
LLHLLLL	2-bit	LHHLLLL	DB0	HLHLLLL	unc	HHHLLLL	2-bit
LLHLLLH	unc	L H H L L L H	2-bit	HLHLLLH	2-bit	H H H L L L H	DB16
LLHLLHL	DB29	L H H L L H L	2-bit	HLHLLHL	2-bit	H H H L L H L	unc
LLHLLHH	2-bit		unc	нгнггнн	DB13	HHHLLHH	2-bit
LLHLHLL	DB28	LHHLHLL	2-bit	HLHLHLL	2-bit	HHHLHLL	DB17
LLHLHLH	2-bit	LHHLHLH	DB1	нгнгнгн	DB12	H H H L H L H	2-bit
LLHLHHL	2-bit	LHHLHHL	unc		DB11	нннінні	2-bit
LLHLHHH	DB27	L H H L H H H	2-bit	Нгнгннн	2-bit	ннн L н н н	CB3
LLHHLLL	DB26	LHHHLLL	2-bit	HLHHLLL	2-bit	HHHLLL	unc
LLHHLLH	2-bit	LHHHLLH	unc		DB10	ннннггн	2-bit
LLHHLHL	2-bit	LHHHLHL	unc	НГННГНГ	DB9,	H H H H L H L	2-bit
LLHHLHH	DB25	LHHHLHH	2-bit	нгннгнн	2-bit	ннннгнн	CB2
LLHHHLL	2-bit	LHHHHLL	unc	HLHHHLL	DB8	нннннгг	2-bit
LLHHHLH	DB24	L н н н ь н	2-bit	н	2-bit	ннннн	CB1
LLHHHHL	unc	Гнининг	2-bit	Нгннннг	2-bit	ннннны	CB0
LLHHHHH	2-bit	L н н н н н	СВ6	НГННННН	CB5	ннннннн	none

CB X= error in check bit X DB Y= error in data bit Y 2-bit = double-bit error unc = uncorrectable multibit error

read-modify-write (byte control) operations

The 'AS632 is capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, SO = L) to the latch input mode (SI = H, SO = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking LEDBO from a low to a high.

Byte control can now be employed on the data word through the OEBO through OEBO controls. OEBO controls DB0-DB7 (byte 0), OEB1 controls DB8-DB15 (byte 1), OEB2 controls DB16-DB23 (byte 2), and OEB3 controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and SO low. Table 6 lists the read-modify-write functions.



TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	í	TROL SO	BYTEn†	ŌEBn†	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL	ERROR FLAG ERR MERR
Read	Read & Flag	Н	L	Input	Н	×	Input	н .	Enabled
Read	Latch input data & check bits	н	н	Latched Input data	Н -	L	Latched input check word	н	Enabled
Read	Latch corrected data word into output latch	н	н	Latched output data word	н	н	Hi-Z Output Syndrome bits	<u>H</u>	Enabled
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTEO Output unchanged BYTEO	H 	н	Output check word	L	нн

[†] OEBO controls DB0-DB7 (BYTE0), OEB1 controls DB8-DB15 (BYTE1), OEB3 controls DB16-DB23 (BYTE2), OEB3 controls DB24-DB31 (BYTE3).

diagnostic operations

The 'AS632 and 'AS634 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the checkword is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known checkword. If the user applies a diagnostic data word with an error in any bit location, the $\overline{\text{ERR}}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{\text{MERR}}$ flag should be low. After the checkword is latched into the input latch, it can be verified by taking $\overline{\text{OECB}}$ low. This outputs the latched checkword. With the 'AS632, the diagnostic data word can be latched into the output data latch and verified. It should be noted that the 'AS634 does not have this pass-through capability because they do not contain an output data latch. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 ('AS632) and Table 8 ('AS634) list the diagnostic functions.

SN54AS632, SN54AS634 SN74AS632, SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

TABLE 7. 'AS632 DIAGNOSTIC FUNCTION

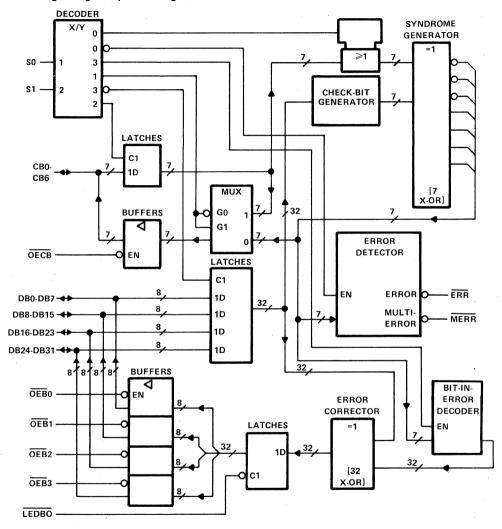
EDAC FUNCTION		TROL S0	DATA I/O	DB BYTE CONTROL OEBn	DB OUTPUT LATCH LEDBO	CHECK I/O	CB CONTROL OECB	ERROR FLAGS ERR MERR
Read & flag	Н	L	Input correct data word	Н	x	Input correct check bits	н	н н
Latch input check word while data input latch remains transparent	L	Н	Input diagnostic data word [†]	н	L	Latched input check bits	н	Enabled
Latch diagnostic data word into output latch	L	Н	Input diagnostic data word [†]	Н	н	Output latched check bits Hi-Z	L	Enabled
Latch diagnostic data word into input latch	н	Н	Latched input diagnostic data word	н	Н	Output syndrome bits Hi-Z	L 	Enabled
Output diagnostic data word & syndrome bits	н	н	Output diagnostic data word	L	Н	Output syndrome bits Hi-Z	L	Enabled
Output corrected diagnostic data word & output syndrome bits	Н	Н	Output corrected diagnostic data word	L	L	Output syndrome bits Hi-Z	L	Enabled

TABLE 8. 'AS634 DIAGNOSTIC FUNCTION

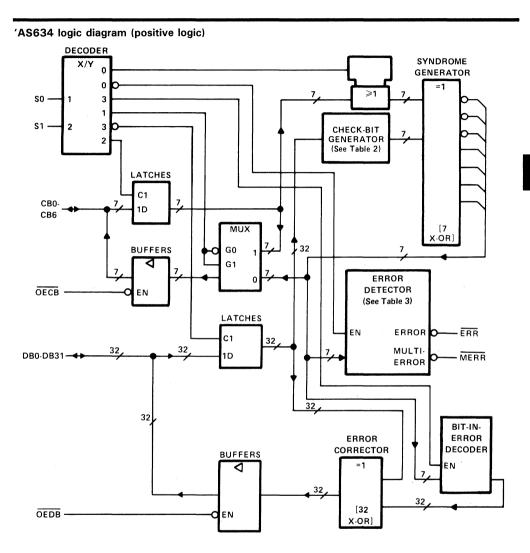
EDAC FUNCTION	CON	TROL	5474.10	DB CONTROL	CHECK I/O	CB CONTROL	ERROR FLAGS
EDAC FUNCTION	S1	S0	DATA I/O	OEDB	CHECK I/O	OECB	ERR MERR
Read & flag	н	L	Input correct data_word	н	Input correct check bits	н	`н н
Latch input check bits while data input latch remains transparent	L	Н	Input diagnostic data word [†]	Н	Latched input check bits	Н	Enabled
Output input check bits	L	Н	Input diagnostic data word [†]	Н	Output input check bits	L	Enabled
Latch diagnostic data into input latch	н	Н	Latched input diagnostic data word	н	Output syndrome bits Hi-Z	L	Enabled
Output corrected diagnostic data word	н	н	Output corrected diagnostic data word	L	Output syndrome bits Hi-Z	L H	Enabled

[†]Diagnostic data is a data word with an error in one bit location except when testing the MERR error flag. In this case, the diagnostic data word will contain errors in two bit locations.

'AS632 logic diagram (positive logic)



SN54AS634, SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC (see Note 1)
Input voltage: CB and DB
All others
Operating free-air temperature range:
SN74AS632, SN74AS6340°C to 70°C
Operating case temperature range:
SN54AS632, SN54AS634
Storage temperature range65°C to 150°C

recommended operating conditions

			1	N54AS		1	N74AS		UNIT
				NOM		MIN		MAX	0
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage		<u> </u>		0.8			0.8	V
		ERR or MERR			-0.4			-0.4	
ЮН	High-level output current	DB or CB	1		- 1			-2.6	mA
		ERR or MERR			4			8	
IOL	Low-level output current	DB or CB	1		12	<u> </u>		24	mA
t _w	Pulse duration	LEDBO low							ns
^t su	Setup time	(1) Data and check word before S0↑ (S1 = H) (2) S0 high before LEDBO↑ (S1 = H)↑ (3) LEDBO high before the earlier of S0↓ or S1↓↑ (4) LEDBO high before S1↑ (S0 = H) (5) Diagnostic data word before S1↑ (S0 = H) (6) Diagnostic check word before the later of S1↓ or S0↑ (7) Diagnostic data word before							ns
^t h	Hold time	LEDBO↑ (S1 = L and S0 = H) [‡]							ns
t _{corr}	Correction time (see Figure	1)							ns
TC	Operating case temperature		- 55		125				°C
TA	Operating free-air temperatu	ire ,				0		70	°C

[†] These times ensure that corrected data is saved in the output data latch.



[‡]These times ensure that the diagnostic data word is saved in the output data latch.

SN54AS632, SN54AS634, SN74AS632, SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH 3-STATE OUTPUTS

'AS632, 'AS634 electrical characteristics over recommended operating temperature range (unless otherwise noted)

P	ARAMETER	TEST CO	ONDITIONS		N54AS6 N54AS6		1	N74AS6 N74AS6		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
	All outputs	$V_{CC} = 4.5 \text{ V to 5.1}$	$5 \text{ V}, \text{ I}_{OH} = -0.4 \text{ mA}$	Vcc-2	2		Vcc-2	2		
∨он	DB or CB	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	DD 01 0D	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	ERR or MERR	$V_{CC} = 4.5 V,$	$I_{OH} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL	ETHT OF MILITA	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5] ,
100	DB or CB	$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4]
	55 01 05	$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
l _l	S0 or S1	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
''	All others	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	IIIA
ин	DB or CB [‡]	Vcc = 5.5 V,	$V_1 = 2.7 V$			20			20	
יור	All others [‡]	VCC = 3.5 V,	V - 2.7 V			20			20	μΑ
IIL.	S0 or S1	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.4			-0.4	
'IL	All others [‡]	ν _{CC} = 3.3 ν ,	V - 0.4 V			-0.1			-0.1	mA
IO§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Icc		$V_{CC} = 5.5 V,$	See Note 1		150			150		mA

NOTE 1: ICC is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

'AS632 switching characteristics, $V_{CC} = 4.5 \text{ V}$ to 5.5 V, $C_L = 50 \text{ pF}$, $T_C = -55 ^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$ for SN54AS632, $T_A = 0$ °C to 70 °C for SN74AS632

PARAMETER	FROM	то	TEST CONDITIONS	SN54AS632	SN74AS632	UNIT
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN TYP† MAX	MIN TYP [†] MAX	UNIT
	DB and CB	ERR	S1 = H, S0 = L, $R_L = 500 \Omega$	17	17	ns
^t pd	DB	ERR	S1 = L, S0 = H, R_L = 500 Ω	17	17	115
	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	26	26	ns
^t pd	DB	MERR	S1 = L, S0 = H, R _L = 500 Ω	26	26	115
t _{pd}	S0↓ and S1↓	СВ	R1 = R2 = 500 Ω	26	26	ns
^t PLH	S0↓ and S1↓	ERR	R _L = 500 Ω	9	9	ns
^t pd	DB	СВ	S1 = L, S0 = L, R1 = R2 = 500 Ω	26	26	ns
^t pd	LEDBO↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	17	17	ns
^t pd	S1↑	СВ	S0 = H, R1 = R2 = 500 Ω	26	26	ns
t _{en}	OECB↓	СВ	S0 = H, S1 = X, R1 = R2 = 500 Ω	12	12	ns
^t dis	OECB↑	СВ	S0 = H, S1 = X, R1 = R2 = 500 Ω	12	12	ns
t _{en}	OEBO thru OEB3↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	12	12	ns
^t dis	OEBO thru OEB3↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	12	12	ns

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

 $^{^{\}ddagger}For~I/O$ ports, the parameters $I_{\mbox{\scriptsize IH}}$ and $I_{\mbox{\scriptsize IL}}$ include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS634, SN74AS634 32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS WITH 3-STATE OUTPUTS

'AS634 switching characteristics, VCC = 4.5 V to 5.5 V, CL = 50 pF, TC = -55 °C to 125 °C for SN54AS634, TA = 0 °C to 70 °C for SN74AS634

DADAMETED	FROM	то	TEST CONDITIONS	SN54AS634	SN74AS634	
PARAMETER	(INPUT)	(OUTPUT)	TEST CONDITIONS	MIN TYP† MAX	MIN TYP† MAX	UNIT
+ .	DB and CB	ERR	S1 = H, S0 = L, R_L = 500 Ω	17	17	ns
^t pd	DD and CD	LINI	S1 = L, S0 = H, $R_L = 500 \Omega$	17	17	115
t	DB and CB	MERR	S1 = H, S0 = L, $R_L = 500 \Omega$	26	26	ns
^t pd	DB dild CB	IVILITY	S1 = L, S0 = H, $R_L = 500 \Omega$	26	26	113
^t pd	S0↓ and S1↓	СВ	R1 = R2 = 500 Ω	23	23	ns
tPLH	S0↓ and S1↓	ERR	$R_L = 500 \Omega$	9	9	ns
^t pd	DB	СВ	S1 = L, S0 = L, R1 = R2 = 500 Ω	23	23	ns
^t pd	S1↑	СВ	S0 = H, R1 = R2 = 500 Ω	23	23	ns
t _{en}	OECB↓	СВ	S1 = X, S0 = H, R1 = R2 = 500 Ω	12	. 12	ns
^t dis	OECB↑	СВ	S1 = X, S0 = H, R1 = R2 = 500 Ω	12	12	ns
t _{en}	OEDB↓	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	12	12	ns
^t dis	ŌEDB↑	DB	S1 = X, S0 = H, R1 = R2 = 500 Ω	12	12	ns

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

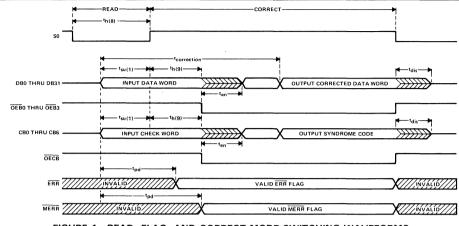


FIGURE 1. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

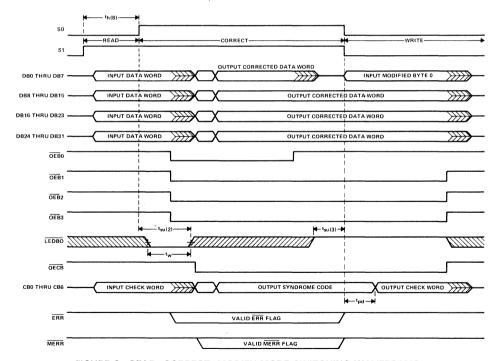


FIGURE 2. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS



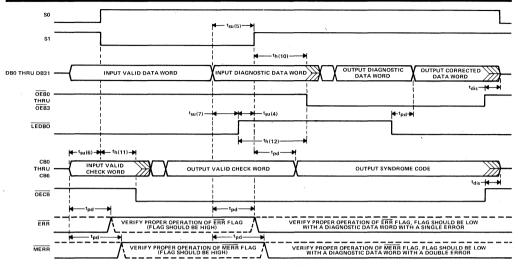


FIGURE 3. DIAGNOSTIC MODE SWITCHING WAVEFORM

SN54ALS638A, SN54ALS639A, SN54AS638, SN54AS639 SN74ALS638A, SN74ALS639A, SN74AS638, SN74AS639 OCTAL BUS TRANSCEIVERS

D2261, DECEMBER 1983 - REVISED MAY 1986

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- A Bus Outputs are Open-Collector; B Bus Outputs are 3-State
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $(\overline{\mathbb{G}})$ can be used to disable the device so the buses are isolated.

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS638A, 'AS638	Open-Collector	3-State	Inverting
'ALS639A, 'AS639	Open-Collector	3-State	True

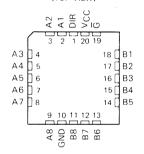
The -1 versions of the SN74ALS' parts are identical to the standard versions except that recommended maximum of I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54′ family, is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74′ family is characterized for operation from 0 °C to 70 °C.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)

DIR [1	U 20	Dvcc
A1 [2	19	ĪĠ
A2 []3	18	□ B1
АЗ []4	17	□ B2
A4 []5	16	□ B3
A5 []6	15	□ B4
A6 []7.	14	☐ B5
A7 []8	13	□ B6
A8 []9	12	B7
GND []10	11	□ B8

SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

	TROL	OPERA	ATION
INPUTS		'ALS638A	'ALS639A
G	DIR	'AS638	'AS639
L	L	B data to A bus	B data to A bus
L	Н	Ā data to B bus	A data to B bus
Н	X	Isolation	Isolation

logic symbols† logic diagrams (positive logic) 'ALS638A, 'AS638 'ALS638A, 'AS638 G (19) DIR (1) 3 EN1 [BA] 3 EN2 [AB] (<u>18)</u> B1 DIR (<u>17)</u> B2 А3 -В2 (13) B6 (12) B7 TO SIX OTHER TRANSCEIVERS 'ALS639A, 'AS639 'ALS639A, 'AS639 G (19) DIR (1) 3 EN1 [BA] 3 EN2 [AB] DIR (16) (15) (14) (13) (12) TO SIX OTHER TRANSCEIVERS

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS638A, SN54ALS639A, SN74ALS638A, SN74ALS639A OCTAL BUS TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Suppl	oltage, VCC
Input	tage: All inputs
	A bus I/O ports
	B bus I/O ports
Opera	g free-air temperature range:SN54ALS638A, SN54ALS639A
	SN74ALS638A, SN74ALS639A 0 °C to 70 °C
Storac	remperature range

recommended operating conditions

				54ALS6			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
Voн	High-level output voltage	A ports			5.5			5.5	٧
ЮН	High-level output current	B ports			-12			- 15	mA
lou	1 1	A D			12			24	^
lor	Low-level output current	A or B ports						48†	mA
TA	Operating free-air temperatu	re	-55		125	0		70	°C

 $^{^{\}dagger}$ The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS638A-1 and SN74ALS639A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COND	ITIONS		54ALS6		SN74ALS638A SN74ALS639A			UNIT
					TYP‡	MAX	MIN	TYP‡	MAX	
VIK		$V_{CC} = 4.5 V,$	I _I = ~18 mA			-1.5			-1.5	V
ЮН	A ports	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1			0.1	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$		V _{CC} -2			V _{CC} -2			
	B ports		$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
Voн	b ports	$V_{CC} = 4.5 V,$	l _{OH} ≈ −12 mA	2)
		$V_{CC} = 4.5 V,$	I _{OH} ≈ -15 mA				2			
		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
v_{OL}	A or B ports	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA		-			0.05		V
		(I _{OL} = 48 mA for -1 ver	(I _{OL} = 48 mA for -1 versions)					0.35	0.5	
	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
11	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	mA
L	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	
lн	A or B ports§	VCC = 5.5 V,	V = 2.7 V			20			20	μΑ
1	Control inputs	V F F V	V: 0.4.V			-0.1			-0.1	mA
ΊL	A or B ports§	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1			-0.1	mA
Io¶	B ports	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
			Outputs high		18	36		18	30	
	'ALS638A		Outputs low		25	48		26	41	
loo		V _{CC} = 5.5 V	Outputs disabled		16	35		16	30	mA
lcc		7 VCC - 3.5 V	Outputs high		25	45		25	40	1 1114
	'ALS639A		Outputs low		30	55		30	50	1
			Outputs disabled		33	60		33	54	

[‡]All typical values are at V_{CC} = 5 V, T_A = 25 °C
\$For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



'ALS638A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L R1 T _A	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_L = 680 \Omega \text{ (A outputs),}$ $R1 = R2 = 500 \Omega \text{ (B outputs),}$ $T_A = \text{MIN to MAX}$ $SN54ALS638A \qquad SN74ALS638A$			UNIT
			MIN	MAX	MIN	MAX	
^t PLH	Α	В	2	15	2	12	ns
tPHL	1 ^		2	15	2	12	115
tPLH	В	Α	8	30	8	25	ns
^t PHL	٦	^	8	35	8	30	113
^t PLH	G	A	5	30	5	25	ns
tPHL			10	50	10	45	113
^t PZH	G	В	5	25	5	20	ns
^t PZL	J	נ	5	28	5	22	115
^t PHZ	G	В	2	12	2	10	ns
^t PLZ	l	2	3	18	3	15	,,,,

'ALS639A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L R1 T _A	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T _A = MIN to MAX SN54ALS639A SN74ALS639A			UNIT
•			MIN	MAX	MIN	MAX	
tPLH		6	2	15	2	12	
^t PHL	A	В	2	15	2	12	ns
tPLH	В	A	10	35	10	30	
^t PHL	1	A	5	28	5	22	ns
^t PLH	G	A	10	35	10	30	ns
^t PHL		^	10	40	10	35	lis
tPZH	G	В	6	28	6	21	ns
tPZL]	5	8	30	8	25] ''5
^t PHZ	G	. В	2	12	2	10	ns
^t PLZ		. в		19	3	16	,13

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS638, SN54AS639, SN74AS638, SN74AS639 OCTAL BUS TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage: All inputs
A bus I/O ports
B bus I/O ports
Operating free-air temperature range: SN54AS638, SN54AS639 – 55 °C to 125 °C
SN74AS638, SN74AS639
Storage temperature range

recommended operating conditions

			1 -	SN54AS638 SN54AS639		SN74AS638 SN74AS639			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	٧
Voн	High-level output voltage	A ports			5.5			5.5	V
ЮН	High-level output current	B ports			-12			- 15	mA
lOL	Low-level output current	A or B ports			48			64	mA
TA	Operating free-air temperatu	re	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	TEST CONDITIONS		N54AS		SN74AS638 SN74AS639			UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5 V$,	$l_1 = -18 \text{ mA}$			-1.2			-1.2	V
IOH	A ports	$V_{CC} = 4.5 V$	$V_{OH} = 5.5 V$			0.1			0.1	mA
		$V_{CC} = 4.5 \text{ V, to } 5.5 \text{ V, I}_{OH} = -2 \text{ mA}$		v _{cc} -	2		v _{cc} -	2		
Voн	B ports	$V_{CC} = 4.5 V$,		2.4	3.2		2.4	3.2		V
VOH	B ports	$V_{CC} = 4.5 V,$	I _{OH} ≈ -12 mA	2.4						ľ
	$V_{CC} = 4.5 V$	lOH = −15 mA				2.4			Ī	
VOL	A or B ports	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.3	0.55				V
VOL	A of B ports	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 64 \text{ mA}$					0.35	0.55	`
l _l	Control inputs	$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1		-	0.1 mA	
l '1	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	IIIA
ЧН	Control inputs	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	- IΔ I
чн	A or B ports‡	VCC = 8.8 V,	V - 2.7 V			70			70	
կլ	Control inputs	.,				-0.5			-0.5	
'IL	A or B ports‡	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.75			-0.75	mA
lo§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 150	- 50		- 150	mA
	,		Outputs high		24	40		24	40	
	'AS638		Outputs low		75	122		75	122	
loo		$V_{CC} = 5.5 V$	Outputs disabled		37	61		37	61	
¹cc		VCC = 5.5 V	Outputs high		56	92		56	92	mA
'AS639	'AS639		Outputs low		95	154		95	154	ļ
		Outputs disabled		62	100		62	100		

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{o}C.$

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



 $^{{\}rm \ddagger For}\ I/O$ ports, the parameters $I_{\mbox{\scriptsize IH}}$ and $I_{\mbox{\scriptsize IL}}$ include the off-state output current.

'AS638 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _L R _L R1	C = 4.5 V to = 50 pF, = 500 Ω (A e = R2 = 500 = MIN to M	outputs),) Ω (B outp		UNIT
			MIN	MAX	MIN	MAX	
^t PLH	Α	В	2	8	2	7	ns
^t PHL		. ^	2	7.5	2	6.5	115
^t PLH	В	Α	5	23	5	20	
^t PHL	J	A	2	8	2	7	ns
^t PLH	G	Α	5	20	5	19	ns
tPHL		^	2	10	2	9	118
tPZH	G	В	2	10	2	8	no.
^t PZL	1 6	6 B	2	12	2	10	ns
tPHZ	G	В	2	8	2	7	ns
^t PLZ	,	B 1	2	12	2	10	

'AS639 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	CL RL R1	C = 4.5 V to = 50 pF, = 500 Ω (A = R2 = 500 = MIN to M	outputs), Ο Ω (B outp	outs),	UNIT	
		ı		SN54AS639 SN74AS639				
			MIN	MAX	MIN	MAX		
^t PLH	_A	В	2	11	2	9.5	ns	
^t PHL	7 ^		2	10.5	2	9	1115	
^t PLH	В	^	5	25	5	22		
^t PHL	7	A	2	10	2	9	ns	
^t PLH	G	Α	5	23	5	21.5		
^t PHL	7 "	A	2	12.5	2	11.5	ns	
^t PZH	Ğ	В	. 2	12	2	10.5		
[†] PZL	7 "	В	2	2 12 2	2	10.5	ns	
^t PHZ	G	В	2	7.5	2	7		
^t PLZ	7 '	В	2	12	2	10.5	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS640A THRU SN54ALS645A, SN54AS640 THRU SN54AS645 SN74ALS640A THRU SN74ALS645A, SN74AS640 THRU SN74AS645 OCTAL BUS TRANSCEIVERS

D2661, DECEMBER 1983-REVISED MAY 1986

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

	DEVICE	OUTPUT	LOGIC
	'ALS640A, 'AS640	3-State	Inverting
	'ALS641A, 'AS641	Open-Collector	True
i	'ALS642A, 'AS642	Open-Collector	Inverting
i	'ALS643A, 'AS643	3-State	True and Inverting
	'ALS644A, 'AS644	Open-Collector	True and Inverting
į	'ALS645A, 'AS645	3-State	True

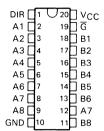
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so the buses are effectively isolated.

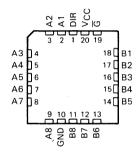
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)

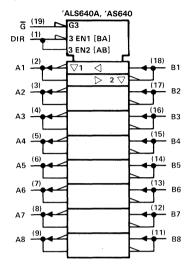


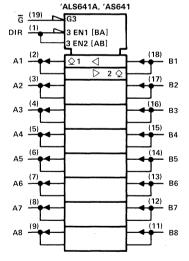
FUNCTION TABLE

CON	TROL		OPERATION							
INPUTS		'ALS640A, 'AS640	'ALS641A, 'AS641	'ALS643A, 'AS643						
Ğ	DIR	'ALS642A, 'AS642	'ALS645A, 'AS645	'ALS644A, 'AS644						
L	L	B data to A bus	B data to A bus	B data to A bus						
L	Н	Ā data to B bus	A data to B bus	Ā data to B bus						
Н	Х	Isolation	Isolation	Isolation						

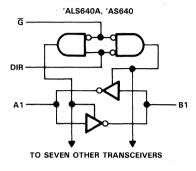
SN54ALS640A, SN54ALS641A, SN54AS640, SN54AS641 SN74ALS640A, SN74ALS641A, SN74AS640, SN74AS641 OCTAL BUS TRANSCEIVERS

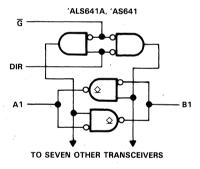
logic symbols†





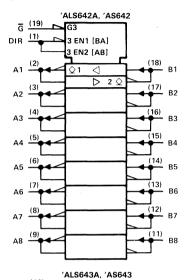
logic diagrams (positive logic)

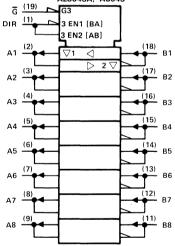




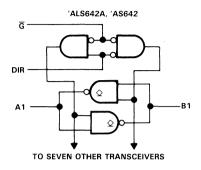
 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

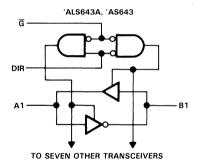
logic symbols†





logic diagrams (positive logic)

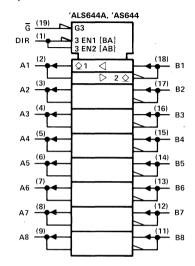


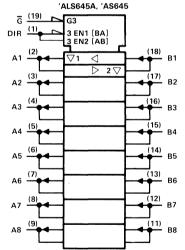


 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

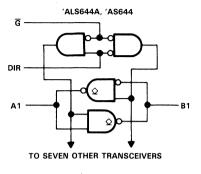
SN54ALS644A, SN54ALS645A, SN54AS644, SN54AS645 SN74ALS644A, SN74ALS645A, SN74AS644, SN74AS645 OCTAL BUS TRANSCEIVERS

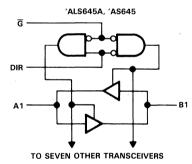
logic symbols†





logic diagrams (positive logic)





[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

SN54ALS640A, SN54ALS643A, SN54ALS645A SN74ALS640A, SN74ALS643A, SN74ALS645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCÇ	
Input voltage: All inputs	
I/O ports	
Operating free-air temperature range: SI	N54ALS640A, SN54ALS643A, SN54ALS645A – 55 °C to 125 °C
SI	N74ALS640A, SN74ALS643A, SN74ALS645A 0 °C to 70 °C
Storage temperature range	

recommended operating conditions

		SN	SN54ALS640A SN54ALS643A SN54ALS645A		SN74ALS640A SN74ALS643A SN74ALS645A			UNIT
		MIŅ	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-12			-15	mA
lou	1 1			12			24	
lor	Low-level output current						48†	mA
TA	Operating free-air temperature	-55		125	0		70	°C

[†] The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

The 48-mA limit applies for the SN74ALS640A-1, SN74ALS643A-1, and SN74ALS645A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COMP	ITIONS	S	N54AL	S'	S	N74AL	S'	UNIT
,	ARAMETER	TEST COND	ITIONS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNII
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			-1.5	٧
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
Varia	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v	
VOH		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2						· •
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$				2			
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 12 \text{ mA} \qquad 0.25 0.4$			0.25	0.4					
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	V
		$(l_{OL} = 48 \text{ mA for } -1 \text{ ver}$						0.35	0.5	
1.	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lį	A or B ports	$V_{CC} = 5.5 V,$	$V_I = 5.5 V$			0.1			0.1	IIIA
l	Control inputs	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
ΊΗ	A or B ports§	VCC = 5.5 V,	V = 2.7 V			20			20	L
Iμ	Control inputs	V _{CC} = 5.5 V,	$V_1 = 0.4 \text{ V}$			-0.1			-0.1	mA
ЧL	A or B ports§	1	·			-0.1			-0.1	
101		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	-30		-112	mA
			Outputs high		19	35		19	30	
	'ALS640A		Outputs low		27	45		27	40	
			Outputs disabled		28	48		28	43	
			Outputs high		25	37		25	35	
Icc	'ALS643A	$V_{CC} = 5.5 V$	Outputs low		33	47		33	45	mA
			Outputs disabled		35	50		35	48	
		Outputs high		30	48		30	45		
	'ALS645A		Outputs low		36	60		36	55	
			Outputs disabled		38	63		38	58	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios.



 $[\]S$ For I/O ports, the parameters IIH and IIL include the off-state output current.

SN54ALS640A, SN54ALS643A, SN54ALS645A SN74ALS640A, SN74ALS643A, SN74ALS645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

'ALS640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5~V$ to 5.5 V, $C_L=50~pF$, $R1=500~\Omega$, $R2=500~\Omega$, $T_A=MIN~to~MAX$		V ,	UNIT	
			SN54A	LS640A	SN74/	ALS640A	
			MIN	MAX	MIN	MAX	
^t PLH	A or B	B or A	2	14	2	1-1	ns
^t PHL	AUIB	BOIA	2	13	2	10	1 "s
^t PZH	G	A or B	5	25	5	21	ns
tPZL		AOIB	8	27	8	24	115
^t PHZ	G	A or B	2	12	2	10	ns
^t PLZ	9	A or B	3	20	3	15] ''s

'ALS643A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $SN54ALS643A \qquad SN74ALS643A$			UNIT	
			MIN	MAX	MIN	MAX	1
[‡] PLH	А	В	2	15	2	13	ns
^t PHL		B	2	13	2	11	1 '''
^t PLH	В	А	2	15	2	13	ns
tPHL]	and the second s	2	13	2	11] '''
^t PZH	G	А	5	28	5	25	ns
tpZL			5	28	5	25] '''
^t PHZ	G	Α	2	12	2	10	ns
^t PLZ			3	22	3	17] '''
^t PZH	G	В	5	28	5	25	ns
^t PZL	1		5	28	5	25] ""
^t PHZ	G	В	2	12	2	10	ns
^t PLZ			3	22	3	17	

'ALS645A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$			UNIT
			SN54A	LS645A	SN74A	LS645A	
			MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	1	19	3	10	ns
^t PHL	A 01 B	1 BOYA F	1	14	3	10	7 ''*
^t PZH		A or B	2	30	5	. 20	ns
tPZL	,	7016	2	29	5	20	
tPHZ	G	A or B	2	14	2	10	ns
tPLZ		7016	2	30	4	15	7 115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS641A, SN54ALS642A, SN54ALS644A SN74ALS641A, SN74ALS642A, SN74ALS644A OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings o	ver operating mee-air temperature range (unless otherwise noted)	
Supply voltage, VCC	7 V	
Input voltage: All inputs a	and I/O ports	
Operating free-air tempera		
	SN54ALS641A, SN54ALS642A, SN54ALS644A 55 °C to 125 °C	
	SN74ALS641A, SN74ALS642A, SN74ALS644A 0°C to 70°C	
Storage temperature range	-65°C to 150°C	

recommended operating conditions

		sn	SN54ALS641A SN54ALS642A SN54ALS644A		SN74ALS641A SN74ALS642A SN74ALS644A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output current			5.5			5.5	V
1	Low-level output current			12			24	mA
lor	Low-lever output current						48†	1 '''^
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}\,\text{The}$ extended limits apply only if VCC is maintained between 4.75 V and 5.25 V.

The 48-mA limit applies for the SN74ALS641A-1, SN74ALS642A-1, and SN74ALS644A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER					54ALS6			74ALS6		
		TEST CONDITIONS			SN54ALS642A		SN74ALS642A			UNIT
		1201 GGNSTINGTO		SN	SN54ALS644A			SN74ALS644A		
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.5			- 1.5	V
Іон		$V_{CC} = 4.5 \text{ V},$	$V_{OH} = 5.5 V$			0.1			0.1	mA
		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 24 \text{ mA}$					0.35	0.5	V
		$(I_{OL} = 48 \text{ mA for -1})$	versions)					0.33	0.5	
14	Control inputs	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
'1	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	1111/
ΊΗ	Control inputs	V _{CC} = 5.5 V,	= 5.5 V, $V_1 = 2.7 V$			20			20	μА
"H	A or B ports§	VCC = 5.5 V,				20			20] "
1	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
կլ	A or B ports§	VCC = 3.5 V,	V = 0.4 V			-0.1			-0.1	1 '''
	'ALS641A		Outputs high		25	40		25	37	
	ALS041A		Outputs low		33	50		33	47	
	'ALS642A	V _{CC} = 5.5 V	Outputs high		8	15		8	15	m _A
1CC	AL3042A	vCC = 5.5 v	Outputs low		18	28		18	28] '''^
	'ALS644A		Outputs high		16	32		16	29]
	AL3044A		Outputs low		25	44		25	40	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



SN54ALS641A, SN54ALS642A, SN54ALS644A SN74ALS641A, SN74ALS642A, SN74ALS644A OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

'ALS641A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	$\begin{array}{c} \text{V}_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}, \\ \text{C}_{\text{L}} = 50 \text{ pF}, \\ \text{TO} \\ \text{R}_{\text{L}} = 680 \Omega, \\ \text{(OUTPUT)} \\ \text{T}_{\text{A}} = \text{MIN to MAX} \end{array}$		ν,	UNIT		
			SN54A	LS641A	SN74	ALS641A	
	•		MIN	MAX	MIN	MAX	
^t PLH	A or B	B or A	5	30	5	25	ns
^t PHL	AOIB	B OI A	. 3	23	3	18] '''
^t PLH	G	A or B	8	35	8	30	ns
^t PHL	9	A 01 B	8	35	8	30	1115
^t PLH	DIR	A or B	8	37	8	32	ns
tPHL	DIII	A 01 B	8	37	8	32	113

'ALS642A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX SN54ALS642A SN74ALS642A MIN MAX MIN M.			UNIT	
^t PLH	Α	В	10	35	10	30	
^t PHL	^		5	25	5	22	ns
^t PLH	G or DIR	A or B	10	35	10	30	ns
^t PHL	G of Bill	AUIB	15	43	15	38] ''*

'ALS644A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS644A SN74ALS64				UNIT
			MIN	MAX	MIN	MAX	
^t PLH	Α	В	10	35	10	30	ns
^t PHL	^		5	25	5	22	1 "
^t PLH	Б	А	10	35	10	30	ns
. t _{PHL}	В		5	23	5	21	
^t PLH		Α	8	35	8	30	ns
tPHL	G	^	10	38	10	35	7 "
^t PLH		В	8	31	8	26	ns
tPHL	G	B	15	40	15	35	1 115
t _{PLH}	DIR		8	31	8	26	ns
^t PHL	DIK	A	10	40	10	35	1 118
tPLH	DIR	В	10	35	10	30	T
tPHL	אוט	R	15	40	15	35	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS640, SN54AS643, SN54AS645 SN74AS640, SN74AS643, SN74AS645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage: All inputs	
I/O ports	5.5 V
Operating free-air temperature range:	
SN54AS640, SN54AS643, SN54	4AS645

recommended operating conditions

		s	SN54AS640 SN54AS643 SN54AS645		SN74AS640 SN74AS643 SN74AS645			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ТОН	High-level output current			- 12			- 15	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEST COMP	TIONS	T	SN54AS	3'		SN74AS	3'	UNIT
Ρ,	ARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	Vcc-	2		Vcc-	2		
		V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.4	3.2		. 2.4	3.2] _v
Vон		V _{CC} = 4.5 V,	IOH = -12 mA	2.4] ' '
1		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2.4]
V		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA		0.30	0.55				V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 64 mA					0.35	0.55	1
1.	Control inputs	$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1			0.1	mA
l _l	A or B ports	$V_{CC} = 5.5 V$,	$V_{I} = 5.5 \text{ V}$			0.1			0.1	IIIA
I	Control inputs	Vcc = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ΊΗ	A or B ports‡	vCC - 5.5 v,	V = 2.7 V			70			70	1 μΑ
t	Control inputs	Vcc = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
ΊL	A or B ports‡	VCC = 5.5 V,	VI = 0.4 V	-0.75				-0.75] '''^	
IO§		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 50		- 150	-50		- 150	mA
			Outputs high		37	58		37	58	
	'AS640		Outputs low		78	123		78	123	1
			Outputs disabled		51	80		51	80]
			Outputs high		48	79		48	79	
Icc	'AS643	$V_{CC} = 5.5 V$	Outputs low		88	143		88	143	mA
			Outputs disabled		61	100		61	100	
			Outputs high		62	97		62	97	ļ
	'AS645		Outputs low		95	149		95	149]
			Outputs disabled		79	123		79	123	l

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to MAX}$		5 V,	UNIT	
			SN54AS640		SN74AS640		Ì
			MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	2	8	2	7	ns
^t PHL	A 01 B	. BUIA	2	7	2	6	115
^t PZH	G	A or B	2	10	2	8	ns
tPZL		A 01 B	2	12	2	10	1 '''s
tPHZ	G	A or B	2	9	2	8	ns
t _{PLZ}		7018	2	16	2	13] ''S

'AS643 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				
			MIN	AS643 MAX	MIN	AS643 MAX	
tPLH			2	10	2	8	
tPHL	А	В	2	7.5	2	7	ns
^t PLH	В	^	2	11.5	2	10	
^t PHL	В	A	2	10	2	9	ns
^t PZH	G	А	2	13	2	11	
^t PZL	G	^	2	_ 13	2	11	ns
^t PHZ	G	·A	2	8.5	2	7.5	ns
^t PLZ	G	·A	2	12	2	10.5	1115
^t PZH	G	В	. 2	11.5	2	10	ns
tPZL	<u> </u>		2	12	2	10] ''5
^t PHZ	G	В	2	8	2	7	ns
tPLZ	9		2	12	2	10	115

'AS645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				
			SN54	SN54AS645		SN74AS645	
			MIN	MAX	MIN	MAX	1
t _{PLH}	A or B	B or A	2	11	2	9.5	ns
tPHL	AOID	BOIA	2	10.5	2	9] ""
^t PZH	G	A or B	. 2	12	2	11	ns
^t PZL		7016	2	12	2	10] ''`
^t PHZ	G	A or B	2	8	2	7	ns
^t PLZ		A 01 B	2	13	2	12] '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS641, SN54AS642, SN54AS644 SN74AS641, SN74AS642, SN74AS644 OCTAL BUS TRANSCEIVERS WITH OPEN COLLECTOR OUTPUTS

absolute maximum ratings o	ver operating free-air temperature range (uniess other	erwise noted)
Supply voltage, VCC		7 V
Input voltage: All inputs a	and I/O ports	7 V
Operating free-air tempera	ture range:	
	SN54AS641, SN54AS642, SN54AS644	-55°C to 125°C
	SN74AS641, SN74AS642, SN74AS644	0°C to 70°C
Storage temperature range	9	-65°C to 150°C

recommended operating conditions

		s	SN54AS641			SN74AS641			
		s	N54AS6	42	Si	42	UNIT	1	
		Si	SN54AS644			SN74AS644			
		MIN	NOM	MAX	MIN	NOM	MAX]	l
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	1
VIH	High-level input voltage	2			2			V	1
VIL	Low-level input voltage			0.8			0.8	V	1
Voн	High-level output current			5.5			5.5	V]
lOL	Low-level output current			48			64	V]
TA	Operating free-air temperature	- 55		125	0		70	°C]

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST C	TEST CONDITIONS		SN54AS641 SN54AS642 SN54AS644			SN74AS641 SN74AS642 SN74AS644		
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	$I_I = -18 \text{ mA}$			-1.2			- 1.2	V
Іон		$V_{CC} = 4.5 V,$	$V_{OH} = 5.5 V$			0.1			0.1	mA
N-		$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.3	0.55				V
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 64 \text{ mA}$					0.35	0.55] `]
l _l	Control inputs	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
11	A or B ports	$V_{CC} = 5.5 V$,	$V_{ } = 5.5 V$			0.1			0.1] ""^
ΊΗ	Control inputs	V _{CC} = 5.5 V,	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$			20			20 .	μΑ
1111	A or B ports [‡]	VCC = 5.5 V,	1, 2., .			70			70	μ, ,
I _I L	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
'IL	A or B ports [‡]	V((= 5.5 V)	V - 0.4 V ,		-0.75			-0.75		
	'AS641		Outputs high		50	82		50	82	
	A5641		Outputs low		84	136		84	136	
	'AS642	V 5.5.V	Outputs high		25	42		25	42	mA
lcc	A3042	AS642 V _{CC} = 5.5 V Outputs low		64	104		64	104] '''^ [
	'AS644		Outputs high		38	62		38	62]
	A3044		Outputs low		76	124		76	124]



 $^{^{\}dagger}$ All typical values are at VCC = 5 V, T_A = 25 °C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS641 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = MIN$, }, to MAX		UNIT
			SN54AS641 SN74AS641				
	·		MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	5	23	5	21	ns
tPHL .]	1	8.5	1	7.5] '''
tpLH	G	A or B	5	24	5	21	ns
tPHL)	7 01 15	1	10	1	9	1,13
tPLH	DIR	A or B	5	26	5	22	ns
tPHL	DIN	A 01 B	1	11	1	10	113

'AS642 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4.5 C _L = 50 pr R _L = 500 sr T _A = MIN	=, ì,	V,	UNIT
			SN54AS642 SN74AS64		AS642	1	
			MIN	MAX	MIN	MAX	1
tPLH		B or A	5	28.5	5	24	ns
tPHL	A or B		1	8.5	1	7.5	1 "5
tPLH	G	A or B	5	- 25	5	22	ns
tPHL	ď	AorB	1	11	1	10] ""
. tplH	DIR	A or B	5	26.5	5	23.5	ns
^t PHL	Din .	7 01 5	1	12.5	1	11.5] '''

'AS644 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \text{ G}$ $T_A = \text{MIN}$	=, Ω,	<i>1</i> ,	UNIT
			SN54	AS644	SN74.]	
			MIN	MAX	MIN	MAX	
^t PLH	А	В	5	28.5	5	24	ns
^t PHL	*		1	8.5	1	7.5	7 ''`
^t PLH	В	А	5	23	5	21	ns
^t PHL	, в	A	1	8.5	1	7.5	7 '''
^t PLH	G	A or B	5	24	5	21	ns
^t PHL	ď	A 01 B	1	10	1	9] ''3
^t PLH	DIR	A or B	5	26	5	22	ns
^t PHL	DIK	A 01 B	1	11	1	10	1 113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1983-MAY 1986

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS647	Open-Collector	True
'ALS648, 'AS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

description

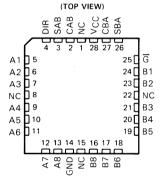
These devices consist of bus transceiver circuits. with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (G) and direction (DIR) pins are provided to control the transceiver functions. In the

SN54ALS', SN54AS', ... JT PACKAGE SN74ALS', SN74AS' . . . DW OR NT PACKAGE (TOP VIEW)

САВ[1	U 24	D	Vcc
SAB[2	23		CBA
DIR [3	22		SBA
A1 []4	21		G
A2 [] 5	20		B1
A3 []6	19		B2
A4 []7	18		В3
A5 []8	17		В4
A6 [] 9	16		B5
A7 [10	15		B6
A8 [11	14		В7
GND [112	13	h	B8-

SN54ALS', SN54AS' . . . FK PACKAGE SN74ALS', SN74AS' . . . FN PACKAGE



NC-No internal connection

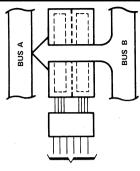
transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \overline{G} is active (low). In the isolation mode (control \overline{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum IOI is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

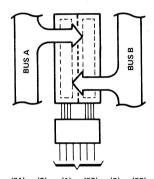
The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.





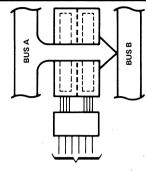
(21) (3) (23) (22) (1) (2) G DIR CAB CBA SAB SBA х x х L

REAL-TIME TRANSFER BUS B TO BUS A



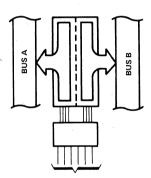
(21)(3) (1) (23)(2) (22)G DIR CAB CBA SAB SBA х х х х х x х х х ×

STORAGE FROM A, B, OR A AND B



(21) (3) (1) (23) (2) (22) G DIR CAB CBA SAB SBA L H X X L X

REAL-TIME TRANSFER BUS A TO BUS B



(21)(3) (23)(2) (22)(1) G DIR CAB CBA SAB SBA HorL х н х н HorL х **TRANSFER** STORED DATA

TO A OR B

SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

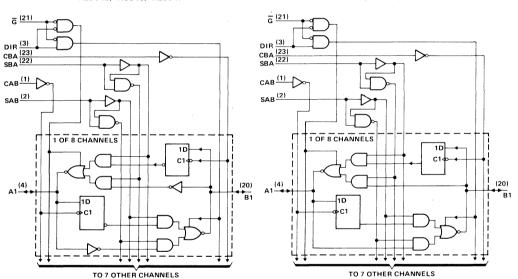
		INF	PUTS			DATA	A I/O	OPERATION OR FUNCTION			
								'ALS646, 'ALS647	'ALS648, 'ALS649		
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS646	'AS648		
X	X	1	X	Х	X	Input	Unspecified [†]	Store A, B unspecified [†]	Store A, B unspecified [†]		
×	X	X	1	Χ	X	Unspecified †	Input	Store B, A unspecified [†]	Store B, A unspecified †		
Н	X	1	1	X	X	Input	1	Store A and B Data	Store A and B Data		
Н	Χ	H or L	H or L	Х	X	input	Input	Isolation, hold storage	Isolation, hold storage		
L	L	Х	X	Х	L	Outrout	lane	Real-Time B Data to A Bus	Real-Time B Data to A Bus		
L	L	X	H or L	X	Н	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus		
L	Н	X	X	L	X		Outnut	Real-Time A Data to B Bus	Real-Time A Data to B Bus		
L	Н	H or L	Х	Н	Х	Input	Output	Stored A Data to B Bus	Store A Data to B Bus		

[†]The data output functions may be enabled or disabled by various signals at the \overline{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

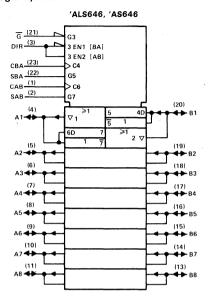
'ALS646, 'AS646, 'ALS647

'ALS648, 'AS648, 'ALS649

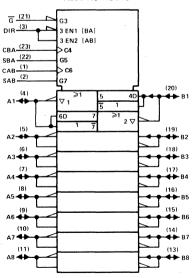


Pin numbers shown are for DW, JT, and NT packages.

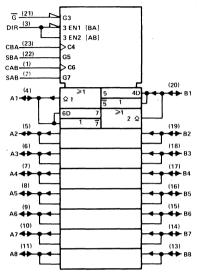
logic symbols†



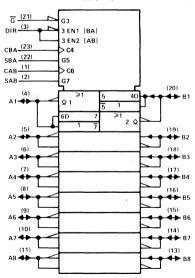
'ALS648, 'AS648



'ALS647



'ALS649



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



SN54ALS646, SN74ALS646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	٧
Input voltage: Control inputs	V
I/O ports	٧
Operating free-air temperature range: SN54ALS646	°C
SN74ALS646 0°C to 70	٥С
Storage temperature range	°C

recommended operating conditions

		SI	SN54ALS646			SN74ALS646			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			- 12			- 15	mA	
lau	Low-level output current			12			24	mA	
lor							48 [†]] ""A]	
fclock	Clock frequency	0		35	0		40	MHz	
t _w	Pulse duration, clocks high or low	14.5			12.5			ns	
t _{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns	
th	Hold time, A after CAB↑ or B after CBA↑	0		-	0			ns	
TA	Operating free-air temperature	- 55		125	0		70	°C	

 $^{^{\}dagger}$ The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS646-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	******	TF0T 0		SN	54ALS	646	SI	N74ALS	646	
PAR	AMETER	TEST CO	ONDITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.9$	$5 \text{ V, I}_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		v _{cc} -	2		
Voн		$V_{CC} = 4.5 V$,	I _{OH} = ~3 mA	2.4	3.2		2.4	3.2] _v
VOH		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2						1 °
		$V_{CC} = 4.5 V$,	I _{OH} = -15 mA				2			1
		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.05		V
		$(I_{OL} = 48 \text{ mA for } -$	- 1 version)				0.35		0.5	
I _I	Control inputs	$V_{CC} = 5.5 \text{ V},$	V ₁ = 7 V			0.1			0.1	mA
'}	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	1 '''A
l	Control inputs	Vcc = 5.5 V,	V ₂ = 2.7.V			20			20	μА
ΉΗ	A or B ports§	νCC = 5.5 ν,	V) = 2.7 V			20			20	μΑ
1	Control inputs	V _{CC} = 5.5 V,	V: - 0.4.V			-0.2			-0.2	m ^
11L	A or B ports§	vCC = 5.5 v,	V = 0.4 V		-0.2		-0.2		-0.2	mA
10¶		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		- 112	mA
			Outputs high		47	76		47	76	
lcc		$V_{CC} = 5.5 V$	Outputs low		55	88		55	. 88	mΑ
			Outputs disabled		55	88		55	88	1

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



 $^{^{\}ddagger}All$ typical values are at VCC =5 V, T_A $=25\,^{\circ}C$ SFor I/O ports, the parameters I $_{IH}$ and I $_{IL}$ include the off-state output current.

SN54ALS646, SN74ALS646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

'ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 5 R1 = 5 R2 = 5 T _A = 2	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25 °C 'ALS646		l	4ALS646	UNIT		
f _{max}			5	0		35		40		MHz
t _{PLH}	CBA or CAB	A or B	2	0	25	10	35	10	30	ns
^t PHL	CDA OF CAB	AUIB	1	1	15	5	20	5	17	115
^t PLH	A or B	B or A	1	1	17	5	22	5	20	ns
^t PHL	A 01 B	BOLA	7.	5	10	3	15	3	12	115
^t PLH	SBA or SAB [†]	A or B	2	4	32	15	40	15	35	ns
t _{PHL}	(with A or B low)	A OF B	1	3	17	5	23	5	20] ''3
^t PLH	SBA or SAB [†]	A or B	1	7	22	8	30	8	25	ns
^t PHL	(with A or B high)		1	3	17	5	24	5	20	115
^t PZH	<u></u> G.	A or B	1	0	15	3	20	3	17	ns
tPZL	G.	A 01 B	1	0	15	5	22	5	20	115
^t PHZ	G	A or B		6	8	1	12	1	10	ns
^t PLZ	J	7010	1	0	13	2	20	2	16	''3
^t PZH	DIR	A or B	2	2	28	10	38	10	30	ns
^t PZL	Dill		14.	5	20	5	. 30	5	25	113
^t PHZ	DIR	A or B		6	8	1	12	1	10	ns
tPLZ	DIN	A or B	1	0	13	2	21	2	16	118

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS647, SN74ALS647 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	/
Input voltage	/
Operating free-air temperature range: SN54ALS647)
SN74ALS647 0 °C to 70 °C	2
Storage temperature range65°C to 150°C)

recommended operating conditions

		Si	V54ALS	647	SN	74ALS6	47	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
1	Low lovel output dispose			12			24	mA
lor	Low-level output current						48 [†]	IIIA
fclock	Clock frequency	0		25	0		30	MHz
t _W	Pulse duration, clocks high or low	20			16.5			ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
th	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

[†]The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.

DADA	METER	TEST CONDITIO	N/C	SN54ALS	647	SN	74ALS	647	LINUT
PARA	METER	TEST CONDITIONS		MIN TYP‡	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA		-1.2			- 1.2	٧
ГОН		$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V		0.1			0.1	mA
		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA	0.25	0.4				
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 24 \text{ mA}$				0.35	0.5	V
		$(I_{OL} = 48 \text{ mA for } - 1)$	48 mA for -1 versions)				0.35		
11	A or B ports	$V_{CC} = 5.5 V,$	$V_1 = 7 V$		0.1			0.1	mA
"	Control inputs	$V_{CC} = 5.5 V,$	V ₁ = 7 V		0.1			0.1	"""
lu.	A or ports§	V _{CC} = 5.5 V,	V _I = 2.7 V		20			20	μА
l IH	Control inputs	VCC = 5.5 V,	V - 2.7 V		20			20	μΑ
lu.	Control inputs	$V_{CC} = 5.5 V,$	V _I = 0.4 V		-0.2			-0.2	mA
IIL.	A or B ports§	VCC = 5.5 V,	V) = 0.4 V		-0.2			-0.2	111/2
loo		V _{CC} = 5.5 V	Outputs high	35	60		35	60	mA
lcc		vCC = 9.5 v	Outputs low	40	65		40	65	

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$

The 48-mA limit applies for the SN74ALS647-1 only.

For I/O ports, the parameters IIH and IIL include the off-state output current.

SN54ALS647, SN74ALS647 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

'ALS647 switching characteristics (see Note 1)

PARAMETER	PARAMETER FROM (INPUT)		C _L R _L T _A	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 680 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX SN54ALS647 SN74ALS647				UNIT	
			MIN	ALS64 TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}			1	40		25		30		MHz	
tPLH	CDA or CAD	A a. D		38	50	19	72	19	58		
tPHL	CBA or CAB	A or B		12	20	6	24	6	22	ns	
tPLH	A or B	B or A		35	39	17	70	17	54	ns	
tPHL	1 4016	BULA	B 01 A		10	13	4	19	4	16	115
tPLH	SBA or SAB [†]	A D		40	51	20	72	20	60		
tPHL	(with A or B low)	A or B		12	17	6	26	6	22	ns	
tPLH	SBA or SAB [†]			40	- 51	20 -	72	20	60		
tPHL	(with A or B high)	A or B		12	17	6	26	6	22	ns	
tPLH	G	A or B		20	27	10	37	10	31	ns	
tPHL		AUID		10	15	2	20	2	17	1115	
tPLH	DIR	A or B		20	25	9	34	9	29	ns	
tPHL		7 37 5		13	17	2	22	2	19	1115	

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS648, SN74ALS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage: Control inputs
I/O ports
Operating free-air temperature range: SN54ALS648 55°C to 125°C
SN74ALS648
Storage temperature range65°C to 150°C

recommended operating conditions

		SN	54ALS	648	SN	174ALS	648	UNIT
	·	MIN	NOM	MAX	MIN	NOM	MAX	וואטן
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
loн	High-level output current			- 12			- 15	mA
loi	Low-level output current			12			24	mA
lOL	Low-level output current						48 [†]	I IIIA
fclock	Clock frequency	0		35	0		40	MHz
t _W	Pulse duration, clocks high or low	14.5			12.5			ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	15			10			ns
t _h	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger} \text{The extended conditon applies if V}_{CC}$ is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS648-1 only.

	2404445750	TEAT COMPLET	2010	SN	54ALS	648	SN	74ALS	648	
'	PARAMETER	TEST CONDIT	IONS	MIN	TYP‡	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V, I _{OH} = -0.4 mA	V _{CC} - 2			Vcc-	2		
Voн		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -3 mA	2.4	3.2		2.4	3.2		l _v
VOH		$V_{CC} = 4.5 V,$	I _{OH} = -12 mA	2						ľ
		$V_{CC} = 4.5 V,$	I _{OH} = -15 mA				2			
		$V_{CC} = 4.5 V,$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 V,$	IOL = 24 mA ·					0.05	0.5	V
		(I _{OL} = 48 mA for -1	version)					.0.35	0.5	
1.	Control inputs	$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1			0.1	mA
l _l	A or B ports	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 V$			0.1			0.1	1117
lu.	Control inputs	V _{CC} = 5.5 V,	V: - 2.7.V			20			20	μА
ΉΗ	A or B ports§	vCC = 5.5 v,	V = 2.7 V			20			20	μΑ
Lu	Control inputs	V _{CC} = 5.5 V,	V 0 4 V			-0.2			-0.2	mA
ll L	A or B ports§	vCC = 5.5 v,	V = 0.4 V			-0.2			-0.2	IIIA
lof		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
			Outputs high		47	76		47	76	
Icc		$V_{CC} = 5.5 V$	Outputs low		57	88		57	88	mA
			Outputs disabled		57	88		57	88	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5·V, T_A = 25 °C

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN54ALS648, SN74ALS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

'ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	= 50 = 500 = 500 = 25 ALS64		C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to ALS648	MAX	/, 1ALS648 MAX	UNIT
f _{max}			IVIIIV	50	WIAA	35	IVIAA	40	WAA	MHz
tPLH			<u> </u>	21	29	8	39	8	33	
tPHL	CBA or CAB	A or B		13	18	5	23	5	20	ns
tPLH		5 4		10	15	3	20	3	17	
tPHL	A or B	B or A		6	8	2	12	2	10	ns
t _{PLH}	SBA or SAB [†]	A or B		24	32	5	44	5	39	
^t PHL	(with A or B low)	Aorb		15	21	4	26	4	22	ns
t _{PLH}	SBA or SAB [†]	A B		16	22	6	30	6	25	
tPHL	(with A or B high)	A or B		14	19	6	25	6	21	ns
^t PZH	G	A or B		12	18	4	25	4	22	ns
tPZL	ď	A 01 B		12	18	4	25	4	22	113
^t PHZ	G	A or B		5	8	1	12	1	10	ns
t _{PLZ}	G	7, 0, 5		7	12	2	21	2	15	110
^t PZH	DIR	A or B		. 14	22	4	35	4	27	ns
^t PZL	2.11	,, 51 5		10	17	3	25	3	19	
^t PHZ	DIR	A or B		7	12	1	17	1	14	ns
tPLZ				7	13	2	22	2	15	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS649, SN74ALS649 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V	′
Input voltage	7 V	1
Operating free-air temperature range:	SN54ALS649 55°C to 125°C	;
	SN74ALS649	;
Storage temperature range	-65°C to 150°C	

recommended operating conditions

		SN	54ALS	649	SN	4ALS6	49	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
1	Low-level output current			12			24	mA
lOL	Low-level output current						48 [†]	IIIA
fclock	Clock frequency	0		25	0		30	MHz
t _W	Pulse duration, clocks high or low	20			16.5			ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	15			10	***************************************		ns
th	Hold time, A after CAB↑ or B after CBA↑	0			0			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}\text{The extended condition applies if V}_{CC}$ is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS649-1 only.

		TEAT COMPLETE	0.10	SN54ALS	649	SN74			
PAH	RAMETER	TEST CONDITI	TEST CONDITIONS		MAX	MIN T	YP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$		-1.2			-1.2	V
Тон		$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V		0.1			0.1	mA
		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA	0.25	0.4				
V _{OL}		$V_{CC} = 4.5 \text{ V},$ (I _{OL} = 48 mA for -	I _{OL} = 24 mA 1 versions)			С	.35	0.5	V
	A or B ports	$V_{CC} = 5.5 V$,	V _I = 7 V		0.1			0.1	mA
1	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V		0.1			0.1	ma
1	A or ports§	V _{CC} = 5.5 V,	V _I = 2.7 V		20			20	^
ΊΗ	Control inputs	vCC = 5.5 v,	V = 2.7 V		20			20	μΑ
1	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.2			-0.2	mA
l IIL	A or B ports§	VCC = 5.5 V,	V = 0.4 V		-0.2			-0.2	IIIA
laa		V _{CC} = 5.5 V	Outputs high	40	60		40	60	mA
lcc		VCC = 8.5 V	Outputs low	45	70		45	70	



 $^{^{\}ddagger}AII$ typical values are at V_{CC} = 5 V, T_A = 25 °C $^{\$}For$ I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN54ALS649, SN74ALS649 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

'ALS649 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L T _A	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 680 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$ 'ALS649		C R _I T,	CC = 4.5 V L = 50 pF, $L = 680 \Omega$, A = MIN to ALS649	٠.	UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax				40		25		30		MHz
^t PLH	CBA or CAB	A or B		40	52	19	77	19	62	ns
t _{PHL}	CBA OF CAB	X 01 B		12	18	6	22	6	20	113
^t PLH	A or B	B or A		30	41	13	65	13	50	ns
tPHL	, or p	BOIA		6	9	2	11	2	10	115
^t PLH	SBA or SAB [†]	A or B		35	46	20	72	20	55	ns
^t PHL	(with A or B low)	AOIB		15	21	6	26	6	22	IIIS
^t PLH	SBA or SAB [†]	A or B		35	46	20	72	20	55	
^t PHL	(with A or B high)	AOID		15	21	6	26	6	22	ns
^t PLH	G	A or B		16	22	8	28	8	25	ne
^t PHL] ,	7 01 0		13	18	2	23	2	20	ns
^t PLH	DIR	A or B		16	22	8	. 28	8	25	ns
^t PHL	Diii\	AVIB		13	17	2	23	2	20	1115

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS646, SN54AS648, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless of	otherwise noted)
Supply voltage, VCC	7 V
Input voltage: Control inputs	7 ∀
I/O ports	5.5 V
Operating free-air temperature range: SN54AS646, SN54AS648	55°C to 125°C
SN74AS646, SN74AS648	0°C to 70°C
Storage temperature range	65°C to 150°C

recommended operating conditions

			S	N54AS	646	s	N74AS	646	
1			S	N54AS	648	S	N74AS	648	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	ONT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
loн	High-level output current				-12			- 15	mA
IOL	Low-level output current				32			48	mA
fclock	Clock frequency		0		75	0		90	MHz
	Pulse duration	Clock high	6			5			
t _w	ruise duration	Clock high	7			6			ns
t _{su}	Setup time, A before CA	Bt or B before CBAt	7			6			ns
th	Hold time, A after CAB↑	or B after CBA↑	0			0			ns
TA	Operating free-air tempera	ature	- 55		125	0		70	°C

Р	ARAMETER	TEST CONDITION	DNS	SN	54AS6 54AS6	48	SN	46 48	UNIT	
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$l_{OH} = -2 \text{ mA}$	V _{CC} -2	2		v _{cc} -	2		
Vон		$V_{CC} = 4.5 V$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		_v
VOH		$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2						
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$				2]
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 32 \text{ mA}$		0.25	0.50				V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 48 mA					0.35	0.50]
Ч	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
''	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	I IIIA
l	Control inputs	$V_{CC} = 5.5 V_{r}$	V _I = 2.7 V			20			20	
ΉΗ	A or B ports [‡]	VCC = 5.5 V,	V - 2.7 V			70			70	μΑ
1	Control inputs	V _{CC} = 5.5 V,	V: - 0.4.V			-0.5			-0.5	
IIL.	A or B ports§	VCC = 5.5 V,	V = 0.4 V			-0.75			-0.75	mA
lo§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Outputs high		120	195		120	195	
	'AS646		Outputs low		130	211		130	211]
loo		$V_{CC} = 5.5 V$	Outputs disabled		130	211		130	211	
ICC		VCC - 5.5 V	Outputs high		110	185		110	185	mA
	'AS648		Outputs low		120	195		120	195	1
			Outputs disabled		120	195		120	195	1

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



 $^{^{\}dagger}All$ typical values are at VCC =5 V, TA $=25\,^{\circ}C$ $^{\ddagger}For$ I/O ports, the parameters I $_{IH}$ and I $_{IL}$ include the off-state output current.

SN54AS646, SN54AS648, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	($V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500 \text{ s}$ $R2 = 500 \text{ s}$ $V_{CC} = 4.5$	e, n, n, to MAX		UNIT
			MIN	AS646 MAX	SN74 MIN	AS646 MAX	
f _{max}			75	WAX	90	WAA	MHz
tPLH			2	9.5	2	8.5	
tPHL	CBA or CAB	A or B	2	10	2	9	ns
tPLH	A or B	A or B B or A		11	2	9	ns
tPHL	AOIB	BOFA	1	8	1	7	115
tPLH:	SBA or SAB†	A or B	2	12	2	11	ns
^t PHL	SBA OF SAB	5 5	2	10	2	9	113
tPZH		A or B	2	10	2	9	ns
tPZL		X 5/ B	3	15	3	14	
^t PHZ	<u> </u>	A or B	2	11	2	9	ns
tPLZ	G G	35	2	11	2	9	113
tPZH	DIR	A or B	. 3	19	3	16.	ns
tPZL	5		3	21	3	· 18	
[†] PHZ	DIR	A or B	2	12	2	10	ns
tPLZ	5.11	,, 3, 5	2	12	2	10	

'AS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	. F	$\begin{array}{cccccccccccccccccccccccccccccccccccc$					
f _{max}			75		90		MHz		
tPLH	CDA - CAD	A D	2	9.5	2	8.5			
t _{PHL}	CBA or CAB	A or B	2	10	2	9	ns		
^t PLH	A or B	r B B or A		9	2	8	ns		
^t PHL	AUIB	BOLA	1	8	1	7	l lis		
^t PLH	SBA or SAB†	A or B	2	.12	2	11	ns		
tPHL .	JBA OI JAB	A UI B	2	10	2	9	1115		
tPZH	- G	A or B	2	10	2	9	ns		
tPZL .		AUID	3	18	3	15	115		
^t PHZ	G	A or B	2	11	2	9			
tPLZ		A UI B	2	11	2	9	ns		
[†] PZH	DIR	A or B	3	19	3	16	ns		
^t PZL	DIK	A UI D	3	21	3	18] '''s		
[†] PHZ	DIR	A or B	2	12	2	10	ns		
^t PLZ	— DIN	A UI D	2	12	2	10	1115		

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

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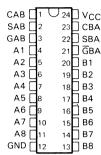
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

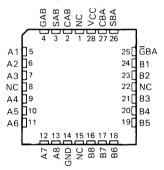
description

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether realtime or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and realtime data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

SN54ALS', SN54AS'... JT PACKAGE SN74ALS', SN74AS'... DW OR NT PACKAGE (TOP VIEW)



SN54ALS', SN54AS'...FK PACKAGE SN74ALS', SN74AS'...FN PACKAGE (TOP VIEW)



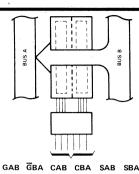
NC No internal connection

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{G}}\text{BA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

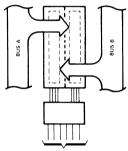
The -1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

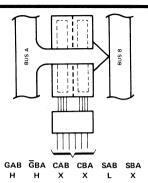




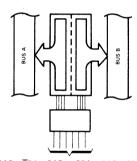
REAL-TIME TRANSFER **BUS B TO BUS A**



GAB GBA CAB CBA SBA х н х х х х х х х н х х STORAGE FROM A AND/OR B



REAL-TIME TRANSFER BUS A TO BUS B



GAB GBA CAB. CBA L Horl Horl

TRANSFER STORED DATA TO A AND/OR B

SN54ALS651 THRU SN54ALS654, SN54AS651, SN54AS652 SN74ALS651 THRU SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

FUNCTION TABLE

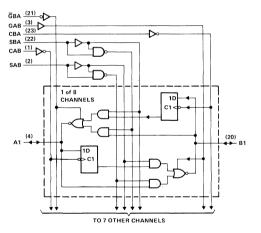
		INP	UTS			DAT	A I/O	OPERATION (OR FUNCTION
								'ALS651, 'ALS653	'ALS652, 'ALS654
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS651	'AS652
L	Н	HorL	H or L	X	X	la musa	lamin	Isolation	Isolation
L	Н	•	†	X	×	Input	Input	Store A and B Data	Store A and B Data
X	н		H or L	X	×	Input	Unspecified [†]	Store A, Hold B	Store A, Hold B
Н	Н	*	1	X [‡]	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	1	×	X	Unspecified †	Input	Hold A, Store B	Hold A, Store B
L	L		· ↑	X	X [‡]	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Outmut	lamus	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	Н	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus
Н	. н	Х	X	L	X	la accept	0	Real-Time A Data to B Bus	Real-Time A Data to B Bus
Н	Н	H or L	X	н	×	Input	Output	Stored A Data to B Bus	Stored A Data to B Bus
н		H or L	Harl	Н	Н	Output	Output	Stored A Data to B Bus and	Stored A Data to B Bus and
	L	lu or r	HOLL	"	п	Output	Output	Stored B Data to A Bus	Stored B Data to A Bus

[†]The data output functions may be enabled or disabled by various signals at the GAB or $\overline{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Select control = H: clocks must be staggered in order to load both registers.

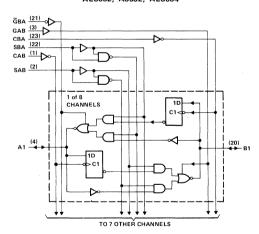
logic diagram (positive logic)

'ALS651, 'AS651, 'ALS653



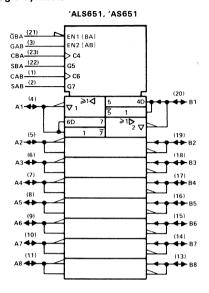
Pin numbers shown are for DW, JT, and NT packages.

'ALS652, 'AS652, 'ALS654

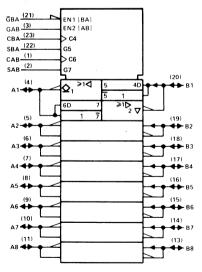


^{*}Select control = L: clocks can occur simultaneously.

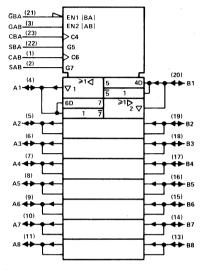
logic symbols†



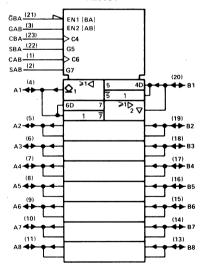
'ALS653



'ALS652, 'AS652



'ALS654



 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwi	ise noted)
Supply voltage, VCC	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652	55°C to 125°C
SN74ALS651, SN74ALS652	. 0°C to 70°C
Storage temperature range	35°C to 150°C

recommended operating conditions

			SN54ALS651 SN74ALS651 SN54ALS652 SN74ALS652				UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ГОН	High-level output current			- 12			- 15	mA	
lou	Low-level output current				12			24	mA
lOL	Low-level output current							48 [†]	1 '''
fclock	Clock frequency		0		35	0		40	MHz
	Pulse duration	CBA or CAB high	14.5			12.5			
t _w	ruise duration	CBA or CAB low	14.5			12.5			ns
t _{su}	Setup time before CAB↑ or CBA↑	A or B	15			10			ns
th	Hold time after CAB† or CBA†	A or B	5			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

 $^{^\}dagger$ The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 and if V_{CC} is maintained between 4.75 V and 5.25 V.

SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

	PARAMETER	TEST COND	TIONS		I54ALS			174ALS6 174ALS6		UNIT
		•		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$		V _{CC} -:	2		V _{CC} -:	2		
Voн		$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2] _v
VOH		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2]
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$				2			
		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 V$	$I_{OL} = 24 \text{ mA}$					0.35	0.5	v
		$V_{CC} = 4.75 \text{ V, } I_{OL} = 4$								
կ	Control inputs	$V_{CC} = 5.5 V$,				0.1			0.1	m _A
''	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	11171
ηн	Control inputs	$V_{CC} = 5.5 V_{c}$	$V_{I} = 2.7 \text{ V}$			20			20	μΑ
"""	A or B ports‡		.,			20			20	
IIL	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
'IL	A or B ports [‡]	VCC = 0.5 V,	V - 0.4 V			-0.2			-0.2] ""A
IO§	B ports	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Outputs high		42	68		42	68	
	'ALS651		Outputs low		52	82		52	82]
lcc		V _{CC} = 5.5 V	Outputs disabled		52	82		52	82	mA I
'''		₹CC - 3.3 ₹	Outputs high		47	76		47	76] '''^
	'ALS652		Outputs low		55	88		55	88] [
			Outputs disabled		55	88		55	88	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, T_A = 25 °C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS651, SN54ALS652, SN74ALS651, SN74ALS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

'ALS651 switching characteristics (see Note 1)

			1 -	-	٧,	1	CC = 4.5 V	to 5.5 V	',	
			$C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$							
	FROM	то					$1 = 500 \Omega$,			
PARAMETER	(INPUT)	(OUTPUT)	R2	= 50	Ο,	R	$2 = 500 \Omega$,			UNIT
	(1141 01)		T _A = 25°C			Т,	A = MIN to	MAX		
			',	ALS65	1	SN54	ALS651	SN74	ALS651	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	<u> </u>
fmax				50		35		40		MHz
^t PLH	CBA or CAB	A or B		20	27	10	38	10	32	
^t PHL	CBA OF CAB	AOIB		11	15	5	21	5	17	ns
^t PLH	A or D	B or A	1	9	13	4	20	4	18	
^t PHL	A or B	BOFA		5	8	2	12	2	10	ns
^t PLH	SBA or SAB [†]	A or B		24	31	13	45	13	38	
^t PHL	(with A or B low)	AOFB		13	18	7	25	7	21	ns
t _{PLH}	SBA or SAB†			15	20	8	30	8	25	
[†] PHL	(with A or B high)	A or B		13	18	7	25	7	21	ns
^t PZH	Gва	А		12	16	5	22	5	20	
tPZL	GBA	A		11	15	5	21	5	18	ns
^t PHZ	Gва			4	7	2	10	2	9	
tPLZ	GBA	Α		7	10	3	16	3	12	ns
^t PZH	GAB	В		14	19	7	25	7	22	
^t PZL] GAB	B		13	18	7	25	7	21	ns
tPHZ	GAB	В		5	10	2	14	2	12	T.,
tpi Z	1 GAB	В В		7	10	2	20	2	14	ns

'ALS652 switching characteristics (see Note 1)

				C = 5			c = ,4.5 V	to 5.5 V	•	
				$C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$		$C_L = 50 \text{ pF},$ R1 = 500 Ω ,				Ì
PARAMETER	FROM	TO (OUTPUT)	ľ	= 500		1	$= 500 \Omega,$			UNIT
	(INPUT)		T _A = 25°C			l	= MIN to	MAX		
				ALS65		SN54	ALS652	SN74ALS652		1
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax				50		35		40		MHz
^t PLH	CBA or CAB	A or B		20	25	10	35	10	30	ns
^t PHL	CBA OF CAB	A 01 B		11	15	5	20	5	17	1113
^t PLH	A or B	B or A		11	15	5	20	5	18	ns
^t PHL	AOIB	BOIA		8	10	3	15	3	12	115
tPLH	SBA or SAB†	A or B		24	32	15	40	15	35	
^t PHL	(with A or B low)	AOIB		13	17	6	23	6	20	ns
^t PLH	SBA or SAB [†]	A		17	22	8	30	8	25	
tpHL	(with A or B high)	A or B		13	17	5	24	5	20	ns
tPZH	GBA	А		10	15	3	20	3	17	ns
^t PZL	GBA			10	14	5	22	5	18	1115
^t PHZ	ĞВА	А		6	8	1	12	1	10	ns
^t PLZ	J GSA	^		10	13	2	20	2	16] "
^t PZH	GAB	В		15	20	8	25	8	22	ns
tPZL	J GAB	,		12	16	6	21	6	18] ''3
tPHZ	GAB	В		6	8	1	12	1	10	ns
tPLZ]			10	13	2	21	2	16	"

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS653, SN54ALS654, SN74ALS653, SN74ALS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

abso	olute maximum ratings over operating free-air temperature range (unless otherwise noted)
	Supply voltage, VCC
	Input voltage: All inputs and A I/O ports
	B I/O ports
	Operating free-air temperature range: SN54ALS653, SN54ALS654 55°C to 125°C
	SN74ALS653, SN74ALS6540°C to 70°C
	Storage temperature range65°C to 150°C

recommended operating conditions

			SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2		,	V
VIL	Low-level input voltage				0.7			0.8	V
Voн	High-level output voltage	A ports			5.5		,	5.5	V
ГОН	High-level output current	B ports			-12			- 15	mA
la.	Low-level output current				12			24	mA
lOL	Low-level output current							48 [†]] ""
fclock	Clock frequency		0		25	0		35	MHz
	Pulse duration	CBA or CAB high	20			14.5			
tw	Pulse duration	CBA or CAB low	20		****	14.5			ns
t _{su}	Setup time before CAB↑ or CBA↑ A or B		15		-	10			ns
th	Hold time after CAB↑ or CBA↑ A or B		5			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]The 48-mA limit applies only for the SN74ALS653-1 and SN74ALS654-1 and if V_{CC} is maintained between 4.75 V and 5.25 V.



SN54ALS653, SN54ALS654, SN74ALS653, SN74ALS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

Р	ARAMETER	TEST CON	DITIONS	1	154ALS		1	174ALS6 174ALS6		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	VCC-	2		VCC-	2		
Vон	B ports	$V_{CC} = 4.5 V,$	IOH = -3 mA	2.4	3.2		2.4	3.2		
VOH	b ports	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2						ľ
		$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2			
ЮН	A ports	$V_{CC} = 4.5 \text{ V},$	$V_{OH} = 5.5 V$			0.1			0.1	mA
		$V_{CC} = 4.5 V,$	$l_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	
v_{OL}		V _{CC} = 4.5 V,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	V
		$V_{CC} = 4.75 \text{ V, } I_{OL} =$		<u> </u>						
lş .	Control inputs	$V_{CC} = 5.5 V$,				0.1			0.1	mA
'4	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	111/5
чн	Control inputs	V _{CC} = 5.5 V,	$V_1 = 2.7 \text{ V}$			20			20	μА
1111	A or B ports [‡]	. *()(= 0.0 *,	V1 - 2.7 V			20			. 20	μ.
i	Control inputs	Vcc = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
IĮL	A or B ports [‡]	VCC = 5.5 V,	VI = 0.4 V			-0.2			-0.2	11112
lo§	B ports	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Outputs high		47	76		47	76	
	'ALS653		Outputs low		55	88		55	88	
loo		V _{CC} = 5.5 V	Outputs disabled		55	88		55	88	mA
ICC		VCC - 5.5 V	Outputs high		47	76		47	76	I IIIA
	'ALS654		Outputs low		55	88		55	88	
			Outputs disabled		55	88		55	88	

 $^{^{\}dagger}_{.}$ All typical values are at VCC = 5 V, TA = 25 °C.

For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that objects a proximates one half of the true short-circuit output current, IQS.

SN54ALS653, SN54ALS654, SN74ALS653, SN74ALS654 OCTAL BUS TRANSCEIVERS AND REGISTERS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R1 = R2 = 500 Ω (B outputs), T _A = 25 °C 'ALS653 'ALS654				$V_{CC} = 4.5 \text{ V} \text{ t}$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega \text{ (A}$ $R2 = R2 = 50$ $T_A = \text{MIN to N}$ $54\text{ALS}653$ $54\text{ALS}654$	outputs), O Ω (B out IAX SN74	puts), ALS653 ALS654 MAX	UNIT
fmax				40		25	****	35		MHz
tPLH tPHL	СВА	Α		30 11	50 15	- 16 - 6	71 24	16 6	64 22	ns
tPLH tPHL	САВ	В		20 11	25 15	10 5	35 20	10 5	30 17	ns
t _{PLH}	А	В		11 10	15 13	5 2	20 18	5 2	18 15	ns
t _{PLH}	В	Α		20 10	44 13	12	63 18	12 2	56 15	ns
t _{PLH}	SBA [†] (with B low)	Α		35 15	50 22	19 5	68 27	19 5	62 25	ns
^t PLH ^t PHL	SBA [†] (with B high)	Α		35 15	50 22	19 5	68 27	19 5	62 25	ns
t _{PLH}	SAB [†] (with A low)	В		24 13	32 18	12 6	40 25	15 6	35 22	ns
t _{PLH}	SAB [†] (with A high)	В		18 13	22 19	8 6	30 25	8	25 22	ns
tPLH tPHL	Ğва	. A		17 14	23 20	6 6	35 27	6	30 24	ns
^t PZH ^t PZL	GAB	В		15 13	20 17	8 6	25 25	8	22 22	ns
tPHZ tPLZ	GAB	В		8 10	12 13	2	16 21	1 2	14 16	ns

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS651, SN54AS652, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	
Supply voltage, VCC	
Input voltage: Control inputs	
I/O ports	
Operating free-air temperature range: SN54AS651, SN54AS652 55°C C to 125°C	
CN74ACGE1 CN74ACGE2 00C to 700C	

SN74AS651, SN74AS652 0°C to 70°C Storage temperature range

recommended operating conditions

			S	SN54AS651 SN54AS652			V74AS6	51	
	-		s				SN74AS652		
			MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
ViH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ГОН	High-level output current				-12			- 15	mA
loL	Low-level output current				32			48	mA
fclock	Clock frequency		0		75	0		90	MHz
	Pulse duration	CBA or CAB high	6			5			
tw	ruise duration	CBA or CAB low	7			6			ns
t _{su}	Setup time before CAB↑ or CBA↑ A or B		7			6			ns
th	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

P	ARAMETER	TEST COND	ITIONS	1	N54AS6		ĺ	174AS6 174AS6		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	1
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = −2 mA	V _{CC} -2	2		Vcc-2	2		
Voн		$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2] _/
VOH		$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2] `
		$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2]
V/a.		$V_{CC} = 4.5 V,$	$I_{OL} = 32 \text{ mA}$		0.25	0.50				V
VoL		$V_{CC} = 4.5 V$,	$I_{OL} = 48 \text{ mA}$					0.35	0.50	
Control inputs		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
"	A or B ports	$V_{CC} = 5.5 V$,	$V_1 = 5.5 V$			0.1			0.1	_ '''^_
ίн	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			-20			20	μА
Hוי	A or B ports [‡]	V(C = 0.5 V,	V - 2.7 V			70			70	μ
1 ₁ L	Control inputs	Vcc = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
'IL	A or B ports [‡]	VCC = 3.3 V,	V = 0.4 V			-0.75			-0.75	1
lo§		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
			Outputs high		110	185		110	185	
	'AS651		Outputs low		120	195		120	195]
Icc		V _{CC} = 5.5 V	Outputs disabled		130	195		130	195	mA
100		VCC = 0.3 V	Outputs high		120	195		120	195	'''^
	'AS652		Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



 $^{^{\}ddagger}$ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500 \text{ s}$ $R2 = 500 \text{ s}$ $T_A = MIN$ AS651	=, Ω, Ω, to MAX	V, AS651	UNIT	
			MIN	MAX	MIN	MAX		
f _{max}			75		90		MHz	
tPLH	CBA or CAB	A or B	2	9.5	2	8.5		
^t PHL	CBA OF CAB	, A or B	2	10	2	9	ns	
^t PLH	A or B	B or A	2	9	2	8	ns	
^t PHL	7 01 5	BUIA	1	8	1	7	115	
^t PLH	SBA or SAB†	A or B	2	12	2	11	ns	
t _{PHL}	SUA OF SAB	A 01 B	2	10	2	9	115	
^t PZH	 Gва	Α	. 2	11	2	10	ns	
^t PZL	GBA		3	18	3	16	113	
tPHZ ·	G ва	A	2	10	2	9	ns	
^t PLZ	GDA .		2	10	2	9	115	
^t PZH	GAB	В	3	12	٠3	11	ns	
t _{PZL}	J. J. J. J. J. J. J. J. J. J. J. J. J. J		3	20	3	16	113	
^t PHZ	GAB	В	2	11	2	10	ns	
t _{PLZ}] GAB		2	12	2	11	115	

'AS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$					
			MIN	AS652 MAX	SN74AS652			
f _{max}			75	IVIAA	90	MAX	MHz	
tPLH			2	9.5	2	8.5		
tPHL	CBA or CAB	A or B	2	10	2	9	ns	
^t PLH	1	D 4	2	11	2	9		
^t PHL	A or B	B or A	- 1	8	1	7	ns	
^t PLH	SBA or SAB [†]	A or B	2	12	2	11		
^t PHL	SBA UI SAB	AOIB	2	10	2	9	ns	
tPZH .	- GBA	Α	2	11	2	10	ns	
^t PZL		A .	3	18	3	16	115	
^t PHZ	ĞВА	Α	2	10	2	9	ns	
^t PLZ		Α ,	2	10	2	9	115	
^t PZH	GAB	В	3	12	3	11	ns	
tPZL ·		ь	3	20	3	16	115	
^t PHZ	GAB	В	2	11	2	10	ns	
^t PLZ		В	2	12	2	11] '''	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

D2855, JUNE 1984 -- REVISED MAY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic 'ALS666 . . . True Outputs 'ALS667 . . . Inverting Outputs
- Preset and Clear Inputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer type output and are easily utilized in bus-structured applications.

The eight latches of the 'ALS666 and 'ALS667 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS666 will follow the data (D) inputs. On the 'ALS667, the \overline{Q} outputs will provide the inverse of what is applied to its data (D) inputs. On both devices, the Q or \overline{Q} output will be in the high-impedance state if either output control, $\overline{OE}1$ or $\overline{OE}2$, is at a high logic level.

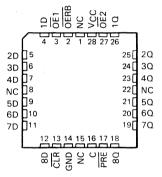
Read-back is provided thru the read-back control input (OERB). When OERB is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, caution should be exercised not to create a busconflict situation.

The SN54ALS666 and SN54ALS667 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS666 and SN75ALS667 are characterized for operation from 0°C to 70°C.

SN54ALS666 . . . JT PACKAGE SN74ALS666 . . . DW OR NT PACKAGE (TOP VIEW)



SN54ALS666 . . . FK PACKAGE SN74ALS666 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

SN54ALS667 . . . JT PACKAGE SN74ALS667 . . . DW OR NT PACKAGE (TOP VIEW)

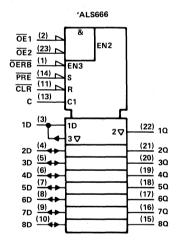
٠,	,										
OERB C	1 U	24	VCC OE2								
1D 🗀	3	22	1 <u>0</u>								
2D 🗀	4	210	20								
3D 🗀	5	20[]	3 <u>0</u>								
4D 🗀	6	19[_]	4₫								
5D 🗀	7	18	5 <u>0</u>								
6D [8	17[]	6 <u>0</u>								
7D [9	16	70								
_8D [10	15	<u>80</u>								
CLR [11	14	PRE								
GND [12	13 l l	С								

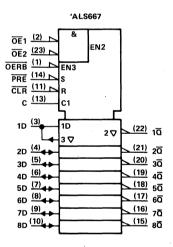
SN54ALS667 . . . FK PACKAGE SN74ALS667 . . . FN PACKAGE (TOP VIEW)

			•		-		•			
		5	0E1	OERB	Š	ر در	0E2	10		
1		4	3	7	7	28	27	26		
2D	5								25[2 <u>0</u>
]6								24[30
4D]7								23[40
NC]8								22[NC
5D]9								21[50
6D]10								20[6 <u>0</u>
7D	וים								19[70
		12	13	14	15	16	17	18		l

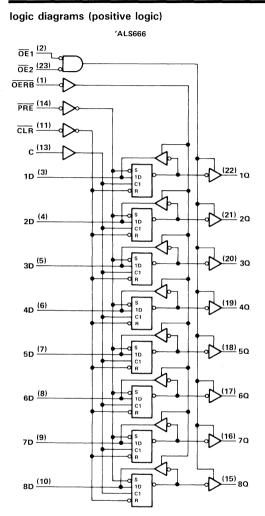
NC-No internal connection.

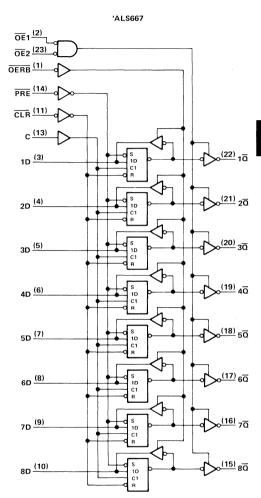
logic symbols†





 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 Pin numbers shown are for DW, JT, and NT packages.

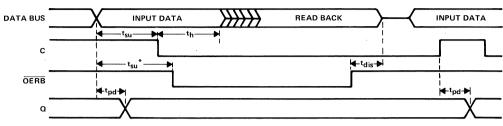




Pin numbers shown are for DW, JT, and NT packages.

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

timing diagram



 $\overline{CLR} = H$, $\overline{PRE} = H$, $\overline{OE1} = L$, $\overline{OE2} = L$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, vCC	
Input voltage (all inputs except D input	ut) 7 V
Voltage applied to D inputs and to dis	sabled 3-state outputs 5.5 V
Operating free-air temperature range:	SN54ALS666, SN54ALS667 – 55 °C to 125 °C
	SN74ALS666, SN74ALS667 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

				SN	154ALS	666	SI	N74ALS	366	
						67	SI	N74ALS	367	UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	,		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	***************************************		2			2			V
VIL	Low-level input voltage					0.7			0.8	V
lau	High-level output current		Q			- 1			- 2.6	^
Іон	riigii-level output current	D			- 0.4			-0.4	mA	
lai	Load-level output current		Q			12			24	mΑ
lOL	Load-level output current		D			4			8	IIIA
		En	able C high	15			10			
tw	Pulse duration	CL	R low	10			10			ns
		PR	Ē low	10			10			
	Setup time	Da	ta before C↓	15			10			
^t su	Setup time	Da	ta before OERB ↓	15			10			ns
th	Hold time	Da	ta after C1	10			5			ns
Тд	Operating free-air temperature		- 55		125	0		70	°C	



^{*}This setup time ensures the readback circuit will not create a conflict on the input data bus.

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 **8 BIT D-TYPE TRANSPARENT READ-BACK LATCHES** WITH 3-STATE OUTPUTS

PARAI	METER	TEST COND	DITIONS	i	I54ALS			N74ALS N74ALS		UNIT
				MIN	TYPt	MAX	MIN	TYPt	MAX	[
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			-1.2	V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} - 2			
V_{OH}	Q or Q	$V_{CC} = 4.5 V,$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					
	4 6/ 4	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	D	$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	IOL = 8 mA					0.35	0.5	l v
VOL	Q or Q	$V_{CC} = 4.5 V,$	$I_{OL} = 12 \text{ mA}$	1	0.25	0.4		0.25	0.4	ľ
	2012	$V_{CC} = 4.5 V,$	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
lozh	Q or \overline{Q}	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μА
lozL	7 4 61 4	$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μ
I.	D inputs	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 \text{ V}$			0.1			0.1	mA
lį .	All others	$V_{CC} = 5.5 V,$	V = 7 V			0.1			0.1	'''A
	D inputs‡	.,	V = 2.7 V			20			20	
ΊΗ	All others	$V_{CC} = 5.5 V,$	V = 2,7 V			20			20	μΑ
,	D inputs‡	V = 55 V	V 0.4.V	1		-0.1			-0.1	
IL	All others	$V_{CC} = 5.5 V,$	V ₁ = 0.4 V			-0.1			-0.1	mA .
10 §		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Q outputs high		25	50		25	50	
	'ALS666		Q outputs low		40	73		40	73	
		$V_{CC} = 5.5 V,$	Q outputs disabled		30	55		30	55	
ICC		OERB high	◯ outputs high		25	50 .		25	50	mA
	'ALS667		Q outputs low		45	79′		45	79	
	ALS007		Q outputs disabled	1	30	60		30	60	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output currents, IOS.

SN54ALS666, SN54ALS667, SN74ALS666, SN74ALS667 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

'ALS666 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	C = 5 = 50 p = 25°	oF, C	CNIE	$V_{CC} = 4.5$ $C_L = 50 \text{ pF},$ $T_A = \text{MIN to}$ $4\text{ALS}666$	MAX	, ALS666	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tplH	D	-		7	10	3	18	3	14	
tpHL	U	Q		11 -	15	4	22	4	18	ns
^t PLH	С			12	16	6	25	6	21	
[†] PHL	C	Q		16	21	8	32	8	27	ns
^t PHL	ČLR	Q		17	22	9	32	9	29	
^t PHL	CLN	D		17	24	11	36	11	32	ns
tPLH	PRE	Q		13	18	7	28	7	22	
^t PHL	FRE .	D		17	22	9	35	9	28	ns
t _{en}	ŌĒRB	D		11	17	4	25	4	21	
t _{dis}	OEND	U		6	11	1	18	1	14	ns
t _{en}	OE1, OE2	Q		11	17	4	25	4	21	
t _{dis}	OL1, UEZ	<u> </u>		6	11	1	18	1	14	ns

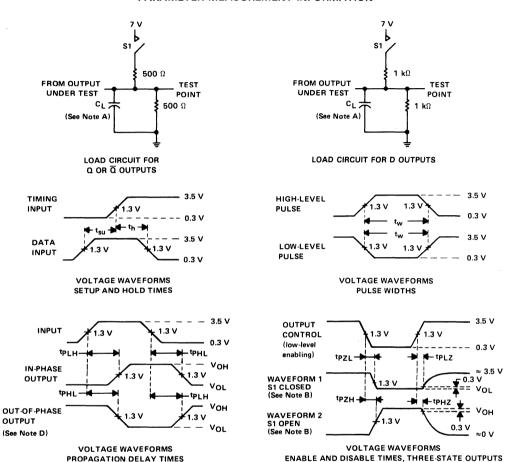
'ALS667 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	(INPUT) (OUTPUT)			$\begin{array}{c c} \text{IPUT} & \text{T}_{A} = 25^{\circ}\text{C} \\ \hline & \text{'ALS667} \end{array}$			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $T_A = \text{MIN to MAX}$ $SN54ALS667$ $SN74ALS667$					
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	1			
^t PLH	D	ā		13	17	6	24	6	20	ns			
t _{PHL}		<u>u</u> .		9	13	4	18	4	15	115			
tPLH	С	ā		18	23	9	35	9	28	no			
^t PHL	C			14	19	7	27	7	22	ns			
t _{PLH}	CLR	ā		14	19	7	28	, 7	24				
^t PHL	CLA	D		17	23	8	30	8	26	ns			
^t PHL	PRE	ā		17	23	8	30	8	25				
^t PL [:] H	FNE	D		18	25	9	35	9	28	ns			
t _{en}	ŌĒRB	D		11	17	4	25	4	21				
^t dis	OLNB			6	11	1	20	1	14	ns			
t _{en}	OE1, OE2	ā		11	17	4	25	4	21	ns			
t _{dis}	OL1, OL2	Q.		6	11	1	. 20	.1	14] "			

 $t_{en} = t_{PZH} \text{ or } t_{PZL}$ $t_{dis} = t_{PHZ} \text{ or } t_{PLZ}$



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1



SN54ALS677A, SN54ALS678, SN74ALS677A, SN74ALS678 16-BIT ADDRESS COMPARATORS

D2661, JUNE 1982-REVISED MAY 1986

- 'ALS677A is a 16-bit Address Comparator with Enable
- 'ALS678 is a 16-bit Address Comparator with Latch
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

The 'ALS677A and 'ALS678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'ALS677A features an enable input (\overline{G}) . When \overline{G} is low, the device is enabled. When \overline{G} is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS677A and SN54ALS678 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN54ALS677A and SN74ALS678 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS677A . . . JT PACKAGE SN74ALS677A . . . DW OR NT PACKAGE

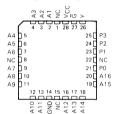
(TOP VIEW) A2 [23 G 22 Y A3 []3 A4 4 A5 5 A6 6 A7 7 31F P3 20 P2 19 Īρο 18 17 A 16 A8 08 16 A 15 15 A 14 A10 A ₹ A 1 3

SN54ALS677A . . . FK PACKAGE SN74ALS677A . . . FN PACKAGE

13 A 12

GND 12

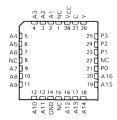
(TOP VIEW)



SN54ALS678 . . . JT PACKAGE SN74ALS678 . . . DW OR NT PACKAGE



SN54ALS678 . . . FK PACKAGE SN74ALS678 . . . FN PACKAGE (TOP VIEW)



NC No internal connection

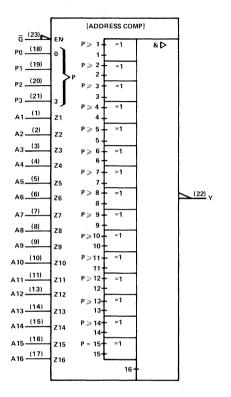
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

INPUTS COMMON TO 'ALS677A AND 'ALS678

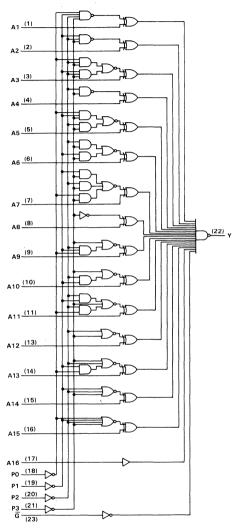
'ALS677A	'ALS678						NPU	TS C	OMI	ION	TO '	ALS6	77A	ANG	'AL	S678	3					ООТРОТ
Ğ	С	Р3	P2	P1	PO	Α1	A2	А3	Α4	Α5	Α6	Α7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
] L]	н	L	L	L	н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	. Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	н	Н	Н	Н	Н	Н	L
L	Н	L	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	Н	L	н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	Н	Н	L	L	L	L	L	L	L	Н	Н	Н	н	Н	Н	Н	Н	Н	H	L
L	н	L	Н	Н	н	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	Н	L	L	Н	L	L	L	L	L	Ĺ	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
L	Н	н	L	Н	L	L	L	L	, L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	L
L	Н	н	L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	L
L	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	L
L	н	н	Н	L	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	L
L	Н	н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Н	н	L
L	Н	н	Н	Н	н	L	L	L	L	L	L	L	Ł	L	L	L	L	L	L	L	Н	L
L	Н		All other combinations									Н										
Н			'ALS677A: Any combination								Н											
	L		'ALS678: Any combination								Latched											

FUNCTION TABLE

'ALS677A logic symbol[†]

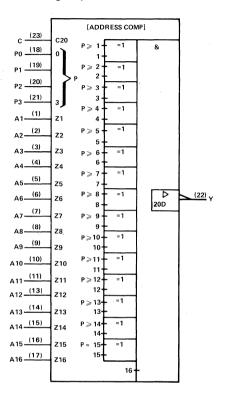


'ALS677A logic diagram (positive logic)

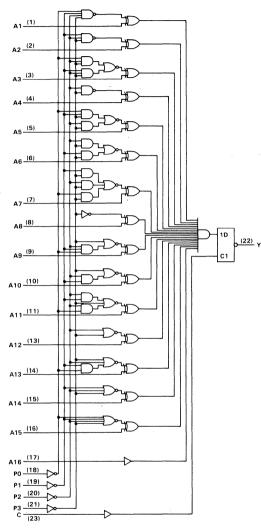


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

'ALS678 logic symbol[†]



'ALS678 logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



SN54ALS677A, SN54ALS678, SN74ALS677A, SN74ALS678 16-BIT ADDRESS COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise	se noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS677A, SN54ALS678	5°C to 125°C
SN74ALS677A, SN74ALS678	0°C to 70°C
Storage temperature range	5°C to 150°C

recommended operating conditions

					54ALS6 I54ALS		1	74ALS6		UNIT
			,	MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	*		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
ЮН	High-level output current					- 1			-2.6	mA
lOL	Low-level output current					12			24	mΑ
t _W	Pulse duration, enable C high	'ALS678		45			40			ns
t _{su}	Setup time, data before Cl	'ALS678		50			45			ns
th	Hold time, data after C↓	'ALS678		10			5			ns
TA	Operating free-air temperature			- 55		125	0		70	°C

PARAMETER	TEST COND	ITIONS		54ALS6 N54ALS			SN74ALS677A SN74ALS678			
			MIN	TYP	MAX	MIN	TYP [†]	MAX		
ViK	$V_{CC} = 4.5 V,$	I _j = -18 mA			-1.2			-1.2	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		v _{cc} -	2			
Voн	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V	
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2			
VoL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V	
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5	ľ	
11	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA	
IH	V _{CC} = 5.5 V,	$V_1 = 2.7 \text{ V}$			20			20	μΑ	
IIL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.1			-0.1	mA	
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA	
ICC ALS677A	V _{CC} = 5.5 V			21	33		21	33	mΑ	
ALS678	7 VCC = 5.5 V			21	35		21	35	IIIA	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS677A, SN54ALS678, SN74ALS677A, SN74ALS678 16-BIT ADDRESS COMPARATORS

'ALS677A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R _L T _A	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ ALS677A MIN TYP MAX		SN54A	V _{CC} = 4.5 C _L = 50 pl R _L = 500 S T _A = MIN LS677A MAX	=, ⊋, to MAX	V, ALS677A MAX	UNIT	
			IVIIIV	111							
tPLH	Any P	Y		11	18	4	28	4	25	ns	
tPHL	, .				22	32	8	43	8	38	.,.
^t PLH	Any A	Y		10	17	5	26	5	22	ns	
tPHL	Ally A	<u>'</u>		16	25	5	35	5	30	115	
^t PLH	G	Υ		6	10	3	15	3	13	ns	
^t PHL	9	Y	· · · · ·		16	30	5	40	5	35	115

'ALS678 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX		UNIT	
			SN54	ALS678	SN74	ALS678	
			MIN	MAX	MIN	MAX	
^t PLH	Any P	Υ	6	27	6,	22	
^t PHL	Anyr	T	10	52	10	43	ns
^t PLH	Any A	Υ	5	25	5	21	
t _{PHL}	any A	'	5	40	5	35	ns
^t PLH	С	Y	3	25	3	20	
^t PHL	1	ĭ	15	54	15	48	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'ALS677A and 'ALS678 can be wired to recognize any one of 2¹⁶ addresses. The number of ''lows'' in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15 A14 A13 A12 A11 A10 Δ9 Α8 Α7 Α6 Α5 Α4 Α3 Α2 Α1 AΩ Н Н L Н Н

Since the address contains 6 lows and 10 highs, the following connections are made:

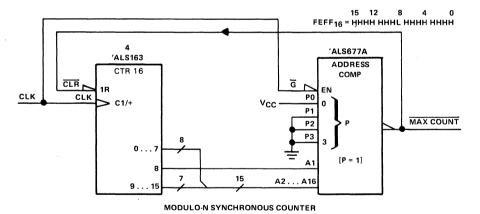
P3 to 0 V, P2 to VCC, P1 to VCC, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when $N = FEFF_{16}$.



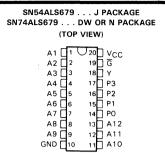
- 'ALS679 is a 12-Bit Address Comparator with Enable
- 'ALS680 is a 12-Bit Address Comparator with Latch
- Package Options Include "Small Outline"
 Packages, Ceramic Chip Carriers, and
 Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

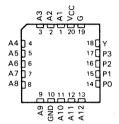
The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high-to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'ALS679 features an enable input (\overline{G}) . When \overline{G} is low, the device is enabled. When \overline{G} is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

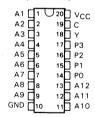
The SN54ALS679 and SN54ALS680 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS679 and SN74ALS680 are characterized for operation from 0°C to 70°C.



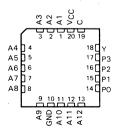
SN54ALS679 . . . FK PACKAGE



SN54ALS680 . . . J PACKAGE SN74ALS680 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS680 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

'ALS679	'ALS680				INPL	JTS (СОМ	MON	то	ALS	679	AND	'ALS	680)			ОПТРИТ
Ğ	С	Р3	P2	P1	P0	A1	A2	А3	Α4	Α5	Α6	Α7	A8	Α9	A10	A11	A12	Y
L	H	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	L	Н	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	Н	L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
L	н	L	Н	Н	L	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	L
L	Н	L	Н	Н	Н	L	L	L	L	L	L	L	Н	н	Н	Н	Н	L
L	Н	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	L
L	Н	Н	L	L	Н	L	L	L	L	L	L	L	L	L	Н	н	н	L
L	Н	н	L.	Н	L	L	L	L	L	L	L	L	L	L	L	Н	Н	L
L	H.	н	L	H	Н	L	L	L	L	L	L	L	L	L	L	L	Н	L
L	H	Н	н	L	L	L	L	L	L	ι	L	L	L	Н	н	Н	L	LŤ
L	н	н	н	L	н	L	L	ι	L	L	L	ι	L	L	н	н	L	Lt
L	н	н	н	Н	L	ι	L	L	L	ι	L	L	Ļ	Ł	L	Н	Ļ	L.t
L	Н	Н	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	L	L	L
L	Н						Α	ll oth	er co	mbir	nation	าร						н
Н							'ALS	5679	: An	y cor	nbina	tion						Н
	L						'ALS	3680	: An	y cor	nbina	ition						Latched

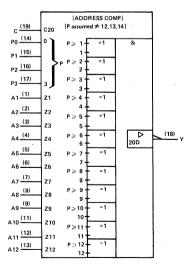
[†]The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P=12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change $P \ge 9$ to $P=9 \dots 11/13 \dots 15$, $P \ge 10$ to P=10/11/14/15, and $P \ge 11$ to P=11/15.

logic symbols[‡]

'ALS679

[ADDRESS COMP] G (19) [P assumed # 12,13,14] PO (14) 8.5 P1 (15) P2 (16) P3 (17) **Z**1 A2 (2) Z2 A3 (3) Z3 A4_(4) (18) 74 A5_(5) **Z**5 A6-(6) **Z**6 P > 8 **Z**7 A8 (8) P ≥ 9 Z8 A9 (9) **Z**9 P ≥ 10 A10 (11) 10 Z10 P≥ 11 A11 (12) Z11 11 P > 12 Z12 12

'ALS680

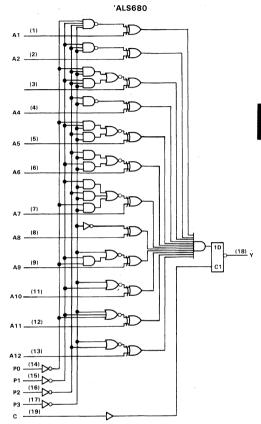


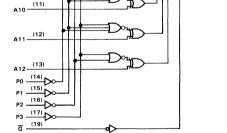
[‡]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



A1 (1) A2 (2) A3 (3) A4 (4) A5 (5) A6 (6) A7 (7) A8 (8)

(9)





SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680 12-BIT ADDRESS COMPARATORS

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54ALS679, SN54ALS680 55 °C to 125 °C
	SN74ALS679, SN74ALS680 0 °C to 70 °C
Storage temperature range	65°C to 150°C

recommended operating conditions

				154ALS 154ALS		SN74ALS679 SN74ALS680			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2		-	V
VIL	Low-level input voltage	· · · · · · · · · · · · · · · · · · ·			0.7			0.8	V
^Т ОН	High-level output current				- 1			- 2.6	mA
IOL	Low-level output current				12			24	mA
t _W	Pulse duration, Enable C high	'ALS680	45			40			ns
t _{su}	Setup time, Data before C↓	'ALS680	50			45			ns
th	Hold time, Data after C↓	'ALS680	10			5			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS679 SN54ALS680	SN74ALS679 SN74ALS680	UNIT
		MIN TYP [†] MAX	MIN TYP† MAX	1
VIK	$V_{CC} = 4.5 \text{ V}, \qquad I_{I} = -18 \text{ mA}$	-1.5	- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$	V _{CC} 2	V _{CC} - 2	
VoH	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -1 \text{ mA}$	2.4 3.3		\ \
	$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -2.6 \text{ mA}$		2.4 3.2	
Va. '	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 12 \text{ mA}$	0.25 0.4	0.25 0.4	
VOL ,	$V_{CC} = 4.5 \text{ V}, \qquad I_{OL} = 24 \text{ mA}$		0.35 0.5	1
4	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 7 \text{ V}$	0.1	0.1	mA
IIH	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$	20	20	μΑ
IIL	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 0.4 \text{ V}$	-0.1	-0.1	mA
10 [‡]	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.25 \text{ V}$	-30 -112	-30 -112	mA
'ALS679	V E E V	17 28	17 28	
CC ALS680	V _{CC} = 5.5 V	18 27	18 27	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS679, SN54ALS680, SN74ALS679, SN74ALS680 12-BIT ADDRESS COMPARATORS

'ALS679 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)		$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX					
			SN54	ALS679	SN74			
			MIN	MAX	MIN	MAX		
^t PLH	Any P	Any P Y	4	28	4	25	ns	
^t PHL	Ally		8	40	8	35		
t _{PLH}	Δ αν. Δ	, ,	5	26	5	22	nc	
^t PHL	Any A	Y	5	35	5	30	ns	
t _{PLH}	G		3	15	3	13	ns	
t _{PHL}		'	5	30	5	25	115	

'ALS680 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500 Ω T_A = MIN to MAX					
			SN54	ALS680	SN74ALS680]		
			MIN	MAX	MIN	MAX	1		
^t PLH	Any D	у Р	6	27	6	22	ns		
^t PHL	Any P		10	43	10	38	ns		
^t PLH	Any A	~	5	25	5	21	ns		
[†] PHL	Ally A	r	5	28	5	25	1 115		
^t PLH	C Y		3	25	3	20	ns		
^t PHL	1	Ţ	15	48	15	42	'''		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2¹² addresses. The number of ''lows'' in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

Since the address contains 4 lows and 8 highs, the following connections are made:

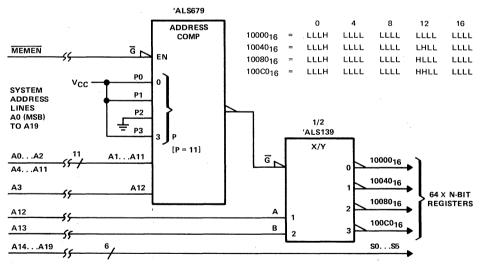
P3 to 0 V, P2 to VCC, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



REGISTER BANK DECODER

SN54ALS688, SN54ALS689, SN74ALS688, SN74ALS689 8-BIT IDENTITY COMPARATORS

D2661, JUNE 1982 - REVISED MAY 1986

- Compares Two Eight-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

TYPE	OUTPUT FUNCTION AND CONFIGURATION
'ALS688†	$\overline{P} = Q$ totem pole
'ALS689	P = Q open-collector

†'ALS688 is identical to 'ALS521

description

These identity comparators perform comparisons of two eight-bit binary or BCD words. The 'ALS688 and 'ALS689 provide $\overline{P}=\overline{Q}$ outputs. The 'ALS688 has totem-pole outputs, while 'ALS689 has open-collector outputs.

The SN54ALS688 and SN54ALS689 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS688 and SN74ALS689 are characterized for operation from 0 °C to 70 °C.

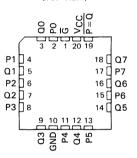
FUNCTION TABLE

INP	UTS	OUTPUT		
DATA P,Q	ENABLE G	$\overline{P} = \overline{\Omega}$		
P=Q	L	L		
P>Q	L	Н		
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н		
Х	Н	Н		

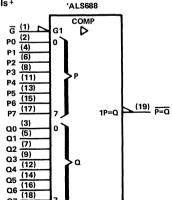
SN54ALS688, SN54ALS689 . . . J PACKAGE SN74ALS688, SN74ALS689 . . . DW OR N PACKAGE (TOP VIEW)

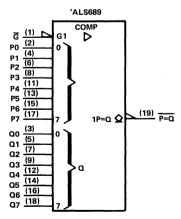
U20] VCC \overline{G} 19 P=Q P0 ∏ 2 18 D Q 7 വെ∏ദ 17 P7 P1 ∏4 Q1 | 5 16 \ Q6 15 P6 P2 ∏6 Q2 🗆 7 14 \ Q5 13 P5 P3 ∏8 озПэ 12 1 0.4 GND ☐10 11 P4

SN54ALS688, SN54ALS689 . . . FK PACKAGE (TOP VIEW)



logic symbols ‡



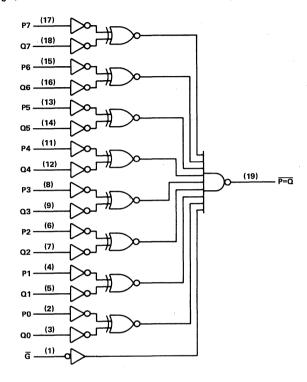


[‡]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Texas Instruments

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage:	7 V
Off-state output voltage: 'ALS689	7 V
Operating free-air temperature range: SN54ALS688, SN54AS689	125°C
SN74ALS688, SN74AS689 0 °C to	
Storage temperature range -65 °C to	150°C



SN54ALS688, SN74ALS688 8-BIT IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

		S	N54ALS	688	SN74ALS688			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
ViH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон	High-level output current			- 1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			154ALS	688	SN	UNIT		
PARAMETER	TEST CO	NUTTIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNI
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V, I _{OH} = -0.4 mA	Vcc-	2		V _{CC} -	2		
Voн	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					\ \
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		Ì
V/	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5	ľ
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V		-	0.1			0.1	mA
ΉΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
Iμ	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	-30		-112	mA
^I CC	V _{CC} = 5.5 V	See Note 1		12	19		12	19	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A_{c}} = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	RAMETER FROM (INPUT) (OU		F	$C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $R_A = MIN \text{ to}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{min to MAX}$					
			SN54A	LS688	SN74ALS688		_			
1			MIN	MAX	MIN	MAX	l			
^t PLH	Р	P=Q	3	16	3	12				
^t PHL	[r=u	5	25	5	20	ns			
^t PLH	Q	P=Q	3	16	3	12				
^t PHL] "	r=u	5	25	5	20	ns			
^t PLH	G	P=Q	3	15	3	12	ns			
^t PHL		r - u	5	25	5	22	1115			

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: ICC is measured with G grounded, P and Q at 4.5 V.

SN54ALS689, SN74ALS689 8-BIT IDENTITY COMPARATORS WITH OPEN COLLECTOR OUTPUTS

recommended operating conditions

		SI	SN54ALS689			SN74ALS689		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vсс	Supply voltage	4.5	5	5.5	4.5	. 5	5.5	V
v_{IH}	High-level input voltage	2			2			٧
V_{IL}	Low-level input voltage			0.7			0.8	٧
Iон	High-level output current			5.5			5.5	٧
^l OL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS689	SN74ALS689	UNIT
PARAMETER	TEST CONDITIONS	MIN TYP† MAX	MIN TYP [†] MAX	ONII
VIK	$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$	-1.5	-1.5	V
^І ОН	$V_{CC} = 5.5 \text{ V}, V_{OH} = 5.5 \text{ V}$	0.1	0.1	mA
V	$V_{CC} = 4.5 \text{ V}, I_{OL} = 12 \text{ mA}$	0.25 0.4	0.25 0.4	V
VOL	$V_{CC} = 4.5 \text{ V}, I_{OL} = 24 \text{ mA}$		0.35 0.5	1 °
Ц	$V_{CC} = 5.5 \text{ V}, V_{I} = 7 \text{ V}$	0.1	0.1	mA
ΊΗ	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$	20	20	μΑ
IIL	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.4 \text{ V}$	-0.1	-0.1	mA
lcc	V _{CC} = 5.5 V, See Note 1	12 19	12 19	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

NOTE 1: ICC is measured with G grounded, P and Q at 4.5 V.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R	CC = 4.5 V L = 50 pF, L = 680 Ω, A = MIN to	MAX		UNIT
			SN54A	LS689	SN74ALS	6689	
			MIN	MAX	MIN	MAX	
tPLH	P	P=Q	10	30	10	25	ns
tPHL	Г		[.] 5	25	5	23] ""
^t PLH	Q.	<u>P=Ω</u>	10	30	10	25	ns
t _{PHL}	G.	1-4	5	25	5	23] '''
^t PLH	G	P=Q	8	30	8	25	ns
tPHL	u u	r=u	8	30	8	25] '''s

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747 OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS

AUGUST 1984 - REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Pull-Up Resistors Added for Data Bus Termination
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. In addition, 20 kilohm resistors have been added between all inputs and VCC. This eliminates adding external resistors in applications where the data bus must be at a high level whenever all other connecting devices are at a high impedance state.

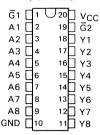
The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS746 provides inverted data and the 'ALS747 provides true data at the outputs.

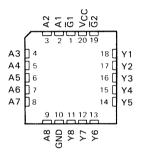
The -1 versions of the SN74ALS746 and SN74ALS747 parts are identical to the standard versions except that the recommended maximum IOL is increased to 48 milliampers. There are no -1 versions of the SN54ALS746 and SN54ALS747.

The SN54ALS746 and SN54ALS747 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN54ALS746 and SN74ALS747 are characterized for operation from 0°C to 70°C.

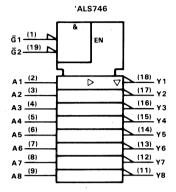
SN54ALS746, SN54ALS747 . . . J PACKAGE SN74ALS746, SN74ALS747 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS746, SN54ALS747 . . . FK PACKAGE (TOP VIEW)



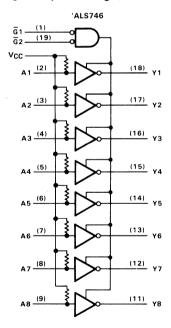
logic symbols†

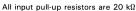


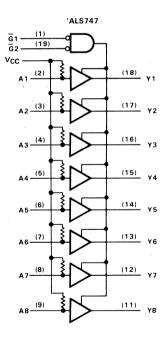
	'ALS	S747	
$\overline{G}_1 \xrightarrow{(1)} \overline{G}_2 \xrightarrow{(19)} \overline{C}_1$	&	EN	
A1 (2) A2 (3) A3 (4) A4 (5) A5 (6) A6 (7) A6 (8) A7 (9)		→	(18) Y1 (17) Y2 (16) Y3 (15) Y4 (14) Y5 (13) Y6 (12) Y7 (11) Y8

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)









SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747 OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54ALS746, SN54ALS747
	SN74ALS746, SN74ALS747 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SI	SN54ALS746 SN54ALS747			SN74ALS746			
		SI				SN74ALS747			
		MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
ViH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
loн	High-level output current			12			- 15	mA	
lou	Low-level output current			12			24	mA	
lOL	Low-level output current						48 [†]] ""^]	
T_A	Operating free-air temperature	- 55		125	0		70	°C	

 $^{^{\}dagger}$ The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

ł				S	SN54ALS746			74ALS	746	
P	ARAMETER	TEST C	ONDITIONS	s	N54ALS	747	SN	174ALS	747	UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{\parallel} = -18 \text{ mA}$			-1.2			- 1.2	V
			V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
Vон		$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	. 3.2		2.4	3.2		v
VOH			$I_{OH} = -12 \text{ mA}$	2] `
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA				2			
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
·OL		$V_{CC} = 4.5 V,$	I _{OL} = 24 mA¶					0.35	0.5	V
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
l _l	Α	$V_{CC} = 5.5 V,$	V _j = 5.5 V			0.1			0.1	mA
'1	G1, G2	$V_{CC} = 5.5 \text{ V},$	$V_I = 7 V$			0.1			0.1	111/2
ΊΗ	Α	Vcc = 5.5 V,	V ₁ = 2.7 V			-0.2			-0.2	mA
'IH	G1, G2	VCC = 3:3 V,	v ₁ = 2.7 v			20			20	μΑ
4L	Α	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.6			-0.6	mA
	Ğ1, Ğ2					-0.1			-0.1	
IO [§]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		- 112	- 30		- 112	mA
			Outputs high		7	12		7	12	
	'ALS746	$V_{CC} = 5.5 V,$	Outputs low		13	22		13	22	mA
Icc			Outputs disabled		11	19		11	19	
.00			Outputs high		6	14		6	14	
	'ALS747	$V_{CC} = 5.5 V$,	Outputs low		18	30		18	30	mA
	1	[Outputs disabled		12.5	22		12.5	22	



The 48 mA limit applies for the SN74ALS746-1 and SN74ALS747-1 only.

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

[¶]IOI = 48 mA for -1 versions.

SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747 OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS

'ALS746 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C 'ALS746	C _L R1 R2	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to LS746	MAX	ALS746	UNIT
tPLH		V	7.5	3	14	3	12	
tPHL	A	Y	5.6	2	11	2	9	ns
tPZH	G	V	9	5	. 18	5	15	
tPZL	G	T	12.5	8	24	8	20	ns
tPHZ	G	· ·	4	1	12	1	10	ns
t _{PLZ}	G Y		7	2	14	2	12	l lis

'ALS747 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to	MAX		UNIT
			'ALS747	SN54ALS747		SN74AL\$747		
			TYP	MIN	MAX	MIN	MAX	1
tPLH	A	V	8.7	4	17	4	14	ns
^t PHL	7 ^	T	7.4	2	12	2	10	1 115
^t PZH	G	V	9 .	5	18	5	15	
^t PZL	1 .	T T	12.5	8	24	8	20	ns
tPHZ	G		4	1	12	1	10	
tPLZ		, ,	7	2	14	2	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS756, SN54AS756, SN54AS757 SN74ALS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

D2661, DECEMBER 1983-REVISED MAY 1986

- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Eliminates the Need for 3-State Overlap Protection
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Open-Collector Versions of 'ALS240A, 'ALS241A, and 'AS240, 'AS241
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for three-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

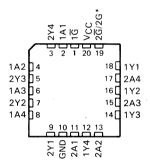
The -1 version of the SN74ALS756 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes. There is no -1 version of the SN54ALS756.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE

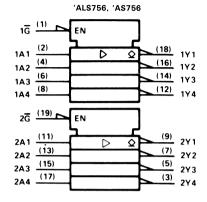
(TOP VIEW) 1G 1 U20 VCC 1A1 \Box 2 19 2G/2G* 18 T 1 Y 1 2Y4 [3 17 2A4 1A2 ∏4 2Y3∏5 16 1Y2 1A3∏6 15 2A3 14 T 1 Y 3 2Y2 7 1A4 13 2A2 2Y1 ∏9 12 1Y4 GND ∏10 11 2A1

SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)



*2G for 'ALS756, 'AS756 or 2G for 'AS757.

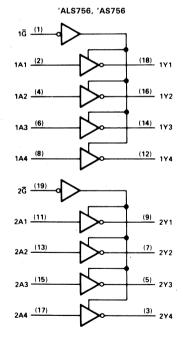
logic symbols†

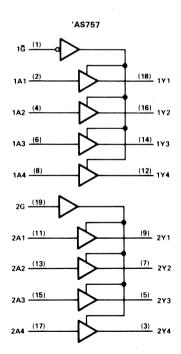


		'AS7	57		
1Ğ	(1)	EN			
1A1 1A2 1A3 1A4	(2) (4) (6) (8)	→	\$	(16) (14) (12)	Y1 Y2 Y3 Y4
2G 2A1 2A2 2A3 2A4	(19) (11) (13) (15) (17)	EN D		(9) 2 (7) 2 (5) 2	Y1 Y2 Y3

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)







SN54ALS756, SN74ALS756 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		7 V
Off-state output voltage		7 V
Operating free-air temperature range: \$	N54ALS756 55	°C to 125°C
	N74ALS756	0°C to 70°C
Storage temperature range	65	°C to 150°C

recommended operating conditions

		SN	SN54ALS756			SN74ALS756			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Voн	High-level output voltage			5.5			5.5	V	
101	Low-level output current			12			24	mA	
lor	Low-level output current						48 [†]	1 "'^	
TA	Operating free-air temperature	- 55		125	0		70	°C	

 $^{^\}dagger$ The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TECT CON	TEST CONDITIONS		SN54ALS756			SN74ALS756			
PARAMETER	TEST CON	IDITIONS	MIN T	гүр‡	MAX	MIN	TYP [‡]	MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			- 1.5	V	
¹ ОН	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1			0.1	mA	
V _{OL}	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA	,	0.25	0.4		0.25	0.4	V	
VOL.	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA §					0.35	0.5	*	
1	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
Iн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ	
ЧL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA	
1	Vac = 5.5.V	Output high		7	11		7	11	m A	
lcc	$V_{CC} = 5.5 V$	Output low		13	22		13	22	mA_	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$		$V_{CC} = 4.5$ $C_L = 50 \text{ p}$ $R_L = 500 \text{ s}$ $T_A = MIN$	F, Ω,	V,	UNIT
		['ALS756	SN54ALS756 SN74ALS756		ALS756		
] [TYP	MIN	MAX	MIN	MAX	
^t PLH	Α	Y	14	8	29	8	24	200
^t PHL		1 1	5	2	12	2	10	ns
tPLH	G		16	8	29	8	24	ns
[‡] PHL	1		12	6	23	6	20	1115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



 $^{^{\}S}$ V_{CC} = 4.75 V and I_{OL} = 48 mA for -1 versions.

SN54AS756, SN54AS757, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54AS756, SN54AS757
SN74AS756, SN74AS757 0°C to 70°C
Storage temperature range — 65 °C to 150 °C

recommended operating conditions

		SN54AS756 SN54AS757		SN74AS756 SN74AS757			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Voн	High-level output voltage			5.5			5.5	V
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		- 1	SN54AS756 SN54AS757		SI SI	UNIT		
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX]
v_{iK}		V _{CC} = 4.5 V,	$I_1 = -18 \text{ mA}$			-1.2			-1.2	V
ЮН		$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V		,	0.1			0.1	mA
VoL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA		0.55					V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 64 mA						0.55	1 °
1յ		$V_{CC} = 5.5 V$	V _I = 7 V			0.1			0.1	mA
ΙН		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
lu.	A inputs of 'AS757 only	Vcc = 5.5 V,	V _I = 0.4 V			- 1			1	
ΊL	All other inputs	vCC = 5.5 v,	V = 0.4 V			-0.5			-0.5	mA
	'AS756		Output high		9	15		9	15	
	A5756	V	Output low		51	80		51	80	1.1
Icc	'AS757	$V_{CC} = 5.5 V$,	Output high		21	33		21	33	mA
		S757			61	95		61	95	1

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.



SN54AS756, SN54AS757, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

'AS756 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = \text{MIN}$	F, Ω,	V,	UNIT
			SN54AS756 SN74AS756				
	1	1	MIN	MAX	MIN	MAX	1
t _{PLH}	Α	V	3	20	3	19	
^t PHL	7 ^	,	1	7	1	6	ns
t _{PLH}	G	V	3	22 3 19		19.5	ns
^t PHL	7 "	'	1	8.5	1	7.5	1 ''5

'AS757 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX				
			SN54	AS757	SN74	AS757		
			MIN	MAX	MIN	MAX		
tPLH	A		3	19.5	3	18.5	ns	
^t PHL	1 ^	Ţ.	1	7	1	6	115	
^t PLH	1 <u>G</u>		3	21	3	20	ns	
^t PHL	1 '6	,	1	8	1	7	115	
^t PLH	2G		3	22.5	3	21	ns	
^t PHL] 29	'	1	8.5	1	7.5	,13	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS758, SN54AS758, SN54AS759 SN74ALS758, SN74AS758, SN74AS759 QUADRUPLE BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

D2910, DECEMBER 1983-REVISED MAY 1986

- 2-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce Loading
- Open-Collector Versions of 'ALS242A, 'ALS243A and 'AS242, 'AS243
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These four-data-line transceivers are designed for asynchronous two-way communications between data buses.

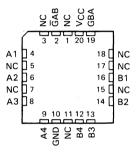
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum IQL is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0 °C to 70 °C.

SN54' . . . J PACKAGE SN74' . . . D OR N PACKAGE (TOP VIEW)

GAB [1	U 14	□vcc
NC (]2	13	☐ GBA
A1 []3	12	□ NC
A2]4	11	B1
A3 [5	10	☐ B2
A4 (] 6	9	B3
GND (72	8	☐ B4

SN54' . . . FK PACKAGE (TOP VIEW)



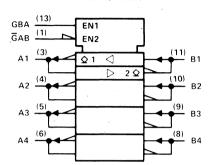
NC-No internal connection

FUNCTION TABLE

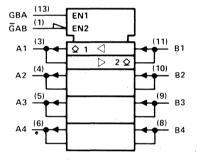
INF	PUTS	'ALS758	'AS759
GAB	GBA	'AS758	A5755
L	L	Ā to B	A to B
Н	Н	B to A	B to A
Н	L	Isolation	Isolation
	н	Latch A and B	Latch A and B
-	''	$(A = \overline{B})$	(A = B)

logic symbols†

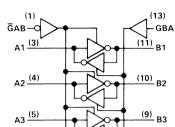
'ALS758, 'AS758



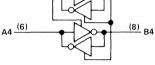
'AS759



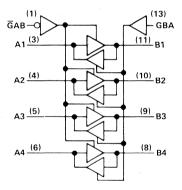
logic diagrams (positive logic)



'ALS758, 'AS758



'AS759



 $^{^{\}dagger} These$ symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 	7 V
Input voltage: All inputs	s and I/O ports	 	7 V
Operating free-air temp	erature range: SN54'	 55°C 1	to 125°C
	SN74'	 0°C	to 70°C
Storage temperature rai	nge	-65°C 1	to 150°C

SN54ALS758, SN74ALS758 QUADRUPLE BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

-		SN	SN54ALS758			SN74ALS758			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Vон	High-level output voltage			5.5			5.5	V	
1	Law lavel autout august			12			24	A	
lOL	Low-level output current						48 [†]	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

 $^{^{\}dagger}\text{The}$ extended limit applies only if VCC is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TECT OF	MOITIONS	SN54ALS	758	SN74	ALS	758	UNIT
	PARAMETER	1651 00	ONDITIONS	MIN TYP‡	MAX	MIN T	YP‡	MAX	UNII
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA		-1.2			-1.2	V
ЮН		$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V		0.1			0.1	mA
Vol		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA	0.25	0.4	(0.25	0.4	V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 24 mA §			(0.35	0.5	1 '
	Control inputs	$V_{CC} = 5.5 V$,	V ₁ = 7 V		0.1			0.1	mA
ij	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V		0.1			0.1	1 ""
1	Control inputs	Vcc = 5.5 V,			20			20	_
lН	A or B ports¶	νCC = 5.5 v,	$V_1 = 2.7 V$		20		_	20	μΑ
	Control inputs	V 55.V			-0.1			-0.1	
A or B ports	A or B ports¶	$V_{CC} = 5.5 \text{ V}, V_1 = 0.4 \text{ V}$	V ₁ = 0.4 V		-0.1			-0.1	mA
1		Outputs high		6	10		6	10	^
ICC		$V_{CC} = 5.5 V$	Outputs low	10	16		10	16	mA

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PRODUCTION DATA documents contain information current as of publication date Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega,$ $T_A = 25 ^{\circ}\text{C}$	$V_{CC} = 4.5 \text{ V to}$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega,$ $T_A = \text{MIN to M}.$:	UNIT
	1 1		'ALS758	SN54	ALS758	SN74/	ALS758	OWN
			TYP	MIN	MAX	MIN	MAX	1
tPLH	A az D	B or A	20	10	33	10	28	
[†] PHL	A or B	D OF A	5	2	15	2	12	ns
^t PLH	GBA	A	18	10	33	10	28	
^t PHL	GBA	A	13	6	25	6	21	ns
^t PLH	- GAB	В	18	10	33	10	28	
^t PHL	GAB	В	13	6	25	6	21	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



The 48 mA limit applies for the SN74ALS758-1.

 $^{{}^{\}S}I_{OL}$ = 48 mA for -1 versions.

For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN54AS758, SN74AS758 QUADRUPLE BUS TRANSCEIVERS WITH OPEN COLLECTOR OUTPUTS

recommended operating conditions

		SN54AS758 SN			SN	74AS7	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
VoH	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	SN54AS758	SN74AS758	UNIT
	PARAMETER	TEST CON	IDITIONS	MIN TYP† MAX	MIN TYPT MAX	UNII
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA	-1.2	-1.2	V
ІОН		$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V	0.1	0.1	mA
Vol		$V_{CC} = 4.5 V$,	$I_{OL} = 48 \text{ mA}$	0.55		V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 64 mA		0.55	ľ
lį	Control inputs	$V_{CC} = 5.5 V,$	V ₁ = 7 V	0.1	0.1	mA
"	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V	0.1	0.1	IIIA
ΊΗ	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V	20	20	
ЧH	A or B ports	VCC = 5.5 V,	V - 2.7 V	50	50	μΑ
Lo	Control inputs	$V_{CC} = 5.5 V_{c}$	V _I = 0.4 V	-0.5	-0.5	mA
Iμ	A or B ports [‡]	VCC = 5.5 V,	VI - 0.4 V	-0.5	-0.5	
lcc		Vcc = 5.5 V	Outputs high	17 27	17 27	mA
100		VCC = 5.5 V	Outputs low	38 60	38 60	1 '''^ I

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				
			SN54	AS758	SN74	AS758		
			MIN	MAX	MIN	MAX		
[†] PLH	A or B	B or A	3	20.5	3	19.5		
^t PHL	A OF B	BOTA	1	7	1	6	ns	
^t PLH	GBA	A	3	22	3	19.5	no	
^t PHL]	^	1	8.5	1	7.5	ns	
^t PLH	GАВ	В	3	22	3	21	ns	
t _{PHL}			1	8.5	1	8	115	

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.



 $^{^{\}dagger}All$ typical values are at V_{CC} = 5 V, T_A = 25 °C. $^{\ddagger}For$ I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

SN54AS759, SN74AS759 QUADRUPLE BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

		SN54AS759 SN74AS759		UNIT				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
ViH	. High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COM	DITIONS	SN54AS7	59	SN	74AS7	59	
	PARAMETER	TEST CONDITIONS		MIN TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA		- 1.2			-1.2	V
IOH		$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V		0.1			0.1	mA
VOL	,	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$		0.55				V
VOL		$V_{CC} = 4.5 \text{ V},$	IOL = 64 mA			l		0.55	1 °
l ₁	Control inputs	V _{CC} = 5.5 V,	V _I = 7 V		0.1			0.1	mA
"	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V		0.1			0.1	'''A
1	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V		20			20	
۱н	A or B ports	vCC = 5.5 v,	V = 2.7 V		50			50	μΑ
1	Control inputs	V F F V	V _I = 0.4 V		-0.5			-0.5	
IIL	A or B ports‡	$V_{CC} = 5.5 V,$	V = 0.4 V		- 1			- 1	mA
laa		V 5 5 V	Outputs high	27	43		27	43	^
¹cc		$V_{CC} = 5.5 V$	Outputs low	47	74		47	74	mA _.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$					
			SN54.	AS759	SN74	AS759	1		
			MIN	MAX	MIN	MAX	1		
tPLH	A == D	D A	3	21	3	20			
^t PHL	A or B	B or A	1	7	1	6	ns		
^t PLH	GBA	А	3	21	3	20	ns		
^t PHL	- GBA	1	1	8	1	7	115		
t _{PLH}	GAB	В	3	22.5	3	21	ns		
^t PHL	7 GAB	l B	1	8.5	1	7.5	115		

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

 $^{^{\}dagger}All$ typical values are at VCC = 5 V, TA = 25 °C. $^{\ddagger}For$ I/O ports, the parameters I $_{IH}$ and I $_{IL}$ include the off-state output current.

SN54ALS760, SN54AS760, SN74ALS760, SN74AS760 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983 - REVISED MAY 1986

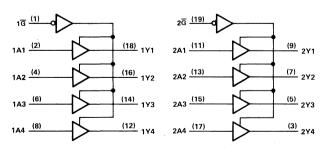
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Eliminates the Need for 3-State Overlap Protection
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Open-Collector Versions of 'ALS244 and 'AS244
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the 'ALS756, 'AS756, and 'AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical \overline{G} (active-low input control) inputs, and complimentary G and \overline{G} inputs.

The SN54ALS760 and SN54AS760 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS760 and SN74AS760 are characterized for operation from 0 °C to 70 °C.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

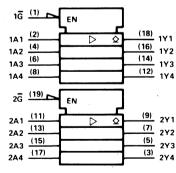
SN54ALS760, SN54AS760 . . . J PACKAGE SN74ALS760, SN74AS760 . . . DW OR N PACKAGE (TOP VIEW)

1 G 🗆	1	U20	Jvcc
1A1 🗆	2	19] 2Ğ
2Y4 🗌	3	18] 1Y1
1A2 🗌	4	17]2A4
2Y3 🗌	5	16] 1Y2
1A3 🗌	6	15]2A3
2Y2 🗌	7	14] 1Y3
1A4 🗌	8	13]2A2
2Y1 🔲	9	12] 1Y4
GND [10	11]2A1

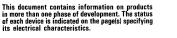
SN54ALS760, SN54AS760 . . . FK PACKAGE (TOP VIEW)

	274 1A1 1G VCC	7	
	3 2 1 20 1	9	
1A2 🛮 4		18[1 Y 1
2Y3 🛭 5		17	2A4
1A3 [] 6		16	1Y2
2Y2 🛮 7		15	2A3
1A4 [] 8		14	1Y3
	9 10 11 12 13	3	
	2Y1 GND 2A1 1Y4	7 W 7	

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





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recommended operating conditions

	,	SN54ALS760 SN74ALS760			UNIT			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	SN	54ALS7	60	SN	UNIT		
PANAIVIETEN	1531 CO	LOT COMPITIONS		TYP [†]	MAX	MIN	TYP	MAX	ONIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V
ЮН .	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1			0.1	mA
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.5		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	
l ₁ ,	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
¹ıн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
l _{IL}	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.1			-0.1	mA
laa	V _{CC} = 5.5 V	Outputs high		9			9		mA
lcc	vCC = 2.5 v	Outputs low		15			15		IIIA

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX					
			SN54ALS760	SN74ALS760	1			
	:		MIN TYP† MAX	MIN TYP† MAX	1			
tPLH	^	V	22	22				
^t PHL	A	'	13	13	ns			
tPLH	G	v	25	25	no			
tPHL	g	Y	24	24	ns			

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS760, SN74AS760 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54AS760
SN74AS7600°C to 70°C
Storage temperature range65°C to 150°C

recommended operating conditions

		SI	N54AS7	60	SI	N74AS7	60	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
ViH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Voн	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	TEST CONDITIONS		SN54AS760			SN74AS760			
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX		
VIK	$V_{CC} = 4.5 V,$	$I_1 = -18 \text{ mA}$			- 1.2			-1.2	V	
Чон	$V_{CC} = 4.5 V,$	$V_{OH} = 5.5 V$			0.1			0.1	mA	
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 48 mA			0.55				V	
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 64 \text{ mA}$					0.55	ľ		
I _I	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA	
ИН	$V_{CC} = 5.5 V$,	V ₁ = 2.7 V			20			20	μΑ	
I _{IL} G	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA	
'IL A	VCC = 5.5 V,	V = 0.4 V			- 1			- 1	, IIIA	
laa	V _{CC} = 5.5 V	Outputs high		20	32		20	32	mA	
lcc	VCC = 5.5 V	Outputs low		60	94		60	94	111/4	

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		UNIT			
	,		SN54	AS760	SN74	AS760	
			MIN	MAX	MIN	MAX	
tPLH	. А	V	3	19.5	3	18.5	
tPHL	^		1	7	1	6	ns
^t PLH	G	V	3	19.5	3	18.5	
^t PHL	G G	Ť	1	8	1	7	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS762, SN54ALS763, SN54AS762, SN54AS763 SN74ALS762, SN74ALS763, SN74AS762, SN74AS763 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- 'ALS762 and 'AS762 Have True and Complementary Outputs
- 'ALS763 and 'AS763 Have Complementary G and G Inputs
- Open-Collector Outputs Drive Bus Lines or **Buffer Memory Address Registers**
- Eliminates the Need for 3-State Overlap Protection
- Current Sinking Capability Up to 64 mA
- Dependable Texas Instruments Quality and Reliability

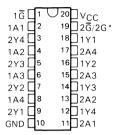
description

These octal buffers and line drivers are designed specifically to improve the performance of threestate memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G (active-low output control) inputs, and complementary G and $\bar{\mathsf{G}}$ inputs.

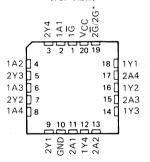
The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum IQI is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS', SN54AS' . . . J PACKAGE SN74ALS', SN74AS' . . . DW OR N PACKAGE (TOP VIEW)

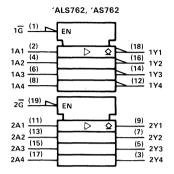


SN54ALS', SN54AS' . . . FK PACKAGE (TOP VIEW)



*2G for 'ALS762, 'AS762 and 2G 'ALS763, 'AS763

logic symbols†

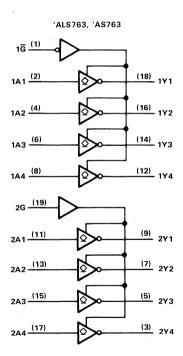


	ALS76	3, 'AS76	3	
1G (1)	EN]	
1A1 (2)		DΩ	(18)	1Y1
1A2 (4) 1A3 (6)			(16)	1Y2
1A3 (8)			(12)	174
2G (19)	EN		ĺ	
2A1 (11)		$\frac{\Box}{\Box}$	(9)	2Y1
2A2 (13)			(7)	2Y2
2A3 (17)			(3)	2Y3
244	Щ.			214

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'ALS762, 'AS762 1G (1) (<u>18)</u> 1Y1 1A1 (2) (<u>16)</u> 1Y2 1A2 (4) (<u>14)</u> 1Y3 1A3 (6) 1A4 (8) (12) 1Y4 2G (19) 2A1 (11) (9) 2Y1 2A2 (13) (7) 2Y2 (5) 2Y3 2A3 (15) 2A4 (17) (3) 2Y4





SN54ALS762, SN74ALS762 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	absolute	maximum	ratings	over	operating	free-air	temperature	range	(unless	otherwise noted)
---	----------	---------	---------	------	-----------	----------	-------------	-------	---------	-----------------	---

Supply voltage, V _{CC}
Input voltage
Off-state output voltage
Operating free-air temperature range: SN54ALS762
SN74ALS762
Storage temperature range

recommended operating conditions

		SN	SN54ALS762 SN74ALS762					
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
VoH	High-level output voltage			5.5			5.5	V
la.	Low-level output current			12			24	mA
lOL	Low-level output current						48†	""
TA	Operating free-air temperature	- 55		125	0		70	°C

[†]The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

The 48-mA limit applies for the SN74ALS762-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	SI	154ALS	762	SN	74ALS7	62	UNIT
FANAIVIETEN	lESI C	TEST CONDITIONS		TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	II = -18 mA			-1.2			-1.2	٧
10Н	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1			0.1	mA
	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V _{OL}	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	V
	$(I_{OL} = 48 \text{ mA fo})$	r -1 versions)					0.33	0.5	
lį	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			- 0.1			-0.1	mA
ICC 'ALS762	V _{CC} = 5.5 V	Outputs high		11			11		mA
ICC ALS762	VCC = 5.5 V	Outputs low		18			18		IIIA

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

'ALS762 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25 °C 'ALS762	C _L = 50 pl R _L = 680 s			UNIT
			TYP	MIN MA	K MIN	MAX	1
t _{PLH}	A		17				
^t PHL	^		6				ns
^t PLH	G	V	14				
tPHL	J	'	18				ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PRODUCT PREVIEW documents contain information INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

recommended operating conditions

		SI	154ALS7	763	SN	74ALS	763	LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
1	Low lovel output owners			12			24	mA
lor	Low-level output current	-					48†	'''A
TA	Operating free-air temperature	- 55		125	0		70	°C

[†]The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48-mA limit applies for the SN74ALS763-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

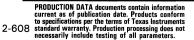
24.5	AAAFTED	TEST SOMBITIONS		SI	154ALS	763	SN	LINUT		
PAH	AMETER	IESI C	TEST CONDITIONS		TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I = -18 mA			- 1.2			- 1.2	V
ЮН		$V_{CC} = 4.5 V,$	V _{OH} = 5.5.V			0.1			0.1	mA
		$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
v_{OL}		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	V
			A for -1 versions)				0.55		0.5	
lj		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lіН		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
ΙΙL		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
1	'ALS763	V 5 5 V	Outputs high		7	11		7	11	
lcc	AL3/63	$V_{CC} = 5.5 V$	Outputs low		14	22		14	22	mA

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

'ALS763 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 680 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω , T_A = MIN to MAX				UNIT		
			'ALS763	SN54ALS763		SN74ALS763		1		
			TYP	MIN	MAX	MIN	MAX			
[†] PLH	А	^	V	16	7	28	7	25	ns	
^t PHL		1	5	2	11	2	9	113		
t _{PLH}	G		-		18	8	28	9	25	ns
tPHL			13	5	25	5	21	113		
^t PLH	G	· · · · · · · · · · · · · · · · · · ·	18	8	28	9	25	ns		
^t PHL		0)		13	5 -	25	5	21	1113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.





SN54AS762, SN54AS763, SN74AS762, SN74AS763 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN COLLECTOR OUTPUTS

recommended operating conditions

			SN54AS762 SN54AS763		SN74AS762 SN74AS763			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	1
V _C C	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Voн	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54AS762 SN54AS763			SN74AS762 SN74AS763		
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.2			- 1.2	V
Тон		V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1			0.1	mA
VOL		$V_{CC} \approx 4.5 \text{ V},$	I _{OL} = 48 mA			0.55				V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 64 mA						0.55	ľ
ſμ		$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA
ΉΗ		$V_{CC} \approx 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
	'AS762	V _{CC} = 5.5 V,	V ₁ = 0.4 V		-1				- 1	
ηL	2A inputs only									mA
	All others					-0.5			-0.5	
	'AS762	V _{CC} = 5.5 V	Output high		15	23		15	· 23	
loo		ν(C = 3.5 V	Output low		55	87		55	87	mA
lcc l	'AS763	V _{CC} = 5.5 V	Output high		10	16		10	16] '''^
			Output low		52	82		52	82	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

SN54AS762, SN54AS763, SN74AS762, SN74AS763 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

'AS762 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS762 \qquad SN74AS762$			UNIT	
	*		MIN	MAX	MIN	MAX		
tpLH	1.0	11/	3	20	3	19	ns	
^t PHL	1A	1Y	1	7	1	6	115	
^t PLH	2A .	2Y	3	19.5	3	18.5	ns	
^t PHL	ZA .	21	1	. 7	1	6	115	
^t PLH	G	1Y	3	22	3	19.5	ne	
^t PHL	٥		1	8	1	7.5	ns '	
^t PLH	G	2Y	3	20	3	19	ns	
tPHL	, ,	21	1	8	1	7	1 ''5	

'AS763 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT	
			SN54	AS763	SN7	4AS763		
			MIN	MAX	MIN	MAX	1	
^t PLH	А	Υ	3	20	3	19		
t _{PHL}			1	7	1	6	ns	
^t PLH	· G	V	3	22	3	19.5	ns	
^t PHL	G	Ţ	1	8.5	1	7.5	7 '''	
^t PLH	G	, ,	3	22	3	20	ns	
^t PHL	9	ľ	1	8.5	1	. 8] '''5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS804A, SN54AS804B, SN74ALS804A, SN74AS804B HEX 2-INPUT NAND DRIVERS

D2661, DECEMBER 1982 - REVISED MAY 1986

- High Capacitive Drive Capability
- 'ALS804A has Typical Delay Time of 4 ns (C_L = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate
- 'AS804B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per Gate
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

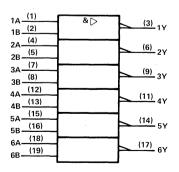
These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS804A and SN54AS804B are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS804A and SN74AS804B are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each driver)

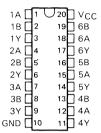
IN	PUTS	OUTPUT
Α	В	Y
Н	Н	L
L	×	н
X	L	н

logic symbol†

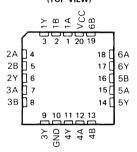


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

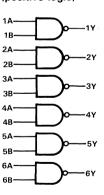
SN54ALS804A, SN54AS804B . . . J PACKAGE SN74ALS804A, SN74AS804B . . . DW OR N PACKAGE (TOP VIEW)

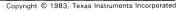


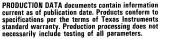
SN54ALS804A, SN54AS804B . . . FK PACKAGE (TOP VIEW)



logic diagram (positive logic)









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
Operating free-air temperature range:	SN54ALS804A
	SN74ALS804A 0 °C to 70 °C
Storage temperature range	-65°C to 50°C

recommended operating conditions

		SN	54ALS80)4A	SI	174ALS	804A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон	High-level output current			- 12			- 15	miA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLE	rionic	SNS	4ALS8	04A	SN	74ALS8	04A	T
PARAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -0.4 mA	V _{CC} -2			V _{CC} -2			
Vou	V _{CC} = 4.5 V,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		. v
Voн	V _{CC} = 4.5 V,	1 _{OH} = -12 mA	2						V
	V _{CC} = 4.5 V,	IOH = -15 mA				2			
VoL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5]
lį .	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lін	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25$	- 30		-112	- 30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.9	2.5		0.9	2.5	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		7	12		7	12	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 \text{ °C}$ 'ALS804A TYP	C _L R _L T _A	C = 4.5 V = 50 pF, = 500 Ω, = MIN to LS804A	MAX	LS804A MAX	UNIT
^t PLH	A or B	V	4	2	9	2	7	200
t _{PHL}	700	'	4	2	. 9	2	8	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54AS804B
	SN74AS804B 0 °C to 70 °C
Storage temperature range	65°C to 50°C

recommended operating conditions

		SN54AS804B			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	\ \
ІОН	High-level output current			- 40			- 48	mA
loL	Low-level output current			40			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLE	FLONIC	SN	4AS80	4B	SN	74AS80)4B	UNIT
PARAMETER	TEST CONDIT	TIONS	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} – 2			V _{CC} - 2			
VOH	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		1 _v 1
V ∪H	$V_{CC} = 4.5 V,$	$I_{OH} = -40 \text{ mA}$	2						1 1
	V _{CC} = 4.5 V _i .	I _{OH} = -48 mA				2			
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 40 mA		0.25	0.5				V
VOL.	V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5	1 '
II.	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lΉ	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ПL	V _{CC} = 5.5 V,	V ₁ = 0.4 V			-0.5			- 0.5	mA
10‡	V _{CC} = 5.5 V,	$V_0 = 2.25$	- 50		- 200	- 50		- 200	mA
ГССН	V _{CC} = 5.5 V,	$V_I = 0 V$		3.5	5		3.5	5	mA
lCCL	V _{CC} = 5.5 V,	V _I = 4.5 V		16	27		16	27	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A \approx 25 ^{\circ}\text{C}$.

switching characteristics (see note 1)

PARAMETER	AMETER FROM TO (OUTPUT)		C R	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega$ $T_A = \text{MIN to MAX}$				
			SN54	AS804B	SN74	AS804B		
			MIN	MAX	MIN	MAX	1 1	
tPLH	A or B	V	1	5	1	4		
t _{PHL}	AOIB	T	1	5	1	4	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS805A, SN54AS805B, SN74ALS805A, SN74AS805B HEX 2-INPUT NOR DRIVERS

D2661, DECEMBER 1982 - REVISED MAY 1986

- High Capacitive Drive Capability
- 'ALS805A has Typical Delay Time of 4.2 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate
- 'AS805B has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of 12 mW per Gate
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

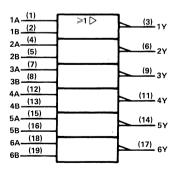
These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS805A and SN54AS805B are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS805A and SN74AS805B are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each driver)

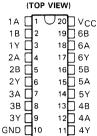
ſ	INP	UTS	OUTPUT
Γ	Α	В	Υ
ſ	Н	Х	L
	X	Н	L
1	L	L	н

logic symbol†

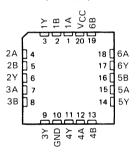


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

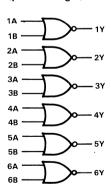
SN54ALS805A, SN54AS805B . . . J PACKAGE SN74ALS805A, SN74AS805B . . . DW OR N PACKAGE



SN54ALS805A, SN54AS805B . . . FK PACKAGE (TOP VIEW)



logic diagram (positive logic)





 $SN74ALS805A 0 ^{\circ}C to 70 ^{\circ}C \\ Storage temperature range -65 ^{\circ}C to 150 ^{\circ}C \\$

recommended operating conditions

		SN	54ALS8	05A	SN	74ALS8	05A	LIBUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	. 4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 12			- 15	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

040445750	TEST SOUR		SN	54ALS8	05A	SN	MIN TYP† VCC-2 2.4 3.2 2 0.25 0.35		N74ALS805A		
PARAMETER	TEST CONDI	IIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT		
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V		
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2					
V _{OH}	$V_{CC} = 4.5 V,$	IOH = -3 mA	2.4	3.2		2.4	3.2] _v		
VOH	V _C C = 4.5 V,	I _{OH} = -12 mA	2					,	7 °		
	V _{CC} = 4.5 V,	I _{OH} = -15 mA				2			1		
Vol	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V		
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	1 °		
l _l	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA		
IH	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ		
l L	$V_{CC} = 5.5 V,$	V _I = 0.4 V .			-0.1			-0.1	mA		
lo [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA		
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		2	4		2	4	mA		
ICCL	V _{CC} = 5.5 V,	V _I = 4.5 V		8	14		8	14	mA		

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 \text{ °C}$ $ALS805A$ TYP	C _L R _L T _A	C = 4.5 V = 50 pF, = 500 Ω, = MIN to LS805A	MAX	LS805A MAX	UNIT
tPLH	A D		4	2	9	2	7	
t _{PHL}	A or B	Ť	4	2	9	2	8	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) SN74AS805B 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		SN	54AS80)5B	SN	74AS80	05B	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-40			-48	mA
lOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	ITIONE	SN	54AS8	05B	SN	74AS80)5B	LIBUT
PARAMETER	TEST COND	ITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			
V	V _{CC} = 4.5 V,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -40 mA	2						v
	V _{CC} = 4.5 V,	I _{OH} = -48 mA				2			
V	$V_{CC} = 4.5 V,$	IOL = 40 mA		0.25	0.5				V
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5	·
lj .	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
. IH	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
lıL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
10‡	V _{CC} = 5.5 V,	V _O = 2.25 V	- 50		- 200	- 50		- 200	mA
Iссн	V _{CC} = 5.5 V,	V _I = 0 V		6.5	.10		6.5	10	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		20	32		20	32	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	SN54	$V_{CC} = 4$ $C_L = 50$ $R_L = 500$ $T_A = MIR$ AS805B	Ω, N to MAX	S805B MAX	UNIT
t _{PLH}	A 2		1	4.8	1	4.3	
^t PHL	A or B	i '	1	4.8	1	4.3	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS808A, SN54AS808B, SN74ALS808A, SN74AS808B HEX 2-INPUT AND DRIVERS

D2661, DECEMBER 1982 - REVISED MAY 1986

- High Capacitive Drive Capability
- 'ALS808A has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate
- 'AS808B has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

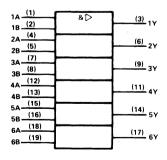
These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS808A and SN54AS808B are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS808A and SN74AS808B are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each driver)

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Н
L	X	L
X	L	L

logic symbol[†]

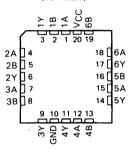


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

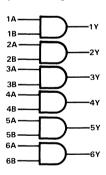
SN54ALS808A, SN54AS808B . . . J PACKAGE SN74ALS808A, SN74AS808B . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS808A, SN54AS808B . . . FK PACKAGE (TOP VIEW)



logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS808A -55°C to 125°C SN74ALS808A 0°C to 70°C

Storage temperature range -65°C to 150°C

recommended operating conditions

		SN	54ALS8	A80	SN	74ALS8	A80	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ГОН	High-level output current			-12			- 15	mA
lor	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDIT	TIONS	SN	54ALS8	08A	SN	74ALS	808A	
PARAMETER	TEST CONDI	IUNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
	$V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
	$V_{CC} = 4.5 V$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		
VoH	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2]
	V _{CC} = 4.5 V,	I _{OL} = -15 mA				. 2]
Vol	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA		-			0.35	0.5	ľ
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lΗ	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$	1.		20			20	μΑ
IL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.1			-0.1	mA
lo‡	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		4.5	7		4.5	7	mA
^I CCL	V _{CC} = 5.5 V,	$V_I = 0 V$		8	16		8	16	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 $^{\circ}$ C

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS808A	C R T SN54A	CC = 4.5 $CC = 50$ pF, $CC = 500$ $CC = 5$	o MAX	LS808A	UNIT
			TYP	MIN	MAX	MIN	MAX	1
tPLH	A or B	V	6	2 ,	11	2	9	ns
tPHL	7. 51 5		4	1	10	1	8] '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54AS808B -55°C to 125°C SN74AS808B 0°C to 70°C

Storage temperature range -65°C to 150°C

recommended operating conditions

		SI	V54AS8	08B	SN	74AS80	08B	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
ГОН	High-level output current			- 40			- 48	mA
lor	Low-level output current			40			48	mA
Тд	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEAT COMPA	FIONO	SN	154AS8	08B	SN	174AS8	08B	LIBUT
PARAMETER	TEST CONDIT	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		
Vон	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -40 \text{ mA}$	2						
VОН	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -48 mA				2			7 °
VOL	V _{CC} = 4.5 V,	I _{OL} = 40 mA		0.25	0.5				V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5	1 °
II	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
lΗ	V _{CC} = 5.5 V,	$V_1 = 2.7 V$			20			20	μΑ
IIL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
10‡	V _{CC} = 5.5 V,	V _O = 2.25 V	- 50		- 200	- 50		-200	mA
ГССН	V _{CC} = 5.5 V,	V _I = 4.5 V		8	13		8	13	mA
ICCL	V _{CC} = 5.5 V,	V _I = 0 V		20	33		20	33	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}, T_{A} = 25 ^{\circ}\text{C}$

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega$ $T_A = MIN \text{ to}$	э МАХ		UNIT
			SN54	AS808B	SN744	AS808B	
			MIN	MAX	MIN	MAX	
^t PLH	A or B		1	6.5	1	6	no.
t _{PHL}	7.01.0		1	6.5	1	6	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[†]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS810, SN54AS810, SN74ALS810, SN74AS810 OUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

D2837, MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline"
 Packages, Ceramic Chip Carriers, and Standard Plastic
 and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

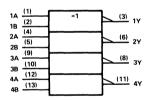
description

These devices contain four independent Exclusive-NOR gates. They perform the Boolean functions $Y = \overline{A \oplus B} = (A + \overline{B}) \cdot (\overline{A} + B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS810 and SN54AS810 are characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ALS810 and SN74AS810 are characterized for operation from 0° to 70°C.

logic symbol[†]



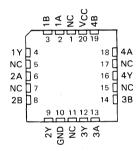
FUNCTION TABLE (each gate)

(outil gate)						
INP	UTS	OUTPUT				
Α	В	Υ				
L	L	Н				
L	Н	L				
Н	L	L				
Н	Н	Н				

SN54ALS810, SN54AS810 . . . J PACKAGE SN74ALS810, SN74AS810 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS810, SN54AS810 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

exclusive-NOR logic

An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR

These are five equivalent Exclusive-NOR symbols valid for an 'ALS810 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT



The output is active (High) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



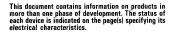
The output is active (High) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (Low) if an odd number of inputs (i.e., only 1 of the 2) are active.

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[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

SN54ALS810, SN74ALS810 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range	SN54ALS810
	SN74ALS810 0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN	SN54ALS810			SN74ALS810		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-0.4			-0.4	mA
lor	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	154ALS	B10	SN	74ALS8	10	LIBUT
PANAMETEN	TEST CONI	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			-1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		Vcc-	2		V
Vai	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA					0.35	0.5	· ·
11	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΉΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	- 30		-112	mA
lcc	V _{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 R _L = 500	-	5 V,	UNIT
			SN54	ALS810	SN74	ALS810	
			MIN	MAX	MIN	MAX	
tPLH	A or B		5	23	5	20	no
^t PHL	(other input low)	'	3	17	3	14	ns
^t PLH	A or B		5	21	5	18	ns
^t PHL	(other input high)	'	3	17	3	14	115



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS810, SN74AS810 QUADRUPLE 2-INPUT EXCLUSIVE NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS810	5°C
SN74AS810	0°C
Storage temperature range -65 °C to 15	O°C

recommended operating conditions

	•	SI	SN54AS810		SN74AS810			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
IOH	High-level output current			- 2	-		- 2	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	N54AS8	10	SI	N74AS8	10	LIBUT
PARAMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	II = -18 mA			- 1.5			-1.5	٧
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			V
V _{OL}	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I _I	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			- 0.1			-0.1	mA
10 [‡]	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
¹ ССН	$V_{CC} = 5.5 V$			18			18		mA
^I CCL	$V_{CC} = 5.5 V$			15			15		mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	AMETER FROM TO (OUTPUT)		V _{CC} = 4.5 C _L = 50 pf R _L = 500 (T _A = MIN - SN54AS810	UNIT	
			MIN TYP† MAX	MIN TYP† MAX	1
^t PLH	A or B	Y	3.4	3.4	ns
^t PHL	(other input low)	'	5.3	5.3] '''
tPLH	A or B	V	3.4	3.4	
^t PHL	(other input high)	1	5.3	5.3	ns

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS811, SN74ALS811, SN54AS811, SN74AS811 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

D2837, MARCH 1984-REVISED MAY 1986

- Package Options Include Plastic "Small Outline"
 Packages, Ceramic Chip Carriers, and Standard Plastic
 and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

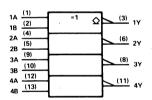
description

These devices contain four independent Exclusive-NOR gates with open-collector outputs. They perform the Boolean functions $Y = \overline{A \oplus B} = (A + \overline{B}) \cdot (\overline{A} + B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS811 and SN54AS811 are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN74ALS811 and SN74AS811 are characterized for operation from 0 °C to 70 °C.

logic symbol†



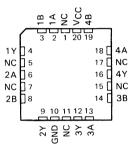
FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
А В		Υ
L	L	Н
L	Н	L
Н	L	L
н н		н

SN54ALS811, SN54AS811 . . . J PACKAGE SN74ALS811, SN74AS811 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS811, SN54AS811 . . . FK PACKAGE (TOP VIEW)



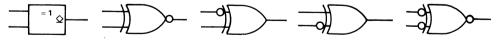
NC - No internal connection

Pin numbers shown are for D, J, and N packages.

exclusive-NOR logic

An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR



These are five equivalent Exclusive-NOR symbols valid for an 'ALS811 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT



The output is active (high) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (low) if an odd number of inputs (i.e., only 1 of the 2) are active.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.



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[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS811, SN74ALS811 QUADRUPLE 2-INPUT EXCLUSIVE NOR GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		7 V
Off-state output voltage		7 V
Operating free-air temperature range:	SN54ALS811	
	SN74ALS811	
Storage temperature range		

recommended operating conditions

		SN	SN54ALS811			SN74ALS811			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Vон	High-level output voltage			5.5		***************************************	5.5	V	
lOL	Low-level output current			4			8	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TFOT /	CANDITIONS	SN	SN54ALS811			SN74ALS811			
PARAMETER	1591 (CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			1.5			- 1.5	٧	
ЮН	$V_{CC} = 4.5 V$,	$V_{OH} = 5.5 V$			0.1			0.1	mA	
V _{OL}	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	\ \	
	$V_{CC} = 4.5 V$,	I _{OL} = 8 mA					0.35	0.5	V	
Ц	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
lН	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ	
IIL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			- 0.1			-0.1	mA	
^I cc	$V_{CC} = 5.5 V,$	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R _L = 2 k T _A = MII	pF,		UNIT
			SN54/	ALS811	SN74		
			MIN	MAX	MIN	MAX]
[†] PLH	A or B		25	. 60	25	55	ns
[†] PHL	(other input low)		5	30	5	28	115
[†] PLH	A or B		20	55	20	50	ns
[†] PHL	(other input high)	<u>'</u>	5	28	5	23	115



SN54AS811, SN74AS811 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 7 V
Input voltage		 7 V
Off-state output voltage		 7 V
Operating free-air temperature range:	SN54AS811	 -55°C to 125°C
	SN74AS811	 0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		s	SN54AS811			SN74AS811			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
ViH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
Voн	High-level output voltage			5.5			5.5	V	
lOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		sı	SN54AS811			SN74AS811			
FANAIVIETEN	1531	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 4.5 \text{ V},$	^I I = -18 mA			- 1.5			-1.5	V	
loн	V _{CC} = 4.5 V	V _{OH} = 5.5 V			2			2	mA	
V _{OL}	$V_{CC} = 4.5 V$,	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V	
lį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA	
lн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μÀ	
l _I L	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA	
Іссн	$V_{CC} = 5.5 \text{ V}$			18			18		mA	
ICCL	V _{CC} = 5.5 V			15			15		mA	

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{o}C.$

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $RL = 2 \text{ k}\Omega$ $T_A = \text{MIN}$		UNIT
			SN54AS811	SN74AS811	
			MIN TYP† MAX	MIN TYP [†] MAX	
^t PLH	A or B	Υ	10.0	10.0	ns
^t PHL	(other input low)	1	5.7	5.7	113
^t PLH	A or B	٧	10.0	10.0	ns
^t PHL	(other input high)	r	5.7	5.7	1115

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

SN54AS821, SN54AS822, SN74AS821, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983-REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29821 and AM29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flipflops. On the positive transition of the clock the Q outputs on the 'AS821 will be true, and on the 'AS822 will be complementary to the data input.

A buffered output-control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control (\overline{OC}) does not affect the internal operation of the flipflops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS' family is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74AS' family is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

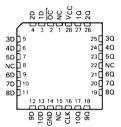
SN54AS821 . . . JT PACKAGE SN74AS821 . . . DW OR NT PACKAGE (TOP VIEW)

> 724 V_{CC} 1D 🗖 2 22 20 2D 3 30 21 30 4D 🗆 5 5D 🛮 6 19 5Q 6D 18 60 7D 🛮 8 17/170 16 80 15 9Q

SN54AS821 . . . FK PACKAGE SN74AS821 . . . FN PACKAGE (TOP VIEW)

13 CLK

GND 12

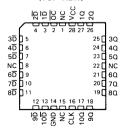


SN54AS822 . . . JT PACKAGE SN74AS822 . . . DW OR NT PACKAGE

(TOP VIEW)

SN54AS822 . . . FK PACKAGE SN74AS822 . . . FN PACKAGE

(TOP VIEW)



NC-No internal connection

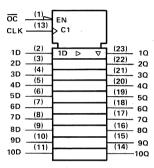


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'AS821 FUNCTION TABLE (EACH FLIP-FLOP)

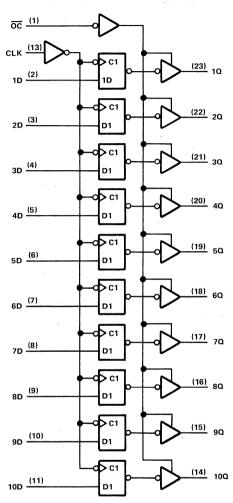
	INPUTS		OUTPUT
ŌĊ	CLK	D	Q
L	1	Н	Н
L	↑	L	L
L	L	X	Ω ₀
Н	X	X	z

'AS821 logic symbol†



 $^{\dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS821 logic diagram (positive logic)



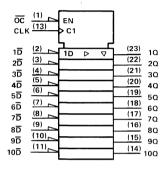
Pin numbers shown are for DW, JT, and NT packages.

SN54AS822, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS822 FUNCTION TABLE (EACH FLIP-FLOP)

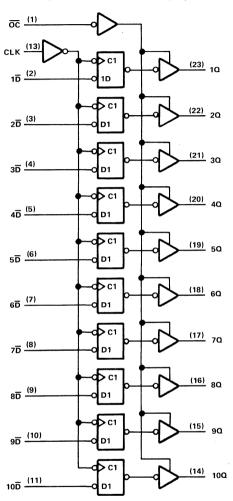
	INPUTS		OUTPUT
ŌC	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	X	Ω0
н	X	X	Z

'AS822 logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS822 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

SN54AS821, SN54AS822, SN74AS821, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54AS821, SN54AS822	-55°C to 125°C
SN74AS821, SN74AS822	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			SN54AS821 SN54AS822			SN74AS821 SN74AS822		
		MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8		***************************************	0.8	V
Гон	High-level output current			- 24			- 24	mA
lOL	Low-level output currrent			32			48	mΑ
t _w	Pulse duration, CLK high or low	9			8			ns
t _{su}	Setup time, data before CLK↑	7			6			ns
th	Hold time, data after CLK↑	0			0			ns
TA	Operating free-air temperature	- 55		125 -	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST CO	NDITIONS	1	N54AS8 N54AS8		SN74AS821 SN74AS822			UNIT
				MIN	TYP†	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -2 \text{ mA}$	v _{cc} -	2		v _{cc} -	2		
Vон		$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$	2.4	3.2		2.4	3.2		\ \ \
		$V_{CC} = 4.5 V$,	$I_{OH} = -24 \text{ mA}$	2			2			
VOL		$V_{CC} = 4.5 V$,	$I_{OL} = 32 \text{ mA}$		0.25	0.5				V
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5	· .
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 \text{ V}$			50			50	μΑ
^l OZL		$V_{CC} = 5.5 V;$	$V_0 = 0.4 V$			- 50			- 50	μΑ
l _l		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
^I IН		$V_{CC} = 5.5 \text{ V},$	$V_1 = 2.7 V$			20			20	μΑ
Iμ		$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.5			-0.5	mA
lO‡		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Outputs high		55	88		55	88	
	'AS821		Outputs low		68	109		68	109]
lcc -		V F F V	Outputs disabled		70	113		70	113	mA
		V _{CC} = 5.5 V	Outputs high		55	88		55	88	'''A
	1 1 1	Outputs low		68	109		68	109		
			Outputs disabled		70	113		70	113	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS821, SN54AS822, SN74AS821, SN74AS822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1	$V_{CC} = 4.5 \text{ V} \cdot C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to N}$ $SN54AS821$		AS821	UNIT
			SN54	AS822	SN74	AS822]
			MIN	MAX	MIN	MAX	1
[†] PLH	CLK	Any Q	3.5	9	3.5	7.5	ns
^t PHL	CLK		3.5	11.5	3.5	10.5	1 '18
^t PZH	oc	Any Q	4	12	4	11	ns
^t PZL		Ally Q	4	13	4	12] '''
^t PHZ	ōc	Any Q	2	10	2	8	ns
tPZL	1	Any d	2	10	2	8	1 1/3

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS823, SN54AS824 SN74AS823, SN74AS824

9-BIT BUS INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984-REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29823 and AM29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable (CLKEN) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'AS823 has noninverting D inputs and the 'AS824 has inverting D inputs. Taking the CLR input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input (\overline{OC}) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

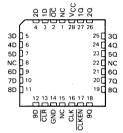
SN54AS823 . . . JT PACKAGE SN74AS823 . . . DW OR NT PACKAGE

(TOP VIEW) ō€ П₁ U24 VCC 1 D C 23 10 22/1 20 2D 🖂 3 3D 🗖 21 30 4D [20 40 19 50 50 7 6D □ 18 1 60 7D ٦ 70 16 80 8D 🗇 9D 10 15 9Q CLR 14 CLKEN

SN54AS823 . . . FK PACKAGE SN74AS823 . . . FN PACKAGE (TOP VIEW)

13 T CLK

GND 712



SN54AS824 . . . JT PACKAGE SN74AS824 . . . DW OR NT PACKAGE

(TOP VIEW)

oc [17 C	24	Vcc
1 D	2	23	10
2D []3	22	2Q
ЗĎ []4	21	30
4D [5	20	4Q
5D [6	19	5Q
6D [7	18	6Q
7D [8	17	70
8D [9	16	80
9D [10	15	90
CLR [11	14	CLKEN
GND []12	13	CLK

SN54AS824 . . . FK PACKAGE SN74AS824 . . . FN PACKAGE

(TOP VIEW)



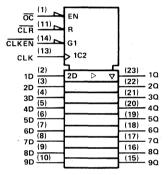
Texas VI

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS823 FUNCTION TABLE

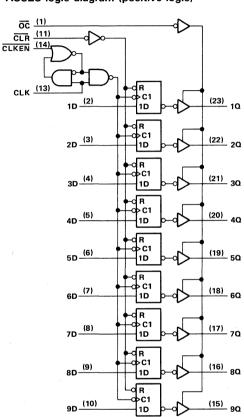
	OUTPUT				
оc	CLR	CLKEN	CLK	D	α
L	L	Х	X	X	L
L	н	L .	↑	н	н
L	н	L	1	L	L
L	н	Н	X	X	α ₀
н	X	Χ	Х	X	z

'AS823 logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 Pin numbers shown are for DW, JT, and NT packages.

'AS823 logic diagram (positive logic)



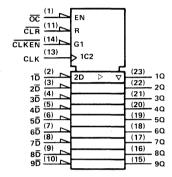


SN54AS824, SN74AS824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS824 FUNCTION TABLE

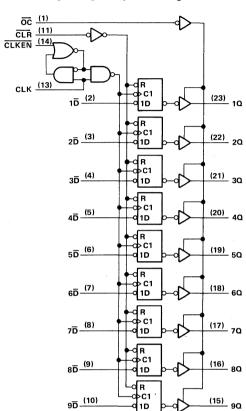
		INPUTS			OUTPUT
ōc	CLR	CLKEN	CLK	D	a
L	L	Х	Х	X	L
L	Н	L	1	н	L
L	Н	L	↑	L	н
L	Н	Н	X	X	α ₀
н	X	×	X	×	z

'AS824 logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS824 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

SN54AS823, SN54AS824, SN74AS823, SN74AS824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

Operating free-air temperature range: SN54AS823, SN54AS824 – 55°C to 125°C SN74AS823, SN74AS824 0°C to 70°C

Storage temperature range -65 °C to 150 °C

recommended operating conditions

				SN54AS823 SN54AS824		SN74AS823 SN74AS824			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	v
ЮН	High-level output current				- 24			- 24	mA
lOL	Low-level output current				32			48	mA
	Pulse duration	CLR low	5			4			ns
tw	ruise duration	CLK high or low	9			8			
	Catura tima a	CLR inactive	8			8			
t _{su}	Setup time	Data	7			6			ns
	before CLK↑	CLKEN high or low	7			6			
th	Hold time, CLKEN or data after CLK↑		0			0			ns
ŤΑ	Operating free-air temperatur	e	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		1	N54AS8 N54AS8		SN74AS823 SN74AS824		UNIT	
				MIN	TYP [†]	MAX	MIN	TYP	MAX	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	$V_{IOH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2		
Vон		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA	2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5 V$,	I _{OH} = -24 mA	2			2			
Vai		$V_{CC} = 4.5 V,$	I _{OL} = 32 mA		0.3	0.5				V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5	V
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			50			50	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 50			- 50	μΑ
կ		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΉΗ		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
ηL		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
10 [‡]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Outputs high		49	80		49	80	
	'AS823	$V_{CC} = 5.5 V$	Outputs low		61	100		61	100	mA
laa		· ·	Outputs disabled		64	103		64	103	
100	lcc		Outputs high		49	80		49	80	
	'AS824	$V_{CC} = 5.5 V$	Outputs low		61	100		61	100	mA
	1		Outputs disabled		64	103		64	103	1

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



SN54AS823, SN54AS824, SN74AS823, SN74AS824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	i i			,	UNIT
						4AS823	
			MIN	MAX	MIN	4AS824 MAX	
tPLH	CLIK	Any Q	3.5	9	3.5	7.5	
tPHL	CLK		3.5	12	3.5	11	ns
tPHL	CLR	Any Q	3.5	14	3.5	13	ns
^t PZH	oc	Any O	4	12	4	11	
^t PZL	00	Any Q	4	13	4	12	ns
^t PHZ	oc	Any Q	2	10	2	8	ns
^t PLZ		73117 42	2	10	2	8	''5

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54AS825, SN54AS826 SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS D2825, JUNE 1984—REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29825 and AM29826
- Improved IOH Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

description

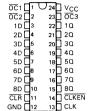
These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has non-inverting D inputs and the 'AS826 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ input low causes the eight Ω outputs to go low independently of the clock.

Multiuser buffered output-control inputs $(\overline{OC}1,\overline{OC}2,$ and $\overline{OC}3)$ can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a busorganized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

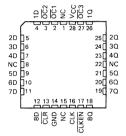
SN54AS825 . . . JT PACKAGE SN74AS825 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS825 . . . FK PACKAGE SN74AS825 . . . FN PACKAGE

(TOP VIEW)



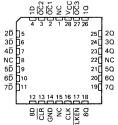
SN54AS826 . . . JT PACKAGE SN74AS826 . . . DW OR NT PACKAGE

(TOP VIEW)

OC1	1 0	24	Vcc
OC2	2	23	OC3
1Đ 🗌	3	22	10
2D 🗌	4	21	20
3D 🗌	5	20	30
4D 🗌	6	19	40
5D 🗌	7	18	5Q
6Ď 🗌	8	17	6Q
7Ē 🗀	9	16	7Q
8Ď 🗌	10	15	80
CLR [11	14	CLKEN
GND [12	13	CLK

SN54AS826 . . . FK PACKAGE SN74AS826 . . . FN PACKAGE

(TOP VIEW)



NC-No internal connection

TEXAS INSTRUMENTS

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SN54AS825, SN54AS826, SN74AS825, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54AS' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74AS' family is characterized for operation from 0 °C to 70 °C.

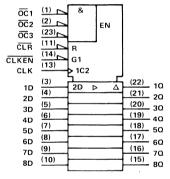
'AS825 FUNCTION TABLE

		INPUTS			OUTPUT
OC*	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	X	L
L	Н	L	1	н	н
L	Н	L	1	L	L
L	Н	Н	X	Х	σ_0
Н	X	X	X	Х	Z

 $\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high.

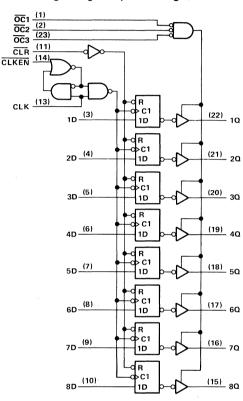
 $\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

'AS825 logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS825 logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.



SN54AS826, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

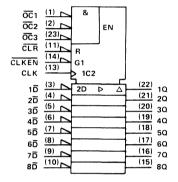
'AS826 FUNCTION TABLE

		INPUTS			OUTPUT
ōc∗	CLR	CLKEN	CLK	D	a
L	L	Х	X	Х	L
L	н	L	†	Н	L
L	Н	L	†	L	н
L	Н	Н	X	Х	a_0
н	Х	×	Х	X	z

 $\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high.

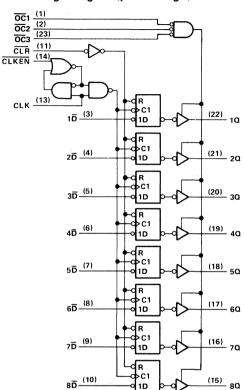
 $\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

'AS826 logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'AS826 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



SN54AS825, SN54AS826, SN74AS825, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Operating free-air temperature range:

recommended operating conditions

			İ	SN54AS SN54AS		l	SN74AS SN74AS		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
lон	High-level output current				-24			- 24	mA
lOL	Low-level output current				32			48	mA
	Pulse duration	CLR low	5			4			ns
t _w	ruise duration	CLK high or low	9			8			115
		CLR inactive	8			8			
t _{su}	Setup time before CLK↑	Data	7			6			ns
		CLKEN high or low	7			6			
th	Hold time, CLKEN or data afte	r CLK↑	0			0			ns
TA	Operating free-air temperature		- 55		125	.0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COMPU	TEST CONDITIONS		N54AS8 N54AS8		SN74AS825 SN74AS826			UNIT
r	ANAINETEN	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	JOINIT
V_{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$i_{OH} = -2 \text{ mA}$	V _{CC} -	2		Vcc-	2		
Voн		$V_{CC} = 4.5 V,$	I _{OH} = -15 mA	2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -24 mA	2			2			
Vol		$V_{CC} = 4.5 V,$	$I_{OL} = 32 \text{ mA}$		0.3	0.5				V
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$					0.35	0.5	\ \ \
lozh	,	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 50			- 50	μΑ
lj ,		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lН		$V_{CC} = 5.5 V,$	$V_1 = 2.7 \text{ V}$			20			20	μA
l _{IL}		$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.5			-0.5	mA
lo‡		$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
			Outputs high		45	73		45	73	
	'AS825	$V_{CC} = 5.5 V$	Outputs low		56	90		56	90	mA
			Outputs disabled		59	95		59	95	1
¹ CC			Outputs high		45	73		45	73	
	'AS826	$V_{CC} = 5.5 V$	Outputs low		56	90		56	90	mA
			Outputs disabled		59	95		59	95	7

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54AS825, SN54AS826, SN74AS825, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	RAMETER FROM (INPUT)	ТО (ОИТРИТ)		$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R1=500$ Ω , $R2=500$ Ω , $T_A=MIN$ to MAX				
				AS825 AS826	l	4AS825 4AS826		
			MIN	MAX	MIN	MAX		
t _{PLH}	011/		3.5	9	3.5	7.5		
tPHL	CLK	Any Q	3.5	11.5	3.5	11	ns	
tPHL	CLR	Any Q	3.5	14	3.5	13	ns	
^t PZH	ōc	Any Q	4	12	4	11	ns	
tPZL		Ally d	4	13	4	12	_ ''s	
tPHZ	ōc	Any Q	2	10	2	8	ns	
tPLZ		7, 4	2	10	2	8	.,,	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 - REVISED MAY 1986

SN54ALS832A, SN54AS832B, SN74ALS832A, SN74AS832B

High Capacitive Drive Capability

- 'ALS832A has Typical Delay Time of 4.8 ns (C_I = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate
- 'AS832B has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil **DIPs**
- Dependable Texas Instruments Quality and Reliability

description

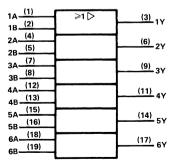
These devices contain six independent 2-input OR drivers. They perform the Boolean functions Y = A + B or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54ALS832A and SN54AS832B are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS832A and SN74AS832B are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

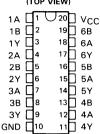
INP	UTS	OUTPUT
Α	В	Y
Н	Х	Н
X	Н	н
L	L	L

logic symbol†

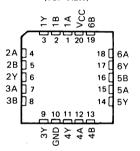


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

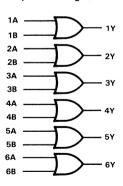
SN54ALS832A, SN54AS832B . . . J PACKAGE SN74ALS832A, SN74AS832B . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS832A, SN54AS832B . . . FK PACKAGE (TOP VIEW)



logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS832A -55 °C to 125 °C SN74ALS832A °C to 70 °C Storage temperature range -65 °C to 150 °C

recommended operating conditions

		SN	SN54ALS832A		SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
^I ОН	High-level output current			- 12			- 15	mA
l _{OL}	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST SOUR	FIGNIC	SNE	4ALS8	32A	SN	74ALS8	32A	LIBUT
PARAMETER	TEST CONDI	IONS	MIN	TYP [†]	MAX	MIN	TYP	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
. Van	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2] ,
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -12 mA	2]
	$V_{CC} = 4.5 V,$	$l_{OH} = -15 \text{ mA}$				2			
Vai	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5]
Ξ	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
¹ ІН	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
ΙΙL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	-30		-112	mA
¹ ссн	$V_{CC} = 5.5 V,$	V _I = 4.5 V		6	9		6	9	mA
^I CCL	V _{CC} = 5.5 V,	V _I = 0 V		9.5	16		9.5	16	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}, T_{A} = 25 ^{\circ}\text{C}$

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS832A	C R T	$C_{CC} = 4.5$ $C_{L} = 50 \text{ pF}$ $C_{L} = 500 \Omega$ $C_{A} = MIN \text{ total}$ $C_{L} = 500 \Omega$	o MAX	V, LS832A	UNIT
			TYP	MIN	MAX	MIN	MAX	1
tPLH	A or B	V	6	2	11	2	9	ns
^t PHL	1 7016	, ,	4	1	10	1.	8] '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54AS832B
	SN74AS832B °C to 70 °C
Storage temperature range	65°C to 150°C

		Si	SN54AS832B		SI	32B	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	DINIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Іон	High-level output current			-40			- 48	mA
lor	Low-level output current			40			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDIT	TIONE	SN	54AS83	32B	SN	UNIT		
PARAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} - 2			V _{CC} – 2			
.,	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		l v
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -40 mA	2						
	V _{CC} = 4.5 V,	I _{OH} = -48 mA				2			
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 40 mA		0.25	0.5				V
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5	
łį	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
IH ·	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ήL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.5			-0.5	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 50		- 200	-50		- 200	mA
Iссн	V _{CC} = 5.5 V,	V _I = 4.5 V		11	17		11	17	mA
ICCL	V _{CC} = 5.5 V,	V _I = 0 V		22	36		22	36	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50$ pF, $R_L = 500 \Omega$ $T_A = MIN to AS832B$	MAX	AS832B	UNIT
	·		MIN	MAX	MIN	MAX	
tPLH	A or B	V	1	7	1	6.3	ns
^t PHL	A 01 B	'	1	7	1	6.3	113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS841, SN54AS841, SN54ALS842, SN54AS842 SN74ALS841, SN74AS841, SN74ALS842, SN74AS842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus Driving Latches
 Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

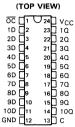
The ten latches are transparent D-type. The 'ALS841 and 'AS841 have noninverting data (D) inputs. The 'ALS842 and 'AS842 have inverting \overline{D} inputs.

A buffered output control (\overline{OC}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

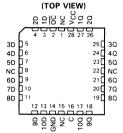
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS841 and SN74ALS842 parts are identical to the standard versions except that the recommended maximum IoL is increased to 48 milliamperes. There are no -1 versions of the SN54ALS841 and SN54ALS842.

SN54ALS841, SN54AS841 . . . JT PACKAGE SN74ALS841, SN74AS841 . . . DW OR NT PACKAGE



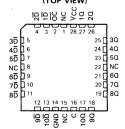
SN54ALS841, SN54AS841 . . . FK PACKAGE SN74ALS841, SN74AS841 . . . FN PACKAGE



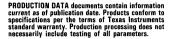
SN54ALS842, SN54AS842 . . . JT PACKAGE SN74ALS842, SN74AS842 . . . DW OR NT PACKAGE



SN54ALS842, SN54AS842 . . . FK PACKAGE SN74ALS842, SN74AS842 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection





The SN54ALS841, SN54AS841, SN54ALS842, and SN54AS842 are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to $125\,^{\circ}$ C. The SN74ALS841, SN74AS841, SN74ALS842, and SN74AS842 are characterized for operation from $0\,^{\circ}$ C to $70\,^{\circ}$ C.

FUNCTION TABLES

'ALS841, 'AS841

IN	IPUTS	OUTPUT	
ŌĊ	C D		Q
L	Н	Н	Н
L	Н	L	L
L	L	X	a_0
Н	Х	Х	z

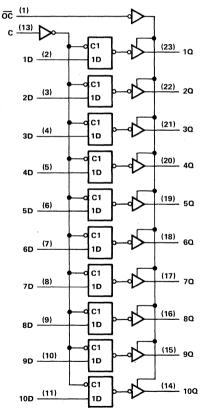
'ALS842, 'AS842

- 11	IPUTS	OUTPUT	
oc	С	D	Q
L	Н	Н	L
L	Н	L	н
L	L	Х	a_0
Ŧ	Х	Х	Z

'ALS841, 'AS841 logic symbol†

OC (13)	EN C1	
1D (2)	1D D V	(23)
2D (3)		(22) 20
3D (4)		(21) 30
4D (5)	}	(20) 40
5D (6)	}	(19) 5Q
6D (7)		(18) 6Q
(8)	 	(17) 70
7D (9)	}	(16) 8Q
8D (10)		(15) 90
9D (11)]	(14)
10D	1	100

'ALS841, 'AS841 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS842, 'AS842 logic symbol[†]

8Đ

(10)

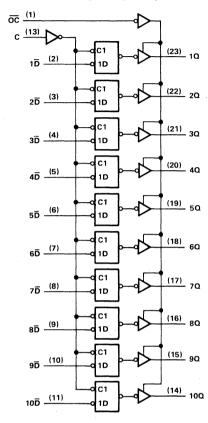
(11) 10D

(13)C1 (2<u>3)</u> 1Q (2) 1D 10 (3) (22) 2D (4) (21) 30 3Ď (5) (20) 4Đ (6) (19)50 (7) (18)6D 60 (17) 70 (8) 7Ď (9) (16)

80

(15) 90 (14) 100

'ALS842, 'AS842 logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range:	
SN54ALS841, SN54AS841, SN54ALS842, SN54AS842	-55°C to 125°C
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842	0°C to 70°C
Storage temperature range	-65°C to 150°C

Pin numbers shown are for DW, JT, and NT packages.

		SN	54ALS	341	SN	74ALS	341	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			-2.6	mA
loL	Low-level output current			12			24	mA
·OL	zow lover output durient						48 [†]	"""
t _w	Pulse duration, enable C high	25			20			ns
t _{su}	Setup time, data before enable C↓	16			10			ns
th	Hold time, data after enable C↓	7			5			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}$ The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	CONDITIONS	SN	154ALS8	41	SN	74ALS8	341	UNIT
FANAMETER	TEST CONDITIONS		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	ONIT
VIK	$V_{CC} = 4.5 V$,	i _l = -18 mA			- 1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		V _{CC} -:	2		
VoH	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 V$,	$l_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V _{OL}	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	V
	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 48 \text{ mA} (-1 \text{ versions})$					0.35	0.5	
Iozh	$V_{CC} = 5.5 \text{ V},$	V _O = 2.7 V			20			20	μΑ
IOZL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20			·- 20	μΑ
II	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IJL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1			- 0.1	mA
lo§	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	- 30		- 112	mA
		Outputs high		19	. 30		19	30	
lcc	$V_{CC} = 5.5 V$	Outputs low		38	62		38	62	mA
		Outputs disabled		23	40		23	40	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. § The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS841, SN74ALS841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A		pF, Ο Ω, Ο Ω,	SN MIN	C _L = R1 = R2 = T _A = 54ALS	50 pF. 500 Ω 500 Ω MIN to	, , o MAX	74ALS	841 MAX	UNIT
^t PLH	D	Q		8.5	11	2		15	2		. 13	20
^t PHL		u u		8.5	11	2		15	. 2		13	ns
^t PLH	С	Q		14	18	7		25	7		21	ns
^t PHL	C	Q.		17	23	8		30	8		26	115
^t PZH	оc	Q		7.5	10	2		14	2		12	ns
^t PZL		ď		7.5	10	2		14	2		12	115
^t PHZ	<u>oc</u>	Q		6	8	2		12	2		10	ns
tPLZ	L	4		7	9	2		14	2		12	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS842, SN74ALS842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

		SI	SN54ALS842			74ALS	342	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 1			- 2.6	mA
loL	Low-level output current			12			24 48 [†]	mA
t _w	Pulse duration, enable C high	25			20		481	ns
t _{su}	Setup time, data before enable C↓	16			10			ns
th	Hold time, data after enable C↓	7			5			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}$ The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	CONDITIONS	SN	154ALS	842	SN	174ALS8	342	UNIT
FANAMETER	TEST CONDITIONS		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	ONT
. V _{IK}	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$.V _{CC} -	2		v _{cc} -	2		
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		,
	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V _{OL}	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	V
	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 48 \text{ mA} (-1 \text{ versions})$					0.35	0.5	
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
lį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 0.1			- 0.1	mA
IO§	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
		Outputs high		20	35		20	35	
lcc	$V_{CC} = 5.5 V$	Outputs low		48	74		48	74	mA
		Outputs disabled		27	44		27	44	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



⁵The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS842, SN74ALS842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	C = 5 = 500 = 500 = 500 = 25° ALS842	pF,) Ω,) Ω,) C	SN54	$V_{CC} = 4.5$ $C_L = 50 \text{ pf}$ $R1 = 500 \text{ s}$ $R2 = 500 \text{ s}$ $T_A = MIN$ $ALS842$ MAX	=, Ω, Ω, to MAX	V, ALS842 MAX	UNIT
^t PLH	D	Q		11	15	4	22	4	18	ns
t _{PHL}] [Q.		8	11	3	17	3	13	1115
^t PLH	С	Q ·		17	23	8	31	8	27	ns
^t PHL		<u>u</u>		13	18	6	24	6	20	115
t _{PZH}	<u>oc</u>	Q		8	10	2	14	2	12	ns
^t PZL		<u>u</u>		8	11	2	14	2	12	1115
^t PHZ	<u>oc</u>	Ω		6	8	1	12	1	10	ns
^t PLZ		4		7	. 9	2	14	2	12	""

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



		SI	SN54AS841			174AS8	41	UNIT
		SI	154AS8	42	SI	SN74AS842		
		MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
^I ОН	High-level output current			- 24			- 24	mA
loL	Low-level output current			32			48	mA
t _w	Pulse duration, enable C high	5			4			ns
t _{su}	Setup time, data before enable C↓	3.5			2.5			ns
th	Hold time, data after enable C↓	3.5			2.5			ns
TA	Operating free-air temperature	- 55		125	0	***************************************	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER	TEST CO	TEST CONDITIONS		N54AS8 N54AS8	• •		N74AS8 N74AS8		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			-1.2	٧
		$V_{CC} = 4.5 \text{ V to 5.5}$	$5 \text{ V}, \text{ I}_{OH} = -2 \text{ mA}$	v _{cc} -	2		v _{cc} -	2		
Vон		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA	2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -24 \text{ mA}$	2			2			
		$V_{CC} = 4.5 V,$	I _{OL} = 32 mA		0.25	0.5				V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 48 mA					0.35	0.5	V
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			50			50	μΑ
IOZL		$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 50			- 50	μΑ
l ₁		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ЧН		$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
ΊL		$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.5			-0.5	mA
lo‡		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Outputs high		36	60		36	60	
	'AS841		Outputs low		58	94		58	94	
loo		$V_{CC} = 5.5 \text{ V}$	Outputs disabled		56	92		56	92	mA
Icc		VCC - 5.5 V	Outputs high		38	62		38	62	IIIA
	'AS842		Outputs low		60	97		60	97	
			Outputs disabled		58	95		- 58	95	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS841, SN54AS842 SN74AS841, SN74AS842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)		$V_{CC} = 4.5 \text{ N}$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to}$,	UNIT
			SN54	AS841	SN74	IAS841	
			MIN	MAX	MIN	MAX	
^t PLH	D	α	1	8.5	1	6.5	ns
^t PHL	,	ų d	1	10	1	9	''5
[†] PLH	С	Q	2	13	2	12	ns
^t PHL		4	2	13	2	12	1115
^t PZH	ŌĊ	Q	2	13.5	2	10.5	ns
^t PZL	00	4	2	15	2	13.5	'''
tPHZ	ōc	α	1	10	1	8	ns
tPLZ	00	3	1	10	1	8	113

'AS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ N}$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to}$	MAX		UNIT
				AS842		4AS842	Į.
			MIN	MAX	MIN	MAX	
^t PLH	ā	Q	1	11	1	8.5	ns
tPHL		<u> </u>	1	10	1	9	113
^t PLH	С	Q	2	13	2	12	ns
^t PHL	<u> </u>	<u>u</u>	2	13	2	12	115
^t PZH	ŌC	a	2	14.5	2	12	ne
^t PZL		<u> </u>	2	15	2	12.5	ns
tPHZ	oc	Q	1	10	1	. 8	ns
tPLZ	00	<u> </u>	1	10	1	. 8	113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS843, SN54AS843, SN54ALS844, SN54AS844 SN74ALS843, SN74AS843, SN74ALS844, SN74AS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, DECEMBER 1983 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- **Bus-Structured Pinout**
- Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or **Buses with Parity**
- **Buffered Control Inputs to Reduce DC** Loading
- Power-Up High Impedance
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control (OC) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

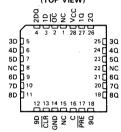
The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The -1 versions of the SN74ALS843 and SN74ALS844 parts are identical to the standard versions except that the recommended maximum IQL is increased to 48 milliamperes. There are no -1 versions of the SN54ALS843 and SN54ALS844.

SN54ALS843, SN54AS843 . . . JT PACKAGE SN74ALS843, SN74AS843 . . . DW OR NT PACKAGE

(TOP VIEW) U24 VCC 23 1 1 Q 22 2 2 Q 1D F 2D [21 30 3D F 20 40 4D 15 5D [50 19 18 60 7D 78 7Q 17 8D [16 80 9D 10 15 90 CLR 711 PRE GND ☐12 13 C

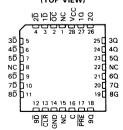
SN54ALS843, SN54AS843, . . FK PACKAGE SN74ALS843, SN74AS843 . . . FN PACKAGE (TOP VIEW)



SN54ALS844, SN54AS844 . . . JT PACKAGE SN74ALS844, SN74AS844 . . . DW OR NT PACKAGE

> (TOP VIEW) OC | 1 | 2 | 2 | 3 | 3 | 5 | 6 | 6 | 23 10 22 20 21 30 40 20 40 19 50 60 [70 [18 GQ 70 8D 0 9D 0 0 CLR 0 16 BQ 15 90 14 PRE GND 12 13 C

SN54ALS844, SN54AS844 . . . FK PACKAGE SN74ALS844, SN74AS844 ... FN PACKAGE (TOP VIEW)



NC-No internal connection



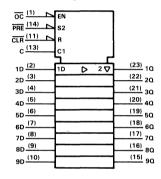
SN54ALS843, SN54AS843, SN54ALS844, SN54AS844 SN74ALS843, SN74AS843, SN74ALS844, SN74AS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0°C to 70°C.

'ALS843, 'AS843 FUNCTION TABLE

		NPUT	S		OUTPUT
PRE	CLR	<u>oc</u>	С	D	a
L	Х	L	Х	Х	H
н	L	L	Х	Х	L
н	Н	L	Н	L	L
Н	Н	L	Н	Н	Н
Н	Н	L	L	X	αo
×	X	Н	X	Х	z

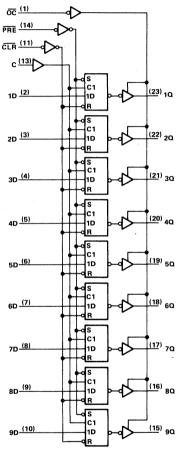
'ALS843, 'AS843 logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS843, 'AS843 logic diagram (positive logic)



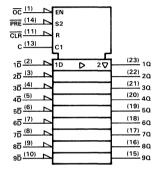


SN54ALS843, SN54AS843, SN54ALS844, SN54AS844 SN74ALS843, SN74AS843, SN74ALS844, SN74AS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS844, 'AS844 FUNCTION TABLE

		INPUT	S		OUTPUT
PRE	CLR	\overline{oc}	С	ō	Q
L	Х	L	X	Х	Н
н	L	L	X	Χ	L
Н	Н	L	Н	L	н
н	Н	L	Н	Н	L
н	Н	L	L	X	QΟ
×	Х	Н	Х	Χ	z

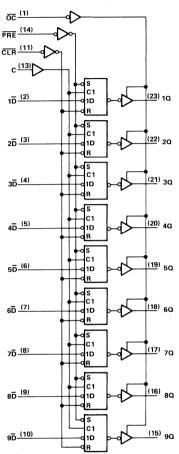
'ALS844, 'AS844 logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS844, 'AS844 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS', SN54AS'
SN74ALS', SN74AS'
Storage temperature range



				154ALS8 154ALS8		SN SN	UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	55	4.5	5	5.5	V
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0. 7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
lÒF	Low-level output current				12			24 48 [†]	mA
	B.1	CLR or PRE low	40			35			1
tw	Pulse duration	C high	25			20			ns
t _{su}	Setup time, data before enable C1		16			10			ns
th	Hold time, data after enable C↓		7			5			ns
TA	Operating free-air temperature		-55		125	0		70	°C

 $^{^\}dagger$ The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST	CONDITIONS		54ALS			74ALS8		UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	$6 \text{ V, I}_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -	2		
VOH		$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	. 3.3					V
		$V_{CC} = 4.5^{\circ}V$,					2.4	3.2		
		$V_{CC} = 4.5 \text{ V},$			0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	V
		$V_{CC} = 4.75 V$,	$I_{OL} = 48 \text{ mA} (-1 \text{ versions})$					0.35	0.5	
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
li ,		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ЧН		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL .		$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 0.1			-0.1	mA
lo§		$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA
			Outputs high		21	36		21	36	
	'ALS843		Outputs low		41	67		41	67	
l'cc		V _{CC} = 5.5 V	Outputs disabled		25	42		25	42	mA
100		VCC = 0.0 V	Outputs high		21	36		21	36	111/2
	'ALS844		Outputs low		41	72		41	72	
			Outputs disabled		28	48		28	48	



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. § The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS843, SN54ALS844 SN74ALS843, SN74ALS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$ $ALS843$ MIN TYP MAX		SN5	V, VALS843	UNIT			
tPLH			IVIIIV	7	11	MIN 2	MAX 15	MIN 2	MAX 13	
tPHL	D	Q		11	15	4	20	4	18	ns
t _{PLH}	С	Q		12	18	5	25	5	21	
tPHL	C	u l		16	23	8	30	8	26	ns
^t PLH	PRE	Q		13	19	5	25	5	22	, no
t _{PHL}	TILL	4		19	26	4	35	6	30	ns
^t PLH	CLR	Q		19	26	4	35	6	30	
t _{PHL}	OLIT	<u> </u>		14	21	6	27	6	23	ns
^t PZH	ōc	Q.		7	10	2	14	2	12	ns
tPZL	30			9	12	4	16	4	14	115
tPHZ	ŌĊ	Q		6	9	2	12	2	10	ns
tPLZ				7	10	2	14	2	12	115

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS844		SN5	V, ALS844	UNIT			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	D	Q		11	16	4	22	4	20	
tPHL	1 5	4		9	13	3	17	3	15	ns
^t PLH	С	Ω		17	24	8	32	8	29	ns
^t PHL	7	4		14	19	6	26	6	22	115
tPLH	PRE	Ω		13	19	5	25	5	22	
tPHL	7	4		19	26	4	35	6	30	ns
^t PLH	CLR	Q		19	26	4	35	6	30	
^t PHL	7	"		16	23	8	29	8	25	ns
tPZH	oc	Q		10	15	2	19	4	17	
tPZL	1 00	"		12	18	3	22	5	20	ns
^t PHZ	oc	Q		7	10	1	12	1	11	
tPLZ	7 00 .	"		5	9	1	14	1	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

			- 1	N54AS8 N54AS8		i	N74AS8 N74AS8		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage		4.5	5	55	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				- 24			- 24	mA
lOL	Low-level output current				32			48	mA
	Pulse duration, enable C high	CLR or PRE low	5			4			
tw	ruise duration, enable e nign	C high	5			4			ns
t _{su}	Setup time, data before enable C↓		3.5			2.5			ns
th	Hold time, data after enable C↓		3.5			2.5			ns
		PRE	17			15			
t _r	Recovery time	CLR	16			14			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST COM	NDITIONS	1	N54AS		1	N74AS8 N74AS8		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	٧
		$V_{CC} = 4.5 V$	$l_{OH} = -2 \text{ mA}$	v _{cc} -	2		v _{cc} -	2		
۷он		$V_{CC} = 4.5 \text{ V},$	I _{OH} = -15 mA	2.4	3.2		2.4	3.2		V
		$V_{CC} = 4.5 V$,	I _{OH} = -24 mA	2			2			
Vol		$V_{CC} = 4.5 V$	I _{OL} = 32 mA		0.25	0.5				v
VOL.		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5	\
lozh		$V_{CC} = 5.5 \text{ V},$	V _O = 2.7 V			50			50	μΑ
lozL		VCC = 5.5 V,	V _O = 0.4 V			- 50			- 50	μΑ
IĮ		VCC = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA
Ιн		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL		$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.5			-0.5	mA
lo‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
			Outputs high		37	62		37	62	
	'AS843		Outputs low		56	92		56	92	
· lcc		$V_{CC} = 5.5 \text{ V},$	Outputs disabled		56	92		56	92	mA
100		ν _{CC} = 3.5 ν,	Outputs high		39	64		39	64] '''^
	'AS844		Outputs low		58	95		58	95	
			Outputs disabled		58	95		58	95	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS843, SN54AS844 SN74AS843, SN74AS844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)		$VCC = 4.5$ $C_L = 50$ pF, R1 = 500 Ω , R2 = 500 Ω , $T_A = MIN$ to	, , o MAX		UNIT
			MIN	AS843 MAX	MIN	AS843 MAX	ĺ
tPLH			1	8.5	1	6.5	
t _{PHL}	D	a	1	10	1	9	ns
t _{PLH}	С	0	2	13	2	12	
^t PHL	C		2	13	2	12	ns
[†] PLH	PRE	Q	2	. 12	2	10	ns
tPHL	CLR	Q	2	14	2	13	ns
^t PZH	ŌC	Q	2	13.5	2	10.5	ns
[†] PZL		"	2	15	2	13.5	115
^t PHZ	ōc	a	1	10	1	8	ns
[†] PLZ		l	1	10	1	8	

'AS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to}$ $AS844$ MAX	MAX	AS844 MAX	UNIT
^t PLH	D	0	1	11	1	8.5	
^t PHL	J J	Q.	1	11	1	10	ns
^t PLH	С	0	2	14	2	12.5	
^t PHL		,	2	14	2	13	ns
^t PLH	PRE	Q	2	12	2	10	ns
^t PHL	CLR	. Q.	2	14.5	2	13.5	ns
tPZH	ŌC	a	2	14.5	2	. 12	ns
^t PZL	00		2	15	2	13.5	115
^t PHZ	oc	a	1	10	1	8	ns
^t PLZ			1	10	1	8	.113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983-REVISED APRIL 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus Driving Latches
 Necessary for Wider Address/Data Paths or
 Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting D inputs. Since CLR and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a busorganized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54ALS845, SN54AS845 . . . JT PACKAGE SN74ALS845, SN74AS845 . . . DW OR NT PACKAGE

(TOP VIEW) ōC1 ☐ī U24 VCC <u>oc</u>2 ∏2 23 OC 3 1 D \square 3 22 10 21 20 2D [20 30 4n Ē 19 1 40 18 50 5D 🗖 7 6D **∏**8 17 60 7D [16 70 8D 10 15 80 14 PRE CLR 11

SN54ALS845, SN54AS845 . . . FK PACKAGE SN74ALS845, SN74AS845 . . . FN PACKAGE

13 T C

GND 12

(TOP VIEW)



SN54ALS846, SN54AS846 . . . JT PACKAGE SN74ALS846, SN74AS846 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS846, SN54AS846 . . . FK PACKAGE SN74ALS846, SN74AS846 . . . FN PACKAGE (TOP VIEW)

> = 200 × 200 = ЗĐ 24 30 hб 40 40 NC 38 22 NC 5D ۱9 21 5Q Б₁₀ คกิ 60 7D 19 70

NC-No internal connection



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The -1 versions of the SN74ALS845 and SN74ALS846 parts are identical to the standard versions except that the recommended maximum IOL is increased to 48 milliamperes. There are no -1 versions of the SN54ALS845 and SN54ALS846.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'ALS845, 'AS845

			NPUT	INPUTS									
PRE	CLR	ŌC1	ŌC2	OC3	С	D	a						
L.	Н	L	L	L	Х	Х	Н						
Н	L	L	L	L	Х	Χ	L						
L	L	L	L	L	Х	X	н						
Н	Н	L	L	L	Н	L	L						
Н	Н	L	L	L	Н	Н	н						
Н	Н	L	L	L	L	Χ	α ₀						
Х	X	X	Х	Н	Χ	X	Z						
X	X	X	Н	X	Χ	X	z						
X	X	Н	Χ	×	Х	Х	z						

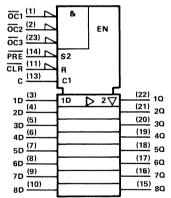
1				NPUTS	3			OUTPUT
	PRE	CLR	ŌC1	OC2	OC3	С	D	Q
1	L	Н	L	L	L	Х	Х	Н
ı	Н	L	L	L	L	X	X	L
	L	L	L.	L	L	X	Х	н
	Н	Н	L	L	L	Н	L	н
ı	Н	Н	L	L	L	Н	Н	L
1	Н	Н	L	L	L	L	Х	a_0
	X	X	Χ.	Χ	Н	Х	Х	z
I	Χ	X	Χ	Н	Χ	Х	Х	Z
	Х	Х	Н	Х	Х	Х	Х	Z

'ALS846, 'AS846

'ALS846, 'AS846

logic symbols†

'ALS845, 'AS845



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

OC1 (1) OC2 ΕN OC3 (23) r (14)PRE $(11)_{i}$ CLR $(13)_{1}$ (<u>22)</u> 1Q (3) 1D (4) (21)2D (5) (20) зĐ 30 (19)(6)4Q 4D (18) (7) 5D 5Ω (8) (17)6D 60 (16) (9) 70 7D

(15) 80

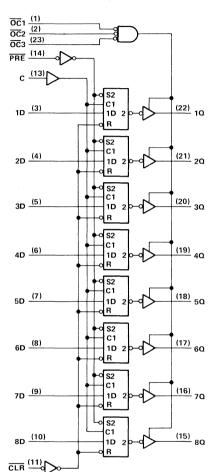
8D (10)



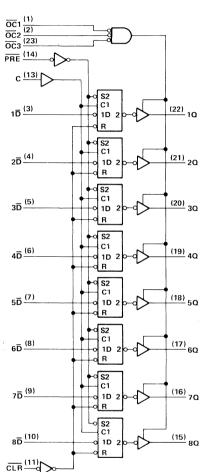
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

voltage, VCC	7 V
ltage	7 V
applied to a disabled 3-state output	5.5 V
ng free-air temperature range:	
54ALS845, SN54AS845, SN54ALS846, SN54AS846	-55°C to 125°C
74ALS845, SN74AS845, SN74ALS846, SN74AS846	-0°C to 70°C
temperature range	-65°C to 150°C



SN54ALS845, SN74ALS845 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN	154ALS	345	SN	174ALS	345	UNIT
1		,	MIN	NOM	MAX	MIN	NOM	MAX	ONIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
loL	Low-level output current				12			24	mA
'OL	Low-level output current							48 [†]	IIIA
١.	Pulse duration	CLR or PRE low	40			35			
t _w	ruise duration	C high	25			20			ns
t _{su}	Setup time, data before enable C↓		16			10			ns
t _h	Hold time, data after enable C↓		7			5			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS845-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONI	DITIONS	SN	54ALS	345	- SN	74ALS	345	UNIT
PANAMETER	TEST CON	DITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA	•		-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
Voн	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	$V_{CC} = 4.5 V,$	IòL = 24 mA					0.35	0.5	\ \
	(I _{OL} = 48 mA for -1 v	ersions)					0.55	0.5	
lozh	0.0	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL	$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μΑ
_	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1			0.1	mA
¹ IH	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
Iμ	$V_{CC} = 5.5 \text{ V}, .$	$V_I = 0.4 V$			-0.1			-0.1	mA
IO [§]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	- 30		-112	mA
		Outputs high		21	36		21	36	
Icc-	$V_{CC} = 5.5 V$	Outputs low		41	67		41	67	mA
	•	Outputs disabled		25	42		25	42	1

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS845, SN74ALS845 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	= 50 p = 500 = 500 = 25°	ο F , Ω, Ω, C	ONE	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R1 = 500$ $R2 = 500$ $T_A = MIN$ $4ALS845$	F, Ω, Ω, to MAX	V, ALS845	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	ł ł
tPLH	D	0		7	11	. 2	15	2	13	
t _{PHL}	U	σ,		11	15	4	20	4	18	ns
t _{PLH}	С	Q		12	18	5	25	5	21	ns
t _{PHL}	C	<u> </u>		16	23	8	30	8	26	115
^t PLH	PRE	Q		13	19	5	25	6	22	ns
tPHL	FNL	ď		19	26	4	35	6	30	ns
^t PLH	CLR	Q		19	26	4	35	6	30	ns
tPHL	CLIT	<u> </u>		16	22	6	. 28	6	24	ns
^t PZH	oc	Q		9	14	2	18	3	16	ns
tPZL	00	ď		12	17	4	20	5	18	115
^t PHZ	ōc	Q		4	9	1	12	1	11	ns
^t PLZ	- 50	Q .		6	11	2	14	2	12	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

			SN	54ALS	346	SN	74ALS	346	UNIT
	•		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
lou	Low-level output current				12			24	mA
lOL	Low-level output current							48†	""
	Pulse duration	CLR or PRE low	40			35			
tw	Pulse duration	C high	25			20			ns
t _{su}	Setup time, data before enable C↓		16			10			ns
th	Hold time, data after enable C↓		7			5		-	ns
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS846-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	154ALS	346	SN	74ALS	346	UNIT
PARAMETER	TEST CON	IDITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -	2.		
v _{oh} [$V_{CC} = 4.5 V,$		2.4	3.3					\ \
	$V_{CC} = 4.5 \text{ V},$					2.4	3,2]
	V _{CC} = 4.5 V,			0.25	0.4				
VOL	$V_{CC} = 4.5 V$	$I_{OL} = 24 \text{ mA}$					0.05	0.5	V
	$(I_{OL} = 48 \text{ mA for -1})$	versions)					0.35	0.5	
lozh	$V_{CC} = 5.5 V$				20			20	μΑ
IOZL	V _{CC} = 5.5 V,				- 20			- 20	μΑ
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
lін	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.1			-0.1	mA
10 [§]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 30		-112	-30		-112	mA
		Outputs high		22	36		22	36	
¹ cc	$V_{CC} = 5.5 V$	Outputs low		43	72		43	72	mA
		Outputs disabled		28	48		28	48	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. $^{\$}$ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS846, SN74ALS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	C = 5 = 500 = 500 = 25° ALS846	ο F , Ω, Ω, C		$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R1 = 500 $ $R2 = 500 $ $T_A = \text{MIN}$ 4ALS846	F, Ω, Ω, to MAX SN74/	ALS846	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	D	a		11	16	4	22	4	20	ns
^t PHL	_			9	13	3	17	3	15	
tPLH	С	Q		17	23	8	31	8	27	ns
^t PHL	Ü	١		14	19	6	26	6	22	,113
^t PLH	PRE	a		13	17	5	24	5	20	ns
tPHL	FNE	4		18	24	9	36	9	26	115
^t PLH	CLR	Q		14	19	6	23	6	21	n.
tPHL .	CLN	"		16	21	9	25	9	23	ns
^t PZH	<u>oc</u>	Q		10	13	3	17	3	15	
^t PZL		4		13	17	5	20	5	18	ns
^t PHZ	<u>oc</u>	Q		7	10	1	12	1	11	ns
^t PLZ		<u> </u>		7	11	2	14	2	12	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



			1	SN54AS845 SN54AS846		SN74AS845 SN74AS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
Іон	High-level output current				- 24			- 24	mA
loL	Low-level output current				32			48	mA
	Pulse duration	CLR or PRE low	5			4			
t _w	ruise duration	C high	5			4			ns
t _{su}	Setup time, data before enable C↓		3.5			2.5			ns
th	Hold time, data after enable C↓		3.5			2.5			ns
	Pagarana tima	PRE	17			15			
tr	Recovery time	CLR	16			14			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CO	ONDITIONS		N54AS8 N54AS8			N74AS8 N74AS8		UNIT
			•	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK	-	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 V$,	IOH = -2 mA	Vcc-	2		Vcc-	2		
V_{OH}		$V_{CC} = 4.5 \text{ V},$	IOH = -15 mA	2.4	3.2		2.4	3.2		1 v
		$V_{CC} = 4.5 \text{ V},$	IOH = -24 mA	2			2			1
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 32 mA		0.25	0.5				·v
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 48 mA				-	0.35	0.5	1 '
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ
lozL		$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 50			- 50	μΑ
l _l		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
ΊL		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
lo‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	-30		-112	mA
			Outputs high		35	58		-35	58	
	'AS845		Outputs low		52	85		52	85]
1	1	V _{CC} = 5.5 V	Outputs disabled		52	85	,	52	85	
lcc		VCC = 5.5 V	Outputs high		36	59		36	59	mA
	'AS846	,	Outputs low		53	,87		53	87	
			Outputs disabled		53	87		53	87	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS845, SN54AS846 SN74AS845, SN74AS846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ TO \\ (OUTPUT) \\ \end{array}$				V,	UNIT
	1			4AS845	SN74	AS845	
		<u> </u>	MIN	MAX	MIN	MAX	
^t PLH	D	a	1	8.5	1	6.5	ns
^t PHL	7]	1	10	1	9	115
^t PLH	С	Q	2	13	2	12	ns
^t PHL	1	<u> </u>	2	13	2	12	1 115
^t PLH	PRE	Q	2	12	2	10	ns
[†] PHL .	CLR	Q	2	14	2	13	ns
[†] PHL	ōc	Q	2	13.5	2	10.5	
tPZL ,	7	L u	2	15	2	13.5	ns
^t PHZ	ōc	0	1	10	1	8	ns
tPLZ	7 00	a	1	10	1	8] "

'AS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS846		SN74AS846		
			MIN	MAX	MIN	MAX	
^t PLH	D	Q	1	11	1	8.5	ns
tPHL			1	11	1	10	
^t PLH	C	Q	2	14	2	12.5	ns
^t PHL			2	14	2	13	
[†] PLH	PRE	a	2	12	2	10	ns
[†] PHL	CLR	Q	2	14.5	2	13.5	ns
t _{PHL}	oc	a	2	14.5	2	12	ns
tPZL			2	15	2	13.5	
^t PHZ	ōc	Q	1	10	1	8	ns
tPLZ			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS850, SN74AS851 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2822, DECEMBER 1983-REVISED JANUARY 1986

4-Line to 1-Line Data Selectors/Multiplexers
That Can Select 1 of 16 Data Inputs.
Typical Applications:

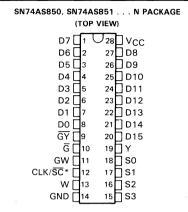
Boolean Function Generators Parallel-to-Serial Converters Data Source Selectors

- Cascadable to n-Bits
- 3-State Bus Driver Outputs
- 'AS850 Offers Clocked Selects; 'AS851 Offers Enable-Controlled Selects
- Has a Master Output Control (G) for Cascading and Individual Output Controls (GY, GW) for Each Output
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

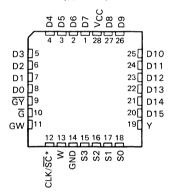
description

These four-line to one-line data selectors/multiplexers provide full binary decoding to select one-of-sixteen data sources with complementary Y and W outputs. The 'AS850 has a clock-controlled select register allowing for a symmetrical presentation of the select inputs to the decoder while the 'AS851 has an enable-controlled select register allowing the user to select and hold one particular data line.

A buffered group of output controls $(\overline{G}, \overline{GY}, GW)$ can be used to place the two-outputs in either a normal logic (high or low logic level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.



SN74AS850, SN74AS851 . . . FN PACKAGE
(TOP VIEW)



*CLK for 'AS850 or SC for 'AS851

The output controls do not affect the internal operations of the data selector/multiplexer. New data can be setup while the outputs are in the high-impedance state.

The SN74AS850 and SN74AS851 are characterized for operation from 0°C to 70°C.

SN74AS850, SN74AS851 1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

INPUT SELECTION TABLE

SI	ELECT	INPUT	ΓS	'AS850	'AS851	INPUT
S3	S2	S1	S0	CLK	SC	SELECTED
L	L	L	L	1	L	D0 .
L	L.	L	Н	1	L	, D1
L	L	Н	L	Ť	L	D2
L	L	Н	Н	1	L	D3
L	Н	L	L	1	L	D4
L	Н	L	Н	t	L	D5
L	Н	Н	L	1	L	D6
L	Н	Н	Н	Ť	L.	D7
Н	L	L	L	1	L	D8
Н	L	L	Н	1	L	D9
Н	L	Н	L	1	L	D10
Н	L	Н	Н	1	L	D11
Н	Н	L	L	1	L	D12
Н	Н	L	Н	î	L	D13
Н	Н	Н	L	1	L	D14
Н	Н	Н	Н	1	L	D15
Х	Х	Х	Х	H or L	Н	Dn

 $\mbox{Dn} = \mbox{the input selected before the most-recent low-to-high transition of CLK or $\overline{\mbox{SC}}$.}$

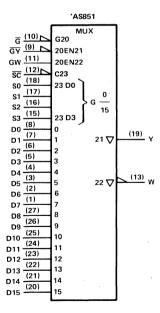
logic symbols†

[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

OUTPUT FUNCTION TABLE

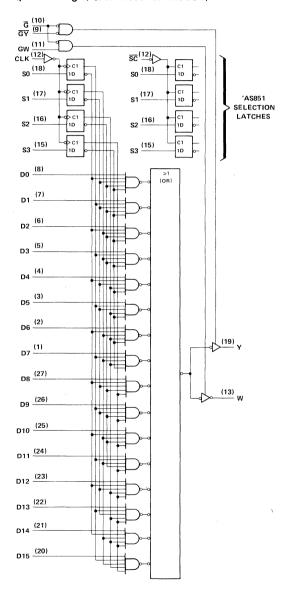
G	GΥ	GW	OU.	TPUTS
٥	GT	GW	Υ	w
Н	Χ	X	Z	Z
L	·H	L	Z	. Z
L	L	L.	D	Z [°]
L	Н	Н	Z	D
L	L	Н	D	ō

D = level of selected input D0-D15





'AS850 logic diagrams (positive logic) (see inset for 'AS851)



SN74AS850, SN74AS851 1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SN74AS850 recommended operating conditions

				MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4.5	5	5.5	V
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
ЮН	High-level output current					- 15	mA
loL	Low-level output current				48	mA	
f _{clock}	Clock frequency			0		60	MHz
	Bules duration	CLK hig	ı	8			ns
t _w	ruise duration	CLK lov		8		0.8 - 15 48] ""]
t _{su}	Pulse duration CLK high CLK low 8 Setup time, select inputs before CLK↑ 10						ns
th	Hold time, select inputs after CLK↑ 0			ns			
TA	Operating free-air tempera	iture		0		70	°C

SN74AS850 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITI	ONS	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
VOH	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} - 2			V
VOH	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$	2	3.3		1 °
V _{OL}	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA		0.35	0.5	V
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			50	μΑ
IOZL	$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 50	μΑ
l _i	$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1	mA
lн	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
D, G	V	V 04V			- 1	Ι
All others	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$				mA
10 [‡] ·	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	mA
1	V	Outputs active		50	81	
Icc	$V_{CC} = 5.5 V$	Outputs disabled		52	85	mA mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.



[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

SN74AS850 1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SN74AS850 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V _{CC} = 4.5 C _L = 50 pF R1 = 500 G R2 = 500 G T _A = 0°C	Ω, Ω,	UNIT
f _{max}		 	60	WAA	MHz
t _{PLH}			3	10.5	
t _{PHL}	Any D	Y	3	11	ns
[†] PLH			3	8	
t _{PHL}	Any D	W	1	6	ns
t _{PLH}	CLK		3	14.5	
^t PHL	CLK	Y	3	17.5	ns
^t PLH	CLK	w	3	15	
^t PHL	CLK	VV	3.5	13	ns
^t PZH	<u> </u>	Y	2	8	
^t PZL			3	11	ns
^t PHZ	<u>G</u>	Y	1	6	ns
^t PLZ		1	2	8	1115
^t PZH	G	w	2	8	ns
^t PZL	9	**	3	21	113
^t PHZ	\overline{G}	W	1	66	ns
tPLZ			2	8	113
^t PZH	GY	Y	2	8	ns
tPZL	<u> </u>	,	3	11	113
^t PHZ	GY	Υ	1	. 6	ns
^t PLZ	<u> </u>		2	8	
^t PZH	GW	W	2	10	ns
t _{PZL}			3	25	
^t PHZ	GW	. w	1	6	ns
tPLZ			2	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN74AS851 1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SN74AS851 recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
V _I L	Low-level input voltage			0.8	V
Іон	High-level output current			- 15	mA
loL	Low-level output current			48	mΑ
t _W	Pulse duration, SC low	10			ns
t _{su}	Setup time, select inputs before \overline{SC} 1	4.5			ns
th	Hold time, select inputs after SC↑	0			ns
TA	Operating free-air temperature	0		70	°C

SN74AS851 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2	С
1/		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			
VOH		$V_{CC} = 4.5 V,$	I _{OH} = -15 mA	2	3.3		1
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 48 mA		0.35	0.5	V
lozн		$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50	μA
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50	μΑ
lį		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1	mA
ΉΗ		$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20	μΑ
l	D, G	V EEV	V 0.4 V			- 1	mA
١١٢	All others	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.5] ""A
lo‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	mA
		V F F V	Outputs active		50	81] m^
lcc		$V_{CC} = 5.5 V$	Outputs disabled		52	85	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, Ios.

SN74AS851 1 OF 16 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SN74AS851 switching characteristics (see Note 1)

			V _{CC} = 4.5 C _L = 50 p	V to 5.5 V,	_	
	FROM	то	R1 = 500			
PARAMETER	(INPUT)	(OUTPUT)		$R2 = 500 \Omega,$		
	(iiii 01)	(001101)	TA = 0°C			
			MIN			
tPLH	A D	Y	3	10.5		
tPHL	Any D	Y	3	11	ns	
^t PLH	Any D	D W	3	8		
t _{PHL}	Any D	VV	1	6	ns	
tPLH	S0, S1, S2, S3	Y	3	18		
t _{PHL}	30, 51, 52, 53	'	3	19	ns	
^t PLH	S0, S1, S2, S3	w	3	16		
^t PHL	. 30, 31, 32, 33	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	3	15	ns	
^t PLH	<u>sc</u>	Y	3	18	ns	
^t PHL	36	'	3	20	113	
^t PLH	SC	W	3	16	ns	
^t PHL	36	1 **	3	15	113	
^t PZH	G	Y	2	8	ns	
^t PZL	9		3	11	1	
t _{PHZ}	G	Y	1	6	ns	
^t PLZ			2	8	1.13	
[†] PZH	G	W	2	8	ns	
^t PZL			3	21	1	
^t PHZ	G	W	1	6	ns	
^t PLZ	9	1	2	. 8	1.0	
^t PZH	Θ̈́Υ	Y	2	8	ns	
^t PZL	-	,	3	11		
^t PHZ	ĞΫ	Υ	1	6	ns	
tPLL			2	8		
^t PZH	GW	W	2	10	ns	
tPZL	3		3	25		
^t PHZ	GW	W	1	6	ns	
^t PLZ		<u> </u>	2	11		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The 'AS850 or 'AS851 can be used as a 1-of-16 Boolean function generator. Figure 1 shows the 'AS850 in one example.

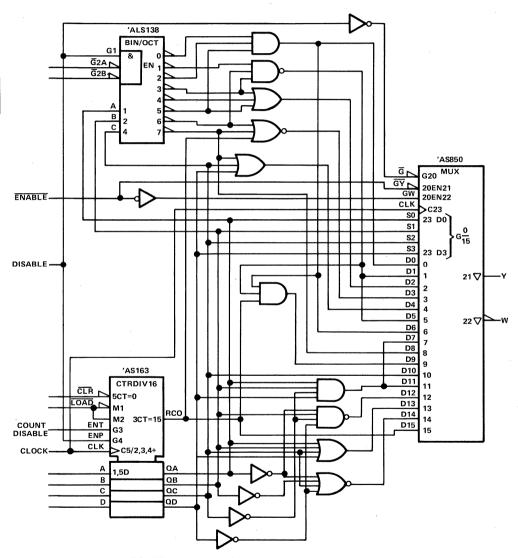


FIGURE 1. 1-of-16 BOOLEAN FUNCTION GENERATOR



TYPICAL APPLICATION DATA

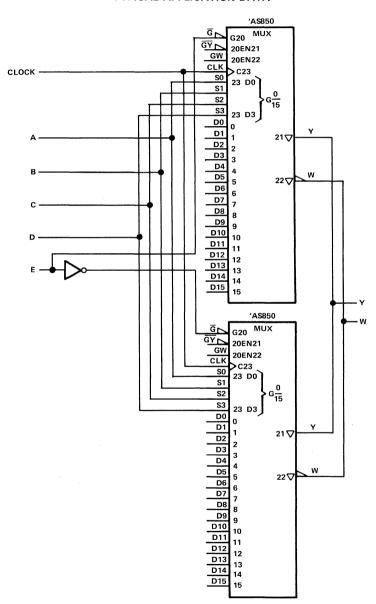
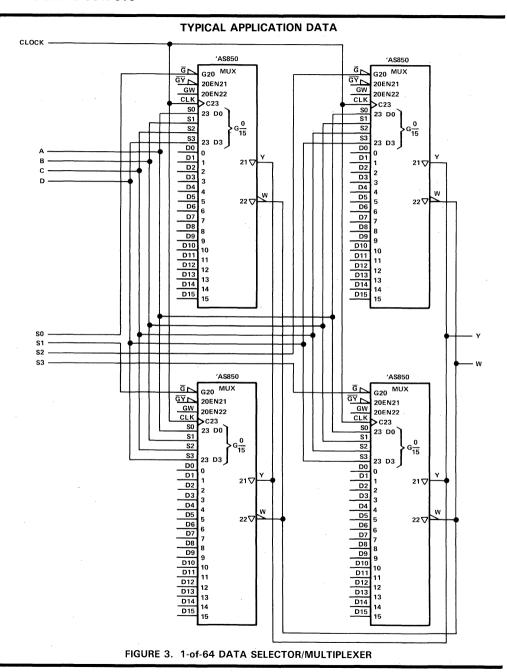


FIGURE 2. 1-of-32 DATA SELECTOR/MULTIPLEXER







SN54AS852, SN74AS852 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

D2810, JUNE 1984-REVISED JANUARY 1986

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:

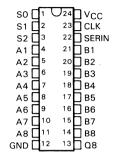
A to B or B to A
Register to A or B
Shifted to A from B or Shifted to
B from A
Off-Line Shifts (A and B Ports
Transceiving or in High-Impedance
State)
Register Clear

- Particularly Suitable for Use in Diagnostics Circuitry
- Serial Register Provides:
 - Parallel Storage of Either A or B Input Data
 - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

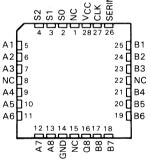
description

The 'AS852 features two 8-bit I/O ports (A1-A8 and B1-B8), and 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions

SN54AS852 . . . JT PACKAGE SN74AS852 . . . DW or NT PACKAGE (TOP VIEW)



SN54AS852 . . . FK PACKAGE SN74AS852 . . . FN PACKAGE (TOP VIEW)

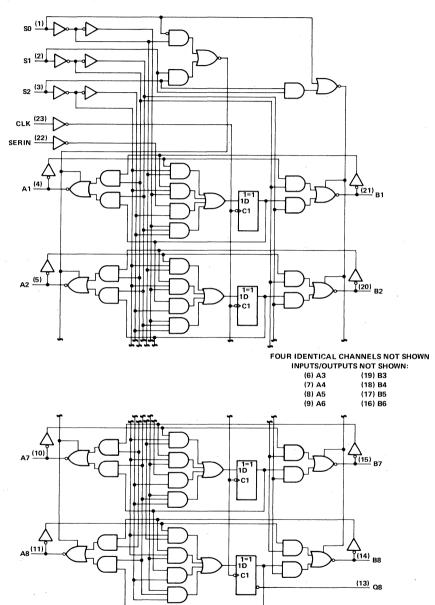


NC-No internal connection

include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port from the opposite port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. The 'AS852 can simultaneously transfer data from A to B or B to A and perform an off-line serial shift of data in the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS852 is ideally suited for applications implementing diagnostic circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS852 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS852 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



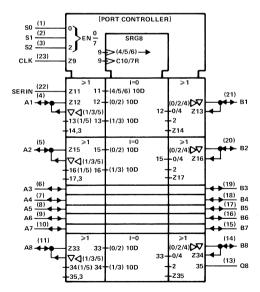
SN54AS852, SN74AS852 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

FUNCTION TABLE

MODE	01.004	05000	44.04.04	40.00.00	40.00.00	A 4 0 4 B 4	45 OF DE	40.00.00	47.07.07	A8 Q8 B8	PORT
S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 U3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A/U/B/	A8 U8 B8	FUNCTION
LLL	H or L	Х	Z Q _n A1	Z Q _n A2	Z Q _n A3	Z Q _n A4	Z Q _n A5	Z Q _n A6	Z Q _n A7	Z Q _n A8	А ТО В
LLL	1	×	Z A1 A1	Z A2 A2	A A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	A 10 B
LLH	H or L	Х	B1 Q _n Z	B2 Q _n Z	B3 Q _n Z	B4 Q _n Z	B5 Q _n Z	B6 Q _n Z	B7 Q _n Z	B8 Q _n Z	втоа
LLH	1	×	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	BIOA
LHL	H or L	Х	Χ Q _n Q1	X Q _n Q2	х a _n aз	X Q _n Q4	X Q _n Q5	Χ Q _n Q6	Χ Q _n Q7	х а _п ав	Q _N TO B _N
LHL	1	×	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	an 10 bn
LHH	H or L	Х	Q1 Q _n Χ	Q2 Q _n Χ	03 0 _n X	Q4 Q _n Χ	Q5 Q _n Χ	Q6 Q _n Χ	Q7 Q _n Χ	08 0 _n X	Q _N TO A _N
LHH	1	×	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	an 10 An
HLL	HorL	X	Z Q _n A1	Z Q _n A2	Z Q _n A3	Z Q _n A4	Z Q _n A5	Z Q _n A6	Z Q _n A7	Z Q _n A8	SHIFT
HLL	1	Н	Z H A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	AND
HLL	1	L	Z L A1	Z Q1 A2	Z Q2 A3	Z Q3 A4	Z Q4 A5	Z Q5 A6	Z Q6 A7	Z Q7 A8	А ТО В
HLH	H or L	×	B1 Q _n Z	B2 Q _n Z	B3 Q _n Z	B4 Q _n Z	B5 Q _n Z	B6 Q _n Z	B7 Q _n Z	B8 Q _n Z	SHIFT
HLH	↑	н	B1 H Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	AND
ньн	1	L	B1 L Z	B2 Q1 Z	B3 Q2 Z	B4 Q3 Z	B5 Q4 Z	B6 Q5 Z	B7 Q6 Z	B8 Q7 Z	B TO A
HHL	H or L	Х	z Q _n z	Z Q _n Z	z Q _n z	z Q _n z	z Q _n z	z Q _n z	Z Q _n Z	z Q _n z	
ннь	1	н	ZHZ	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT
ннь	1	L	ZLZ	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	z Q7 z	
ннн	H or L	Х	z Q _n z	ZQn	z o _n z	z α _n z	zα _n z	z o _n z	z Q _n z	z o _n z	CLEAR
ннн	1	х	ZLZ	ZLZ	Z L Z	ZLZ	ZLZ	ZLZ	ZLZ	Z L Z	CLEAR

 $n = level of Q_n(n = 1, 2, \dots 8)$ established on the most recent \uparrow transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



Supply voltage, VCC 7 V Input voltage: All inputs 7 V I/O ports 5.5 V Voltage applied to a disabled 3-state output 5.5 V Operating free-air temperature range: SN54AS852 -55°C to 125°C SN74AS852 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

			SI	V54AS8	52	SI	SN74AS852			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage		2			2			V	
VIL	Low-level input voltage			0.8			0.8	٧		
1	High-level output current	A1-A8, B1-B8			-12			- 15	mA	
ЮН	High-level output current	Q8			-2			-2		
	Law lavel autout auront	A1-A8, B1-B8			32			48	mA	
IOL	Low-level output current	Q8			20			20	MA	
fclock	Clock frequency		0		45	0		50	MHz	
t _w	Duration of clock pulse		11			10			ns	
	Satura tima bafasa CI KI	A1-A8, B1-B8, SERIN	5.5			5.5				
^t su	Setup time before CLK1	S0, S1, S2	5.5			5.5		, , , , , , , , , , , , , , , , , , , 	ns	
<u>.</u>	Hald sizes alone of a CLK1	A1-A8, B1-B8, SERIN	0			0				
th	Hold-time, data after CLK1	S0, S1, S2	0			0			ns	
TA	Operating free-air temperture		- 55		125	0		70	°C	



SN54AS852, SN74AS852 **8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CO	ONDITIONS	SI	V54AS8	52	SI	174AS8	52	UNIT
	AKAMETEN	1251 CC	MUTTONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	l₁ = −18 mA			-1.2			- 1.2	V
	A1-A8, B1-B8	$V_{CC} = 4.5 V$,	$l_{OH} = -12 \text{ mA}$	2.4	3.2					
Voн	711 710, 51 50	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2.4	3.3		V
	All outputs		5 V , $I_{OH} = -2 \text{ mA}$	Vcc-	2		vcc-	2		
	All outputs except Q8	$V_{CC} = 4.5 V$,	$I_{OL} = 32 \text{ mA}$		0.3	0.5				
VOL	All outputs except 40	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 48 \text{ mA}$					0.35	0.5	V
	Q8	$V_{CC} = 4.5 V$,	$I_{OL} = 20 \text{ mA}$		0.25	0.5		0.25	0.5	
	S0, S1, S2	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.3			0.3	
l _l	CLK and SERIN	VCC = 3.5 V,	V = / V			0.1	<u> </u>		0.1	mA
	A1-A8, B1-B8	$V_{CC} = 5.5 V,$	$V_{ } = 5.5 V$			0.2			0.2	
	S0, S1, S2					60			60	
Ιн	CLK and SERIN	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
	A1-A8, B1-B8 [‡]					70			70_	
	S0, S1, S2					- 1			- 1	
IIL.	CLK and SERIN	$V_{CC} = 5.5 V$,	$V_i = 0.4 V$			-0.5			-0.5	mA
<u></u>	A1-A8, B1-B8 [‡]					-0.5			-0.5	1
lo§	Except Q8	V 5 5 V	V= - 2.25 V	- 30		-112	- 30		-112	A
103	Q8	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 20		-112	- 20		-112	mA
Icc		V _{CC} = 5.5 V			136	220		136	220	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	R _L = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX SN54AS852 SN74AS852 MIN MAX MIN MAX			
f _{max}			45		50		MHz
tPLH	A A	A B 4	2	9	2	7.5	
^t PHL	Any A port	Any B port	3	12.5	3	11	ns
^t PLH	Any B port	Any A nest	2	9	2	7.5	
^t PHL	Ally B port	Any A port	3	12.5	3	11	ns
^t PLH	S0, S1, S2¶	Any A or B	3	11.5	3	10	
tPHL	50, 51, 521	port	3	12	3	10.5	ns
tPLH	CLK	Any A or B	2	11	2	9	
^t PHL	CLK	port	3	14	3	12.5	ns
^t PLH	CLK	Q8	2	10.5	2	8	
^t PHL	CLK	40	3	11.5	3	10	ns
^t PHZ			2	. 9	2	7	ns
^t PLZ	S0, S1, S2	Any A or B	3	13	3	10.5	IIIS
^t PZH	30, 31, 32	port	2	9	2	7	ns
^t PZL			3	13	3	10.5	l iis

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

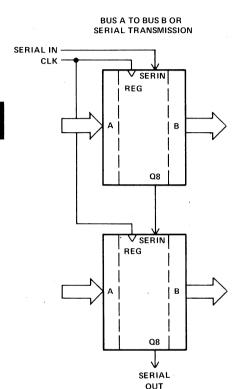
The positive transition of S1 control pin will cause low-level data on the A or B bus to be invalid for 17.5 ns.

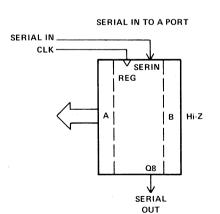


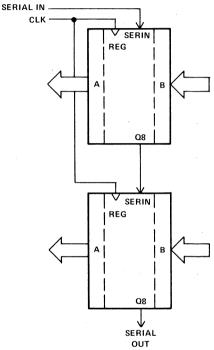
 $^{^{\}ddagger}$ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

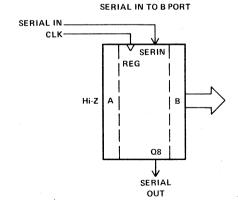
[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

TYPICAL APPLICATION DATA









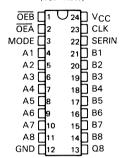


SN54AS856, SN74AS856 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

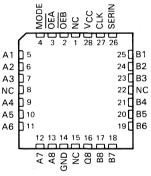
D2814, DECEMBER 1983-REVISED MARCH 1985

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
 - B to A
 - Register to A and/or B
 - Off-Line Shifts (A and B Ports in High-Impedance State)
 - Shifted to A and/or B
- Particularly Suitable for Use in Diagnostics Analysis Circuitry
- Serial Register Provides:
 - Parallel Storage of Either A or B Input Data
 - Serial Transmission of Data from Either
 A or B Port
 - Readback Mode B to A
- Dependable Texas Instruments Quality and Reliability

SN54AS856 . . . JT PACKAGE SN74AS856 . . . DW or NT PACKAGE (TOP VIEW)



SN54AS856 . . . FK PACKAGE SN74AS856 . . . FN PACKAGE (TOP VIEW)



NC - No internal connection

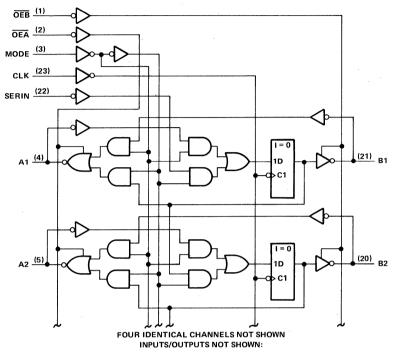
description

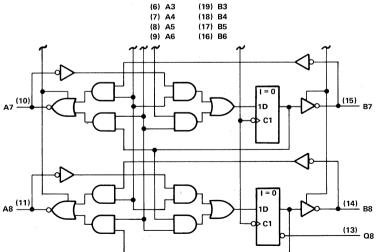
The 'AS856 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three control lines OEA, OEB, and MODE. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), serial shifting data to either or both ports, and performing off-line shifts (with A and B ports active as transceivers in a high-impedance state). Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS856 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS856 is characterized for operation over the full military temperaure range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS856 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.



logic diagram (positive logic)





Pin numbers shown are for DW, JT, and NT packages.



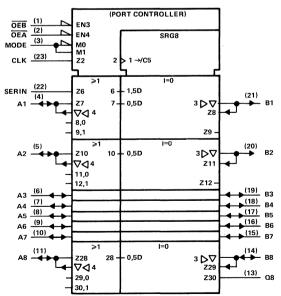
SN54AS856, SN74AS856 **8 BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS**

FUNCTION TABLE

	MODE		01 001	CEDIN	44 04 84	40.00.00	42.02.02	44.04.04	45.05.05	46.00.00	47.07.07	40.00.00	FUNCTION
MODE	ŌEĀ	OEB	CLOCK	SERIN	ATUTET	A2 U2 B2	A3 U3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A/U/B/	A8 Q8 B8	FUNCTION
L	L	L	H or L	Х	Q1 Q1 Q1	Q2 Q2 Q2	Q3 Q3 Q3	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	08 Q8 Q8	FEEDBACK
L	L	L	1	х	Q1 Q1 Q1	Q2 Q2 Q2	O3 O3 O3	Q4 Q4 Q4	Q5 Q5 Q5	G 6 G 6 G 6	Q7 Q7 Q7	Q8 Q8 Q8	PEEDBACK
L	L	Н	H or L	Х	B1 Q1 Z	B2 Q2 Z	B3 Q3 Z	B4 Q4 Z	B5 Q5 Z	B6 Q6 Z	B7 Q7 Z	B8 Q8 Z	B to A
L	L	н	1	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	A to Q
L	н	L	H or L	Х	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	Z Q8 Q8	A to Q
L	н	L	1	Х	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	Q to B
L	Н	н	H or L	X	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	Z Q8 Z	A to Ω
L	Н	н	1	Х	Z A1 Z	Z A2 Z	Z A3 Z	Z A4 Z	Z A5 Z	Z A6 Z	Z A7 Z	Z A8 Z	Atou
Н	L	L	H or L	Х	Q1 Q _n Q1	Q2 Q _n Q2	03 0 _n 03	Q4 Q _n Q4	Q5 Q _n Q5	Q6 Q _n Q6	07 Q _n Q7	Q8 Q _n Q8	SHIFT
Н	L	L	1	н	ннн	Q1 Q1 Q1	Q2 Q2 Q2	03 03 03	Q4 Q4 Q4	Q5 Q5 Q5	Q6 Q6 Q6	Q7 Q7 Q7	то
н	L	L	1	L	LLL	Q1 Q1 Q1	Q2 Q2 Q2	O3 O3 O3	Q4 Q4 Q4	Q5 Q5 Q5	GE GE GE	Q7 Q7 Q7	A and B
н	L	Н	H or L	Х	Q1 Q _n Z	Q2 Q _n Z	Q3 Q _n Z	Q4 Q _n Z	Ω5 Q _n Z	Q6 Q _n Z	Q7 Q _n Z	Q8 Q _n Z	SHIFT
н	L	н	1	н	ннг	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	то
Н	L	н	1	L	LLZ	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	Α
Н	н	L	H or L	Х	Z Q _n Q1	Z Q _n Q2	Z Q _n Q3	Z Q _n Q4	Z Q _n Q5	Z Q _n Q6	z Q _n Q7	Z Q _n Q8	SHIFT
Н	н	L	1	н	z н н	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	то
Н	Н	L	1	L	ZLL	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	В
Н	Н	Н	HorL	Х	z Q _n z	z a _n z	z Q _{n Z}	z Q _n z	z o _n z	z o _n z	z Q _n z	z Q _n z	011157
н	Н	н	1	н	ZHZ	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT
н	н	н	î	L	ZLH	Z Q1 Z	Z Q2 Z	z 03 z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	

n = level of Q_n(n = 1, 2 . . . 8) established on most recent ↑ transition of CLK. Q1 through Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

logic symbol†



Pin numbers shown are for DW, JT, and NT packages.

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



absolute maximum ratings over free-air temperature range 7 V Supply voltage, VCC 7 V Input voltage: All inputs 7 V I/O ports 5.5 V Voltage applied to a disabled 3-state output 5.5 V Operating free-air temperature range: SN54AS856 -55°C to 125°C SN74AS856 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

			SI	V54AS8	56	SI	SN74AS856		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	High-level input voltage				2			V
VIL	Low-level input voltage				0.8			0.8	V
1	High lavel autout august	A1-A8, B1-B8			-12			- 15	mA
Іон	High-level output current	Ω8			- 2			- 2	""A
1	OL Low-level output current	A1-A8, B1-B8			32			48	mA
IOL		Q8			20			20	1 mA
fclock	Clock frequency		0		45	0		50	MHz
t _w	Duration of clock pulse		11			10			ns
	Setup time before CLK↑	A1-A8, B1-B8 SERIN .	5.5			5.5			
t _{su}	Setup time before CEK	OEB, OEA, MODE	5.5			5.5			ns
	Hald sime a data after CLKA	A1-A8, B1-B8 SERIN	0			0			
th	Hold-time, data after CLK↑	OEB, OEA, MODE	0			0			ns
TA	Operating free-air temperature		-55		125	0		70	°C

SN54AS856, SN74AS856 **8 BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST COND	TIONE	SI	N54AS8	56	SN	74AS8	56	UNIT
P	ARAMETER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			- 1.2	V
	A1-A8	$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2	3.2					
∨он	B1-B8	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2	3.3		V
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
	All outputs except Q8	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 32 \text{ mA}$		0.25	0.5				
VOL	All outputs except Qo	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 48 \text{ mA}$					0.35	0.5	V
	Q8	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 20 \text{ mA}$			0.5			0.5	
	OEB, OEA, MODE	$V_{CC} = 5.5 V_{c}$	V 7 V			0.2			0.2	
l,	CLK and SERIN	vCC = 5.5,v,	V = 7 V			0.1			0.1	mA
	A1-A8, B1-B8	$V_{CC} = 5.5 V$,	$V_{ } = 5.5 V$			0.2			0.2	
	OEB, OEA, MODE					40			40	
ЧН	CLK and SERIN	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
	A1-A8, B1-B8 [‡]					70			70	
	OEB, OEA, MODE					- 1			- 1	
l _{IL}	CLK and SERIN	$V_{CC} = 5.5 V$	$V_l = 0.4 V$			-0.5			-0.5	mA
	A1-A8, B1-B8 [‡]					-0.5			-0.5	
lo§	Except Q8	V FEV	\/- 2.2E.\/	- 30		-112	- 30		-112	mA
103	Ω8	$V_{CC} = 5.5 V$,	$v_0 = 2.25 \text{ V}$	- 20		-112	- 20		-112	mA
Icc		$V_{CC} = 5.5 V$			118	200		118	200	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $SN54AS856 \qquad SN74AS856$			
f _{max}			45	MAX	MIN 50	MAX	MHz
tPLH			2	8	2	7	
tPHL	Any B port	Any A port	2	10.5	2	9.5	ns
^t PLH		Any A or B	2	8.5	2	7.5	
t _{PHL}	↑MODE¶	port	5	20	5	19	ns
^t PLH	IMODE	Any A or B	2	8.5	2	7.5	
[†] PHL	→ ↓MODE	port	2	9.5	. 2	8	ns
tPLH	CLK	Any A or B	3	12	3	9	ns
^t PHL	- CLK	port	3	12	3	11	115
^t PLH	CLK	Q8	2	9	2	7.5	ns
^t PHL	CER		2	10	2	9	113
^t PHZ			2	9	2	7	ns
[†] PLZ	OEA or OEB	Any A or B	2	12	2	9.5	
^t PZH	J SEA SI GEB	port	2	8	2	7	ns
tPZL			2	11	2	10	,,,,

The positive transition of the MODE control will cause low-level data at the A output Bus or stored in Q to be invalid for 12 ns. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS857, SN54AS857, SN74ALS857, SN74AS857 HEX 2-TO-1 UNIVERSAL MULTIPLEXERS

D2661, DECEMBER 1982 - REVISED MAY 1986

- Selects True or Complementary Data
- Performs AND/NAND (masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detects Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'ALS857 and 'AS857 are hextuple 2-line to 1-line multiplexers with three-state outputs. The devices can provide either true (COMP low) or inverted (COMP high) data at the Y outputs. In addition, the 'ALS857 and 'AS857 perform the logical AND function (A-B) and the clear function as well. The four modes of operation are:

Select A data inputs, Select B data inputs, AND A inputs with B inputs, Clear

In either of the first two modes, OPER = 0 is high if all the selected A or B inputs are low.

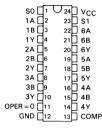
The six Y outputs and the OPER = 0 output are all three-state and rated at 12 mA and 24 mA \mid_{OL} for the SN54ALS857 and SN74ALS857, respectively, and at 32 mA and 48 mA \mid_{OL} for the SN54AS857 and SN74AS857, respectively. All outputs can be placed into the high-impedance state by applying a high level to the COMP, SO, and S1 inputs simultaneously. The complete function table is shown below.

The SN54ALS857 and SN54AS857 are characterized for operation over the full military temperature range of $-55\,^{\rm o}C$ to 125 °C. The SN74ALS857 and SN74AS857 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

COMP	S1	S0	Y OUTPUTS	OPER = ZERO
L	L	L	Α	H = all A inputs L
L	L	Н	В	H = all B inputs L
L	н	L	A·B	Z
L	н	н	L	· L
н	L	L	Ā	H = all A inputs L
н	L	Н	B	H = all B inputs L
н	Н	L	Ā·B	Z
Н	Н	н	z	Z

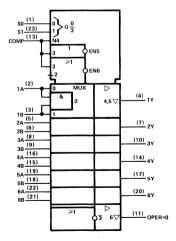
SN54ALS857, SN54AS857 . . . JT PACKAGE SN74ALS857, SN74AS857 . . . DW OR NT PACKAGE (TOP VIEW)



SN54ALS857, SN54AS857 . . . FK PACKAGE SN74ALS857, SN74AS857 . . . FN PACKAGE

> For chip carrier information contact factory

logic symbol[†]



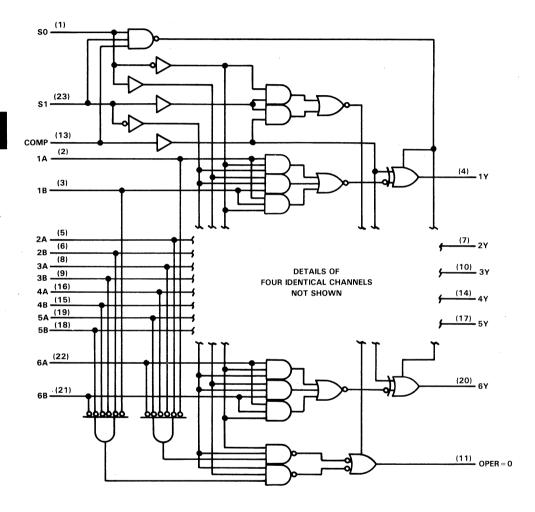
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

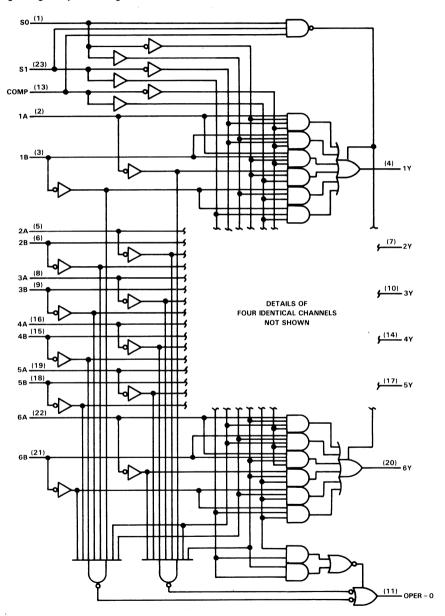


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'ALS857 logic diagram (positive logic)



'AS857 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS857 – 55 °C to 125 °C
SN74ALS857
Storage temperature range

recommended operating conditions

		S	N54ALS	B57	SN	74ALS8	57	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ІОН	High-level output current			- 1			-2.6	mA
^I OL	Low-level output current			12			- 24	mA
TΔ	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	S	N54ALS	857	SN	74ALS	357	LINUT
PARAMETER	1551 C	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	5 V , $1_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		
Voн	$V_{CC} = 4.5 V$,	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		}
Vai	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5]
lozн	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
^I OZL	$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 20			- 20	μΑ
lı .	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
ΊL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
lo [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 15		- 70	- 15		- 70	mA
	Vcc = 5.5 V,	Outputs high		11	24		11	24	
lcc	See Note 1	Outputs low		16	33		16	33	mA
	See Note 1	Outputs disabled		18	36		18	36	l

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 $^{\bar{o}}$ C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

SN54ALS857, SN74ALS857 HEX 2-TO-1 UNIVERSAL MULTIPLEXERS

switching characterisitcs (see Note 1)

PARAMETER	FROM (INPUT)	(INPUT) (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_{L} = 50 \text{ pF,}$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $SN54ALS857 \qquad SN74ALS857$					
	A or B	Y	MIN	MAX	MIN	MAX			
t _{pd}	(COMP high)	(Inverting)	4	28	4	25	ns		
^t pd	A or B (COMP low)	Y (Noninverting)	4	21	4	18	ns		
t _{pd}	S0 or S1	Y	7	37	7	33			
t _{pd}	COMP	Y	6	22	6	18	ns		
^t pd	A or B	OPER = 0	5	45	5	. 37	115		
t _{pd}	S0 or S1	OPER = 0	5	30	5	23			
t _{en}	S0 or S1	Y	7	38	7	35	ns		
^t dis	30 01 31	'	2	29	2	23	113		
t _{en}	COMP	Y	8	27	8	24	ns		
^t dis	COM	· · · · · · · · · · · · · · · · · · ·	6	27	6	21	113		
t _{en}	so	OPER = 0	6	24	6	20	ns		
t _{dis}	30	0. 2.11 = 0	11	34	11	27	,113		
t _{en}	S1	OPER = 0	6	28	6	25	ns		
^t dis	٠,	01 211 - 0	3	23	3	19			
t _{en}	COMP	OPER = 0	9	30	9	25	ns		
^t dis	JOWN .	5, 2,1 = 0	6	24	6	20	3		

 $t_{pd} = t_{PLH} \text{ or } t_{PHL}$

 $t_{en} = t_{PZH} \text{ or } t_{PZL}$

 $t_{dis} = t_{PHZ} \text{ or } t_{PLZ}$

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54AS857
SN74AS857
Storage temperature range

recommended operating conditions

			SI	N54AS8	57	,	SN74AS	857	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
1	High level output ouwant	Y Outputs			-12			- 15	
ЮН	High-level output current	OPER = 0			- 2			-2	mA
1	I am family and a second	Y Outputs	.		32			48	
IOL	Low-level output current	OPER = 0			20			20	mA
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ARAMETER	TEST CONDITIO	N.C	S	SN54AS857 SN74AS857				57	LIBUT
Р	AKAMETEK	TEST CONDITIO	INS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
Vικ		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	Y Outputs	$V_{CC} = 4.5 V,$	IOH = -12 mA	2.4	3.2					
۷он	1 Outputs	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2.4	3.3		V
	All Outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2		
	Y Outputs	$V_{CC} = 4.5 V,$	$I_{OL} = 32 \text{ mA}$		0.35	0.5				
Vol	1 Outputs	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5	V
	OPER = 0	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.25	0.5		0.25	0.5	
lozh		$V_{CC} = 5.5 V,$	$I_{OL} = 2.7 V$			50			50	μΑ
lozL		$V_{CC} = 5.5 \text{ V},$	$V_0 = 0.4 V$			- 50			- 50	μΑ
Ιį		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
Ιн		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
Ŀ		$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 2			- 2	mA
lo‡		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 150	- 50		- 150	mA
		V _{CC} = 5.5 V,	Outputs high		97	140		97	140	
1cc		See Note 1	Outputs low		127	175		127	175	mA
		Jee Note 1	Outputs disabled		92	135		92	135	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CC} is measured with all possible inputs grounded while achieving the stated output conditions.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)				$V_{CC} = 4.5 \text{ V, to } 5.5 \text{ V,}$ $C_{L} = 50 \text{ pF,}$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $\text{SN54AS857} \qquad \text{SN74AS857}$					
			MIN			MIN MAX				
^t pd	A or B (COMP high)	Y (Inverting)	2	15	2	12	ns			
^t pd	A or B (COMP low)	Y (Noninverting)	2	12	2	10	ns			
t _{pd} .	S0 or S1	Y	2	15	2	13				
^t pd	COMP	Y	2	15	2	13	ns			
^t pd	A or B	OPER = 0	2	16	2	14	115			
^t pd	S0 to S1	OPER = 0	2	20	2	18				
t _{en}	S0 to S1	Y	2	14	2	12	ns			
^t dis	30 10 01	'	2	13	2	11	113			
t _{en}	COMP	Y	2	14	2	12	ns			
^t dis	COM	'	2	10	2	9	115			
^t en	S0	OPER = 0	2	14	2	12	ns			
^t dis	90	OI LIT = 0	2	10	2	9	113			
t _{en}	S1	OPER = 0	2	14	2	12	ns			
^t dis		0.211 - 0	2	10	2	9	113			
t _{en}	COMP	OPER = 0	2	15	2	13	ns			
^t dis	351111	0.211 - 0	2	10	2	9	113			

 $t_{pd} = t_{PLH} \text{ or } t_{PHL}$

ten = tpzH or tpAL

tdis = tpHZ or tpLZ

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.

SN54AS866, SN74AS866 8-BIT MAGNITUDE COMPARATORS

D2661, DECEMBER 1982-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Input and Output Latches with Active-High Enables
- Fast Compare to Zero
- Arithmetic and Logical Comparison
- Open-Collector P = Q Output
- Dependable Texas Instruments Quality and Reliability

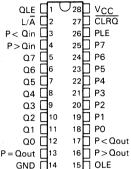
description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P>Q and P<Q outputs of each stage to the P>Q and P<Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The open-collector P=Q output may be wire-ANDed together.

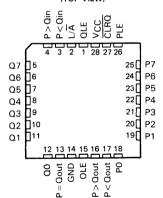
Both input words P and Q plus all three outputs (P>Q, P<Q, and P=Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or QLE is high.

The enable inputs PLE and QLE and data inputs P and Q utilize p-n-p input transistors to reduce the low-level input current requirement to typically -0.25 mA, which minimizes loading effects.

SN54AS866 . . . JD PACKAGE SN74AS866 . . . N PACKAGE (TOP VIEW)



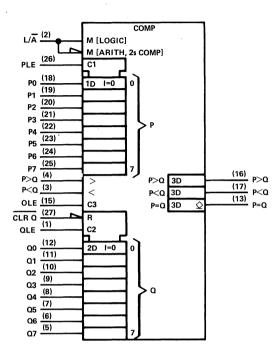
SN54AS866 . . . FK PACKAGE SN74AS866 . . . FN PACKAGE (TOP VIEW)



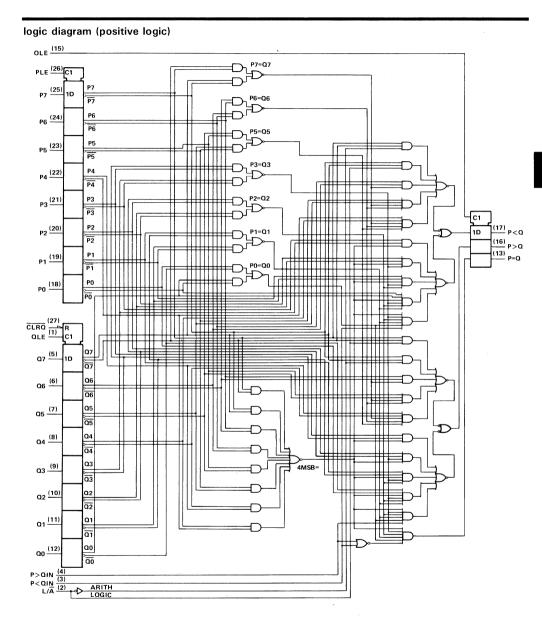
The Q register may be cleared to zero for a fast comparison of the P word to zero.

The SN54AS866 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS866 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

logic symbol†



 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



FUNCTION TABLE

COMPARISON	L/Ā	DATA INPUTS INPUTS		UTS		OUTPUTS		
COMPARISON	L/A	ΡΟ-Ρ7, QΟ-Q7	P > Q	P < Q	P > Q	P < Q	P=Q	
Logical	н	P > Q	Х	Х	Н	L	L	
Logical	Н	P < Q	x	Х	L	Н	L	
Logical	Н	P=Q	L	L	L	L	Н	
Logical	Н	P=Q	L	Н	L	Н	L	
Logical	Н	P=Q	Н	L	Н	L	L	
Logical	Н	P=Q	Н	Н .	Н	Н	L	
Arithmetic	L	P AG Q	х	Х	Н	L	L	
Arithmetic	L	Q AG P	Х	Х	L	Н	L	
Arithmetic	L	P=Q	L	L	L	L	Н	
Arithmetic	L	P=Q	L	Н	L	Н	L	
Arithmetic	L	P=Q	Н	L	Н	L	L	
Arithmetic	L	P=Q	Н	Н	Н	Н	L	

AG = arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Off-state output voltage, P=Q output
Operating free-air temperature range: SN54AS866
SN74AS866
Storage temperature range65°C to 150°C

recommended operating conditions

	DADAMETED	SN54AS866			SN			
	PARAMETER	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
ПОН	High-level output current, all outputs except P = Q			-2			-2	mA
Voн	High-level output voltage, $P = Q$ output			5.5			5.5	V
OL	Low-level output current			20			20	mA
t _{su}	Setup time to PLE, QLE, OLE	2			.2			
th	Hold time after PLE, QLE, OLE↓	4			4			ns
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

В	ARAMETER	TEST CO	ONDITIONS	SN	SN54AS866 SN74AS866			6		
	ANAIVIETEN	1231 00	MUITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.2			-1.2	V
Voн	P > Q, P < Q	$V_{CC} = 4.5 \text{ V to } 5.5$	5 V , $1_{OH} = -2 \text{ mA}$	V _{CC}	2		Vcc-	2		
loн	P = Q only	$V_{CC} = 4.5 \text{ V},$	V _{OH} = 5.5 V	T		0.25			0.25	mA
VOL		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 20 \text{ mA}$		0.35	0.5		0.35	0.5	V
lγ		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lu.	L/Ā, OLE	V _{CC} = 5.5 V,	V _I = 2.7 V	7	,	40			40	^
lін	Others					20			20	μΑ
	L/Ã, OLE,									
	P > Qin,					-4	,		- 4	
1/L	P < Qin	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$				1			mA
	CLRQ					- 2			- 2	
	P, Q, PLE, QLE				-0.25	- 1		-0.25	- 1	
10‡		$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	- 20		-112	- 20		- 112	mA
1cc		V _{CC} = 5.5 V,	See Note 1		160	240		160	240	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$						
Į.		SN54AS866 SN74AS				N74AS	866	1	
			MIN	TYP [†]	MAX	MIN	TYP	MAX	ı
tPLH	L/Ā		1	8.5	14	1	8.5	13	ns
^t PHL	L/A		1	7.5	14	1	7.5	13	1 115
[†] PLH	P < Q,	1	1	5	10	1	5	8	
^t PHL	P > Q	P < Q,	1	5.5	10	1	5.5	8	ns
^t PLH	Any P or Q	P > Q	1	13.5	21	1	13.5	17.5	
^t PHL	Data Input		1	10	17	1	10	15	ns
^t PLH	CLRQ	1	1	16	21	1	16	20	
tPHL	CLHO		1	12	17	1	12	16	ns

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L	= 4.5 = 50 pF = 280 Ω = MIN t	, 2,			UNIT
			SN54AS866		AS866 SN74AS866				
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX]
^t PLH	P < Q,	P = Q	1	6.5	12	1	6.5	11	200
tPHL	P > Q	F = Q	1	8	14	1	8	13	ns
^t PLH	Any P or Q	P = Q	1	10	15	1	10	14	ns
tPHL	Data Input	1 - 4	1	9	14	1	9	13	113
^t PLH	CLRQ	P = Q	1	12	17	1	12	16	ns
tPHL	CENG	J U	1	13	18	1	13	17	""

†All typical values are at $V_{CC}=5$ V, $T_{A}=25$ °C. NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[†]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, IOS. NOTE 1: ICC is measured with all inputs high except L/A, which is low.

TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the $\overline{\text{CLRQ}}$ function can be used to perform dual comparisons of the varying P terms (P0, P1, etc.). When $\overline{\text{CLRQ}}$ is high, the P term is compared to the Q term. When $\overline{\text{CLRQ}}$ is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

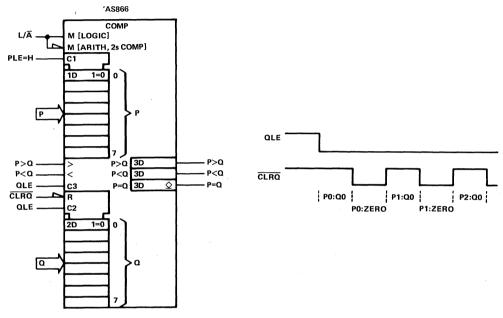


FIGURE 1. MAGNITUDE COMPARISONS COMBINED WITH QUICK COMPARISONS TO ZERO (RANGE VERIFICATIONS)

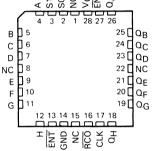
SN54ALS867, SN54AS867, SN54ALS869, SN54AS869 SN74ALS867, SN74AS867, SN74ALS869, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

D2661, DECEMBER 1982 - REVISED MAY 1986

IT DAOKAOE

- Fully Programmable with Synchronous Counting and Loading
- '867 Has Asynchronous Clear, '869 Has Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Ripple Carry Output for n-Bit Cascading
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54' JT PACKAGE
SN74' DW OR NT PACKAGE
(TOP VIEW)
SO 1 024 VCC S1 2 23 ENP A 3 22 QA B 4 21 QB C 5 20 QC D 6 19 QC E 7 18 QF G 9 16 QG H 10 15 QH ENT 11 14 CLK
GND 12 13 RCO
SN54' FK PACKAGE (TOP VIEW)
A 50 0 2 7 26 QB
n



NC-No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs (ENP and ENT) must be low to count. The direction of the count is determined by the levels of the select inputs (see Function Table). Input ENT is fed forward to enable the carry output. The ripple carry output thus enabled will produce a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable ENP and ENT inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

The SN54ALS' and SN54AS' families are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS' and SN74AS' families are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

logic symbols†

ALS and AS Circuits

'ALS, 'AS869 'ALS, 'AS867 CTRDIV 256 CTRDIV 256 (1)(1) SO so (2) (2) S1. S1 (13) RCO (13) RCO 1,4,5CT = 01,4,5CT = 0ENT (11) ENT_(11) G4 G4 3,4,5CT = 2553,4,5CT = 255ENP_(23) (23) G5 ENP. G5 (14) (14)CLK. C6/1,4,5-/3,4,5+ CLK. C6/1,4,5-/3,4,5+ 0R 0.6R (22) QA (<u>22)</u> QA (3) (3)2.6D Α 2 6D (21) QB (21) QB (4)(4) (20) OC (20) QC (5) (5) (19) QD (19) QD (6) (6) (7) (18) QE (18) QE (7)(8) (17) QF (8) (17) QF (16) QG (16) QG (9) (9) (15) OH (15) QH (10)(10)

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

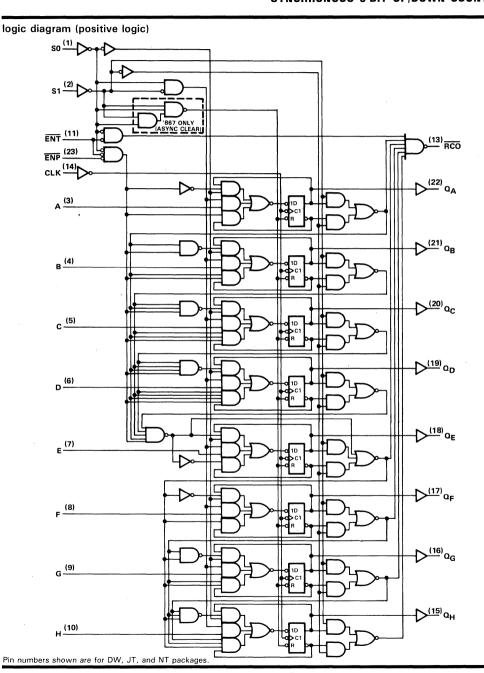
FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	Н	Count down
Н	L	Load
Н	Н	Count up

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _C C
Input voltage
Operating free-air temperature range: SN54ALS', SN54AS' 55°C to 125°C
SN74ALS', SN74AS'
Storage temperature range - 65°C to 150°C







recommended operating conditions

			SN	154ALS	367	SN	74ALS	867	UNIT
			MIN	МОИ	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				-0.4			-0.4	mA
lOL	Low-level output current				8.0			8.0	mA
fclock	Clock frequency		0		45	0		45	MHz
tw(clock)	Duration								ns
tw(clear)	Duration of clear pulse (SO and	S1 low)							ns
		Data inputs A-H							ns
		Enable P (ENP) or							ns
		Enable T (ENT)	1						10
t _{su}	Setup time [†]	S0 or S1 (load)	J						ns
٠		S0 or S1 (clear)					,		ns
		S0 or S1 (count down)]						ns
		S0 or S1 (count up)	1						ns
t _h	Hold time at any input with res	pect to clock [†]				,			ns
+ .	Skew time between S0 and S1	(maximum to							ns
t _{skew}	avoid inadvertent clear)								118
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	RAMETER	TEST CO	NDITIONS	SN	154ALS	367	SN	74ALS8	867	UNIT
FA	NAMETER	TEST CO	NUTTIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			. – 1.5			- 1.5	V
Voн		$V_{CC} = 4.5 \text{ V to 5}$	$.5 \text{ V}, l_{OH} = '-0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			V
1/		$V_{CC} = 4.5 V,$	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
V_{OL}		$V_{CC} = 4.5 V$,	IOL = 8 mA					0.35	0.5	v
lį		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
1	ENT		V ₁ = 2.7 V	Ī .		40			40	
ΉΗ	Other Inputs	$V_{CC} = 5.5 V$,	V = 2.7 V			20			20	μΑ
	ENT					-0.4			-0.4	
ΊL	Other inputs	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.2			-0.2	mA
, 10 [§]		$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	- 30		- 112	- 30		- 112	mA
lcc		$V_{CC} = 5.5 V$,			28.5			28.5		mA

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS869, SN74ALS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS WITH SYNCHRONOUS CLEAR

recommended operating conditions

			SN	54ALS	369	SI	74ALS	369	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
IOH	High-level output current				- 2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency				40			45	MHz
tw(clock)	Duration					-			ns
		Data inputs A-H							ns
		Enable P (ENP) or							
		Enable T (ENT)							ns
t _{su}	Setup time [†]	S0 or S1 (load)							ns
		S0 or S1 (clear)							ns
		S0 or S1 (count down)	1						ns
		S0 or S1 (count up)							ns
th	Hold time at any input with res	pect to clock1							ns
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	RAMETER	TEST COL	NDITIONS	SN	154ALS	369	SN	74ALS8	869	UNIT
FAI	MAINETER	TEST CO	NDITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
Vон		$V_{CC} = 4.5 \text{ V to 5}$	$.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2			V _{CC} -2			V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
\ VOL		V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	v
η		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
1	ENT	.V EEV	V _I = 2.7 V			40			40	^
ЧН	Other Inputs	$V_{CC} = 5.5 \text{ V},$	V = 2.7 V			20			20	μΑ
	ENT	\/ F.F.\/	.,			-0.4			-0.4	
.lţL	Other inputs	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.2			-0.2	mA
IO [§]		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		-112	mA
Icc		$V_{CC} = 5.5 V,$			28.5			28.5		mA

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

'ALS867 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 500 R _L = 500 T _A = MIN SN54ALS867), to MAX SN74ALS867	UNIT
f _{max}			MIN TYP [†] MAX	MIN TYP [†] MAX	MHz
tPLH		<u> </u>	14	14	141112
tPHL	CLK	RCO	13	13	ns
t _{PLH}	CLK	A O	10	10	
tPHL	CLK	Any Q	12	12	ns
^t PLH	ENT	RCO	7.5	7.5	ns
^t PHL	LIVI	NCO	8.5	8.5	115
^t PLH	ENP	RCO	11.5	11.5	ns
^t PHL	LIVI	Neo	8.5	8.5	115
tPHL .	Clear (S0, S1 low)	Any Q	17	17	ns
tPLH	S0, S1	RCO	12	12	
[†] PHL	(count up/down)	NCO	13	13	ns
^t PHL	Clear (S0, S1 low)	RCO	22	22	ns

'ALS869 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5~V$ to 5.5 V, $C_L=500~pF,$ $R_L=500~\Omega,$ $T_A=MIN~to~MAX$						
			SN	154ALS		SN	174AL\$8	369	
			MIN	TYP [†]	MAX.	MIN	TYP [†]	MAX	
f _{max}			45			45			MHz
^t PLH	CLK	RCO		14			14		ns
^t PHL	OLK	l neo		13			13		113
^t PLH	CLK	Any Q		10			10		ns
^t PHL	CLIK	Ally G		12			12		115
^t PLH	ENT	RCO		7.5			7.5		ns
^t PHL	LIVI	NCO		8.5			8.5		115
^t PLH	ENP	RCO		11.5			11.5		ns
^t PHL		NCO .		8.5			8.5		115
^t PLH	S0, S1	RCO		12			12		
^t PHL	(count up/down)	l neo		13			13		ns
^t PHL	Clear (S0, S1 low)	RCO		22			22		ns
tPHL	Clear (S0, S1 low)	Any Q		17			17		ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



SN54AS867, SN74AS867 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS WITH ASYNCHRONOUS CLEAR

recommended operating conditions

			S	N54AS	867	SN	174AS8	67	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
Iон	High-level output current				- 2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		40	0		50	MHz
tw(clock)	Duration		12.5			10			ns
tw(clear)	Duration of clear pulse (SO and S1 lov	v)	12.5			10			ns
		Data inputs A-H	5			4			ns
		Enable P (ENP) or	9			8			
	·	Enable T (ENT)	9			°			ns
t _{su}	Setup time [†]	S0 or S1 (load)	11			10			ns
		S0 or S1 (clear)	11			10			ns
		S0 or S1 (count down)	42			40			ns
		S0 or S1 (count up)-	42			40			ns
th	Hold time at any input with respect to	clock↑	0			0			ns
tskew	Skew time between SO and S1 (maxin	num to							
skew	avoid inadvertent clear)		8			7			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST SOND	ITIONS	SN	54AS	367	SI	V74AS	867	UNIT
,	PARAMETER	TEST COND	THONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
V _{IK}		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			- 1.2	V
Voн		$V_{CC} = 4.5 \text{ V to 5}.$	5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -	2		V
VOL		$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.34	0.5		0.34	0.5	V
lj .	,	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
1	ENT	V E E V	$V_1 = 2.7 \text{ V}$			40			40	
ΉН	Other inputs	$V_{CC} = 5.5 V$,	V = 2.7 V			20			20	μΑ
	ENT					- 4			-4	^
ηL	Other inputs	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			- 2			- 2	mA
10 [§]		$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
^I CC		V _{CC} = 5.5 V			134	195		134	195	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS869, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS WITH SYNCHRONOUS CLEAR

recommended operating conditions

			s	N54AS	369	S۱	74AS8	69	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
Iон	High-level output current				- 2			- 2	mA
lOL	Low-level output current				20			20	mA
fclock	Clock frequency		0		40	0		45	MHz
tw(clock)	Duration		12.5			11			ns
		Data inputs A-H	6			5			ns
		Enable P (ENP) or Enable T (ENT)	10			9			ns
t _{su}	Setup time [†]	S0 or S1 (load)	13			11			ns
		S0 or S1 (clear)	13			11			ns
		SO or S1 (count down)	52			50			ns
		S0 or S1 (count up)	52			50			ns
th	Hold time at any input with respect to	o clock1	0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

[†]This setup time is required to ensure stable data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	TEST CONDITIONS		S869	SN	74AS	869	
	FANAIVICIEN	1231	CONDITIONS	MIN TYP	‡ MAX	MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	II = -18 mA		- 1.2	T		- 1.2	V
Vон		$V_{CC} = 4.5 \text{ V to 5}$	5 V, I _{OH} = -2 mA	V _{CC} 2		V _{CC} 2			V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA	0.3	4 0.5		0.34	0.5	V
- II		$V_{CC} = 5.5 V,$	V _I = 7 V		0.1			0.1	mA
Lea	ENT	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V		40			40	^
ΙΗ	Other inputs	VCC = 5.5 V,	V - 2.7 V		20			20	μΑ
L	ENT	V 5 5 V	V _I = 0.4 V		- 4			- 4	A
, IL	Other inputs	$V_{CC} = 5.5 \text{ V},$	V = 0.4 V		- 2			- 2	mA
lo§		$V_{CC} = 5.5 V$,	$V_{O} = 2.25 \text{ V}$	- 30	- 112	- 30		-112	mA
· ICC		$V_{CC} = 5.5 V$		12	5 180		125	180	mA

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS867, SN74AS867, SN54AS869, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

'AS867 switching characteristics (see note 1)

PARAMETER	FROM (INPUT	то оитрит	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX					
				AS867		AS867		
			MIN	MAX	MIN	MAX		
f _{max}			40		50		MHz	
^t PLH	CLK	RCO	5	31	5	22	ns	
^t PHL		1100	6	19	6	16	115	
^t PLH	CLK	Any Q	3	12	3	11		
^t PHL	CLK	Any G	4	16	4	15	ns	
tPLH	ENT	RCO	3	19	3	10		
^t PHL		RCO	5	21	5	17	ns	
^t PLH	ENP	RCO	5	14	. 5	14	ns	
^t PHL		1	5	21	5	17	115	
[†] PHL	Clear (S0, S1 low)	Any Q	7	23	7	21	ns	

'AS869 switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	(F	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega$ $T_A = \text{MIN to MAX}$				
				AS869		AS869		
			MIN	MAX	MIN	MAX		
f _{max}			40		45		MHz	
tPLH	CLK	RCO	6	35	6	35	ns	
t _{PHL}	CER	1100	6	20	6	18] '''	
tPLH	CLK	Any Q	3	12	3	11	no	
^t PHL	CLK ,	Ally d	4	16	4	15	ns	
^t PLH	ENT	RCO	3	25	3	15		
^t PHL	ENI	1100	6	21	6	17	ns	
^t PLH	ENP	RCO	5	27	5	19	no.	
^t PHL	CINE	1100	6	21	6	18	ns	

SN54ALS870, SN54AS870, SN54ALS871, SN54AS871 SN74ALS870, SN74AS870, SN74ALS871, SN74AS871 **DUAL 16-BY-4 REGISTER FILES**

D2661, DECEMBER 1982 - REVISED MAY 1986

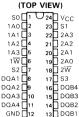
- 'ALS870 and 'AS870 in 24-Pin Small Outline, 300-mil DIP and Both Plastic and Ceramic 28-Pin Chip Carriers
- 'ALS871 and 'AS871 in 28-Pin 600-mil DIP and Both Plastic and Ceramic Chip Carriers
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Typical Access Time: 'ALS is 16 ns 'AS is 11 ns
- Each Register File Has Individual Write **Enable Controls and Address Lines**
- **Designed Specifically for Multibus** Architecture and Overlapping File Operations
- Prioritized B Input Port Prevents Write Conflicts During Dual Input Mode
- Dependable Texas Instruments Quality and Reliability

description

These devices feature two 16-word by 4-bit register files. Each register file has individual write-enable controls and address lines. The 'AS870 has two 4-bit data I/O ports (DQA1-DQA4 and DQB1-DQB4). The 'AS871 has one 4-bit data I/O port (DQB1-DQB4) with the other data port having individual data inputs (DA1-DA4) and data outputs (QA1-QA4). The data I/O ports can output to Bus A and Bus B. receive input from Bus A and Bus B, receive input from Bus A and output to Bus B, or output to Bus A and receive input from Bus B. To prevent writing conflicts in the dual-input mode, the B input port takes priority. Two select lines, SO and S1, control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0-1A3 or 2A0-2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN54ALS' and SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS' and SN74AS' family is characterized for operation from 0°C to 70°C.

SN54ALS870, SN54AS870 . . . JT PACKAGE SN74ALS870, SN74AS870 . . . DW OR NT PACKAGE

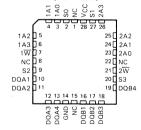


SN54ALS871, SN54AS871 . . . JD PACKAGE SN74ALS871, SN74AS871 . . . N PACKAGE

(TOP VIEW)

DA1	1T	28	J∨cc
DA2	2	27	DA4
so [3	26	□DA3
1A0 [4	25]s1
1A1 🗌	5	24]2A3
1A2 [6	23	32A2
1A3 🗌	7	22]2A1
1W	8	21] 2A0
S2 [9	20	2W
QA1	10	19	S3
QA2	11	18	DQB4
QA3	12	17] DQB3
QA4 [13	16	DQB2
GND [14	15	DQB1

SN54ALS870, SN54AS870 . . . FK PACKAGE SN74ALS870, SN74AS870 . . . FN PACKAGE (TOP VIEW)



SN54ALS871, SN54AS871 . . . FK PACKAGE SN74ALS871, SN74AS871 . . . FN PACKAGE (TOP VIEW)

SO DA2 DA1 DA4 1A1 1A2 🖥 6 2A3 1A3**[**] 7 2A2 23 € 1₩**|**] 8 22 2A1 S2 **5**9 21 2AC 2A0 QA1 10 19 □ S3

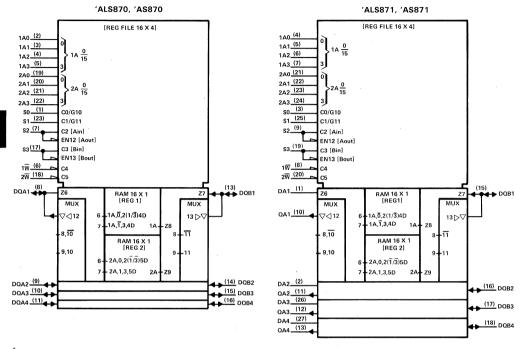
NC-No internal connection

INSTRUMENTS

3082

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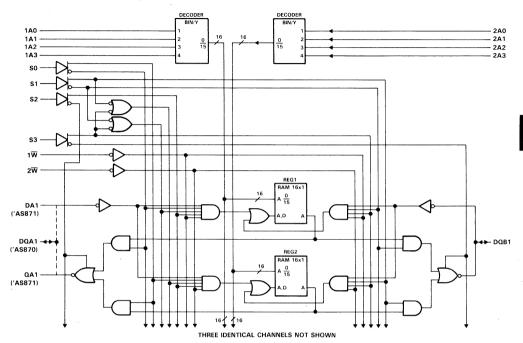
logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54ALS870, SN54AS870, SN54ALS871, SN54AS871 SN74ALS870, SN74AS870, SN74ALS871, SN74AS871

logic diagram (positive logic)



FUNCTION TABLE

	FILE S	SELECT		INPUT/OUT	PUT
S0	S 1	FILE SEL	S2	S3	I/O SEL
L	L	1R TO A, 1R TO B			
н	L	2R TO A, 1R TO B		1	A OUT, B OUT
L	н	1R TO A, 2R TO B	L	L	A 001, B 001
н	. н	2R TO A, 2R TO B			
L	L	A TO 1R, 1R TO B			
н	L	A TO 2R, 1R TO B	н	L	A IN, B OUT
L	н	A TO 1R, 2R TO B		L	A IN, B 001
н	н	A TO 2R, 2R TO B			
L	L	1R TO A, B TO 1R			
н	L	2R TO A, B TO 1R	1	н	A OUT, B IN
L	н	1R TO A, B TO 2R	L	п	A 001, B IIV
н	Н	2R TO A, B TO 2R			
L	L	B TO 1R			
Н	L	A TO 2R, B TO 1R	н	н	A IN, B IN
L	"H	A TO 1R, B TO 2R	**	**	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
н	н	B TO 2R			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Operating free-air temperature range: SN54ALS870, SN54ALS871..... -55°C to 125°C SN74ALS870, SN74ALS871......0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

				SN54ALS870 SN54ALS871		SN74ALS870 SN74ALS871			UNIT
		*	MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	, , , , , , , , , , , , , , , , , , , ,	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		. 2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
lOL	Low-level output current		T		12			24	mA
tw	Duration of write pulse		1.	10			10		ns
		Address before write!		2			2		
t _{su}	Setup times	Data before write1		4			4		⁴ns
		Select before write		3.5			3.5		1
		Address after write1		0			0		
th .	Hold times	Data after write1		0			0		ns
		Select after write1		0			0		1
TA .	Operating free-air temperature		- 55		125	0		70	°C

'ALS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	ITIONS		54ALS			74ALS		UNIT	
	.,	1201 00110		MIN	TYP [†]	MAX	MIN	TYP [↑]	MAX		
٧ _{IK}		$V_{CC} = 4.5 \text{ V},$	l _I = −18 mA			-1.2			- 1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V , $I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2			V _{CC} - 2				
۷он		$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.2					V	
		$V_{CC} = 4.5 \text{ V},$	IOH = -2.6 mA				2.4	3.2			
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.5				V	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	· · · · · · · · · · · · · · · · · · ·	
1.	Control inputs	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA	
Ŋ	DQA and DQB ports	V _{CC} = 5.5 V,	$V_1 = 5.5 \text{ V}$			0.2			0.2	mA	
	1₩ and 2₩		-			20			20		
۱н	Other control inputs	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			40			40	μΑ	
	DQA and DQB ports [‡]	·				50			50		
1	Control inputs	V 55.V	V ₁ = 0.4 V			-0.2			-0.2	^	
ΗL	DQA and DQB ports [‡]	$V_{CC} = 5.5 V,$	VI = 0.4 V			-0.2			-0.2	mA	
10 [§]		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.25 \text{ V}$	- 30		-112	-,30		- 112	mA	
lcc		V _{CC} = 5.5 V			70.5			70.5		mA	

'ALS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDIT	IONS	SN	54ALS	371	SN	74ALS8	371	UNIT
	OL OL OL OZH QA outputs OZL QA outputs CONTrol and DA input	TEST CONDIT	IONS	MIN	TYP [↑]	MAX	MIN	TYP [†]	MAX	ONIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
V_{OH}		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.2					V
		$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
Va		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$		0.25	0.5				V
VOL.		$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
lozh	QA outputs	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL	QA outputs	$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
	Control and DA inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1 mA	
11	DQB ports	$V_{CC} = 5.5 V,$	$V_1 = 5.5 V$			0.2			0.2	IIIA
	$1\overline{W}$, $2\overline{W}$, and DA inputs					20			20	
Лн.	Other control inputs	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			40			40	μΑ
ĺ	DQB ports [‡]					50			50	
	Control and DA inputs	V E E V	V: - 0.4.V			-0.2			-0.2	mA
11L	DQB ports [‡]	$V_{CC} = 5.5 \text{ V}, \qquad V_{I}$	V ₁ = 0.4 V			-0.2			-0.2	IIIA
10 [§]		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
Icc		$V_{CC} = 5.5 V$			70.5			70.5		mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, Ios.

'ALS870 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 C _L = 500 p R ₁ = 500 Q R ₂ = 500 Q T _A = MIN 1	oF, 2, 2,	UNIT	
1			SN54ALS870	SN74ALS870		
			MIN TYP† MAX	MIN TYP† MAX		
t _{a(A)}	Any A	Any DQ	11.5	11.5	ns	
	S0	Any DQA	16	16		
t _a (S)	S1	Any DQB	16 ⁻	16	ns	
+	S2	Any DQA	9.5	9.5		
^t dis	S3	Any DQB	9.5	9.5	ns	
	S2	Any DQA	7.5	7.5	200	
^t en	S3	Any DQB	7.5	7.5	ns	
	\overline{W}	Any DQ 12.5		12.5		
t _{pd}	DQA	DQB	16.5	16.5	ns	
	DQB	DQA	16.5	16.5	L	

'ALS871 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 C _L = 500 R ₁ = 500 R ₂ = 500 T _A = MIN	UNIT		
•			SN54ALS871	SN74ALS871		
			MIN TYP† MAX	MIN TYP† MAX		
t _{a(A)}	Any.A	Any QA or DQB	11.5	11.5	ns	
+ 101	S0	Any QA	16	16	ns	
t _a (S)	S1	Any DQB	16	16	115	
+	S2	Any QA	9.5	9.5	ns	
^t dis	S3	Any DQB	9.5	9.5	1 115	
	S2	Any QA	7.5	7.5		
t _{en}	S 3	Any DQB	7.5	7.5	ns	
	₩	Any QA or DQB	12.5	12.5		
t _{pd}	DA	DQB	16.5	16.5	ns	
•	DQB	QA	16.5	16.5		

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

SN54AS870, SN74AS870, SN54AS871, SN74AS871 DUAL 16-BY-4 REGISTER FILES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC 7 V
Input voltage: All inputs
I/O ports
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54AS870, SN54AS871
SN74AS870, SN74AS871 0°C to 70°C
Storage temperature range65°C to 150°C

recommended operating conditions

				SN54AS	870	s	N74AS	870	
				SN54AS	871	S	N74AS	871	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	1
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltaç	le .	2			2			V
VIL	Low-level input voltag	e			0.8			0.8	V
IOH	High-level output curr	ent			- 12			- 15	mA
lOL	Low-level output curre	ent			32			48	mA
t _w	Duration of write puls	е	12			12	,		ns
		Address before write↓	5			5			
t _{su}	Setup times	Data before write↑	15			15			ns
		Select before write↓	12			12	-		
		Address after write↑	. 0			0			
th	Hold times	Data after write↑	0			0			ns
		Select after write↑	12		-	12			1
TA	Operating free-air tem	perature	- 55		125	0		70	°C

'AS870 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	ITIONE	S	N54AS	370	SI	N74AS8	70	UNIT	
	PARAMETER	TEST COND	THONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.2			- 1.2	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$'_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -2 \text{ mA}$		2		Vcc -	2			
Voн		V _{CC} = 4.5 V,	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V	
	,	V _{CC} = 4.5 V,	I _{OH} = -15 mA				2.4	3.2			
Vai		$V_{CC} = 4.5 V,$	I _{OL} = 32 mA		0.25	0.5				V	
Vol		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5	· ·	
1.	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA	
l)	DQA and DQB ports	$V_{CC} = 5.5 V,$	$V_{I} = 5.5 V$			0.2			0.2	""A	
	1W and 2W					20			20		
ΊΗ	Other control inputs	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			40			40	μΑ	
	DQA and DQB ports [‡]					50			50	1	
lu.	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			- 2			- 2	mΑ	
l IIL	DQA and DQB ports [‡]	VCC = 5.5 V,	V - 0.4 V			- 2			- 2	l IIIA	
IO§	-	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		112	- 30		~ 112	mA	
Icc		V _{CC} = 5.5 V			120	190		120	190	mA	

'AS871 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		00ND:			SN54AS	871	S	N74AS	371	
,	PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.2			- 1.2	. V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	/, I _{OH} = -2 mA	Vcc-	2		Vcc	2		
VoH		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2.4	3.2			,		V
		V _{CC} = 4.5 V,	$I_{OH} = -15 \text{ mA}$				2.4	3.2		
1/		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.5				V
V_{OL}		V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5	v
lozh	QA outputs	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	QA outputs	$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 50			- 50	μΑ
I.	Control and DA inputs	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mΑ
Ц	DQB ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.2			0.2	IIIA
	$1\overline{W}$, $2\overline{W}$, and DA inputs					20			20	
ΙН	Other control inputs	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			40			40	μΑ
	DQB ports [‡]					50			50	
	Control and DA inputs	Vcc = 5.5 V,	V _I = 0.4 V			- 2			- 2	mA
IIL	DQB ports [‡]	vCC - 5.5 v,	VI - 0.4 V			- 2			- 2	11174
IO§		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		- 112	- 30		- 112	mA
lcc		V _{CC} = 5.5 V			120	190		120	190	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.



[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, Ios.

SN54ALS870, SN74ALS870, SN54ALS871, SN74ALS871 DUAL 16-BY-4 REGISTER FILES

'AS870 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4$ $C_L = 50$ $R_1 = 500$ $R_2 = 500$ $T_A = MII$	Ο Ω, Ο Ω,	V,	UNIT
			SN54	AS870	SN74	S870	
			MIN	MAX	MIN	MAX	
t _{a(A)}	Any A	Any DQ	5	20	5	15	ns
+	S0	Any DQA	3	15	3	13	
^t a(S) .	S1	Any DQB	3	15	3	13	ns
+	S2	Any DQA	3	12	3	11	20
^t dis	S3	Any DQB	3	12	3	11	ns
	S2	Any DQA	3	15	3	12	
t _{en}	S3	Any DQB	3	15	3	12	ns
	W	Any DQ	5	23	5	19	
t _{pd}	DQA	DQB	5	25	5 '	22	
	DQB	DQA	5	25	5	22	

'AS871 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	SN54	$V_{CC} = 4$ $C_L = 50$ $R_1 = 500$ $R_2 = 500$ $T_A = MIN$ AS871) Ω,) Ω,		UNIT
			MIN	MAX	MIN	MAX	
t _{a(A)}	Any A	Any QA or DQB	5	20	5	16	ns
	S0	Any QA	3	15	3	13	ns
t _a (S)	S1	Any DQB	3	15	3	13	ns
4	S2	Any QA	3	12	3	11	
^t dis	S3	Any DQB	3	12	3	11	ns
	S2	Any QA	3	15	3	12	
t _{en}	S3	Any DQB	3	15	3	12	ns
	W	Any QA or DQB	5	23	5	19	
t _{pd}	DA	DQB	5	26	5 .	23	ns
·	DQB	QA	5	26	5	23	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS873B, SN54AS873, SN74ALS873B, SN74AS873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2661, APRIL 1982 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- 'ALS880A and 'AS880 are Alternative Versions with Inverting Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{\text{CLR}}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{\text{OC}}$ (output control) is at a high logic level.

The SN54ALS873B and SN54AS873 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS873B and SN74AS873 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

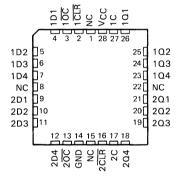
FUNCTION TABLE (EACH LATCH)

	IN	PUTS		OUTPUT
OC	CLR	D	α	
L	L	Х	Х	L
L	н	н	Н	н
L	н	н	L	L
L	н	L	×	a_0
Н	X	×	Χ	Z

SN54ALS873B, SN54AS873 . . . JT PACKAGE SN74ALS873B, SN74AS873 . . . DW OR NT PACKAGE (TOP VIEW)

	_		—
1CLR	Ц1	O 24	∐ Vcc
10C	2	23] 1C
1D1]3	22	101
1D2	4	21	102
1D3	_ 5	20	103
1D4	∏ 6	19] 104
2D1	7	18	201
2D2	8	17	202
2D3	∏ 9	16] 203
2D4	1 0	15	204
20C	∐ 11	14	2C
GND	<u> </u> 12	13	2CLF

SN54ALS873B, SN54AS873 . . . FK PACKAGE SN74ALS873B, SN74AS873 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol[†]

10C (2) (23)1C-(1) 1CLR-(22) (3) 1D1 1D (21) 102 (4) 1D2 (20) 103 (5) 1D3 (19) 104 (6) (11)(14)2C (13)2CLR

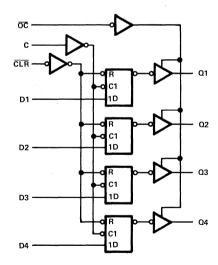
2C (13) R

2D1 (7) 1D ∇ (18) 201

2D2 (9) (16) 203

2D4 (10) (15) 204

logic diagram (each quad latch, positive logic)



 $^{^{\}dagger} This$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

SN54ALS873B, SN54AS873, SN74ALS873B, SN74AS873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	
Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	.5 V
Operating free-air temperature range: SN54ALS873B, SN54AS873 55 °C to 12	5°C
SN74ALS873B, SN74AS873	0°C
Storage temperature range $\dots -65^{\circ}\text{C}$ to 15	0°C

recommended operating conditions

			SN	54ALS	373B	SN	74ALS8	373B	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
Іон	High-level output current				- 1			-2.6	mA
loL	Low-level output current				12			24	mA
	Pulse duration	CLR low	15			15			
t _w	ruise duration	Enable C high	10			10			ns
t _{su}	Setup time, data before e	nable CI	10			10			ns
th	Hold time, data after enab	le CI	7			7			ns
TA	Operating free-air tempera	ture	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SNS	54ALS8	373B	SN	UNIT		
PARAMETER	1551 C	ONDITIONS	MIN	TYP [†]	MAX	MAX MIN - 1.2 V _{CC} -	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_1 = -18 \text{ mA}$			-1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to 5}.$	5 V, IOH = -0.4 mA	V _{CC} -	2		Vcc-	2		
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		1
Vai	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	, V
Vol	V _{CC} = 4.5 V,	I _{OL} = 24 mA					0.35	0.5	1 °
lozh	$V_{CC} = 5.5 V,$	V _O = 2.7 V			20			20	μΑ
IOZL	$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 20			- 20	μΑ
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
IL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2			-0.2	mA
10 [‡]	$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
		Outputs high		11	21		11	21	
^I CC	$V_{CC} = 5.5 V$	Outputs low		16	29		16	29	mA
		Outputs disabled		20	31		20	31	l

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

-SN54ALS873B, SN74ALS873B DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	C = 5 = 50 = 500 = 500 = 25 LS873	pF OΩ OΩ °C B	C _L R1 R2 Тд	CC = 4.5 V = 50 pF, = 500 Ω = 500 Ω = MIN to	MAX SN74	ALS873B	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Ω		7	11	2	17	2	14	ns
tPHL		Q.		7	10	2	15	2	14	115
^t PLH	С	a		13	17	8	29	8	22	ns
tPHL	Č	u		14	18	8	26	8	21	113
t _{PHL}	CLR	Q		12	16	6	24	6	20	ns
^t PZH	ōc	α		11	14	4	22	4	18	ns
tPZL	UC .	u u		11	15	4	23	4	18	115
tPHZ	ōc	Q		7	9	2	12	2	10	ns
tPLZ				7	11	2	21	2	15	1115

SN54AS873, SN74AS873 **DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS**

recommended operating conditions

			IS S	V54ASE	373	SN	74AS87	73	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage)	2			2			V
VIL	Low-level input voltage	:			0.8			0.8	٧
ІОН	High-level output curre	nt			-12			- 15	mA
lOL	Low-level output currer	nt			32			48	mA
	Pulse duration	CLR low	4.5			3.5			
t _W	ruise duration	Enable C high	5.5			4.5			ns
t _{su}	Setup time, data before	e enable CI	2			2			ns
th	Hold time, data after er	nable CI	3			3			ns
TA	Operating free-air temp	erature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEGT C	ONDITIONS	SN	54AS8	73	SN	74AS8	73	LINUT
PARAMETER	TEST C	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_I = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	$5 \text{ V}, \text{ I}_{OH} = -2 \text{ mA}$	Vcc-	2		Vcc-	2		
VOH	$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V
1	$V_{CC} = 4.5 V$,	$I_{OH} = -15 \text{ mA}$				2.4	3.3		
Va	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.5				V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5	L
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			50			50	μΑ
IOZL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50			- 50	μΑ
ij	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ЧĤ	$V_{CC} = 5.5 V$,	$V_{\parallel} = 2.7 \text{ V}$			20			20	μΑ
IIL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.5			-0.5	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
		Outputs high		68	110		68	110	
lcc	V _{CC} = 5.5 V	Outputs low		67	109		67	109	mA
		Outputs disabled		80	129		80	129	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS873, SN74AS873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO . (OUTPUT)		V _{CC} = 4.5 C _L = 50 pF R1 = 500 S R2 = 500 S T _A = MIN	e, Ω, Ω, to MAX SN74	AS873	UNIT
			MIN 3	MAX 9	MIN 3	MAX 6	ļ
t _{PLH}	D	α					ns
t _{PHL}			3	7	3	6	
t _{PLH}	С	α	6	14	6	11.5	ns
^t PHL		Q .	4	9	4	7.5	113
^t PHL	CLR	Q.	3	8.5	3	7.5	ns
^t PZH	ŌĊ	Q	2	8	2	6.5	
†PZL	UC .	u u	4	11	4	9.5	ns
^t PHZ	<u> </u>	Q	2	8	2	6.5	ns
tPLZ			2	8.5	2	7.5	l '' ^s

SN54ALS874B, SN54ALS876A, SN54AS874, SN54AS876 SN74ALS874B, SN74ALS876A, SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

D2661, APRIL 1982 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic 'ALS874B, 'AS874 True Outputs 'ALS876A, 'AS876 Inverting Outputs
- Asynchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These dual four-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices paricularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ALS874B and 'AS874 have $\overline{\text{CLR}}$ inputs and noninverting Q outputs; the 'ALS876A and 'AS876 have $\overline{\text{PRE}}$ inputs and inverting Q outputs. In each case, taking this input low causes the four Q or Q outputs to go low independently of the clock.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C.

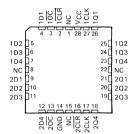
SN54ALS874B, SN54AS874 . . . JT PACKAGE SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE (TOP VIEW)

> U24[] VCC 1018 11 10C 2 23 1CLK 1D1 22 1Q1 21 1Q2 1D2 114 1D3 F 20 103 1D4 F 19 104 104 2D1 [202 [17 202 2D3 Г 16 2Q3 15 2Q4 2D4 20C 14 2 2CLK

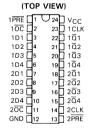
13 7 2 CLR

SN54ALS874B, SN54AS874 . . . FK PACKAGE SN74ALS874B, SN74AS874 . . . FN PACKAGE (TOP VIEW)

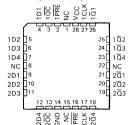
GND



SN54ALS876A, SN54AS876 . . . JT PACKAGE SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE



SN54ALS876A, SN54AS876 . . . FK PACKAGE SN74ALS876A, SN74AS876 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

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FUNCTION TABLES

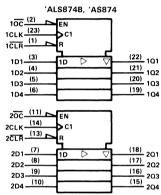
'ALS874B, 'AS874 (EACH FLIP-FLOP)

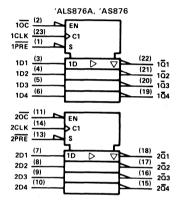
	INPU	OUTPUT		
ŌĊ	CLR	CLK	D	Ο.
L	L	Х	Х	L
L	Н	1	Н	Н.
L	Н	1	L	L
L	Н	L	Χ	a_0
Н	X	Х	Χ	Z

'ALS876A, 'AS876 (EACH FLIP-FLOP)

	INPL	OUTPUT		
ОС	PRE	CLK	D	ā
L	L	Х	Χ	L
L	Н	1	Н	L
L	Н	1	L	н
L	Н	L	Х	\bar{a}_0
Н	Х	Х	Х	Ζ.

logic symbols†

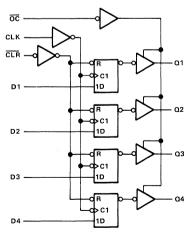




 $^{^{\}dagger}$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617.12.

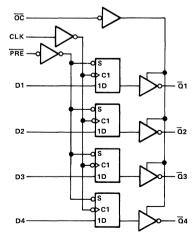
logic diagrams (positive logic)

'ALS874B, 'AS874 (EACH QUAD FLIP-FLOP)



Pin numbers shown are for DW, JT, and NT packages.

'ALS876A, 'AS876 (EACH QUAD FLIP-FLOP)





SN54ALS874B, SN54ALS876A SN74ALS874B, SN74ALS876A DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC 7 V
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS874B, SN54ALS876A 55 °C to 125 °C
SN74ALS874B, SN74ALS876A
Storage temperature range65 °C to 150 °C

recommended operating conditions

			SNS	4ALS8	74B	SN	74ALS	374B	
			SNS	4ALS8	76A	SN	74ALS	376A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX]
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
¹ ОН	High-level output current				- 1			-2.6	mA
lOL	Low-level output current				12			24	mA
fclock	Clock frequency		0		25	0		30	MHz
		PRE or CLR low	10			10			
tw	Pulse duration	CLK high	20			16.5			ns
		CLK low	20			16.5			
	Cotton time before CLK!	Data	15			15			
t _{su}	Setup time before CLK1	PRE or CLR inactive	10			10			ns
th	Hold time, data after CLK1		4			0			ns
TA	Operating free-air tempera	ture	- 55		125	0		. 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST CO	NDITIONS	0	4ALS8	–		4ALS8		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{\rm A} = -0.4 \text{ mA}$	V _{CC} - 2			V _{CC} -	2		
∨он		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					\ \ \
		$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL.		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 24 \text{ mA}$					0.35	0.5]
lozh		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 V$			20			20	μΑ
^l OZL		$V_{CC} = 5.5 \text{ V},$	V _O = 0.4 V			- 20			- 20	μΑ
11		$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
ЧН		$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IIL		$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.2			-0.2	mA
1o‡		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
			Output high		14	21		14	21	
	'ALS874B		Outputs low		19	30		19	30	1
loo		$V_{CC} = 5.5 \text{ V}$	Outputs disabled		20	32		20	32] ,
1cc		VCC = 0.5 V	Outputs high		14	21		14	21	mA
	'ALS876A		Outputs low		18	29		18	29	
			Outputs disabled		20	31		20	31	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN74ALS874B, SN74ALS876A **DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

'ALS874B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	C _L R1 R2 T _A	C = 5 = 50 = 50 = 50 = 25	pF, D Ω, D Ω, °C	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to	MAX	ALS874B	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax			40	50		25		30		MHz
^t PLH	CLK.	Any Q		8	10	4	15	4	14	ns
^t PHL	CEIX.	Ally Q		8	13	4	15	4	14	113
^t PHL	CLR	Any Q		11	14	5	20	5	17	ns
^t PZH	oc	Any Q		9	12	4	21	4	18	ns
^t PZL	ÜC.	Ally U		11	15	4	21	4	18	l iis
tPHZ	oc	Any Q		6	8	2	12	2	10	ns
^t PLZ	00	Ally Q		5.7	8	3	15	3	12	115

'ALS876A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R ₁ R ₂	CC = 50 = 50 = 50 = 50 = 25	pF, Ο Ω, Ο Ω,	C _L R1 R2 T _A	C = 4.5 C = 50 pF, = 500 Ω , = 500 Ω , = MIN to	мах		UNIT
•				TYP	 		LS876A MAX	SN74	ALS876A MAX	
	***************************************		MIN		IVIAA	MIN 25	IVIAA		IVIAA	MHz
fmax			40	50				- 30		IVITIZ
tPLH .	CLK	Any Q		8	11	4	15	4	14	ns
t _{PHL}	CER	Ally Q		9	12	4	15	4	14] "
^t PHL	PRE	. Any $\overline{\Omega}$		10	16	6	22	6	19	ns
^t PZH	oc	Any Q		10	13	4	21	4	18	ns
^t PZL	00	Ally Q		11	15	4	21	4	18	
^t PHZ	оc	· Any Q		6	8	2	12	2	10	ns
tPLZ	00	Ally Q		7	10	3	15	3	. 13	1 !!3

SN54AS874, SN54AS876, SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) SN74AS874, SN74AS876 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

				SN54AS874 SN54AS876			74AS87 74AS87		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX]
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				-12			- 15	mA
lOL	Low-level output current				32			48	mA
fclock	Clock frequency		0		100	0		125	MHz
		PRE or CLR low	4			2			
t_{W}	Pulse duration	CLK high	4			3			ns
		CLK low	5			4			Ī
	Setup time	Data	2.5			2			
t _{su}	before CLK↑	PRE or CLR inactive	5			4			ns
th	Hold time, data after CLK↑		1			1			ns
TA	Operating free-air temperat	ure	- 55		125	0		.70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			154AS8 154AS8		Į.	74AS87 74AS87		UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 \text{ V},$	•			- 1.2			- 1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	5 V, IOH = -2 mA	V _{CC} -	2		V _{CC} -	2		
Vон		$V_{CC} = 4.5 V$,	$I_{OH} = -12 \text{ mA}$	2.4	3.2					V
		$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -15 \text{ mA}$					2.4	3.3		1
1/01		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.4				V
VOL		$V_{CC} = 4.5 V$	I _{OL} = 48 mA					0.35	0.5	1 °
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50			- 50	μΑ
l ₁		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΙΗ		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			10	μΑ
Lie	D	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 3			- 2	mA
IL	All other	vCC = 5.5 v,	V = 0.4 V			-0.5			-0.5	IIIA
10 [‡]		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
			Output high		82	133		82	133	
	'AS874		Outputs low		92	149		92	149	
1	сс	V F F V	Outputs disabled		100	160		100	160	mA
CC		$V_{CC} \approx 5.5 \text{ V}$	Outputs high		88	142		88	142	
	'AS876		Outputs low		94	150		94	150	
	1 1		Outputs disabled		100	160		100	160	1

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54AS874, SN54AS876, SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

'AS874 switching characteristics (see Note 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to MAX}$ $SN54AS874 = SN74AS874$					
			MIN	MAX	MIN	MAX		
· f _{max}			100		125		MHz	
^t PLH	CLK	Any Q	3	11.5	3	8.5		
^t PHL	CLK	Any Q	4	12.5	4	10.5	ns	
tPHL	CLR	Any Q	4	11	4	9.5	ns	
^t PZH	ōc	Any Q	2	8	2	7	20	
tPZL		Ally C	3	11.5	3	10.5	ns	
t _{PHZ}	ŌĊ	Any Q	- 2	7	2	6	ns	
tPLZ		Ally Q	2	8.5	2	7.5	115	

'AS876 switching characteristics (see Note 1)

PARAMETER	PARAMETER FROM TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$					
		Į.	SN54	AS876	SN74	AS876	I	
			MIN	MAX	MIN	MAX		
fmax			100		125		MHz	
^t PLH	CLK	Any Q	3	11.5	3	8.5	ns	
^t PHL	CLK	Ally Q	4	12.5	4	10.5	l iis	
t _{PHL}	PRE	Any Q	4	11	4	9.5	ns	
^t PZH	ŌC	Any Q	2	. 8	2	7		
tPZL	OC	Ally Q	3	11.5	3	10.5	ns	
tPHZ	ŌC	Any Q	2	7	2	6	ns	
^t PLZ	00	Any Q	2	7	2	6	1115	

SN54AS877, SN74AS877 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

D2661, DECEMBER 1982-REVISED AUGUST 1985

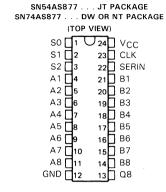
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascaded to n-Bits
- Eight Selectable Transceiver/Port Functions:
 A to B or B to A
 Register to A or Register to B
 Shifted to A or Shifted to B
 Off-Line Shifts (A and B Ports in High-Impedance State)
 Register Clear
- Particularly Suitable for Use in Signature-Analysis Circuitry
- Serial Register Provides:

 Parallel Storage of Either A or B Input
 Data

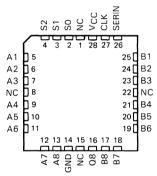
 Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines SO, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port.



SN54AS877....FK PACKAGE SN74AS877....FN PACKAGE (TOP VIEW)



NC-No internal connection

serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS877 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS877 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

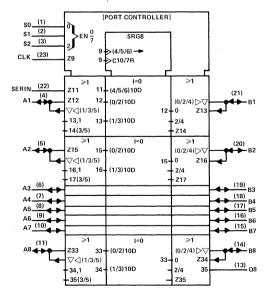
MODE

FUN	CTION	TABLE

S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	FUNCTION	
LLL	H or L	X	Z Q _n A1	Z Q _n A2	Z Q _n A3	Z Q _n A4	Z Q _n A5	Z Q _n A6	Z Q _n A7	Z Q _n A8	A TO B	
LLL	1	×	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	АТОВ	
LLH	H or L	Х	B1 Q _n Z	B2 Q _n Z	B3 Q _n Z	B4 Q _n Z	B5 Q _n Z	В6 Q _n Z	B7 Q _n Z	B8 Q _n Z	в то а	
LLH	1	×	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	ВІОА	
L H,L	H or L	Х	Χ Q _n Q1	X Q _n Q2	X Q _n Q3	Χ Q _n Q4	Χ Q _n Q5	Χ Q _n Q6	Χ Q _n Q7	Χ Q _n Q8	Q _N TO B _N	
LHL	1	×	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	GM 10 BM	
LHH	H or L	Х	Q1 Q _n X	Q2 Q _n X	Ω3 Ω _n X	Q4 Q _n Χ	Q5 Q _n Χ	Q6 Q _n Χ	Q7 Q _n Χ	Q8 Q _n Χ	Q _N TO A _N	
LHH	1	Х	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	QN TO AN	
HLL	H or L	X	Z Q _n Q1	Z Q _n Q2	Z Q _n Q3	Z Q _n Q4	Z Q _n Q5	Z Q _n Q6	Z Q _n Q7	Z Q _n Q8	SHIFT	
HLL	1	н	ZHH	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO	
HLL	1	L	ZLL	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	В	
HLH	H or L	X	Q1 Q _n Z	Q2 Q _n Z	03 0 _n Z	Q4 Q _n Z	Q5 Q _n Z	Q6 Q _n Z	Q7 Q _n Z	Ω8 Ω _n Z	SHIFT	
H L H	1	н	HHZ	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO	
HLH	1	L	LLZ	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	Α	
HHL	H or L	X	z Q _n z	z Q _n z	z Q _n z	z Q _n z	z Q _n z	z Q _n z	z o _n z	Z Q _n Z		
HHL	1	Н	ZHZ	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	SHIFT	
HHL	1	L	ZLZ	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z		
ннн	H or L	Х	z Q _n ż	z Q _n z	z Q _n z	z Q _n z	z Q _n z	z o _n z	z Q _n z	ZQnZ	CLEAR	
ннн	1	Х	ZLZ	ZLZ	ZLZ	ZLZ	ZLZ	ZLZ	ZLZ	ZLZ	CLLAN	

level of Q_n(n = 1, 2...8) established on most recent 1 transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

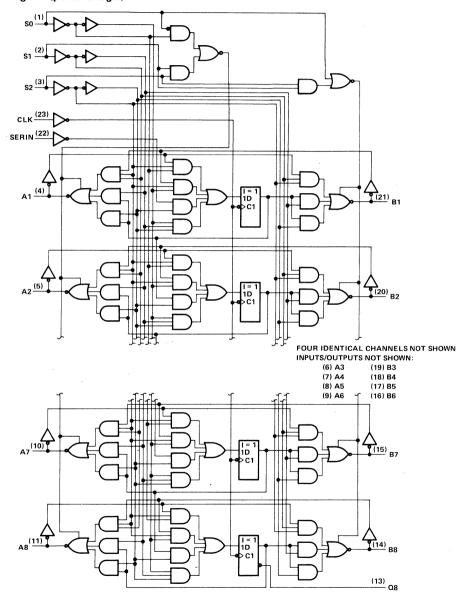
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



Supply voltage, VCC 7 V Input voltage: All inputs 7 V I/O ports 5.5 V Voltage applied to a disabled 3-state output 5.5 V Operating free-air temperature range: SN54AS877 -55°C to 125°C SN74AS877 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

			S	SN54AS877			SN74AS877			
	•		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage		2			2			V	
VIL	Low-level input voltage				0.8			0.8	V	
lau	High-level output current	A1-A8, B1-B8			- 12			- 15	j	
Іон	riigii-ievei output current	Q8			- 2			- 2	mA	
lOL	Low lovel output ourrent	A1-A8, B1-B8			32			48	mA	
	Low-level output current	Ω8			20			20		
fclock	Clock frequency		0		45	0		50	MHz	
t _w	Duration of clock pulse		11			10			ns	
		A1-A8, B1-B8	5.5			5.5				
t _{su}	Setup time before CLK↑	SERIN	5.5			5.5			ns	
		S0, S1, S2	5.5			5.5			Ī	
^t h		A1-A8, B1-B8	0							
	Hold time, data after CLK1	SERIN	"	0 0			ns			
		S0, S1, S2	0			0				
TA	Operating free-air temperature		- 55		125	0		70	°C	

SN54AS877, SN74AS877 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise

PARAMETER		TEST CONDITIONS			154AS8	377	SI	UNIT			
	PANAIVIETEN	TEST CONDITIONS			TYP [†]	MAX	MIN	TYP [†]	MAX	UNII	
V_{IK}		$V_{CC} = 4.5 V,$	I _I = 18 mA			- 1.2			- 1.2	V	
Vон	A1-A8	$V_{CC} = 4.5 V,$	I _{OH} = -12 mA	2	3.2						
	B1-B8	V _{CC} = 4.5 V,	I _{OH} = -15 mA				2	3.3		v	
	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -	2		Vcc-	- 2		t	
	All outputs except Q8	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 32 mA		0.25	0.5				V	
VOL	All outputs except do	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA					0.35	0.5		
	Q8	V _{CC} = 4.5 V,	I _{OL} = 20 mA	0.25	0.5		0.25	0.5]		
	S0, S1, S2	V _{CC} = 5.5 V,	V _I = 7 V			0.3			0.3		
l _l	CLK and SERIN	vCC = 5.5 v,				0.1			0.1	mA	
	A1-A8, B1-B8	V _{CC} = 5.5 V,	V _I = 5.5 V			0.2			0.2	1	
	S0, S1, S2		V _I = 2.7 V			60			60		
ήн	CLK and SERIN	$V_{CC} = 5.5 V$,				20			20	μΑ	
	A1-A8, B1-B8 [‡]					70			70	1	
	S0, S1, S2		VI = 0.4 V			- 1			- 1		
IIL	CLK and SERIN	$V_{CC} = 5.5 V$,				- 0.5			-0.5	mA	
	A1-A8, B1-B8 [‡]					- 0.75			-0.75	1	
	Except Q8	V 55.V	0.05.1/	- 30		- 112	- 30		- 112		
IO§	Q8	V _{CC} = 5.5 V,	V _O = 2.25 V	- 20		- 112	- 20		- 112	mA	
lcc .		V _{CC} = 5.5 V			136	220		136	220	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	(F F	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS877 \qquad SN74AS877$ $MIN \qquad MAX \qquad MIN \qquad MAX$				
f _{max}			45		50		MHz	
[‡] PLH	Any A port	Any B port	2	8.5	2	7		
^t PHL	Any A port		3	10.5	3	9	ns	
tPLH	Any B port	Any A port	2	9	2	7.5	ns	
^t PHL	7 Ally B port		3	10.5	3	9] ""	
^t PLH	S0, S1, S2	Any A or B	3	11.5	3	10	ns	
[†] PHL	50, 51, 52	port	2	9.5	2	8	115	
^t PLH	CLK	Any A or B	2	11	2	9	ns	
^t PHL	CLK	port	3	13	3	11.5	115	
^t PLH	CLK	QB	2	10.5	2	8	ns	
[†] PHL	CLK	QB	3	10	3	8.5	1115	
^t PHZ			2	7.5	2	6.5	ns	
tPLZ	S0, S1, S2	Any A or B	3 `	13	3	10.5	,,,,	
^t PZH] 30, 31, 32	port	2	9	2	7	ns	
^t PZL			3	11.5	3	9.5] ''3	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

The positive transition of S2 will cause low-level data at the A output Bus or stored in the shift register to be invalid for 12 ns.



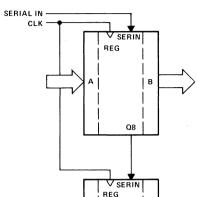
 $^{^{\}ddagger}$ For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.

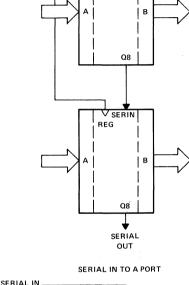
The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

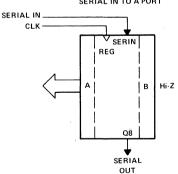
BUS A TO BUS B OR

SERIAL TRANSMISSION

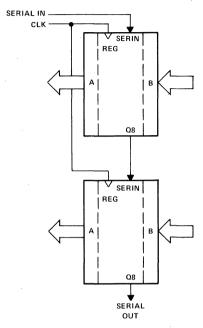
TYPICAL APPLICATION DATA



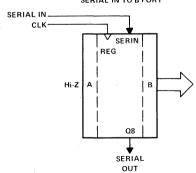




BUS B TO BUS A OR SERIAL TRANSMISSION



SERIAL IN TO B PORT



SN54ALS878A, SN54ALS879A, SN54AS878, SN54AS879 SN74ALS878A, SN74ALS879A, SN74AS878, SN74AS878 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2661, APRIL 1982 REVISED MAY 1986

- 3-State Bus Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Choice of True or Inverting Logic 'ALS878A, 'AS878 True Outputs 'ALS879A, 'AS879 Inverting Outputs
- Synchronous Clear
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit edge-triggered flip-flops enter data on the low-to-high transition of the clock (1CLK and 2CLK). All types have individual synchronous clear inputs and output control pins for each group of 4-bit registers.

The SN54ALS' and SN54AS' devices are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS' and SN74AS' devices are characterized for operation from 0°C to 70°C .

SN54ALS878A, SN54AS878 . . . JT PACKAGE SN74ALS878A, SN74AS878 . . . DW OR NT PACKAGE (TOP VIEW)

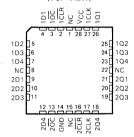
∪24] ∨_{CC} 23] 1CLK 1CLB 10C 🗖 22 101 1D1 🛚 3 1D2 | 1D3 | 21 102 20 103 104 19 104 18 201 17 202 2D1 🗆 202 귀 2D3 16 203 2D4 10 2OC 11 15 2Q4 14 2CLK

SN54ALS878A, SN54AS878 . . . FK PACKAGE SN74ALS878A, SN74AS878 . . . FN PACKAGE

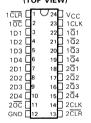
GND T12

(TOP VIEW)

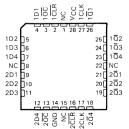
13 2CLR



SN54ALS879A, SN54AS879 . . . JT PACKAGE SN74ALS879A, SN74AS879 . . . DW OR NT PACKAGE (TOP VIEW)



SN54ALS879A, SN54AS879 . . . FK PACKAGE SN74ALS879A, SN74AS879 . . . FN PACKAGE (TOP VIEW)



NC - No internal connection

TEXAS INSTRUMENTS

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SN54ALS878A, SN54ALS879A, SN54AS878, SN54AS879 SN74ALS878A, SN74ALS879A, SN74AS878, SN74AS879 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS878A, 'AS878 (EACH FLIP-FLOP)

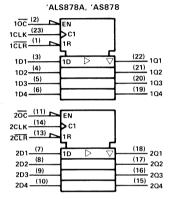
(2710111211112011									
	INP	UTS		OUTPUT					
ОC	CLR	CLK	D	a					
L	L	1	Х	L					
L	Н	†	Н	' н					
L	Н	†	L	L					
L	Н	L	X	σ_0					
Н	Х	X	Х	z					

FUNCTION TABLES

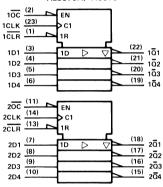
'ALS879A, 'AS879 (EACH FLIP-FLOP)

	INP	UTS		OUTPUT
ŌĊ	CLR	CLK	D	ā
L	L	1	Х	Н
L	Н	↑	Н	L
L	Н	†	L	н
L	Н	L	Х	a_0
Н	Х	Χ	Х	Z

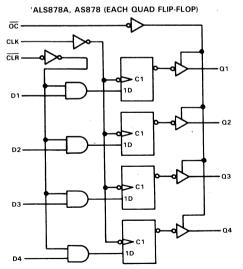
logic symbols†



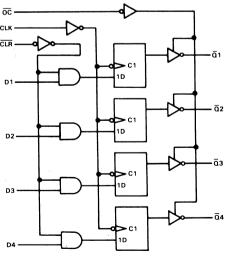
'ALS879A, 'AS879



logic diagrams (positive logic)



'ALS879A, 'AS879 (EACH QUAD FLIP-FLOP)



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



SN54ALS878A, SN54ALS879A, SN74ALS878A, SN74ALS879A DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state	output
Operating free-air temperature range:	SN54ALS878A, SN54ALS879A 55 °C to 125 °C
	SN74ALS878A, SN74ALS879A 0°C to 70°C
Storage temperature range	

recommended operating conditions

				SN54ALS878A SN54ALS879A		,	74ALS8		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
IOL	Low-level output current				12			24	mA
£	Clock frequency	'ALS878A	0		25	0		30	MHz
^f clock		'ALS879A	0		20	0		25	
	Pulse duration	'ALS878A CLK high or low	20			16.5			
t _w	ruise duration	'ALS879A CLK high or low	25			20			ns
	Setup time	Data	15			15			
t _{su}	before CLK1	CLR	20			20			ns
+.	Hold time	Data	4			4			
٠h	th after CLK1	CLR	0			0			ns
TA	Operating free-air tempera	ture	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				N54ALS			74ALS8		
PARAMETER	TEST CONDITIONS		SI	V54ALS	879A	SN74ALS879A			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ĺ
VIK	$V_{CC} = 4.5 V,$	$I_I = -18 \text{ mA}$			- 1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	$5 \text{ V}, \text{ I}_{OH} = -0.4 \text{ mA}$	Vcc-	2		Vcc-	2		
Voн	$V_{CC} = 4.5 V$,	I _{OH} = -1 mA	2.4	3.3					\ \
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V	I _{OL} = 24 mA					0.35	0.5	ľ
lozh	$V_{CC} = 5.5 V$,	V _O = 2.7 V			20			20	μΑ
^I OZL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20			- 20	μΑ
l _l	$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA
IH	$V_{CC} = 5.5 V$,	V ₁ = 2.7 V			20			20	μΑ
IIL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.2			-0.2	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		- 112	mA
		Outputs high		14	23		14	23	
^I cc	$V_{CC} = 5.5 V$	Outputs low		18	31		18	31	mA
		Outputs disabled		20	33		20	33	l

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



SN54ALS878A, SN54ALS879A, SN74ALS878A, SN74ALS879A DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM	TO (OUTPUT)	C _L R1 R2 T _/	CC = \{	pF, 0 Ω, 0 Ω, 5°C	C F T SN544	$C_{CC} = 4.5$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega$ $R_{L} = 500 \Omega$ $R_{L} = MIN \text{ to}$ $R_{L} = 878A$ $R_{L} = 879A$	MAX SN74	V, ALS878A ALS879A	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	'ALS8'	78A	40	50		25		30		MHz
'max	'ALS8'	79A	40	50		20		25		101112
^t PLH	CLK	Q or Q		8	10	4	15	4	14	ns
tPHL	CLK	2012		9	13	4	17	4	16	115
^t PZH	oc	Q or $\overline{\mathbb{Q}}$		9	13	4	22	4	20	no
†PZL		2012		11	15	4	22	4	20	ns
[†] PHZ	oc	Q or $\overline{\Omega}$		6	8	2	12	2	10	ns
t _{PLZ}	00	0 01 0		7	10	3	18	3	15	IIS

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS878, SN54AS879, SN74AS878, SN74AS879 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operate	ting free-air temperature range (unless otherwise noted)
· •	
Operating free-air temperature range	SN54AS878, SN54AS879 55 °C to 125 °C
Storage temperature range	SN74AS878, SN74AS879 0°C to 70°C65°C to 150°C

recommended operating conditions

				SI	V54AS8	78	SN	74AS87	78		
				SN54AS879 SN74AS879		UNIT					
				MIN	NOM	MAX	MIN	NOM	MAX	ONII	
Vcc	Supply voltage			4.5	5	5.5	4.5	5	5.5	V	
\vee_{IH}	High-level input voltage			2			2			V	
VIL	Low-level input voltage				0.8			0.8	V		
ГОН	High-level output current					- 12			- 15	mA	
loL	Low-level output current					32			48	mA	
fclock	Clock frequency	Clock frequency		0		100	0		125	MHz	
t _w	Pulse duration	CLK low		4			2				
·W	- use duration	CLK high		5			4			ns	
	Setup time	Data		3			2				
t _{su}	before CLK1	CLR		6.5			5.5			ns	
	Hold time	Data		3			2				
th	after CLK1	CLR		0			0			ns	
T_A	Operating free-air tempera	iture		- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

					V54AS8			74AS87	-	
PARA	METER	TEST C	ONDITIONS	SI	V54AS8	79	SN	74AS87	79	UNIT
				MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}, I_{OH} = -2 \text{ mA}$		2		Vcc-	2		
∨он		$V_{CC} = 4.5 V$,	I _{OH} = -12 mA	2.4	3.2					1 v
		$V_{CC} = 4.5 V,$	I _{OH} = -15 mA				2.4	3.3		1
1/2:		$V_{CC} = 4.5 V$,	1 _{OL} = 32 mA		0.29	0.5				V
VOL		V _{CC} = 4.5 V	$I_{OL} = 48 \text{ mA}$					0.33	0.5	1 °
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			50			50	μΑ
lozL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 50			- 50	μΑ
Ч		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
lu	D	V _{CC} = 5.5 V,	V _I = 0.4 V			- 3			- 2	mA
ΊL	All other	VCC = 3.5 V,	V = 0:4 V			-0.5			-0.5	1 ''''
10‡		$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 30		~112	- 30		- 112	mA
			Outputs high		82	132		82	132	
	'AS878	,	Outputs low		96	155		96	155	1
		$V_{CC} = 5.5 V$,	Outputs disabled		100	160		100	160	
lcc		See Note 1	Outputs high		88	142		88	142	mA
	'AS879		Outputs low		94	150		94	150	
			Outputs disabled		100	160		100	160	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R1=500$ Ω , $R2=500$ Ω , $T_A=MIN$ to MAX		ν,	UNIT	
				SN54AS878 SN54AS879		NS878	1	
			MIN	MAX	SN74A MIN	MAX	1	
f _{max}			100		125		MHz	
^t PLH	CLK	Q or Q	3	11.5	3	8.5		
t _{PHL}	1 CLK	0 0 0	4	12.5	4	10.5	ns	
t _{PZH}	ōc	Q or Q	2	8	2	7		
tPZL t	1	u or u	d or d	[′] 3	11.5	3	10.5	ns
^t PHZ	oc	Q or Q	2	7	2	6	ns	
t _{PLZ}	7 ~~	1 2010	2	7	2	6	118	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CC} is measured with CLR and all D inputs grounded, and CLK and OC at 4.5 V.

SN54ALS880A, SN54AS880, SN74ALS880A, SN74AS880 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982 - REVISED MAY 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- 'ALS873B is Alternative Version with Noninverting Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These dual 4-bit registers feature three-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the $\overline{\Omega}$ outputs will follow the data (D) inputs in inverted form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When \overline{PRE} goes low, the $\overline{\Omega}$ outputs go low independently of the clock. The outputs are in a high-impedance state when \overline{OC} (output control) is at a high logic level.

The SN54ALS880A and SN54AS880 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS880A and SN74AS880 are characterized for operation from 0 °C to 70 °C.

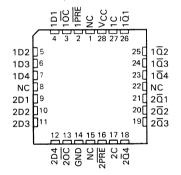
FUNCTION TABLES (EACH LATCH)

	. IN	PUTS		ОИТРИТ
ОC	PRE	ENABLE C	D	ã
L	L	X	Х	L
L	Н	н	Н	L
L	Н	н	L	н
L	н	L	×	\bar{a}_0
Н	X	Х	Х	Z

SN54ALS880A, SN54AS880 . . . JT PACKAGE SN74ALS880A, SN74AS880 . . . DW OR NT PACKAGE (TOP VIEW)

1PRE	1	U 24	þ	۷c	С
10C	2	23	р	1C	
1D1 🗀	3	22	Р	10	1
1D2 🗌	4	21	р	10	2
1D3 🗌	5	20	р	10	3
1D4 🗌	6	19	р	10	
2D1 🗌	7	18		20	1
2D2 🗌	8	17		20	2
2D3 🗌	9	16		20	3
2D4 🗌	10	15	D	20	4
20C	11	14		2C	
GND [12	13	р	2P	RE

SN54ALS880A, SN54AS880 . . . FK PACKAGE SN74ALS880A, SN74AS880 . . . FN PACKAGE (TOP VIEW)

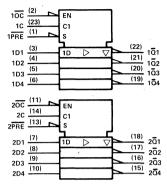


NC-No internal connection



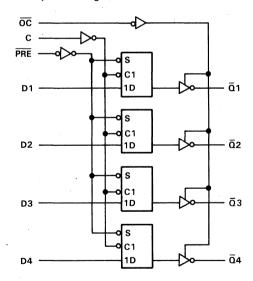
SN54ALS880A, SN74AS880, SN74ALS880A, SN74AS880 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

logic symbol†



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

logic diagram (each quad latch, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS880A, SN54AS880
SN74ALS880A, SN74AS880 0 °C to 70 °C
Storage temperature range65°C to 150°C



SN54ALS880A, SN74ALS880A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN	54ALS	380A	SN	74ALS8	80A	UNIT
			 MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltag	е	2			2			V
VIL	Low-level input voltage	9			0.7			0.8	V
ЮН	High-level output curre	nt			- 1			-2.6	mA
lOL	Low-level output curre	nt			12			24	mA
	Pulse duration	PRE low	15			15			ns
tw	ruise duration	Enable C high	15			15			115
t _{su}	Setup time, data befor	e enable C↓	10			10			ns
th	Hold time, data after e	nable C↓	10			10			ns
TA	Operating free-air temp	perature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT (CONDITIONS	SN	54ALS	380A	SN	UNIT		
PARAMETER	IESI C	CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to 5}.$	5 V, I _{OH} = -0.4 mA	V _{CC} -	2		V _{CC} -	2		
Voн	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5]
lozн	$V_{CC} = 5.5 V$,	V _O = 2.7 V			20			20	μΑ
lozL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20			- 20	μΑ
11	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
JiL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.2			-0.2	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
		Outputs high		14	21		14	21	
^I CC	$V_{CC} = 5.5 V$	Outputs low		19	29		19	29	mA
		Outputs disabled		20	31		20	31	1

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS880A, SN74ALS880A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	C _L R1 R2 T _A	= 50 = 500 = 500 = 500 = 25	pF, Ο Ω, Ο Ω, °C	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω = 500 Ω = MIN to	MAX	, LS880A	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	D	ā		14	19	3 -	23	3	20	ns
^t PHL	U	Q.		9	12	3	15	3	14] '''
. tplh	С	ā		17	22	8	31	8	24	ns
tPHL	C			14	18	8	22	8	21	113
tPHL	PRE	ā		12	16	6	24	6	21	ns
^t PZH	ōc	α		12	15	4	21	4	18	
^t PZL	OC.	u		13	17	4	2.1	4	18	ns
^t PHZ	ōc	. <u>a</u>		6	9	2	12	2	10	ns
^t PLZ	50	· ·		8	11	3	21.	3	17] ''5

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS880, SN74AS880 **DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS**

recommended operating conditions

				N54AS	880	SN	74AS8	80	UNIT
			MI	NON	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.	5 5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage			2		2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				-12			- 15	mA
loL	Low-level output current				32			48	mA
	Pulse duration	PRE low	4.	5		3.5			
t _w	Pulse duration	Enable C high		4		2.5			ns
t _{su}	Setup time, data before er	nable C↓		2		2			ns
th	Hold time, data after enab	le C↓		1		1			ns
TA	Operating free-air tempera	ture	- 5	5	125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEGT OF	NIDITIONIO	SN54	AS880	SN	74AS8	80	UNIT
PARAMETER	TEST CC	ONDITIONS	MIN TY	P [†] MA	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA		- 1.:	2		-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -2 \text{ mA}$	V _{CC} - 2		Vcc-	- 2		
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2.4	3.2				V
	$V_{CC} = 4.5 V,$	I _{OH} = -15 mA			2.4	3.3		1
V	$V_{CC} = 4.5 V,$	I _{OL} = 32 mA	0	.30 0.	5		-	V
VOL -	V _{CC} = 4.5 V,	I _{OL} = 48 mA				0.35	0.5	1 °
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$		5)		50	μΑ
lozL	$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$		- 5)		- 50	. μΑ
l _l	$V_{CC} = 5.5 V,$	V ₁ = 7 V		0.	1		0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V		2)		20	μΑ
ΊL	$V_{CC} = 5.5 V,$	V _I = 0.4 V		-0.	5		-0.5	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30	- 11:	2 -30		-112	mA
		Outputs high		73 11	3	73	118	
lcc l	$V_{CC} = 5.5 V$	Outputs low		76 12	2	76	122	mA
		Outputs disabled		86 13	7	86	137	1

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CNE	$V_{CC} = 4.5$ $C_{L} = 50 \text{ pf}$ $R1 = 500 \text{ s}$ $R2 = 500 \text{ s}$ $T_{A} = MIN$	=, Ω, Ω, to MAX	5 V,	UNIT
			MIN	MAX	MIN	MAX	
tPLH	D	ā	4	11	4	9.5	
^t PHL	U	u .	4	9	4	8.5	ns
tPLH	С	ā	6	14	6	11.5	ns
^t PHL		4	4	10	4	8	115
tPHL	PRE	ā	4	11.5	4	10	ns
^t PZH	ōc	ā	2	8	2	7.5	ns
tPZL		<u> </u>	4	11	4	10	115
^t PHZ	οc	ā	2	. 8	2	6.5	ns
^t PLZ		<u> </u>	2	9	2	8	113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2661, DECEMBER 1982 - REVISED MAY 1986

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Full Look-Ahead for High-Speed Operations on Long Words
- **Arithmetic Operating Modes:**

Addition

Subtraction

Shift Operand A One Position

Magnitude Comparison

Plus Twelve Other Arithmetic Operations

Logic Function Modes

Exclusive-OR

Comparator

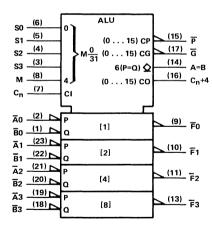
AND, NAND, OR, NOR

'AS881A Provides Status Register Checks

Plus Ten Other Logic Operations

Dependable Texas Instruments Quality and Reliability

logic symbol†



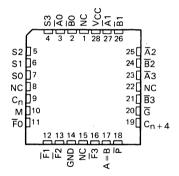
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for DW, JT, and NT packages

SN54AS181A . . . J OR JT PACKAGE SN54AS881A . . . JT PACKAGE SN74AS181A . . . N OR NT PACKAGE SN74AS881A . . . DW OR NT PACKAGE (TOP VIEW)

50	╓	U 24	h
BO	ч'	O 24	⊔ ∨сс
ĀΟ	□2	23	□ Ā1
S3	Πз	22	□ <u>B</u> 1
S2	□4	21	□ Ā2
S1	∏ 5	20	<u>B</u> 2
S0	∏ 6	19	<u></u> ⊼з
c_n	D٦	18	<u>B</u> 3
М	[]8	17	□ē
FΟ	[]9	16	Cn+4
F1	∐ 10	15	ĪĒ
F2	□ 11	14] A = B
GND	∐ 12	13	

SN54AS181A, SN54AS881A . . . FK PACKAGE SN74AS181A, SN74AS881A . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

For complete information on the SN54AS881A and the SN74AS881A, see page 2-187.



SN54AS882A, SN74AS882A 32-BIT LOOK-AHEAD CARRY GENERATORS

D2661, DECEMBER 1982 - REVISED NOVEMBER 1985

- Directly Compatible with 'AS181B. 'AS1181, 'AS881B, and 'AS1881 ALUs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Capable of Anticipating the Carry Across a Group of Eight 4-Bit Binary Adders
- Cascadable to Perform Look-Ahead Across n-Bit Adders
- Typical Carry Time, C_n to Any C_{n+i}, is Less Than 6 ns
- Dependable Texas Instruments Quality and Reliability

description

The 'AS882A is a high-speed look-ahead carry generator capable of anticipating the carry across a group of eight 4-bit adders permitting the designer to implement look-ahead for a 32-bit ALU with a single package or, by cascading 'AS882A's, full look-ahead is possible across n-bit adders.

The SN54AS882A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS882A is characterized for operation from 0°C to 70°C.

'AS882A LOGIC EQUATIONS

 $C_{n+8} = G1 + P1G0 + P1P0C_n$

 $C_{n+16} = G3 + P3G2 + P3P2G1 + P3P2P1G0$

+P3P2P1P0Cn

 $C_{n+24} = G5 + P5G4 + P5P4G3 + P5P4P3G2$

+P5P4P3P2G1+P5P4P3P2P1G0 +P5P4P3P2P1P0Cn

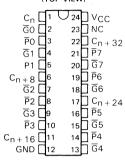
 $C_{n+32} = G7 + P7G6 + P7P6G5 + P7P6P5G4$

+P7P6P5P4G3+P7P6P5P4P3G2

+P7P6P5P4P3P2G1+P7P6P5P4P3P2P1G0

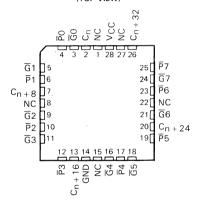
+P7P6P5P4P3P2P1P0Cn

SN54AS882A . . . JT PACKAGE SN74AS882A . . . DW OR NT PACKAGE (TOP VIEW)



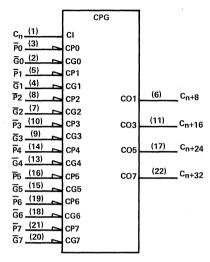
SN54AS882A . . . FK PACKAGE SN74AS882A . . . FN PACKAGE

(TOP VIEW)



NC No internal connection

logic symbol†



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE FOR Cn + 32 OUTPUT

										NPUT	s							OUTPUT
	Ğ7	Ğ6	Ğ5	G4	Ğ3	Ğ2	G1	ĞΟ	Ē7	P6	P5	P4	P3	P2	P1	P0	Cn	C _{n+32}
	L	Х	Х	Х	Х	X	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	н .
	X	L	X	Χ	X	Х	X	Χ	L	Х	Х	Х	Х	X	Х	Х	X	н
1	X	X	L	X	X	X	X	Χ	L	L	X	Х	Χ	X	Х	Х	X	н
	Х	Х	Х	L	X	Х	X	Χ	L	Ĺ	L	Х	Χ	Χ	Χ	Χ	Χ	н
	Х	Х	Х	Х	L.	X	Х	Χ	L	L	L	L	Х	Х	Χ	Х	X	н
İ	X	Х	Х	X	X	L	X	X	L	L	L	L	L	Х	X	Χ	X	н
	Х	Х	Х	X	X	X	L	Χ	L	L	L	L	L	L	Х	Х	Χ	н
	Χ	Х	Х	Х	Х	X	Χ	L	L	L	L	L	L	L	L	Х	Χ	н
	Х	Х	Х	Х	X	X	X	Х	L	L	L	L	L.	L.	L	Ł	Н	н
								Α	II othe	r comb	oination	าร						L

FUNCTION TABLE FOR Cn + 24 OUTPUT

					l.	NPUTS							OUTPUT
Ğ5	G4	G3	G2	Ğ1	Ğ0	P̄5	P4	P3	P2	P1	₽0	Cn	Cn + 24
L	Х	Х	X	X	Х	Х	X	X	X	Х	X	X	Н
X	L	X	X	X	X	L	X	X	X	X	X	X	н
×	X	L	X	X	X	L	L	X	X	X	X	X	Н
X	X	×	L	×	X	L	L	L	×	×	X	X	Н
x	X	X	Х	L	· X	L	L	Ł	L	X	Х	Х	н
X	X	X	X	X	L	L	L	L	L	L	X	Х	н
x	×	X	Х	Х	X	L	L	L	L	L	L	н	Н
					All o	ther com	binations	;					L

FUNCTION TABLE FOR Cn + 16 OUTPUT

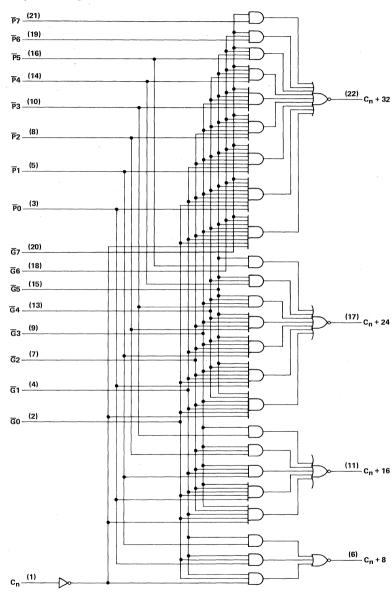
				INF	UTS				OUTPUT
ĞЗ	Ĝ2	Ğ1	Ğ0	P3	P2	P1	ΡO	Cn	C _{n+16}
L	Х	Х	Х	X	Х	Х	Х	Х	Н
Χ	L	Х	Х	L	Х	Х	Х	X	ј н
Х	Х	L	Х	L	L	X	Х	X	н
Х	Х	Х	L	L	L	L	Х	X	H
Х	·X	Х	X	L	L	L	L	Н	н
		ΑII	othe	r con	nbina	tions			L

FUNCTION TABLE FOR Cn+8 OUTPUT

	If	OUTPUT			
G1	Ğ0	P1	P0	Cn	Cn+8
L	Х	X	Х	Х	H ·
X	L	L	X	×	Н
Х	X	L	L	Н	н
	All oth	er con	nbinatio	ons	L

Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



SN54AS882A, SN74AS882A 32-BIT LOOK-AHEAD CARRY GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	
Operating free-air temperature range:	SN54AS882A
	SN74AS822A
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN	SN54AS882A				SN74AS882A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT		
Vcc	Supply voltage	4.5	5	5.5	4.5	- 5	5.5	V		
V _{IH} .	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.8			0.8	V		
ГОН	High-level output current			- 2			-2	mA		
lor	Low-level output current			20			20	mA		
TA	Operating free-air temperature	- 55		125	0		70	°C		



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA.	DAMETED	TECT C	ONDITIONS	SN	54AS88	32A	SN74AS882A			UNIT		
PAI	RAMETER	TEST C	UNDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX			
VIK		$V_{CC} = 4.5 V,$	$I_1 = -18 \text{ mA}$			- 1.2			-1.2	V		
Voн			$5.5 \text{ V, I}_{OH} = -2 \text{ mA}$	V _{CC} -			V _{CC} -2			V		
VOL	,	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	. V		
	C _n , PO, P1					0.4			0.4			
	Ğ0, Ğ6	ļ				0.8			0.8			
1 .	G1, G2, G4					1.2			1.2			
11	<u>G</u> 3, <u>G</u> 5	V _{CC} = 5.5 V,	V1 = 7 V			1.5			1.5	mA		
''	Ğ7	VCC = 5.5 V,				0.9			0.9			
'	₽2, ₽3					0.3			0.3			
	₽4, ₽5					0.2			0.2			
-	₱6, ₱7					0.1			0.1			
	C _n , PO, P1					80			80			
1	<u>G</u> 0, <u>G</u> 6					160			160	0		
]	<u>G</u> 1, <u>G</u> 2, <u>G</u> 4	1				240			240	ı		
1.	G3, G5	1	V ₁ = 2.7 V			300			300			
۱н	G7	VCC = 5.5 V				180			180	μA		
. 1	Ē2, Ē3			60			60			60		
	₽4, ₽5	1				40			40	10		
1	₽6, ₽7			20					20	,		
	C _n , ₱0, ₱1					- 2			- 2			
	<u>G</u> 0, <u>G</u> 6	1 .				-4			- 4			
	G1, G2, G4	1				- 6		- 6				
	<u>G</u> 3, <u>G</u> 5	1				- 7.5			- 7.5			
IIL .	G7	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-4.5			-4.5	mA		
	P2, P3	1				-1.5			- 1.5			
	P4, P5					- 1			- 1			
	P6, P7	1			-0.5			-0.5				
10 [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		- 130	- 30		- 130	mA		
Icc		V _{CC} = 5.5 V		1	44	70		44	70	mA		
		·					L			·		

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS822A \qquad SN74AS882A$					
			MIN	MAX	MIN	MAX			
^t PLH	6	A	2	10	2	9			
^t PHL	C _n	Any output	3	15	3	14			
^t PLH	P or G	<u> </u>	2	8	2	7			
^t PHL	F 01 G	C _{n+8}	2	8	2	7			
^t PLH	PorG	C _{n+16}	2	8	2 .	7	ns		
^t PHL		℃n + 16	2	8	2	7	115		
^t PLH	P or G		. 2	8	2	7			
^t PHL	Pord	C _{n + 24}	2	11	2	10			
^t PLH	P or G	C _{n+32}	1.5	9	2	8			
tPHL	1 01 0	○n + 32	2	13	2	12			

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The application given in Figure 1 illustrates how the 'AS882A can implement look-ahead carry for a 32-bit ALU (in this case, the popular 'AS881A) with a single package. Typical carry times shown are derived using the standard Advanced Schottky load circuit.

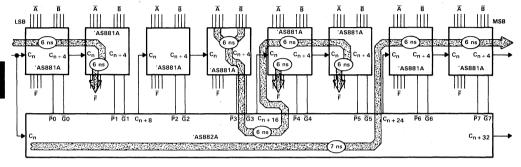


FIGURE 1

Likewise, Figure 2 illustrates the same 32-bit ALU using two 'AS882s. This shows the worst-case delay from LSB to MSB to be 19 ns as opposed to 25 ns in Figure 1.

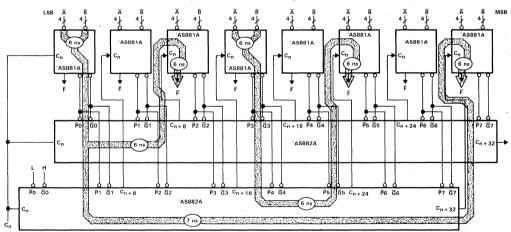


FIGURE 2

SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

D2661, DECEMBER 1982 REVISED MARCH 1985

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Latchable P Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (2's Complement) Comparison
- Data and PLE Inputs Utilize P-N-P Input Transistors to Reduce DC Loading Effects
- Approximately 35% Improvement in AC Performance Over Schottky TTL while Performing More Functions
- Cascadable to n-Bits while Maintaining High Performance
- 10% Less Power than STTL for an 8-Bit Comparison
- Dependable Texas Instruments Quality and Reliability

description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. The P > Q and P < Q outputs of a stage handling less-significant bits may be connected to the P > Q and P < Q inputs of the next stage handling more-significant bits to obtain comparisons of words of longer lengths. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in the typical application data.

SN54AS885 . . . JT PACKAGE SN74AS885 DW OR NT PACKAGE (TOP VIEW) U24∐ VCC L/Ā 🔲 ī 23 PLE P < OIN [P > OIN 22 P7 21 P6 07 🗆 20 P5 06 [Q5 **[**6 19 P4 18 P3 0.4 Q3 **∏**8 17 P2 16∏ P1 Ω2 [

SN54AS885 FK PACKAGE SN74AS885 FN PACKAGE (TOP VIEW)

10

ο1 Γ

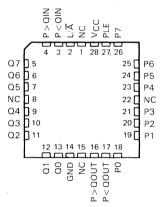
00 🗆 11

GND ∏12

15 PO

14∏ P < QOUT

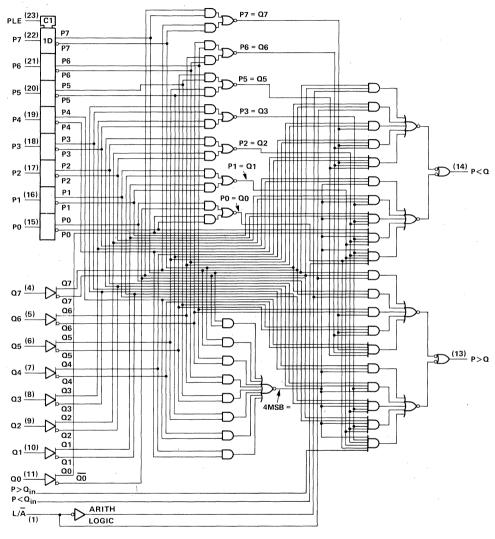
13 P > 00UT



The latch is transparent when P Latch Enable (PLE) is high; the P input port is latched when PLE is low. This provides the designer with temporary storage for the P data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE and P and Q data inputs utilize p-n-p input transistors to reduce the low-level current input requirement to typically –0.25 mA, which minimizes dc loading effects.

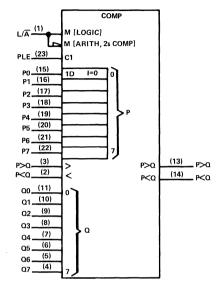
The SN54AS885 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74AS885 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE

COMPARISON	L/Ā	DATA INPUTS	INPUT	INPUT	OUTI	PUTS
CONFANISON	L/A	P0-P7, Q0-Q7	P>Q	P <q< th=""><th>P>Q</th><th>P<q< th=""></q<></th></q<>	P>Q	P <q< th=""></q<>
LOGICAL	Н	P>Q	Х	Х	Н	L
LOGICAL	Н	P < Q ·	Х	Х	L	н
LOGICAL [‡]	Н	P = Q	HORL	H OR L	HORL	H OR L
ARITHMETIC	L	P AG Q	Х	X	Н	L
ARITHMETIC	L	QAGP	Х	X	L	Н
ARITHMETIC [‡]	L	P = Q	H OR L	H OR L	HORL	H OR L

 $^{^{\}ddagger}$ In these cases the P>Q output will follow the P>Q input, and the P<Q output will follow the P<Q input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		 	7 V
Input voltage		 	7 V
Operating free-air temperature range:	SN54AS885	 	-55°C to 125°C
	SN74AS885	 	0°C to 70°C
Storage temperature range		_	-65°C to 150°C

AG - arithmetically greater than

SN54AS885, SN74AS885 **8-BIT MAGNITUDE COMPARATORS**

recommended operating conditions

	PARAMETER	S	SN54AS885 SN74AS885							
ŀ	FANAIVIETEN	MIN	MIN NOM MAX		MIN	NOM	MAX	UNIT		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
VIH	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.8			0.8	V		
Тон	High-level output current			- 2			- 2	mA		
loL	Low-level output current			20			20	mA		
t _{su}	Setup time to PLE↓	2			2					
th	Hold time after PLE↓	4			4			ns		
TA	Operating free-air temperature	- 55		125	0		70	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-	ARAMETER	TEST CO	UDITIONS	SN54AS	885	SN	74AS8	85	
	Analvic I ch	1231 CO	NDITIONS	MIN TYP1	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA		- 1.2			-1.2	V
∨он		$V_{CC} = 4.5 \text{ to } 5.5 $	/, I _{OH} = −2 mA	V _{CC} – 2		Vcc-	2		V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 20 mA	0.35	0.5		0.35	0.5	V
կ		$V_{CC} = 5.5 V_{c}$	V ₁ = 7 V		0.1			0.1	μΑ
1	L/Ā	$V_{CC} = 5.5 V_{c}$	$S = 5.5 \text{ V}, \qquad V_1 = 2.7 \text{ V}$		40			40	_
ЧΗ	Others	ACC = 2.2 A'	V = 2.7 V		20			20	μΑ
	L/Ā				- 4			- 4	
١.	P > Q _{in}	.,							
IL	P < Q _{in}	$V_{CC} = 5.5 V$,	VI = 0.4 V		2	- 2		- 2	mA
	P. Q. PLE				- 1			- 1	
10‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 20 ·	- 112	- 20		- 112	mA
Icc		$V_{CC} = 5.5 V$	See Note 1	130	210		130	210	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCI CL RL TA SN54AS	85	UNIT		
			MIN TYP†	MAX	MIN TYP [†]	MAX]
tPLH .	LA		8.5	14	8.5	13	ns
^t PHL	LA		7.5	14	7.5	13	115
^t PLH	P < Q _{in}	P < Q,	5	10	5	8	nc
tPHL	P > Qin	P > Q	5.5	10	5.5	8	ns
tpLH	Any P or Q	, ·	13.5	21	13.5	17.5	ns
tPHL	Data Input		10	17	10	15	115

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{\circ}C.$

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}. NOTE 1: I_{CC} is measured with all inputs high except L/\overline{A} , which is low.

TYPICAL APPLICATION DATA

The 'AS885 can be cascaded to compare words longer than 8-bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n-bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25 °C, and use the standard Advanced Schottky load of $R_L = 500 \Omega$, $C_L = 50 pF$.

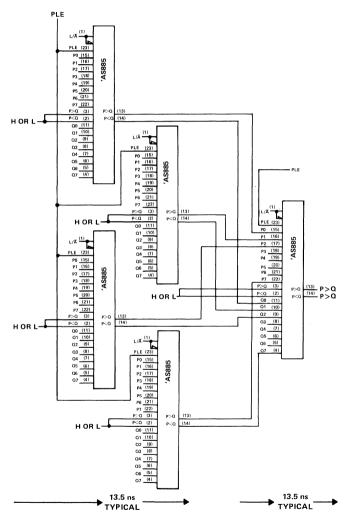


FIGURE 1. 32-BIT TO 72 (N)-BIT MAGNITUDE COMPARATOR

TYPICAL APPLICATION DATA

The method shown in Figure 2 is the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at $V_{CC}=5$ V, $T_{A}=25$ °C, and use the standard Advanced Schottky load of $R_{L}=500$ Ω , $C_L = 50 pF$.

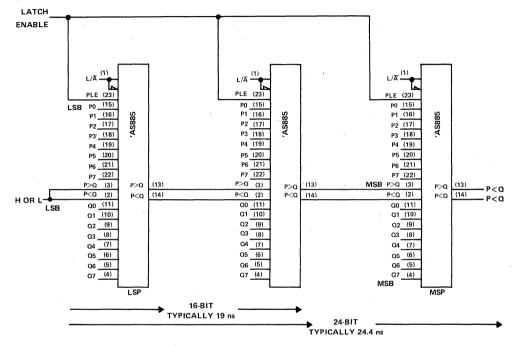


FIGURE 2

SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

D2881, NOVEMBER 1985-REVISED MAY 1986

- Serial-to-Parallel and Parallel-to-Serial Conversions
- Parallel I/O Registers
- Data Exchangeable Between I/O Register and Shift Register
- Choice of Synchronous and/or Asynchronous Clear
- Independent or Dual Register Clocking
- Functionally Similar to National Semiconductor DM74LS962
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'ALS963 and 'ALS964 each contain an 8-bit shift register in parallel with an 8-bit I/O register. In addition to serial-to-parallel and parallel-to-serial conversions, these devices are capable of exchanging data between the shift and I/O registers. Control lines determine the mode of operation as shown in the function table.

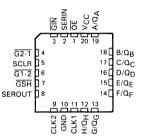
The 'ALS963 features individual shift and I/O register clock inputs whereas the 'ALS964 features simultaneous register clocking through a single clock input. Clocking in both cases is achieved by positive transitions at the clock inputs.

The clear function for the 'ALS963 is synchronous (active high). The 'ALS964 features active-high synchronous and asynchronous clearing.

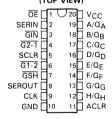
The SN54ALS963 and SN54ALS964 are characterized for operation over the full military of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS963 and SN74ALS964 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS963 . . . JT PACKAGE SN74ALS963 . . . DW OR NT PACKAGE (TOP VIEW) OE TI U20 VCC SERIN 2 19 A/QA GIN □3 18 B/QB G2-1 17 C/QC 16 D/QD SCLR ∏5 G1-2 76 15 E/QE GSH 7 14 F F/QE SEROUT 18 13 G/QG CLK2 TI9 12 H/QH GND 10 11 CLK1

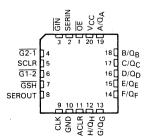
SN54ALS963 . . . FK PACKAGE (TOP VIEW)



SN54ALS964 . . . JT PACKAGE SN74ALS964 . . . DW OR NT PACKAGE (TOP VIEW)



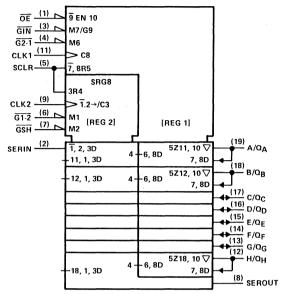
SN54ALS964 . . . FK PACKAGE (TOP VIEW)





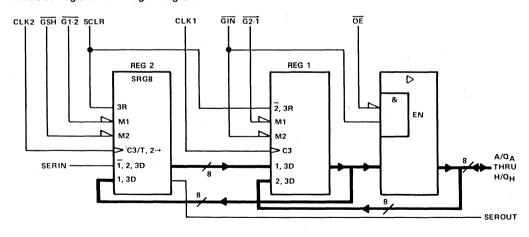
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'ALS963 logic symbol[†]

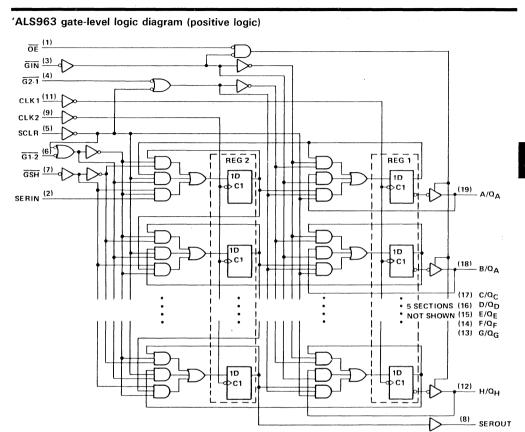


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS963 register-level logic diagram



SN54ALS963, SN74ALS963 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS



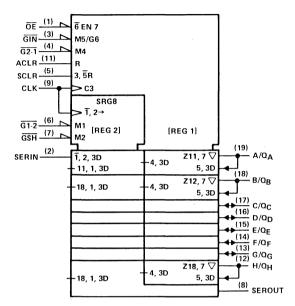


'ALS963 FUNCTION TABLE

			IN	PUTS				A/QA THROUGH	OPERATION OR FUNCTION
ŌĒ	GIN	GE-1	G1-2	GSH	CLK1	CLK2	SCLR	H/QH	OPERATION OR FUNCTION
Н	Н	Н	Н	Н	X	×	L	HI-Z	All data stable
L	Н	н	Н	Н	Х	X	L	OUTPUT	All data stable
X	L	Н	Н	Η,	1	X	L	INPUT	Enter data from I/O into Reg 1
Н	Н	L	Н	Н	1	X	L	HI-Z	Copy data from Reg 2 to Reg 1
L	Н	L	Н	Н	1	X	L	OUTPUT	Copy data from Reg 2 to Reg 1
X	L	L	н	Н	1	1	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
Н	Н	Н	L	Х	X	1	L	HI-Z	Copy data from Reg 1 to Reg 2
L	Н	Н	Ł	Χ	X	1	L	OUTPUT	Copy data from Reg 1 to Reg 2
X	L	н	L	Χ	1	1	L	INPUT	Copy data from Reg 1 to Reg 2,
									enter new data from I/O into Reg 1
Н	Н	L	L	Χ	1	1	L	HI-Z	Exchange data between registers
L	Н	L	L	Χ	1	1	L	OUTPUT	Exchange data between registers
Х	L	L	L	Χ	1	1	L	INPUT	Copy data from Reg 1 to Reg 2,
									Reg 1 ORs data from Reg 2 and I/O
Н	Н	Н	Н	L	X	1	L	HI-Z	Shift data in Reg 2
L	Н	Н	Н	L	X	1	L	OUTPUT	Shift data in Reg 2
X	L	Н	Н	L	1	1	L	INPUT	Shift data in Reg 2, enter new data
_									from I/O into Reg 1
Н	Н	L	Н	Ĺ	1	1	L	HI-Z	Copy data from Reg 2 to Reg 1,
									shift data in Reg 2
L	H-	Ļ	н	. L	1	1	L	OUTPUT	Copy data from Reg 2 to Reg 1,
									shift data in Reg 2
X	L	L	Н	L	1	1	L	INPUT	Reg 1 ORs data from Reg 2 and I/O,
									shift data in Reg 2
X	Н	×	Χ.	Х	1	X	Н		Synchronously clear Reg 1
X	X	×	×	Χ	X	Ť	Н		Synchronously clear Reg 2
Х	Н	Χ	Х	Χ	1	1	Н		Synchronously clear both registers
Х	L	X	X	X	1	Ť	Н	INPUT	Enter data from I/O into Reg 1 and
									synchronously clear Reg 2
X	L	×	X	×	1	X	Н	INPUT	Enter data from I/O into Reg 1

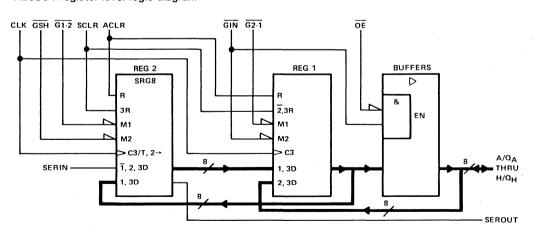
SN54ALS964, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS964 logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS964 register-level logic diagram



'ALS964 gate-level logic diagram (positive logic) OE (1) (4) G2-1 CLK (9) ACLR (11) SCLR (5) REG 2 REG 1 1D (19) A/QA SERIN (2) (18) B/QB c/qc D/QD • 5 SECTIONS NOT SHOWN (15) E/QE (14) F/QF (13) G/QG (12) H/QH

(8) SEROUT

SN54ALS964, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

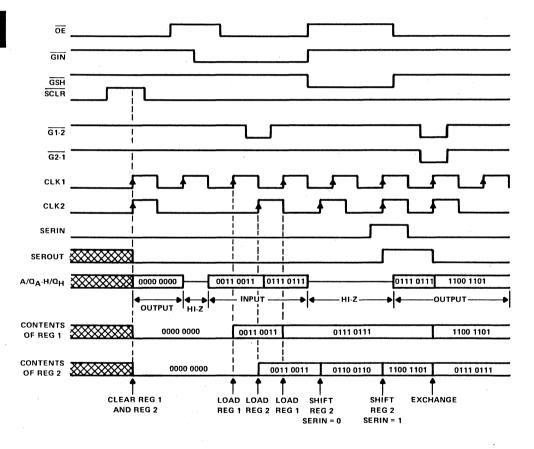
'ALS964 **FUNCTION TABLE**

			IN	PUTS				A/QA THROUGH	OPERATION OR FUNCTION
ŌĒ	GIN	G2-1	G1-2	GSH	CLK	ACLR	SCLR	H/QH	OPERATION OR FUNCTION
Н	Н	Н	Н	Н	X	<u>-</u>		HI-Z	All data stable
L	Н	Н	Н	Н	X	L	L	OUTPUT	All data stable
X		Н	Н	Н	^ ↑	_	-	INPUT	Enter data from I/O into Reg 1
	H		<u></u>		<u>_</u>	L	<u>L</u>	HI-Z	Copy data from Reg 2 to Reg 1
Н.		L	Н	Н		L .	L	OUTPUT	''
L	H	L			1	L	L		Copy data from Reg 2 to Reg 1
X	L	L	Н.	H	1	<u> </u>	L	INPUT	Reg 1 ORs data from Reg 2 and I/O
Н	Н	Н	L	X	1	L	L	HI-Z	Copy data from Reg 1 to Reg 2
L	Н	Н	L	X	1	L	L	OUTPUT	Copy data from Reg 1 to Reg 2
Х	L	Н	L	Х	1	L	L	INPUT	Copy data from Reg 1 to Reg 2,
									enter new data from I/O into Reg 1
Н	Н	L	L	X	1	L	L	HI-Z	Exchange data between registers
L	Н	L	L	X	1	L	Ĺ	OUTPUT	Exchange data between registers
Х	L	L	L	X	1	L	L	INPUT	Copy data from Reg 1 to Reg 2,
									Reg 1 ORs data from Reg 2 and I/O
Н	Н	Н	Н	L	1	L	L	HI-Z	Shift data in Reg 2
L	Н	Н	Н	L	1	L	L	OUTPUT	Shift data in Reg 2
Х	L	н	Н	L	1	L	L	INPUT	Shift data in Reg 2, enter new data
									from I/O into Reg 1
Н	Н	L	Н	L	1	L	L	HI-Z	Copy data from Reg 2 to Reg 1,
									shift data in Reg 2
L	Н	L	н	L	†	L	L	ОИТРИТ	Copy data from Reg 2 to Reg 1,
									shift data in Reg 2
x	L	L	н	L	1	L	L	INPUT	Reg 1 ORs data from Reg 2 and I/O,
-									shift data in Reg 2
×	Н	X	X	X	1	L	Н		Synchronously clear Reg 1 and Reg 2
X	X	X	X	×	X	н	X		Asynchronously clear Reg 1 and Reg 2
X	L	X	X	Х	1	L	Н	INPUT	Enter data from I/O into Reg 1 and
l	-	,,				-			synchronously clear Reg 2

'ALS963 typical sequence

Illustrated below is the following sequence:

- 1. Clear both registers to zero.
- Input 0011 0011 in Reg 1.
 Transfer 0011 0011 from Reg 1 to Reg 2.
- 4. Input 0111 0111 into Reg 1.
- 5. Shift contents of Reg 2, SERIN = 0
- 6. Shift contents of Reg 2, SERIN = 1
- 7. Exchange contents of Reg 1 with Reg 2.

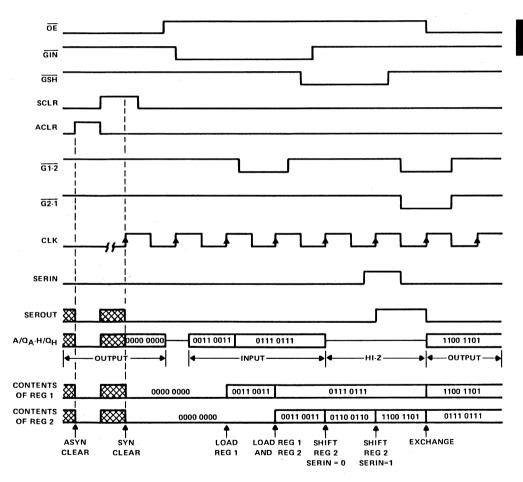


SN54ALS964, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS964 typical sequence

Illustrated below is the following sequence:

- 1. Asynchronously clear Reg 1 and Reg 2 to zero, operate, then synchronously clear.
- 2. Input 0011 0011 into Reg 1.
- 3. Transfer 0011 0011 from Reg 1 to Reg 2 and input 0111 0111 into Reg 1.
- 4. Shift contents of Reg 2, SERIN = 0
- 5. Shift contents of Reg 2, SERIN = 1
- 6. Exchange contents of Reg 1 with Reg 2.



SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC
Input voltage: All inputs
I/O ports
Operating free-air temperature range: SN54ALS963, SN54ALS964 55 °C to 125 °C
SN74ALS963, SN74ALS964 0 °C to 70 °C
Storage temperature range -65°C to 150°C

'ALS963 recommended operating conditions

			SN	154ALS	963	SN	74ALS	963	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 1			-2.6	mA
1		SEROUT			8			16	mA
lOL	Low-level output current	Q _A thru Q _H			12			24	mA
f _{clock}	Clock frequency (at 50%	duty cycle)	0		25	0		25	MHz
	Pulse duration	CLK1 high or low	20			20			
tw		CLK2 high or low	20			20			ns
		Data before CLK1↑							
		GIN before CLK1↑							
	Setup time	G1-2 before CLK2↑							ns
t _{su}	Setup time	G2-1 before CLK11							113
		GSH before CLK2↑							
		SCLR before CLK1↑ or CLK2↑							
th	Hold time after CLK1↑ or	CLK2↑							ns
TA	Operating free-air tempera	ature	- 55		125	0		70	°C

'ALS964 recommended operating conditions

			SN	54ALS	964	SN	74ALS	964	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0.8			0.8	٧
Іон	High-level output current				- 1			-2.6	mΑ
1	Low-level output current	SEROUT			8			16	mA
lOL	Low-level output current	Q _A thru Q _H			12			24	
f _{clock}	Clock frequency (at 50%	duty cycle)	0		25	0		25	MHz
	Pulse duration	CLK high or low	20			20			ns
t _W		ACLR low							ns
		Data before CLK↑							
		GIN before CLK1							
	Setup time	G1-2 before CLK↑							ns
t _{su}	Setup time	G2-1 before CLK↑							113
		GSH before CLK↑] .
		SCLR before CLK1							ĺ
th	Hold time after CLK↑								ns
TA	Operating free-air tempera	ature	- 55		125	0		70	°C



SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964 **DUAL RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D.	ARAMETER	TEST CONDITION	ONE	1	54ALS			74ALS9		UNIT
	ANAME I EN	TEST CONDITION	5115		TYP†			TYP		01111
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5	1		- 1.5	V
		V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -0.4 mA	Vcc-	2		Vcc	- 2		
v_{OH}		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					1 v
		$V_{CC} = 4.5 V,$	I _{OH} = -2.6 mA				2.4	3.2		
	SEROUT	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA		0.25	0.4		0.25	0.4	
Vol	SENOOT	$V_{CC} = 4.5 V,$	I _{OL} = 16 mA					0.35	0.5] ,
VOL	Q _A thru Q _H	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4]
	da tilla de	$V_{CC} = 4.5 V,$	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
lı	A thru H	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA
'1	Any other	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	l IIIA
lн‡		$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			20			20	μА
ا _{ال} ‡		V _{CC} = 5.5 V,	V ₁ = 0.4 V			-0.1			-0.1	mA
IO§		$V_{CC} = 5.5 V,$	V _O ≈ 2.25 V	- 30		-112	- 30		- 112	mA
			Outputs high							
	'ALS963	V _{CC} = 5.5 V	Outputs low							mA
loo			Outputs disabled]
¹cc			Outputs high							
	'ALS964	V _{CC} = 5.5 V	Outputs low							mA
			Outputs disabled							

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25\,^{\circ}$ C.

[‡]For I/O ports (Q_A throuh Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS963, SN54ALS964, SN74ALS963, SN74ALS964 DUAL-RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

'ALS963 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$					
				54ALS963 TYP [†] MAX	SN74ALS963 MIN TYP [†] MAX			ļ
			MIN	IYP' MAX	MIN	TYP	WAX	
f _{max}	CLK1 or CLK2	Any Q	25	30	25	30		MHz
^t PLH	0.44			10		10		
t _{PHL}	CLK1	Any Q		14				ns
tPLH	01.10	OFFICIAL		10		10		
t _{PHL}	CLK2	SEROUT		14		14		ns
t _{PHZ}	ŌĒ	40		15		15		
[†] PLZ	- OE	Any Q		18 18				ns
^t PZH	ŌĒ	A= O		12		12		ns
^t PZL	- UE .	Any Q		12				

'ALS964 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	FROM TO		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				
			SN	SN54ALS964		SN74ALS964		
			MIN	TYP [†]	MAX	MIN	TYP [†] MAX]
fmax	CLK	Any Q	25	30		25	30	MHz
^t PLH	CLK	Any Ω		10			10	ns
^t PHL		Ally U		14			14	1 "
^t PLH	CLK	SEROUT		10			10	ns
^t PHL	CLK	3ENOO1		14			14	1115
^t PHZ	ACLR	Any Q or SEROUT		14			14	ns
tPHZ	ŌĒ	Any Q		15			15	
tPLZ]	Any Q		18		18		ns
^t PZH	ŌĒ	Any Q		12			12	
tPZL	1 06	Any C		12			12	ns

 $^{\dagger}AII$ typical values are at VCC = 5 V, T_A = 25 °C. NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN74ALS990, SN74ALS991 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

D2835, APRIL 1984-REVISED MAY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic 'ALS990 . . . True Outputs 'ALS991 . . . Inverting Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The eight latches of the 'ALS990 and 'ALS991 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS990 will follow the data (D) inputs. For the 'ALS991, the Q outputs will provide the complement of what is applied to its data (D) inputs.

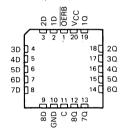
Read-back is <u>provided</u> through the read-back control input (OERB). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a busconflict situation.

The SN74ALS990 and SN74ALS991 are characterized for operation from 0 °C to 70 °C.

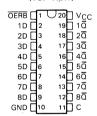
SN74ALS990 . . . DW OR N PACKAGE (TOP VIEW)

2555		T	
OERB [i C	20	Vcc
1D [2	19	1Q
2D 🗌	3	18	2Q
3D [4	17	3Q
4D 🗌	5	16	40
5D 🗌	6	15	5Q
6D [7	14	60
7D 🗌	8	13	7Q
8D 🗀	9	12	98
GND [10	11	С

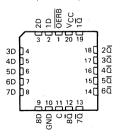
SN74ALS990 . . . FN PACKAGE



SN74ALS991 . . . DW OR N PACKAGE (TOP VIEW)

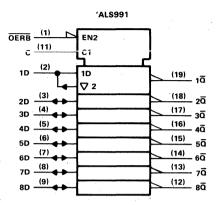


SN74ALS991 . . . FN PACKAGE (TOP VIEW)



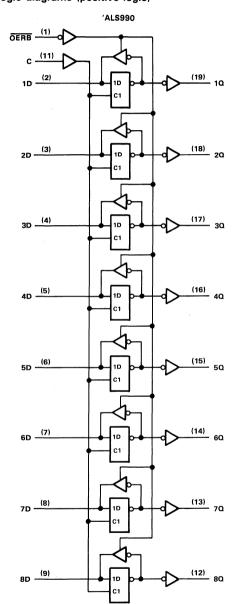
logic symbols†

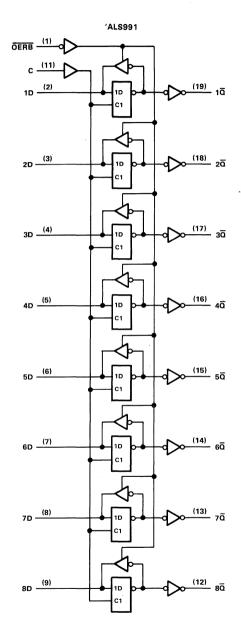
'ALS990 OERB (1) c (11) 1D (19) 10 **▽** 2 (3) (18) 2D (4) (17) 30 (16) (5) 4Q (15)(14) (7)(13) (12)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)





TIMING diagram DATA BUS INPUT DATA READ BACK INPUT DATA C C OERB P^tpd Q

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

,	Supply voltage, VCC				7	٧
I	nput voltage, (OERB and C inputs)				7	٧
١	Voltage applied to D inputs			. 5	.5	٧
(Operating free-air temperature range SN74ALS990, SN74ALS991		0°C	to 7	70°	С
5	Storage temperature range	-69	5°C to	15	60°	С

recommended operating conditions

				MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4:5	5	5.5	V
VIH	High-level input volt	age		2			V
VIL	Low-level input volt	age				0.8	V
lou	High-level output cu	rront	Q			-2.6	mA
ЮН	nigh-level output cu	irrent	D			-0.4	mA
I			Q			24	^
lOL	Low-level output cu	rrent	D			8	mA
t _w	Pulse duration, enal	ole C high		10			ns
	C-+	Data before C		10			
t _{su}	Setup time	Data before OF	RB↓	10			ns
th	Hold time	Data after C↓		5			ns
TA	Operating free-air te	mperature		0		70	°C

[†]This setup time ensures the readback circuit will not create a conflict on the input data bus.

SN74ALS990, SN74ALS991, 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDIT	TIONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_I = -18 \text{ mA}$			- 1.2	V
Va.,	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V
۷он	Q or Q	$V_{CC} = 4.5 \text{ V},$	IOH = -2.6 mA	2.4	3.2		ľ
	D	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 4 mA		0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	IOL = 8 mA		0.35	0.5] _v
VOL	Q or Q	$V_{CC} = 4.5 \text{ V},$	IOL = 12 mA		0.25	0.4	ľ
	2012	$V_{CC} = 4.5 V,$	IOL = 24 mA		0.35	0.5	
l _l	OERB, C	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
1	D inputs	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1	"'A
ΊΗ	OERB, C	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
.1111	D inputs [‡]	vCC = 5.5 v,	V = 2.7 V			20	μΑ
1 _{IL}	OERB, C	VCC = 5.5 V,	V _I = 0.4 V			-0.1	mA
11.	D inputs [‡]	VCC = 5.5 V,	V = 0.4 V			-0.1	l IIIA
lo§		V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	mA
	'ALS990		Q outputs high		27	50	
1	ALSSSO	$V_{CC} = 5.5 \text{ V, } \overline{\text{OERB}} \text{ high}$	Q outputs low		40	70	mA
lcc	'ALS991	VCC = 5.5 V, OERB High	Q outputs high		25	45] ""A
	ALSSSI		Q outputs low		45	75	

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, T_A = 25 °C. $^{\ddagger}For$ I/O ports, the parameters I $_{IH}$ and I $_{IL}$ include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

'ALS990 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, T _A = 25 °C, See Figures 1 and 2			V _{CC} = 4.1 C _L = 50 p T _A = 0°C See Figure	UNIT	
			MIN	TYP	MAX	MIN	MAX	
tPLH	D	Q		8	14	4	17	
tPHL	D	u u		11	22	5	24	· · ns
tPLH	С	Q		13	22	6	26	
tPHL		u		16	23	8	26	ns
t _{en}	OERB	D		12	18	4	21	no
^t dis	OEND			10	18	4	19	ns

 $t_{en} = t_{PZL} \text{ or } t_{PZH}$ tdis = tPLZ or tPHZ

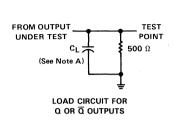
'ALS991 switching characteristics (see Figure 1)

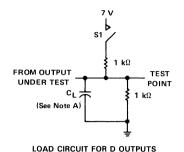
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L =	= 5 V, 50 pF, 25°C, igures 1	and 2	CL = 50	c to 70°C,	UNIT
			MIN	TYP	MAX	MIN	MAX	
^t PLH	D	ā		12	15	4	20	ns
^t PHL				9	12	4	15	115
^t PLH	С	ā		17	21	9	28	ns
^t PHL	Ĭ	<u> </u>		14	18	7	23	115
t _{en}	OERB	. D		12	17	4	22	ns
t _{dis}	l GENB	, 0		8	12	4	17	113

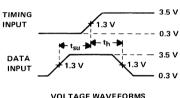
ten = tpzL or tpzH $t_{dis} = t_{PLZ} \text{ or } t_{PHZ}$



PARAMETER MEASUREMENT INFORMATION

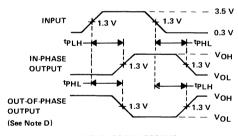




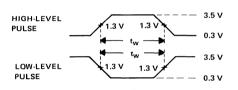


NOTE A: CL includes probe and jig capacitance.

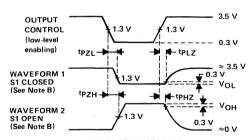
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS **PULSE WIDTHS**



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_f = t_f = 2$ ns, duty cycle = 50%.
 - D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1



D2836, APRIL 1984 REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic 'ALS992 . . . True Outputs 'ALS993 . . . Inverting Outputs
- Designed with 9 Bits for Parity Applications
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily implemented in parity applications.

The nine latches of the 'ALS992 and 'ALS993 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS992 will follow the data (D) inputs. For the 'ALS993, the $\overline{\Omega}$ outputs will provide the complement of what is applied to its data (D) inputs. On both devices, the Q or $\overline{\Omega}$ outputs will be in the 3-state condition when output enable \overline{OEQ} is high.

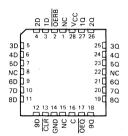
Read-back is provided through the read-back control input (OERB). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a busconflict situation.

The SN74ALS992 and SN74ALS993 are characterized for operation from 0 °C to 70 °C.

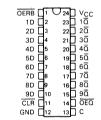
SN74ALS992 . . . DW OR NT PACKAGE (TOP VIEW)

OERB	hπ	724∐ V _C	_
1D	∄₂ `		C
	∟ ,∠		
2D	□з	22 2Q	
3D	□4	21 30	
4D	□5	20 40	
5D	∏ 6	19 5Q	
6D	□7	18 60	
7D	∏ 8	17 70	
8D	<u>∏</u> 9	16 80	
9D	10	15 90	
CLR	∐ 11	14 OE	ā
GND	12	13 C	

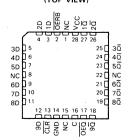
SN74ALS992 . . . FN PACKAGE (TOP VIEW)



SN74ALS993 . . . DW OR NT PACKAGE (TOP VIEW)



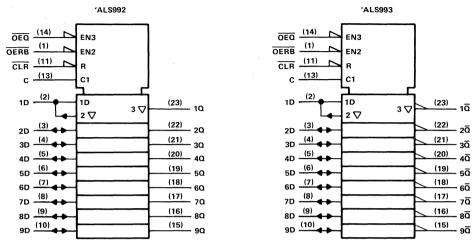
SN74ALS993 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection



logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers are for DW and NT packages.



(<u>23)</u> 1Q

(22) 20

(2<u>1)</u> 3Q

(2<u>0)</u> 4<u>0</u>

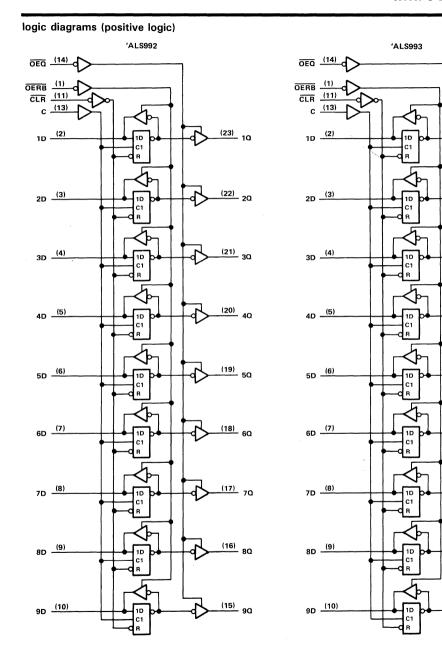
(<u>19)</u> 5Q

(18) 6Q

<u>(17)</u> 7Q

(<u>16)</u> 8Q

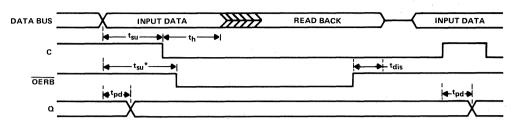
(<u>15)</u> 9Q



Pin numbers are for DW and NT packages.



timing diagram



 $\overline{CLR} = H, \overline{OEQ} = L$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage, (OERB, OE, CLR, and C inputs)
Voltage applied to D inputs and to disabled 3-state outputs
Operating free-air temperature range
Storage temperature range65 °C to 150 °C

recommended operating conditions

				MII	NOM	MAX	UNIT
Vcc	Supply voltage			4.	5 5	5.5	V
VIH	High-level input voltage				2		V
VIL	Low-level input voltage					0.8	V
1	High-level output current	J	Q or Q			-2.6	mA
ЮН	nigh-level output current	,	D			-0.4	l ma
1	. Love lovel output overest		Q or Q			24	^
IOL	Low-level output current		D			8	mA
	Pulse duration		Enable C high	11)		
t _w	ruise duration		CLR low	14)		ns
+	Setup time		Data before C↓	11)		
t _{su}	Setup time		Data before OERB↓	1) .		ns
.t _h	Hold time		Data after C↓		5		ns
TA	Operating free-air temperature)	70	°C



^{*}This setup time ensures the readback circuit will not create a conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDIT	TIONS	MIN	TYPt	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2	V
Voн	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} -2			V
•он	Q or Q	$V_{CC} = 4.5 V,$	I _{OH} = -2.6 mA	2.4	3.2		
	D	$V_{CC} = 4.5 V$	I _{OL} = 4 mA		0.25	0.4	
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 8 mA		0.35	0.5	V
VOL	Q or $\overline{\mathbf{Q}}$	$V_{CC} = 4.5 V$	I _{OL} = 12 mA		0.25	0.4	1
	4 01 4	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA		0.35	0.5	
lozh	Q or $\overline{\mathbf{Q}}$	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20	μА
lozL	1 404	$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20	μ.
l _l	D inputs	$V_{CC} = 5.5 V$,	$V_1 = 5.5 V$			0.1	mA
'1	All other	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1	'''^
	D inputs [‡]	$V_{CC} = 5.5 V$				20	
lН	All other	VCC = 5.5 V,	$V_{\parallel} = 2.7 \text{ V}$			20	μΑ
	D inputs [‡]		V 0.4 W			-0.1	
IIL	All other	$V_{CC} = 5.5 V$,	$V_{\parallel} = 0.4 V$			-0.1	mA
IO [§]		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	mA
			Q outputs high		30	50	
	'ALS992	$V_{CC} = 5.5 \text{ V}, \overline{OERB} \text{ high}$	Q outputs low		50	80	mA
loo			Q outputs disabled		35	55	
Icc			0 outputs high		30	50	
	'ALS993	$V_{CC} = 5.5 \text{ V}, \overline{OERB} \text{ high}$	Q outputs low		52	82	mA
	1		Qoutputs disabled		40	60	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, T_A = 25 °C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, IOS.

'ALS992 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		/ _{CC} = 5 C _L = 50 T _A = 25°	pF,	C _L = 50	5 V to 5.5 V, pF, C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX]
^t PLH	D	Q		7	10	3	14	ns
^t PHL		Q.		9	13	4	16	1115
^t PLH	С	a		12	15	6	20	ns
tPHL		<u>u</u>		15	19	8	25] '''
^t PHL	CLR	Q.		12	16	6	20	ns
^t PHL	CLN	D		15	22	8	26	1115
t _{en}	OERB:	D		11	17	4	21	
^t dis	OENB	U		6	11	2	14	ns
t _{en}	ŌĒQ	α		11	16	4	18	200
^t dis_		<u> </u>		6	10	1	14	ns

'ALS993 switching characteristics (see Figure 1)

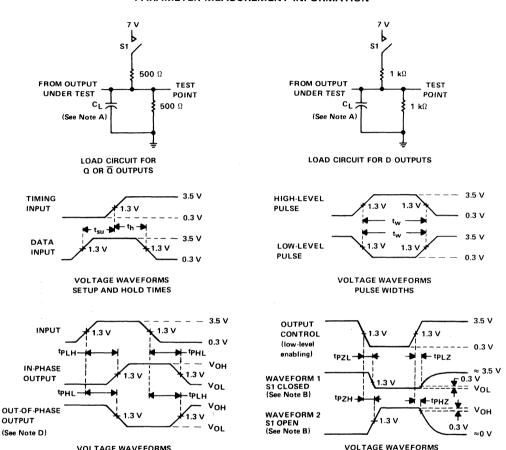
PARAMETER	FROM (INPUT)	TO (OUTPUT)	0	$CC = 5$ $C_L = 50$ $C_A = 25$	pF,	$V_{CC} = 4.$ $C_L = 50 \text{ g}$ $T_A = 0 \text{ °C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
^t PLH	D	ā		11	14	6	20	ns
^t PHL]	Q.		8	11	4	15	113
^t PLH	С	<u> </u>		16	20	9	28	-
^t PHL		u		13	16	7	22	ns
t _{PLH}	CLR	ā		10	13	5	17	
[†] PLH		D		15	22	8	26	ns
t _{en}	OERB	D		11	17	4	21	ns
[†] dis	J OENB	D		6	11	2	14	l lis
t _{en}	OEQ	<u> </u>		11	16	4	20	1
t _{dis}] 050	u		6	10	1	12	ns

t_{en} = t_{PZH} or t_{PZL} t_{dis} = t_{PHZ} or t_{PLZ}



ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C. includes probe and jig capacitance.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1



SN74ALS994, SN74ALS995 10 BIT D TYPE TRANSPARENT READ BACK LATCHES

D2856, OCTOBER 1984-REVISED JANUARY 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- Choice of True or Inverting Logic 'ALS994 . . . True Outputs 'ALS995 . . . Inverting Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

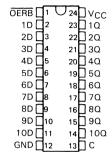
These 10-bit latches are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto the input data bus.

The ten latches of the 'ALS994 and 'ALS995 are transparent D-type. While the enable (C) is high, the Q outputs of the 'ALS994 will follow the data (D) inputs. For the 'ALS995, the Q outputs will provide the inverse of what is applied to its data (D) inputs.

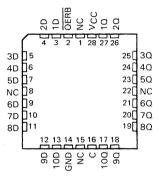
Read-back is <u>provided</u> through the read-back control input (OERB). When the control is taken low, the data present at the output of the data latches will be allowed to pass back onto the input data bus. When it is taken high, the output of the data latches will be isolated from the data (D) inputs. The read-back control does not affect the internal operation of the latches; however, precautions should be taken not to create a busconflict situation.

The SN74ALS994 and SN74ALS995 are characterized for operation from 0 °C to 70 °C.

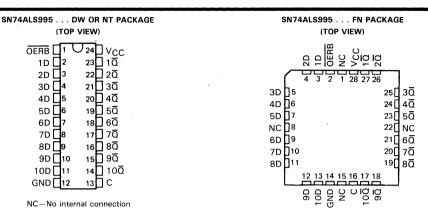
SN74ALS994 . . . DW OR NT PACKAGE (TOP VIEW)



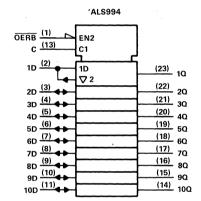
SN74ALS994 . . . FN PACKAGE
(TOP VIEW)

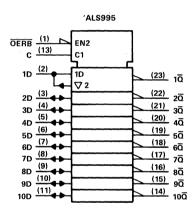


NC-No internal connection.

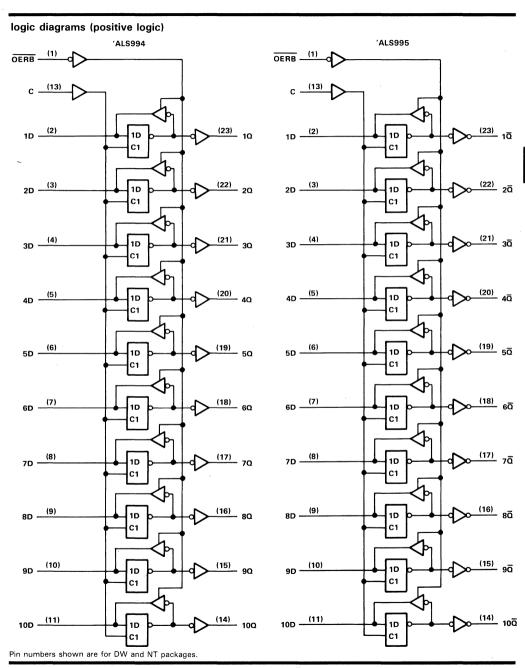


logic symbols†



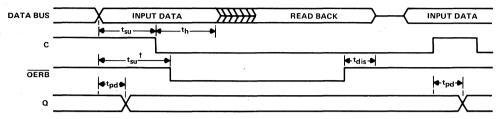


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW and NT packages.





timing diagram



[†]This setup time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	 7 V
Input voltage (OERB and C)	 7 V
Voltage applied to D inputs	 5.5 V
Operating free-air temperature range	 0°C to 70°C
Storage temperature range	 -65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage		2		,	V
VIL	Low-level input voltage				0.8	V
1	I limb land and a summer	Q or Q			-2.6	T A
ЮН	High-level output current	D			-0.4	mA
1	Law law Law Law Law Law Law Law Law Law Law L	Q or Q			24	mA
IOL	Low-level output current	D .			8	7
t _W	Pulse duration, enable C high		10	,		ns
	Setup time	Data before C↓	10			1
t _{su}	Setup time	Data before OERB ↓ †	10			ns
th	Hold time	Input data after C↓	5			ns
TA	Operating free-air temperature		0		70	°C

[†] This setup time ensures the readback circuit will not create a conflict on the input data bus.

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	ITIONS	MIN TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA		-1.2	V
V/011	All outputs	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -0.4 mA	V _{CC} - 2		V
Vон	Q or Q	$V_{CC} = 4.5 V,$	I _{OH} = -2.6 mA	2.4 3.2]
	D	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 4 mA	0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA	0.35	0.5] ,
VOL	Q or Q	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA	0.25	0.4	'
	4014	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA	0.35	. 0.5	
I.	OERB, C	V _{CC} = 5.5 V,	V _I = 7 V		0.1	mA
Ŋ	D inputs	V _{CC} = 5.5 V,	V _I = 5.5 V		0.1	l ma
1	OERB, C	Vcc = 5.5 V,	V - 2 7 V		20	μА
IIH	D inputs [‡]	VCC = 5.5 V,	V = 2.7 V		20	μΑ
1	OERB, C	Vcc = 5.5 V,	V ₁ = 0.4 V		-0.1	mA
IIL.	D inputs [‡]	VCC = 5.5 v,	V = 0.4 V		-0.1	
IO [§]		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30	-112	mA
	'ALS994		Q outputs high	30	50	
1	AL3994	$V_{CC} = 5.5 V$,	Q outputs low	52	82	mA
lcc	'ALS995	OERB high	Q outputs high	30	50] '''A
	AL3335		Q outputs low	55	85	1

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, T_A = 25 °C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit output current, IOS.

SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

'ALS994 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL	C = 5 = 50 p = 25°	ο F ,	CL = 50	.5 V to 5.5 V, pF, C to 70°C	UNIT
		•	MIN	TYP	MAX	MIN	MAX	
^t PLH	D	Q		7	10	3	14	ns
^t PHL	D	<u>u</u>		11	15	4	. 18	115
tpLH	С	0		12	16	6	21	
tPHL	C	ū.		16	21	8	27	ns
t _{en}	OERB	D		11	17	4	21	ns
t _{dis}	OENB			9	13	2	16	1 115

'ALS995 switching characteristics (see Figure 1)

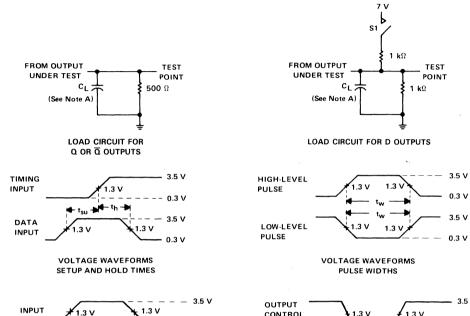
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL	C = 5 = 50 = 25°	οF,	C _L = 50	5 V to 5.5 V, pF, C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	
^t PLH	D	ō		12	16	6	20	ns
^t PHL	U	<u>u</u>		9	12	4	15	1115
tPLH	С	ō		17	23	9	28	ns
^t PHL		ď		14	19	7	22	1115
t _{en}	OERB	D		12	18	4	21	no
t _{dis}	OLNB			8	12	2	15	ns

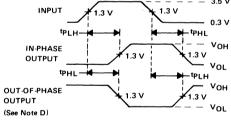
 $t_{en} = t_{PZH} or t_{PZL}$ $t_{dis} = t_{PHZ} \text{ or } t_{PLZ}$



SN74ALS994, SN74ALS995 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

3.5 V CONTROL 1.3 V 1.3 V (low-level - 0.3 V enabling) - tPLZ ≈ 3.5 V WAVEFORM 1 0.3 V 1.3 V == VOL S1 CLOSED (See Note B) Vон WAVEFORM 2 1.3 V S1 OPEN 0.3 V (See Note B)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_f = t_f = 2$ ns, duty cycle = 50%.
 - D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

D2854, OCTOBER 1984-REVISED JUNE 1986

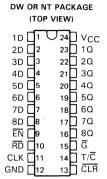
- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/C Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic "Small Outline"
 Packages, Both Plastic and Ceramic Chip
 Carriers, and Standard Plastic and Ceramic
 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

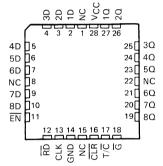
These 8-bit registers are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable (\overline{EN}) is low. Data can be read-back onto the data inputs by taking the read input (\overline{RD}) low, in addition to having \overline{EN} low. Whenever \overline{EN} is high, both the read-back and write modes are disabled. Transitions on \overline{EN} should only be made with CLK high in order to prevent false clocking.

The polarity of the Q outputs can be controlled by the polarity input T/\overline{C} . When T/\overline{C} is high, Q will be the same as is stored in the flip-flops. When T/\overline{C} is low, the output data will be inverted. The Q outputs can be placed in a high-impedance state by taking the output control \overline{G} 0 high. The output control \overline{G} does not affect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.



FN PACKAGE (TOP VIEW)



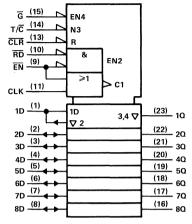
NC-No internal connection.

A low level at the clear input (CLR) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version except that the recommended maximum IOI is increased to 48 milliamperes.

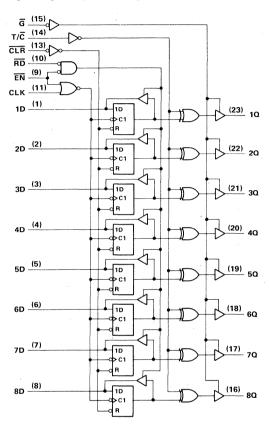
The SN74ALS996 is characterized for operation from 0°C to 70°C.

logic symbol†



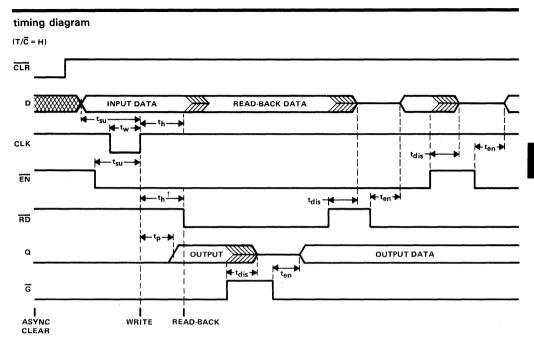
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW and NT packages.

SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES



[†]This hold time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC
Input voltage (G, RD, EN, CLK, CLR, and T/C)
Voltage applied to D inputs and to disabled 3-state outputs
Operating free-air temperature range
Storage temperature range – 65 °C to 150 °C

recommended operating conditions

	-			MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		,	4.5	5	5.5	V	
VIH	High-level input voltage			2			V	
V_{IL}	Low-level input voltage					0.8	V	
ЮН	High-level output current	Q				-2.6	mA	
		. D				-0.4		
lOL	Low-level output current	Q				24		
						48 [†]	mA	
		D				8		
f _{clock}	Clock frequency .			0		35	MHz	
t _W	Pulse duration	CLR low		10			ns	
		CLK low		14.5				
		CLK high		14.5				
t _{su}	Setup time	Data before CLK↑		15			ns	
		EN low before CLK↑		10				
		CLK high before EN↑‡		15				
		CLR high (inactive) before CLK1		10				
th	Hold time	Data after CLK↑		0			ns	
		EN low after CLK↑		5				
		RD high after CLK↑§		5				
TA	Operating free-air temperature			0		70	°C	

 $^{^\}dagger$ The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

 $^{{}^{\}ddagger}\text{This}$ setup time guarantees that $\overline{\text{EN}}$ will not false clock the data register.

[§]This hold time ensures there will be no conflict on the input data bus.

SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TES	ST CONDITIONS	MIN	TYP [†] MAX		UNIT	
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2	V	
VOH	All outputs	$V_{CC} = 4.5 \text{ V to 5}.$	$.5 \text{ V}, I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2			V	
	Q	$V_{CC} = 4.5 V$,	I _{OH} = -2.6 mA	2.4	3.2			
	D	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		
		$V_{CC} = 4.5 V$,	$I_{OL} = 8 \text{ mA}$		0.35	0.5	V	
VOL	Q	$V_{CC} = 4.5 V,$	IOL = 12 mA		0.25	0.4		
		$V_{CC} = 4.5 V,$	I _{OL} = 24 mA		0.35	0.5		
		$V_{CC} = 4.75 V$,	I _{OL} = 48 mA (-1 versions)		0.35	0.5		
JOZH	a	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20		
lozL	7 °	$V_{CC} = 5.5 V$,	V _I = 0.4 V			- 20	μΑ	
t _l	D inputs	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1	mA	
	All others	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1] ""^	
ΙΉ	D inputs [‡]	V 55V	$V_{CC} = 5.5 \text{ V}, \qquad V_{I} = 2.7 \text{ V}$			20		
	All others	VCC = 5.5 V,	$V_I = 2.7 V$			20	μΑ	
I _{IL}	D inputs [‡]		V _I = 0.4 V			-0.1		
	All others	$V_{CC} = 5.5 \text{ V},$				-0.1	mA	
lo§		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	mA	
		V _{CC} = 5.5 V,	Q outputs high		35	55		
Icc			Q outputs low		55	85	mA	
		EN, RD low	Q outputs disabled		42	65	1	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $T_A = 25 ^{\circ}\text{C}$			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $T_A = 0 ^{\circ}\text{C to } 70 ^{\circ}\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	1
f _{max}				40		35		MHz
^t PLH	CLK	0		16	24	5	28	l ne
^t PHL_	$(T/\overline{C} = H \text{ or } L)$	Q		16	24	5	28	ns
^t PLH	\overline{CLR} $(T/\overline{C} = L)$	Q		15	23	7	27	ns
^t PHL	\overline{CLR} (T/ $\overline{C} = H$)	· ·		13	19	7	23	l iis
^t PLH	T/\(\overline{\overline{C}}	Q		13	20	5	23	ns
^t PHL	1/0	ď		13	20	5	23	115
t _{PHL}	CLR	D		19	25	8	.30	ns
t _{en}	RD	D .		9	15	3	16	ns
t _{dis}		U ·		10	16	3	19	115
t _{ën}	ĒN	D		9	14	3	16	ns
^t dis	EIN			10	16	3	19	1 ''5
t _{en}	G	Q		8	13	4	15	ns
^t dis		u		4	8	1	10] '''s

ten = tpzH or tpzL

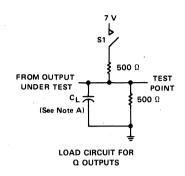


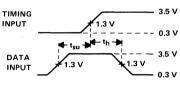
 $^{^{\}ddagger}$ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, IOS.

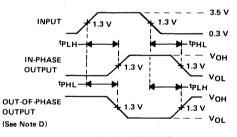
tdis = tPHZ or tPLZ

PARAMETER MEASUREMENT INFORMATION

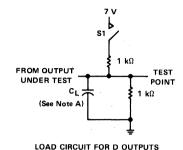


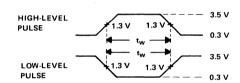




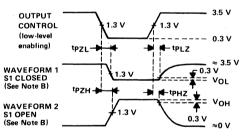


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES





VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

SN54ALS1000A, SN74ALS1000A, SN54AS1000A, SN74AS1000A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

D2661, APRIL 1984-REVISED MAY 1986

- 'ALS1000A is a Buffer Version of 'ALS00B
- 'AS1000A is a Driver Version of 'AS00
- 'AS1000A Offers High Capacitive-Driver Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

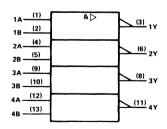
These devices contain four independent 2-input NAND buffers/drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS1000A and SN54AS1000A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1000A and SN74AS1000A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT		
Α	В	Y		
Н	Н	L		
L	Х	н		
x	1	н		

logic symbol†



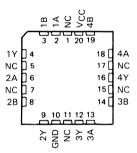
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54ALS1000A, SN54AS1000A . . . J PACKAGE SN74ALS1000A, SN74AS1000A . . . D OR N PACKAGE (TOP VIEW)

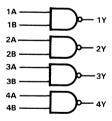
1 A 🗆 🗖	1111	hvaa
1A 🔲 1	U 14	□ vcc
1B 🔲 2	2 13	4B
1Y 🛚 3	12] 4A
2A 🛮 4	11	☐ 4Y
2B 🗌 5	10] 3B
2Y. 🗌 6	9] 3A
GND 🗆	7 8] 3Y

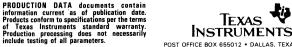
SN54ALS1000A, SN54AS1000A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic diagram (positive logic)





SN54ALS1000A, SN74ALS1000A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC 7 V
Input voltage
Operating free-air temperature range: SN54ALS1000A55°C to 125°C
SN74ALS1000A 0 °C to 70 °C
Storage temperature range

recommended operating conditions

		SN	SN54ALS1000A			SN74ALS1000A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ГОН	High-level output current			- 1			-2.6	mA	
OL	Low-level output current			12			24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETED	TEGT COMP	TIONO	SN5	SN54ALS1000A SN74ALS1000A			000A UNI		
PARAMETER	TEST COND	ITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
V _{IK}	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		
V _{OH}	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3] v
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		İ
\/ - ·	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA·		0.25	0.4		0.25	0.4 V	
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5]
l _l	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1	l		0.1	mA
Iн	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1		_	-0.1	mA
10 [‡]	$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	- 30		- 112	-30		-112	mA
Іссн	$V_{CC} \approx 5.5 \text{ V},$	V _I = 0 V		0.86	1.6		0.86	1.6	mA
¹ CCL	V _{CC} ≈ 5.5 V,	$V_1 = 4.5 \text{ V}$		4.8	7.8		4.8	7.8	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} \text{V}_{\text{CC}} = 5 \text{ V,} \\ \text{C}_{\text{L}} = 50 \text{ pF,} \\ \text{R}_{\text{L}} = 500 \Omega, \\ \text{T}_{\text{A}} = 25 ^{\circ}\text{C} \\ \text{'ALS1000A} \\ \end{array}$	SN54AL MIN	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = \text{MIN}$.S1000A	F, Ω, to-MAX	\$1000A MAX	UNIT
tPLH	AorB	Υ	4	2	10	2	8	ns
^t PHL	A or B	Υ .	5	2	10	2	7	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS1000A, SN74AS1000A QUADRUPLE 2-INPUT POSITIVE-NAND DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Operating free-air temperature range:	SN54AS1000A	-55°C to 125°C
	SN74AS1000A	0°C to 70°C
Storage temperature range	-	-65°C to 150°C

recommended operating conditions

		SN	SN54AS1000A			SN74AS1000A		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Iон	High-level output current			-40			- 48	mA
lOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS SN54AS1000A		SNZ	74AS10	00A	UNIT			
PARAMETER	IEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -:	2		V _{CC} - 2	2		
	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		\ \
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -40 \text{ mA}$	2						
	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = -48 \text{ mA}$				2			
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 40 \text{ mA}$		0.25	0.5				l _v
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 48 \text{ mA}$					0.35	0.5	Ľ
ŀμ	$V_{CC} = 5.5 V,$	$V_{I} = 7 V$			0.1			0.1	mA
lін	$V_{CC} = 5.5 V,$	$V_{ } = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
lo [‡]	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	-50		- 200	- 50		-200	mA
ICCH	$V_{CC} = 5.5 V,$	$V_I = 0 V$		2.2	3.5		2.2	3.5	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		12	19		12	19	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54A MIN	$V_{CC} = 4.5$ $C_{L} = 50 \text{ p}$ $R_{L}1 = 500$ $T_{A} = MIN$ $S1000A$ MAX	F, Ω, to MAX	S1000A MAX	UNIT
t _{PLH}	A or B	Y	1	5	1	4	ns
^t PHL	A or B	Y	1	5	1	4	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.



The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1002A, SN74ALS1002A QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

D2661, DECEMBER 1983-REVISED MAY 1986

- Quad Versions of 'ALS805A
- Buffer Version of 'ALS02
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NOR buffers. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54ALS1002A is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS1002A is characterized for operation from 0° C to 70° C.

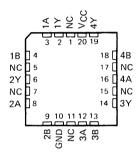
FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Х	L
Χ	Н	L
L	L	Н

SN54ALS1002A . . . J PACKAGE SN74ALS1002A . . . D OR N PACKAGE (TOP VIEW)

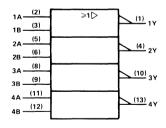
1Y 🛮 1	U14	□vcc
1A 🗆 2	13	□4 Y
1 B 🛚 3	12] 4B
2Y 🛮 4	11]4A
2A∏5	10]3Y
2B [6	9] 3B
GND 7	8	□3A

SN54ALS1002A . . . FK PACKAGE (TOP VIEW)



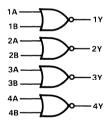
NC-No internal connection

logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



SN54ALS1002A, SN74ALS1002A QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54ALS1002A – 55 °C to 125 °C
SN74ALS1002A 0 °C to 70 °C
Storage temperature range65°C to 150°C

recommended operating conditions

	`	SN	SN54ALS1002A				SN74ALS1002A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT		
Vcc	Supply voltage	4.5	5	5.5	4.5	. 5	5.5	V		
VIH	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.7			0.8	٧		
Іон	High-level output current			- 1			-2.6	mA		
lOL	Low-level output current			12			24	mA		
TA	Operating free-air temperature	- 55		125	0		70	°C		

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		SNE	4ALS10	SN54ALS1002A			002A	UNIT
PARAMETER	1EST CONDI	1231 CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	$I_1 = -18 \text{ mA}$			-1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -	2		
VoH	V _{CC} = 4.5 V,	IOH = -1 mA	2.4	3.3] v
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
\/-·	$V_{CC} = 4.5 V,$	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
l)	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
liH	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
IIL	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	-30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		1.7	2.8		1.7	2.8	mA
^I CCL	$V_{CC} = 5.5 \text{ V},$	V _I = 4.5 V		5.6	9		5.6	9	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS1002A		$V_{CC} = 4.5$ $C_{L} = 50 \text{ pl}$ $R_{L} = 500 \text{ s}$ $T_{A} = \text{MIN}$ $-\text{S}1002\text{A}$	F, Ω, to MAX SN74AL	.S1002A	UNIT
			TYP	MIN	MAX	MIN	MAX	
^t PLH	A or B	Y	4	2	10	2	8	ns
tPHL	A or B	Y	4	2	10	2	7	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.



[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1003A, SN74ALS1003A QUADRUPLE 2-INPUT POSITIVE NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Buffer Version of 'ALS03B
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

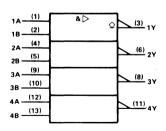
These devices contain four independent 2-input NAND buffers. They perform the Boolean functions $Y=\overline{A\bullet B}$ or $Y=\overline{A}+\overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1003A is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $\,^{\circ}$ C. The SN74ALS1003A is characterized for operation from 0 $\,^{\circ}$ C to 70 $\,^{\circ}$ C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
L	Χ	Н
x	L	Н

logic symbol†



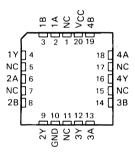
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

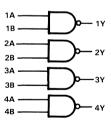
SN54ALS1003A . . . J PACKAGE SN74ALS1003A . . . D OR N PACKAGE (TOP VIEW)

	_	
1A 🗌	1	U14∏ Vcc
1B 🗌	2	13 🗌 4B
1Y 🛚	3	12 🗌 4A
2A 🗌	4	11 🛮 4Y
2B 🗌	5	10 🗌 3B
2Y 🗌	6	9 🗌 3A
GND 🗌	7	8 🗌 3Y

SN54ALS1003A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



SN54ALS1003A, SN74ALS1003A QUADRUPLE 2-INPUT POSITIVE NAND GATES WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		7 V
Off-state output voltage		7 V
Operating free-air temperature range:	: SN54ALS1003A55°C to 12	5°C
	SN74ALS1003A 0 °C to 7	O°C
Storage temperature range	−65°C to 15	O°C

recommended operating conditions

		SNE	4ALS10	03A	SN7	UNIT		
	•	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating-free-air temperature range (unless otherwise noted)

PARAMETER	TECT O	TEST CONDITIONS		SN54ALS1003A			4ALS10	03A	UNIT
PANAMETER	TEST CONDITIONS			TYP [†]	MAX	MIN	TYP [†]	MAX	ONII
V _{IK}	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
IOH	$V_{CC} = 4.5 V$,	V _{OH} = 5.5 V			0.1			0.1	mA
Vo	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	$V_{CC} = 4.5 V$,	$I_{OL} = 24 \text{ mA}$					0.35	0.5	l '
1	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1	i		0.1	mA
lн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μА
IΙL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
¹ ССН	V _{CC} = 5.5 V,	V _I = 0 V		0.86	1.6		0.86	1.6	mA
^I CCL -	$V_{CC} = 5.5 V,$	V _I = 4.5 V		4.8	7.8		4.8	7.8	mA

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 680 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS1003A	SN54AL	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 680 \Omega$ $T_A = MIN$.S1003A	to MAX	.S1003A MAX	UNIT
tPLH	A or B	Y	18	10	40	10	33	ns
tPHL	A or B	Y	7	2	18	2	12	ns

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.



SN54ALS1004, SN54AS1004A, SN74ALS1004, SN74AS1004A HEX INVERTING DRIVERS

D2661, APRIL 1982 - REVISED MAY 1986

- 'AS1004A Offers High Capacitive-Drive Capability
- Driver Version of 'ALS04 and 'AS04
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

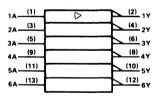
These devices contain six independent inverting drivers. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS1004 and SN54AS1004A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1004 and SN74AS1004A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

INPUT	OUTPUT
Α	Y
Н	L
L	н

logic symbol†



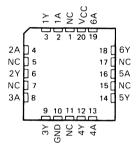
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

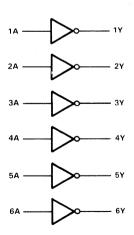
SN54ALS1004, SN54AS1004A . . . J PACKAGE SN74ALS1004, SN74AS1004A . . . D OR N PACKAGE (TOP VIEW)

1A 🗌	1	U14	۷cc
1 Y 🗌	2	13	6A
2A 🗌	3	12	6Y
2Y 🗌	4	11	5A
3A 🗌	5	10	5Y
3Y 🗌	6	9	4A
GND 🗌	7	8	4Y

SN54ALS1004, SN54AS1004A . . . FK PACKAGE (TOP VIEW)



NC – No internal connection



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS1004 -55°C to 125°C SN74ALS1004 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		SN	SN54ALS1004			SN74ALS1004			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5,	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ПОН	High-level output current			- 12			- 15	mA	
lOL	Low-level output current			12			24	mA	
Тд	Operating free-air temperature	- 55		125	0		. 70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	54ALS	1004	SN	74ALS	1004	UNIT
PARAMETER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			Vcc-	2		
V	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2]
∨он	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -12 mA	2						1 °
	$V_{CC} = 4.5 \text{ V},$	IOH = -15 mA				2			
Vai	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4).4 V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5	1 °
l ₁	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΊΗ	V _{CC} = 5.5 V,	V ₁ = 2.7 V			20			20	μΑ
IIL III	$V_{CC} = 5.5 V,$	V ₁ = 0.4 V			-0.1			-0.1	mA
lO‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
Iссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.84	3		0.84	3	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		7	12		7	12	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}, T_{A} = 25 ^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R _I T,	CC = 4.5 V L = 50 pF, $L = 500 \Omega,$ L = MIN to I L = MIN ALS = MIN ALS = MIN To I	мах	ALS1004 MAX	UNIT
tPLH	A	V	1	9	1	7	ns
^t PHL	1	,	1	8	1	6] '''

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	/
Input voltage	/
Operating free-air temperature range: SN54AS1004A55°C to 125°C	2
SN74AS1004A 0 °C to 70 °C	2
Storage temperature range -65°C to 150°C	

recommended operating conditions

		SN	54AS10	04A	SN	74AS10	04A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	\ \
ViH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	\ \
^I OH	High-level output current			- 40			- 48	mA
^I OL	Low-level output current			40			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT COND.	TIONE	SN	54AS10	04A	SN	74AS10	004A	UNIT
PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONIT
ViK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	٧
	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} - 2			Vcc-	2		
V	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		l v
Voн	$V_{CC} = 4.5 \text{ V},$	I _{OH} = 40 mA	2						1 '
	$V_{CC} = 4.5 V,$	I _{OH} = -48 mA				2			1
V	$V_{CC} = 4.5 V,$	I _{OL} = 40 mA		0.25	0.5				V
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.35	0.5]
11	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA
1н	$V_{CC} = 5.5 V,$	V ₁ = 2.7 V			20			20	μΑ
1 ₁ L	V _{CC} = 5.5 V,	V ₁ = 0.4 V			-0.5			-0.5	mA
lO‡	V _{CC} = 5.5 V,	$V_0 = 2.25 V$	- 50		- 200	- 50		- 200	mA
Iссн	$V_{CC} = 5.5 V,$	V _I = 0 V		3.5	5		3.5	5	mÁ
¹ CCL	$V_{CC} = 5.5 \text{ V},$	V ₁ = 4.5 V		16	27		16	27	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _I R _I T,	CC = 4.5 V L = 50 pF, $L = 500 \Omega,$ A = MIN to I CC = 4.5 V $A = 500 \Omega,$ A = MIN to I	MAX	AS1004A MAX	UNIT
tPLH	A or B		1	5	1	4	ns
t _{PHL}	AOIB	, ,	1	5	1	4	1115



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS1005, SN74ALS1005 HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Buffer Version of 'ALS05
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

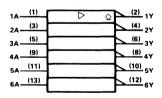
These devices contain six independent inverting buffers. They perform the Boolean function $Y=\overline{A}$. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS1005 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS1005 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each inverter)

INPUT	OUTPUT
Α	Υ
Н	L
L	н

logic symbol[†]

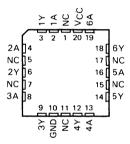


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

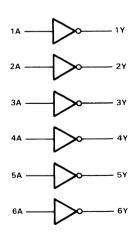
SN54ALS1005 . . . J PACKAGE SN74ALS1005 . . . D OR N PACKAGE (TOP VIEW)

1 A 🗌	1	14]v _{cc}
1Y 🗌	2	13]6A
2A 🗌	3	12] 6Y
2Y 🗌	4	11]5A
3A 🗌	5	10] 5Y
3Y 🗌	6	9]4A
GND 🗌	7	8]4Y

SN54ALS1005 . . . FK PACKAGE (TOP VIEW)



NC -- No internal connection



Pin numbers shown are for D, J, and N packages.

recommended operating conditions

		SN	SN54ALS1005		SN74ALS1005			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
Vон	High-level output voltage			5.5			5.5	V
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TECT O	ONDITIONS	SN	54ALS1	005	SN	74ALS1	005	UNIT
PARAMETER	TEST C	ONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.5			-1.5	V
Іон	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1			0.1	mA ·
1/	$V_{CC} = 4.5 V$,	I _{OL} ≈ 12 mA	T	0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$,	IOL ≈ 24 mA	T				0.35	0.5	1 "
l ₁	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 \dot{V}$	V _I = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
Іссн	V _{CC} = 5.5 V,	V _I = 0 V		0.9	3		0.9	3	mA
^I CCL	V _{CC} = 5.5 V,	V _I = 4.5 V		7	12		7	12	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 R _L = 680 T _A = MIN	Ω, N to MAX		UNIT
			MIN	LS1005 MAX	MIN	LS1005 MAX	ł
			IVIIIV		WIIIV		ļ
t _{PLH}			5	35	5	30	
^t PHL	Α	r	2	12	2	10	ns



SN54ALS1008A, SN54AS1008A, SN74ALS1008A, SN74AS1008A QUADRUPLE 2-INPUT POSITIVE-AND BUFFERS/DRIVERS

D2661, DECEMBER 1982-REVISED MAY 1986

- 'ALS1008A is a Buffer Version of 'ALS08
- 'AS1008A is a Driver Version of 'AS08
- 'AS1008A Offers High Capacitive Drive Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

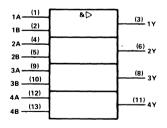
These devices contain four independent 2-input AND buffers/drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS1008A and SN54AS1008A are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1008A and SN74AS1008A are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

ſ	INP	UTS	OUTPUT
	Α	В	Υ
T	Н	Τ	Τ
1	Ĺ	Х	L
1	Х	L	L

logic symbol†

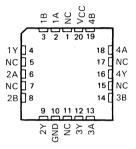


Pin numbers shown are for D, J, and N packages.

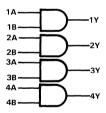
SN54ALS1008A, SN54AS1008A . . . J PACKAGE SN74ALS1008A, SN74AS1008A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS1008A, SN54AS1008A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operat	ing free-air temperature range (unless otherwise noted)
Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range:	SN54ALS1008A55°C to 125°C
	SN74ALS1008A 0 °C to 70 °C
Storage temperature range	65°C to 150°C

recommended operating conditions

		SNS	4ALS1	A800	SN7	4ALS1	A800	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	ONIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			- 1			- 2.6	mA
lOL	Low-level output current			12			24	mA
ТД	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEGT CONDITIONS		SN5	4ALS1	A800	SN7	UNIT		
PARAMETER	TEST CONDITIONS			TYP [†]	MAX	MIN	TYP†	MAX	וואטן
VIK	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.1$	5 V , $1_{OH} = -0.4 \text{ mA}$	V _{CC} - 3	2		V _{CC} -	- 2		
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					1 v
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		1
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4				V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA					0.35	0.5	1
l _l	$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA
ήн	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IIL III	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			- 0.1	mA
lo‡	$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 30		- 112	- 30		- 112	mA
¹ ССН	V _{CC} = 5.5 V,	V _I = 4.5 V		1.8	3		1.8	3	mA
ICCL	V _{CC} = 5.5 V,	V _I = 0 V		5.7	9.3		5.7	9.3	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PARAMETER	FROM (INPUT)	PUT) (OUTPUT)	SN54AI	V _{CC} = 4.5 C _L = 50 pF R _L = 500 (T _A = MIN -	o MAX SN74A	LS1008A	UNIT
	1		MIN	MAX	MIN	MAX	
^t PLH	A or B	ÿ	2	11	2	9	ns
[†] PHL	AOID	.'	3	11	3	9	1 115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54AS1008A, SN74AS1008A QUADRUPLE 2-INPUT POSITIVE-AND DRIVERS

absolute maximum ratings over operati	ing free-air temperature range (unless othe	rwise noted)
Supply voltage, VCC		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54AS1008A	– 55°C to 125°C
	SN74AS1008A	0°C to 70°C
Storage temperature range		-65°C to 150°C

recommended operating conditions

		SN5	4AS10	A80	SN7	4AS10	08A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
Тон	High-level output current			- 40			- 48	mA
loL	Low-level output current			40			48	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN5	4AS10	A80	SN7	UNIT		
PARAMETER	TEST CONDITIO	JNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	_I = -18 mA			-1.2			- 1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V, I}$	OH = -2 mA	V _{CC} -	2		Vcc	2		
Vall	$V_{CC} = 4.5 \text{ V},$	OH = -3 mA	2.4	3.2		2.4	3.2		V
Voн	$V_{CC} = 4.5 \text{ V},$	OH = -40 mA	2]
	$V_{CC} = 4.5 \text{ V},$	OH = -48 mA				2			1
Vol	$V_{CC} = 4.5 \text{ V},$	OL = 40 mA		0.25	0.5	•			V
VOL	$V_{CC} = 4.5 \text{ V},$	OL = 48 mA					0.35	0.5	ľ
l ₁	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
l _{IL}	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			- 0.5	mA
10‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 200	- 50		- 200	mA
¹ ссн	$V_{CC} = 5.5 \text{ V},$	V _I = 4.5 V		5.6	9.5		5.6	9.5	mA
CCL	$V_{CC} = 5.5 \text{ V},$	V _I = 0 V		13.5	22		13.5	22	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PARAMETER	FROM (INPUT)	то (оитрит)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX					
1			SN54AS	S1008A	SN74A	S1008A		
	1	<u> </u>	MIN	MAX	MIN	MAX		
tPLH	A or B	· ·	1	6.5	1	6	ns	
^t PHL	7 401 5	'	1	6.5	1	6	113	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS1010A, SN74ALS1010A TRIPLE 3-INPUT POSITIVE NAND BUFFERS

D2661, APRIL 1982-REVISED MAY 1986

- Buffer Version of 'ALS10A
- Package Options Include Plastic "Small Outline" DIPs and Ceramic Chip Carriers in Addition to the Standard 300-mil Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

description

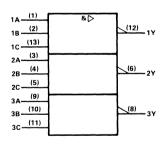
These devices contain three independent 3-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS1010A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1010A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH GATE)

	NPUTS	;	OUTPUT
Α	В	С	Υ
Н	Н	Н	L
L	X	x	н
×	L	х	н
×	Х	L	н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

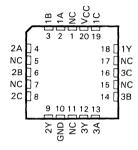
Pin numbers shown are for D, J, and N packages.

PRODUCTION DATA documents contain information current as of publication date Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

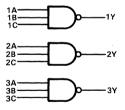
SN54ALS1010A . . . J PACKAGE SN74ALS1010A . . . D OR N PACKAGE (TOP VIEW)

1A [1	\bigcup_{14}	□vcc
1B [12	13] 1C
2A []3	12] 1Y
2B []4	11] 3C
2C [1 5	10] 3B
2Y [] 6	9] 3A
GND [7	8] 3Y

SN54ALS1010A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS1010A -55°C to 125°C SN74ALS1010A 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		SN54ALS10			A SN74ALS1010A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ГОН	High-level output current			· - 1			-2.6	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEGT O	CAUDITIONIC	SN	54ALS	1010A	SN	UNIT		
PARAMETER	IESI C	TEST CONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	$5 \text{ V, I}_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		v _{cc} -	2		
Vон	$V_{CC} = 4.5 V$,	$I_{OH} = -1 \text{ mA}$	2.4	3.3] ∨
	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	1 °
lj.	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lн	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$			20			20	μΑ
Iμ	$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	-30		-112	- 30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		0.65	1.2		0.65	1.2	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		3.6	5.8		3.6	5.8	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS1010A TYP	C _L R _L T _A	C = 4.5 V = 50 pF, = 500 Ω, = MIN to LS1010A MAX		 010A MAX	UNIT
tPLH	Any		5	2	12	2	8	ns
^t PHL	Ally	<u> </u>	5	2	12	2	8	115



^{*} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1011A, SN74ALS1011A TRIPLE 3-INPUT POSITIVE-AND BUFFERS

D2661, APRIL 1982-REVISED MAY 1986

- Buffer Version of 'ALS11
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

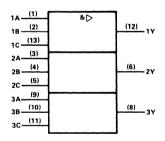
These devices contain three independent 3-input AND buffers. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A + B + \overline{C}}$ in positive logic.

The SN54ALS1011A is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS1011A is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

	NPUT	S	OUTPUT
Α	В	С	Υ
Н	Н	Н	Н
L	Х	Х	L
х	L	Х	L
Х	Х	L	L

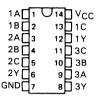
logic symbol[†]



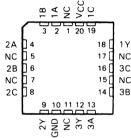
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

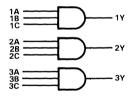
SN54ALS1011A . . . J PACKAGE SN74ALS1011A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS1011A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





recommended operating conditions

		SN5	SN7	UNIT				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	, 5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			- 1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

040445750		71010	SN5	SN54ALS1011A			SN74ALS1011A		
PARAMETER	TEST COND	HONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			-1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
VoH	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					V
	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
V	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	V _{CC} = 4.5 V ₁	I _{OL} = 24 mA					0.35	0.5	
11	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
Iн	$V_{CC} = 5.5 V,$	V ₁ = 2.7 V			20			20	μΑ
Iμ	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 4.5 V		1.4	2.3		1.4	2.3	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 0 V		4.3	7		4.3	7	mA

[†]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX				
			SN54A	SN54ALS1011A		SN74ALS1011A		
			MIN	MAX	MIN	MAX	}	
^t PLH	Δ	V	2	12	2	10		
^t PHL	Any	Y	3	11	3	9	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



^{\$\}pm\$The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1020A, SN74ALS1020A DUAL 4-INPUT POSITIVE-NAND BUFFERS

D2661, APRIL 1982-REVISED MAY 1986

- Buffer Version of 'ALS20B
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

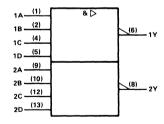
These devices contain two independent 4-input NAND buffers. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54ALS1020A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1020A is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

	INP	OUTPUT		
Α	В	Υ		
Н	Н	Н	Н	L
L	Х	X	Х	Н
×	L	X	X	Н
×	X	L	X	н
x	Х	X	L	н

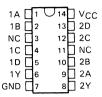
logic symbol†



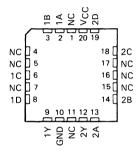
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

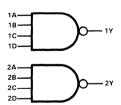
SN54ALS1020A . . . J PACKAGE SN74ALS1020A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS1020A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS1020A -55°C to 125°C SN74ALS1020A 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		SNS	SN54ALS1020A			SN74ALS1020A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ТОН	High-level output current			- 1			-2.6	mA	
lOL	Low-level output current	1		12			24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COM	TEST CONDITIONS		54ALS1	020A	SN74ALS1020A			UNIT	
PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	VCC = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V	
	$V_{CC} = 4.5 \text{ V to } 5.5$	5 V, I _{OH} = -0.4 mA	Vcc	- 2		Vcc-	- 2			
Voн	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA},$	2.4	3.3					v	
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.3		1	
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V	
VOL	$V_{CC} = 4.5 \text{ V},$	IOL = 24 mA					0.35	0.5] `	
11	$V_{CC} = 5.5 V,$. V _I = 7 V			0.1			0.1	mA	
IH	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ	
ΙΙL	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.1			-0.1	mA	
1O‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA	
Іссн	$V_{CC} = 5.5 V$,	V ₁ = 0 V		0.5	0.8		0.5	0.8	mA	
^I CCL	$V_{CC} = 5.5 V,$	$V_{I} = 4.5 V$		2.4	3.9		2.4	3.9	mA	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS1020A TYP	SN54AL MIN	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = \text{MIN}$.S1020A	=, ⊋, to MAX	.S1020A MAX	UNIT
^t PLH	Anv	v	5	2	10	2	8	ns
^t PHL	Ally	·	5	2	10	2	7	113

NOTE 1. Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1032A, SN54AS1032A, SN74ALS1032A, SN74AS1032A QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

D2661, DECEMBER 1982-REVISED MAY 1986

- 'ALS1032A is a Buffer Version of 'ALS32
- 'AS1032A is a Driver Version of 'AS32
- 'AS1032A Offers High Capacitive Drive Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

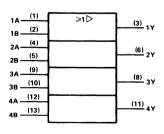
These devices contain four independent 2-input OR buffers/drivers. They perform the Boolean functions Y = A + B or $Y = \overline{A \cdot B}$ in positive logic.

The SN54ALS1032A and SN54AS1032A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1032A and SN74AS1032A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
Н	Х	Н
Х	Н	Н
L	L	L

logic symbol†



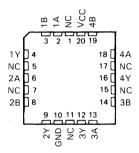
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

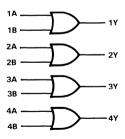
SN54ALS1032A, SN54AS1032A . . . J PACKAGE SN74ALS1032A, SN74AS1032A . . . D or N PACKAGE (TOP VIEW)

_	_		_	
1 A 🗌	1	U 14	Ш	VCC
1B 🗌	2	13		4B
1 Y 🗌	3	12		4A
2A 🗌	4	11		4Y
2B 🗌	5	10		3В
2Y 🗌	6	9		ЗА
GND [7	8		3Y

SN54ALS1032A, SN54AS1032A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)						
Operating free-air temperature range: SN54	4ALS1032A					
	-65°C to 150°C					

recommended operating conditions

		SI	SN54ALS1032A			SN74ALS1032A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
V _C C	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			8.0	٧	
Іон	High-level output current			-1			-2.6	__ mA	
lOL	Low-level output current			12			24	mA	
TΑ	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEGT 001	DITIONO	SI	N54ALS	1032A	SI	N74ALS	1032A	V V MA
PARAMETER	TEST CON	DITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			- 1.5			- 1.5	V
	$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		v _{cc} -	2		
VoH	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -1 mA	2.4	3.3					V
	V _{CC} = 4.5 V,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2]
Voi	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	·
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1	T		0.1	mA
lін	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μА
ηL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
10 [‡]	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	-30		-112	mA
1ссн	$V_{CC} = 5.5 V,$	V _I = 4.5 V		2.5	5		2.5	5	mA
^I CCL	$V_{CC} = 5.5 V,$	V _I = 0 V		6.6	10.6		6.6	10.6	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS1032A	SN54AL	/, LS1032A	UNIT		
			TYP	MIN	MAX	MIN	MAX	
tPLH	A or B	V	6	2	12	2	9	ns
^t PHL	AOIB		7	3	15	3	12] ""



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54AS1032A, SN74AS1032A QUADRUPLE 2-INPUT POSITIVE-OR DRIVERS

absolute maximum ratings over operat	ing free-air temperat	ure range (unless o	otherwise noted)
Supply voltage, VCC			7 V
Input voltage			7 V
Operating free-air temperature range:	SN54AS1032A		55°C to 125°C
	CNIZAACAOQQA		000 +0 7000

Storage temperature range recommended operating conditions

		SI	SN54AS1032A			SN74AS1032A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
ТОН	High-level output current			-40			- 48	mA	
loL	Low-level output current			40			48	mA	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDIT	TONC	SN54AS1032A SN74AS1032A		032A	UNIT			
PARAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	V
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} - 2			Vcc-	2		
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
VOH	$V_{CC} = 4.5 V,$	I _{OH} ≈ -40 mA	2]
	$V_{CC} = 4.5 V,$	$I_{OH} = -48 \text{ mA}$				2]
VOL	$V_{CC} = 4.5 V$,	IOL = 40 mA		0.25	0.5				
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$					0.35	0.5	l v
lμ	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
I _{IL}	V _{CC} = 5.5 V,	$V_1 = 0.4 V$			-0.5			-0.5	mA
lo [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 50		- 200	- 50		- 200	mA
Іссн	V _{CC} = 5.5 V,	V _I = 4.5 V		7.7	11.5		7.7	11.5	mA
ICCL	V _{CC} = 5.5 V,	V _I = 0 V		14.7	24		14.7	24	mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54A	$V_{CC} = 4.5$ $C_{L} = 50 \text{ pi}$ $R_{L} = 500 \text{ s}$ $T_{A} = \text{MIN}$ $S1032A$	F, Ω, to MAX	V, AS1032A	UNIT
			MIN	MAX	MIN	MAX	
^t PLH	A or B	V	1	7	1	6.3	
` ^t PHL	A 01 B		1	7	1	6.3	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1034, SN54AS1034A, SN74ALS1034, SN74AS1034A HEX DRIVERS

D2661, APRIL 1982-REVISED MAY 1986

- 'AS1034A Offers High Capacitive-Drive Capability
- Noninverting Drivers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent noninverting drivers. They perform the Boolean functions Y = A.

The SN54ALS1034 and SN54AS1034A are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1034 and SN74AS1034A are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each buffer)

INPUT	OUTPUT
Α	Y
Н	Ι
L .	L

logic symbol †

1A (1)	D	(2) 1Y
2A (3)		(4) (6) 3Y
3A (9)		(8) (8)
5A (11)		(10) _{5Y}
6A (13)		(12) 6Y

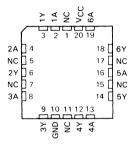
 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

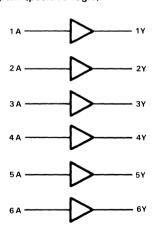
SN54ALS1034, SN54AS1034A . . . J PACKAGE SN74ALS1034, SN74AS1034A . . . D OR N PACKAGE (TOP VIEW)



SN54ALS1034, SN54AS1034A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	,
Input voltage	
Operating free-air temperature range:	SN54ALS103455 °C to 125 °C
	SN74ALS1034 0 °C to 70 °C
Storage temperature range	65°C +0 150°C

recommended operating conditions

		SN54ALS1034		034	SN74ALS1034			UNIT
	·	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
IОН	High-level output curent			- 12			- 15	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDI	TIONS	SN54ALS1034 SN74ALS1034			034	UNIT		
PARAMETER	TEST CONDI	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	l ₁ = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	2		v _{cc} -	2		
Voн	$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
VOH	$V_{CC} = 4.5 V$,	I _{OH} = -12 mA	2						
	$V_{CC} = 4.5 V$	$I_{OH} = -15 \text{ mA}$,	2			
VOL	$V_{CC} = 4.5 V$	$I_{OL} = 12 \text{ mA}$		0.25	0.4				v
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 24 mA	1				0.35	0.5	V
Ιį	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
lн	$V_{CC} = 5.5 V$,	$V_1 = 2.7 \text{ V}$			20			20	μΑ
I _I L	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
10 [‡]	$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	- 30		-112	- 30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V ₁ = 4.5 V		3	6		3	6	mA
ICCL	V _{CC} = 5.5 V,	$V_I = 0 V$		8	14		8	14	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 $^{\circ}$ C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}=4.5$ V to 5.5 V, $C_L=50$ pF, $R_L=500$ Ω , $T_A=MIN$ to MAX		$C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$		V,	UNIT
			SN54A	LS1034	SN74A	LS1034	i	
			MIN	MAX	MIN	MAX		
tPLH		V	1	11	1	8		
tPHL	A	, Y	1 .	13	1	8	ns	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

recommended operating conditions

		SN	SN54AS1034A			SN74AS1034A		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-40			-48	mA
loL	Low-level output current			40			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	54AS10	34A	SN7	UNIT		
PARAMETER			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	l _l = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
V	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -40 \text{ mA}$	2						
	$V_{CC} = 4.5 V,$	$I_{OH} = -48 \text{ mA}$				2			
V	$V_{CC} = 4.5 V$,	$I_{OL} = 40 \text{ mA}$		0.25	0.5				V
VOL	$V_{CC} = 4.5 V$,	I _{OL} = 48 mA					0.35	0.5]
Ц	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ήн	$V_{CC} = 5.5 V,$	V ₁ = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.5			-0.5	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 200	- 50		- 200	mA
ICCH	$V_{CC} = 5.5 V,$	V _I = 4.5 V		9	15		9	15	mA
ICCL	$V_{CC} = 5.5 V,$	V ₁ = 0 V		21	35		21	35	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _I R _I	CC = 4.5 \ L = 50 pF, _ = 500 Ω, _ = MIN to AS1034A MAX	MAX	S1034A MAX	UNIT
^t PLH	A or B	V	1	6.5	1	6	ns
^t PHL	7010	, t	1	6.5	1	6	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS1035, SN74ALS1035 HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

D2661, APRIL 1982-REVISED MAY 1986

- Noninverting Buffers with Open-Collector Outputs
- Package Options Include Plastic "Small Outline"
 Packages, Ceramic Chip Carriers, and Standard Plastic
 and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent noninverting buffers. They perform the boolean functions Y=A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher $V_{\mbox{OH}}$ levels.

The SN54ALS1035 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1035 is characterized for operation from 0 $^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each buffer)

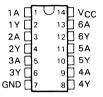
INPUT	OUTPUT
Α	Y
Н	Н
L	L

logic symbol[†]

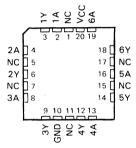
1A (1)	D Q	(<u>2)</u> 1Y
2A (3) 3A (5)		(4) 2Y (6) 3Y
4A (9)		(8) 4Y
5A (11) 6A (13)		(10) 5Y (12) 6Y
٠,		٠,

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

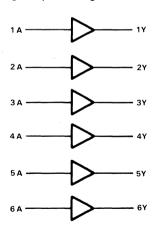
SN54ALS1035 . . . J PACKAGE SN74ALS1035 . . . D OR N PACKAGE (TOP VIEW)



SN54ALS1035 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC		7 V
Input voltage		7 V
Off-state output voltage		7 V
Operating free-air temperature range	SN54ALS1035	5°C
	SN74ALS1035	0°C
Storage temperature range	- 65 °C to 150	o o c

recommended operating conditions

		SI	SN54ALS1035		SN74ALS1035			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Voн	High-level output voltage			5.5			5.5	V
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS	1035	SN	74ALS1	035	UNIT
	IESI C	UNDITIONS	MIN TYP†	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 V,$	l _l = -18 mA		-1.5			-1.5	٧
ЮН	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V		0.1			0.1	mA
V	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA	0.25	0.4		0.25	0.4	→ ∨
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA				0.35	0.5	
I _I	$V_{CC} = 5.5 V,$	V ₁ = 7 V		0.1			0.1	mA
lн	$V_{CC} = 5.5 V$,	$V_1 = 2.7 V$		20			20	μΑ
lir.	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$		-0.1			-0.1	mA
Іссн	$V_{CC} = 5.5 V$,	V _I = 4.5 V	3	6		3	6	mA
^I CCL	$V_{CC} = 5.5 V_{c}$	V _I = 0 V	8	14		8	14	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4.5 C _L = 50 pF R _L = 680 S T _A = MIN t LS1035 MAX	, ?, o MAX	ALS1035 MAX	UNIT
^t PLH	_	V	5	35	5	30	ns
^t PHL	Α	Y	2	14	2	12	115



SN54AS1036A, SN74AS1036A QUADRUPLE 2-INPUT POSITIVE-NOR DRIVERS

D2661, DECEMBER 1983-REVISED MAY 1986

- Quad Versions of AS805B
- Offers High Capacitive-Drive Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

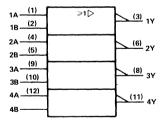
These devices contain four independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A} + \overline{B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54AS1036A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74AS1036A is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В] Y
Н	Х	L
X	Н	L
L	L	н ।

logic symbol



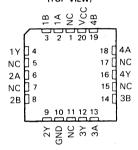
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

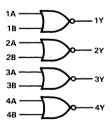
SN54AS1036A . . . J PACKAGE SN74AS1036A . . . D OR N PACKAGE (TOP VIEW)

_		
1A 🔲	1 🔾 14	□vcc
1B 🔲 :	2 13] 4B
1Y 🛚	3 12	□4A
2A 🛛	4 11] 4Y
2B 🔲	5 10] 3B
2Y 🛮 🤅	5 9] 3A
IND []	7 8	□ 3Y

SN54AS1036A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54AS1036A -55 °C to 125 °C SN74AS1036A 0 °C to 70 °C Storage temperature range -65 °C to 150 °C

recommended operating conditions

		SN	SN54AS1036A			SN74AS1036A		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-40			-48	mA
lOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	SN54AS1036A			SN74AS1036A		
			MIN	TYPt	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2	-		
V	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		٧
VOH	$V_{CC} = 4.5 V,$	$I_{OH} = -40 \text{ mA}$	2						
	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -48 mA				2			
Va.	$V_{CC} = 4.5 V,$	$I_{OL} = 40 \text{ mA}$		0.25	0.5				-
VOL	$V_{CC} = 4.5 V,$	$I_{OL} = 48 \text{ mA}$					0.35	0.5	
Ŋ	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1			0.1	mA
hH '	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.5			-0.5	mA
10‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 50		- 200	- 50		- 200	mA
Іссн	$V_{CC} = 5.5 V,$	$V_I = 0 V$		4.3	7		4.3	7	mA
^I CCL	$V_{CC} = 5.5 V,$	$V_{I} = 4.5 V$		14	23		14	23	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _I R _I	CC = 4.5 N = 50 pF, = 500 Ω , $\Lambda = MIN \text{ to}$ MAX	MAX	, AS1036A MAX	UNIT
^t PLH	A or B	Υ	1	4.8	1	4.3	ns
^t PHL	7 31 5		1	4.8	1	4.3	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54AS1181, SN74AS1181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D1915, MAY 1985-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:

Addition

Subtraction

Shift Operand A One Position

Magnitude Comparison

Plus Twelve Other Arithmetic Operations

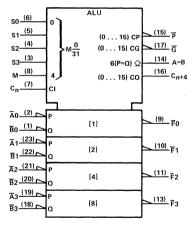
- Logic Function Modes
 - Exclusive-OR

Comparator

AND, NAND, OR, NOR

 Dependable Texas Instruments Quality and Reliability

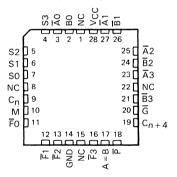
logic symbol †



SN54AS1181 . . . JT OR JW PACKAGE SN74AS1181 . . . DW, NT, OR NW PACKAGE (TOP VIEW)

		_
Во∐¹	U 24	J ∨cc
Āo □2	23	∏ Ā1
S3 🔲 3	22	☐ <u>B</u> 1
S2 🛛 4	21	∏ Ā2
S1 🔲 5	20] <u>B</u> 2
SO 🔲 6	19	ĪĀЗ
C _n 🔲 7	18	_ ₹3
М 🔲 в	17] <u>G</u>
Fo □ 9	16] C _{n + 4}
F1 □10	15	₽
F2 🛮 11	14	$\Box A = B$
GND 🛮 12	13] F 3

SN54AS1181 . . . FK PACKAGE SN74AS1181 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

TYPICAL ADDITION TIMES (C $_L$ = 15 pF, R $_L$ = 280 $\Omega,\ T_{\mbox{\scriptsize A}}$ = 25 $^{o}\mbox{\scriptsize C}$

NUMBER		ADDITION TIMES		PACK	CARRY METHOD		
OF	USING 'AS1181	USING 'AS181A	USING 'S181	ARITHMETIC	LOOK-AHEAD	BETWEEN	
BITS	AND'AS882	AND 'AS882	AND 'S182	LOGIC UNITS	CARRY GENERATORS	ALUs	
1 to 4	5 ns	5 ns	11 ns	1		NONE	
5 to 8	10 ns	10 ns	18 ns	2		RIPPLE	
9 to 16	14 ns	14 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD	
17 to 64	19 ns	19 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD	

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, JW, NT, and NW packages.

description

The 'AS1181 arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS1181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	ĀO	Вo	Ā1	B ₁	Ā2	B2	Ā3	B3	ĒΟ	F1	F2	F 3	Cn	C_{n+4}	P	G
Active-high data (Table 2)	A0	во	Α1	В1	A2	B2	А3	В3	FO	F1	F2	F3	Ĉn	Ĉ _{n + 4}	Х	Υ

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'AS1181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with $C_n=H$ when performing this comparison. The A=B output is open-collector so that it can be wired-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

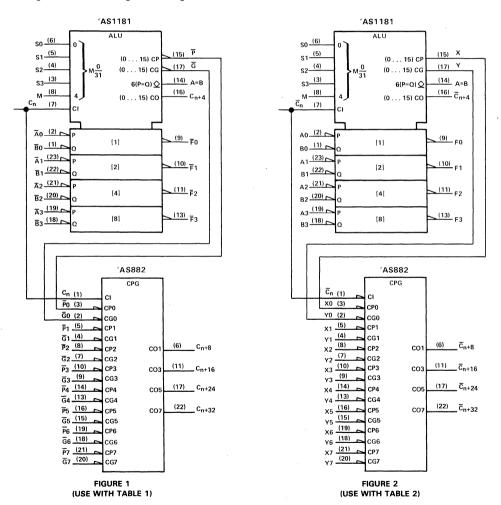
	INPUT C _n	OUTPUT Cn+4	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
İ	Н	Н	A≥B	A≤B
	Н	L	A < B	A>B
	L	н	A > B	A < B
	L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.



signal designations

In both Figures 1 and 2, the polarity indicators () indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS1181 together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.



Pin numbers shown for the 'AS1181 are for DW, JT, JW, NT, and NW packages.



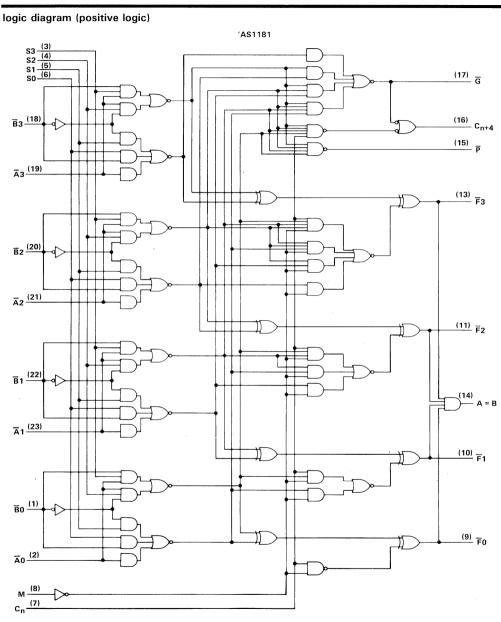
TABLE 1

		710			ACTIVE-LOW [DATA
3	ELEC	-110	N	M = H	M = L; ARITHME	TIC OPERATIONS
				LOGIC	C _n = L	C _n = H
53	S2	31	30	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F = Ā	F = A MINUS 1	F = A
L	L	L	н	F = \overline{AB}	F = AB MINUS 1	F = AB
L	L	Н	L	F = A + B	F = AB MINUS 1	F = AB
L	L	Н	н	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	Н	. L	L	F = A + B	F = A PLUS (A + B)	F - A PLUS (A + B) PLUS 1
L	Н	L	H	F = B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
L	Н	Н	L	F = A + B	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	Н	н	F = A + B	F = A + B	F = (A + B) PLUS 1
Н	L.	L	L	F = ĀB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
н	L	L	Н	F=A	F = A PLUS B	F = A PLUS B PLUS 1
н	L	н	L	F≂B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
н	L	Н	н	F = A + B	F = (A + B)	F = (A + B) PLUS 1
Н	Н	L	L	F = 0	F = A PLUS A †	F = A PLUS A PLUS 1
н	Н	L	Н	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	Н	н	L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
н	Н	Н	Н	F = A	F = A	F = A PLUS 1

TABLE 2

	LEC				ACTIVE-HIGH [DATA
56	LEC	, 110	110	M = H	M = L; ARITHME	TIC OPERATIONS
62				LOGIC	C _n = H	Ĉ _n = L
33	S2	51	50	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F≈Ā	F = A	F = A PLUS 1
L	L	L	H	F = A + B	F = A + B	F = (A + B) PLUS 1
L	L	н	L	F = ĀB	F = A + B	F = (A + B) PLUS 1
L	L	Н	Н	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	Н	L	L	F = AB	F = A PLUS AB	F = A PLUS AB PLUS 1
L	Н	L	Н	F = B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
L	н	Н	L	F - A ⊕ B	F = A MINUS B MINUS 1	F - A MINUS B
L	Н	Н	Н	F = AB	F = AB MINUS 1	F = AB
н	L	L	L	F = A + B	F = A PLUS AB	F = A PLUS AB PLUS 1
н	L	L	Н	F = A + B	F = A PLUS B	F = A PLUS B PLUS 1
н	L	Н	L.	F = B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
н	L	н	Н	F = AB	F = AB MINUS 1	F = AB
н	н	L	L	F = 1	F = A PLUS A †	F = A PLUS A PLUS 1
н	Н	L	Н	F = A + B	F = (A + B) PLUS A	F : (A + B) PLUS A PLUS 1
н	Н	Н	L	F = A + B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
н	н	н	н	F = A	F = A MINUS 1	F = A

 $^{^{\}dagger}\text{Each}$ bit is shifted to the next more significant position.



Pin numbers shown are for DW, JT, JW, NT, and NW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	
Supply voltage, VCC	V
Input voltage	✓
Off-state output voltge (A = B output only)	V
Operating free-air temperature range: SN54AS118155°C to 125°C	2
SN74AS1181 0 °C to 70 °C	С
Storage temperature range	2

recommended operating conditions

			SI	154AS1	181	SN	74AS11	81	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
Vон	High-level output voltage	A = B output only			5.5			5.5	V
^І он	High-level output current	All outputs except $A = B$ and \overline{G}			- 2			- 2	mA
0		G output			- 3			- 3	mA
		All outputs except G			20			20	mA
IOL	Low-level output current	G output			48			48	mA
TA	Operating free-air temperatu	re	- 55		125	0		70	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ADAMETED	TECT CONDI	TIONIC	SI	154AS1	181	SI	174AS1	181	UNIT
'	PARAMETER	TEST CONDI	HUNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
Vон	Any output except A = B	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	v _{cc} -	2		v _{cc} -	2		V
i	G	$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3		2.4	3		V
ЮН	A = B	$V_{CC} = 4.5 V,$	V _{OH} = 5.5 V			0.1			0.1	mA
VOL	Any output except \overline{G}	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	G	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 48 mA		0.4	0.5		0.4	0.5	V
	M input					0.1			0.1	
۱.	Any A or B input	$V_{CC} = 5.5 \text{ V},$	V 7 V			0.3			0.3	mA
lı lı	Any S input	VCC = 5.5 V,	V - / V			0.4			0.4] '''^
	Carry input					0.6			0.6	
	M input					20			20	
	Any A or B input	V _{CC} = 5.5 V,	V 2.7.V			60			60	μΑ
ΉΗ	Any S input	VCC = 5.5 V,	V = 2.7 V			80			80	μΑ
	Carry input					120			120	
	M input					-0.5			- 0.5	
l	Any A or B input	$V_{CC} = 5.5 V$	V 0.4 V			- 1.5			- 1.5	mA
IIL.	Any S input	VCC = 5.5 V,	V - 0.4 V			- 2			- 2] ""A
	Carry input	<u> </u>				- 3			- 3	
	All outputs except			- 30		- 112	- 30		-112	
lo‡	$A = B$ and \overline{G}	$V_{CC} = 5.5 V$,	$V_O = 2.25 V$							mA
	G			- 30		- 125	- 30		-125	
1cc		V _{CC} = 5.5 V			74	117		74	117	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

^{*}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IQS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	($V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $R_A = MIN \Omega$ AS1181	, o MAX	V, AS1181	UNIT
				MIN	MAX	MIN	MAX	1
[†] PLH				3	9	3	8.5	†
tPHL t	- C _n	Cn+4		2	7	2	6.5	ns
^t PLH	Any		M = 0 V, S1 = S2 = 0 V,	3.5	13	5	12	—
^t PHL	A or B	C _{n+4}	$S0 = S3 = 4.5 \text{ V } (\overline{SUM} \text{ mode})$	3.5	12.5	5	12	ns
tPLH	, Any	6	M = 0 V, S0 = S3 = 0 V,	5	14.5	5	13	
tPHL	☐ A or B	C _{n+4}	S1 = S2 = 4.5 V (DIFF mode)	5	13.5	5	12.5	ns
tPLH	+			3	10.5	3	9	<u> </u>
tPHL	C _n	Any F	M = 0 V (SUM or DIFF mode)	3	8	3	7.5	ns
tPLH	Any	G	M=0 V, S1=S2=0 V,	3	8.5	3	8	
[†] PHL	A or B	G	$S0 = S3 = 4.5 \text{ V } (\overline{\text{SUM}} \text{ mode})$	2	7	2	6	ns
tPLH	Any	G	M = 0 V, S0 = S3 = 0 V,	3	10.5	3	9.5	T
tPHL	A or B		S1 = S2 = 4.5 V (DIFF mode)	2	9	2	7	ns
tPLH	Any	P	M = 0 V, S1 = S2 = 0 V,	3	8.5	3	7.5	ns
^t PHL	A or B	[[$S0 = S3 = 4.5 \text{ V } (\overline{\text{SUM}} \text{ mode})$. 2	7.5	2	6	l lis
^t PLH	Any	P	M=0 V, S0=S3= 0 V,	3	10.5	3	9	
^t PHL	A or B		S1 = S2 = 4.5 V (DIFF mode)	3	8.5	3	8	ns
^t PLH	Ai or	Fi	M=0 V, S1=S2= 0 V,	3	11	3	9.5	ns
^t PHL	Bi	F' .	$S0 = S3 = 4.5 \text{ V } (\overline{\text{SUM}} \text{ mode})$	3	9	3	7.5] '''s
^t PLH	Āi or	Fi	M = 0 V, S0 = S3 = 0 V,	3	12	3	10.5	ns
^t PHL	Bi		S1 = S2 = 4.5 V (DIFF mode)	3	11	3	9.5	""
^t PLH	Any	Any F	M = 0 V, S1 = S2 = 0 V,	3	13.5	3	12	ns
^t PHL	A or B	Ally I	S0 = S3 = 4.5 V (SUM mode)	3	13	3	11.5] "
^t PLH	Any	Any F	M = 0 V, $S0 = S3 = 0 V$,	3	16	3	14.5	ns
^t PHL	A or B	Z.11 y 1	S1 = S2 = 4.5 V (DIFF mode)	3	13	3	12.5	1113
^t PLH	Āi or	Fi	M = 4.5 V (LOGIC mode)	3	12.5	3	11	ns
^t PHL	Bi	``		3	10	3	9.5	
^t PLH	Any	A=B	M = 0 V, S0 = S3 = 0 V,	4	19	4	17	ns
^t PHL	A or B		S1 = S2 = 4.5 V (DIFF mode)	5	18.5	5	15	
tPLH tPLH	Any S	Any F	M = 0 V (ARITH mode)	3	12.5	3	11	ns
^t PHL				3	11.5	3	11	<u> </u>
^t PLH	Any S	A=B	M = 0 V (ARITH mode)	5	20	5	18	ns
^t PHL	<u> </u>			5	21	5	18	<u> </u>
^t PLH	Any S	Cn+4	M = 4.5 V (LOGIC mode)	2	16.5	4.5	15.5	ns
tPHL .	<u> </u>			3	12.5	3	12	<u> </u>
^t PLH	Any S	G	$M = 0 V (\overline{ARITH} \text{ mode})$	3	9.5	3	9	ns
tPHL	 				6.5	2		<u> </u>
tPLH	Any S	P	M = 4.5 V (LOGIC mode)	3	8.5	3	7.5	ns
t _{PHL}	 	-	61 62 0 1		6.5	2	6.5	
t _{PLH}	М	Any F	- S1 = S2 = 0 V,	5	12	5	11.5	ns
tPHL .	 		S0 = S3 = 4.5 V (SUM mode) S1 = S2 = 0 V.	7	12	5	11.5	
tPLH	М	A = B			19	·	17.5	ns
^t PHL			S0 = S3 = 4.5 V (SUM mode)	8	21	8	17.5	



PARAMETER MEASUREMENT INFORMATION

SUM MÖDE TEST TABLE FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT		R INPUT E BIT	OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM
PANAMETER	TEST	APPLY	APPLY	APPLY	APPLY	TEST	(SEE NOTE 1)
		4.5 V	GND	4.5 V	GND		
^t PLH	Āi	Bi	None	Remaining Ā and B	Cn	Fi	In-Phase
^t PHL		ļ					
tPLH	Bi	Āi	None	Remaining A and B	C _n	Fi	In-Phase
tPHL .				A and B			
^t PLH	Āi	Bi	None	None	Remaining	P	In-Phase
^t PHL					\overline{A} and \overline{B} , C_n		
[†] PLH	Bi	Āi	None	None	Remaining	P	In-Phase
^t PHL] .) ^:·	140710	140110	\overline{A} and \overline{B} , C_n	· ·	liii i iiuse
^t PLH	Āi	None	Bi	Remaining	Remaining	G	In-Phase
^t PHL	1	None	ы	B	\overline{A} , C_n	G	in-riiase
^t PLH	Bi	None	Āi	Remaining	Remaining	G	- 5
^t PHL	В	None	Ai	B	Ā, C _n	G	In-Phase
[†] PLH				All	All	Any F	. 51
^t PHL	C _n	None	None	Ā	B	or C _{n+4}	In-Phase
[†] PLH	Āi	None	Bi	Remaining	Remaining	6 .	Out-of-Phase
^t PHL	A	None	DI DI	B	Ā, C _n	C _{n + 4}	Out-of-Phase
^t PLH	Bi	None	Āi	Remaining	Remaining	C .	Out-of-Phase
[†] PHL	1 5	None	AI	B	Ā, C _n	C _{n + 4}	Out-of-Phase
[†] PLH	Any	None	Bi	Remaining	Remaining	Any	In-Phase
[†] PHL	Ā	None	ы	B̄, Ā3	Ā, Cn	F	in-Phase
tPLH	Any	None	Āi	Remaining	Remaining	Any	In-Phase
^t PHL	B	None		Ā, <u>B</u> 3	B, Cn	F	in-rhase

PARAMETER MEASUREMENT INFORMATION

DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER	-,	R INPUT E BIT	OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM
PANAMETER	TEST	APPLY	APPLY	APPLY	APPLY	TEST	(SEE NOTE 1)
	1531	4.5 V	GND	4.5 V	GND	1691	(SEE NOTE I)
^t PLH	Āi	None	Bi	Remaining	Remaining	Fi	In-Phase
^t PHL		None	, Di	Ā	¯B, C _n		iii i iiasc
tPLH	Bi	Āi	None	Remaining	Remaining	Fi	Out-of-Phase
^t PHL] "	Λ'	None	Ā	B̄, C _n	, , ,	Out-or-mase
t _{PLH}	Āi	None	Bi	None	Remaining	P	In-Phase
[†] PHL		TVOITE	Di	140110	\overline{A} and \overline{B} , C_n	·	III T TIGGE
^t PLH	Bi	Āi	None	None	Remaining	Ē	Out-of-Phase
^t PHL		Α'	None	None	\overline{A} and \overline{B} , C_n		Out of Friday
^t PLH	Āi	Bi	None	None	Remaining	G	In-Phase
^t PHL	/ "	5	140110	140110	\overline{A} and \overline{B} , C_n		III T TIGGO
^t PLH	Bi	None	Āi	None	Remaining	G	Out-of-Phase
^t PHL]		/ \"		\overline{A} and \overline{B} , C_n		out or ridge
t _{PLH}	Āi	None	Bi	Remaining	Remaining	A = B	In-Phase
[†] PHL	/ "		J.	Ā	B, C _n	Λ υ	
, ^t PLH	Bi	Āi	None	Remaining	Remaining	A = B	Out-of-Phase
^t PHL		, ,	140110	Ā	B, C _n		out or ridge
^t PLH	Cn	None	None	All	None	C _{n+4} _	In-Phase
^t PHL	. "	140110	140770	A and B		or any F	
tPLH	Āi	Bi	None	None	Remaining	C _{n+4}	Out-of-Phase
t _{PHL}	1	5	110.10	110110	Ā, B, C _n	911+4	out or muse
t _{PLH}	Bi	None	Āi	None	Remaining	C _{n+4}	In-Phase
^t PHL		140110	/ "	110110	Ā, Ħ, C _n		III T TIGOS
^t PLH	Any	Bi	None	Ā3	Remaining	Any	In-Phase
^t PHL	Ā	<u> </u>		,	Ā, Ħ, C _n	F	
t _{PLH}	Any	None	Āi	Āз	Remaining	Any	Out-of-Phase
^t PHL	B				Ā, B̄, C _n	F	

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER	OTHER SAM	INPUT E BIT	OTHER I	DATA INPUTS	OUTPUT	OUTPUT WAVEFORM
I ANAMETER	TEST	APPLY	APPLY	APPLY	APPLY	TEST	(SEE NOTE 1)
	1531	4.5 V	GND	4.5 V	GND	1531	(SEE NOTE 1)
^t PLH	Āi	B	None	None	Remaining	Fi	Out-of-Phase
^t PHL			None	None	A and B, C _n		Out-or-rhase
^t PLH	Bi	Āi	None	None	Remaining	Fi	Out-ot-Phase
[†] PHL	ы	AI AI	None	None	A and B, C _n		Out-ot-rhase

INPUT BITS EQUAL/NOT EQUAL TEST TABLE FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

DADAMETER	INPUT	OTHER SAM		OTHER DAT	A INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM
PARAMETER	UNDER	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	(SEE NOTE 1)
tPLH tPHL	Āi	Bi	None	Remaining Ā and B̄, C _n	None	P	Out-of-Phase
tPLH tPHL	Bi	Āi	None	Remaining \overline{A} and \overline{B} , C_n	None	P	Out-of-Phase
tPLH tPHL	Āi	None	Bi	Remaining Ā and B̄, C _n	None	P	In-Phase
^t PLH ^t PHL	Bi	None	Āi	Remaining Ā and B̄, C _n	None	P	In-Phase
tPLH tPHL	Āi	Bi	None	Remaining \overline{A} and \overline{B} , C_n	None	C _{n+4}	In-Phase
^t PLH ^t PHL	Bi	Āi	None	Remaining \overline{A} and \overline{B} , C_n	None	C _{n+4}	In-Phase
tPLH tPHL	Āi	None	Bi	Remaining A and B, Cn	None	C _{n+4}	Out-of-Phase
tPLH tPHL	Bi	None '	Āi	Remaining A and B, Cn	None	C _{n+4}	Out-of-Phase

INPUT PAIRS HIGH/NOT HIGH TEST TABLE FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0V

PARAMETER	INPUT UNDER		R INPUT IE BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT	
	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5V	APPLY GND	TEST	(SEE NOTE 1)	
^t PLH	Āi	Bi	None	Remaining	Remaining	P	In-Phase	
tPHL tPLH		Āi		Ā, C _n Remaining	Remaining	Ē	la Obassa	
tPHL	Ві	Ai	None	B̄, Cn	Ā	Р	In-Phase	
tPLH	Āi	Bi	None	Remaining	Remaining	C _{n+4}	Out-of-Phase	
^t PHL		J.	1,101.0	Ā, C _n	B	-11-4	+4 0401111400	
tPLH	Bi	Āi	None	Remaining	Remaining	C _{n+4}	Out-of-Phase	
tPHL	, 51	"	1	B, C _n	A	-11+4]	



PARAMETER MEASUREMENT INFORMATION

SELECT INPUT/LOGIC MODE TEST TABLE FUNCTION INPUTS: M = 4.5 V

PARAMETER	INPUT UNDER	1	INPUT E BIT	OTHER DA	TA INPUTS	OUTPUT UNDER	OUTPUT WAVEFORM	
FANAIVIETEN .	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	(SEE NOTE 1)	
tPLH tPHL	Any S	-	_	Remaining B	Ā, Bo, C _n	C _{n+4}	Out-of-Phase	
tPLH tPHL	Any S	_		B, Ā2	Remaining A, C _n	P	In-Phase	

SELECT INPUT/ARITH MODE TEST TABLE FUNCTION INPUTS: M = 0 V

PARAMETER	INPUT UNDER	I	R INPUT E BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT	
PANAIVIETEN	TEST	APPLY APPLY		APPLY 4.5 V	APPLY GND	TEST	(SEE NOTE 1)	
^t PLH	Any			Remaining	Ão, Bo	Any	In-Phase	
^t PHL	S			A and B, C _n	A0, B0	F	III-Filase	
^t PLH	Any			Remaining	Ão, Bo	A≔B	In-Phase	
^t PHL	s	_	_	A and B, C _n	AU, BU	A=D	in-Filase	
^t PLH	Any			Remaining	Ão, Bo	G	In-Phase	
^t PHL	s	_	_	A and B, C _n	A0, B0		in-Friase	

MODE INPUT/SUM MODE TEST TABLE FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = 0 V

PARAMETER	INPUT UNDER		E BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT WAVEFORM
TANAMETER	TEST	APPLY 4.5 V	APPLY GND	APPLY APPLY 4.5 V GND		TEST	(SEE NOTE 1)
tPLH	М			Remaining	B 2, A 2, C n	Any	In-Phase
^t PHL				A and B	B2, A2, On	F	III-I IIdae
^t PLH	М	_	_	Remaining	B1, A1, Cn	A = B	In-Phase
tPHL				A and B	B1, A1, Cn	A-0	III-I IIase



SN54ALS1240, SN74ALS1240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- Low-Power Version of 'ALS240A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{\mathbb{G}}$ (active-low output control) inputs, and complementary \mathbb{G} and $\overline{\mathbb{G}}$ inputs. These devices feature high fan-out and improved fan-in.

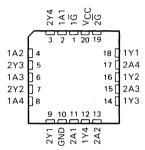
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1240 is characterized for operation from 0°C to 70°C.

SN54ALS1240 . . . J PACKAGE SN74ALS1240 . . . DW OR N PACKAGE (TOP VIEW)

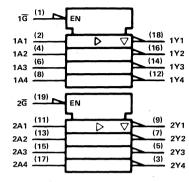
1Ğ [1	U20		Vcc
1A1 [2	19		2Ğ
2Y4 🗌	3	18		1Y1
1A2 [4	17		2A4
2Y3 [5	16		1Y2
1A3 [6	15		2A3
2Y2 [7	14		1Y3
1A4 [8	13		2A2
2Y1 [9	12		1Y4
GND [10	11	П	2A1

SN54ALS1240 . . . FK PACKAGE
(TOP VIEW)



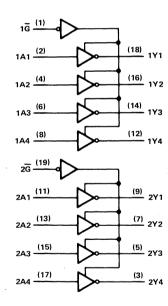


logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54ALS1240, SN74ALS1240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS1240
SN74ALS1240
Storage temperature range

recommended operating conditions

			SN54ALS1240			SN74ALS1240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	ONT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			>
VIL	Low-level input voltage				0.7			0.8	V
Іон	High-level output current	,			- 12			- 15	mA
					8			16	
lOL	Low-level output current					24†	mA		
TA	Operating free-air temperature		- 55		125	0		70	°C

 $^{^{\}dagger}$ The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.

The 24-mA limit applies for the SN74ALS1240-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	IDITIONS	SN	54ALS1	240	SN	74ALS1	240	UNIT	
PANAMETER	TEST CON	DITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	ONIT	
V _{IK} .	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			- 1.2	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2		3	V _{CC} -2				
Vou	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v	
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2						,	
	$V_{CC} = 4.5 V,$	$I_{OH} = -15 \text{ mA}$				2				
	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA		0.25	0.4		0.25	0.4		
V _{OL}	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 16 \text{ mA}$					0.35	0.5	v	
	(I _{OL} = 24 mA for -1 ve	<u> </u>				0.00	0.0			
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ	
IOZL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			- 20			- 20	μΑ	
. 4	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
liH\$	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ	
I _{IL} §	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			- 0.1	mA	
10¶	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA	
		Outputs high		5	8		5	8		
1cc	V _{CC} = 5.5 V	Outputs low		8.5	14		8.5	14	mA	
		Outputs disabled		8.1	13		8.1	13		

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C 'ALS1240	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to LS1240	MAX	/, ALS1240 MAX	UNIT
tPLH		V	7.5	2	16	2	13	
^t PHL	A	Y	6.5	2	16	2	13	ns
^t PZH	G		11.5	4	23	4	20	
^t PZL]	Y	14	6	28	6	22	ns
[†] PHZ	G	V	7.5	2	12	2	10	ns
[†] PLZ		•	8	3	18	3	13	1115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS1242, SN74ALS1242 OUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- 2-Way Asynchonous Communication Between Data Buses
- P-N-P Inputs Reduce DC Loading
- Low-Power Version of 'ALS242
- Three-State Outputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil
- Dependable Texas Instruments Quality and Reliability

description

These quadruple bus transceivers are designed for two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{G}AB$).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'ALS1242 the capability to store data by simultaneous enabling of \$\overline{G}\$AB and \$\overline{G}\$BA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (8 in all) will remain at their last states. The 4-bit codes appearing on the two sets of buses will be complementary for the 'ALS1242.

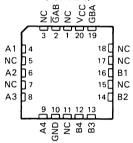
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54ALS1242 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1242 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS1242 . . . J PACKAGE SN74ALS1242 . . . D OR N PACKAGE (TOP VIEW)

GAB ☐	1	U 14]	Vcc
NC 🗌	2	13		GBA
A1 🛚	3	12]	NC
A2 🔲	4	11]	B1
АЗ 🗌	5	10]	B2
A4 🔲	6	9]	В3
GND [7	8]	B4

SN54ALS1242 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

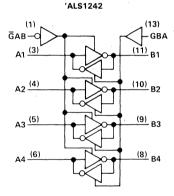
	GAB	GBA	OPERATION
	L	L	Ā to B
I	Н	Н	B̄ to A
	Н	L	Isolation
			Latch A and B
1	L	Н	$(A = \overline{B})$

logic symbol†

'ALS1242

 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage: All inputs
I/O ports
Operating free-air temperature range: SN54ALS1242 – 55°C to 125°C
SN74ALS1242 0 °C to 70 °C
Storage temperature range

SN54ALS1242, SN74ALS1242 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

		SN54ALS1242			SN	242	LINUT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			12			-15	mA
lou	Low-level output current			8			16	A
lOL							24 †	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}$ The 24-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEC	T COMPLETIONS	SN	54ALS1	242	SN	74ALS1	242	UNIT
	PANAIVIETEN	159	T CONDITIONS	MIN	TYP [‡]	MAX	MIN	TYP‡	MAX	UNII
VIK	<	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	V , $I_{OH} = -0.4 \text{ mA}$	VCC -	2		V _{CC} -2	2		
V _o		$V_{CC} = 4.5 V$,		2.4	3.2		2.4	3.2		V
1	'n	$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2						ľ
		$V_{CC} = 4.5 V,$	0				2			
		$V_{CC} = 4.5 V,$	I _{OL} = -8 mA		0.25	0.4		0.25	0.4	
v_{OL}		$V_{CC} = 4.5 V$,	$I_{OL} = 16 \text{ mA}$					0.35	0.5	V
		$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 24 \text{ mA } (-1 \text{ Versions})$					0.35	0.5	
11	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
_		$V_{CC} = 5.5 V$,	$V_1 = 5.5 V$			0.1			0.1	
ΉН	Control inputs	$V_{CC} = 5.5 \text{ V},$	V ₁ = 2.7 V			20			20	μΑ
	A or B ports §		V - 2.7 V	l		20	ŀ		20	μ.
1	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	^
ηL	A or B ports§	νCC = 5.5 V,	V = 0.4 V			-0.1			-0.1	mA
10	ſ	V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
			Outputs high		8	14		8	12	
Icc	$V_{CC} = 5.5 V$	Outputs low		10	17		10	15	mA	
			Outputs disabled		9	16		9	14	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

 $[\]S$ For I/O ports, the parameters IIH and IIL include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}\text{C}$ 'ALS1242	$C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to } N$ $SN54ALS1242$		R1 = 500 Ω , R2 = 500 Ω , T _A = MIN to MAX		pF, 0 Ω, 0 Ω, N to MAX 2 SN74ALS1242		UNIT
	+		TYP 6	WIIN 2	14	MIN 2	12	 		
^t PLH	A or B	B or A						ns		
tPHL			5	2	12	2	10			
^t PZH	ĞАВ	В	10	4	20	4	17	ns		
t _{PZL}	J	, ь	13	5	23	5	21	'''		
^t PHZ	ĞАВ	В	6	2	12	2	10	ns		
tPLZ	7 GAB	Ь	5	2	12	2	10	l lis		
^t PZH	GBA	Α	12	5	23	5	20			
^t PZL	7 GBA	A	14	6	25	6	23	ns		
^t PHZ	GBA	Α	6	2	12	2	10			
[†] PLZ			6	2	15	2	12	ns		

SN54ALS1244A, SN74ALS1244A OCTAL BUFFER AND DRIVER WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- Low-Power Version of 'ALS244A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Plastic "Small Outline"
 Packages, Ceramic Chip Carriers, and Standard Plastic
 and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

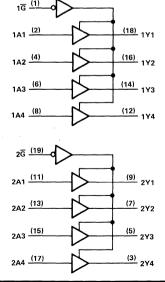
description

This octal buffer and line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS1240 this device provides the choice of selected combinations of inverting and noninverting outputs symmetrical \overline{G} (active-low input control) inputs, and complementary G and \overline{G} inputs.

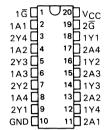
The -1 version of the SN74ALS1244A is identical to the standard version except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1244A.

The SN54ALS1244A is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1244A is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

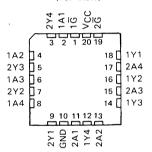
logic diagram (positive logic)



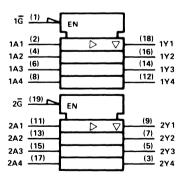
SN54ALS1244A . . . J PACKAGE SN74ALS1244A . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS1244A . . . FK PACKAGE (TOP VIEW)



logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC			7 V
Input voltage			7 V
	output		
Operating free-air temperature range:	SN54ALS1244A	-55°C to 12	5°C
	SN74ALS1244A	0°C to 70	0°C
Storago temperature range		-65°C to 150	೧೦೧

recommended operating conditions

		SN	54ALS1	244A	SN74ALS1244A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			- 12			- 15	mA
loL	Low-level output current			8			16	^
							24 [†]	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

 $^{^{\}dagger}$ The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V. The 24-mA limit applies for the SN74ALS1244A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		SN	54ALS1	244A	SN7	4ALS12	244A	UNIT	
PARAMETER	TEST CONDIT	IONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT	
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V	
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -0.4 mA	V _{CC} -	2		Vcc-	2			
∨он -	$V_{CC} = 4.5 V,$	IOH = -3 mA	2.4	3.2		2.4	3.2		v	
VOH [$V_{CC} = 4.5 V,$	IOH = -12 mA	2						·	
	V _{CC} = 4.5 V,	$I_{OH} = -15 \text{ mA}$				2				
	$V_{CC} = 4.5 V$	IOL = 8 mA		0.25	0.4		0.25	0.4		
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 16 mA					0.35	0.5	V	
	$(I_{OL} = 24 \text{ mA for} - 1 \text{ vers})$	ions)					0.35	0.5		
^I OZH	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$			20			20	μΑ	
lozL	V _{CC} = 5.5 V,	V _I = 0.4 V			- 20			- 20	μΑ	
l _l	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA	
ΉΗ	V _{CC} = 5.5 V,	$V_1 = 2.7 V$	7		20			20	μΑ	
IIL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA	
IO§	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA	
		Outputs high		6	15		6	11		
¹cc	$V_{CC} = 5.5 V$	Outputs low		10	20		10	17	mA	
1		Outputs disabled		11	25		11	20		

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.



^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54ALS1244A, SN74ALS1244A OCTAL BUFFER AND DRIVER WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = \text{MIN to MAX}$ $SN54ALS1244A = SN74ALS1244A$			
			SN544	ALS1244A	SN74		
	· ·		MIN	MAX	MIN	MAX	
t _{PLH}	А	V	3	21	3	14	ns
t _{PHL}	^	,	3	16	3	14	113
^t PZH	G	V	6	28	6	22	nc
· t _{PZL}	G	T	6	26	6	22	ns
^t PHZ	G	V	2	15	2	10	ns
tPLZ	3	1	3	25	3	13	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- 'Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Lower-Power Version of 'ALS245A
- 'ALS1245A is Identical to 'ALS1645A
- Package Options Include Plastic "Small Outline"
 Packages, Ceramic Chip Carriers, and Standard Plastic
 and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

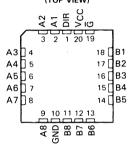
The -1 version of the SN74ALS1245A is identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1245A.

The SN54ALS1245A is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS1245A is characterized for operation from 0 °C to 70 °C.

SN54ALS1245A . . . J PACKAGE SN74ALS1245A . . . DW OR N PACKAGE (TOP VIEW)

DIR 🛛 1	∪ 20	□vcc
A1 □2	19	ŪĞ
A2 □3	18	□ B1
A3 □ 4	17	□ B2
A4 □5	16] вз
A5 🛮 6	15	_ B4
A6 🏻 7	14	B5
A7 🛮 8	13	<u>⊟</u> в6
A8 🗖 9	12	B7
GND 1	0 11	П вв

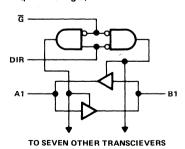
SN54ALS1245A . . . FK PACKAGE (TOP VIEW)



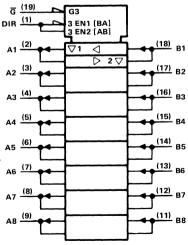
FUNCTION TABLE

1	TROL UTS	OPERATION
Ğ	DIR	1 .
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

logic diagram (positive logic)



logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V	•
Input voltage: All inputs	7 V	,
I/O ports	.5 V	1
Operating free-air temperature range: SN54ALS1245A	5°C	;
SN74ALS1245A 0°C to 7	0 ° C	;
Storage temperature range -65°C to 15	o o c	

recommended operating conditions

		SN54ALS1245A			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	[
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
loн	High-level output current			- 12			-15	mA
lo	Low-level output current			8			16	mA
lOL	Low-level output current						24†] "" [
TA	Operating free-air temperature	-55		125	0		70	°C

 $^{^{\}dagger}$ The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	********	TEGT COM	DITIONS	SNE	4ALS1	245A	SN	74ALS1	245A	LINUT
,	PARAMETER	TEST CONDITIONS		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.5			-1.5	V
		$V_{CC} = 4.5 \text{ V to } 5.5$	$5 \text{ V}, \text{ I}_{OH} = -0.4 \text{ mA}$	v _{cc} -	2		Vcc-	2		
\ \/ a		$V_{CC} = 4.5 \text{ V},$	$l_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
Voн		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$	2] *
		$V_{CC} = 4.5 \text{ V},$	$l_{OH} = -15 \text{ mA}$				2			
		$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 16 mA					0.35	0.5	\ \
1		(IOL = 24 mA for -	1 version)				}	0.55	0.5	L
1.	Control inputs	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
1 11	A, B ports§	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	'''^
1	Control inputs	VCC = 5.5 V,	V _I = 2.7 V			20			20	
ήн	A, B ports§	$\int_{VCC} = 9.9 \text{ V},$	V = 2.7 V			20			20	μA
1	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
l IIL	A, B ports§	$\int ACC = 0.2 \text{ A}$	VI = 0.4 V			-0.1			-0.1	11114
101		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA
			Output high		21	33		21	. 30	
lcc	V _{CC} = 5.5 V	Output low		23	36		23	33	mA	
			Output disabled		25	40		25	36	

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.



The 24-mA limit applies for the SN74ALS1245A-1 only.

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1245A, SN74ALS1245A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	!	$V_{CC} = 4.5 \text{ N}$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to}$	MAX		UNIT
				S1245A MAX		ALS1245A MAX	
			MIN		MIN		
^t PLH	A or B	B or A	2	19	2	13	ns
^t PHL	7 01 5	B 01 A	2	15	2	13	113
t _{PZH}	G	A or B	8	30	8	25	
^t PZL	· ·	A 01 B	8	29	8	25	ns
tPHZ	G	A or B	2	14	2	12	ns
[†] PLZ	9	AUID	3	30	3	18	IIS

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



SN54ALS1640A, SN74ALS1640A, SN54ALS1645A, SN74ALS1645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2661, DECEMBER 1982-REVISED MAY 1986

- Bidirectinal Bus Transceivers in High-Density 20-Pin Packages
- Lower-Power Versions of 'ALS640 Series
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

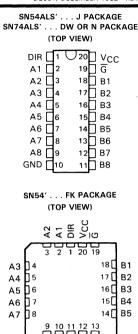
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so the buses are effectively isolated. The 'ALS1640A features inverting logic, while the 'ALS1645A features noninverting logic.

The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There are no -1 versions of the SN54ALS' parts.

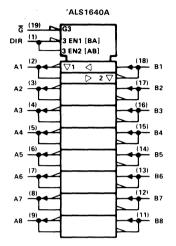
The SN54ALS' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS' family is characterized for operation from 0 °C to 70 °C.

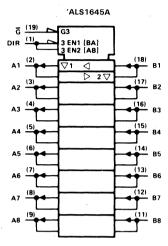
FUNCTION TABLE

	TROL PUTS	OPERA:	TION
Ğ	DIR	'ALS1640A	'ALS1645A
L	L	B data to A bus	B data to A Bus
L	Н	Ā data to B bus	A data to Bus
Н	Х	Isolation	Isolation



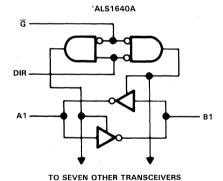
logic symbols†

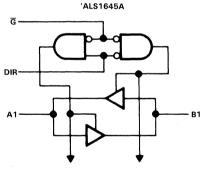




[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)





SN54ALS1640A, SN54ALS1645A SN74ALS1640A, SN74ALS1645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)
Supply voltage, VCC 7 V
Input voltage All inputs
I/O ports
Operating free-air temperature range: SN54ALS1640A, SN54ALS1645A 55°C to 125°C
SN74ALS1640A, SN74ALS1645A 0°C to 70°C
Storage temperature range65°C to 150°C

recommended operating conditions

		SN54ALS1640A		640A	SN7				
		SN	54ALS1	645A	SN7	4ALS16	45A	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
Іон	High-level output current			- 12			- 15	mA	
1	Low level output output			8			16	mΑ	
lOL	Low-level output current						24†] "''^	
TA	Operating free-air temperature	- 55		125	0		70	°C	

 $^{^{\}dagger}$ The 24-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		т	EST CONDITIONS		54ALS1 54ALS1		1	4ALS16		UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX]
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.5			- 1.5	V
		$V_{CC} = 4.5 \text{ V to } 5$.5 V, I _{OH} = -0.4 mA	Vcc	- 2		Vcc	- 2		
VOF		$V_{CC} = 4.5 V$,	I _{OH} = -3 mA	2.4	3.2		2.4	3.2] ,
VOF	1	$V_{CC} = 4.5 V$,	I _{OH} = -12 mA	2						7 '
		$V_{CC} = 4.5 V$,	I _{OH} = -15 mA				2			1
		$V_{CC} = 4.5 V$,	IOL = 8 mA		0.25	0.4		0.25	0.4	
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 16 mA					0.35	0.5] _v
		$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 24 \text{ mA} (-1 \text{ Versions})$					0.35	0.5	7
l _l	Control inputs	$V_{CC} = 5.5 V$,	V ₁ = 7 V			0.1			0.1	mA.
''	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	- IIIA
1	Control inputs	Vcc = 5.5 V,	V _I = 2.7 V			20			20	
ΉН	A or B ports§	vCC = 5.5 v,	V = 2.7 V			20			20	μΑ
1	Control inputs	V 5 5 V	V: - 0.4 V			-0.1			-0.1	mA
IL	A or B ports§	$V_{CC} = 5.5 V,$	V) = 0.4 V			-0.1			-0.1	7 ""
101		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		- 112	mA
	'ALS1640A	V _{CC} = 5.5 V			18	35		18	32	mA
ICC	'ALS1645A	VCC = 3.5 V			25	40		25	36	_ <i>'''A</i>



 $^{^{\}ddagger}All$ typical values are at VCC =5 V, TA $=25\,^{\circ}C.$ §For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1640A, SN74ALS1640A, SN54ALS1645A, SN74ALS1645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

'ALS1640A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$V_{CC} = 4$ $C_L = 50$ $R1 = 50$ $R2 = 50$ $T_A = MI$	pF, Ο Ω, Ο Ω, Ν to ΜΑ	×	UNIT
			SN54ALS1640A SN74ALS1640A			4ALS1640A	
			MIN	MAX	MIN	MAX	
tPLH	A or B	B or A	5	17	5	15	ns
[†] PHL	AOIB	BOIA	2	13	2	10	115
tPZH	G	A or B	5	23	5	20	ns
^t PZL		7 01 15	5	25	5	22	115
^t PHZ	G	A or B	2	12	2	10	ns
[†] PLZ		7 01 5	5	16	5	13	113

'ALS1645A switching characteristics (see Note 1)

PARAMETER	AMETER FROM TO (OUTPUT)			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = MIN \text{ to } MAX$ $SN54ALS1645A SN74ALS1645A$				
•			MIN	MAX	MIN	MAX	1	
tPLH		5	2	15	2	13		
^t PHL	A or B	B or A	2	15	2	13	ns	
^t PZH	Ğ	A or B	8	28	8	25		
^t PZL	9	AOIB	8	28	8	25	ns	
^t PHZ	G	A or B	2	14	2	12	ns	
^t PLZ		7016	3	22	3	18] '''	

SN54ALS1804A, SN54AS1804, SN74ALS1804A, SN74AS1804 **HEX 2-INPUT NAND DRIVERS**

AUGUST 1984-REVISED MAY 1986

- **High Capacitive Drive Capability**
- 'ALS1804A Has Typical Delay Time of 4 ns (CL = 50 pF) and Typical Power Dissipation of 3.4 mW per Gate
- 'AS1804 Has Typical Delay Time of 2.6 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 9 mW per Gate
- Center VCC and GND Configuration Provides Minimum Lead Inductance in High **Current Switching Applications**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil **DIPs**
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent 2-input NAND drivers. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The center pin configuration used in the 'ALS1804A and 'AS1804 provides a reduction of lead inductance when compared to the 'ALS804A and 'AS804B. This reduction of lead inductance will minimize noise generated onto either the VCC or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1804A and SN54AS1804 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1804A and SN74AS1804 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

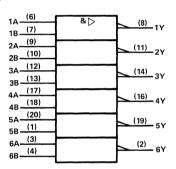
INP	UTS	OUTPUT
Α	В	Y
Н	Н	L
L	Х	н
Х	L	н

SN54ALS1804A, SN54AS1804 . . . J PACKAGE SN74ALS1804A, SN74AS1804 . . . DW OR N PACKAGE (TOP VIEW)

,		V.L.	• •		
5B [1	U 20	D	5A	,
6Y [2	19		5Y	
6A [3	18		4B	
6в [4	17		4A	
vcc 🗆	5	16	\Box	4Y	
1A [6	15		GNE)
1В 🗆	7	14		3Y	
1Y 🗌	8	13		3В	
2A 🗌	9	12	р	3А	
2B 🗌	10	11		2Y	

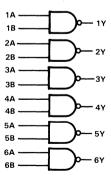
Use 'ALS804A or 'AS804B for chip carrier option.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54ALS1804A
	SN74ALS1804A
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS1804A			SN	UNIT		
		MIN NOM MAX MIN NOM MA 4.5 5 5.5 4.5 5 5 2 2 2 2 C -12 -12 - - 12 - 12 -	MAX	UNIT				
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
Іон	High-level output current	T		-12			- 15	mA
loL	Low-level output current	1		12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		SN	4ALS1	304A	SN7	4ALS18	304A	LINUT	
PARAMETER	TEST CONDIT	TIONS	MIN	TYP [†]	MAX	MIN	TYP†	MAX	UNIT	
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	٧	
[$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	Vcc-	- 2		Vcc-	2			
Va	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2]	
Voн	$V_{CC} = 4.5 V$	IOH -12 mA	2]	
	$V_{CC} = 4.5 V,$	I _{OH} - 15 mA				2				
VoL	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V	
VOL	$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5] <u> </u>	
l _i	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA	
ΊΗ	V _{CC} = 5.5 V,	V ₁ = 2.7 V			20			20	μΑ	
ΊL	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA	
10 [‡]	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.25$	- 30		-112	-30		-112	mA	
^I ССН	V _{CC} = 5.5 V,	V _I = 0 V		0.9	2.5		0.9	2.5	mA	
ICCL I	V _{CC} = 5.5 V,	V _I = 4.5 V		7	12		7	12	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25 ^{\circ}\text{C}$ 'ALS1804A TYP	C _L R _L T _A	C = 4.5 V = 50 pF, = 500 Ω = MIN to .S1804A MAX	MAX	, LS1804A MAX	UNIT
tPLH	A or B	V	4	2	9	2	7	ns
^t PHL	A OI B	. '	4	2	9	2	8	1115



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	<i></i> .	 	7 V
Input voltage		 	7 V
Operating free-air temperature range:	SN54AS1804	 	-55°C to 125°C
	SN74AS1804	 	0°C to 70°C
Storage temperature range		_	-65°C to 150°C

recommended operating conditions

		SN	SN54AS1804		SN74AS1804			LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-40			-48	mA
lOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

0404445750	TEST CONDITIONS		SN	SN54AS1804			SN74AS1804		
PARAMETER			MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
M	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		- v
Voн	$V_{CC} = 4.5 V,$	I _{OH} = -40 mA	2						
	$V_{CC} = 4.5 V,$	I _{OH} = -48 mA				2			
\/ -	$V_{CC} = 4.5 V,$	IOL = 40 mA		0.25	0.5				5 V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5	
l ₁	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ
IL	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.5			-0.5	mA
10 [‡]	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 200	- 50		- 200	mA
¹ ССН	$V_{CC} = 5.5 V,$	V ₁ = 0 V		3.5	5		3.5	5	mA
^I CCL	$V_{CC} = 5.5 V,$	V ₁ = 4.5 V		16	27		16	27	· mA

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _i R _i T,	CC = 4.5 V L = 50 pF, L = 500 Ω A = MIN to AS1804 MAX	MAX	AS1804 MAX	UNIT
^t PLH	A or B	V	1	5	1	4	
t _{PHL}	AUIB	· ·	1	. 5	1	4	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1805A, SN54AS1805, SN74ALS1805A, SN74AS1805 **HEX 2-INPUT NOR DRIVERS**

AUGUST 1984-REVISED MAY 1986

- High Capacitive Drive Capability
- 'ALS1805A Has Typical Delay Time of 4.2 ns (C_L = 50 pF) and Typical Power Dissipation of 4.2 mW per Gate
- 'AS1805 Has Typical Delay Time of 2.6 ns (CL = 50 pF) and Typical Power Dissipation of Less than 12 mW per Gate
- Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High **Current Switching Applications**
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil **DIPs**
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent 2-input NOR drivers. They perform the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A \cdot B}$ in positive logic.

The center pin configuration used in the 'ALS1805A and 'AS1805 provides a reduction of lead inductance when compared to the 'ALS805A and 'AS805B. This reduction of lead inductance will minimize noise generated onto either the VCC or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1805A and SN54AS1805 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1805A and SN74AS1805 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

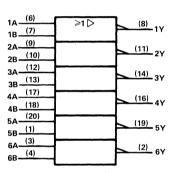
INP	UTS	ОИТРИТ
Α	В	Y
Н	X	L
X	Н	L
L	L	н

SN54ALS1805A, SN54AS1805 . . . J PACKAGE SN74ALS1805A, SN74AS1805...N PACKAGE

(TOP VIEW)							
5B		U 20] 5A				
6Y	□ 2	19] 5Y				
6A	3	18] 4B				
6B	□4	17] 4A				
Vcc	□5	16] 4Y				
1 A	□ 6	15	GNE				
1B	7	14] 3Y				
1Y	8	13] 3B				
2A	9	12] 3A				
2B	∐ 10	11] 2Y				

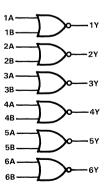
Use 'ALS805A or 'AS805B for chip carrier option.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS1805A -55°C to 125°C SN74ALS1805A 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		SN54ALS1805A			SN7	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ЮН	High-level output current			-12			- 15	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		SN5	4ALS18	05A	SN7	4ALS18	305A	UNIT
PARAMETER	TEST CONDI	ONDITIONS		TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	٧
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$l_{OH} = -0.4 \text{ mA}$	V _{CC} - 2			V _{CC} -2			
Va [$V_{CC} = 4.5 V$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2]
Voн	$V_{CC} = 4.5 V,$	$I_{OH} = -12 \text{ mA}$	2						1
	$V_{CC} = 4.5 V,$	I _{OH} = -15 mA				2			7
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5	7 °
lj .	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1		-	0.1	mA
ΉΗ	V _{CC} = 5.5 V,	V ₁ = 2.7 V			20			20	μΑ
ΊL	$V_{CC} = 5.5 V,$	$V_{ } = 0.4 \text{ V}$			-0.1			-0.1	mA
10‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30.		-112	- 30		-112	mA
Іссн	$V_{CC} = 5.5 V,$	V _I = 0 V		2	4		2	4	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		8	14		8	14	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$ 'ALS1805A TYP	SN54AL MIN	$V_{CC} = 4.5$ $C_L = 50 \text{ pl}$ $R_L = 500 \text{ s}$ $T_A = \text{MIN}$ $C_A = M_A$	F, ກໍ່, to MAX	LS1805A MAX	UNIT
tPLH	A or B		4	2	9	2	7	ns
^t PHL	AUID		5	2	10	2	8	113



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}	′ V
Input voltage	′ V
Operating free-air temperature range: SN54AS1805	°C
SN74AS1805	°C
Storage temperature range	°C

recommended operating conditions

		SI	SN54AS1805			SN74AS1805		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage		-	0.8			0.8	V
ЮН	High-level output current			-40			-48	mA
lOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise

PARAMETER	TEST CONDI	TIONS	SN	54AS1	305	SN	74AS1	805	UNIT
PARAMETER	TEST CONDI	HUNS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
\/~··	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
Voн	$V_{CC} = 4.5 V$	IOH = -40 mA	2						
	$V_{CC} = 4.5 V$,	$I_{OH} = -48 \text{ mA}$				2			
V	$V_{CC} = 4.5 V,$	IOL = 40 mA		0.25	0.5				~
VOL	$V_{CC} = 4.5 V$	I _{OL} = 48 mA					0.35	0.5	V
lı lı	$V_{CC} = 5.5 V,$	V ₁ = 7 V			0.1			0.1	mA
lih ($V_{CC} = 5.5 V$,	V _i = 2.7 V			20			20	μΑ
lir.	$V_{CC} = 5.5 V$,	V ₁ = 0.4 V			-0.5			-0.5	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 200	- 50		- 200	mA
1ссн	$V_{CC} = 5.5 V,$	V ₁ = 0 V		6.5	10		6.5	10	mA
ICCL	$V_{CC} = 5.5 V,$	$V_1 = 4.5 \text{ V}$		20	32		20	32	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}$ $SN54AS1805 \qquad SN74AS1805$				UNIT	
			SN54	SN54AS1805		AS1805		
			MIN	MAX	MIN	MAX		
tPLH	A or B	or B Y	1	4.8	1	4.3		
^t PHL	A OF B		1	4.8	1	4.3	ns	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS1808A, SN54AS1808, SN74ALS1808A, SN74AS1808 HEX 2-INPUT AND DRIVERS

AUGUST 1984-REVISED MAY 1986

- High Capacitive Drive Capability
- 'ALS1808A Has Typical Delay Time of 4.8 ns (C_L = 50 pF) and Typical Power Dissipation of 4.5 mW per Gate
- 'AS1808 Has Typical Delay Time of 3.2 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 13 mW per Gate
- Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent 2-input AND drivers. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The center pin configuration used in the 'ALS1808A and 'AS1808 provides a reduction of lead inductance when compared to the 'ALS808A and 'AS808B. This reduction of lead inductance will minimize noise generated onto either the V_{CC} or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1808A and SN54AS1808 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS1808A and SN74AS1808 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE (each driver)

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Н
L	X	L
Х	L	L

SN54ALS1808A, SN54AS1808 . . . J PACKAGE SN74ALS1808A, SN74AS1805 . . . N PACKAGE (TOP VIEW)

_			
]1	U 20		5A
2	19		5Y
]3	18		4B
]4	17		4A
]5	16		4Y
]6	15		GND
]7	14		3Y
]8	13		3B
9	12	D	ЗА
10	11		2Y
	3 4 5 6 7 8 9	2 19 3 18 4 17 5 16 6 15 7 14 8 13 9 12	2 19 3 18 4 17 5 16 7 14 3 13 9 12 3

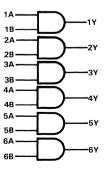
Use 'ALS808A or 'AS808B for chip carrier option.

logic symbol†

1A (6)	& 🗅	(8)
1B		1Y
2A (9)		(11)
2B (10)		2Y
(12)		
3A (13)		(14)_3Y
(17)		
4A (18)		(16) 4Y
4B (20)		
5A (1)		(19) 5Y
28		31
6A (3)		(2)
6B (4)		6Y
		ı

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Operating free-air temperature range:	SN54ALS1808A
	SN74ALS1808A 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	·	SN54ALS1808A		SN7	UNIT			
}		MIN	NOM	MAX	MIN	MOM	MAX	Civil
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ГОН	High-level output current			-12			- 15	mA
lOL	Low-level output current			12			24	mA
TA	Operating free-air temperature.	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDIT	FIONE	SN5	4ALS18	A80	SN7	UNIT		
PANAMETER	TEST CONDIT	TIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _{I.} = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
VoH	$V_{CC} = 4.5 V$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
1 VOH	$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2						ľ
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$				2			
VoL	$V_{CC} = 4.5 V$,	$I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	·
11	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA
ин	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ĪL.	$V_{CC} = 5.5 V,$	$V_1 = 0.4 \text{ V}$			-0.1			-0.1	mA
lo [‡]	$V_{CC} = 5.5 V,$	V _O = 2.25 V	-30		-112	- 30		-112	mA
ГССН	$V_{CC} = 5.5 \text{ V},$	V _I = 4.5 V		4.5	7		4.5	7	mA
¹ CCL	V _{CC} = 5.5 V,	V _I = 0 V		8	16		8	16	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$ 'ALS1808A TYP	C _L R _L T _A	C = 4.5 V = 50 pF, = 500 Ω = MIN to LS1808A MAX	MAX	LS1808A MAX	UNIT
^t PLH	A or B	Y	6	2	11	2	9	ns
^t PHL] // 5/ 5	·	4	1	10	1	8]

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54AS180855°C to 12	25°C
SN74AS1808 0 °C to 7	70°C
Storage temperature range - 65 °C to 15	ã0°C

recommended operating conditions

		SN	SN54AS1808			SN74AS1808		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
ЮН	High-level output current			-40			-48	mA
lOL	Low-level output current			40			48	mA
TA	Operating free-air temperature	- 55		125	0	***************************************	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDI	TIONIC	SN	154AS1	808	SN	74AS1	808	UNIT
PARAMETER	TEST CONDI	TIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	$I_1 = -18 \text{ mA}$			-1.2			-1.2	>
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			
	$V_{CC} = 4.5 V,$	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		v
Vон	$V_{CC} = 4.5 V,$	$I_{OH} = -40 \text{ mA}$	2						·
	$V_{CC} = 4.5 V,$	$I_{OH} = -48 \text{ mA}$				2			
V	$V_{CC} = 4.5 V,$	$I_{OL} = 40 \text{ mA}$		0.25	0.5				v
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5) v
l _l	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
hн	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	$V_1 = 0.4 V$			-0.5			-0.5	mA
lo‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 50		- 200	- 50		- 200	mA
1ссн	$V_{CC} = 5.5 V,$	$V_{j} = 4.5 V$		8	13		8	13	mA
ICCL	$V_{CC} = 5.5 V,$	V ₁ = 0 V		20	33		20	33	mA

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}, T_{A} = 25 \,^{\circ}\text{C}$

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)		UNIT			
			SN54	AS1808	SN74A	S1808	1
			MIN	MAX	MIN	MAX].
^t PLH	A or B	V	1	6.5	1	6	
^t PHL	AOrB	Y	1	6.5	1	6	ns



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS1832A, SN54AS1832, SN74ALS1832A, SN74AS1832 HEX 2-INPUT OR DRIVERS

AUGUST 1984-REVISED MAY 1986

- High Capacitive Drive Capability
- 'ALS1832A Has Typical Delay Time of 5 ns (C_L = 50 pF) and Typical Power Dissipation of 5.3 mW per Gate
- 'AS1832 Has Typical Delay Time of 3.9 ns (C_L = 50 pF) and Typical Power Dissipation of Less than 17 mW per Gate
- Center V_{CC} and GND Configuration Provides Minimum Lead Inductance in High Current Switching Applications
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain six independent 2-input OR drivers. They perform the Boolean functions Y = A + B or $Y = \overline{A \cdot B}$ in positive logic.

The center pin configuration used in the 'ALS1832A and 'AS1832 provides a reduction of lead inductance when compared to the 'ALS832A and 'AS832B. This reduction of lead inductance will minimize noise generated onto either the VCC or GND bus. This reduction is significant in high current switching applications.

The SN54ALS1832A and SN54AS1832 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS1832A and SN74AS1832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each driver)

INP	UTS	OUTPUT
Α	В	Υ
Н	Х	Н
Х	н	Н
L	L	L

SN54ALS1832A, SN54AS1832 . . . J PACKAGE SN74ALS1832A, SN74AS1832 . . . N PACKAGE (TOP VIEW)

5B [<u> 1</u> 7	U 20	Ď 5A	
6Y [2	19	□ 5Y	
6A []3	18	☐ 4B	
6B []4	17] 4A	
/cc[] 5	16] 4Y	
1A [] 6	15	GN	D
1B [7	14] 3Y	
1Y []8	13] 3B	
2A []9	12] 3A	
2B [10	11	2Y	

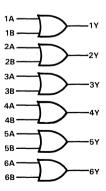
Use 'ALS832A or 'AS832B for chip carrier option.

logic symbol†

1A (6)	≥1 ▷	(8)
1B)	,	1Y
10)		
2A -(3	0)		(11) 2Y
28			
3A _(1	2)		(14)
3B	3)		(14) 3Y
/1	7)		
4A			(16) 4Y
4B(1			7,
5A _(2	0)		(19)
5B(1)		5Y
13	3)		
6A			(2) 6Y
6B(4	'		0,
			,

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 7 V Operating free-air temperature range: SN54ALS1832A -55°C to 125°C SN74ALS1832A 0°C to 70°C Storage temperature range -65°C to 150°C

recommended operating conditions

		SN	SN54ALS1832A			SN74ALS1832A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage			0.7			0.8	٧	
ЮН	High-level output current			- 12			- 15	mA	
¹ OL	Low-level output current		-	12			24	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDI	TION 0	SN5	4ALS18	SN54ALS1832A			SN74ALS1832A			
PARAMETER	TEST CONDIT	IONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT		
VIK	$V_{CC} = 4.5 V$			-1.2			-1.2	٧			
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -0.4 mA	V _{CC} -2			V _{CC} -2					
v _{oh}	$V_{CC} = 4.5 V$,	I _{OH} = -3 mA	2.4	3.2		2.4	3.2] , .		
VOH	$V_{CC} = 4.5 V$,	IOH = -12 mA	2] `		
	$V_{CC} = 4.5 V$	IOH = -15 mA				2			1		
VOL	$V_{CC} = 4.5 V$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V		
VOL	$V_{CC} = 4.5 V$	IOL = 24 mA					0.35	0.5]		
lı .	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA		
lн	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ		
IIL	$V_{CC} = 5.5 V,$	V ₁ = 0.4 V			-0.1			-0.1	mA		
10 [‡]	V _{CC} = 5.5 V,	$V_0 = 2.25 \text{ V}$	- 30		-112	- 30		-112	mA		
^І ссн	$V_{CC} = 5.5 V,$	V _I = 4.5 V		6	9		6	9	mA		
ICCL	V _{CC} = 5.5 V,	V _I = 0 V		9.5	16		9.5	16	· mA		

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C 'ALS1832A	C _L R _L T _A	C = 4.5 V = 50 pF, = 500 Ω = MIN to	MAX	LS1832A	UNIT	
}				TYP	MIN	MAX	MIN	MAX	1
t _{PLH}	A or B	V	6	2	11	2	9	ns	
t _{PHL}	AUID	T	4	1	10	1	8	1115	



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

recommended operating conditions

			SN54AS1832 SN74AS1832			UNIT			
		N	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				-40			-48	mA
lOL	Low-level output current				40			48	mA
TA	Operating free-air temperature	T -	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	54AS1	832	SI	174AS1	832	LIBUT
PARAMETER	TEST CONDI	TIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -2 mA	V _{CC} -2			V _{CC} -2			
	$V_{CC} = 4.5 V$,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		V
Vон	$V_{CC} = 4.5 V$,	$I_{OH} = -40 \text{ mA}$	2						\ \ \
	$V_{CC} = 4.5 V$,	$I_{OH} = -48 \text{ mA}$				2			
\/ -	$V_{CC} = 4.5 V,$	I _{OL} = 40 mA		0.25	0.5				V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 48 mA					0.35	0.5	\ \ \
11	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	$V_1 = 2.7 \text{ V}$			20			20	μΑ
l L	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.5			-0.5	mA
. IO‡	$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 50		- 200	- 50		-200	mA
1ссн	V _{CC} = 5.5 V,	V _I = 4.5 V		11	17		11	17	mA
ICCL	$V_{CC} = 5.5 V,$	V _I = 0 V		22	36		22	36	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)		C _l R _l T,	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω T_A = MIN to MAX					
1			SN54	AS1832	SN74	AS1832			
			MIN	MAX	MIN	MAX			
^t PLH	A or B	V	1	7	1	6.3	no		
[†] PHL	AOIB	Y	1 .	7	1	6.3	ns		



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS2240, SN74ALS2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D2910, JULY 1985-REVISED MAY 1986

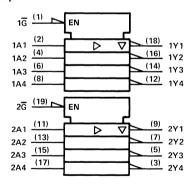
- Bidirectional Quadruple Bus Transceivers for Driving MOS Devices
- I/O Ports have 25 Ohm Series Resistors so No External Resistors are Required
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

The SN54ALS2240 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS2240 is characterized for operation from 0 °C to 70 °C.

logic symbol†

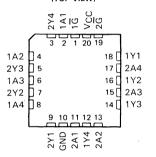


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

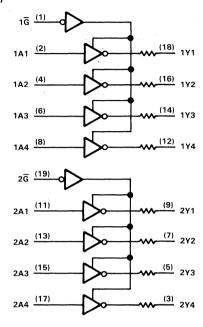
SN54ALS2240 . . . J PACKAGE SN74ALS2240 . . . DW OR N PACKAGE (TOP VIEW)

1G [1A1 [2Y4 [1A2 [2Y3 [1A3 [2Y2 [1 2 3 4 5 6 7	20 V _{CC} 19 2G 18 1Y1 17 2A4 16 1Y2 15 2A3 14 1Y3	
2Y3 [1A3 [վ~	16 1Y2 15 2A3 14 1Y3	
2Y1 [GND [9 10	12 1Y4	

SN54ALS2240 . . . FK PACKAGE
(TOP VIEW)



logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage: All inputs	
I/O ports	5.5 V
Operating free-air temperature range:	SN54ALS224055°C to 125°C
	SN74ALS2240 0 °C to 70 °C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN	54ALS2	240	SN74ALS2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	(111)
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
TA	Operating free-air temperature	- 55		125	0		70	°C

SN54ALS2240, SN74ALS2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3 STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COM	IDITIONS	SN	54ALS2	240	SN	74ALS22	240	UNIT
PANAMETEN	lesi cor	ADITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	V, $IOH = -0.4 mA$	V _{CC} -2			V _{CC} -2			V
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	
lozh	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL	$V_{CC} = 5.5 V$,	V _O = 0.4 V			-20			- 20	μΑ
11	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΊΗ	$V_{CC} = 5.5 V$,	$V_1 = 2.7 \text{ V}$			20			20	μΑ
I _{IL}	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
lo‡	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		112	- 30		-112	mA
ГОН	$V_{CC} = 4.5 \text{ V},$	$V_0 = 2 V$	- 15			- 15			mA
lOL	$V_{CC} = 4.5 \text{ V},$	V _O = 2 V	15			15			mA
		Outputs high		6	11		6	11	
^I CC	V _{CC} = 5.5 V	Outputs low		13	23		13	23	mA
		Outputs disabled		12	20		12	20	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \, ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$ 'ALS2240	C _L R1 R2 T _A SN54A			NLS2240	UNIT
			TYP	MIN	MAX	MIN	MAX	
^t PLH	Α	Y	6	2	14	2	10	ns
t _{PHL}			6	2	14	2	10	115
t _{PZH}	G	V	10	5	20	5	17	ns
tPZL	G	Y	12	7	25	7	20	115
t _{PHZ}	G	V	7	2	12	2	10	
tPLZ]	4	9	4	20	.4	15	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

^{*} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS2242, SN74ALS2242 QUADRUPLE BUS TRANSCEIVERS/MOS DRIVER

MAY 1985-REVISED MAY 1986

- Bidirectional Quadruple Bus Transceivers For Driving MOS Devices
- I/O Ports Have 25 Ohm Series Resistors so No External Resistors are Required
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These quadruple bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

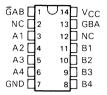
These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and $\overline{G}AB$).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

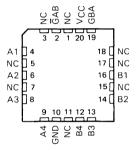
The dual-enable configuration gives the 'ALS2242 the capability to store data by simultaneous enabling of GBA and $\overline{G}AB$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary.

The SN54ALS2242 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS2242 is characterized for operation from 0 °C to 70 °C.

SN54ALS2242 . . . J PACKAGE SN74ALS2242 . . . D OR N PACKAGE (TOP VIEW)



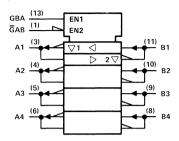
SN54ALS2242 . . . FK PACKAGE



NC-No internal connection

SN54ALS2242, SN74ALS2242 QUADRUPLE BUS TRANSCEIVERS/MOS DRIVER

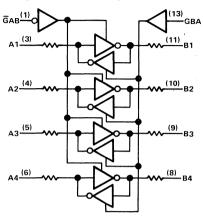
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage: All inputs
I/O ports
Operating free-air temperature range: SN54ALS224255°C to 125°C
SN74ALS2242
Storage temperature range65°C to 150°C

recommended operating conditions

		SN	SN54ALS2242 SN74ALS2242				UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	CIVIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			8.0	V
TA	Operating free-air temperature	- 55		125	0		70	°C

SN54ALS2242, SN74ALS2242 QUADRUPLE BUS TRANSCEIVERS/MOS DRIVER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER			SN	54ALS2	242	SN	74ALS2	242	UNIT
	PARAMETER	TEST COM	NDITIONS	MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			- 1.2			- 1.2	V
Vон		$V_{CC} = 4.5 \text{ V to 5.9}$	5 V, I _{OH} = -0.4 mA	Vcc	2		vcc-	2		V
Val		$V_{CC} = 4.5 V$,	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	v
	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
1 1	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	IIIA
	Control inputs	V F.F.V	V _I = 2.7 V			20			20	_
11H	A or B ports‡	$V_{CC} = 5.5 V$,	V) - 2.7 V			20			20	μΑ
111	Control inputs	V 55 V				- 0.1			- 0.1	
11	A or B ports‡	$V_{CC} = 5.5 V,$	V _I = 0.4 V			- 0.1			- 0.1	mA
Io§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		- 112	mA
ІОН		V _{CC} = 4.5 V,	V _O = 2 V	- 15			- 15			mA
IOL		$V_{CC} = 4.5 V$,	V _O = 2 V	30			30			mΑ
			Outputs high		10	20		10	16	
Icc		$V_{CC} = 5.5 V$	Outputs low		14	26		14	21	mΑ
			Outputs disabled		13	24		13	19	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} V_{CC} = 5 \text{ V}, \\ C_L = 50 \text{ pF}, \\ R_1 = 500 \Omega, \\ R_2 = 500 \Omega, \\ T_A = 25 ^{\circ}\text{C} \\ \text{'ALS2242} \end{array}$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$			UNIT	
			TYP	MIN	MAX	MIN	MAX	
.tPLH	A or B	B or A	5	2	15	2	11	ns
tpHL .	/\ 0. b	3 3777	5	2	14	2	10	
^t PZH	- GAB	В	8	3	18	3	16	ns
tPZL	_ GAB	J	11 .	5	22	5	20	1
^t PHZ	- GAB	В	6	2	12	2	10	ns
tPLZ		D .	6	2	18	2	12	115
^t PZH	GBA	Α	10	3	18	3	16	ns
^t PZL	7 354	A	12	5	22	5	20	1 15
^t PHZ	GBA	Α	6	2	12	2	10	ns
^t PLZ	7 384	, , , , , , , , , , , , , , , , , , ,	6	2	18	2	14	115

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.



[‡]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, log.

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

JUNE 1984-REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Outputs have 25 Ω Series Resistor, No External Resistors are Required
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

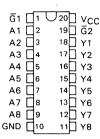
These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS240A/SN74ALS240A series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

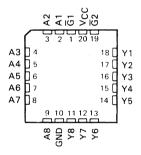
The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

The SN54ALS' is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS' is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

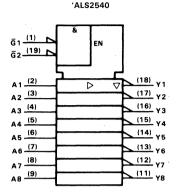
SN54ALS2540, SN54ALS2541 . . . J PACKAGE SN74ALS2540, SN74ALS2541 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS2540, SN54ALS2541 . . . FK PACKAGE (TOP VIEW)



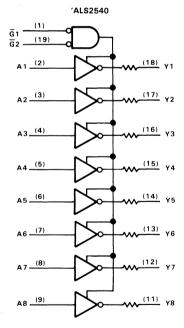
logic symbols[†]

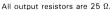


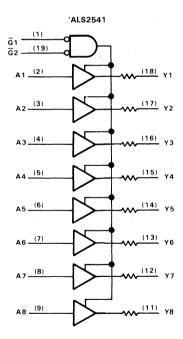
	'ALS2541	
G1 (1) CG2 (19) C	& EN	
A 1 (2)	$\triangleright \ $	(18) Y1
A2 (3)		(17) Y2
A3 (4)		(16) Y3
A4 (5)		(15) Y4
A5 (6)		(14) Y5
A6 (7)		(13) Y6
(8)		(12)
A7 (9)		(11) (11) Y8
ı	<i></i>	

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)









SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating	g free-air temperature range (unless otherwise noted)
Supply voltage, VCC	
Input voltage	
Voltage applied to a disabled 3-state o	utput
Operating free-air temperature range: \$	SN54ALS2540, SN54ALS2541 55 °C to 125 °C
•	SN74ALS2540, SN74ALS2541 0 °C to 70 °C
Storage temperature range	−65°C to 150°C

recommended operating conditions

		SI	SN54ALS2540 SN54ALS2541			SN74ALS2540 SN74ALS2541			
		SI							
		MIN	NOM	MAX	MIN	NOM	MAX	İ	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			-0.4			-0.4	mA	
lOL	Low-level output current			12			12	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			N54ALS		SN74ALS2540 SN74ALS2541				
'	PARAINETER	TEST	TEST CONDITIONS		TYP†	MAX	MIN	TYP [†]	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			- 1.2	V	
Voн		$V_{CC} = 4.5 \text{ V to 5}.$	5 V, I _{OH} ≈ -0.4 mA	Vcc-	2		Vcc-	2		V	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	V	
VOL		$V_{CC} = 4.5 \text{ V},$			0.35	0.8		0.35	0.8	1 °	
lozh		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$			20			20	μΑ	
IOZL		$V_{CC} = 5.5 V$,	V _O = 0.4 V			- 20			- 20	μΑ	
ЮН		$V_{CC} = 4.5 \text{ V},$	V _O = 2 V	- 15			- 15			mA	
lOL		$V_{CC} = 4.5 \text{ V},$	$V_0 = 2 V$	30			30			mA	
11		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA	
ΉΗ		$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ	
IL		$V_{CC} = 5.5 \text{ V},$	V _I = 0.4 V			-0.1			- 0.1	mA	
10‡		$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.25 \text{ V}$	- 15		- 70	- 15		- 70	mA	
		1	Outputs high		5	10		5	10		
	'ALS2540	$V_{CC} = 5.5 V$	Outputs low		13	22		13	22	mA	
laa			Outputs disabled		11	19		11	19	1	
'cc		Outputs high		6	14		6	14			
	'ALS2541	'ALS2541 V _{CC} = 5.5 V	Outputs low		15	25		15	25	mA	
			Outputs disabled		13.5	22		13.5	22	1	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS2540, SN54ALS2541, SN74ALS2540, SN74ALS2541 OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	(INPUT) (OUTPUT) $R2 = 50$ $T_A = 29$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{min to } \text{MAX}$				UNIT
	i		'ALS2540	SN54ALS2540		SN74ALS2540		1 1
			TYP	MIN	MAX	MIN	MAX	
tPLH	A	V	7.5	2	· 14	2	12	ns
tPHL	1 ^	. '	5.6	2 .	13	2	11	115
^t PZH	G	V	9	5	18	5	15	ns
tPZL]	'	12.6	8	24	8	20	115
tPHZ	G		4	1	12	1	10	ns
^t PLZ		,	7	2	14	2	12	115

'ALS2541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_{L} = 50 pF$, R1 = 500 Ω, R2 = 500 Ω, $T_{A} = 25 °C$	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to			UNIT			
			'ALS2541	SN54A	LS2541	SN74ALS2541]			
			TYP	MIN	MAX	MIN	MAX				
^t PLH	A	Y	8.7	2	17	2	15				
t _{PHL}	7 ^		r	ĭ	ľ	ĭ	7	2	14	2	12
* tPZH	G	Υ	9	5	18	5	15				
tPZL	7 "	Y	12.6	8	24	8	20	ns			
tPHZ	- G	Y	4	1	12	1	10				
^t PLZ	7 '	,	7	2	14	2	12	ns			

SN54AS2620, SN54AS2623, SN74AS2620, SN74AS2623 OCTAL BUS TRANSCEIVERS/MOS DRIVER

Bidirectional Octal Bus Transceivers For

Driving MOS Devices

 I/O Ports Have 25 Ohm Series Resistors So No External Resistors Are Required

- Local Bus-Latch Capability
- Choice of True or Inverting Logic
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs $(\overline{G}BA)$ and $(\overline{G}AB)$.

The enable inputs can be used to disable the device so that the buses are effectively isolated.

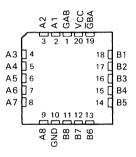
The dual-enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

The SN54AS2620 and SN54AS2623 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS2620 and SN74AS2623 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

SN54AS' . . . J PACKAGE SN74AS' . . . DW OR N PACKAGE (TOP VIEW)

GAB A1 A2 A3 A4 A5 A6 A7	<u>החחחחחח</u>	1 2 3 4 5 6 7 8 9	U	20 19 18 17 16 15 14 13	VCC GBA B1 B2 B3 B4 B5 B6 B7
A8 GND		9 10		12 11	B7 B8

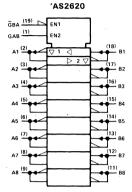
SN54AS' . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE

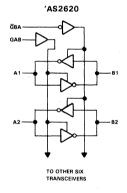
ENABLE	INPUTS	OPER#	TION	
GBA	GAB	'AS2620	'AS2623	
L	, L	B data to A bus	B data to A bus	
Н	Н	Ā data to B bus	A data to B bus	
Н	L	Isolation	Isolation	
		B data to A bus,	B data to A bus,	
L	н	Ā data to B bus	A data to B bus	

logic symbols†

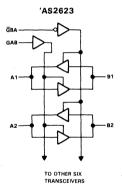


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



AS 2623 GBA (19) EN1 GAB (11) EN2 A1 (2) V1 (3) ES (18) B A2 (3) (16) B A3 (4) (16) B A4 (5) (14) B A5 (6) (14) B A6 (7) (13) B A7 (8) (11) B A8 (9) (11) B



SN54AS2620, SN54AS2623, SN74AS2620, SN74AS2623 OCTAL BUS TRANSCEIVERS/MOS DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

recommended operating conditions

Storage temperature range

			SN54AS2620 SN54AS2623		SN74AS2620 SN74AS2623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Р	PARAMETER TE		r conditions		54AS2(54AS2(SN74AS2620 SN74AS2623			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V	
Vон		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -2 mA	V _{CC} -2			V _{CC} -2			٧	
V		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 1 mA		0.15	0.4		0.15	0.4	v	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.35	0.7		0.35	0.7	l v	
1.	Control inputs	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA	
lį	A or B ports	$V_{CC} = 5.5 V,$	$V_1 = 5.5 V$			0.1			0.1	mA	
L.	Control inputs	V 5 5 V	\/ 2.7\/			20			20		
ΉΗ	A or B ports‡	$V_{CC} = 5.5 V,$	$V_{\dagger} = 2.7 \text{ V}$			70			70	μΑ	
L	Control inputs	V E E V	$V_1 = 0.4 \text{ V}$			-0.5			-0.5	mA	
IIL	A or B ports‡	$V_{CC} = 5.5 \text{ V},$	V = 0.4 V			-0.75			-0.75	mA	
lo§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 50		- 150	- 50		- 150	mA	
ЮН		$V_{CC} = 4.5 V,$	$V_0 = 2 V$	-35			-35			mA	
loL		$V_{CC} = 4.5 V,$	$V_0 = 2 V$	35			35			mA	
			Outputs high		62	100		62	100		
	'AS2620	$V_{CC} = 5.5 V$	Outputs low		74	121		74	121		
lcc	C /AS2623 V _{CC} = 5.5 V	Outputs disabled		48	77		48	77	mA		
icc				Outputs high		57	93		57	93] "IIA
			Outputs low		116	189		116	189		
			Outputs disabled		72	116		72	116	1	

f All typical values are at $V_{CC}=5$ V, $T_A=25$ °C ‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ins.

'AS2620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54	$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_A = \text{MIN to MAX} \\ \hline \text{SN54AS2620} & \text{SN74AS2620} \\ \hline \text{MIN} & \text{MAX} & \text{MIN} & \text{MAX} \end{array}$			
				MAX	MIN	MAX	
tPLH	А	В	1	9.5	1	8	ns
^t PHL		, В	1	7.5	1	6.5	115
^t PLH	В	А	1	9.5	1	8	ns
tPHL	,		1	7.5	1	6.5	115
^t PZH	Ğва	А	1	11	1	10	ns
tPZL	GDA	A	1	12	1	11	115
^t PHZ	Ğва	А	1	7.5	1	6	ns
tPLZ	GBA	<u>^</u>	1	15	1	12	115
tPZH	GAB	В	1	9	1	8	
tPZL	GAB	ь	1	9	1	8	ns
^t PHZ	GAB	В	1	12	1	11	
tPLZ	GAB	В	1	12	1	11	ns

'AS2623 switching characteristics (see Note 1)

PARAMETER	FROM TO (OUTPUT)		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$					
			SN54	AS2623	SN74A	S2623		
		N		MAX	MIN	MAX		
^t PLH	Α	В	1	9.5	1	8.5	ns	
^t PHL	^ .	D	1	8.5	1	7.5	115	
^t PLH	В	А	1	10	1	9		
^t PHL	ь	1 ^	1	9	1	7.5	ns	
t _{PZH}	GBA .	А	1	12.5	1	11		
tPZL	GBA	^	1	12	-1	11	ns	
t _{PHZ}	G BA	А	1	8.5	1	7.5		
tPLZ	GBA	^	1	13	1	12	ns	
^t PZH	GAB	В	1	13	1	12		
^t PZL	GAB	В	1	13.5	1	12	ns	
^t PHZ	CAR	5	1	7.5	1	7		
tPLZ	GAB	В	1	14.5	1	12.5	ns	

SN54AS2640, SN54AS2645 SN74AS2640, SN74AS2645 OCTAL BUS TRANSCEIVER/MOS DRIVER

DECEMBER 1983-REVISED MAY 1986

- Bidirectional Octal Bus Transceivers For Driving MOS Devices
- I/O Ports Have 25 Ohm Series Resistors So
 No External Resistors Are Required
- Choice of True or Inverting Logic
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

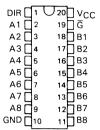
description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

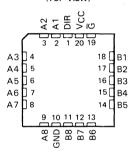
The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so the buses are effectively isolated.

The SN54AS' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74AS' family is characterized for operation from 0 °C to 70 °C.

SN54AS' . . . J PACKAGE SN74AS' . . . DW or N PACKAGE (TOP VIEW)



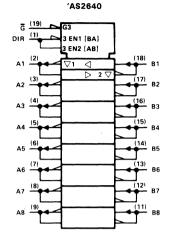
SN54AS' . . . FK PACKAGE (TOP VIEW)

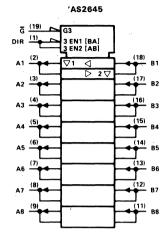


FUNCTION TABLE

CONTROL		OPERATION				
INPUTS		'AS2640	'AS2645			
G	DIR	A52640	A32045			
L	L	B data to A bus	B data to A bus			
L	Н	Ā data to B bus	A data to B bus			
нх		Isolation	Isolation			

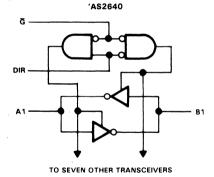
logic symbols†

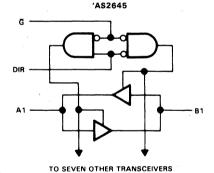




 $^\dagger \text{These symbols}$ are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagrams (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
nput voltage: All inputs
I/O ports
Derating free-air temperature range: SN54AS2640, SN54AS264555°C to 125°C
SN74AS2640, SN74AS2645 0°C to 70°C
Storage temperature range 65 °C to 150 °C

recommended operating conditions

	·		SN54AS2640			SN74AS2640		
		Si	SN54AS2645		SN74AS2645			
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-Ivel input voltage			0.8			0.8	V
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	ADAMETED	TEST COMP	ITIONS		SN54A	S'		SN74AS	3 ′	
Ρ,	ARAMETER	TEST COND	THUNS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$			- 1.2			- 1.2	V
∨он		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	Vcc-	2		V _{CC} -	- 2		V
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 1 mA		0.15	0.4		0.15	0.4	V
VOL		$V_{CC} = 4.5 V,$	$I_{OL} = 12 \text{ mA}$		0.35	0.7		0.35	0.7	V
4	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
''	A or B ports	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	IIIA
чн	Control inputs	V _{CC} = 5.5 V,	$V_1 = 2.7 \text{ V}$			20			20	μΑ
I 'IH	A or B ports [‡]	\(\(\text{CC} = 3.3 \text{V}\)	V - 2.7 V			70			70	μ^
l _{IL}	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
'1L	A or B ports [‡]	3.5 4,	V) = 0.4 V			-0.75			-0.75	""
IO§		$V_{CC} = 5.5 V,$	$V_0 = 2.25 V$	- 50		- 150	- 50		- 150	mA
IOH		$V_{CC} = 4.5 V$,	V _O = 2 V	- 35			- 35			mA
lor		$V_{CC} = 4.5 \text{ V},$	$V_{OL} = 2 V$	35			35			mA
			Outputs high		37	58		37	- 58	
	'AS2640		Outputs low		78	123		78	123	
loo		VCC = 5.5 V	Outputs disabled		51	80		51	80	mA
lcc		VCC - 3.3 V	Outputs high		58	95		58	95	
	'AS2645		Outputs low		95	155		95	155	
			Outputs disabled		73	119		73	119	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

 $^{^{\}ddagger}\text{For I/O}$ ports, the parametes I_{IH} and I_{JL} include the off-state output current.

[§]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

'AS2640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_A = \text{MIN to MAX} \\ \hline SN54AS2640 & SN74AS2640 \end{array}$		1	UNIT	
			SN54/			SN54AS2640 SN74AS2640		
			MIN	MAX	MIN	MAX		
^t PLH	A or B	D A	1	9.5	1	7.5		
tPHL *	Aorb	B or A	1	7	1	6.5	ns	
^t PZH	G	A or B	. 2	11	2	9		
^t PZL	G	A or B	2	12	2	10	ns	
^t PHZ	G	A D	1	8	1	7		
[†] PLZ	G A or B		2	15	2	13	ns	

'AS2645 switching characteristics (see Note 1)

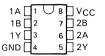
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$			V,	UNIT	
			SN54AS2645		SN74AS2645]	
			MIN	MAX	MIN	MAX		
tPLH			1	12	1 .	10		
tPHL	A or B	B or A	1	11	1	9.5	ns	
tPZH	-	1	1	13	1	11.5	d ne	
^t PZL	G	A or B	1	13	1	10.5		
^t PHZ			1	9	1	8		
tPLZ	G	A or B	1	13	1	12	ns	

SN54ALS8003, SN74ALS8003 DUAL 2-INPUT POSITIVE-NAND GATES

D2746, JULY 1983-REVISED MAY 1986

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability.

SN54ALS8003 . . . JG PACKAGE SN74ALS8003 . . . D OR P PACKAGE (TOP VIEW)



description

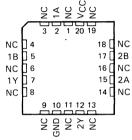
These devices contain two independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS8003 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN74ALS8003 is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (each gate)

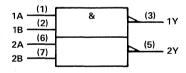
Γ	INP	UTS	OUTPUT
Γ	Α	В	Υ
Γ	Н	Н	L
	L	X	Н
	Х	L	Н

SN54ALS8003 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

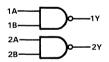
logic symbol[†]



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, JG and P packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS8003	– 55°C to 125°C
SN74ALS8003	0°C to 70°C
Storage temperature	65°C to 150°C

recommended operating conditions

			SN	54ALS8	003	SN74ALS8003			UNIT
		Γ	MIN	NOM	MAX	MIN	NOM	MAX	ONLI
Vcc	Supply voltage		4,5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
Iон	High-level output current				-0.4			-0.4	mA
^I OL	Low-level output current				4			8	mA
TA	Operating free-air temperature		- 55		125	0		,70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	154ALS	3003	SN	174ALS	3003	UNIT	
PARAMETER			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNII	
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			- 1.5			- 1.5	V	
Voн	$V_{CC} = 4.5 \text{ V to } 5.5$	$V_{1} = -0.4 \text{ mA}$	V _{CC} -2	2		V _{CC} -2			V	
Vai	V _{CC} = 4.5 V,	IOL = 4 mA		0.25			0.25	0.4	0.4 V	
VOL	V _{CC} = 4.5 V,	I _{OL} = 8 mA					0.35	0.5	1 ' I	
l _l	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mΑ	
lн	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μΑ	
ΊL	V _{CC} = 5.5 V,	V _I = 0.4 V	i		-0.1			-0.1	mA	
1 ₀ ‡	$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	15		- 70	-15		- 70	mA	
Іссн	$V_{CC} = 5.5 \text{ V},$	V ₁ = 0 V		0.22	0.43		0.22	0.43	mΑ	
^I CCL	$V_{CC} = 5.5 V,$	V _I = 4.5 V		0.81	1.5		0.81	1.5	mA	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	SN544	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX SN54ALS8003 SN74ALS8003			UNIT
			MIN	MAX	MIN	MAX	
tPLH	A or B	V	. 3	14	3	11	ns
tPHL	1 4016	1	2	10	. 2	8	1115

[‡]The output conditions have been chosen to produce a current that closely approximats one half of the true short-circuit output current, IOS.

SN54ALS29806, SN54ALS29809 SN74ALS29806, SN74ALS29809 COMPARATOR AND 2- TO 4-BIT DECODER

D2934, MARCH 1986

- 'ALS29806 is a 6-Bit Identity Comparator Controlling a 2- to 4-Bit Decoder
- 'ALS29809 is a 9-Bit Identity Comparator
- Low Power Dissipation . . . 50 mW Typical
- 'ALS29806 and 'ALS29809 are Functionally Equivalent to AM29806 and AM29809
- Internal Pull-Up Resistor on Q Inputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

The 'ALS29806 and 'ALS29809 are 6-bit and 9-bit comparators, respectively. The 'ALS29806 and 'ALS29809 compare two data words applied to the P and Q inputs. When the two words are identical, the $\overline{P}=\overline{Q}$ output goes low. Both devices feature an open-collector acknowledge (\overline{ACK}) output that goes low when $\overline{P}=\overline{Q}$ and the controlling input (\overline{C}) are low. The 'ALS29806 features a 2- to 4-bit decoder whose selected output goes low when the $\overline{P}=\overline{Q}$ output is low. The 'ALS29806 and 'ALS29809 can be cascaded by tying the $\overline{P}=\overline{Q}$ output to the enable \overline{G} of the next device. If the \overline{G} input is high, all the outputs will be inactive (high).

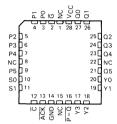
The SN54ALS29806 and SN54ALS29809 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS29806 and SN74ALS29809 are characterized for operation from 0°C to 70°C.

SN54ALS29806 . . . JT PACKAGE SN74ALS29806 . . . DW OR NT PACKAGE (TOP VIEW)

GГ U24 VCC P0 72 23 1 00 P1 3 22 Q1 P2[21 02 20 1 0 3 P4 16 19 104 18 05 P5 so De 17 TYO S1[16 Y1 Ē ☐10 15 Y2 ACK 14 TY3 GND

SN54ALS29806 . . . FK PACKAGE SN74ALS29806 . . . FN PACKAGE

(TOP VIEW)

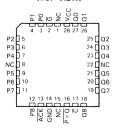


SN54ALS29809 . . . JT PACKAGE SN74ALS29809 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54ALS29809 . . . FK PACKAGE SN74ALS29809 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection



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FUNCTION TABLE FOR $\overline{P} = \overline{Q}$ AND \overline{ACK} OUTPUTS

	INPUTS	OUTPUTS				
G	P,Q	c	$\overline{P} = \overline{Q}$	ACK		
Н	X	Х	H	Н		
Х	P≠Q	Х	н	н		
L	P = Q	L	L	L		
L	P = Q	н	L	н		

FUNCTION TABLE FOR DECODER OUTPUTS

	INPUTS				OUTPUTS			
	G	P,Q	S1	S0	Y3	Y2	Y1	YO
Г	Н	X	Х	Х	Н	Н	Н	Н
	X	$P \neq Q$	×	X	н	н	Н	н
	L	P = Q	L	L	н	н	Н	L
l	L	P = Q	L	н	, н	Н	L	н
1	L	P = Q	Н	L	Н	·L	Н	Н
	L	P = Q	Н	Н	L	·H	Н	н

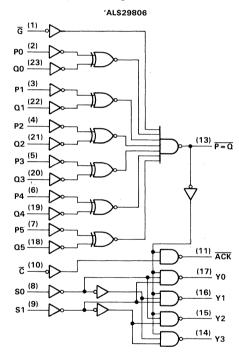
logic symbol†

'ALS29806 COMP G (2) PΩ (3) (4) P2 (5) РЗ (6) (7) (13) $\overline{P} = \overline{Q}$ (23)QΟ (22)(21) (11) ACK (20) 4(P = Q) **△** (19)Q4 (1<u>7)</u> YO (18) Q5 O(P = Q) $\overline{c} \frac{\overline{(10)}}{}$ (<u>16)</u> Y1 1(P = Q)so (8) (15) Y2 2(P = Q) (<u>14)</u> y3 (9) 3(P = Q)

 $^{\dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT and NT packages.

logic diagram (positive logic)





FUNCTION TABLE

	INPUTS	OUTPUTS		
G	P,Q	c	P = Q	ACK
Н	X	Х	Н	Н
X	P≠Q	X	н	Н
L	P = Q	L	L	L
L	P = Q	н	L	Н

logic symbol†

Q6 (17)

Q7 (16)

 $\frac{08}{\overline{C}}\frac{\overline{(15)}}{(14)}$

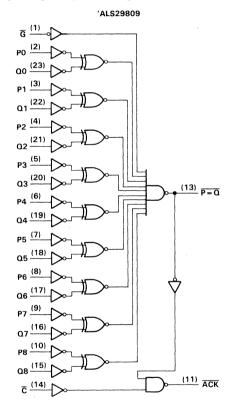
<u>G</u> (1) COMP PO (2) P1 (3) P2 (4) P3 (5) P4 (6) (7) P5 (8) (9) (13) $\overline{P=0}$ P8 (10) (23) Q1 (22) (1) ACK 1(P = Q) **△** 02 (21) Q3 (20) Q4 (19) Q5 (18)

'ALS29809

 $^{\dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT and NT packages.

logic diagram (positive logic)





recommended operating conditions

					SN54ALS29806 SN54ALS29809			SN74ALS29806 SN74ALS29809		
				MIN	NOM	·MAX	MIN	NOM	MAX	1
Vcc	Supply voltage	-		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage						2			V
VIL	Low-level input voltage					0.7			0.8	V
Vон	High-level output voltage	ACK				5.5			5.5	V
loн	High-level output current	$\overline{P} = \overline{Q}$, Y				-3			-3	mA
1	Low-level output current	ACK .				32			32	mA
IOL Low-level output current		$\overline{P} = \overline{Q}$, Y				12			24] ""^
TA	Operating free-air temperature			- 55		. 125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			4ALS29		SN7	UNIT			
				MIN	TYP	MAX	MIN	TYP [†]	MAX	1	
VIK		$V_{CC} = 4.5 \text{ V},$	l _j = -18 mA			-1.2			-1.2	V	
1/		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} - 2.	2		V _{CC} -2			V	
VOH		V _{CC} = 4.5 V,	$I_{OH} = -3 \text{ mA}$	2.4	3.2		2.4	3.2		ľ	
ЮН	ACK	V _{CC} = 5.5 V,	V _{OH} = 5.5 V			0.1			0.1	mA	
	/OL P=0, Y	V _{CC} = 4.5 V,	IOL = 12 mA		0.25	0.4		0.25	0.4		
v_{OL}		$V_{CC} = 4.5 \text{ V},$	IOL = 24 mA					0.32	0.5	7 v	
	ACK	$V_{CC} = 4.5 V,$	I _{OL} = 32 mA		0.34	0.5		0.34	0.5	1	
11		V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	mA	
	Q‡	., 55.				- 250			- 250		
lН	All other	$V_{CC} = 5.5 V$,	$V_I = 2.4 V$			20			20	μA	
	Q‡	==				- 2			- 1	Ι.	
ΊL	All other	$V_{CC} = 5.5 V$,	$V_I = 0.5 V$			-0.6			-0.6	mA	
los§		$V_{CC} = 5.5 V,$	V _O = 0 V	- 60		- 150	-60		- 150	mA	
1	'ALS29806	V	C N 1		14	22		14	22		
lcc	$V_{CC} = 5.5 \text{ V},$		See Note 1		10	20		10	20	mA mA	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

NOTE 1: ICC is measured with \overline{G} grounded and P and Q at 4.5 V.



 $^{^{\}ddagger}$ All Q inputs have internal pull-up resistors of 27 k Ω nominal.

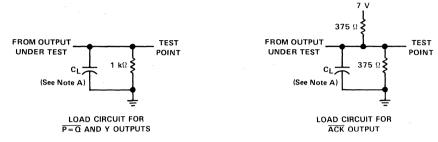
[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54ALS29806, SN54ALS29809 SN74ALS29806, SN74ALS29809 COMPARATOR AND 2- TO 4-BIT DECODER

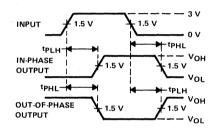
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = (see Figure 1), T _A = 25 °C 'ALS29806 'ALS29809			T _A = MIN to MAX SN54ALS29806 SN74 SN54ALS29809 SN74			LS29806 LS29809	UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
^t PLH	P or Q	$\overline{P} = \overline{Q}$		8	11	3	15	3	13	ns	
tPHL				7	10	2	13	2	11		
^t PLH	PorQ	Y		9	11	3	17	3	13	ns	
tPHL				9	12	5	17	5	14	,,,,	
tPLH	Ğ	$\overline{P} = \overline{\Omega}$		9	12	3	15	3 .	14	ns	
tPHL		1-0		7	10	2	14	2	12	1115	
t _{PLH}	G	Υ		8	11	3	17	3	15		
tPHL	9	'		10	13	5	19	5	16	ns	
tPLH	S0 or S1	Υ		6	10	2	15	2	13		
tPHL	30 01 31	,		8	11	2	15	2	13	ns	
tPLH	P or Q	ACK		11	14	5	22	5	17		
tPHL	roru	ACK		10	13	4	18	4	16	ns	
tPLH	G	ACK		10	14	5	22	5	17		
tPHL	G	ACK		10	14	4	19	4	17	ns	
tPLH	<u>c</u>	ĀCK		8	11	. 3	21	3	18		
tPHL	C	ACK		7	11	3	17	3	15	ns	

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 1

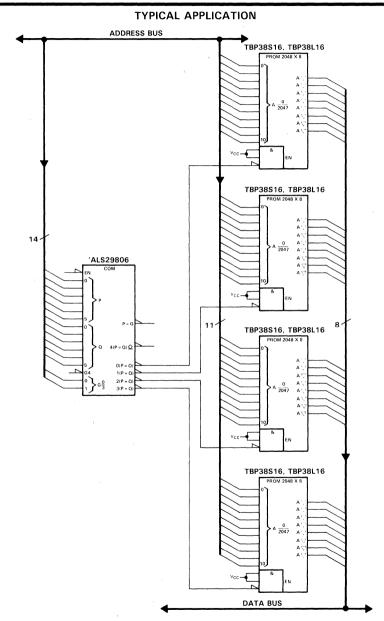


FIGURE 2. MEMORY BANK DECODER



D2825, JANUARY 1986

- Functionally Equivalent to AMD's AM29821 and AM29822
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flipflops. On the positive transition of the clock the Q outputs on the 'ALS29821 will be true, and on the 'ALS29822 will be complementary to the data input.

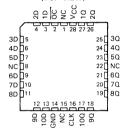
A buffered output-control (\overline{OC})input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54'family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54ALS29821 . . . JT PACKAGE SN74ALS29821 . . . DW OR NT PACKAGE

(1	UP	VIE	N)	•
OC [1	U 24	þ	Vcc
1D[2	23		10
2D [3	22		2Q
3D [4	21		30
4D [5	20		4Q
5D [6	19		5Q
6D [7	18		6Q
7D [[8	17		7Q
8D [9	16		90
9D [10	15		90
10D [11	14		100
GNDE	112	12	\Box	CIK

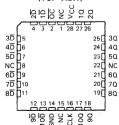
SN54ALS29821 ... FK PACKAGE SN74ALS29821 ... FN PACKAGE (TOP VIEW)



SN54ALS29822 . . . JT PACKAGE SN74ALS29822 . . . DW OR NT PACKAGE (TOP VIEW)

SN54ALS29822 . . . FK PACKAGE SN74ALS29822 . . . FN PACKAGE

(TOP VIEW)



NC-No internal connection

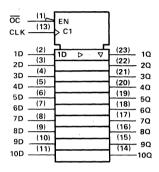
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'ALS29821 FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
<u>oc</u>	CLK	D	a
L	1	Н	Н
L	Ť	L	L
L	L	X	Ω0
Н	×	×	z

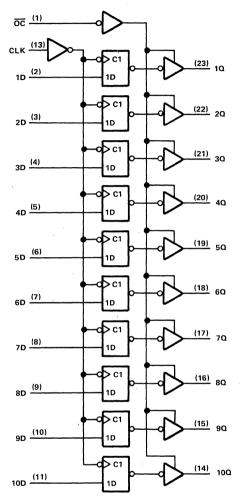
'ALS29821 logic symbol[†]



 $^{\dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS29821 logic diagram (positive logic)



SN54ALS29822, SN74ALS29822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS29822 FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
<u>oc</u>	CLK	Q	
L	1	Н	L
L	1	L	Н
L	L	X	a_0
н	X	X	Z

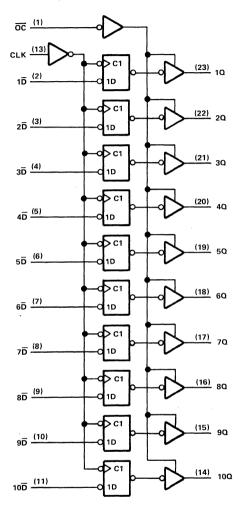
'ALS29822 logic symbol†

0C CLI 1D 2D 3D 4D 5D 6D 7D 8D	(2) (3) (4) (5) (6) (7) (8) (9)	EN > C1	(23) 10 (22) 20 (21) 30 (20) 40 (19) 50 (18) 60 (17) 70 (15) 80
	(9) (10) (11)		J (16)

 $^{^{\}dagger}\textsc{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'ALS29822 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC 7 V
Input voltage
Voltage applied to a disabled 3-state output
Input current
Output current
Operating free-air temperature range: SN54ALS29821, SN54ALS2982255°C to 125°C
SN74ALS29821, SN74ALS29822 0°C to 70°C
Storage temperature range65 °C to 150 °C

recommended operating conditions

			SN54ALS29821 SN54ALS29822			SN74ALS29821		
		SN				SN74ALS29822		
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7		***************************************	0.8	V
ЮН	High-level output current			- 15			- 24	mA
lOL	Low-level output currrent			32			48	mA
t _W	Pulse duration, CLK high or low							ns
t _{su}	Setup time, data before CLK↑							ns
th	Hold time, data after CLK↑							ns
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST COND	ITIONS†		54ALS2 54ALS2		SN74ALS29821 SN74ALS29822			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
VIK		$V_{CC} = MIN,$	I _I = -18 mA			-1.2			-1.2	V
		$V_{CC} = MIN \text{ to MAX},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2		Vcc-	2			
Vон		V _{CC} = MIN,	$I_{OH} = -15 \text{ mA}$	2.4	3.3] v
		V _{CC} = MIN,	$I_{OH} = -24 \text{ mA}$				2.4	3.2		
VOL		V _{CC} = MIN,	$I_{OL} = 32 \text{ mA}$		0.25	0.4		0.25	0.4	V
		V _{CC} = MIN,	$I_{OL} = 48 \text{ mA}$					0.35	0.5	l
lozh		$V_{CC} = MAX$,	$V_0 = 2.4 \text{ V}$			20			20	μΑ
lozL		$V_{CC} = MAX$,	$V_0 = 0.4 V$			- 20	-		- 20	μA
=	*	$V_{CC} = MAX$,	$V_{ } = 5.5 V$			0.1			0.1	mA
۱н		$V_{CC} = MAX$,	$V_I = 2.7 V$			20			20	μΑ
IIL.		V _{CC} = MAX,	V _I = 0.4 V			-0.1			-0.1	mA
los§		V _{CC} = MAX,	V _O = 0 V	- 75		- 250	- 75		- 250	mA
			Outputs high					-		
	'AL\$29821		Outputs low							
¹cc		V _{CC} = MAX	Outputs disabled		48			48		1 _,
100		ACC - MAX	Outputs high							mA
	'ALS29822		Outputs low							
			Outputs disabled		48			48		1

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

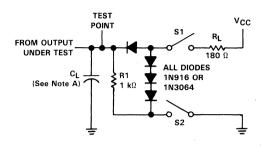
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	V _{CC} = 5 V, T _A = 25 °C 'ALS29821 'ALS29822 MIN TYP MAX		SN54A SN54A	V _{CC} = MIN T T _A = MIN TC SN54ALS29821 SN54ALS29822 MIN MAX								
tPLH			C _L = 300 pF												
tPHL	CLK	Any Q	C[= 300 pr								ns				
^t PLH	CLK	Any u	Any Q	Any Q	Ally Q	A., Q	C _I = 50 pF		6] ""5
^t PHL			С = 50 рі		7										
^t PZH	İ		$C_{I} = 300 pF$]				
tPZL	оc	Any Q	Any O	Any O	GE - 000 bi	о _С осо р.	l							ns	
^t PZH		/, 🖫	C _L = 50 pF		12] ""				
tPZL			GE = 90 bi		11										
^t PHZ			$C_1 = 50 pF$												
tPLZ	oc	Any Q	ο _L = 30 μι								ns				
^t PHZ		Ally C	C ₁ = 5 pF		5] '''				
tPLZ			OL		6	•									

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

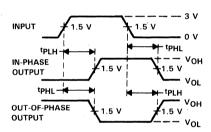
PARAMETER MEASUREMENT INFORMATION



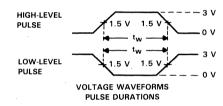
LOAD CIRCUIT

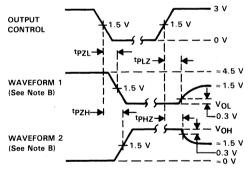
SWITCH POSITION TABLE TEST **S**1 **S2** Closed Closed t_{PLH} Closed Closed t_{PHL} Open Closed tPZH tPZL Closed Open Closed Closed ^tPHZ Closed Closed tpLZ

TIMING 3 V 1.5 V DATA INPUT VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES





VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.

FIGURE 1



SN54AS29821, SN54AS29822, SN74AS29821, SN74AS29822 10-RIT RUS INTERFACE FURTHORS WITH 3-STATE OUTPUTS

D2825, MAY 1986

 Designed to be Interchangeable with AMD AM29821 and AM29822

- Ideal for Data Synchronization of Wider Data Paths
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Production Circuitry
- Power-Up High Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS29821 will be true, and on the 'AS29822 will be complementary, to the data input.

A buffered output control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AS29821 . . . JT PACKAGE SN74AS29821 . . . DW OR NT PACKAGE

(TOP VIEW) ōc ∏₁ U24 VCC 1D 2 23 10 2D 3 22 20 21 7 30 30 □4 4D 🛮 5 20 40 50 🗇 19/7 50 18 60 60 □ 7D 🗆 8 17 70 8D [16 80 9D 110 15 9Q 10D []11 14 100 GND □12 13 CLK

SN54AS29821 . . . FK PACKAGE SN74AS29821 . . . FN PACKAGE

> (TOP VIEW) U24] VCC oc I 23 10 22 20 1D 2 20 □3 21 30 3DT 450 40 5DT 7 5a 6<u>D</u> | 17 18 T 6Q 707 770 8D7 16∏80 90 🗖 10 15 90 10D []11 14 100 13 FI CLK

SN54AS29822 . . . FK PACKAGE SN74AS29822 . . . FN PACKAGE (TOP VIEW)

NC-No internal connection

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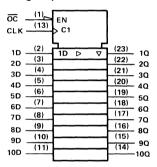


The SN54AS29821 and SN54AS29822 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS29821 and SN74AS29822 are characterized for operation from 0°C to 70°C.

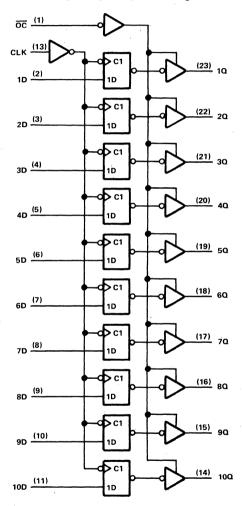
'AS29821 FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
оc	CLK	D	Q
L	Ť	Н	Н
L 1	1	L	L
L	L	Х	a_0
Н	X	Х	Z

'AS29821 logic symbol†



'AS29821 logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



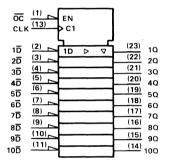
Pin numbers shown are for DW, JT, and NT packages.

SN54AS29822, SN74AS29822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

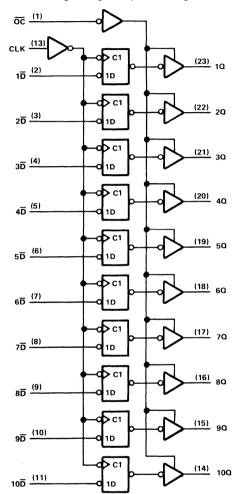
'AS29822 FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS		ОИТРИТ
ŌĊ	CLK	D	α
L	1	Н	L
L	1	L	н
L	L	Χ	αo
н	X	Χ	Z

'AS29822 logic symbol[†]



'AS29822 logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D2825, JANUARY 1986

- Functionally Equivalent to AMD's AM29823 and AM29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- **Outputs Have Undershoot Protection** Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

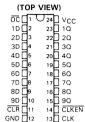
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable (CLKEN) low, the nine Dtype edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'ALS29823 has noninverting D inputs and the 'ALS29824 has inverting D inputs. Taking the CLR input low causes the nine Q outputs to go low independently of the clock.

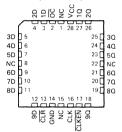
A buffered output-control input (OC)can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the highimpedance state.

SN54ALS29823 . . . JT PACKAGE SN74ALS29823 . . . DW OR NT PACKAGE



SN54ALS29823 . . . FK PACKAGE SN74ALS29823 . . . FN PACKAGE

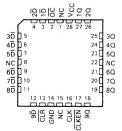
(TOP VIEW)



SN54ALS29824 . . . JT PACKAGE SN74ALS29824 . . . DW OR NT PACKAGE

> (TOP VIEW) U24 VCC 1D [2D [23 10 22 20 30 □4 21 30 4D ☐ 5 5D ☐ 6 20 40] 5Q 18 60 6D □7 7D 78] 7Q 17 8D []9 16 80 9D ☐10 15 90 CLR 11 14 CLKEN GND 12 13 CLK

SN54ALS29824 . . . FK PACKAGE SN74ALS29824 . . . FN PACKAGE (TOP VIEW)



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The SN54AS' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74AS' family is characterized for operation from 0 °C to 70 °C.

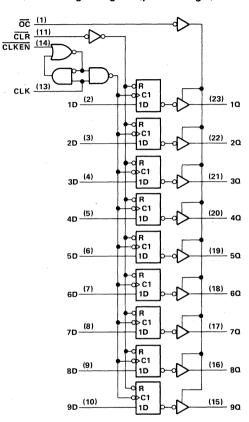
'ALS29823 FUNCTION TABLE

	INPUTS							
ОC	CLR	CLKEN	CLK	D	a			
L	L	×	X	X	L			
L	Н	L	†	Н	н			
L	Н	L	1	L	L			
L	Н	н	X	X	α ₀			
H	X	X	X	Χ	z			

'ALS29823 logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'ALS29823 logic diagram (positive logic)



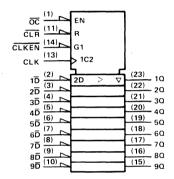


SN54ALS29824, SN74ALS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS29824 FUNCTION TABLE

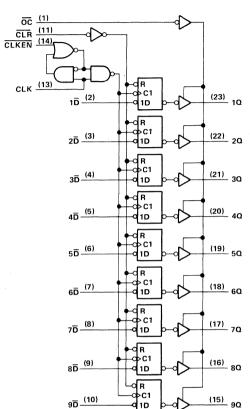
	INPUTS							
ОC	CLR	CLKEN	CLK	D	α			
L	L	X	X	Χ	L			
L	н	L	†	Н	L			
L	н	L	1	L	н			
L	н	Н	X	Χ	α ₀			
Н	X	Χ	X	X	z			

'ALS29824 logic symbol[†]



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS29824 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) Supply voltage, VCC 7 V Input voltage 5.5 V Voltage applied to a disabled 3-state output 5.5 V Input current 100 mA Output current -30 mA to 5 mA Operating free-air temperature range: SN54ALS29823, SN54ALS29824 -55°C to 125°C SN74ALS29823, SN74ALS29824 0°C to 70°C

Storage temperature range -65°C to 150°C

recommended operating conditions

			1	SN54ALS29823 SN54ALS29824			SN74ALS29823 SN74ALS29824			
			MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V	
VIH	High-level input voltage		2			2			V	
VIL	Low-level input voltage				0.7			0.8	V	
ГОН	High-level output currer	t			- 15			- 24	mA	
loL	Low-level output curren	t			32			48	mA	
	Pulse duration	CLR low	•							
t _W	Pulse duration	CLK high or low							ns	
	C-4 +i	CLR inactive								
t _{su}	Setup time	Data							ns	
	before CLK1	CLKEN high or low].			1	
th	Hold time, CLKEN or da	ta after CLK↑				T			ns	
TA	Operating free-air tempe	erature	- 55		125	0		70	°C	



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS†			54ALS2 54ALS2		SN74ALS29823 SN74ALS29824			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
VIK		V _{CC} = MIN	I _I = -18 mA			-1.2			-1.2	٧
		$V_{CC} = MIN \text{ to MAX},$	I _{OH} = -0.4 mA	Vcc	- 2		Vcc	-2		
Vон		$V_{CC} = MIN,$	$I_{OH} = -15 \text{ mA}$	2.4	3.3					V
		$V_{CC} = MIN,$	$I_{OH} = -24 \text{ mA}$				2.4	3.2]
VOL		$V_{CC} = MIN,$	$I_{OL} = 32 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = MIN,$	I _{OL} = 48 mA					0.35	0.5	
lozh		$V_{CC} = MAX$,	$V_0 = 2.4 \text{ V}$			20			20	μΑ
lozL		$V_{CC} = MAX$,	$V_0 = 0.4 \text{ V}$			- 20			- 20	μΑ
11		$V_{CC} = MAX$,	V _I = 5.5 V			0.1			0.1	mA
ΊΗ		V _{CC} = MAX,	V _I = 2.7 V			20			20	μΑ
IIL		V _{CC} = MAX,	V ₁ = 0.4 V			-0.1			-0.1	mA
los §		$V_{CC} = MAX$,	$V_O = 0 V$	- 75		- 250	- 75		-250	mA
			Outputs high							
	'ALS29823		Outputs low] .
lcc		V _{CC} = MAX	Outputs disabled		48			48		mA
1.00		VCC - WIAX	Outputs high] ""A
	'ALS29824		Outputs low							
			Outputs disabled		48			48		

 $^{^\}dagger$ For conditions shown as MIN or MAX, use appropriate value specificed under recommended operating conditions.

Additional Information on these products can be obtained from the factory as it becomes available.

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

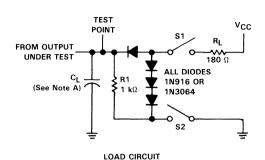
switching characteristics

200000000000000000000000000000000000000	FROM	то	TEST	TA			$T_A = 25$ °C $T_A = MIN TO MAX^{\dagger}$ 'ALS29823 SN54ALS29823 SN74ALS		= MIN TO MAX [†] 9823 SN74ALS29823			
PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS See Figure 1								UNIT	
			occ rigure r	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH			C _I = 300 pF									
^t PHL	CLK Any	CLK	Any O	CL = 300 pr								ns
tPLH	OLK ,		Anya	C _L = 50 pF		5.5						113
· tphl			CL - 50 bi		6.5							
tPHL	CLR	Any Q	$C_L = 50 pF$		13						ns	
^t PZH			$C_1 = 300 \text{ pF}$									
tPZL	oc	Any Q	GE - 300 pr								ns	
[†] PZH		Ally C	$C_I = 50 \text{ pF}$		12						113	
tpZL			GL - 00 bi		11							
^t PHZ			$C_L = 50 pF$									
tPLZ	oc	Any 0	OC Any Q	5 30 pi								ns
t _{PHZ}		/, a	$C_1 = 5 pF$		5						,,,,	
tPLZ			or abi		5.5							

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

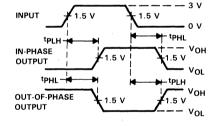
PARAMETER MEASUREMENT INFORMATION



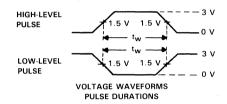
SWITCH POSITION TABLE								
TEST	S1	S2						
tPLH	Closed	Closed						
t _{PHL}	Closed	Closed						
tPZH	Open	Closed						
tPZL	Closed	Open						
^t PHZ	Closed	Closed						
^t PLZ	Closed	Closed						

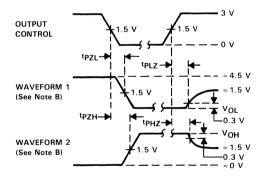
TIMING INPUT DATA INPUT

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES





VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_\Gamma \leq 2.5~ns$, $t_f \leq 2.5 \text{ ns.}$

FIGURE 1



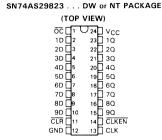
- Designed to be Interchangeable with AMD AM29823 and AM29824
- Ideal for Data Synchronization of Wider **Data Paths**
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with
- **Outputs Have Undershoot Protection** Circuitry
- Power-Up High-Impedance State
- **Buffered Control Inputs to Reduce DC** Loading Effects
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working reaisters.

With the clock enable (CLKEN) low, the nine Dtype edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'AS29823 has noninverting D inputs and the 'AS29824 has inverting D inputs. Taking the CLR input low causes the nine Q outputs to go low independently of the clock.

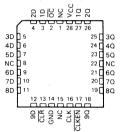
The buffered output-control input (OC) can be used to place the nine outputs in either a normal logic state (high or low levels) or a highimpedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



SN54AS29823 . . . JT PACKAGE

SN54AS29823 . . . FK PACKAGE SN74AS29823 . . . FN PACKAGE

(TOP VIEW)



SN54AS29824 . . . JT PACKAGE SN74AS29824 . . . DW or NT PACKAGE

> (TOP VIEW) U24□ v_{CC} oc 📭 23 10 1D 2 22 20 21 30 2页 □3 30 □4 20 40 4D □5 50 ☐6 19 50 6D 🗗 18 60 70 A 17 70 8D [16 80 15 90 14 CLKEN 90 110

SN54AS29824 . . . FK PACKAGE SN74AS29824 . . . FN PACKAGE (TOP VIEW)

13 CLK

CER 11

GND 🛮 12

NC - No internal connection

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products without notice.

The SN54AS29823 and SN54AS29824 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74AS29823 and SN74AS29824 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

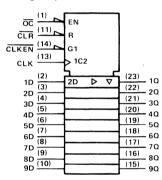
'AS29823

	INPUTS								
ŌĈ	CLR	CLKEN	CLK	D	α				
L	L	X	X	Х	L				
L	Н	L	1	Н	Н				
L	Н	L .	1	L	L				
L	Н	• н	X	X	a_0				
Н.	X	X	X	X	Z				

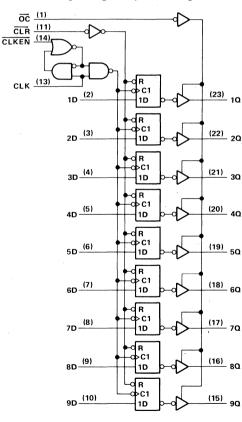
'AS29824

	INPUTS								
ŌC	CLR	CLKEN	CLK	D	Q				
L	F	Х	X	Х	L				
L	Н	L	1	Н	L				
L	Н	Ł	1	L	Н				
L	Н	Н	X	Х	αo				
н	X	X	×	Х	Z				

'AS29823 logic symbol†



'AS29823 logic diagram (positive logic)

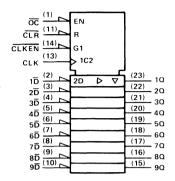


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

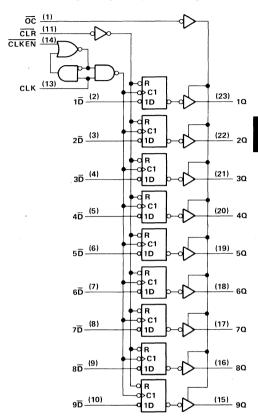


SN54AS29824, SN74AS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS29824 logic symbol[†]



'AS29824 logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

D2829, JANUARY 1986

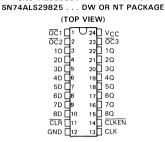
- Functionally Equivalent to AMD's AM29825 and AM29826
- Improved IOH Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29825 has non-inverting D inputs and the 'ALS29826 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ input low causes the eight Ω outputs to go low independently of the clock.

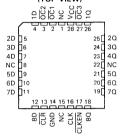
Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a busorganized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



SN54ALS29825 ... JT PACKAGE

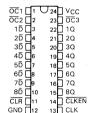
SN54ALS29825 . . . FK PACKAGE SN74ALS29825 . . . FN PACKAGE

(TOP VIEW)



SN54ALS29826 . . . JT PACKAGE SN74ALS29826 . . . DW OR NT PACKAGE

(TOP VIEW)



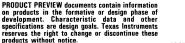
SN54ALS29826 . . . FK PACKAGE SN74ALS29826 . . . FN PACKAGE

(TOP VIEW)



NC-No internal connection

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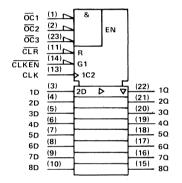
The SN54' family is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74' family is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

'ALS29825 FUNCTION TABLE

	OUTPUT				
OC*	CLR	CLKEN	CLK	D	α
L	L	X	Х	Х	L
L	н	L	†	н	н
L	Н	L	↑	L	L
L	н	Н	X	Х	σ_0
н	X	×	X	Х	Z

 $\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ is high. $\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

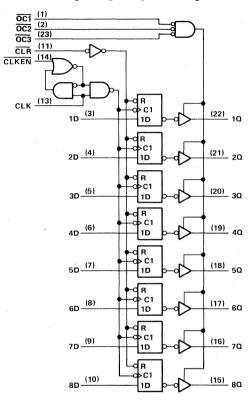
'ALS29825 logic symbol[†]



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

Pin numbers shown are for DW, JT, and NT packages.

'ALS29825 logic diagram (positive logic)



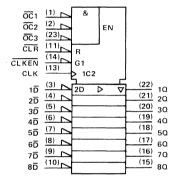
'ALS29826 FUNCTION TABLE

1		INPUTS			OUTPUT
OC*	CLR	CLKEN	CLK	Ď	Q
L	L	X	X	Х	L
L	Н	L	1	Н	L
L	Н	L	†	L	н
L	Н	Н	X	X	σ_0
Н	X	X	X	X	Z

 $\overline{OC}^* = H \text{ if any of } \overline{OC}1, \overline{OC}2, \text{ or } \overline{OC}3 \text{ is high.}$

 $\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

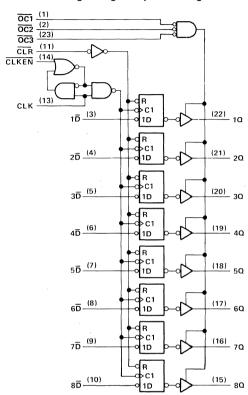
'ALS29826 logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for DW, JT, and NT packages.

'ALS29826 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Input current
Output current
Operating free-air temperature range:
SN54ALS29825, SN54ALS29826
SN74ALS29825, SN74ALS29826
Storage temperature range65 to 150 °C

recommended operating conditions

				SN54ALS29825 SN54ALS29826		SN74ALS29825 SN74ALS29826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX]
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				- 15			-24	mA
lOL	Low-level output current				32			48	mA
		CLR low							ns
t_W	Pulse duration	CLK high							
		CLK low							
		CLR inactive							
t _{su}	Setup time before CLK†	tup time before CLK† Data							ns
		CLKEN high or low							7
	11.11 1 6. 01.14	Data							
th	Hold time, data after CLK↑	CLKEN							ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

,	PARAMETER	TEST CONDIT	rions†		SN54ALS29825 SN54ALS29826			SN74ALS29825 SN74ALS29826		
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}		V _{CC} = MIN,	$I_J = -18 \text{ mA}$			-1.2			- 1.2	V
		V _{CC} = MIN to MAX,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		V _{CC} -2	2		
Voн		V _{CC} = MIN,	IOH = -15 mA	2.4	3.3					7 v
		V _{CC} = MIN,	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							
VOL		V _{CC} = MIN,	$I_{OL} = 32 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL		V _{CC} = MIN,	I _{OL} = 48 mA					0.35	0.5]
lozh		V _{CC} = MAX,	$V_0 = 2.4 \text{ V}$			20			20	μA
lozL		V _{CC} = MAX,	$V_0 = 0.4 V$			- 20			- 20	μΑ
4		$V_{CC} = MAX$,	$V_{I} = 5.5 V$			0.1			0.1	mA
ЧH		$V_{CC} = MAX$,	$V_{ } = 2.7 V$			20			20	μA
1/L		$V_{CC} = MAX,$	$V_I = 0.4 V$			-0.1			-0.1	mA
los§		$V_{CC} = MAX,$	$V_0 = 0 V$	- 75		- 250	- 75		- 250	mA
			Outputs high				Ī		-	
	'ALS29825		Outputs low							
		V _{CC} = MAX	Outputs disabled		48			48] [
lcc		ACC = INIAX	Outputs high] '''' [
	'ALS29826		Outputs low							
	N=WP-1		Outputs disabled		48			48		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

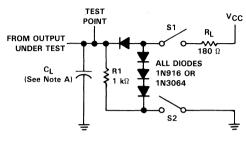
switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	Τ _Δ Ά			MAX [†] SN74AL								
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	1				
^t PLH	CLK		C ₁ = 300 pF												
tPHL		LK Any Q	С[= 300 рі								ns				
tPLH		A.1., Q	C ₁ = 50 pF		6]				
^t PHL			СС - 30 рі		7										
^t PHL	CLR	Any Q	$C_L = 50 pF$		13						ns				
^t PZH						1	$C_1 = 300 pF$]
tPZL	oc i	Any Q	Any O	с 300 рг								ns			
^t PZH		7.117 @	C _I ≈ 50 pF		12] "				
tPZL			С[- 30 рі		11										
^t PHZ			C _I ≈ 50 pF												
tPLZ	oc	Any Q	ο _L = 30 μι								ns				
tPHZ		1 ' 1	Aily C	Ally U	Ally Q	Ally C	C _I ≈ 5 pF		5] ""
tPLZ			CL ~ 3 pr		6	~~~									

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Additional information on these products can be obtained from the factory as it becomes available.

PARAMETER MEASUREMENT INFORMATION

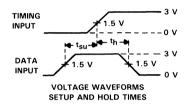


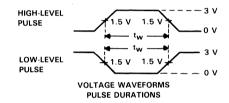
SWITCH POSITION TABLE									
TEST	S1	S2							
^t PLH	Closed	Closed							
^t PHL	Closed	Closed							
^t PZH	Open -	Closed							
^t PZL	Closed	Open							
^t PHZ	Closed	Closed							

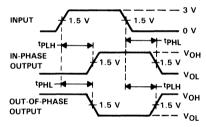
Closed

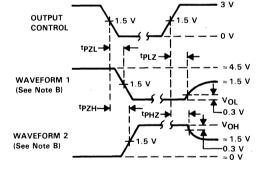
Closed

LOAD CIRCUIT









VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A.CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C . All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

FIGURE 1



PRODUCT PREVIEW

SN54AS29825, SN54AS29826, SN74AS29825, SN74AS29826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, MAY 1986

- Designed to be Interchangeable with AMD's AM29825 and AM29826
- Improved IOH Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Production Circuitry
- Power-Up High Impedance State
- Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

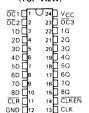
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock enable (CLKEN) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high will disable the clock buffer, thus latching the outputs. The 'AS29825 has inverting D inputs and the 'AS29826 has inverting D inputs. Taking the CLR input low causes the eight Q outputs to go low independently of the clock.

The buffered output-control inputs $(\overline{OC}1, \overline{OC}2,$ and $\overline{OC}3)$ can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a busorganized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

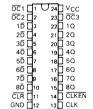
SN54AS29825 . . . JT PACKAGE SN74AS29825 . . . DW OR NT PACKAGE (TOP VIEW)



SN54AS29825 . . . FK PACKAGE SN74AS29825 . . . FN PACKAGE

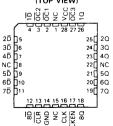
SN54AS29826 . . . JT PACKAGE SN74AS29826 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS29826 . . . FK PACKAGE SN74AS29826 . . . FN PACKAGE

(TOP VIEW)



NC - No internal connection

Texas Instruments

The SN54AS29825 and SN54AS29826 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS29825 and SN74AS29826 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

FUNCTION TABLES

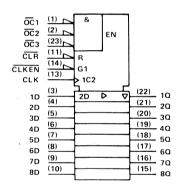
AS29825									
	OUTPUT	l							
ŌC*	CLR	CLKEN	CLK	D	Q	l			
L	L	Х	Х	Х	L	l			
L	Н	L	1	Н	Н	l			
L	H	L	1	L	L	l			
L	Н	Н	Х	Χ	Ω ₀	١			
Н	X	X	Х	Χ	z	l			

	OUTPUT									
ŌC*	CLR	CLKEN	CLK	D	α					
L	L	X	Х	Х	L					
L	Н	L	1	Н	L					
L	Н	L	1	L	. н					
L	Н	Н	X	Χ	α ₀					
Н	X	X	Χ	Χ	Z					
					L					

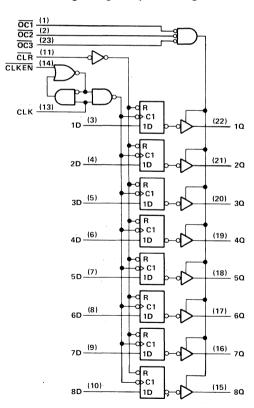
'AS29826

 $\overline{OC}^* = H$ if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ is high. $\overline{OC}^* = L$ if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

'AS29825 logic symbol†



'AS29825 logic diagram (positive logic)

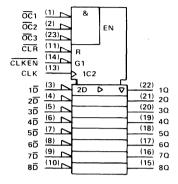


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

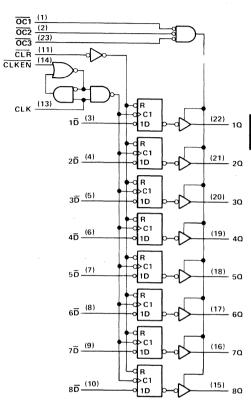


SN54AS29826, SN74AS29826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS29826 logic symbol†



'AS29826 logic diagram (positive logic)



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

D2912, JANUARY 1986-REVISED MAY 1986

- Functionally Equivalent to AM29827 and AM29828
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs
- Dependable Texas Instruments Quality and Reliability

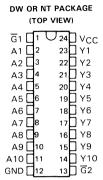
description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or busses carrying parity.

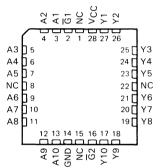
The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ is high, all ten outputs are in the high-impedance state.

The SN74ALS29827 provides true data and the SN74ALS29828 provides inverted data at the outputs.

The SN74' family is characterized for operation from 0° C to 70° C.



FN PACKAGE (TOP VIEW)



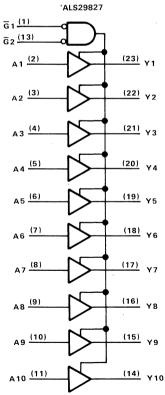
logic symbols†

	'ALS29827	
$\overline{G}_1 \xrightarrow{(1)}$ $\overline{G}_2 \xrightarrow{(13)}$	& EN	
A1 (2) A2 (3)	D 0	(23) (22) Y2
A3 (4) A4 (5)		(21) Y3 (20) Y4
A5 (6) A6 (7) A7 (8)		(19) Y5 (18) Y6 (17) Y7
A8 (9)		(16) Y8 (15) Y9
A9 (10) A10 (11)		(14) (14) Y10

	'ALS	29828		
$\overline{G}_1 \stackrel{(1)}{\frown}$ $\overline{G}_2 \stackrel{(13)}{\frown}$	&	EN		
A1 (2)	1	> 4	(23	- Y I
A2 (3)			(22	
A2 (4)			(21	
Δ4 (5)			(20	
A5 (6)			(19) Y5
A6 (7)			(18	Y6
A7 (8)			(17	Y7
A8 (9)			(16) Y8
A9 (10)			(19) Y9
A10 (11)			(14	1) Y10

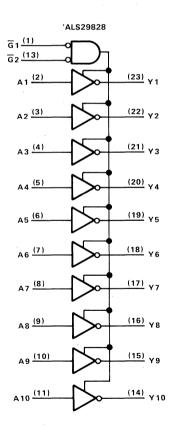
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



A10 (11) (14

Pin numbers shown are DW and NT packages.





SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	
Input voltage	V
Voltage applied to a disabled 3-state output	V
Operating free-air temperature range	°C
Storage temperature range65 °C to 150	°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
ViH	High-level input voltage	2	_	2	V
VIL	Low-level input voltage			0.8	V
ЮН	High-level output current			- 24	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.75 \text{ V}, I_{\parallel} = -18 \text{ mA}$			- 1.2	V
Vон		$V_{CC} = 4.75 \text{ V}, I_{OH} = -15 \text{ mA}$	2.4			V
VOH		$V_{CC} = 4.75 \text{ V}, I_{OH} = -24 \text{ mA}$	2			V
VOL		$V_{CC} = 4.75 \text{ V}, I_{OL} = 48 \text{ mA}$		0.35	0.5	V
lozh		$V_{CC} = 5.25 \text{ V}, V_{O} = 2.4 \text{ V}$			20	μΑ
lozL		$V_{CC} = 5.25 \text{ V}, V_{O} = 0.4 \text{ V}$			- 20	μΑ
1		$V_{CC} = 5.25 \text{ V}, V_{I} = 5.5 \text{ V}$			0.1	mA
Ιн		$V_{CC} = 5.25 \text{ V}, V_{I} = 2.7 \text{ V}$			20	μΑ
IIL.		$V_{CC} = 5.25 \text{ V}, V_{I} = 0.4 \text{ V}$			- 0.1	mA
los‡		$V_{CC} = 5.25 \text{ V}, V_{O} = 0 \text{ V}$	- 75		- 250	mA
laa	'ALS29827	$V_{CC} = 5.25 V$		25	40	mA
1CC	'ALS29828	V _{CC} = 5.25 V		25	40	A

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74ALS29827 switching characteristics

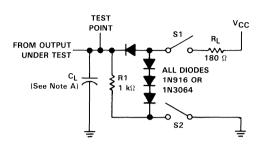
PARAMETER	FROM	TO	TEST . CONDITIONS		CC = 5 '		$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V},$ $T_A = 0 ^{\circ}\text{C to } 70 ^{\circ}\text{C}$	UNIT
	(INPUT)	(OUTPUT)	See Figure 1	MIN	TYP	MAX	MIN MAX	1
^t PLH			C _I = 300 pF		7.5	11	15	
^t PHL] _A	Y	CL = 300 pi		11	16	18	ns
^t PLH] ^	'	C _I = 50 pF		3.5	6	8	115
t _{PHL}			CL = 50 pr		6.5	8	10	
^t PZH			C _I = 300 pF		13	17	.20	
^t PZL	G	Y	CL = 300 pi		16	. 21	23	ns
^t PZH] "	,	C _I = 50 pF		6.5	12	15] ''s
^t PZL			CL = 30 pi		9.5	12	15	
^t PHZ			C _I = 50 pF		10	16	. 17	
tPLZ	G	Y	CL = 30 pr		4	9	12	ns
tPHZ]	'	C _I = 5 pF		4.5	8	9] "
^t PLZ			С[= 5 рг		4.5	8	9	

SN74ALS29828 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		CC = 5° A = 25°		V _{CC} = 4.75 T _A = 0°C		UNIT	
	(INFOT)	(001701)	See Figure 1	MIN	TYP	MAX	MIN	MAX	1	
tPLH			C ₁ = 300 pF		7.3	10		14		
^t PHL]	Y	C[= 300 pr		8.5	12.9		14]	
t _{PLH}		, T	$C_1 = 50 pF$		4	5.2		7	ns .	
^t PHL			C[= 50 pr		3	5.9		7.5		
^t PZH			$C_1 = 300 \text{ pF}$		13	17		20		
^t PZL	\overline{G}	Y	CL = 300 bi		16	21		23	ns	
tPZH	7	1	'	C ₁ = 50 pF		6.5	12		15	1 115
^t PZL	7		CL = 50 pr		9.5	12		15	1 .	
tPHZ			C 50 pF		10	16		17		
^t PLZ	<u>ਰ</u>	Y	$C_L = 50 pF$		4 -	. 9		12	1	
^t PHZ	7 '	,	$C_1 = 5 pF$		4.5	8		9	ns	
tPLZ	7		CL = 5 pr		4.5	8		9	1	

SN74ALS29827, SN74ALS29828 10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

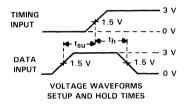


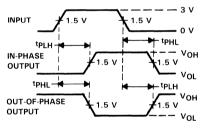
SWITCH POSITION TABLE					
TEST	S1	S2			
tPLH	Closed	Closed			
t _{PHL}	Closed	Closed			
tPZH	Open	Closed			
tPZL	Closed	Open			
tPHZ	Closed	Closed			

Closed

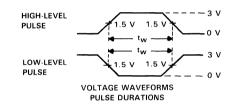
Closed

LOAD CIRCUIT

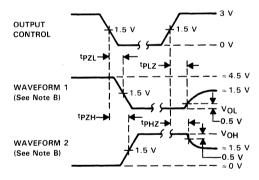




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



^tPLZ



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_I includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Q = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1



SN54AS29841, SN54AS29842, SN74AS29841, SN74AS29842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, MAY 1986

Designed to be Interchangeable with AMD AM29841 and AM29842

- **Bus-Structured Pinout**
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or **Buses with Parity**
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type. The 'AS29841 has noninverting data (D) inputs. The 'AS29842 has inverting \overline{D} inputs.

A buffered output control (OC) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\overline{OC}) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

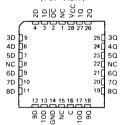
The SN54AS29841 and SN54AS29842 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS29841 and SN74AS29842 are characterized for operation from 0°C to 70°C.

SN54AS29841 . . . JT PACKAGE SN74AS29841 . . . DW OR NT PACKAGE (TOP VIEW)

> ōc □1 U24 VCC 1D 2 2D 3 23 10 3D 4 4D 5 21 30 20 40 19 50 5D 76 6D 🗖7 18 60 7D [17 70 16 80 80 16 9D | 10 10D | 11 15 90 14 100 GND 712 13Fi c

SN54AS29841 . . . FK PACKAGE SN74AS29841 . . . FN PACKAGE

(TOP VIEW)



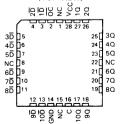
SN54AS29842 . . . JT PACKAGE SN74AS29842 . . . DW OR NT PACKAGE

(TOP VIEW)



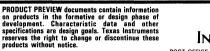
SN54AS29842 . . . FK PACKAGE SN74AS29842 . . . FN PACKAGE

(TOP VIEW)



NC - No internal connection

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ALS and AS Circuits

SN54AS29841, SN54AS29842, SN74AS29841, SN74AS29842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

FUNCTION TABLES

'AS29841

I	NPUTS	OUTPUT	
оc	С	D	α
L	Н	Н	Н
L	Н	L	L
L	L	X	QO
Н	Х	Х	Z

'AS29842

11	NPUT	OUTPUT	
ōc	С	D	Q
L	Н	Н	L
L	Н	L	Н
L	L	X	αo
Н	X	X	Z

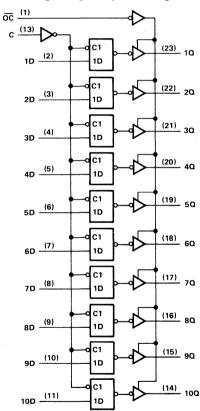
'AS29841 logic symbol[†]

OC (1) (13) (2) (3) (4) (4)	EN C1 1D D V	(23) (22) (21) 3Q
4D (5) 5D (6) 6D (7) 7D (8) (9)		(20) 4Q (19) 5Q (18) 6Q (17) 7Q (16) 8Q
9D (10) 10D (11)		(15) 9Q (14) 10Q

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'AS29841 logic diagram (positive logic)





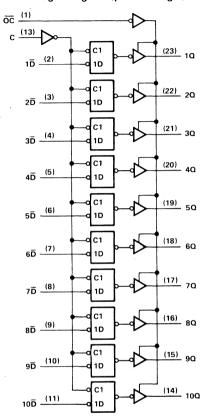
SN54AS29841, SN54AS29842, SN74AS29841, SN74AS29842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS29842 logic symbol†

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

'AS29842 logic diagram (positive logic)





SN54AS29843, SN54AS29844, SN74AS29843, SN74AS29844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2910, MAY 1986

Designed to be Interchangeable with AMD AM29843 and AM29844

- **Bus-Structured Pinout**
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or **Buses with Parity**
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type. The 'AS29843 has noninverting data (D) inputs. The 'AS29844 has inverting D inputs.

A buffered output control (OC) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

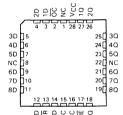
The output control (\overline{OC}) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54AS29843 and SN54AS29844 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS29843 and SN74AS29844 are characterized for operation from 0°C to 70°C.

SN54AS29843 . . . JT PACKAGE SN74AS29843 . . . DW OR NT PACKAGE



SN54AS29843 . . . FK PACKAGE SN74AS29843 . . . FN PACKAGE (TOP VIEW)



SN54AS29844 . . . JT PACKAGE SN74AS29844 . . . DW or NT PACKAGE (TOP VIEW)

SN54AS29844 . . . FK PACKAGE SN74AS29844 . . . FN PACKAGE (TOP VIEW)

14 PRE

13 C

NC No internal connection

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FUNCTION TABLES

'AS29843

	1	OUTPUT			
PRE	CLR OC C D		Q		
· L	Х	L	Х	Х	• Н
Н	L	L	X	Х	L
н	Н	L	Н	L	L
н	Н	L	Н	н	н
н	Н	L	L	Х	σo
Х	X	Н	X	Х	· z

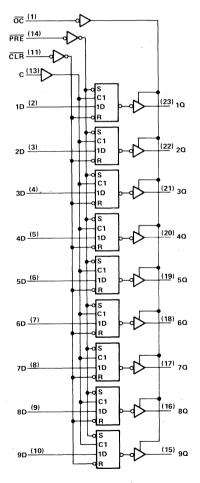
AS29844

		OUTPUT			
PRE	CLR	ос	С	D	Q
L	Х	L	Χ	Х	Н
Н	L	L	X	Χ	L
Н	Н	L	Н	L	н
Н	Н	L	Н	Н	L
Н	Н	L	L	X	σo
×	X	Н	X	X	z

'AS29843 logic symbol†

OC (1) PRE (14) CLR (11) C (13) 1D (2) (3) 3D (4) 4D (5) 5D (6) 6D (7) 6D (8)	EN S2 R C1	D	2∇	(23) 10 (22) 20 (21) 30 (20) 40 (19) 50 (18) 60 (17) 70
5D (6) 6D (7) 7D (8) 8D (9) 9D (10)				(19) 50 (18) 60 (17) 70 (16) 80 (15) 90

'AS29843 logic diagram (positive logic)



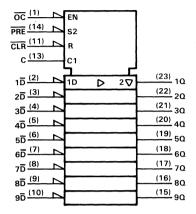
Pin numbers shown are for DW, JT, and NT packages.



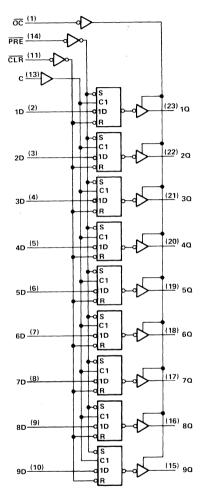
 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54AS29844, SN74AS29844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

'AS29844 logic symbol[†]



'AS29844 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D2910, MAY, 1986

Designed to be Interchangeable with AMD AM29845 and AM29846

- **Bus-Structured Pinout**
- **Provides Extra Bus-Driving Latches** Necessary for Wider Address/Data Paths or **Buses with Parity**
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The 'AS29845 has noninverting data (D) inputs. The 'AS29846 has inverting \overline{D} inputs. Since \overline{CLR} and PRE are independent of the clock, taking the CLR input low will cause the eight Q outputs to go low. Taking the PRE input low will cause the eight Q outputs to go high. When both PRE and CLR are taken low, the outputs will follow the preset condition.

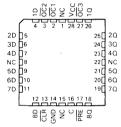
The buffered output controls input $(\overline{OC1}, \overline{OC2},$ and \overline{OC} 3) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the highimpedance state, the outputs neither load nor drive the bus lines significantly. The highimpedance state and increased drive provide the capability to drive the bus lines in a busorganized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AS29845 . . . JT PACKAGE SN74AS29845 . . . DW OR NT PACKAGE (TOP VIEW)

oc1 □1 U24 VCC 23 OC3 22 10 21 20 1D 🗌 2D [3D 🗖 5 20 7 30 19 40 18 50 4D 5D 7. 6D **□**8 17 60 7D 16 70 15 80 01 T 08 14∏ PRE CLR []11 GND 712 C.

SN54AS29845 . . . FK PACKAGE SN74AS29845 . . . FN PACKAGE

(TOP VIEW)



SN54AS29846 . . . JT PACKAGE SN74AS29846 . . . DW OR NT PACKAGE

(TOP VIEW)

J24 <u>VC</u> C
23 OC3
22 1 1 Q
21 20
20 3Q
19 40
18 🛚 5Q
17 60
16 70
15 8Q
14 PRE
13 🖸 C

SN54AS29846 . . . FK PACKAGE SN74AS29846 . . . FN PACKAGE

(TOP VIEW)



NC-No internal connection.

INSTRUMENTS

ALS and AS Circuits

SN54AS29845, SN54AS29846, SN74AS29845, SN74AS29846 8-BIT INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

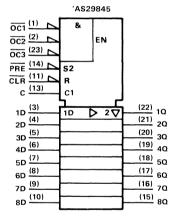
The SN54AS29845 and SN54AS29846 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74AS29845 and SN74AS29846 are characterized for operation from 0°C to 70°C.

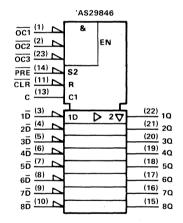
FUNCTION TABLES

	INPUTS								
PRE	CLR	OC1	ŌC2	OC3	С	D	Q		
L	Н	L	L	L	Х	Χ	Н		
Н	L	L	L	L	Χ	X	L		
L	L	L	L	L	Χ	X	н		
H	H	L	L	L	Н	L	L		
H	Н	L	L	Ł	Н	Н	Н		
Н	Н	L	L	L	L	Χ	σ0		
Х	Х	Х	Х	Н	Χ	Х	Z		
Х	X	Χ	Н	Х	Χ	Χ	Z		
X	X	Н	Х	Х	Х	X	Z		

		OUTPUT					
PRE	CLR	OC1	OC2	OC3	С	Ď	a
L	Н	L	L	L	Х	Х	Н
Н	L	L	L	L	Х	X	н
L	L	L	L	L	Χ	X	н
н	Н	L	L	L	Н	L	н
Н	Н	L	L	L	Н	Н	L
Н.	Н	L	L	L	L	X	Q _O
X	Х	Х	Х	Н	X	Х	Z
×	X	X	Н	X	X	X	z
L X	Х	Н	Х	Х	Х	Х	Z

logic symbols†



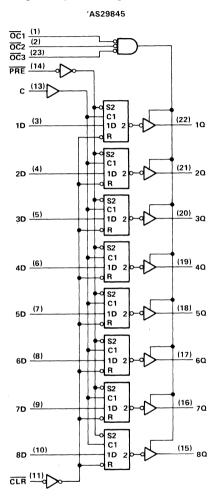


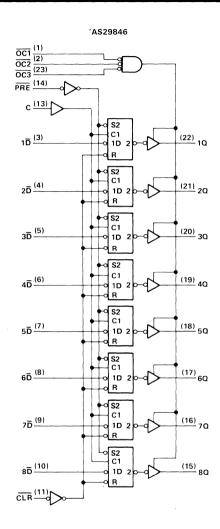
[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



SN54AS29845, SN54AS29846, SN74AS29845, SN74AS29846 8-BIT INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

logic diagrams (positive logic)





Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	٧
Input voltage	V
Voltage applied to a disabled 3-state output	V
Operating free-air temperature range: SN54AS'	С
SN74AS' 0°C to 70°	С
Storage temperature range -65 °C to 150 °	C



SN74ALS29861, SN74ALS29862 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2915, JANUARY 1986-REVISED MAY 1986

- Functionally Equivalent to AM29861 and AM29862
- Choice of True or Inverting Logic
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 10-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

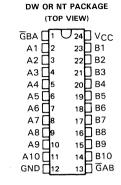
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs (GBA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

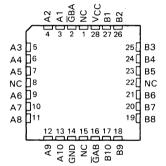
The SN74' family is characterized for operation from 0° C to 70° C.

FUNCTION TABLE

INP	UTS	OPERATION			
GAB	ĞΒΑ	ALS29861	ALS29862		
L	Η	A to B	Ā to B		
н	L	B to A	B̄ to A		
Н	н	Isolation	Isolation		
L	L	Latch A and B	Latch A and B		
		(A = B)	$(A = \overline{B})$		

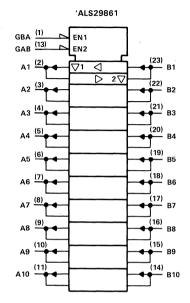


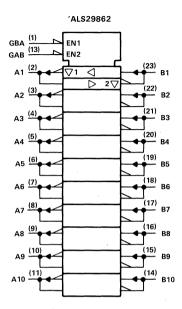
FN PACKAGE (TOP VIEW)



NC-No internal connection

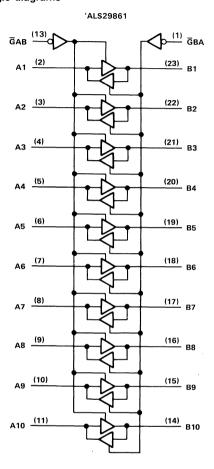
logic symbols†





 $^{^\}dagger$ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW and NT packages.

logic diagrams



'ALS29862 <u>Бав</u> (13) (23) B1 A1 (2) (22) B2 A2 (3) A3 (4) (21) B3 (<u>20)</u> B4 A4 (5) A5 (6) (19) B5 A6 (7) (<u>18)</u> B6 (<u>17)</u> B7 A7 (8) A8 (9) (16) B8 (<u>15)</u> B9 A9 (10) (14) B10 A10 (11)

Pin numbers shown are for DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted).

Supply voltage, VCC
Input voltage: All inputs and I/O ports
Operating free-air temperature range
Storage temperature range -65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	Ņ
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	٧
ІОН	High-level output current			- 24	mA
IOL	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.75 \text{ V}, I_{I} = -18 \text{ mA}$			-1.2	V	
VOH		$V_{CC} = 4.75 \text{ V}, I_{OH} = -15 \text{ mA}$	2.4			V	
I VOH		$V_{CC} = 4.75 \text{ V}, I_{OH} = -24 \text{ mA}$	2			'	
VOL		$V_{CC} = 4.75 \text{ V}, I_{OL} = 48 \text{ mA}$		0.35	0.5	V	
II.		$V_{CC} = 5.25 \text{ V}, V_{I} = 5.5 \text{ V}$			0.1	mA	
ΊΗ	Control inputs	$V_{CC} = 5.25 \text{ V}, V_1 = 2.7 \text{ V}$			20	μА	
''Н	A or B ports [‡]	VCC = 5.25 V, V1 = 2.7 V		-1.2 2.4 2 0.35 0.5 0.1	μΑ		
1	Control inputs	V _{CC} = 5.25 V, V ₁ = 0.4 V		20	mA		
ηL	A or B ports [‡]	- VCC = 5.25 V, V1 = 0.4 V			-0.1	"''	
los		$V_{CC} = 5.25 \text{ V}, V_{O} = 0 \text{ V}$	- 75		- 250	mA	
loo	'ALS29861	VCC = 5.25 V		40	65		
lcc	'ALS29862	VCC = 5.25 V		40	65	mA	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, T_A = 25 °C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

SN74ALS29861, SN74ALS29862 10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

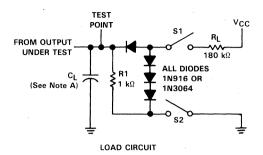
SN74ALS29861 switching characteristics

PARAMETER	FROM TO (INPUT) (OUTPUT)		TEST CONDITIONS		CC = 5		V _{CC} = 4.75	UNIT						
	(IIVFOT)	(0017017	See Figure 1	MIN	TYP	MAX	MIN	MAX 15 15 8 8 20						
^t PLH	}		$C_1 = 300 pF$		8	11		15						
^t PHL	A or B	BorA	C[= 300 pr		11	14		15	ns					
^t PLH	7 ~ 6 6	B 01 A	BOIA	BOIA	BOIA	BOIA	C _I = 50 pF		4.8	6		8] '''	
^t PHL	1				CL = 30 pr		5.2	6.2		8	1			
^t PZH	ĞАВ	A or B	A or B	$C_1 = 300 pF$		11	17		20					
†PZL	or			A or B	A or B	A or B	A or B	С[– 300 рі		17	21		23	ns
^t PZH	GBA						$C_1 = 50 pF$	1	6.5	12		15] '''	
†PZL	7 954		CL = 30 pr		9.5	12		15	1					
^t PHZ	GAB		$C_1 = 50 pF$		10	16		17						
^t PLZ	or G BA	A or B	CL = 50 pr		4.5	9		12	ns					
^t PHZ		7 01 6	$C_1 = 5 pF$		3.5	8		9] ''s					
^t PLZ] ""		CL = 5 PF		3.5	8		9	1					

SN74ALS29862 switching characteristics

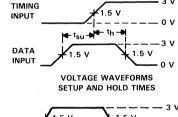
PARAMETER	FROM	то	TEST CONDITIONS	$V_{CC} = 5 V$. $T_{A} = 25 ^{\circ}C$			$V_{CC} = 4.75$ $T_{\Delta} = 0^{\circ}$	UNIT			
	(INPUT)	(OUTPUT)	See Figure 1	MIN	TYP	MAX	MIN	MAX	1		
tPLH			C _I = 300 pF		8	10		14			
^t PHL	A or B	B or A	CL = 300 pr		9	12.9		14	ns		
^t PLH	7 4016	BOIA	BOIA	C _I = 50 pF		4	5.2		7	1 115	
^t PHL	7						CL = 50 pr		3	5.9	
^t PZH	GAB		C _I = 300 pF		11	17		20			
[†] PZL	or	A or B	CL = 300 pr		17	21		23	ns		
^t PZH	GBA	AUIB	$C_1 = 50 \text{ pF}$		6.5	12		15	7 "		
tPZL	7 054	ł	CL = 50 pr		9.5	12		15	1		
tPHZ	- GAB		C _I = 50 pF		10	16		17			
tPLZ	or	A or B	CL = 50 pr		4.5	9		12	ns		
tPHZ	GBA	AOIB	$C_1 = 5 pF$		3.5	8		9	1 118		
tPLZ	7 984	1	CL = 5 pr		3.5	8		9	1		

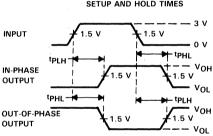
PARAMETER MEASUREMENT INFORMATION



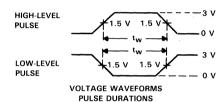
SWITC	SWITCH FOSITION TABLE									
TEST	S1	S2								
tPLH ·	Closed	Closed								
tPHL	Closed	Closed								
tPZH	Open	Closed								
tPZL	Closed	Open								
tPHZ	Closed	Closed								
tPLZ	Closed	Closed								

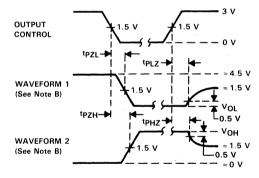
CWITCH DOCITION TABLE





VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A.CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C . All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

FIGURE 1



SN74ALS29863, SN74ALS29864 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2915, JANUARY 1986-REVISED MAY 1986

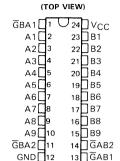
- Functionally Equivalent to AM29863 and AM29864
- Choice of True or Inverting Logic
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 9-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

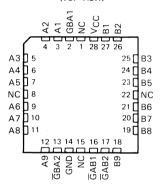
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA1$, $\overline{G}BA2$, $\overline{G}AB1$, and $\overline{G}AB2$).

The SN74' family is characterized for operation from 0°C to 70°C.



DW OR NT PACKAGE

FN PACKAGE (TOP VIEW)

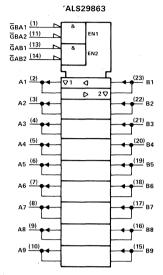


NC - No internal connection

FUNCTION TABLE

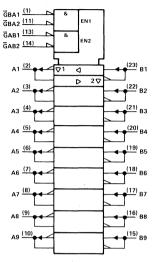
	ENABLE	INPUTS	3	OPERATION				
GAB1	GAB2	GBA1	GBA2	'ALS29863	'ALS29864			
L	L	L	L	Latch A and B	Latch A and B			
L	L	Н	X A to B		A to B			
L	L	X	Н	ALOB	A 10 B			
Н	X	L	L	B to A	B to A			
×	Н	L	L	BIOA	BIOA			
Н	X	Н	X					
Н	X	X	Н	Isolation	Isolation			
×	Н	X	Н	isolation	isolation			
×	Н	Н	X					

logic symbols†



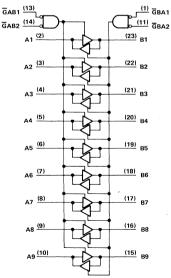
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS29864



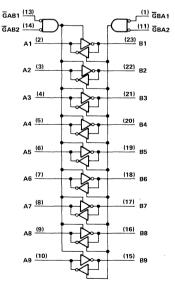
logic diagrams

'ALS29863



Pin numbers shown are for DW and NT packages.

'ALS29864





SN74ALS29863, SN74ALS29864 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless other	rwise noted)
Supply voltage, V _C C	0°C to 70°C

recommended operating conditions

1		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
ЮН	High-level output current			- 24	mA
IOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.75 \text{ V}, I_{I} = -18 \text{ mA}$			-1.2	V
νон		$V_{CC} = 4.75 \text{ V}, I_{OH} = -15 \text{ mA}$	2.4			V
٧ОН		$V_{CC} = 4.75 \text{ V}, I_{OH} = -24 \text{ mA}$	2			, v
VOL		$V_{CC} = 4.75 \text{ V}, I_{OL} = 48 \text{ mA}$		0.35	0.5	V
lį		$V_{CC} = 5.25 \text{ V}, V_{I} = 5.5 \text{ V}$			0.1	mA
Ιн	Control inputs	$V_{CC} = 5.25 \text{ V}, V_{I} = 2.7 \text{ V}$			20	μΑ
'IH	A or B ports [‡]	VCC = 5.25 V, V = 2.7 V			20	μΑ
1	Control inputs	V F 2F V V - 0 4 V			-0.1	
ΙL	A or B ports [‡]	$V_{CC} = 5.25 \text{ V}, V_{I} = 0.4 \text{ V}$			-0.1	mA
los §		$V_{CC} = 5.25 \text{ V}, V_{O} = 0 \text{ V}$	- 75		- 250	mA
lcc	'ALS29863	V _{CC} = 5.25 V		40	65	mA
,CC	'ALS29864	VCC = 3.23 V		40	65] ""A

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, T_A = 25 °C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

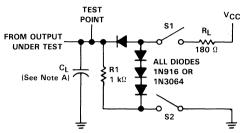
SN74ALS29863 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		CC = 5 \ A = 25°		$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V},$ $T_A = 0 ^{\circ}\text{C to } 70 ^{\circ}\text{C}$	UNIT								
	(1141 01)	(001101)	See Figure 1	MIN	TYP	MAX	MIN MAX	٦.								
^t PLH			C _I = 300 pF		7.5	11	15									
^t PHL	A or B	B or A	CL = 300 pr		11	16	18	ns								
tPLH	7 01 5	BOIA	BOLA	BUIA	$C_1 = 50 pF$		3.5	6	. 8	115						
tPHL					C[= 50 pr		6.5	8	10							
^t PZH	GAB	A or P	A or B	A or P	C _I = 300 pF		13	17	20							
^t PZL	or				A or B	A or B	A or B	A or B	A or B	A or B	A or B	A or B	A or B	,		16
tPZH	GBA	AOIB	$C_I = 50 pF$		6.5	12	15	lis								
^t PZL	GBA		CL = 50 pr		9.5	12	15									
tPHZ	GAB		$C_I = 50 \text{ pF}$		10	16	17									
tPLZ	or	A or B	A or B	A or B	A or B	A or B	A or B			4	9	12				
^t PHZ	GBA		C ₁ = 5 pF		4.5	8	9	ns								
^t PLZ	GBA					CL = 5 PF		4.5	8	9						

SN74ALS29864 switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS		CC = 5°		V _{CC} = 4.75 T _A = 0°C	UNIT			
	(INPOT)	(001701)	See Figure 1	MIN	TYP	MAX	MIN	MAX	1		
^t PLH			$C_{I} = 300 \text{ pF}$		8	11		14			
^t PHL	AorB	BorA	CL = 300 pr		10	12.9		14]		
^t PLH	7 4016	BULA	BOIA	BUIA	C _I = 50 pF		5	7	,	8	ns
tPHL /	1		C[= 50 pr		3	5.9		7.5	1		
^t PZH	ĞАВ				C _I = 300 pF		11	17		20	
tPZL	or	A or B	CL = 300 pr		19	23		24]		
^t PZH	GBA	AOIB	C _I = 50 pF		6.5	12		15	ns		
tPZL	GBA		C[= 50 pr		9.5	12		15	1		
tPHZ	GAB		. C FO-F		10	16		17			
^t PLZ		A or B	$C_L = 50 pF$		4	9		12	1		
^t PHZ	or GBA	AOFB	AOFB	C E = E		6	8		. 9	ns	
tPLZ	T GBA		$C_L = 5 pF$		3.5	8		9	1		

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

SWITCH POSITION TABLE TEST \$1 \$2 tPLH Closed Closed tPHL Closed Closed tpyH Open Closed

Closed

Closed

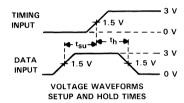
Closed

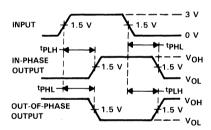
Open

Closed

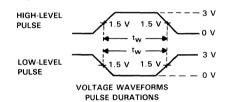
Closed

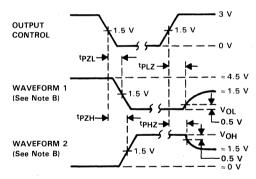
sold tpzH tpzH tpzL tpHZ tpHZ tpLZ





VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.

FIGURE 1

General Information

1

Numerical Index
Glossary
Explanation of Function Tables
D Flip-Flop and Latch Signal Conventions
Thermal Information
Parameter Measurement Information
Functional Index

Logic ALS and AS Circuits

2

Linear Interface ALS Circuits

3

Application Reports

4

Advanced Schottky Family (ALS/AS) Metastable Characteristics

Mechanical Data

5

Ordering Instructions Package Data

D2299, FEBRUARY 1986

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN75ALS130)
- Minimum Output Voltage of 3.11 V at IOH = -60 mA
- Fault Flag Circuit Output Signals Driver **Output Fault**
- **Fault-Detection Current Limit Circuit** Minimizes Power Dissipation During a Fault Condition
- **Advanced Low-Power Schottky Circuitry**
- **Dual Common Enable**
- Individual Fault Flags
- Designed to be an Improved Replacement for the MC3481

description

The SN75ALS126 quadruple line driver is

designed to meet the IBM360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at $I_{OH} = -59.3$ milliamperes) over the recommended ranges of supply voltage

condition by causing the fault-flag output to go low.

The SN75ALS126 is compatible with standard TTL logic and supply voltages. The SN75ALS126 employs the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault

(4.5 volts to 5.5 volts) and temperature (0°C to 70°C). Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground.

The SN75ALS126 will drive a 50-ohm load as required in the IBM GA22-6974-3 specification or a 90-ohm load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75ALS126 is characterized for operation from 0°C to 70°C.

SN75ALS126 . . . D, J, OR N PACKAGE (TOP VIEW)

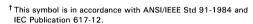
1Y 🗆	1	U ₁₆ VCC
1F 🗀	2	15 4Y
1 A 🗌	3	14 🗆 4 🖡
1,2G 🗌	4	13 🛮 4A
2A 🗌	5	12 3,4G
2F 🗌	6	11 🛮 3A
2Y 🗌	7	10 🔲 3₹
GND [8	9 🗌 3Y

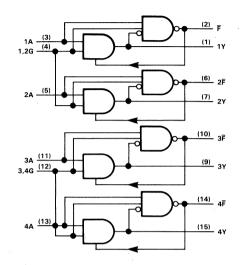
FUNCTION TABLE

INP	JTS	OUTPUTS				
G	Α	Υ	F			
L	X	L	Н			
н	Н	Н	Н			
н	H	s	L			

H = high level, L = low level, X = irrelevant, S = shorted to

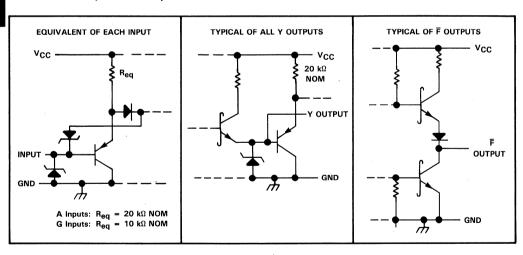
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schematics of inputs and outputs

Interface ALS Circuits



SN75ALS126 QUADRUPLE LINE DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	٧
Input voltage	٧
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 1):	
D package	Ν
J package	Ν
N package	Ν
Operating free-air temperature range	С
Storage temperature range65 °C to 150 °C	С
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D, N package 260 ol	
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package	С

NOTE 1: For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/°C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C.

recommended operating conditions

	M	IN	NOM	MAX	UNIT
Supply voltage, VCC	4	.5	5	5.95	V
High-level input voltage, VIH		2			V
Low-level input voltage, V _{IL}				0.8	V
High-level output current, IOH				-59.3	mA
Operating free-air temperature, TA		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

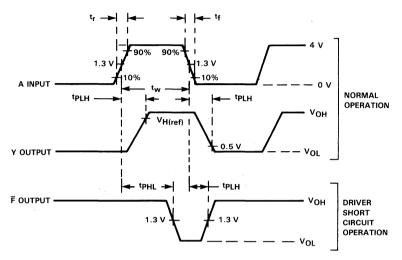
	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
VIK	Input clamp voltage	A,G	I _I = -18 mA		-1.5	V
		Y	$V_{CC} = 4.5 \text{ V}, I_{OH} = -59.3 \text{ mA}$ $V_{IH} = 2 \text{ V}$	3.11		
Vон	High-level output voltage	Y	$V_{CC} = 5.25 \text{ V}, I_{OH} = -41 \text{ mA}$ $V_{IH} = 2 \text{ V}$	3.9		V
		F	$V_{CC} = 4.5 \text{ V}, I_{OH} = -400 \mu\text{A}$ $V_{IH} = 2 \text{ V}$	2.5		
	Υ	$V_{CC} = 5.5 \text{ V}, I_{OL} = -240 \mu\text{A},$ $V_{IL} = 0.8 \text{V}$		0.15		
VOL	VOL Low-level output voltage	Y	$V_{CC} = 5.95 \text{ V}, I_{OL} =1 \text{ mA},$ $V_{IL} = 0.8 \text{ V}$		0.15	V
		F	$V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA}, \text{Y at 0 V}$		0.5	
IO(off)	Off-state output current	Υ	$V_{CC} = 4.5 \text{ V}, V_{IL} = 0, \qquad V_{O} = 3.11 \text{ V}$ $V_{CC} = 0, \qquad V_{IL} = 0, \qquad V_{O} = 3.11 \text{ V}$		100	μА
0(011)	(Off) Of State Output Carrent	Υ	$V_{CC} = 0$, $V_{IL} = 0$, $V_{O} = 3.11 V$		200	,
ų	Input current	G	V _{CC} = 4.5 V, V _{IH} = 5.5 V		100 400	μΑ
ΊΗ	High-level input current	A G	V _{CC} = 4.5 V, V _{IH} = 2.7 V		20 80	μΑ
ЧL	Low-level input current	A G	V _{CC} = 5.95 V, V _{IL} = 0.4 V			μΑ
	Chart	Υ F	V _{CC} = 5.5 V, V _O = 0	-15	- 5 - 100	
los	Short-circuit output	Y	V _{CC} = 5.95 V, V _O = 0	- 15	- 5 - 110	mA
1	Supply current, all		V _{CC} = 5.5 V, No load		25	
ІССН	outputs high		V _{CC} = 5.95 V, No load		27	mA
loci	Supply current,		V _{CC} = 5.5 V, No load		45	mA
ICCL	Y outputs low		V _{CC} = 5.95 V, No load		47	"'^

switching characteristics over recommended operating free-air temperature range

	PARAMETER	FROM	то	TEST CONDITIONS	MIN	MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output			V _{CC} = 4.5 V to 5.5 V,		30	ns
^t PHL	Propagation delay time, high-to-low-level output	A	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$R_L = 50 \Omega$, $C_L = 50 pF$, $V_{H(ref)} = 3.11 V$,		28	ns
^t PLH t _{PHL}	Ratio of propagation delay times			See Figures 1 and 2	0.3 ·	3	
^t PLH	Propagation delay time, low-to-high-level output	I A	Y	$V_{CC} = 5.25 \text{ V to } 5.95 \text{ V},$ $R_L = 90 \Omega, \qquad C_L = 50 \text{ pF},$		34	ns
tPHL	Propagation delay time, high-to-low-level output		Ť	$V_{H(ref)} = 3.9 V$ See Figures 1 and 2		34	ns
^t PLH	Propagation delay time, low-to-high-level output		F	$V_{CC} = 5 \text{ V}, R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$		45	ns
^t PHL	Propagation delay time, high-to-low-level output		'	See Figures 1 and 2		75	ns

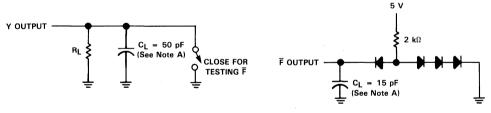


PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_f \le 6$ ns, $t_{f} \le 6$ ns, $t_{out} = 50 \Omega$.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



NOTE A: CL includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN75ALS126)
- Minimum Output Voltage of 3.11 V at IOH = −60 mA
- Fault-Flag Circuit Output Signals Driver Output Fault
- Fault-Detection Current Limit Circuit
 Minimizes Power Dissipation During a Fault
 Condition
- Advanced Low-Power Schottky Circuitry
- Common Enable and Common Fault Flag
- Designed to be an Improved Replacement for the MC3485

description

The SN75ALS130 quadruple line driver is designed to meet the IBM 360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at IOH = -59.3 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0 °C to 70 °C). Driver outputs use a fault-detection current limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75ALS130 is compatible with standard TTL logic and supply voltages.

D, J, OR N PACKAGE (TOP VIEW)

1Y 🗀	1	\bigcup_{16}	□vcc
1W [2	15] 4Y
1A [3	14	☐ 4W
G [4	13	☐ 4A
2A [5	12	□F
2W [6	11] 3A
2Y 🗌	7	10	□ sw
GND 🗌	8	9	□ 3Y

FUNCTION TABLE

INP	JTS	OUTPUTS				
G [†] A		Υ	ĒΤ	w		
L	Х	L	Н	Н		
Х	L	L	Н	Н		
Н	Н	H	Н	L		
Н	н	S	L	н		

H = high level, L = low level, X = irrelevant, S = shorted to ground

† G and F are common to the four drivers. If any of the four Y outputs is shorted, the Fault-Flag will respond.

The SN75ALS130 employs the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into the off (low) state and signals a fault condition by causing the fault-flag output to go low.

The SN75ALS130 will drive a 50-ohm load as required in the IBM GA22-6974-3 specification or a 90-ohm load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75ALS130 is characterized for operation from 0°C to 70°C.

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without notice.

logic symbol† 13 (12) F G (4) 23 Ω 33 43 11EN12,Z13 1A (3) 12 ♦ (2) 1W 11 21EN22,Z23 2A (5) G21 (<u>7)</u> 2Y <u>22</u> ℧ (6) 2W 21 D 31EN32,Z33 3A (11) G3 (9) 3Y 32 ℧ (<u>10)</u> 3W 31 41EN42,Z43 4A (13) G41 (<u>15)</u> 4Y

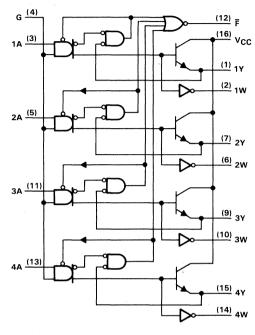
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

42 ♦

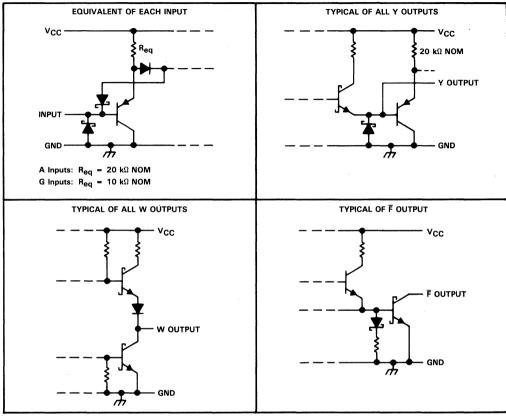
41

(14) 4W

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Continuous total dissipation at (or below)
25 °C free-air temperature (see Note 1): D package
J package 1025 mW
N package
Operating free-air temperature range
Storage temperature range65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N package 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C

NOTE 1: For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/ °C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.95	V
High-level input voltage, VIH	2			V
Low-level input voltage, V _{IL}			0.8	V
High-level output current, IOH			- 59.3	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

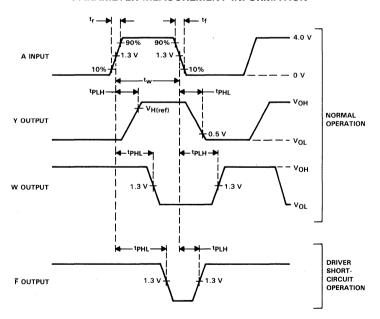
	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
VIK	Input clamp voltage	A,G	I _I = -18 mA		1.5	٧	
		Y	$V_{CC} = 4.5 \text{ V}, I_{OH} = -59.3 \text{ mA}, V_{IH} = 2 \text{ V}$	3.11			
Vон	High-level output voltage	Y	$V_{CC} = 5.25 \text{ V}, I_{OH} = -41 \text{ mA}, V_{IH} = 2 \text{ V}$	3.9		V	
		W	$V_{CC} = 4.5 \text{ V}, I_{OH} = -400 \mu\text{A}, V_{IH} = 2 \text{ V}$	2.5		1	
		Y	$V_{CC} = 5.5 \text{ V}, I_{OL} = -240 \mu\text{A}, V_{IL} = 0.8 \text{V}$		0.15		
VOL	Low-level output voltage	Υ	$V_{CC} = 5.95 \text{ V}, I_{OL} = -1 \text{ mA}, V_{IL} = 0.8 \text{ V}$		0.15	l _v	
VOL	OL Low-level output voltage	F	$V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA}, \qquad \text{Y at 0 V}$		0.5	ľ	
		W	$V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA}$		0.5	1	
la	Off-state output current	Υ	$V_{CC} = 4.5 \text{ V}, V_{IL} = 0, \qquad V_{O} = 3.11 \text{ V}$		100		
IO(off)	On-state output current	Υ	$V_{CC} = 0$, $V_{IL} = 0$, $V_{O} = 3.11 V$		200	μΑ	
ЮН	High-level output current	Ē	V _{CC} = 5.95 V, V _{OH} = 5.95 V		100	μΑ	
1.	Input current	A,	V _{CC} = 4.5 V, V _{IH} = 5.5 V		100	_	
l _l	input current	G	VCC = 4.5 V, VIH = 5.5 V		400	μΑ	
lu i	High-level input current	Α	V _{CC} = 4.5 V, V _{IH} = 2.7 V		20	μА	
lH	Trigit-level input current	G	VCC = 4.5 V, VIH = 2.7 V		80	μΑ	
I _I L	Low-level input current	Α	VCC = 5.95 V, V _{II} = 0.4 V		250	μА	
'IL		G	VCC = 0.00 V, VIL = 0.4 V		- 1000	μ.,	
		Y	$V_{CC} = 5.5 \text{ V}, V_{C} = 0$		- 5		
los	Short-circuit output	W	10C 313 17 10 3	- 15	- 100	mA	
.03		Y	$V_{CC} = 5.95 \text{V}, V_{CC} = 0$		– 5	""	
		W	100 111 1, 10	- 15	- 110		
Іссн	Supply current, all		V _{CC} = 5.5 V, No load		30	mA	
-ссп	outputs high		V _{CC} = 5.95 V, No load		32		
^I CCL	Supply current,		V _{CC} = 5.5 V, No load		45	mA	
CCL	Y outputs low		V _{CC} = 5.95 V, No load	1	47]	



switching characteristics over recommended operating free-air temperature range

	PARAMETER	FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output			V _{CC} = 4.5 V to 5.5 V,		30	ns
^t PHL	Propagation delay time, high-to-low-level output	A	Y	$R_L = 50 \Omega$, $C_L = 50 pF$, $V_{H(ref)} = 3.11 V$, Input $f = 1 MHz$		28	ns
tPLH tPHL	Ratio of propagation delay times			See Figures 1 and 2	0.3	3	
^t PLH	Propagation delay time, low-to-high-level output	А	v	$V_{CC} = 5.25 \text{ V to } 5.95 \text{ V},$ $R_L = 90 \Omega, \qquad C_L = 50 \text{ pF},$		34	ns
[†] PHL	Propagation delay time, high-to-low-level output		T	$V_{H(ref)} = 3.9 V$, Input $f = 5 MHz$ See Figures 1 and 2		34	ns
^t PLH	Propagation delay time, low-to-high-level output	А	w	$V_{CC} = 5 \text{ V},$ $R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$		34	ns
^t PHL	Propagation delay time, high-to-low-level output		VV	CL = 15 pr, See Figures 1 and 2		21	ns
^t PLH	Propagation delay time, low-to-high-level output	А	Ē	$V_{CC} = 5 \text{ V},$ $R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$		45	ns
tPHL	Propagation delay time, high-to-low-level output		,	See Figures 1 and 2		75	ns

PARAMETER MEASUREMENT INFORMATION

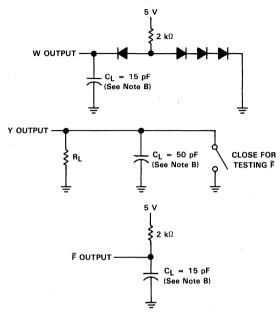


NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_{\Gamma} \le 6$ ns, $t_f \le 6 \text{ ns}, Z_{out} = 50 \Omega.$

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



PARAMETER MEASUREMENT INFORMATION



NOTE B: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

The SN75ALS160 eight-channel generalpurpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS160 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

DW. J. OR N PACKAGE (TOP VIEW) TE 1 20 VCC B1 ∏2 19 D1 В2 ∏3 18 D2 B3 ∏4 17 D D 3 GPIB В4 ∏5 16 D4 TERMINAL I/O В5 ∏6 15 D5 I/O PORTS **PORTS** в6 П7 14 D6 13 D7 B7 ∏8 В8 ∏9 12 D8 GND II 10 11 PE

FUNCTION TABLES

EACH DRIVER

EACH RECEIVER

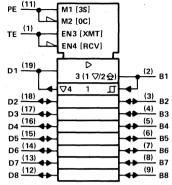
IF	NPUT	s	OUTPUT	11	NPUT	s	OUTPU
D	TE	PE	В	В	TE	PE	D
Н	Н	Н	Н	L	L	Х	L
L	Н	X	L	Н	L	Х	н
Н	X	L	Z [†]	Х	Н	Х	z
Χ	L	X	z†				

H = high level, L = low level, X = irrelevant,

Z = high-impedance state.

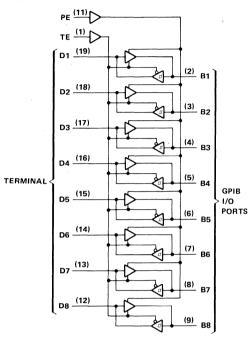
[†] This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic symbol† PE (11)

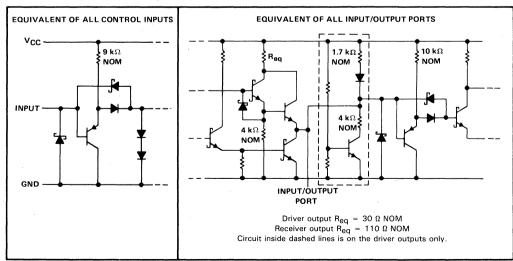


- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ∇ Designates 3-state outputs.
- ◆ Designates passive-pullup outputs.

logic diagram (positive logic)



schematics of inputs and outputs



SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)
Input voltage
Low-level driver output current
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package
J package
N package
Operating free-air temperature range
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package 300 °C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260 °C

- NOTES: 1. All voltage values are with respect to network ground terminal.
 - 2. For operation above 25 °C free-air temperature, derate the DW package to 720 mW at 70 °C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70 °C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, V _{IH}		2			V
Low-level input voltage, V _{IL}				0.8	V
	Bus ports with pullups active			- 5.2	mA
High-level output current, IOH	Terminal ports			-5.2 -800	μΑ
Law level autout aument 1-	. Bus ports			48	^
Low-level output current, IOL	w-level output current, IOL Terminal ports		16	mA	
Operating free-air temperature, TA		0		70	°C

SN75ALS160 OCTAL GENERAL PURPOSE INTERFACE BUS TRANSCEIVER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER			TEST	CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage		I _I = -18 mA				-0.8	- 1.5	V
V _{hys}	Hysteresis (V _{T+} - V _{T-})	Bus				0.4	0.65		V
V _{OH} ‡	High-level	Terminal	$I_{OH} = -800$	μА,	TE at 0.8 V	2.7	3.5		V
VOH.	output voltage	Bus	$I_{OH} = -5.2 \text{ r}$	nΑ,	PE and TE at 2 V	2.5	3.3		ľ
VOL	Low-level	Terminal	I _{OL} = 16 mA,	. ,	TE at 0.8 V		0.3	0.5	V
VOL	output voltage	Bus	I _{OL} = 48 mA,		TE at 2 V		0.35	0.5	· ·
lι	Input current at maximum input voltage	Terminal	V _I = 5.5 V				0.2	100	μΑ
liH .	High-level input current	Terminal,	V _I = 2.7 V				0.1	20	μΑ
IIL.	Low-level input current	PE, or TE	$V_{ } = 0.5 V$				- 10	- 100	μΑ
	Voltage at bus port		Driver disabled		$I_{I(bus)} = 0$	2.5	3.0	3.7	V
V _{I/O(bus)}	voltage at bus port				$I_{I(bus)} = -12 \text{ mA}$			- 1.5	ľ
					$V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$	- 1.3			
		Power on			$V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$	0		-3.2	
I _{I/O(bus)}	Current into bus port		Driver disabled	l	V _{I(bus)} = 2.5 V to 3.7 V			+ 2.5 - 3.2	mA .
					V _{I(bus)} = 3.7 V to 5 V	0		2.5	1
					$V_{I(bus)} = 5 \text{ V to } 5.5 \text{ V}$	0.7		2.5	Į
-		Power off	$V_{CC} = 0$,		$V_{I(bus)} = 0 V \text{ to } 2.5 V$			-40	μΑ
1	Short-circuit	Terminal				- 15	- 35	- 75	
los	output current	Bus				- 25	- 50	- 125	mA
1	Cumply assument		No load	Term	inal outputs low and enabled		42	56	
ICC	Supply current	*	INO IOAG	Bus o	outputs low and enabled		52	70	mA
C _{i/o(bus)}	Bus-port capacitance		V _{CC} = 5 V to f = 1 MHz	0 V	$V_{I/O} = 0 \text{ to } 2 \text{ V},$		30		pF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies to three-state outputs only.

SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

	PARAMETER	FROM	то	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
tour	Propagation delay time,					10	20	
tPLH	low-to-high-level output	Terminal	Bus	C _L = 30 pF,		10	20]
tou	Propagation delay time,	Termina	bus	See Figure 1		12	20	ns
tPHL	high-to-low-level output					12	20	
tout	Propagation delay time,					5	10	
	low-to-high-level output	Bus	Terminal	$C_L = 30 pF$,			10	ns
tou	Propagation delay time,	bus	Terminal	See Figure 2		7	14	115
tPHL	high-to-low-level output					· ·	14	
^t PZH	Output enable time to high level		Bus	C _L = 15 pF, See Figure 3		11	20	ns
^t PHZ	Output disable time from high level	TE				3	10	
tPZL	Output enable time to low level	16				18	35] "5
^t PLZ	Output disable time from low level					5	20]
^t PZH	Output enable time to high level					5	20	
^t PHZ	Output disable time from high level	TE	Terminal	$C_L = 15 pF$,		8	20	ns l
^t PZL	Output enable time to low level	1.	Terminal	See Figure 4		9	20] " 5
tPLZ	Output disable time from low level					8	20	
t _{en}	Output pull-up enable time	PE	Bus	$C_L = 15 pF$,		3	10	ns
^t dis	Output pull-up disable time		Dus	See Figure 5		4	12	_ '''s

 $^{^{\}dagger}$ Typical values are at T_A = 25 °C.

PARAMETER MEASUREMENT INFORMATION

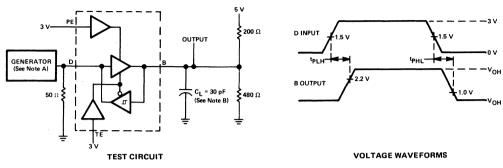


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

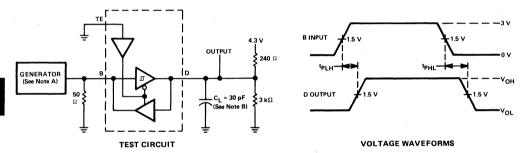


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

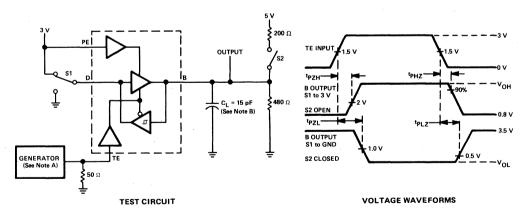


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} = 50 \ \Omega$.

B. C₁ includes probe and jig capacitance.



SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

PARAMETER MEASUREMENT INFORMATION

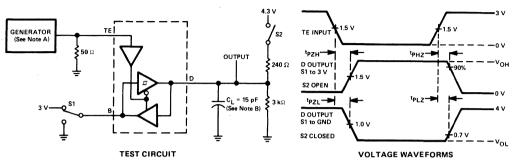


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

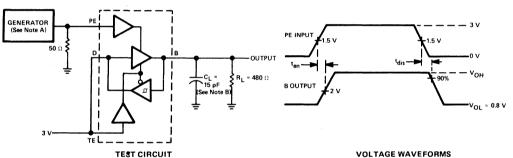
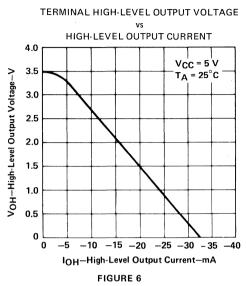


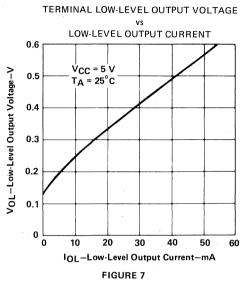
FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

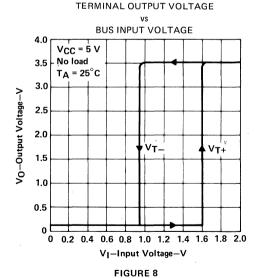
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} = 50 \Omega$.

B. C_L includes probe and jig capacitance.

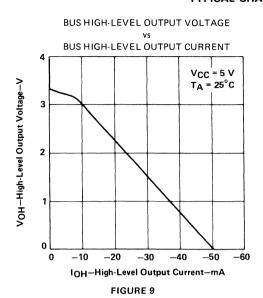
TYPICAL CHARACTERISTICS

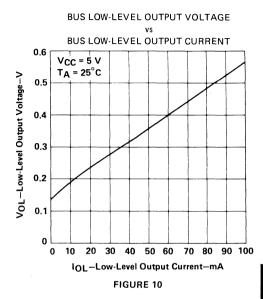


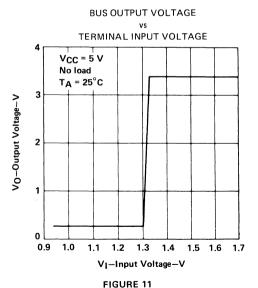


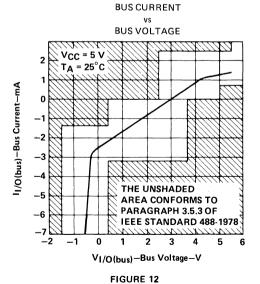


TYPICAL CHARACTERISTICS









TEXAS INSTRUMENTS

Interface ALS Circuits

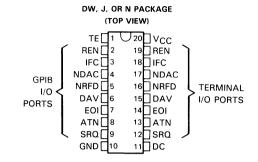
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

The SN75ALS161 eight-channel generalpurpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the busmanagement and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS161 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS161 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.



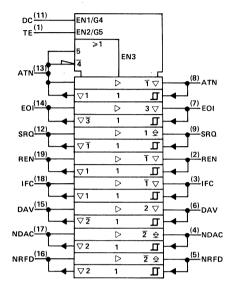
CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	Control
ATN	Attention	
SRQ	Service Request	Bus
REN	Remote Enable	Management
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data
NDAC	Not Data Accepted	Transfer
NRFD	Not Ready for Data	ranster

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when $V_{CC} = 0$. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

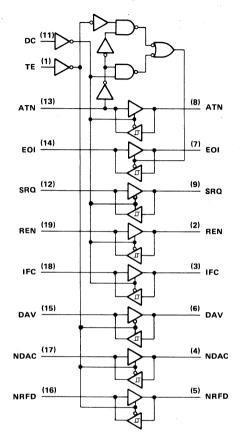
The SN75ALS161 is manufactured in a 20-pin package and is characterized for operation from 0 °C to 70 °C.

logic symbol†



- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- □ Designates 3-state outputs.
- ◆ Designates passive-pullup outputs.

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

C	CONTROL	.S	BI	JS-MANA	GEMENT	CHANNEL	.s	DATA-TRANSFER CHANNE			
DC	TE	ATN [†]	ATN [†]	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD	
				(Controlled by DC)					ntrolled b	y TE)	
Н	Н	Н		-		_	T	_		_	
Н	Н	L	R	T R	К	R R	R		R	R	
L	L	Н		Б.	-	_	R		_	_	
L	L	L	1. '.	R	ı	T	Т	R	Т	Т	
Н	L	Х	R	Т	R	R	R	R	Т	Т	
L	Н	X	T	R	Т	Т	T	Т	R	R	

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

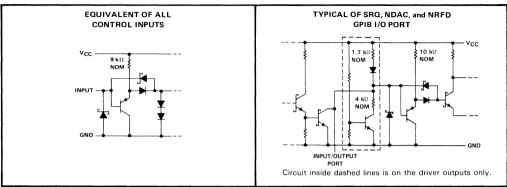
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

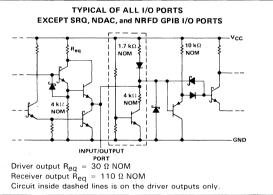
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):	
DW package	1125 mW
J package	1375 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	ge 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate the DW package to 720 mW at 70 °C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70 °C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.



OCTAL GENERAL PURPOSE INTERFACE BUS TRANSCEIVER

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, VIH		2			V
Low-level input voltage, V _{IL}			0.8	V	
IP to the second	Bus ports with pullups active			-5.2	mA
High-level output current, IOH	Terminal ports			-800	μА
Low lovel output ourset I	Bus ports			48	A
Low-level output current, IOL	Terminal ports			16	mA
Operating free-air temperature, TA		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CO	NDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage		$I_{\parallel} = -18 \text{ mA}$			-0.8	- 1.5	V
V_{hys}	Hysteresis (V _{T+} - V _{T-})	Bus			0.4	0.65		V
VoH [‡]	High-level	Terminal	$I_{OH} = -800 \mu A$		2.7	3.5		V
VOH.	output voltage	Bus	IOH = -5.2 mA		2.5	3.3		
Vai	Low-level	Terminal	I _{OL} = 16 mA			0.3	0.5	v
VOL	output voltage	Bus	$I_{OL} = 48 \text{ mA}$			0.35	0.5	·
1.	Input current at	Terminal	V _I = 5.5 V			0.2	100	μА
l _l	maximum input voltage	Terrinia	V = 5.5 V			0.2	100	μ.Λ.
hie .	High-level	Terminal	V _I = 2.7 V			0.1	20	μА
'IH	input current	and	V = 2.7 V	· · · · · · · · · · · · · · · · · · ·				μ, ,
IIL	Low-level $V_{I} = 0.5 \text{ V}$				- 10	- 100	μА	
'IL	input current	inputs		_				<i>P**</i>
V _{I/O(bus)}	Voltage at bus port		Driver disabled	$I_{I(bus)} = 0$	2.5	3.0	3.7	_v
- 1/O(bus)	voitage at bus port		Driver disabled	$I_{I(bus)} = -12 \text{ mA}$	1		- 1.5	
				$V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3			
				$V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$	0		-3.2	
				$V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$			+2.5	
I _{I/O(bus)}	Current into bus port	Power on,	Driver disabled	(I(Bus) 2.0 C to 0.7 C			-3.2	mA
				$V_{I(bus)} = 3.7 \text{ V to 5 V}$	0		2.5	
	•			$V_{I(bus)} = 5 V \text{ to } 5.5 V$	0.7		2.5	
		Power off	$V_{CC} = 0$,	$V_{I(bus)} = 0 V to 2.5 V$			- 40	μΑ
los	Short-circuit Terminal				- 15	- 35	- 75	mA
	output current	Bus			- 25			
^l cc	Supply current		No load,	TE and DC low		55	75	mA
C _{i/o(bus)}	Bus-port capacitance		$V_{CC} = 5 V \text{ to } 0 V,$		30			pF
-1/0(008)		,	$V_{I/O} = 0$ to 2 V, f = 1 MHz			<u> </u>		P'

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.



[‡]V_{OH} applies for three-state outputs only.

SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

	PARAMETER	FROM	то	TEST CONDITIONS	MIN TYP [†]	мах	UNIT	
tPLH	Propagation delay time, low-to-high-level output			C ₁ = 30 pF,	10	20	ns	
tPHL	Propagation delay time, high-to-low-level output	Terminal	Bus	See Figure 1	12	20	- 113	
tPLH	Propagation delay time, low-to-high-level output	D	Tamaiaal	C _L = 30 pF,	5	10		
tPHL	Propagation delay time, high-to-low-level output	Bus	Terminal	See Figure 2	7	14	ns	
tPZH	Output enable time to high level		BUS			30		
tPHZ	Output disable time from high level	TE or DC	(ATTN, EOI,	$C_{L} = 15 \text{ pF},$		20] _ [
tPZL	Output enable time to low level	1 12 01 00	REN, IFC,	See Figure 3		45	ns	
tPLZ	Output disable time from low level	1	and DAV)			20	1 !	
tPZH	Output enable time to high level					20		
tPHZ	Output disable time from high level	TE or DC	Terminal	$C_L = 15 pF,$		25]	
tPZL	Output enable time to low level	1 12 01 DC	reminai	See Figure 4		30	ns	
tPLZ	Output disable time from low level	<u> </u>	l			25	l	

 $^{^{\}dagger}$ All typical values are at $T_A = 25 \,^{\circ}$ C.

PARAMETER MEASUREMENT INFORMATION

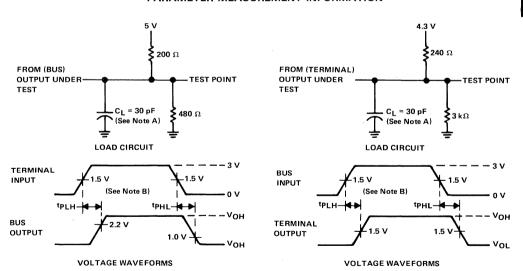


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

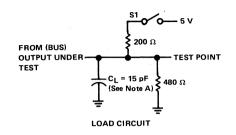
FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

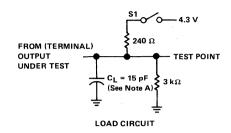
NOTES: A. C_L includes probe and jig capacitance.

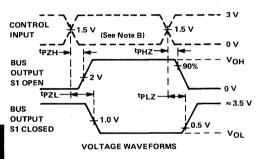
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} = 50 \Omega$.



PARAMETER MEASUREMENT INFORMATION







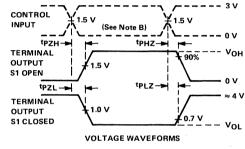


FIGURE 3. BUS ENABLE AND DISABLE TIMES

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

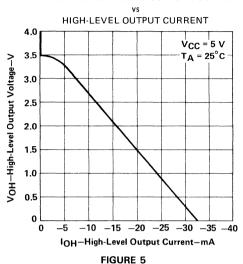
NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{Out} = 50 \Omega$.

SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE



TERMINAL LOW-LEVEL OUTPUT VOLTAGE

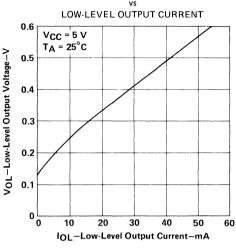


FIGURE 6

TERMINAL OUTPUT VOLTAGE

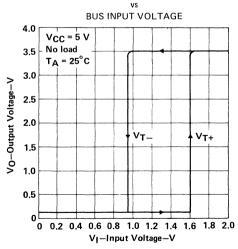
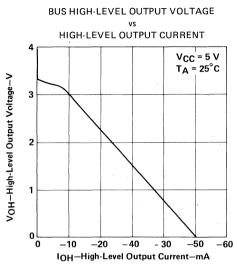
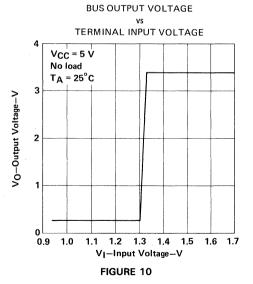


FIGURE 7

TYPICAL CHARACTERISTICS







BUS-LOW LEVEL OUTPUT VOLTAGE

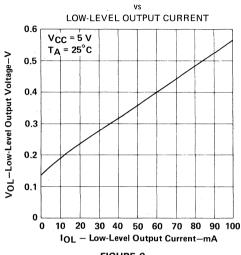
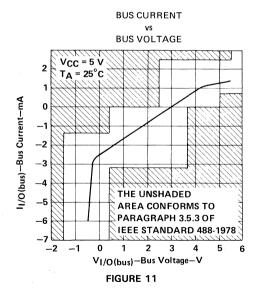


FIGURE 9





Interface ALS Circuits

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

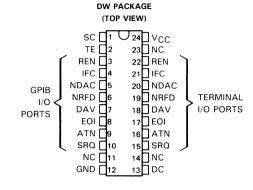
The SN75ALS162 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration

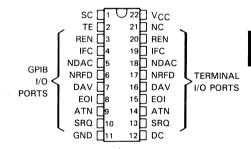
to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when $V_{CC}=0$. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS162 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C .



N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC-No internal connection.

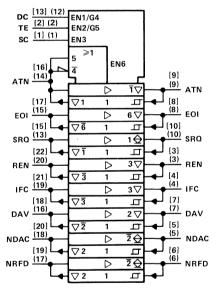
ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.



CHANNEL IDENTIFICATION TABLE

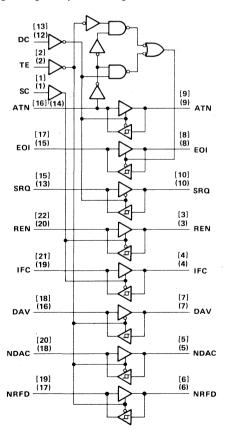
NAME	IDENTITY	CLASS
DC	Direction Control	
TE	Talk Enable	Control
sc	System Control	
ATN	Attention	
SRQ	Service Request	Bus
REN	Remote Enable	Management
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data
NDAC	Not Data Accepted	Transfer
NRFD	Not Ready for Data	rranster

logic symbol†



- $^\dagger This$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ▼ Designates 3-state outputs.
- ◆ Designates passive-pullup outputs.

logic diagram (positive logic)



- [] Denotes pin numbers for DW package.
- () Denotes pin numbers for N package.



SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

RECEIVE/TRANSMIT FUNCTION TABLE

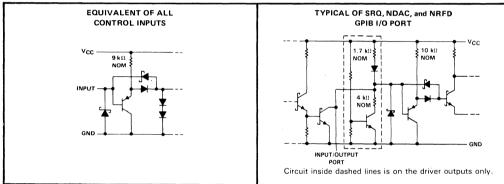
	CONT	ROLS		BUS-MANAGEMENT CHANNELS				DATA-TRANSFER CHANNELS			
sc	DC	TE	ATN [†]	ATN [†]	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlle	d by DC)	(Controlle	ed by SC)		(Co	ntrolled by	/ TE)
	Н	Н	Н	R	т			T	т	R	R
	Н	Н	L	1 " '			R	'	n n	Γ.	
	L	L	Н	т	R			R	R	т	т
	L	Ł	L	'	n			Т			1
	Н	L	Х	R	Т			R	R	T	T
	L	Н	Х	T	R			Т	Т	R	R
Н						Т	Т				
L						R	R				

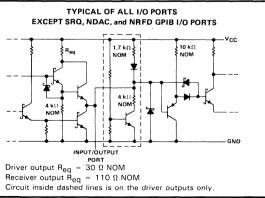
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†]ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs







OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage
Low-level driver output current
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):
DW package
N package
Operating free-air temperature range
Storage temperature range
Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate the DW package to 864 mW at 70 °C at the rate of 10.8 mW/ °C, and derate the N package to 1088 mW at 70 °C at the rate of 13.6 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, VCC			4.75	5	5.25	V
High-level input voltage, VIH			2			V
Low-level input voltage, V _{IL}					0.8	V
	Bus ports with 3-state outputs				- 5.2	mA
High-level output current, IOH	Terminal ports				0.8	μΑ
1 1 1	Bus ports	, , , , , , , , , , , , , , , , , , , ,			48	^
Low-level output current, IOL	Terminal ports				16	mA
Operating free-air temperature, TA			0		70	°C



SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CONDITIONS			TYP [†]	MAX	UNIT
VIK	Input clamp voltage		I _I = -18 mA			-0.8	- 1.5	V
V _{hys}	Hysteresis (V _{T+} - V _{T-})	Bus			0.4	0.65		V
v. t	High-level	Terminal	$I_{OH} = -800 \mu A$		2.7	3.5		V
^V он [‡]	output voltage	Bus	I _{OH} = -5.2 mA		2.5	3.3		V
VOL	Low-level	Terminal	I _{OL} = 16 mA			0.3	0.5	V
VOL	output voltage	Bus	I _{OL} = 48 mA			0.35	0.5	\ \
lj.	Input current at	Terminal	V _I = 5.5 V			0.2	100	μΑ
	maximum input voltage	Terminal						ļ
lіН	High-level input current	and	V _I = 2.7 V			0.1	20	μΑ
	Low-level	control						
կը Մ	input current	inputs	V _I = 0.5 V			- 10	- 100	μΑ
VI/O(bus)	Voltage at bus port	.out D		disabled I _{I(bus)} = 0		3.0	3.7	v
1/0(bus)	voltage at bus port		Driver disabled	$I_{I(bus)} = -12 \text{ mA}$			- 1.5] *
				$V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3			
				$V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$	0		-3.2	
II/O(bus)	Current into bus port	Power on	Driver disabled	$V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$			+ 2.5 - 3.2	mA
1/01003/	·			$V_{I(bus)} = 3.7 \text{ V to 5 V}$	0		2.5	
				V _{I(bus)} = 5 V to 5.5 V	0.7		2.5	
		Power off	V _{CC} = 0,	V _{I(bus)} = 0 V to 2.5 V			- 40	μΑ
1	Short-circuit	Terminal			- 15	- 35	- 75	mA
los	output current	Bus			- 25	- 50	- 125	IIIA
lcc	Supply current		No load,	TE, DC, and SC low		55	75	mA
C: /- //	Bus-port capacitance		$V_{CC} = 5 V \text{ to } 0 V,$		30			pF
C _{i/o(bus)}			$V_{I/O} = 0$ to 2 V, f = 1 MHz					ρı

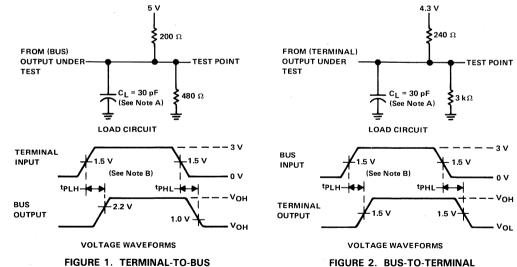
 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies for three-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

	PARAMETER	FROM	то	TEST CONDITIONS	MIN TYP	† MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	Terminal	Bus	C _L = 30 pF, See Figure 1	1	0 20	ns
tPHL	Propagation delay time, high-to-low-level output				1	2 20	
tPLH.	Propagation delay time, low-to-high-level output	Bus	Terminal	C _L = 30 pF, See Figure 2		5 10	ns
tPHL	Propagation delay time, high-to-low-level output					7 14	
tPZH tPHZ tPZL tPLZ	Output enable time to high level Output disable time from high level Output enable time to low level Output disable time from low level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	C _L = 15 pF, See Figure 3		30 20 45 20	ns
tPZH tPHZ tPZL tPLZ	Output enable time to high level Output disable time from high level Output enable time to low level Output disable time from low level	TE, DC, or SC	Terminal	C _L = 15 pF, See Figure 4		20 25 30 25	ns

 $^{^{\}dagger}$ All typical values are at $T_A = 25$ °C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

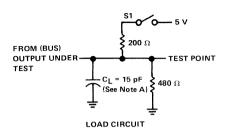
PROPAGATION DELAY TIMES

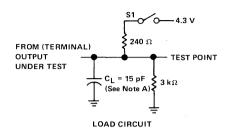
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{Out} = 50 \Omega$.

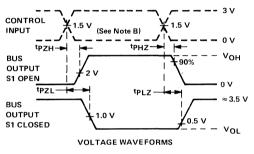
PROPAGATION DELAY TIMES

SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

PARAMETER MEASUREMENT INFORMATION







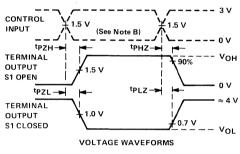


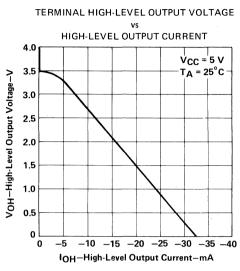
FIGURE 3. BUS ENABLE AND DISABLE TIMES

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. CL includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} = 50 \Omega$.

TYPICAL CHARACTERISTICS



TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs

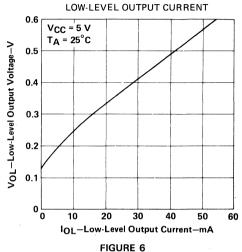


FIGURE 5

TERMINAL OUTPUT VOLTAGE

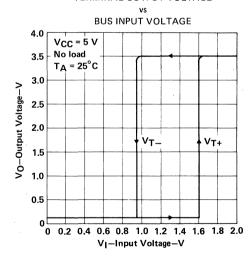
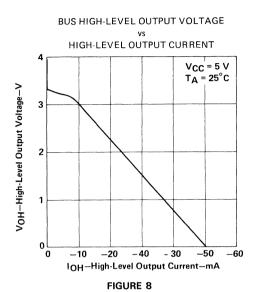
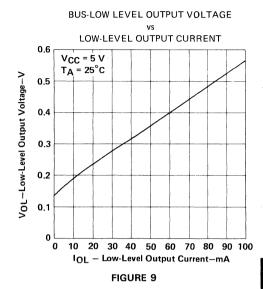


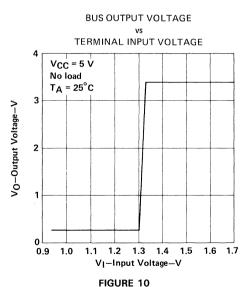
FIGURE 7

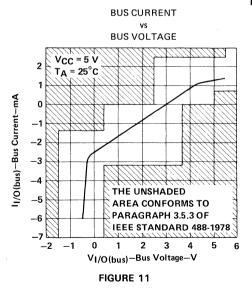
SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

TYPICAL CHARACTERISTICS









nterface ALS Circuits

- 8-Channel Bidirectional Transceivers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- **Open-Collector Driver Output Option**
- No Loading of Bus When Device is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

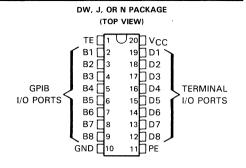
The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, highspeed, Advanced Low-Power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or threestate mode. If Talk Enable (TE) is high, these outputs have the characteristics of opencollector outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 millivolts minimum of quaranteed hysteresis for increased noise immunity.

Output glitches during power-up and powerdown are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$.

The SN75ALS163 is characterized for operation from 0°C to 70°C.

data and other specifications are subject to change

without notice.



FUNCTION TABLES

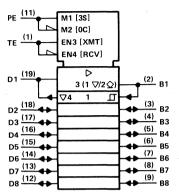
EACH RECEIVER

EACH DRIVER

INPUTS			OUTPUT		NPUT	3	OUTPUT
D TE PE		В	в те		PE	D	
Н	Н	Н	Н	L	L	Х	L
L	Н	Χ	L	Н	L	X	н
ы	Y	1	7	l v	н	Y	7

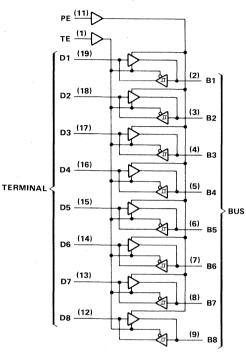
H = high level, L = low level, X = irrelevant, Z = High-impedance state

logic symbol†

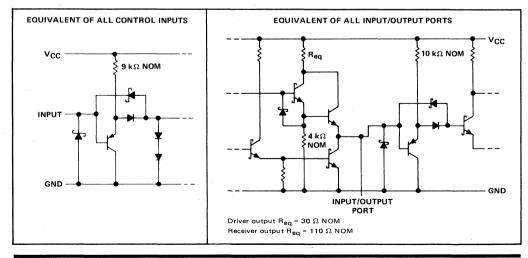


- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ∇ Designates 3-state outputs.
- ◆ Designates open-collector outputs.

logic diagram (positive logic)



schematics of inputs and outputs





abs	solute maximum ratings over operating free-air temperaturë range (unless otherwise noted)	
	Supply voltage, V _{CC} (see Note 1) 7 V Input voltage 5.5 V	
	Low-level driver output current	
	Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):	
	DW package 1125 mW	
	J package	
	N package	
	Operating free-air temperature range	
	Storage temperature range - 65 °C to 150 °C	

NOTES: 1. All voltage values are with respect to network ground terminal.

For operation above 25 °C free-air temperature, derate the DW package to 720 mW at 70 °C at the rate of 9.0 mW/°C, derate
the J package to 880 mW at 70 °C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70 °C at the rate
of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, VIH		2			V
Low-level input voltage, VIL				0.8	V
High level autout avenue I	Bus ports with pullups active			- 10	mA
High-level output current, IOH	Terminal ports			-800	μΑ
Law law law a war a war a law	Bus ports	48 16		48	
Low-level output current, IOL	Terminal ports			16	mA
Operating free-air temperature range, TA		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage		I _I = -18 mA				-0.8	- 1.5	٧
V _{hys}	Hysteresis (V _{T+} - V _{T-}) [‡]	Bus				0.4	0.65		٧
	High level	Terminal	Iон = −	800 μΑ,	TE at 0.8 V	2.7	3.5		V
Vон	output voltage	Bus	IOH = -	10 mA,	PE and TE at 2 V	2.5	3.3		v
1/	Low-level	Terminal	al I _{OL} = 16 mA, TE at 0.8 V				0.3	0.5	V
VOL	output voltage	Bus	I _{OL} = 48	mA,	PE and TE at 2 V		0.35	0.5	v
	High-level output current	Bus	$V_0 = 5.9$	5 V,	PE at 0.8 V,			100	^
Іон	(open-collector mode)	Bus	D and TE at 2 V					100	μΑ
1	Off-state output current	D	PE at 2 V	,	$V_0 = 2.7 \text{ V}$			20	^
loz	(3-state mode)	Bus	TE at 0.8 V		$V_0 = 0.5 V$			- 100	μΑ
ų.	Input current at	Terminal	V _I = 5.5 V				0.2	100	μΑ
'	maximum input voltage	reminai					0.2	100	μΑ
1	High-level	Terminal	V _I = 2.7				0.1	20	^
ΊΗ	input current	PE or TE	V = 2.7	V			0. (20	μΑ
	Low-level	Terminal	V 05				10	- 100	^
ΊL	input current	PE or TE	$V_1 = 0.5$	V			- 10	- 100	μΑ
	Short-circuit	Terminal				- 15	- 35	- 75	
los	output current	Bus				- 25	- 50	- 125	mA
			N- II	Terminal	outputs low and enabled		42	56	
lcc	Supply current	No load Bus outputs low and enabled				52	70	·mA	
C _{i/o(bus)}	Bus-port capacitance		1	$V_{CC} = 5 \text{ V or } 0 \text{ V}, V_{I/O} = 0 \text{ to } 2 \text{ V},$ $f = 1 \text{ MHz}$			30		pF

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

	PARAMETER	FROM	то	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
tPLH	Propagation delay time, PLH low-to-high-level output		,	C ₁ = 30 pF,		10	20	
tPHL	Propagation delay time, high-to-low-level output	Terminal	Bus	See Figure 1		12	20	ns
tPLH	Propagation delay time, low-to-high-level output			C _L = 30 pF,		5	10	
tPHL	Propagation delay time, high-to-low-level output	Bus	Terminal	See Figure 2		7	14	ns
tPZH	Output enable time to high level		Bus			11	20	ns
tPHZ	Output disable time from high level	TE .		$C_L = 15 pF$,		3	10	
tPZL	Output enable time to low level	''-		See Figure 3		18	35	
tpLZ	Output disable time from low level					5	20	
tPZH	Output enable time to high level					5	20	
tPHZ	Output disable time from high level	TE	Terminal	C _L = 15 pF,		8	20	ns
tPZL	Output enable time to low level	1 15	rerminai	See Figure 4		9	20	
tPLZ	Output disable time from low level					8	20	
t _{en}	Output pull-up enable time	PE	Bus	C _L = 15 pF,		3	10	
tdis	Output pull-up disable time	1 5	bus	See Figure 5		4	12	ns

 $^{^{\}dagger}$ All typical values are at T_A = 25 °C.



[‡] Hysteresis is the difference between the positive-going input threshold voltage, V_{T +}, and the negative-going input threshold voltage, V_{T -}.

PARAMETER MEASUREMENT INFORMATION

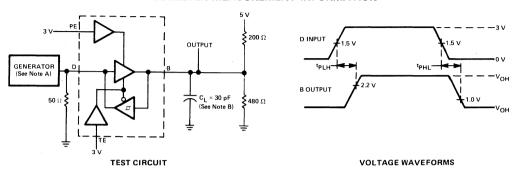


FIGURE 1. TERMINAL TO BUS PROPAGATION DELAY TIMES

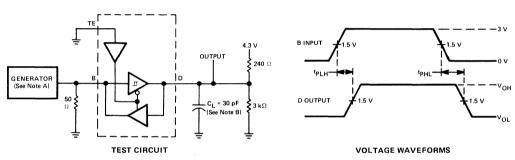


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

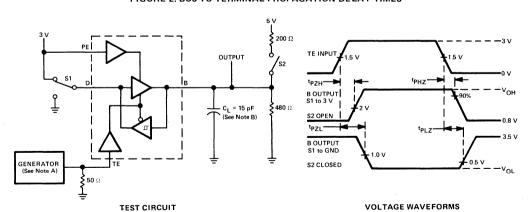


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{OUT} =$ 50 Ω .

B. C_L includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

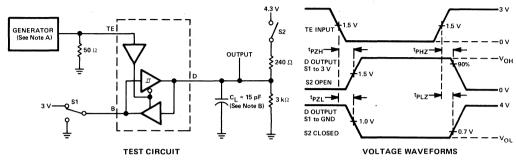


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

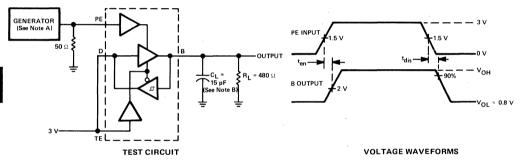
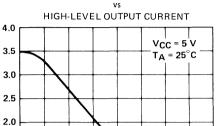


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\rm f} \leq$ 6 ns, $t_f \, \leq \, 6 \, \, \text{ns, Z}_{out} \, = \, 50 \, \, \Omega.$
 - B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS



TERMINAL HIGH-LEVEL OUTPUT VOLTAGE

VOH-High-Level Output Voltage-V 3.5 3.0 2.5 2.0 1.5 1.0 0.5

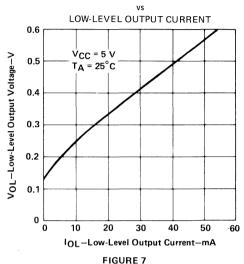
0

0

IOH-High-Level Output Current-mA FIGURE 6

-10 -15 -20 -25 -30 -35 -40

TERMINAL LOW-LEVEL OUTPUT VOLTAGE



TERMINAL OUTPUT VOLTAGE

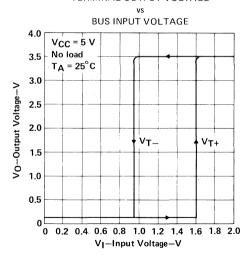
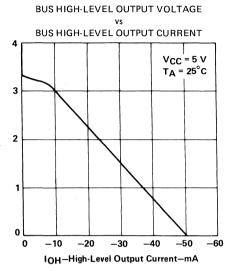


FIGURE 8

VOH-High-Level Output Voltage-V

TYPICAL CHARACTERISTICS



BUS LOW-LEVEL OUTPUT VOLTAGE BUS LOW-LEVEL OUTPUT CURRENT 0.6 Vcc = 5 V TA = 25°C VOL-Low-Level Output Voltage-V 0.5 0.4 0.3 0.2 0.1 0 10 30 40 50 60 70 80 90 100 0 IOI -Low-Level Output Current-mA FIGURE 10

FIGURE 9

BUS OUTPUT VOLTAGE

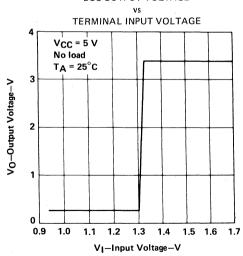


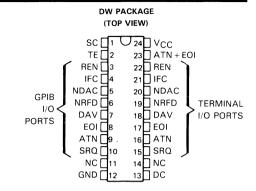
FIGURE 11

- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per
 Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (Vcc = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

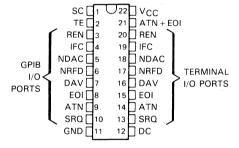
description

The SN75ALS164 eight-channel generalpurpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS164 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS164 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75ALS164 is identical to the SN75ALS162 with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.



N DUAL-IN-LINE PACKAGE (TOP VIEW)



 ${\sf NC-No}$ internal connection.

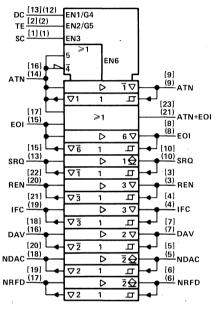
CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	
TE	Talk Enable	Control
sc	System Control	
ATN	Attention	
SRQ	Service Request	Bus
REN	Remote Enable	Management
IFC	Interface Clear	
EOI	End or Identify	
ATN + EOI	ATN logical OR EOI	Logic
DAV	Data Valid	Data
NDAC	Not Data Accepted	Transfer
NRFD	Not Ready for Data	Transier

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage VCC is 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

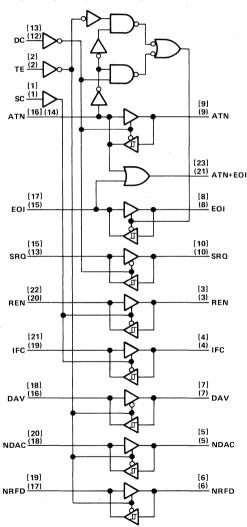
The SN75ALS164 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C.

logic symbol†



- [†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ∇Designates 3-state outputs.
- Designates passive-pullup outputs.

logic diagram (positive logic)



- [] Denotes pin numbers for DW package.
- () Denotes pin numbers for N package.



RECEIVE/TRANSMIT FUNCTION TABLE

	CONT	ROLS		BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS			
sc	DC	TE	ATN†	ATN [†]	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD	
				(Controlle	Controlled by DC) (Co		(Controlled by SC)		(Controlled		/ TE)	
	Н	н	Н	R	т			T	т.	R	J	
	Н	Н	L	l "	<u>'</u>			R	'	n	К	
	L	L	Н	т	R			R	R	т	т	
	L	L	L		n .			T	r.		'	
	Н	L	Х	R	Т			R	R	Т	Т	
	L	Н	Х	Т	R			Т	Т	R	R	
Н						Т	Т					
L						R	R					

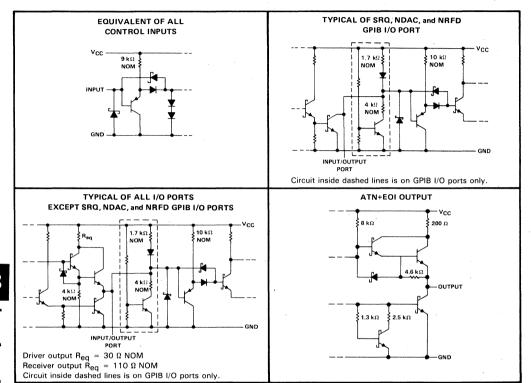
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

ATN + EOI FUNCTION TABLE

INPL	JTS	OUTPUT				
ATN	EOI	ATN + EOI				
Н	Х	Н				
Х	Н	н				
L	L	L				

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†]ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage
Low-level driver output current
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
DW package
N package
Operating free-air temperature range
Storage temperature range65°C to 150°C
Lead temperature 1.6 mm (1/16) inch from the case for 10 seconds: DW or N package 260°C

- NOTES: 1. All voltage values are with respect to network ground terminal.
 - 2. For operation above 25°C free-air temperature, derate the DW package to 864 mW at 70°C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70°C at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, VIH		2			V
Low-level input voltage, VIL				0.8	V
	Bus ports with 3-state outputs			- 5.2	mA
High-level output current, IOH	Terminal ports			- 800	
	ATN + EOI		4.75 5 5.25 2 0.8 -5.2 -800 -400 48	μΑ	
	Bus ports			5.25 0.8 -5.2 -800 -400 48 16 4	
Low-level output current, IOL	Terminal ports			16	mA
	ATN + EOI			4	1
Operating free-air temperature, TA				70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
V _{IK}	Input clamp voltage		I _I = -18 mA			-0.8	- 1.5	V
V _{hys}	Hysteresis (V _{T+} - V _{T-})	Bus			0.4	0.65		V
		Terminal	$I_{OH} = -800 \mu\text{A}$ $I_{OH} = -5.2 \text{mA}$			3.5		
V _{OH} ‡	High-level output voltage	Bus				3.3		V
		ATN + EOI	$I_{OH} = -400 \mu$	1	2.7			
	·	Terminal	I _{OL} = 16 mA			0.3	0.5	
v_{OL}	Low-level output voltage	Bus	I _{OL} = 48 mA			0.35	0.5	V
	·	ATN + EOI	IOL = 4 mA				0.4	
l _l	Input current at	Terminal §	$V_{I} = 5.5 V$			0.2	100	
'1	maximum input voltage	ATN, EOI	$V_{ } = 5.5 V$				200	μΑ
		Terminal	V ₁ = 2.7 V			0.1	20	
lн	High-level input current	control				0.1	20	μΑ
		ATN, EOI	$V_1 = 2.7 V$				40	Ì
		Terminal,	V _I = 0.5 V			_ 10	- 100	
liL.	Low-level input current	control	· ·			- 10	- 100	μΑ
		ATN, EOI	V _I = 0.5 V				- 500	ļ
V _{I/O(bus)}	Voltage at bus port		Driver disabled II(bus) = 0		2.5	3.0	3.7	V
				$I_{l(bus)} = -12 \text{ mA}$			- 1.5	
				$V_{l(bus)} = -1.5 \text{ V to 0.4 V}$	-1.3			
				$V_{l(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$	0		- 3.2	
I _{I/O(bus)}	Current into bus port	Power on	Driver disabled	$V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$			+ 2.5 mA	
1/O(bus/							-3.2	''''
				$V_{I(bus)} = 3.7 \text{ V to 5 V}$	0		2.5	1
				$V_{I(bus)} = 5 \text{ V to } 5.5 \text{ V}$	0.7		2.5	
		Power off	$V_{CC} = 0,$	$V_{I(bus)} = 0 V to 2.5 V$	ļ		-40	μΑ
		Terminal			- 15	- 35	- 75	ĺ
los	Short-circuit output current	Bus	L		- 25	- 50	-125	mA
		ATN + EOI			-10		- 100	
lcc	Supply current		No load,	TE, DC, and SC low		55	75	mA
C _{i/o(bus)}	Bus-port capacitance		$V_{CC} = 5 \text{ V to C}$ $V_{I/O} = 0 \text{ to 2 V}$			30		рF

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies for three-state outputs only.



[§] Except ATN and EOI terminal pins.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

	PARAMETER	FROM	то	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	Terminal	Bus	C _L = 30 pF,		10	20	ns
tPHL	Propagation delay time, high-to-low-level output	Terrima	-	See Figure 1		12	20	
^t PLH	Propagation delay time low-to-high-level output	Bus	Terminal	C _L = 30 pF,		5	10	ns
tPHL	Propagation delay time, high-to-low-level output		Terrima	See Figure 2		7	14	113
^t PLH	Propagation delay time, low-to-high-level output	Terminal ATN or Terminal EOI	ATN + EOI	C _L = 15 pF, See Figure 3		3.5	10	ns
tPHL	Propagation delay time, high-to-low-level output	Terminal ATN or Terminal EOI	ATN + EOI	C _L = 15 pF, See Figure 3		7	15	ns
tPZH	Output enable time to high level	TE, DC,	BUS				30	
tPHZ	Output disable time from high level	or	(ATTN, EOI,	$C_L = 15 pF$,			20	ns
^t PZL ^t PLZ	Output enable time to low level Output disable time from low level	sc	REN, IFC, and DAV)	See Figure 4			45 20	
tPZH tPHZ	Output enable time to high level Output disable time from high level Output enable time to low level	TE, DC,	Terminal	CL = 15 pF,			20 25 30	ns
^t PZL ^t PLZ	Output disable time from low level	SC		See Figure 5			25	

PARAMETER MEASUREMENT INFORMATION 5 V 4.3 V **200** Ω **240** Ω FROM (BUS) FROM (TERMINAL) OUTPUT UNDER-TEST POINT OUTPUT UNDER TEST POINT TEST TEST $C_1 = 30 pF$ C_L = 30 pF **480** Ω (See Note A) (See Note A) LOAD CIRCUIT LOAD CIRCUIT - 3 V TERMINAL BUS 1 5 V INPUT INPUT (See Note B) (See Note B) tPHL-₩ tPLH-₩ tPHL-₩ BUS TERMINAL 2.2 V OUTPUT OUTPUT 1.5 1.0 V VOL ۷он **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS**

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

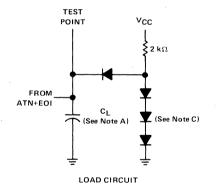


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

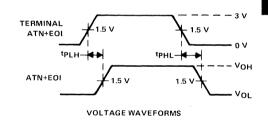


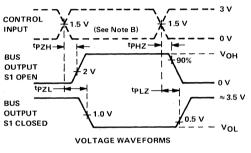
FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \le 6$ ns, $Z_{out} = 50 \Omega$. C. All diodes are 1N916 or 1N3064.



PARAMETER MEASUREMENT INFORMATION **200** Ω **240** Ω FROM (BUS) FROM (TERMINAL) OUTPUT UNDER TEST POINT OUTPUT TEST POINT TEST UNDER TEST C_L = 15 pF C_L = 15 pF **480** Ω $3 k\Omega$ (See Note A (See Note A) LOAD CIRCUIT LOAD CIRCUIT



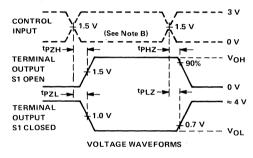
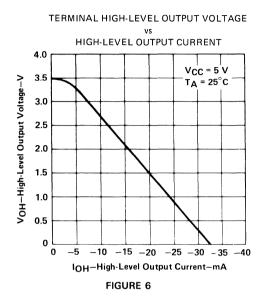


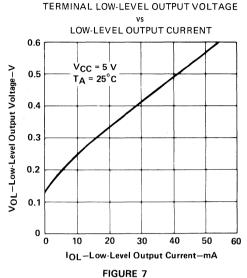
FIGURE 4. BUS ENABLE AND DISABLE TIMES

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. CL includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{Out} =$ 50 Ω .





TERMINAL OUTPUT VOLTAGE

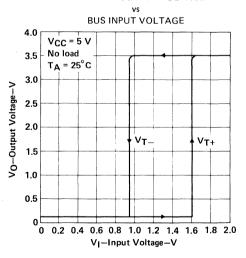
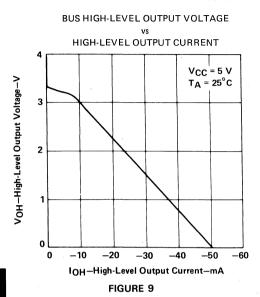
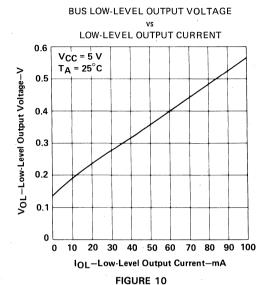
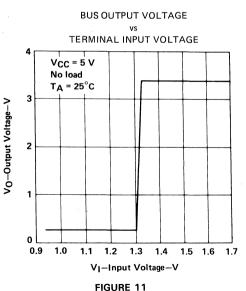
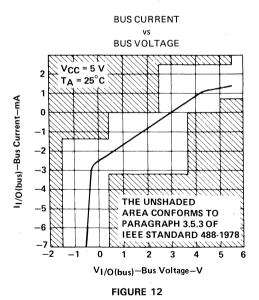


FIGURE 8









MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- No Loading of Bus When Device is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)
- Driver and Receiver Can Be Disabled Simultaneously

description

The SN75ALS165 eight-channel generalpurpose interface bus transceiver is a monolithic. high-speed, Advanced Low-Power Schottky designed for two-way communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. Taking TE and PE low places both the drivers and receivers in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when $V_{CC} = 0$. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS165 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

(TOP VIEW) U20 VCC TE [1 19 D1 B2 ∏3 18 D2 17 D3 B3 🗆 4 BUS В4 ∏5 16 D4 TERMINAL I/O PORTS B5 ∏6 15 D5 I/O PORTS B6 ∏7 14 D6 13 D7 B7 ∏8 12 D8 B8 ∏9 GND 10 11 PE

DW. J. OR N PACKAGE

FUNCTION TABLES

EACH DRIVER

EACH RECEIVER

INPUTS		S	OUTPUT	INPUTS			OUTPUT	
D	TE	PE	В		B TE PE		D	
Н	Н	Н	Н	ſ	L	L	Н	L
L	Н	X	L	Ì	Н	L	н	н
Н	Χ	L	Z [†]	Į	Х	Н	X	Z
Х	L	Х	Z [†]		Χ	Х	L	Z

H = high level, L = low level, X = irrelevant,

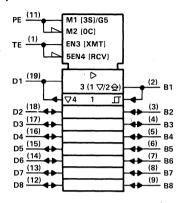
Z = high-impedance state.

[†]This is the high-impedance state of a normal 3-state output modified by the internal resistors to VCC and ground.

nterface ALS Circuits



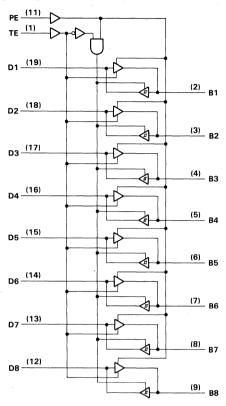
logic symbol†



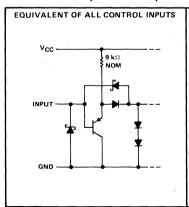
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

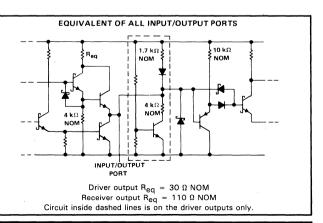
- ∇ Designates 3-state outputs.
- ◆ Designates passive-pullup outputs.

logic diagram (positive logic)



schematics of inputs and outputs





INSTRUMENTS

1125 mW

SN75ALS165 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

Supply voltage, VCC (see Note 1)										 		7 V
Input voltage											 		5.5 V
Low-level driver outpu	t current										 	. 1	100 mA
Continuous total dissip	oation at (or	below)	25°C	free-a	ir temp	eratur	e (se	e No	te 2):			

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

J package
N package
Operating free-air temperature range
Storage temperature range65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package 300°0

NOTES: 1. All voltage values are with respect to network ground terminal.
 For operation above 25°C free-air temperature, derate the DW package to 720 mW at 70°C at the rate of 9.0 mW/°C, derate the J package to 880 mW at 70°C at the rate of 11.0 mW/°C, and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

.

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, VIH		2			V
Low-level input voltage, V _{IL}				0.8	V
	Bus ports with pullups active			- 5.2	mA
High-level output current, IOH	Terminal ports			0.8	μΑ
I am land a dank a man I a	Bus ports			48	mΑ
High-level output current, IOH Bus ports with pullups active Terminal ports Bus ports Bus ports Terminal ports Terminal ports			16	1112	
Operating free-air temperature, TA		0		70	°C



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER			TES1	CONDITIONS	MIN	TYP [†]	MAX	UNIT	
V _{IK}	Input clamp voltage		$I_{\parallel} = -18 \text{ mA}$			-0.8	- 1.5	V		
V_{hys}	Hysteresis (V _{T+} - V _{T-})	Bus				0.4	0.65		v	
VoH [‡]	High-level	Terminal	$I_{OH} = -800$		TE at 0.8 V	2.7	3.5		V	
VOH	output voltage	Bus	$I_{OH} = -5.2$	mA,	PE and TE at 2 V	2.5	3.3		L	
VOL	Low-level	Terminal	I _{OL} = 16 m		TE at 0.8 V		0.3	0.5	V	
VOL	output voltage	Bus	IOL = 48 m.	A,	TE at 2 V		0.35	0.5	_ `	
l _l	Input current at maximum input voltage	Terminal	V _I = 5.5 V				0.2	100	μΑ	
ΊΗ	High-level input current	Terminal and	V _I = 2.7 V		,		0.1	20	μΑ	
hL.	Low-level input current	control inputs	V ₁ = 0.5 V			- 10	- 100	μΑ		
V	/ - Valtage at less and		Driver disabled II(bus) = 0		2.5	3.0	3.7	V		
V _{I/O(bus)}	Voltage at bus port		Driver disabil	eu	$I_{I(bus)} = -12 \text{ mA}$			- 1.5		
					$V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$	-1.3				
					$V_{l(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$	0		- 3.2	ſ	
					$V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$			+2.5	l	
I _I /O(bus)	Current into bus port	Power on	Driver disable	ed				-3.2	mA	
					$V_{I(bus)} = 3.7 \text{ V to 5 V}$	0		2.5		
					V _{I(bus)} = 5 V to 5.5 V	0.7		2.5		
		Power off	$V_{CC} = 0$,		$V_{l(bus)} = 0 V to 2.5 V$			- 40	μА	
los	Short-circuit	Terminal				- 15	- 35	- 75	_{mA}	
-03	output current	Bus				- 25	- 50	- 125		
lcc	Supply current		No load		ninal outputs low and enabled		42	56	mA	
					outputs low and enabled		52	70		
C _{i/o(bus)}	Bus-port capacitance		$V_{CC} = 5 V$ f = 1 MHz	to 0 V	V , $V_{I/O} = 0$ to 2 V,		30		pF	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies for three-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 V$

	PARAMETER	FROM	то	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
tPLH	Propagation delay time,					10	20	
YFLH	low-to-high-level output	Terminal	Bus	$C_L = 30 pF$,				ns
tPHL	Propagation delay time,	Terrinital	Dus .	See Figure 1		12	20	113
YPHL	high-to-low-level output						20	
tou	Propagation delay time,				,	5	10	
tPLH	low-to-high-level output	Bus	Terminal	$C_L = 30 pF$,				ns
tou	Propagation delay time,	bus	1 eminar	See Figure 2		7	14	115
^t PHL	high-to-low-level output							
tPZH	Output enable time to high level	TE Bus				11	20	
tPHZ	Output disable time from high level		$C_L = 15 pF$,		3	10	ns	
tPZL	Output enable time to low level	112	- Bus	See Figure 3		18	35	1 1
tPLZ	Output disable time from low level					5	20	
^t PZH	Output enable time to high level					5	20	
tPHZ	Output disable time from high level	TE	Terminal	$C_L = 15 pF$,		8	20	ns
tPZL	Output enable time to low level	1 -	Terrinia	See Figure 4		9	20	
^t PLZ	Output disable time from low level					8	20	
t _{en}	Output pull-up enable time	PE	Terminal	$C_L = 15 pF$,		3	10	ns
^t dis	Output pull-up disable time	1 E	Terrinia	See Figure 5		4	12	115

 $^{^{\}dagger}AII$ typical values are at TA = 25 °C.

TEST CIRCUIT

GENERATOR (See Note A) OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT TE OUTPUT OUTPUT OUTPUT Tell

PARAMETER MEASUREMENT INFORMATION

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS

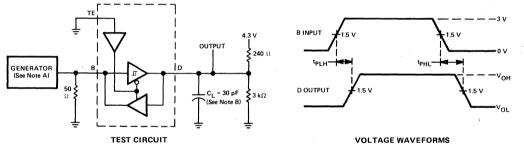


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

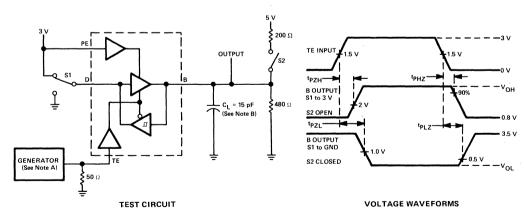


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} = 50 \Omega$.

B. C_L includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

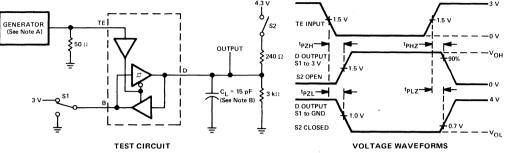


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

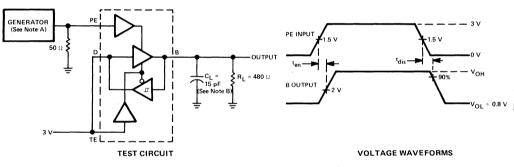
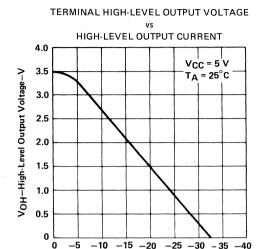


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\text{f}} \leq$ 6 ns, $t_{\text{f}} \leq$ 6 ns, $t_{\text{Out}} = 50~\Omega$.
 - B. C_I includes probe and jig capacitance.

0

TYPICAL CHARACTERISTICS



TERMINAL LOW-LEVEL OUTPUT VOLTAGE

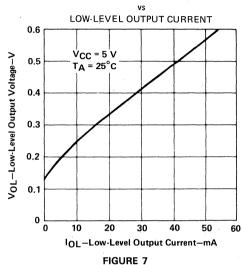
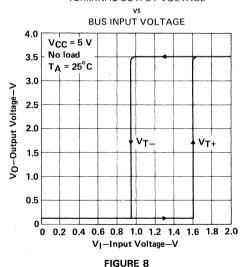


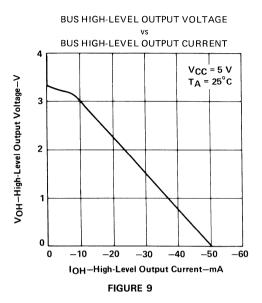
FIGURE 6

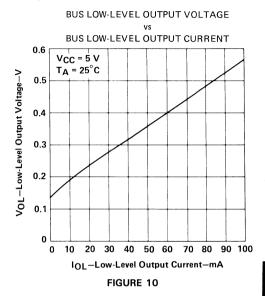
IOH-High-Level Output Current-mA

TERMINAL OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS





BUS OUTPUT VOLTAGE TERMINAL INPUT VOLTAGE VCC = 5 V No load T_A = 25°C 3 Vo-Output Voltage-V 2 1 0 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 V_I-Input Voltage-V

FIGURE 11

SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVERS

D2904, JULY 1985

- Meets EIA Standard RS-422-A
- High-Speed, Low-Power ALS Design
- 3-State TTL Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Complementary Output Enable Inputs
- Improved Replacement for the AM26LS31

description

This quadruple complementary-output line driver is designed for data transmission over twistedpair or parallel-wire transmission lines. It meets the requirements of EIA Standard RS-422-A and is compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 milliamperes, while typical propagation delay time is less than 10 nanoseconds.

SN75ALS192 . . . D, J, N DUAL-IN-LINE PACKAGE (TOP VIEW)

	_		
1 A 🗌	1	U ₁₆]vcc
1Y 🗌	2	15]4A
1Z 🗀	3	14]4Y
ENABLE G	4	13] 4Z
2Z 🗌	5	12] ENABLE G
2A 🗌	6	11] 3Z
1 A 🗌	7	10]3Y
GND 🗌	8	9]3A

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUT	PUTS
Α	G	G	Y	Z
Н	Н	X	Н	L
L	Н	Χ	L	Н
Н	×	L	н	L
L	×	L	L	Н
X	L	Н	Z	Z

H = high level, L = low level,

Z = high impedance (off),

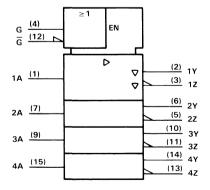
X = irrelevant

High-impedance inputs maintain input currents low, less than 1 microampere for a high level and less than 100 microamperes for a low level. Complementary control inputs, G and \overline{G} , allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver.

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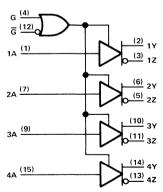
The SN75ALS192 is characterized for operation from 0°C to 70°C.

logic symbol†



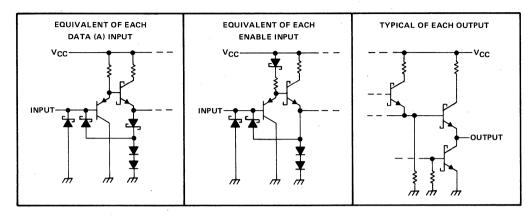
 $^{^\}dagger This$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage, V _I
Output off-state voltage
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):
D package
J package
N package
Operating free-air temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300 °C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C

- NOTES: 1. All voltage values except differential output voltage VOD are with respect to network ground terminal.
 - For operation above 25 °C free-air temperature, refer to the Dissipation Derating Table. In the J package, SN75ALS192 chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	T _A = 25°C	DERATING	ABOVE	T _A = 70°
FACRAGE	POWER RATING	FACTOR	T_{A}	POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW
J (Glass mount)	1000 mW	8.2 mW/°C	28°C	656 mW
N	875 mW	7.0 mW/°C	25 °C	560 mW

SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVERS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, VCC	4.75	5	5.25	٧
High-level input voltage, V _{IH}	2			V
Low-level input voltage, V _{IL}			0.8	V
High-level output current, IOH			- 20	mA
Low-level output current, IOL			20	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

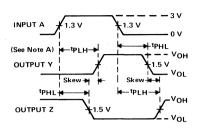
	PARAMETER	TEST CONDITIONS	MIN	TYP† N	ИАХ	UNIT
VIK	Input clamp voltage	$V_{CC} = 4.75 \text{ V}, \text{ I}_{I} = -18 \text{ mA}$		_	- 1.5	V
Vон	High-level output voltage	$V_{CC} = 4.75 \text{ V}, I_{OH} = -20 \text{ mA}$	2.5			V
VOL	Low-level output voltage	$V_{CC} = 4.75 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
	Off-state (high-impedance state) output current	$V_{CC} = 5.25 \text{ V} \frac{V_0 = 0.5 \text{ V}}{V_0 = 2.5 \text{ V}}$		-	- 20	
loz	On-state (nigh-impedance state) output current	$VCC = 5.25 \text{ V}$ $V_0 = 2.5 \text{ V}$			20	μΑ
Ц	Input current at maximum input voltage	V _{CC} = 5.25 V, V _I = 7 V			0.1	mA
ΊΗ	High-level input current	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 2.7 \text{ V}$			20	μΑ
IIL	Low-level input current	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 0.4 \text{ V}$			0.2	mA
los	Short-circuit output current [‡]	V _{CC} = 5.25 V	- 30	_	150	mA
Icc	Supply current (all drivers)	V _{CC} = 5.25 V, All outputs disabled		26	45	mA

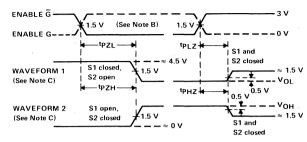
switching characteristics, VCC = 5 V, TA = 25 °C (see Figure 1)

	PARAMETER TEST CONDITIONS		MIN	TYP	MAX	UNIT	
tPLH	Propagation delay time, low-to-high-level output				6	13	ns
^t PHL	Propagation delay time, high-to-low-level output	$C_L = 30 pF,$	S1 and S2 open		9	14	ns
	Output-to-output skew				3	6	ns
^t PZH	Output enable time to high level	$R_L = 75 \Omega$			11	15	ns
tPZL	Output enable time to low level	$R_L = 180 \Omega$			16	20	ns
^t PHZ	Output disable time from high level	C _L = 10 pF,	S1 and S2 closed		8	15	ns
^t PLZ	Output disable time from low level				18	20	ns

 $^{^{\}dagger}All$ typical values are at VCC = 5 V, TA = 25 °C. $^{\ddagger}Not$ more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

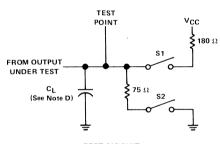




PROPAGATION DELAY TIMES AND SKEW

ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



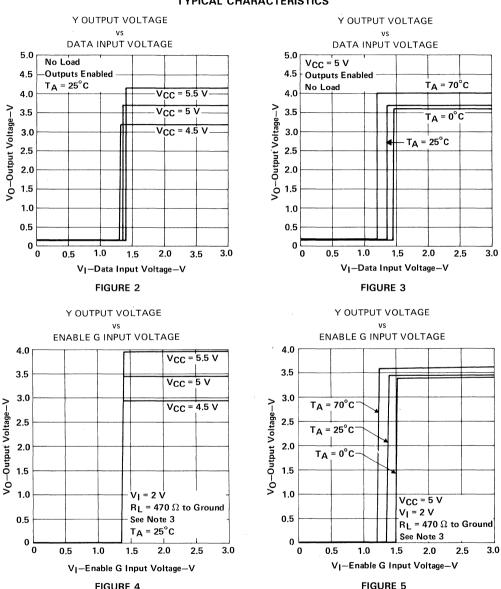
TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.

- B. Each enable is tested separately.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the enable inputs.

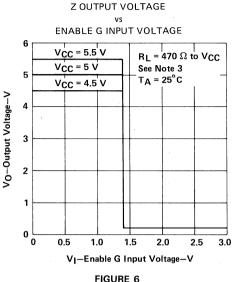
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the enable inputs.
 - D. C_L includes probe and jig capacitance.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{out} \approx 50 \Omega$, $t_r \leq 15$ ns, and $t_f \leq 6$ ns.

FIGURE 1. SWITCHING TIMES



NOTE 3: The A input is connected to VCC during the testing of the Y outputs and to ground during the testing of the Z outputs.

FIGURE 4



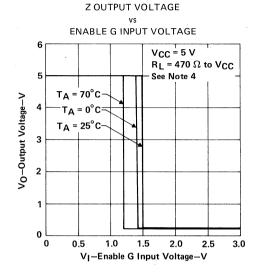


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

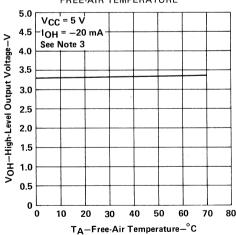


FIGURE 7



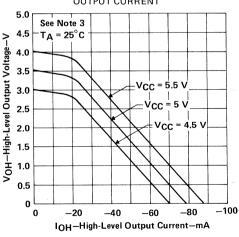
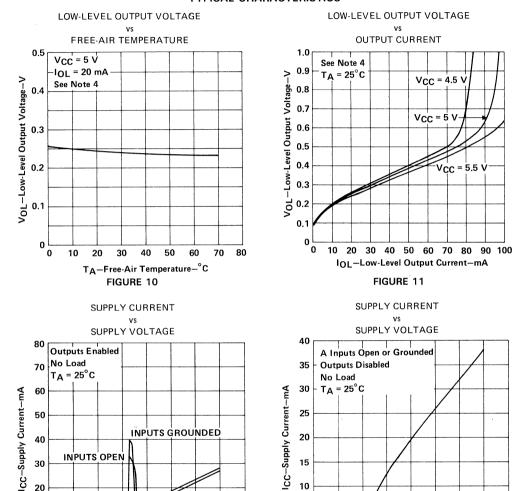


FIGURE 8

FIGURE 9

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.



INPUTS OPEN

FIGURE 12

V_{CC}-Supply Voltage-V

NOTES: 3. The A input is connected to VCC during the testing of the Y outputs and to ground during the testing of the Z outputs. 4. The A input is connected to ground during the testing of the Y outputs and to VCC during the testing of the Z outputs.

 VCC-Supply Voltage-V FIGURE 13

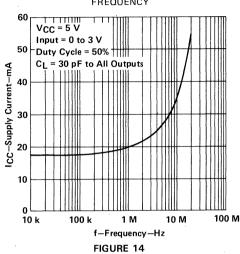


Interface ALS Circuits

TYPICAL CHARACTERISTICS

SUPPLY CURRENT





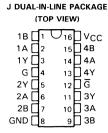
- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . - 7 V to 7 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low ICC Requirements:
 ICC . . . 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A

description

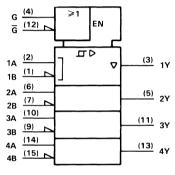
The SN75ALS193 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A, RS-423-A, and RS-485. It features three-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are

The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of $\pm\,200$ millivolts over a common-mode input voltage range of $-\,7$ to 7 volts. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS193 is characterized for operation from 0° C to 70° C.

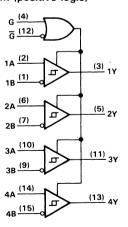


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL	ENA	BLES	OUTPUT
A∸B	G	G	Υ
V:- > 0.2 V	Н	Х	Н
V _{ID} ≥ 0.2 V	X	L	н
0.2.1/ 0.2.1/	Н	Х	?
$-0.2 \text{ V} < \text{V}_{1D} < 0.2 \text{ V}$	х	L	?
V 02V	Н	Х	L
$V_{ID} \leq -0.2 V$	Х	L	L
X	L	Н	Z

H = high level

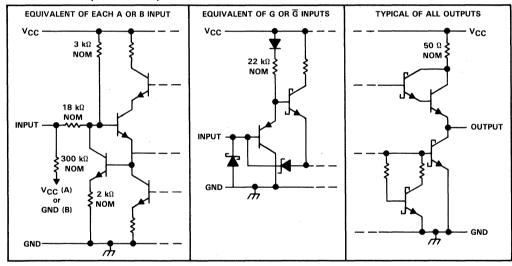
L = low level

X = irrelevant

? = indeterminate

Z = high-impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)
Input voltage, A or B inputs
Differential input voltage (see Note 2)
Enable input voltage
Low-level output current
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3) 1025 mW
Operating free-air temperature range
Storage temperature range65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 - 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
 - For operation above 25°C free-air temperature, derate to 656 mW at 70°C at the rate of 8.2 mW/°C. In the J package, SN75ALS193 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.75	5	5.25	V
Common-mode input voltage, V _{IC}			± 7	V
Differential input voltage, V _{ID}			± 12	V
High-level input voltage, VIH	2			V
Low-level input voltage, V _{IL}			0.8	V
High-level output current, IOH			- 400	μΑ
Low-level output current, I _{OL}			16	mA
Operating free-air temperature, TA	0		70	°C



electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	MIN	TYP [†]	MAX	UNIT	
V _{T+}	Positive-going threshold voltage		1			200	mV	
V _T –	Negative-going threshold voltage			- 200 [‡]			mV	
V _{hys}	Hysteresis §				120		mV	
VIK	Enable-input clamp voltage	I _I = -18 mA				-1.5	V	
VOH	High-level output voltage	V _{ID} = 200 mV,	$I_{OH} = -400 \mu A$	2.7	3.6		V	
Vol	Low-level output voltage	V _{ID} = -200 mV	I _{OL} = 8 mA			0.45	V	
VOL	Low-level output voltage	VID = -200 IIIV	I _{OL} = 16 mA			0.5		
loz	High-impedance-state output current	V _{CC} = 5.25 V	$V_0 = 2.4 \text{ V}$			20	μΑ	
102			$V_0 = 0.4 V$			- 20		
l _l	Line input current	Other input at 0 V,	V _I = 15 V		0.7	1.2	mA	
''		See Note 4	$V_{I} = -15 \text{ V}$		-1.0	-1.7	11114	
ΊΗ	High-level enable-input current		V _{IH} = 2.7 V			20	μА	
чн	riigh-level enable-input current		$V_{IH} = 5.25 V$			100	μΑ	
Ι _Ι L	Low-level enable-input current	$V_{IL} = 0.4 V$				- 100	μΑ	
	Input resistance			12	18		kΩ	
laa	Short-circuit output current	$V_{ID} = 3 V$,	$V_0 = 0$,	- 15	70	- 130	mA	
los		See Note 5			- 78	- 130	mA	
Icc	Supply current	Outputs disabled			22	35	mA	

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	TEST CONDITIONS		TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V, } C_L = 15 \text{ pF,}$		15	22	ns
tPHL	Propagation delay time, high-to-low-level output	See Figure 2		15	22	ns
tPZH	Output enable time to high level	C _I = 15 pF, See Figure 3		13	25	ns
tPZL	Output enable time to low level	C[= 15 pi, See Figure 5		11	25	115
tPHZ	Output disable time from high level	C _I = 15 pF, See Figure 3		13	25	ns
tPLZ	Output disable time from low level	CL = 15 pr, See Figure 5		15	22	115



[†] The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

^{5.} Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

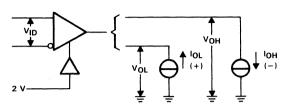
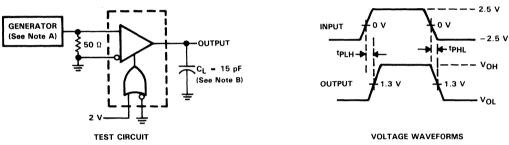


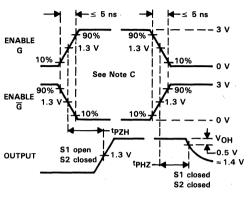
FIGURE 1. VOH, VOL

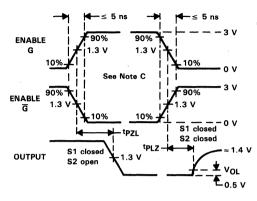


- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{OUT} = 0.00$ 50 Ω , $t_r \leq 6$ ns, $t_f \leq 6$ ns.
 - B. CL includes probe and jig capacitance.

FIGURE 2. tpLH, tpHL

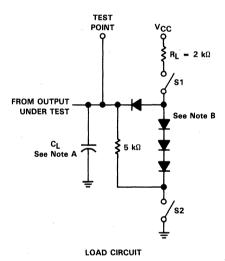
PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS FOR tPHZ, tPZH

VOLTAGE WAVEFORMS FOR tPLZ, tPZL



NOTES: A. $C_{\mbox{\scriptsize L}}$ includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Enable G is tested with \overline{G} high; \overline{G} is tested with G low.

FIGURE 3. tPHZ, tPZH, tPLZ, tPZL

D2917, OCTOBER 1985

- Meets EIA Standard RS-422-A
- High-Speed ALS Design
- 3-State TTL-Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Two Pairs of Drivers Independently Enabled
- Designed as a Replacement for the MC3487 with Improvements: ICC 50% Lower, Switching Speed 30% Faster

description

This quadruple complementary-output line driver is designed for data transmission over twistedpair or parallel-wire transmission lines. It meets the requirements of EIA Standard RS-422-A and is compatible with 3-state TTL circuits. D. J. OR N DUAL-IN-LINE PACKAGE (TOD) ((E)40)

(TOP VIEW)									
1A	II.	U ₁₆	□vcc						
1 Y	\square^2	15] 4A						
1Z	□3	14] 4Y						
1,2EN	□4	13] 4Z						
2Z	□5	12] 3,4EN						
2Y	□6	11] 3Z						
2A	□ 7	10] 3Y						
GND	□ 8	9] 3A						

FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT	OUTPUTS				
INFO	ENABLE	Y	Z			
Н	Н	Н	L			
Ł	н	L	н			
X	L	High-Impedance	High-Impedance			

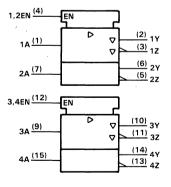
H = TTL high level, L = TTL low level, X = irrelevant

Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 milliamperes, while typical propagation delay time is less than 10 nanoseconds and enable/disable times are typically less than 16 nanoseconds.

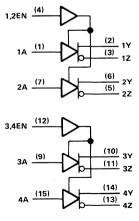
High-impedance inputs keep input currents low, less than 1 microampere for a high level and less than 100 microamperes for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN75ALS194 is capable of data rates in excess of 10 megabits per second and is designed to operate with the SN75ALS195 quadruple line receiver.

The SN75ALS194 is characterized for operation from 0°C to 70°C.

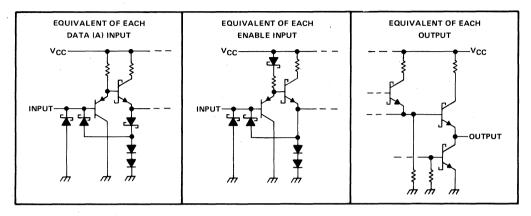
logic symbol



logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	
Input voltage, V _I	
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):	
D package	
J package	
N package	
Operating free-air temperature range	
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C	
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package	

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	T _A = 25°C	DERATING	ABOVE	T _A = 70°C
1 AORAGE	POWER RATING	FACTOR	TA	POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW
J (Glass mount)	1025 mW	8.2 mW/°C	25 °C	656 mW
N	875 mW	7.0 mW/°C	25°C	560 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.75	5	5.25	V
High-level input voltage, V _{IH}	2			V
Low-level input voltage, V _{IL}			0.8	V
High-level output current, IOH			- 20	mA
Low-level output current, IOL			48	mA
Operating free-air temperature, T _A	0		70	°C



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
VIK	Input clamp voltage	I _I = -18 mA				- 1.5	V
Voн	High-level output voltage	I _{OH} = -20 mA		2.5			V
VOL	Low-level output voltage	I _{OL} = 48 mA				0.5	V
VO	Output voltage	10 = 0		0		6	V
V _{OD1}	Differential output voltage	10 = 0		2		6	V
V _{OD2}	Differential output voltage	<u> </u>		½ V _{OD}	1		V
Δ V _{OD}	Change in magnitude of differential output voltage [‡]	$R_L = 100 \Omega$, S	See Figure 1			±0.4	V
Voc	Common-mode output voltage					± 3	V
Δ V _{OC}	Change in magnitude of common-mode output voltage [‡]					±0.4	٧
10	Output current with power off	V _{CC} = 0	$V_0 = 6 V$ $V_0 = -0.25 V$			100 - 100	μΑ
loz	High-impedance state output current	Output enables at 0.8 V	$V_0 = 2.7 \text{ V}$ $V_0 = 0.5 \text{ V}$			100 - 100	μΑ
l _l	Input current at maximum input voltage	V _I = 5.5 V				100	μА
I _{IH}	High-level input current	V ₁ = 2.7 V				50	μА
1 _{IL}	Low-level input current	V _I = 0.5 V				- 200	μA
los	Short-circuit output current §	V _I = 2 V		-40		-140	mA
Icc	Supply current (all drivers)	$V_{CC} = 5.25 \text{ V},$	All outputs disabled		26	45	mA

switching characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	TEST CONDTIONS		MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output				6	13	ns
tPHL	Propagation delay time, high-to-low-level output	C _L = 15 pF, S	0 15 5 0 5	9	14	ns	
	Output-to-output skew		See Figure 1		3.5	6	ns
tTD	Differential-output transition time	$C_L = 15 pF$,	See Figure 2		8	14	ns
tPZH	Output enable time to high level				9	12	ns
tPZL	Output enable time to low level	C _L = 15 pF, Se	See Figure 3		12	20	ns
tPHZ	Output disable time from high level		See Figure 3		9	14	ns
tPLZ	Output disable time from low level				12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A
v _o	V _{oa} , V _{ob}
VOD1	V _o
V _{OD2}	$V_t (R_L = 100 \Omega)$
Δ V _{OD}	$ V_t - \overline{V}_t $
Voc	V _{os}
Δ V _{OC}	V _{os} − V̄ _{os}
los	I _{sa} , I _{sb}
ю	I _{xa} , I _{xb}

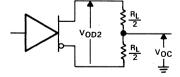


FIGURE 1. DRIVER VOD AND VOC



[†] All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ Δ |V_{OD}| and Δ |V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

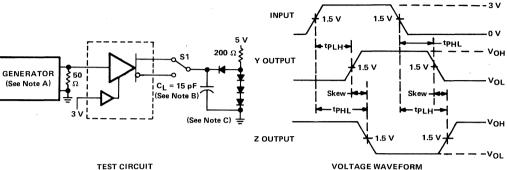


FIGURE 2. PROPAGATION DELAY TIMES

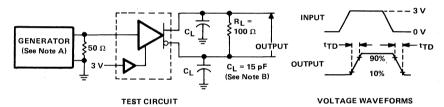
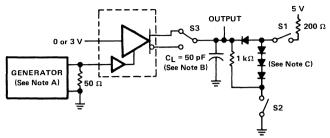


FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_0 = 50$ Ω .

- B. C_L includes probe and stray capacitance.
- C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



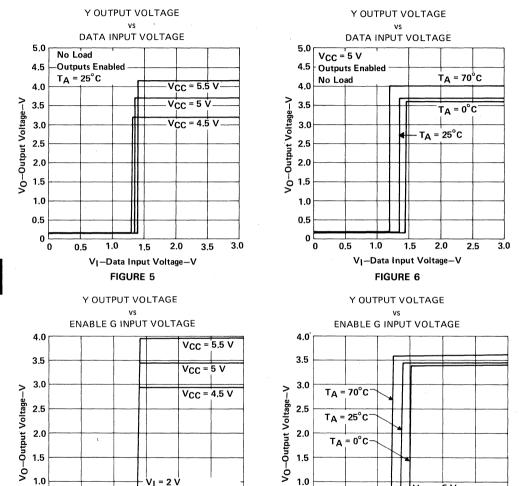
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_{\text{f}} \leq 5$ ns, $t_{\text{f}} \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_{\text{O}} = 50$ Ω .
 - B. C_L includes probe and stray capacitance.
 - C. All diodes are 1N916 or 1N3064.

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES



TYPICAL CHARACTERISTICS



NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

3,0

0.5

0

0

0.5

1.0

 $R_L = 470 \Omega$ to Ground

2.5

See Note 3

 $T_A = 25^{\circ}C$

2.0

1.5

V_I-Enable G Input Voltage-V FIGURE 7

V_{CC} = 5 V

See Note 3

2.0

 $R_L = 470 \Omega$ to Ground

2.5

3.0

V_I = 2 V

1.5

V_I-Enable G Input Voltage-V

FIGURE 8



0.5

0

ō

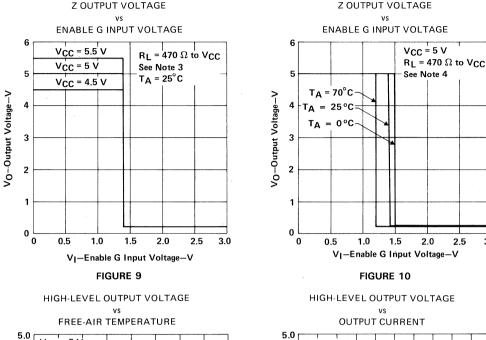
0.5

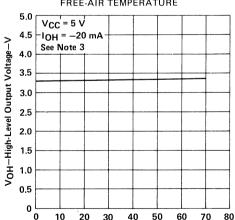
1.0

2.5

3.0

TYPICAL CHARACTERISTICS





TA-Free-Air Temperature-°C FIGURE 11

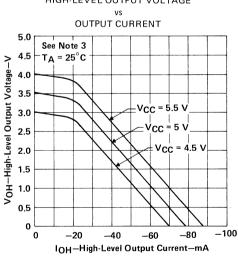


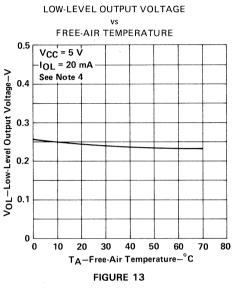
FIGURE 12

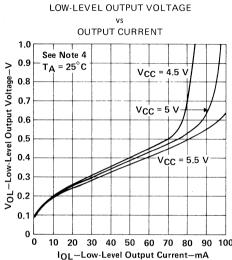
NOTES: 3. The A input is connected to VCC during the testing of the Y outputs and to ground during the testing of the Z outputs.

4. The A input is connected to ground during the testing of the Y outputs and to VCC during the testing of the Z outputs.



TYPICAL CHARACTERISTICS





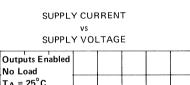
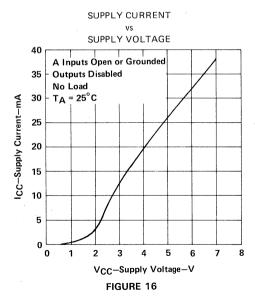
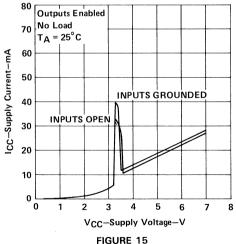


FIGURE 14





NOTE 4: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.



TYPICAL CHARACTERISTICS

SUPPLY CURRENT



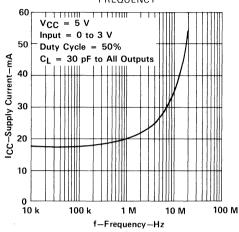


FIGURE 17

and RS-485

Meets EIA Standards RS-422-A, RS-423-A,

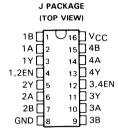
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- 7 V to 7 V Common-Mode Range with 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 k Ω Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement . . . 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

description

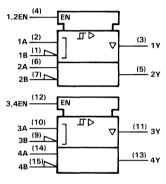
The SN75ALS195 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. provides combined technology improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A, RS-423-A and RS-485.

The SN75ALS195 features three-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 millivolts over a common-mode input voltage range of ± 7 volts. It also features an active-high enable function for each of two receiver pairs. The SN75ALS195 is designed for optimum performance when used with the SN75ALS194 quadruple differential line driver.

The SN75ALS195 is characterized for operation from 0°C to 70°C.

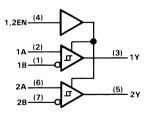


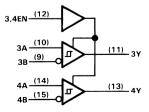
logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram





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QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL	ENA	BLES	OUTPUT
A-B	G	G	Υ
V- > 0.2 V	Н	Х	Н
V _{ID} ≥ 0.2 V	Х	L	н
0.2.1/ - 1/1 0.2.1/	Н	Х	?
$-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$	Х	L	?
V 02V	Н	Х	L
$V_{ID} \leq -0.2 V$	Х	L	· · L
X	L	Н	Z

H = high level

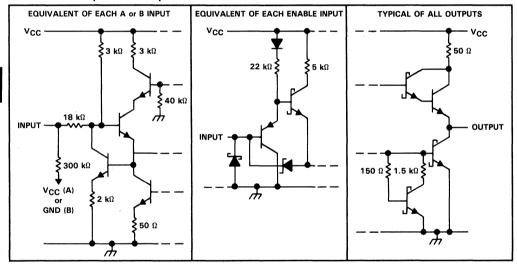
= low level

irrelevant

= indeterminate

Z = high-impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage, A or B inputs, V _I
Differential input voltage (see Note 2)
Enable input voltage
Low-level output current
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3) 1025 mW
Operating free-air temperature range
Storage temperature range
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 - 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
 - 3. For operating above 25 °C free-air temperature, derate the J package to to 656 mW at 70 °C at the rate of 8.2 mW/°C. In the J package, SN75ALS195 chips are glass mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.75	5	5.25	V
Common-mode input voltage, V _{IC}			± 7	V
Differential input voltage, V _{ID}			±12	V
High-level input voltage, VIH	2			V
Low-level input voltage, V _{IL}			0.8	V
High-level output current, IOH			-400	μΑ
Low-level output current, IOL			16	mA
Operating free-air temperature, TA	0		70	°C



electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST COM	NDITIONS	MiN	TYP [†]	MAX	UNIT	
V _{T+}	Positive-going threshold voltage					200	mV	
V _T _	Negative-going threshold voltage			- 200 [‡]			mV	
V _{hys}	Hysteresis §				120		mV	
VIK	Enable-input clamp voltage	I _I = -18 mA				- 1.5	V	
VOH	High-level output voltage	$V_{ID} = 200 \text{ mV},$	$I_{OH} = -400 \mu A$	2.7	3.6		V	
VOL	Low-level output voltage	$V_{1D} = -200 \text{ mV}$	IOL = 8 mA			0.45	V	
VOL	25W level output voltage	VID = 200 IIIV	I _{OL} ≈ 16 mA			0.5		
	High-impedance state output current	V _{IL} = 0.8 V,	$V_{ID} = -3 V$			20		
loz		$V_0 = 2.7 \text{ V}$					μΑ	
,02		$V_{IL} = 0.8 V,$	$V_{ID} = 3 V$,	1		- 20	μ., .	
		$V_0 = 0.5 V$						
1	Line input current	Other input at 0 V,	V _I = 15 V		0.7	1.2	mA	
''	zine inpat derrent	See Note 4	$V_{I} = -15 \text{ V}$		-1.0	- 1.7		
Ιн	High-level enable-input current	High-level enable-input current		$V_{IH} = 2.7 V$			20	μΑ
אוי	riigii-level eliable-liiput current		$V_{IH} = 5.25 \text{ V}$			100	μ.	
ΙΙL	Low-level enable-input current	V _{IL} = 0.4 V				- 100	μΑ	
	Input resistance			12	18		kΩ	
loo	Short-circuit output current	V _{ID} = 3 V,	V _O = 0,	_ 15	- 78	120	mA	
los		See Note 5		-15	- 76	- 130	IIIA	
Icc	Supply current	Outputs disabled			22	35	mA	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \, ^{\circ}\text{C}$.

- NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.
- 5. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

l	PARAMETER	TEST CONDITIONS	N	IIN TY	MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V, } C_L = 15$	pF,	15	22	ns
^t PHL	Propagation delay time, high-to-low-level output	See Figure 2		15	22	ns
tPZH	Output enable time to high level	C _I = 15 pF, See Figure	. 3	13	25	ns
tPZL	Output enable time to low level	CL = 13 bi , See Figure		11	25	113
^t PHZ	Output disable time from high level	C _I = 15 pF, See Figure	. 3	13	25	ns
tPLZ	Output disable time from low level	C _L = 15 μr, See rigure	. 3	1 5	22	113

[‡] The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only. § Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage,

PARAMETER MEASUREMENT INFORMATION

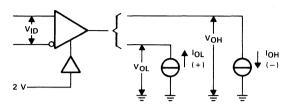
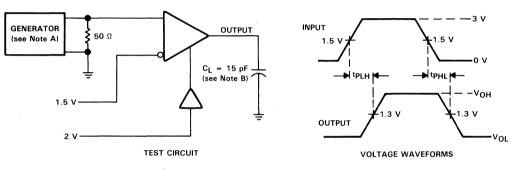
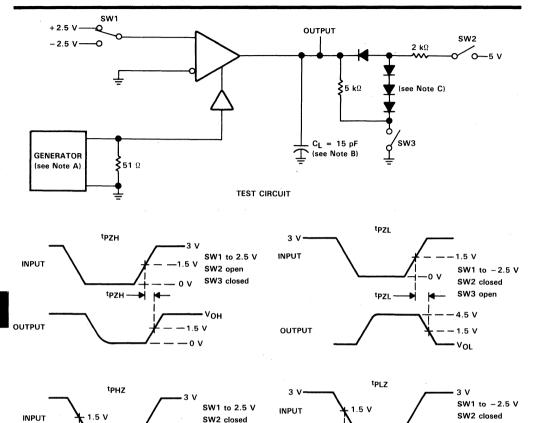


FIGURE 1. VOH, VOL



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{OUT} = 50 Ω , $t_f \leq$ 6 ns. $t_f \leq$ 6 ns.
 - B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS

tPLZ-

0.5 V

OUTPUT

SW3 closed

۷он

SW3 closed

VOL

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} = 50 \Omega_r t_f \leq 6 \text{ ns. } t_f \leq 6 \text{ ns.}$
 - B. C_L includes probe and jig capacitance.

0.5 V

OUTPUT

C. All diodes are 1N3064 or equivalent.

FIGURE 3. ENABLE AND DISABLE TIMES



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Advanced Schottky Family



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Advanced Schottky Family (ALS/AS) Application

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INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high preformance state-of-theart designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower that the 54S/74S series but had a much lower power consumption.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table 1 provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

- TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
- 2. Suppresses the effects of line ringing and significantly reduces undershoot
- 3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
- 4. Input current requirement reduced by up to 50%

^{*}Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

MINIMIZING POWER MINIMIZING DELAY TIME PROP PWR SPD/PWR MAXIMUM PROP PWR SPD/PWR MAXIMUM DISS CIRCUIT TECHNOLOGY PRODUCT FLIP-FLOP FREO FAMILY DELAY DISS **PRODUCT** FLIP-FLOP FREQ FAMILY DELAY (mW) (ns) (mW) (La) (MHz) (ns) (pJ) (MHz) 100 35 TTI 10 10 100 35 TTL 10 10 Gold Doped L TTL 33 1 33 3 H TTL 6 22 132 50 LS TTL 2 S TTL 3 19 125 9 18 45 57 Schottky Clamped 'ALS 4 1.2 4.8 70 'AS 1.7 8 13.6 200

Table 1. Typical Performance Characteristics by TTL Series

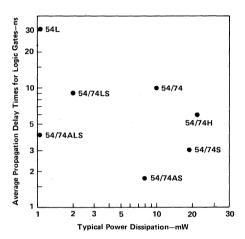


Figure 1. Speed-Power Relationships of Digital Integrated Circuits

- 5. Fanout is doubled
- Terminated lines or controlled impedance circuit boards are normally not required.
- The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
- 8. The maximum flip-flop frequency has been increased to 200 MHz.

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving effeciency at the lower speeds. The 'AS devices

are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totempole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

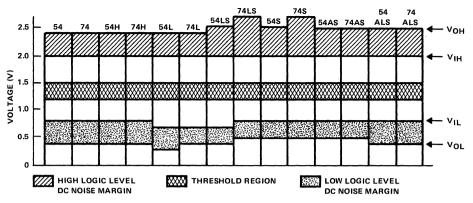


Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

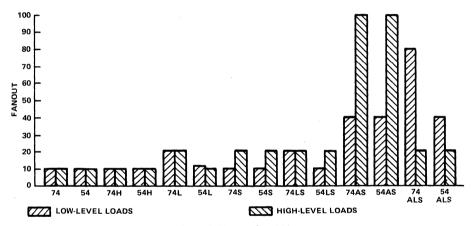


Figure 3. Fanout Capability

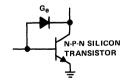


Figure 4. Baker Clamp

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which

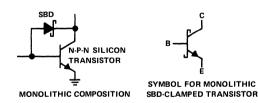


Figure 5. The Schottky-Clamped Transistor

has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metalsemiconductor contact formed between a metal and a highly doped N semiconductor.

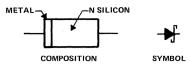


Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F.

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the currentvoltage characteristics according the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

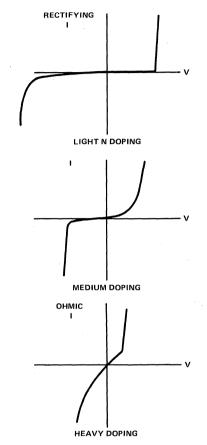


Figure 8. Metal-N Diode Current-Voltage Characteristics

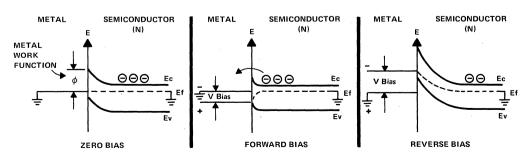


Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

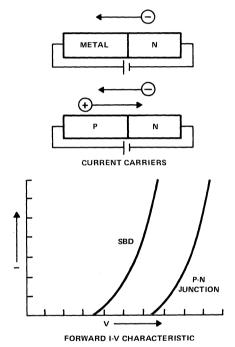


Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/'S process which consists of conventional masks, junction isolation, and a

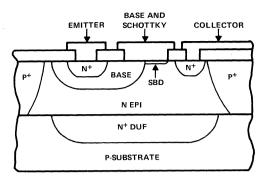


Figure 10. Standard Process ('LS/'S)

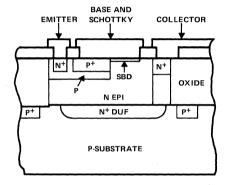


Figure 11. Advanced Process ('ALS/'AS)

standard metal system and Figure 11 illustrates the 'ALS/'AS process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

- Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
- Elimination of transistor storage time provides stable switching times across the temperature range.
- An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

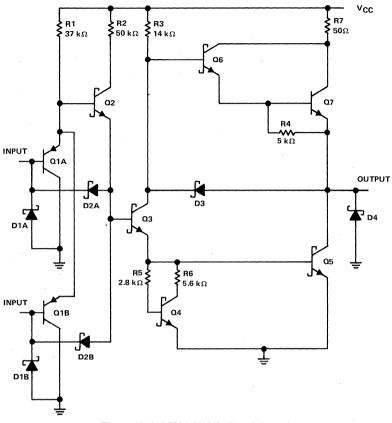


Figure 12. 'ALSOOA NAND Gate Schematic

- 4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
- The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
- The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$VT = V_{BE} \text{ of } Q2 + V_{BE} \text{ of } Q3$$

$$+ V_{BE} \text{ of } Q5 - V_{BE} \text{ of } Q1A$$

$$(\text{or } V_{BE} \text{ of } Q1B) \tag{1}$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = V_{CC} - V_{BE} \text{ of Q1A}$$

- $V_{I}/[R(h_{FE}^{4} \text{ of Q1A} + 1)]$ (2)

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically $-10 \mu A$ for the 'ALS00A and $-50 \mu A$ for the 'AS00. Highlevel output voltage V_{OH} is determined primarily by V_{CC} ,

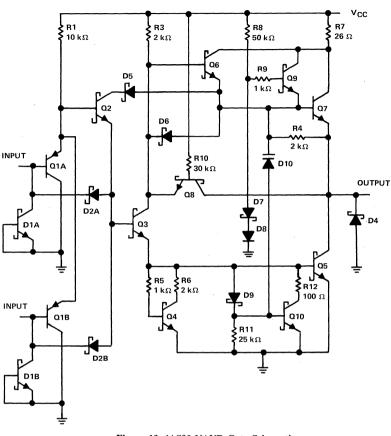


Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC}-V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC}-V_{BE}$ of Q6 — V_{BE} of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than 1 μ A and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through } R7} \times R7$$
$$- V_{CE} \text{ of } Q6 - V_{BE} \text{ of } Q7$$
(3)

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14 Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a '54ALS device that is driving a '54ALS device and up to 80 for a '74ALS device, that is driving a '74ALS device and provides a guaranteed low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of '54ALS/'74ALS devices, a factor four times better than '54LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are guaranteed over the entire temperature range (-55°C to 125°C) for series 54ALS/54AS and 0°C to 70°C for series 74ALS/74AS)]. In addition, the dc limits are guaranteed over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} The voltage value required for a low-level input voltage that guarantees operation
- V_{IH} The voltage value required for a high-level input voltage that guarantees operation
- Vol. The guaranteed maximum low-level output voltage of a gate
- V_{OH} The guaranteed minimum high-level output voltage of a gate.

With the exception of high-level ouput voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS''AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

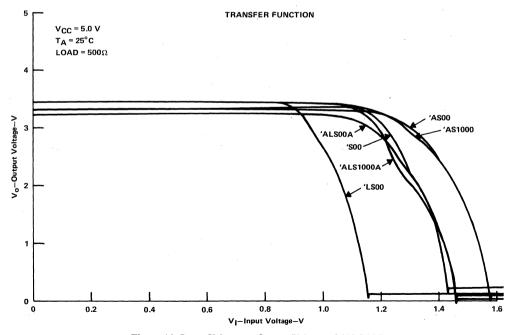


Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

| Applications

a better high-level noise immunity in 'ALS and and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I, characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out

of a device input terminal is designated as negative. Lowlevel input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

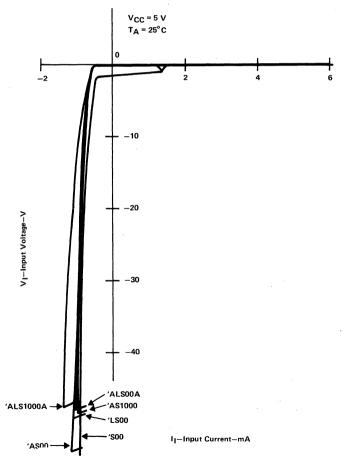


Figure 15. Input Current vs Input Voltage for TTL Families

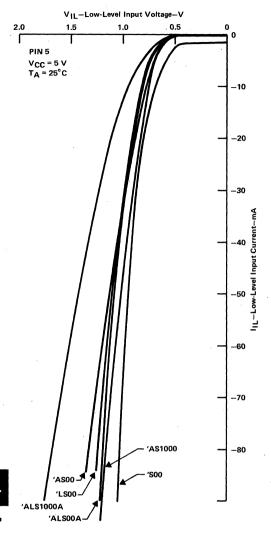


Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

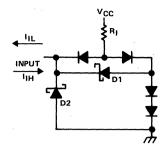


Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than -1.2 V for 'AS and -1.5 V for 'ALS with a forward current of 18 mA. These values are guaranteed at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdissipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the pushpull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing IoS capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

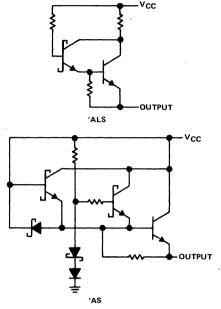


Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage VOI. This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are guaranteed on Series 'ALS and 'AS gates: propagation delay time for a high-level to a low-level at the output tpHI, and a low-level to high-level transition time tpl.H. Both parameters are specified with respect to the input pulse using standard test conditions as follows:

$$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$$
 $C_L = 50 \text{ pF}$
 $R_L = 500$
 $T_A = \text{MIN to MAX}$

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

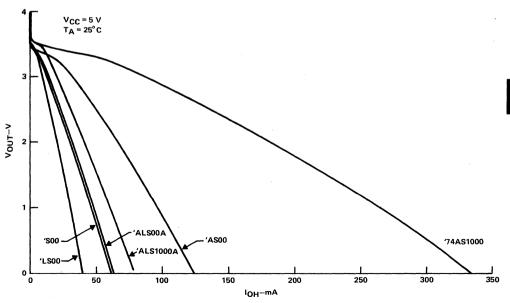


Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification which guarantees the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL}

maximum) and the guaranteed worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table 2 lists the worst-case output limits for the 'AS and 'ALS families.

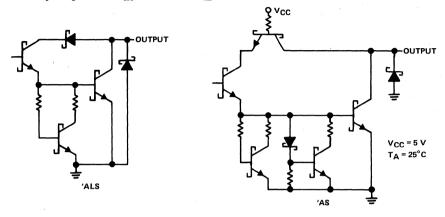


Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

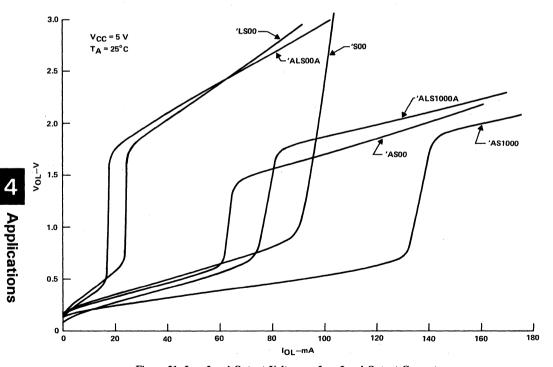


Figure 21. Low-Level Output Voltage vs Low-Level Output Current

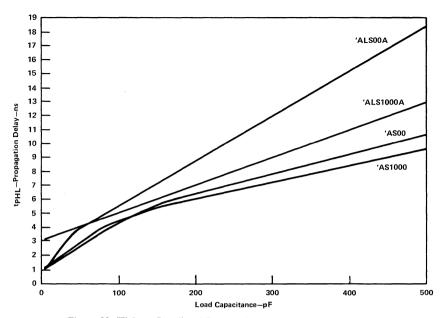


Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

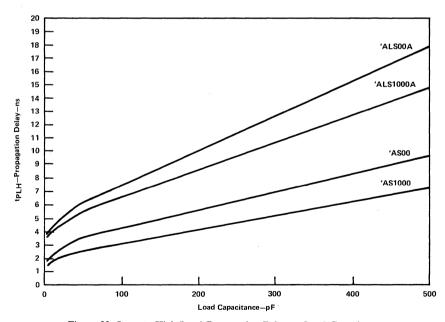


Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

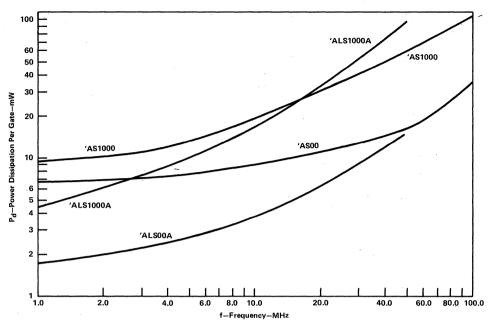


Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting VOH minimum from VIH minimum. The low-level noise margin is obtained by subtracting VII, maximum from VOI. maximum. The worst-case high-level noise margin is guaranteed to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To guarantee an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device will not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table 2.	Worst	Case	Output	Paramet	ters
----------	-------	------	--------	---------	------

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (-55°C to 125°C)	'ALS (-55°C to 125°C)	
V _{IH} (MIN)	2	2	2	2	
V _{IL} (MAX)	0.8	0.8	0.8	0.8	
V _{OH} (MIN) @ _{CC} = 4.5 V*	2.5	2.5	2.5	2.5	
V _{OL} (MAX)	0.5	0.5	0.5	0.4	
High Level Noise Margin (VOH-VIH)	0.5	0.5	0.5	0.5	
Low Level Noise Margin (V _{IL} -V _{OL})	0.3	0.3	0.3	0.4	

^{*}Actual specification for VOH(min) is VCC - 2 V.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

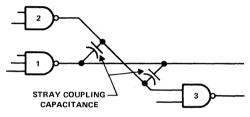


Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed 1 for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse shown in Figure 26(c) is a ramp input.

$$e_i(t) = \frac{E_i}{T} t$$

where

 E_i = Maximum input voltage and T = Total rise time of input voltage

The output pulse is represented analytically by

$$e_0(t) = \frac{E_i}{T} RC \left(1 - e^{-i/T}\right)$$

$$e_0(i) = E_i \tau \left(1 - e^{-i/\tau}\right)$$

where '

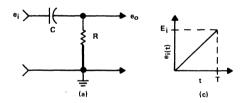
$$\tau = \frac{RC}{T}$$

$$\theta(i) = \tau \left(1 - e^{-i/\tau}\right)$$

$$\theta(i) = \frac{eO(i)}{E_i}$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ . Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i . Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns



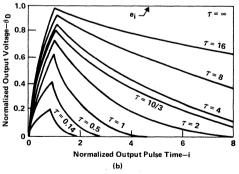


Figure 26. Evaluations of Gate Response to Fast Input Pulses

with gate 2 at a high-logic state. Assume a nominal output impedance of 58 Ω (30 Ω for 'AS) and coupling capacitance of 10 pF. Use the following formula:

Total rise time T =
$$\frac{3 \text{ V}}{1 \text{ V/ns**}}$$
 = 3 ns[†]

$$\tau = \frac{\text{RC}}{\text{T}} = \frac{(10 \times 10^{-12})(58)}{3}$$

$$= \frac{0.58 \times 10^{-9}}{3} = 0.19 \text{ ns}$$

**2.5 V/ns for 'AS †1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns. The output voltage scale will be multiplied by 3 V. Using the $\tau = 0.19$ curve gives a peak e_0 of 0.57 V (0.19 \times 3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (0.57 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

If an open-collector gate is used with a passive 1 k Ω pullup resistor, the situation would change. Use the following formula:

Total rise time =
$$\frac{3 \text{ V}}{1 \text{ V/ns**}} = 3 \text{ ns}^{\dagger}$$

 $\tau = \frac{(10 \times 10^{-12})(1 \times 10^3)}{3}$
 $= \frac{10 \times 10^{-9}}{3} = \frac{10}{3} \text{ ns}$

**2.5 V/ns for 'AS †1.2 ns for 'AS

Now the amplitude (from the curves) approaches 2.58 V (0.86×3) and the pulse width at the 50% points is approximately 8.52 ns (2.84 \times 3). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emhasized noise rejection.

Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate

networks and, because of their small size, are more superior in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.

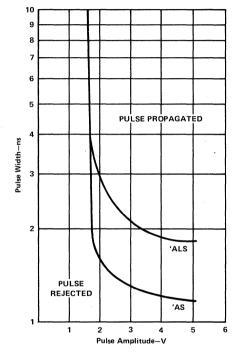
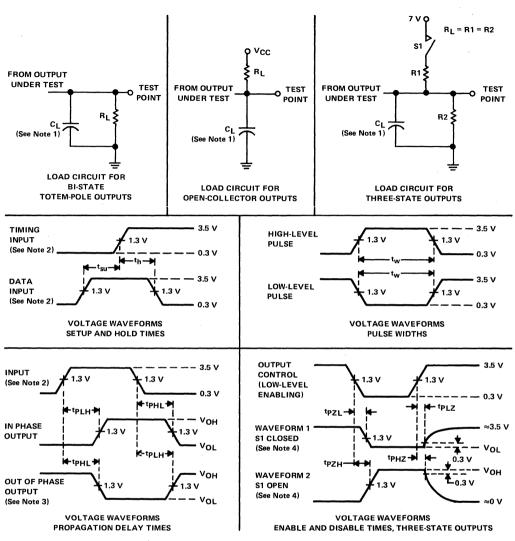


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables 3 through 6 provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.



- NOTES: 1. C_L includes probe and jig capacitance.
 - 2. All input pulses have the following characteristics PRR \leq 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - 3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
 - 4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise

margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still

operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS/'AS devices is specified as supply voltage $-2 \text{ V } (V_{CC} - 2 \text{ V})$.

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

Table 3. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable.
	Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a
	dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at
	higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293–3913). For twisted-
	pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving
	ends. V _{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded
	parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays
	are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter
	than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving
	end of long cables. This provides added noise margin and more rapid rise times.

Table 4. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V _{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table 5. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V _{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 µF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 µF capacitors between VCC and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or VCC mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table 6. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Rise and fall times should be equal to or less than 15 ns/V and essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows:
clear inputs of flip-flops	1. Directly to V _{CC} , if the input voltage rating of 5.5 V maximum is not exceeded.
	2. Through a resistor equal to or greater than 1 k Ω to V $_{CC}$. Several inputs can be tied to one resistor.
	Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased.
	 Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE}$$
 of Q2 + V_{BE} of Q3 + V_{BE} of Q5

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\Delta V_{R} = V_{R} \left(\frac{R1/\beta}{R1/\beta + R2} \right)$$
$$= V_{R} \left(\frac{R1}{R1 + \beta R2} \right)$$

R1 = source impedance β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30 Ω . Because of cancellation between the driving gate and the driven gate, low-frequency ripple is not a problem.

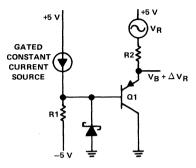


Figure 29. Effect of Source Impedance on Input Noise

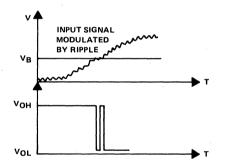


Figure 30. Spurious Output Produced by Supply Voltage Ripple

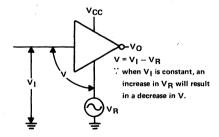


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic

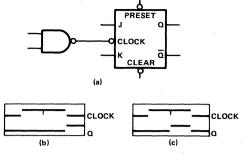


Figure 32. Typical Logic Circuit with Noisy Input

circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)], the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)], the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

- External noise External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field-generating. The methods of controlled to be considered are shielding, grounding, or decoupling.
- Power-line noise Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
- Cross talk Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
- Signal-current noise Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
- Transmission-line reflections Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
- Supply-current spikes Noise caused by switching several digital loads simultaneously.
 The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc. line driving, etc... must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance ZS connected to an impedance Z₀, and loaded with a resistance R₁.

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For

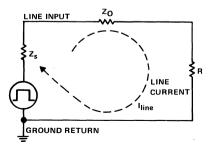


Figure 33. Diagram Representing a Gate Driving a **Transmission Line**

explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω . When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

$$V_I = E \frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where

E = source voltage

 Z_0 = line impedance

 Z_S = source impedance

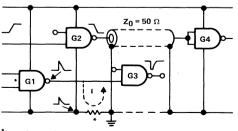
For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following

$$I_{line} = \frac{V_{in}}{Z_0} = \frac{2.5}{50} = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver. a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

> 1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.



*Impedance of poor ground return

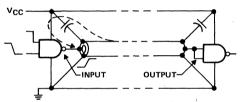
Figure 34. Noise Generation Caused by Poor **Transmission-Line Return**

2. Decouple the supply voltage of line-driving and line-receiving gates with a 0.1-µF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state. the external loading, the transients caused by charging and discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt}$$
 (4)

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

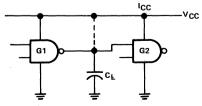


Broken arrow shows path of line-charging current

Figure 35. Ideal Transmission-Line **Current Handling**

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance CL (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low,



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

the load capacitance is shorted to ground by transistor O5 (shown in Figures 12 and 13) and has no effect on supply current.

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors O7 and O5 (shown in Figures 12 and 13). The situation arises because transistor O7 can turn on faster than transistor O5 can turn off. This places a direct circuit consisting of transistors O7 and O5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CC}max = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects; the difference in highlevel and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring VO and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of 50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to

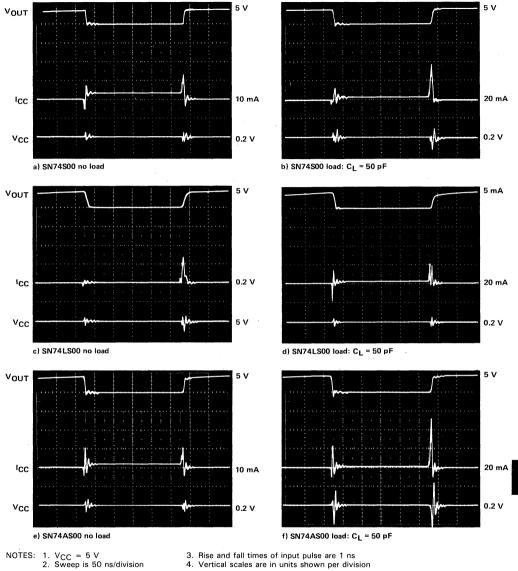


Figure 37(a). Supply-Current Transient Comparisons



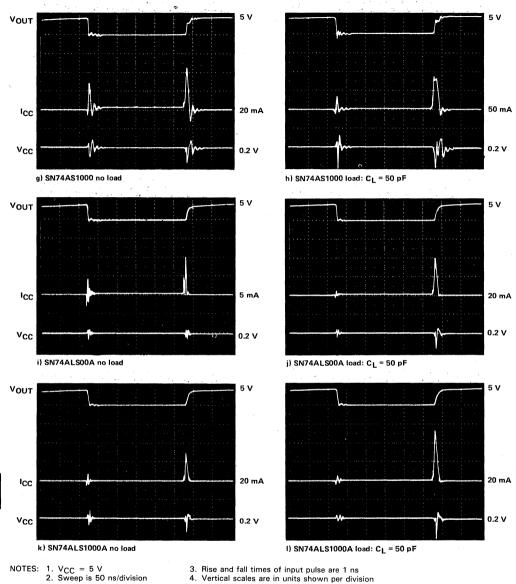


Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

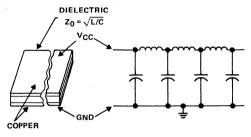


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

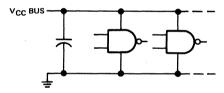


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C1 by assuming that the parameters have common values as follows:

$$\Delta I_{CC} = 50 \text{ mA}$$

$$\Delta V = 0.1 \text{ V}$$

$$\Delta T = 20 \text{ ns}$$

Then the equation is as follows:

$$C1 = \frac{\Delta I_{CC}}{\Delta V / \Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})}$$
$$= \frac{50 \times 10^{-3}}{0.1} = 10,000 \times 10^{-12}$$
$$= 0.01 \ \mu F$$

The same method may be used for the low-frequency capacitor C2. However, the factor ΔT , which was a worst-case transient time for calculating C2, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using $10~\mu F$ to $50~\mu F$ capacitors.

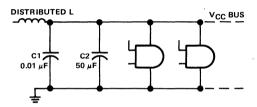


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μ H to 10 μ H is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

- Use as wide a ground strap as possible.
 Form a complete loop around the board by
- 2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 µF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 µF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

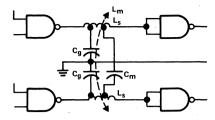
Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

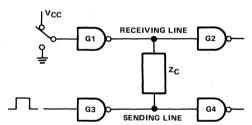


ALL GATES SN74ALS00

Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_{C} onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.



(Z_C) - COUPLING IMPEDANCE

Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \tag{5}$$

where

 V_{G3} = open-circuit logic voltage swing generated by gate G3

R_{S3} = output impedance of gate G3

 Z_0 = line impedance

V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_{C} into

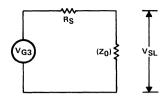


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z₀₁ (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5 Z_0 + Z_c)}$$

The voltage impressed on the receiving line (VRI) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2 V_{RL} = V_{G3} \left(\frac{1}{1.5 + \frac{Z_c}{Z_0}} \right) \left(\frac{Z_0}{RS3 + Z_0} \right)$$

In the switching period, the transistor has a very low output impedance. Then RS3 << Z0 and Vin(2) can be simplified to the following:

$$V_{in(2)} = V_{G3} \left(\frac{1}{1.5 + \frac{Z_c}{Z_0}} \right)$$

The term $V_{in(2)/V_{G3}}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very highspeed logic circuits has a guaranteed noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

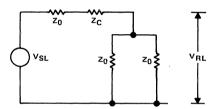


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

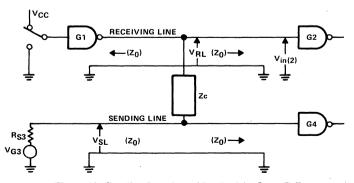


Figure 44. Coupling Impedances Involved in Cross Talk

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables 7 and 8.

Table 7. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance	Capacitance		
H (mils)	W (mils)	Z _O (Ω)	per Foot (pF)		
6	20	35	40		
6	15	40	35		
15	20	56	30		
15	15	66	26		
30	20	80	20		
30	15	89	18		
60	20	105	16		
60	15	114	14		
100	20	124	13		
100	15	132	12		

Relative dielectric constant ≈5

Table 8. Typical Impedance of Strip Lines

Dimens	ions	Line Impedance	Capacitance		
H'a = H'b =	W (mils)	Z _O (Ω)	per Foot (pF)		
(mils)		20 (11)	per root (pr)		
6	20	27	80		
6	15	32	70		
10	20	34	67		
10	15	40	56		
12	20	37	57		
12	15	43	48		
20	20	44	48		
20	15	51	42		
30	20	55	39		
30	15	61	35		

Relative dielectric constant ≈5, and H'a = H'b

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

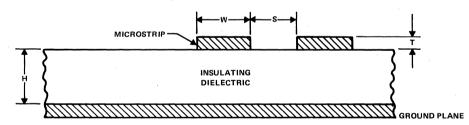


Figure 46. Microstrip Line

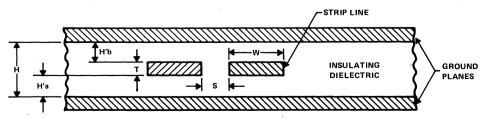


Figure 47. Strip Line

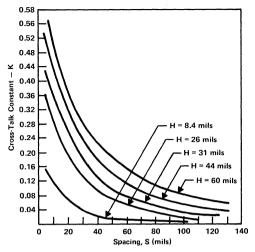


Figure 48. Line Spacing Versus Cross-Talk Constant

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately 30 Ω . To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ ($Z_0=30~\Omega$), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0 , the driver output voltage is determined by the intersection of

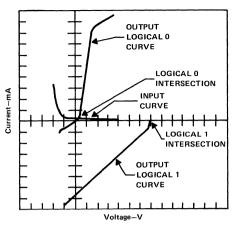


Figure 49. TTL Bergeron Diagram

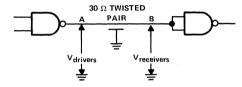


Figure 50. 'ALS/'AS Driving Twisted Pair

 $-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)}-t_n$ = time delay of line], the receiving gate sees -0.7 V. Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0 , the driver output rises to 2.2 V and, at time t_1 , the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

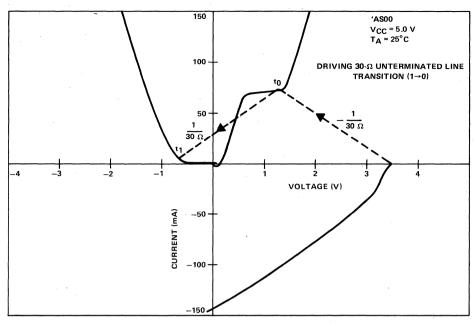


Figure 51. 'AS -ve Transition Bergeron Diagram

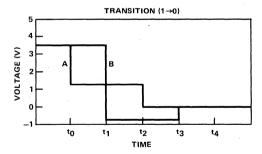


Figure 52. 'AS -ve Voltage/Time Plot

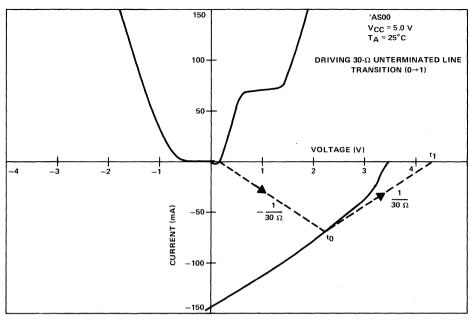


Figure 53. 'AS +ve Transition Bergeron Diagram

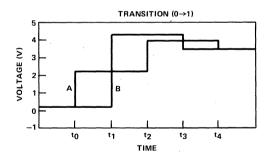


Figure 54. 'AS +ve Voltage/Time Plot

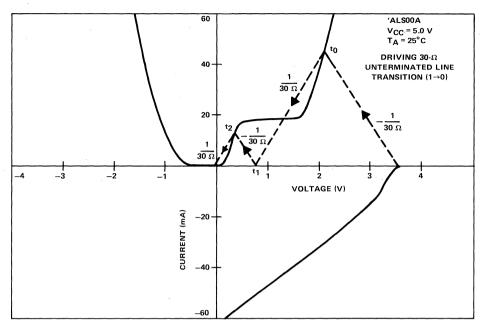


Figure 55. 'ALS -ve Transition Bergeron Diagram

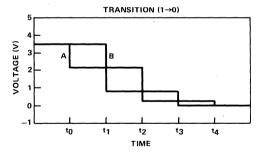


Figure 56. 'ALS -ve Voltage/Time Plot

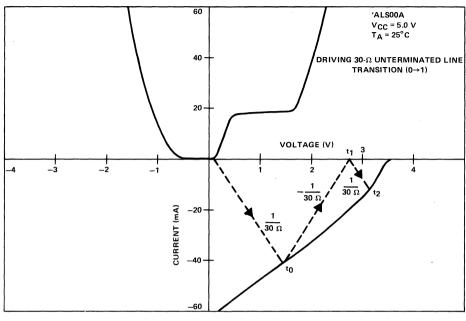


Figure 57. 'ALS +ve Transition Bergeron Diagram

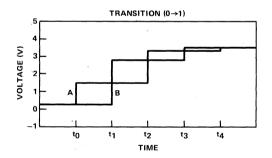


Figure 58. 'ALS +ve Voltage/Time Plot

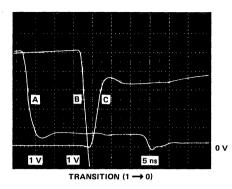


Figure 59. Oscilloscope Photograph of 'AS001 -ve Transition Using 50-Ohm Line

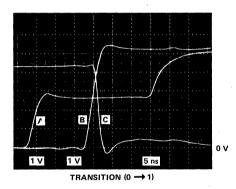


Figure 60. Oscilloscope Photograph of 'AS00 +ve Transition Using 50-Ohm Line

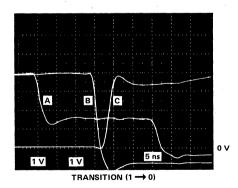


Figure 61. Oscilloscope Photograph of 'AS00 -ve Transition Using 25-Ohm Line

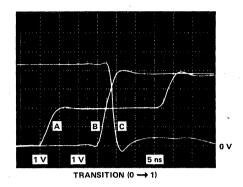


Figure 62. Oscilloscope Photograph of 'AS00 +ve Transition Using 25-Ohm Line

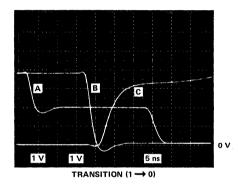


Figure 63. Oscilloscope Photograph of 'ALS00A -ve Transition Using 50-Ohm Line

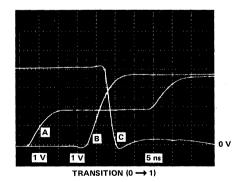


Figure 64. Oscilloscope Photograph of 'ALS00A +ve Transition Using 50-Ohm Line

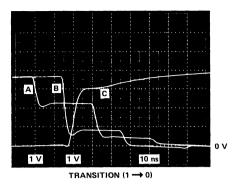


Figure 65. Oscilloscope Photograph of 'ALS00A -ve Transition Using 25-Ohm Line

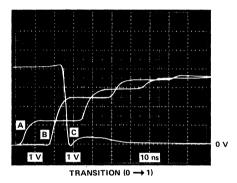


Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

- 1. W.C. Elmore and M. Sands, Electronics Experimental Techniques, McGraw-Hill Book Co., New York, 30ff. (1949).
- 2. M. Williams and S. Miller, Series 54ALS/74ALS Schottky TTL Applications B215, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input cuurent requirements in Table A-1), which can be summed and compared directly to the fanout capability (see Table A-2) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-1 AND A-2

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-1). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-2.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

SERIES	1/0	INPUT	INPUT CORRENT NORMALIZED								
	1/0	(mA)	'00	'H00	'L00	'LS00	'S00	'AS00	'ALSOOA	'AS1000	'ALS1000A
54/7400	н	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	н	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11,11	5	1	4	20	4	20
54/74L00	н	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	н	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	н	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	н	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	н	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	Н	0.02	0.5	0.4	2	- 1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-1. Normalized Input Currents

Table A-1 is normally used (in combination with Table A-2) when replacing one logic family with another in an existing

Table A-2 is normally used when originally designing a system which employs several TTL families to optimize performance.

Table A-2. Fanout Capability (Output Currents Normalized to Input Currents)

		OUTPUT	OUTPUT DRIVE NORMALIZED								
SERIES		1	,00	'H00	'L00	'LS00	'S00	'AS00	'ALSOOA	'AS1000	'ALS1000A
	1/0	CURRENT	*HI 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02
		(mA)	[†] LO 1.6	2	0.18	0.4	2	0.5	0.1	0.5	0.1
54/7400	н	0.4	10	8	40	20	8	20	20	20	20
54/7400	LO	16	10	8	88.89	40	8	32	160	32	160
54H/74H00	HI	0.5	12.5	10	50	25	10	25	25	25	25
54H/74H00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54L00	HI	0.1	2.5	2	10	, 5	2	5	5	5	5
54L00	LO	2	1.25	1	11.11	5	1	4	20	4	20
74L00	Hi	0.2	5	4	20	10	4	10	10	10	10
74L00	LO	3.6	2.25	1.8	20	9	1.8	7.2	36	7.2	36
54LS/74LS00	HI	0.4	10	8	40	20	8	20	20	20	20
54LS00	LO	4	2.5	2	22.22	10	2	8	40	8	40
74LS00	LO	8	5	4	44.44	20	4	16	80	16	80
54S/74S00	н	1	25	20	100	50	20	50	50	50	50
54S/74S00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54AS/74AS00	н	2	50	40	200	100	40	100	100	100	100
54AS/74AS00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54ALS/74ALS00A	н	0.4	10	8	40	20	8	20	20	20	20
54ALS00A	LO	4	2.5	2	22.22	10	2	8	40	8	40
74ALS00A	LO	8	5	4	44.44	20	4	16	80	16	80
54AS1000	н	40	1000	800	4000	2000	800	2000	2000	2000	2000
54AS1000	LO	40 -	25	20	222.22	100	20	80	400	80	400
74AS1000	н	48	1200	960	4800	2400	960	2400	2400	2400	2400
74AS1000	LO	48	30	24	266.67	120	24	96	480	96	480
54ALS1000A	HI	1	25	20	100	50	20	50	50	50	50
54ALS1000A	LO	12	7.5	6	66.67	30	6	24	120	24	120
74ALS1000A	н	2	65	52	260	130	52	130	130	130	130
74ALS1000A	LO	24	15	12	133.33	60	12	48	240	48	240

^{*}Input Current HI

[†]Input Curent LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

High-level input voltage ViH

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

VII. Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Positive-going threshold voltage V_{T+}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, VT -.

Negative-going threshold voltage V_{T}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

High-level output voltage VOH

The voltage at an output terminal for a specified output current IOH with input conditions applied that according to the product specification will establish a high level at the output.

Low-level output voltage VOL

The voltage at an output terminal for a specified output current IQL with input conditions applied that according to the product specification will establish a low level at the output.

On-state output voltage V_{O(on)}

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

VO(off) Off-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

High-level input current ΙΉ

The current flowing into* an input when a specified high-level voltage is applied to that input.

Ш Low-level input current

The current flowing into* an input when a specified low-level voltage is applied to that input.

^{*}Current flowing out of a terminal is a negative value.

Applications

IOH High-level output current

The current flowing into* the output with a specified high-level output voltage VOH applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

IO(off) Off-state output current

The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

IOS Short-circuit output current

The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

ICCH Supply current, output(s) high

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

ICCL Supply current, output(s) low

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

fmax Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

tHZ. Output disable time (of a three-state output) from high level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

tLZ Output disable time (of a three-state output) from low level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

tpLH Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

tPHL Propagation delay time, high-to-low-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

tTLH Transition time, low-to-high-level output

The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

tTHI. Transition time, high-to-low-level output

The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

tw Average pulse width

The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

^{*}Current flowing out of a terminal is a negative value.

th Hold time

The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

Release time trelease

The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

Setup time tsn

The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

Output enable time (of a three-state output) to high level tzH.

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

Output enable time (of a three-state output) to low level tzI.

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration

Integrated circuits of less complexity than medium-scale integration (MSI).

^{*}Current flowing out of a terminal is a negative value.

Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families

Robert K. Breuninger and Kevin Frank



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INTRODUCTION

At some point in every system designers career, they are faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically solved by synchronizing one of the signals, to the local clock, through a flip-flop. However, this solution presents an awkward dilemma, the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop used can influence overall system reliability. The purpose of this application report is to give the system designer a better understanding of the metastable characteristics pertaining to Texas Instruments Advanced Schottky Bipolar Logic Family.

METASTABLE DEFINITION

Whenever a flip-flops setup and hold time is violated, the flip-flops output response is uncertain. Presently, there is no circuit that can 100% guarantee its response. This is why the device manufacturer does not guarantee its operation. Specifically, the metastable state is defined as that time period when the output of a digital logic device, is not at a logic level 1 (V_{out} less than 2 V) or a logic level 0 (V_{out} greater than 0.8 V), but instead between 0.8 V and 2 V. Since the input data is changing at the time of being clocked, the system designer does not care if the flip-flop goes to either a high or low logic level, just so long as the output does not hang up in the metastable region. The metastable characteristics for a particular flip-flop will determine how long the device stays in the metastable region. This concept is illustrated in the timing diagram of Figure 1.

METASTABLE EVALUATION

Anyone who has tried to evaluate the metastable characteristics for a particular flip-flop, has probably found it is not an easy task. The number of times the output hangs up in the metastable region is extremely small when compared to total number of clock transitions. In addition, the amount of time the output is actually in the metastable region is a variable and dependent on the type of flip-flop used (LS, ALS, AS, etc.).

From the design engineers viewpoint, when using a flip-flop as a data synchronizer, they can no longer use the specified data sheet maximum for propagation delay. Instead, to guarantee reliable system operation, they need to know how long after the specified data sheet maximum they need to wait before using the data. Conventional test equipment is not designed to measure these parameters, so a special test circuit is required for characterizing MTBF (Mean Time Between Failures) and Δt (time between CLK and Q valid). With these two parameters specified, the system designer can make a rational decision about what type of flip-flop to use, and how long to wait before using the data.

Circuit Description

The circuit in Figure 2 can be used in evaluating MTBF and Δt for a selected flip-flop (DUT, Device Under Test). Two 'AS04s are used to detect whenever the Q output of the DUT is in the metastable region. This is accomplished by adjusting the input threshold to 2 V on one inverter and 0.8 V on the other. Notice that input thresholds are adjusted by referencing the ground input pins to 0.6 V and -0.6 V respectively. Therefore, whenever the Q output of the DUT

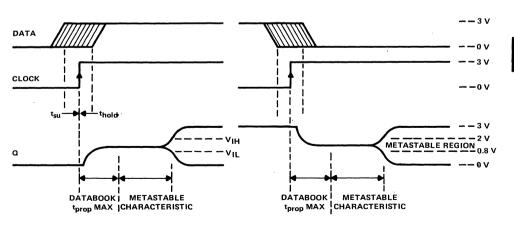


Figure 1. Metastable Timing Diagram

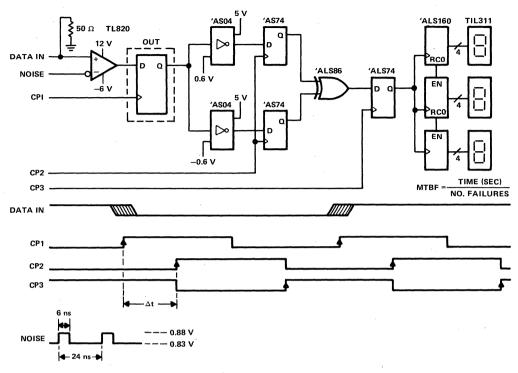


Figure 2. Metastable Evaluation Test Circuit

is between 0.8 V and 2 V, the inverters will be in opposite states. Whenever the Q output of the DUT is higher than 2 V or lower than 0.8 V, both inverters will be at the same logic level. The outputs of the 'AS04s are then clocked (CP2) into two 'AS74s a selected time (Δt) after the DUT clock (CP1). The outputs of the 'AS74s are compared through an 'ALS86 and clocked (CP3) into another 'ALS74. This guarantees against any false clocking by the evaluation circuit. The output of the 'ALS74 is then feed to a series of three 'ALS160 counters, and on into three TIL311s for counter display.

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal must jitter around the threshold of the input clock. The width of the jitter should equal, or exceed the setup and hold time specification for the device. In our evaluation circuit, this is accomplished by feeding a low level noise signal into the negative input of a TIL820 operational amplifier. The pictures shown in Figure 3 show the noise generated around the DUT clock (CP1) for both input data transitions.

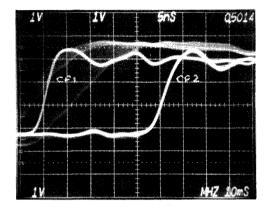
It should be intuitively obvious that the worst-case condition, for any specified input data frequency, will be when the input data always violates the data setup and hold times. This condition is shown in the timing diagram of Figure 2. Any other relationship of CP1 to DATA IN, would provide less chance for the device to enter the metastable state. Therefore, it can be concluded that the worst-case condition for a given input data frequency, will be 0.5 times the DUT clock rate where the input data always violates the setup and hold time.

By using the described circuit, MTBF can be determined for several different values of Δt . Plotting this information on semilog paper reveals the metastable characteristics, for the selected flip-flop, at the desired input data frequency.

Test Circuit Limitations

Before we proceed to the AS/ALS test results, it is important to analyze the limitations of our test circuit. In this way, we can better understand its effects on the test results. Two major areas which can greatly affect the test results are not centering the jitter around the input clock, and propagation delay of the 'AS04s. By not centering the jitter around the input clock, the risk of entering the metastable state is reduced. Proper care must be taken to ensure that the jitter is always centered around the input clock to guarantee worst-case conditions.

The propagation delay of the 'AS04s affect the test results because they add propagation delay between the output of the DUT, and the data being clocked into the 'AS74s. For



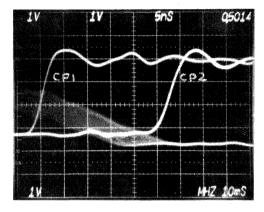


Figure 3. Test Waveforms

example, the output on the DUT may come out of the metastable region, but the 'AS04s may not switch before CP2 occurs. This causes an inappropriate reading. The typical propagation delay of the 'AS04s, as configured in the test circuit, is approximately 4 ns. This 4 ns delay should be considered when evaluating the test results. If inverters slower than the 'AS04s are used in the test circuit, a larger offset must be considered.

ALS/AS Test Results

Using the test circuit described in Figure 2, 'ALS74s, 'ALS273s and 'ALS374s were evaluated at several different Δt time periods. The input clock frequency used was 1 MHZ with an input data frequency of 500 kHz. The devices were allowed to run until an appropriate amount of errors were recorded. The number of errors were then divided by the total time the devices were allowed to run. This results in a MTBF for the selected Δt . The information was then recorded on semilog paper for analysis. It was found that all three device types exibited basically the same metastable

characteristics within +3 ns of each other. This was expected since all three device types come from the same technology. The same experiment was performed using AS and LS devices. The average characteristics for all three device families are shown in Figure 4. The 4-ns offset generated by the test circuit has not been subtracted from the data.

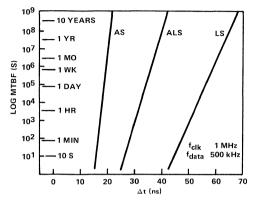


Figure 4. AS/ALS/LS Metastable Characteristics

Other Clock Frequencies

Clock frequencies other than 1 MHz will either increase or decrease the probability of the device entering the metastable state. The faster the frequency, the higher the probability of entering the metastable state. Likewise, the slower the frequency, the lower the probability of entering the metastable state. From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies. Equation (1) relates input clock and data frequency, to metastable characteristics.

Metastable Equation

$$\frac{1}{\text{MTBF}} = f_{cp} \times f_{data} \times C1 \ e^{(-C2 \ \Delta t)}$$
 (1)

As stated earlier, the worst case situation for the test circuit shown in Figure 2, is when the data setup and hold time is always violated. Based on this assumption, the equation is reduced to the following.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times C1 \ e^{(-C2 \ \Delta t)}$$
 (2)

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data graphed in Figure 4, these constants can be solved for each device family. As an example, the constants are solved below for the ALS device family.

C2 is defined by the slope of the line. Picking two data points off the graph yields the following.

$$C2 = \frac{10^8 - 10^2}{40.2 - 28.2} (2.302) = \frac{6}{12} (2.302) = 1.151$$

By plugging C2 into equation 2, along with using one of the data points off the graph, C1 can be solved for.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times \text{C1 e}(-1.51 \Delta t)$$

$$\frac{1}{10^8} = \frac{1}{2} (10^6)^2 \times \text{C1 e}(-1.151 \times 40.2)$$

$$\text{C1} = 2.49$$

Inserting C1 and C2 into equation 2, yields the metastable equation for ALS.

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{\text{cp}}^2 \times 2.49 \text{ e}(-1.151 \Delta t)$$

Given this worst-case equation, the system designer can determine the metastable characteristics for ALS when using other input clock frequencies.

The equations for AS and LS can be derived using the same procedure. They are as follows.

AS:

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{\text{cp}}^2 \times 1.53 \times 10^7 \text{ e}(-2.92 \text{ }\Delta t)$$

LS:

$$\frac{1}{\text{MTBF}} = \frac{1}{2} f_{cp}^2 \times 306 \text{ e}^{-0.783 \Delta t}$$

To get a feel for the effect of changing the input clock frequency, Figure 5 shows the change in the metastable characteristics from 1 MHz to 10 MHz.

METASTABLE CHARACTERISTICS OF PROGRAMMABLE LOGIC

The PAL16R4A and TIBPAL16R4-15 from the programmable logic family were also evaluated. They exhibited very similar characteristics to the ALS curve. This was expected because they utilize the same technology. One important consideration when evaluating programmable logic in the test circuit described, is positioning the jittery data a few nanoseconds before CP1. This compensates for the delay of the AND/OR array which is usually positioned in front of the flip-flop. Remember that the jittery data must be violating the setup and hold time at the input to the flip-flop, not just at the device input. Some experimentation is usually required to find the worst-case condition.

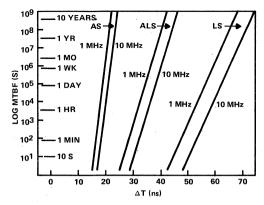


Figure 5. AS/ALS/LS Metastable Characteristics Variation with Frequency

As a general rule, a system designer can usually get a feel for the metastable characteristics of a device by simply looking at the setup and hold time specifications. Usually, the smaller the setup and hold time numbers, the better its metastable characteristics will be. However, in the case of programmable logic, the setup and hold time numbers are not reflective of metastable characteristics. This is because the setup and hold time numbers also reflect the propagation delay time of the AND/OR logic in front of the flip-flops.

SUMMARY

The metastable characteristics of a flip-flop used for data synchronization can greatly affect system reliability. Based on the information presented in this application report, the system designer can make a rational decision about what type of flip-flop to use, and what its metastable characteristics will be.

It is easy to see from the experimental data shown in Figure 4, that AS offers the best metastable characteristics. It has a much narrower setup and hold time window, and is quicker to recover once it gets into the metastable region. However, with adequate sampling time, ALS and LS will also perform well. The selection of what type of flip-flop to use must be based on the speed of the application. As a general rule, the faster the flip-flop, the better its metastable characteristics.

We at Texas Instruments believe that the graphs shown and equations derived, represent a reasonable assumption about the metastable characteristics for the device families discussed. However, we strongly recommend that when using flip-flops as data synchronizers, an adequate amount of guardband is allowed between the characteristics shown, and when the output of the flip-flop is actually sampled.

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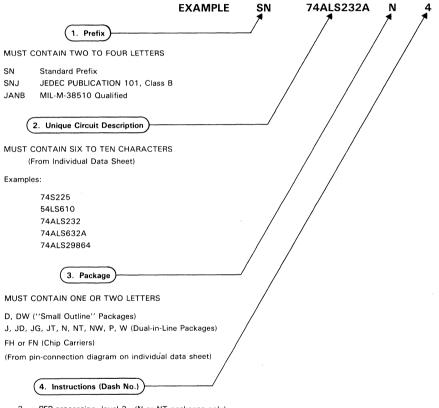
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Ordering Instructions Package Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



PEP processing, level 3 (N or NT packages only)

Dual-in-Line (J, JD, JG, JT, N, NT, NW, P, W)

- A-Channel Plastic Tubing
- Tape and Reel
- Barnes Carrier (W only)

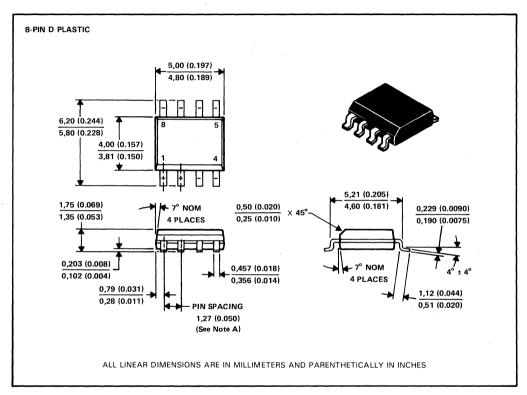


[†]These circuits in dual-in-line and "small outline" packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

[&]quot;Small Outline" (D, DW)

D plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

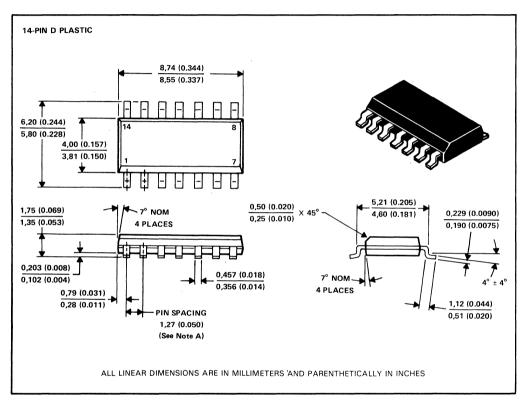


- NOTES: A. Body dimensions do not include mold flash or protrusion.
 - B. Mold flash or protrusion shall not exceed 0,15 (0.006).
 - C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
 - D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.



D plastic "small outline" packages

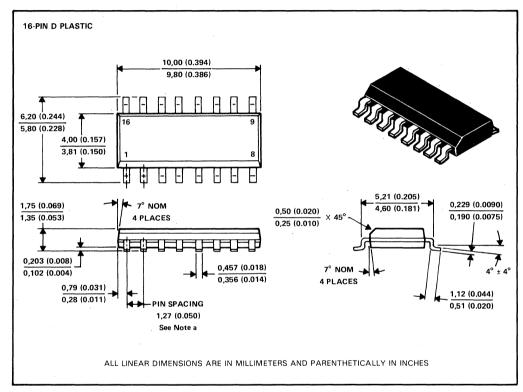
Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Body dimensions do not include mold flash or protrusion.
 - B. Mold flash or protrusion shall not exceed 0,15 (0.006).
 - C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
 - D. Lead tips to be planar within ± 0.051 (0.002) exclusive of solder.

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Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

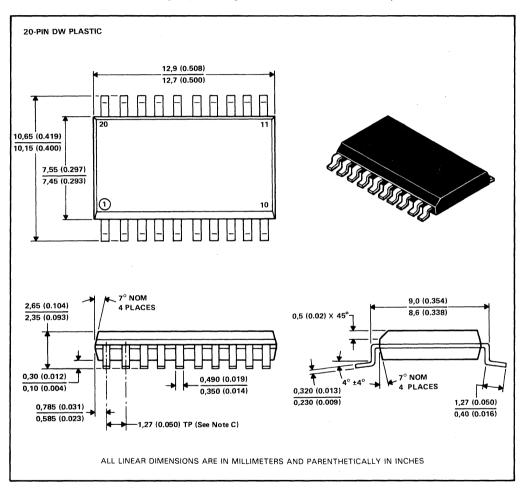


NOTES: A. Body dimensions do not include mold flash or protrusion.

- B. Mold flash or protrusion shall not exceed 0,15 (0.006).
- C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
- D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

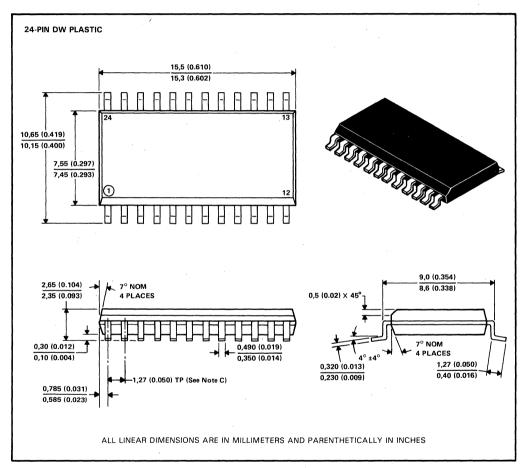


- NOTES: A. Body dimensions do not include mold flash or protrusion.
 - B. Mold flash or protrusion shall not exceed 0,15 (0.006).
 - C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
 - D. Lead tips to be planar within ± 0.051 (0.002) exclusive of solder.



DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Body dimensions do not include mold flash or protrusion.

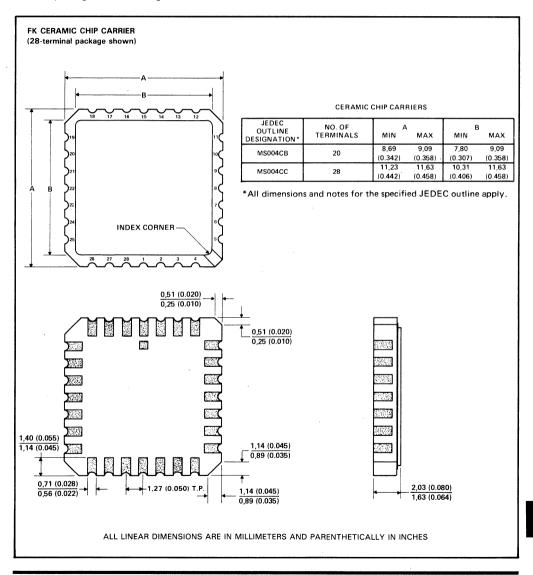
- B. Mold flash or protrusion shall not exceed 0,15 (0.006).
- C. Leads are within 0.25 (0.010) radius of true position at maximum material dimension.
- D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.



FK ceramic chip carrier packages

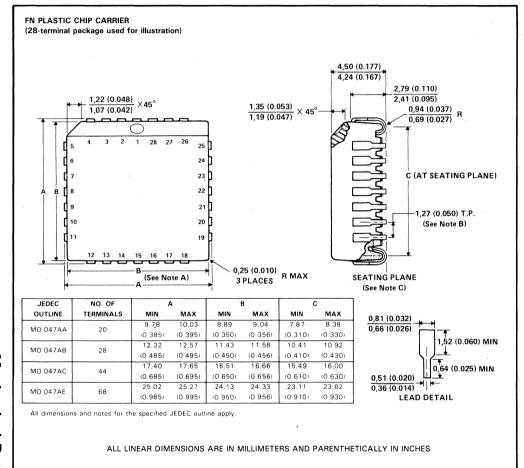
Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers, terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.



FN plastic chip carrier packages

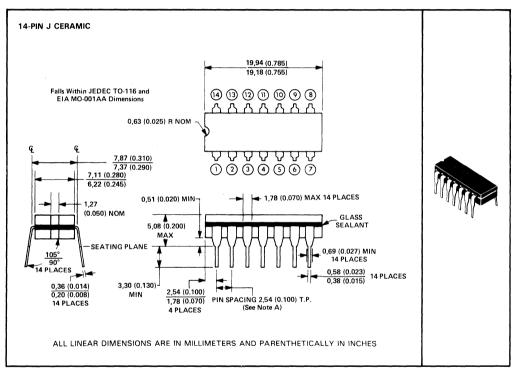
Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Centerline of center pin each side within 0,10 (0.004) of package centerline as determined by dimension B.
 - B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
 - C. The lead contact points are planar within 0,10 (0.004)

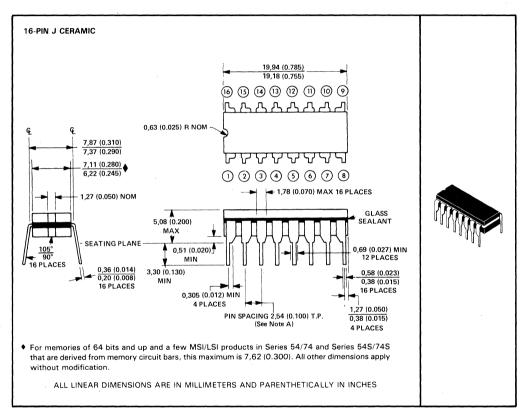


Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



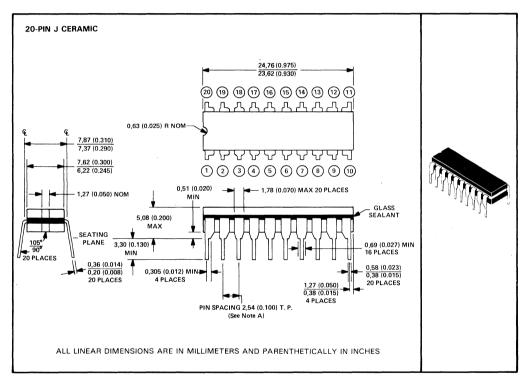
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.



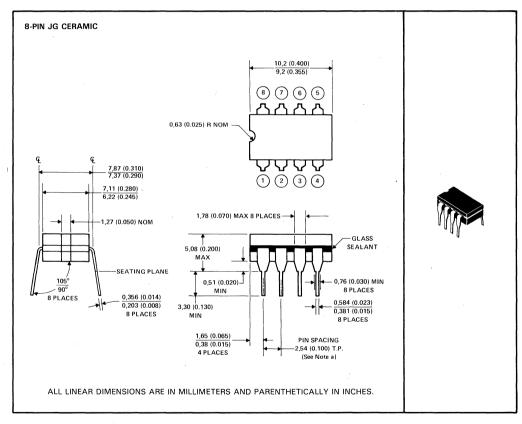
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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NOTE A: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

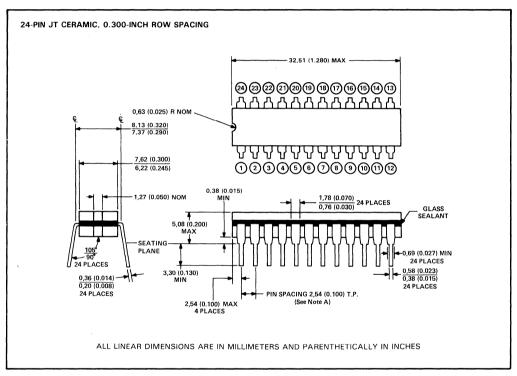
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NOTE A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



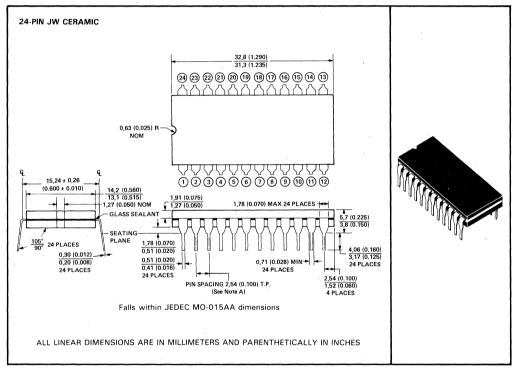
Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

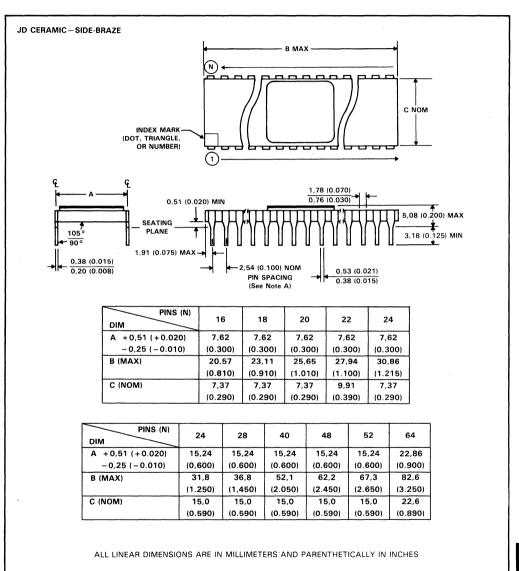


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

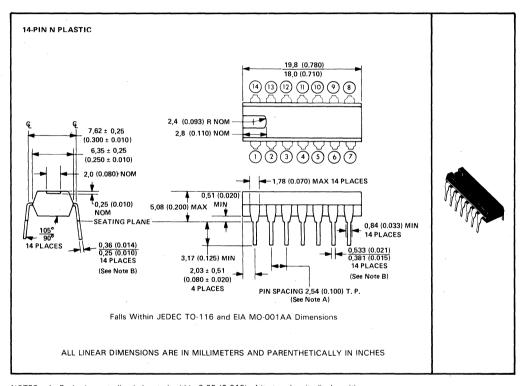


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

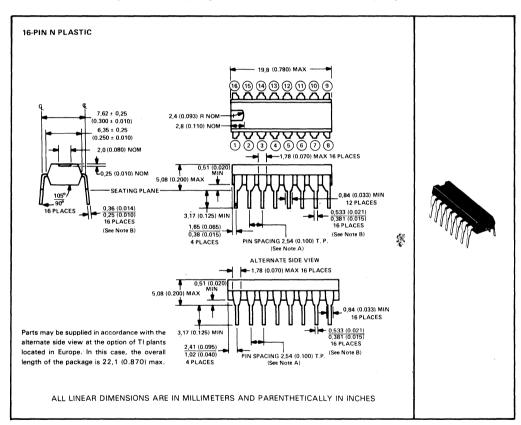
NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

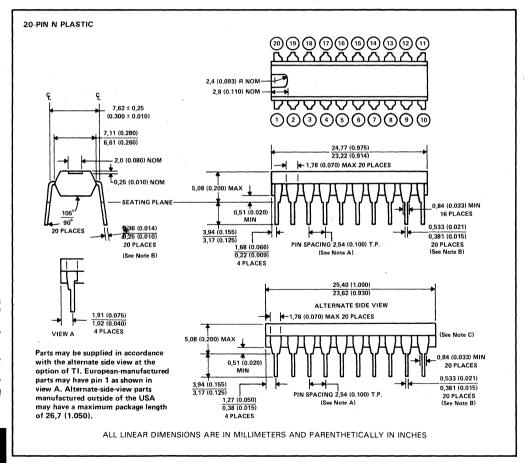


NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.



B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

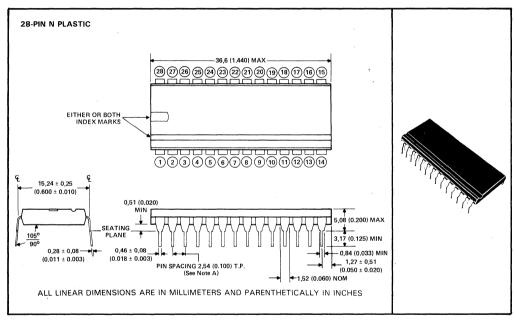
Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 - B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.
 - C. Parts may be supplied with a draft angle of 7° typical at the option of TI.

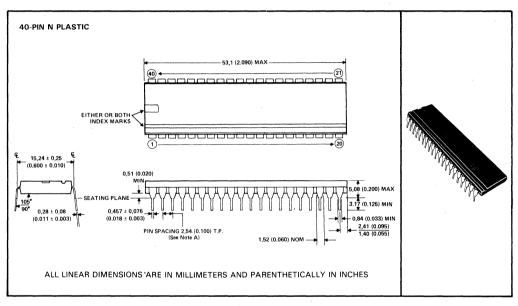


Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



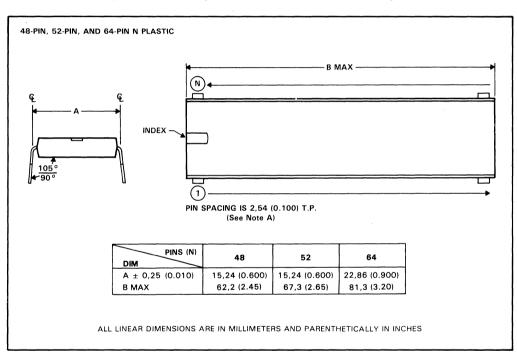
- NOTES: A, Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
 - B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

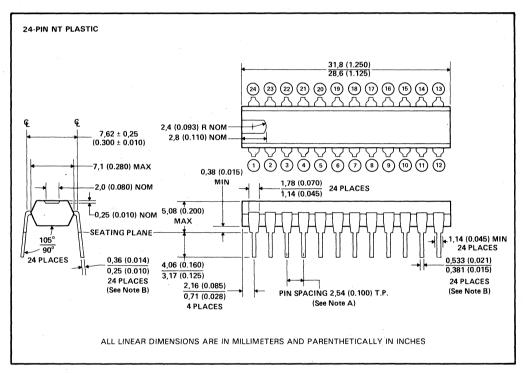
Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

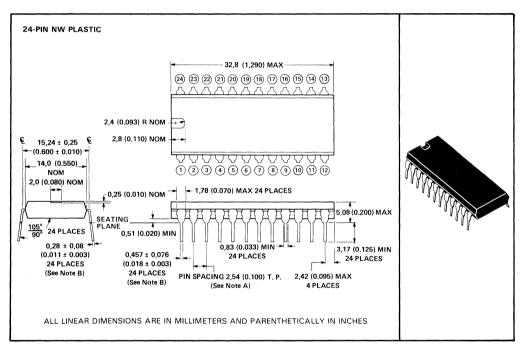
NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

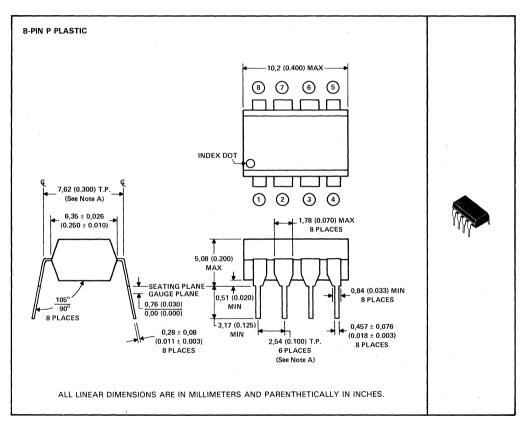
Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300), 15,24 (0.600), or 22,86 (0.900) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 - B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

P dual-in-line plastic package

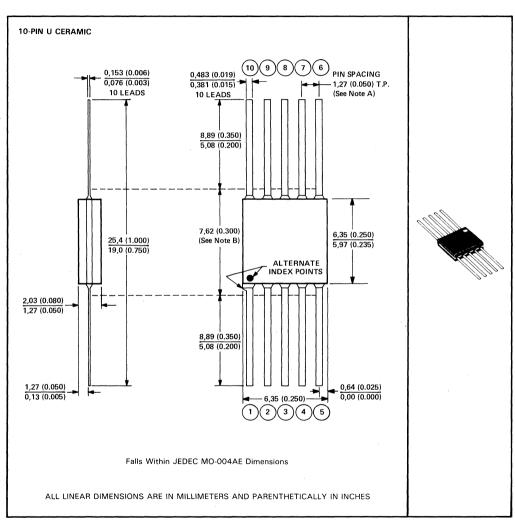
This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62-mm (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in solder assembly.



NOTE: A. Each pin is within 0,13 (0.0005) radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

U ceramic flat package

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

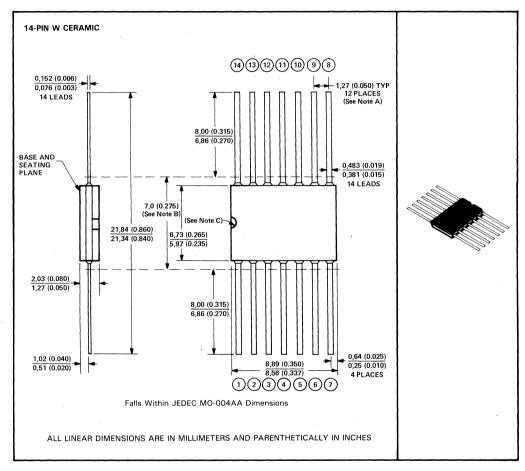


NOTES: A. Leads are within 0.005 radius of true position (T.P.) at maximum material conditions.

B. This dimension determines a zone within which all body and lead irregularities lie.



Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

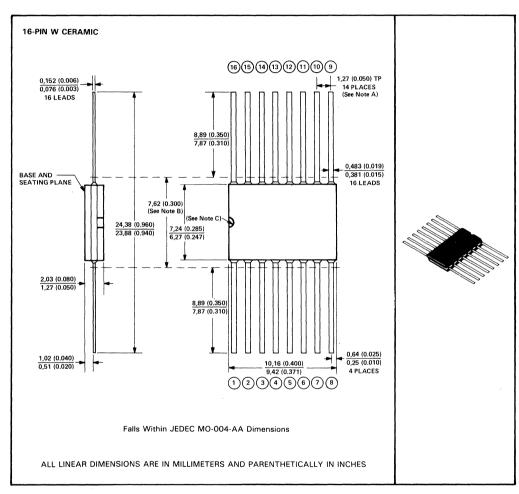


NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.

- B. This dimension determines a zone within which all body and lead irregularities lie.
- C. Index point is provided on cap for terminal identification only.



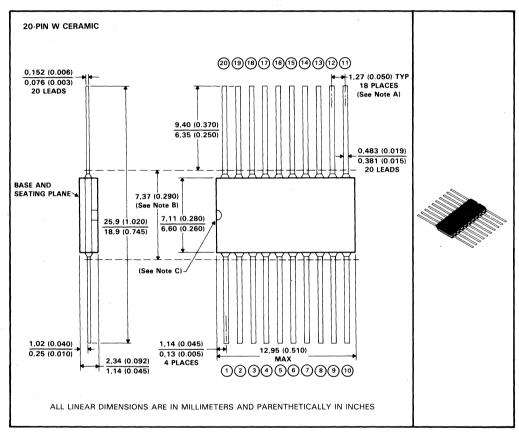
Each of these hermetically sealed flat packages consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
 - B. This dimension determines a zone within which all body and lead irregularities lie.
 - C. Index point is provided on cap for terminal identification only.



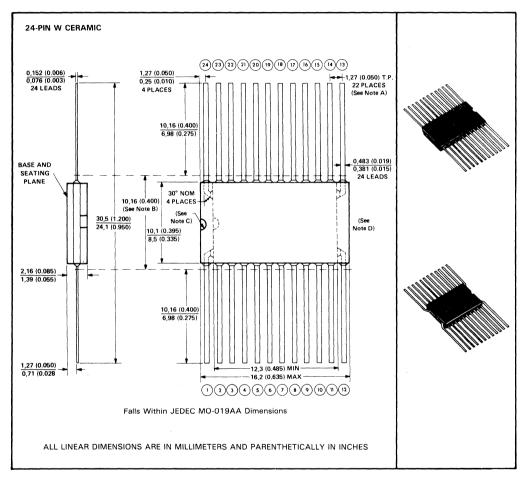
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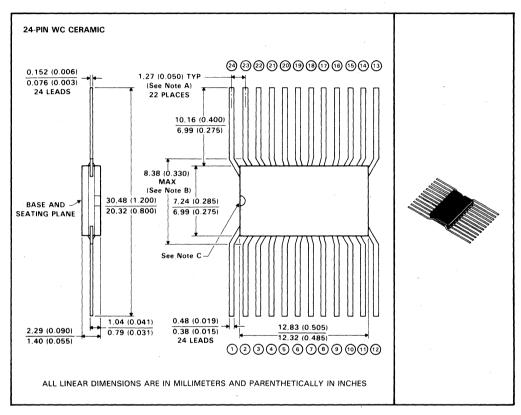
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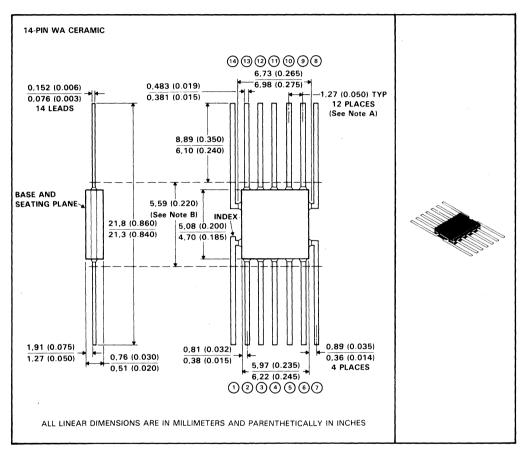


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