TEXAS INSTRUMENTS

Advanced CMOS Logic

Data Book

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1988

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Information contained in this handbook supersedes all data for this technology published by TI in the United States of America before May 1988.

Printed in the U.S.A.
Revised January 1988
Revised May 1988

INTRODUCTION

Benefits of the 1-micron EPIC™ Advanced CMOS Logic (ACL) family (54/74AC/ACT11XXX) from Texas Instruments include:

- Advanced bipolar propagation delays
- Low CMOS power consumption
- 24-mA output drive
- Significant reduction in output voltage noise

Featuring both CMOS- (AC) and TTL- (ACT) compatible functions, the new devices can enhance the performance of high-speed CMOS designs or reduce power requirements in advanced bipolar designs without sacrificing the advantages of either technology.

EPIC™ ACL ensures reliable system operation by reducing simultaneous switching noise, voltage noise generated when multiple outputs are switched. A function of package inductance and the rate of change in current (di/dt), switching noise is of greater concern for ACL than for bipolar designs because of the wider swings of CMOS transistors.

Because the "end-pin" location of power and ground maximizes package inductance, conventionally-packaged ACL creates noise spikes that can lead to the loss of stored data, output glitching, and performance degradation. To ensure system reliability, the designer is forced to use noise-control techniques that detract from system performance, such as adding series resistors to device outputs.

In EPIC™ ACL, power and ground pins have been assigned to package-center to reduce overall package inductance. Combined with a new circuit design technique called OEC™ (Output Edge Control), which softens the edges of the output wave without compromising overall speed, center-pin packaging significantly reduces system-level noise.

TI's EPIC™ ACL family provides the following:

- 50% noise level reduction over end-pin ACL; 10% reduction over advanced bipolar devices
- Flow-through architecture that simplifies design
- Lower design cost due to lower parts count (no space sacrificed to passive components)
- A broad range of over 100 planned functions
- Co-development with Philips/Signetics.

This data book presents pertinent technical information on available EPIC™ ACL devices. In addition, the General Information section contains a functional index of all EPIC™ ACL devices, available or under development, as well as device pinout information for the entire EPIC™ ACL family.

Further information on TI's EPIC™ ACL and other semiconductor products is available from your nearest TI field sales office, local authorized distributor, or by calling Texas Instruments at 1-800-232-3200.

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54AC11027	74AC11027	2-67	1-28
54ACT11027	74ACT11027	2-71	1-28
54AC11030	74AC11030	2-75	1-28
54ACT11030	74ACT11030	2-79	1-28
54AC11032	74AC11032	2-83	1-28
54ACT11032	74ACT11032	2-87	1-28
54AC11034	74AC11034	2-91	1-28
54ACT11034	74ACT11034	2-95	1-28
54AC11074	74AC11074	2-99	1-28
54ACT11074	74ACT11074	2-105	1-28
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†For more information on these devices, contact the factory.

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54ACT11169	74ACT11169	†	1-30
54AC11174	74AC11174	†	1-30
54ACT11174	74ACT11174	†	1-30
54AC11175	74AC11175	†	1-30
54ACT11175	74ACT11175	†	1-30
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54ACT11190	74ACT11190	†	1-30
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54AC11192	74AC11192	†	1-30
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54ACT11251	74ACT11251	†	1-31
54AC11253	74AC11253	†	1-32
54ACT11253	74ACT11253	†	1-32
54AC11257	74AC11257	†	1-32
54ACT11257	74ACT11257	†	1-32
54AC11258	74AC11258	†	1-32
54ACT11258	74ACT11258	†	1-32
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54AC11286	74AC11286	†	1-32
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†For more information on these devices, contact the factory.

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54AC11353	74AC11353	†	1-33
54ACT11353	74ACT11353	†	1-33
54AC11373	74AC11373	2-167	1-33
54ACT11373	74ACT11373	2-173	1-33
54AC11374	74AC11374	2-179	1-33
54ACT11374	74ACT11374	2-185	1-33
54AC11378	74AC11378	†	1-33
54ACT11378	74ACT11378	†	1-33
54AC11379	74AC11379	†	1-33
54ACT11379	74ACT11379	†	1-33
54AC11520	74AC11520	2-191	1-33
54ACT11520	74ACT11520	2-197	1-33
54AC11521	74AC11521	2-203	1-33
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54AC11534	74AC11534	2-223	1-33
54ACT11534	74ACT11534	2-229	1-33
54AC11568	74AC11568	†	1-34
54ACT11568	74ACT11568	†	1-34
54AC11569	74AC11569	†	1-34
54ACT11569	74ACT11569	†	1-34
54AC11579	74AC11579	†	1-34
54ACT11579	74ACT11579	†	1-34
54AC11620	74AC11620	2-235	1-34
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54AC11623	74AC11623	2-247	1-34
54ACT11623	74ACT11623	2-253	1-34
54AC11640	74AC11640	2-259	1-34
54ACT11640	74ACT11640	2-265	1-34
54AC11643	74AC11643	2-269	1-34
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54AC11646	74AC11646	2-279	1-34
54ACT11646	74ACT11646	2-287	1-34
54AC11648	74AC11648	†	1-34
54ACT11648	74ACT11648	†	1-34
54AC11651	74AC11651	†	1-35
54ACT11651	74ACT11651	†	1-35
54AC11652	74AC11652	†	1-35
54ACT11652	74ACT11652	†	1-35
54AC11657	74AC11657	†	1-35
54ACT11657	74ACT11657	†	1-35
54AC11818	74AC11818	†	1-35
54ACT11818	74ACT11818	†	1-35
54AC11819	74AC11819	†	1-35
54ACT11819	74ACT11819	†	1-35
54AC11821	74AC11821	†	1-35
54ACT11821	74ACT11821	†	1-35
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54ACT11822	74ACT11822	†	1-36
54AC11823	74AC11823	†	1-36
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†For more information on these devices, contact the factory.

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54AC11827	74AC11827	†	1-36
54ACT11827	74ACT11827	†	1-36
54AC11828	74AC11828	†	1-37
54ACT11828	74ACT11828	†	1-37
54AC11833	74AC11833	†	1-37
54ACT11833	74ACT11833	†	1-37
54AC11834	74AC11834	†	1-37
54ACT11834	74ACT11834	†	1-37
54AC11841	74AC11841	†	1-37
54ACT11841	74ACT11841	†	1-37
54AC11842	74AC11842	†	1-37
54ACT11842	74ACT11842	†	1-37
54AC11843	74AC11843	†	1-37
54ACT11843	74ACT11843	†	1-37
54AC11844	74AC11844	†	1-38
54ACT11844	74ACT11844	†	1-38
54AC11845	74AC11845	†	1-38
54ACT11845	74ACT11845	†	1-38
54AC11846	74AC11846	†	1-38
54ACT11846	74ACT11846	†	1-38
54AC11853	74AC11853	†	1-38
54ACT11853	74ACT11853	†	1-38
54AC11854	74AC11854	†	1-38
54ACT11854	74ACT11854	†	1-38
54AC11861	74AC11861	†	1-38
54ACT11861	74ACT11861	†	1-38
54AC11862	74AC11862	†	1-39
54ACT11862	74ACT11862	†	1-39
54AC11863	74AC11863	†	1-39
54ACT11863	74ACT11863	†	1-39
54AC11864	74AC11864	†	1-39
54ACT11864	74ACT11864	†	1-39
54AC11873	74AC11873	†	1-39
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54ACT11874	74ACT11874	†	1-39
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†For more information on these devices, contact the factory.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**
The internal capacitance at an input of the device.

C_o **Output capacitance**
The internal capacitance at an output of the device.

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):
$P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

ΔI_{CC} **Supply current change (ACT devices only)**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

*Current out of a terminal is given as a negative value.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.
NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a three-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).
NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{G}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them, $t_{en} = t_{PHL}$.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic elelment according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{+}.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

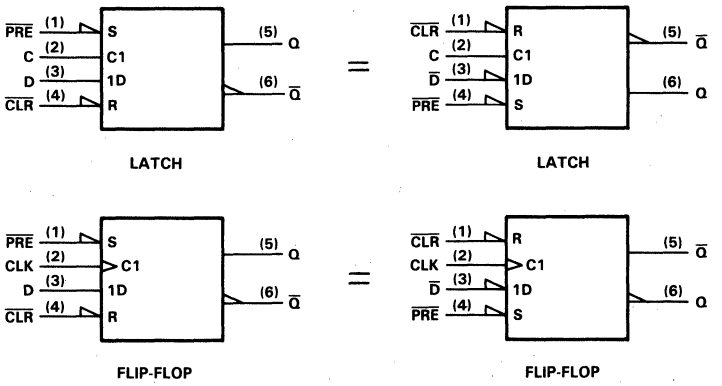
The function table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



The figures show that when Q and $\overline{Q}$ exchange names, the Preset and Clear pins also exchange names. The polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

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In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_J = R_{\theta JA} \times P_T + T_A \qquad (1)$$

where

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY

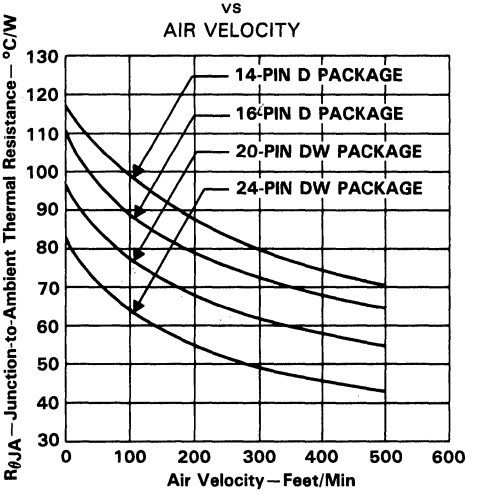

FIGURE 1

$$P_T = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \qquad (2)$$

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o) \qquad (3)$$

where

V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum) see Note 1
I_{CC} = quiescent supply current (specified on device data sheet)
C_{pd} = Power dissipation capacitance (from the device data sheet)
f_i = input frequency
C_L = output load capacitance
f_o = output frequency
N = number of inputs drivenf by a TTL device
dc = duty cycle
ΔI_{CC} = increase in supply current (specified on device data sheet)

NOTE 1: In system applications I_{CC} can be minimized by keeping input voltage levels less than 1 V for V_{IL} and greater than $V_{CC} - 1$ V for V_{IH} and input rise and fall times less than 15 ns.

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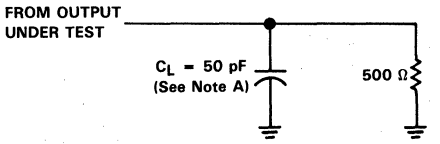
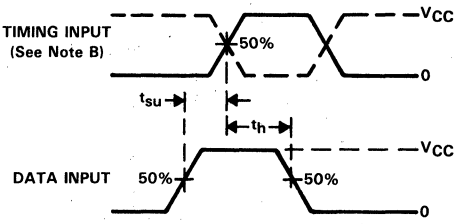
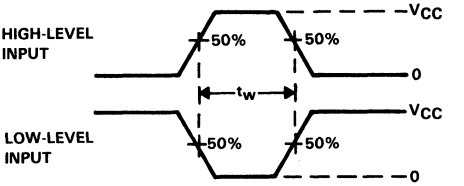
SERIES 54AC11XXX AND 74AC11XXX DEVICES



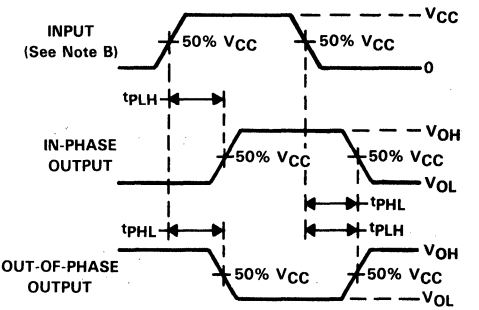
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



SETUP AND HOLD TIMES



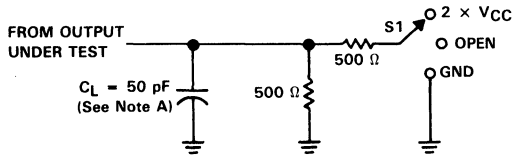
PULSE DURATION



PROPAGATION DELAY TIMES

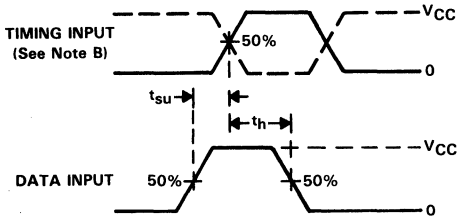
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. The outputs are measured one at a time with one input transition per measurement.

SERIES 54AC11XXX AND 74AC11XXX DEVICES

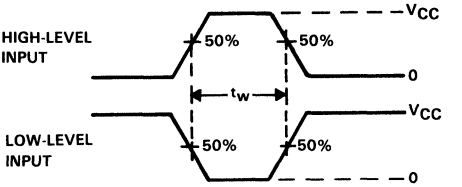


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

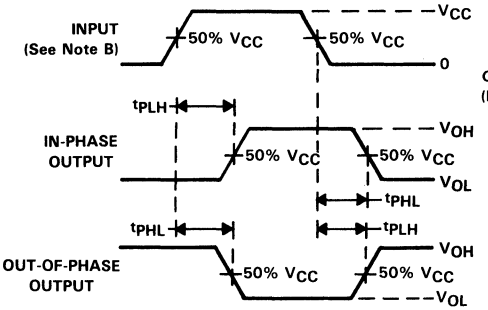
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



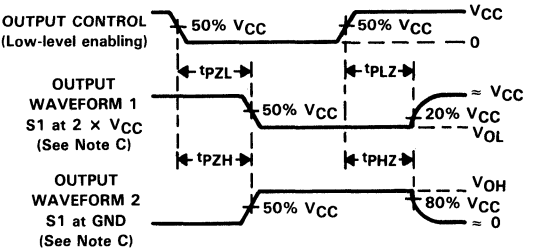
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

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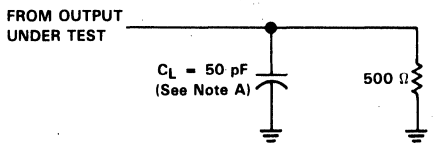
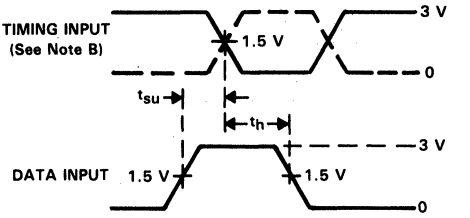
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

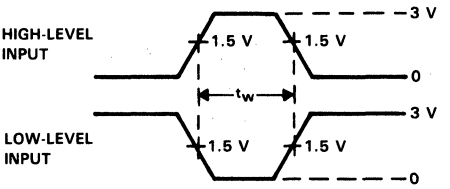
SERIES 54ACT11XXX AND 74ACT11XXX DEVICES



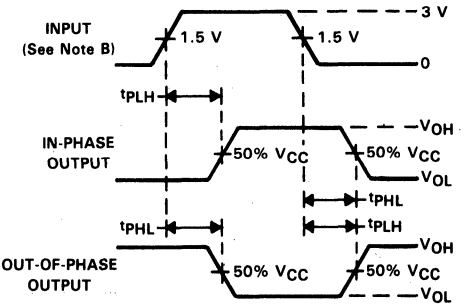
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

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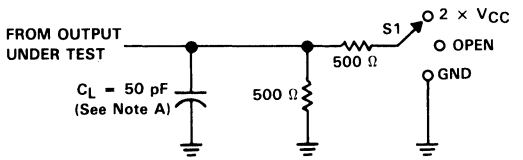
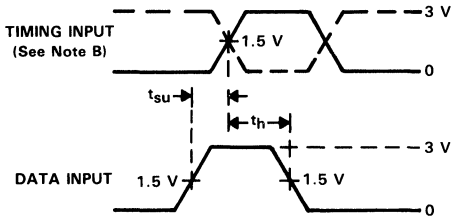
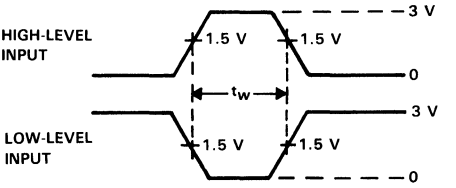


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

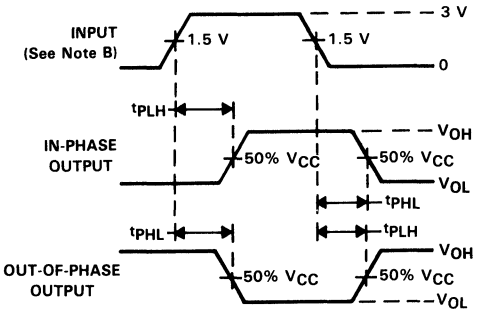
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



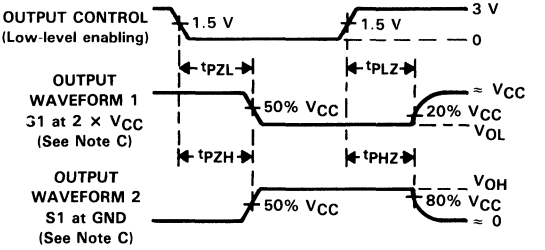
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

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D. The outputs are measured one at a time with one input transition per measurement.

GATES AND INVERTERS WITH TWO-STATE OUTPUTS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Hex inverter	004	●	●
Hex noninverter	034	●	●
Triple 3-input gate	010	●	●
Dual 4-input gate	020	●	●
8-input gate	030	●	●

POSITIVE-AND GATES

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Quadruple 2-input gate	008	●	●
Triple 3-input gate	011	●	●
Dual 4-input gate	021	●	●

POSITIVE-NOR GATES

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Quadruple 2-input gate	002	●	●
Triple 3-input gate	027	●	●

POSITIVE-OR GATES

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Quadruple 2-input gate	032	●	●

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Hex inverter	014	▲	▲
Dual 4-input positive NAND	013	▲	▲
Quadruple 2-input positive NAND	132	▲	▲

● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

BUFFERS, DRIVERS, AND TRANSCEIVERS WITH THREE-STATE OUTPUTS

BUFFERS, DRIVERS, AND TRANSCEIVERS

DESCRIPTION	# of BITS	TYPE	AVAILABILITY	
			AC	ACT
Noninverting buffer/driver	10	827	▲	▲
	8	241	●	●
	8	244	●	●
Inverting buffer/driver	10	828	▲	▲
	8	240	●	●
Noninverting transceiver	10	861	▲	▲
	9	863	▲	▲
Inverting transceiver	10	862	▲	▲
	9	864	▲	▲

8-BIT BIDIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Noninverting	245	●	●
	623	▲	▲
	652	▲	▲
Inverting	620	▲	▲
	651	▲	▲
	640	▲	●
Inverting and noninverting	643	▲	▲
Noninverting registered	646	▲	▲
Inverting registered	648	▲	▲
Noninverting with parity	657	▲	▲
Noninverting registered	833	▲	▲
Inverting registered	834	▲	▲
Noninverting latched	853	▲	▲
Inverting latched	854	▲	▲

● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS WITH ASYNC CLEAR AND PRESET

DESCRIPTION	TYPE	CLOCK EDGE	AVAILABILITY	
			AC	ACT
Dual J-K edge triggered	109	POS	●	●
	112	NEG	▲	▲
Dual D-type	074	POS	●	●

QUAD AND HEX FLIP-FLOPS WITH POSITIVE CLOCK EDGE

DESCRIPTION	OUTPUT	# of F:F	CLEAR	TYPE	AVAILABILLITY	
					AC	ACT
D-type	Q	6	ASYNC	174	▲	▲
	Q	6	–	378	▲	▲
	Q,$\overline{Q}$	4	ASYNC	175	▲	▲
	Q,$\overline{Q}$	4	–	379	▲	▲

8-, 9-, and 10-BIT D-TYPE FLIP-FLOPS WITH THREE-STATE OUTPUTS

DESCRIPTION	# OF BITS	CLEAR	CLOCK EDGE	TYPE	AVAILABILITY	
					AC	ACT
Noninverting	8	–	POS	374	●	●
Noninverting dual 4-bit	8	ASYNC	POS	874	▲	▲
Inverting	8	–	POS	534	●	●
Noninverting	8	ASYNC	POS	825	▲	▲
Inverting	8	ASYNC	POS	826	▲	▲
Noninverting	9	ASYNC	POS	823	▲	▲
Inverting	9	ASYNC	POS	824	▲	▲
Noninverting	10	–	POS	821	▲	▲
Inverting	10	–	POS	822	▲	▲

● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

COUNTERS AND LATCHES

SYNCHRONOUS COUNTERS WITH POSITIVE-EDGE CLOCK

DESCRIPTION	# OF BITS	OUTPUT	CLEAR	PARALLEL LOAD	TYPE	AVAILABILITY	
						AC	ACT
Decade	4	TOTEM-POLE	ASYNC	SYNC	160	▲	▲
	4	TOTEM-POLE	SYNC	SYNC	162	▲	▲
Decade up/down	4	TOTEM-POLE	–	SYNC	168	▲	▲
	4	TOTEM-POLE	–	ASYNC	190	▲	▲
	4	TOTEM-POLE	ASYNC	ASYNC	192	▲	▲
	4	TOTEM-POLE	BOTH	SYNC	568	▲	▲
Binary	4	TOTEM-POLE	ASYNC	SYNC	161	▲	▲
	4	TOTEM-POLE	SYNC	SYNC	163	▲	▲
Binary up/down	4	TOTEM-POLE	–	SYNC	169	▲	▲
	4	TOTEM-POLE	–	ASYNC	191	▲	▲
	4	TOTEM-POLE	ASYNC	ASYNC	193	▲	▲
	4	3-STATE	BOTH	SYNC	569	▲	▲
Bidirectional binary	8	TOTEM-POLE	–	SYNC	269	▲	▲
	8	3-STATE	BOTH	SYNC (I/O)	579	▲	▲

8-, 9-, AND 10-BIT LATCHES WITH THREE-STATE OUTPUTS

DESCRIPTION	# OF BITS	CLEAR	PRESET	TYPE	AVAILABILITY	
					AC	ACT
Transparent	8	–	–	373	●	●
Noninverting dual 4-bit	8	X	–	873	▲	▲
Inverting	8	–	–	533	●	●
Noninverting	8	X	X	845	▲	▲
Inverting	8	X	X	846	▲	▲
Noninverting	9	X	X	843	▲	▲
Inverting	9	X	X	844	▲	▲
Noninverting	10	–	–	841	▲	▲
Inverting	10	–	–	842	▲	▲

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DATA SELECTORS/MULTLIPLEXERS AND DECODERS/DEMULTIPLEXERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	OUTPUT	TYPE	AVAILABILITY	
			AC	ACT
8-to-1	TOTEM-POLE	151	▲	▲
	3-STATE	251	▲	▲
Dual 4-to-1	TOTEM-POLE	153	▲	▲
	3-STATE	253	▲	▲
	TOTEM-POLE	352	▲	▲
	TOTEM-POLE	353	▲	▲
Quad 2-to-1	TOTEM-POLE	157	▲	▲
	TOTEM-POLE	158	▲	▲
	3-STATE	257	▲	▲
	3-STATE	258	▲	▲

DECODERS/DEMULTIPLEXERS WITH TWO-STATE OUTPUTS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
3-to-8	138	▲	▲
Dual 2-to-4	139	▲	▲
3-to-8	238	●	▲
Dual 2-to-4	239	▲	▲

● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

REGISTERS WITH POSITIVE-CLOCK EDGE

SHIFT REGISTERS

DESCRIPTION	OUTPUT	# OF BITS	MODES					TYPE	AVAILABILITY	
			SR	SL	LOAD	HOLD	CLEAR		AC	ACT
Parallel in	3-STATE	8	X	X	X	X	ASYNC	299	▲	▲
Parallel out	3-STATE	8	X	X	X	X	SYNC	323	▲	▲
Bidirectional	TOTEM-POLE	4	X	X	X	X	ASYNC	194	▲	▲

OTHER REGISTERS

DESCRIPTION	OUTPUT	# OF BITS	MODES					TYPE	AVAILABILITY	
			SR	SL	LOAD	HOLD	CLEAR		AC	ACT
Universal	3-STATE	8	X	X	X	X	ASYNC	299	▲	▲
	3-STATE	8	X	X	X	X	SYNC	323	▲	▲
Diagnostic/pipeline	3-STATE	8	X	–	–	–	–	818	▲	▲
818 w/parity	3-STATE	8	X	–	–	–	–	819	▲	▲

● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

ARITHMETIC LOGIC UNITS, COMPARATORS, AND PARITY GENERATORS/CHECKERS

ARITHMETIC LOGIC UNITS AND LOOK-AHEAD CARRY GENERATORS

DESCRIPTION	OUTPUT	TYPE	AVAILABILITY	
			AC	ACT
4-bit ALU/function generator	TOTEM-POLE	181	▲	▲
	TOTEM-POLE	881	▲	▲
32-bit look-ahead carry generator	TOTEM-POLE	882	▲	▲

COMPARATORS WITH TWO-STATE OUTPUTS

DESCRIPTION	# BITS	$\overline{P=Q}$	$P=Q$	$\overline{P>Q}$	$P>Q$	$P<Q$	TYPE	AVAILABILITY	
								AC	ACT
20-kΩ pull-up	8	NO	YES	NO	NO	NO	520	●	●
Standard	8	NO	YES	NO	NO	NO	521	●	●

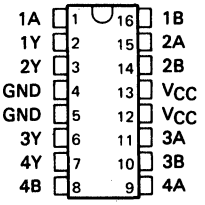
9-BIT PARITY GENERATORS/CHECKERS WITH TWO-STATE OUTPUTS

DESCRIPTION	TYPE	AVAILABILITY	
		AC	ACT
Odd/Even parity Generators/Checkers	280	▲	▲
	286	▲	▲

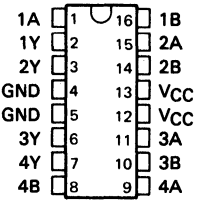
● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

EPIC™ ACL PINOUTS

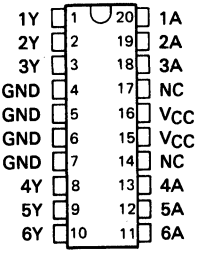
'AC11000, 'ACT11000
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
(TOP VIEW)



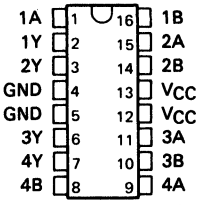
'AC11002, 'ACT11002
QUADRUPLE 2-INPUT POSITIVE-NOR GATES
(TOP VIEW)



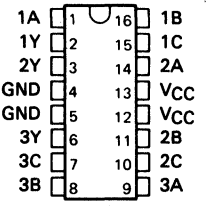
'AC11004, 'ACT11004
HEX INVERTERS
(TOP VIEW)



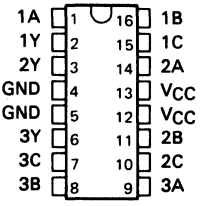
'AC11008, 'ACT11008
QUADRUPLE 2-INPUT POSITIVE-AND GATES
(TOP VIEW)



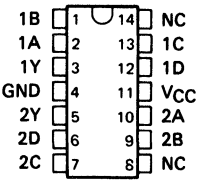
'AC11010, 'ACT11010
TRIPLE 3-INPUT POSITIVE-NAND GATES
(TOP VIEW)



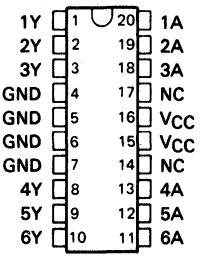
'AC11011, 'ACT11011
TRIPLE 3-INPUT POSITIVE-AND GATES
(TOP VIEW)



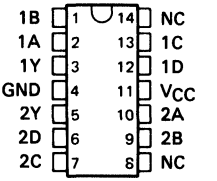
'AC11013, 'ACT11013
DUAL 4-INPUT GATES
(TOP VIEW)



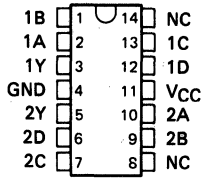
'AC11014, 'ACT11014
HEX INVERTERS
(TOP VIEW)



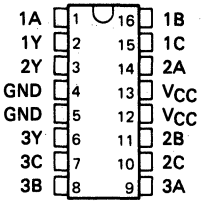
'AC11020, 'ACT11020
DUAL 4-INPUT POSITIVE-NAND GATES
(TOP VIEW)



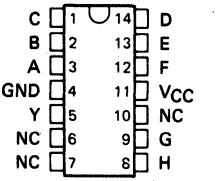
'AC11021, 'ACT11021
DUAL 4-INPUT POSITIVE-AND GATES
(TOP VIEW)



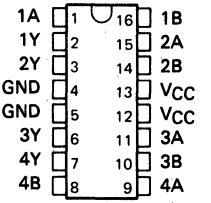
'AC11027, 'ACT11027
TRIPLE 3-INPUT POSITIVE-NOR GATES
(TOP VIEW)



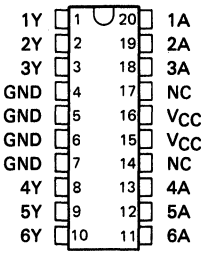
'AC11030, 'ACT11030
8-INPUT POSITIVE-NAND GATES
(TOP VIEW)



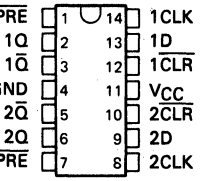
'AC11032, 'ACT11032
QUADRUPLE 2-INPUT POSITIVE-OR GATES
(TOP VIEW)



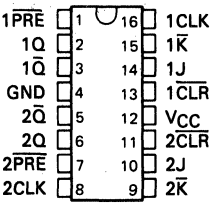
'AC11034, 'ACT11034
HEX NONINVERTERS
(TOP VIEW)



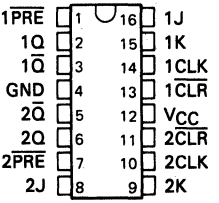
'AC11074, 'ACT11074
DUAL D-TYPE POSITIVE-EDGE TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



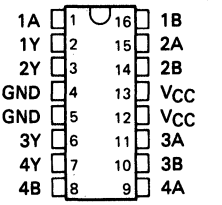
'AC11109, 'ACT11109
DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



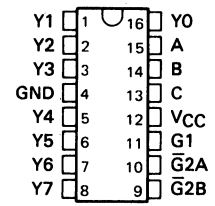
'AC11112, 'ACT11112
DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



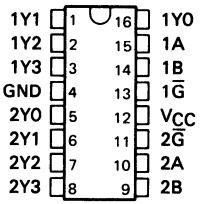
'AC11132, 'ACT11132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS
(TOP VIEW)



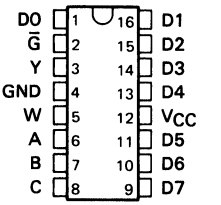
'AC11138, 'ACT11138
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
(TOP VIEW)



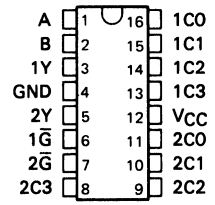
'AC11139, 'ACT11139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS
(TOP VIEW)



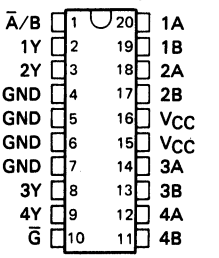
'AC11151, 'ACT11151
1 OF 8 DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



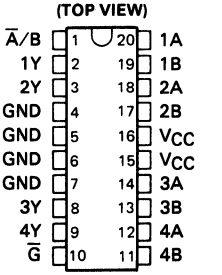
'AC11153, 'ACT11153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



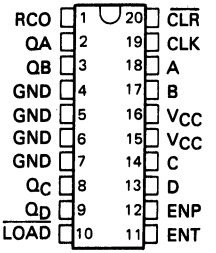
'AC11157, 'ACT11157
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



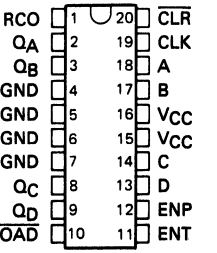
'AC11158, 'ACT11158
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



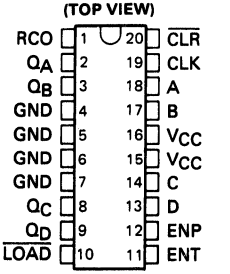
'AC11160, 'ACT11160
SYNCHRONOUS 4-BIT BINARY COUNTERS
(TOP VIEW)



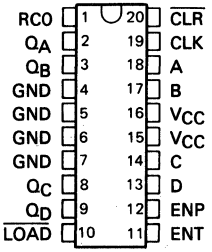
'AC11161, 'ACT11161
SYNCHRONOUS 4-BIT DECADE COUNTERS
(TOP VIEW)



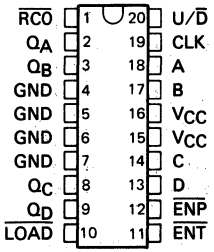
'AC11162, 'ACT11162
SYNCHRONOUS 4-BIT BINARY COUNTERS
(TOP VIEW)



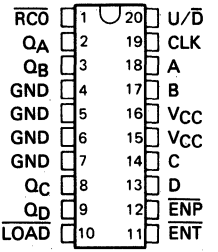
'AC11163, 'ACT11163
SYNCHRONOUS 4-BIT DECADE COUNTERS
(TOP VIEW)



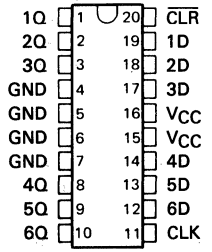
'AC11168, 'ACT11168
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS
(TOP VIEW)



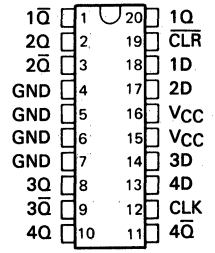
'AC11169, 'ACT11169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS
(TOP VIEW)



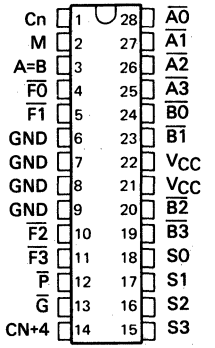
'AC11174, 'ACT11174
HEX D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)



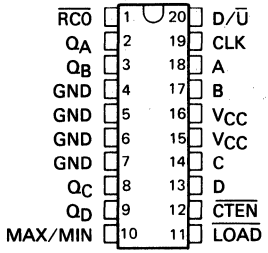
'AC11175, 'ACT11175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)



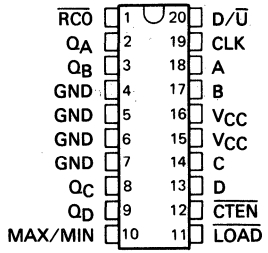
'AC11181, 'ACT11181
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(TOP VIEW)



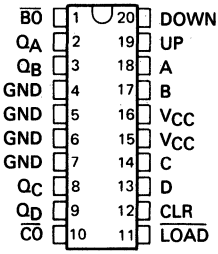
'AC11190, 'ACT11190
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS
(TOP VIEW)



'AC11191, 'ACT11191
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS
(TOP VIEW)



'AC11192, 'ACT11192
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)
(TOP VIEW)



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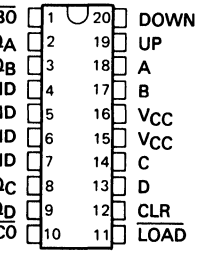
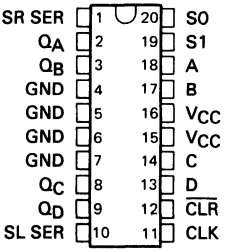
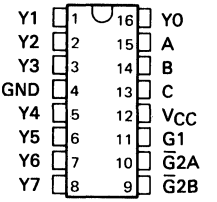
'AC11193, 'ACT11193
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS (DUAL CLOCK WITH CLEAR)
(TOP VIEW)



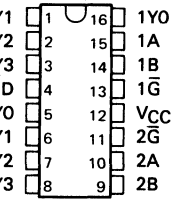
'AC11194, 'ACT11194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS
(TOP VIEW)



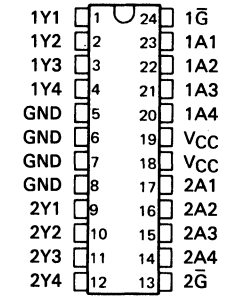
'AC11238, 'ACT11238
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
(TOP VIEW)



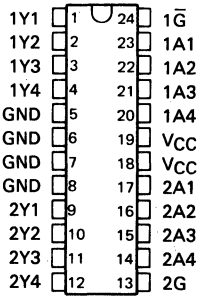
'AC11239, 'ACT11239
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS
(TOP VIEW)



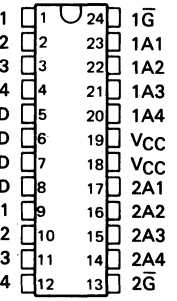
'AC11240, 'ACT11240
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



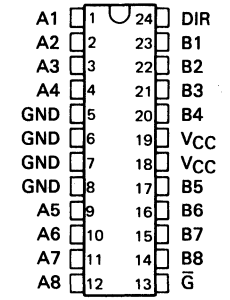
'AC11241, 'ACT11241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



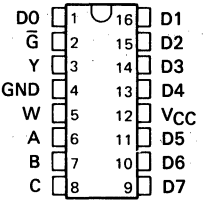
'AC11244, 'ACT11244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



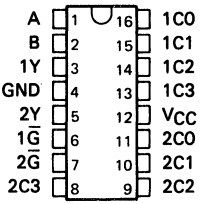
'AC11245, 'ACT11245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



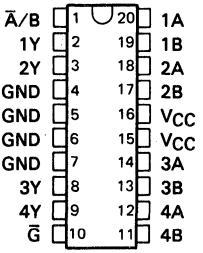
'AC11251 'ACT11251
1 OF 8 DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



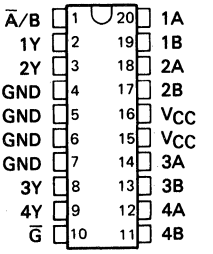
'AC11253, 'ACT11253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



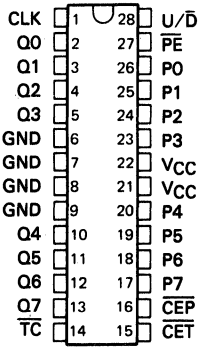
'AC11257, 'ACT11257
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



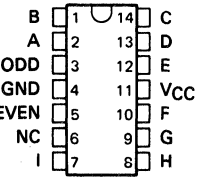
'AC11258, 'ACT11258
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



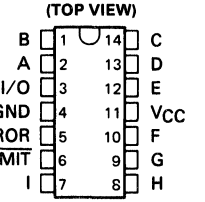
'AC11269, 'ACT11269
8-BIT BIDIRECTIONAL BINARY COUNTER
(TOP VIEW)



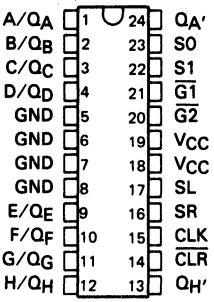
'AC11280, 'ACT11280
9-BIT PARITY GENERATORS/CHECKERS
(TOP VIEW)



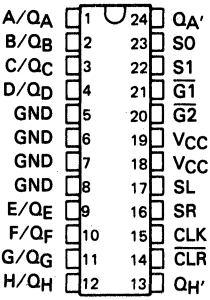
'AC11286, 'ACT11286
9-BIT PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT
(TOP VIEW)



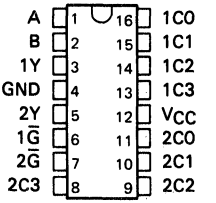
'AC11299, 'ACT11299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11323, 'ACT11323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11352 'ACT11352
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



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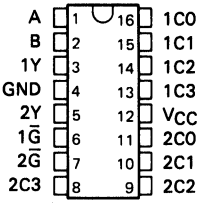
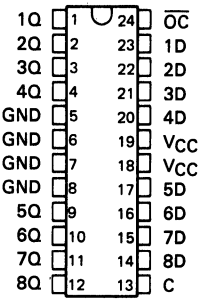
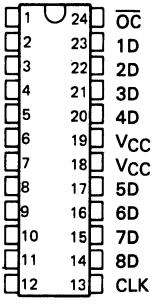
'AC11353, 'ACT11353
DUAL 1 OF 4 DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



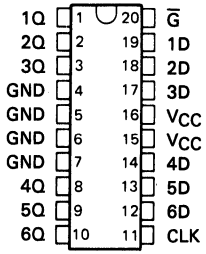
'AC11373, 'ACT11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



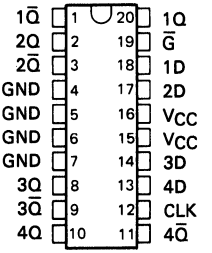
'AC11374, 'ACT11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)



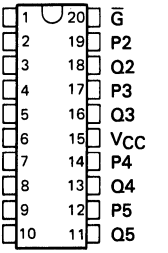
'AC11378, 'ACT11378
HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE
(TOP VIEW)



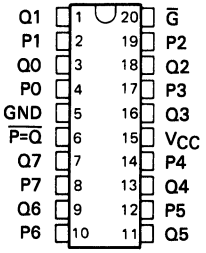
'AC11379, 'ACT11379
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)



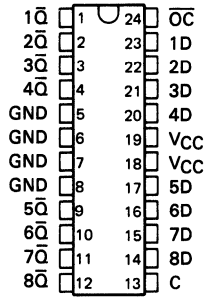
'AC11520, 'ACT11520
8-BIT IDENTITY COMPARATOR
(TOP VIEW)



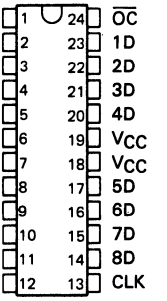
'AC11521, 'ACT11521
8-BIT IDENTITY COMPARATOR
(TOP VIEW)



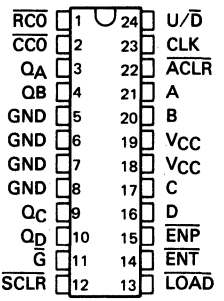
'AC11533, 'ACT11533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUT
(TOP VIEW)



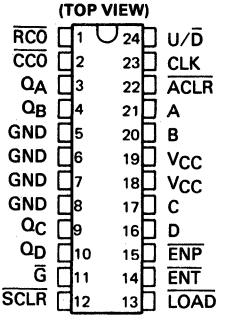
'AC11534, 'ACT11534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUT
(TOP VIEW)



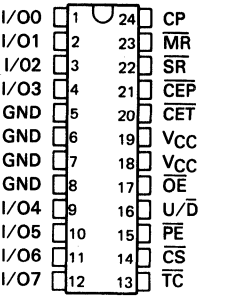
'AC11568, 'ACT11568
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



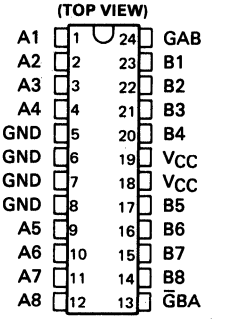
'AC11569, 'ACT11569
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



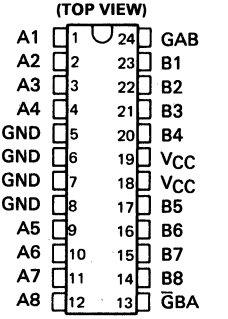
'AC11579, 'ACT11579
8-BIT BIDIRECTIONAL BINARY COUNTER WITH 3-STATE OUTPUTS
(TOP VIEW)



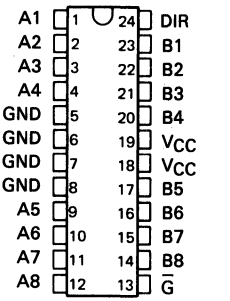
'AC11620, 'ACT11620
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



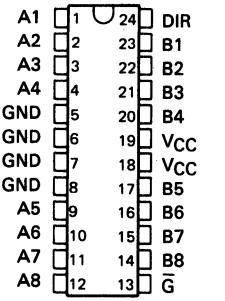
'AC11623, 'ACT11623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



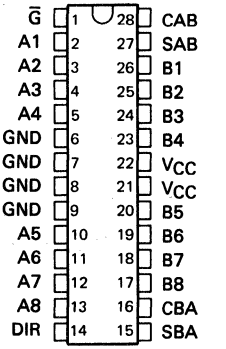
'AC11640, 'ACT11640
OCTAL BUS TRANSCEIVERS
(TOP VIEW)



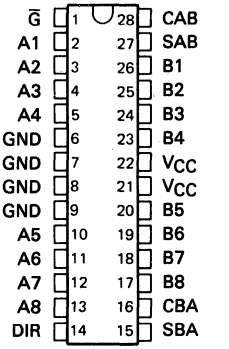
'AC11643, 'ACT11643
OCTAL BUS TRANSCEIVERS
(TOP VIEW)



'AC11646, 'ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



'AC11648, 'ACT11648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



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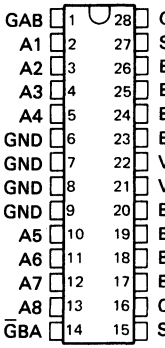
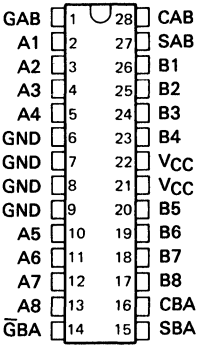
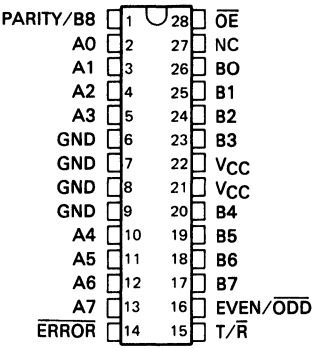
'AC11651, 'ACT11651
OCTAL BUS TRANSCEIVERS AND REGISTERS
(TOP VIEW)



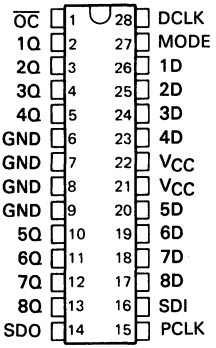
'AC11652, 'ACT11652
OCTAL BUS TRANSCEIVERS AND REGISTERS
(TOP VIEW)



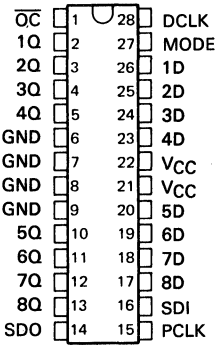
'AC11657, 'ACT11657
OCTAL BIDIRECTIONAL TRANSCEIVERS WITH 8-BIT PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS
(TOP VIEW)



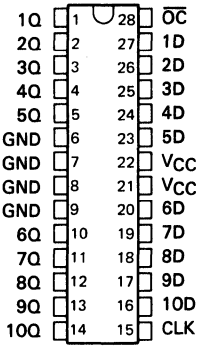
'AC11818, 'ACT11818
DIAGNOSTIC/PIPELINE REGISTER
(TOP VIEW)



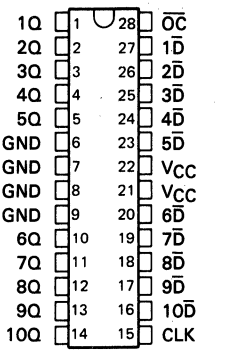
'AC11819, 'ACT11819
DIAGNOSTIC/PIPELINE REGISTER
(TOP VIEW)



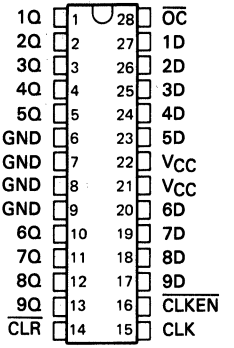
'AC11821, 'ACT11821
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



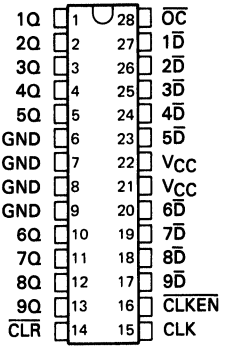
'AC11822, 'ACT11822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



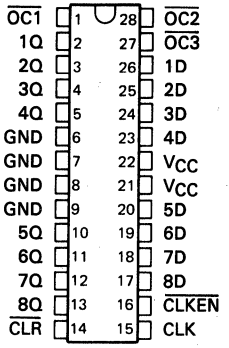
'AC11823, 'ACT11823
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



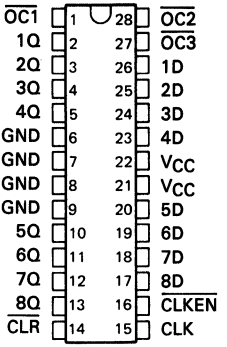
'AC11824, 'ACT11824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



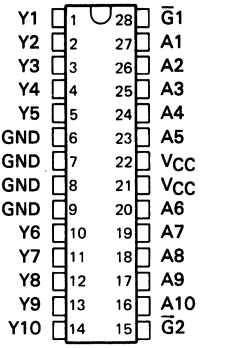
'AC11825, 'ACT11825
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



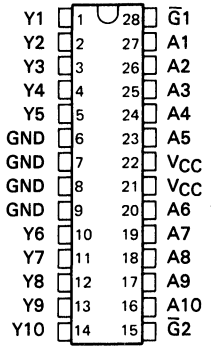
'AC11826, 'ACT11826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



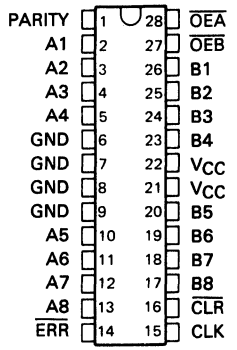
'AC11827, 'ACT11827
10-BIT BUFFERS WITH 3-STATE OUTPUTS
(TOP VIEW)



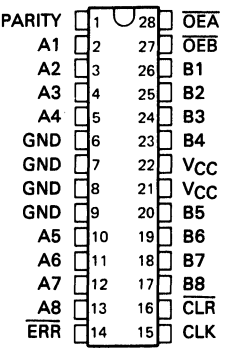
'AC11828, 'ACT11828
10-BIT BUFFERS WITH 3-STATE OUTPUTS
(TOP VIEW)



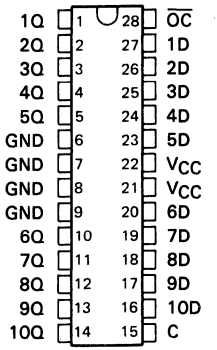
'AC11833, 'ACT11833
PARITY BUS TRANSCEIVERS
(TOP VIEW)



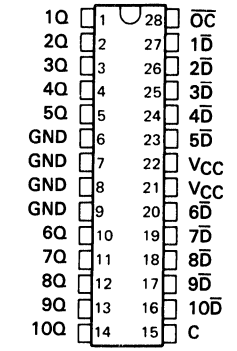
'AC11834, 'ACT11834
PARITY BUS TRANSCEIVERS
(TOP VIEW)



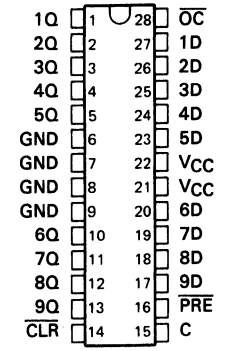
'AC11841, 'ACT11841
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



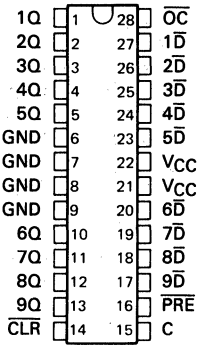
'AC11842, 'ACT11842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



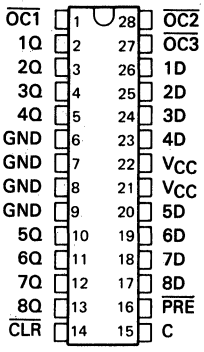
'AC11843, 'ACT11843
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



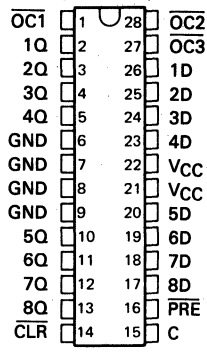
'AC11844, 'ACT11844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



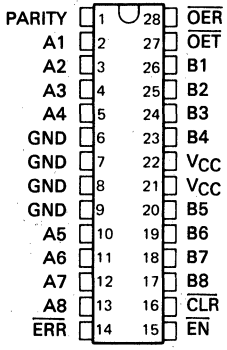
'AC11845, 'ACT11845
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



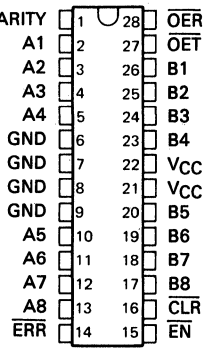
'AC11846, 'ACT11846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



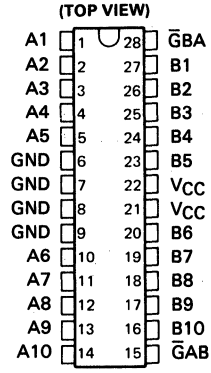
'AC11853, 'ACT11853
PARITY BUS TRANSCEIVERS
(TOP VIEW)



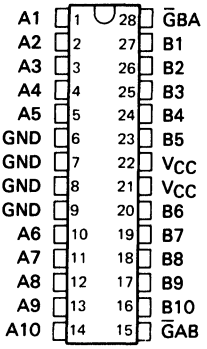
'AC11854, 'ACT11854
PARITY BUS TRANSCEIVERS
(TOP VIEW)



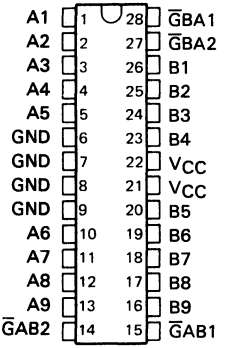
'AC11861, 'ACT11861
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



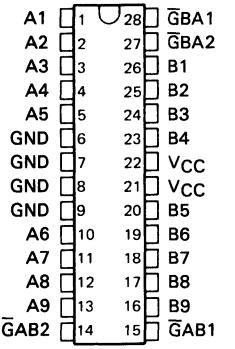
'AC11862, 'ACT11862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



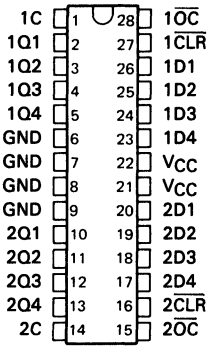
'AC11863, 'ACT11863
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



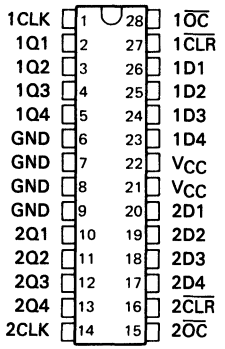
'AC11864, 'ACT11864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



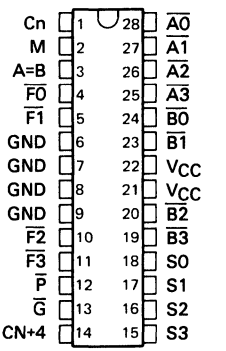
'AC11873, 'ACT11873
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



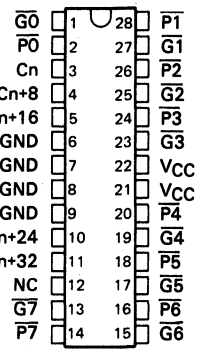
'AC11874, 'ACT11874
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)



'AC11881, 'ACT11881
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(TOP VIEW)



'AC11882, 'ACT11882
32-BIT LOOK-AHEAD CARRY GENERATORS
(TOP VIEW)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TEXAS INSTRUMENTS
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D2957, APRIL 1987

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

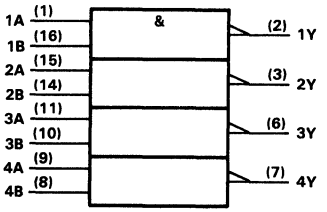
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54AC11000 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11000 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

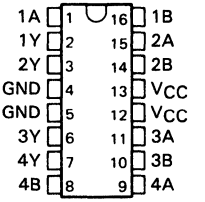
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

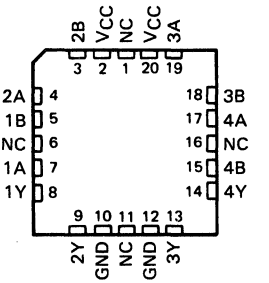


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11000 . . . J PACKAGE
74AC11000 . . . D OR N PACKAGE
(TOP VIEW)

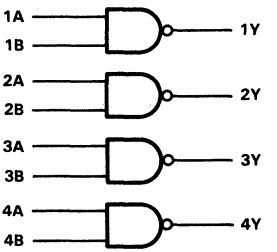


54AC11000 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11000			74AC11000			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11000		74AC11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

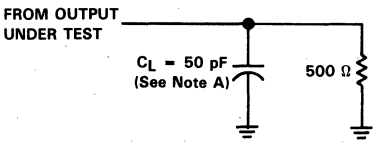
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11000		74AC11000		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3.3 ±0.3 V	1.5	7.2	9.8	1.5	11.9	1.5	11.1	ns
			5 ±0.5 V	1.5	5	6.5	1.5	8.1	1.5	7.4	
t_{PHL}			3.3 ±0.3 V	1.5	5.8	8.6	1.5	10.2	1.5	9.6	
			5 ±0.5 V	1.5	4.4	6.1	1.5	7.3	1.5	6.8	

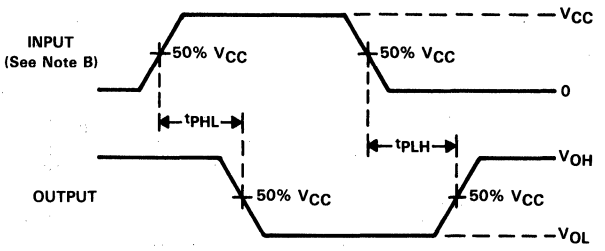
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	33	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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D2957, JUNE 1987

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

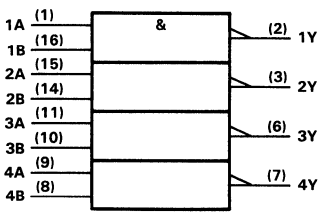
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54ACT11000 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11000 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

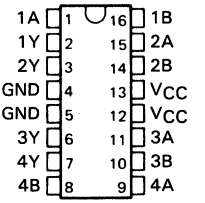
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

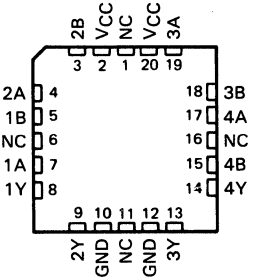


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11000 . . . J PACKAGE
74ACT11000 . . . D OR N PACKAGE
(TOP VIEW)

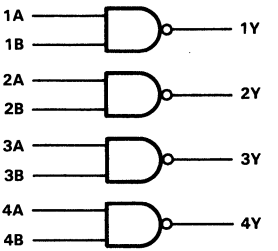


54ACT11000 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11000		74ACT11000		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11000		74ACT11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

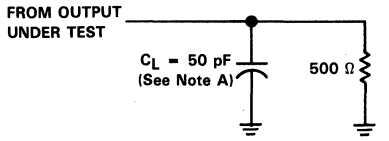
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11000		74ACT11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	7.2	10.9	1.5	13.3	1.5	12.3	ns
t_{PHL}			1.5	5.8	8	1.5	9.5	1.5	8.8	

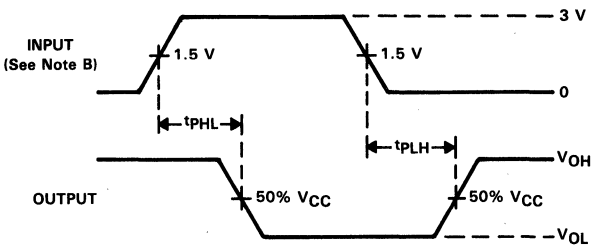
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2957, JUNE 1987—REVISED OCTOBER 1987

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

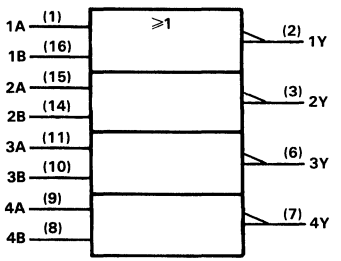
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54AC11002 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11002 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

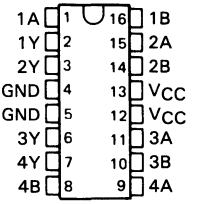
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

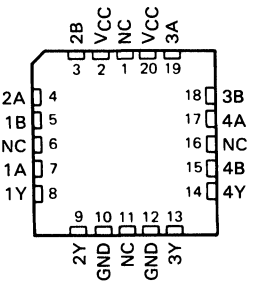


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11002 . . . J PACKAGE
74AC11002 . . . D OR N PACKAGE
(TOP VIEW)

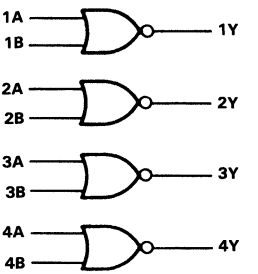


54AC11002 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11002			74AC11002			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11002		74AC11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_I	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

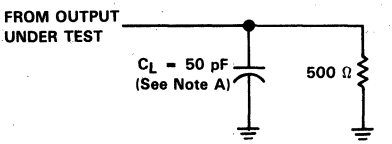
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11002		74AC11002		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3.3 ±0.3 V	1.5	7	8.6	1.5	10.7	1.5	9.9	ns
			5 ±0.5 V	1.5	4.5	6.1	1.5	7.4	1.5	6.9	
t_{PHL}			3.3 ±0.3 V	1.5	6	7.5	1.5	9	1.5	8.4	
			5 ±0.5 V	1.5	4	5.7	1.5	6.8	1.5	6.4	

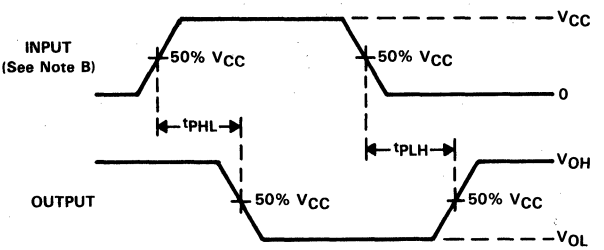
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2957, JUNE 1987

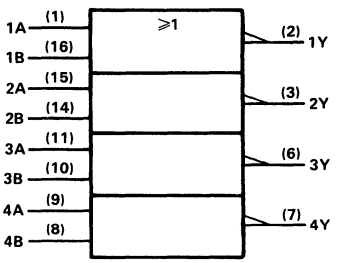
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A + B}$ in positive logic.

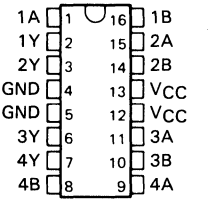
The 54ACT11002 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11002 is characterized for operation from −40°C to 85°C.

logic symbol†

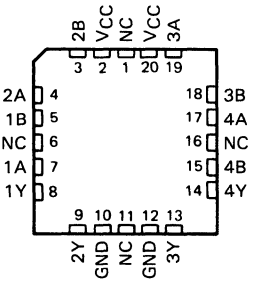


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11002 . . . J PACKAGE
74ACT11002 . . . D OR N PACKAGE
(TOP VIEW)

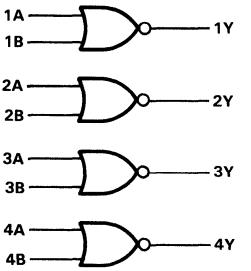


54ACT11002 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11002		74ACT11002		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11002		74ACT11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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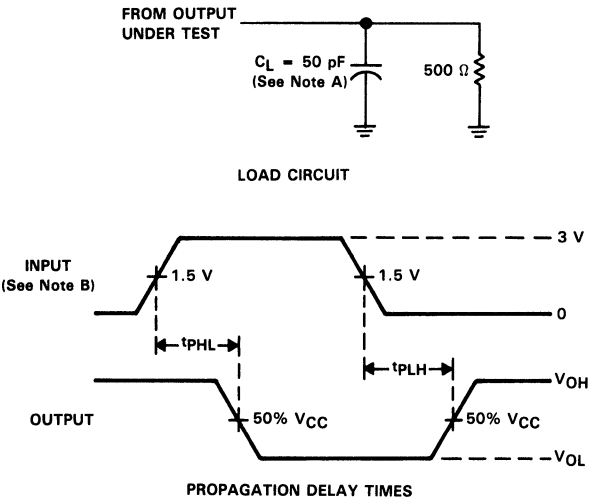
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11002		74ACT11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.1	9.4	1.5	11.3	1.5	10.6	ns
t_{PHL}			1.5	5.3	7.8	1.5	9.3	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, FEBRUARY 1988

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

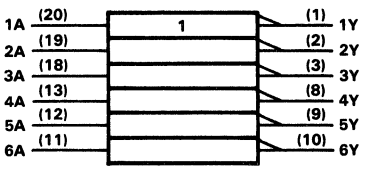
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The 54AC11004 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11004 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

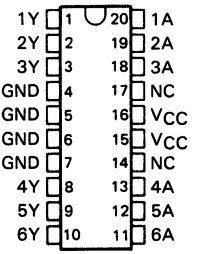
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

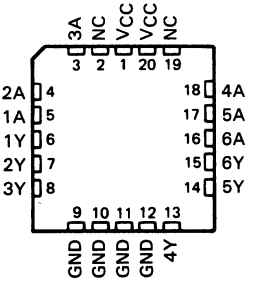


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

54AC11004 . . . J PACKAGE
74AC11004 . . . DW OR N PACKAGE
(TOP VIEW)

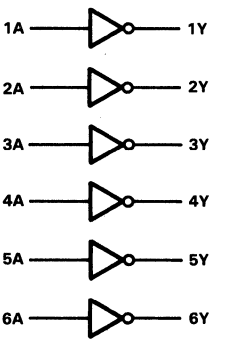


54AC11004 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±150 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11004			74AC11004			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11004		74AC11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

V_{CC} = 3.3 V ± 0.3 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11004			74AC11004			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1.5	6.1	9	1.5		10.4	1.5		10	ns
t_{PHL}			1.5	5.2	7.4	1.5		8.9	1.5		8.2	

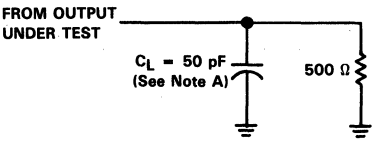
V_{CC} = 5 V ± 0.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11004			74AC11004			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1.5	4.2	6.3	1.5		7.5	1.5		7.1	ns
t_{PHL}			1.5	3.8	5.5	1.5		6.4	1.5		6	

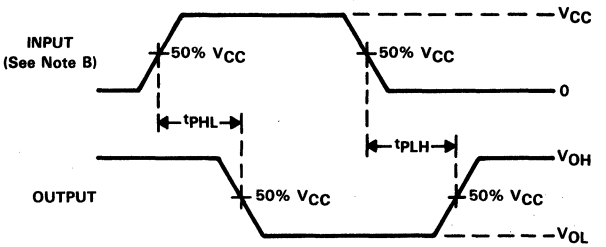
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF,	f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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D2957, JANUARY 1988

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

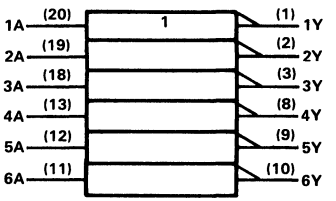
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The 54ACT11004 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11004 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

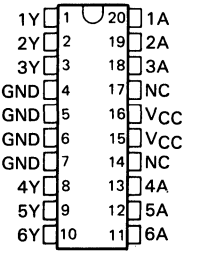
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

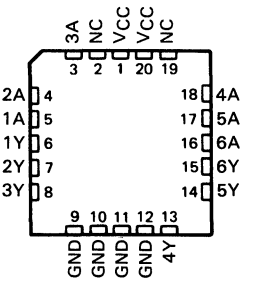


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

54ACT11004 . . . J PACKAGE
74ACT11004 . . . DW OR N PACKAGE
(TOP VIEW)

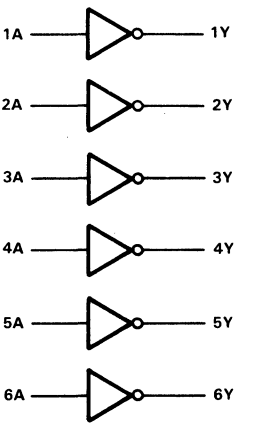


54ACT11004 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±150 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11004		74ACT11004		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11004		74ACT11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ns.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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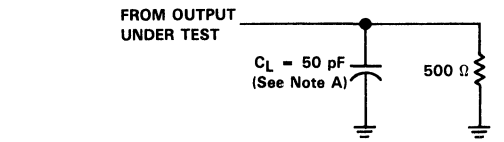
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11004		74ACT11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5.3	9	1.5	10.2	1.5	9.7	ns
t_{PHL}			1.5	6.4	8.7	1.5	10.3	1.5	9.6	

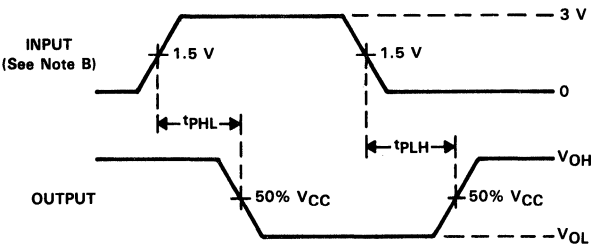
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, AUGUST 1987

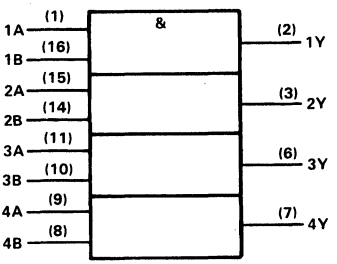
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

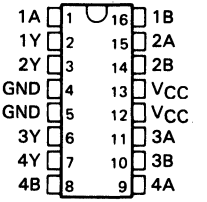
The 54AC11008 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11008 is characterized for operation from −40°C to 85°C.

logic symbol†

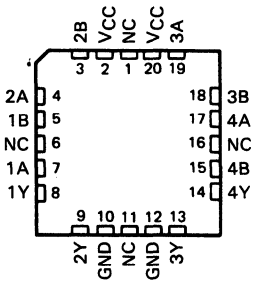


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11008 . . . J PACKAGE
74AC11008 . . . D OR N PACKAGE
(TOP VIEW)

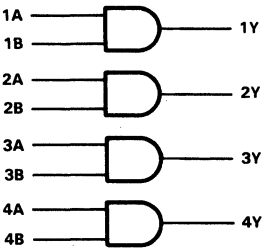


54AC11008 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11008			74AC11008			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11008		74AC11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

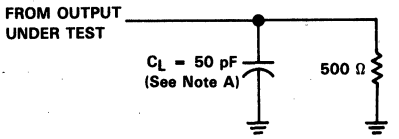
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11008			74AC11008			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A or B	Y	3.3 ±0.3 V	1.5	6.3	9	1.5		11	1.5		10.2	ns
			5 ±0.5 V	1.5	4.3	6.2	1.5		7.3	1.5		6.9	
t_{PHL}			3.3 ±0.3 V	1.5	5.6	7.8	1.5		9	1.5		8.6	
			5 ±0.5 V	1.5	4	5.9	1.5		6.8	1.5		6.5	

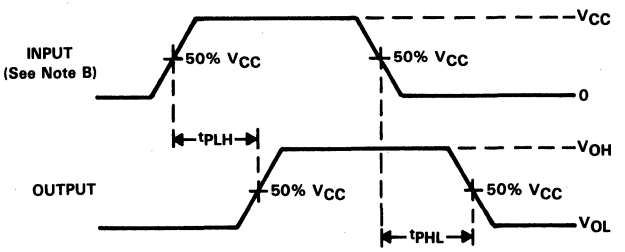
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2957, AUGUST 1987

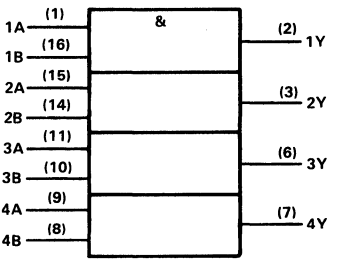
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A}+\overline{B}}$ in positive logic.

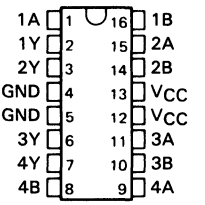
The 54ACT11008 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11008 is characterized for operation from −40°C to 85°C.

logic symbol†

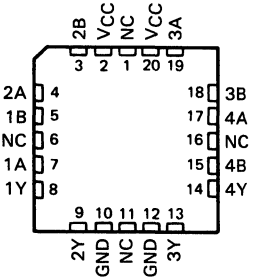


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11008 . . . J PACKAGE
74ACT11008 . . . D OR N PACKAGE
(TOP VIEW)

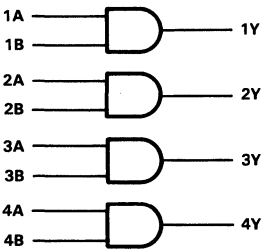


54ACT11008 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11008		74ACT11008		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11008		74ACT11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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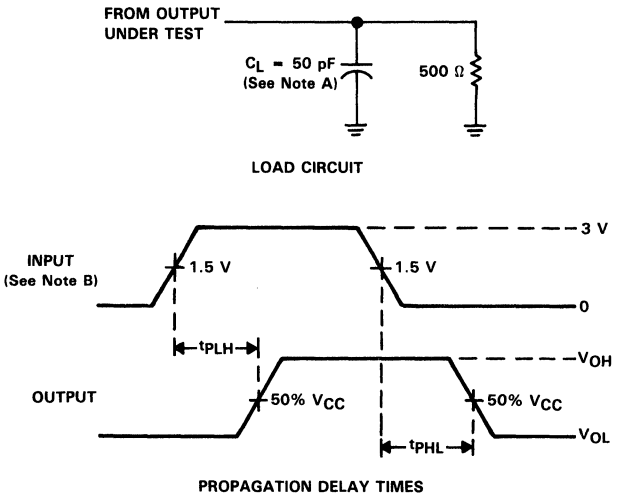
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11008		74ACT11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5.8	8	1.5	9.4	1.5	9	ns
t_{PHL}			1.5	5.2	7.7	1.5	8.6	1.5	8.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, MAY 1987

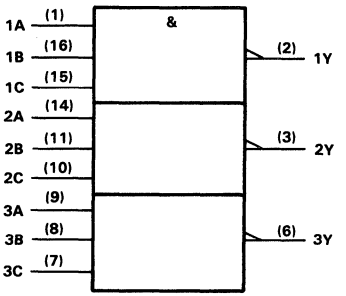
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

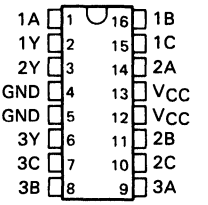
The 54AC11010 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11010 is characterized for operation from −40°C to 85°C.

logic symbol†

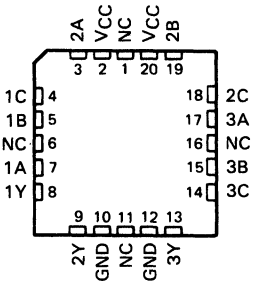


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11010 . . . J PACKAGE
74AC11010 . . . D OR N PACKAGE
(TOP VIEW)



54AC11010 . . . FK PACKAGE
(TOP VIEW)

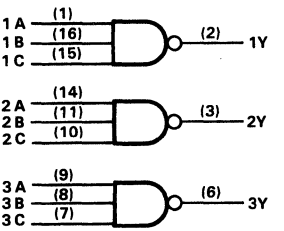


NC—No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

			54AC11010			74AC11010			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} less than 3 volts. Operation between 2 volts and 3 volts is not recommended, but within that range, a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11010		74AC11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

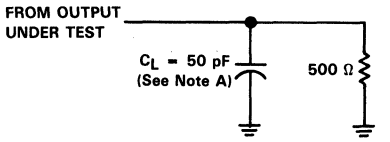
switching characteristics (see Figure 1 for load circuits and waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11010		74AC11010		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	ANY	Y	3.3 V ± 0.3 V	1.5	5.9	8.5	1.5	10	1.5	9.3	ns
			5 V ± 0.5 V	1.5	4.4	6.2	1.5	7.1	1.5	6.7	
t_{PHL}			3.3 V ± 0.3 V	1.5	5.8	9	1.5	10.4	1.5	9.9	ns
			5 V ±0.5 V	1.5	4.6	6.4	1.5	7.4	1.5	7	

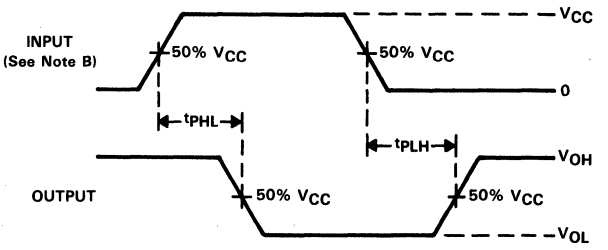
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2957, JULY 1987

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
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description

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

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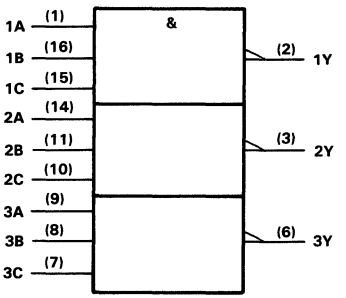
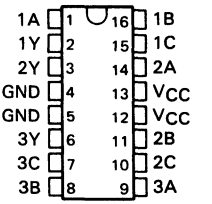
logic symbol†

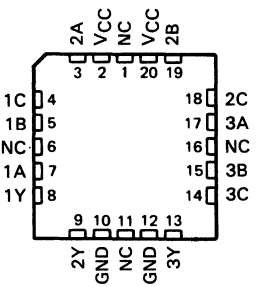


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11010 . . . J PACKAGE
74ACT11010 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11010 . . . FK PACKAGE
(TOP VIEW)

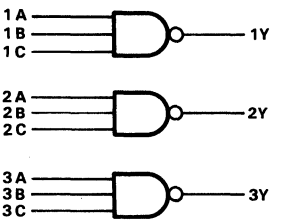


NC—No internal connection

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11010		74ACT11010		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11010		74ACT11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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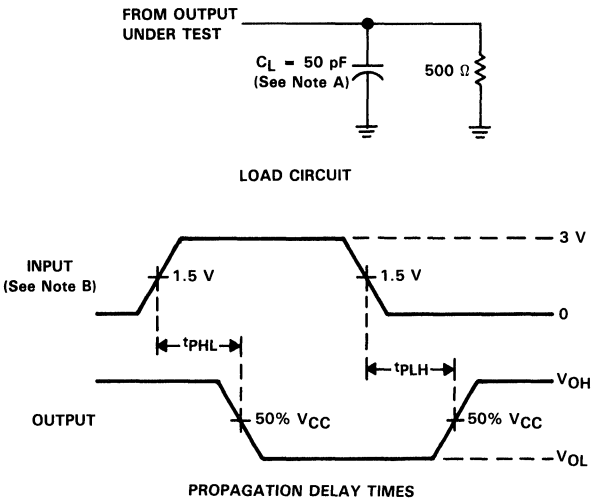
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11010		74ACT11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.8	8.2	1.5	9.3	1.5	8.9	ns
t_{PHL}			1.5	5.7	7.4	1.5	8.7	1.5	8.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, JULY 1987—REVISED NOVEMBER 1987

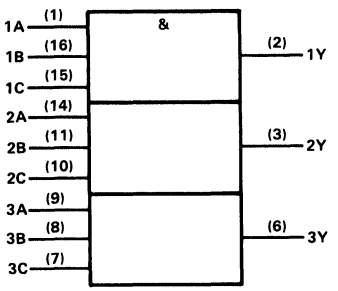
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

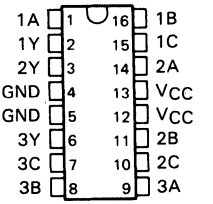
The 54AC11011 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11011 is characterized for operation from −40°C to 85°C.

logic symbol†

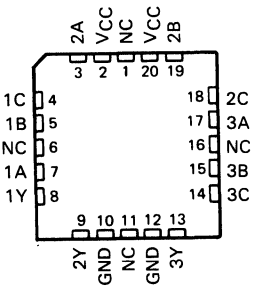


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11011 . . . J PACKAGE
74AC11011 . . . D OR N PACKAGE
(TOP VIEW)

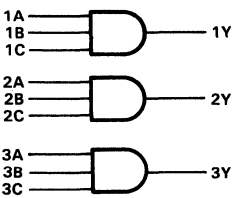


54AC11011 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11011			74AC11011			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11011		74AC11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

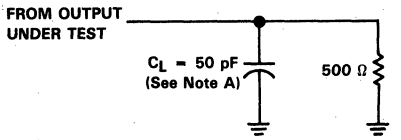
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11011		74AC11011		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3.3 ±0.3 V	1.5	6	8.3	1.5	9.7	1.5	9.1	ns
			5 ±0.5 V	1.5	4	5.9	1.5	6.9	1.5	6.5	
t_{PHL}			3.3 ±0.3 V	1.5	6	8.2	1.5	9.6	1.5	9	
			5 ±0.5 V	1.5	4.5	6.4	1.5	7.3	1.5	6.9	

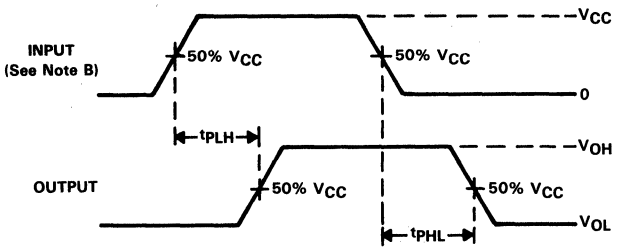
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	28	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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D2957, JULY 1987—REVISED NOVEMBER 1987

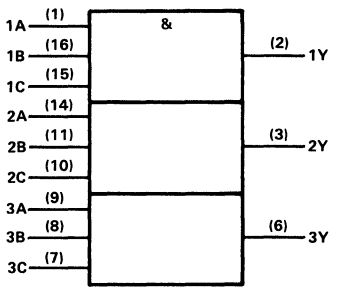
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

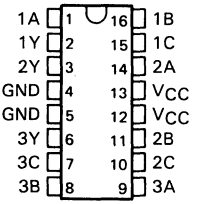
The 54ACT11011 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11011 is characterized for operation from −40°C to 85°C.

logic symbol†

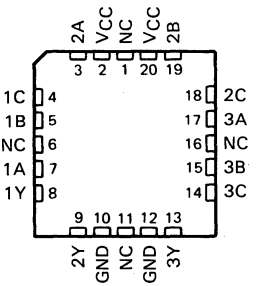


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11011 . . . J PACKAGE
74ACT11011 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11011 . . . FK PACKAGE
(TOP VIEW)

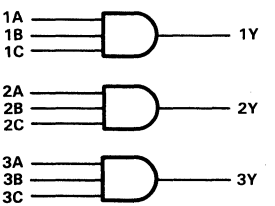


NC—No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11011		74ACT11011		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11011		74ACT11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

TEXAS INSTRUMENTS
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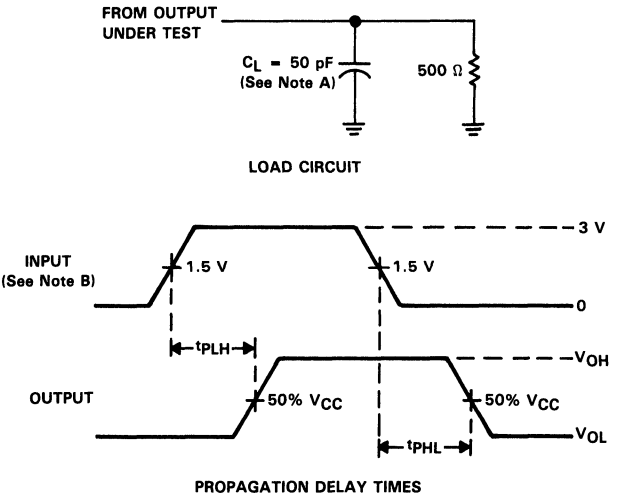
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11011		74ACT11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	1.5	6.5	8.6	1.5	10.2	1.5	9.6	ns
t_{PHL}			1.5	5.5	7.9	1.5	9.2	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	28	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

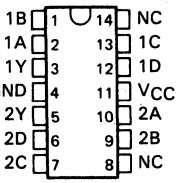
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

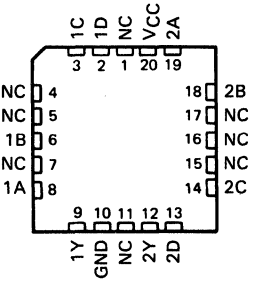
D2957, MARCH 1987

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11020 . . . J PACKAGE
74AC11020 . . . D OR N PACKAGE
(TOP VIEW)



54AC11020 . . . FK PACKAGE
(TOP VIEW)



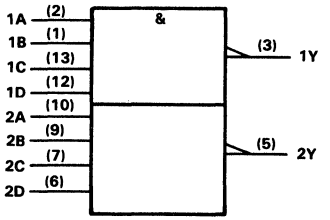
NC—No internal connection

description

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

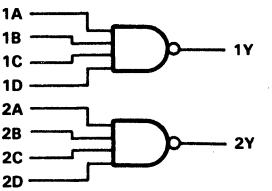
The 54AC11020 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11020 is characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

EPIC is a trademark of Texas Instruments Incorporated

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11020			74AC11020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 milliseconds.

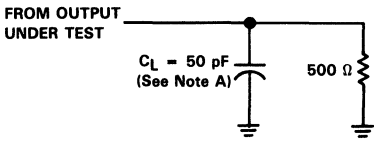
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11020		74AC11020		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3.3 ±0.3 V	1.5	6.4	8.6	1.5	10	1.5	9.4	ns
			5 ±0.5 V	1.5	4.3	6.3	1.5	7	1.5	6.7	
t_{PHL}			3.3 ±0.3 V	1.5	6.4	9.2	1.5	10.7	1.5	10.1	
			5 ±0.5 V	1.5	4.4	6.7	1.5	7.7	1.5	7.3	

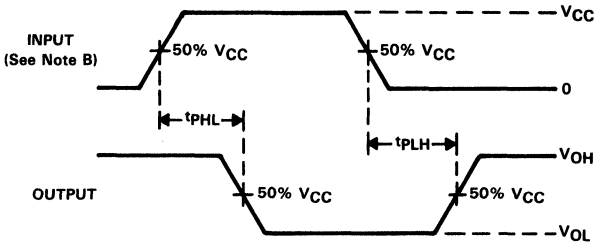
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	19	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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D2957, JUNE 1987

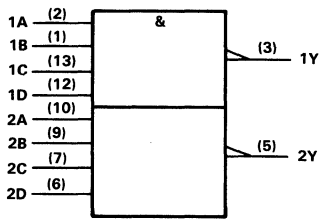
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

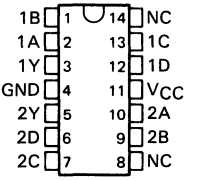
The 54ACT11020 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11020 is characterized for operation from −40°C to 85°C.

logic symbol†

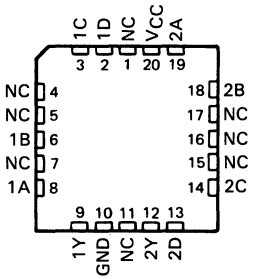


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11020 . . . J PACKAGE
74ACT11020 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11020 . . . FK PACKAGE
(TOP VIEW)

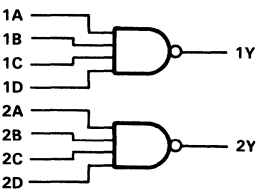


NC—No internal connection

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11020		74ACT11020		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11020		74ACT11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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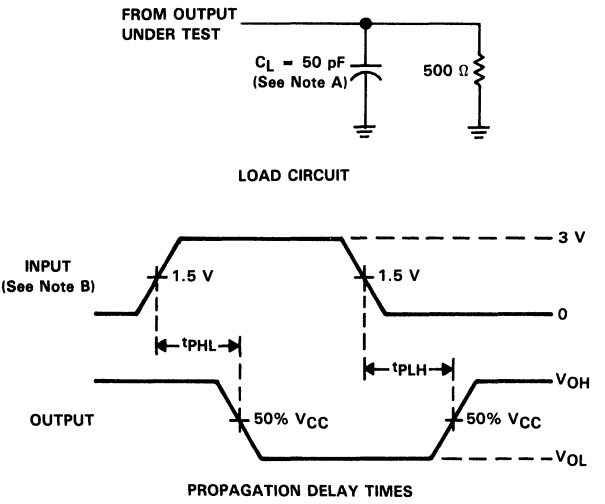
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11020		74ACT11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.6	8.5	1.5	9.5	1.5	9.1	ns
t_{PHL}			1.5	6.1	8.4	1.5	9.8	1.5	9.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, JULY 1987—REVISED DECEMBER 1987

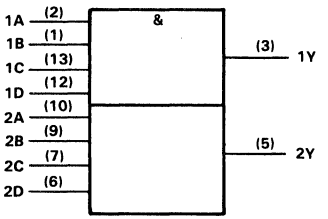
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

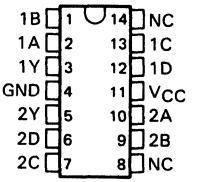
The 54AC11021 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11021 is characterized for operation from −40°C to 85°C.

logic symbol†

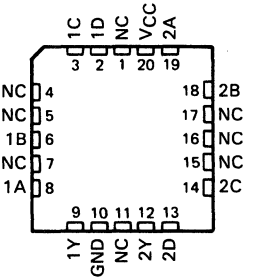


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11021 . . . J PACKAGE
74AC11021 . . . D OR N PACKAGE
(TOP VIEW)

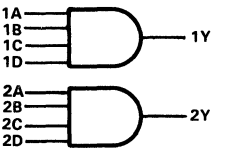


54AC11021 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11021			74AC11021			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11021		74AC11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

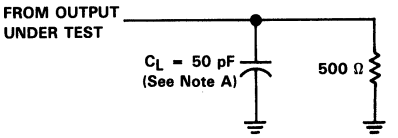
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11021		74AC11021		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3.3 ±0.3 V	1.5	8.2	11.4	1.5	13.9	1.5	13	ns
			5 ±0.5 V	1.5	5.6	7.8	1.5	9.4	1.5	8.8	
t_{PHL}			3.3 ±0.3 V	1.5	6.4	8.7	1.5	9.9	1.5	9.3	
			5 ±0.5 V	1.5	4.6	6.5	1.5	7.4	1.5	6.9	

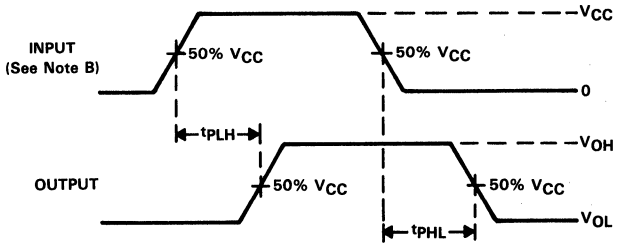
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	38	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

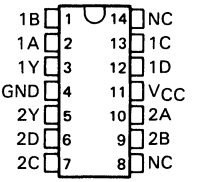
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

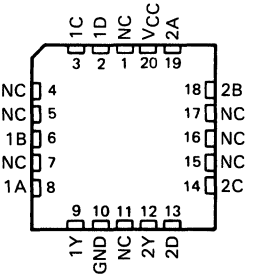
D2957, JULY 1987—REVISED DECEMBER 1987

- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11021 . . . J PACKAGE
74ACT11021 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11021 . . . FK PACKAGE
(TOP VIEW)



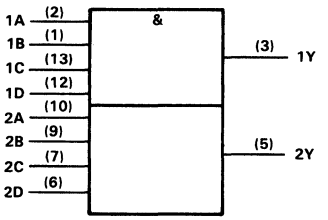
NC—No internal connection

description

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}$ in positive logic.

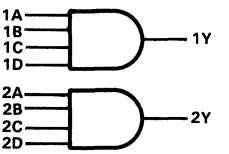
The 54ACT11021 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11021 is characterized for operation from −40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11021		74ACT11021		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11021		74ACT11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

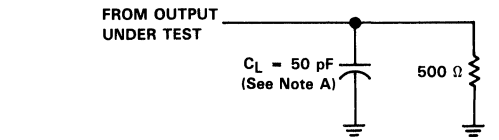
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11021		74ACT11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.7	8.8	1.5	10.4	1.5	9.8	ns
t_{PHL}			1.5	5.4	8.3	1.5	9.5	1.5	8.9	

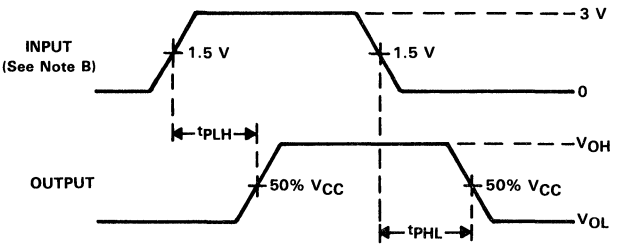
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	37	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, JULY 1987

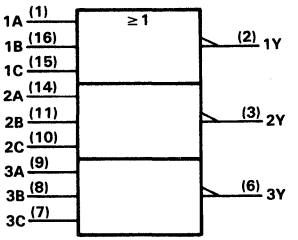
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A}\cdot\overline{B}\cdot\overline{C}$ in positive logic.

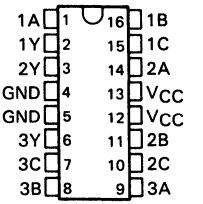
The 54AC11027 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11027 is characterized for operation from −40°C to 85°C.

logic symbol†

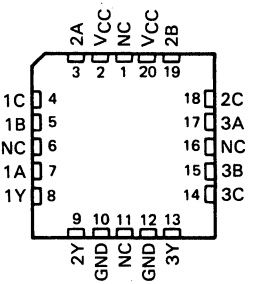


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11027 . . . J PACKAGE
74AC11027 . . . D OR N PACKAGE
(TOP VIEW)



54AC11027 . . . FK PACKAGE
(TOP VIEW)

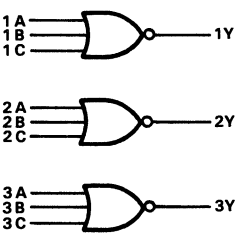


NC—No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

2 Advanced CMOS Circuits

recommended operating conditions

			54AC11027			74AC11027			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} less than 3 volts. Operation between 2 volts and 3 volts is not recommended, but within that range a device output will maintain a previously established logic state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11027		74AC11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

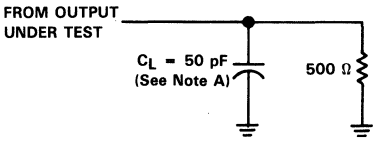
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11027		74AC11027		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	ANY	Y	3.3 V ± 0.3 V	1.5	6.3	9.8	1.5	11.7	1.5	10.9	ns
			5 V ± 0.5 V	1.5	4.3	6.8	1.5	8.1	1.5	7.7	
t_{PHL}			3.3 V ± 0.3 V	1.5	7.6	10.9	1.5	12.9	1.5	12	ns
			5 V ±0.5 V	1.5	4.5	7.5	1.5	8.9	1.5	8.1	

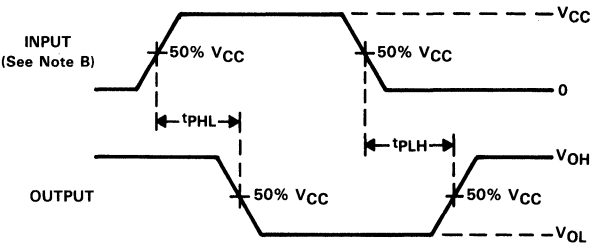
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz,	24	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing, f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2957, JULY 1987

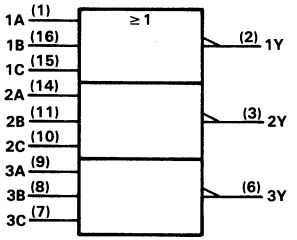
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A+B+C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

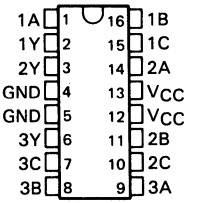
The 54ACT11027 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11027 is characterized for operation from −40°C to 85°C.

logic symbol†

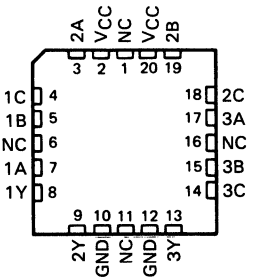


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11027 . . . J PACKAGE
74ACT11027 . . . D OR N PACKAGE
(TOP VIEW)

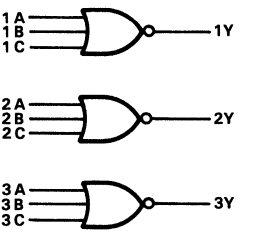


54ACT11027 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11027		74ACT11027		
		MIN	MAX	MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11027		74ACT11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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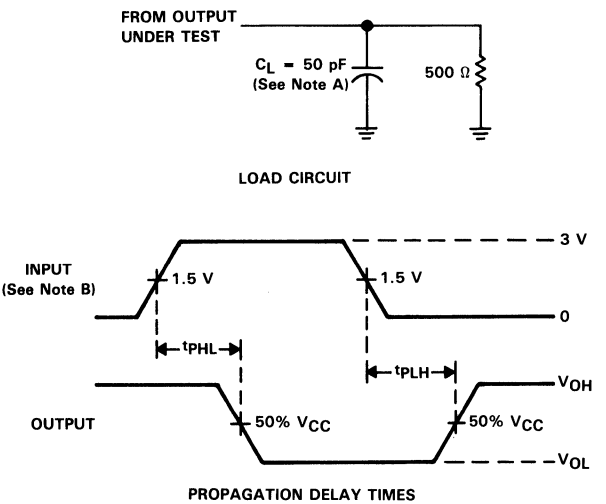
switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11027		74ACT11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5	9.2	1.5	10.6	1.5	10.1	ns
t_{PHL}			1.5	6	8.6	1.5	10	1.5	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

Advanced CMOS Circuits

D2957, JUNE 1987

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

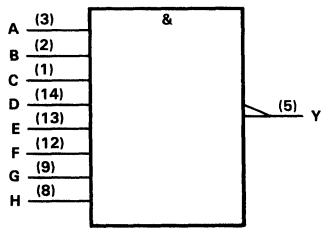
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The 54AC11030 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11030 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

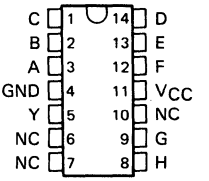
INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†

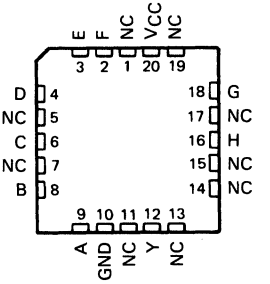


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11030 . . . J PACKAGE
74AC11030 . . . D OR N PACKAGE
(TOP VIEW)

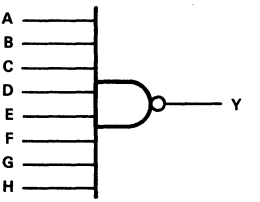


54AC11030 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11030			74AC11030			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11030		74AC11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

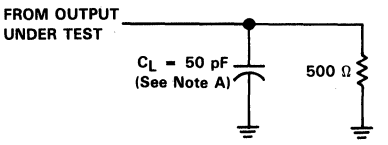
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11030			74AC11030			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Any	Y	3.3 ± 0.3 V	1.5	6.9	9.1	1.5		10.6	1.5		9.9	ns
			5 ± 0.5 V	1.5	4.8	6.7	1.5		7.7	1.5		7.2	
t_{PHL}			3.3 ± 0.3 V	1.5	6.4	8.8	1.5		10.6	1.5		9.8	
			5 ± 0.5 V	1.5	4.8	6.7	1.5		8	1.5		7.4	

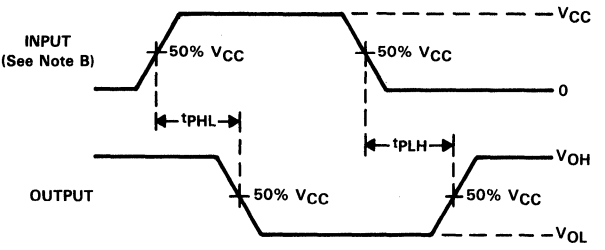
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	42	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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D2957, MARCH 1987

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

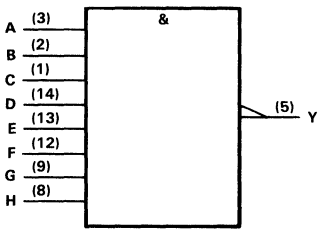
These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

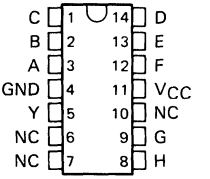
The 54ACT11030 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11030 is characterized for operation from −40°C to 85°C.

logic symbol†

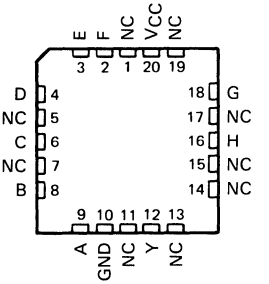


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54ACT11030 . . . J PACKAGE
74ACT11030 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11030 . . . FK PACKAGE
(TOP VIEW)

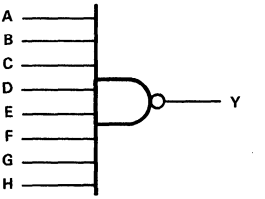


NC—No internal connection

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11030		74ACT11030		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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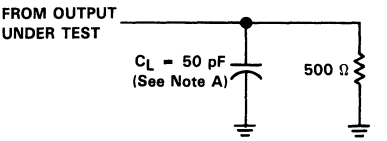
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.4	8.1	1.5	8.8	1.5	8.5	ns
t_{PHL}			1.5	5.9	7.8	1.5	9.3	1.5	8.7	

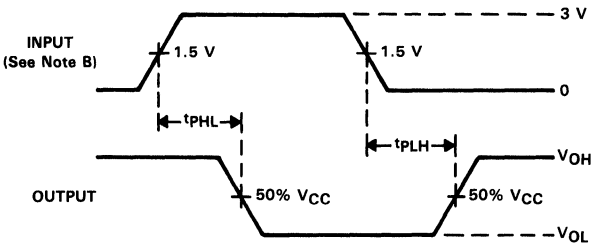
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	41	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

D2957, JULY 1987—REVISED OCTOBER 1987

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

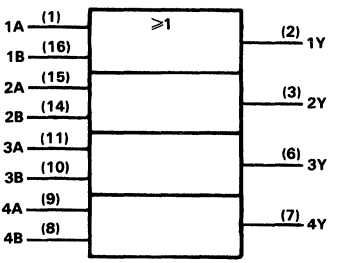
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{A \cdot B}$ in positive logic.

The 54AC11032 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11032 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

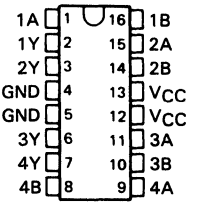
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†

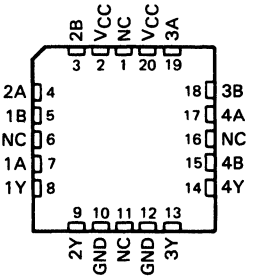


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

54AC11032 . . . J PACKAGE
74AC11032 . . . D OR N PACKAGE
(TOP VIEW)

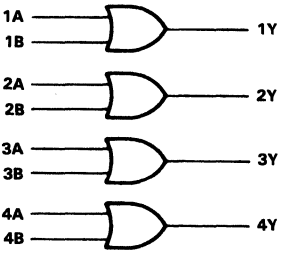


54AC11032 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11032			74AC11032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11032		74AC11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_I	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

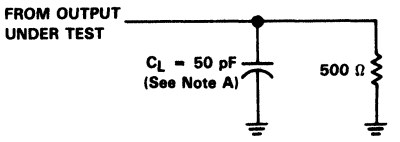
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11032		74AC11032		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3.3 ±0.3 V	1.5	6.3	8.7	1.5	10.7	1.5	9.7	ns
			5 ±0.5 V	1	4.3	6.2	1.5	7.3	1.5	6.7	
t_{PHL}			3.3 ±0.3 V	1.5	5.4	7.4	1.5	8.5	1.5	8	
			5 ±0.5 V	1	3.8	5.5	1.5	6.3	1.5	5.9	

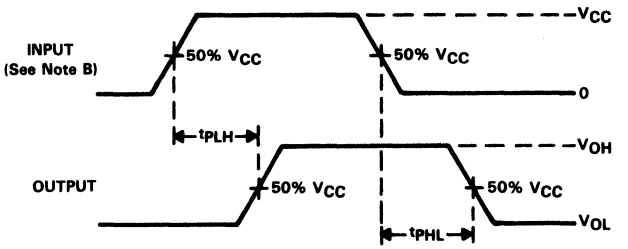
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	24	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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D2957, JULY 1987—REVISED OCTOBER 1987

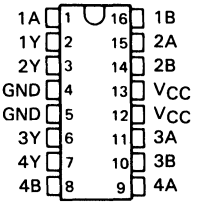
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

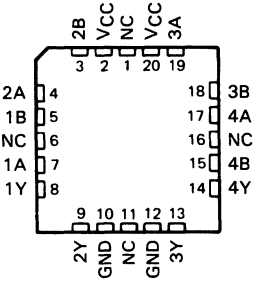
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A+B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ positive logic.

The 54ACT11032 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11032 is characterized for operation from −40°C to 85°C.

54ACT11032 . . . J PACKAGE
74ACT11032 . . . D OR N PACKAGE
(TOP VIEW)

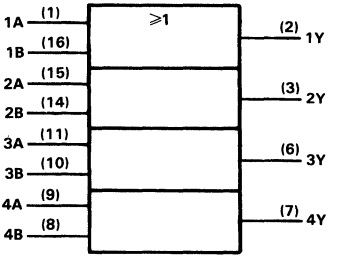


54ACT11032 . . . FK PACKAGE
(TOP VIEW)



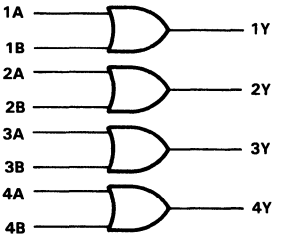
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

EPIC is a trademark of Texas Instruments Instruments.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11032		74ACT11032		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11032		74ACT11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_I	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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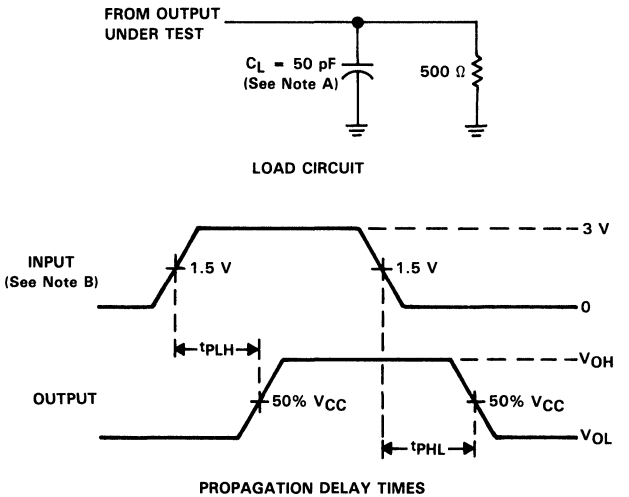
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11032		74ACT11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.2	8.1	1.5	9.6	1.5	9	ns
t_{PHL}			1.5	4.9	7.4	1.5	8.4	1.5	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	25	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

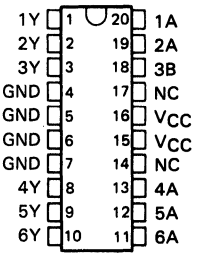
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

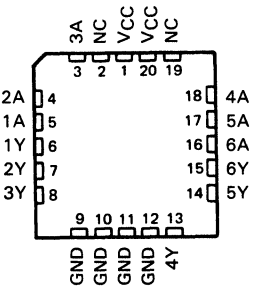
D2957, FEBRUARY 1988

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11034 . . . J PACKAGE
74AC11034 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11034 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

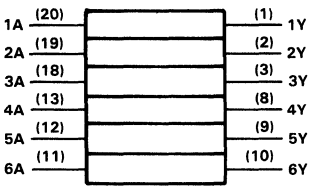
These devices contain six independent noninverters. They perform the Boolean function $Y = A$.

The 54AC11034 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11034 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each buffer)

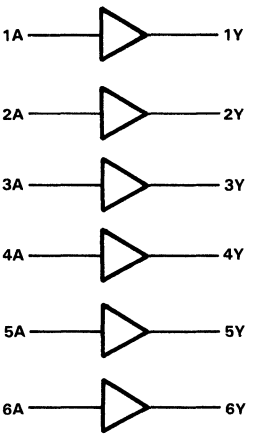
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±150 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11034			74AC11034			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	V_{CC}	T_A = 25°C			54AC11034		74AC11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

V_{CC} = 3.3 V ± 0.3 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11034			74AC11034			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1.5	5.7	9.1	1.5		10.7	1.5		10.1	ns
t_{PHL}			1.5	5.5	8.3	1.5		9.9	1.5		9.2	

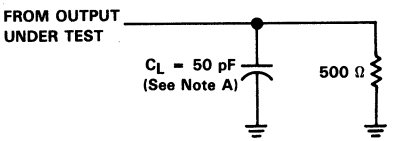
V_{CC} = 5 5 ± 0.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11034			74AC11034			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	1.5	4	6.3	1.5		7.4	1.5		6.9	ns
t_{PHL}			1.5	4	6.2	1.5		7.3	1.5		6.8	

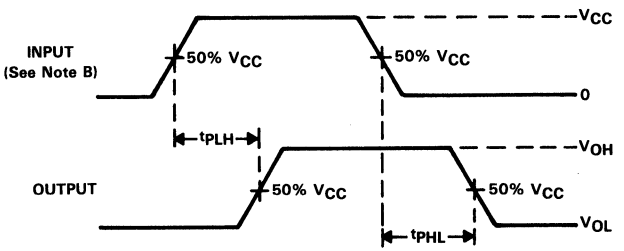
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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D2957, FEBRUARY 1988

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

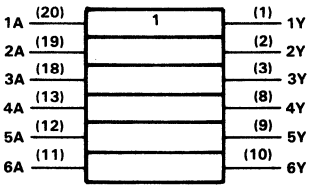
These devices contain six independent noninverters. They perform the Boolean function Y = A.

The 54ACT11034 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11034 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each buffer)

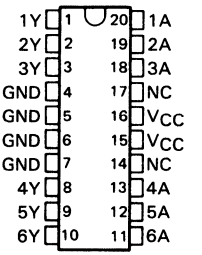
INPUTS A	OUTPUT Y
H	H
L	L

logic symbol†

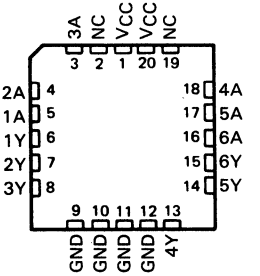


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

54ACT11034 . . . J PACKAGE
74ACT11034 . . . DW OR N PACKAGE
(TOP VIEW)

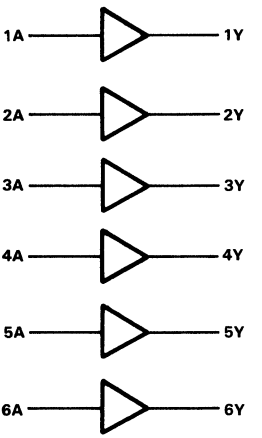


54ACT11034 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±150 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11034		74ACT11034		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11034		74ACT11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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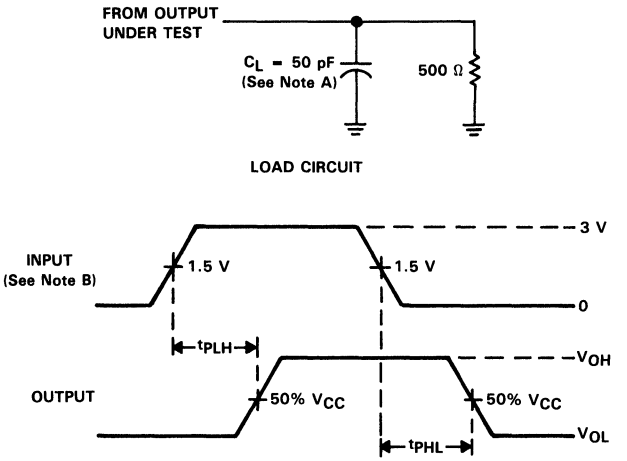
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11034		74ACT11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.1	8.9	1.5	10.5	1.5	9.9	ns
t_{PHL}			1.5	5.2	8	1.5	9.6	1.5	8.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

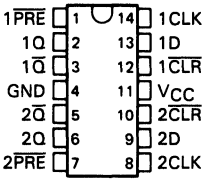
The 54AC11074 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11074 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

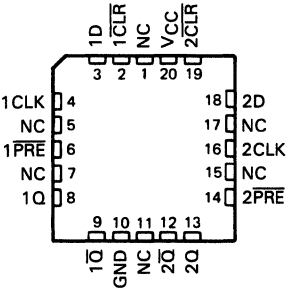
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

54AC11074 . . . J PACKAGE
74AC11074 . . . D OR N PACKAGE
(TOP VIEW)

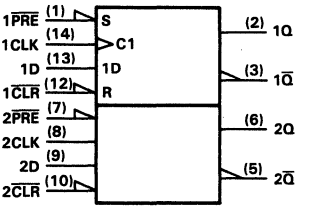


54AC11074 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2 Advanced CMOS Circuits

recommended operating conditions

			54AC11074			74AC11074			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11074		74AC11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

			V_{CC}	T_A = 25°C		54AC11074		74AC11074		UNIT
			RANGE	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		3.3 ±0.3 V	0	100	0	100	0	100	MHz
			5 ±0.5 V	0	125	0	125	0	125	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	3.3 ±0.3 V	4		4		4		ns
			5 ±0.5 V	4		4		4		
		CLK low or CLK high	3.3 ±0.3 V	5		5		5		
			5 ±0.5 V	4		4		4		
t_{su}	Setup time data before CLK↑	Data high or low	3.3 ±0.3 V	5		5		5		ns
			5 ±0.5 V	3.5		3.5		3.5		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	3.3 ±0.3 V	1		1		1		
			5 ±0.5 V	1		1		1		
t_h	Hold time data after CLK↑		3.3 ±0.3 V	0		0		0		ns
			5 ±0.5 V	0		0		0		

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11074		74AC11074		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			3.3 ±0.3 V	100	125		100		100		MHz
			5 ±0.5 V	125	150		125		125		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3.3 ±0.3 V	1.5	5.8	9.3	1.5	10.5	1.5	10	ns
			5 ±0.5 V	1.5	4.2	6.6	1.5	7.5	1.5	7.1	
t_{PHL}			3.3 ±0.3 V	1.5	6.5	11.4	1.5	12.9	1.5	12.2	
			5 ±0.5 V	1.5	4.7	8.2	1.5	9.6	1.5	9	
t_{PLH}	CLK	Q or $\overline{Q}$	3.3 ±0.3 V	1.5	7.7	10.5	1.5	12.1	1.5	11.3	ns
			5 ±0.5 V	1.5	5.4	7.5	1.5	8.7	1.5	8.2	
t_{PHL}			3.3 ±0.3 V	1.5	7.3	9.7	1.5	11.3	1.5	10.6	
			5 ±0.5 V	1.5	5	6.9	1.5	8	1.5	7.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 1 MHz	30	pF

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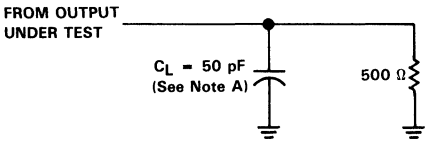
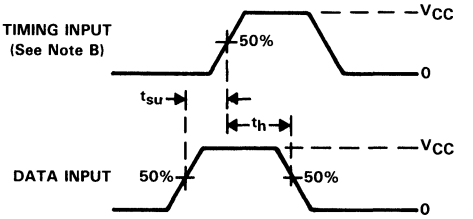
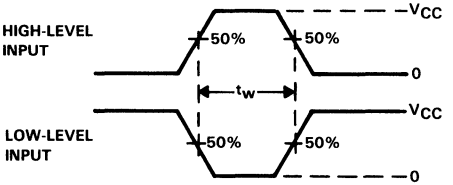
PARAMETER MEASUREMENT INFORMATION



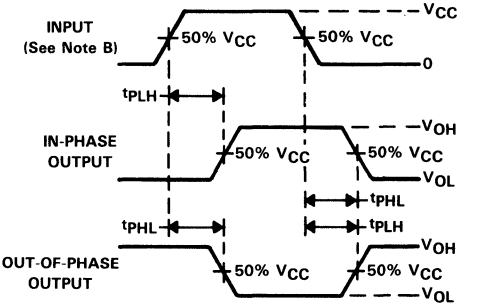
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, DECEMBER 1986—REVISED MARCH 1987

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

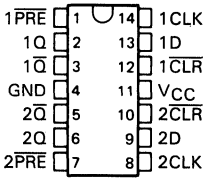
The 54ACT11074 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11074 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

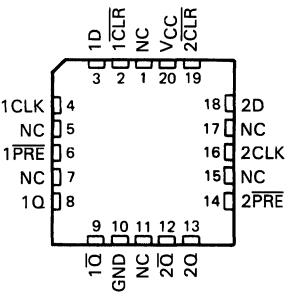
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

54ACT11074 . . . J PACKAGE
74ACT11074 . . . D OR N PACKAGE
(TOP VIEW)

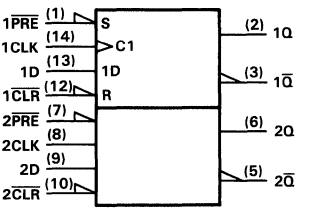


54ACT11074 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol‡



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11074		74ACT11074		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.
§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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timing requirements, V_{CC} = 5 V ±0.5 V (see Figure 1)

			T_A = 25°C		54ACT11074		74ACT11074		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		5		ns
		CLK low or CLK high	5		5		5		
t_{su}	Setup time data before CLK↑	Data high or low	4.5		4.5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time data after CLK↑		0		0		0		ns

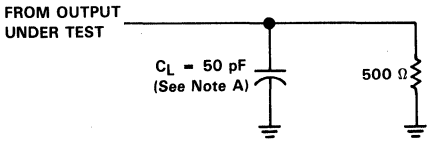
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	5.7	8.9	1.5	10.1	1.5	9.6	ns
t_{PHL}			1.5	6.6	11.3	1.5	13.3	1.5	12.5	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	6	8.5	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	5.7	8	1.5	9.4	1.5	8.8	

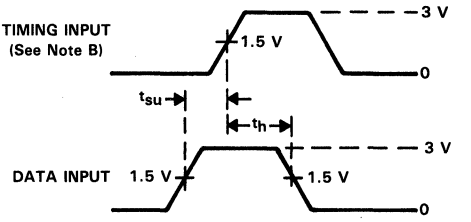
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 1 MHz	30	pF

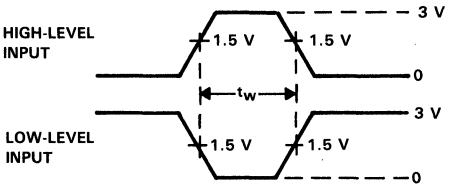
PARAMETER MEASUREMENT INFORMATION



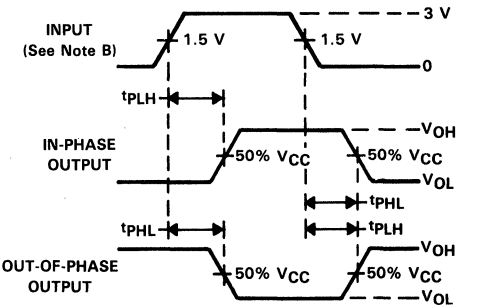
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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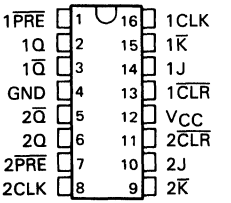
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

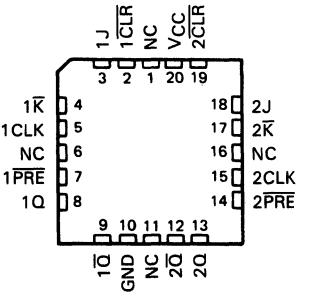
These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops by tying the J and $\overline{K}$ inputs together.

The 54AC11109 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11109 is characterized for operation from −40°C to 85°C.

54AC11109 . . . J PACKAGE
74AC11109 . . . D OR N PACKAGE
(TOP VIEW)

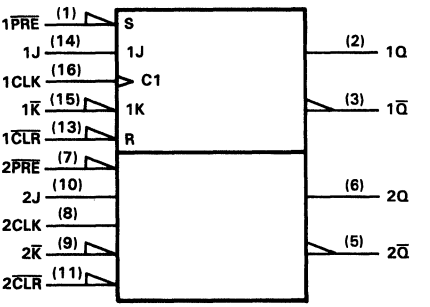


54AC11109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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FUNCTION TABLE (each gate)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to the inactive (high) level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11109			74AC11109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

PARAMETER			V_{CC} RANGE	T_A = 25°C		54AC11109		74AC11109		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		3.3 ± 0.3 V	0	70	0	70	0	70	MHz
			5 ± 0.5 V	0	100	0	100	0	100	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	3.3 ± 0.3 V	5		5		5		ns
			5 ± 0.5 V	4		5		4		
		CLK high or low	3.3 ± 0.3 V	7.2		7.2		7.2		
			5 ± 0.5 V	5		5		5		
t_{su}	Setup time before CLK ↑	Data high or low	3.3 ± 0.3 V	5.5		5.5		5.5		ns
			5 ± 0.5 V	4.5		4.5		4.5		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	3.3 ± 0.3 V	2.5		2.5		2.5		
			5 ± 0.5 V	2		2		2		
t_h	Hold time, data after CLK ↑		3.3 ± 0.3 V	0		0		0		ns
			5 ± 0.5 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM	TO	V_{CC} RANGE	T_A = 25°C			54AC11109		74AC11109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			3.3 ± 0.3 V	70	100		70		70		MHz
			5 ± 0.5 V	100	125		100		100		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3.3 ± 0.3 V	1.5	6.5	9	1.5	10.5	1.5	9.9	ns
			5 ± 0.5 V	1.5	4.5	6.5	1.5	7.6	1.5	7.1	
t_{PHL}			3.3 ± 0.3 V	1.5	8	12.6	1.5	14.4	1.5	13.7	
			5 ± 0.5 V	1.5	5	8.6	1.5	10.2	1.5	9.6	
t_{PLH}	CLK	Q or $\overline{Q}$	3.3 ± 0.3 V	1.5	8	11.4	1.5	13.5	1.5	12.7	ns
			5 ± 0.5 V	1.5	5.5	7.9	1.5	9.4	1.5	8.8	
t_{PHL}			3.3 ± 0.3 V	1.5	7.5	10.5	1.5	12.7	1.5	11.8	
			5 ± 0.5 V	1.5	5	7.3	1.5	8.6	1.5	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF,	f = 1 MHz	32	pF

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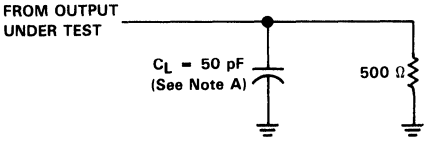
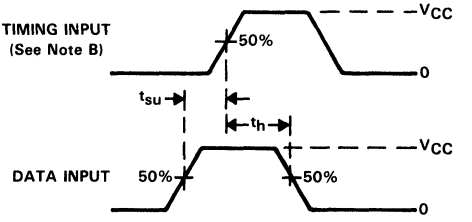
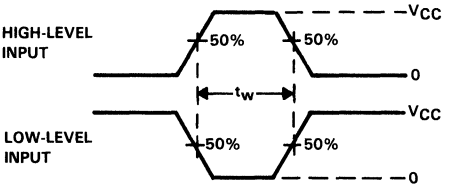
PARAMETER MEASUREMENT INFORMATION



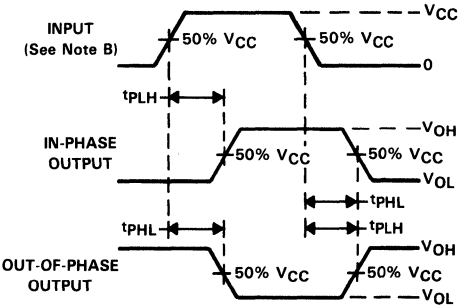
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

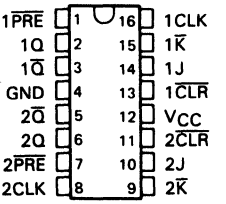
Advanced CMOS Circuits

54ACT11109, 74ACT11109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

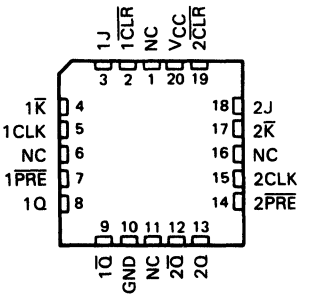
D2957, FEBRUARY 1987—REVISED MARCH 1987

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11109 . . . J PACKAGE
74ACT11109 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The 54ACT11109 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11109 is characterized for operation from −40°C to 85°C.

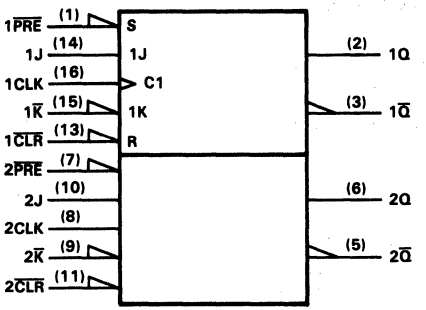
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to the inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11109			74ACT11109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

			T_A = 25°C		54ACT11109		74ACT11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5.5		5.5		5.5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time before CLK↑	Data high or low	5.5		5.5		5.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time data after CLK↑		0		0		0		ns

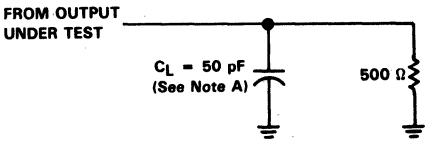
switching characteristics V_{CC} = 5 ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	5.5	8.6	1.5	9.8	1.5	9.2	ns
t_{PHL}			1.5	6	10.8	1.5	12.6	1.5	11.8	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	6	8.3	1.5	9.7	1.5	9.1	ns
t_{PHL}			1.5	5.5	7.6	1.5	9	1.5	8.3	

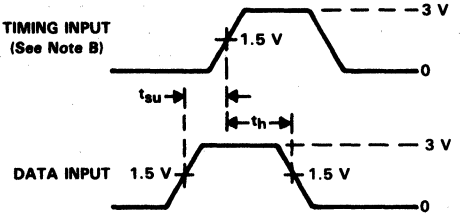
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 1 MHz	31	pF

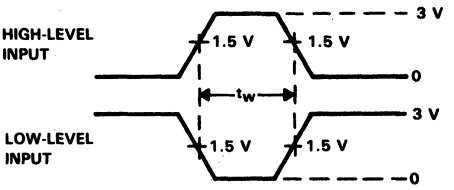
PARAMETER MEASUREMENT INFORMATION



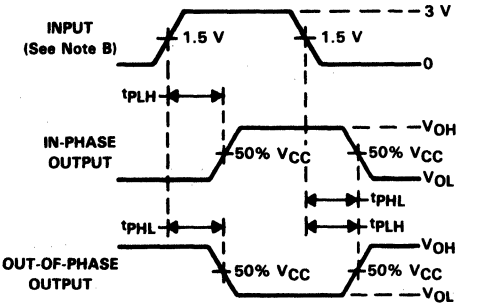
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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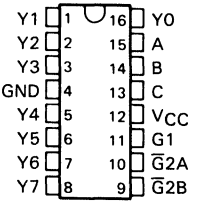
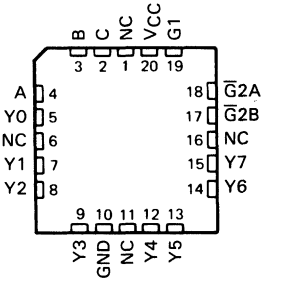
D3103, APRIL 1988

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Noninverting Version of 'AC11138**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11238 . . . J PACKAGE
74AC11238 . . . D OR N PACKAGE
(TOP VIEW)



54AC11238 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

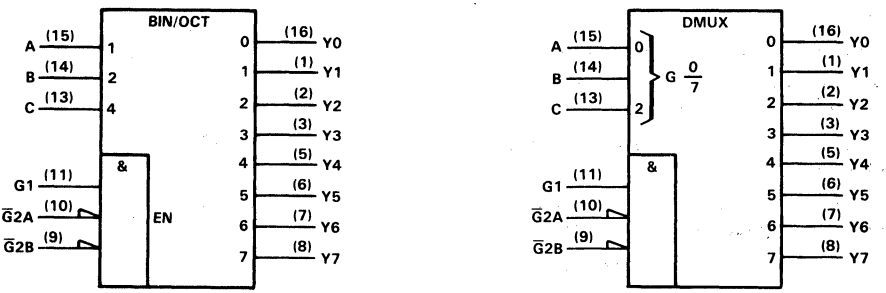
The 'AC11238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 54AC11238 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11238 is characterized for operation from −40°C to 85°C.

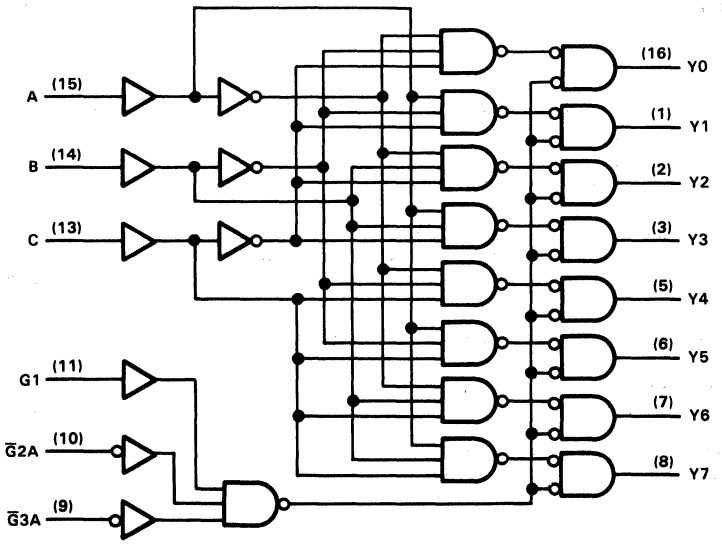
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

TEXAS INSTRUMENTS
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FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11238			74AC11238			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11238		74AC11238		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (See Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11238		74AC11238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A,B,C	Any Y	1.5	8.5	10.6	1.5	12.7	1.5	11.7	ns
t_{PHL}			1.5	9.6	11.9	1.5	14.3	1.5	13.3	
t_{PLH}	G1	Any Y	1.5	8.2	10.3	1.5	12.3	1.5	11.4	ns
t_{PHL}			1.5	9.6	11.7	1.5	14	1.5	13	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	1.5	9.1	11.2	1.5	13.4	1.5	12.5	ns
t_{PHL}			1.5	10.7	12.9	1.5	15.6	1.5	14.5	

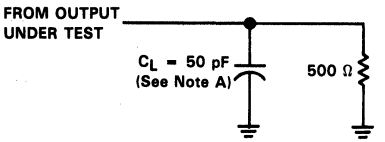
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (See Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11238		74AC11238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	1.5	5.4	7.3	1.5	9	1.5	8.5	ns
t_{PHL}			1.5	6.3	8.6	1.5	10.9	1.5	10.2	
t_{PLH}	G1	Any Y	1.5	5.2	6.9	1.5	8.7	1.5	8.1	ns
t_{PHL}			1.5	6.5	8.5	1.5	10.6	1.5	9.9	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Any Y	1.5	5.6	7.5	1.5	9.6	1.5	8.9	ns
t_{PHL}			1.5	7.2	9.3	1.5	11.8	1.5	11	

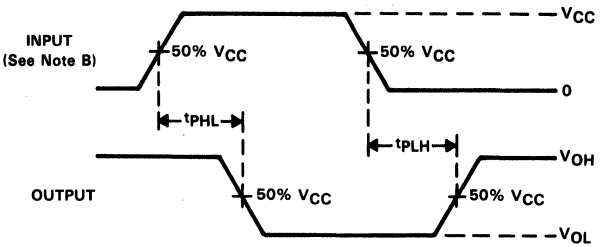
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	44	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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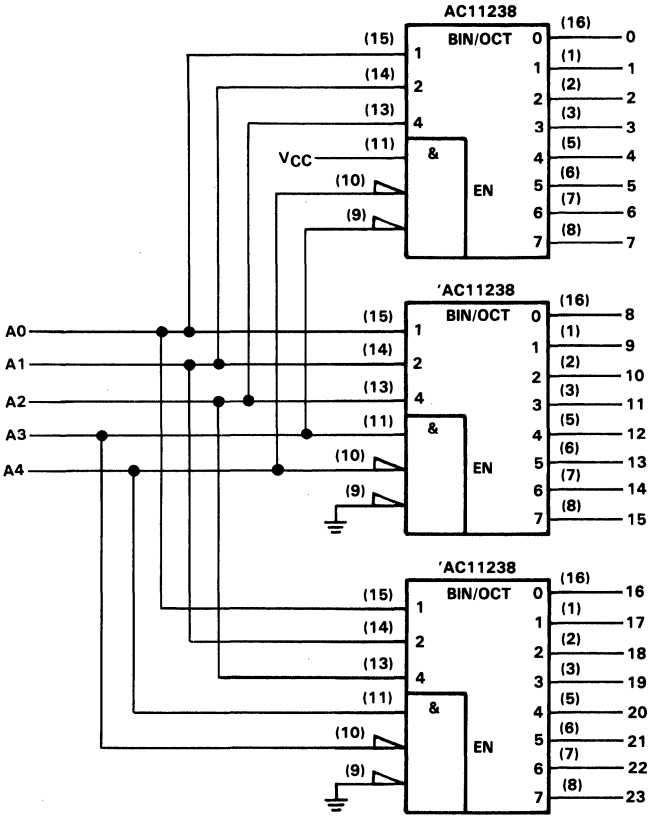
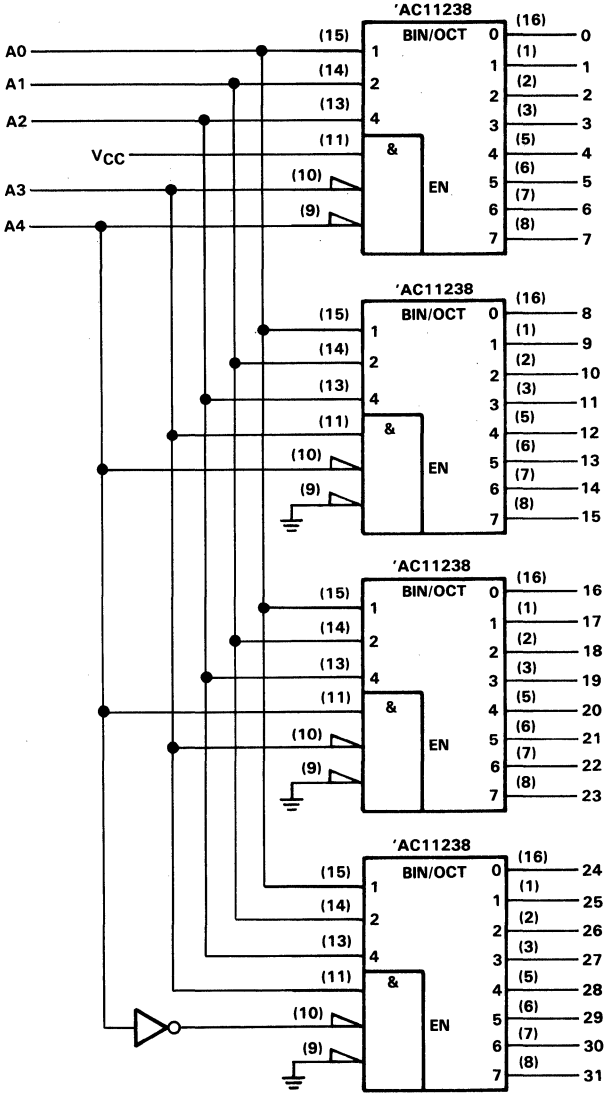
TYPICAL APPLICATION DATA



Pin numbers shown are for D, J, and N packages.

FIGURE 2. 24-BIT DECODING SCHEME

TYPICAL APPLICATION DATA



Pin numbers shown are for D, J, and N packages.

FIGURE 3. 32-BIT DECODING SCHEME

MAY 1987—REVISED JANUARY 1988

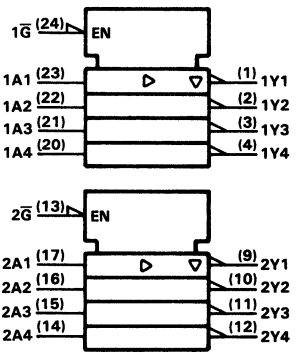
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\overline{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

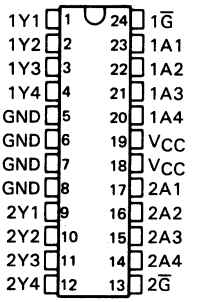
The 54AC11240 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11240 is characterized for operation from −40°C to 85°C.

logic symbol†

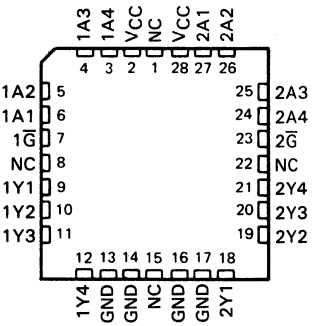


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

54AC11240 . . . JT PACKAGE
74AC11240 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11240 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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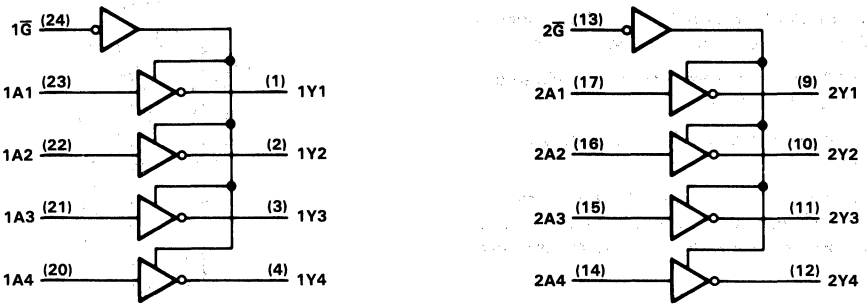
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

			54AC11240			74AC11240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level nput voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	$\overline{G}$	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11240		74AC11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11240		74AC11240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.3 ± 0.3 V	1.5	7.6	10.5	1.5	12.8	1.5	11.7	ns
			5 ± 0.5 V	1.5	5.4	7.5	1.5	9	1.5	8.4	
t_{PHL}	A	Y	3.3 ± 0.3 V	1.5	6.3	8.6	1.5	10.2	1.5	9.5	ns
			5 ± 0.5 V	1.5	4.6	6.6	1.5	7.8	1.5	7.2	
t_{PZH}	$\overline{G}$	Y	3.3 ± 0.3 V	1.5	8.2	11.6	1.5	13.4	1.5	12.7	ns
			5 ± 0.5 V	1.5	5.7	8.2	1.5	9.9	1.5	9.2	
t_{PZL}	$\overline{G}$	Y	3.3 ± 0.3 V	1.5	7.6	10.8	1.5	13	1.5	12	ns
			5 ± 0.5 V	1.5	5.3	7.7	1.5	9.4	1.5	8.7	
t_{PHZ}	$\overline{G}$	Y	3.3 ± 0.3 V	1.5	5.5	7.5	1.5	8.1	1.5	7.8	ns
			5 ± 0.5 V	1.5	4.7	6.3	1.5	6.9	1.5	6.6	
t_{PLZ}	$\overline{G}$	Y	3.3 ± 0.3 V	1.5	6.7	9.4	1.5	10	1.5	9.8	ns
			5 ± 0.5 V	1.5	5.2	7.3	1.5	8	1.5	7.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		12	

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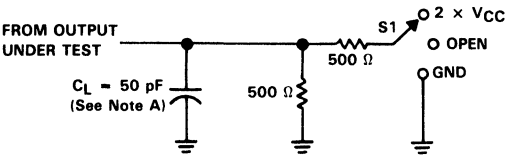
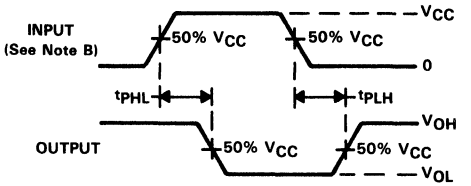
PARAMETER MEASUREMENT INFORMATION

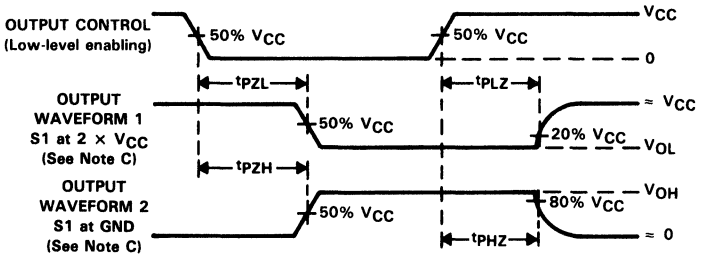


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

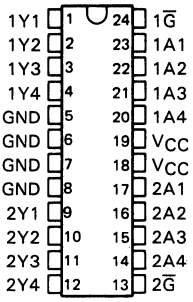
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

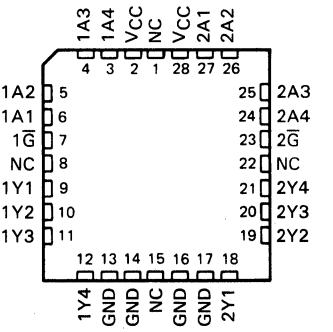
MAY 1987—REVISED JANUARY 1988

- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11240 . . . JT PACKAGE
74ACT11240 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11240 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\overline{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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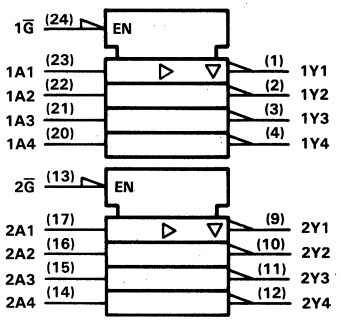
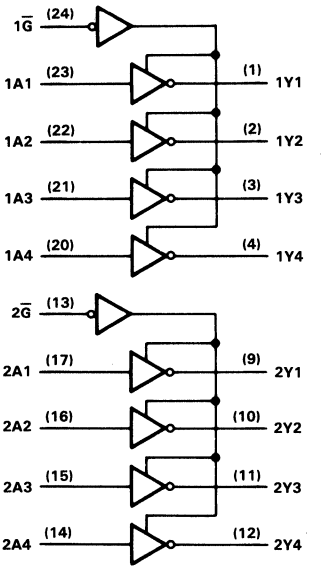
logic symbol†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC} +0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11240			74ACT11240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

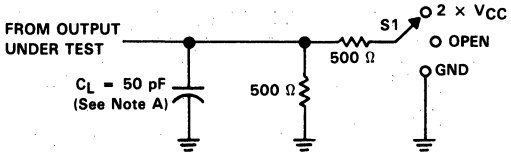
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.5	9.9	1.5	11.1	1.5	10.6	ns
t_{PHL}			1.5	6	8	1.5	9.2	1.5	8.7	
t_{PZH}	$\overline{G}$	Y	1.5	7.5	11.7	1.5	13.1	1.5	12.5	ns
t_{PZL}			1.5	7.3	11.5	1.5	12.8	1.5	12.3	
t_{PHZ}	$\overline{G}$	Y	1.5	7.3	9.4	1.5	10.3	1.5	10	ns
t_{PLZ}			1.5	7.9	10.3	1.5	11.2	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

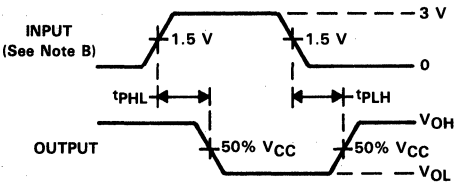
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
	Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

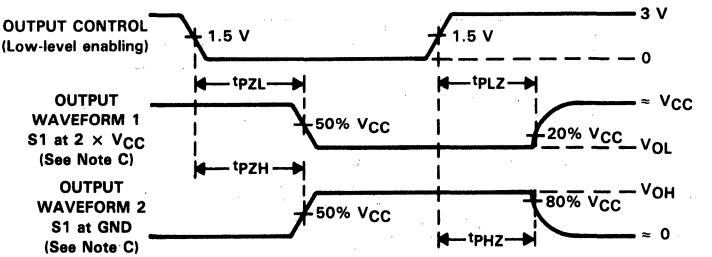


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

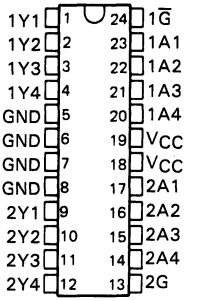
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

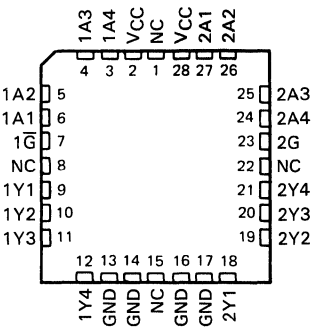
D2957, JULY 1987—REVISED NOVEMBER 1987

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11241 . . . JT PACKAGE
74AC11241 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11241 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This octal buffer and line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the AC11240 and AC11244, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. This device features a high fan-out.

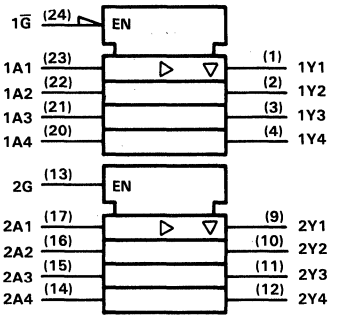
The 54AC11241 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11241 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT	OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$	1A	1Y	2G	2A	2Y
H	X	Z	L	X	Z
L	L	L	H	L	L
L	H	H	H	H	H

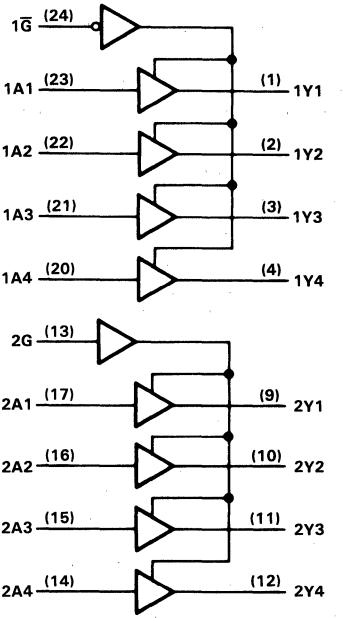
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11241			74AC11241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			9.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		$\overline{G}$	0		5	0		5	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11241		74AC11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11241		74AC11241		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.3 ±0.3 V	1.5	7	10	1.5	12.2	1.5	11.4	ns
			5 ±0.5 V	1.5	4.9	7.1	1.5	8.5	1.5	8	
t_{PHL}			3.3 ±0.3 V	1.5	6.2	8.4	1.5	10.2	1.5	9.2	
			5 ±0.5 V	1.5	4.5	6.3	1.5	7.2	1.5	6.8	
t_{PZH}	$\overline{G}$ or G	Y	3.3 ±0.3 V	1.5	7.8	11.4	1.5	13.8	1.5	12.9	ns
			5 ±0.5 V	1.5	5.4	8	1.5	9.7	1.5	9	
t_{PZL}			3.3 ±0.3 V	1.5	7.7	10.6	1.5	12.6	1.5	11.7	
			5 ±0.5 V	1.5	5.3	7.6	1.5	9	1.5	8.4	
t_{PHZ}	$\overline{G}$ or G	Y	3.3 ±0.3 V	1.5	5.8	7.6	1.5	8.2	1.5	7.9	ns
			5 ±0.5 V	1.5	4.9	6.6	1.5	7.2	1.5	6.9	
t_{PLZ}			3.3 ±0.3 V	1.5	7.1	9.3	1.5	10.3	1.5	9.9	
			5 ±0.5 V	1.5	5.6	7.5	1.5	8.3	1.5	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer		Outputs enabled	C_L = 50 pF, f = 1 MHz	26	pF
		Outputs disabled		10	

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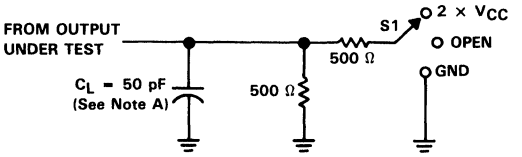
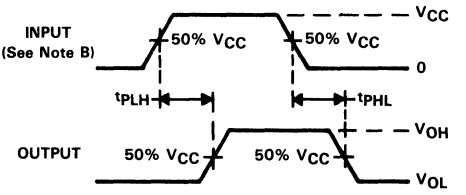
PARAMETER MEASUREMENT INFORMATION

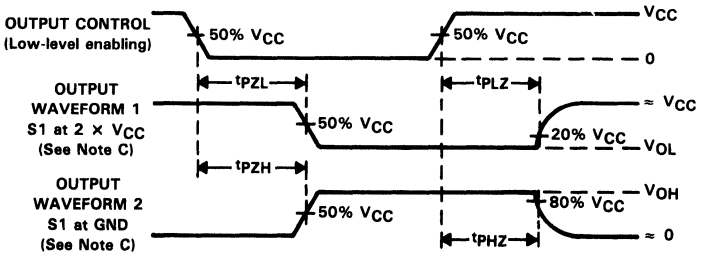


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

D2957, JULY 1987—REVISED NOVEMBER 1987

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
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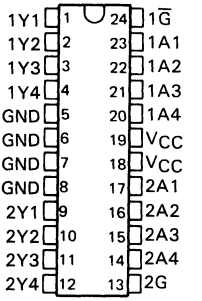
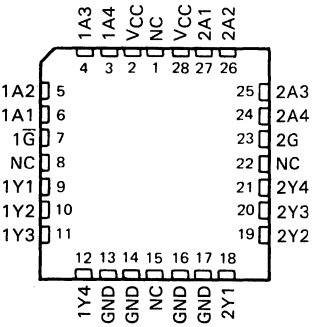
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11241 . . . JT PACKAGE
74ACT11241 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11241 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ACT11240 and ACT11244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out.

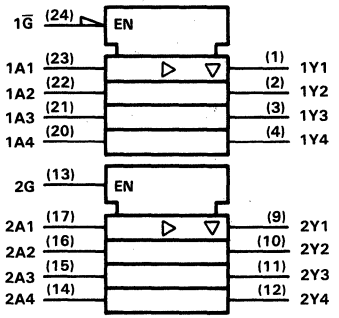
The 54ACT11241 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11241 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT	OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$	1A	1Y	2G	2A	2Y
H	X	Z	L	X	Z
L	L	L	H	L	L
L	H	H	H	H	H

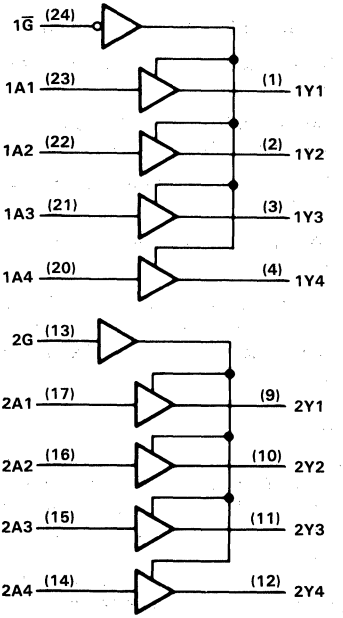
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11241		74ACT11241		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

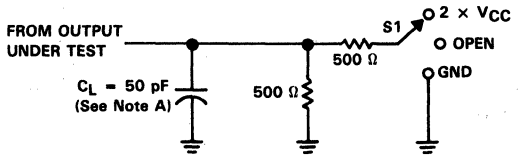
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6.6	9	1.5	10.7	1.5	10	ns
t_{PHL}			1.5	6.3	8.5	1.5	9.5	1.5	9.1	
t_{PZH}	G or $\overline{G}$	Y	1.5	7.5	11.3	1.5	13	1.5	12.3	
t_{PZL}			1.5	7.4	10.5	1.5	11.9	1.5	11.3	
t_{PHZ}	G or $\overline{G}$	Y	1.5	7.6	10.6	1.5	11.4	1.5	11	
t_{PLZ}			1.5	8.2	11.2	1.5	12	1.5	11.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

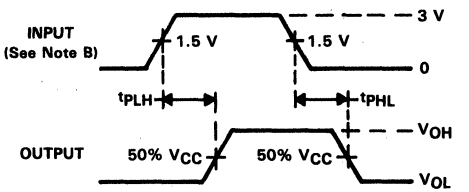
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	27	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

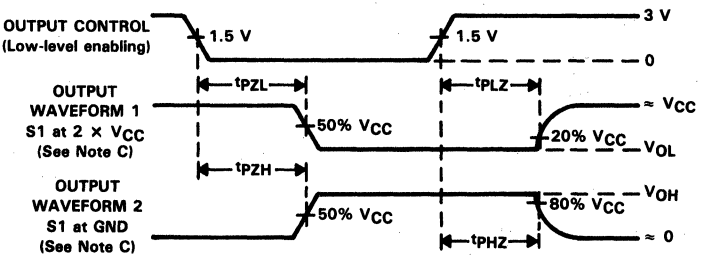


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

MAY 1987—REVISED JANUARY 1988

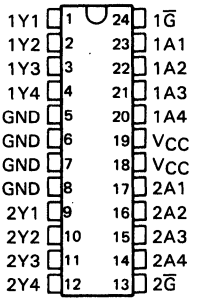
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

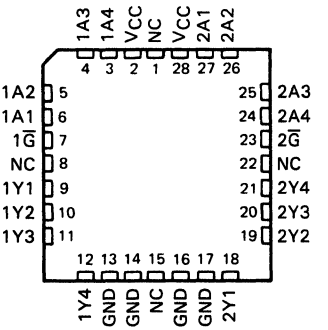
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the AC11240 and AC11241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The 54AC11244 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11244 is characterized for operation from −40°C to 85°C.

54AC11244 . . . JT PACKAGE
74AC11244 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11244 . . . FK PACKAGE
(TOP VIEW)



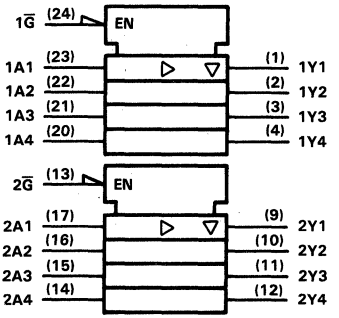
NC—No internal connection

FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$, $2\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

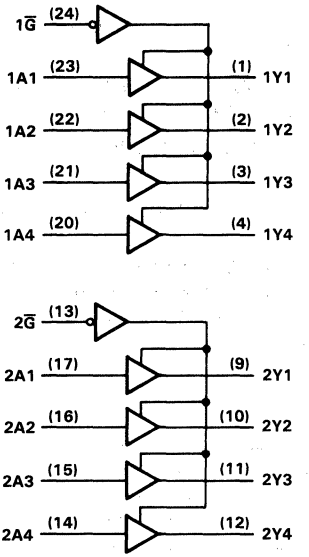
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11244			74AC11244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	$\overline{G}$	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11244		74AC11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

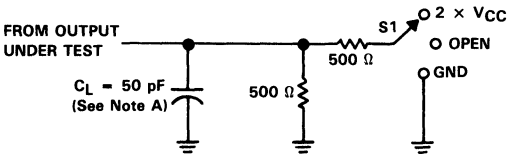
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11244		74AC11244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.3 ±0.3 V	1.5	7.1	9.3	1.5	10.8	1.5	10.2	ns
			5 ±0.5 V	1.5	4.9	6.7	1.5	7.7	1.5	7.3	
t_{PHL}			3.3 ±0.3 V	1.5	6.3	8.6	1.5	10.5	1.5	9.5	
			5 ±0.5 V	1.5	4.5	6.4	1.5	7.4	1.5	6.9	
t_{PZH}	$\overline{G}$	Y	3.3 ±0.3 V	1.5	8	10.7	1.5	12.9	1.5	11.8	ns
			5 ±0.5 V	1.5	5.4	7.7	1.5	9.3	1.5	8.5	
t_{PZL}			3.3 ±0.3 V	1.5	7.9	10.6	1.5	12.9	1.5	11.9	
			5 ±0.5 V	1.5	5.4	7.6	1.5	9.1	1.5	8.5	
t_{PHZ}	$\overline{G}$	Y	3.3 ±0.3 V	1.5	5.9	7.9	1.5	8.7	1.5	8.3	ns
			5 ±0.5 V	1.5	5.2	7	1.5	7.6	1.5	7.3	
t_{PLZ}			3.3 ±0.3 V	1.5	7.2	9.4	1.5	10.4	1.5	9.9	
			5 ±0.5 V	1.5	5.8	7.8	1.5	8.6	1.5	8.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	27	pF
		Outputs disabled		9	

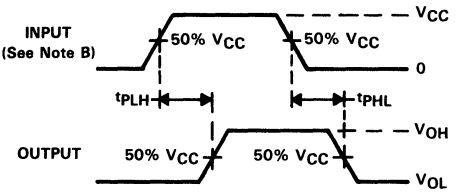
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

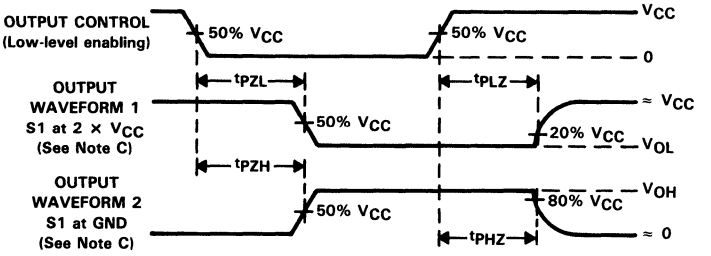


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, AUGUST 1987—REVISED JANUARY 1988

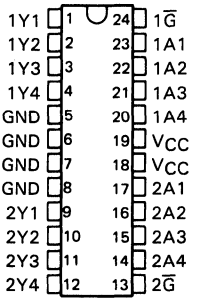
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

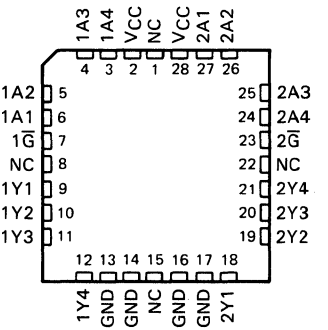
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ACT11240 and 'ACT11241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The 54ACT11244 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11244 is characterized for operation from −40°C to 85°C.

54ACT11244 . . . JT PACKAGE
74ACT11244 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11244 . . . FK PACKAGE
(TOP VIEW)



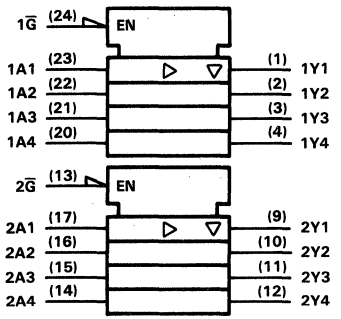
NC—No internal connection

FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$, $2\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

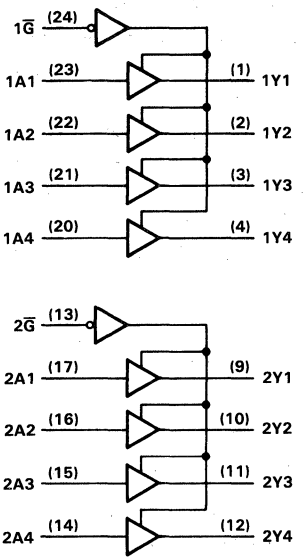
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11244		74ACT11244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11244		74ACT11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

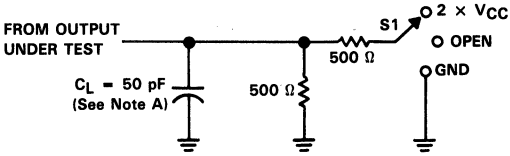
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11244		74ACT11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6	8.9	1.5	10.6	1.5	9.9	ns
t_{PHL}			1.5	5.4	8.6	1.5	9.7	1.5	9.2	
t_{PZH}	$\overline{G}$	Y	1.5	6.6	11.3	1.5	13.4	1.5	12.5	ns
t_{PZL}			1.5	6.7	10.5	1.5	12.2	1.5	11.4	
t_{PHZ}	$\overline{G}$	Y	1.5	7.4	9.8	1.5	10.8	1.5	10.4	ns
t_{PLZ}			1.5	7.8	10.6	1.5	11.6	1.5	11.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

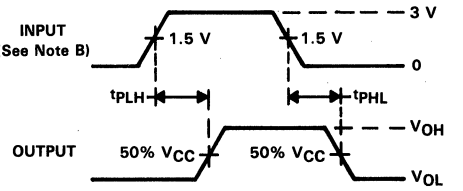
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	27	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

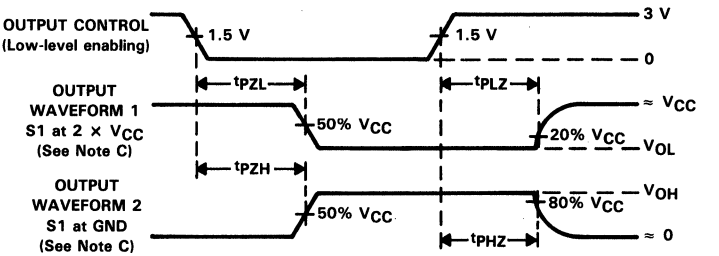


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

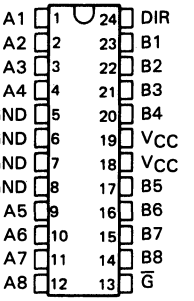
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

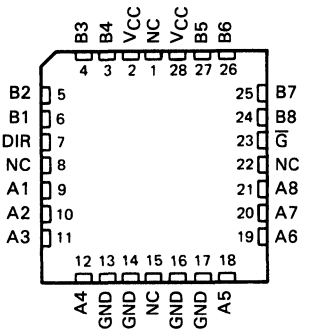
D2957, JULY 1987—REVISED MAY 1988

- 3-State Outputs Drive Bus Lines Directly
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11245 . . . JT PACKAGE
74AC11245 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11245 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

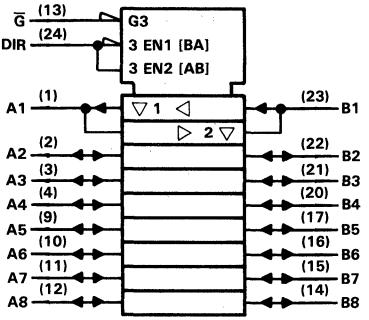
The 54AC11245 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

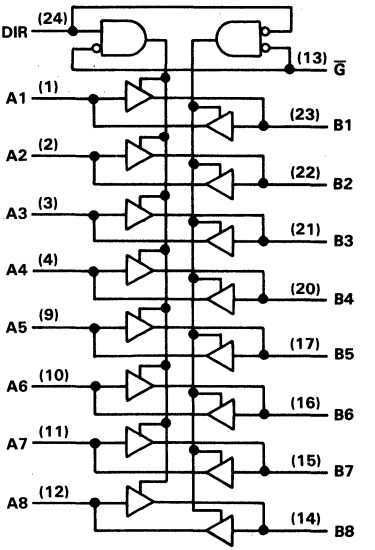
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11245			74AC11245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11245		74AC11245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
	$\overline{G}$ or DIR					±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i		V_I = V_{CC} or GND	5 V		4						pF
C_{io}		V_O = V_{CC} or GND	5 V		12						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡For I/O ports, the parameter I_I includes the off-state output current.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	64	pF
	Outputs disabled		16	

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

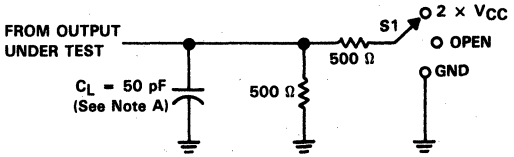
switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11245		74AC11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.5	11.2	1.5	13.3	1.5	12.5	ns
t_{PHL}			1.5	5.7	8.5	1.5	10.3	1.5	9.7	
t_{PZH}	$\overline{G}$	B or A	1.5	8.6	14.2	1.5	17.1	1.5	15.9	ns
t_{PZL}			1.5	8.2	11.5	1.5	13.7	1.5	12.7	
t_{PHZ}	$\overline{G}$	B or A	1.5	7.7	10.5	1.5	11.9	1.5	11.3	ns
t_{PLZ}			1.5	8.5	12	1.5	13.8	1.5	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

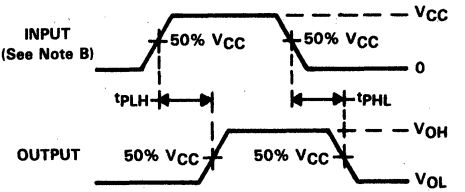
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11245		74AC11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	4.8	8.5	1.5	10.2	1.5	9.5	ns
t_{PHL}			1.5	4.1	6.3	1.5	7.4	1.5	6.9	
t_{PZH}	$\overline{G}$	B or A	1.5	6.2	10.2	1.5	12.4	1.5	11.4	ns
t_{PZL}			1.5	5.9	8.6	1.5	10.3	1.5	9.5	
t_{PHZ}	$\overline{G}$	B or A	1.5	6.4	8.8	1.5	10	1.5	9.5	ns
t_{PLZ}			1.5	7	9.6	1.5	11	1.5	10.4	

PARAMETER MEASUREMENT INFORMATION

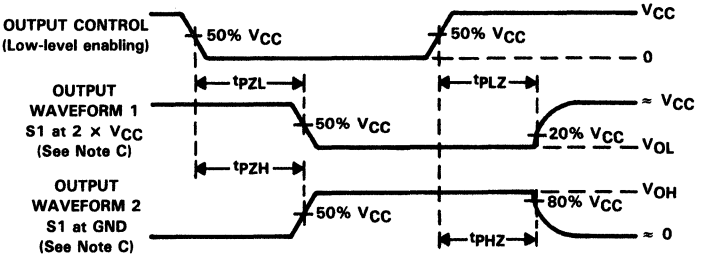


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

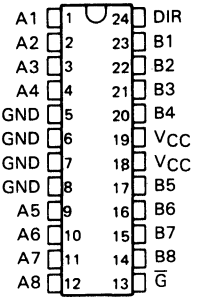
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

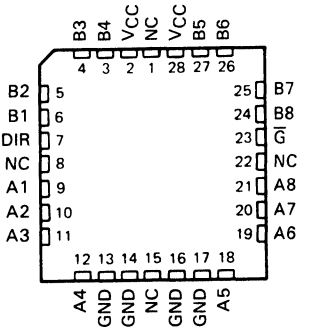
D2957, JULY 1987—REVISED AUGUST 1988

- **3-State Outputs Drive Bus Lines Directly**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11245 . . . JT PACKAGE
74ACT11245 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11245 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

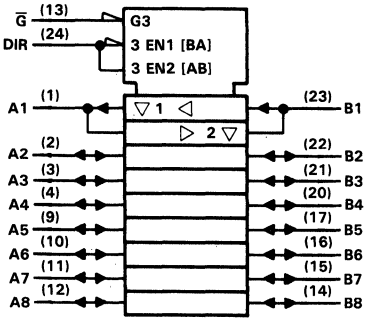
The 54ACT11245 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

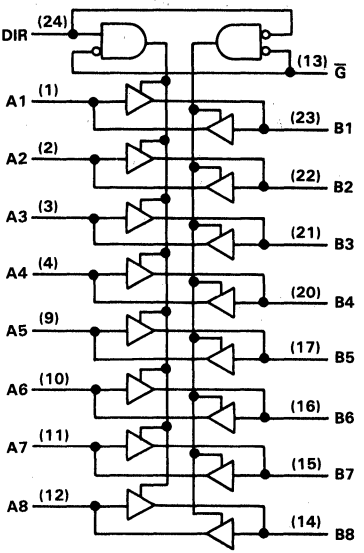
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

		54ACT11245		74ACT11245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_{io}	V_{IO} = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

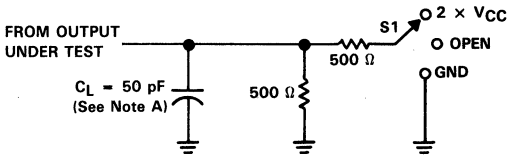
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.2	9.2	1.5	10.6	1.5	10	ns
t_{PHL}			1.5	5.4	8.6	1.5	9.6	1.5	9.1	
t_{PZH}	$\overline{G}$	A or B	1.5	8.1	12	1.5	14.1	1.5	13.2	
t_{PZL}			1.5	8.2	11.7	1.5	13.7	1.5	12.9	
t_{PHZ}	$\overline{G}$	A or B	1.5	9.3	11.8	1.5	13.6	1.5	12.9	
t_{PLZ}			1.5	9.8	12.9	1.5	14.6	1.5	13.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

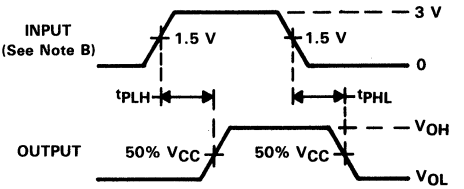
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	66	pF
		Outputs disabled		19	

PARAMETER MEASUREMENT INFORMATION

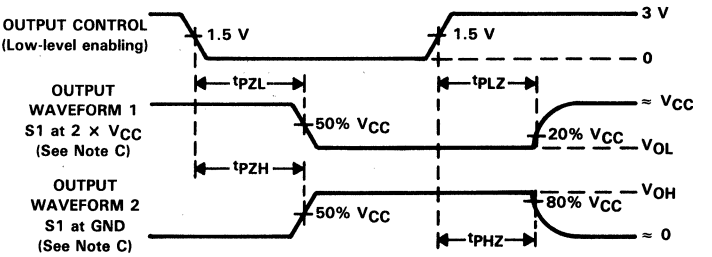


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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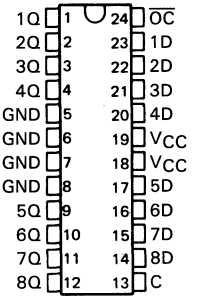
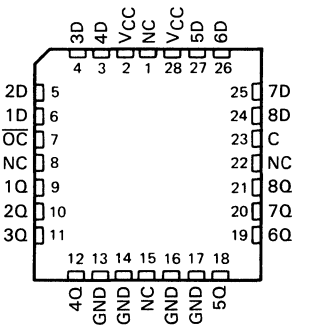
D2957, MAY 1987—REVISED JANUARY 1988

- 8 Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11373 . . . JT PACKAGE
74AC11373 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11373 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'AC11373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

FUNCTION TABLE (EACH LATCH)

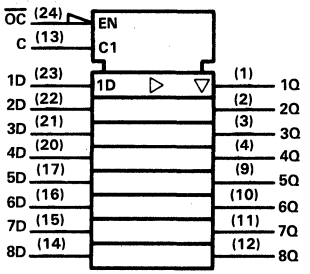
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54AC11373 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11373 is characterized for operation from −40°C to 85°C.

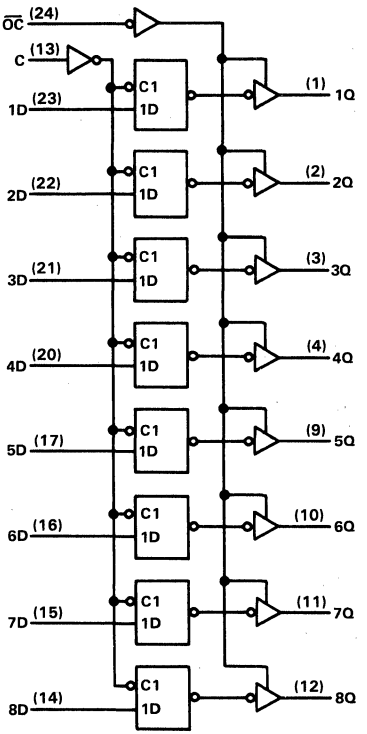
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

			54AC11373			74AC11373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	$\overline{OC}$	0		5	0		5	ns/V
		Data, C	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

	V_{CC}	T_A = 25°C		54AC11373		74AC11373		UNIT
	RANGE	MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, enable C high	3.3 ±0.3 V	5.5		5.5		5.5		ns
	5 ±0.5 V	4		4		4		
t_{su} Setup time, data before enable C↓	3.3 ±0.3 V	4		4		4		ns
	5 ±0.5 V	3.5		3.5		3.5		
t_h Hold time data after enable C ↓	3.3 ±0.3 V	2		2		2		ns
	5 ±0.5 V	2		2		2		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			54AC11373		74AC11373		UNIT
			RANGE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.3 ±0.3 V	1.5	9	13.1	1.5	15.7	1.5	14.8	ns
			5 ±0.5 V	1.5	6	8.9	1.5	11.1	1.5	10.3	
t_{PHL}			3.3 ±0.3 V	1.5	8	10.6	1.5	12.4	1.5	11.7	
			5 ±0.5 V	1.5	5.5	7.6	1.5	9.1	1.5	8.4	
t_{PLH}	C	Any Q	3.3 ±0.3 V	1.5	10	14.5	1.5	17.4	1.5	16.3	ns
			5 ±0.5 V	1.5	6.5	10	1.5	12.1	1.5	11.3	
t_{PHL}			3.3 ±0.3 V	1.5	9.5	12.8	1.5	15.2	1.5	14.2	
			5 ±0.5 V	1.5	6.5	9.1	1.5	11	1.5	10.2	
t_{PZH}	$\overline{OC}$	Any Q	3.3 ±0.3 V	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
			5 ±0.5 V	1.5	6.5	9.5	1.5	11.6	1.5	10.8	
t_{PZL}			3.3 ±0.3 V	1.5	8.5	11.6	1.5	14.1	1.5	13.1	
			5 ±0.5 V	1.5	6	8.6	1.5	10.9	1.5	9.7	
t_{PHZ}	$\overline{OC}$	Any Q	3.3 ±0.3 V	1.5	9.5	12	1.5	13.1	1.5	12.7	ns
			5 ±0.5 V	1.5	8.5	10.6	1.5	11.5	1.5	11.1	
t_{PLZ}			3.3 ±0.3 V	1.5	7.5	10.2	1.5	11.3	1.5	10.8	
			5 ±0.5 V	1.5	6	8.2	1.5	9.1	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
	Outputs disabled		36	

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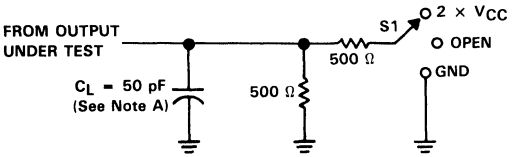
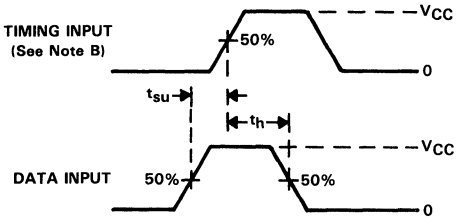
PARAMETER MEASUREMENT INFORMATION

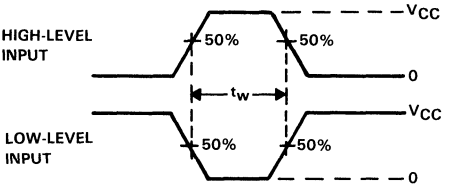


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

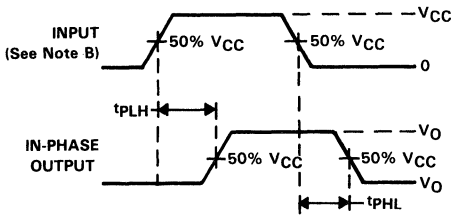
LOAD CIRCUIT



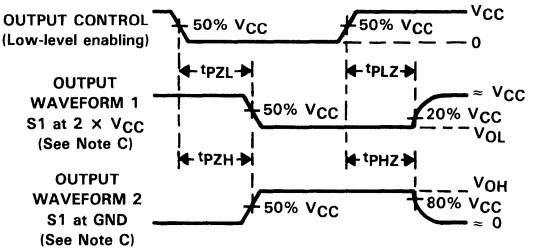
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D2957, JUNE 1987

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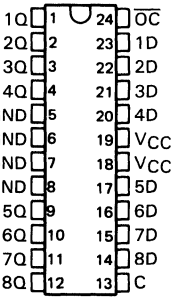
54ACT11373 . . . JT PACKAGE
74ACT11373 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11373 . . . FK PACKAGE
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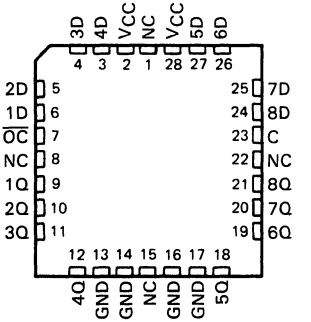

NC—No internal connection

description

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A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

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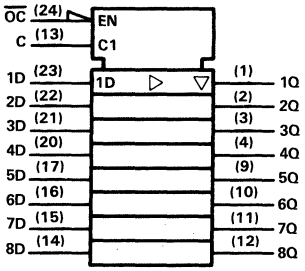
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE (EACH LATCH)

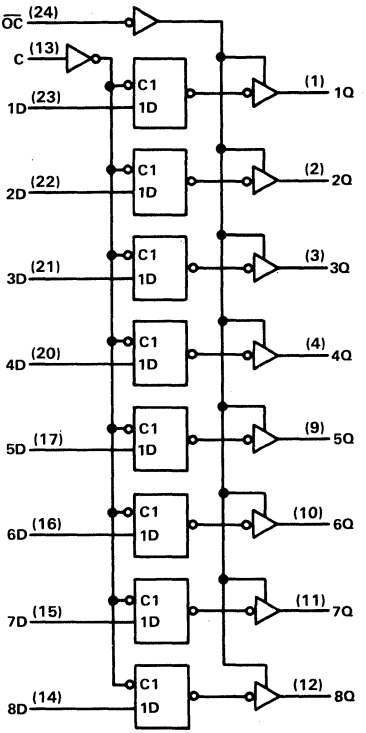
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TEXAS INSTRUMENTS
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recommended operating conditions

		54ACT11373		74ACT11373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ±0.5 V (see Figure 1)

	T_A = 25°C		54ACT11373		74ACT11373		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, enable C high	5		5		5		ns
t_{su} Setup time, data before enable C↓	3.5		3.5		3.5		ns
t_h Hold time data after enable C ↓	3.5		3.5		3.5		ns

switching characteristics, V_{CC} = 5 V ±0.5 V(see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	7.5	10.3	1.5	12.7	1.5	11.8	ns
t_{PHL}			1.5	6.5	9.3	1.5	10.6	1.5	10	
t_{PLH}	C	Any Q	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
t_{PHL}			1.5	8.5	10.9	1.5	13	1.5	12.2	
t_{PZH}	$\overline{OC}$	Any Q	1.5	7	10.7	1.5	13.6	1.5	12.5	ns
t_{PZL}			1.5	7.5	10.9	1.5	12.9	1.5	12	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	10	12.1	1.5	12.7	1.5	12.5	ns
t_{PLZ}			1.5	7.5	9.5	1.5	10.5	1.5	10.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	65	pF
		Outputs disabled		54	

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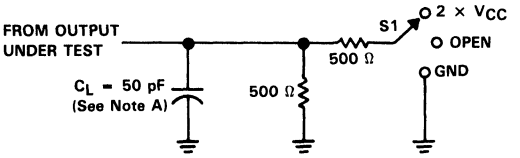
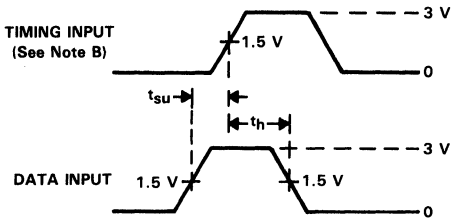
PARAMETER MEASUREMENT INFORMATION

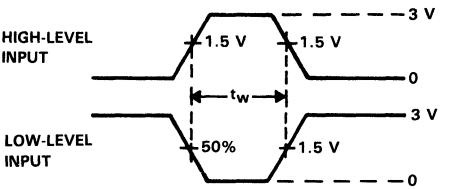


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

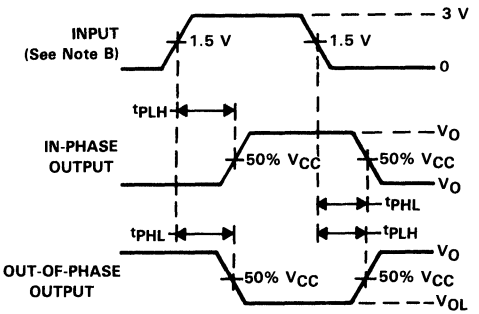
LOAD CIRCUIT



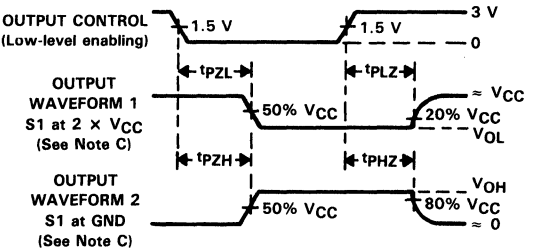
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

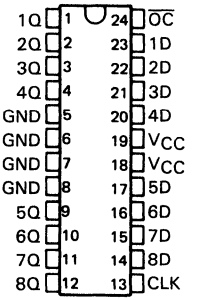
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

Advanced CMOS Circuits

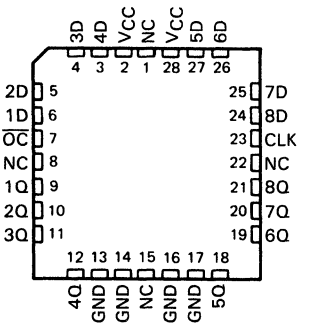
D2957, JULY 1987—REVISED DECEMBER 1987

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11374 . . . JT PACKAGE
74AC11374 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11374 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'AC11374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state provides the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

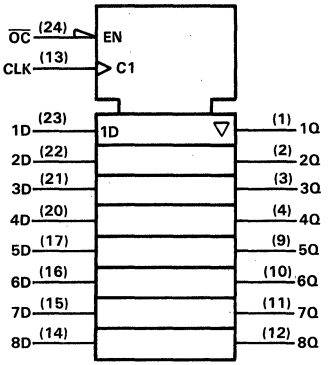
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
L	↓	X	Q_0
H	X	X	Z

The 54AC11374 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11374 is characterized for operation from −40°C to 85°C.

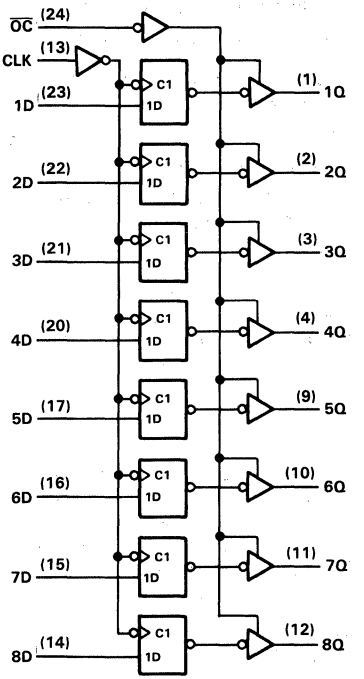
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

			54AC11374			74AC11374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		$\overline{OC}$	0		5	0		5	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11374		74AC11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

timing requirements (see Figure 1)

			V_{CC} RANGE	T_A = 25°C		54AC11374		74AC11374		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		3.3 ± 0.3 V	0	75	0	75	0	75	MHz
			5 ± 0.5 V	0	95	0	95	0	95	
t_w	Pulse duration	CLK low or CLK high	3.3 ± 0.3 V	6.5		6.5		6.5		ns
			5 ± 0.5 V	5		5		5		
t_{su}	Setup time data before CLK↑		3.3 ± 0.3 V	2.5		2.5		2.5		ns
			5 ± 0.5 V	2.5		2.5		2.5		
t_h	Hold time data after CLK↑		3.3 ± 0.3 V	4.5		4.5		4.5		ns
			5 ± 0.5 V	3.5		3.5		3.5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11374		74AC11374		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			3.3 + 0.3 V	75	90		75		75		MHz
			5 ± 0.5 V	95	110		95		95		
t_{PLH}	CLK	Any Q	3.3 ± 0.3 V	1.5	9.5	12.5	1.5	15.2	1.5	14.2	ns
			5 ± 0.5 V	1.5	6.5	9	1.5	10.9	1.5	10.2	
t_{PHL}			3.3 ± 0.3 V	1.5	9	12.6	1.5	14.9	1.5	14	
			5 ± 0.5 V	1.5	5.5	9.1	1.5	10.8	1.5	10.1	
t_{PZH}	$\overline{OC}$	Any Q	3.3 ± 0.3 V	1.5	8	10.9	1.5	13.3	1.5	12.3	ns
			5 ± 0.5 V	1.5	5.5	8	1.5	9.8	1.5	9.1	
t_{PZL}			3.3 ± 0.3 V	1.5	8	11.1	1.5	13.2	1.5	12.3	
			5 ± 0.5 V	1.5	5.5	8.4	1.5	10.2	1.5	9.4	
t_{PHZ}	$\overline{OC}$	Any Q	3.3 ± 0.3 V	1.5	10	12.1	1.5	12.9	1.5	12.5	ns
			5 ± 0.5 V	1.5	9	11	1.5	11.4	1.5	11.2	
t_{PLZ}			3.3 ± 0.3 V	1.5	8	10.7	1.5	12.1	1.5	11.6	
			5 ± 0.5 V	1.5	6	8.6	1.5	9.6	1.5	9.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	75	pF
		Outputs disabled		66	

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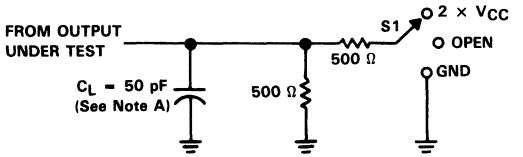
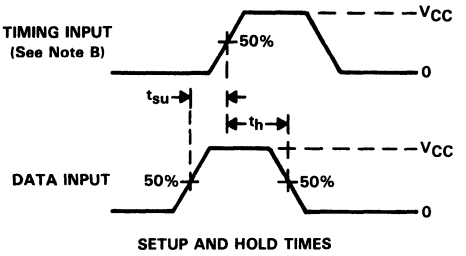
PARAMETER MEASUREMENT INFORMATION

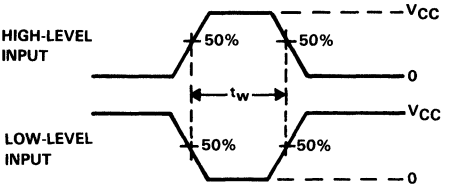


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

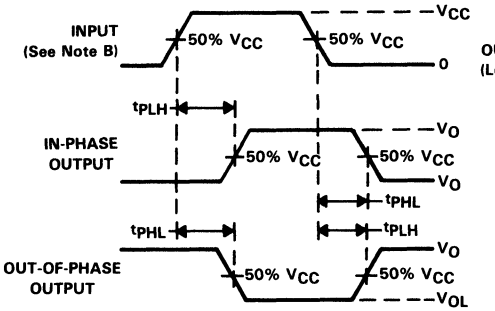
LOAD CIRCUIT



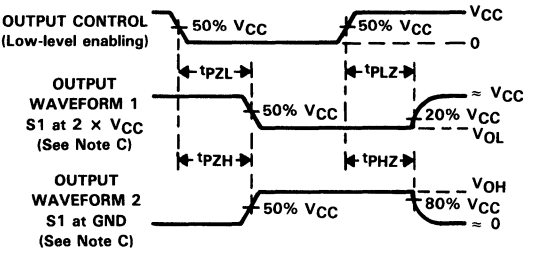
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

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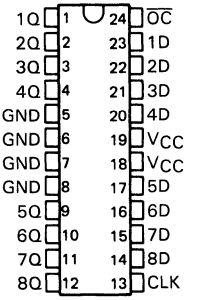
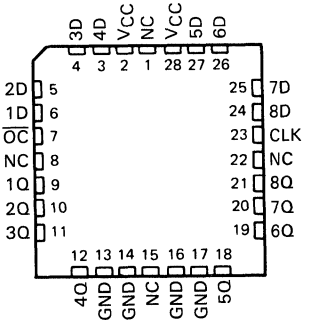
54ACT11374 . . . JT PACKAGE
74ACT11374 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11374 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

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An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state provides the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

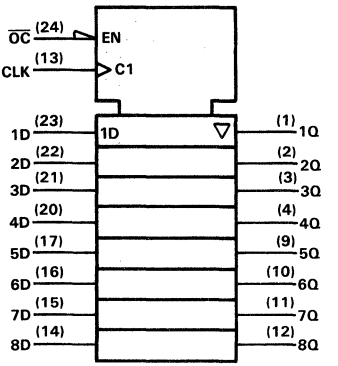
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
L	↓	X	Q_0
H	X	X	Z

The 54ACT11374 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11374 is characterized for operation from −40°C to 85°C.

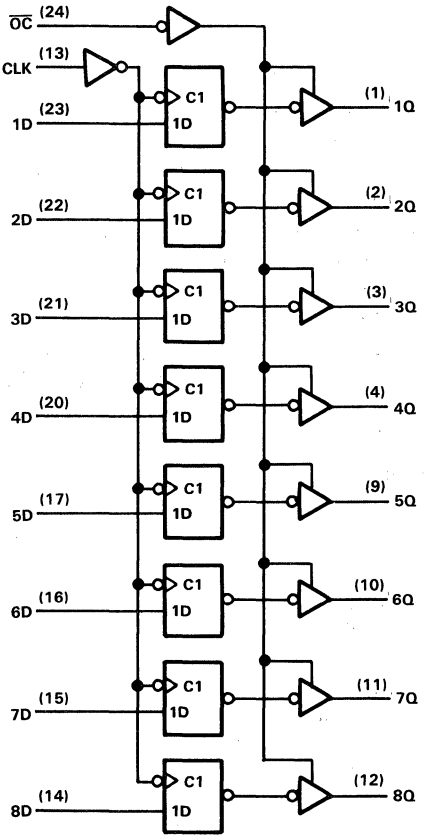
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TEXAS INSTRUMENTS
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recommended operating conditions

		54ACT11374		74ACT11374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11374		74ACT11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ±0.5 V (see Figure 1)

		T_A = 25°C		54ACT11374		74ACT11374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	55	0	55	0	55	MHz
t_w	Pulse duration, enable C high	9		9		9		ns
t_{su}	Setup time, data before enable C↓	3		3		3		ns
t_h	Hold time data after enable C ↓	5.5		5.5		5.5		ns

switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11374		74ACT11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			55	70		55		55		MHz
t_{PLH}	CLK	Any Q	1.5	8.5	10.7	1.5	13.3	1.5	12.4	ns
t_{PHL}			1.5	8.5	11.3	1.5	13.9	1.5	13	
t_{PZH}	$\overline{OC}$	Any Q	1.5	7.5	11	1.5	13.2	1.5	12.3	ns
t_{PZL}			1.5	7.5	11	1.5	13.2	1.5	12.3	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	11	12.7	1.5	13.6	1.5	13.2	ns
t_{PLZ}			1.5	8	10	1.5	11.3	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	107	pF
		Outputs disabled		96	

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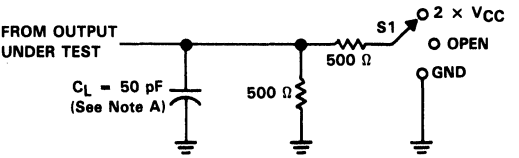
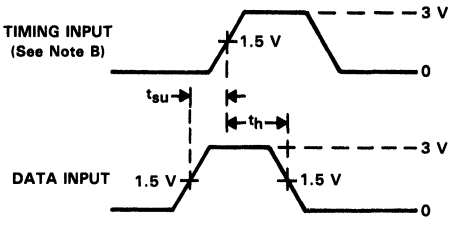
PARAMETER MEASUREMENT INFORMATION

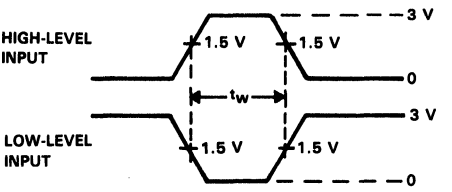


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

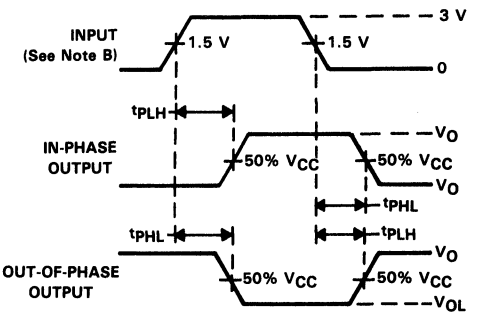
LOAD CIRCUIT



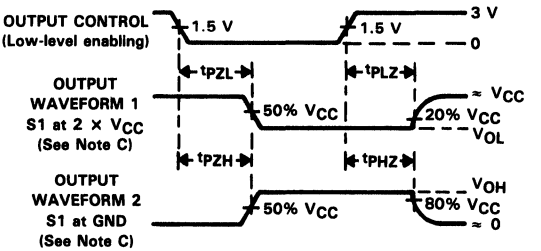
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

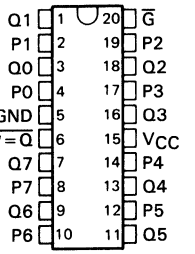
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

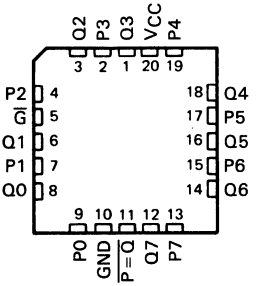
D2957, JULY 1987—REVISED AUGUST 1987

- **Compares Two 8-Bit Words**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **The Device has the Equivalent of 20-kΩ Pull-up Resistor on Q Inputs**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11520 . . . . J PACKAGE
74AC11520 . . . . DW OR N PACKAGE
(TOP VIEW)



54AC11520. . . . FK PACKAGE
(TOP VIEW)



description

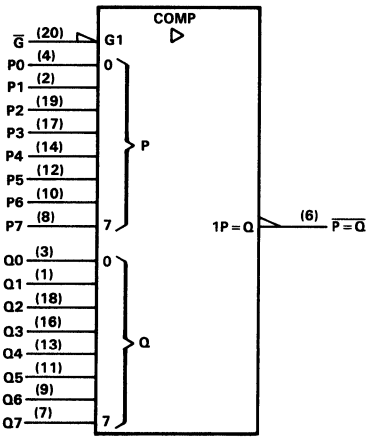
These identity comparators perform comparisons on two 8-bit binary or BCD words. Features include: 20-k ohm pull-up termination resistors on the Q inputs for analog or switch data, provision for $\overline{P = Q}$ totem-pole outputs.

The 54AC11520 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11520 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$\overline{P = Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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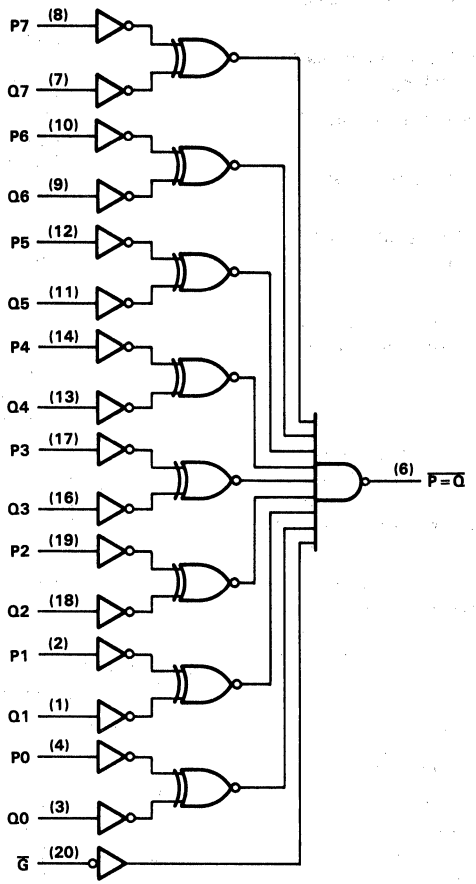
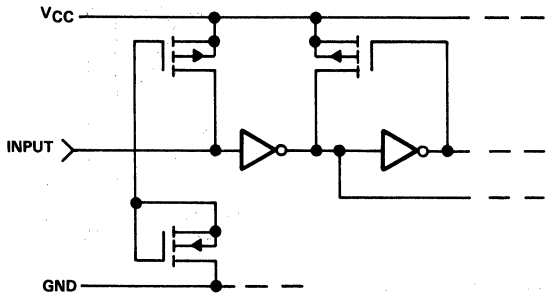
logic diagram (positive logic)



schematic of Q inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11520			74AC11520			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11520		74AC11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9	2.9		2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{IH}	V_I = V_{CC}, Q inputs only	5.5 V			10		10		10	μA
I_{IL}	V_I = GND, Q inputs only	5.5 V		−0.3	−0.6		−1		−1	mA
I_I	V_I = V_{CC} or GND, P and $\overline{G}$ inputs only	5.5 V			±0.1		±1		±1	μA
I_{CC}	Q inputs at GND Other inputs V_I = V_{CC} or GND	5.5 V		2.3	4.8		8		8	mA
	Q inputs open Other inputs V_I = V_{CC} or GND	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output or input should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			54AC11520		74AC11520		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	3.3 ± 0.3 V	1.5	12	16.5	1.5	20.1	1.5	18.6	ns
			5 ± 0.5 V	1.5	8.1	11.1	1.5	13.7	1.5	12.6	
t_{PHL}			3.3 ± 0.3 V	1.5	10.4	14.4	1.5	17.6	1.5	16.3	ns
			5 ± 0.5 V	1.5	7.1	10.1	1.5	12.3	1.5	11.3	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	3.3 ± 0.3 V	1.5	6.9	9	1.5	10.8	1.5	10	ns
			5 ± 0.5 V	1.5	4.9	6.6	1.5	8	1.5	7.4	
t_{PHL}			3.3 ± 0.3 V	1.5	6.3	8.6	1.5	10.2	1.5	9.5	ns
			5 ± 0.5 V	1.5	4.8	7.1	1.5	8.2	1.5	7.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	42	pF

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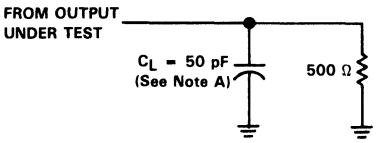
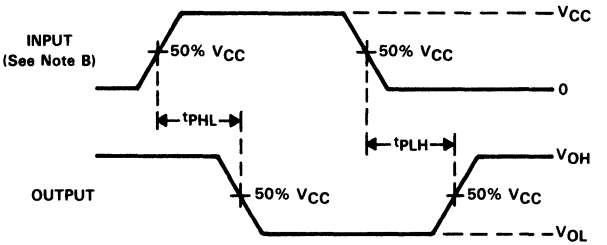
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

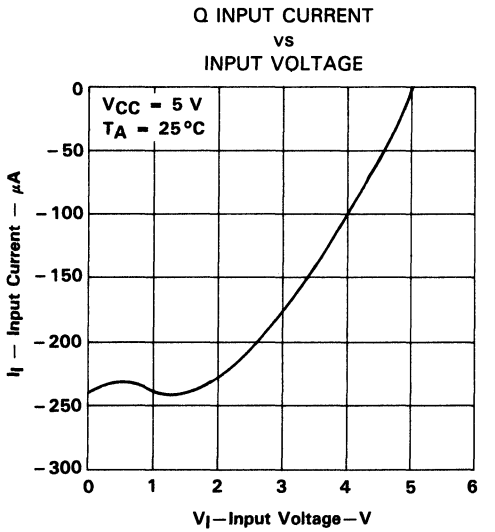


FIGURE 2

D2957, JULY 1987—REVISED AUGUST 1987

- **Compares Two 8-Bit Words**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
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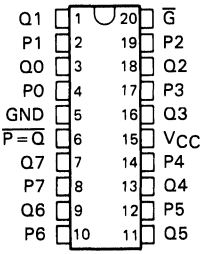
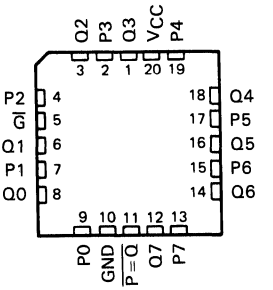
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11520 . . . J PACKAGE
74ACT11520 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11520. . . . FK PACKAGE
(TOP VIEW)



description

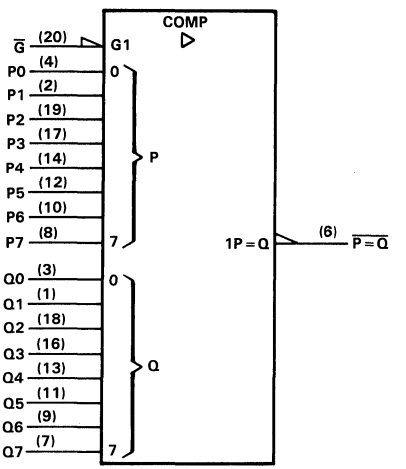
These identity comparators perform comparisons on two 8-bit binary or BCD words. Features include: 20-k ohm pull-up termination resistors on the Q inputs for analog or switch data, provision for $\overline{P = Q}$ totem-pole outputs.

The 54ACT11520 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11520 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$\overline{P = Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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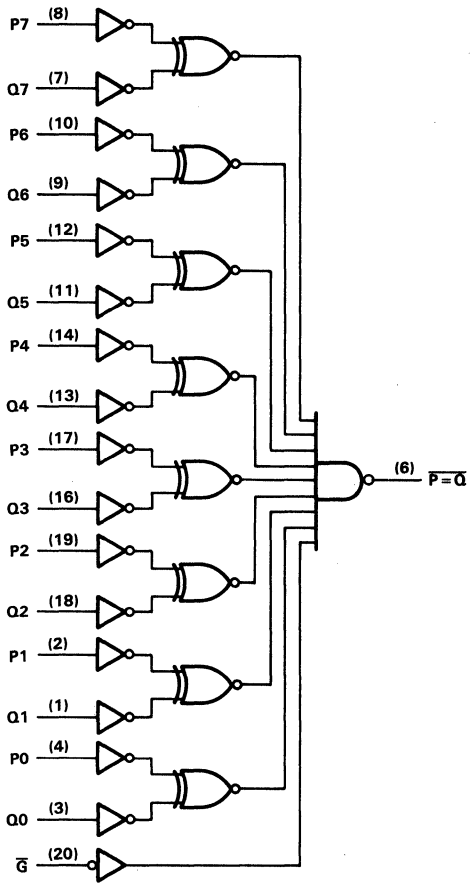
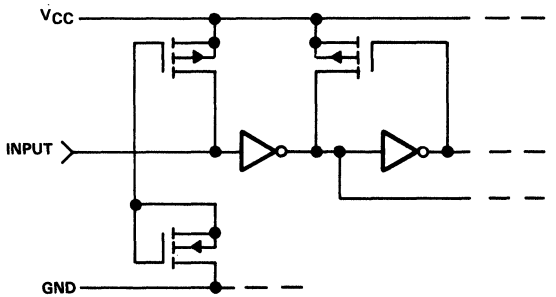
logic diagram (positive logic)



schematic of Q inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11520			74ACT11520			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11520		74ACT11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{IH}	V_I = V_{CC}, Q inputs only	5.5 V			10		10		10	μA
I_{IL}	V_I = GND, Q inputs only	5.5 V		−0.3	−0.6		−1		−1	mA
I_I	V_I = V_{CC} or GND, P and $\overline{G}$ inputs only	5.5 V			±0.1		±1		±1	μA
I_{CC}	Q inputs at GND Other inputs V_I = V_{CC} or GND	5.5 V		2.3	4.8		8		8	mA
	Q inputs open Other inputs V_I = V_{CC} or GND	5.5 V			8		160		80	μA
ΔI_{CC}‡	Q inputs open One input at 3.4 V and other inputs at V_{CC} or GND, P and $\overline{G}$ inputs only	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11520		74ACT11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	1.5	8.6	12.7	1.5	15.4	1.5	14.3	ns
t_{PHL}			1.5	8	12.4	1.5	14.8	1.5	13.9	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	1.5	6.4	8.5	1.5	10.2	1.5	9.5	ns
t_{PHL}			1.5	5.8	9	1.5	10.4	1.5	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	40	pF

TEXAS INSTRUMENTS
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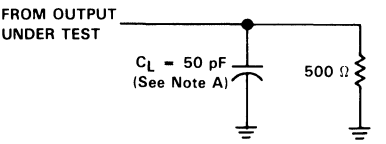
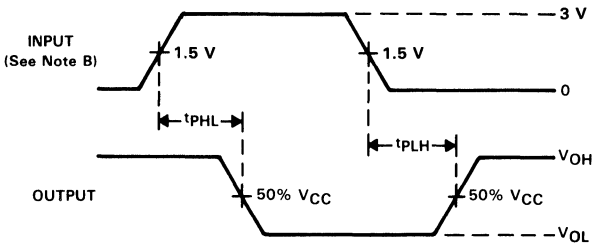
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

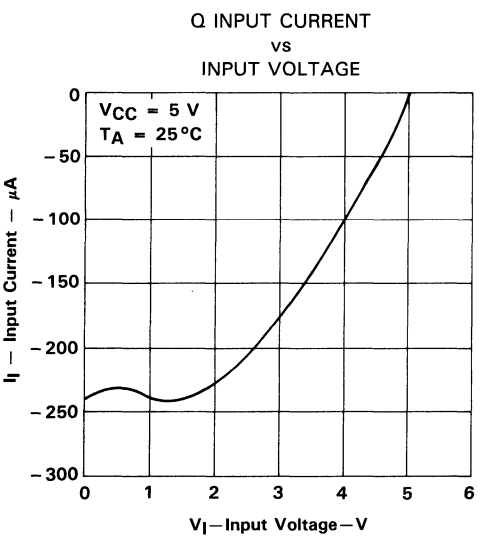


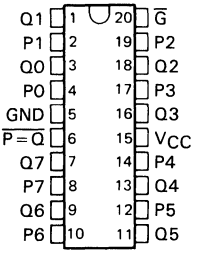
FIGURE 2

2 Advanced CMOS Circuits

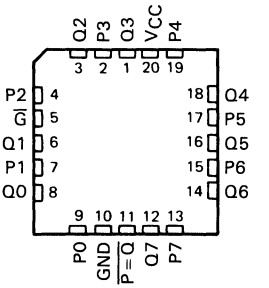
D2957, JULY 1987—REVISED SEPTEMBER 1987

- **Compares Two 8-Bit Words**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11521 . . . J PACKAGE
74AC11521 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11521. . . . FK PACKAGE
(TOP VIEW)



description

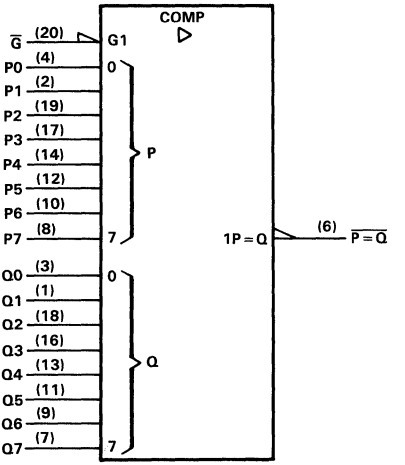
These identity comparators perform comparisons on two 8-bit binary or BCD words. Also included is a provision for $\overline{P = Q}$ totem-pole outputs.

The 54AC11521 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11521 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$\overline{P = Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

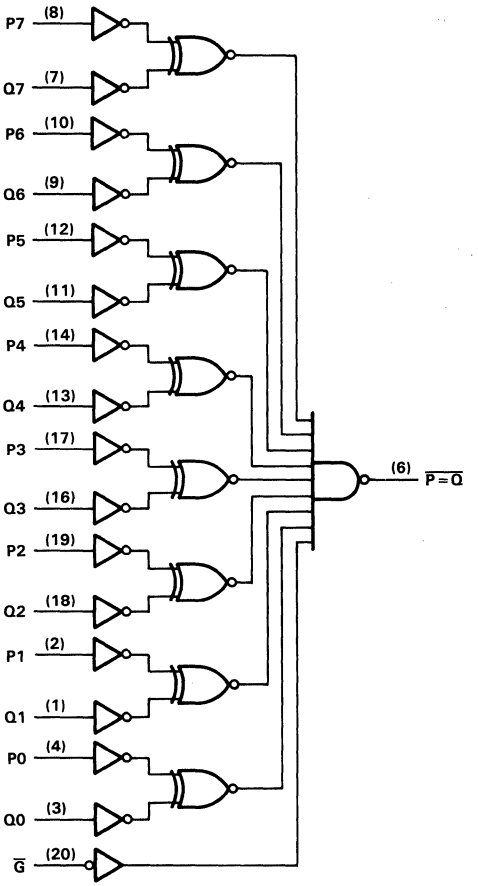
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±100 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11521			74AC11521			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11521		74AC11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

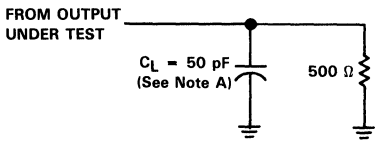
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			54AC11521		74AC11521		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	3.3 ± 0.3 V	1.5	12.5	16.6	1.5	20.4	1.5	19	ns
			5 ± 0.5 V	1.5	8.3	11.3	1.5	14	1.5	13	
t_{PHL}			3.3 ± 0.3 V	1.5	10.5	14.1	1.5	17.4	1.5	16.1	ns
			5 ± 0.5 V	1.5	7.2	10.1	1.5	12.2	1.5	11.4	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	3.3 ± 0.3 V	1.5	7.1	9.8	1.5	11.4	1.5	10.8	ns
			5 ± 0.5 V	1.5	5.1	7.1	1.5	8.4	1.5	7.9	
t_{PHL}			3.3 ± 0.3 V	1.5	6.4	8.8	1.5	10.8	1.5	10.1	ns
			5 ± 0.5 V	1.5	4.8	7.1	1.5	8.6	1.5	8.1	

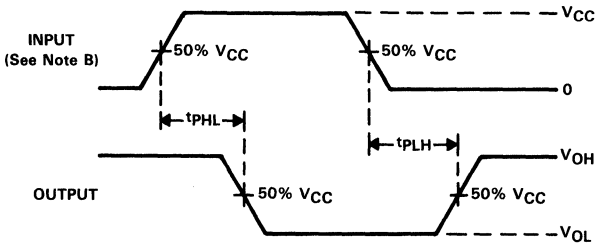
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	42	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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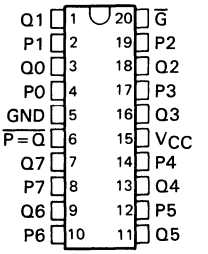
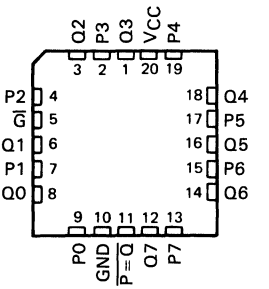
D2957, JULY 1987—REVISED SEPTEMBER 1987

- **Compares Two 8-Bit Words**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11521 . . . J PACKAGE
74ACT11521 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11521. . . .FK PACKAGE
(TOP VIEW)



description

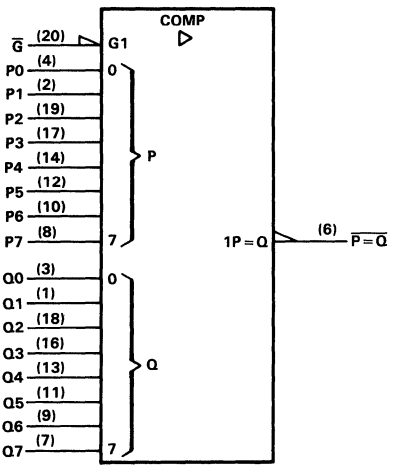
These identity comparators perform comparisons on two 8-bit binary or BCD words. Also included is a provision for $\overline{P = Q}$ totem-pole outputs.

The 54ACT11521 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11521 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	$\overline{P = Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

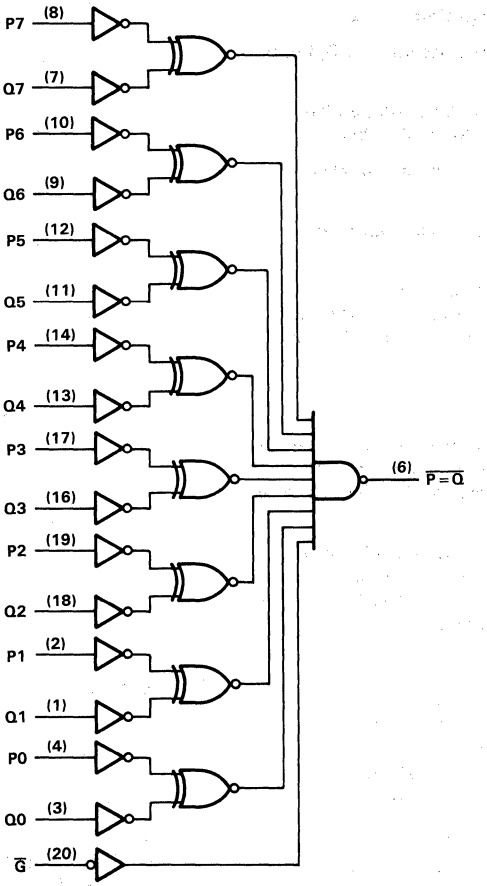
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11521			74ACT11521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11521		74ACT11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

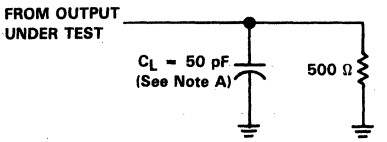
switching characteristics V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11521		74ACT11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	1.5	8.8	13	1.5	15.9	1.5	14.7	ns
t_{PHL}			1.5	8.2	12	1.5	14.6	1.5	13.6	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	1.5	6.7	9.3	1.5	11.2	1.5	10.5	ns
t_{PHL}			1.5	6.8	8.8	1.5	10.2	1.5	9.7	

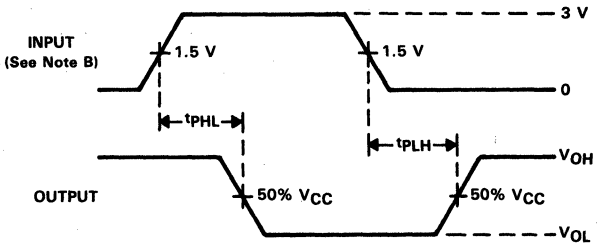
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

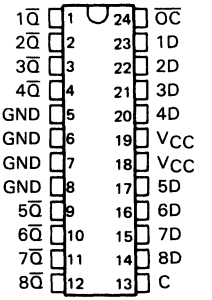
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

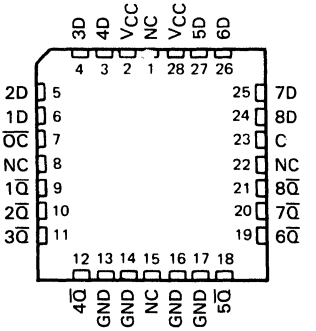
D2957, JULY 1987

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11533 . . . JT PACKAGE
74AC11533 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11533 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'AC11533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the (D) inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'AC11533 is functionally equivalent to the 'AC11373 except for having inverted outputs.

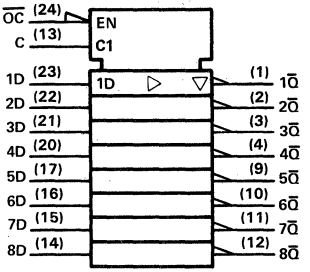
A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54AC11533 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11533 is characterized for operation from 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated

logic symbol†

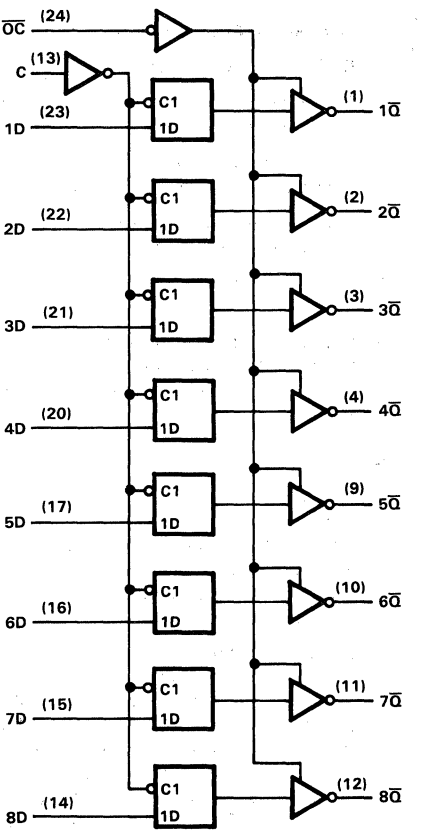


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TEXAS INSTRUMENTS
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recommended operating conditions

			54AC11533			74AC11533			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5.5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

		V_{CC} RANGE	T_A = 25°C MIN	T_A = 25°C MAX	54AC11533 MIN	54AC11533 MAX	74AC11533 MIN	74AC11533 MAX	UNIT
t_w	Pulse duration, enable C high	3.3 ± 0.3 V	5.5		5.5		5.5		ns
		5 ± 0.5 V	4		4		4		
t_{su}	Setup time, data before enable C↓	3.3 ± 0.3 V	4		4		4		ns
		5 ± 0.5 V	3.5		3.5		3.5		
t_h	Hold time, data after enable C↓	3.3 ± 0.3 V	2		2		2		ns
		5 ± 0.5 V	2		2		2		

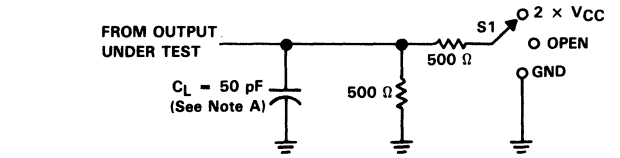
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	54AC11533 MIN	54AC11533 MAX	74AC11533 MIN	74AC11533 MAX	UNIT
t_{PLH}	D	$\overline{Q}$	3.3 ±0.3 V	1.5	8.5	12.6	1.5	15.2	1.5	14.3	ns
			5 ±0.5 V	1.5	5.5	8.4	1.5	10.6	1.5	9.8	
t_{PHL}			3.3 ±0.3 V	1.5	7.5	10.1	1.5	12	1.5	11.3	
			5 ±0.5 V	1.5	5	7.1	1.5	8.6	1.5	8	
t_{PLH}	C	Any $\overline{Q}$	3.3 ±0.3 V	1.5	10	14.5	1.5	17.6	1.5	16.5	ns
			5 ±0.5 V	1.5	6.5	10	1.5	12.1	1.5	11.3	
t_{PHL}			3.3 ±0.3 V	1.5	9.5	12.8	1.5	15.2	1.5	14.3	
			5 ±0.5 V	1.5	6.5	9.1	1.5	11	1.5	10.3	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	3.3 ±0.3 V	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
			5 ±0.5 V	1.5	6.5	9.5	1.5	11.7	1.5	10.8	
t_{PZL}			3.3 ±0.3 V	1.5	8.5	11.6	1.5	14.1	1.5	13.1	
			5 ±0.5 V	1.5	6	8.6	1.5	10.9	1.5	9.7	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	3.3 ± 0.3 V	1.5	9.5	12	1.5	13.2	1.5	12.8	ns
			5 ± 0.5 V	1.5	8.5	10.7	1.5	11.7	1.5	11.4	
t_{PLZ}			3.3 ± 0.3 V	1.5	7.5	10.2	1.5	11.4	1.5	11	
			5 ± 0.5 V	1.5	6	8.2	1.5	9.3	1.5	8.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

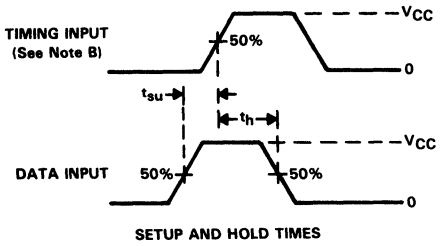
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	55	pF
		Outputs disabled		44	

PARAMETER MEASUREMENT INFORMATION

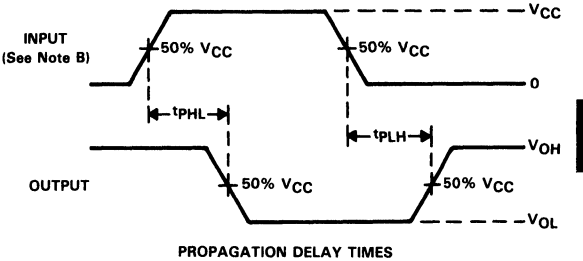


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

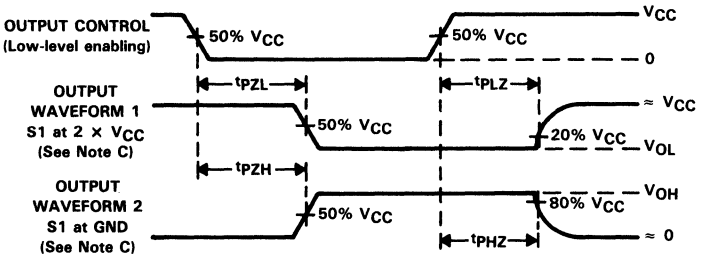
LOAD CIRCUIT



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, JULY 1987

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Inputs are TTL-Voltage Compatible
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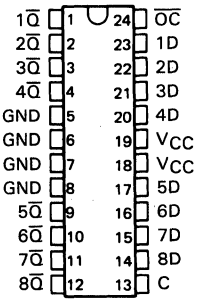
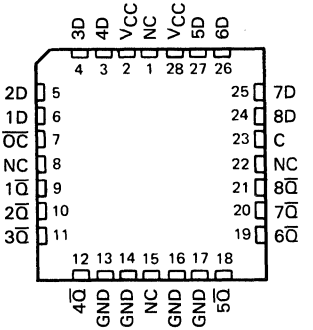
54ACT11533 . . . JT PACKAGE
74ACT11533 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11533 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ACT11533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the (D) inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'ACT11533 is functionally equivalent to the 'ACT11373 except for having inverted outputs.

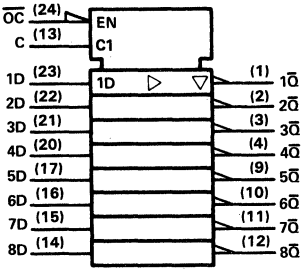
A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54ACT11533 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11533 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

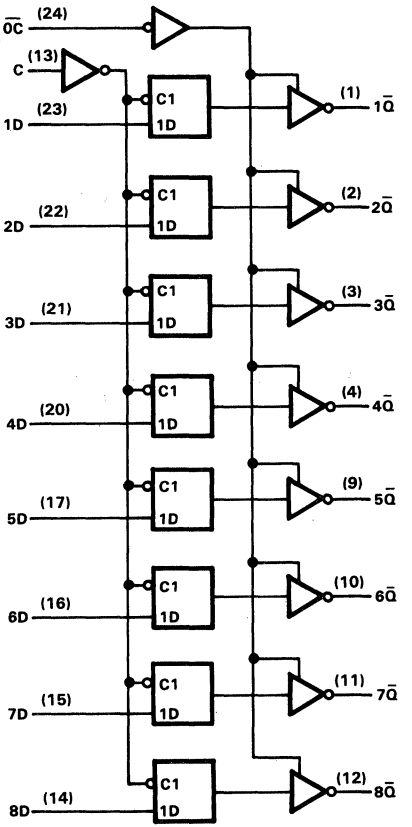


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TEXAS INSTRUMENTS
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recommended operating conditions

		54ACT11533		74ACT11533		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ±0.5 V (see Figure 1)

	T_A = 25°C		54ACT11533		74ACT11533		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration, enable C high	5		5		5		ns
t_{su} Setup time, data before enable C↓	3.5		3.5		3.5		ns
t_h Hold time data after enable C ↓	3.5		3.5		3.5		ns

switching characteristics, V_{CC} = 5 V ±0.5 V(see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	1.5	7	10.1	1.5	11.9	1.5	11.3	ns
t_{PHL}			1.5	6.5	8.4	1.5	10.2	1.5	9.5	
t_{PLH}	C	Any Q	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
t_{PHL}			1.5	8.5	10.7	1.5	13.2	1.5	12.2	
t_{PZH}	$\overline{OC}$	Any Q	1.5	7.5	10.7	1.5	13.6	1.5	12.5	ns
t_{PZL}			1.5	7.5	10.9	1.5	12.9	1.5	12	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	10.5	12.1	1.5	13.1	1.5	12.8	ns
t_{PLZ}			1.5	7.5	9.5	1.5	10.7	1.5	10.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	69	pF
		Outputs disabled		58	

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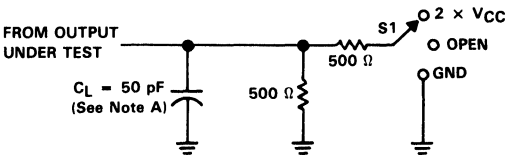
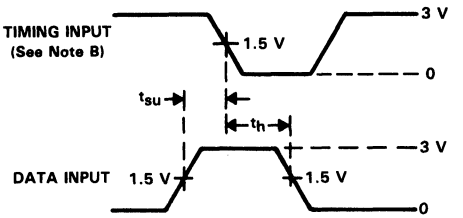
PARAMETER MEASUREMENT INFORMATION

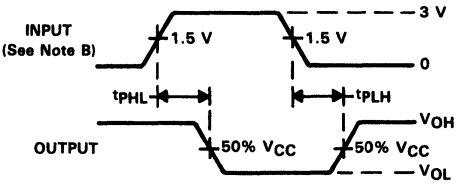


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

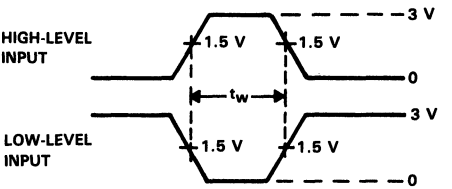
LOAD CIRCUIT



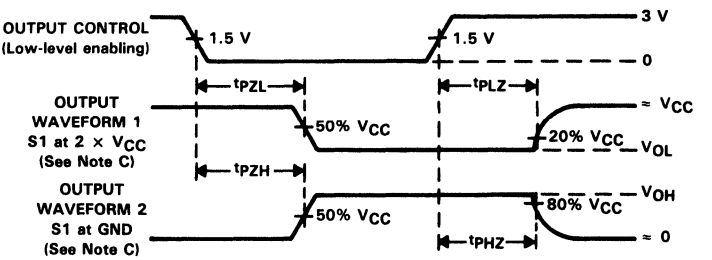
SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



PULSE DURATION



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus Driving Inverting Outputs
- Full Parallel Access for Loading
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

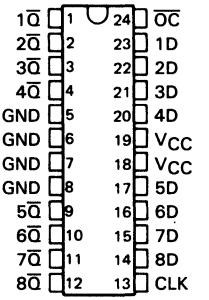
These 8-bit flip-flops feature 3-state outputs designed for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AC11534 are edge-triggered, D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the logic levels that were set up at the D inputs. The AC11534 is functionally equivalent to the AC11374 except for having inverted outputs.

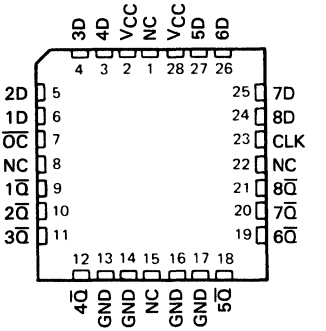
An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 54AC11534 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11534 is characterized for operation from −40°C to 85°C.

54AC11534 . . . JT PACKAGE
74AC11534 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11534 . . . FK PACKAGE
(TOP VIEW)



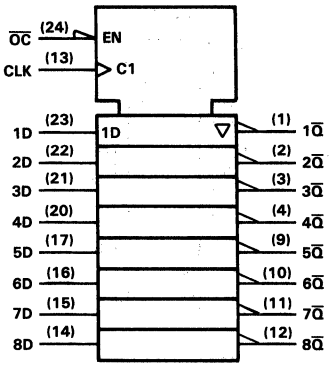
NC—No internal connection

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

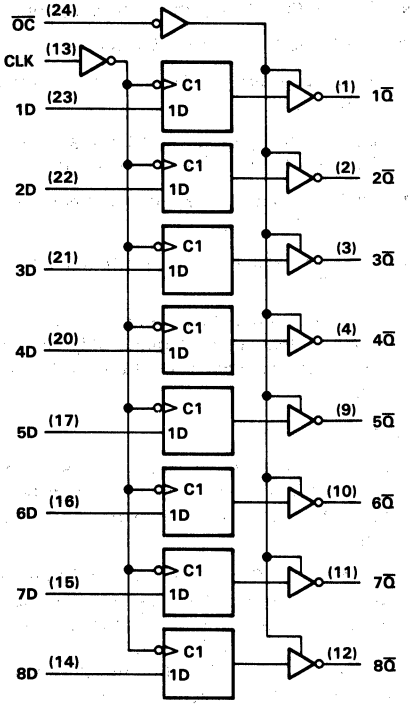
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

			54AC11534			74AC11534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OC}$	0		5	0		5	ns/V
		D	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

		T_A = 25°C		54AC11534		74AC11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	50	0	50	0	50	MHz
t_w	Pulse duration, CLK low or CLK high	10		10		10		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		3.5		ns
t_h	Hold time, data after CLK↑	5.5		5.5		5.5		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

		T_A = 25°C		54AC11534		74AC11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CLK low or CLK high	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		3.5		ns
t_h	Hold time, data after CLK↑	4.5		4.5		4.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (See Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			50	75		50		50		MHz
t_{PLH}	CLK	$\overline{Q}$	1.5	11	15.3	1.5	19.1	1.5	17.6	ns
t_{PHL}			1.5	11	15.7	1.5	19	1.5	17.7	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	1.5	9	12.8	1.5	15.8	1.5	14.6	ns
t_{PZL}			1.5	9	12.6	1.5	15.6	1.5	14.3	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	1.5	10	12.6	1.5	13.8	1.5	13.3	ns
t_{PLZ}			1.5	8	13	1.5	14.2	1.5	13.8	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (See Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75	100		75		75		MHz
t_{PLH}	CLK	$\overline{Q}$	1.5	7	10.3	1.5	12.7	1.5	11.7	ns
t_{PHL}			1.5	7	10.7	1.5	13.2	1.5	12.1	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	1.5	6	9.2	1.5	11.2	1.5	10.4	ns
t_{PZL}			1.5	6	9.2	1.5	11.3	1.5	10.4	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	1.5	9	11.1	1.5	11.9	1.5	11.6	ns
t_{PLZ}			1.5	6	8.8	1.5	9.6	1.5	9.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	75	pF
		Outputs disabled		65	

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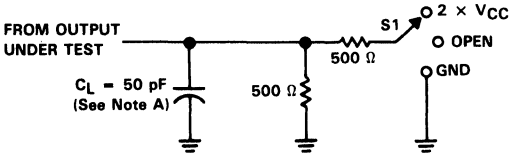
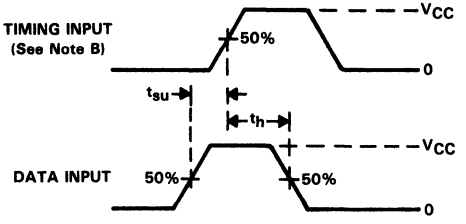
PARAMETER MEASUREMENT INFORMATION

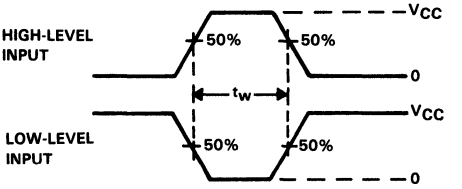


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

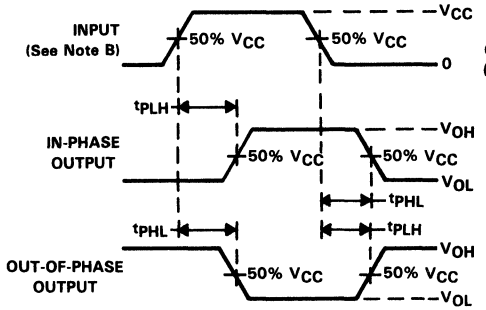
LOAD CIRCUIT



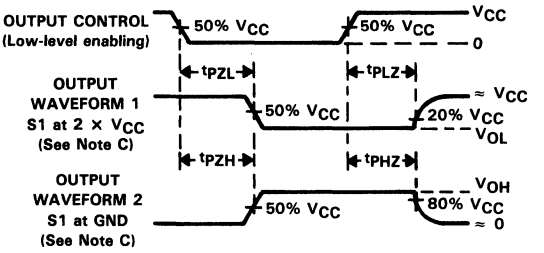
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus Driving Inverting Outputs
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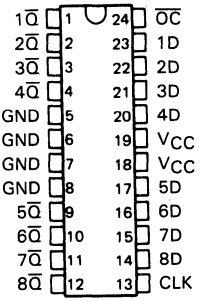
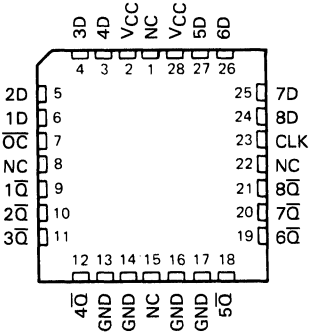
54ACT11534 . . . JT PACKAGE
74ACT11534 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11534 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 8-bit flip-flops feature 3-state outputs designed for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ACT11534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the logic levels that were set up at the D inputs. The ACT11534 is functionally equivalent to the ACT11374 except for having inverted outputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained, or new data can be entered while the outputs are in the high-impedance state.

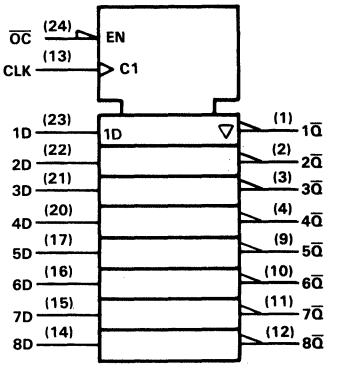
The 54ACT11534 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11534 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

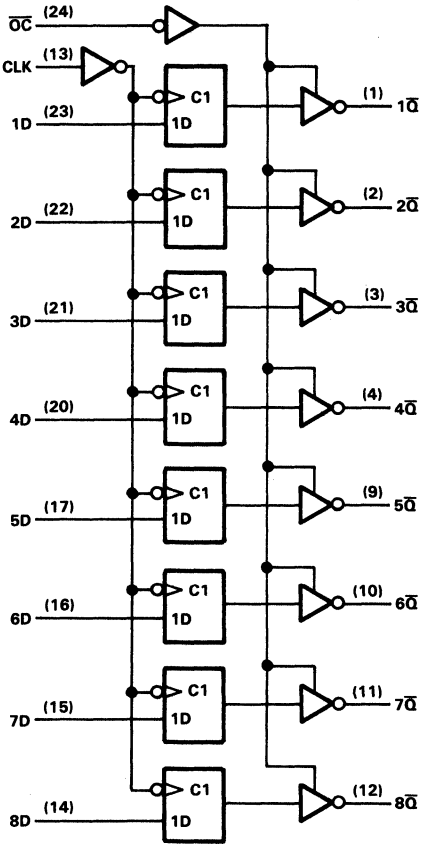
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11534		74ACT11534		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11534		74ACT11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

		T_A = 25°C		54ACT11534		74ACT11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	55	0	55	0	55	MHz
t_w	Pulse duration, CLK low or CLK high	9		9		9		ns
t_{su}	Setup time, data before CLK ↑	3		3		3		ns
t_h	Hold time, data after CLK↑	5.5		5.5		5.5		ns

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11534		74ACT11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			55	70		55		55		MHz
t_{PLH}	CLK	Any $\overline{Q}$	1.5	8.5	12.7	1.5	15.7	1.5	14.5	ns
t_{PHL}			1.5	8.5	13.3	1.5	16.3	1.5	15	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1.5	7.5	12	1.5	14.2	1.5	13.3	ns
t_{PZL}			1.5	7.5	12.2	1.5	14.5	1.5	13.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	1.5	11	12.9	1.5	13.9	1.5	13.5	ns
t_{PLZ}			1.5	8	11.2	1.5	12.5	1.5	12	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs	C_L = 50 pF, f = 1 MHz	92	pF
		Outputs disabled		82	

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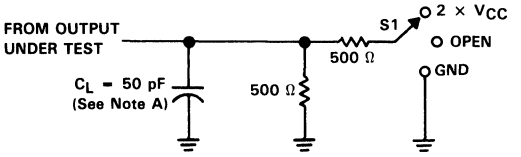
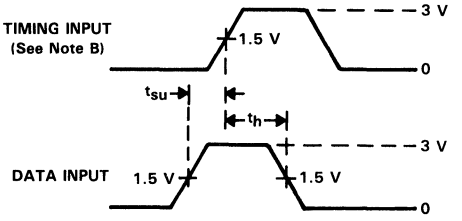
PARAMETER MEASUREMENT INFORMATION

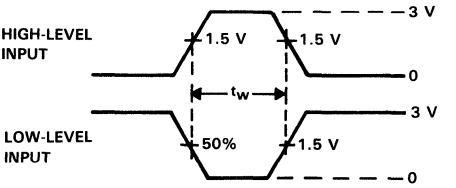


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

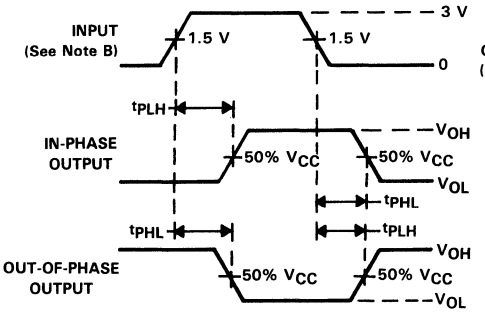
LOAD CIRCUIT



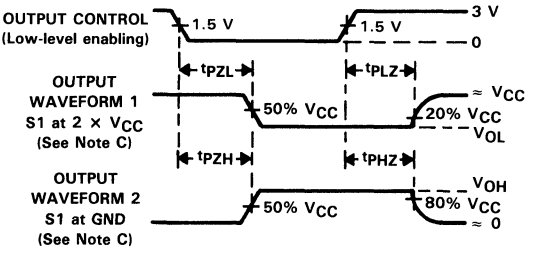
SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

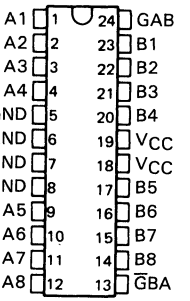
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

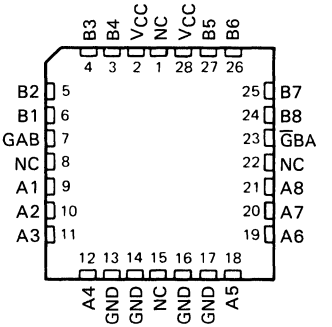
D2957, JULY 1987

- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11620 . . . JT PACKAGE
74AC11620 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11620 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the AC11620.

The 54AC11620 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11620 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

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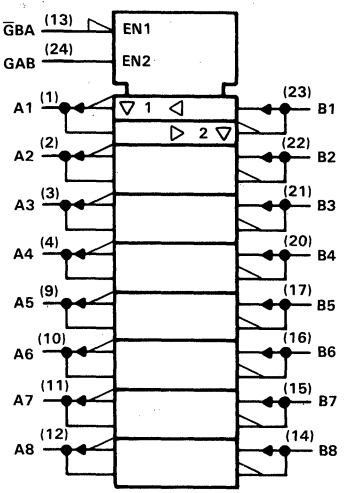
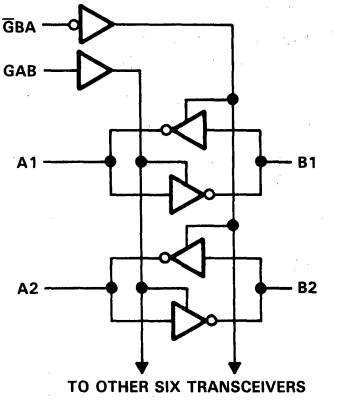
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

			54AC11620			74AC11620			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11620		74AC11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11620		74AC11620		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.3						
t_{PHL}			3.3 ± 0.3 V								
			5 ± 0.5 V		4.8						
t_{PZH}	$\overline{G}$BA	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.5						
t_{PZL}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.1						
t_{PHZ}	$\overline{G}$BA	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						
t_{PLZ}			3.3 ± 0.3 V								
			5 ± 0.5 V		4.2						
t_{PZH}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.9						
t_{PZL}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.6						
t_{PHZ}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.5						
t_{PLZ}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.6						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

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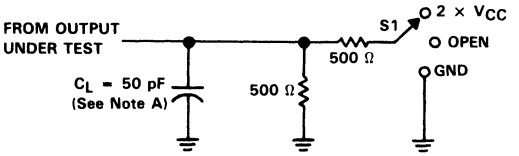
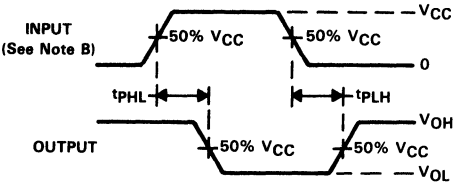
PARAMETER MEASUREMENT INFORMATION

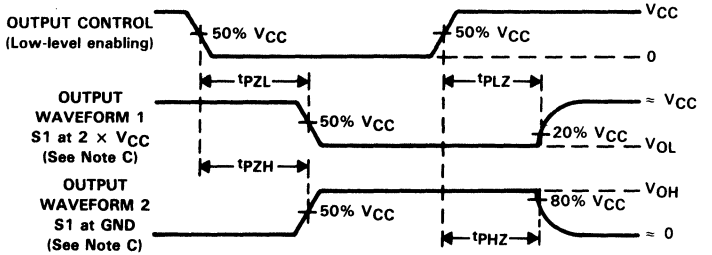


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, JULY 1987

- **Local Bus-Latch Capability**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
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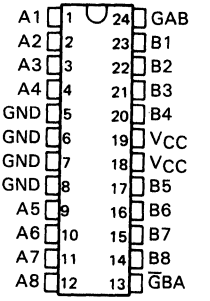
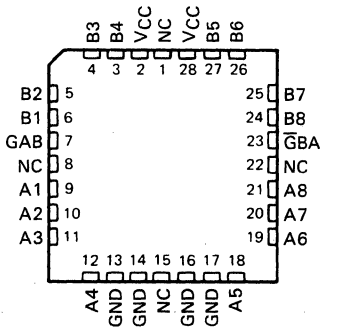
54ACT11620 . . . JT PACKAGE
74ACT11620 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11620 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the ACT11620.

The 54ACT11620 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11620 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

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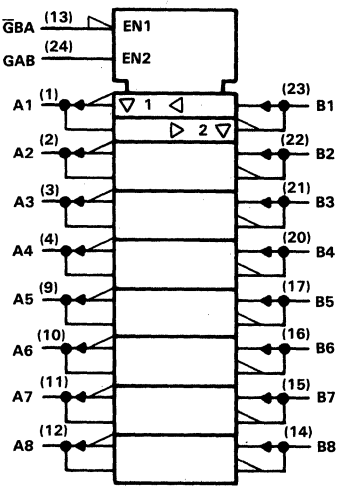
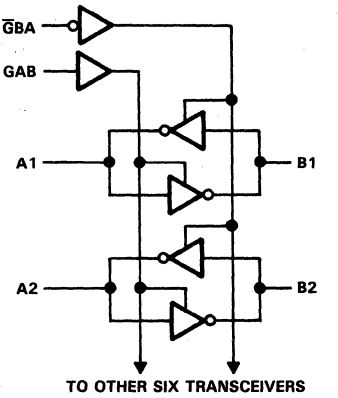
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54ACT11620			74ACT11620			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V	3.15			3.15			V
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V			1.35			1.35	V
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 4.5 V			−24			−24	mA
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 4.5 V			24			24	mA
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11620		74ACT11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11620		74ACT11620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A		5.5						ns
t_{PHL}				5.7						
t_{PZH}	$\overline{G}$BA	A		6.1						ns
t_{PZL}				7.1						
t_{PHZ}	$\overline{G}$BA	A		7.8						ns
t_{PLZ}				7.6						
t_{PZH}	GAB	B		6.4						ns
t_{PZL}				7.8						
t_{PHZ}	GAB	B		7.2						ns
t_{PLZ}				7.1						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

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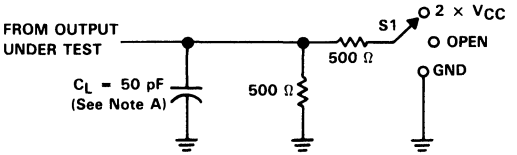
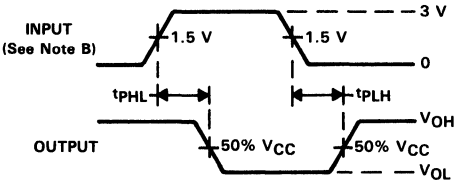
PARAMETER MEASUREMENT INFORMATION

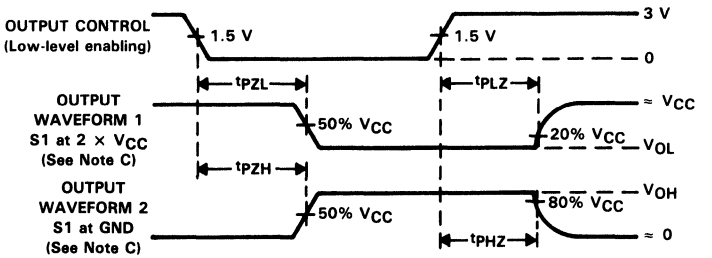


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

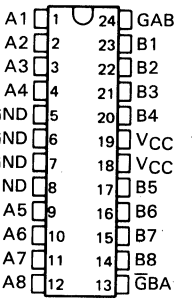
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

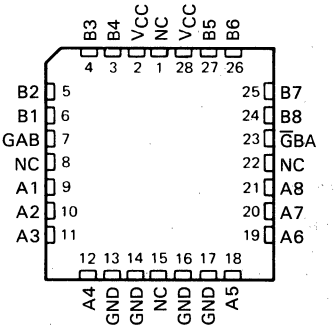
D2957, JULY 1987

- **Local Bus-Latch Capability**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11623 . . . JT PACKAGE
74AC11623 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11623 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the AC11623.

The 54AC11623 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11623 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

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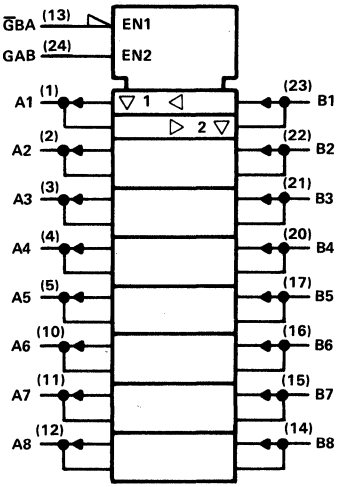
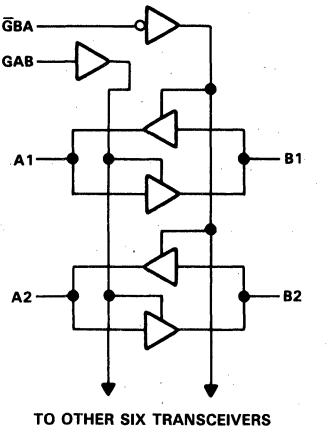
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC} +0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			54AC11623			74AC11623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11623		74AC11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

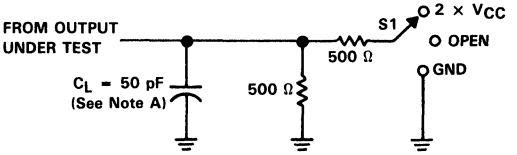
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C MIN	TYP	MAX	54AC11623 MIN	MAX	74AC11623 MIN	MAX	UNIT
t_{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.1						
t_{PHL}			3.3 ± 0.3 V								
			5 ± 0.5 V		4.5						
t_{PZH}	$\overline{G}BA$	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.5						
t_{PZL}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.1						
t_{PHZ}	$\overline{G}BA$	A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.6						
t_{PLZ}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.7						
t_{PZH}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.9						
t_{PZL}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.6						
t_{PHZ}	GAB	B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.5						
t_{PLZ}			3.3 ± 0.3 V								
			5 ± 0.5 V		5.6						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

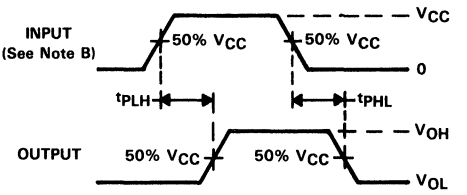
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

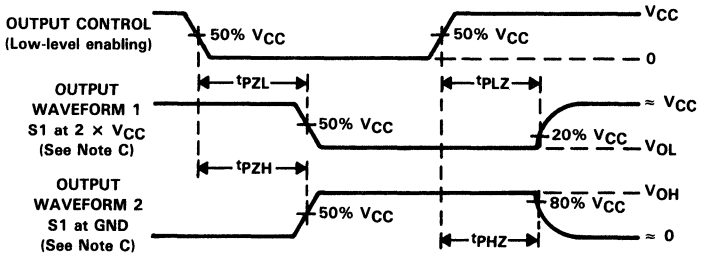


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

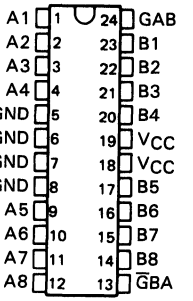
FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

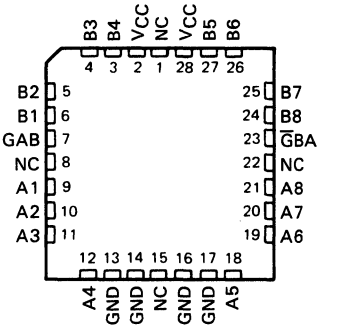
D2957, JULY 1987

- **Local Bus-Latch Capability**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11623 . . . JT PACKAGE
74ACT11623 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11623 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the ACT11623.

The 54ACT11623 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11623 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

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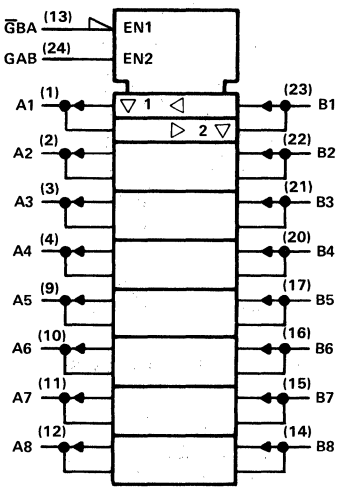
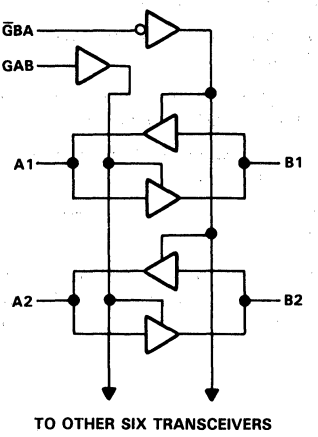
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

			54ACT11623			74ACT11623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V	3.15			3.15			V
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V			1.35			1.35	V
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 4.5 V			−24			−24	mA
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 4.5 V			24			24	mA
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11623		74ACT11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11623		74ACT11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A		5.2						ns
t_{PHL}				5.7						
t_{PZH}	$\overline{G}$BA	A		6						ns
t_{PZL}				7						
t_{PHZ}	$\overline{G}$BA	A		7.8						ns
t_{PLZ}				7.6						
t_{PZH}	GAB	B		6.4						ns
t_{PZL}				7.4						
t_{PHZ}	GAB	B		7.2						ns
t_{PLZ}				7						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

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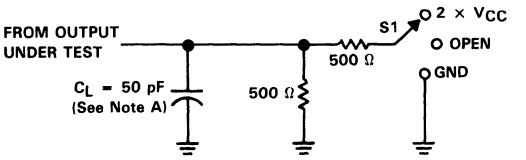
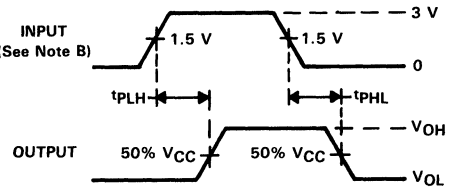
PARAMETER MEASUREMENT INFORMATION

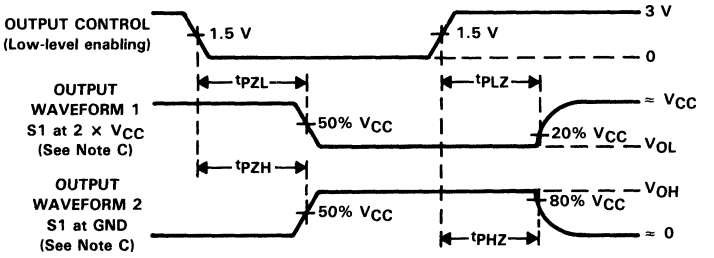


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

D2957, JULY 1987

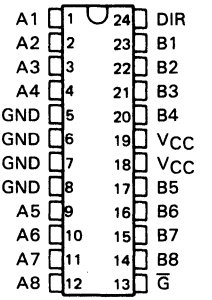
- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

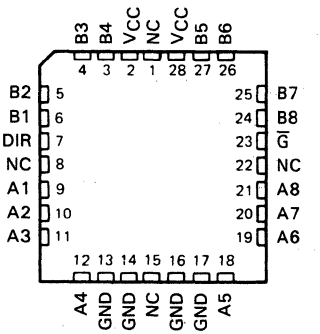
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so the buses are effectively isolated.

The 54AC11640 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11640 is characterized for operation from −40°C to 85°C.

54AC11640 . . . JT PACKAGE
74AC11640 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11640 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

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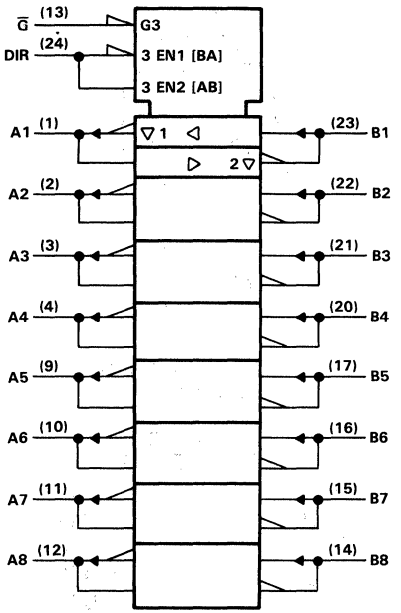
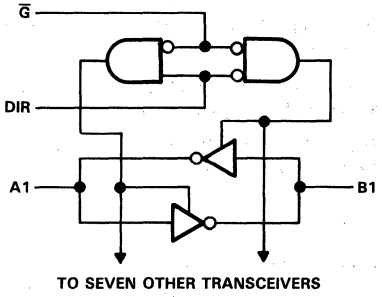
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 6 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11640			74AC11640			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	$\overline{G}$ or DIR	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11640		74AC11640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11640		74AC11640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.9						
t_{PHL}	A or B	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.8						
t_{PZH}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.7						
t_{PZL}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		7.4						
t_{PHZ}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		8.4						
t_{PLZ}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		8						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
	Outputs disabled		12	

TEXAS INSTRUMENTS
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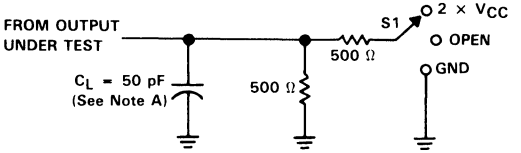
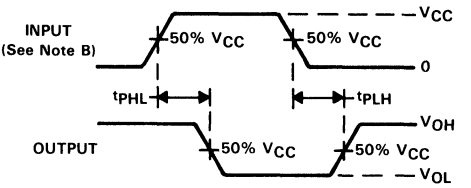
PARAMETER MEASUREMENT INFORMATION

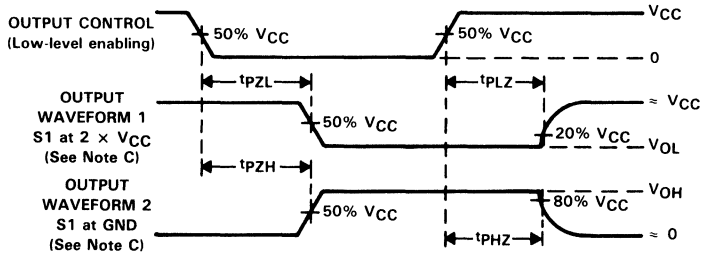


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

D2957, JULY 1987—REVISED SEPTEMBER 1987

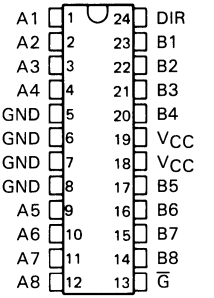
- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

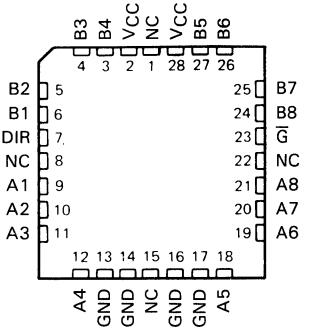
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so the buses are effectively isolated.

The 54ACT11640 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11640 is characterized for operation from −40°C to 85°C.

54ACT11640 . . . JT PACKAGE
74ACT11640 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11640 . . . FK PACKAGE
(TOP VIEW)



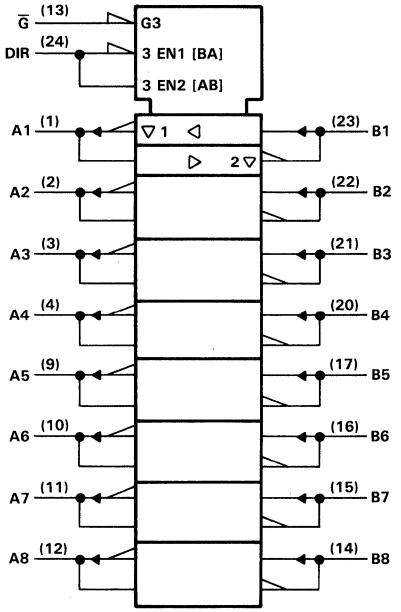
NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

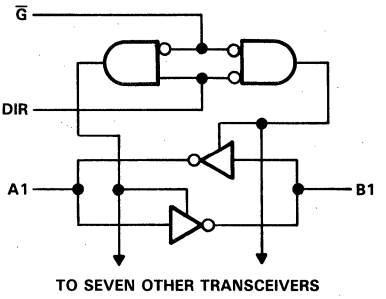
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11640			74ACT11640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11640		74ACT11640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B Ports	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	$\overline{G}$ or DIR	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$\overline{G}$ or DIR	V_I = V_{CC} or GND	5 V		4						pF
C_{io}	A or B Ports	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

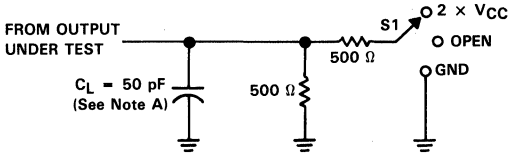
switching characteristics V_{CC} = 5 V ±0.5 V, (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11640		74ACT11640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.3	9.6	1.5	11	1.5	10.5	ns
t_{PHL}			1.5	5.7	8.6	1.5	10	1.5	9.5	
t_{PZH}	$\overline{G}$	A or B	1.5	8.8	12.2	1.5	14.2	1.5	13.4	ns
t_{PZL}			1.5	8.4	12.3	1.5	14.5	1.5	13.6	
t_{PHZ}	$\overline{G}$	A or B	1.5	9.1	12.9	1.5	14.5	1.5	13.9	ns
t_{PLZ}			1.5	9.6	13.1	1.5	15	1.5	14.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

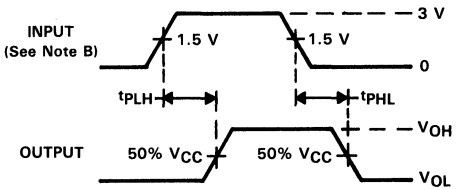
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

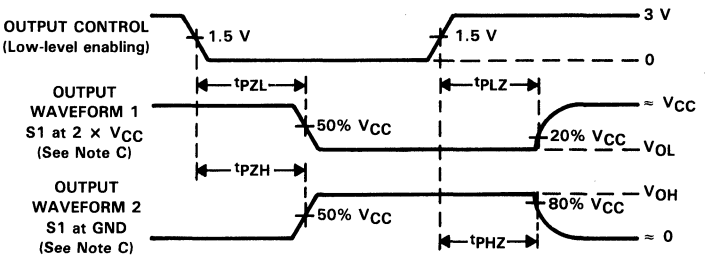


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2957, JULY 1987

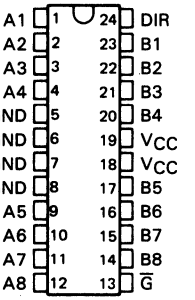
- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

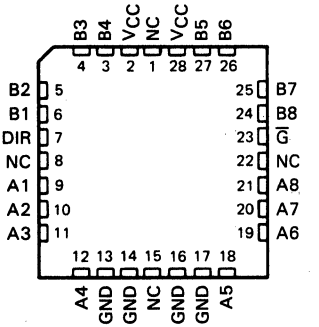
These octal transceivers are designed for asynchronous, two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The 54AC11643 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11643 is characterized for operation from −40°C to 85°C.

54AC11643 . . . JT PACKAGE
74AC11643 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11643 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

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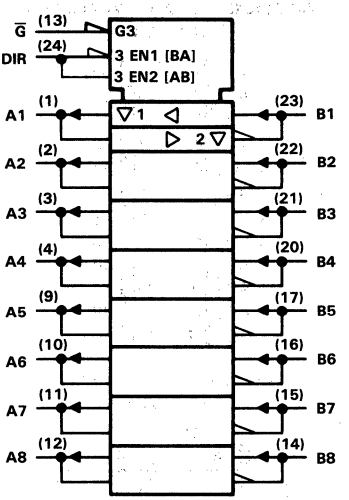
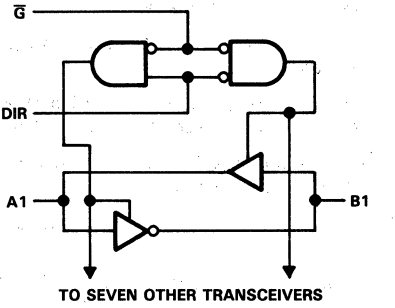
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11643			74AC11643			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	$\overline{G}$ or DIR	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11643		74AC11643		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C MIN	TYP	MAX	54AC11643 MIN	54AC11643 MAX	74AC11643 MIN	74AC11643 MAX	UNIT
t_{PLH}	A or B	B or A	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.3						
t_{PHL}	A or B	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.8						
t_{PZH}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		4.7						
t_{PZL}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		5.4						
t_{PHZ}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.6						
t_{PLZ}	$\overline{G}$	A or B	3.3 ± 0.3 V								ns
			5 ± 0.5 V		6.5						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

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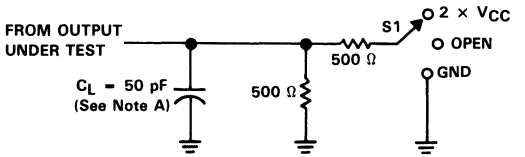
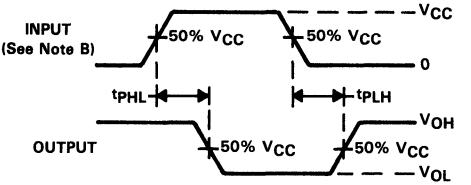
PARAMETER MEASUREMENT INFORMATION

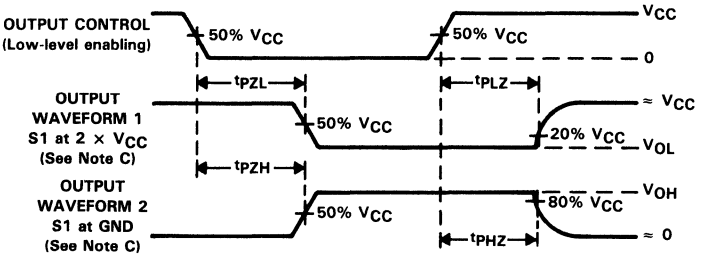


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

2 Advanced CMOS Circuits

D2957, JULY 1987

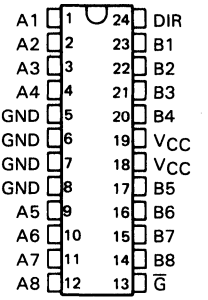
- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **Inputs are TTL-Voltage Compatible**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

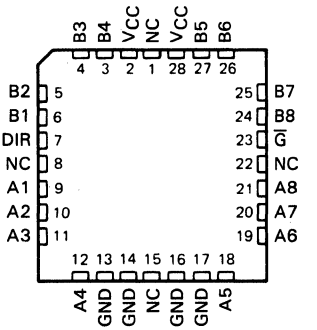
These octal bus transceivers are designed for asynchronous, two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ can be used to disable the device so the buses are effectively isolated.

The 54ACT11643 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11643 is characterized for operation from −40°C to 85°C.

54ACT11643 . . . JT PACKAGE
74ACT11643 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11643 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

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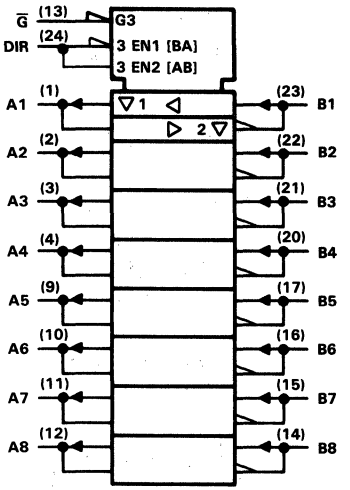
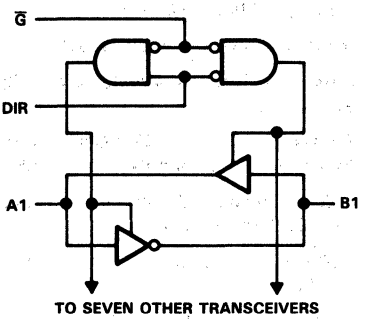
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11643			74ACT11643			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11643		74ACT11643		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

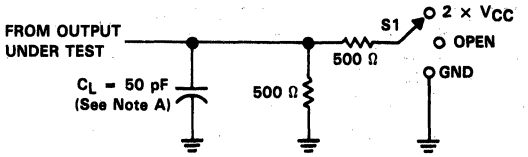
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11643		74ACT11643		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A		5.4						ns
t_{PHL}				5.3						
t_{PZH}	$\overline{G}$	A or B		5.2						ns
t_{PZL}				6						
t_{PHZ}	$\overline{G}$	A or B		6.9						ns
t_{PLZ}				6.8						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

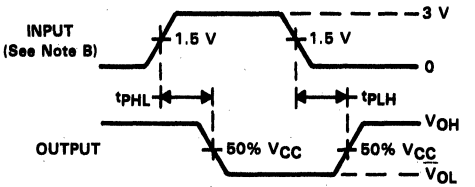
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
	Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

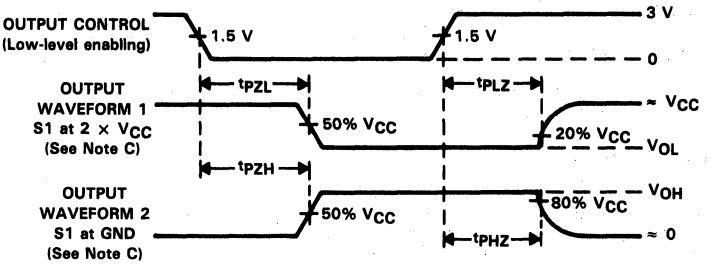


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **New Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
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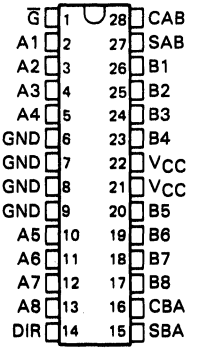
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs**

54AC11646 . . . JD PACKAGE
74AC11646 . . . DW OR NW PACKAGE
(TOP VIEW)



54AC11646 . . . FK PACKAGE
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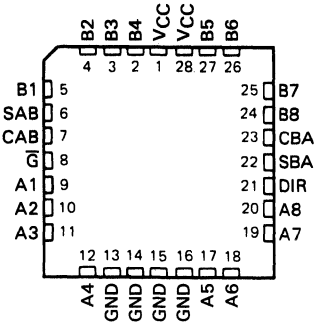

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

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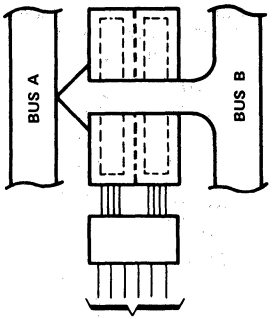
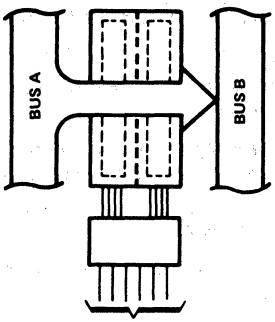


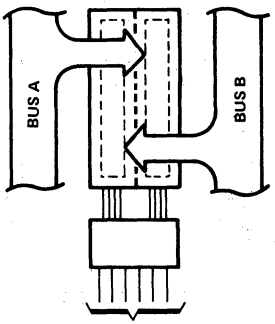
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



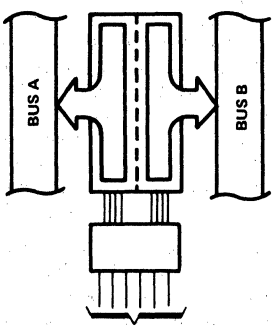
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

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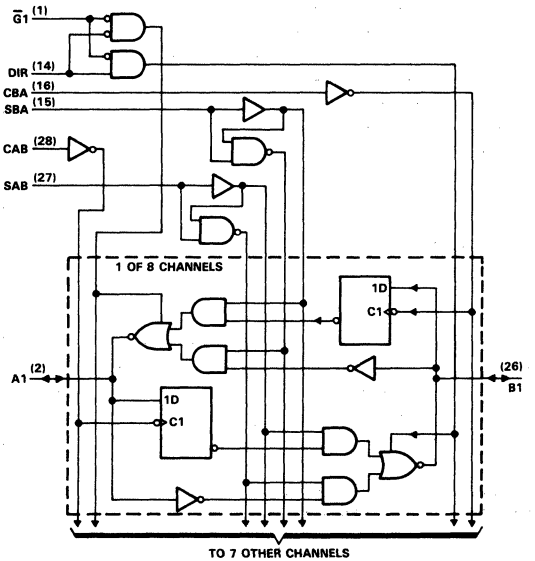
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

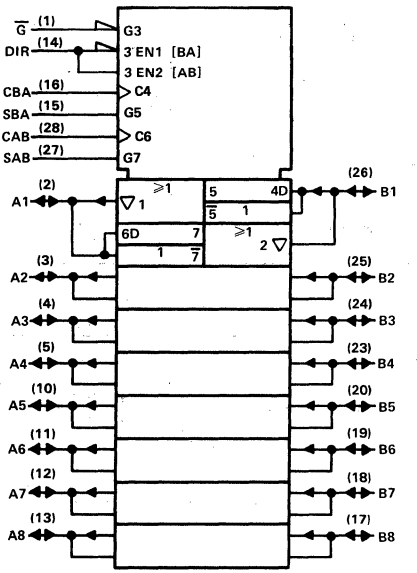
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JD, and NW packages.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JD, and NW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11646			74AC11646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Input voltage		0		V_{CC}	0		V_{CC}	V
dt/dv	Input transition rise or fall rate	Control	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11646		74AC11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

		V_{CC} RANGE	T_A = 25°C		54AC11646		74AC11646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	3.3 ±0.3 V							MHz
		5 +0.5 V							
t_w	Pulse duration, CAB or CBA high or low	3.3 ±0.3 V							ns
		5 ±0.5 V							
t_{su}	Setup time, A before CAB↑ or B before CBA↑	3.3 ±0.3 V							ns
		5 ±0.5 V							
t_h	Hold time, A after CAB↑ or B after CBA↑	3.3 ±0.3 V							ns
		5 ±0.5 V							

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C MIN	TYP	MAX	54AC11646 MIN	54AC11646 MAX	74AC11646 MIN	74AC11646 MAX	UNIT
f_{max}			3.3 ±0.3 V								MHz
			5 ±0.5 V								
t_{PLH}	A or B	B or A	3.3 ±0.3 V								ns
			5 ±0.5 V		4.8						
t_{PHL}			3.3 ±0.3 V								
			5 ±0.5 V		6						
t_{PZH}	$\overline{G}$	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		6.1						
t_{PZL}			3.3 ±0.3 V								
			5 ±0.5 V		8.5						
t_{PHZ}	$\overline{G}$	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		5.4						
t_{PLZ}			3.3 ±0.3 V								
			5 ±0.5 V		5						
t_{PLH}	CBA or CAB	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		7						
t_{PHL}			3.3 ±0.3 V								
			5 ±0.5 V		8.8						
t_{PLH}	SBA or SAB† (A or B high)	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		5.6						
t_{PHL}			3.3 ±0.3 V								
			5 ±0.5 V		6.9						
t_{PLH}	SBA or SAB† (A or B low)	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		5.6						
t_{PHL}			3.3 ±0.3 V								
			5 ±0.5 V		6.9						
t_{PZH}	DIR	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		6.4						
t_{PZL}			3.3 ±0.3 V								
			5 ±0.5 V		8.4						
t_{PHZ}	DIR	A or B	3.3 ±0.3 V								ns
			5 ±0.5 V		2.7						
t_{PLZ}			3.3 ±0.3 V								
			5 ±0.5 V		3.2						

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
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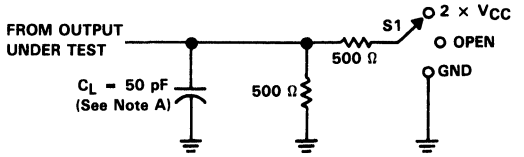
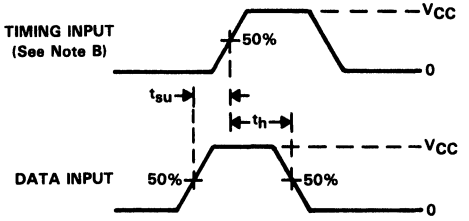
PARAMETER MEASUREMENT INFORMATION

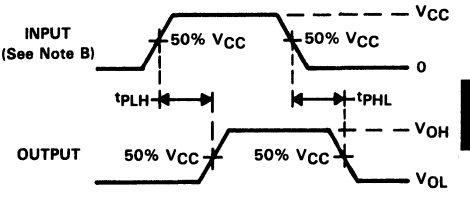


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



SETUP AND HOLD TIMES



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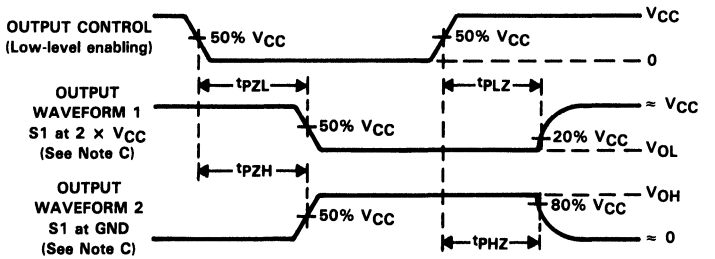

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2 Advanced CMOS Circuits

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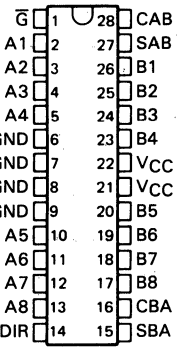
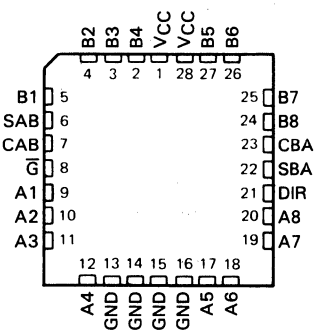


54ACT11646 . . . FK PACKAGE
(TOP VIEW)



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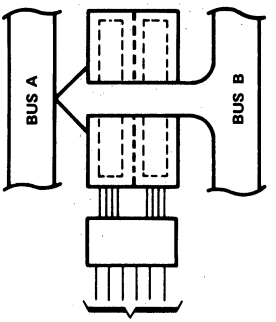
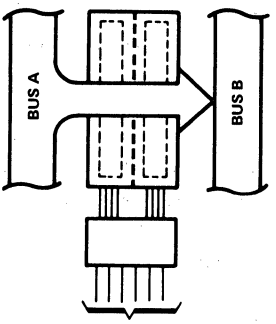


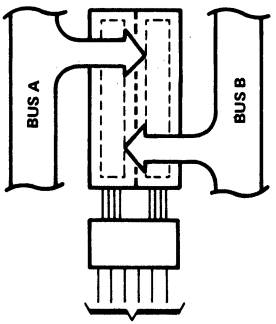
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



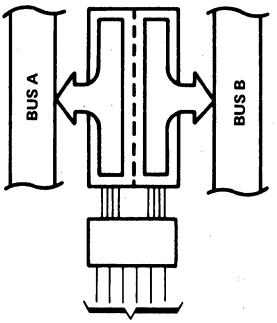
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

TRANSFER
STORED DATA
TO A OR B

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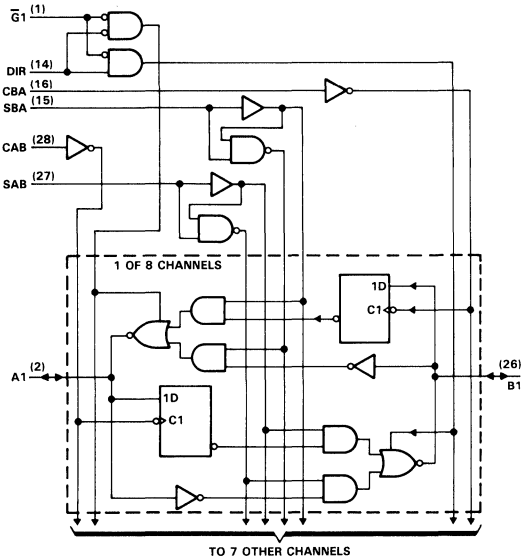
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

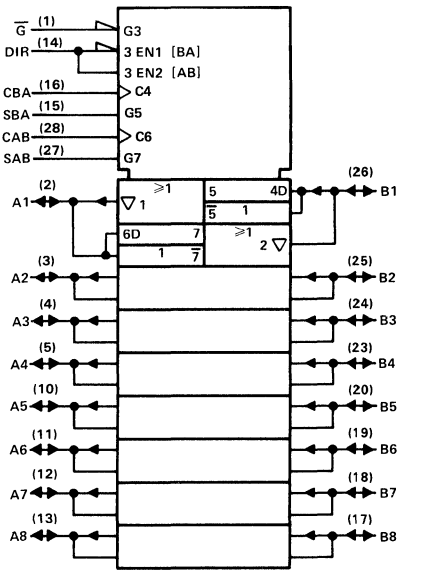
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JD, and NT packages.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JD, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . −0.5 V to 6 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
dt/dv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11646		74ACT11646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements, V_{CC} = 5 ± 0.5 V (see Figure 1)

		T_A = 25°C		54ACT11646		74ACT11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, CAB or CBA high or low							ns
t_{su}	Setup time, A before CLK↑ or B before CBA↑							ns
t_h	Hold time, A after CAB↑ or B after CBA↑							ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54ACT11646		74ACT11646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			5.0 ±0.5 V								MHz
t_{PLH}	A or B	B or A	5.0 ±0.5 V		5.1						ns
t_{PHL}					7.2						
t_{PZH}	$\overline{G}$	A or B	5.0 ±0.5 V		6.2						ns
t_{PZL}					7.2						
t_{PHZ}	$\overline{G}$	A or B	5.0 ±0.5 V		6.5						ns
t_{PLZ}					7.2						
t_{PLH}	CBA or CAB	A or B	5.0 ±0.5 V		6.4						ns
t_{PHL}					9						
t_{PZH}	DIR	A or B	5.0 ±0.5 V		7						ns
t_{PZL}					8						
t_{PHZ}	DIR	A or B	5.0 ±0.5 V		6.6						ns
t_{PLZ}					7.3						
t_{PLH}	SBA OR SAB (A or B high)	A or B	5.0 ±0.5 V		6.1						ns
t_{PHL}					8.3						
t_{PLH}	SBA or SAB (A or B low)	A or B	5.0 ±0.5 V		6.1						ns
t_{PHL}					8.3						

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
	Outputs disabled		12	

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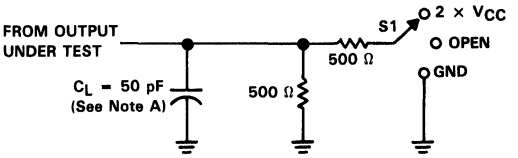
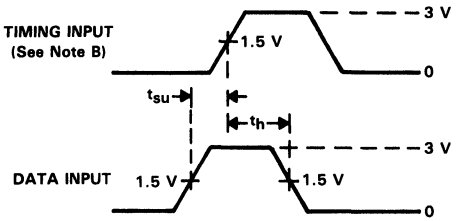
PARAMETER MEASUREMENT INFORMATION

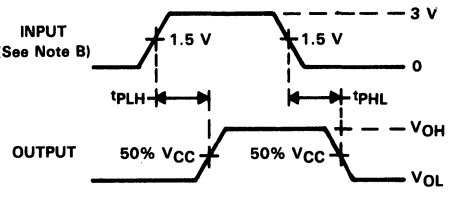


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

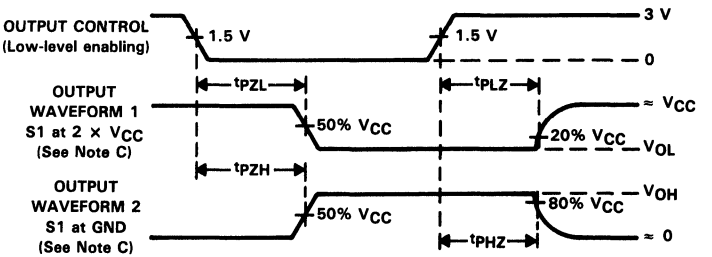
LOAD CIRCUIT



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

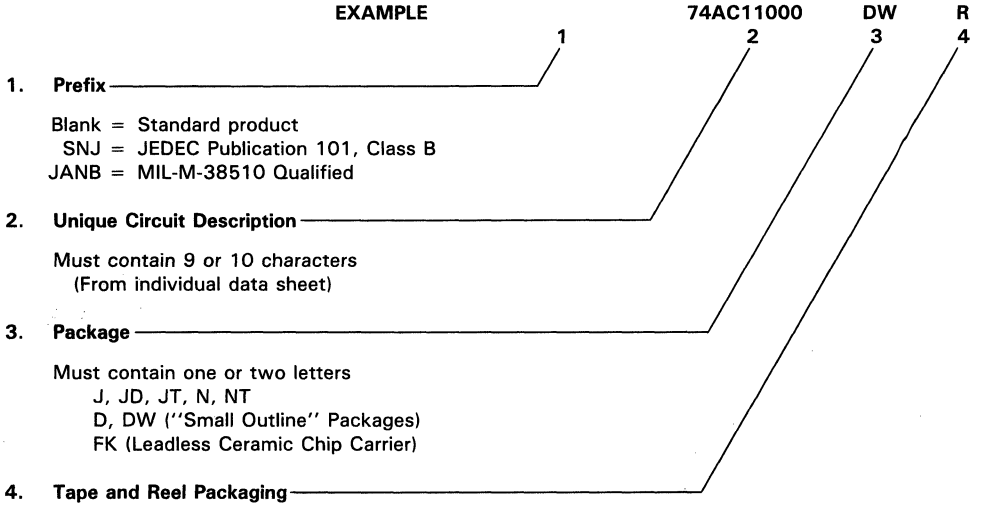
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

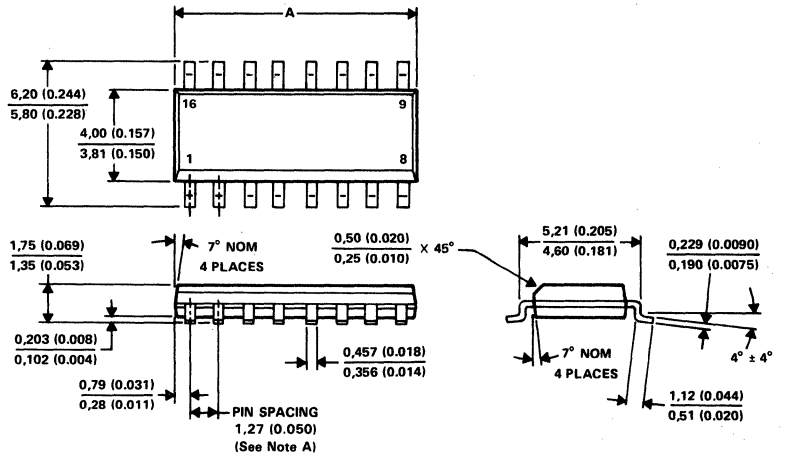
Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

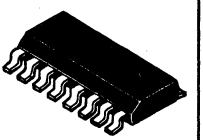


D014 and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D014
D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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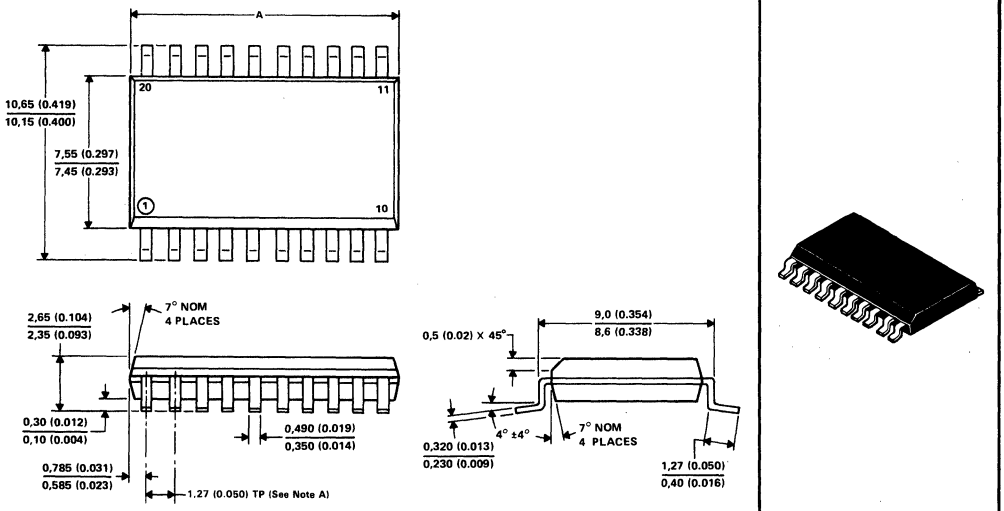
DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW020
DW024
DW028
(20-pin package used for illustration)



DIM \ PINS	16	20	24	28†
A MIN	10,16	12,70	15,29	17,68
	(0.400)	(0.500)	(0.602)	(0.696)
A MAX	10,36	12,90	15,49	17,88
	(0.408)	(0.508)	(0.610)	(0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

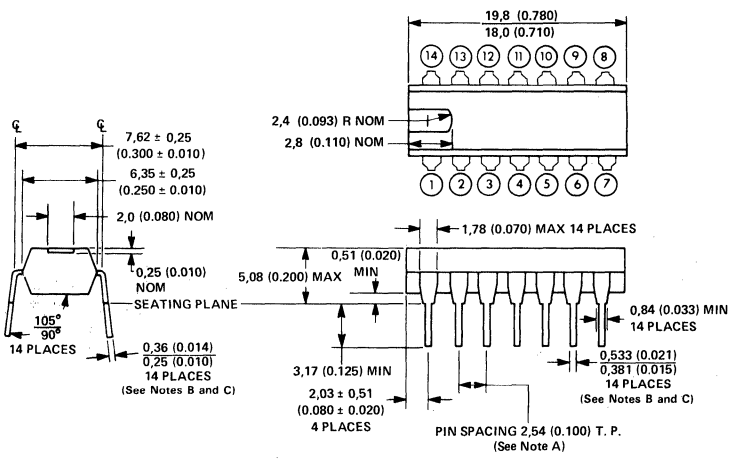
†The 28-pin package drawing is presently classified as Advance Information.

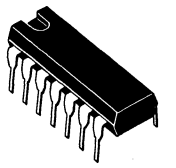
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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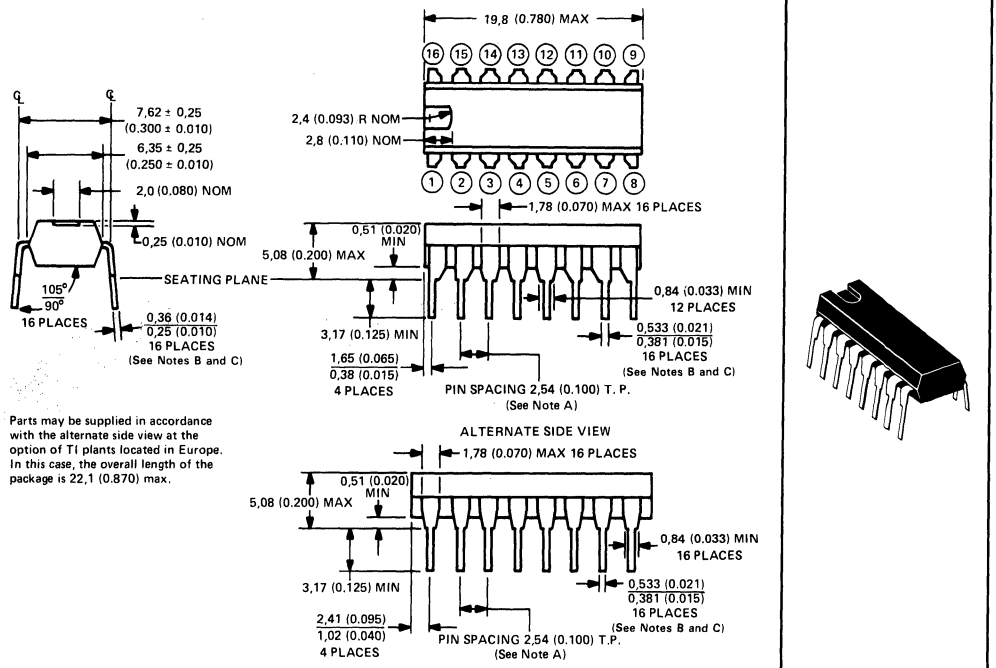
N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N016

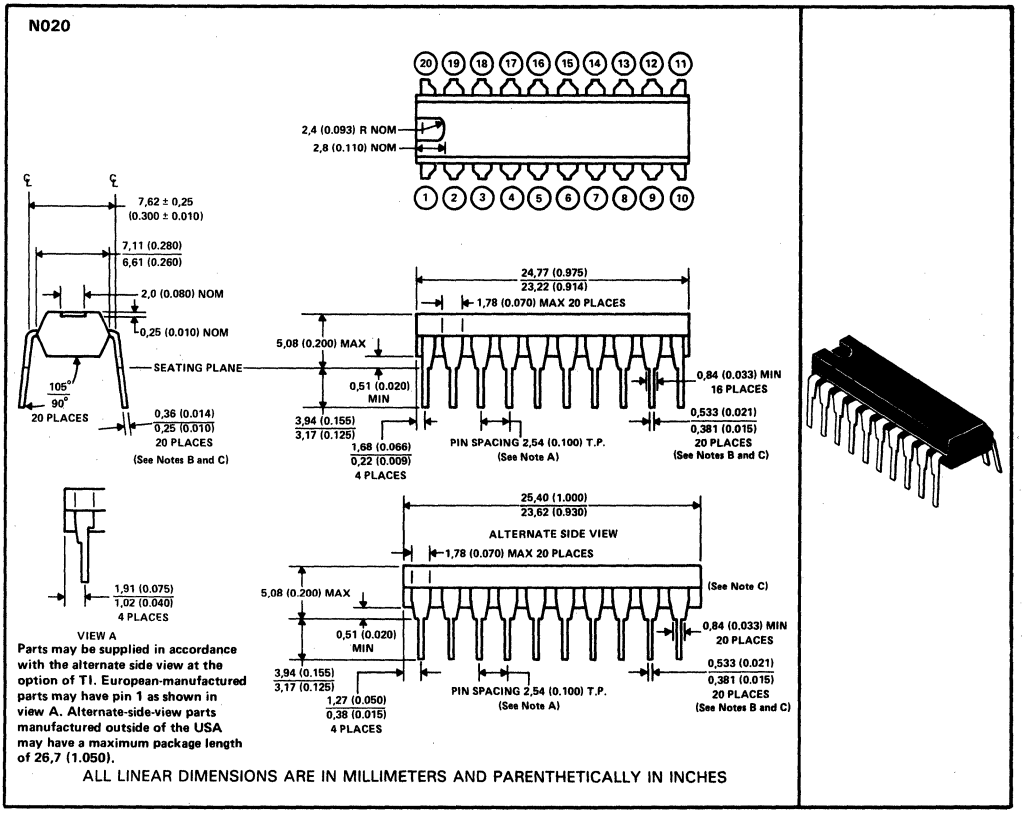


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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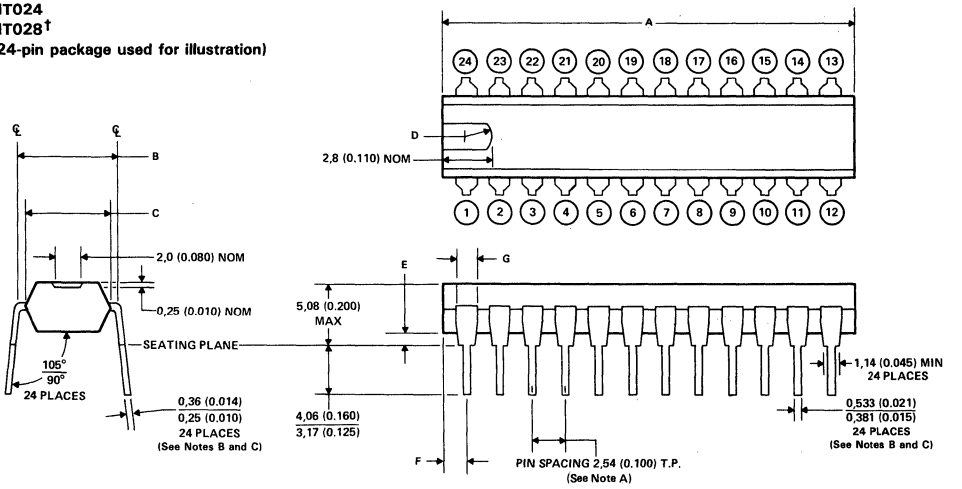
NT024 and NT028† plastic dual-in-line packages

Each of these packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin and 28-pin packages, the letter N is used by itself since the 24-pin and 28-pin packages may be available in more than one row-spacing. For the 24-pin and 28-pin packages, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024
NT028†
(24-pin package used for illustration)



DIM / DESIGNATION	A MIN	A MAX	B	C MAX	D R NOM	E MIN	F MIN	F MAX	G MIN	G MAX
NT024	28,6 (1.125)	31,8 (1.250)	7,62 ± 0,25 (0.300 ± 0.010)	7,1 (0.280)	2,4 (0.093)	0.38 (0.015)	0,71 (0.028)	2,16 (0.085)	1,14 (0.045)	1,78 (0.070)
NT028†	34,0 (1.338)	37,1 (1.462)	7,88 ± 0,25 (0.310 ± 0.010)	6,86 (0.270)	1,02 (0.040)	0,51 (0.020)	0,51 (0.020)	2,03 (0.080)	1,02 (0.040)	1,78 (0.070)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† The 28-pin package drawing is presently classified as Advance Information.

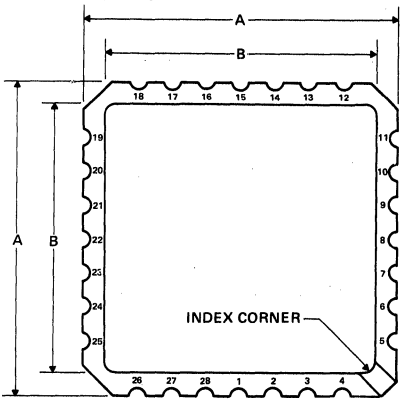
NOTES: A. Each pin centerline is located within 0.25 mm (0.010 inch) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

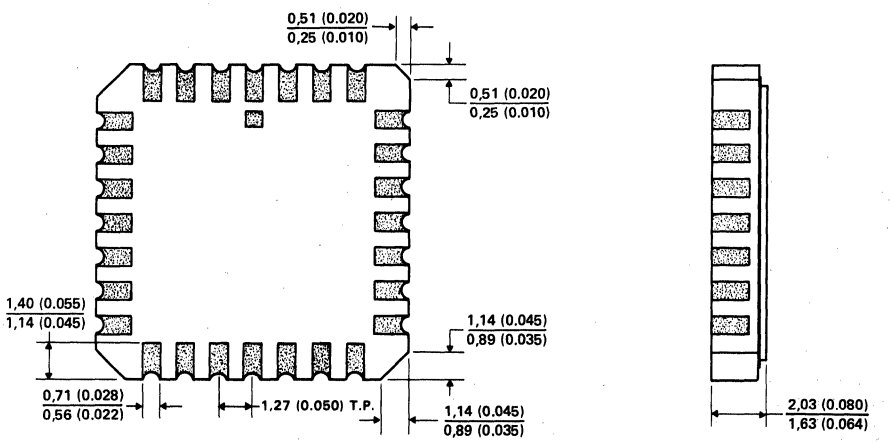
FK020
FK028
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.



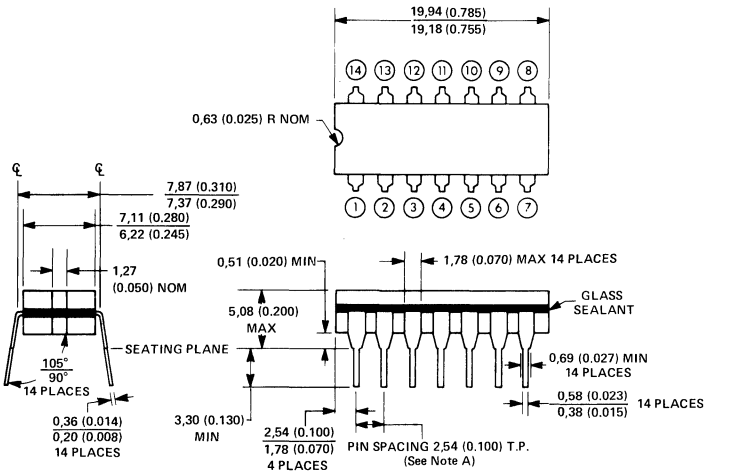
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

J014 ceramic dual-in-line package

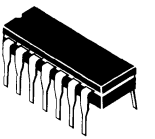
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J014



Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

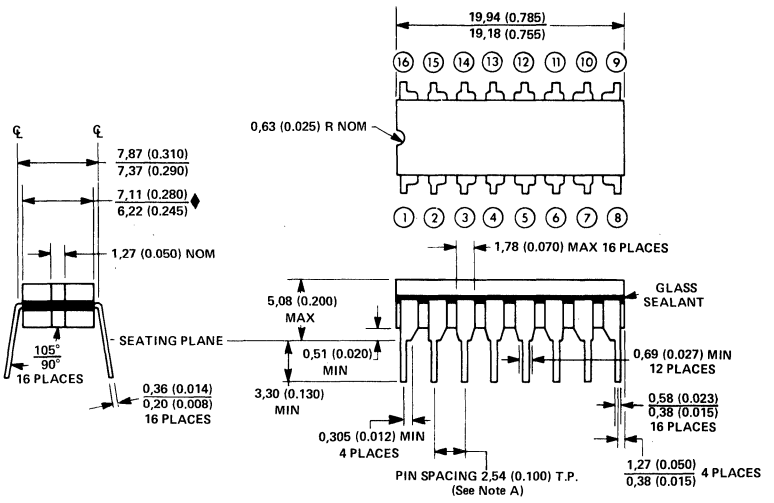


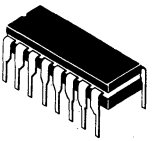
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J016





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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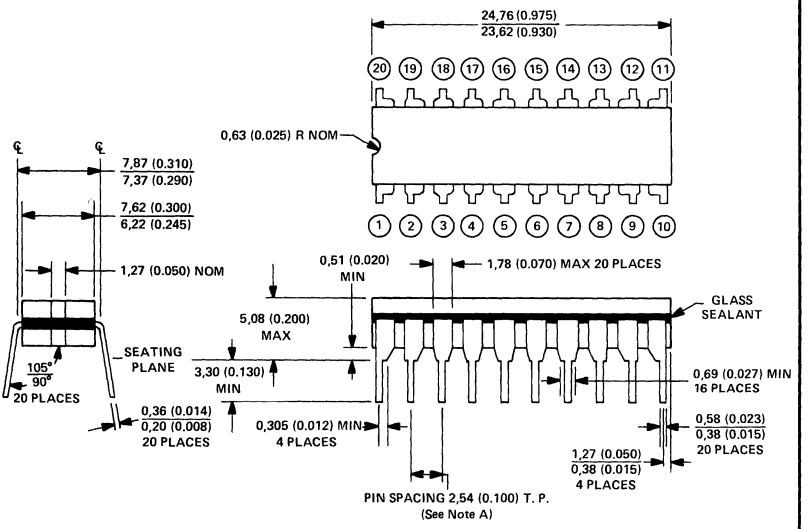
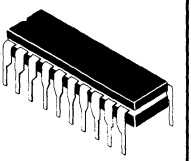
J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J020





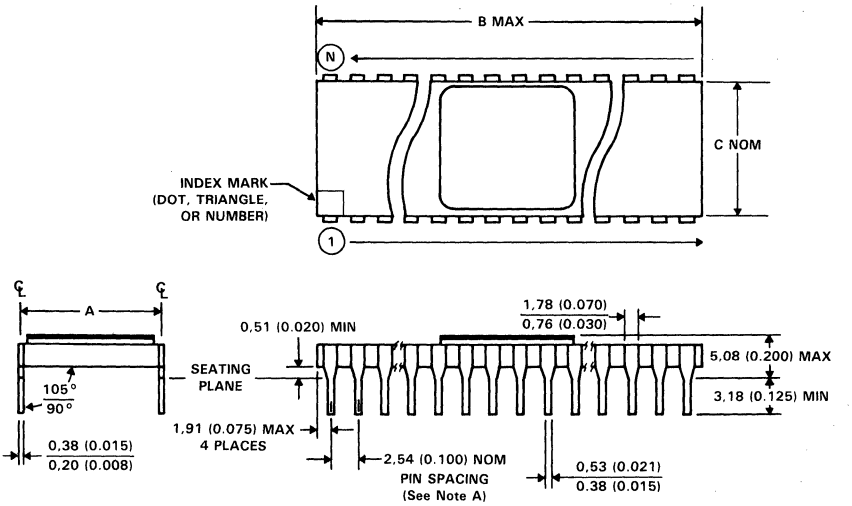
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC—SIDE-BRAZE



DIM \ PINS (N)	24	28
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)
B (MAX)	31,8 (1.250)	36,8 (1,450)
C (NOM)	15,0 (0.590)	15,0 (0.590)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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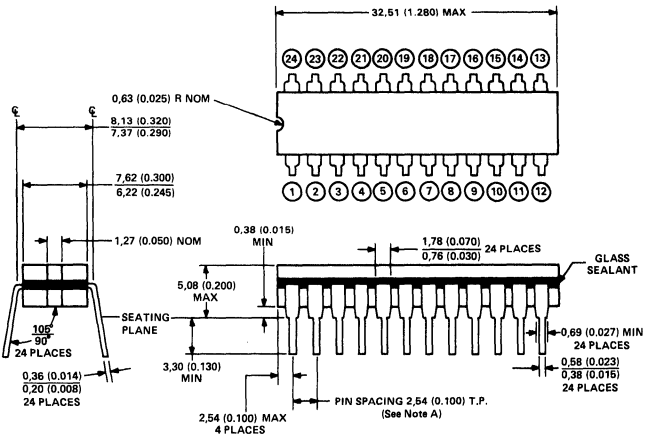
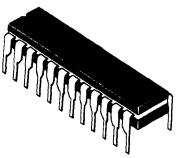
JT024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-diped") pins require no additional cleaning or processing when used in soldered assembly.

JT024





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

NOTES

NOTES

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